

Structure (2A)

- Configuration

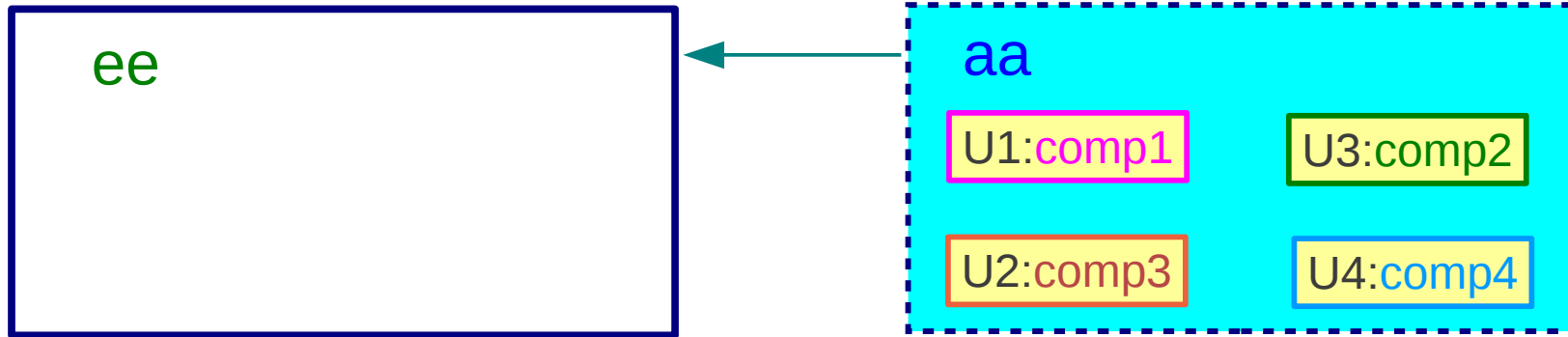
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Structural Hierarchy



Component Declaration

```
component comp1 is
  port ( );
end comp1;
component comp2 is
  port ( );
end comp2;
component comp3 is
  port ( );
end comp3;
component comp4 is
  port ( );
end comp4;
```

architecture aa of ee is

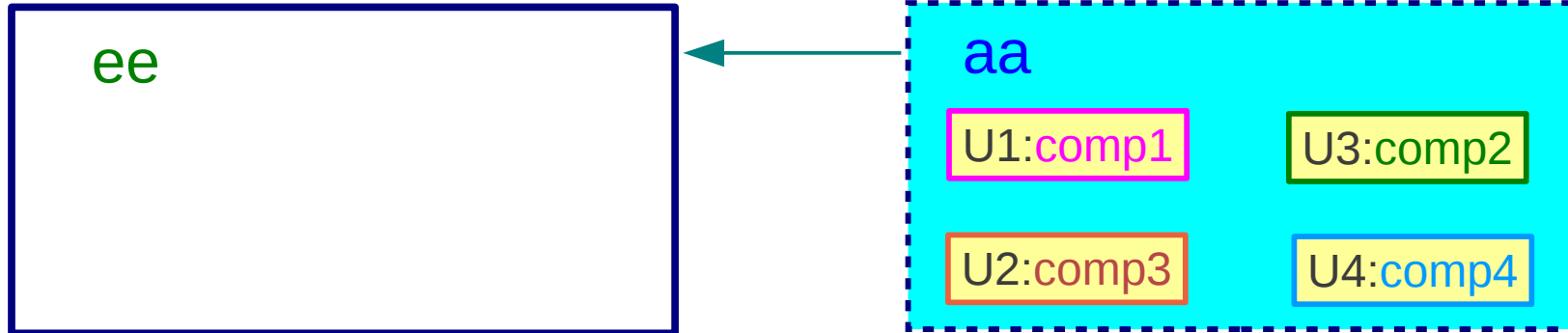
begin

Component Instantiation

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

end aa;

Which Entity - Architecture pairs?



- *Default Binding*
- *Configuration Specification*
- *Configuration Declaration*
 - *Default Configuration*
 - *Component Configuration*
 - *entity-architecture configuration*
 - *low level configuration*
 - *Block Configuration*

architecture **aa** of **ee** is



begin

Component Instantiation

```
U1: comp1 port map ( );  
U2: comp2 port map ( );  
U3: comp3 port map ( );  
U4: comp4 port map ( );
```

end aa;

Default Binding

```
entity comp1 is
  port ( );
end comp1;
```

```
entity comp2 is
  port ( );
end comp2;
```

```
entity comp3 is
  port ( );
end comp3;
```

```
entity comp4 is
  port ( );
end comp4;
```

```
architecture bhv of comp1 is
  ...
end comp1;
```

```
architecture bhv of comp2 is
  ...
end comp2;
```

```
architecture bhv of comp3 is
  ...
end comp3;
```

```
architecture bhv of comp4 is
  ...
end comp4;
```

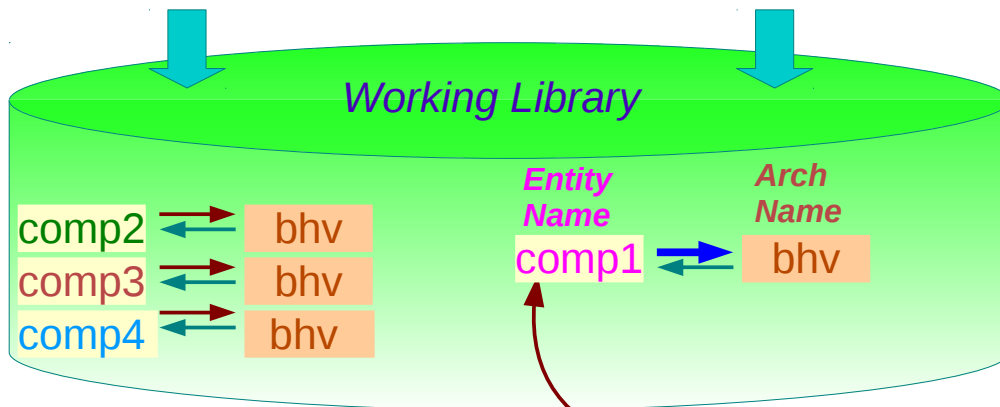
```
architecture aa of ee is
```

```
begin
```

Component Name

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

```
end aa;
```



Component - Entity Binding

Component Name = Entity Name

Entity - Architecture Binding

Last compiled Architecture

Configuration Specification (1)

Component Declaration

```
component comp1 is
  port ( );
end comp1;

component comp2 is
  port ( );
end comp2;

component comp3 is
  port ( );
end comp3;

component comp4 is
  port ( );
end comp4;
```

Configuration Specification :
For each component instance,
Specify the selection of

- Entity declaration and
- Architecture body.

architecture aa of ee is



begin

Component Instantiation

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

end aa;

Configuration Specification (2)

Component Declaration

```
component comp1 is
  port ( );
end comp1;

component comp2 is
  port ( );
end comp2;

component comp3 is
  port ( );
end comp3;

component comp4 is
  port ( );
end comp4;
```

architecture aa of ee is

begin

Component Instantiation

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

Component Name

end aa;

Library Name Entity Name Arch Name

```
for U1: comp1 use entity work.comp1(bhv);
for U2: comp2 use entity work.comp2(bhv);
for U3: comp3 use entity work.comp3(bhv);
for U4: comp4 use entity work.comp4(bhv);
```

Configuration Specification :
For each component instance,
Specify the selection of

- Entity declaration and
- Architecture body.

Configuration Declaration (1)

Component Declaration

```
component comp1 is
  port ( );
end comp1;

component comp2 is
  port ( );
end comp2;

component comp3 is
  port ( );
end comp3;

component comp4 is
  port ( );
end comp4;
```

architecture aa of ee is

begin

Component Instantiation

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

end aa;

A Configuration :

A Design Unit

*compiled separately
stored in a library*

Recompilation

*of the entire design
can be avoided*

configuration conf3 of ee is

for aa

for U1: comp1 * * * ;

for U2: comp2 * * * ;

for U3: comp3 * * * ;

for U4: comp4 * * * ;

end for;

end conf1;

Configuration Declaration (2)

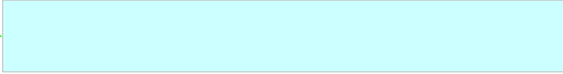
Component Declaration

```
component comp1 is
  port ( );
end comp1;

component comp2 is
  port ( );
end comp2;

component comp3 is
  port ( );
end comp3;

component comp4 is
  port ( );
end comp4;
```

```
architecture aa of ee is
  
begin
  Component Instantiation
  U1: comp1 port map ( );
  U2: comp2 port map ( );
  U3: comp3 port map ( );
  U4: comp4 port map ( );
end aa;
```

- *Default Configuration*
- *Component Configuration*
 - *entity-architecture configuration*
 - *low level configuration*
- *Block Configuration*

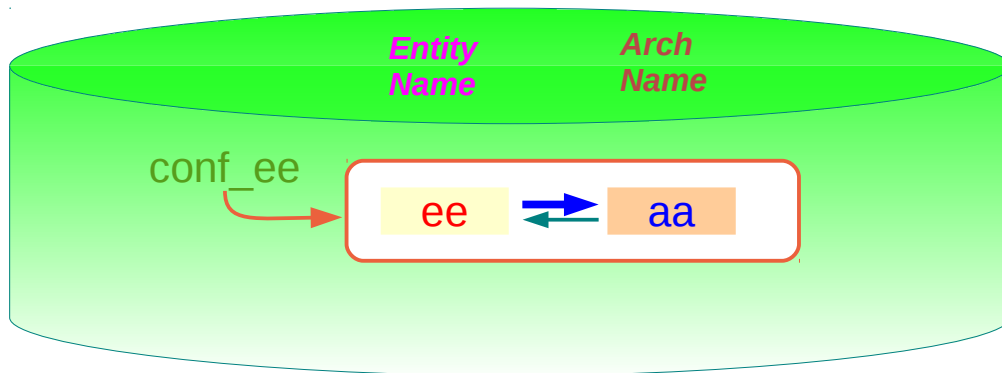
The configuration of an entity is
For a specific architecture specify

- **Component Configuration**
- **Block Configuration**

Default Configuration (1)

```
entity ee is
  port ( );
end ee;
```

default configuration of the entity ee



```
architecture aa of ee is
```

```
begin
```

Component Name

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

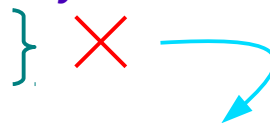
```
end aa;
```

```
configuration conf_ee of ee is
  for aa
  end for;
end conf_ee;
```

The configuration of an entity is

For a specific architecture specify

- *Component Configuration*
- *Block Configuration*



*Default Configuration:
No specific configuration
for any block or component*



Default Binding

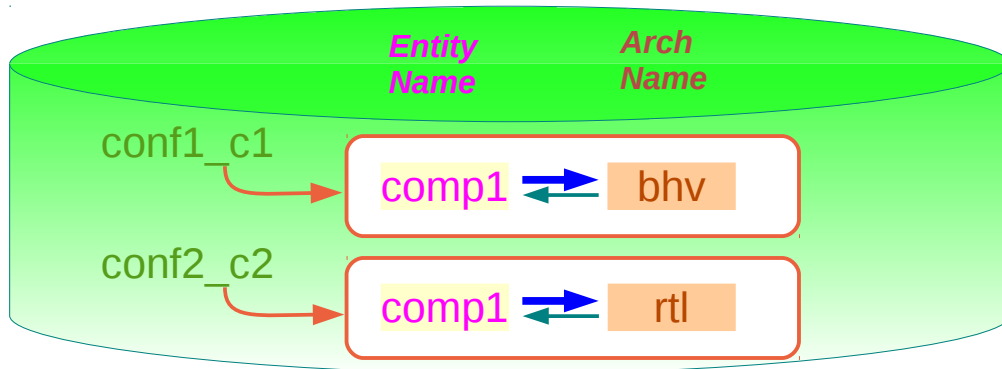
Default Configuration (2)

```
entity comp1 is
  port ( );
end comp1;
```

default configurations
of the entity comp1

```
architecture bhv of comp1 is
  ...
end comp1;
```

```
architecture rtl of comp1 is
  ...
end comp1;
```



```
architecture aa of ee is

begin
  Component
  Name
  U1: comp1 port map ( );
  U2: comp2 port map ( );
  U3: comp3 port map ( );
  U4: comp4 port map ( );

end aa;
```

```
configuration conf1_c1 of comp1 is
  for bhv
  end for;
end conf1;
```

```
configuration conf2_c1 of comp1 is
  for rtl
  end for;
end conf2;
```

The configuration of an entity is

For a specific architecture specify

- Component Configuration
- Block Configuration



Default Configuration:
No specific configuration
for any block or component

Default Configuration (3)

```
entity comp1 is
  port ( );
end comp1;

entity comp2 is
  port ( );
end comp2;

entity comp3 is
  port ( );
end comp3;

entity comp4 is
  port ( );
end comp4;
```

```
architecture bhv of comp1 is
  ...
end comp1;

architecture bhv of comp2 is
  ...
end comp2;

architecture bhv of comp3 is
  ...
end comp3;

architecture bhv of comp4 is
  ...
end comp4;
```

```
architecture aa of ee is

begin
  Component Name
  U1: comp1 port map ( );
  U2: comp2 port map ( );
  U3: comp3 port map ( );
  U4: comp4 port map ( );

end aa;
```

No Component Configuration
No Block Configuration

Use Default Binding

| Entity Name | Arch Name |
|-------------|-----------|
|-------------|-----------|



```
configuration conf1_c1 of comp1 is
  for bhv
  end for;
end conf1;
```

```
configuration conf2_c1 of comp1 is
  for rtl
  end for;
end conf2;
```

Component Configuration

Entity-Arch Configuration

```
configuration conf3 of ee is
  for aa
    for U1: comp1 use entity work.comp1(bhv); end for;
    for U2: comp2 use entity work.comp2(bhv); end for;
    for U3: comp3 use entity work.comp3(bhv); end for;
    for U4: comp4 use entity work.comp4(bhv); end for;
  end for;
end conf1;
```

Library Name Entity Name Arch Name

↓ ↓ ↓

- Default Configuration
- Component Configuration
 - entity-architecture configuration
 - low level configuration
- Block Configuration

Low Level Configuration

```
configuration conf4 of ee is
  for aa
    for U1: comp1 use configuration work.conf_c1; end for;
    for U2: comp2 use configuration work.conf_c2; end for;
    for U3: comp3 use configuration work.conf_c3; end for;
    for U4: comp4 use configuration work.conf_c4; end for;
  end for;
end conf1;
```

Library Name Conf Name

↓ ↓

Entity – Architecture Configuration

Component Declaration

```
component comp1 is
  port ( );
end comp1;

component comp2 is
  port ( );
end comp2;

component comp3 is
  port ( );
end comp3;

component comp4 is
  port ( );
end comp4;
```

architecture aa of ee is

begin

Component Instantiation

```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

end aa;

configuration conf_ea of ee is

for aa

```
for U1: comp1 use entity work.comp1(bhv); end for;
for U2: comp2 use entity work.comp2(bhv); end for;
for U3: comp3 use entity work.comp3(bhv); end for;
for U4: comp4 use entity work.comp4(bhv); end for;
```

end for;

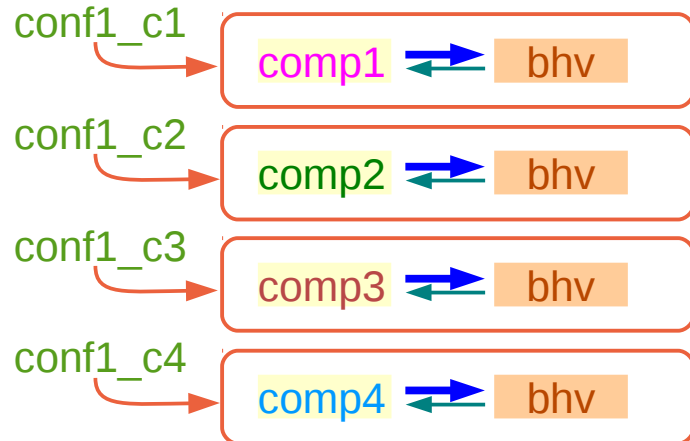
end conf_ea;

| Library Name | Entity Name | Arch Name |
|--------------|-------------|-----------|
|--------------|-------------|-----------|

Low Level Configuration (1)

Component Declaration

```
component comp1 is  
  port ( );  
end comp1;
```



```
architecture aa of ee is
```

```
begin
```

Component Instantiation

```
U1: comp1 port map ( );  
U2: comp2 port map ( );  
U3: comp3 port map ( );  
U4: comp4 port map ( );
```

```
end aa;
```

```
configuration conf_ll of ee is
```

```
  for aa
```

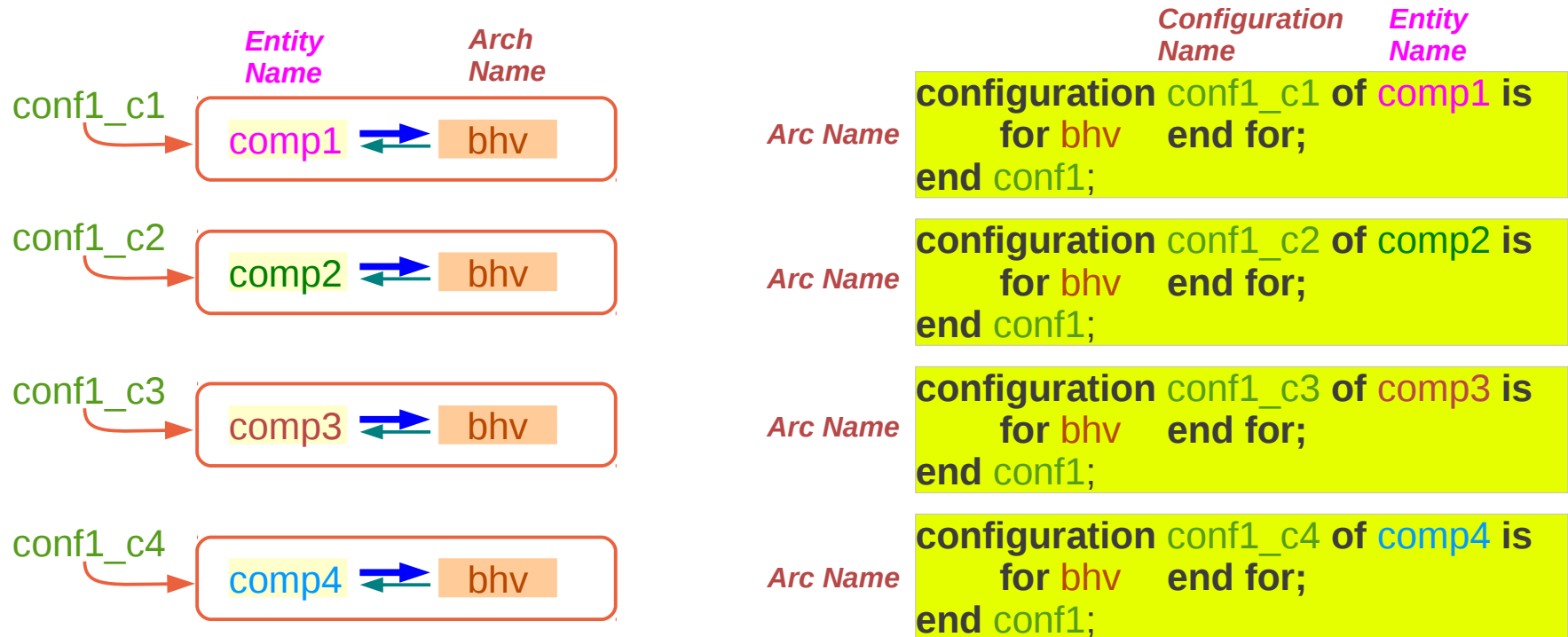
```
    for U1: comp1 use configuration work.conf1_c1; end for;  
    for U2: comp2 use configuration work.conf1_c2; end for;  
    for U3: comp3 use configuration work.conf1_c3; end for;  
    for U4: comp4 use configuration work.conf1_c4; end for;
```

```
  end for;
```

```
end conf_ll;
```

| Library Name | Configuration Name |
|--------------|--------------------|
|--------------|--------------------|

Low Level Configuration (2)

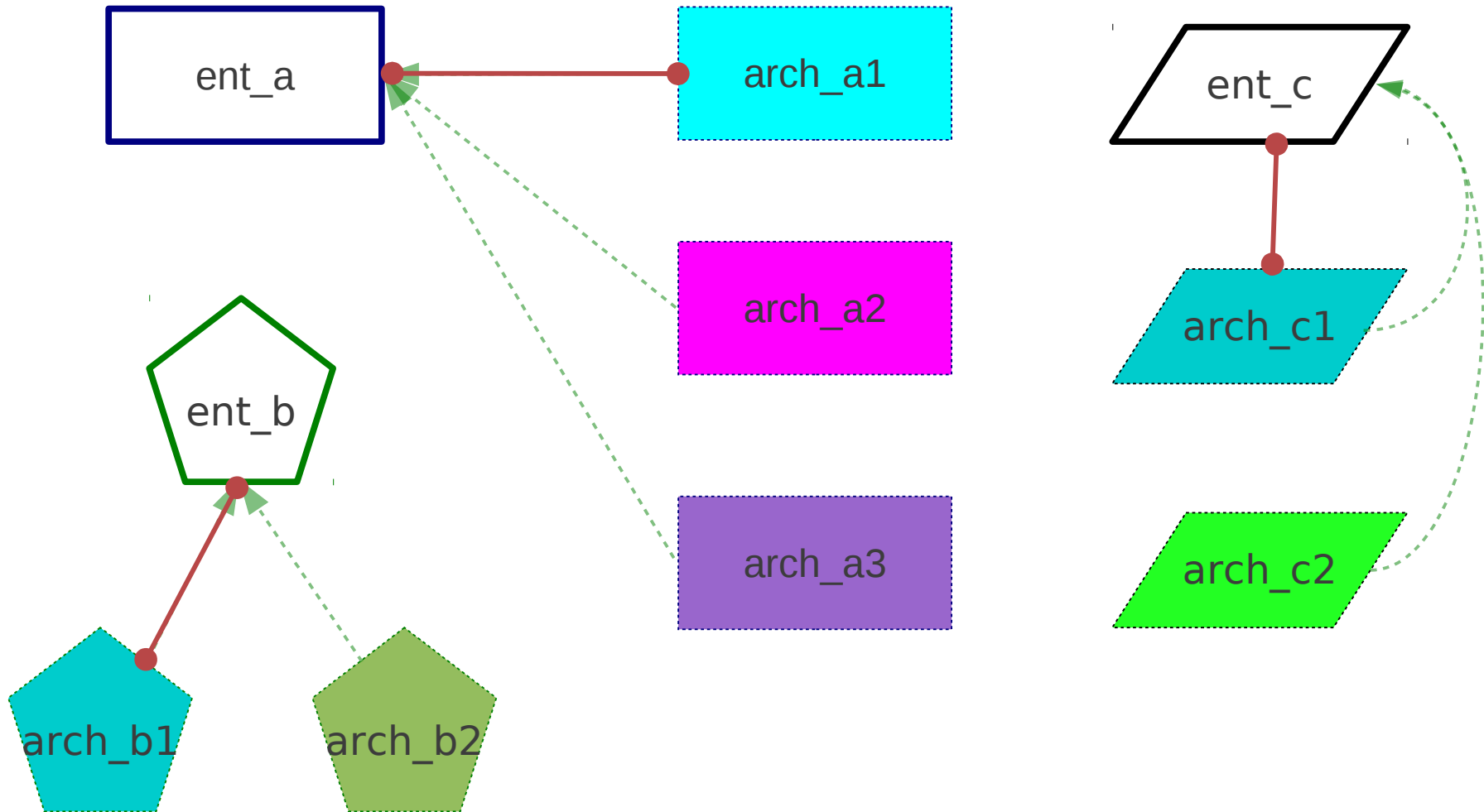


```

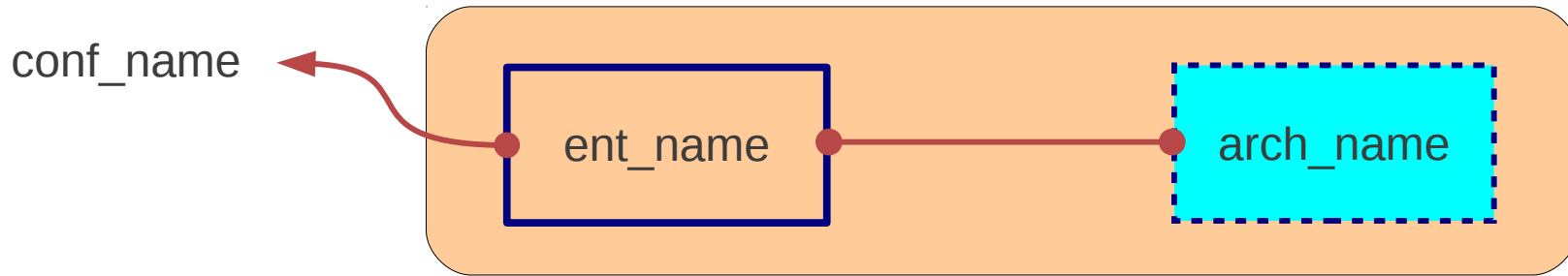
configuration conf_ll of ee is
  for aa
    for U1: comp1 use configuration work.conf1_c1; end for;
    for U2: comp2 use configuration work.conf1_c2; end for;
    for U3: comp3 use configuration work.conf1_c3; end for;
    for U4: comp4 use configuration work.conf1_c4; end for;
  end for;
end conf_ll;
    
```


Sequential Assignment (1)

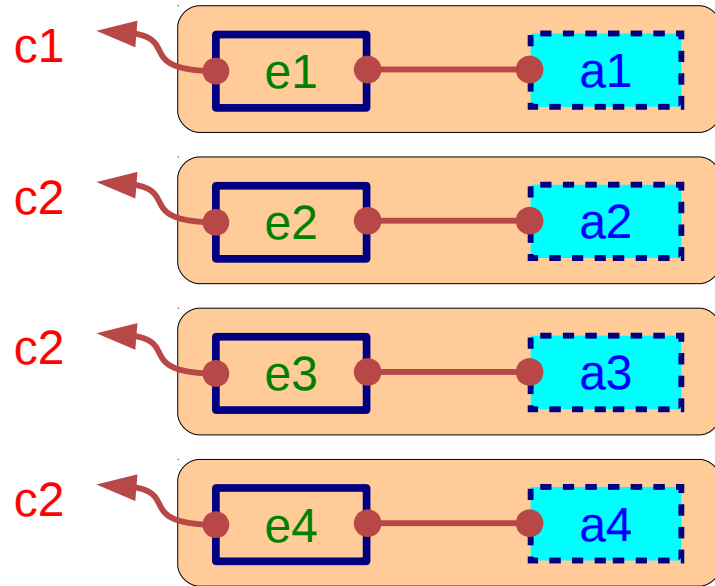
Entity - Architecture Binding



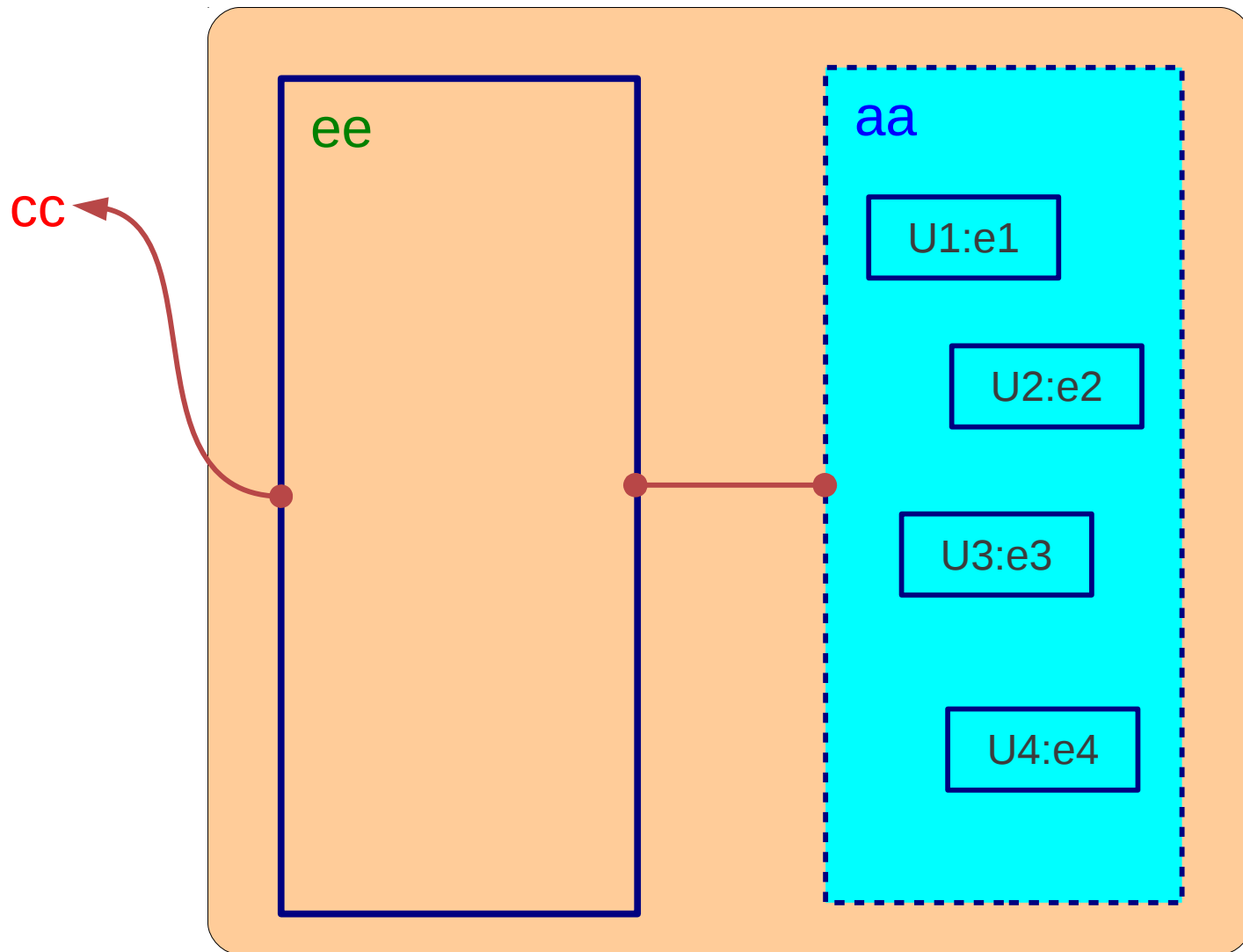
Configuration



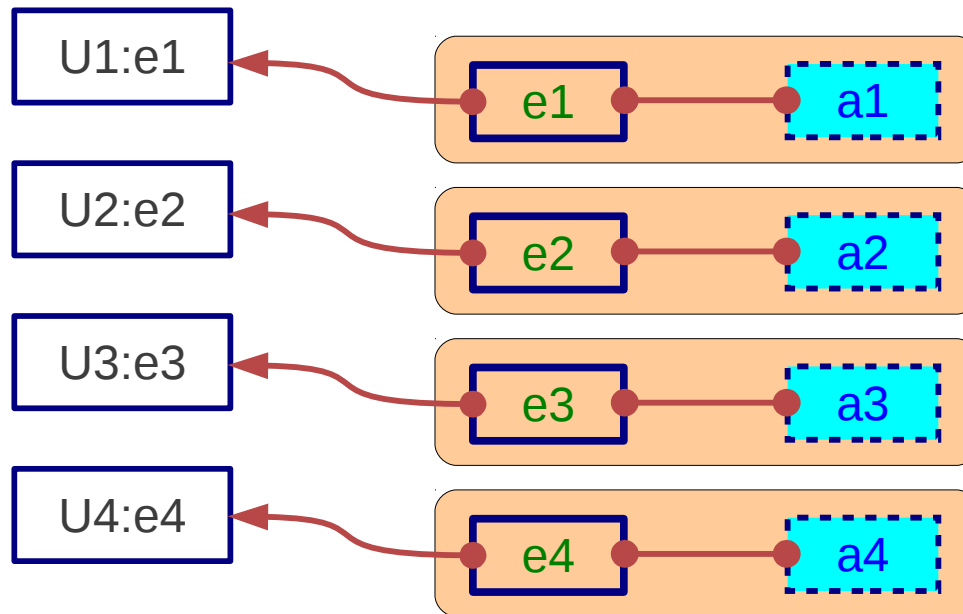
Configuration



Sequential Assignment (2)



Sequential Assignment (2)



Sequential Assignment (1)

Default Binding

Sequential Assignment (1)

Sequential Assignment (2)

Sequential Assignment (2)

References

- [1] <http://en.wikipedia.org/>
- [2] J. V. Spiegel, VHDL Tutorial,
http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
- [3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
- [4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
- [5] D. Smith, HDL Chip Design
- [6] <http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html>
- [7] VHDL Tutorial - VHDL online www.vhdl-online.de/tutorial/