

# Signals & Variables (3A)

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Synthesis

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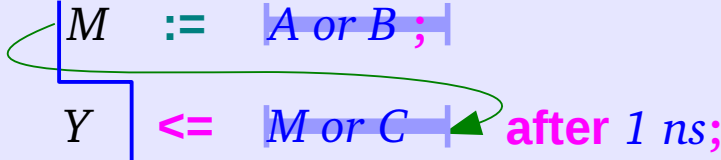
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# Ex 1

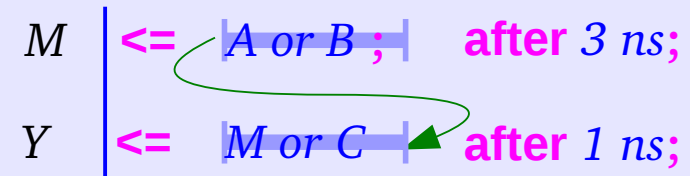
```
process (A, B, C)
  variable M: std_logic
begin
  M := A or B ;
  Y <= M or C after 1 ns;
end process;
```



end

# Ex 2

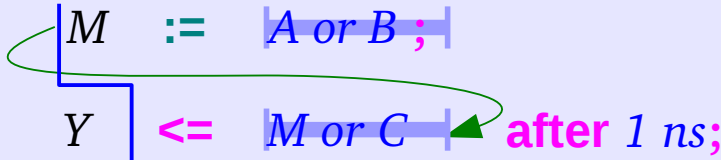
```
process (A, B, C, M)
  signal M: std_logic
begin
  M <= A or B ; after 3 ns;
  Y <= M or C ; after 1 ns;
end process;
```



end

# Ex 3

```
process (Clock)
  variable M: std_logic
begin
  if rising_edge(Clock) then
    M := A or B;
    Y <= M or C after 1 ns;
  end if;
end process;
```



end

# Ex 4

```
process (Clock)
  signal M: std_logic
begin
  if rising_edge(Clock) then
    M <= A or B ; after 3 ns;
    Y <= M or C ; after 1 ns;
  end if;
end process;
```

## References

- [1] <http://en.wikipedia.org/>
- [2] J. V. Spiegel, VHDL Tutorial,  
[http://www.seas.upenn.edu/~ese171/vhdl/vhdl\\_primer.html](http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html)
- [3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
- [4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
- [5] D. Smith, HDL Chip Design
- [6] <http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html>
- [7] VHDL Tutorial - VHDL online [www.vhdl-online.de/tutorial/](http://www.vhdl-online.de/tutorial/)