Signals & Variables (3A)

Synthesis

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Ex 1

```
process (A, B, C)
        variable M: std_logic
begin
        M    :=   A or B ;
        Y    <=   M or C  after 1 ns;
end process;
```

end

Ex 2

```
process (A, B, C, M)
        signal M: std_logic
begin
        M  <=  A or B ;     after 3 ns;
        Y  <=  M or C       after 1 ns;
end process;
```

end

Ex 3

```
process (Clock)
      variable M: std_logic
begin
    if rising_edge(Clock) then
        M   :=   A or B ;
        Y   <=   M or C  after 1 ns;
    end if;
end process;
```

end

Ex 4

```
process (Clock)
      signal M: std_logic
begin
    if rising_edge(Clock) then
        M  <=  A or B ;    after 3 ns;
        Y  <=  M or C      after 1 ns;
    end if;
end process;
```

References

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