```
--------------------------------------------------------------------------------
--
--  Purpose:
--
--    Add / Sub
--
--  Discussion:
--
--
--  Licensing:
--
--    This code is distributed under the GNU LGPL license.
--
--  Modified:
--
--    2012.03.26
--
--  Author:
--
--    Young W. Lim
--
--  Parameters:
--
--    Input:
--
--    Output:
--------------------------------------------------------------------------------

library STD;
use STD.textio.all;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;


entity addsub is
  port (an, bn,    : in  std_logic_vector (31 downto 0) := X"0000_0000";
        s,         : in  std_logic := '0';
        cn,        : out  std_logic_vector (31 downto 0) := X"0000_0000";
        co         : out  std_logic := '0');
end addsub;


architecture rtl of addsub is
  component adder
    port (an, bn,    : in  std_logic_vector (31 downto 0) := X"0000_0000";
          ci,        : in  std_logic := '0';
          cn,        : out  std_logic_vector (31 downto 0) := X"0000_0000";
          co         : out  std_logic := '0');
  end component;

begin

  process (an, bn, s)
  begin  -- process
    if (s='1') then
      un <= not bn;
    else
      un <= bn;
    end if;
  end process;

  A0: adder
      port map (an => an, bn => un, ci => s, cn => cn, co => co);

end rtl;
```