Idea (4A)

- Multi-byte Multiplication like CORDIC
- Trade-offs between
  Bit-Serial, Bit-Parallel
  Word-Serial, Word-Parallel
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Please send corrections (or suggestions) to youngwlim@hotmail.com.

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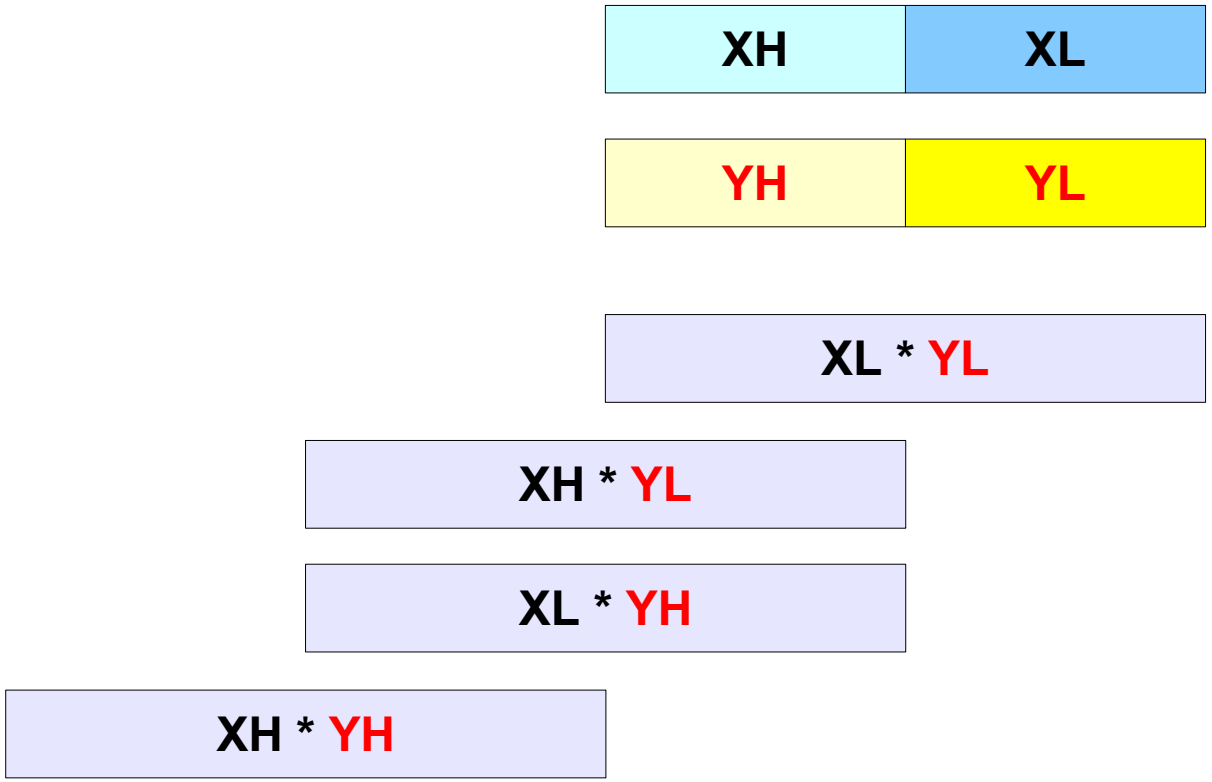
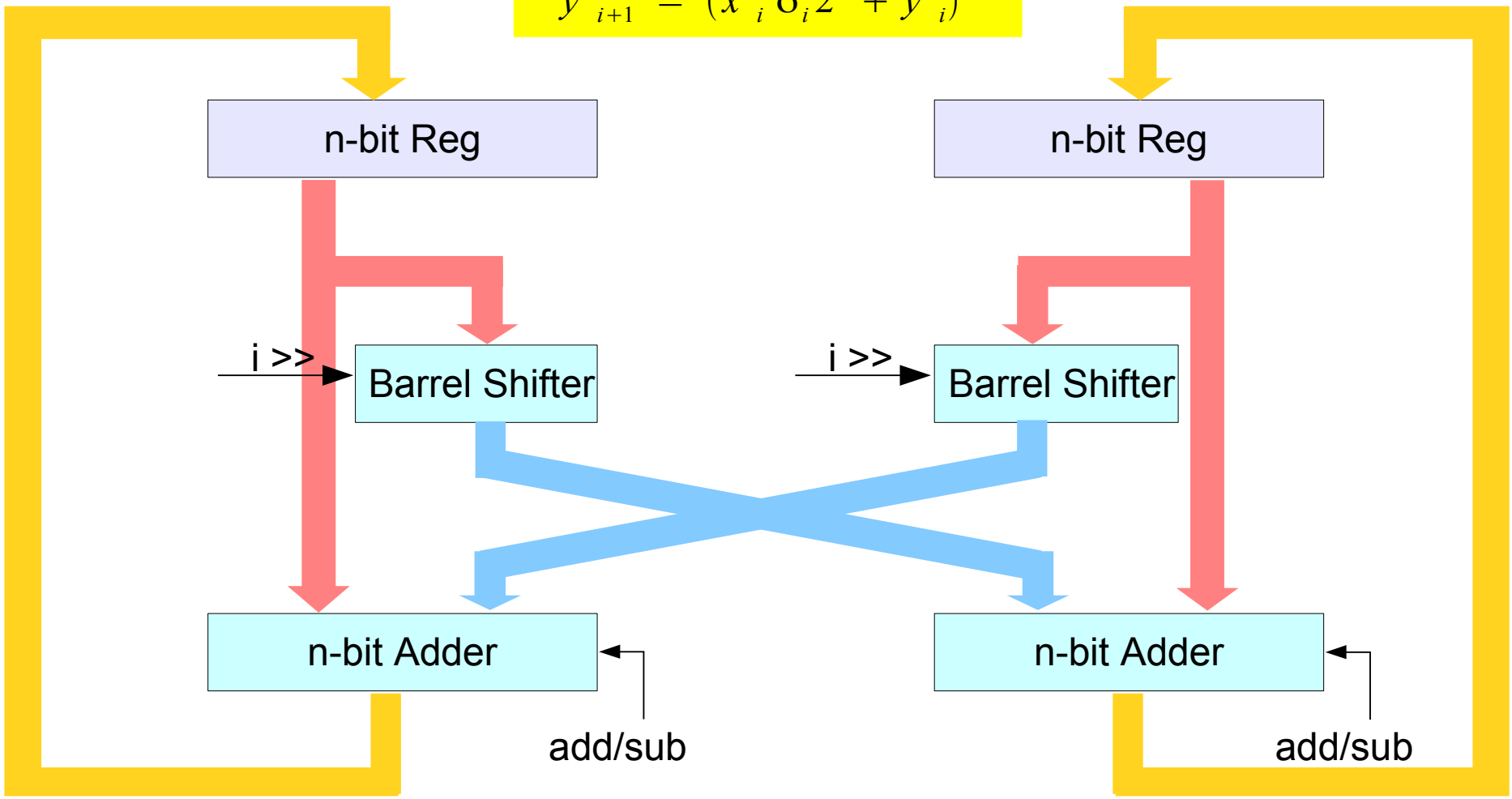
Multi-byte Multiplication

Long Operands Multiplication



$$x'_{i+1} = (x'_i - y'_i \sigma_i 2^{-i})$$
$$y'_{i+1} = (x'_i \sigma_i 2^{-i} + y'_i)$$



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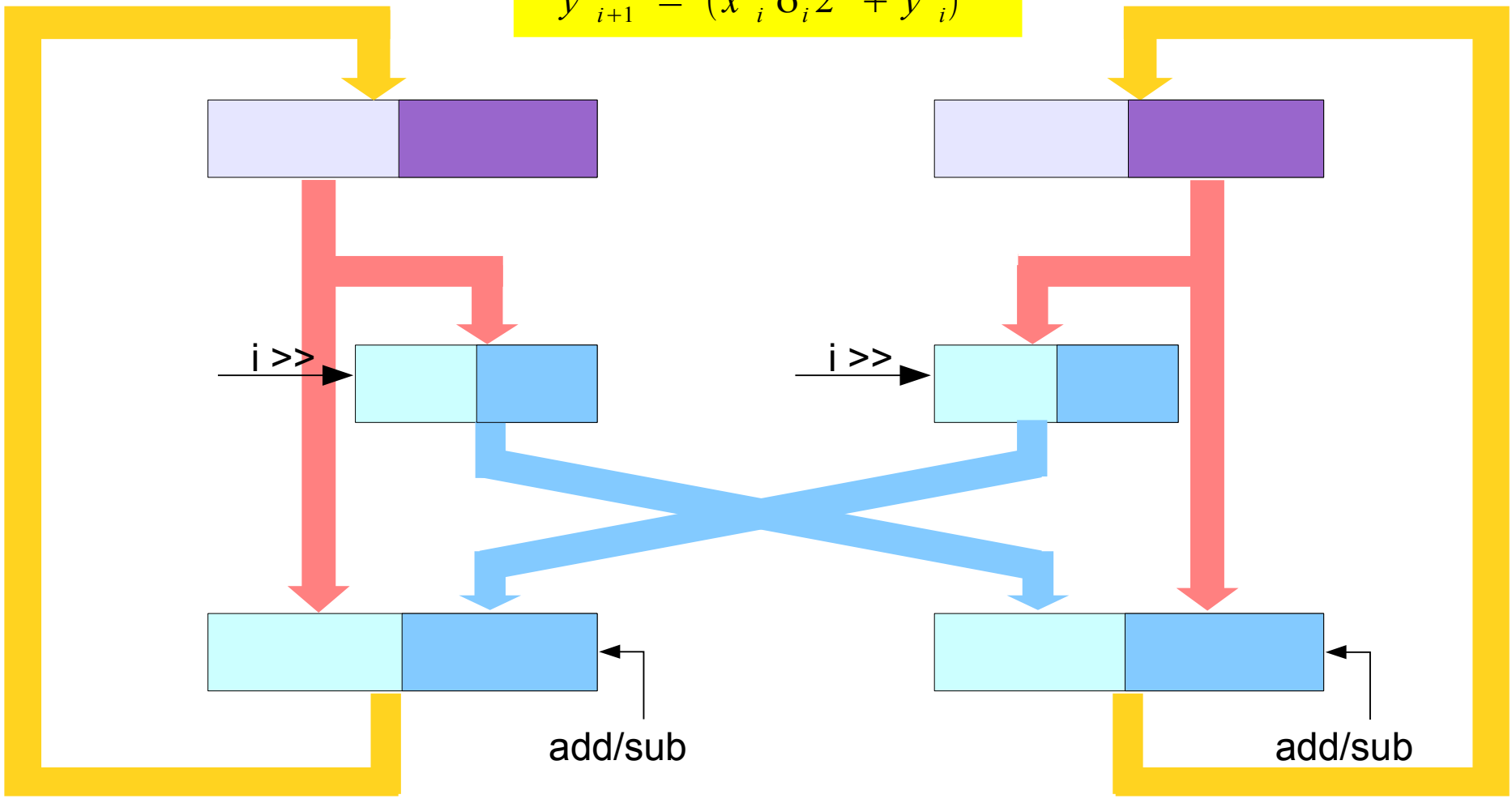

Generalization of multibyte arithmetic

Expect carry propagation time reduced and
Reasonable throughput maintained

May utilized pipeline

Total Latency reduced?, increased?

Power / Area / Time architectural exploration

May not be a new idea

Literature survey is required

References

[1] http://en.wikipedia.org/
[2] J.H. McClellan, et al., Signal Processing First, Pearson Prentice Hall, 2003
[3] A “graphical interpretation” of the DFT and FFT, by Steve Mann