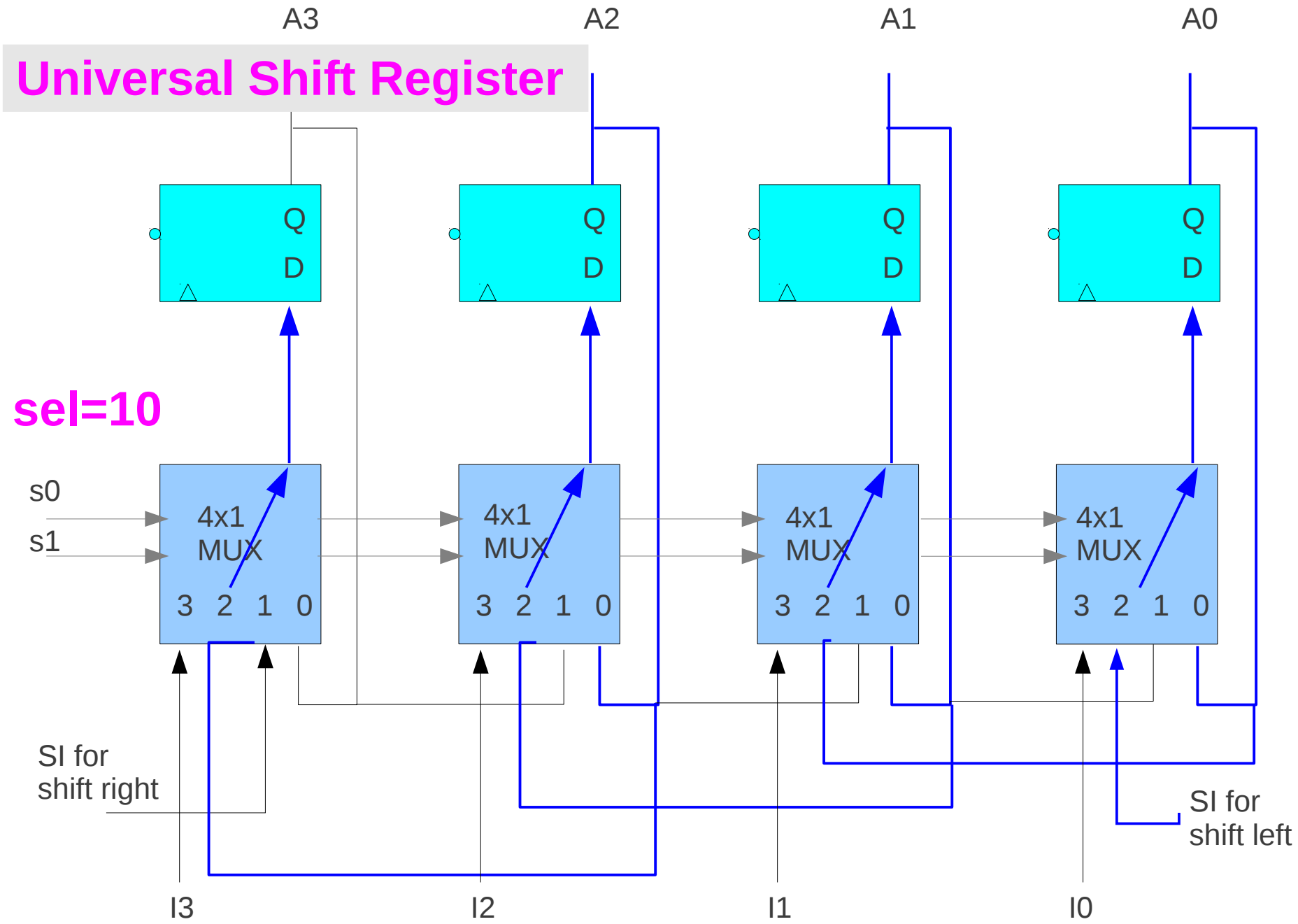
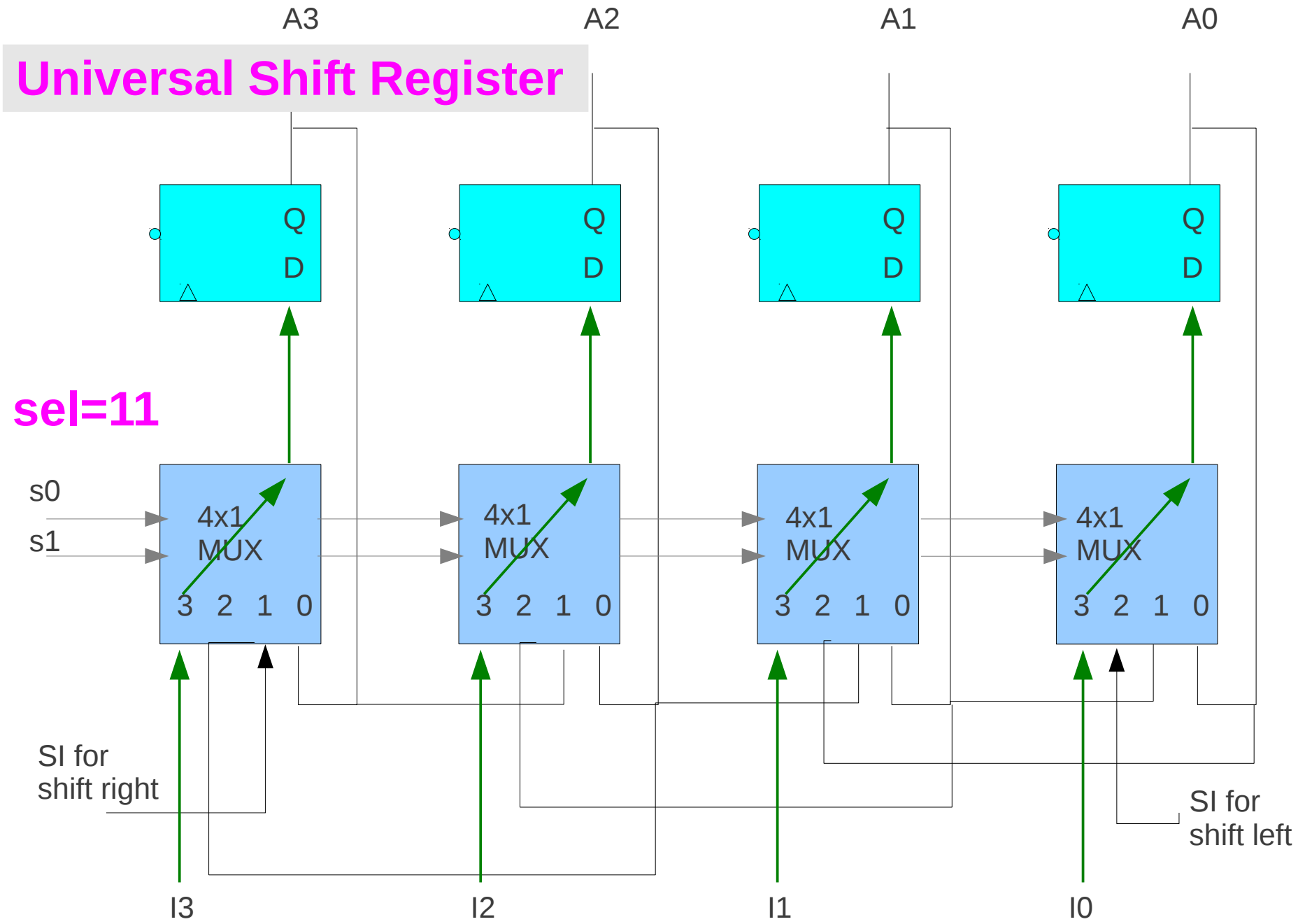
Universal Shift Register

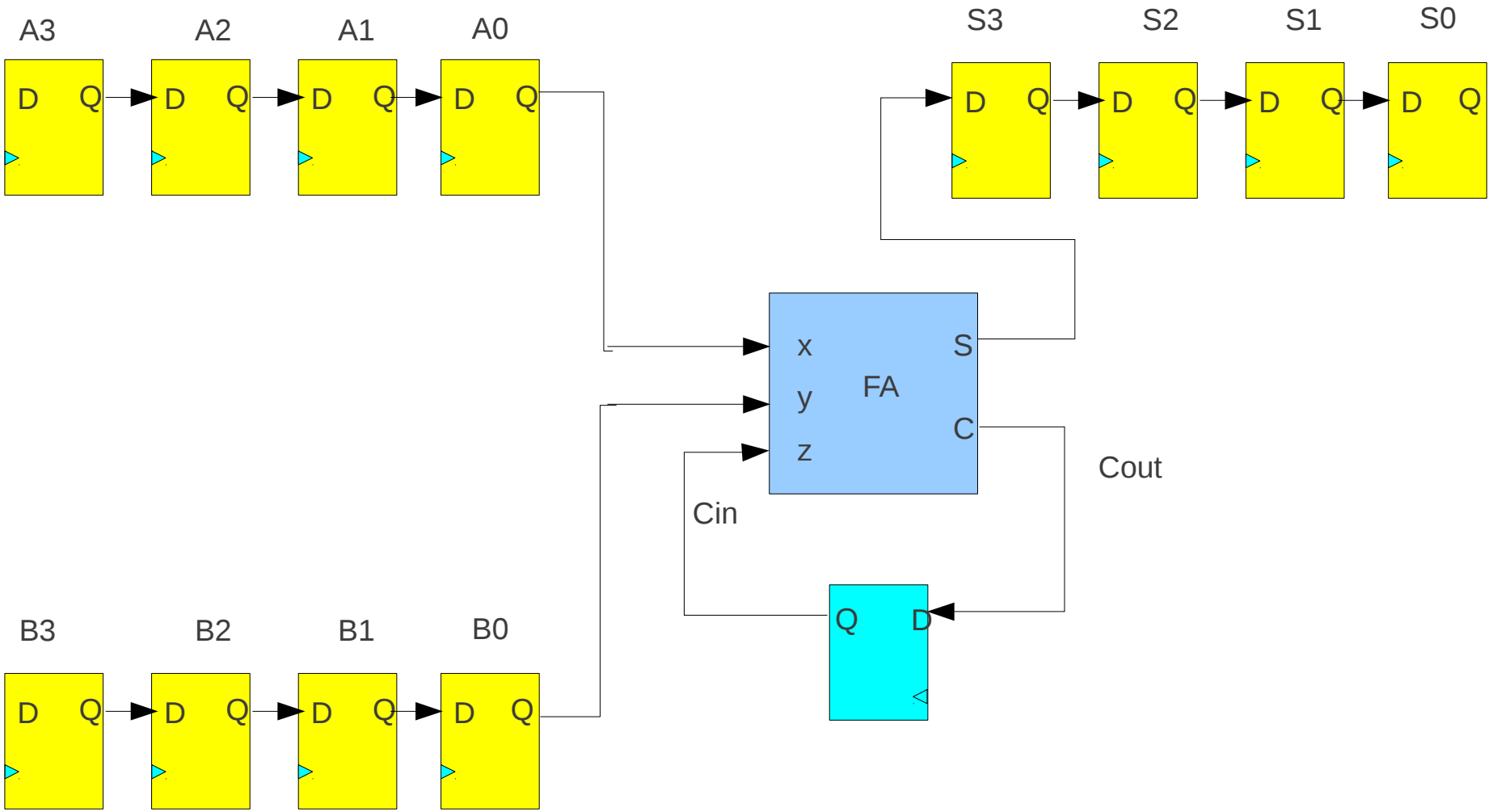


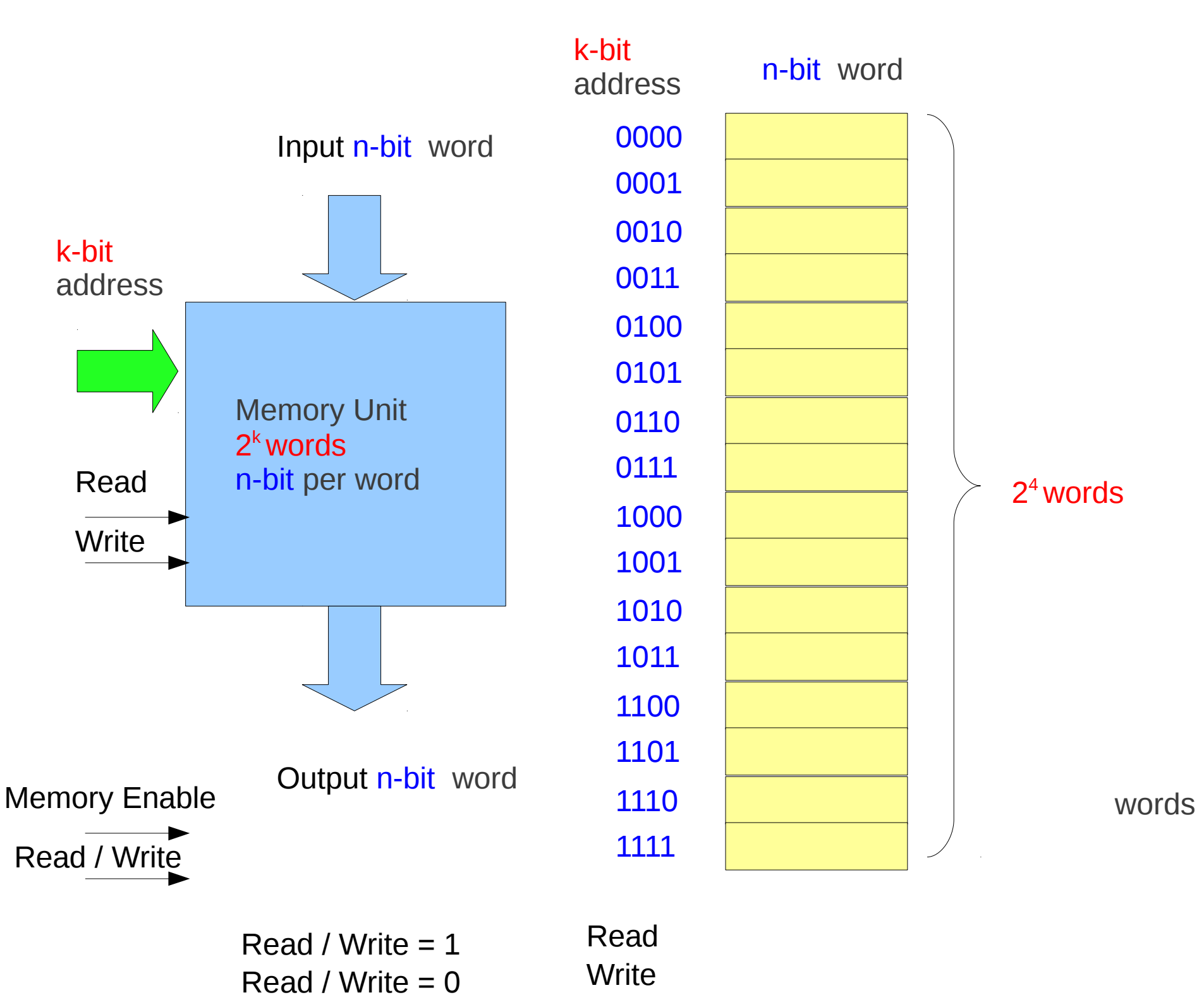
Shift Left (sel=10)

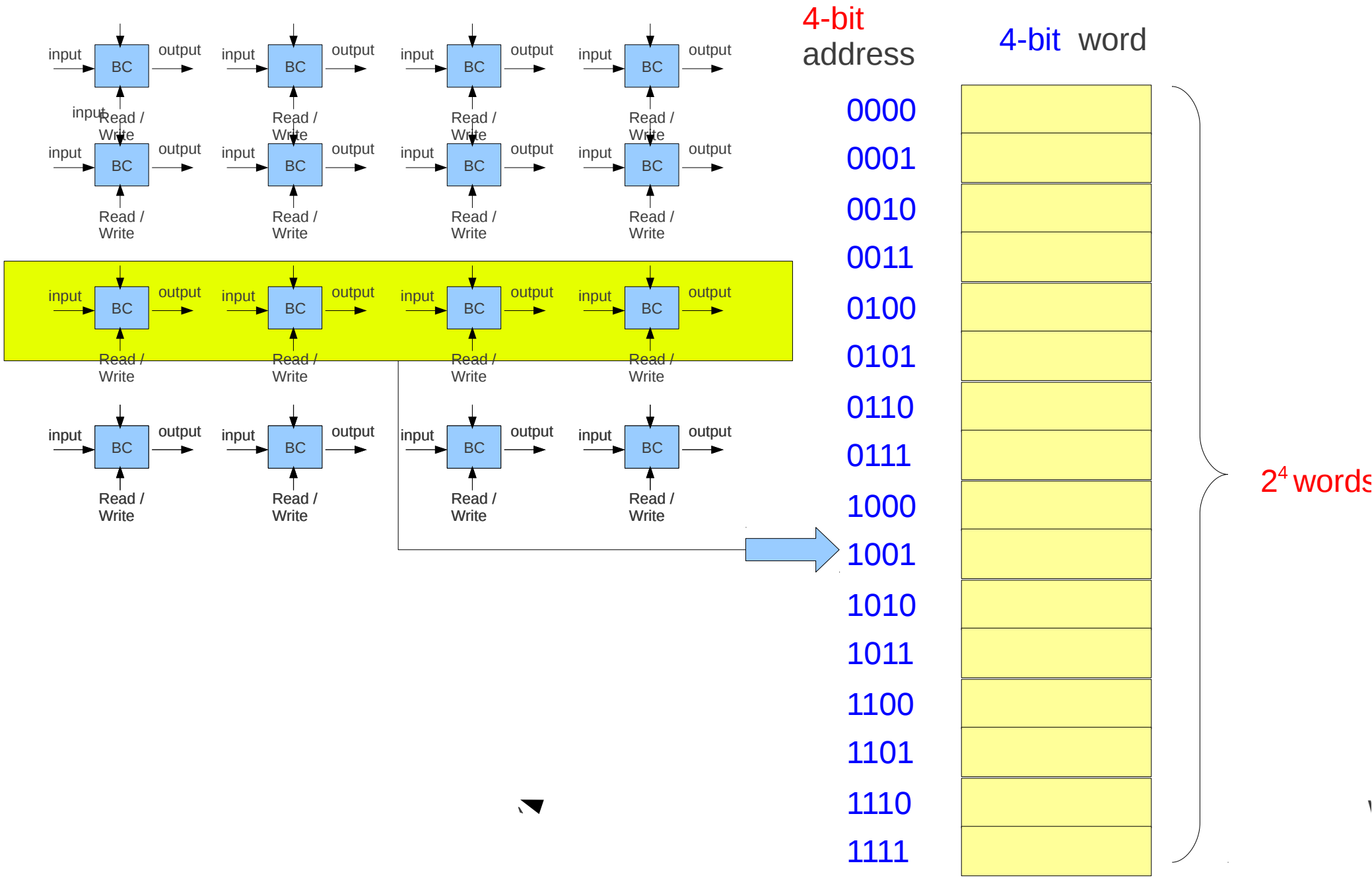
Universal Shift Register

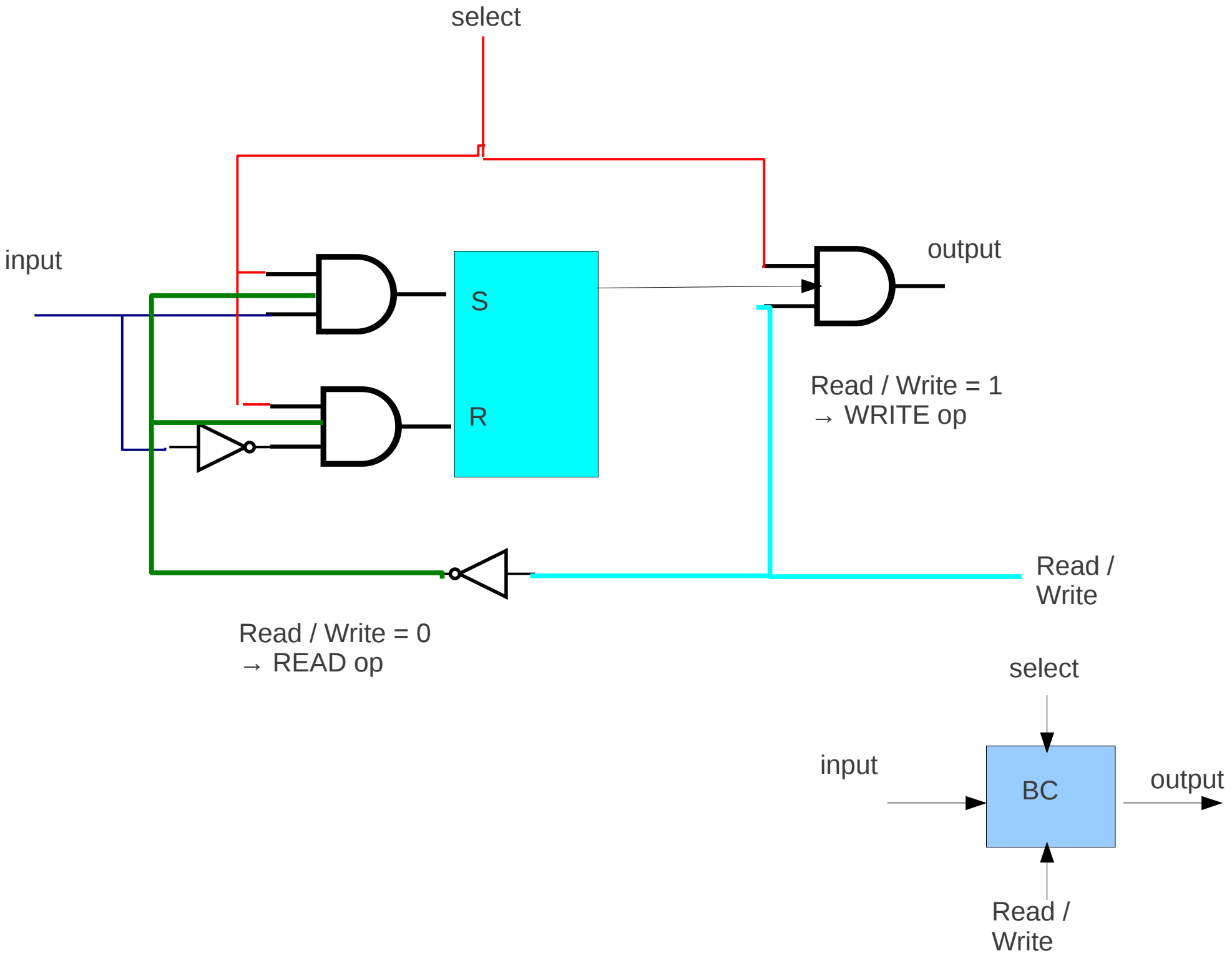


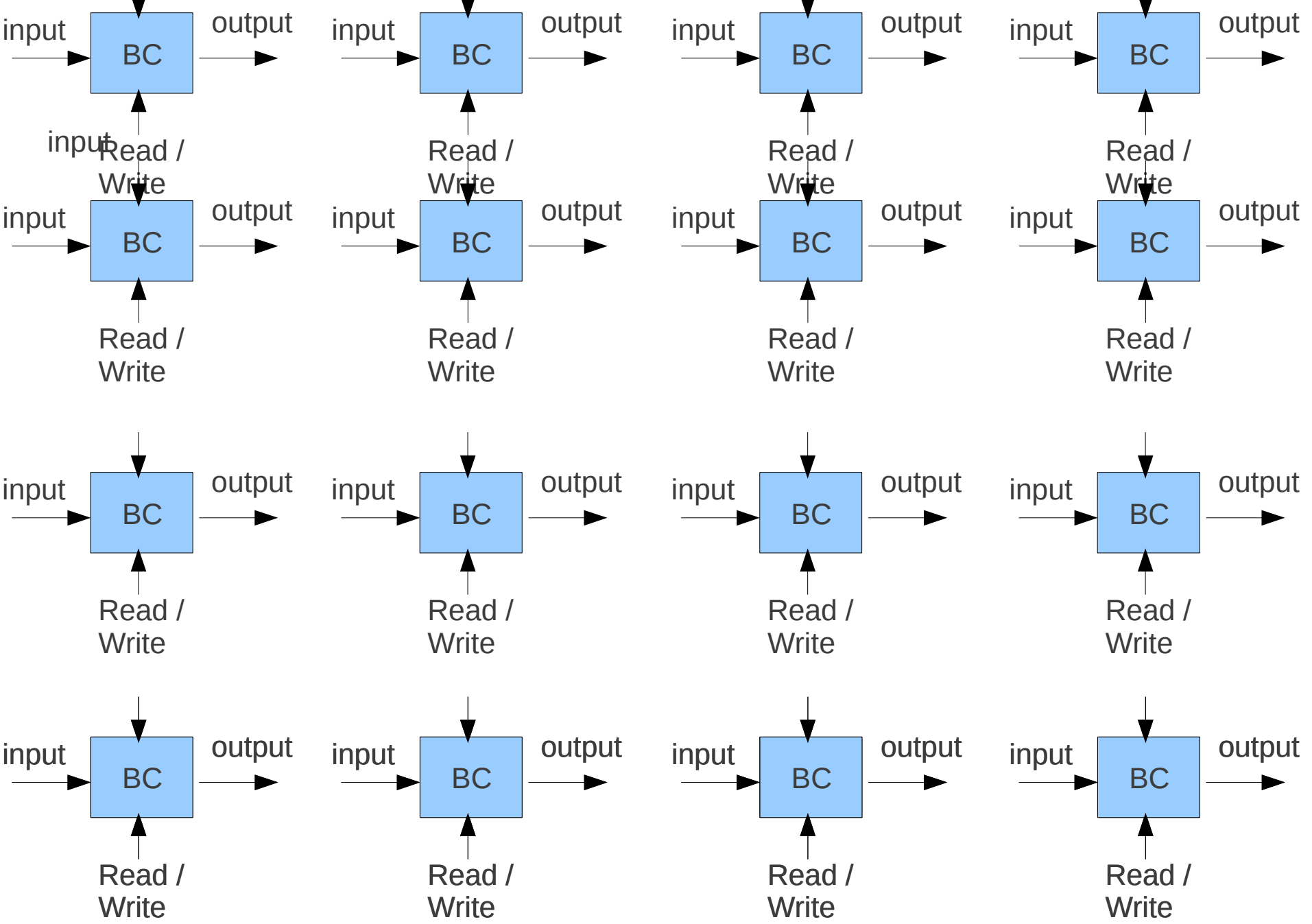
Parallel Load (sel=11)


A3
A2
A1
A0
S3
S2
S1
S0
D
Q
x
y
z
FA
S
C
Cout
Cin
B3
B2
B1
B0


k-bit
address
n-bit word
Input n-bit word
k-bit
address
Memory Unit
2^k words
n-bit per word
Read
Write
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
2^4 words
words
Output n-bit word
Memory Enable
Read / Write
Read / Write = 1
Read / Write = 0
Read
Write


input
BC
output
Read / Write
4-bit address
4-bit word
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
2^4 words


select
input
S
R
output
Read / Write = 1
→ WRITE op
Read / Write = 0
→ READ op
Read /
Write
select
input
BC
output
Read /
Write


input
BC
output
Read /
Write