Signal & Variable

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Concurrent Statement

- Block Statement
- Process Statement
- Component Statement
- Generate Statement
- Concurrent Signal Assignment
- Concurrent Assertion
- Concurrent Procedure Call

- Architecture Body
- Block Statement
- Generate Statement

- Conditional Signal Assignment
- Selected Signal Assignemnt

Sequential Statement

- Wait Statement
- Assertion Statement
- Report Statement
- Generate Statement
- Signal Assignment
- Variable Assignment
- Procedure Call
- If
- Case
- Loop
- Next
- Exit
- Return
- Null

- Case Statement
- If Statement
- Loop Statement
- Process Statement
- Subprogram Body

- Conditional Signal Assignment
- Selected Signal Assignment

Conditional Signal Assignment

```
Z <=    A or B    [ after 1 ns ]    when S0 = '1'  else
        A or C    [ after 2 ns ]    when S1 = '1' else
        A or D    [ after 3 ns ]    ;
```

```
Z <=    A or B    [ after 1 ns ]    when S0 = '1' else
        A or C    [ after 2 ns ]    ;
```

```
Z <=    A or B    [ after 1 ns ]    when S0 = '1' ;
```

```
Z <=    A or B    [ after 1 ns ]    ;
```

⬅ *simple concurrent statement*

- Concurrent Signal Assignment
  - Conditional Signal Assignment
  - Selected Signal Assignment

Selected Signal Assignment

- Conditional Signal Assignment

```
Z <=    A or B    [ after 1 ns ]   when SEL = "00"  else
        A or C    [ after 2 ns ]   when SEL = "01" else
        A or D    [ after 2 ns ]   when SEL = "10" else
        A or E    [ after 3 ns ]   when SEL = "11" else
        A or F    [ after 4 ns ]   ;
```

- Selected Signal Assignment

```
with SEL select
Z <=    A or B    [ after 1 ns ]   when "00",
        A or C    [ after 2 ns ]   when "01",
        A or D    [ after 3 ns ]   when "10",
        A or E    [ after 4 ns ]   when "11",
        A or F    [ after 5 ns ]   when others;
```

Concurrent vs Sequential

```
with SEL select
Z <=    A or B    [ after 1 ns ]    when "00" ,
                  ● ● ●
Z <=    A or B    [ after 1 ns ]    when SEL = "00"  else
                  ● ● ●
```

Should be outside process statement

```
Z <=    A or B    [ after 1 ns ] ;
```

Simple Concurrent signal statement outside process statement

```
process (A, B, C)
begin
    Z <=    A or B    [ after 1 ns ] ;

end
```

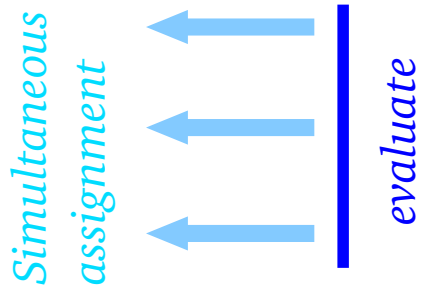
Sequential signal statement inside process statement

- Architecture Body
- Block Statement
- Generate Statement

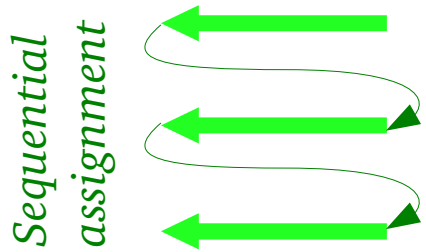
Order

```
architecture arch of entity ent is
begin
    X1 <= A or B ;
    Y1 <= C or D ;
    Z1 <= E or F ;

    process (A, B, C)
    begin
        X1 <= A or B ;
        Y1 <= C or D ;
        Z1 <= E or F ;
    end

end
```

Simulation of parallel activities



The order of statements is important



References

[1] http://en.wikipedia.org/
[2]