

Intel[®] 6 Series Express Chipset SPI Programming Guide

Application Note For Desktop and Notebook Platform

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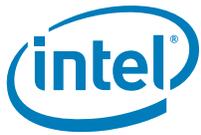
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Revision History

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445780	0.81	<ul style="list-style-type: none">Fixed formatting Errors	March 2010
	0.82	<ul style="list-style-type: none">Added necessary descriptor information to change processor featuresCorrected language on Dual input fast readAdded SMBus Fast mose for SMLINK0Updated Serial Flash requirements for ME	July 2010
	1.0	<ul style="list-style-type: none">updated FLMAP1 recommended valueupdated FLMAP2 recommended valueReclarified VTBA location at FLUMAP1Reclarified ME SMBUS MCTP Address definitionRemoved unused PCHSTRP10 softstrap settingAdding 12:10 bit as reserve in PSCHSTRP15Updated Bit 1 setting to PCHSTRP17Updated VSCC table at session 4.4.3 and 5.7	July 2011

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1 Introduction

1.1 Overview

This manual is intended for Original Equipment Manufacturers and software vendors to clarify various aspects of programming SPI flash on PCH family based platforms. The current scope of this document is Cougar Point Family only. **This Document is not relevant to platforms running on Server Platform Services (SPS) firmware.**

[Chapter 2, "PCH SPI Flash Architecture"](#)

Overview of SPI flash, Non-Descriptor vs. Descriptor, Flash Layout, Cougar Point compatible SPI flash

[Chapter 3, "PCH SPI Flash Compatibility Requirement"](#)

Overview of compatibility requirements for Cougar Point products.

[Chapter 4, "Descriptor Overview"](#)

Overview of the descriptor and Descriptor record definition

[Chapter 5, "Configuring BIOS/GbE for SPI Flash Access"](#)

Describes how to configure BIOS/GbE for SPI flash access.

[Chapter 6, "Flash Image Tool"](#)

This tool creates a descriptor and combines the GBE, BIOS, Platform Data Region and Intel® Management Engine (Intel® ME) firmware into one image.

[Chapter 7, "Flash Programming Tool"](#)

This tool programs the SPI flash device on the Cougar Point family platforms. This section will talk about requirements needed for FPT to work.

[Chapter 8, "SPI Flash Programming Procedures"](#)

Guide on how to program the SPI flash on the Intel CRB and PCH based platforms.

[Chapter 9, "Intel® Management Engine Disable for Debug/Flash Burning Purposes"](#)

Methods of disabling Intel Management Engine for debug purposes.

[Chapter 10, "Recommendations for SPI Flash Programming in Manufacturing Environments for Cougar Point"](#)

Recommendations for manufacturing environments.

[Chapter 11, "FAQ and Troubleshooting"](#)

Frequently asked questions and Troubleshooting tips.



1.2 Terminology

Table 1. Terminology

Term	Description
BIOS	<u>B</u> asic <u>I</u> nput- <u>O</u> utput <u>S</u> ystem
CRB	<u>C</u> ustomer <u>R</u> eference <u>B</u> oard
FPT	<u>F</u> lash <u>P</u> rogramming Tool – programs the SPI flash
FIT	<u>F</u> lash <u>I</u> mage <u>T</u> ool – creates a flash image from separate binaries
FW	<u>F</u> irm <u>w</u> are
FWH	<u>F</u> irm <u>w</u> are <u>H</u> ub – LPC based flash where BIOS may reside
Intel® AMT	<u>I</u> ntel® <u>A</u> ctive <u>M</u> anagement <u>T</u> echnology
GbE	Intel Integrated 1000/100/10
HDCP	<u>H</u> igh-bandwidth <u>D</u> igital <u>C</u> ontent <u>P</u> rotection
Cougar Point	Cougar Point Chipset. Platform Controller Hub
Intel® ME Firmware	Intel firmware that adds Intel Active Management Technology, Intel® QST, Braidwood Technology, Intel Anti-Theft Technology, Corwin Springs, Castle Peak, Sentry Peak, etc.
Intel PCH	<u>I</u> ntel <u>P</u> latform <u>C</u> ontroller <u>H</u> ub
Intel PCHn family	All PCHn derivatives including PCHn (desktop) and PCHnM (mobile)
Intel® QST	<u>I</u> ntel® <u>Q</u> uiet <u>S</u> ystem <u>T</u> echnology – Embedded hardware and firmware solution that allows for algorithmic relationship between system cooling fans and temperature monitors so as to reduce noise without losing thermal efficiency
LPC	<u>L</u> ow <u>P</u> in <u>C</u> ount Bus- bus on where legacy devices such a FWH reside
SPI	<u>S</u> erial <u>P</u> eripheral <u>I</u> nterface – refers to serial flash memory in this document
VSCC	<u>V</u> endor <u>S</u> pecific <u>C</u> omponent <u>C</u> apabilities
LVSCC	<u>L</u> ower <u>V</u> endor <u>S</u> pecific <u>C</u> omponent <u>C</u> apabilities
UVSCC	<u>U</u> pper <u>V</u> endor <u>S</u> pecific <u>C</u> omponent <u>C</u> apabilities



1.3 Reference Documents

Table 2. Reference Documents

Document	Document # / Location
<i>Intel Cougar Point Family External Design Specification (EDS)</i>	Contact Intel field representative
<i>Intel® Flash Image Tool (FIT)</i>	\System Tools\Flash Image Tool of latest <u>Intel® ME</u> kit from VIP/ARMS. The Kit MUST match the platform you intend to use the flash tools for.
<i>Intel® Flash Programming Tool (FPT)</i>	\System Tools\Flash Programming Tool of latest <u>Intel® ME</u> from VIP/ARMS. The Kit MUST match the platform you intend to use the flash tools for.
<i>FW Bring Up Guide</i>	Root directory of latest <u>Intel ME</u> kit from VIP/ARMS. The Kit MUST match the platform you intend to use the flash tools for.

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2 PCH SPI Flash Architecture

PCH SPI interface consists of clock (CLK), MOSI (Master Out Slave In) MISO (Master In Slave Out) and up to two active low chip selects (CSX#) on Cougar Point.

Cougar Point can support SPI flash devices up to 16 Mbytes per chip select. Cougar Point can support frequencies of 20 MHz, 33 MHz, and 50 MHz.

2.1 Non-Descriptor vs. Descriptor Mode

SPI Flash on Cougar Point has two operational modes: descriptor and non-descriptor. **Cougar Point supports descriptor mode only.**

Non-descriptor mode is not supported in due to all Cougar Point platforms requiring Intel ME FW.

Descriptor mode supports up to two SPI flashes, and allows for integrated LAN support, as well as Intel® ME firmware to share a single flash. There is also additional security for reads and writes to the flash. Hardware sequencing, heterogeneous flash space, Intel integrated LAN, Intel ME firmware on SPI flash, require descriptor mode. HDCP will be integrated into the chipset or add in card (not on flash) in all other instances. Descriptor mode requires the SPI flash to be hooked up directly to the PCH's SPI bus.

See [SPI Supported Feature Overview](#) of the latest *Intel I/O Controller Hub Family External Design Specification (EDS)* for Cougar Point for more detailed information.

2.2 Boot Destination Option

2.2.1 Boot Flow for Cougar Point

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x10. The descriptor fetch is triggered whichever comes first, the assertion of MEPWROK or deassertion of LAN_RST#. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the BIOS boot straps to determine the location of BIOS for host boot.

See Boot BIOS strap in the [Functional Straps](#) of the latest *Intel I/O Controller Hub Family External Design Specification (EDS)* for Cougar Point for more detailed information.

If LPC is chosen as the BIOS boot destination, then the PCH will fetch the reset vector on top of the firmware hub flash device.



If SPI is chosen as the BIOS destination, it will either fetch the reset vector on top of the SPI flash device on chip select 0, or if the PCH is in descriptor mode it will determine the location of BIOS through the base address that is defined in the SPI flash descriptor.

See [Chapter 4, “Descriptor Overview”](#) and for more detailed information.

2.3 Flash Regions

Flash Regions only exist in Descriptor mode. The controller can divide the SPI flash in up to five separate regions.

Region	Content
0	Descriptor
1	BIOS
2	ME – Intel® Management Engine Firmware
3	GbE – Location for Integrated LAN firmware and MAC address
4	PDR – Platform Data Region

The descriptor (Region 0) must be located in the first sector of component 0 (offset 0x10). Descriptor and ME regions are required for all Cougar Point based platforms

If Regions 0, 2, 3 or 4 are defined they must be on SPI. BIOS can be on either FWH or SPI. The BIOS that will load on boot will be set by Boot BIOS destination straps.

Only three masters can access the five regions: Host CPU, integrated LAN, and Intel® ME.

2.3.1 Flash Region Sizes

SPI flash space requirements differ by platform and configuration. Please refer to documentation specific to your platform for BIOS and ME Region flash size estimates.

The Flash Descriptor requires one block. GbE requires two separate blocks. The amount of actual flash space consumed for the above regions are dependent on the erase granularity of the flash part. Assuming 2 Mbyte BIOS, 64 Mb flash part is the target size of flash for largest configuration. BIOS size will determine how small of a flash part can be used for the platform.



Table 2-1. Region Size vs. Erase Granularity of Flash Components

Regions	Size with uniform 4 KB blocks
Descriptor	4 KB
GbE	8 KB
Platform Data Region	Varies by platform
BIOS	Varies by platform
ME	Varies by platform and configuration

2.4 Hardware vs. Software Sequencing

Hardware and Software sequencing are the two methods the PCH uses communicates with the flash via programming registers for each of the three masters.

When utilizing software sequencing, BIOS needs to program the OPTYPE and OPMENU registers respectively with the opcode it needs. It also defines how the system should use each opcode. If the system needs a new opcode that has not been defined, then BIOS can overwrite the OPTYPE and OPMENU register and define new functionality as long as the FLOCKDN bits have not been set.

FPT as well as some BIOS implementation use software sequencing.

Hardware sequencing has a predefined list of opcodes with only the erase opcode being programmable. This mode is only available if the descriptor is present and valid. Intel ME Firmware and Integrated LAN FW, and integrated LAN drivers all must use HW sequencing, so BIOS must properly set up the PCH to account for this. The Host VSCC registers and Management Engine VSCC table have to be correctly configured for BIOS, GbE and Intel ME Firmware to have read/write access to SPI.

See [Serial Peripheral Interface Memory Mapped Configuration Registers](#) in *Cougar Point Family External Design Specification (EDS)* for more details.

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3 PCH SPI Flash Compatibility Requirement

3.1 Cougar Point Family SPI Flash Requirements

Cougar Point allows for up to two SPI flash devices to store BIOS, Intel ME Firmware and security keys for Platform Data Region and integrated LAN information.

Intel ME FW is required for all Cougar Point based platforms!

3.1.1 SPI-based BIOS Requirements

- Erase size capability of: 4 KBytes.
- Serial flash device must ignore the upper address bits such that an address of FFFFFFFh aliases to the top of the flash memory.
- SPI Compatible Mode 0 support: Clock phase is 0 and data is latched on the rising edge of the clock.
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must discard the cycle gracefully without any impact on the flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, etc.) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- SPI flash parts that do not meet Hardware sequencing command set requirements may work in BIOS only platforms via software sequencing.

3.1.2 Integrated LAN Firmware SPI Flash Requirements

A serial flash device that will be used for system BIOS and Integrated LAN or Integrated LAN only must meet all the SPI Based BIOS Requirements plus:

Must support [3.1.6 Hardware Sequencing Requirements](#)

4 KBytes erase capability must be supported.

3.1.2.1 SPI Flash Unlocking Requirements for Integrated LAN

BIOS must ensure there is no SPI flash based read/write/erase protection on the GbE region. GbE firmware and drivers for the integrated LAN need to be able to read, write and erase the GbE region at all times.



3.1.3 Intel® Management Engine (Intel® ME) Firmware SPI Flash Requirements

Intel Management Firmware must meet the SPI flash based BIOS Requirements plus:

[3.1.4 JEDEC ID \(Opcode 9Fh\)](#)

[3.1.5 Multiple Page Write Usage Model](#)

[3.1.6 Hardware Sequencing Requirements](#)

Flash part must be uniform 4 KB erasable block throughout the entire part

Write protection scheme must meet guidelines as defined in [3.1.3.1 SPI Flash Unlocking Requirements for Management Engine](#)

3.1.3.1 SPI Flash Unlocking Requirements for Management Engine

Flash devices must be globally unlocked (read, write and erase access on the ME region) from power on by writing 00h to the flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire part. If the SPI flash's status register has non-volatile bits that must be written to, bits [5:2] of the flash's status register must be all 0h to indicate that the flash is unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, BIOS has the ability to lock down small sections of the flash as long as they do not involve the ME or GbE region. See [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) and [5.2 Locking SPI Flash via Status Register](#) for more information about flash based write/erase protection.

3.1.4 JEDEC ID (Opcode 9Fh)

Since each serial flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV1 and is available on the JEDEC website: www.jedec.org.

3.1.5 Multiple Page Write Usage Model

Intel platforms have firmware usage models require that the serial flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Intel firmware usage models require the capability for multiple data



updates within any given page. These data updates occur via byte-writes without executing a preceding erase to the given page. Both the BIOS and Intel Management Engine firmware multiple page write usage models apply to sequential and non-sequential data writes.

Flash parts must also support the writing of a single bytes 1024 times in a single 256 Byte page without erase. There will be 64 pages where this usage model will occur. These 64 pages will be every 16 Kilo bytes.

3.1.6 Hardware Sequencing Requirements

The following table contains a list of commands and the associated opcodes that a SPI-based serial flash device must support in order to be compatible with hardware sequencing.

Commands	OPCODE	Notes
Write to Status Register	01h	Writes a byte to SPI flash's status register. Enable Write to Status Register command must be run prior to this command
Program Data	02h	Single byte or 64 byte write as determined by flash part capabilities and software
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of SPI flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	50h or 06h	Enables a bit in the status register to allow an update to the status register
Erase	Programmable	4 Kbyte erase
Chip Erase	C7h and/or 60	
JEDEC ID	9Fh	See Section 3.1.4 for more information

3.2 Cougar Point SPI AC Electrical Compatibility Guidelines

Table 3-1. SPI Timings (20 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180a	Serial Clock Frequency - 20MHz Operation	17.06	18.73	MHz	1
t183a	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	13	ns	
t184a	Setup of SPI_MISO with respect to serial clock falling edge at the host	16	-	ns	
t185a	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186a	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	



Table 3-1. SPI Timings (20 MHz)

Sym	Parameter	Min	Max	Units	Notes
t187a	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188a	SPI_CLK High time	26.37	-	ns	2
t189a	SPI_CLK Low time	26.82	-	ns	2

Notes:

1. Typical clock frequency driven by Cougar Point is 17.86 MHz
2. Measurement point for low time and high time is taken at .5(VccME3_3)

Table 3-2. SPI Timings (33 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180b	Serial Clock Frequency - 33MHz Operation	29.83	32.81	MHz	1
t183b	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	5	ns	
t184b	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	-	ns	
t185b	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186b	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t187b	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188b	SPI_CLK High time	14.88	-	ns	2
t189b	SPI_CLK Low time	15.18	-	ns	2

Notes:

1. Typical clock frequency driven by Cougar Point is 31.25 MHz
2. Measurement point for low time and high time is taken at .5(VccME3_3)

Table 3-3. SPI Timings (50 MHz)

Sym	Parameter	Min	Max	Units	Notes
t180c	Serial Clock Frequency - 50MHz Operation	46.99	53.40	MHz	1
t183c	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-3	3	ns	
t184c	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	-	ns	
t185c	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	
t186c	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	



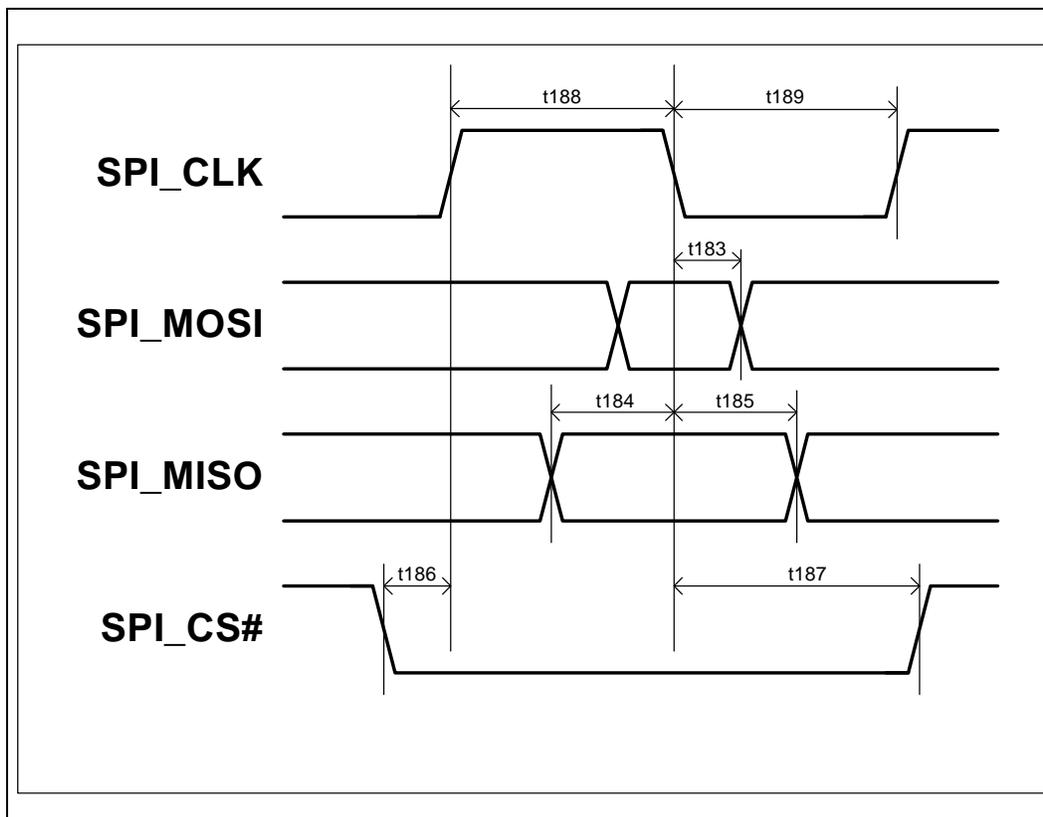
Table 3-3. SPI Timings (50 MHz)

Sym	Parameter	Min	Max	Units	Notes
t187c	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	-	ns	
t188c	SPI_CLK High time	7.1	-	ns	2,3
t189c	SPI_CLK Low time	11.17	-	ns	2,3

Notes:

1. Typical clock frequency driven by Cougar Point is 50 MHz.
2. When using 50 MHz mode ensure target flash component can meet t188c and t189c specifications.
3. Measurement point for low time and high time is taken at .5(VccME3_3)

Figure 3-1. SPI Timing



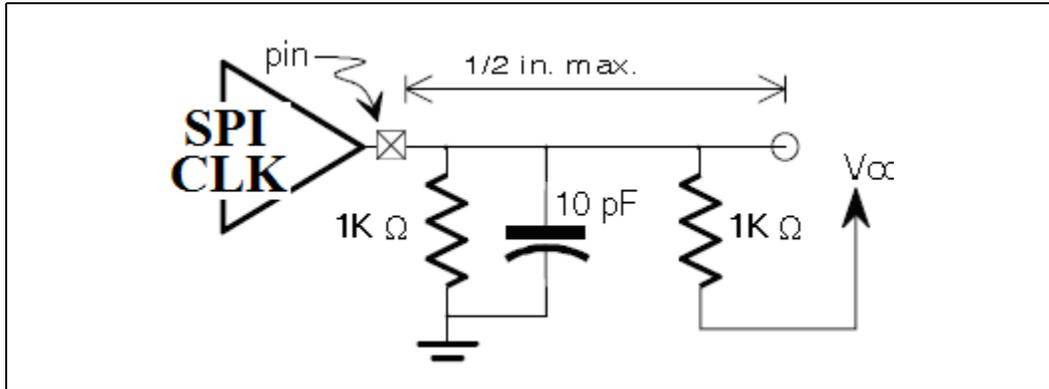
3.3 SPI Flash DC Electrical Compatibility Guidelines

Parameter	Min	Max	Units	Notes
Supply Voltage (Vcc)	3.14	3.7	V	
Input High Voltage	0.5*VCC	VCC+0.5	V	
Input Low Voltage	-0.5	0.3*VCC	V	
Output High Characteristics	0.9*VCC	VCC	V	Ioh = -0.5mA
Output Low Characteristics		0.1*VCC		Iol = 1.5mA
Input Leakage Current	-10	10	uA	
Output Rise Slew Rate (0.2Vcc - 0.6Vcc)	1	4	V/ns	1
Output Fall Slew Rate (0.6Vcc - 0.2Vcc)	1	4	V/ns	1

Notes:

1. Testing condition: 1K pull up to Vcc, 1kohm pull down and 10pF pull down and 1/2 inch trace See Figure 3.3 for more detail.

Figure 3-2. PCH Test Load



§ §



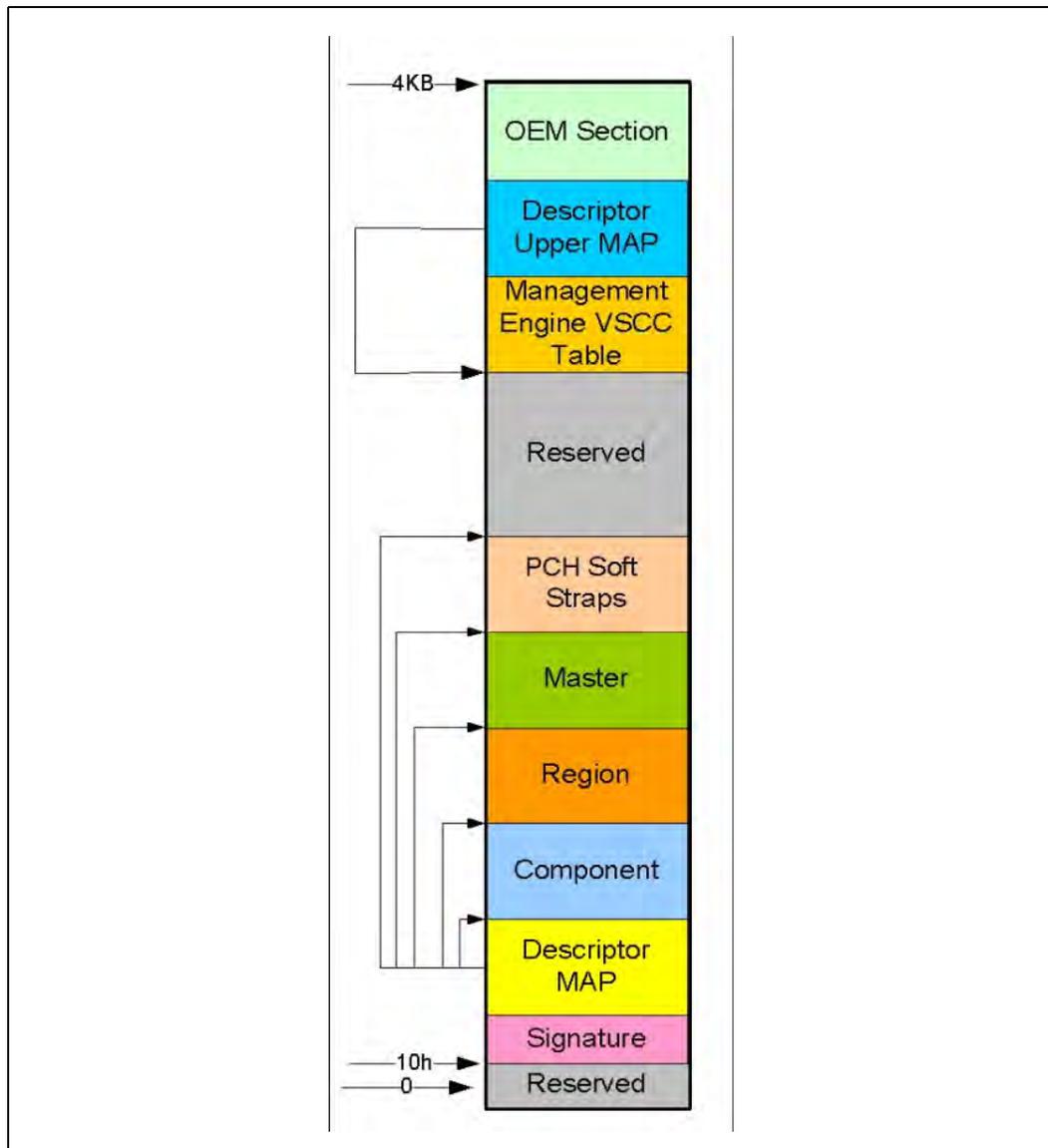
4 Descriptor Overview

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Cougar Point based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

The Descriptor has 9 basic parts:

Figure 4-1. Flash Descriptor (Cougar Point)



- The Flash signature at the bottom of the flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Flash signature at the bottom of the flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.



- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image.
- BIOS and GbE write and erase capabilities depend on LVSCC and UVSCC registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

See [SPI Supported Feature Overview](#) and [Flash Descriptor Records](#) in the *Intel Cougar Point Family External Design Specification (EDS)*.

4.1 Flash Descriptor Content

The following sections describe the data structure of the Flash Descriptor on the SPI device. These are not registers or memory space within PCH. FDBAR - is address 0x0 on the SPI flash device on chip select 0.

4.1.1 Descriptor Signature and Map

4.1.1.1 FLVALSIG - Flash Valid Signature (Flash Descriptor Records)

Memory Address: FDBAR + 010h
 Recommended Value: 0FF0A55Ah

Size: 32 bits

Bits	Description
31:0	Flash Valid Signature. This field identifies the Flash Descriptor sector as valid. If the contents at this location contain 0FF0A55Ah, then the Flash Descriptor is considered valid and it will operate in Descriptor Mode, else it will operate in Non-Descriptor Mode.



4.1.1.2 FLMAP0 - Flash Map 0 Register (Flash Descriptor Records)

Memory Address: FDBAR + 014h

Size: 32 bits

Bits	Description
31:27	Reserved
26:24	Number Of Regions (NR) . This field identifies the total number of Flash Regions. This number is 0's based, so a setting of all 0's indicates that the only Flash region is region 0, the Flash Descriptor region.
23:16	Flash Region Base Address (FRBA) . This identifies address bits [11:4] for the Region portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. Set this value to 04h. This will define FRBA as 40h.
15:10	Reserved
9:8	Number Of Components (NC) . This field identifies the total number of Flash Components. Each supported Flash Component requires a separate chip select. 00 = 1 Component 01 = 2 Components All other settings = Reserved
7:0	Flash Component Base Address (FCBA) . This identifies address bits [11:4] for the Component portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. set this field to 03h. This will define FCBA as 30h

4.1.1.3 FLMAP1—Flash Map 1 Register (Flash Descriptor Records)

Memory Address: FDBAR + 018h

Size: 32 bits

Recommended Value: 12100206h

Bits	Description
31:24	PCH Strap Length (ISL) . Identifies the 1s based number of Dwords of PCH Straps to be read, up to 255 DWs (1KB) max. A setting of all 0's indicates there are no PCH DW straps. This field MUST be set to 12h
23:16	Flash PCH Strap Base Address (FPSBA) . This identifies address bits [11:4] for the PCH Strap portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. Set this field to 10h. This will define FPSBA to 100h
15:10	Reserved
9:8	Number Of Masters (NM) . This field identifies the total number of Flash Masters. Set this field to 10b
7:0	Flash Master Base Address (FMBA) . This identifies address bits [11:4] for the Master portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. Set this field to 06h. This will define FMBA as 60h



4.1.1.4 FLMAP2—Flash Map 2 Register (Flash Descriptor Records)

Memory Address: FDBAR + 01Ch
 Recommended Value: 00210120h

Size: 32 bits

Bits	Description
31:24	Reserved
23:16	<p>ICC Register Init Base Address (ICCRIBA): This identifies address bits [11:4] for the ICC Register Init portion of the Flash Descriptor. Bit [24:12] and bits [3:0] are 0.</p> <p>Set this field to 21h.</p>
15:08	<p>PROC Strap Length (PSL). Identifies the 1's based number of Dwords of Processor Straps to be read, up to 255 DWs (1KB) max. A setting of all 0's indicates there are no Processor DW straps.</p> <p>Set this field to 01h for Sandybridge and Ivybridge</p>
7:0	<p>Flash Processor Strap Base Address (FMSBA). This identifies address bits [11:4] for the Processor Strap portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.</p> <p>Set this field to 20h. This will define FMSBA as 200h</p>

4.1.2 Flash Descriptor Component Section

The following section of the Flash Descriptor is used to identify the different SPI Flash Components and their capabilities.

4.1.2.1 FLCOMP—Flash Components Record (Flash Descriptor Records)

Memory Address: FCBA + 000h

Size: 32 bits

Bits	Description
31	Reserved
30	<p>Dual Output Fast Read Support</p> <p>0 : Dual Output Fast Read is not supported 1 : Dual Output Fast Read is supported</p> <p>Notes:</p> <ol style="list-style-type: none"> If the Dual Output Fast Read Support bit is set to 1b, the Dual Output Fast Read instruction is issued in all cases where the Fast Read would have been issue The Frequencies supported for the Dual Output Fast Read are the same as those supported by the Fast Read Instruction If more than one Flash component exists, this field can only be set to "1" if both component support Dual Output Fast Read The Dual output Fast Fead is only supported using the 3Bh opcode and dual read only affect the read data, not the address phase.
29:27	<p>Read ID and Read Status Clock Frequency.</p> <p>000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other Settings = Reserved</p> <p>Notes:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. If setting to 50 MHz, ensure flash meets timing requirements defined in Table 3-3



Bits	Description
26:24	<p>Write and Erase Clock Frequency. 000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other Settings = Reserved</p> <p>Notes:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. If setting to 50 MHz, ensure flash meets timing requirements defined in Table 3-3
23:21	<p>Fast Read Clock Frequency. This field identifies the frequency that can be used with the Fast Read instruction. This field is undefined if the Fast Read Support field is '0'. 000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other Settings = Reserved</p> <p>Notes:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components. If setting to 50 MHz, ensure flash meets timing requirements defined in Table 3-3
20	<p>Fast Read Support. 0 = Fast Read is not Supported 1 = Fast Read is supported</p> <p>If the Fast Read Support bit is a '1' and a device issues a Direct Read or issues a read command from the Hardware Sequencer and the length is greater than 4 bytes, then the SPI Flash instruction should be "Fast Read". If the Fast Read Support is a '0' or the length is 1-4 bytes, then the SPI Flash instruction should be "Read".</p> <p>Reads to the Flash Descriptor always use the Read command independent of the setting of this bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field can only be set to '1' if both components support Fast Read. It is strongly recommended to set this bit to 1b
19:17	<p>Read Clock Frequency. 000 = 20 MHz All other Settings = Reserved</p> <p>Note:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components.



Bits	Description
16:6	Reserved
5:3	<p>Component 2 Density. This field identifies the size of the 2nd Flash component connected directly to the PCH. If there is not 2nd Flash component, the contents of this field are unused.</p> <p>000 = 512 KB 001 = 1 MB 010 = 2 MB 011 = 4 MB 100 = 8 MB 101 = 16 MB 111 = Reserved</p>
2:0	<p>Component 1 Density. This field identifies the size of the 1st or only Flash component connected directly to the PCH.</p> <p>000 = 512 KB 001 = 1 MB 010 = 2 MB 011 = 4 MB 100 = 8 MB 101 = 16 MB 111 = Reserved</p> <p>Note: If using a flash part smaller than 512 KB, use the 512 KB setting.</p>

4.1.2.2 FLILL—Flash Invalid Instructions Record (Flash Descriptor Records)

Memory Address: FCBA + 004h

Size: 32 bits

Bits	Description
31:24	Invalid Instruction 3. See definition of Invalid Instruction 0
23:16	Invalid Instruction 2. See definition of Invalid Instruction 0
15:8	Invalid Instruction 1. See definition of Invalid Instruction 0
7:0	<p>Invalid Instruction 0.</p> <p>Op-code for an instruction that the Flash Controller should protect against, such as Chip Erase. This byte should be set to 0 if there are no invalid instructions to protect against for this field. Op-codes programmed in the Software Sequencing Opcode Menu Configuration and Prefix-Opcode Configuration are not allowed to use any of the Invalid Instructions listed in this register.</p>



4.1.2.3 FLPB—Flash Partition Boundary Record (Flash Descriptor Records)

Memory Address: FCBA + 008h

Size: 32 bits

Bits	Description
31:13	Reserved
12:0	<p>Flash Partition Boundary Address (FPBA). This register specifies Flash Boundary Address bits[24:12] that logically divides the flash space into two partitions, a lower and an upper partition. The lower and upper partitions can support SPI flash parts with different attributes between partitions that are defined in the LVSCC and UVSCC.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. All flash space in each partition must have the same in the VSCC attributes, even if it spans between different flash parts. 2. If this field is set to all 0s, then there is only one partition, the upper partition, and the entire address space has uniform erasable sector sizes, write granularity, and write state required settings. The FPBA must reside on an erasable sector boundary. If set to all zeros, then only UVSCC register value is used (with the exception of the VCL bit).

4.1.3 Flash Descriptor Region Section

The following section of the Flash Descriptor is used to identify the different Regions of the NVM image on the SPI flash.

Flash Regions:

- If a particular region is not using SPI Flash, the particular region should be disabled by setting the Region Base to all 1's, and the Region Limit to all 0's (base is higher than the limit)
- For each region except FLREG0, the Flash Controller must have a default Region Base of FFFh and the Region Limit to 000h within the Flash Controller in case the Number of Regions specifies that a region is not used.

4.1.3.1 FLREG0—Flash Region 0 (Flash Descriptor) Register (Flash Descriptor Records)

Memory Address: FRBA + 000h

Size: 32 bits

Recommended Value: 00000000h

Bits	Description
31:29	Reserved
28:16	<p>Region Limit. This specifies bits 24:12 of the ending address for this Region.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Set this field to 0b. This defines the ending address of descriptor as being FFFh. 2. Region limit address Bits[11:0] are assumed to be FFFh
15:13	Reserved
12:0	<p>Region Base. This specifies address bits 24:12 for the Region Base.</p> <p>Note: Set this field to all 0s. This defines the descriptor address beginning at 0h.</p>



4.1.3.2 FLREG1—Flash Region 1 (BIOS) Register (Flash Descriptor Records)

Memory Address: FRBA + 004h

Size: 32 bits

Bits	Description
31:29	Reserved
28:16	<p>Region Limit. This specifies bits 24:12 of the ending address for this Region.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Must be set to 0000h if BIOS region is unused (on Firmware hub) 2. Ensure BIOS region size is a correct reflection of actual BIOS image that will be used in the platform 3. Region limit address Bits[11:0] are assumed to be FFFh
15:13	Reserved
12:0	<p>Region Base. This specifies address bits 24:12 for the Region Base.</p> <p>Note: If the BIOS region is not used, the Region Base must be programmed to 1FFFh</p>

4.1.3.3 FLREG2—Flash Region 2 (Intel ME) Register (Flash Descriptor Records)

Memory Address: FRBA + 008h

Size: 32 bits

Bits	Description
31:29	Reserved
28:16	<p>Region Limit. This specifies bits 24:12 of the ending address for this Region.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Ensure size is a correct reflection of actual Intel ME firmware size that will be used in the platform 2. Region limit address Bits[11:0] are assumed to be FFFh
15:13	Reserved
12:0	<p>Region Base. This specifies address bits 24:12 for the Region Base.</p>

4.1.3.4 FLREG3—Flash Region 3 (GbE) Register (Flash Descriptor Records)

Memory Address: FRBA + 00Ch

Size: 32 bits

Bits	Description
31:29	Reserved
28:16	<p>Region Limit. This specifies bits 24:12 of the ending address for this Region.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The maximum Region Limit is 128KB above the region base. 2. If the GbE region is not used, the Region Limit must be programmed to 0000h 3. Region limit address Bits[11:0] are assumed to be FFFh
15:13	Reserved
12:0	<p>Region Base. This specifies address bits 24:12 for the Region Base.</p> <p>Note: If the GbE region is not used, the Region Base must be programmed to 1FFFh</p>



4.1.3.5 FLREG4—Flash Region 4 (Platform Data) Register (Flash Descriptor Records)

Memory Address: FRBA + 010h

Size: 32 bits

Bits	Description
31:29	Reserved
28:16	<p>Region Limit. This specifies bits 24:12 of the ending address for this Region.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. If PDR Region is not used, the Region Limit must be programmed to 0000h 2. Ensure BIOS region size is a correct reflection of actual BIOS image that will be used in the platform 3. Region limit address Bits[11:0] are assumed to be FFFh
15:13	Reserved
12:0	<p>Region Base. This specifies address bits 24:12 for the Region Base.</p> <p>Note: If the Platform Data region is not used, the Region Base must be programmed to 1FFFh</p>

4.1.4 Flash Descriptor Master Section

4.1.4.1 FLMSTR1—Flash Master 1 (Host CPU/ BIOS) (Flash Descriptor Records)

Memory Address: FMBA + 000h

Size: 32 bits

Bits	Description
31:24	<p>Master Region Write Access: Each bit [31:24] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses.</p> <p>Bit 23 is a don't care as the primary master always has read/write permission to it's primary region</p>
23:16	<p>Master Region Read Access: Each bit [23:16] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses.</p> <p>Bit 17 is a don't care as the primary master always read/write permission to it's primary region.</p>
15:0	<p>Requester ID: This is the Requester ID (Bus/Device/Function Number_ of the Host CPU</p> <p>For the host CPU, this should be set to Bus/Device/Function: 0/0/0</p>

4.1.4.2 FLMSTR2—Flash Master 2 (Intel® ME) (Flash Descriptor Records)

Memory Address: FMBA + 004h

Size: 32 bits

Bits	Description
31:24	<p>Master Region Write Access: Each bit [31:24] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses.</p> <p>Bit 26 is a don't care as the primary master always has read/write permission to it's primary region</p>
23:16	<p>Master Region Read Access: Each bit [23:16] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses.</p> <p>Bit 18 is a don't care as the primary master always read/write permission to it's primary region.</p>
15:0	<p>Requester ID: This is the Requester ID (Bus/Device/Function Number_ of the ME</p>



4.1.4.3 FLMSTR3—Flash Master 3 (GbE) (Flash Descriptor Records)

Memory Address: FMBA + 008h

Size: 32 bits

Bits	Description
31:24	<p>Master Region Write Access: Each bit [31:24] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses.</p> <p>Bit 27 is a don't care as the primary master always has read/write permission to it's primary region</p>
23:16	<p>Master Region Read Access: Each bit [23:16] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses.</p> <p>Bit 19 is a don't care as the primary master always read/write permission to it's primary region.</p>
15:0	Requester ID: This is the Requester ID (Bus/Device/Function Number_ of the GbE

4.1.5 PCH Softstraps

See *Appendix A* for Record descriptions and listings.

4.1.6 Descriptor Upper Map Section

4.1.6.1 FLUMAP1—Flash Upper Map 1 (Flash Descriptor Records)

Memory Address: FDBAR + EFCh

Size: 32 bits

Bits	Default	Description
31:16	0	Reserved
15:8	1	Intel ME VSCC Table Length (VTL). Identifies the 1s based number of DWORDS contained in the VSCC Table. Each SPI component entry in the table is 2 DWORDS long.
7:0	1	<p>Intel ME VSCC Table Base Address (VTBA). This identifies address bits [11:4] for the VSCC Table portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0.</p> <p>Note: VTBA should be above the offset for FMSBA+ 04h and below FLUMAP1. It is recommended that this address is set based on the anticipated maximum number of different flash parts entries.</p>

4.1.7 Intel® ME Vendor Specific Component Capabilities Table

Entries in this table allow support for a SPI flash part for Intel Management Engine capabilities including Intel® Active Management Technology . BIOS will still need to set up the proper VSCC registers for BIOS and Integrated Gigabit Ethernet usage.

Each VSCC table entry is composed of two 32 bit fields: JEDEC ID and the corresponding VSCC value.

See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) for information on how to program individual entries.



4.1.7.1 JID0—JEDEC-ID 0 Register (Flash Descriptor Records)

Memory Address: VTBA + 000h

Size: 32 bits

Bits	Description
31:24	Reserved
23:16	SPI Component Device ID 1. This field identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).
15:8	SPI Component Device ID 0. This field identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).
7:0	SPI Component Vendor ID. This field identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).

4.1.7.2 VSCCO—Vendor Specific Component Capabilities 0 (Flash Descriptor Records)

Memory Address: VTBA + 004h

Size: 32 bits

In this table “Lower” applies to characteristics of all flash space below the Flash Partition Boundary Address (FPBA). “Upper” applies to characteristics of all flash space above the FPBA.

Bits	Description
31:24	Lower Erase Opcode (LEO). This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
23:21	Reserved
20	<p>Lower Write Enable on Write Status (LWEWS).</p> <p>'0' = 50h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b.</p> <p>'1' = 06h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b.</p> <p>Note:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.



Bits	Description
19	<p>Lower Write Status Required (LWSR). No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
18	<p>Lower Write Granularity (LWG). 0 = 1 Byte 1 = 64 Byte</p>
17:16	<p>Lower Block/Sector Erase Size (LBES). This field identifies the erasable sector size for all Flash space below the flash partition boundary address. Valid Bit Settings: 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB</p>
15:8	<p>Upper Erase Opcode (UEO). This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.</p>
7:5	Reserved
4	<p>Upper Write Enable on Write Status (UWEWS). '0' = 50h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b. '1' = 06h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.



Bits	Description
3	<p>Upper Write Status Required (UWSR). No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. 2. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Intel Management Engine firmware performs. 4. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs 5. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
2	<p>Upper Write Granularity (UWG). 0 = 1 Byte 1 = 64 Bytes</p>
1:0	<p>Upper Block/Sector Erase Size (UBES). This field identifies the erasable sector size for all Flash components. 00 = 256 Bytes 01 = 4 K Bytes 10 = 8 K Bytes 11 = 64K Bytes</p>

4.1.7.3 JIDn—JEDEC-ID Register n (Flash Descriptor Records)

Memory Address: VTBA + (n*8)h

Size: 32 bits

Note: "n" is an integer denoting the index of the Intel ME VSCC table.

Bits	Description
31:24	Reserved
23:16	SPI Component Device ID 1. This field identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).
15:8	SPI Component Device ID 0. This field identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).
7:0	SPI Component Vendor ID. This field identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).



4.1.7.4 VSCCn—Vendor Specific Component Capabilities n (Flash Descriptor Records)

Memory Address: VTBA + 004h + (n*8)h

Size: 32 bits

Note: “n” is an integer denoting the index of the Intel ME VSCC table.

Note: In this table “Lower” applies to characteristics of all flash space below the Flash Partition Boundary Address (FPBA). “Upper” applies to characteristics of all flash space above the FPBA.

Bits	Description
31:24	Lower Erase Opcode (LEO). This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
23:21	Reserved
20	<p>Lower Write Enable on Write Status (LWEWS). '0' = 50h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b. '1' = 06h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
19	<p>Lower Write Status Required (LWSR). No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
18	<p>Lower Write Granularity (LWG). 0 = 1 Byte 1 = 64 Byte</p>



Bits	Description
17:16	<p>Lower Block/Sector Erase Size (LBES). This field identifies the erasable sector size for all Flash space below the flash partition boundary address.</p> <p>Valid Bit Settings:</p> <p>00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB</p>
15:8	<p>Upper Erase Opcode (UEO). This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.</p>
7:5	Reserved
4	<p>Upper Write Enable on Write Status (UWEWS).</p> <p>'0' = 50h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b. '1' = 06h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b.</p> <p>Note:</p> <ol style="list-style-type: none"> Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
3	<p>Upper Write Status Required (UWSR).</p> <p>No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
2	<p>Upper Write Granularity (UWG).</p> <p>0 = 1 Byte 1 = 64 Bytes</p>
1:0	<p>Upper Block/Sector Erase Size (UBES). This field identifies the erasable sector size for all Flash components.</p> <p>00 = 256 Bytes 01 = 4 K Bytes 10 = 8 K Bytes 11 = 64K Bytes</p>



4.2 OEM Section

Memory Address: F00h

Size: 256 Bytes

256 Bytes are reserved at the top of the Flash Descriptor for use by the OEM. The information stored by the OEM can only be written during the manufacturing process as the Flash Descriptor read/write permissions must be set to Read Only when the computer leaves the manufacturing floor. The PCH Flash controller does not read this information. FFh is suggested to reduce programming time.

4.3 Region Access Control

Regions of the flash can be defined from read or write access by setting a protection parameter in the Master section of the Descriptor. There are only three masters that have the ability to access other regions: CPU/BIOS, Intel ME Firmware, and GbE software/driver running on CPU.

Table 4-1. Region Access Control Table Options

Master Read/Write Access			
Region (#)	CPU and BIOS	ME/MCH	GbE Controller
Descriptor (0)	Read / Write	Read / Write	Read / Write
BIOS (1)	CPU and BIOS can always read from and write to BIOS region	Read / Write	Read / Write
ME (2)	Read / Write	ME can always read from and write to ME region	Read / Write
GbE (3)	Read / Write	Read / Write	GbE software can always read from and write to GbE region
PDR (4)	Read / Write	Read / Write	Read / Write

Note:

1. Descriptor and PDR regions are not masters, so they will not have Master R/W access.
2. Descriptor should NOT have write access by any master in production systems.
3. PDR region should only have read and/or write access by CPU/Host. GbE and ME should NOT have access to PDR region.



4.3.1 Intel Recommended Permissions for Region Access

The following Intel recommended read/write permissions are necessary to secure Intel Management Engine and Intel ME Firmware.

Table 4-2. Recommended Read/Write Settings for Platforms Using Intel® ME Firmware

Master Access	Descriptor Region Bit 0	ME Region Bit2	GbE Region Bit3	BIOS Region Bit1	PDR Region Bit4
ME read access	Y	Y	Y	N	N
ME write access	N	Y	Y	N	N
GbE read access	N	N	Y	N	N
GbE write access	N	N	Y	N	N
BIOS read access	Y	N	Y	Y	‡
BIOS write access	N	N	Y	Y	‡

Note:

1. ‡ = Host access to PDR is the discretion of the customer. Implementation of PDR is optional

The table below shows the values to be inserted into the Flash image tool. The values below will provide the access levels described in the table above.

Table 4-3. Recommended Read/Write Settings for Platforms Using Intel® ME Firmware (Cont'd)

	ME	GbE	BIOS
Read	0b 0000 1101 = 0x0d	0b 0000 1000 = 0x08	0b 000‡ 1011 = 0x‡B
Write	0b 0000 1100 = 0x0c	0b 0000 1000 = 0x08	0b 000‡ 1010 = 0x‡A

Notes:

1. ‡ = Value dependent on if PDR is implemented and if Host access is desired.

4.3.2 Overriding Region Access

Once access Intel recommended Flash settings have been put into the flash descriptor, it may be necessary to update the ME region with a Host program or write a new Flash descriptor.

Assert HDA_SDO low during the rising edge of PWROK to set the Flash descriptor override strap.

This strap should only be visible and available in manufacturing or during product development.

After this strap has been set you can use a host based flash programming tool like FPT.exe to write/read any area of serial flash that is not protected by Protected Range Registers. Any area of flash protected by Protected range Registers will still NOT be writable/readable.

See [5.3 SPI Protected Range Register Recommendations](#) for more details.



4.4 Intel® Management Engine (Intel® ME) Vendor-Specific Component Capabilities Table

The Intel ME VSCC Table defines how the Intel ME will communicate with the installed SPI flash. This table is defined in the descriptor and is the responsibility of who puts together the NVM image. LVSCC and/or UVSCC registers are defined in memory space and must be set by BIOS. This table must define every flash part that is intended to be used. The size (number of max entries) of the table is defined in [4.1.6.1 FLUMAP1—Flash Upper Map 1 \(Flash Descriptor Records\)](#). Each Table entry is made of two parts: the JEDEC ID and VSCC setting.

4.4.1 How to Set a JEDEC ID Portion of Intel® ME VSCC Table Entry

[7.3.2 Device ID](#) shows how to obtain the 3 byte JEDEC ID for the target SPI flash.

[6.4.1 Adding a New Table Entry](#) Shows how to set this value in FITC.

Table 4-4. Jidn - JEDEC ID Portion of Intel® ME VSCC Table

Bits	Description
31:24	Reserved.
23:16	SPI Component Device ID 1: This identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).
15:8	SPI Component Device ID 0: This identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).
7:0	SPI Component Vendor ID: This identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).

If using Flash Image Tool (FIT) refer to System Tools user guide in the Intel ME FW kit and the respective FW Bring up Guide on how to build the image. If not, refer to [4.1.6.1 FLUMAP1—Flash Upper Map 1 \(Flash Descriptor Records\)](#) thru [4.1.7.4 VSCCn—Vendor Specific Component Capabilities n \(Flash Descriptor Records\)](#)

4.4.2 How to Set a VSCC Entry in Intel® ME VSCC Table for Cougar Point Family Platforms

Lower VSCC (bits 31:16) needs to be programmed in instances where the Flash Partition Boundary is not 0x0. When using an asymmetric flash component (part with two different sets of attributes based on address) a Flash Partition Boundary will need to be used. This includes if the system is intended to support both symmetric AND asymmetric SPI flash parts. If all flash parts that will be used on this system are not asymmetric, and if all flash space has all the same attributes (not the same vendor or family), then only UVSCC (bits 15:0) needs to be populated.

It is advised that you program both LVSCC and UVSCC in order to support the widest range of flash components.

Refer to [4.4.3 Example Intel® ME VSCC Table Settings for Cougar Point Family Systems](#).



See text below the table for explanation on how to determine Management Engine VSCC value.

Table 4-5. Vsccn – Vendor-Specific Component Capabilities Portion of the Cougar Point Family Platforms

Bits	Description
31:24	Lower Erase Opcode (LEO) . This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
23:21	Reserved
20	<p>Lower Write Enable on Write Status (LWEWS). '0' = 50h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b. '1' = 06h will be the opcode used to unlock the status register on SPI flash if LWSR (bit 19) is set to 1b.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
19	<p>Lower Write Status Required (LWSR). No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 20 (LWEWS) and/or bit 19 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 19 (LWSR) and 20 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 1b and bit 20 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 19 (LWSR) is set to 0b and bit 20 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
18	<p>Lower Write Granularity (LWG). 0 = 1 Byte 1 = 64 Byte</p>
17:16	<p>Lower Block/Sector Erase Size (LBES). This field identifies the erasable sector size for all Flash space below the flash partition boundary address. Valid Bit Settings: 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB</p>
15:8	Upper Erase Opcode (UEO) . This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.



Table 4-5. Vscn – Vendor-Specific Component Capabilities Portion of the Cougar Point Family Platforms

Bits	Description
7:5	Reserved
4	<p>Upper Write Enable on Write Status (UWEWS). '0' = 50h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b. '1' = 06h will be the opcode used to unlock the status register on SPI flash if UWSR (bit 3) is set to 1b.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
3	<p>Upper Write Status Required (UWSR). No automatic write of 00h will be made to the SPI flash's status register) A write of 00h to the SPI flash's status register will be sent on EVERY write and erase performed by Intel ME to the SPI flash.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Intel Management Engine firmware performs. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Intel Management Engine firmware performs If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
2	<p>Upper Write Granularity (UWG). 0 = 1 Byte 1 = 64 Bytes</p>
1:0	<p>Upper Block/Sector Erase Size (UBES). This field identifies the erasable sector size for all Flash components. 00 = 256 Bytes 01 = 4 K Bytes 10 = 8 K Bytes 11 = 64K Bytes</p>

Upper and Lower Erase Opcode (LEO/UEO) and Upper and Lower Block/Sector Erase Size (LBSES/UBSES) should be set based on the flash part and the firmware on the platform. For Intel ME enabled platforms this should be 4 KB.

Either **Upper and Lower Write Status Required (LWSR and UWSR)** or **Upper Write Enable on Write Status (LWEWS and UWEWS)** should be set on flash devices that require an opcode to enable a write to the status register. Intel ME



Firmware will write a 00h to status register to unlock the flash part for every erase/write operation. If this bit is set on a flash part that has non-volatile bits in the status register then it may lead to pre-mature wear out of the flash.

- Set the **LWSR/UWSR** bit to 1b and **LWEWS/UWEWS** to 0b if the Enable Write Status Register opcode (50h) is needed to unlock the status register. Opcodes sequence sent to SPI flash will bit 50h 01h 00h.
- Set the **LWSR/UWSR** bit to 1b AND **LWEWS/UWEWS** bit to 1b if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h 01h 00h.
- Set the **LWSR/UWSR** bit to 0b AND **LWEWS/UWEWS** bit to 0b or 1b, if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h
- **LWSR/UWSR or LWEWS/UWEWS should be not be set on devices that use non volatile memory for their status register.** Setting this bit will cause operations to be ignored, which may cause undesired operation. Ask target flash vendor if this is the case for the target flash. See [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) and [5.2 Locking SPI Flash via Status Register](#) for more information.

Erase Opcode (EO) and **Block/Sector Erase Size (BES)** should be set based on the flash part and the firmware on the platform.

Write Granularity (WG) bit should be set based on the capabilities of the flash device. If the flash part is capable of writing 1 to 64 bytes (or more) with the 02h command you can set this bit 0 or 1. Setting this bit high will result in faster write performance. If flash part only supports single byte write only, then set this bit to 0.

Bit ranges 23:21 and 7:5 are reserved and should set to all zeros.

4.4.3 Example Intel® ME VSCC Table Settings for Cougar Point Family Systems

Below is a table that provides general guidelines for BIOS VSCC settings for different SPI flash devices. These settings are not part recommendations, nor are they an indication these parts are supported on Intel platforms. Flash parts may change opcodes and architectures so please refer to the respective flash datasheet and flash vendor to confirm.

Please refer to [4.4.2 How to Set a VSCC Entry in Intel® ME VSCC Table for Cougar Point Family Platforms](#) for requirements and how the below values were derived.

Vendor/ Family	Jedec Vendor ID	ME VSCC Table Entry	Upper Flash Erase	Lower Flash Erase	Notes
Atmel* AT25DFxxx or AT26DFxxx1	0x1F	0x20152015, or 0x201D201D	4 KB	4 KB	1, 4, 5
Macronix* MX25L	0xC2	0x20052005	4 KB	4 KB	1, 4
SST* 25VF	0xBF	0x20092009	4 KB	4 KB	1,2,4



Vendor/ Family	Jedec Vendor ID	ME VSCC Table Entry	Upper Flash Erase	Lower Flash Erase	Notes
Numonyx/ Micron* N25Q	0x20	0x20052005	4 KB	4 KB	1,3,4
Winbond* W25X	0xEF	0x20052005	4 KB	4 KB	1,4
Spansion* S25FLxxxK	0xEF	0x20052005	4 KB	4 KB	1,4
EON* EN25F/EN25Q	0x1c	0x20052005	4 KB	4 KB	1,4
AMIC* A25L	0x37	0x20052005	4 KB	4 KB	1,4
GigaDevice* GD25Q	0xC8	0x20052005	4 KB	4 KB	1,4

Note:

1. Upper 2 bytes of ME VSCC Table Entry is not necessary to program if Flash Partition Boundary is zero and flash is not asymmetric. For example: 0x00002005 instead of 0x20052005.
2. *Other names and brands may be claimed as the property of others.
3. Verify the Erase granularity as it may change with revision of flash part. 256 B erase is not supported in any Intel® ME Firmware.
4. Using 0x20012001, 0x20192019 or 0x20112011 will result in slower Intel® ME Firmware performance.
5. Both values are valid.







5 Configuring BIOS/GbE for SPI Flash Access

5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms

BIOS must account for any built in protection from the flash device itself. BIOS must ensure that any flash based protection will only apply to BIOS region only. It should not affect the ME or GbE regions.

All the SPI flash devices that meet the SPI flash requirements in the *Intel Cougar Cougar Point Family External Design Specification (EDS)* will be unlocked by writing a 00h to the SPI flash's status register. This command must be done via an atomic software sequencing to account for differences in flash architecture. Atomic cycles are uninterrupted in that it does not allow other commands to execute until a read status command returns a 'not busy' result from the flash.

Some flash vendors implement their status registers in NVM flash (non-volatile memory). This takes much more time than a write to volatile memory. During this write, the flash part will ignore all commands but a read to the status register (opcode 05h). The output of the read status register command will tell the PCH when the transaction is done.

Recommended flash unlocking sequence:

- Write enable (06h) command will have to be in the prefix opcode configuration register.
- The "write to status register" opcode (01h) will need to be an opcode menu configuration option.
- Opcode type for write to status register will be '01': a write cycle type with no address needed.
- The FDATA0 register should to be programmed to 0000 0000h.
- Data Byte Count (DBC) in Software Sequencing Flash Control register should be 000000b. Errors may occur if any non zero value is here.
- Set the Cycle Opcode Pointer (COP) to the "write to status register" opcode.
- Set to Sequence Prefix Opcode Pointer (SPOP) to Write Enable.
- Set the Data Cycle (DS) to 1.
- Set the Atomic Cycle Sequence (ACS) bit to 1.
- To execute sequence, set the SPI Cycle Go bit to 1.

Please see the [Serial Peripheral Interface Memory Mapped Configuration Registers](#) in the *Intel Cougar Point Family External Design Specification (EDS)* more detailed information.



5.2 Locking SPI Flash via Status Register

Flash vendors that implement their status register with non-volatile memory can be updated a limited number of times. This means that this register may wear out before the desired endurance for the rest of the flash. It is highly recommended that BIOS vendors and customers do NOT use the SPI flash's status register to protect the flash in multiple master systems.

BIOS should try to minimize the number of times that the system is locked and unlocked.

Care should be taken when using status register based SPI flash protection in multiple master systems such as Management Engine firmware and/or integrated GbE. BIOS must ensure that any flash based protection will only apply to BIOS region only. It should affect not the ME or GbE regions.

Please contact your desired flash vendor to see if their status register protection bits are volatile or non-volatile. Flash parts implemented with volatile systems do not have this concern.

5.3 SPI Protected Range Register Recommendations

The PCH has a mechanism to set up to 5 address ranges from HOST access. These are defined in PR0, PR1, PR2, PR3 and PR4 in the PCH EDS. These address ranges are NOT unlocked by assertion of Flash descriptor Override.

It is strongly recommended to use a protected range register to lock down the factory default portion of Intel® ME Ignition Firmware region. The runtime portion should be left unprotected as to allow BIOS to update it.

It is strongly recommended that if Flash Descriptor Override strap (which can be checked by reading **FDOPSS (0b Flash Descriptor override is set, 1b not set) in PCH memory space (SPIBAR+4h bit 13)**) is set, do not set a Protected range to cover the Intel ME Ignition FW factory defaults. This would allow a flashing of a complete image when the Flash descriptor Override strap is set.

5.4 Software Sequencing Opcode Recommendations

It is strongly recommended that the "9Fh" JEDEC ID be used instead of "90h" or "AB". The JEDEC ID Council ensures that every SPI flash model is unique. There are flash vendors that have flash parts of different sizes that report out the same value using the "90h" opcode.

Intel utilities such as the Flash Programming tool will incorrectly detect the flash part in the system and it may lead to undesired program operation.

Intel Flash Programming tool requires the following software sequencing opcodes to be programmed in the OPMENU and corresponding OPTYPE register.

It is strongly recommended that you do not program opcodes write enable commands into the OPMENU definition. These should be programmed in the PREOP register.



Order of the opcodes is not important, but the OPMENU and OPTYPE do have to correspond. see [OPTYPE— Opcode Type Configuration Register](#) [OPMENU— Opcode Menu Configuration Register](#) in the *Intel Cougar Point Family External Design Specification (EDS)*.

Table 5-1. Recommended opcodes for FPT operation

Function	OPMENU	OPTYPE
Write to Status Register	0x01	'01'
Program Data	0x02	'11'
Read Data	0x03	'10'
Read Status Register	0x05	'00'
4 KB Erase	0x20	'11'
JEDEC ID	0x9F	'00'

Table 5-2. Recommended opcodes for FPT operation

Function	PREOP
Write Enable	0x06
Enable Status Register Write	0x50

5.5 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits

5.5.1 Flash Configuration Lockdown

It is strongly recommended that BIOS sets the Host and GbE **Flash Configuration Lock-Down (FLOCKDN)** bits (located at SPIBAR + 04h and MBAR +04h respectively) to '1' on production platforms. If these bits are not set, it is possible to make register changes that can cause undesired host, integrated GbE and Intel® ME functionality as well as lead to unauthorized flash region access.

Refer to [HSFS— Hardware Sequencing Flash Status Register](#) in the [Serial Peripheral Interface Memory Mapped Configuration Registers](#) section and [HSFS— Hardware Sequencing Flash Status Register](#) in the [GbE SPI Flash Programming Registers](#) section in the *Intel Cougar Point Family External Design Specification (EDS)*.

5.5.2 Vendor Component Lock

It is strongly recommended that BIOS sets the **Vendor Component Lock (VCL)** bits. These bits are located in the BIOS/GbE LVSCC registers. VCL applies the lock to both LVSCC and UVSCC even if LVSCC is not used. Without the VCL bits set, it is possible to make Host/GbE VSCC register(s) changes in that can cause undesired host and integrated GbE SPI flash functionality.

Refer to [LVSCC— Lower Vendor Specific Component Capabilities Register](#) in the *Intel Cougar Point Family External Design Specification (EDS)* for more information.



5.6 Host Vendor Specific Component Control Registers (LVSCC and UVSCC) for Cougar Point Family Systems

LVSCC and UVSCC are memory mapped registers are used by the PCH when BIOS or Integrate LAN reads, programs or erases the SPI flash via Hardware sequencing.

All SPI flash address space above or equal to the Flash Partition Boundary Address (FPBA) that is in the Flash Partition Boundary Register (FLPB) utilizes the UVSCC register for flash access. All SPI flash address space below what is defined as the Flash Partition Boundary Address (FPBA) uses the LVSCC register for flash access.

If SPI flash space has only one set of attributes, UVSCC needs to be set. In addition, the Flash Partition Boundary Address in the FLPB in the descriptor must be set to all 0's. The bit definitions for UVSCC and LVSCC are identical, they just apply to different areas of SPI flash space.

Refer to [LVSCC— Lower Vendor Specific Component Capabilities Register](#) and [UVSCC— Upper Vendor Specific Component Capabilities Register](#) in the *Intel Cougar Point Family External Design Specification (EDS)*.

See text below the tables for explanation on how to determine LVSCC and UVSCC register values.

Table 5-3. LVSCC - Lower Vendor-Specific Component Capabilities Register

Bit	Description
31:24	Reserved
23	Vendor Component Lock (VCL): — RW/L: '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. This bit applies to both UVSCC and LVSCC registers. All bits locked by (VCL) will remained locked until a global reset.
22:16	Reserved
15:8	Lower Erase Opcode (LEO) — RW: This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (VCL) bit.
7:5	Reserved



Table 5-3. LVSCC - Lower Vendor-Specific Component Capabilities Register

Bit	Description
4	<p>Lower Write Enable on Write Status (LWEWS) — RW:</p> <p>'0' = 50h will be the opcode used to unlock the status register on the SPI flash if LWSR (bit 3) is set to 1b.</p> <p>'1' = 06h will be the opcode used to unlock the status register on the SPI flash if LWSR (bit 3) is set to 1b.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (LWEWS) and/or bit 4 (LWSR) should not be set to 1b if there are non volatile bits in the SPI flash device's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the flash part. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (LWSR) and 4 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Processor or Intel GbE FW performs. If bit 3 (LWSR) is set to 1b and bit 4 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs. If bit 3 (LWSR) is set to 0b and bit 4 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
3	<p>Lower Write Status Required (LWSR) — RW:</p> <p>'0' = No automatic write of 00h will be made to the SPI flash's status register.</p> <p>'1' = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash performed by Host and GbE.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> Bit 3 (LWEWS) and/or bit 4 (LWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. If both bits 3 (LWSR) and 4 (LWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Processor or Intel GbE FW performs. If bit 3 (LWSR) is set to 1b and bit 4 (LWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs. If bit 3 (LWSR) is set to 0b and bit 4 (LWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
2	<p>Lower Write Granularity (LWG) — RW:</p> <p>0: 1 Byte</p> <p>1: 64 Byte</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature in page writable SPI flash.
1:0	<p>Lower Block/Sector Erase Size (LBES)— RW: This field identifies the erasable sector size for all Flash components.</p> <p>Valid Bit Settings:</p> <p>00: 256 Byte</p> <p>01: 4 KByte</p> <p>10: 8 KByte</p> <p>11: 64 K</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.</p>



Lower Erase Opcode (LEO) and **Lower Block/Sector Erase Size (LBSES)** should be set based on the flash part and the firmware image on the platform.

Either **Lower Write Status Required (LWSR)** OR **Lower Write Enable on Write Status (LWEWS)** should be set on flash devices that require an opcode to enable a write to the status register. BIOS and GbE will write a 00h to status register to unlock the flash part for every erase/write operation. If this bit is set on a flash part that has non-volatile bits in the status register then it may lead to pre-mature wear out of the flash and may result in undesired flash operation.

- Set the **LWSR** bit to 1b and **LWEWS** to 0b if the Enable Write Status Register opcode (50h) is needed to unlock the status register. Opcodes sequence sent to SPI flash will bit 50h 01h 00h.
- Set the **LWSR** AND **LWEWS** bit to 1b if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h 01h 00h.
- Set the **LWSR** bit to 0b AND **LWEWS** bit to 0b/1b if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h.
- **LWSR or LWEWS should be not be set on devices that use non volatile memory for their status register.** Setting this bit will cause operations to be ignored, which may cause undesired operation. Ask target flash vendor if this is the case for the target flash. See [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) and [5.2 Locking SPI Flash via Status Register](#) for more information.
- **Lower Write Granularity (LWG)** bit should be set based on the capabilities of the flash device. If the flash part is capable of writing 1 to 64 bytes (or more) with the 02h command you can set this bit 0 or 1. Setting this bit high will result in faster write performance. If flash part only supports single byte write only, then set this bit to 0. Setting this bit high requires that BIOS ensure that no multiple byte write operation does not cross a 256 Byte page boundary, as it will have unintended results. This is a feature of page programming capable flash parts.

Vendor Component Lock (VCL) should remain unlocked during development, but locked in shipping platforms. When **VCL** and **FLOCKDN** are set, it is possible that you may not be able to use in system programming methodologies including Intel Flash Programming Tool if programmed improperly. It will require a system reset to unlock this register and BIOS not to set this bits. See [5.5 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits](#) for more details.

Bit ranges 31:24 and 22:16 and 7:5 are reserved and should set to all zeros.



See table below for explanation on how to set bits.

Table 5-4. UVSCC - Upper Vendor Specific Component Capabilities Register

Bit	Description
31:16	Reserved
15:8	<p>Upper Erase Opcode (UEO)— RW: This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (VCL) bit.</p>
7:5	Reserved
4	<p>Upper Write Enable on Write to Status (UWEWS) — RW: '0' = 50h will be the opcode used to unlock the status register if UWSR (bit 3) is set to 1b. '1' = 06h will be the opcode used to unlock the status register if UWSR (bit 3) is set to 1b.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to 1b if there are non volatile bits in the SPI flash device's status register. This may lead to premature flash wear out. 2. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the flash part. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Processor or Intel GbE FW performs. 4. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs. 5. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.



Table 5-4. UVSCC - Upper Vendor Specific Component Capabilities Register

Bit	Description
3	<p>Upper Write Status Required (UWSR) — RW:</p> <p>'0' = No automatic write of 00h will be made to the SPI flash's status register '1' = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash performed by Host and GbE.</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Bit 3 (UWEWS) and/or bit 4 (UWSR) should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. 2. This is not an atomic (uninterrupted) sequence. The PCH will not wait for the status write to complete before issuing the next command, potentially causing SPI flash instructions to be disregarded by the SPI flash part. If the SPI flash component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. If both bits 3 (UWSR) and 4 (UWEWS) are set to 1b, then sequence of 06h 01h 00h is sent to unlock the flash on EVERY write and erase that Processor or Intel GbE FW performs. 4. If bit 3 (UWSR) is set to 1b and bit 4 (UWEWS) is set to 0b then sequence of 50h 01h 00h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs 5. If bit 3 (UWSR) is set to 0b and bit 4 (UWEWS) is set to 0b or 1b then sequence of 60h is sent to unlock the SPI flash on EVERY write and erase that Processor or Intel GbE FW performs.
2	<p>Upper Write Granularity (UWG) — RW:</p> <p>0: 1 Byte 1: 64 Byte</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature in page writeable SPI flash.</p>
1:0	<p>Upper Block/Sector Erase Size (UBES)— RW: This field identifies the erasable sector size for all Flash components.</p> <p>Valid Bit Settings:</p> <p>00: 256 Byte 01: 4 KByte 10: 8 KByte 11: 64 K</p> <p>This register is locked by the Vendor Component Lock (VCL) bit.</p> <p>Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.</p>

Upper Erase Opcode (UEO) and **Upper Block/Sector Erase Size (UBSES)** should be set based on the flash part and the firmware on the platform.

Either **Upper Write Status Required (UWSR)** or **Upper Write Enable on Write Status (UWEWS)** should be set on flash devices that require an opcode to enable a write to the status register. BIOS and GbE will write a 00h to the SPI flash's status register to unlock the flash part for every erase/write operation. If this bit is set on a flash part that has non-volatile bits in the status register then it may lead to pre-mature wear out of the flash and may result in undesired flash operation.

- Set the **UWSR** bit to 1b and **UWEWS** to 0b if the Enable Write Status Register opcode (50h) is needed to unlock the status register. Opcodes sequence sent to SPI flash will bit 50h 01h 00h.



- Set the **UWSR** bit to 1b AND **UWEWS** bit to 1, if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h 01h 00h.
- Set the **UWSR** bit to 0b AND **UWEWS** bit to 0b or 1b, if write enable (06h) will unlock the status register. Opcodes sequence sent to SPI flash will bit 06h
- **UWSR or UWEWS should be not be set on devices that use non volatile memory for their status register.** Setting this bit will cause operations to be ignored, which may cause undesired operation. Ask target flash vendor if this is the case for the target flash. See [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) and [5.2 Locking SPI Flash via Status Register](#) for more information.

Upper Write Granularity (UWG) bit should be set based on the capabilities of the flash device. If the flash part is capable of writing 1 to 64 bytes (or more) with the 02h command you can set this bit 0 or 1. Setting this bit high will result in faster write performance. If flash part only supports single byte write only, then set this bit to 0. Setting this bit high requires that BIOS ensure that no multiple byte write operation does not cross a 256 Byte page boundary, as it will have unintended results. This is a feature of page programming capable flash parts. **Bit ranges 31:16 and 7:5** are reserved and should set to all zeros.

5.7 Example Host VSCC Register Settings for Cougar Point Family Systems

Below is a table that provides general guidelines for BIOS VSCC settings for different SPI flash devices. These settings are not part recommendations, nor are they an indication these parts are supported on Intel platforms. Flash parts may change opcodes and architectures so please refer to the respective flash datasheet and flash vendor to confirm.

** Please refer to [3 PCH SPI Flash Compatibility Requirement](#) and [5.4 Software Sequencing Opcode Recommendations](#), [5.6 Host Vendor Specific Component Control Registers \(LVSCC and UVSCC\) for Cougar Point Family Systems](#) for requirements and how the below values were derived.

Vendor/Family	Jedec Vendor ID	UVSCC	LVSCC	Upper Flash Erase	Lower Flash Erase	Notes
Atmel* AT25DFxxx or AT26DFxxx1	0x1F	0x2015 (mbw), 0x2011 (sbw) or 0x201D (mbw), 0x2019 (sbw)	0x802015 (mbw), 0x802011 (sbw), or 0x80201D (mbw), 0x802019 (sbw)	4 KB	4 KB	1,4,5,6,7,8
Macronix* MX25L	0xC2	0x2005 (mbw) or 0x2001 (sbw)	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8
SST* 25VF	0xBF	0x2009	0x802009	4 KB	4 KB	1,2,4,6



Vendor/Family	Jedec Vendor ID	UVSCC	LVSCC	Upper Flash Erase	Lower Flash Erase	Notes
Numonyx/Micron N25Q	0x20	0x2005 (mbw) or 0x2001 (sbw)	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,3,4,5,6,8
Winbond* W25X / W25Q	0xEF	0x2005 (mbw) or 0x2001 (sbw)	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8
Spansion* S25FLxxxK	0xEF	0x20052005	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8
EON* EN25F/EN25Q	0x1c	0x2005	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8
AMIC* A25L	0x37	0x2005	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8
GigaDevice* GD25Q	0xC8	0x2005	0x802005 (mbw) or 0x802001 (sbw)	4 KB	4 KB	1,4,5,6,8

Notes:

1. It is not necessary to program LVSCC if the Flash Partition boundary is 0x0.
2. *Other names and brands may be claimed as the property of others.
3. Verify the Erase granularity as it may change with different revisions of flash part. 256 B erase is not supported in any Intel® ME Firmware.
4. Flash performance may improve with larger erase granularity settings in BIOS only platforms.
5. Use sbw setting if BIOS does not prevent the writing across 256 Byte page boundaries with multiple byte writes.
6. It is strongly recommended to set bit 23 of LVSCC on shipping platforms. See [5.5.2 Vendor Component Lock](#) for more details.
7. When using values of 0x2015, 0x2011, 0x802015, and/or 0x802011 you must unlock the status register. See [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) for details
8. mbw = multiple byte write capable. sbw = single byte write capable.





6 Flash Image Tool

This is a general overview to the Flash Image Tool (FIT). Please refer to the documentation that comes with the flash tools executables for the correct feature set for the version of the flash tool being used.

The purpose of the Flash Image Tool is to simplify the creation and configuration of the Flash image for the Intel Cougar Point family platforms. The Flash Image Tool makes a flash image by creating a descriptor and combining the following image files:

- BIOS
- Intel Integrated Gigabit LAN
- Intel ME Firmware
- Platform Data Region

The user is able to manipulate the image layout through a graphical user interface (GUI) and change the various chipset parameters to match the target hardware. Different configurations can be saved to a file so image layouts do not need to be recreated each time.

The user does not need to interact with the GUI each time they need to create an image. The tool supports a set of command line parameters that can be used to build an image from the command prompt or from a makefile. A previously stored configuration can be used to define the image layout, making interacting with the GUI unnecessary.

The Flash Image Tool does not program the flash. The Flash Image tool only generates a binary image file. This image must be burned onto the flash by other means.

6.1 Flash Image Details

A flash image is composed of five regions. The locations of these regions are referred to in terms of where it can be found within the total memory of the flash.

Figure 6-1. Firmware Image Components

Descriptor	ME FW	GbE	PDR	BIOS
------------	-------	-----	-----	------

- **Descriptor:** Takes up a fixed amount of space at the beginning of flash memory. The descriptor contains information such as space allocated for each region of the flash image, read-write permissions for each region, and a space which can be used for vendor-specific data.
- **ME FW:** Required region that contains code and configuration data for ME functions such as ME Clock control, Intel® Active Management Technology (Intel® AMT), etc.
- **GbE:** Optional region that contains code and configuration data for Intel integrated Gigabit Ethernet and 10/100 Ethernet.
- **Platform Data Region:** Optional region that contains data reserved for BIOS/Host usage.
- **BIOS:** Optional region that contains code and configuration for the entire platform. Region is only optional if BIOS is on Firmware Hub.

6.1.1 Flash Space Allocation

FIT/Ftoolc allocates SPI flash space allocation for each region as follows:

1. Each region can be assigned a fixed amount of space. If no fixed space is assigned, then the region occupies only as much space as it requires.
2. If after allocation for all regions there is still space left in flash, then the ME region expands to fill the remaining space.
3. If there is leftover space and the ME region is not implemented, then the BIOS region is expands to use the remaining space.

If there is leftover space and the BIOS region is not implemented, then the GbE region is expands to contain the remaining space.

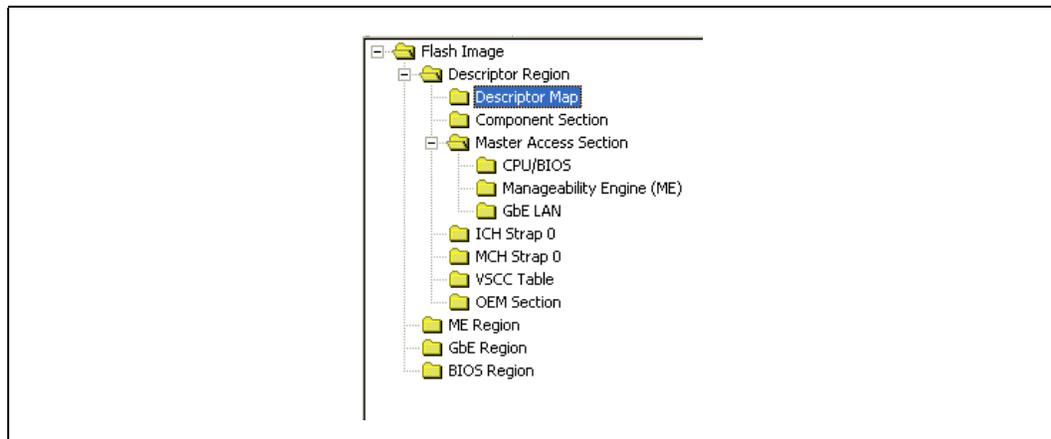
6.2 Modifying the Flash Descriptor Region

The flash descriptor region contains information about the flash image and the target hardware. It is important for this region to be configured correctly or else the target system may not function as desired.

6.2.1 Setting the Number and Size of the Flash Components

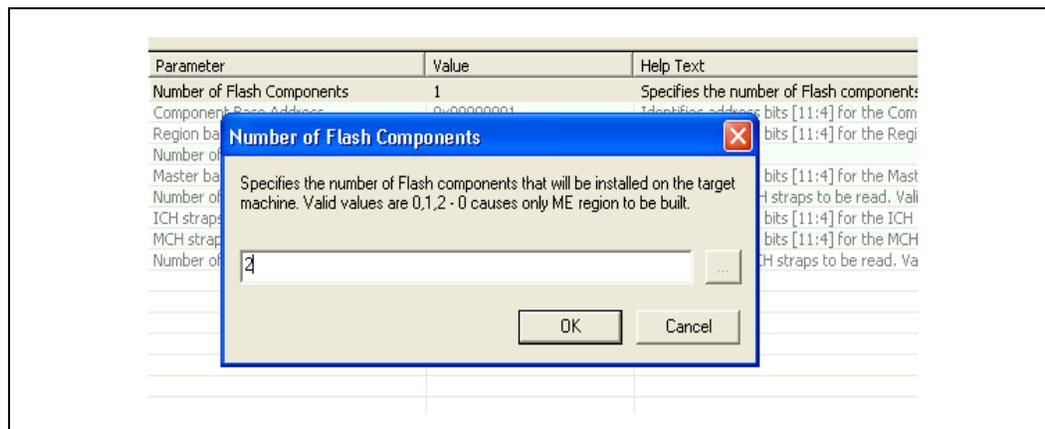
To set the number of flash components, expand the “Descriptor Region” node in the tree on the left side of the main window. Then, select the “Descriptor Map” node (See 3). All of the parameters for the descriptor map section will appear in the list on the right side of the main window.

Figure 6-2. Editable Flash Image Region List



Double-click the list item named “Number of Flash Components” (See Section 6.3). A dialog will appear allowing the user to enter the number of flash components (valid values are 1 or 2). Click “Ok” to update the parameter.

Figure 6-3. Descriptor Region – Descriptor Map Options



Some SPI flash devices support both standard and fast read opcodes. Fast reads are able to operate at faster frequencies than the regular reads. For PCH to support these faster read commands, fast read support must be set to true. For Cougar Point, this should be set to 50 MHz for Intel AMT enabled platforms.

Figure 6-4. Descriptor Region – Fast Read Support Options

Read ID and Read Status clock frequency	20MHz	If more than one Flash component exists, this field must be th
Write and erase clock frequency	20MHz	If more than one Flash component exists, this field must be th
Fast read clock frequency	33MHz	This field is undefined if the Fast Read Support is set to false.
Fast read support	true	Enables/disables "Fast Read" support.
Read clock frequency	20MHz	Sets the Flash read frequency
Flash component 1 density	512KB	This field identifies the size of the 1st Flash component.
Flash component 2 density	512KB	This field identifies the size of the 2nd Flash component.
Illegal Instruction 0	0	Op-code for an illegal instruction that the Flash Controller sho
Illegal Instruction 1	0	Op-code for an illegal instruction that the Flash Controller sho
Illegal Instruction 2	0	Op-code for an illegal instruction that the Flash Controller sho
Illegal Instruction 3	0	Op-code for an illegal instruction that the Flash Controller sho

To set the size of each flash component, expand the "Descriptor Region" tree node and select the "Component Section" node. The parameters "Flash component 1 density" and "Flash component 2 density" specify the size of each flash component. Double-click on each parameter and select the correct component size from the drop-down list. Click "OK" to update the parameters.

Note: The size of the second flash component will only be editable if the number of flash components is set to 2.

Figure 6-5. Descriptor Region - Component Section Options

Parameter	Value	Help Text
Read ID and Read Status clock frequ...	20MHz	If more that one Flash component exists, this f
Write and erase clock frequency	20MHz	If more that one Flash component exists, this f
Fast read clock frequency	33MHz	This field is undefined if the Fast Read Support
Fast read support	true	Enables/disables "Fast Read" support.
Read clock frequency	20MHz	Sets the Flash read frequency
Flash component 1 density	2MB	This field identifies the size of the 1st Flash cor
Flash component 2 density	2MB	This field identifies the size of the 2nd Flash cor
Illegal Instruction 0	0	Op-code for an illegal instruction that the Flash
Illegal Instruction 1	0	Op-code for an illegal instruction that the Flash
Illegal Instruction 2	0	Op-code for an illegal instruction that the Flash
Illegal Instruction 3	0	Op-code for an illegal instruction that the Flash

The Upper and Lower Flash Erase sizes and Flash Partition Boundary address is not editable from this view. In order to modify these entries you must enter the Build Settings dialog box. Note that Assymmetric flash parts are no longer supported.

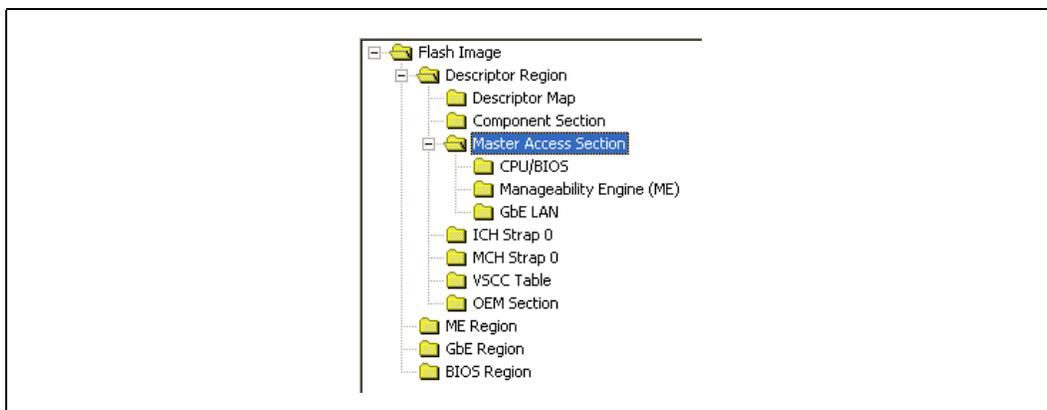
Figure 6-6. Descriptor Region – Flash partition Boundary Address and Upper and Lower Flash Erase Size.

Parameter	Value	Help Text
Read ID and Read Status clock frequ...	20MHz	If more that one Flash component exists, this field must be the lowest commo...
Write and erase clock frequency	20MHz	If more that one Flash component exists, this field must be the lowest commo...
Fast read clock frequency	20MHz	This field is undefined if the Fast Read Support is set to false,
Fast read support	false	Enables/disables Fast Read support.
Read clock frequency	20MHz	Sets the Flash read frequency
Flash component 1 density	2MB	This field identifies the size of the 1st Flash component.
Flash component 2 density	2MB	This field identifies the size of the 2nd Flash component.
Illegal Instruction 0	0	Op-code for an illegal instruction that the Flash Controller should protect again...
Illegal Instruction 1	0	Op-code for an illegal instruction that the Flash Controller should protect again...
Illegal Instruction 2	0	Op-code for an illegal instruction that the Flash Controller should protect again...
Illegal Instruction 3	0	Op-code for an illegal instruction that the Flash Controller should protect again...
Upper Flash Erase Size	0x000000	For Asymmetric flash parts, this is the upper of the two erase sizes.
Lower Flash Erase Size	0x000000	For Asymmetric flash parts, this is the lower of the two erase sizes.
Flash Partition Boundary	0x00000000	For Asymmetric flash parts, this is address bits[24:12] of the boundary that lo...

Region Access Control

In the Flash Image Tool these access values can be set by selecting the "Descriptor Region" tree node and selecting "CPU/BIOS" under "Master Access Section".

Figure 6-7. Region Access Control





The read and write access hexadecimal values can be specified in the appropriate parameters.

Figure 6-8. Descriptor Region – Master Access Section Options

Parameter	Value	Help Text
PCI Bus ID	0	
PCI Device ID	0	
PCI Function ID	0	
Read access	0x00	Each bit corresponds to Regions [7:0]. If the bit is set, read access is locked for that region.
Write access	0x00	Each bit corresponds to Regions [7:0]. If the bit is set, write access is locked for that region.

See [Section 4.3](#) for more information.

The following is the minimum set of the read/write parameters. This sample will lock down descriptor region with a necessary level of security for Management Engine enabled systems. The settings below will lock the flash region and prevent any future changes to the flash device. This includes any changes made via the fixed offset variable mechanism. If using the fixed offset variable mechanism, manufacturers can alternatively lock the descriptor region during manufacturing. By locking the descriptor region late in the manufacturing flow, the manufacturer has more flexibility in the programming of the flash device. As stated above, once the region is locked, changes to the flash device will be more difficult.

6.3 PCH Soft Straps

These sections contain configuration options for the PCH. The number of Soft Strap sections and their functionality differ based on the target PCH. Please refer to Appendix A and the respective FW Bringup Guide.

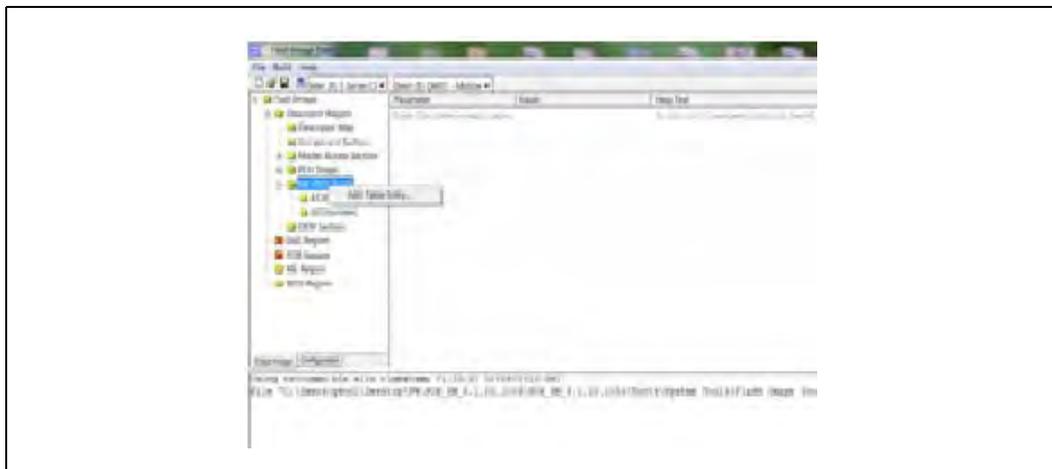
6.4 Management Engine VSCC Table

This section is used to store information to setup flash access for ME. This does not have any effect on the usage of the Flash programming Tool (FPT) if the information in this section is incorrect, the Intel ME Firmware may not communicate with the flash device. See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) This information provided is dependent on the flash device used on the system. for more information. Please contact your flash vendor for information on the specific SPI flash device.

6.4.1 Adding a New Table Entry

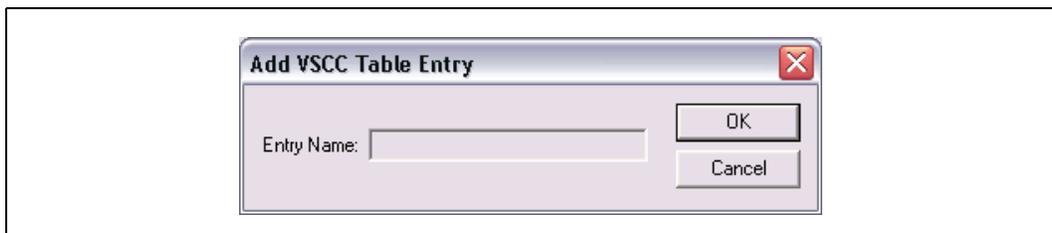
To add a new table, right click on VSCC table and select add a new table entry.

Figure 9. Add New VSCC Table Entry



The program will then prompt the user for a table entry name. To avoid confusion it is recommended that each table entry be unique. FITc will not create an error message for table entries that have the same name.

Figure 10. Add VSCC Table Entry



After a table entry has been added, the user will be able to fill in values for the flash device. The values in the VSCC table are provided by your flash vendor. The information in the VSCC table entry is similar to information that is displayed in the `fparts.txt` file from the Flash Programming tool. See [7.2 Fparts.txt File](#) for information on how to set the Vendor ID, Device ID 0 and Device ID 1 (three components of JEDEC ID) See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) for more detailed information on how to set the VSCC register value.





7 Flash Programming Tool

This is a general overview to the Flash Programming Tool (FPT). Please refer to the documentation that comes with the flash tools executables for the correct feature set for the version of the flash tool being used.

The purpose of the Flash Programming Tool is to program an image file to the flash. The Flash Programming Tool can program the following “regions”, in the form of binary files, into flash:

- Descriptor
- BIOS
- Gigabit Ethernet
- Intel Management Engine
- Platform Data Region

This tool can program an individual region, or the entire flash device.

7.1 BIOS Support

FPT requires proper opcodes programmed if the FLOCKDN bit is set. Please refer to [5.4 Software Sequencing Opcode Recommendations](#) and [5.3 SPI Protected Range Register Recommendations](#) for more details.

7.2 Fparts.txt File

This text file contains a list of all flash devices that this tool supports. If the flash device is not listed below the user will receive the following error:

```
Flash Programming Tool. Version X.X.X  
--- Flash Devices Found ---  
>>> Error: There is no supported SPI flash device installed!
```

If the device is not located in the fparts.txt file, the user is expected to provide information about their device and insert the values into the file using the same format as the rest of the devices. The description and order of the fields is listed below:

1. Display name
2. Device ID (2 or 3 bytes)
3. Device Size (in bits)
4. Block Erase Size (in bytes - 256, 4K, 64K)
5. Block Erase Command
6. Write Granularity (1 or 64)
7. Unused
8. Chip Erase Command



7.3 Configuring a Fparts.txt Entry

This section shows how to add support for a flash device for the Flash Programming Tool (fpt.exe/fptw.exe).

Each valid entry in the fparts.txt is comma delineated and has the following fields:

1. Display name
2. Device ID (2 or 3 bytes)
3. Device Size (in bits)
4. Block Erase Size (in bytes - 256, 4K, 64K)
5. Block Erase Command
6. Write Granularity (1 or 64)
7. Enable Write status (50h opcode required to unlock status register)
8. Chip Erase Command

7.3.1 Display Name

This is a user defined field that FPT will display on the screen to describe that flash part. It is recommended to use the part number to ensure unique and identifiable entry.

7.3.2 Device ID

This is how the flash programming tool identifies a flash part. FPT cycles through three opcodes in order to find a matching entry: JEDEC ID (9Fh), Read ID (90h or ABh) JEDEC ID is a three byte sequence which the industry standard opcode and is guaranteed to be unique to each part number.

When looking in the SPI flash's datasheet for the JEDEC device ID, look for the 9Fh opcode and look for the 3 byte output of that opcode. If there is more than 3 bytes described, just use the first 3 bytes. JEDEC ID, manufacturer ID and Read ID are other keywords to search for.

In parts where JEDEC ID is not available, look for the 2 byte output of 90h or ABh. Read ID is the most common description for this attribute. Read ID is not guaranteed to be unique between different part numbers from the same manufacturer.

7.3.3 Device Size (in Bits)

This defines the size of flash space for the flash programming tool. This value is the size of the flash in bits in hexadecimal (0x) notation.

For example: 8 Mb part = $(8 * 1024 * 1024) = (8,388,608)$ convert to hex \Rightarrow 0x800000.

7.3.4 Block Erase Size (in Bytes - 256B, 4K, 64K)

This tells FPT how to properly configure PCH family parts to set the correct erase granularity, or in other words how big of a block gets erased at a time. This value is limited by the flash part and the PCH SPI controller: 256 B, 4 KB or 64 KB.

The SPI flash's data sheet will tell what erase granularity is supported.



For Cougar Point Platforms the only granularity supported will be 4 KB.

This field is notated in hexadecimal notation. The choices for this field are: 0x100, 0x1000 (default), or 0x10000.

7.3.5 Block Erase Command

This field is the erase command opcode that FPT will use. After the Block Erase size is chosen, use the corresponding opcode in this field. This is a one byte opcode in hexadecimal notation.

For example: 0x20 if the opcode is 20h.

7.3.6 Write Granularity (1 or 64)

This field dictates how many bytes will be written for each write command.

The Cougar Point only supports 1 or 64 B writes. Flash devices that allow writes more than a single byte at a time usually support up to 256 bytes at a time. Look to see how many bytes the 02h opcode can support.

64 B has much better write performance, but if any issues are noted, set this field to 1 B write.

This field is in decimal notation. The choices for this field are: 1 or 64.

7.3.7 Enable Write Status /Unused

Legacy flash parts may only be able to use 50h opcode in order to unlock the status register. Unlocking the status register is described in detail in section [5.1 Unlocking SPI Flash Device Protection for Cougar Point Family Platforms](#) This bit should not be set for most flash parts, only those that do not support 06h opcode for unlocking the status register.

7.3.8 Chip Erase Command

This command is the one that is used to erase the entire flash part when FPT is used with the /c option. This field is in hexadecimal notation.

Example: 0xC7

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8 SPI Flash Programming Procedures

This chapter assumes the use of Intel flash tools: Flash Programming Tool and Flash Image Tool (FPT and FIT/ftoolc).

8.1 Updating BIOS

If the target system does not have a have a working BIOS and no alternate method of booting (for example: FWH) then you must use a third-party, out-of-system programmer.

8.1.1 Updating BIOS in Descriptor Mode

If updating BIOS in a system where the BIOS region is defined in the descriptor, you can use the following command:

```
C:\ fpt /f <file> /bios
```

If unsure that descriptor or the BIOS region is not defined, use `fpt /i`. Make sure that the descriptor is valid and that BIOS region is large enough to accommodate the intended image.

8.1.2 Updating BIOS in Non-Descriptor Mode

A BIOS-only image without a descriptor is not a valid production option for Cougar Point based platforms. See the *Intel Cougar Point Family External Design Specification (EDS)* for all the features of descriptor mode.

Unless there is a descriptor, the PCH family parts automatically look for the rest vector on the top of the flash's address space on chip select 0. If the BIOS is not programmed in this location, the system will not boot. Programming can be performed either in system with FPT or with a third-party programmer.

Example 8-1. 1-MByte BIOS Image (1MB.bin), 2 MByte SPI Flash on Platform.

1. In system programming:
 - a. If BIOS image size is an even factor of the total size of flash, it is possible to manipulate image from the DOS prompt to match the size of the flash to ensure the image will be at the top of flash.

```
C:\ copy /b <input file> + <input file> <result file>
```

Input file is the name of the BIOS binary that you want to double in size.

Result file is the name of resultant binary file.



This DOS command will double the size of the image. Repeat if quadrupling the size is necessary. When the image matches the size of the flash, program the result to flash.

```
C:\ fpt /f <result file>
```

Use fpt to program the one MByte binary image at offset 0x100000.

```
C:\ fpt /f <input file> /address 0x100000
```

2. Third-Party, out-of-system programmer: This is the only option if you do not have a booting system. Begin programming at offset 10 0000h.

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9 Intel® Management Engine Disable for Debug/Flash Burning Purposes

This section is purely for debug purposes. Intel ME firmware is the only supported configuration for Cougar Point based system.

9.1 Intel® ME Disable

It is not necessary to disable Intel ME firmware for flash burning purposes.

The two methods for disabling the Intel ME are:

1. Erase the ME region
2. Use non-descriptor mode

9.1.1 Erasing/Programming Intel® ME Region

If CPU/Host has access to ME region, then one could either erase/program the ME region to all FFh. If there is no access, then one must assert HDA_SDO (Flash descriptor override strap) low during the rising edge of PWROK. If there are Protected Range registers set, then you will not be able to program this w/o a BIOS option to turn off this protected range. (See [5.3 SPI Protected Range Register Recommendations](#)) for more detail.

Note: This depends on the board booting HW defaults for clock configuration. If any clock configuration is required for booting the platform that is not in the HW defaults, then this option may not work for you.

9.1.2 Non-descriptor Mode

This can be performed by either erasing the descriptor or by corrupting the Flash valid signature at address 0x10.

If there is no write access to the descriptor, then one must assert HDA_SDO (Flash descriptor override strap) low during the rising edge of PWROK.

Note:

1. This requires a single flash topology or a topology where BIOS is in FWH or behind an embedded controller. If there is no descriptor the PCH automatically goes to the flash part on SPI chipselect 0 to fetch BIOS code. If you have a 2 flash part system, most likely BIOS is on SPI Chip Select 1. Chip select 1 is not accessible in non-descriptor mode.
2. This depends on the board booting HW defaults for clock configuration. If any clock configuration is required for booting the platform that is not in the HW defaults, then this option may not work for you.



9.2 Non-Intel ME Ignition Disable

Below are the methods for disabling the Intel ME for purposes of in-system programming of the flash. None of these options are necessary for the Intel ME Ignition FW.

1. Temporarily disable the Intel ME through the Intel® Management Engine BIOS Extension (Intel® MEBX). Power off or cold reset. This option is only applicable to non-Intel ME Ignition firmware.
2. HDA_SDO (Manufacturing mode jumper or Flash descriptor override jumper) asserted HIGH on the rising edge of PWROK. Power off or cold reset. This is only valid as long as you do not specifically set the variable Flash Descriptor Override Pin-Strap Ignore in the Flash Image Tool to false.
3. Overwrite the descriptor. WARNING: If using a two flash part platform, this may cause the platform not to boot. The platform will boot in non-descriptor mode, so if the clock configuration is necessary for your platform to boot, this may not be an option.

HECI ME region unlock - There is a HECI command that allows Intel ME firmware to boot up in a temporarily disabled state and allows for a host program to overwrite the ME region.

Note: Removing the DIMM from channel 0 no longer has any effect on Intel Management Engine functionality.

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10 Recommendations for SPI Flash Programming in Manufacturing Environments for Cougar Point

It is recommended that the Intel ME be disabled when you are programming the ME region. Non-Intel Management Engine Ignition firmware performs regular writes/erases to the ME region. Therefore some bits may be changed after programming. Please note that not all of these options will be optimal for your manufacturing process.

Any method of programming SPI flash where the system is not powered will not result in any interference from Management Engine FW. The following methods are for non - Intel ME Ignition FW.

Program via In Circuit Test – System is not fully powered here.

Program via external flash burning solution.

Disable the ME through the BIOS/MEBX before programming fixed offset variables (FOV) into the non-volatile memory area, or before any operation that depends on the base address for fixed variable offsets remaining constant.

Assert HDA_SDO low (Flash Descriptor Override Jumper) on the rising edge of PWROK. Note: this is only valid as long as you do not specifically disable this functionality in fixed offset variable.

With Intel ME Ignition FW, there is no need to disable Intel ME, as Intel ME does not perform writes or erases.

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11 FAQ and Troubleshooting

11.1 FAQ

Q: What is VSCC and why do I need to set this value?

A: VSCC stands for Vendor Specific Component Capabilities. This defines how BIOS and Intel ME communicate with the SPI flash. Improperly BIOS and Intel ME settings can result in improper flash functionality and lead to premature flash wear out. VSCC information is defined in two places. Two host-based VSCC registers (Host LVSCC Register and Host UVSCC Register) that is in memory mapped space and one table of VSCC entries (Management Engine VSCC Table) that is in the Descriptor Table on the SPI flash. These are separate so Intel ME Firmware does not depend on BIOS for identifying the SPI flash part. This adds some robustness as well as accommodates different BIOS flows where SPI flash is not identified until after the Management Engine needs to access the flash.

The host based VSCC registers must be programmed for any host based application, or integrated GbE software to access the SPI flash. This will have to be done by your BIOS and NOT by FITc! See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) and/or [5.5 Recommendations for Flash Configuration Lockdown and Vendor Component Lock Bits](#) for more information.

The Management Engine VSCC table has no flash parts put in by default. All flash parts that are intended to be used by the platform must have an entry in Management Engine VSCC table. This allows the ability for OEM/ODM to add Intel ME support to any flash parts that meet the requirements defined in the *Intel Cougar Point Family External Design Specification (EDS)* See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) and [6.4 Management Engine VSCC Table](#) for more information.

Q: How do I find Flash Programming Tool (FPT) and Flash Image Tool (FITC) for my platform?

A: The aforementioned flash tools are included in the system tools director in Intel ME firmware kit (Intel Active Management Technology, Intel® Quiet System Technology, Intel ASF, etc.) Please ensure that you download the appropriate kit for the target platform.

Target	Platform Name In VIP/ARMS	Kit Name
ICH8	Averill	Intel® Active Management Technology 2.X (use latest version)
ICH8M	Santa Rosa	Intel® Active Management Technology 2.X (use latest version)
ICH9	Weybridge	Intel® Active Management Technology 3.X (use latest version)
ICH9M	Montevina	Intel® Active Management Technology 4.X (use latest version)
ICH10	McCreary	Intel® Active Management Technology 5.X (use latest version)



Target	Platform Name In VIP/ARMS	Kit Name
Ibex Peak	Piketon/Kings Creek	Intel® Active Management Technology 6.X (use latest version)
Ibex Peak-M	Calpella	Intel® Active Management Technology 6.X (use latest version)
Cougar Point	Sugar Bay and Bromolow -WS	Intel® Active Management Technology 7.X (use latest version)
Cougar Point	Maho Bay	Intel® Active Management Technology 8.X (use latest version)

Q: How do I build an Image for my Intel® PCH based platform?

A: For Intel Cougar Point family based platforms, you can follow the appropriate instructions in the FW Bringup Guide which is located in the root directory of the appropriate Intel ME KIT.

Q: Is my flash part supported by the Flash Programming Tool (FPT)? How can I add support for a new flash to FPT?

A: Look at `fparts.txt` to see if the intended flash part is present. If the intended flash part meets the guidelines defined in the *Intel Cougar Point External Design Specification (EDS)*, *Intel® Management Engine (Intel® ME) Firmware SPI Flash Requirements* and support may be added to FPT by referring to [7.3 Configuring a Fparts.txt Entry](#).

Q: Is my flash part supported by Intel® ME Firmware? How can I add support for a new flash to Intel® ME Firmware?

A: As long as the SPI flash devices meets the requirements defined in the *Intel Cougar Point External Design Specification (EDS)*, support may be added for the device. BIOS will have to set up the Host VSCC registers. The Management Engine VSCC table in the descriptor will also have to be set up in order to get Intel ME firmware to work. See [4.4 Intel® Management Engine \(Intel® ME\) Vendor-Specific Component Capabilities Table](#) and [6.4 Management Engine VSCC Table](#) for more information.

Adding support does not imply validation or guarantee a flash part will work. Platform designers/integrators will have to validate all flash parts with their platforms to ensure full functionality and reliability.

Q: Why does FPT/v fail for my system even when I've written nothing to the flash?

A: Intel ME Firmware performs periodic writes to SPI flash when it is active. Due to this the ME region may not match the source file. Please see [10 Recommendations for SPI Flash Programming in Manufacturing Environments for Cougar Point](#) for more information.



Q: How can I overwrite the descriptor when FPT does not have write access? How can I overwrite a region that is locked down by descriptor protections? How do I write to flash space that is not defined by the descriptor?

A: By asserting HDA_SDO (flash descriptor override strap) low on the rising edge of PWROK, you can read, write and erase all of SPI flash space regardless of descriptor protections. Any protections imposed by BIOS or directly to the SPI flash part still apply. This should only be used in debug or manufacturing environments. End customers should **NOT** receive systems with this strap engaged.

Q: I have two flash parts installed on the board. Why does fpt /i only show one flash part?

A: Intel Cougar Point will not recognize the second SPI flash part unless it is in descriptor mode and the Component section of the descriptor properly describes the flash. Another possibility is that you have two different flash parts and the second flash part is not defined in fparts.txt.

11.2 Troubleshooting

Q: I am seeing the following error:

```

-----
Flash Programming Tool. Version 0.8.12
Reading file "fparts.txt" into memory...
Initializing SPI utilities
Reading HSFSTS register... Flash Descriptor: INVALID

--- Flash Devices Found ---

>>> Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

>>> Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

>>> Error: Timedout waiting for hardware to complete read operation!
      SSFSTS register: 0x00

>>> Error: Failed to read the device ID from the flash part!

a:\SR>

```

A: You may be using an incorrect version of FPT. Please ensure that you are using the flash tools that were provided in the kit for the target systems.

Q: What does the following FPT error message mean?

Error: The host does not have write access to the target flash memory!

A: In order for FPT to read or write to a given region, BIOS/Host must have read/write permissions to that target region. This access is set in the descriptor. Look closely at all the addresses defined in the output of FPT /i. If there are any gaps in flash space defined you cannot perform a full flash write. You must update region by region. Refer to [4.3 Region Access Control](#) for more information. You may have to reflash the descriptor to get the proper access.



Q: What does following FPT error message mean?

Error: Flash program registers are locked! HSFSTS[15] (FLOCKDN).

A: The Flash Configuration Lock-Down (FLCOKDN) bit was set HSFSTS (hardware sequencing flash status register). This locks down all the program registers in the ICH. If your BIOS and descriptor do not set up Hardware Sequencing, you will have to leave this bit unset in order to use FPT. You may have to upgrade the latest version of FPT as older versions do not support Hardware Sequencing. Please refer to [Hardware Sequencing Flash Status Register](#) in the *Intel Cougar Point External Design Specification (EDS)* for the location for the HSFSTS. Try reflashing the SPI device with a third-party programmer. If you still see this error message, please contact your BIOS vendor to ensure that they are not setting this bit.

Q: What does following FPT error message mean?

Error: There is no supported SPI flash device installed

A: See the answer to the question above: *Is my flash part supported by the Flash Programming Tool (FPT)? How can I add support for a new flash to FPT?*

If the tool correctly identifies the flash part installed and still gives an error message such as:

```
--- Flash Devices Found ---  
    SPI1234   ID:0x123456   Size: 4096KB (32768Kb)  
    Device ID: 0xFFFF not supported.
```

Error 405: There is no supported SPI flash device installed

This error will result when the descriptor has two flash parts defined. Edit the image via FIT/ftoolc and set the number of flash components to 1. See [6.2 Modifying the Flash Descriptor Region](#) for more information.

This error can also result if BIOS has not correctly set up software sequencing. See [5.4 Software Sequencing Opcode Recommendations](#) for Opcodes required for FPT operation.

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A APPENDIX A - Descriptor Configuration

A.1 Flash Descriptor PCH Soft Strap Section

The following section describes functionality and how to set soft strapping for a target platform. Improper setting of soft straps can lead to undesired operation and may lead to returns/recalls.

Only default values that will be provided are for softstraps that are reserved.

A.2 PCHSTRP0—Strap 0 Record (Flash Descriptor Records)

Flash Address: FPSBA + 000h
 Default Flash Address: 100h

Size: 32 bits

Bits	Description	Usage
31	Reserved, set to '0'	
30:29	<p>BIOS Boot-Block size (BBBS): Sets BIOS boot-block size</p> <p>00: 64 KB. Invert A16 if Top Swap is enabled (Default) 01: 128 KB. Invert A17 if Top Swap is enabled 10: 256 KB. Invert A18 if Top Swap is enabled 11: Reserved</p> <p>Notes: 9. This setting is dependent on BIOS architecture and can be different per design. The BIOS developer for the target platform has to determine this value. 10. If FWH is set as Boot BIOS destination then PCH only supports 64 KB Boot block size. This value has to be determined by how BIOS implements Boot-Block.</p>	<p>BIOS Boot-Block size deals with a BIOS recovery mechanism. It allows for the system to use alternate code in order to boot a platform based upon the Top Swap (GPIO[55] pulled low during the rising edge of PWROK.) strap being asserted.</p> <p>Top Swap inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. The size of the boot-block and setting of this field must be determined by the BIOS developer. If this is not set correctly, then BIOS boot-block recovery mechanism will not work.</p> <p>If BIOS is located on firmware hub, then this value must be set to '00'.</p> <p>Refer to Boot-Block Update Scheme in the latest revision of Intel® 6 Series Express Chipset EDS.</p> <p>Note: This setting is not the same for all designs, is dependent on the architecture of BIOS. The setting of this field must be determined by the BIOS developer.</p>
28:25	Reserved, set to '0'	



Bits	Description	Usage
24	<p>DMI RequesterID Check Disable (DMI_REQID_DIS): The primary purpose of this strap is to support environments with multiple processors that each have a different RequesterID that can each access to Serial Flash.</p> <p>0 = DMI RequesterID Checks are enabled 1 = DMI RequesterID Checks are disabled. No Requester ID checking is done on accesses from DMI.</p>	<p>This bit is only applicable for platforms that contain multiple processor sockets. If multiple processors need to access Serial Flash then this bit would need to set to '1'.</p> <p>Platforms that have a single processor socket set to '0'</p>
23:22	Reserved, set to '0'	
21	<p>MACsec Disable (MACSEC_DIS) 0 = MACsec is Enabled 1 = MACsec is Disabled</p> <p>Notes:</p> <ol style="list-style-type: none"> If not using Intel integrated wired LAN or if disabling it, then set to '1' If using Intel integrated wired LAN solution AND the use of MACsec is desired set to '0'. 	<p>MACsec is a hop-by-hop network security solution. It provides Layer 2 encryption and authenticity/integrity protection for packets traveling between MACsec-enabled nodes of the network. The key components that need to support this functionality are the server, client and switch network interface devices.</p> <p>If not using Intel's integrated wired solution, then this field must be set to '1'.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The platform hardware designer can determine the setting for this</p>
20	<p>LAN PHY Power Control GPIO12 Select (LANPHYPC_GP12_SEL): 0 = GPIO12 default is General Purpose (GP) output 1 = GPIO12 is used in native mode as LAN_PHY_PWR_CTRL</p> <p>Notes:</p> <ol style="list-style-type: none"> If not using Intel integrated wired LAN or if disabling it, then set to '0' If using Intel integrated wired LAN solution AND if GPIO12 is routed to LAN_DISABLE_N on the Intel PHY, this bit should be set to '1'. 	<p>If using Intel integrated wired LAN solution AND if GPIO12 is routed to LAN_DISABLE_N on the Intel PHY, this bit must be set to '1'.</p> <p>If GPIO12 is routed not routed to LAN_DISABLE_N on the Intel PHY, this bit must be set to '0'.</p> <p>If not using Intel integrated wired LAN or if disabling it, this bit must be set to '0'</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The platform hardware designer can determine the setting for this.</p>
19:16	Reserved, set to '0'	
15:14	<p>SMLink0 Frequency (SML0FRQ): These bits determine the physical bus speed supported by the HW.</p> <p>Must be programmed to 11b (SMBus Fast Mode). All other values reserved.</p>	<p>Fast Mode will be the only supported speed of SMLink0 interface. Speed on this bus will between 300 KHz and 350 KHz. Speed is dependent on board topology and layout.</p>
13:12	<p>Intel ME SMBus Frequency (SMB0FRQ): The value of these bits determine the physical bus speed supported by the HW.</p> <p>Must be programmed to 01b (100 kHz)</p>	The Intel ME SMBus
11:10	<p>SMLink1 Frequency (SML1FRQ) Frequency: The value of these bits determine the physical bus speed supported by the HW.</p> <p>Must be programmed to 01b (100 kHz). All other values reserved.</p>	-



Bits	Description	Usage
9	<p>SMLink1 Enable (SML1_EN): Configures if SMLink1 segment is enabled 0 = Disabled 1 = Enabled</p> <p>Note: This must be set to '1' platforms that use PCH SMBus based thermal reporting.</p>	<p>This bit must be set to '1' if using the PCH's Thermal reporting. If setting this bit to '0', there must be an external solution that gathers temperature information from PCH and processor.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.</p>
8	<p>SMLink0 Enable (SML0_EN): Configures if SMLink0 segment is enabled 0 = Disabled 1 = Enabled</p> <p>Notes:</p> <ol style="list-style-type: none"> This bit MUST be set to '1' when utilizing Intel integrated wired LAN. The Intel PHY SMBus controller must be routed to this SMLink 0 Segment. If not using Intel integrated wired LAN solution or if disabling it, then this segment must be set to '0'. 	<p>This bit MUST be set to '1' when utilizing Intel integrated wired LAN.</p> <p>The Intel PHY SMBus controller must be routed to this SMLink 0 Segment.</p> <p>If not using Intel integrated wired LAN solution or if disabling it, then this segment must be disabled (set to '0').</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.</p>
7	<p>Intel ME SMBus Select (SMB_EN): Configures if the ME SMBus segment is enabled 0 = Disabled 1 = Enabled</p> <p>Note: This bit MUST be set to '1'.</p>	<p>This bit must always be set to '1'.</p>
6:3	Reserved, set to '0'	
2:1	Chipset Configuration Softstrap 1: Must be set to 01b.	
0	Reserved, set to '0'	

A.3 PCHSTRP1—Strap 1 Record (Flash Descriptor Records)

Flash Address: FPSBA + 004h
 Default Value: 0000000Fh
 Default Flash Address: 104h

Size: 32 bits

Bits	Description	Usage
31:9	Reserved, set to '0'	
8	Chipset Configuration Softstrap 2: Must be set to 1b.	
7:4		
3:0	Chipset Configuration Softstrap 3: Must be set to Fh.	



A.4 PCHSTRP2—Strap 2 Record (Flash Descriptor Records)

Flash Address: FPSBA + 008h
 Default Flash Address: 108h

Size: 32 bits

Bits	Description	Usage
31:25	<p>Intel® ME SMBus I²C Address (MESMI2CA): Defines 7 bit Intel® ME SMBus I²C target address</p> <p>Note: This field is only used for testing purposes</p>	<p>This address is only used by Intel® ME FW for testing purposes. If MESMI2CEN (PCHSTRP2 bit 24) is set to 1 then the address used in this field must be non-zero and not conflict with any other devices on the segment.</p>
24	<p>Intel® ME SMBus I²C Address Enable (MESMI2CEN): 0 = Intel® ME SMBus I²C Address is disabled 1 = Intel® ME SMBus I²C Address is enabled</p> <p>Note: This field is only used for testing purposes</p>	<p>This field should only be set to '1' for testing purposes.</p>
23:17	<p>Intel® ME SMBus MCTP Address (MESMMCTPA): Defines 7 bit Intel® ME SMBus MCTP target address</p> <p>Note: This field is only used for testing purposes</p>	<p>This address is used by Intel® ME Anti-Theft Technology.</p> <p>If MESMI2CEN (PCHSTRP2 bit 24) is set to 1 then the address used in this field must be non-zero and not conflict with any other devices on the segment.</p>
16	<p>Intel® ME SMBus MCTP Address Enable (MESMMCTPAEN): 0 = Intel® ME SMBus MCTP Address is disabled 1 = Intel® ME SMBus MCTP Address is enabled</p> <p>Note: This field is only used for testing purposes</p>	<p>This field should only be set to '1' for testing purposes on platforms that use 3G Anti-Theft functionality.</p>
15:9	<p>Intel® ME SMBus Alert Sending Device (ASD) Address (MESMASDA): Intel ME SMBus Controller ASD Target Address.</p> <p>Note: This field is only applicable if there is an ASD attached to SMBus and using Intel® AMT</p>	<p>If MESMASDEN(PCHSTRP2 bit 8) is set to '1' there must be a valid address for ASD. The address must be determined by the BIOS developer based on the requirements below.</p> <p>A valid address must be:</p> <ul style="list-style-type: none"> • Non-zero value • Must be a unique address on the Host SMBus segment • Be compatible with the master on SMBus - For example, if the ASD address the master that needs write thermal information to an address "xy"h. Then this field must be set to "xy"h.



Bits	Description	Usage
8	<p>Intel® ME SMBus Alert Sending Device (ASD) Address Enable (MESMASDEN): 0 = Intel ME SMBus ASD Address is disabled 1 = Intel ME SMBus ASD Address is enabled</p> <p>Note: This field is only applicable if there is an ASD attached to SMBus and using Intel® AMT</p>	<p>This bit must only be set to '1' when there is an ASD (Alert Sending Device) attached to Host SMBus. This is only applicable in platforms using Intel® AMT.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.</p>
7:0	Reserved, set to '0'	

A.5 PCHSTRP3—Strap 3 Record (Flash Descriptor Records)

Flash Address: FPSBA + 00Ch
 Default Value: 00000000h
 Default Flash Address: 10Ch

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	



A.6 PCHSTRP4—Strap 4 Record (Flash Descriptor Records)

Flash Address: FPSBA + 010h
 Default Flash Address: 110h

Size: 32 bits

Bits	Description	Usage
31:24	Reserved, set to '0'	
23:17	<p>GbE PHY SMBus Address: This is the 7 bit SMBus address the PHY uses to accept SMBus cycles from the MAC.</p> <p>Note: This field must be programmed to 64h.</p>	<p>This is the Intel PHY's SMBus address. This field must be programmed to 64h.</p> <p>GbE PHY SMBus Address and GbE MAC address have to be programmed to 64h and 70h in order to ensure proper arbitration of SMBus communication between the Intel integrated MAC and PHY.</p>
16	Reserved, set to '0'	
15:9	<p>GbE MAC SMBus Address: This is the 7 bit SMBus address uses to accept SMBus cycles from the PHY.</p> <p>Note: This field must be programmed to 70h.</p>	<p>This is the Intel integrated wired MAC's SMBus address. This field must be programmed to 70h.</p> <p>GbE PHY SMBus Address and GbE MAC address have to be programmed to 64h and 70h in order to ensure proper arbitration of SMBus communication between the Intel integrated MAC and PHY.</p>
8	<p>Gbe MAC SMBus Address Enable (GBEMAC_SMBUS_ADDR_EN): 0 = Disable 1 = Enable</p> <p>Notes: 1. This bit MUST be set to '1' when utilizing Intel integrated wired LAN. 2. If not using Intel integrated wired LAN solution or if disabling it, then this segment must be set to '0'.</p>	<p>This bit must be set to '1' if Intel integrated wired LAN solution is used.</p> <p>If not using, or if disabling Intel integrated wired LAN solution, then this field must be set to '0'.</p>
7:2	Reserved, set to '0'	
01:00	<p>Intel PHY Connectivity (PHYCON[1:0]): This field determines if Intel wired PHY is connected to SMLink0</p> <p>00: No Intel wired PHY connected 10: Intel wired PHY on SMLink0 All other values Reserved</p> <p>Notes: 1. This bit MUST be set to '10' when utilizing Intel integrated wired LAN. 2. If not using, or if disabling Intel integrated wired LAN solution, then this segment must be set to 00b.</p>	<p>This field must be set to "10" if Intel integrated wired LAN solution is used.</p> <p>If not using, or if disabling Intel integrated wired LAN solution, then field must be set to "00".</p>



A.7 PCHSTRP5—Strap 5 Record (Flash Descriptor Records)

Flash Address: FPSBA + 014h
 Default Value: 00000000h
 Default Flash Address: 114h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.8 PCHSTRP6—Strap 6 Record (Flash Descriptor Records)

Flash Address: FPSBA + 018h
 Default Value: 00000000h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.9 PCHSTRP7—Strap 7 Record (Flash Descriptor Records)

Flash Address: FPSBA + 118h
 Default Value: 00000000h

Size: 32 bits

Bits	Description	Usage
31:0	<p>Intel ME SMBus Subsystem Vendor and Device ID (MESMA2UDID): MESMAUDID[15:0] - Subsystem Vendor ID MESMAUDID[31:16] - Subsystem Device ID</p> <p>The values contained in MESMAUDID[15:0] and MESMAUDID[31:16] are provided as bytes 8-9 and 10-11 of the data payload to an external master when it initiates a Directed GET UDID Block Read Command to the Alert Sending Device ASD's address.</p>	<p>This bit must only be set to '1' when there is an ASD (Alert Sending Device) attached to SMBus and when MESMASDEN(PCHSTRP2 bit 8) is set to '1'. This is only applicable in platforms using Intel® AMT. Set this if you want to add a 4 byte payload to an external master when a GET UDID Block read command is made to Intel ME SMBus ASD's address.</p>



A.10 PCHSTRP8—Strap 8 Record (Flash Descriptor Records)

Flash Address: FPSBA + 020h
 Default Flash Address: 120h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.11 PCHSTRP9—Strap 9 Record (Flash Descriptor Records)

Flash Address: FPSBA + 024h
 Default Flash Address: 124h

Size: 32 bits

Bits	Description	Usage
31:30	Reserved, set to '0'.	
29:28	Must be set to 11b.	
27:23	Reserved, set to '0'.	
22	<p>PCHHOT# or SML1ALERT# Select (PCHHOT#_SML1ALERT#_SEL) This strap determines the native mode operation of GPIO74</p> <p>0 = SML1ALERT# is the native functionality of GPIO74 1 = PCHHOT# is the native functionality of GPIO74</p>	<p>PCHHOT# is used to indicate the PCH temperature out of bounds condition to an external agent such as BMC or EC, when PCH temperature is greater than value programmed by BIOS.</p>
21:15	Reserved, set to '0'.	
14	<p>Subtractive Decode Agent Enable (SUB_DECODE_EN) 0 = Disables PCH PCIe ports from Subtractive Decode Agent 1 = Enables PCH's PCIe ports to behave as a subtractive decode agent</p> <p>Note: If connecting a PCI bridge chip to the PCH that requires the PCH to behave as a subtractive decode agent, then set this bit to '1'.</p>	<p>Set this bit to '1' if there is a PCI bridge chip connected to the PCH, that requires subtractive decode agent. Set to '0' if the platform has no PCI bridge chip.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the platform hardware designer.</p>
13:12	Reserved, set to '0'	



Bits	Description	Usage
11	<p>Intel PHY Over PCI Express* Enable (PHY_PCIE_EN): 0 = Intel integrated wired MAC/PHY communication is not enabled over PCI Express*. 1 = The PCI Express* port selected by the PHY_PCIEPORT_SEL soft strap to be used by Intel PHY</p> <p>Note: This bit must be "1" if using Intel integrated wired LAN solution.</p>	<p>This bit MUST be set to '1' if using Intel integrated wired LAN solution.</p> <p>If not using, or if disabling Intel integrated wired LAN solution then set this to '0'.</p>
10:8	<p>Intel PHY PCIe* Port Select (PHY_PCIEPORTSEL): Sets the default PCIe* port to use for Intel integrated wired PHY.</p> <p>000: Port 1 001: Port 2 010: Port 3 011: Port 4 100: Port 5 101: Port 6 110: Port 7 111: Port 8</p> <p>Note: This field only applies when PHY_PCIE_EN = '1'. Set to 000b when PHY_PCIE_EN is set to '0'</p>	<p>This field tells the PCH which PCI Express* port an Intel PHY is connected.</p> <p>If PHY_PCIE_EN is = '0', then this field is ignored.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The platform hardware designer or schematic review can determine what PCIe* Port the Intel wired PHY is routed.</p>
7	<p>Chipset Configuration Softstrap 4 Set to '1'b</p>	
6	<p>DMI and Intel® Flexible Display Interface (FDI) Reversal (DMILR):</p> <p>0 = DMI Lanes 0 - 3 are not reversed. 1 = DMI Lanes 0 - 3 are reversed.</p>	<p>This field is used only when DMI Lanes are reversed on the layout. This usually only is done on layout constrained boards where reversing lanes help routing.</p> <p>Note: This setting is dependent on the board design. The platform hardware designer must determine if DMI needs lane reversal.</p>
5	<p>PCIe* Lane Reversal 2 (PCIELR2): This bit lane reversal behavior for PCIe Port 5 if configured as a x4 PCIe* port.</p> <p>0 = PCIe Lanes 4-7 are not reversed. 1 = PCIe Lanes 4-7 are reversed when Port 5 is configured as a 1x4.</p> <p>Note: This field only is in effect if PCIEPCS2 is set to '11'b.</p>	<p>If configuring PCIe* port 5 as a x4 PCIe* bus, reversing the lanes of this port is done via this strap.</p> <p>PCI Express* port lane reversal can be done to aid in the laying out of the board.</p> <p>Note: This setting is dependent on the board design. The platform hardware designer must determine if this port needs lane reversal.</p>
4	<p>PCIe* Lane Reversal 1 (PCIELR1). This bit lane reversal behavior for PCIe* Port 1 if configured as a x4 PCIe port.</p> <p>0 = PCIe Lanes 0-3 are not reversed. 1 = PCIe Lanes 0-3 are reversed when Port 1 is configured as a 1x4.</p> <p>Note: This field only is in effect if PCIEPCS1 is set to '11'b.</p>	<p>If configuring PCIe* port 5 as a x4 PCIe* bus, reversing the lanes of this port is done via this strap.</p> <p>PCI Express* port lane reversal can be done to aid in the laying out of the board.</p> <p>Note: This setting is dependent on the board design. The platform hardware designer can determine if this port needs lane reversal</p>



Bits	Description	Usage
3:2	<p>PCI Express* Port Configuration Strap 2 (PCIEPCS2).</p> <p>These straps set the default value of the PCI Express port Configuration 2 register covering PCIe ports 5-8.</p> <p>11: 1x4 Port 5 (x4), Ports 6-8 (disabled) 10: 2x2 Port 5 (x2), Port 7 (x2), Ports 6, 8 (disabled) 01: 1x2, 2x1 Port 5 (x2), Port 6 (disabled), Ports 7, 8 (x1) 00: 4x1Ports 5-8 (x1)</p>	<p>Setting of this field depend on what PCIe* ports 5-8 configurations are desired by the board manufacturer. Only the x4 configuration ("11") has the option of lane reversal if PCIELR2 is set to '1'.</p> <p>Note: This field must be determined by the PCI Express* port requirements of the design. The platform hardware designer must determine this setting.</p>
1:0	<p>PCI Express* Port Configuration Strap 1 (PCIEPCS1).</p> <p>These straps set the default value of the PCI Express* Port Configuration 1 register covering PCIe ports 1-4.</p> <p>11: 1x4Port 1 (x4), Ports 2-4 (disabled) 10: 2x2 Port 1 (x2), Port 3 (x2), Ports 2, 4 (disabled) 01: 1x2, 2x1 Port 1 (x2), Port 2 (disabled), Ports 3, 4 (x1) 00: 4x1Ports 1-4 (x1)</p>	<p>Setting of this field depend on what PCIe* ports 1-4 configurations are desired by the board manufacturer. Only the x4 configuration ("11") has the option of lane reversal if PCIELR1 is set to '1'.</p> <p>Note: This field must be determined by the PCI Express* port requirements of the design. The platform hardware designer must determine this setting.</p>

A.12 PCHSTRP10—Strap 10 Record (Flash Descriptor Records)

Flash Address: FPSBA + 028h
 Default Flash Address: 128h

Size: 32 bits

Bits	Description	Usage
31:16	Reserved, set to '0'	
15:9	<p>ME Debug SMBus Emergency Mode Address (MDSMBE_ADD):</p> <p>SMBUS address used for ME Debug status writes. If this field is 00h, the default address, 38h, is used.</p>	This field is only used for testing purposes.
8	<p>ME Debug SMBus Emergency Mode Enable (MDSMBE_EN):</p> <p>0 = Disable Intel ME Debug status writes 1 = Enable Intel ME Debug status writes over SMBUS using the address set by MMADDR.</p>	<p>This field is only used for testing purposes.</p> <p>When this bit is enabled, you will see writes on SMBus to address 38h bits address (70h bit shifted), or value is specified in MMADDR. MMADDR specifies address bits 7:1 of the target address.</p>
7:2	Reserved, set to '0'	
1	<p>ME Boot Flash (ME_Boot_Flash).</p> <p>0 = Intel Management Engine will boot from ROM, then flash 1 = Intel Management Engine will boot from flash</p> <p>Note: This field should only be set to '1b' if the Intel ME binary loaded in the platform has a ME ROM Bypass image</p>	<p>This bit must be set to 0 for production PCH based platforms.</p> <p>This bit will only be set to '1' in order to work around issues in pre-production hardware and Intel ME FW.</p>
0	Reserved, set to '0'	



A.13 PCHSTRP11—Strap 11 Record (Flash Descriptor Records)

Flash Address: FPSBA + 02Ch
 Default Flash Address: 12Ch

Size: 32 bits

Bits	Description	Usage
31:25	<p>SMLink1 I2C* Target Address (SML1I2CA) Defines the 7 bit I2C target address for PCH Thermal Reporting on SMLink1.</p> <p>Notes:</p> <ol style="list-style-type: none"> This field is not active unless SML1I2CAEN is set to '1'. This address MUST be set if there is a device on the SMLink1 segment that will use thermal reporting supplied by PCH. If SML1I2CAEN = '1' then this field must be a valid 7 bit, non-zero address that does not conflict with any other devices on SMLink1 segment. This address can be different for every design, ensure BIOS developer supplies the address. 	<p>When SML1I2CAEN(PCHSTRP11 bit 24) = '1', there needs to be a valid I²C address in this field. This address used here is design specific. The BIOS developer and/or platform hardware designer must supply an address with the criteria below.</p> <p>A valid address must be:</p> <ul style="list-style-type: none"> Non-zero value Must be a unique address on the SMLink1 segment Be compatible with the master on SMLink1 - For example, if the I²C address the master that needs write thermal information to a address "xy"h. Then this filed must be to "xy"h.
24	<p>SMLink1 I²C Target Address Enable (SML1I2CAEN) 0 = SMLink1 I²C Address is disabled 1 = SMLink1 I²C Address is enabled</p> <p>Notes:</p> <ol style="list-style-type: none"> This bit MUST set to '1' if there is a device on the SMLink1 segment that will use PCH thermal reporting. This bit MUST be set to '0' if PCH thermal reporting is not used. 	<p>This bit must be set in cases where SMLink1 has a master that requires SMBus based Thermal Reporting that is supplied by the PCH. Some examples of this master could be an Embedded Controller, a BMC, or any other SMBus Capable device that needs Processor and/or PCH temperature information. If no master on the SMLink1 segment is capable of utilizing thermal reporting, then this field must be set to '0'.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.</p>
23:8	Reserved, set to '0'	
7:1	<p>SMLink1 GP Address (SML1GPA): SMLink1 controller General Purpose Target Address (7:1)</p> <p>Notes:</p> <ol style="list-style-type: none"> This field is not active unless SML1GPAEN is set to '1'. This address MUST be set if there is a device on the SMLink1 segment that will use SMBus based PCH thermal reporting. If SML1GPAEN = '1' then this field must be a valid 7 bit, non-zero address that does not conflict with any other devices on SMLink1 segment. 	<p>When SML1GPAEN = '1', there needs to be a valid GP address in this field. This address used here is design specific. The BIOS developer and/or platform hardware designer must supply an address with the criteria below.</p> <p>A valid address must be:</p> <ul style="list-style-type: none"> Non-zero value Must be a unique address on the SMLink1 segment Be compatible with the master on SMLink1 - For example if the GP address the master that needs read thermal information from a certain address, then this filed must be set accordingly.
0	<p>SMLink1 GP Address Enable(SML1GPAEN): SMLink1 controller General Purpose Target Address Enable 0 = SMLink1 GP Address is disabled 1 = SMLink1 GP Address is enabled</p> <p>Notes:</p> <ol style="list-style-type: none"> This bit MUST set to '1' if there is a device on the SMLink1 segment that will use SMBus based PCH thermal reporting. This bit MUST be set to '0' if PCH thermal reporting is not used. 	<p>This bit must be set in cases where SMLink1 has a master that requires SMBus based Thermal Reporting that is supplied by the PCH. Some examples of this master could be an Embedded Controller, a BMC, or any other SMBus Capable device that needs Processor or PCH temperature information. If no master on the SMLink1 segment is capable of utilizing thermal reporting, then this field must be set to '0'.</p> <p>Note: This setting is not the same for all designs, is dependent on the board design. The setting of this field must be determined by the BIOS developer and the platform hardware designer.</p>



A.14 PCHSTRP12—Strap 12 Record (Flash Descriptor Records)

Flash Address: FPSBA + 030h
Default Value: 00000000h
Default Flash Address: 130h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.15 PCHSTRP13—Strap 13 Record (Flash Descriptor Records)

Flash Address: FPSBA + 034h
Default Value: 00000000h
Default Flash Address: 134h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.16 PCHSTRP14—Strap 14 Record (Flash Descriptor Records)

Flash Address: FPSBA + 038h
Default Value: 00000000h
Default Flash Address: 138h

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	



A.17 PCHSTRP15—Strap 15 Record (Flash Descriptor Records)

Flash Address: FPSBA + 03Ch
 Default Flash Address: 13Ch
 Recommended Value:

Size: 32 bits

Bits	Description	Usage
31:16	Reserved, set to '0'	
15	<p>SLP_LAN#/GPIO29 Select (SLP_LAN#_GP29_SEL)</p> <p>0 = GPIO29 can only be used only as SLP_LAN# for Intel integrated LAN solution. 1 = GPIO29 is available for GPIO configuration</p> <p>Notes:</p> <ol style="list-style-type: none"> This must be set to '0' if the platform is using Intel's integrated wired LAN solution. Set to '1' only if GPIO29 needs to be available for target platform design AND if Intel integrated wired LAN solution is NOT used. 	<p>This strap will allow the usage of GPIO29, which is not available when the Intel integrated LAN functionality is not set.</p> <p>If there is no Intel integrated LAN AND there is a need of GPIO29. Then set this bit to '1'.</p> <p>If Intel integrated LAN is used, then this bit must be set to '0'.</p>
14	<p>SMLink1 Thermal Reporting Select (SMLINK1_THERM_SEL)</p> <p>0 = Intel ME FW will collect temperature from the processor, PCH and DIMMs. It will be available for polling on SMLink1 1 = PCH temperature (1 byte of data) will be available for polling out on SMLink1. Processor and DIMMs temperature monitoring will require an external device.</p>	
13:10	Reserved, set to '0'	
9:8	Chipset Configuration Softstrap 5 Set to '11'b	
7	Reserved, set to '0'	
6	<p>Intel integrated wired LAN Enable(IWL_EN)</p> <p>0 = Disable Intel integrated wired LAN Solution 1 = Enable Intel integrated wired LAN Solution</p> <p>Notes:</p> <ol style="list-style-type: none"> This must be set to '1' if the platform is using Intel's integrated wired LAN solution. Set to '0' if not using Intel integrated wired LAN solution or if disabling it. 	<p>This must be set to '1' if the platform is using Intel's integrated wired LAN solution.</p> <p>This must be set to '0' if not using Intel's integrated wired LAN solution or if disabling it.</p>
5:0	Chipset Configuration Softstrap 6 Set to '111110'b	



A.18 PCHSTRP16—Strap 16 Record (Flash Descriptor Records)

Flash Address: FPSBA + 040h
Default Flash Address: 140h
Recommended Value:

Size: 32 bits

Bits	Description	Usage
31:0	Reserved, set to '0'	

A.19 PCHSTRP17—Strap 17 Record (Flash Descriptor Records)

Flash Address: FPSBA + 044h
Default Flash Address: 144h
Recommended Value:

Size: 32 bits

Bits	Description	Usage
31:2	Reserved, set to '0'	
1	Chipset configuraiton Softstrap 7 Set to 1	
0	Reserved, set to '0'	



A.20 Softstrap Step-Through

General questions help in setting softstraps and certain other descriptor values.

For all configurations, the following must be set:

Name	Location	Value
SMB_EN	PCHSTRP0[7]	1b

A.20.1 Does the target platform use the Intel integrated wired LAN solution?

1. If Yes:

Name	Location	Value
SMLO_EN	PCHSTRP0[8]	1b
GBEPHY_SMBUS_ADDR	PCHSTRP4[23:17]	64h
GBEMAC_SMBUS_ADDR	PCHSTRP4[15:9]	70h
GBE_SMBUS_ADDR_EN	PCHSTRP4[8]	1b
PHYCON[1:0]	PCHSTRP4[1:0]	10b
PHY_PCIE_EN	PCHSTRP9[11]	1b
SLP_LAN#_GP29_SEL	PCHSTRP15[15]	0b
IWL_EN	PCHSTRP15[6]	1b

a. What PCIe* port is the Intel PHY attached? Note: Intel CRBs use port 6.

Name	Location	Value
PHY_PCIEPORTSEL	PCHSTRP9[10:8]	000b: Port 1, 001b: Port 2, 010b: Port 3, 011b: Port 4, 100b: Port 5, 101b: Port 6, 110b: Port 7, 111b: Port 8

b. Is the signal GPIO12 from the PCH routed to the signal LAN_DISABLE_N on the Intel wired PHY?

i. If YES (default):

Name	Location	Value
LANPHYPC_GP12_SEL	PCHSTRP0[20]	1b

ii. If NO:

Name	Location	Value
LANPHYPC_GP12_SEL	PCHSTRP0[20]	0b



c. Is MACsec Disabled?

i. If YES (default):

Name	Location	Value
MACSEC_DIS	PCHSTRP0[21]	1b

ii. If NO:

Name	Location	Value
MACSEC_DIS	PCHSTRP0[21]	0b

2. If the target platform IS **NOT** using Intel intergrated wired LAN solution:

Name	Location	Value
MACSEC_DIS	PCHSTRP0[21]	1b
LANPHYPC_GP12_SEL	PCHSTRP0[20]	0b
SML0_EN	PCHSTRP0[8]	0b
GBE_SMBUS_ADDR_EN	PCHSTRP4[8]	0b
PHYCON[1:0]	PCHSTRP4[1:0]	00b
PHY_PCIE_EN	PCHSTRP9[11]	0b
SLP_LAN#_GP29_SEL	PCHSTRP15[15]	1b
IWL_EN	PCHSTRP15[6]	0b

A.20.2 Are DMI Lanes reversed on target design?

1. If YES:

Name	Location	Value
DMILR	PCHSTRP9[6]	1b

2. If NO:

Name	Location	Value
DMILR	PCHSTRP9[6]	0b



A.20.3 How should PCIe* Lanes 1-4 on the target platform be configured?

1. 1x4: Port 1 (x4), Ports 2-4 (disabled):

Name	Location	Value
PCIEPCS1	PCHSTRP9[1:0]	11b

- a. If 1X4 PCIe lane 1 **is** reversed:

Name	Location	Value
PCIELR1	PCHSTRP9[4]	1b

- b. If 1X4 PCIe lane 1 **is not** reversed:

Name	Location	Value
PCIELR1	PCHSTRP9[4]	0b

2. 2x2: 2x2 Port 1 (x2), Port 3 (x2), Ports 2, 4 (disabled) (Not for Desktop):

Name	Location	Value
PCIEPCS1	PCHSTRP9[1:0]	10b

3. 1x2, 2x1 Port 1 (x2), Port 2 (disabled), Ports 3, 4 (x1) (Not for Desktop):

Name	Location	Value
PCIEPCS1	PCHSTRP9[1:0]	01b

4. 4x1: Ports 1-4 (x1):

Name	Location	Value
PCIEPCS1	PCHSTRP9[1:0]	00b



A.20.4 How should PCIe* Lanes 5-8 on the target platform be configured?

1. 1x4 – one 4 lane PCIe port:

Name	Location	Value
PCIEPCS2	PCHSTRP9[3:2]	11b

a. If 1X4 PCIe lane 5 is reversed:

Name	Location	Value
PCIELR2	PCHSTRP9[5]	1b

b. If 1X4 PCIe lane 5 is NOT reversed:

Name	Location	Value
PCIELR2	PCHSTRP9[5]	0b

2. 2x2: Port 5 (x2), Port 7 (x2), Ports 6, 8 (disabled) (Not for Desktop):

Name	Location	Value
PCIEPCS2	PCHSTRP9[3:2]	10b

3. 1x2, 2x1: Port 5 (x2), Port 6 (disabled), Ports 7, 8 (x1) (Not for Desktop):

Name	Location	Value
PCIEPCS2	PCHSTRP9[3:2]	01b

4. 4x1: Ports 5-8 (x1):

Name	Location	Value
PCIEPCS2	PCHSTRP9[3:2]	00b



A.20.5 Is there a third party device connected to SMLink1 that will gather Thermal Reporting Data on the target platform?

1. If YES:

Name	Location	Value
SML1_EN	PCHSTRP0[9]	1b
SML1I2CA	PCHSTRP11[31:25]	See PCHSTRP11[31:25] usage
SML1I2CAEN	PCHSTRP11[24]	1b
SML1GPA	PCHSTRP11[7:1]	See PCHSTRP11[7:1] usage
SML1GPEN	PCHSTRP11[0]	1b

a. If thermal data to be collected is PCH only:

Name	Location	Value
SMLINK1_THERM_SEL	PCHSTRP15[14]	1b

b. If thermal data is to Processor, and PCH:

Name	Location	Value
SMLINK1_THERM_SEL	PCHSTRP15[14]	0b

2. If NO:

Name	Location	Value
SML1_EN	PCHSTRP0[9]	0b
SML1I2CA	PCHSTRP11[31:25]	00h
SML1I2CAEN	PCHSTRP11[24]	0b
SML1GPA	PCHSTRP11[7:1]	00h
SML1GPEN	PCHSTRP11[0]	0b
SMLINK1_THERM_SEL	PCHSTRP15[14]	0b



A.20.6 What is the size of the boot BIOS block on the target platform?

Note: Value must be determined by BIOS developer.

1. If 64 KB:

Name	Location	Value
BBBS	PCHSTRP0[30:29]	00b

2. If 128 KB:

Name	Location	Value
BBBS	PCHSTRP0[30:29]	01b

3. If 256 KB:

Name	Location	Value
BBBS	PCHSTRP0[30:29]	10b

A.20.7 Is there an alert sending device (ASD) on Host SMBus on the target platform?

NOTE: This is only valid for Intel AMT enabled platforms.

1. If YES:

Name	Location	Value
MESMASDA	PCHSTRP2[15:9]	See PCHSTRP2[15:9] usage
MESMASDEN	PCHSTRP2[8]	1b
MESMA2UDID	PCHSTRP7[31:0]	See PCHSTRP7 usage

2. If NO:

Name	Location	Value
MESMASDA	PCHSTRP2[15:9]	00h
MESMASDEN	PCHSTRP2[8]	0b
MESMA2UDID	PCHSTRP7[31:0]	00000000h



A.20.8 Are there multiple processors in the target system?

1. If NO:

Name	Location	Value
DMI_REQID_DIS	PCHSTRP0[24]	0b

2. If YES:

Name	Location	Value
DMI_REQID_DIS	PCHSTRP0[24]	1b

A.20.9 Enable Intel ME Debug Options. Including Logging for Intel MDDD (Intel ME Memory-attached Debug Display Device), Intel MESSDC (ME SMBus Debug Console)?

Note: All production systems must have logging disabled.

1. If YES:

Name	Location	Value
ME_DEBUG_EN	PCHSTRP10[24]	1b
MDSMBE_ADD	PCHSTRP10[15:9]	38h
MDSMBE_EN	PCHSTRP10[8]	1b

2. If NO: **NOTE:** All production platforms **MUST** disable Options.

Name	Location	Value
ME_DEBUG_EN	PCHSTRP10[24]	0b
MDSMBE_ADD	PCHSTRP10[15:9]	00h
MDSMBE_EN	PCHSTRP10[8]	0b

A.20.10 What is the desired native functionality of GPIO74?

1. If SML1Alert#:

Name	Location	Value
PCHHOT#_SML1ALERT#_SEL	PCHSTRP9[22]	0b

2. If PCHHOT#,

Name	Location	Value
PCHHOT#_SML1ALERT#_SEL	PCHSTRP9[22]	1b



A.20.11 Does the platform have a PCI bridge chip that requires a subtractive decode agent?

Note: If your platform doesn't support PCI set this to NO. If using a Desktop/Server PCH that supports PCI interface and does **NOT** require an external PCI bridge chip then set this to NO.

1. If YES:

Name	Location	Value
SUB_DECODE_EN	PCHSTRP09[14]	1b

2. If NO:

Name	Location	Value
SUB_DECODE_EN	PCHSTRP09[14]	0b

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