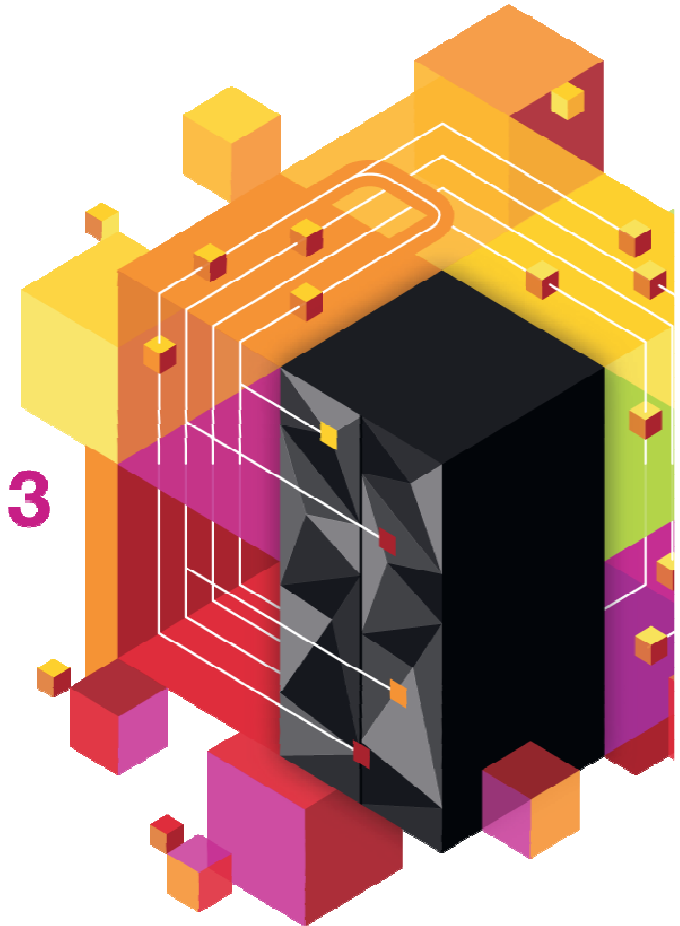
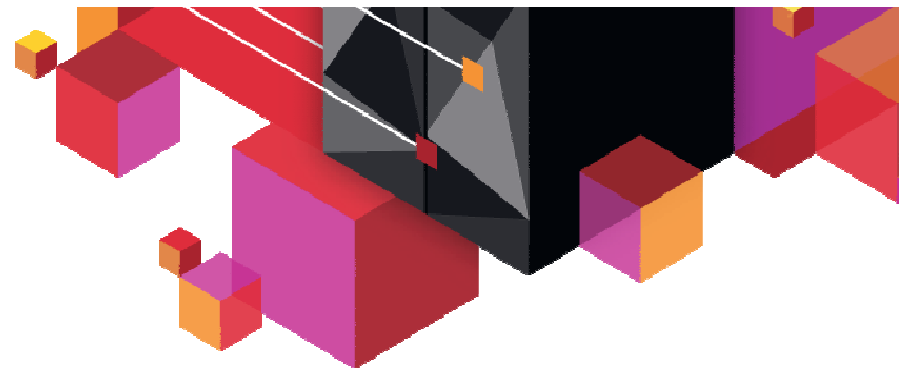




Université du Mainframe 2013

4-5 avril





IBM zEC12

Tout sur le zEC12

(Savez-vous tout de lui ?)

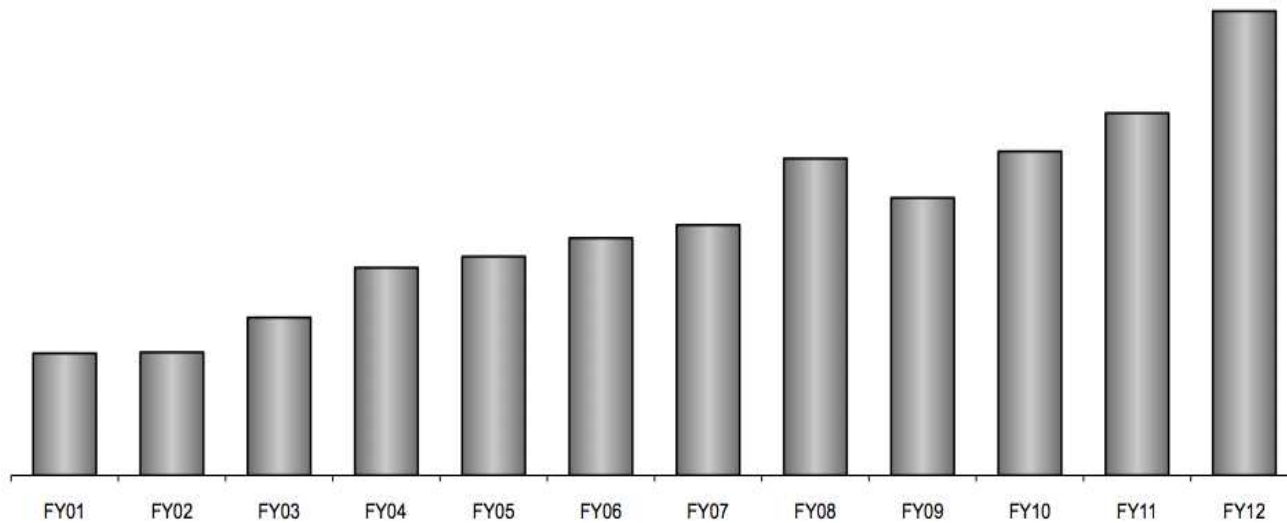
François Launay
Product Manager hardware System z / zEnterprise
flaunay@fr.ibm.com



Université du Mainframe 2013

4-5 avril

The growing IBM zEnterprise System ecosystem



4Q12: 66% yty
The highest shipped MIPS growth in history

System z Total Installed Capacity

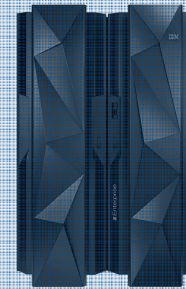
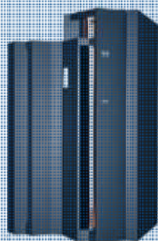
56%	180+	220+	3/4+	1,000+	7,400+
year-to-year revenue growth in 4Q12, the strongest since before 2000	new accounts since 3Q10 IBM zEnterprise® launch, with 1/3+ in growth markets	hybrid computing units shipped since 3Q10	of Top 100 enterprises have installed IFLs	schools in 67 countries are part of the IBM Academic Initiative for System z	ISV apps run on IBM System z; 90 new ISVs added in 2012

[IFL = Linux-on-z Only Engine]

Delivering to Smarter Computing with zEnterprise

Vision:

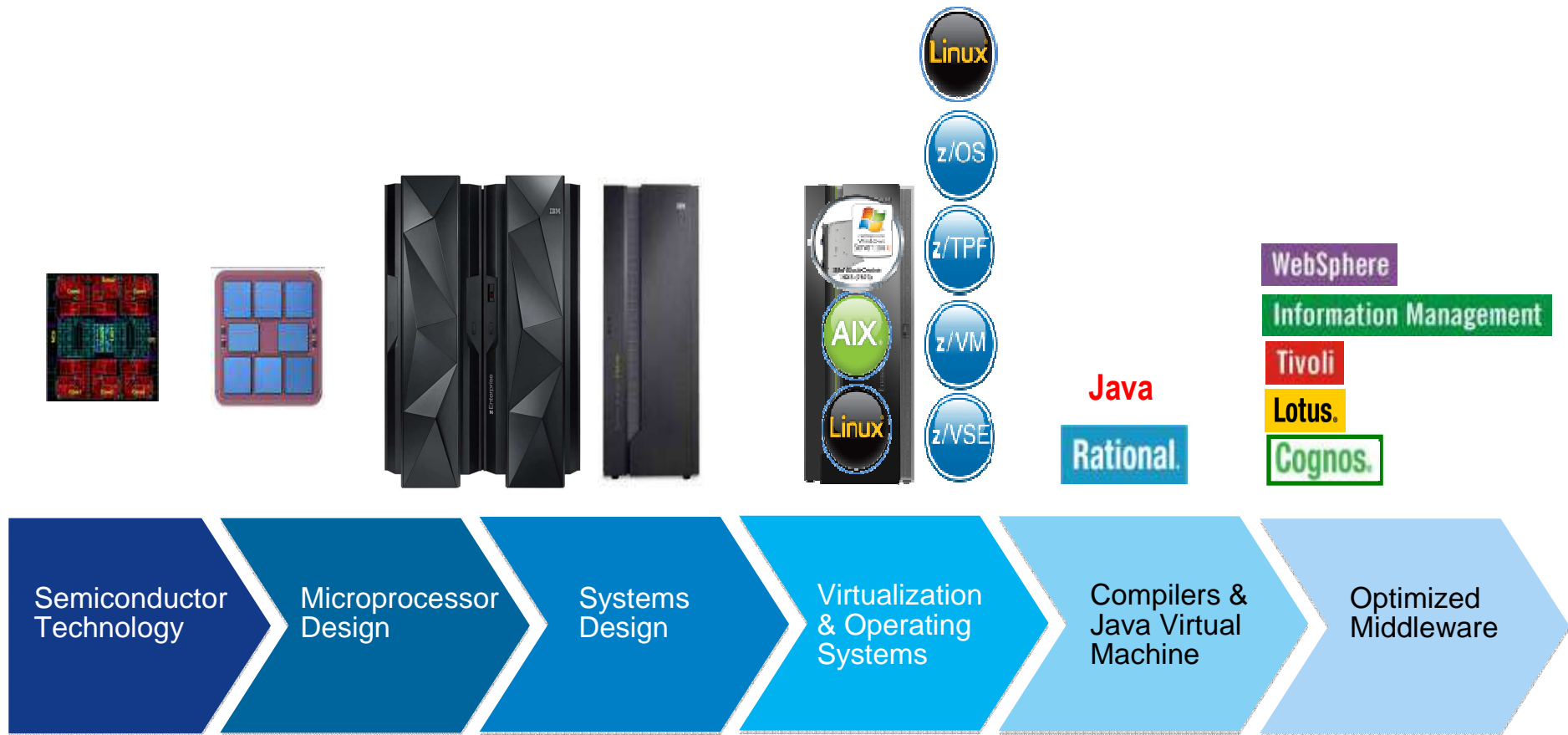
- zEnterprise will continue to invest in improving the virtualization and management capabilities for hybrid computing environments
- zEnterprise will more tightly integrate with PureSystems over time
- zEnterprise and STG will continue to leverage the Tivoli portfolio to deliver enterprise wide management capabilities across all STG systems including PureSystems



All statements regarding IBM's future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only.

© 2013 IBM Corporation

IBM zEnterprise EC12: Optimized from Silicium to Software



Introducing the newest members of the zEnterprise System family

IBM zEnterprise EC12 (zEC12)



IBM zEnterprise Unified Resource Manager and zEnterprise BladeCenter® Extension (zBX) Mod 003

IBM DB2 Analytics Accelerator V3
Plus more flexibility and function by connecting to IDAA

zEnterprise EC12



IBM System z Generations

N-5	N-4	N-3	N-2	N-1
				
<p>z900</p> <ul style="list-style-type: none"> •Announced 10/2000 •770 MHz •Up to 16 assignable cores •CP, IFL, ICF •Up to 64 GB Memory 	<p>z990</p> <ul style="list-style-type: none"> •Announced 5/2003 •1.2 GHz •Up to 32 assignable cores •CP, IFL, ICF, zAAP •Up to 256 GB Memory 	<p>z9 Enterprise Class</p> <ul style="list-style-type: none"> •Announced 7/2005 •1.7 GHz •Up to 54 assignable cores •CP, IFL, ICF, zAAP, zIIP •Up to 512 GB Memory 	<p>z10 Enterprise Class</p> <ul style="list-style-type: none"> •Announced 2/2008 •4.4 GHz •Up to 64 assignable cores •CP, IFL, ICF, zAAP, zIIP •Up to 1.5 TB Memory 	<p>zEnterprise 196</p> <ul style="list-style-type: none"> •Announced 7/22/2010 •5.2 GHz •Up to 80 assignable cores •CP, IFL, ICF, zAAP, zIIP •Up to 3 TB Memory
				
<p>z800</p> <ul style="list-style-type: none"> •Announced 2/2002 •625 MHz •Up to 4 assignable cores •CP, IFL, ICF •Up to 32 GB Memory 	<p>z890</p> <ul style="list-style-type: none"> •Announced 4/2004 •1.0 GHz •Up to 4 assignable cores •CP, IFL, ICF, zAAP •Up to 32 GB Memory 	<p>z9 Business Class</p> <ul style="list-style-type: none"> •Announced 4/2006 •1.4 GHz •Up to 7 assignable cores •CP, IFL, ICF, zAAP, zIIP •Up to 64 GB Memory 	<p>z10 Business Class</p> <ul style="list-style-type: none"> •Announced 10/2008 •3.5 GHz •Up to 10 cfg cores (5 CP) •CP, IFL, ICF, zAAP, zIIP •Up to 248 GB Memory 	<p>zEnterprise 114</p> <ul style="list-style-type: none"> •Announced 7/12/2011 •3.8 GHz •Up to 10 cfg cores (5 CP) •CP, IFL, ICF, zAAP, zIIP •Up to 256 GB Memory

IBM zEnterprise EC12 – new for September 2012

IBM zEnterprise EC12 (2827)



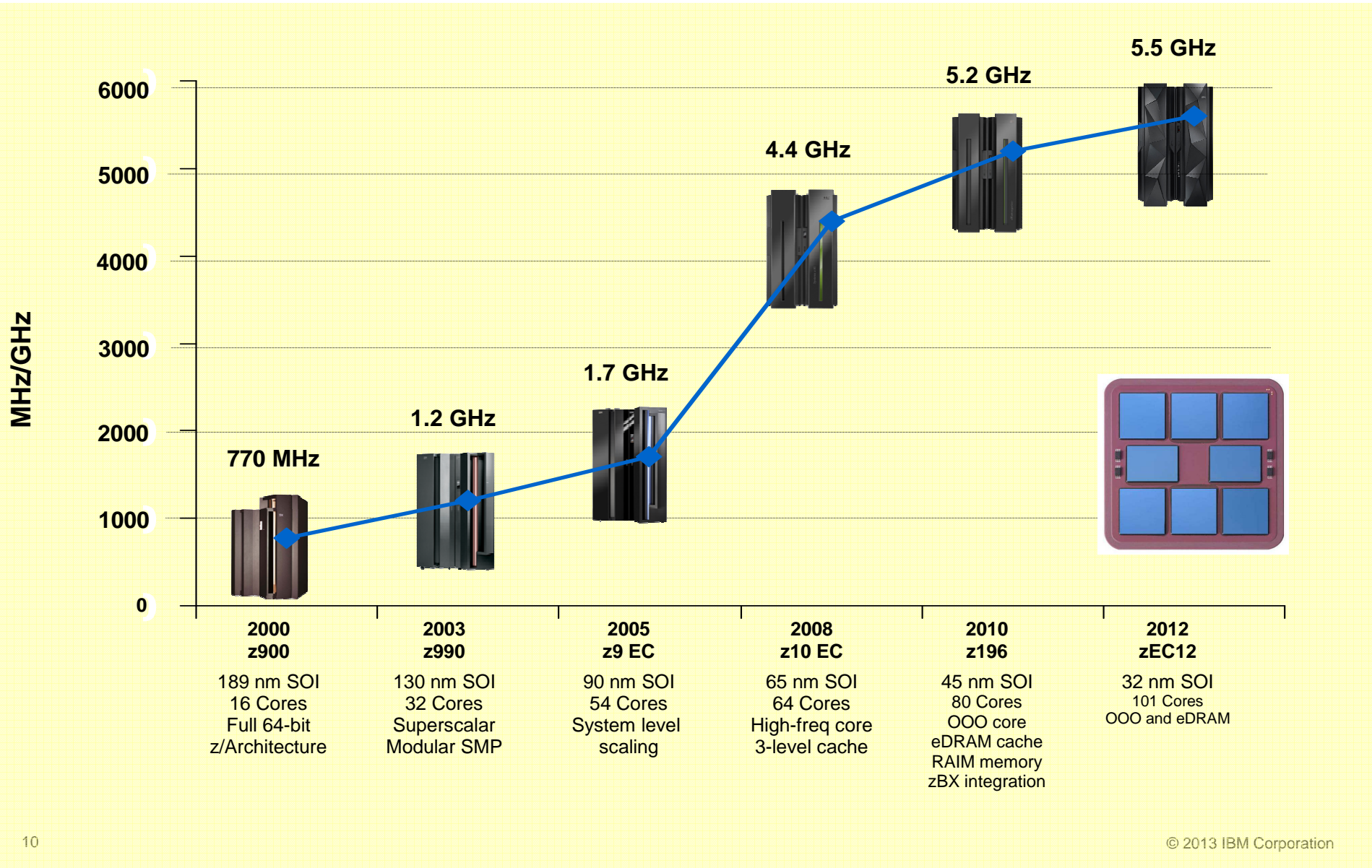
- Announced 08/12 – Server w/ up to 101 PU cores
- 5 models – Up to 101-way
- Granular Offerings for up to 20 CPs
- PU (Engine) Characterization
 - CP, SAP, IFL, ICF, zAAP, zIIP
- On Demand Capabilities
 - CoD, CIU, CBU, On/Off CoD, CPE, FoD
- Memory – up to 3 TB for Server and up to 1 TB per LPAR
 - 32 GB Fixed HSA
- Channels
 - PCIe bus
 - Four LCSSs
 - 3 Subchannel Sets
 - FICON Express8 and 8S
 - zHPF
 - OSA 10 GbE, GbE, 1000BASE-T
 - InfiniBand Coupling Links
 - Flash Express
- Configurable Crypto Express4S
- Parallel Sysplex clustering
- HiperSockets – up to 32
- Up to 60 logical partitions
- Enhanced Availability
- IBM zAware
- Unified Resource Manager
- Operating Systems
 - z/OS, z/VM, z/VSE, z/TPF, Linux on System z

IBM zEnterprise Blade Extension (2458)

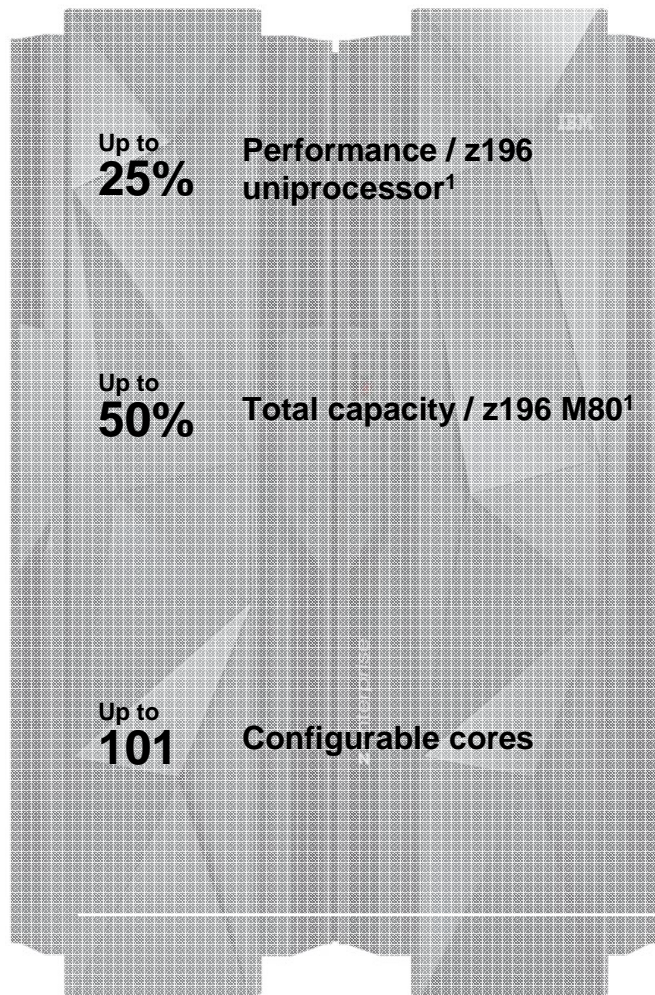


- First Announced 7/10
- Model 003 for zEC12 – 08/12
- zBX Racks with:
 - BladeCenter Chassis
 - N + 1 components
 - Blades
 - Top of Rack Switches
 - 8 Gb FC Switches
 - Power Units
 - Advance Management Modules
- Up to 112 Blades
 - POWER7 Blades
 - IBM System x Blades
 - IBM WebSphere DataPower Integration Appliance XI50 for zEnterprise (M/T 2462-4BX)
- Operating Systems
 - AIX 5.3 and higher
 - Linux for Select IBM x Blades
 - Microsoft Windows for x Blades
- Hypervisors
 - PowerVM Enterprise Edition
 - Integrated Hypervisor for System x

zEC12 Continues the CMOS Mainframe Heritage Begun in 1994

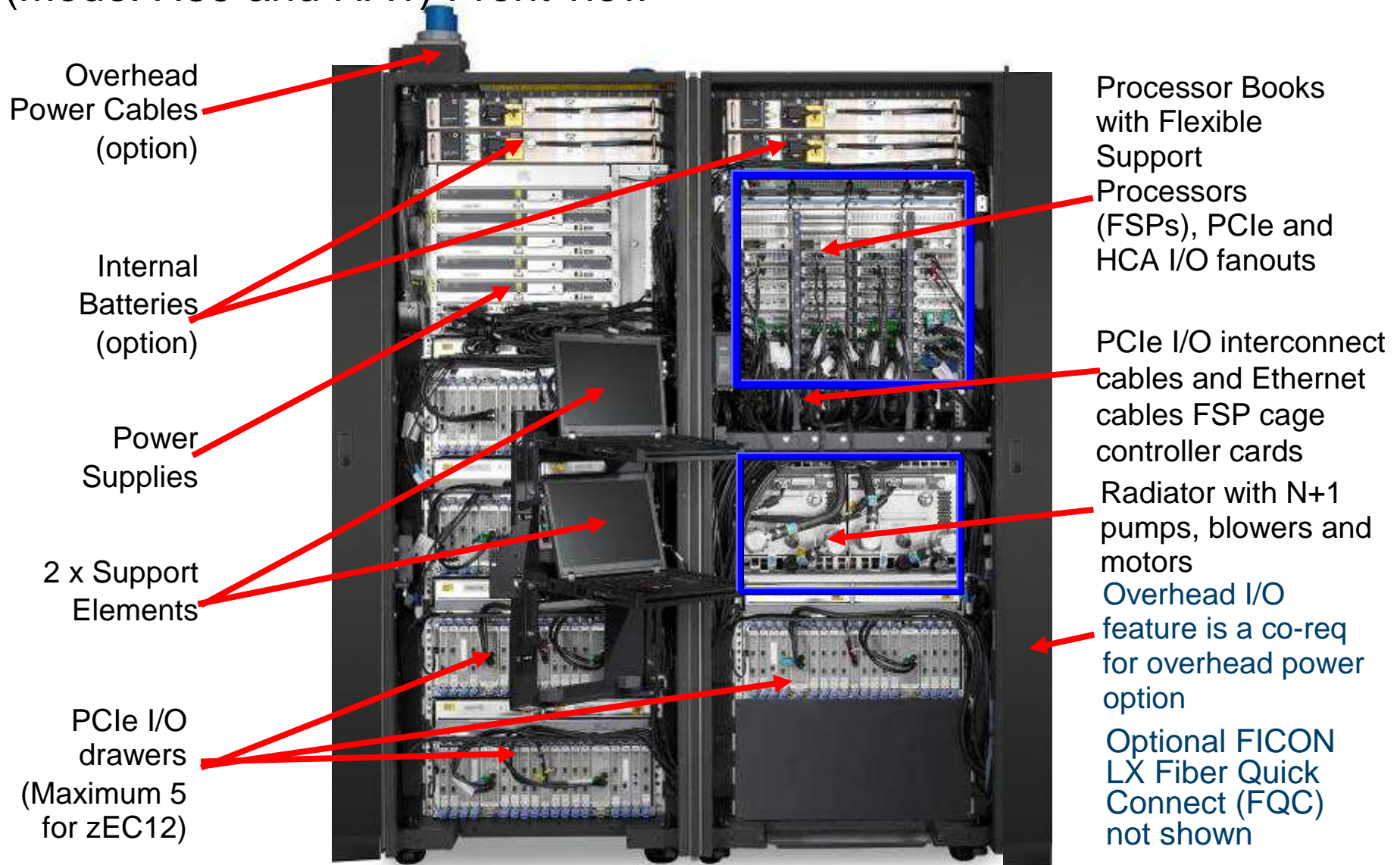


zEnterprise EC12 in one chart

zEC12*2827 Models: H20, H43, H66, H89, HA1*

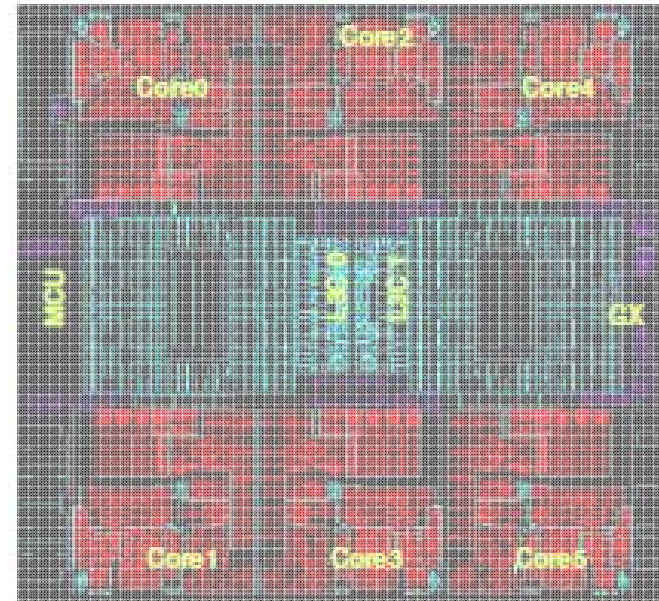
- Advanced Technology 5.5 GHz processor chip for performance boost for all workloads
 - Over **78,000 MIPS** for large scale consolidation
 - **Larger cache** for data serving
- Processor chip optimized for software performance
 - Advanced performance functions exploited by **Java, PL/I, compilers, DB2** and more
- Innovation to drive availability to superior levels
 - **IBM zAware**
 - **FLASH Express and pageable large pages**
- Security and reliability are in our DNA
 - High speed **cryptography integrated as part of the chip**
 - Enhanced support with new **Crypto Express4S**
 - PR/SM designed for **EAL5+ certification**

zEC12 New Build Radiator-based Air cooled – Under the covers (Model H89 and HA1) Front view



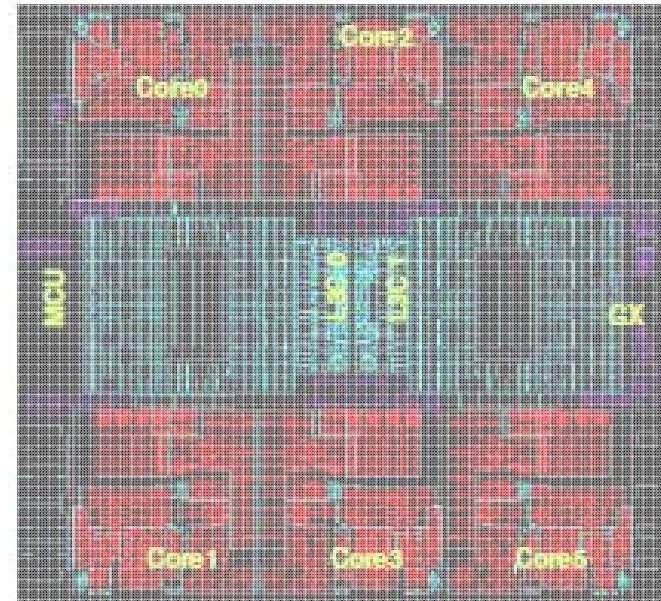
Processor chip optimized for software performance

- **Microprocessor design supports a boost in performance for all workloads**
 - Second generation out of order design

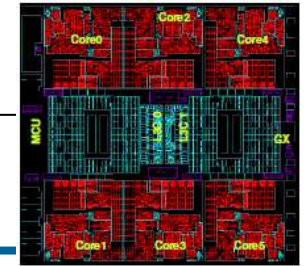


Processor chip optimized for software performance

- Microprocessor design supports a boost in performance for all workloads
- **Larger caches to optimize data serving environments**
 - Almost 2x on chip and 2x additional on book



z196 MCM vs zEC12 MCM Comparison



z196 MCM

- MCM

- 96mm x 96mm in size

- 6 PU chips per MCM

- Quad core chips with 3 or 4 active cores
 - PU Chip size 23.7 mm x 21.5 mm
 - 5.2 GHz
 - Superscalar, OoO execution
 - L1: 64 KB I / 128 KB D private/core
 - L2: 1.5 MB I+D private/core
 - L3: 24 MB/chip – shared

- 2 SC chips per MCM

- L4: 2 x 96 MB = 192 MB L4 per book
 - SC Chip size 24.5 mm x 20.5 mm

- 1800 Watts

zEC12 MCM

- MCM

- 96mm x 96mm in size

- 6 PU chips per MCM

- Hex-core chips with 4 to 6 active cores
 - PU Chip size 23.7mm x 25.2mm
 - 5.5 GHz
 - Superscalar, OoO enhanced
 - L1: 64 KB I / 96 KB D private/core
 - L2: 1 MB I / 1 MB D private/core
 - L3: 48 MB/chip - shared

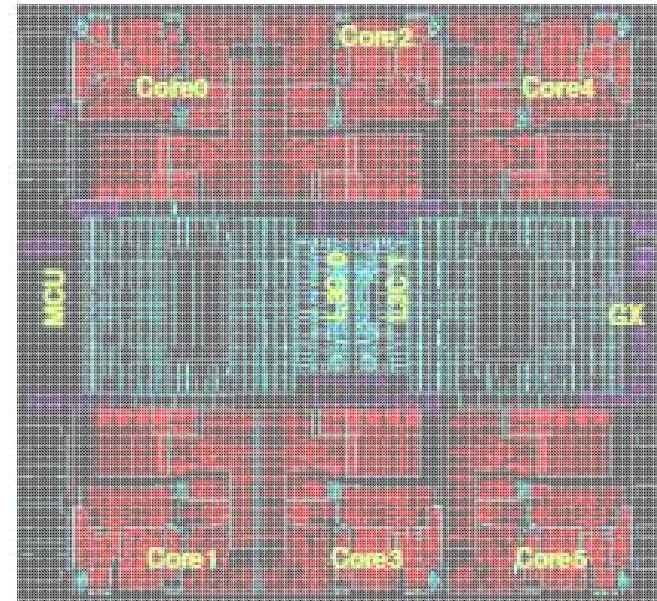
- 2 SC chips per MCM

- L4: 2 x 192 MB = 384 MB L4 per book
 - SC Chip size 28.4mm x 23.9mm

- 1800 Watts

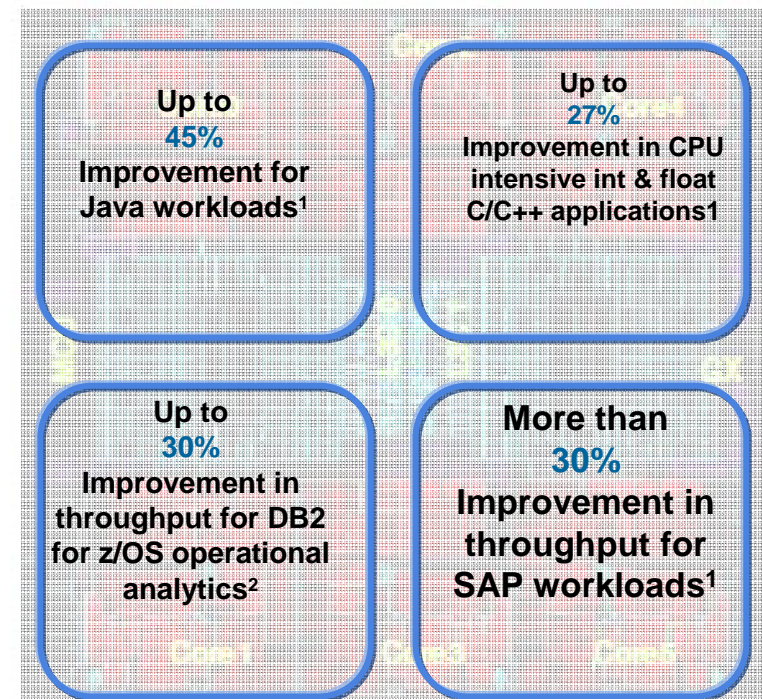
Processor chip optimized for software performance

- Microprocessor design supports a boost in performance for all workloads
- Larger caches to optimize data serving environments
 - Almost 2x on chip and 2x additional on book
- New hardware functions optimized for software performance
 - **Transactional Execution Facility** for parallelism and scalability
 - **Runtime Instrumentation Facility**
 - **2 GB page frames**
 - Up to **30% improvement in IMS throughput**¹
 - New IBM Enterprise PL/I compiler for Decimal format conversions

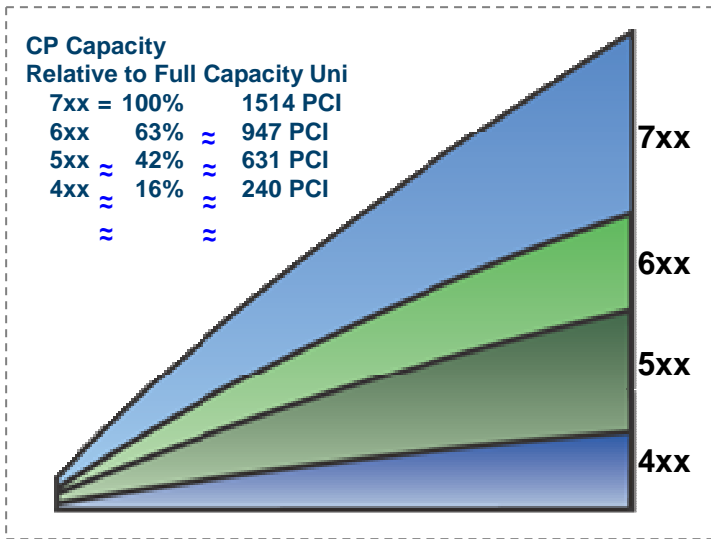


Processor chip optimized for software performance

- **Microprocessor design supports a boost in performance for all workloads**
- **Larger caches to optimize data serving environments**
 - Almost 2x on chip and 2x additional on book
- **New hardware functions optimized for software performance**
 - *Transactional Execution Facility* for parallelism and scalability
 - *Runtime Instrumentation Facility*
 - **2 GB page frames**
 - Up to **30% improvement in IMS throughput**¹
 - New IBM Enterprise PL/I compiler for Decimal format conversions

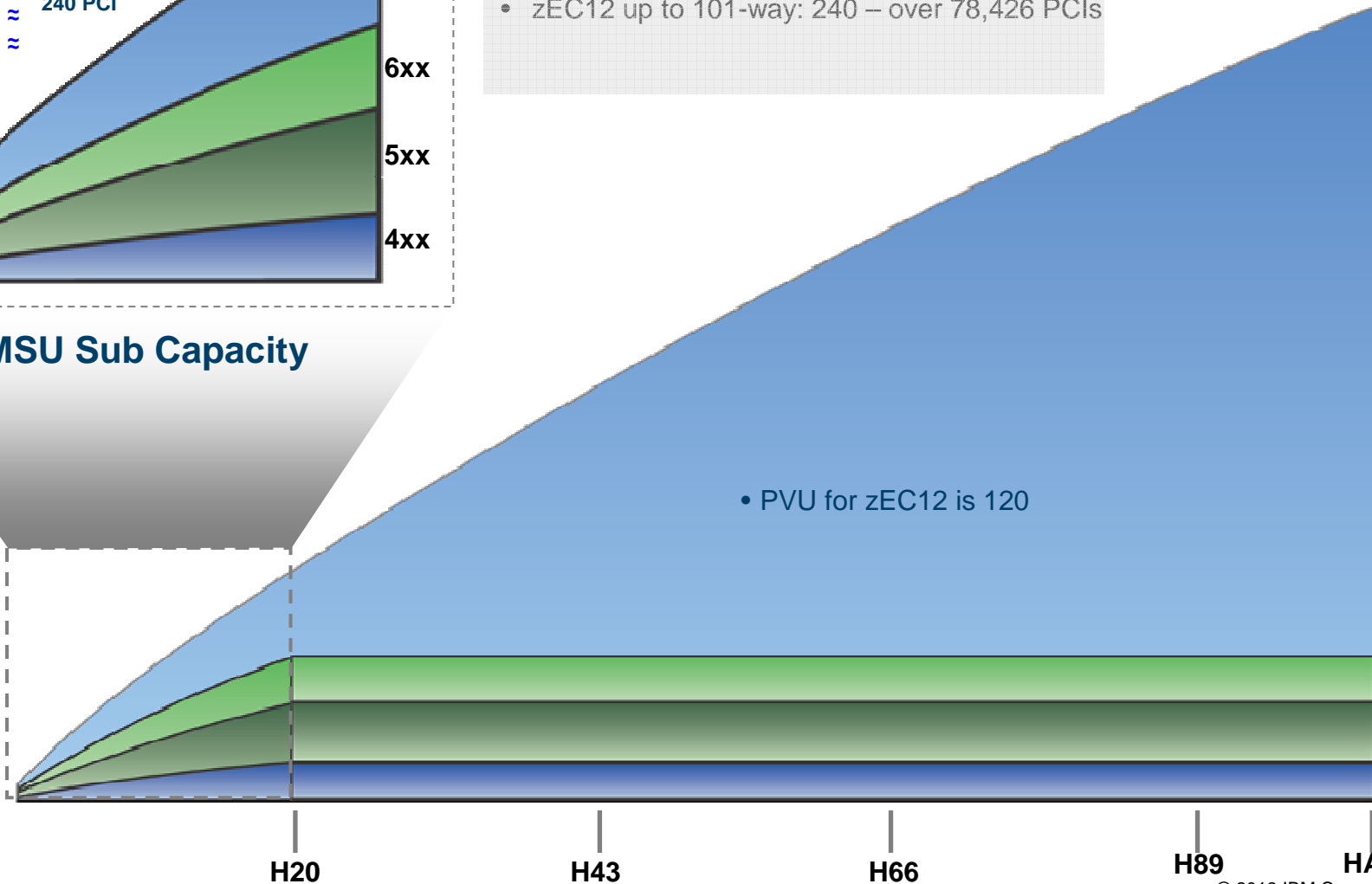


zEC12 Full and Sub-Capacity CP Offerings



- z9 EC up to 54-way: 193 – 18,505 PCIs
- z10 EC up to 64-way: 214 – 31,826 PCIs
- z196 up to 80-way: 240 – 52,286 PCIs
- zEC12 up to 101-way: 240 – over 78,426 PCIs

MSU Sub Capacity



zEC12 Processor Unit allocation/usage

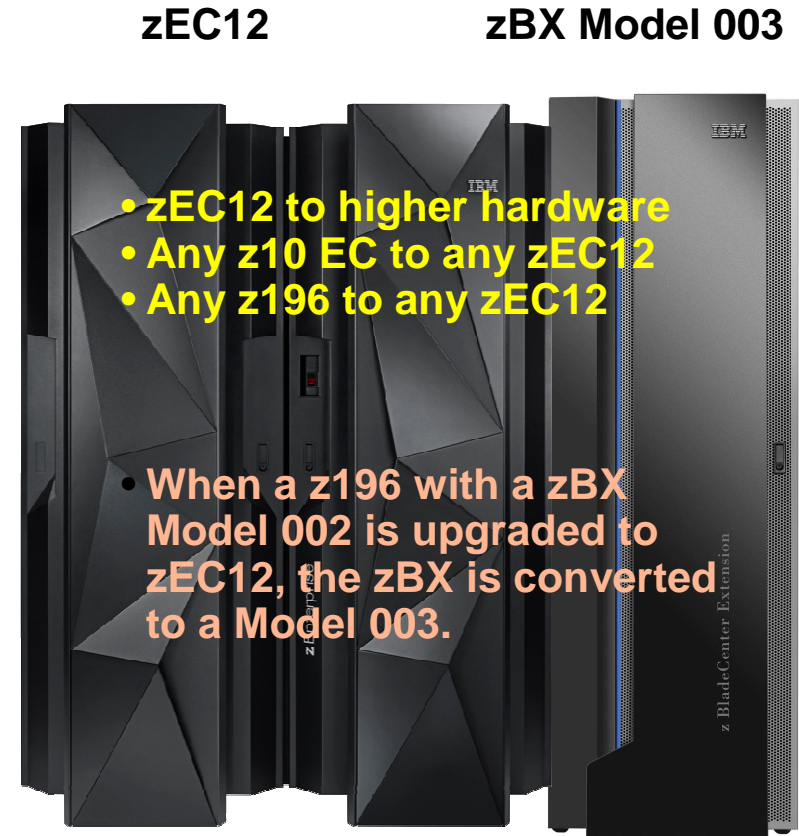
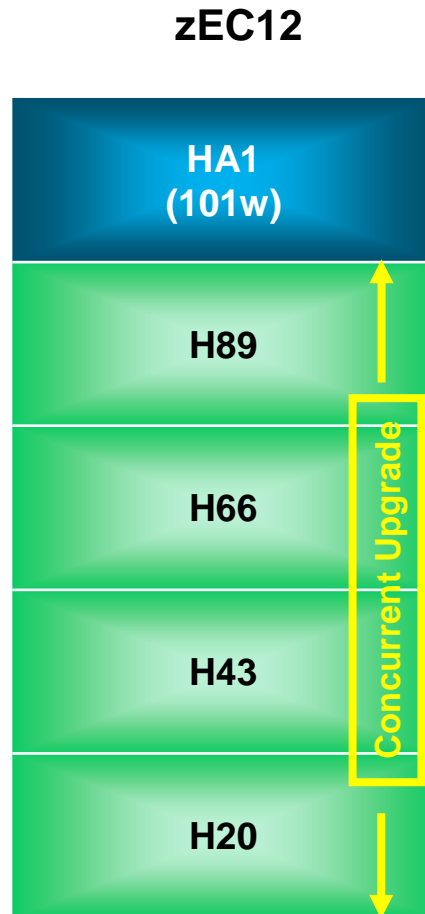
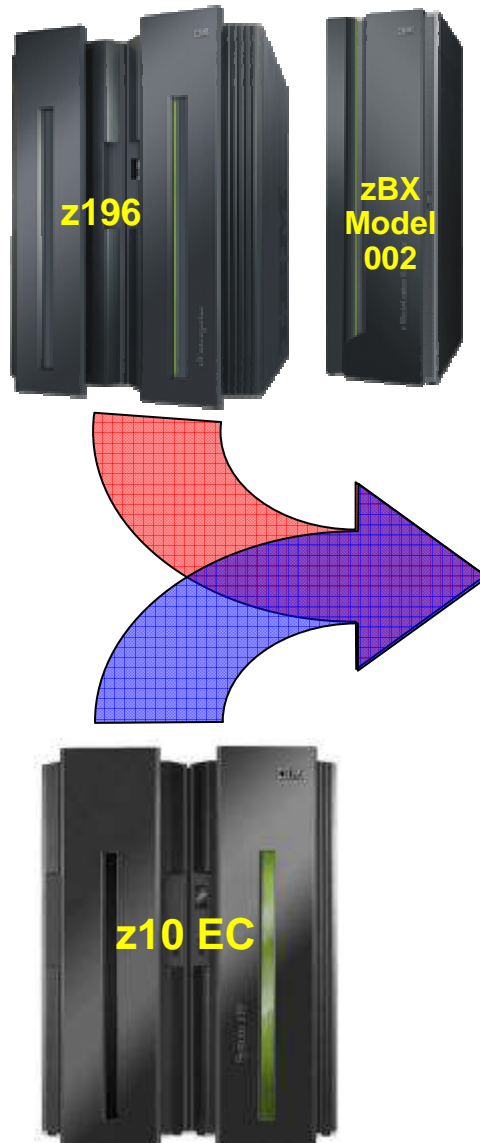
Model	Books/ PUs	CPs	IFLs uIFLs	zAAPs	zIIPs	ICFs	Std SAPs	Optional SAPs	Std. Spares	Rsvd. PUs
H20	1/27	0-20	0-20 0-19	0-10	0-10	0-20	4	0-4	2	1
H43	2/54	0-43	0-43 0-42	0-21	0-21	0-43	8	0-8	2	1
H66	3/81	0-66	0-66 0-65	0-33	0-33	0-66	12	0-12	2	1
H89	4/108	0-89	0-89 0-88	0-44	0-44	0-89	16	0-16	2	1
HA1	4/120	0-101	0-101 0-100	0-50	0-50	0-101	16	0-16	2	1

zEC12 Purchase Memory Offerings

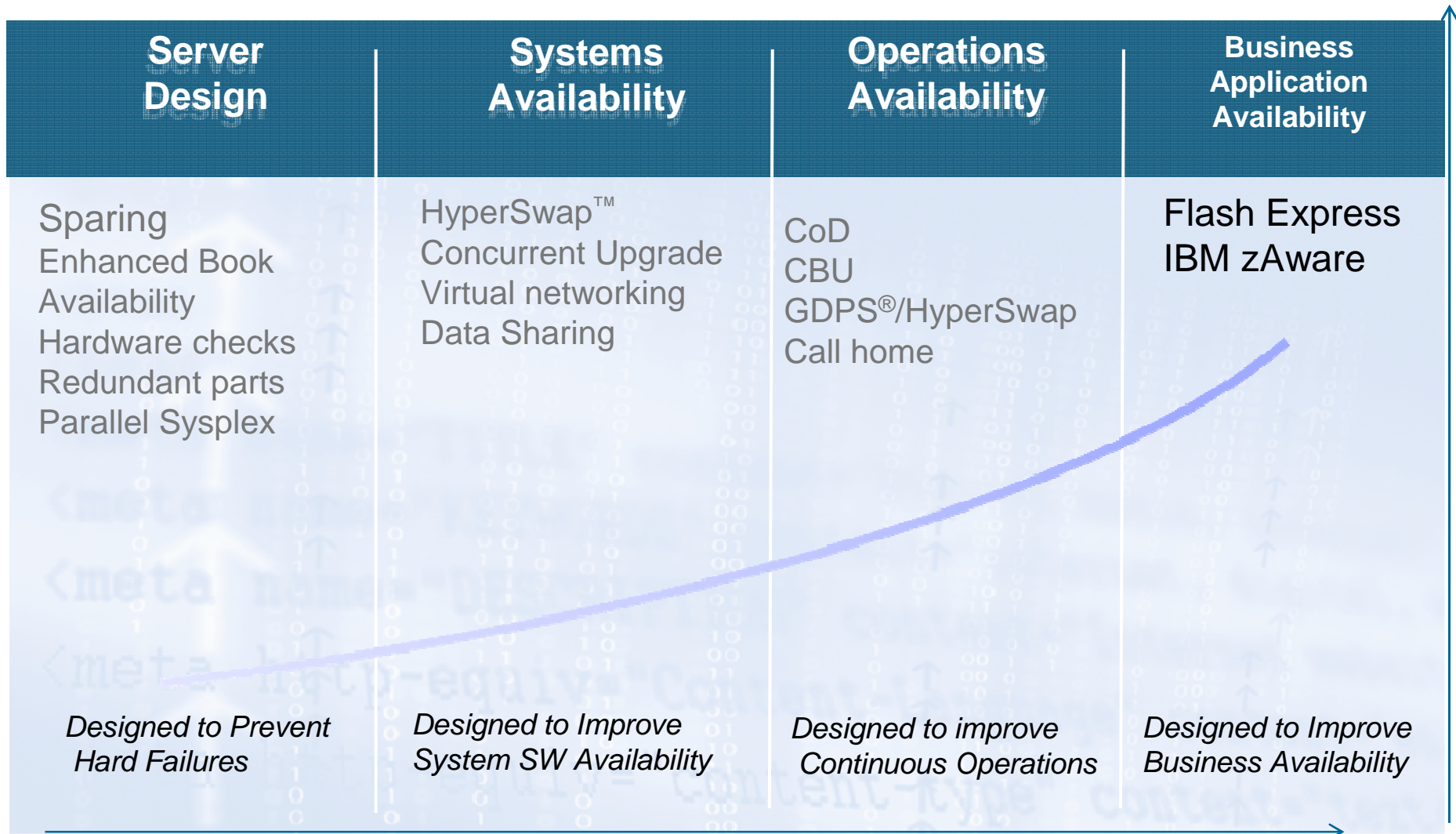
Model	Standard Memory GB	Flexible Memory GB	Plan Ahead Memory GB
H20	32 - 704	NA	32-704
H43	32 - 1392	32 - 704	96 - 1392
H66	32 - 2272	32 - 1392	64 - 2272
H89	32 - 3040	32 - 2272	96 - 3040
HA1	32 - 3040	32 - 2272	96 - 3040

- **Purchase Memory** - Memory available for assignment to LPARs
- **Hardware System Area** – Standard 32 GB outside customer memory for system use
- **Standard Memory** - Provides minimum physical memory required to hold base purchase memory plus 32 GB HSA
- **Flexible Memory** - Provides additional physical memory needed to support activation base customer memory and HSA on a multiple book zEC12 with one book out of service.
- **Plan Ahead Memory** – Provides additional physical memory needed for a concurrent upgrade (LIC CC change only) to a preplanned target customer memory

zEC12 Upgrades



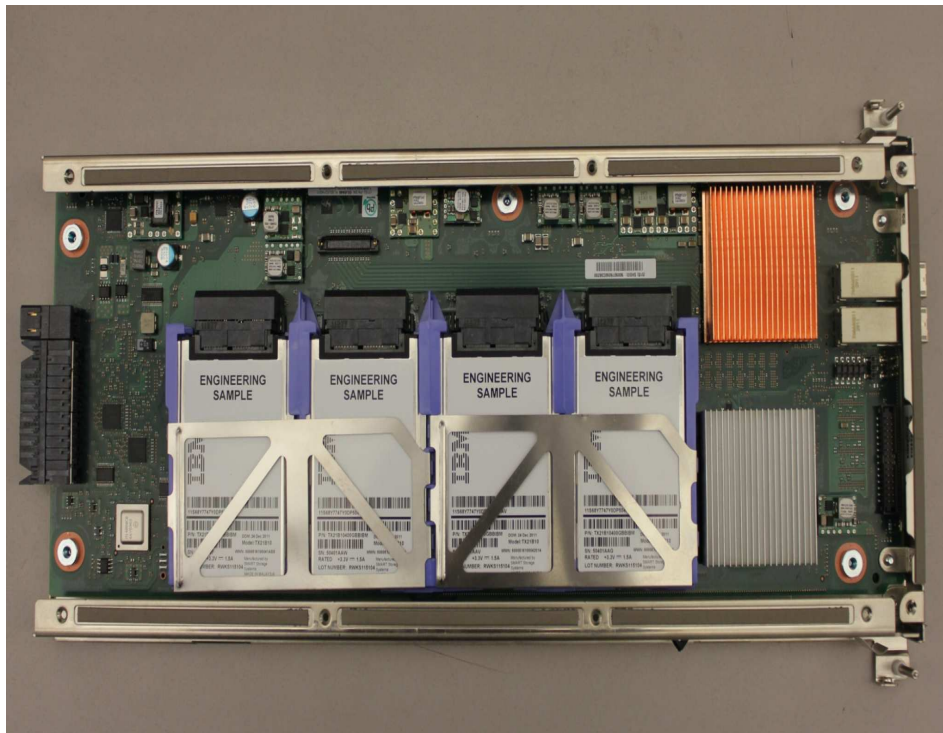
Extending System z Availability with Flash Express and IBM zAware





Flash Express

Flash Express PCIe Adapter Card



More Latency

Time to Read Data measured in System z Instructions
Real Memory: (256B line) ~100 Instructions
Flash Memory (4K page) ~100K Instructions
External Disk (4K page) ~5,000K Instructions

Flash Express strengthens availability



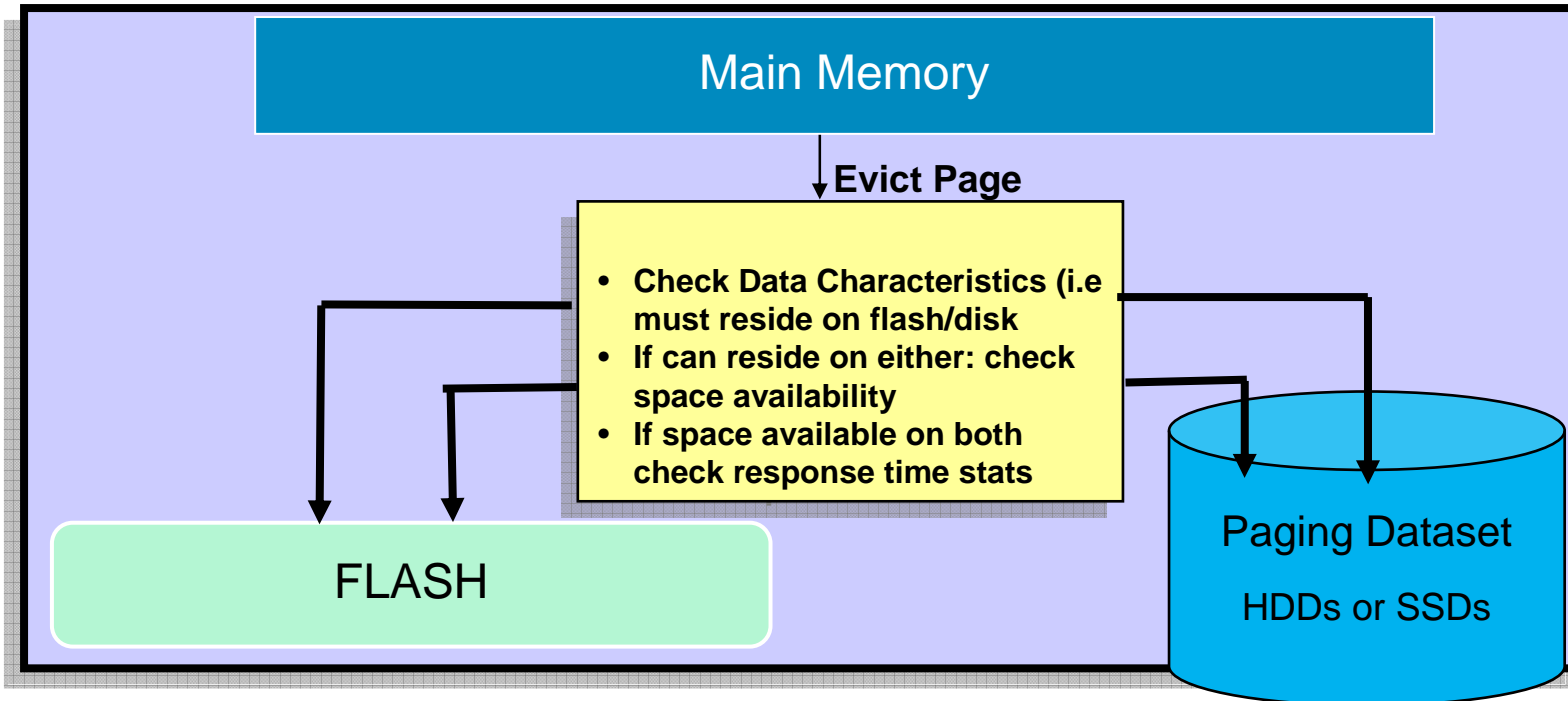
- Innovation to drive availability to exceptional levels
 - Is an *industry unique* application of Flash to improve availability
- Flash Express can improve availability and reduce latency
 - Improves availability during transition periods and spikes
 - Helps accelerate start of day processing - batch to online
 - Enables faster snapshots of diagnostics (e.g. SVC dump, SAD dump)
 - With pageable large pages can improve performance of DB2 and Java
 - Ideal for applications with random read access and high read/write ratios.

Flash Express strengthens availability



- Innovation to drive availability to exceptional levels
- Flash Express can improve availability and reduce latency
 - Improves availability during transition periods and spikes
 - Helps accelerate start of day processing - batch to online
 - Enables faster snapshots of diagnostics (e.g. SVC dump, SAD dump)
 - With pageable large pages can improve performance of DB2 and Java
 - Ideal for applications with random read access and high read/write ratios.
- Minimal configuration- no special skills needed
 - Usable immediately; no special training required
 - Easy to set up and dynamically configurable.

Flash vs Disk Placement Criteria



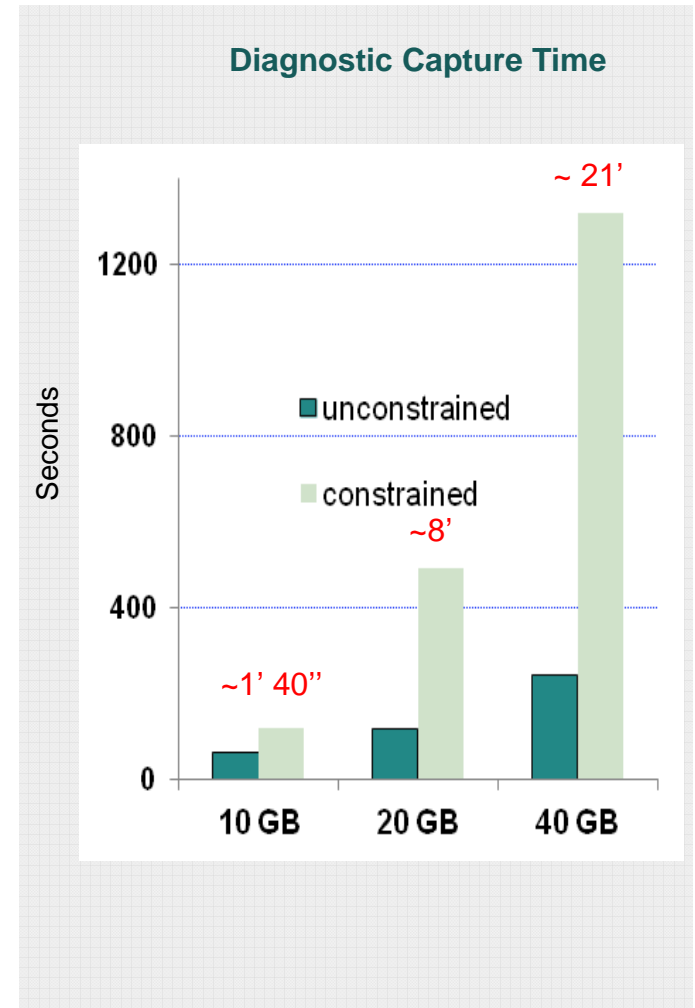
Data Type	Data Page Placement
Pageable Link Pack Area (PLPA)	At IPL/NIP time PLPA pages will be placed both on flash and disk.
VIO	VIO data will always be placed on disk (First to VIO accepting datasets with any spillover flowing to nonvio datasets)
HyperSwap Critical Address Space data	If flash space is available, all virtual pages belonging to a HyperSwap Critical Address Space will be placed on flash memory. If flash space is not available, these pages will be kept in memory and only paged to disk when the system is real storage constrained and no other alternatives exist
Pageable Large Pages	If contiguous flash space is available, pageable large pages will be preferentially written to flash.
All other data	If available space exists on both flash and disk then make a selection based on response time.

Performance benefits from application of Flash Express

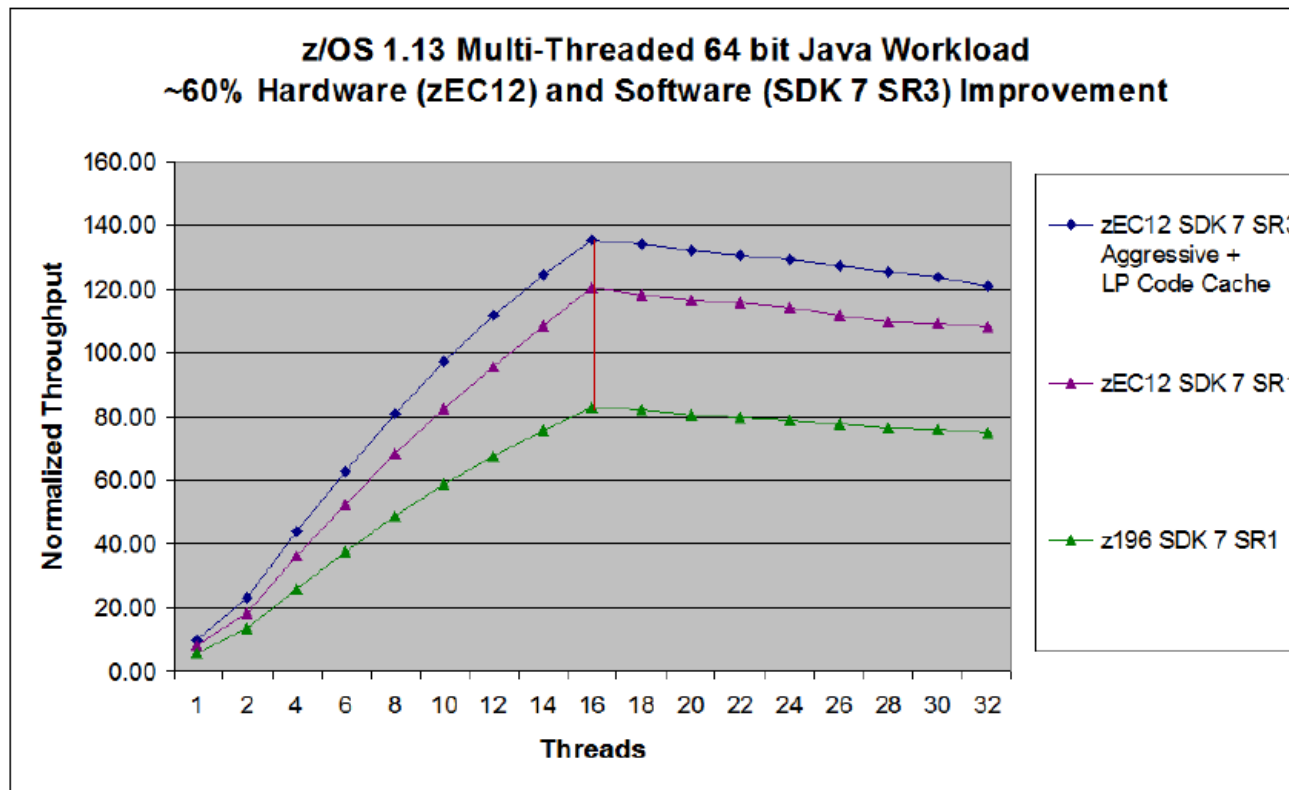
- Achieve outstanding availability
 - Designed to improve availability and improve paging performance
 - Achieve CPU performance benefits from use of pageable large pages

- Expected Benefits based on estimates only *
 - **DB2:** *Estimated* incremental (up to 3%) System CPU for PLP
 - **Java:** *Estimate* up to 3-5% System CPU benefit for PLP
 - **IMS:** expected exploitation for common queues

- Longer roadmap
 - Continued optimization of 1MB pageable large pages vs. 4K pages
 - Additional exploitation expected by Linux® and middleware
 - Available for ISV exploitation



Flash Express and z/OS Java SDK 7: Performance up to 60% Improvement 64-bit Java Multi-threaded Benchmark on 16-Way

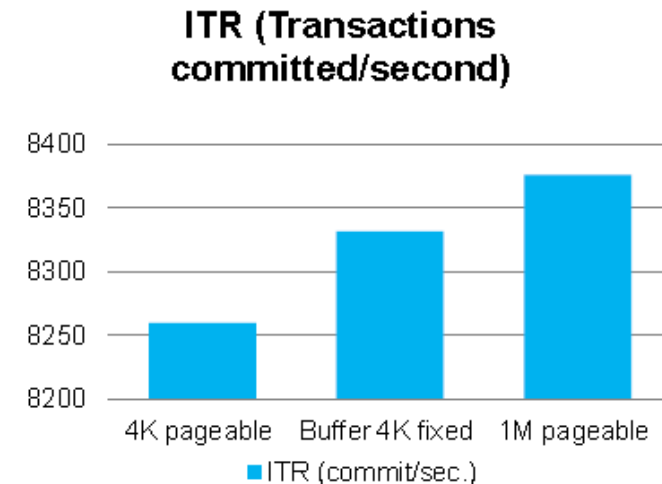


Aggregate 60% improvement from zEC12 and Java7SR3

- zEC12 offers a ~45% improvement over z196 running the Java Multi-Threaded Benchmark
- Java7SR3 offers an additional ~13% improvement (-%Aggregate + Flash Express + pageable 1Meg large page)

Flash Express with zEC12 and DB2

- **Faster CPU – 1.25X compared to z196**
- **50% More System Capacity**
- **New Features DB2 plans to exploit**
 - FLASH Express and 1MB Pageable Large Pages
 - Larger DB2 Buffer Pools
 - 2GB frame support
 - Larger frames expected to provide additional CPU savings, especially for very large memory
 - DB2 code backed by large frames for CPU reductions
- Transactional Execution opportunities for performance gains
- Initial support planned for DB2 10 with APARS



DB2 transaction throughput improvement stems from reduced CPU needed for buffer pool management

❖ Up to 28% improvement in DB2™ throughput due to faster CPU and leveraging Flash Express with Pageable Large Pages (PLP)*

❖ Workloads leveraging Flash Express with PLP can see up to a 8% price performance improvement over the z196.**

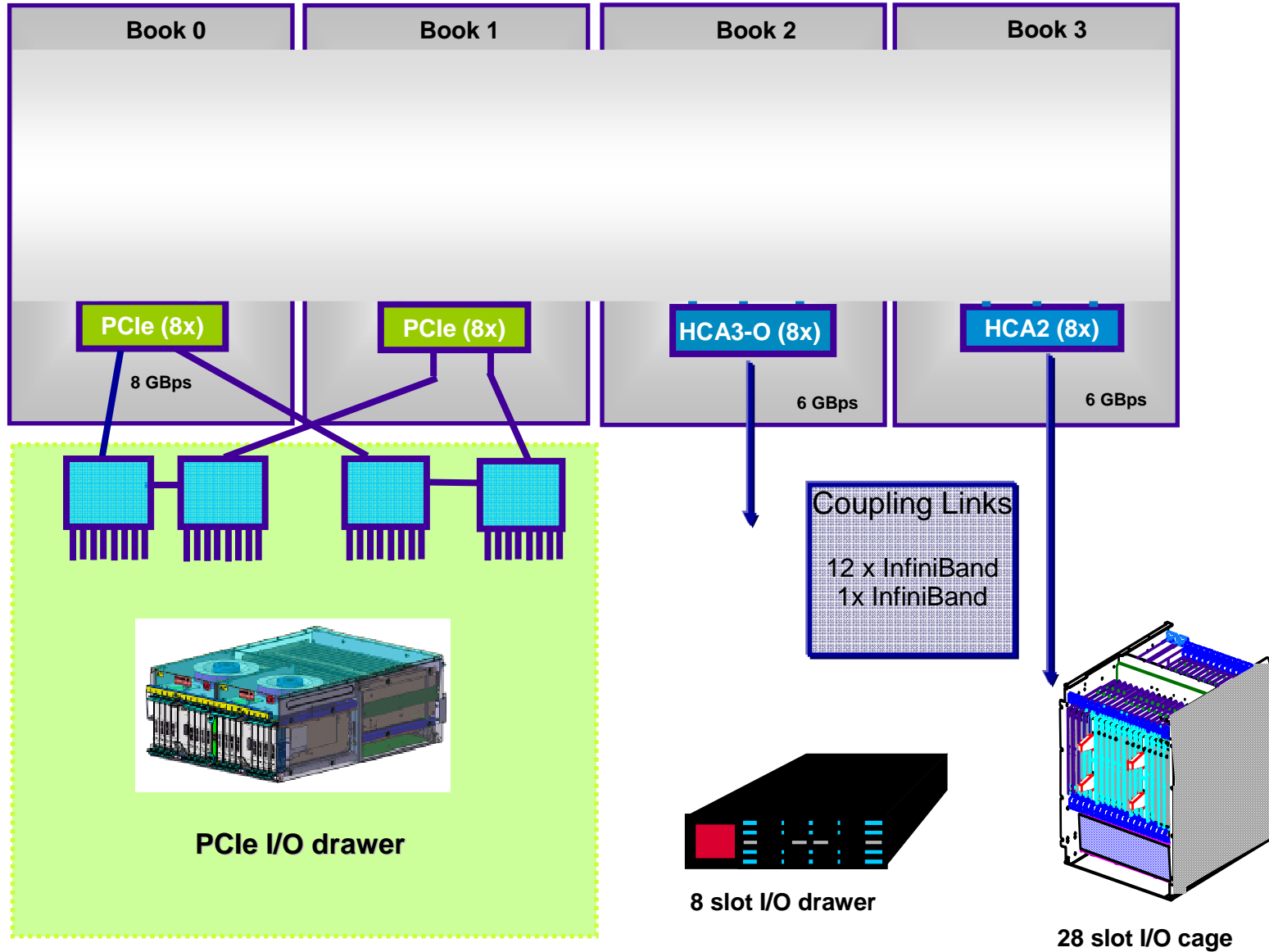
* PLP for DB2 helps DB2 to achieve "additional" up to 3% additional performance on top of zEC12 CPU expected throughput improvements of 25%.

** based on average 5% discount for zEC12 workloads under the AWLC pricing plus up to 3% more performance per MSU with Flash Express.

zEC12 Internal I/O Infrastructure

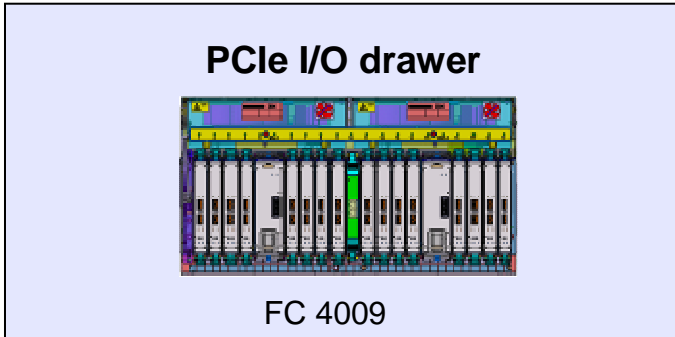


zEC12 I/O infrastructure

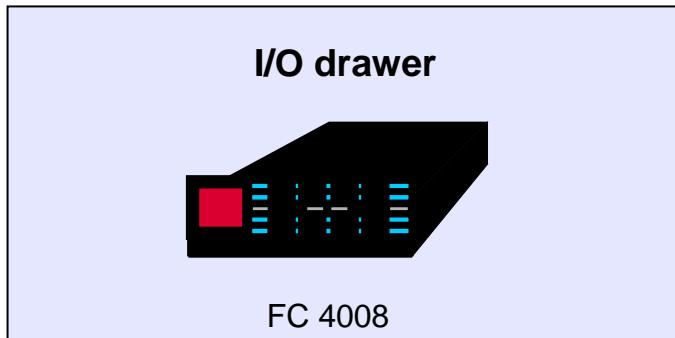


zEC12 I/O Drawers and Cages

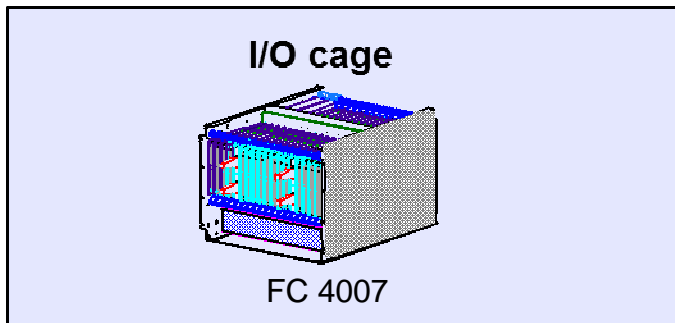
eConfig determines I/O drawer/cage mix and frame placement !



- 4 I/O domains
 - 32 I/O slots (PCIe I/O cards only)
 - At least two PCIe fanouts (4 ports per drawer)
 - 7 EIA Units



- 2 I/O domains
 - 8 I/O slots (legacy I/O cards only)
 - At least 2 HCA2-C fanouts (2 ports per drawer)
 - Up to two drawers on a pair of fanouts
 - 5 EIA Units



- 7 I/O domains
 - 28 I/O slots (legacy I/O cards only)
 - Up to 4 fanouts (z9 and later Systems) for all 7 domains
 - 14 EIA Units

zEC12 GA1 Features Supported – I/O Cage, I/O Drawer, PCIe I/O Drawer

Supported features

- Features – PCIe I/O drawer

- Crypto Express4S
- Flash Express
- FICON Express8S
 - SX and LX
- OSA-Express4S
 - 10 GbE LR and SR
 - GbE SX, LX
 - 1000BASE-T

PCIe I/O drawer

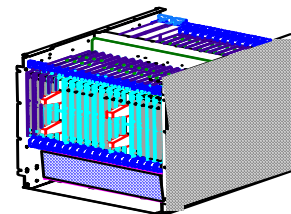


32 I/O slots

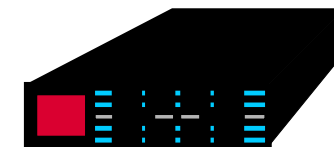
- Features – I/O cage and I/O drawer

(Carry Forward ONLY on System MES – Maximum of 44 features. No ADDs)

- **Not Supported:** ESCON, older FICON, FICON Express4 LX 4 km, OSA-Express2, PSC
- Crypto Express3
- FICON Express8
- FICON Express4 10 km LX and SX
- ISC-3
- OSA-Express3
 - 10 GbE, GbE, 1000BASE-T



28 slot I/O cage



8 slot I/O drawer

zEC12 Storage Connectivity Options

Description	F/C	Ports	Available	Comments
FICON Express8S 10KM LX	0409	2	New and carry forward	Carry forward from z196/z114
FICON Express8S SX	0410	2	New and carry forward	Carry forward from z196/z114
FICON Express8 10KM LX	3325	4	Carry Forward only	Carry forward from z196/z114/z10
FICON Express8 SX	3326	4	Carry Forward only	Carry forward from z196/z114/z10
FICON Express4 10KM LX	3321	4	Carry Forward only	Carry forward from z196/z114/z10
FICON Express4 SX	3322	4	Carry Forward only	Carry forward from z196/z114/z10

Maximum FICON features varies with mix of Cages/Drawers types and Model of the System

All use LC Duplex connectors

Open Systems Adapter in the PCIe I/O drawer (FC4009)

Description	Feature Code	Ports	Available	CHPID
OSA-Express4S GbE LX	0404	2 ¹	New Build	OSD
OSA-Express4S GbE SX	0405	2 ¹	New Build	OSD
OSA-Express4S 10 GbE LR	0406	1	New Build	OSD, OSX
OSA-Express4S 10 GbE SR	0407	1	New Build	OSD, OSX
OSA-Express4S 1000BASE-T	0408	2 ¹	New Build	OSC, OSD, OSE, OSM, OSN

Open Systems Adapter in the I/O cage (FC4007) or I/O drawer (FC4008)

Description	Feature Code	Ports	Available	CHPID
OSA-Express3 GbE LX	3362	4 ¹	Carry Forward	OSD, OSN
OSA-Express3 GbE SX	3363	4 ¹	Carry Forward	OSD, OSN
OSA-Express3 1000BASE-T	3367	4 ¹	Carry Forward	OSD, OSE, OSC, OSN, OSM
OSA-Express3 10 GbE LR	3370	2	Carry Forward	OSD, OSX
OSA-Express3 10 GbE SR	3371	2	Carry Forward	OSD, OSX

¹ Two ports per CHPID

zEC12 Non-PSIFB Coupling Links

Description	F/C	Ports	Available	Comments
ISC-D	0217	N/A	Carry Forward	Mother Card
ISC-D	0218	1 to 2	Carry Forward	ISC-D (Daughter Card)
ISC-3 Link	0219	1 to 4	Carry Forward	Port(s) Enabled
ISC-D RPQ	8P2197		Carry Forward	ISC-3 20KM
ICB-3	0993		Not Available	
ICB-4	3393		Not Available	

**The zEC12 is the last server to support ISC-3 features.
ISC-3 requires an I/O Drawer or I/O Cage**

zEC12 InfiniBand Coupling Fanouts

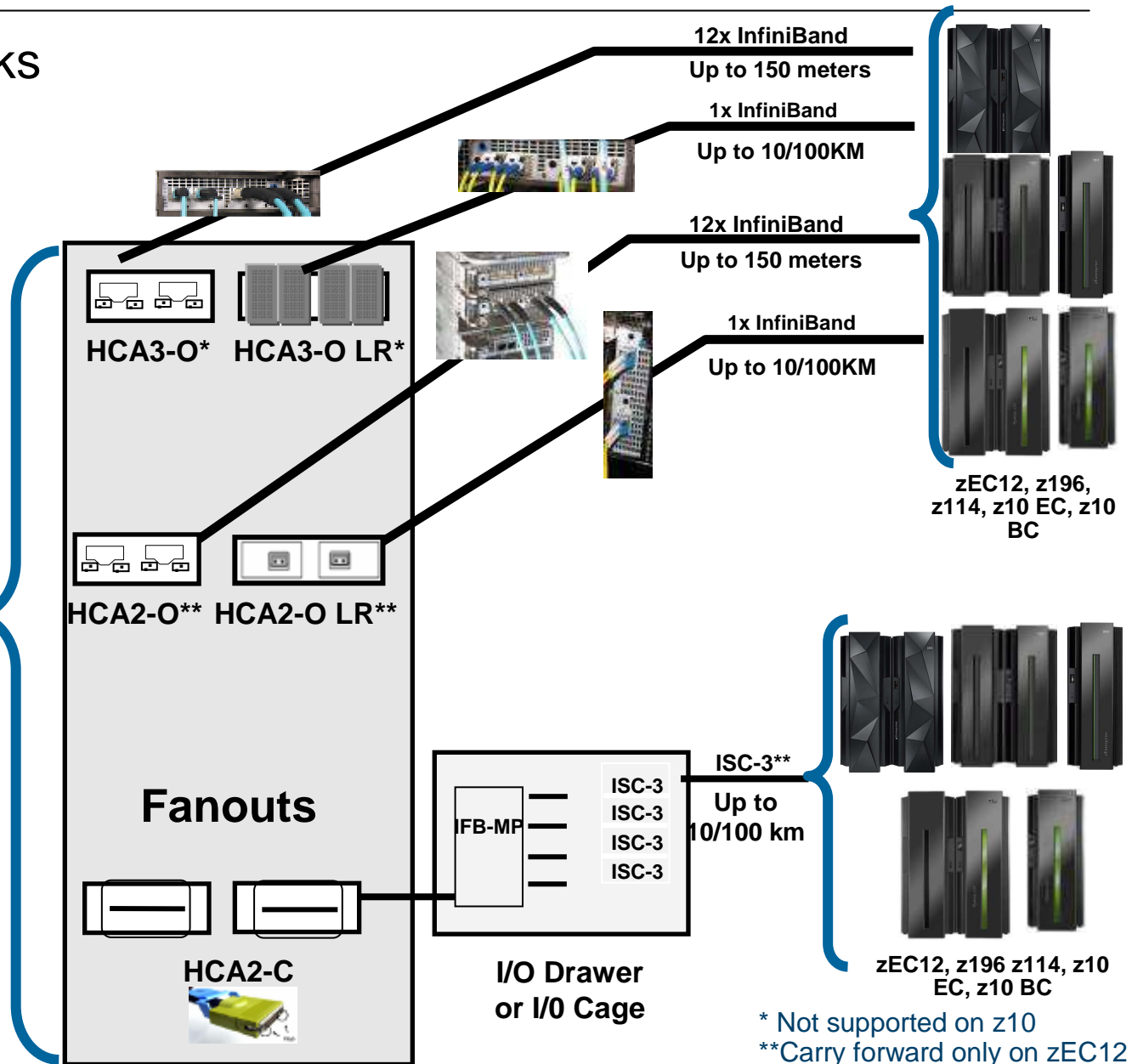
Description	F/C	Ports	Comments
HCA3-O LR 1x InfiniBand DDR	0170	4	PSIFB coupling (10 km unrepeated, 100 km with DWDM) Double port density. 32 subchannels per CHPID
HCA3-O 12x InfiniBand DDR	0171	2	PSIFB coupling (150 m) Improved IFB3 protocol (HCA3-O to HCA3-O)
HCA2-O 12x IB-DDR Carry Forward only	0163	2	Coupling (150 meters)
HCA2-O LR 1x IB-DDR Carry Forward only	0168	2	Coupling (10 km unrepeated, 100 km with DWDM)
<p>Note: Coupling fanouts compete for slots with the HCA2-C and PCIe fanouts for I/O drawers and cages.</p>			

Note: The InfiniBand link data rates do not represent the performance of the link. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.



zEC12 Coupling Links

- Fanout, not I/O slot, used for InfiniBand
- ICB-4 – No longer supported
- ETR – No longer supported
- All coupling links support STP
- Sysplex Coexistence – zEC12, z196, z114, z10 EC and BC only



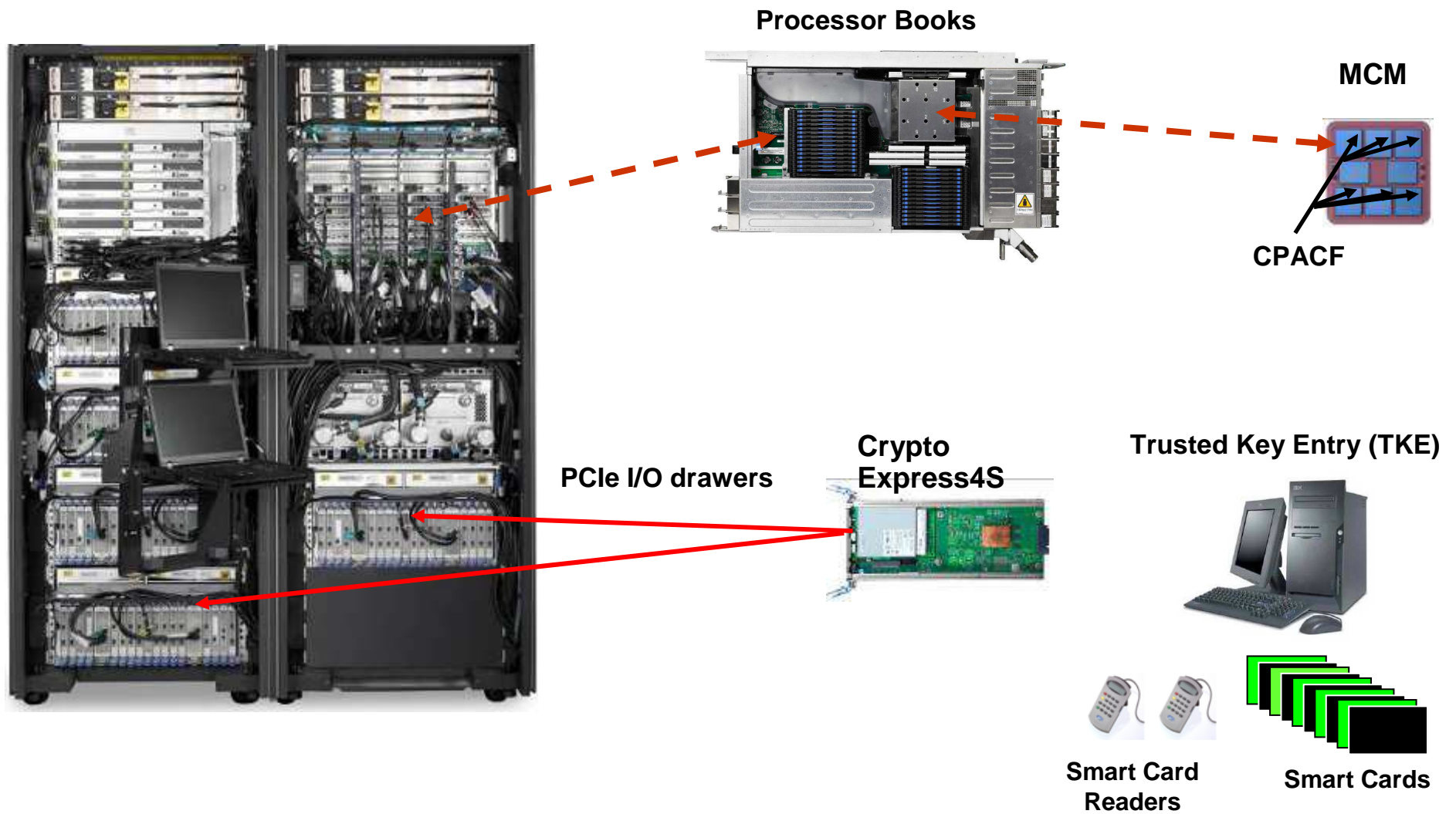
* Not supported on z10
 **Carry forward only on zEC12

IBM System z Security as the Enterprise Standard

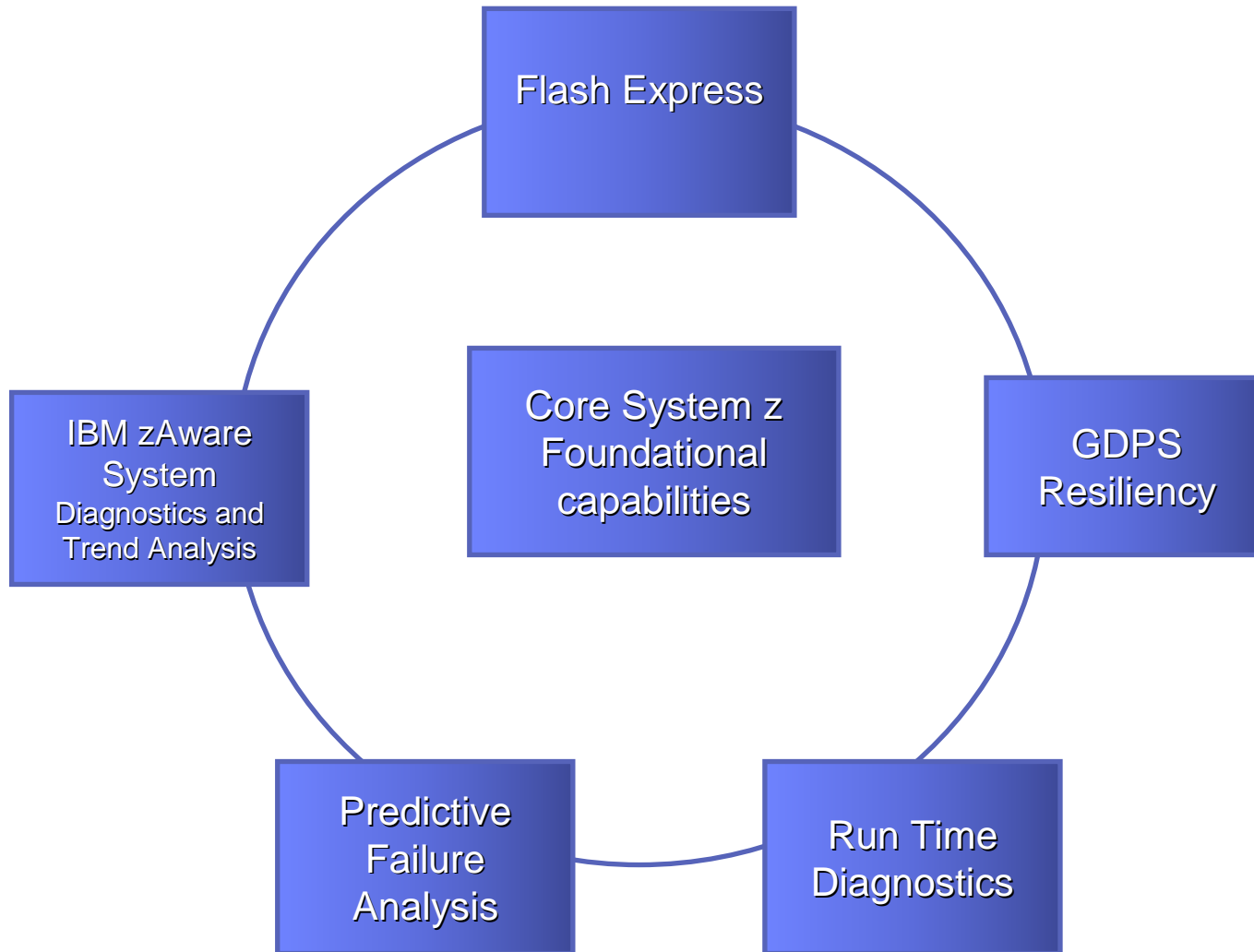


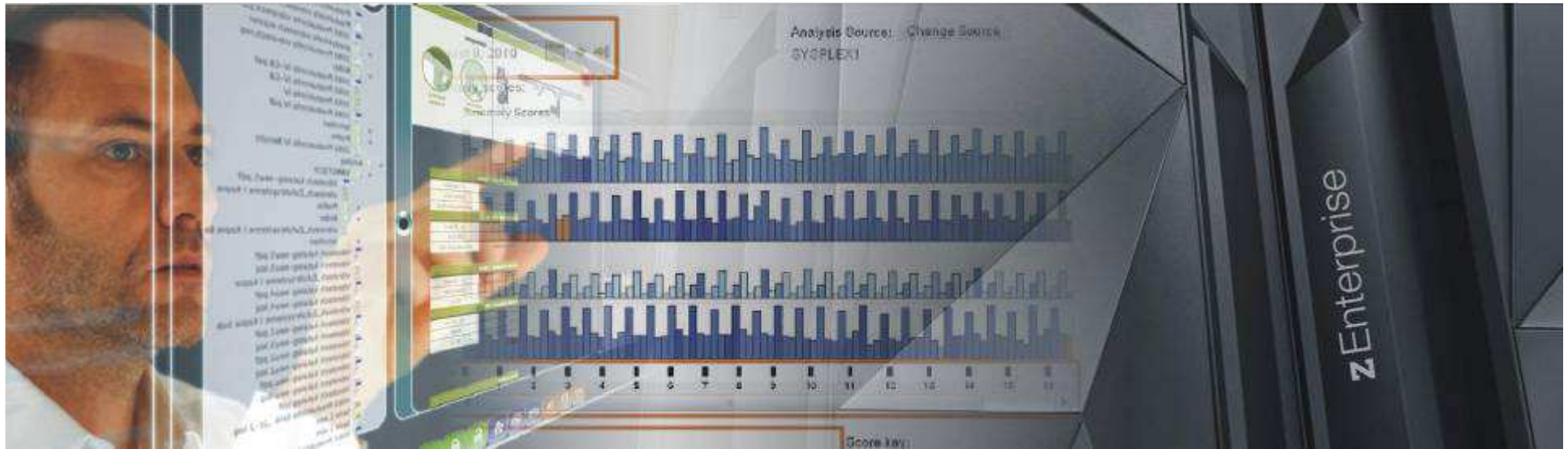
- High speed cryptography integrated on the new Crypto Express4S chip
- Digital signature: new Enterprise PKCS #11 to meet regulatory requirements
- Integration of mainframe security events with IBM zSecure Suite and QRadar
- Designed to maintain EAL5+ common criteria certification – the highest in the industry

Overview – HW Crypto support in System zEC12



System z Availability

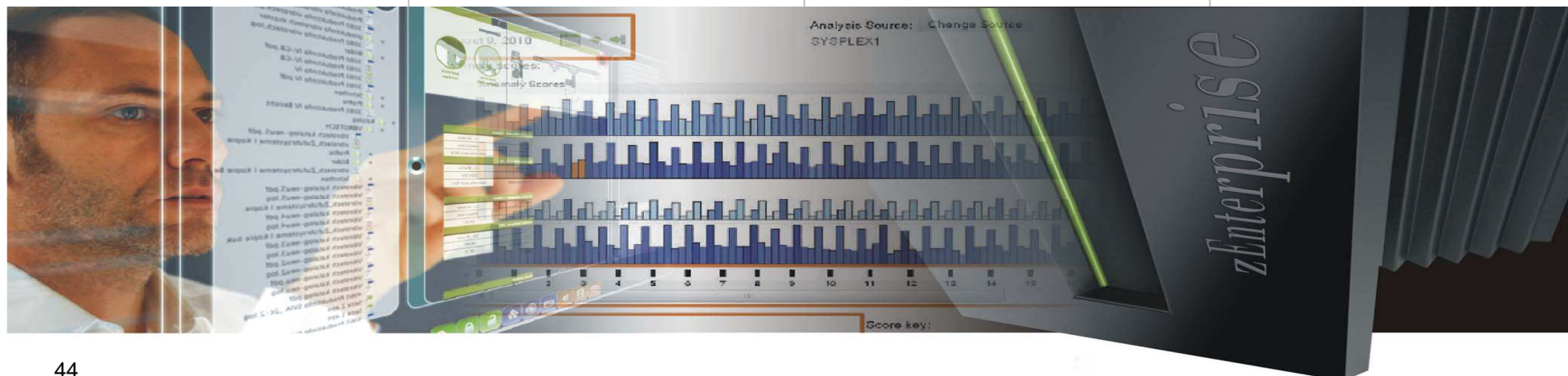




IBM zAware - Identifies unusual system behavior

IBM zAware contains **sophisticated analytics**, applies IBM insight, and **machine learning** to understand your unique system.

Monitoring	Detection	Frequency	Reporting
<ul style="list-style-type: none"> Supports IBM & non IBM middleware and applications Monitors OPERLOG in a Sysplex or Monoplex Assigns a message anomaly score to help identify potential issues 	<ul style="list-style-type: none"> Detects anomalies other solutions might miss Analyzes suppressed or rare messages Can detect a trend in messages to identify a possible problem 	<ul style="list-style-type: none"> Samples every 2 minutes 10 minute interval Uses 90 day rolling baseline; a utility provided to populate baseline 	<ul style="list-style-type: none"> Near real time analysis Intuitive reporting Both high level and drill down Color coder browser display, time slice graphics XML output can feed ISVs or processes



Specific applications of IBM zAware

- **Identify a possible z/OS incident**

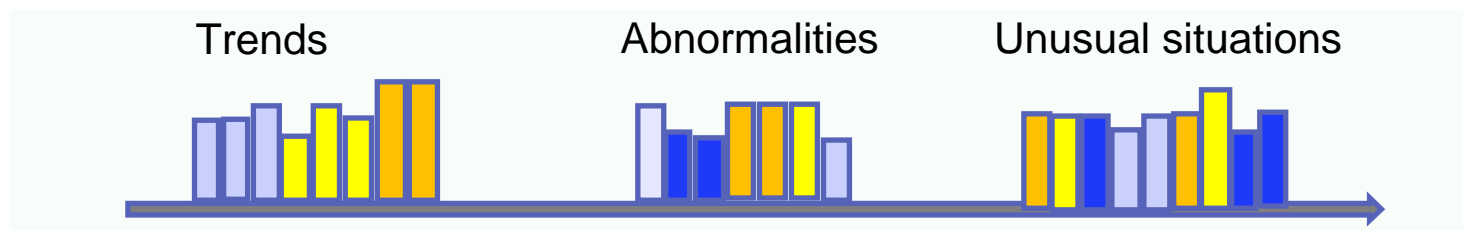
- ▶ *Which image is having a potential problem?*
- ▶ *When did this unusual behavior start?*
- ▶ *Were similar messages issued in the past?*

- **Identify behavior after a change has been made**

- ▶ *Are unusual messages being issued after a change ?*

- **Diagnose intermittent problems**

- ▶ *Are new unusual messages being issued in advance of the problem?*



Reduces time and effort to identify & diagnose problematic messages

Resiliency offering on System z

	Make sure system is likely to work	Find cause of event after event was reported	Report “first” occurrence of event (before externally visible)
Rules Based Performance	Capacity planning – RMF ¹	OMEGAMON [®] XE	OMEGAMON XE
Rules Based Non Performance	Health checker for z/OS	RTD	NetView [®] / TSA
Analytical / Statistically Based Performance	ITM 6.2.1	Netcool [®] Tivoli Performance Analyzer	ITM 6.2.1
Analytical / Statistically Based Non Performance	IBM zAware ²	IBM zAware	PFA – control charts IBM zAware – pattern analysis

¹ RMF collects the data for customer analysis / customer rules

² Changes

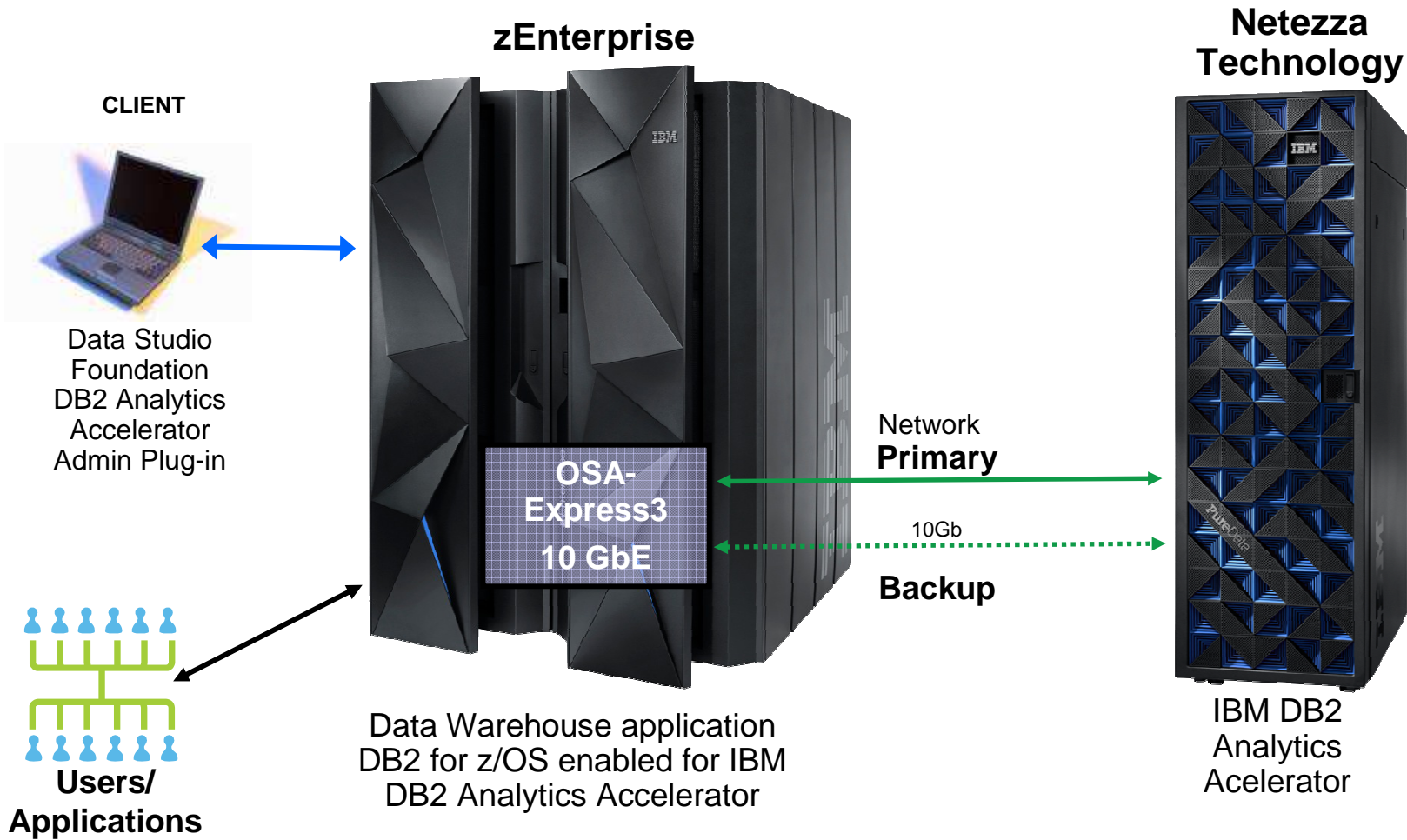
z/OS Support



Release	z10 EC WdfM	z10 BC WdfM	z196	z114	zEC12	End of Service	Coexists with z/OS
z/OS V1.10	X	X	X	X	X	9/11 ¹	V1.12
z/OS V1.11	X	X	X	X	X	9/12 ¹	V1.13
z/OS V1.12	X	X	X	X	X	9/14*	V2.1*
z/OS V1.13	X	X	X	X	X	9/16*	V2.2*

* Planned. All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice.

IBM DB2 Analytics Accelerator Product Components



Note: There are several connection options using switches to increase redundancy

PureData for Analytics N2001 Hardware Overview

12 Disk Enclosures

- 288 600 GB SAS2 Drives
 - 240 User Data, 14 S-Blade
 - 34 Spare
- RAID 1 Mirroring

2 Hosts (Active-Passive)

- 2 6-Core Intel 3.46 GHz CPUs
- 7x300 GB SAS Drives
- Red Hat Linux 6 64-bit

7 PureData for Analytics S-Blades™

- 2 Intel 8 Core 2+ GHz CPUs
- 2 8-Engine Xilinx Virtex-6 FPGAs
- 128 GB RAM + 8 GB slice buffer
- Linux 64-bit Kernel

Scales from ½ Rack to 4 Racks

- User Data Capacity: 192 TB*
- Data Scan Speed: 478 TB/hr*
- Load Speed (per system): 5+ TB/hr

- Power Requirements: 7.5 kW
- Cooling Requirements: 27,000 BTU/hr

DB2 Analytics Accelerator

Large analytic systems at dramatically faster speeds

PureData for Analytics N2001

- **3x Faster than N1001**
- **Increased Throughput**
- **50% more storage /rack**
- **Improved Resiliency**

Over 3 times the performance, 50% more storage capacity, in the same footprint, for a about a 40% increase in price

DB2 Analytics Accelerator V3.1

- **High Performance Storage Saver**
- **Incremental Update**
- **zEnterprise EC12 Support**
- **Query Prioritization**
- **UNLOAD Lite**

41 customers with 56 systems are experincing the speed of analytics on z

zEC12
Power and
Cooling

zEC12 - Introducing Radiator for Air Cooled System

- Closed loop water cooling N+1 pump system replaces modular refrigeration units (MRUs) used for air cooling in z196 and z10 EC

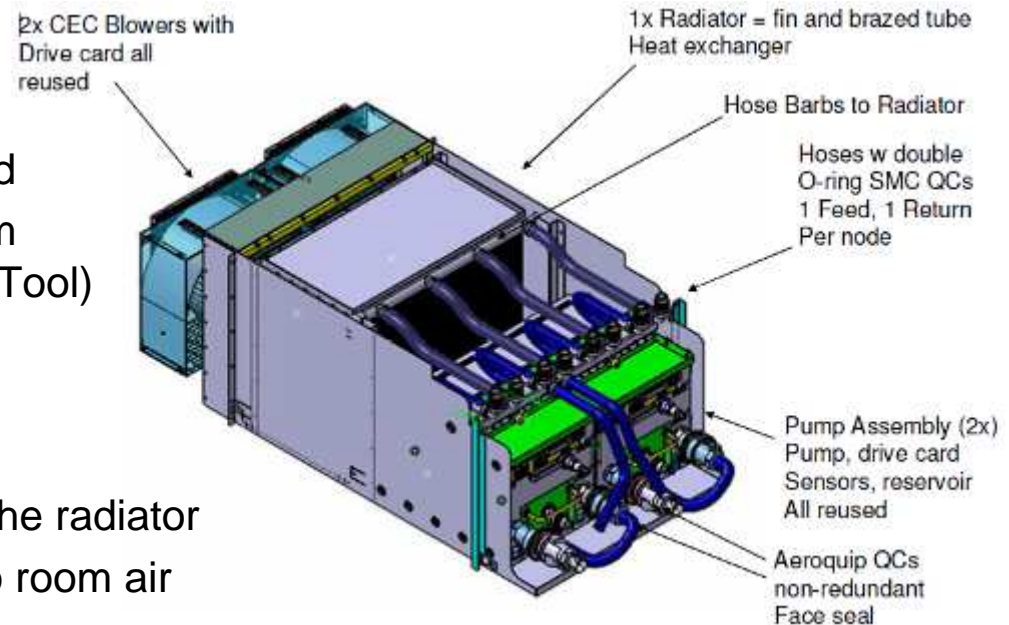
- No connection to chilled water required
- Water added to the closed loop system during installation (New Fill and Drain Tool)

- Normal operation design:

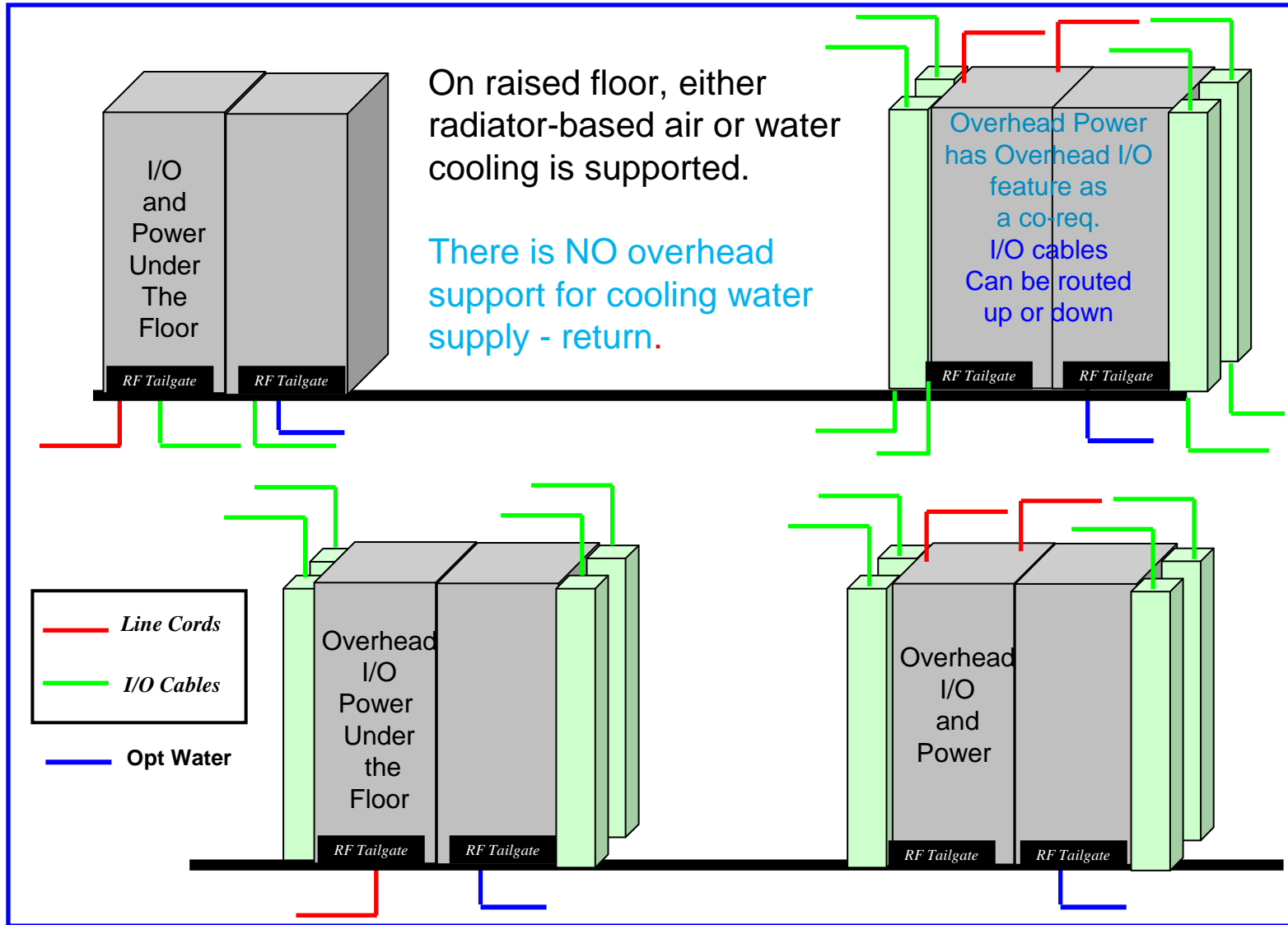
- Heat removed by water circulating to the radiator
- Fans exhaust heat from the radiator to room air

- Backup operation design

- N+1 pump/blower failure: Cooling maintained by closed loop water system without “cycle steering” slow down. Concurrent repair.
- Water cooling system failure: Cooling maintained by backup fans as in the z196 air cooled option with MRUs. “Cycle steering” slow down if needed to maintain operation. Concurrent repair

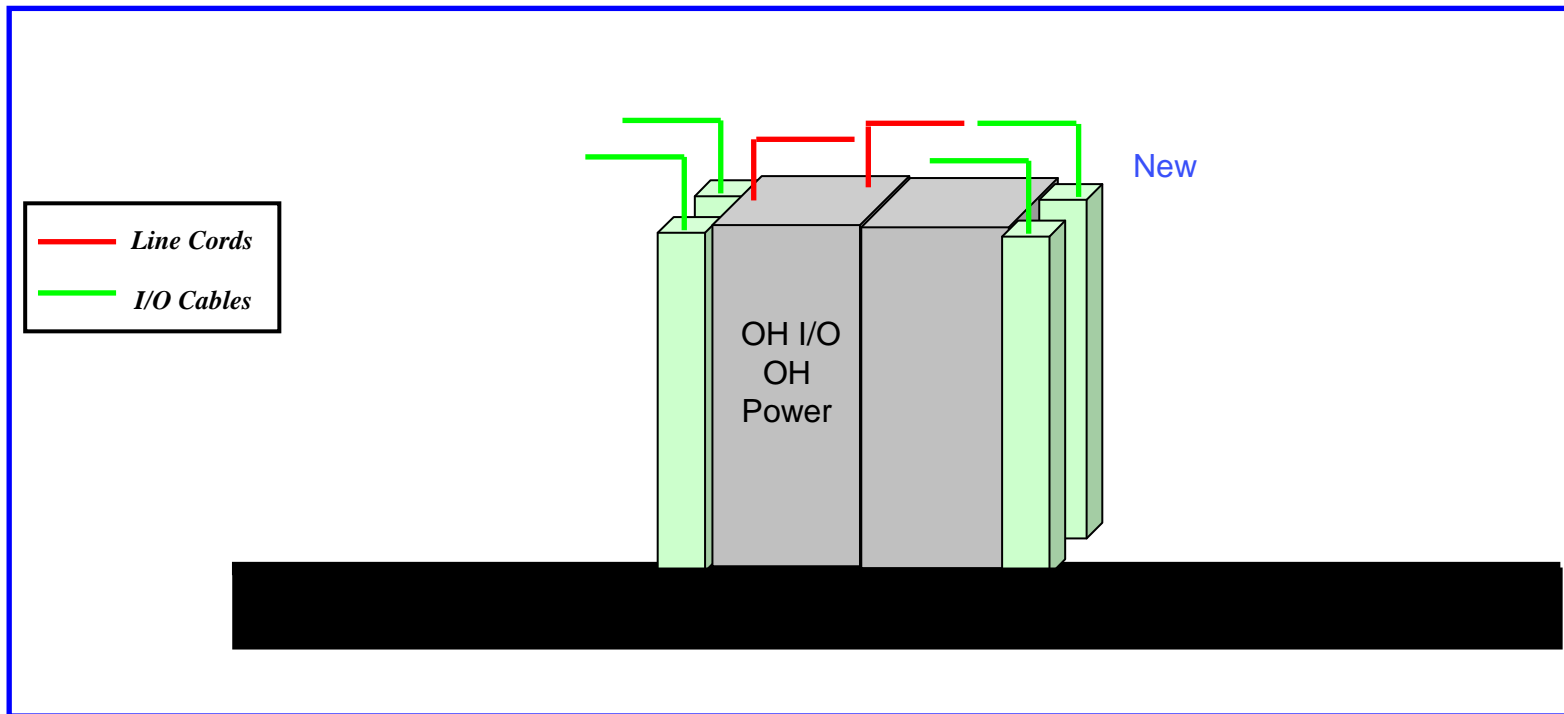


zEC12 Installation - Raised Floor options



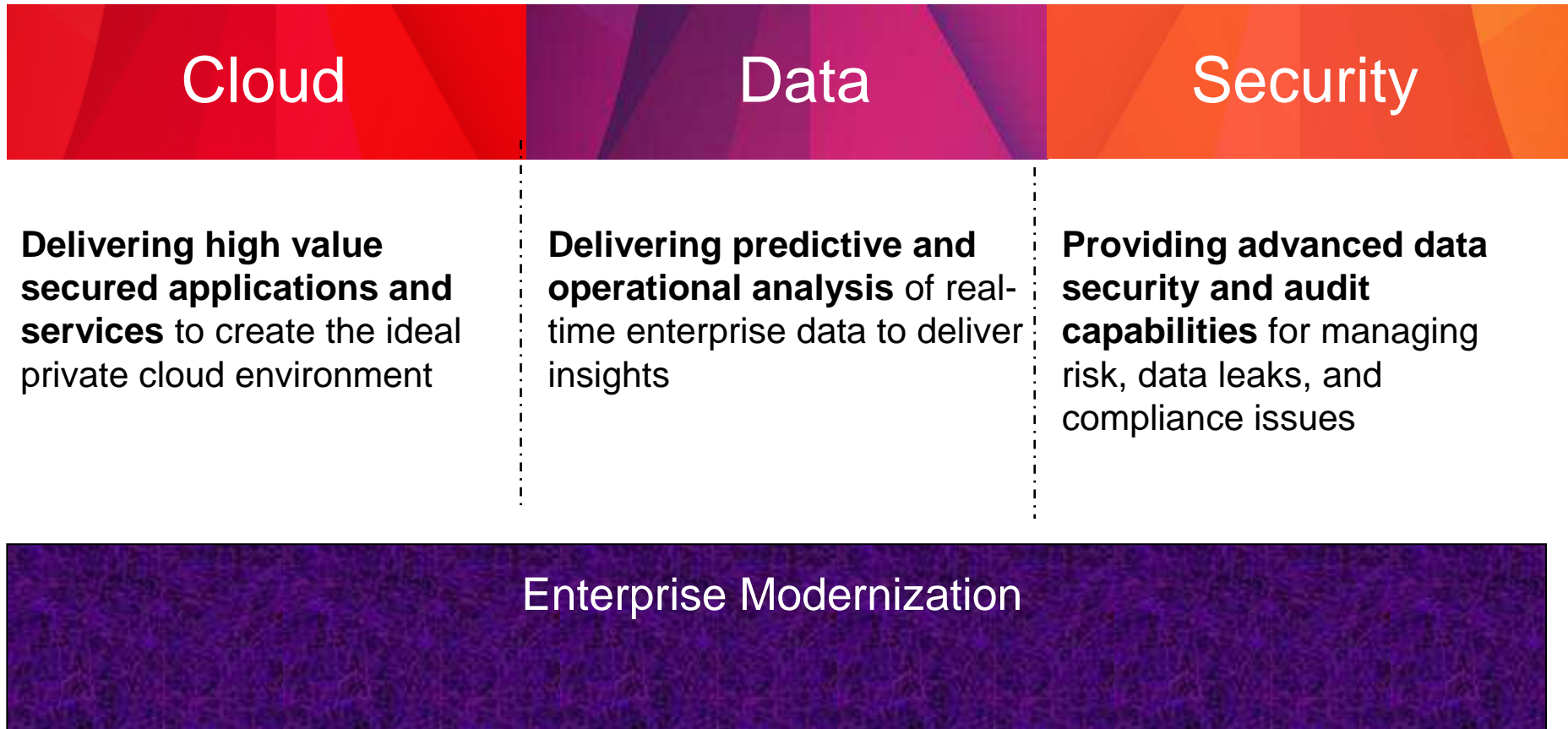
Top Exit Power option: When selected for a raised floor the Top Exit I/O feature is a coreq. Also the diagram for this configuration should depict the I/O routing up thru the I/O chimneys and also routing thru the bottom of the frame using the raised floor tailgates.

zEC12 Installation – Non-Raised Floor option

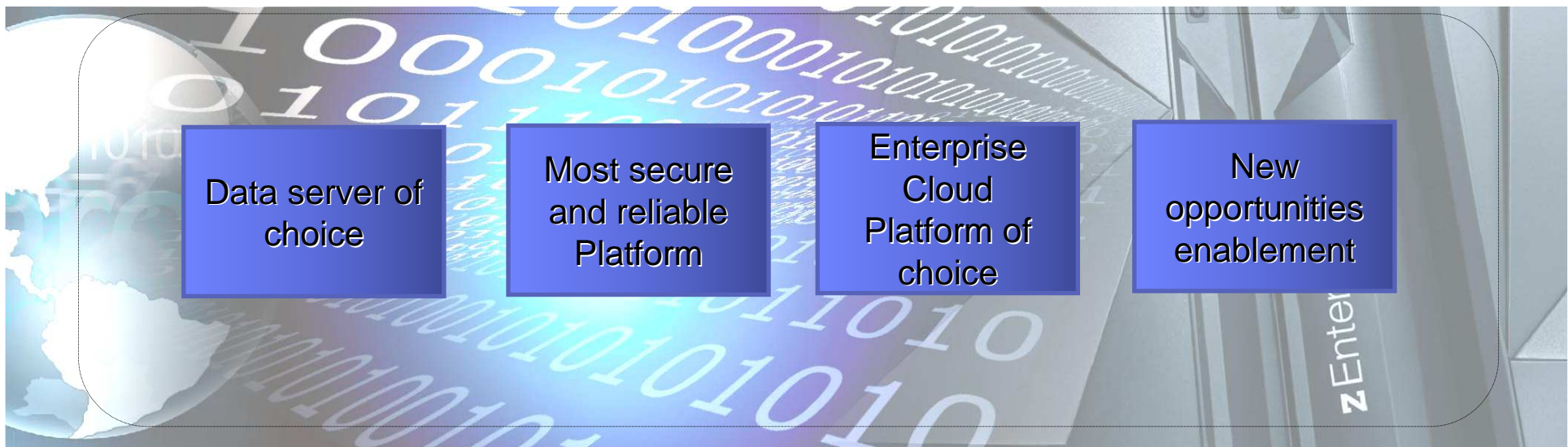
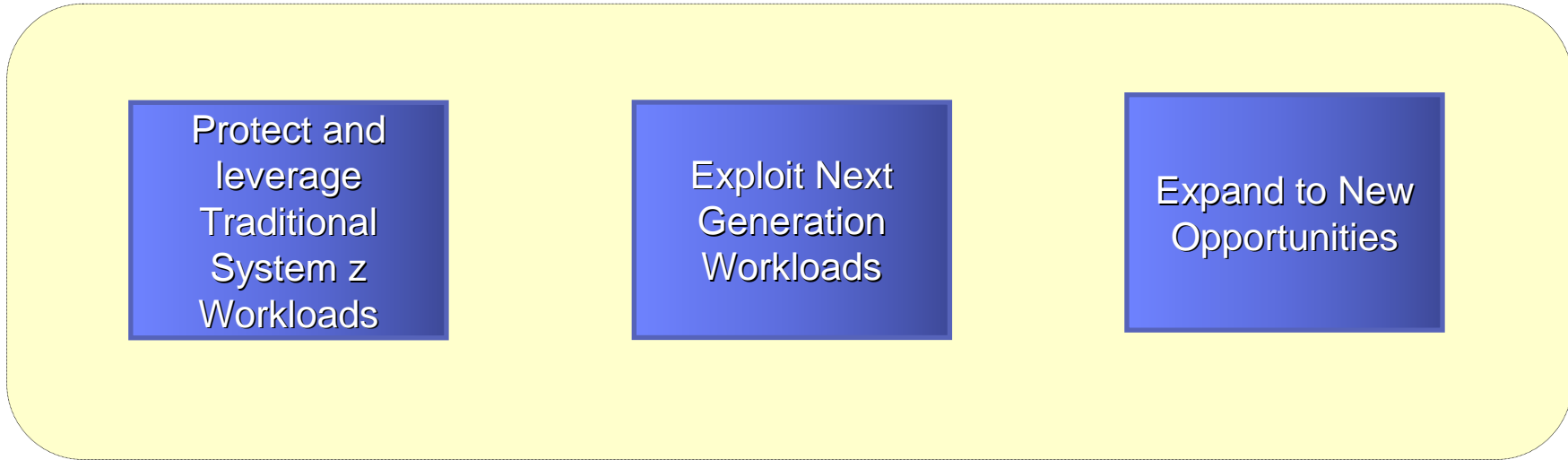


Water cooling is NOT supported. NO cables may exit at floor level.

IBM zEnterprise EC12 Business Initiatives



System z Strategy ... and Future



Cloud

Data

Security



Merci de votre attention

