Enterprise verification management solutions
White paper
September 2009

Address system-on-chip development challenges with enterprise verification management.

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Introduction

Dynamic and highly competitive marketplace demands are forcing manufacturers to put increasing pressure on product development teams and tasking them with:

- *Integrating more functions into single system-on-chip (SoC) devices.*
- *Developing more complex software.*
- *Shrinking product design cycles.*
- *Developing hardware and software in parallel.*
- *Contending with a shortage of skilled engineers.*

These factors are driving more and more businesses to adopt coverage-driven verification, a structured way to test both software and a hardware design simulated in software before expensive physical prototyping. Pre-silicon design verification is critical to the quality, cost and timeliness of the finished product and is typically the most time-consuming and human- and IT-resource-intensive phase of the design lifecycle.

This white paper addresses the multidimensional challenges posed by verification management and offers a compelling solution known as enterprise verification management solution (EVMS) based on over a decade of development and in-house experience at IBM.

Highlights

Building better products with functional verification

Significant changes have occurred in the semiconductor verification process over the past 20 years due to the increasing complexity of semiconductor designs as well as dramatic improvements in simulation tools and infrastructure. Semiconductor verification has also evolved from individual, manual efforts to large-scale efforts involving teams of engineers. And SoC designs now include a significant amount of software.

Process

Functional verification tools help streamline the development process.

Today's leading design teams employ a variety of functional verification tools at various levels of the design, based upon design content and complexity. One or all of these tool kits may be deployed in the process of simulating the entire hardware design in software, including:

- *Formal and semiformal verification.*
- *Instruction set generators for common architectures.*
- *Tools to assist designers in basic tests before handing off to verification engineers.*
- *Verification IP to test standard interfaces and compliance testing.*

Teams may also employ techniques that consist of constrained, random bias tests—tests that have proven to be extremely effective at stressing complex control logic and interacting state machines.

A high-level diagram for a typical semiconductor design process is shown in figure 1.

Highlights

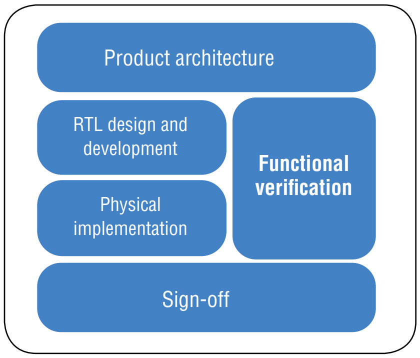

Figure 1: A typical SoC design process includes five stages of development: product architecture, RTL design and development, functional verification, physical implementation and sign-off. The completion of all these stages helps ensure that a design is ready for manufacturing.

Functional verification is the most resource-intensive phase of design.

Of all these steps, functional verification merits the most attention as it is the most time-consuming and resource-intensive phase of the design lifecycle at the 65nm process node and significantly determines the ultimate quality, cost and timeliness of the finished product. Once a design has been committed to silicon, changing the design can be very costly, with re-spins costing millions of dollars below 90nm. Effective functional verification is the key to avoiding re-spins.

A comprehensive test plan is needed ensure optimal use of human and IT resources.

During typical functional verification, tests are run against the compiled VHDL or Verilog code to simulate and verify the key functions of the design. A comprehensive and efficient test plan is needed to define metrics of coverage and ensure optimal use of human and IT resources, and these test plans need to be closely linked to overall product requirements. Teams of engineers are assigned to address different components of the SoC. The verification engineer creates a verification environment against a test plan appropriate for his component. The verification engineer must also develop, maintain and execute the individual tests to achieve functional coverage against the test plan.

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Because modern designs are extremely complex, millions of tests are run per day in a high performance computing environment for the life of the project. Test results are used to identify defects in both hardware and software. Defects are repeatedly addressed until there is a high level of confidence that the design's functionality has met stated requirements.

Key challenges

Product complexity and marketplace pressures are putting demands on the development process.

Product complexity continues to rise with the demand for faster time to market. Development budgets are not keeping pace, so new products must be developed with fewer resources, increasing the probability of projects that are behind schedule, over budget or both. Executives who hold ultimate responsibility for projects are constantly challenged to understand current status, anticipate problems and take corrective actions to ensure that projects meet customer requirements while satisfying cost and schedule objectives.

Time-to-market pressures have also forced designers to develop hardware and its associated embedded software concurrently, therefore requiring effective communication and coordination among engineering teams. Engineers generate and interact with many design artifacts (requirements, specifications, HDL code, compiled code, embedded software, test plans, test scripts, test results, defect logs, etc.) and it is essential to establish a common configuration and change management system to ensure that team members have easy access to the right versions of code and documentation.

Globally distributed teams need to access shared tools.

Globally distributed design teams further complicate the verification effort. Skilled hardware, software and verification personnel can be hard to find in the local geography. Once located, these resources need to access the tools and design content required to perform their jobs without setting up unique or significant new infrastructure.

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The IT challenges are also intense. The volume of coverage-driven simulations places enormous stress on the compute farm. Utilization of the local farm must be kept as high as possible to minimize costs. Degradations in utilization can lead to slipped schedules and missed deadlines. Workload across the compute farm must also be prioritized.

Coordinating development with enterprise verification management

EVMS from IBM takes a systems approach to the development and verification process.

To address the growing complexities of SoC development, EVMS from IBM takes a holistic systems view of the hardware engineering design environment, the embedded software development environment and the required IT architecture/infrastructure.

Solution

The verification process flow is delivered by combined capabilities from IBM Rational® and IBM Tivoli® software, IBM Systems Group, IBM Global Business Services and Cadence Design Systems (Cadence). At a high level, the functional verification process flow involves four steps. These steps utilize Cadence Incisive Enterprise technology for hardware verification.

Plan—Functional verification begins with an executable plan that drives all facets of the verification project. An up-front plan is critical to estimate and secure the needed human and IT resources to execute the verification. This plan must tie directly to product and system requirements to ensure that the test plans test all aspects of the design and that the design meets all requirements. Tasks are assigned to verification engineers and the coverage goals are defined, upon which progress will be measured.

Execute—The team will then execute the different verification scenarios specified in the plan using automated test generation, simulation and sometimes acceleration/emulation.

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EVMS from IBM provides support for all of the stages of the functional verification process.

Measure—It is important to measure the results after each run and assess the coverage achieved and status against plan. Objective measures enable more effective management of the overall project.

React—Finally, teams react to the results by finding, fixing and anticipating problems and/or redirecting future runs to optimize coverage for the uncovered parts of the design.

Key capabilities of the EVMS offering

Capability	Functions	Supporting technology
Systems requirements engineering	Establishes a common set of systems requirements that forms the basis for software and hardware test plans. Linkage to these requirements throughout the development process is necessary to help ensure that the delivered product meets all customer requirements.	Rational
Metric-driven verification management	Helps define and manage holistic verification test plans for hardware and software designs as well as simulations.	Cadence for hardware designs and Rational for software designs
Software lifecycle management	Helps ensure that the latest versions of the code, compiled code and test scripts are tracked and used in the verification process. Software build tasks are executed automatically to help eliminate delays due to manual intervention, and a detailed bill of materials is generated to capture the contents of each release for better reproducibility.	Rational
Workload management	Prioritizes test runs dynamically so that the most critical scripts are processed first.	Tivoli
Compute farm optimization	Provides highly efficient use of computing resources while the underlying file system services provide scalable, high-performance data access.	IBM Systems Group and Tivoli
Development process governance and accounting	Tracks verification progress and key performance indicators (KPIs) through role-based dashboards for executives, project managers and engineers.	Cadence, Rational, IBM Systems Group, Tivoli

Highlights

Benefits

EVMS from IBM offers numerous benefits that address the challenges of SoC development. These benefits are designed to offer SoC manufacturers faster time to market with higher quality of product at lower cost.

By bringing hardware development, software development and verification teams together under a coordinated verification environment, EVMS supports parallel development of hardware and software designs, shrinking the time it takes to design a new chip.

Metric-driven verification provides higher-quality verification than traditional methods because coverage is continually monitored in detail per the verification plan, resulting in more comprehensive verification.

EVMS supports faster time to market for SoC products.

A common requirements management solution provides a central repository for overall product requirements as well as the requirements for the SoC and embedded software. Management of changes in requirements throughout the development process helps reduce costly rework and helps ensure that the product the customer requested is the product that is delivered.

A common version control repository for storing product development artifacts as well as a common change and defect management system enables geographically dispersed teams to work as a single, unified team.

Automation of error-prone, repetitive tasks such as software builds improves accuracy and frees up engineers' valuable time and allows them to focus on more strategic development tasks.

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Significant increases in compute farm utilization can help reduce time to market and lower IT costs. Verification workloads can be prioritized dynamically so that the most critical projects and tasks receive adequate compute resources.

Dashboards provide role-based access to customizable, real-time verification and IT metrics, enabling development team management to anticipate issues and proactively respond to challenges.

Metric-driven verification provides higher-quality results, and central repositories help ease change management and reduce rework.

Verification improves IBM product delivery processes

The concepts underlying EVMS were nurtured over 20 years of IBM product development experience while many have been implemented for over ten years. Today these concepts are incorporated into the IBM global product development environment, supporting not only semiconductor development, but nearly all IBM offerings, including sub-assemblies, servers, mainframes and supercomputers. Over this period of time, the company has observed holistic business benefits from the solution, including a reduction of re-spins, improved developer productivity, increased compute farm utilization and a reduction in IT spend.

Increases in compute farm utilization can help reduce IT costs and time to market.

Using a rigorous, structured verification methodology, IBM has been able to significantly improve the quality of products introduced to the marketplace and has realized more predictable design schedules by targeting defect reduction and improved problem discovery.

By using a metric-driven approach for verification, the size of verification teams has been reduced while allowing the teams to focus on coverage and analysis of designs, not debugging the tests themselves. Reuse of previous verification components has also greatly enhanced verification engineer productivity.

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Since software delivery is a core component of system verification, improving software developer productivity is essential. Customers implementing the version control repository provided by EVMS have been able to increase the number of verification releases and software engineering resource utilization using parallel development.

IBM's own use of verification processes has improved product quality.

By using a single defect management solution for both hardware and software designs, internal IBM results have shown that first-time defects can be rerouted and tracked across what were once significant organizational or geographical boundaries, improving quality and reducing the resources necessary to keep defects in sync.

External research reveals significant benefits to clients using the software build automation component of EVMS, including a 110 percent increase in speed of build and releases, a 42 percent increase in change management team productivity, a 30 percent reduction in errors and a 28 percent increase in developer productivity.

A single defect management solution helps track defects across traditional boundaries.

EVMS provides the tools and practices necessary to improve the efficiency of compute farm resources. IBM experiences compute farm utilization in excess of 90 percent for verification workloads, 24 hours a day, seven days a week, compared with a much lower industry average.

IBM has enjoyed reductions in IT spend for the infrastructure supporting semiconductor development, fabrication, product development and product manufacturing.

Highlights

EVMS from IBM is a fully integrated solution that can help address SoC verification issues.

EVMS can help reduce re-spins, speed time to market, improve scheduling and optimize resources.

Conclusion

The enterprise verification management solution from IBM is a fully integrated solution that can help address issues facing SoC verification and is based on extensive experience gained by the IBM hardware delivery group. EVMS takes a holistic view of the verification process and brings together the hardware design team, the software delivery team, the verification engineering team and the IT team. The solution allows these teams to implement a metric-driven verification environment that can provide higher-quality verification than traditional environments. Coverage is continually monitored in detail per the verification plan resulting in more comprehensive verification. A common software lifecycle management system enables geographically dispersed teams to work as a single, unified team. And EVMS delivers a more efficient utilization of compute resources and provides the hard data to manage compute resources cost-effectively for an individual project or across the entire enterprise. The results are fewer re-spins, shorter time to market, better schedule predictability and a reduction in verification engineer resource requirements.

For more information

To learn more about the enterprise verification management solution from IBM, contact your IBM representative or IBM Business Partner, or visit:

ibm.com/software/plm/partners/pdif.html

IBM Corporation
Software Group
Route 100
Somers, NY 10589
U.S.A.

Produced in the United States of America
September 2009
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