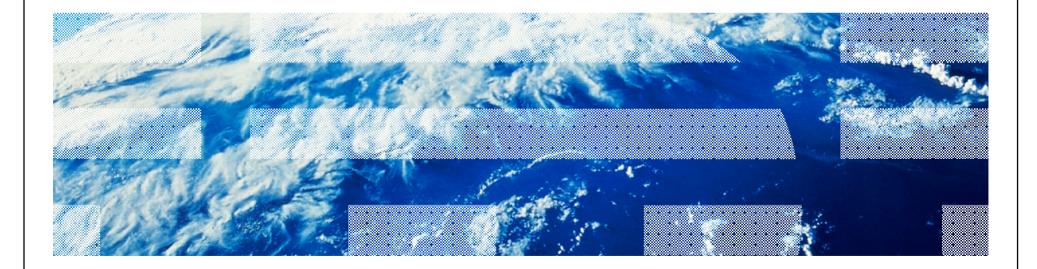
IBM System z



VEARS

IBM z/VSE V4.1, V4.2 and V4.3 Performance Considerations



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IBM System z



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z/VSE V4.1, V4.2 and V4.3 Hardware support

§ z/VSE V4.1, V4.2 and V4.3 runs on the following machines

- IBM System z10 BC or z10 EC
- IBM System z9 BC or z9 EC (formerly z9-109)
- IBM zSeries: z800, z900, z990, z890
- z/VM V5.2 (or later) is a prerequisite for running z/VSE V4 under VM.

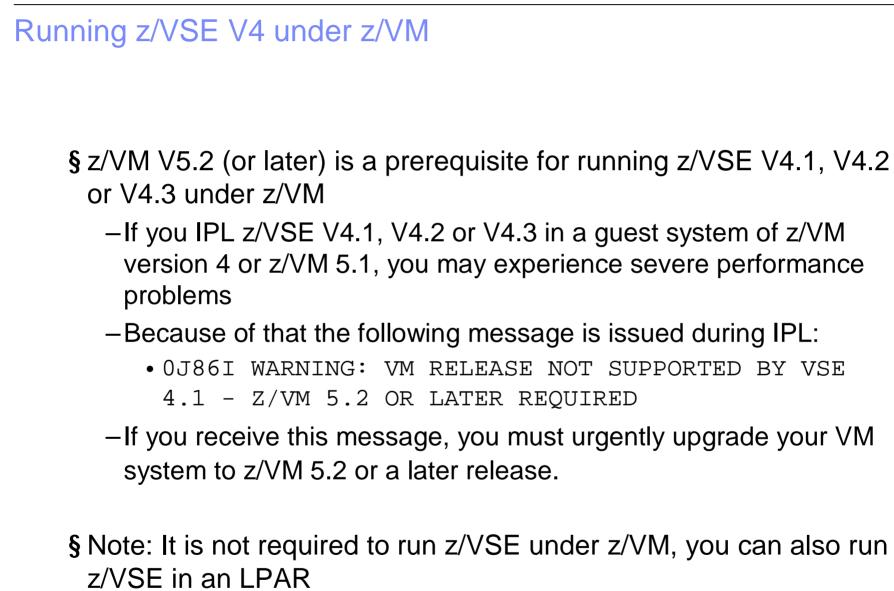




Supported VSE Releases

VSE Release	Available	End of Marketing	End of Service
z/VSE 4.3	11/26/2010		
z/VSE 4.2	10/17/2008	11/26/2010	
z/VSE 4.1	03/16/2007	10/17/2008	04/30/2011
z/VSE 3.1	03/04/2005	05/31/2008	07/31/2009 (out of service)
VSE/ESA 2.7	03/14/2003	09/30/2005	02/28/2007 (out of service)
VSE/ESA 2.6	12/14/2001	03/14/2003	03/31/2006 (out of service)
VSE/ESA 2.5	09/29/2000	12/14/2001	12/31/2003 (out of service)
VSE/ESA 2.4	06/25/1999	09/29/2000	06/30/2002 (out of service)
VSE/ESA 2.3	07/12/1997	06/30/2000	12/31/2001 (out of service)









VSE Server Support

IBM Server	z/VSE 4.3	z/VSE 4.2	z/VSE 4.2	z/VSE 4.1	z/VSE 3.1 (*)	VSE/ESA 2.7 (*)	VSE/ESA 2.6 (*)	VSE/ESA 2.5 (*)	VSE/ESA 2.4/2.3 (*)
IBM zEnterprise 196	Yes	Yes	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	No
IBM System z10 BC/EC	Yes	Yes	Yes	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	Yes (PTF required)	No
IBM System z9 BC/EC (z9-109)	Yes	Yes	Yes	Yes	Yes	Yes	Yes (PTF required)	Yes (PTF required)	No
zSeries 890, 990	Yes	Yes	Yes	Yes	Yes	Yes	Yes (PTF required)	Yes (PTF required)	No
zSeries 800, 900	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
S/390 Parallel Enterprise Server G5/G6	No	No	No	No	Yes	Yes	Yes	Yes	Yes
S/390 Multiprise 3000	No	No	No	No	Yes	Yes	Yes	Yes	Yes
S/390 Parallel Enterprise Server G3/G4	No	No	No	No	No	No	Yes	Yes	Yes
S/390 Multiprise 2000	No	No	No	No	No	No	Yes	Yes	Yes
S/390 Integrated Server	No	No	No	No	No	No	Yes	Yes	Yes
S/390 Parallel Enterprise Server G2 / G1 (out of Service)	No	No	No	No	No	No	Yes	Yes	Yes
ES/9000 – 9221, 9121, 9021 (out of Service)	No	No	No	No	No	No	Yes	Yes	Yes
P/390 and R/390 (out of Service)	No	No	No	No	No	No	Yes	Yes	Yes

(*) Note: Although earlier releases technically run on selected servers, these releases are Out-of-Service anyway.





VSE Hardware Support

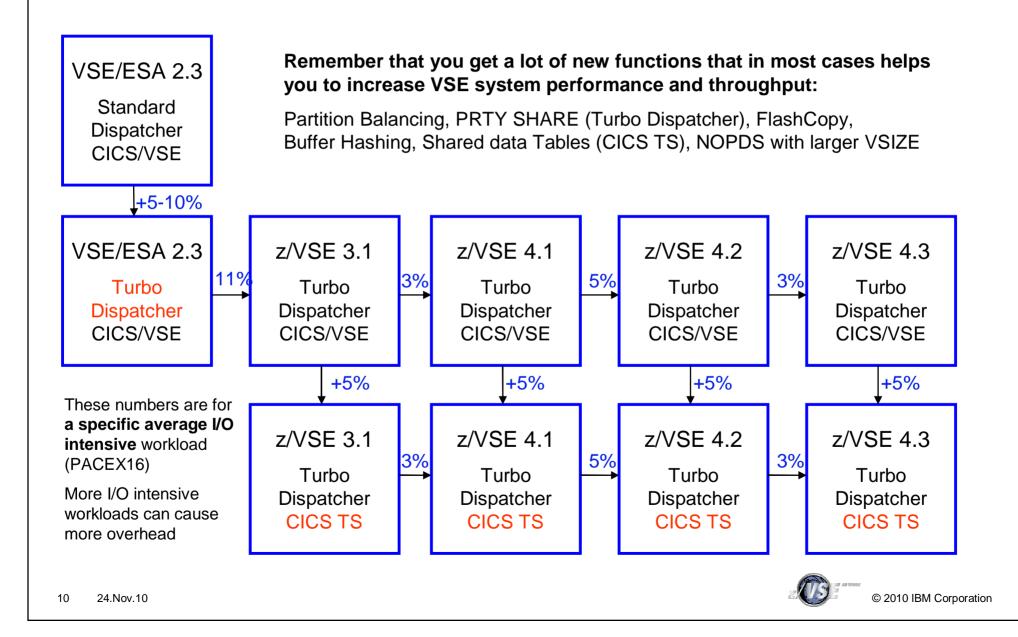
VSE Release	HiperSockets	OSA Express (QDIO mode)	Hardware Crypto
z/VSE 4.3	Yes	Yes	Yes (PCICA, CEX2C, CEX2A, CPACF)
z/VSE 4.2	Yes	Yes	Yes (PCICA, CEX2C, CEX2A, CPACF)
z/VSE 4.1	Yes	Yes	Yes (PCICA, CEX2C, CEX2A, CPACF)
z/VSE 3.1	Yes	Yes	Yes (PCICA, CEX2C, CEX2A, CPACF)
VSE/ESA 2.7	Yes	Yes	Yes (PCICA, CPACF)
VSE/ESA 2.6	No	Yes	No
VSE/ESA 2.5 or earlier	No	No	No

Crypto Card	z800	z900	z890	z990	z9 BC/EC	z10 BC/EC	z196
PCICA	No	Yes	Yes	Yes	No	No	No
CEX2C	No	No	Yes	Yes	Yes	Yes	Yes
CPACF	No	No	Yes	Yes	Yes	Yes	Yes
CEX2A	No	No	No	No	Yes	Yes	Yes





Overhead Deltas for VSE Releases





z/VSE V4.1, V4.2 and V4.3 - z/Architecture mode

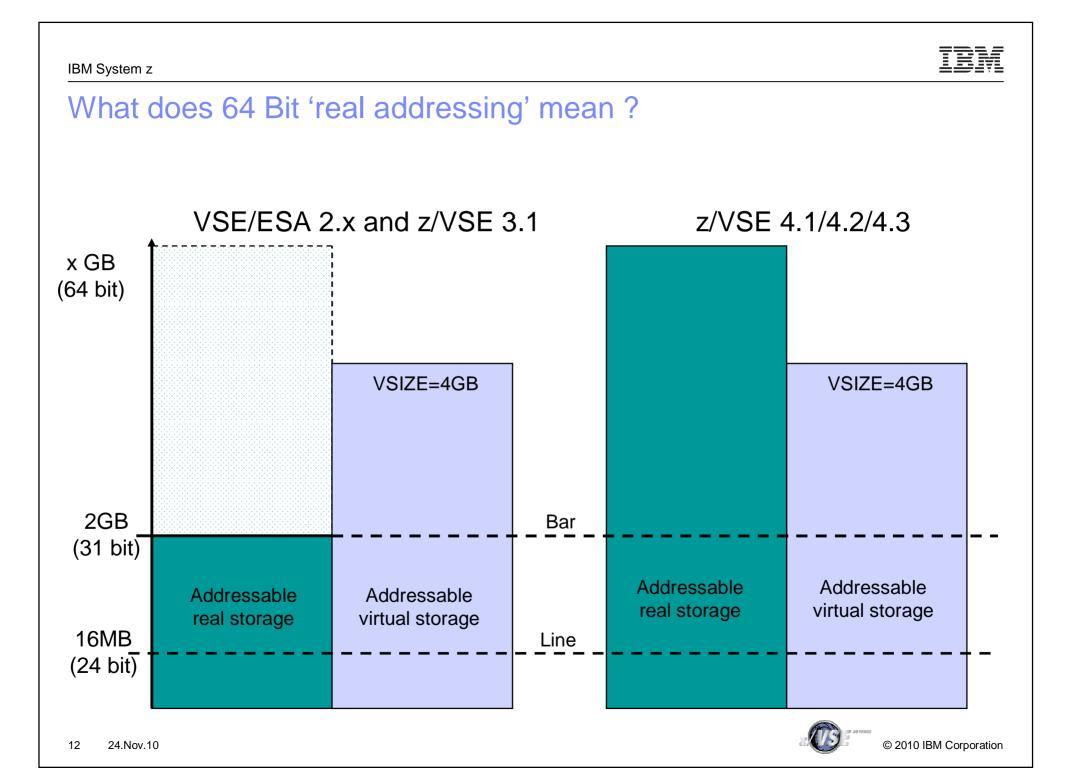
§ z/VSE V4.1, V4.2 and V4.3:

- Supports z/Architecture-capable (64-bit) processors.
- Executes in z/Architecture mode only.
- Supports 64-bit real addressing for selected system functions.
- Supports processor storage up to 8 GB (z/VSE 4.2) / 32GB (z/VSE 4.2).
- The storage beyond 2 GB is managed exclusively by the z/VSE operating system.

§ z/VSE V4.1, V4.2 and V4.3 does not support:

- 64-bit virtual addressing. The size of a virtual address or data space remains restricted to 2 GB.
- For user applications, 64-bit addressing and operations that use 64-bit registers.
- § 64-bit real addressing is transparent to your user applications providing you use IBM-supplied standard interfaces.
- § Customers with especially large z/VSE environments might benefit from lower paging rates.
- § Many z/VSE environments might be able to run without a page data set (using the NOPDS option).







What does 64 Bit 'real addressing' mean ?

§ VSE/ESA V2.x and z/VSE 3.1

- -z/VSE 3.1 or below can address only 2 GB of processor storage
 - 31 bit (real) addressing
- Page data set required if VSIZE (+VIO) > ~ 2GB
- No page data set required as long 2 GB processor storage is sufficient
- \$ z/VSE V4.1, V4.2 and V4.3
 - –z/VSE V4.1 can address up to 8 GB of processor storage, z/VSE V4.2 & V4.3 up to 32 GB
 - 64 bit (real) addressing
 - No page data set required
 - If processor storage >= VSIZE (+VIO)
 - -Virtual address spaces and data spaces are still limited to 2 GB
 - 31 bit (virtual) addressing
 - No changes required to applications





z/VSE V4 – Example with 3 GB of real storage

mar	p real	L						
_	0015		R-SIZE	R-ADDR	PFIX(BELO	W)	PFIX (ABOV	E)
AR	0015				ACTUAL	LIMIT	ACTUAL	LIMIT
AR	0015	SUP	52K	0				
AR	0015	SYS-24			592K	14136K		
AR	0015	BG V			0K	0K	0K	0K
AR	0015	F1 V			148K	400K	0K	1400K
AR	0015	F2 V			32K	144K	0K	0K
AR	0015	F3 V			88K	424K	0K	0K
AR	0015	F4 V			0K	0K	0K	0K
AR	0015	F5 V			0K	0K	0K	0K
AR	0015	F6 V			0K	0K	0K	0K
AR	0015	F7 V			200K	400K	1044K	2100K
AR	0015	F8 V			0K	0K	0K	0K
AR	0015	F9 V			0K	0K	0K	0K
AR	0015	FA V			0K	0K	0K	0K
	0015				0K	0K	0K	0K
AR	0015	SYS-31					7404K	2052264K
		DYN-PA			0K	0K	0K	0K
AR	0015	AVAIL	64K					
		SYSTEM	25068K					
		TOTAL	3145728К		<	/	<	/
AR	0015							
		AVAILABLE FO	OR SETPFIX	:	135	44K	20448	60K
AR	0015							
AR	0015	1I40I READY						



Exploiting 64 Bit real storage § Even on VSE/ESA or z/VSE 3.1 the VSIZE could 'theoretically' be up to 90G § 'Practically' you are limited by Page dataset size and number of extents Page I/O rate

§ With z/VSE V4 you can run with VSIZE+VIO up to approximately 8GB (z/VSE V4.1) / 32 GB (z/VSE 4.2/4.3) without a page dataset (NOPDS)

-If enough processor storage is available

-No time consuming page I/Os

§ You can have more large partitions in your system





Paging considerations

§ 'Paging' is another word for Page Manager activities

- -Assigning real pages to virtual pages
- -Writing pages to the page data set (page-out I/O)
- -Reading pages from the page data set (page-in I/O)

§ Even with 8GB real storage and NOPDS paging happens

- -Assigning real pages to virtual pages
- -Moving pages from <2G to >2GB (above the bar) and vice versa

§ 'Paging' as such is not bad

-But page I/Os are 'bad' (dependent on the page I/O rate)





Paging considerations - PMRMON

§ New SIR command: SIR PMRMON

- -Displays reports from the 'Page Manager Monitor'
- Shows number of page faults, page I/Os, page exchanges (31 <-> 64), ...

§ Usage:

- -SIR PMRMON=ON (resets counters)
- -// run your workload
- -SIR PMRMON
- -SIR MPRMON=OFF
- -Output example, see next foil
- § The output displays mainly internal counters that are for evaluation by IBM support persons





Paging considerations - PMRMON

AR	0015		PAGI	E MANAGER	MONITORING REPORT		
AR	0015	(BA	ASED	ON A 0000	:01:04.801 INTERV	AL)	
AR	0015	IPFQ 31-BIT	=	517126	IPFQ 64-BIT	=	115185
AR	0015	PSQ 31-BIT	=	1500	PSQ 64-BIT	=	527
AR	0015	PF EXCH TOTAL	=	4673	PF EXCH 31->64	=	0
AR	0015	PF EXCH 64->31	=	4673	PGFLT TOTAL	=	25825
AR	0015	PGFLT PMGR	=	0	PGFLT USER	=	25825
AR	0015	PGFLT IMM PO 31	=	0	PGFLT IMM PO 64	=	0
AR	0015	SELCT ON PSQ 31	=	0	SELCT ON PSQ 64	=	0
AR	0015	SELC R=1 MAX 31	=	0	SELC R=1 MAX 64	=	0
AR	0015	RECLAIMS	=	0	NPSQ LOW	=	0
AR	0015	PGOUT I/O TOTAL	=	0	PGIN I/O TOTAL	=	0
AR	0015	PGOUT I/O UNC.	=	0	PGOUT I/O PRE.	=	0
AR	0015	LRA PGM CHECK	=	3904	TFIX 64-BIT FR	=	768
AR	0015	11401 READY					

Description of values see next foil



Paging considerations - PMRMON

Number of unused page frames below 2G
Number of page frames below 2G in page selection queue
Number of unused page frames above 2G
Number of page frames above 2G in page selection queue
Total number of times a page frame exchange is requested
Number of times a page frame is exchanged from below 2G to above 2G (e.g. instead of page-out I/O)
Number of times a page frame is exchanged from above 2G to below 2G (e.g. TFIX)
Total number of page faults
Number of page faults handled by page manager task
Number of page faults handled immediately without activating page manager task
Number of page faults forcing an immediate page-out of a page frame below 2G
Number of page faults forcing an immediate page-out of a page frame above 2G
Number of page selection events on page frames below 2G
Number of page selection events on page frames above 2G
Maximum number of cycles on a page selection event for page frames below 2G
Maximum number of cycles on a page selection event for page frames above 2G
Number of times page frames are reclaimed from the page-out queue
Number of times the available page frames are below a critical minimum
Total number of page-out I/O
Total number of page-in I/O
Total number of unconditional page-out I/O
Total number of pre-page-out I/O
Number of special operation program exceptions on LRA
Number of TFIX requests with page frames above 2G involved





z/VSE V4.2 Performance Considerations

§ More tasks

-z/VSE V4.2 now supports up to 512 tasks

§PAV Performance Considerations
PAV – Performance Considerations

-PAV = Parallel Access Volumes

§CPU Balancing

-Automatically start and stops CPUs according to the current workload





z/VSE V4.2 - More tasks



- § z/VSE 4.2 supports up to 512 concurrent tasks
 - the previous limit was 255 concurrent tasks.
 - Additional task IDs will be in the range X'0100' to X'0200'.
 - A QUERY SYSTEM command has been provided to display information on the current task usage

§ Please note:

- The maximum number of tasks per partition remains 32.
- The default maximum remains 255. If you wish to increase the maximum number of tasks, you must use the SYSDEF command to increase it to any number up to 512.

§ Benefits:

- The workload resulting from CICS and batch programs can now be more efficiently distributed
- Previously, some customers might have been reluctant to perform migration from CICS/VSE to the CICS Transaction Server for VSE/ESA because of its more intensive usage of VSE tasks (compared to CICS/VSE). This inhibitor has now been removed.
- Using more tasks have no measurable performance impact (neither negative nor positive)

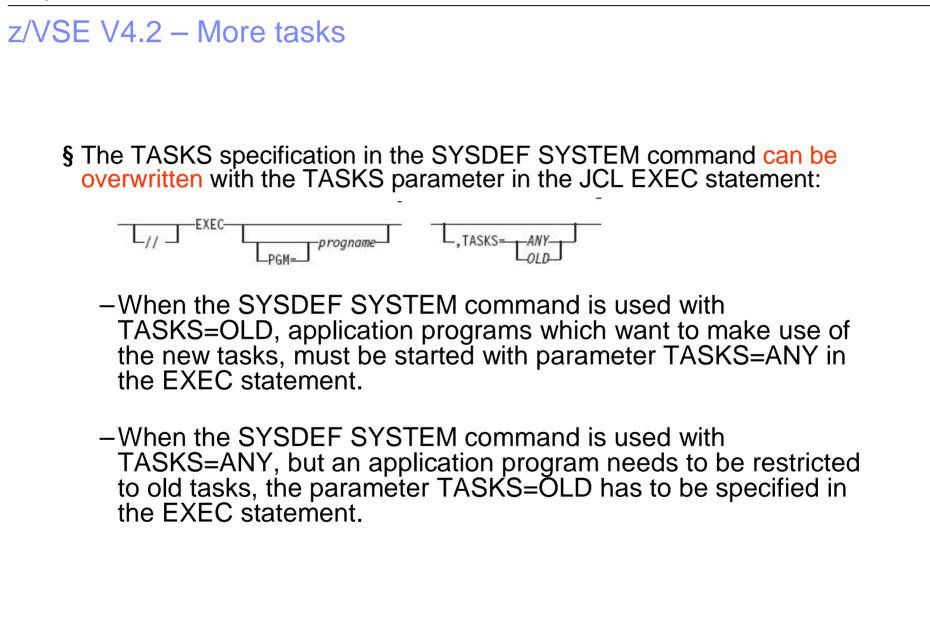




z/VSE V4.2 – More tasks § The SYSDEF SYSTEM command is used to activate the new tasks support system-wide. -, TASKS=ANY-YSDEF SYSTEM . TASKS=0LD-.NTASKS= nnn § NTASKS=nnn|MAX - nnn specifies the total number of tasks (old and new) that can be allocated to the system and application programs. This is possible only during BG ASI processing. The value of nnn can be between 255 and 512. § TASKS=ANY|OLD - This is the system-wide default mode for subtask attaching, it can be run at any time after IPL: • If TASKS=ANY is specified, new or old tasks can be attached as subtasks. However, primarily new tasks will be attached. OLD specifies that only old tasks will be attached as subtasks. **§** Use QUERY SYSTEM to display what has been specified with SYSDEF SYSTEM



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- NEWY
- § Parallel Access Volume (PAV) is an optional licensed feature on the IBM System Storage DS6000/DS8000 series
- § Parallel access volumes:
 - -Are managed by creating multiple addresses (aliases) for a single logical device.
 - -Allow your z/VSE system to access volumes in parallel.
 - -Enable more than one I/O operation to be processed for a single logical device.
 - Depending upon workload, might represent a significant performance improvement by the storage unit over traditional I/O processing.
 - Can significantly reduce device queue delays to busy devices (all I/O operations are normally processed from a single queue).
 - Allow your system to access a single volume from a single z/VSE host with multiple concurrent requests.

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Alias X

Base



- **§** To gain a performance benefit from PAV, it is required that:
 - -the workload can utilize multiple paths (sub channels) to the same volume
 - A single job that starts an I/O and waits until its completion before it starts another I/O does not benefit from PAV by itself
 - -However, running multiple such jobs concurrently in multiple partitions can utilize parallel access to the same volume.
- § Besides the simple 'Start I/O and wait' behavior, more sophisticated programs (like CICS) may be capable to start multiple I/Os and wait for its completion asynchronously
 - -This behavior also is eligible for benefiting form PAV, if the I/Os are for the same volume
- § Jobs that use multiple subtasks that perform I/O operations may benefit from PAV
- **§** Running multiple jobs concurrently in separate partitions and access the same volume are also good candidates for PAV



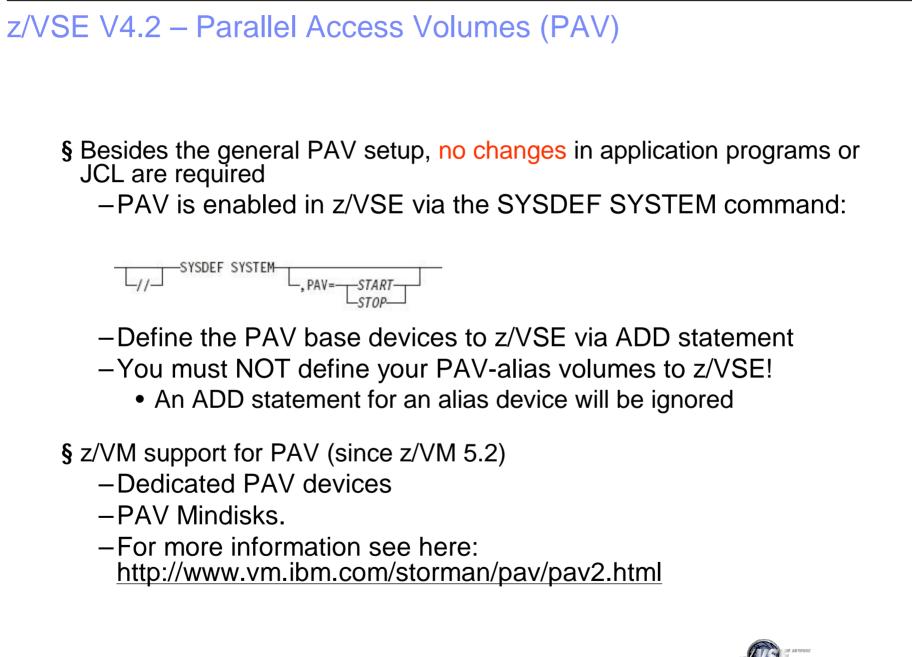


- § Candidates for PAV volumes
 - In general, all volumes that contain files, catalogs of data in general that are used from multiple jobs can benefit from PAV
 - Without PAV, I/Os might get queued and therefore delayed in case of parallel access to the same volume
 - PAV allows parallel access to these files from different jobs without disturbing each other.
 - -VSAM Catalogs
 - Shared VSAM Clusters
 - -VSE Libraries
- **§** Besides volumes that contain files that are shared between multiple jobs, also volumes that contain heavily used system files can benefit from PAV
 - Although there might not be any parallel access to those system files as such, there may be parallel access to other files residing on the same volume
 - Without PAV, I/Os might get queued and therefore delayed in case of parallel access to the same volume
 - PAV allows parallel access to these volumes without being disturbed by access to the system files.
 - POWER Spool files
 - -Workfiles

– Log files

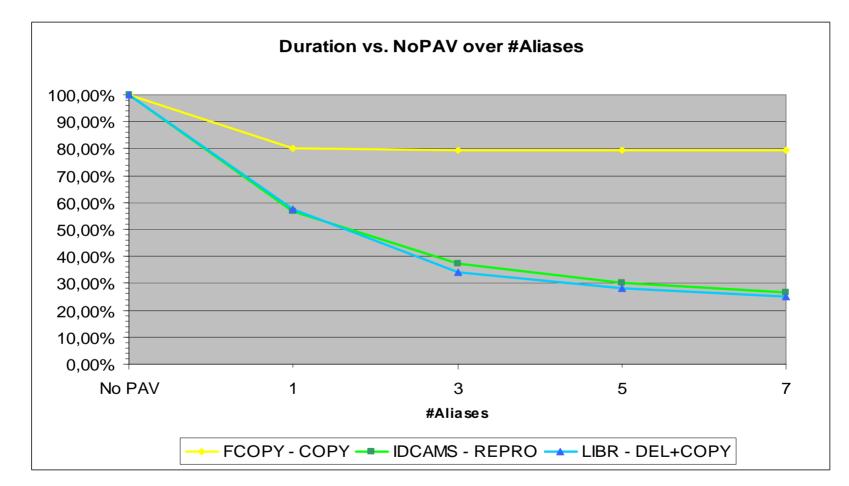


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PAV performance measurements:



Conclusion: Dependent on the workload, PAV can dramatically increase the I/O throughput and reduce the job duration (e.g. 1/3 of the duration when running without PAV), if it is not limited by other factors (like LOCKs).



z/VSE V4.2 – CPU Balancing



§ Using CPU Balancing can reduce the multiprocessing overhead

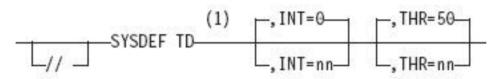
- -When CPU Balancing is active, the Turbo Dispatcher only selects CPUs that are required for the current workload
- -CPU Balancing might also reduce the overhead or performancedegradation for I/O-intensive workloads that are running in one partition only (the remaining partitions are idle) when multiple CPUs are active
- **§** With CPU Balancing active, Turbo Dispatcher inspects the CPU utilization periodically
 - -When the the utilization falls below a certain threshold, CPUs are dynamically stopped
 - -When the the utilization increases over the threshold, CPUs are dynamically started
- § This results in only as many CPUs being active that are utilized by the current workload





z/VSE V4.2 – CPU Balancing

§ CPU Balancing is activated using the SYSDEF TD command



§ INT=nn - nn defines the interval in seconds, after which the CPUs utilization is to be inspected.

- When 0 is specified, CPU balancing will be deactivated
- The default value is 0.
- The value must be in the range of: nn=0..99

§ THR=nn - nn defines the threshold value in percent

- An additional CPU is activated, when the CPU utilization is larger than nn
- The default value is 50
- The value must be in the range of: nn=10..99
- § You can use the QUERY TD command to obtain information about the current status of CPU balancing





z/VSE V4.3 Performance Considerations

- § Support for 4 digit device addresses
- § GETVIS constraint relief
- § Dynamic start/stop of CPUs
- § 1 MB frames for data spaces
- § Fast Path to Linux on System z
- § Queue-I/O Assist (QIOASSIST)
- § Crypto Express3 and AP queue interrupt support
- § FICON Express8
- § SNMP Agent support
- § VSAM Redirector executed in subtask under CICS



z/VSE V4.3 – Support for 4 digit device addresses

- § z/VSE now supports 4 digit device addresses (that is, physical addresses) of up to X'FFFF'
- **§** This support is implemented as follows:
 - z/VSE applications, messages, commands, and so on, do not address a device by the physical address (pcuu), but instead by the VSE address (cuu)
 - VSE addresses are in the range from X'000' to X'FFF'
 - To each physical address (pcuu) there is a corresponding VSE address (cuu)
 - If the physical address is less than or equal to X'FFF', the VSE address (cuu) is equal to the physical address (pcuu)
 - If the physical address is higher than X'FFF' (and therefore outside the range of VSE addresses), the physical address (pcuu) and VSE address (cuu) will be different

§ There is no performance impact by using 4 digit addresses





z/VSE V4.3 – GETVIS below constraint relief

§ Several components have been updated to reduce the usage of GETVIS below the line:

- I/O control blocks
- VSAM code and buffers/control blocks
- DL/1 1.12

§ Allocating I/O Control Blocks Above 16 MB Line

- The IODEV supervisor parameter specifies the number of Input/Output (I/O) devices the z/VSE supervisor will support
- Using the IODEV parameter, you can instruct the z/VSE supervisor to allocate various Input/Output (I/O) control blocks in the 31-bit shared addressing area (below the 2 GB line) instead of in the 24-bit shared addressing area (below the 16 MB line)
- You can set IODEV to either:
 - **1024**, which means the z/VSE supervisor will allocate I/O control blocks in the 31-bit shared area. This is the default value
 - 1023, which means the z/VSE supervisor will allocate I/O control blocks in the 24-bit shared area (as in previous z/VSE releases). This provides compatibility for Vendor programs that will only run when I/O control blocks are allocated in the 24-bit shared area
- Note: If you run z/VSE with IODEV set to 1024, any Vendor-supplied programs that have not been modified so they address control blocks moved to the 31-bit shared area will no longer work! In such situations, contact the appropriate Vendor.





z/VSE V4.3 – GETVIS below constraint relief

§ VSAM GETVIS constraint relief

- VSE/VSAM modules have been relocated from the 24-bit to 31-bit SVA storage area
- VSE/VSAM internal control blocks have been moved from 24-bit to 31-bit partition GETVIS
- VSE/VSAM storage is now acquired from GETVIS sub-pools, therefore allowing real-time monitoring of GETVIS usage
- User-generated VSE/VSAM control blocks (RPL, ACB, EXLST), as well as action macros, can now be located-in / executed-from 31-bit partition GETVIS.
- DLBL statement enhancements:
 - You can now specify allocated space in blocks and cylinders for VSE/VSAM Managed-SAM clusters
 - You can now use the BUFDAT=RMODE31 parameter to allocate buffers in 31-bit partition GETVIS, without the need to recompile legacy applications.

§ DL/1 1.12 GETVIS constraint relief

- z/VSE 4.3 includes a new release (Version 1 Release 12.1) of DL/I VSE providing storage constraint relief in the 24-bit area of a CICS/DLI partition
- In a CICS/DLI online environment, the following DL/I resources can be allocated in 31-bit storage above the 16 MB line:
 - Load PSBs and their transaction working copies
 - HD ESDS buffers.
 - DL/I action modules and user exit routines.





z/VSE V4.3 – Dynamic Starting/Stopping of CPUs

§ z/VSE allows you to start CPUs in that were not online at IPL

- **§** These can be either:
 - CPUs that were in a "standby" state at IPL
 - CPUs that were added to the z/VSE LPAR profile after IPL
- § Note that z/VSE uses the term CPU to refer to Central Processors (CPs).

§ Using the HMC/SE "Logical Processor Add" task, you can add CPUs to an LPAR after IPL. This feature is available on IBM z10 and z196 platforms.

- When CPUs are added to an LPAR, z/VSE automatically updates its CPU configuration.

§ You can then use the:

- SYSDEF TD,STARTSBY=cpuaddr command to set CPUs that are in a "standby" state to an "online" state and start these CPUs
- SYSDEF TD,STOPSBY=cpuaddr command to change the CPU state from "online" to "standby".
- § These functions allow you to exploit z10 and z196 technology and update the CPU configuration depending on workload needs
- § Note: "Standby" CPUs do not consume any CPU share of their LPAR





z/VSE V4.3 – Support for 1 MB Frames for Dataspaces

- § The 1 MB frame support (also referred to as "large page support" or "1 MB page support") allows 1 MB of virtual storage to be backed with 1 MB frames in processor storage
- **§** The 1 MB frame support is available:
 - on IBM z10 and z196 platforms
 - in LPAR mode only.

§ z/VSE uses 1 MB frame support for data spaces.

- Long-running applications accessing data spaces frequently might benefit from improved CPU utilization.
- 1 MB frame support for data spaces might help you to exploit large processor storage to a greater extent.

§ z/VSE implements this support transparently:

- In order to take advantage of z/VSE's 1 MB frame support, you are not required to perform any actions.
- z/VSE decides internally when and how data spaces will be backed with 1 MB frames.
 Therefore, a data space can consist of both "fixed" and "pageable" virtual storage.
- If the z/VSE system runs out of processor storage, one or more 1 MB frames used for backing data spaces will be made available again for use by the system.
- **§** Data space support in z/VSE is configured using the SYSDEF DSPACE command.
 - The default size of a data space (DFSIZE) is 960 KB.
 - All data spaces that you define with a maximum size of at least 960 KB will benefit from 1 MB frame support providing there is sufficient processor storage available.





z/VSE V4.3 – Fast Path to Linux on System z (LFP)

- § The Linux Fast Path uses an IUCV connection between z/VSE and Linux, where both systems run in the same z/VM-mode LPAR on IBM z10 or z196 servers
 - It allows selected TCP/IP applications to communicate with the TCP/IP stack on Linux without using a TCP/IP stack on z/VSE
 - All socket requests are transparently forwarded to a Linux on System z system running in the same z/VM
- § On Linux on System z, the LFP daemon must run
 - This daemon fulfills all socket requests by forwarding them to the Linux TCP/IP stack.
- § The fast path to Linux on System z provides standard TCP/IP socket APIs for programs running on z/VSE:
 - LE/C socket API via an alternative \$EDCTCPV.PHASE (IJBLFPLE)
 - EZA SOCKET and EZASMI interface via an alternative EZA interface phase IJBLFPEZ
 - CSI's (Connectivity Systems, Incorporated) assembler socket interface via the SOCKET macro
 - Other than the basic socket API, no other tools are provided.

§ Performance increase due to:

- Less overhead for TCP/IP processing on z/VSE (TCP, sequence numbers and acknowledging, checksums, resends, etc)
- More reliable communication method (IUCV) compared to HiperSockets, which is a network device, with all its packet drops, resends, etc.



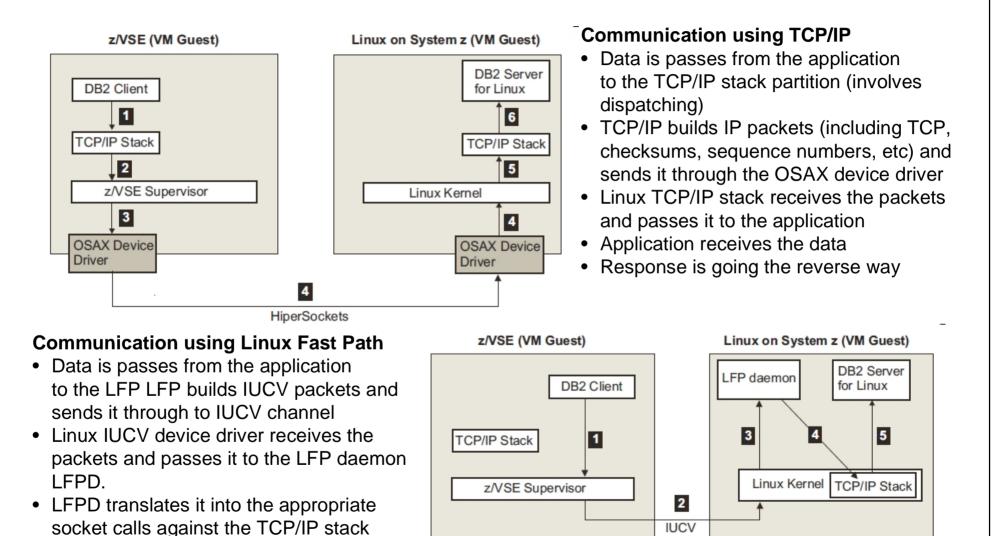


OSAX Device

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Driver

z/VSE V4.3 – Fast Path to Linux on System z (LFP)



OSAX Device

Driver

- TCP/IP passes the data to the application
- Response is going the reverse way



z/VSE V4.3 – Queue-I/O Assist (QIOASSIST)

- § The z/VM function queue-I/O assist (QIOASSIST) provides performance improvements for V=V guests using real adapters and real networking devices that use the Queued Direct I/O (QDIO) facility
- § z/VSE exploits the queue-I/O assist function for:
 - OSA Express devices (CHPID type OSD)
 - HiperSockets devices (CHPID type IQD)
- § To use the queue-I/O assist (QIOASSIST) function in z/VSE, use the z/VM CP command: - SET QIOASSIST ON
- § After you have enabled the queue-I/O assist function, each z/VSE DEFINE LINK,TYPE=OSAX command will then automatically exploit the queue-I/O assist function
- § If you do not wish to use the queue-I/O assist (QIOASSIST) function in z/VSE, disable it using this z/VM CP command:

- SET QIOASSIST OFF



z/VSE V4.3 – Crypto Express3 - AP queue interrupt support

- § z/VSE supports the Crypto Express3 card (a secure coprocessor) in both coprocessor and accelerator mode
- § The Crypto Express3 card is available with IBM System z10 and zEnterprise 196
 - This Crypto Express3 generation of cryptographic cards will provide faster SSL acceleration
 - The Crypto Express3 card is recognized during the startup of the Security Server partition (default FB) in the same way as other supported cards

§ Notes:

- z/VSE uses the Crypto Express3 card with the same functionality as Crypto Express2. New functions and key lengths are not exploited.
- Crypto Express3 support is also available with z/VSE 4.2 and PTF(s).

§ AP queue interrupt support:

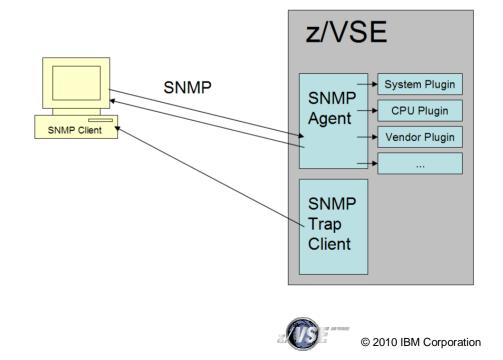
- When performing cryptographic operations on Crypto Express2 and Crypto Express3 cards, the calling program is notified via a hardware interrupt when a response is ready for de-queueing from a card
- The AP-queue adapter-interruption facility is a new function of IBM z10 and zEnterprise 196.
- However, this facility is only available when running in an LPAR (that is, not when running under z/VM).





z/VSE V4.3 – SNMP Monitoring Agent support

- § z/VSE Monitoring Agent enables customers to monitor his z/VSE systems using standard monitoring interfaces (SNMP V1)
 - It also includes an open interface, which enables customers or vendors to use own programs (plugins) to collect additional data
- § Data collected by the IBM provided plugins contains
 - Information about the environment (e.g. Processor, LPAR and z/VM information)
 - Number of partitions (static, dynamic, total, maximum)
 - Partition priorities
 - Number of CPUs (active, stopped, quiced)
 - Paging (page ins, page outs)
 - Performance counters overall and per CPU
 - CPU address and status
 - CPU time, NP time, spin time, allbound time
 - Number of SVCs and dispatcher cycles
- § A MIB (Measurement Information Base) is provided describing the data collected
- § Standard SNMP based monitoring tools can be used to collect, display and analyze z/VSE performance monitoring data
- § z/VSE SNMP Trap client is an application that you can use in (or add to) your batch jobs to send SNMP V1 traps to inform one or more monitoring stations/servers when, for example:
 - the end of a job stream is reached.
 - an error has occurred during a job stream



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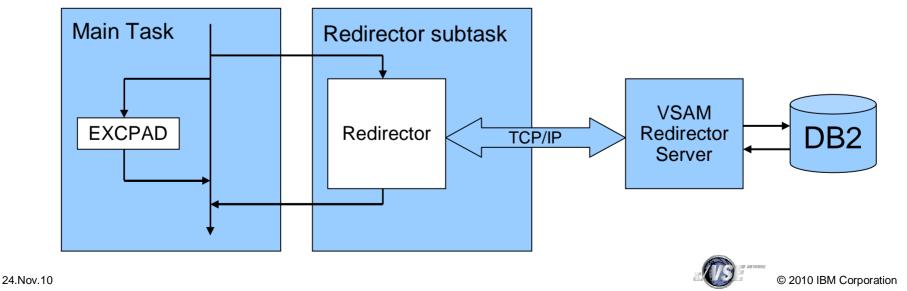
Redirector EXCPAD - Overview

§ Prior to z/VSE 4.3 the VSAM Redirector was executed in the same subtask as VSAM and the application (caller)

- Redirector activities may be time consuming (network transfers, database operations, ...)
 - During this time, no other activities are possible for this subtask
- Under CICS, VSAM normally returns back via EXCPAD exit when waiting for an I/O
 - Allows CICS to perform other activities concurrently

§ Since z/VSE 4.3 VSAM executes the Redirector under a separate subtask

- VSAM now also returns back to CICS via EXCPAD when waiting for Redirector
 - Allows CICS to perform other activities concurrently
- This capability is primarily implemented for CICS TS transactions.
 - The Redirector EXCPAD is not used for VSAM files opened by CICS/VSE.



z/VM 5.4 Considerations

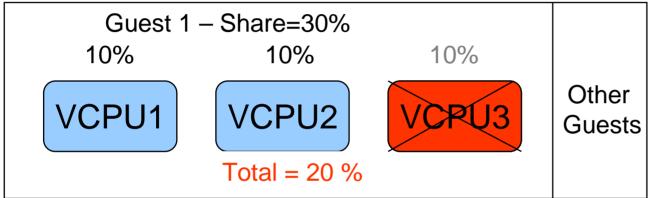
- § z/VM V5.4 removes one of the consequences of stopped virtual processors for virtual processor prioritization
- § Prior to z/VM V5.4, a guest's CPU share was distributed equally among its virtual processors
 - by dividing its share value by the number of non-dedicated virtual processors in the configuration
 - regardless of whether the virtual processors were in a stopped or started state
- § z/VM V5.4 performs share redistribution whenever a virtual processor is started or stopped
 - and no longer includes stopped virtual processors in the calculation of how much share to distribute to each virtual processor
- **§** The share redistribution also continues to occur in z/VM V5.4, as in previous releases
 - at the time a SET SHARE command is issued
 - or when the number of defined virtual processors is altered.





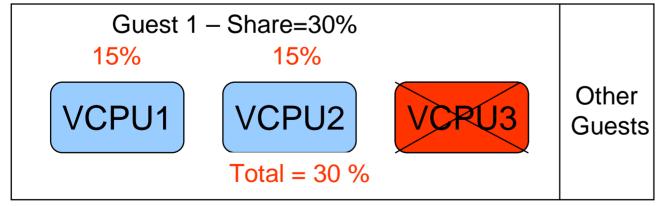
z/VM 5.4 Considerations

<= z/VM 5.3



A guest's CPU share is distributed equally among its virtual processors by dividing its share value by the number of processors, regardless of whether the virtual processors were in a stopped or started state.

z/VM 5.4



z/VM V5.4 performs share redistribution whenever a virtual processor is started or stopped and no longer includes stopped virtual processors in the calculation of how much share to distribute to each virtual processor.





Sizing a system for z/VSE

- § Sizing a system for z/VSE is different from sizing a system for z/OS
 - Although z/VSE supports multiprocessing,
 z/VSE does not scale as good as z/OS does
 - Do not use more than 3 active processors per z/VSE LPAR or z/VM Guest

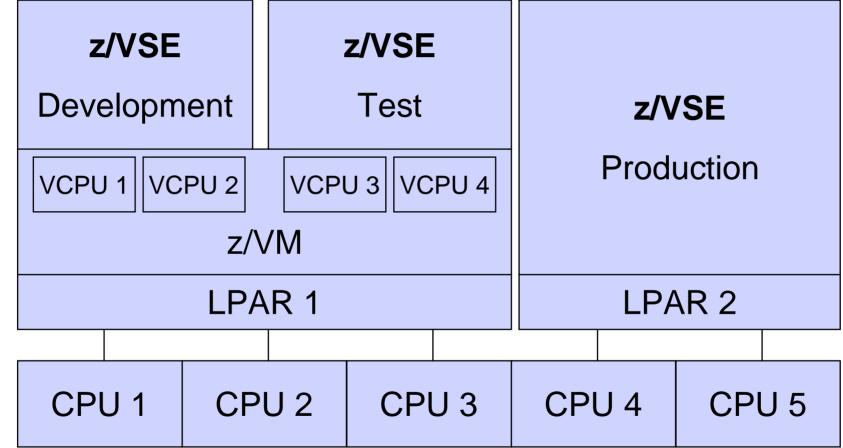


- § In general, a faster single CPU is better than multiple smaller CPUs
 - One partition can only exploit the power of one CPU
 - The largest partition (e.g. CICS) must fit into one single CPU
 - Dependent on nonparallel share (NPS) value
- § Additional CPUs can be useful when multiple LPARs or z/VM Guests are used
 - Define only up to 3 CPUs per LPAR or z/VM Guest, even if more than 3 CPUs are available on the CEC
- § Do not use MIPS tables for capacity planning purposes
 - Use zPCR Tool (see page 24) instead with the CB-L workload
 - Use free of charge Capacity Planning Services from IBM





Sizing a system for z/VSE – Example 1

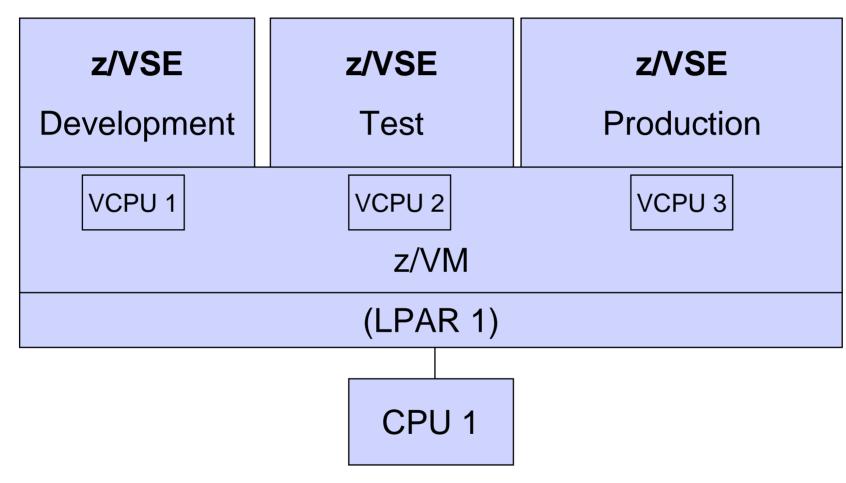


§ Although the CEC has 5 CPUs, each VSE only sees 2 CPUs

§ Test & Development systems have no influence on production system



Sizing a system for z/VSE – Example 2



§ z/VM does a very good job in sharing a single CPU across multiple guests systems

§ Use SET SHARE (ABSOLUTE/RELATIVE) command in z/VM to prioritize production systems







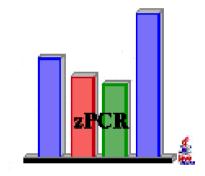
(*) from a single VSE-image point o view

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IBM Processor Capacity Reference for zSeries (zPCR)

§ The zPCR tool was released for customer use on October 25, 2005

- http://www.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/PRS1381
- 'As is', no official support, e-mail to zpcr@us.ibm.com
- § PC-based productivity tool under Windows
- § It is designed to provide capacity planning insight for IBM System z processors running various workload environments



§ Capacity results are based on IBM's LSPR data supporting all IBM System z processors

–Large System Performance Reference: <u>http://www.ibm.com/systems/z/advantages/management/lspr/</u>

§ For VSE use z/VSE workloads Batch, Online or Mixed





VSE CPU Monitor Tool

- § Intended to help customers to measure the CPU utilization of their VSE system over a period of time.
- § When you plan for a processor upgrade it is very important to know the CPU utilization of your VSE system over a day or a week.

-Helps you to estimate the size of the new processor.

- § The VSE CPU Monitor Tool is not intended to replace any existing monitoring product provided by partners.
- § It provides only very basic monitoring capabilities on an overall VSE system level.
- § No details about CPU usage of certain applications are provided
- § New version available (XML Output) for z/VSE Capacity Planning

§ Download

- -http://www.ibm.com/systems/z/os/zvse/downloads/tools.html
- 'As is', no official support, e-mail to zvse@de.ibm.com





VSE CPU Monitor Tool

- **§** CPUMON periodically issues a TDSERV FUNC=TDINFO macro to get performance relevant data.
- § The data provided by the macro is the same as command QUERY TD shows.
- **§** The data from each measurement interval is printed to SYSLST in a comma separated format.
- § Later on this data can be imported into a spreadsheet (EXCEL)
- § CPUMON runs in a VSE partition (dynamic or static).
- § CPUMON is started using:

```
// EXEC DTRIATTN,PARM='SYSDEF TD,RESETCNT`
/*
// EXEC CPUMON,PARM='nn` nn = interval in seconds
/*
```

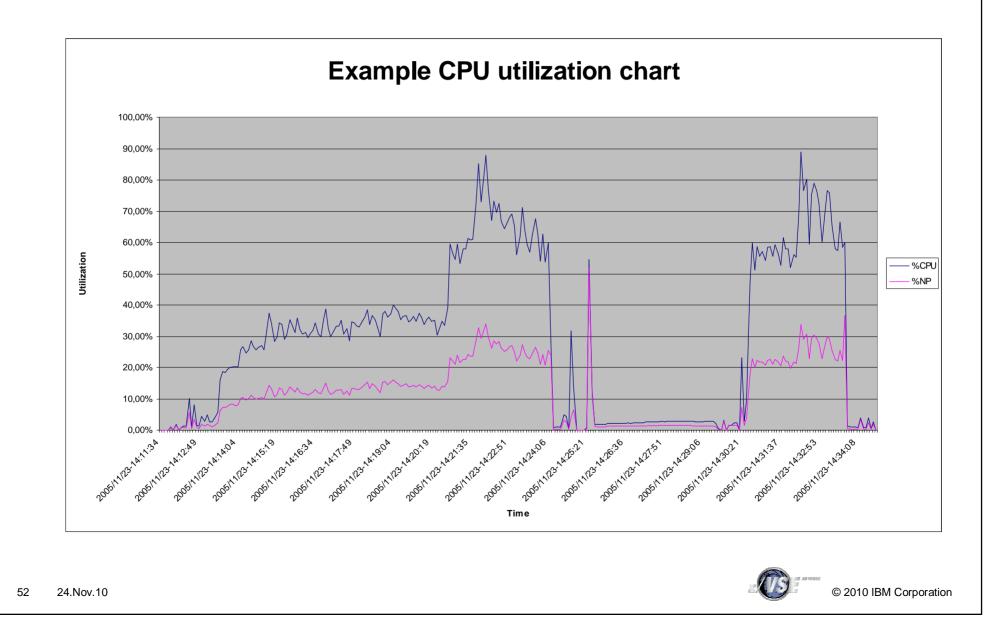
§ The tool can be stopped by entering the following command:

```
MSG xx, DATA=EXIT xx = partition id
```





VSE CPU Monitor Tool





New: z/VSE Capacity Planning Offering

§A brand new z/VSE Capacity Planning Offering is now available

- -Available for Business Partners
- -and Customers

§Performance data collection is based on a new version of the CPUMON Tool

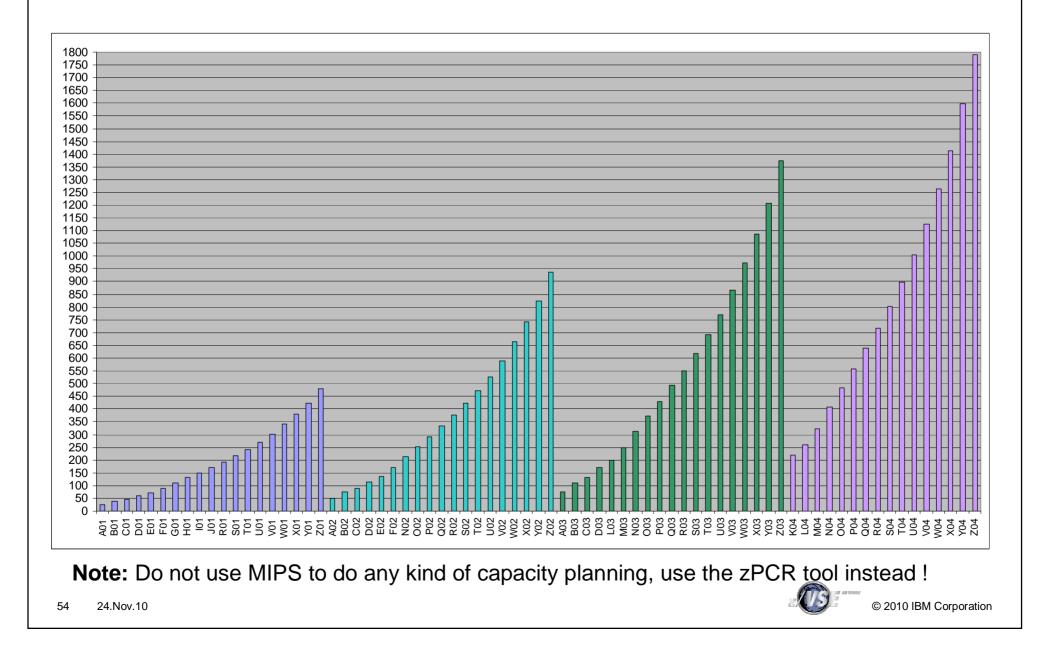
§Contact techline@us.ibm.com and ask for z/VSE Capacity Planning Support





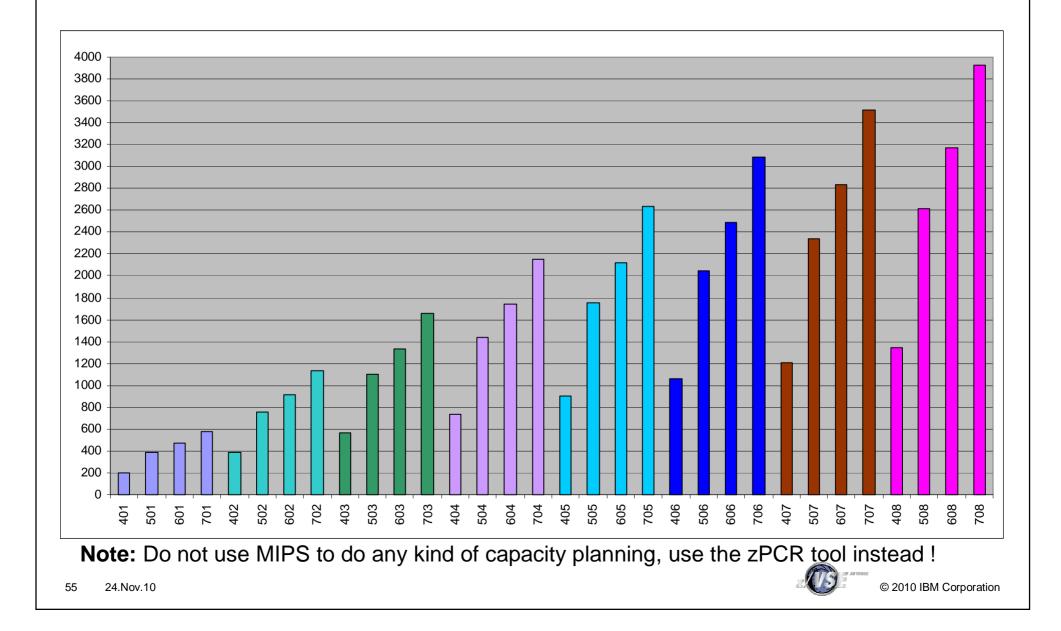


IBM System z9 BC (1-4 CPUs)



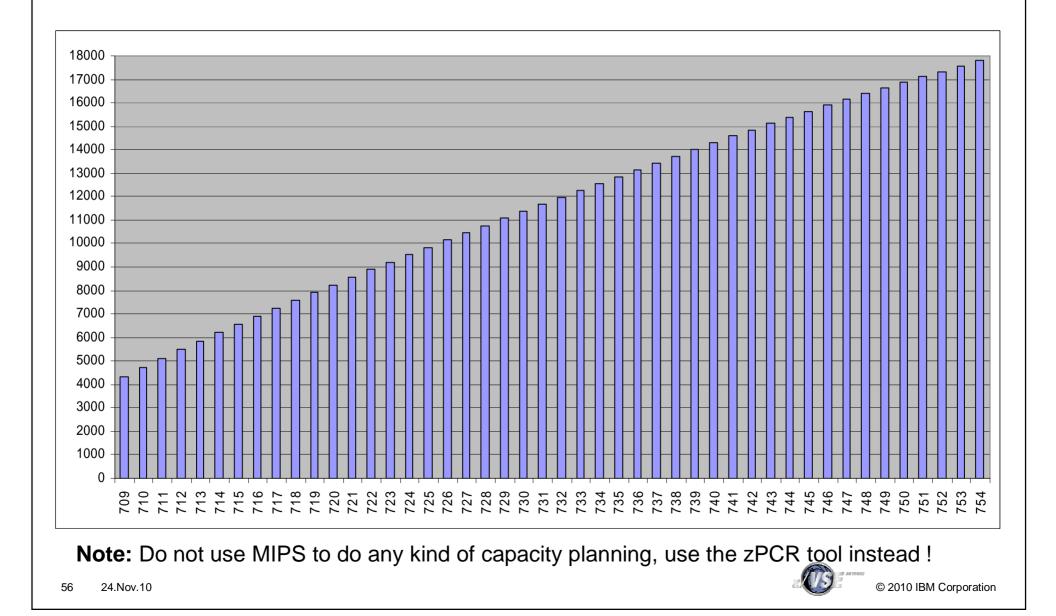


IBM System z9 EC subcapacity models (1-8 CPUs)



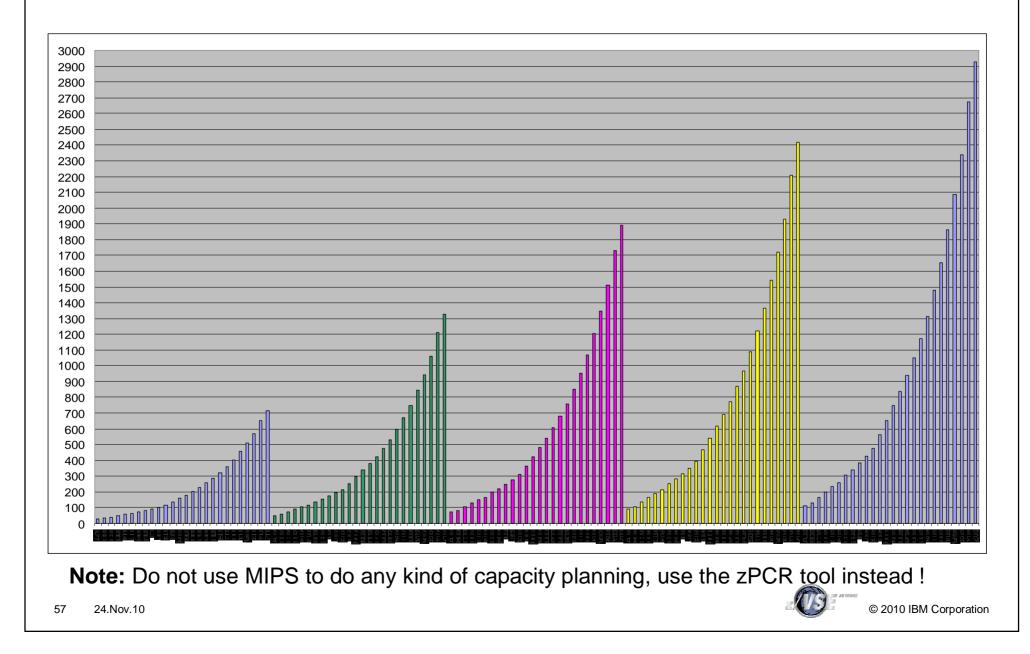


IBM System z9 EC (9-54 CPUs)



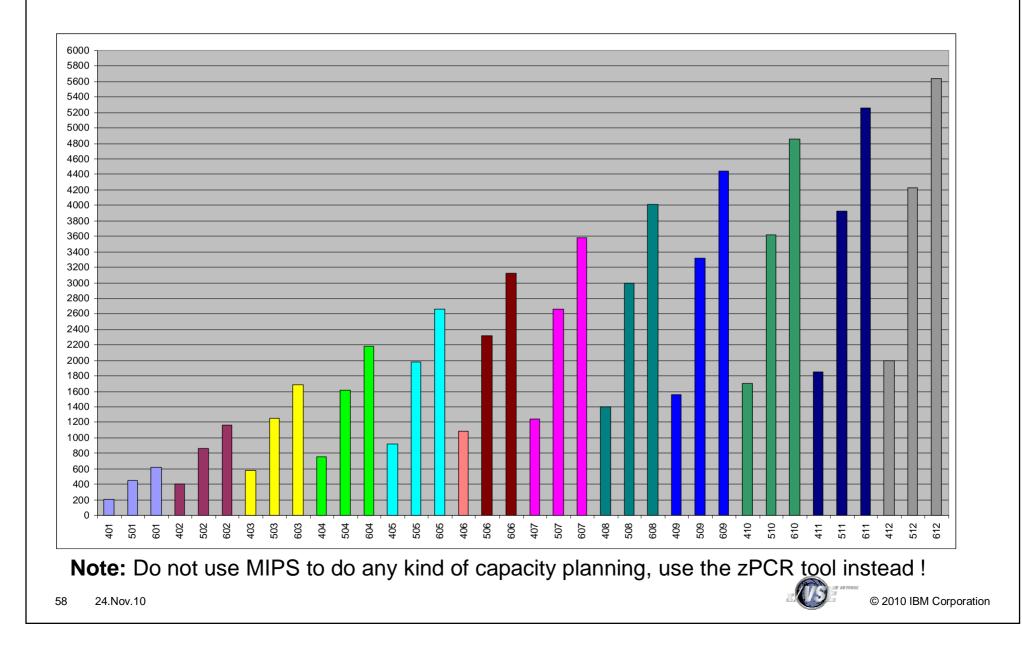


IBM System z10 BC (1-5 CPUs)



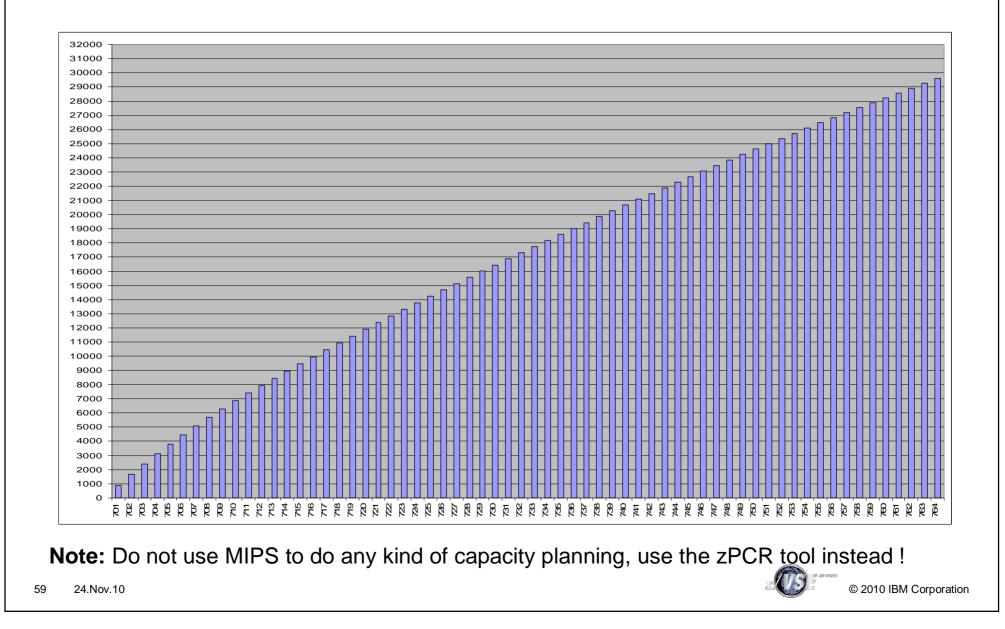


IBM System z10 EC (Models 400, 500, 600)



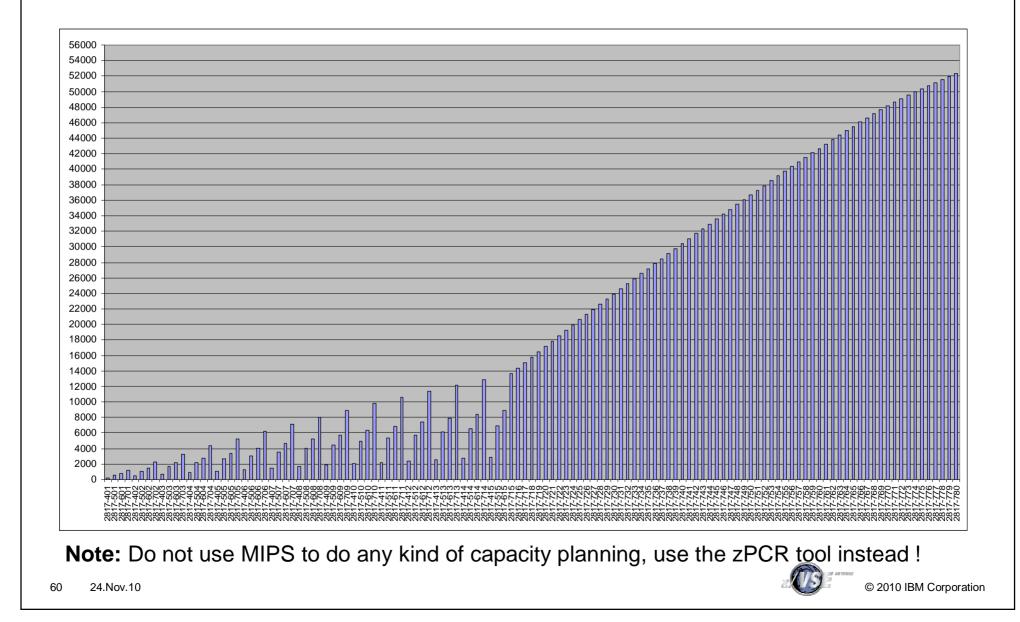


IBM System z10 EC (Models 700)





IBM zEnterprise 196





Performance Tips

- § A partition can only exploit 1 CPU at a time
 - 2 CPUs do not have any benefit for a single CICS partition
 - Use as many partitions as required for selected n-way
- § Use/define only as many CPUs as really needed
 - additional CPUs create more overhead, but no benefit
- § Partitions setup
 - Set up more batch and/or (independent) CICS partitions
 - Split CICS production partitions into multiple partitions (AOR, TOR, FOR)
- § Try to exploit Turbo Dispatcher functions
 - Priority settings
 - Partition balancing
 - Partition balancing groups







Performance Tips (2)

- § 1 CPU must be able to handle all non-parallel workload
- § Non-parallel code limits the n-Way exploitation
 - QUERY TD: NP/TOT = NPS (non parallel share)
 - Measure NPS before migration
 - max CPUs = 0.8 0.9 / NPS



NPS	#CPUs	NPS	#CPUs
0.20	4.0-4.5 (4)	0.45	1.8-2.0 (2)
0.25	3.2-3.6 (3)	0.50	1.6-1.8 (2)
0.30	2.7-3.0 (3)	0.55	1.5-1.6 (2)
0.35	2.3-2.6 (2)	0.60	1.3-1.5 (1)
0.40	2.0-2.2 (2)	0.65	1.2-1.4 (1)



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Performance Tips (3)

- § Non-parallel code limits the maximum MP exploitation
- **§** System code (Key 0) increases non-parallel share
 - Vendor code can have significant impact
- § Overhead increases when NP code limits throughput
- § Data In Memory (DIM) reduces non-parallel code
 - less system calls (I/Os)
 - may increase throughput
 - CICS Shared Data Tables
 - Large/many VSAM Buffers (with buffer hashing)
 - Virtual Disks
- **§** Change VSE/POWER startup to WORKUNIT=PA
- § Switch tracing/DEBUG off for production





zSeries Remarks – Split cache

- **§** Prior to zSeries there is one cache for data and instructions
- § zSeries has split data and instruction cache

§ Performance implications:

- If program variables and code that updates these program variables are in the same cache line (256 byte)
 - Update of program variable invalidates instruction cache
 - Performance decrease if update is done in a loop
- See APAR PQ66981 for FORTRAN compiler





zSeries Remarks – Split cache - example

Killer example:

* prepare length
BCTR R2,0 ADJUST FOR SS-INSTR.
STC R2,*+5
MVC RECEIVER(*-*),SENDER

Better code:

* prepare length
BCTR R2,0 ADJUST FOR SS-INSTR.
EX R2,MVC01
...
MVC01 MVC RECEIVER(*-*),SENDER

STC instruction modifies the next instruction to set the length.

Use EXECUTE instruction instead.

zSeries Performance: Processor Design Considerations:

http://www.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FLASH10208





zSeries Remarks – Split cache - example

Not causing a problem:

	LA	R1, PHASNAME	POINT AT PHASE NAME
	CDDELETE (1)		
+*	SUPERVISOR - CDDELETE - 5686-032-06		
+	CNOP	0,4	
+	BAL	15,*+8	
+	DC	A(B'00010010')	
+	L	15,0(,15)	
+	SVC	65	ISSUE SVC FOR CDDELETE
	DS	OH	

Can cause a problem:

	WTO TEXT=DATA		
+	CNOP	Ο,	
+	BAL	1,IHB0003A	BRANCH AROUND MESSAGE
+	DC	AL2(8)	TEXT LENGTH
+	DC	B'0000000000	010000' MCSFLAGS
+	DC	AL4(0)	MESSAGE TEXT ADDR
+IHB0003A	DS	0H	
+	LR	14,1	FIRST BYTE OF PARM LIST
+	SR	15,15	CLEAR REGISTER 15
+	AH	15,0(1,0)	ADD LENGTH OF TEXT + 4
+	AR	14,15	FIRST BYTE AFTER TEXT
+	LA	15,DATA	LOAD TEXT VALUE
+	ST	15,4(0,1)	STORE ADDR INTO PLIST
+*	SUPERV	SUPERVISOR - SIMSVC - 5686-032	
+	SVC	35	ISSUE SVC 35
@GE00016	DS	0H	

CDDELETE uses an inline flag byte, but does not modify it WTO uses an inline parameter list, but modifies the parameter list

Note: WTO can be coded with an external parameter list: WTO ...,MF=(E,addr)





Possible performance issues with PPRC

§ Issue may occur if

- -PPRC is used
- -VSE runs in native or in LPAR
- Not all devices that are defined in IOCP are also defined in VSE ADD statements

§ In case there is an PPRC state change, interrupts are sent to all LPARs where the related device are defined in IOCP.

- -If the device is defined in VSE ADD, no problem occurs: VSE will process the interrupt correctly.
- If the device is NOT defined in VSE ADD, the interrupt is ignored by VSE and the interrupt is resent very quickly to that LPAR
 - Results in very high channel activity (up to 100%)

§ Solution:

-Define ALL devices in VSE ADD that are defined in IOCP





VSE/POWER POFFLOAD Performance Issues

- § Caused by incompatibility between VSE/POWER tape format and new tape drives
- § 3490F empties cache for FSF used by POFFLOAD LOAD
 - -Install DY46164/DY46245 for VSE/ESA 2.7/2.6

§ 3590 synchronizes cache with tape for each WTM

- Install microcode FC0520 on A60 controller + VSE/AF APAR DY45817 + AR command TAPE WTM=NOSYNC
- -Unfortunately controller A50 is to small to install FC0520





New POWER POFFLOAD Append function

§ New APPEND option (new with z/VSE 4.1):

- POFFLOAD {BACKUP | SAVE | PICKUP],

queue, tapeaddr, density, class, APPEND...

- WAVV requirement WAVV200433
- Requires 3592 tape unit

§ Great performance benefit when using 3592 tape unit:

- Spool time dramatically reduced when using 3592 tape unit (spool time cut half)
- No wasting of time for skipping existing spool entries on tape when APPENDing using "Space End of Data" command

Tape unit	Search for End-Of-Data to begin APPENDing new Offload Entries	Time to Spool 206 new entries at End- of-data
3592	About 1 second	102 seconds
2490E	307 seconds (not supported)	204 seconds





Documentation

- § z/VSE homepage:
 - -http://www.ibm.com/systems/z/os/zvse/
- § z/VSE Performance:

-http://www.ibm.com/systems/z/os/zvse/documentation/performance.html

§ z/VM homepage:

-<u>http://www.ibm.com/vm</u>

- § z/VM Performance:
 - -http://www.vm.ibm.com/perf/
- § z/VM Preferred Guest Migration Considerations
 - -<u>http://www.vm.ibm.com/perf/tips/z890.html</u>
- § IBM System z Software Pricing
 - -http://www.ibm.com/systems/z/resources/swprice/
- § IBM's MSU ratings for IBM System z
 - -<u>http://www.ibm.com/systems/z/resources/swprice/reference/exhibits/hard</u> ware.html

