TeleVideo TS 800A, TS 802 and TS 802H Maintenance Manual

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TeleVideo Systems, Inc.

1.0 INTRODUCTION

The system is basically a complete user system which includes a computer board, a CRT terminal in a integrated unit and a detached keyboard. It is also designed to be used along with one of the TeleVideo Systems Service processors (TS-806 or TS816). The system has three ports. One of the ports is standard RS232 (DTE) serial port which is used for general communication purposes. The second port is for interface to a serial printer, and the third port is a RS422 serial port for interface to a service processor. The block diagram of the system is shown in Figure 1.

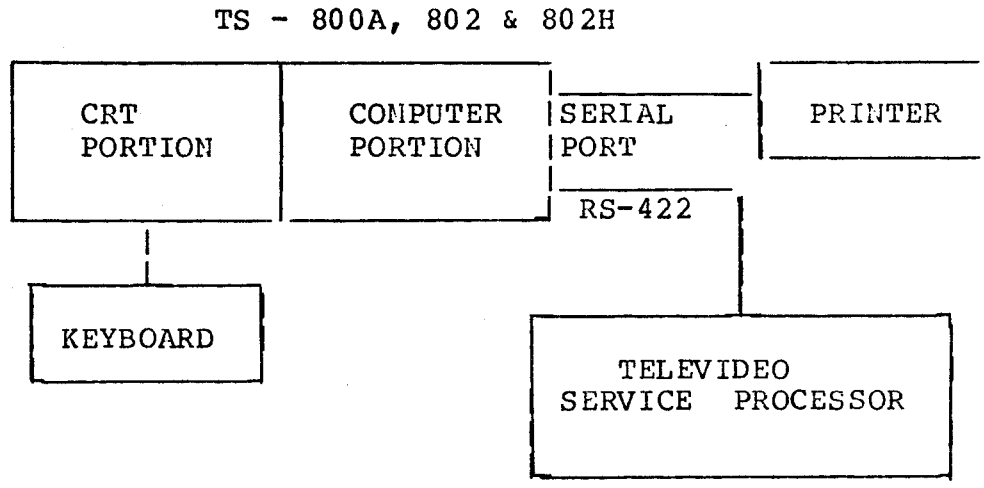


FIGURE 1 SYSTEM BLOCK DIAGRAM

2.0 TS-800A, 802 & 802H GENERAL DESCRIPTION

Logically the system is divided into two portions, a terminal portion and a Z-80 computer portion. The terminal portion is identical to the 950 terminal except that some of the circuits are modified to communicate with the Z-80 computer portion.

The computer board contains five Z-80A family chips CPU, CTC, two SIO's and a DMA; Western Digital floppy disk controller and hard disk interface on the daughter board (TS802, TS802H, Section 6) 64K bytes of dynamic RAM, 4K bytes of EPROM and all the required control logic. The power supply is a small switching power supply (TS-802 and TS-802H), providing power to all the units in the system. Western Digital Winchester disk controller board for TS802H is covered in Section 7.

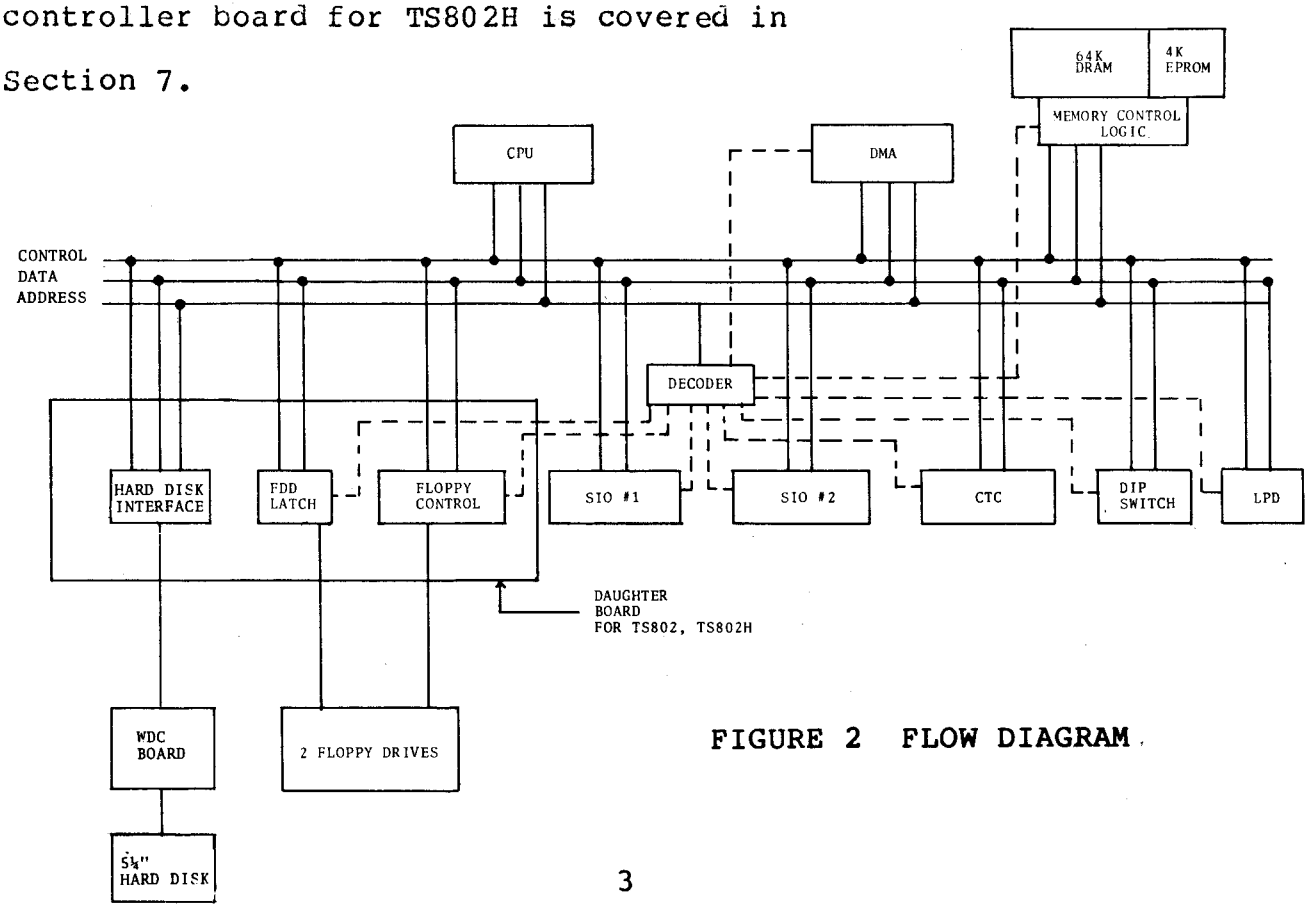


FIGURE 2 FLOW DIAGRAM

FIGURE 2 FLOW DIAGRAM

All the Z-80A chips are driven by a 4 MHz system clock which is also used to generate the necessary timing for the memory control logic. The Z80A-CPU has a 16 bit address BUS which can address up to 64K bytes of memory. The lower eight address lines are also used to address up to 256 input/output devices. During instruction fetch cycles, the CPU sends out refresh addresses and the refresh enable signal to the memory control which refreshes 64K bytes of dynamic RAM.

The computer portion has ten input/output devices which are the DMA, SIO1, SIO2, CTC, floppy disk drive select latch, floppy controller (for TS-802 and TS-802H only), dip switch, LED latch, memory latch, and hard disk interface (TS-802H only). The data BUS is an eight bit bidirectional BUS. The third BUS is the control BUS which includes the following signals, M1-, MREQ-, IORQ-, RD-, WR-, RFSH-, WAIT-, INT-, RESET-, BUSRQ- and BUSAK-. Z80A-CTC is a four channel programmable timing generating chip. It can be programmed as a timer or as a counter. The main function of this CTC is to provide transmit and receive clocks for communication with the terminal portion, RS232, printer port interface.

The Z80A-SIO is a double channel serial input/output controller. Channel A of SIO1 (A24) is programmed to use SDLC mode for the RS-422 interface (fixed 800K bits/sec) and Channel B is programmed to use asynchronous mode for communication between the computer portion and the 950 terminal portion. Channel A of

the second SIO (SIO2 A23) is used for any general purpose RS232 (DTE) communication. Channel B of SIO2 is programmed to use asynchronous mode for the serial printer port (DCE).

The Z80A-DMA is a direct memory access controller. When it is enabled, it controls the data flow between memory and SIO channel or between memory and floppy disk controller in this system. In order to guarantee the CPU refreshes dynamic memory within every 2 msec, the DMA is programmed to be used in burst transfer mode in which the DMA releases all BUSes when SIO Channel A is not requesting any data transfer.

The computer board also provides eight general purpose dip switches and four LEDs on the board. The functions of these dip switches and LEDs are software dependent.

The main memory in the computer board contains eight of 64K x 1 dynamic memory chips. Besides these 64K bytes of dynamic memory 4K bytes of EPROM are used for initialization, system diagnostics and boot operation every time after power is turned on. A detailed description of all memory will be covered in the next section.

3.0 FUNCTION OF THE SYSTEM

The clock generator of computer portion generates 1 MHz, 2 MHz and 4 MHz clock frequencies which are supplied to all CPU,

SIO, CTC, DMA PIO, floppy disk controller and memory control logic. After power is first turned on, all Z80 chips are reset to the idle state and all system chips must then be programmed individually to the correct operating mode by the program in EPROM. Dip switches are read by software and the CTC will be set to the desired clock rate for the communication between the computer portion and terminal portion, the RS232 and the printer communication. RS422 clock frequency is directly supplied from a fixed 800K Hz counter. The DMA is used during data communication between the system and service processor (TS806, TS816) and used during floppy disk data transfer. During DMA operations, the DMA uses all BUSes directly for high speed data transfer.

There are two different kinds of memory chips in the computer board (dynamic RAM and EPROM). After power is first turned on, a latch will automatically select 4K bytes of EPROM and the upper 48 K bytes of dynamic RAM as the memory space accessable by CPU. This memory space is shown in Figure 3.

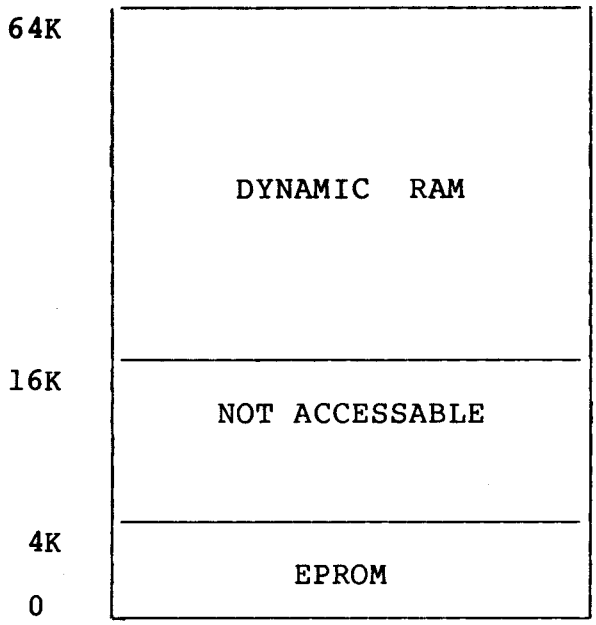


FIGURE 3 MEMORY CONFIGURATION AFTER RESET

The EPROM location from 0 to 4K contains all necessary initialization, diagnostic and system boot programs. Upon completion of the operating system loading, a single instruction (out [04H],A) will be executed and the memory space is switched to all 64K bytes of dynamic RAM as shown in Figure 4.

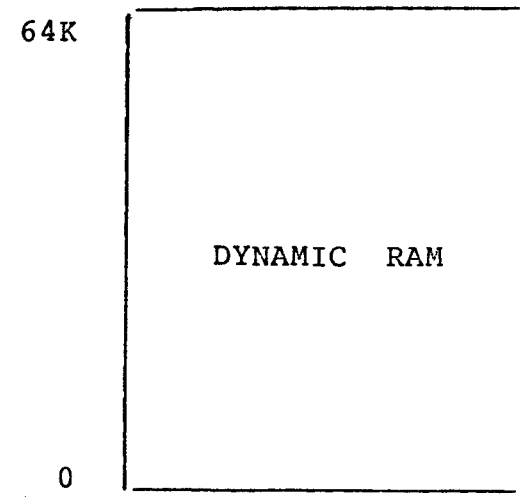


FIGURE 4 MEMORY CONFIGURATION AFTER INSTRUCTION 'OUT 04H,A'

The functions of the memory control logic is to supply necessary read/write signals, address latching signals and refresh signals to the dynamic RAM. Because of the difference in speed of the two types of memories, one cycle of "wait state" is inserted to the read/write cycle when the CPU accesses the EPROM.

4.0 OPERATION OF THE SYSTEM

4.1 Reset Operation

The reset signal in computer portion comes from the 950 portion. Either a power-up hardware reset or a software reset from the 950 portion can reset the Z-80 computer portion. The software reset is generated when the shift-break keys are pressed twice.

4.2 Clock Operation

The clock generating circuit generates 1.23 MHz, 4 MHz and 8 MHz clock which are supplied to all the Z-80A family chips, floppy disk controller and memory control circuit. A counter 93S16 (A29) is used to divide down the 16 MHz clock from the oscillator to 8 MHz clock and 4 MHz clock. Another counter (A28) is used to divide down the 8 MHz clock to 1.23 MHz clock. The system clock (4 MHz) output voltage is a critical signal for all the Z-80A family chips. The high output voltage of the clock must be between 4.4V and 5.3V and the low output voltage of the clock must be between -0.3V and 0.45V (as shown in Figure 5) in order to satisfy this requirement. A transistor (2N2907) is used to pull the clock output high voltage to about 5V.

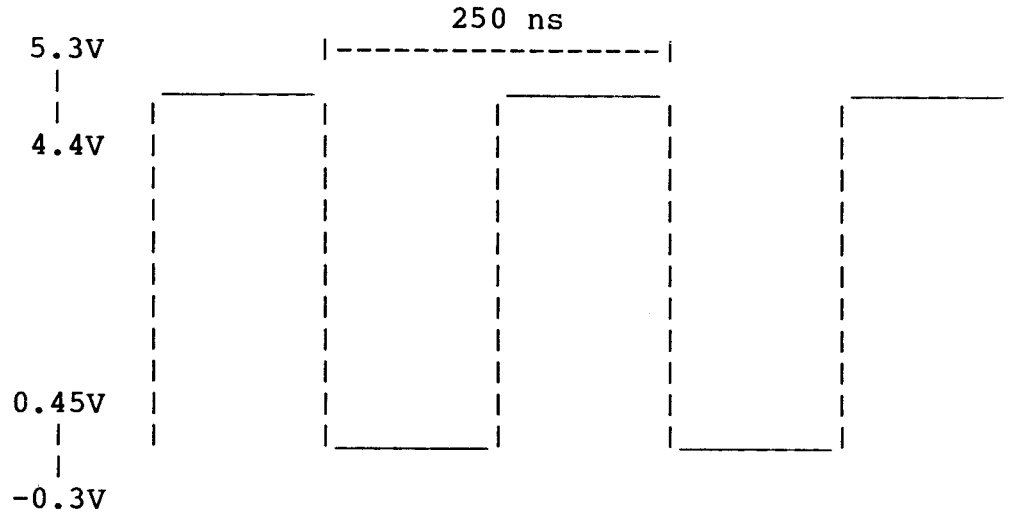
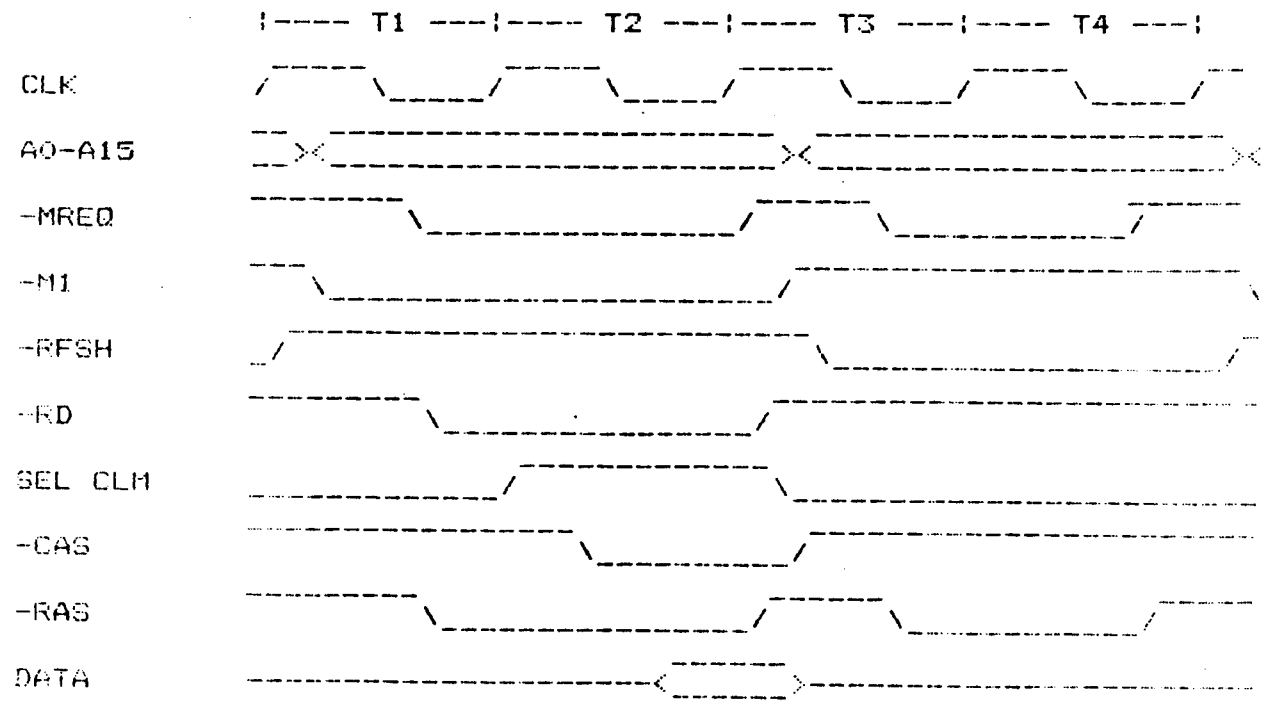


FIGURE 5 SYSTEM CLOCK

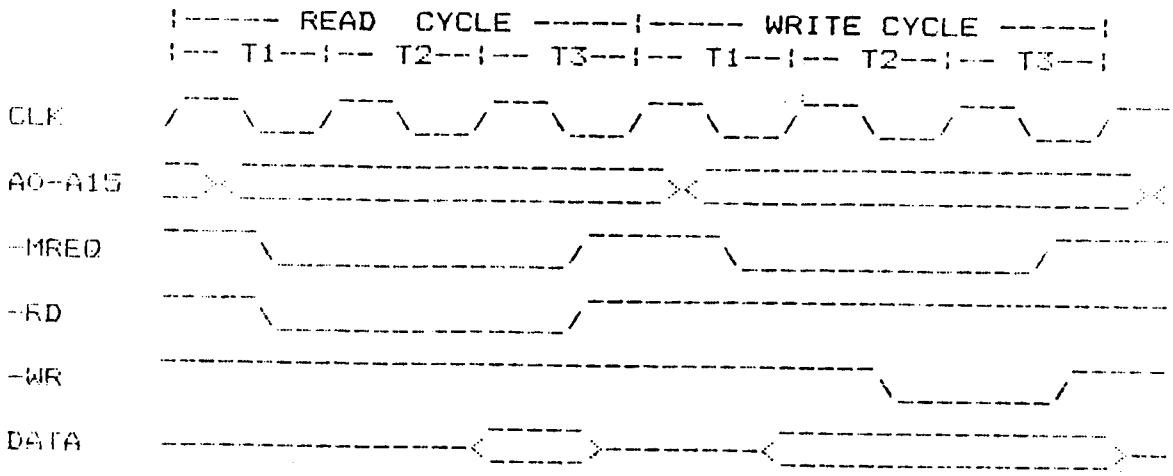
4.3 Memory Operation

Each dynamic RAM used in the computer portion system is organized as a 65536 X 1 word. Eight dynamic RAM chips are used in one system. Multiplexed addressing and periodic refreshing are required for this type of memory. The memory timing diagram is shown in Figure 6. The MREQ- signal and RFSH- signal from the CPU are input to the memory control circuit (sheet 10 of the schematic). Two multiplexers 74S157 (A30 and A38) are used to multiplex the 16 bit address lines from the CPU into the 8 bit address lines on the dynamic memory. Row address and column address are latched internally by the falling edge of the RAS- and CAS- signals, respectively. Each memory cell in the memory chip must be refreshed at least every two milliseconds. The type of refresh mode is "RAS only" for the 64K RAMs and the Z80 CPU operates in the "128 refresh cycle" mode. A serial resistor (68

ohm) is connected to each address line, the RAS- and CAS- signal lines in the dynamic memory. The purpose of using these resistors is to reduce the signal under-shoot on the lines.



INSTRUCTION FETCH FROM DRAM



READ/WRITE FROM DRAM WITHOUT WAIT STATES

FIGURE 6

PREFACE

Any comments and suggestions on this manual are welcome. Please address them to:

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1170 Morse Ave.
Sunnyvale, CA 94086

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4.4 DMA Operation

During DMA operation, the CPU stops sending refresh signals to the memory control circuit. Memory contents will be lost if the DMA holds the BUSes for more than two msec. The other type of memory used in this system is the EPROM. Since the EPROM has a slow access time compared with the Z-80A memory access time, one "wait cycle" is automatically inserted by the "wait control circuit" when the EPROM is accessed (Figure 7). This "wait control circuit" is implemented with two D flip-flops (74LS74) shown on sheet 10 of the schematic.

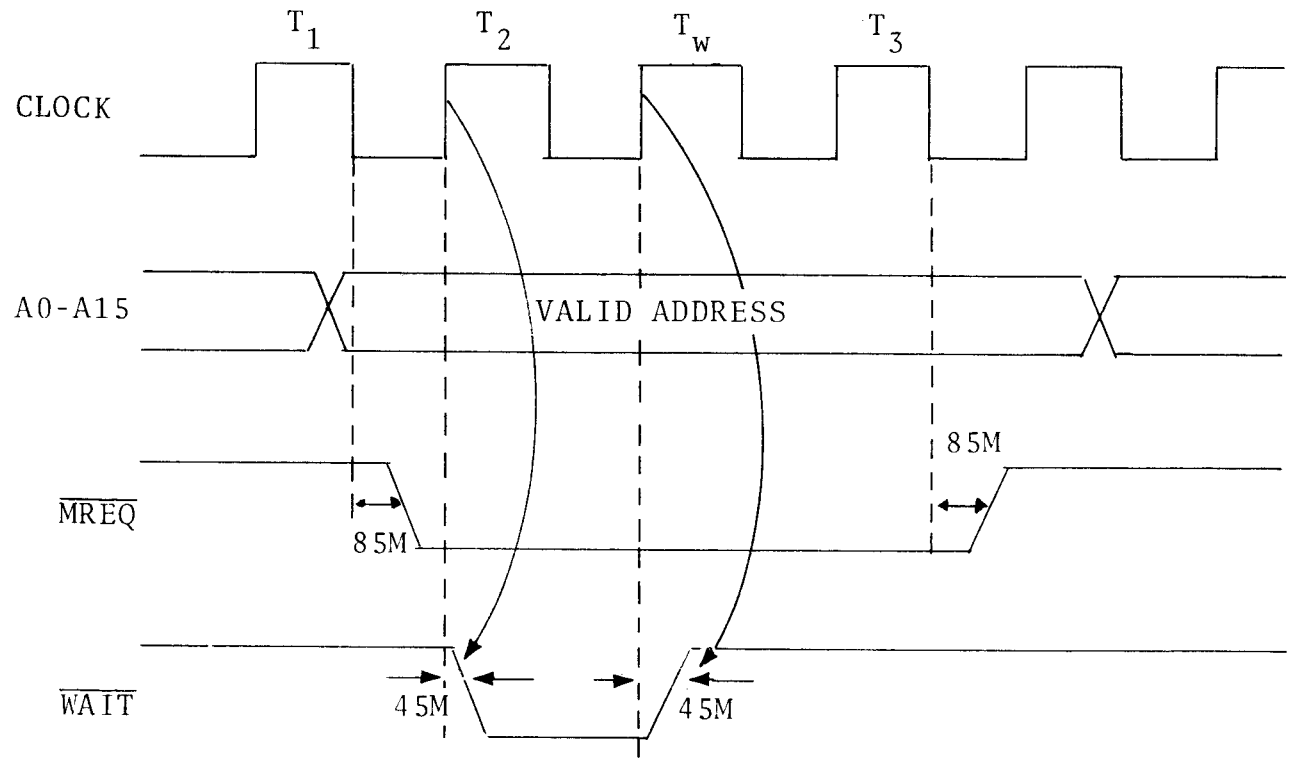


FIGURE 7 WAIT CYCLE INSERTED TIMING

4.5 I/O Operation

The computer board has a total of ten logical I/O devices. They are the dip switch, memory latch, CTC, SIO1, SIO2, DMA and floppy disk controller floppy disk drive select latch, LED latch and hard disk interface.

During CPU input/output, read/write operations, the CPU sends out the I/O device address on the address BUS. The contents of the address BUS is decoded by a decoder 74LS138 (A43) to select one of the I/O devices (Table 1).

INPUT/OUTPUT PORT ADDRESSES OF THE SYSTEM

LOCATION		
	. DIP SWITCH ------ 00H	
	. MEMORY LATCH ------ 04H	
A25	. CTC CHANNEL 0 ------ 08H	
	. CTC CHANNEL 1 ------ 09H	
	. CTC CHANNEL 2 ------ 0AH	
	. CTC CHANNEL 3 ------ 0BH	
A24	. SIO1 CHANNEL A (DATA) ------ 0CH	RS422
	. SIO1 CHANNEL A (COMMAND/STATUS) ------ 0EH	
	. SIO1 CHANNEL B (DATA) ------ 0DH	INTERNAL RS2
	. SIO1 CHANNEL B (COMMAND/STATUS) ------ 0FH	
A21	. DMA ------ 10H	
A23	. SIO2 CHANNEL A (DATA) ------ 20H	RS232 MODEM
	. SIO2 CHANNEL A (COMMAND/STATUS) ------ 22H	
	. SIO2 CHANNEL B (DATA) ------ 21H	RS232 PRINTE
	. SIO2 CHANNEL B (COMMAND/STATUS) ------ 23H	
	. FLOPPY DISK CONTROLLER LATCH ------ 18H	
	. FLOPPY DISK CONTROLLER ------ 14H-17H	
	STATUS REGISTER ------ 14H	
	TRACK REGISTER ------- 15H	
	SECTOR REGISTER ------ 16H	
	DATA REGISTER -------- 17H	
	. LED LATCH ------ 80H	
	. 5 1/4 hard disk ----- 48H-4FH	

TABLE 1

DATA REGISTER ------	48H
ERROR REGISTER -----	49H
SECTOR COUNT -------	4AH
SECTOR NUMBER ------	4BH
CYL. NUMBER LOW ----	4CH
CYL. NUMBER HIGH ---	4DH
SDH ----------------	4EH
STATUS REGISTER ----	4FH

I/O timing of each I/O device is shown from Figure 8 to Figure 15.

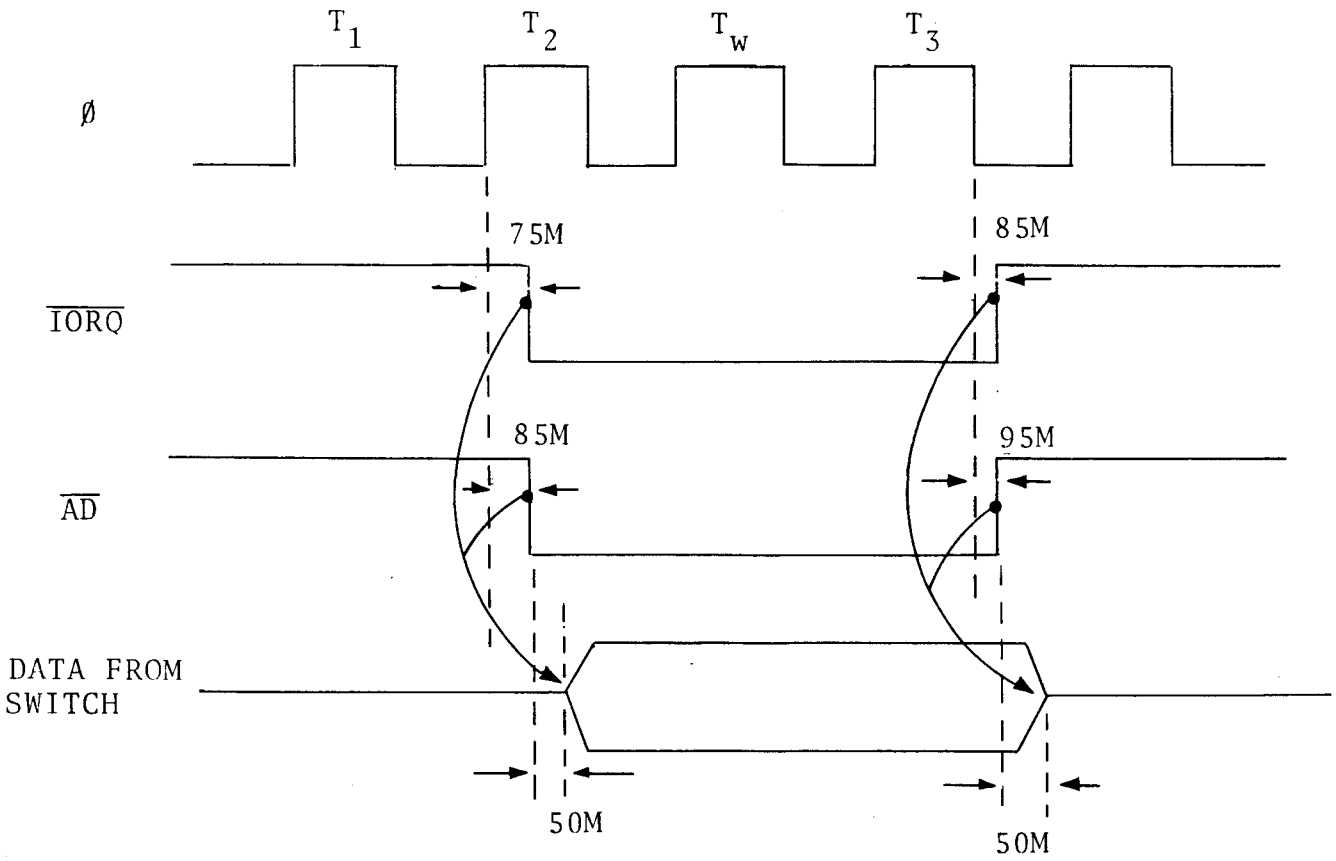


FIGURE 8 SWITCH READING TIMING

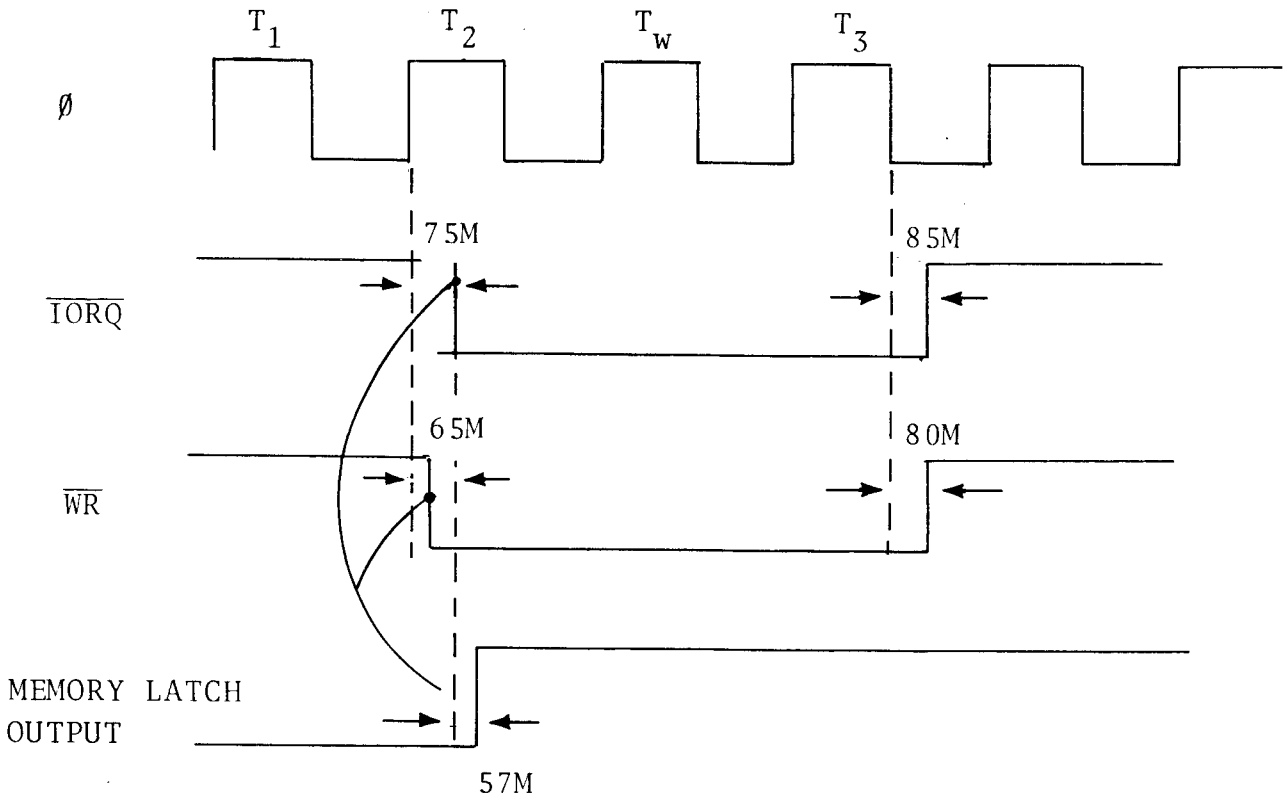
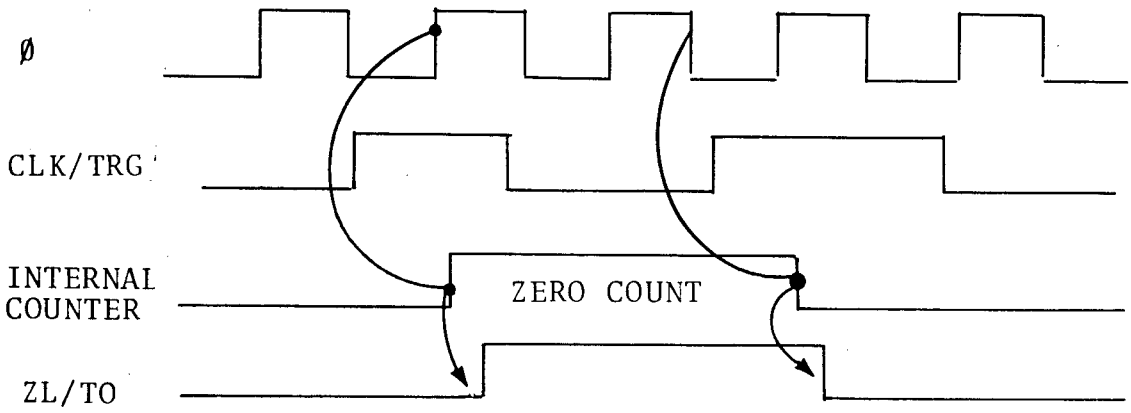
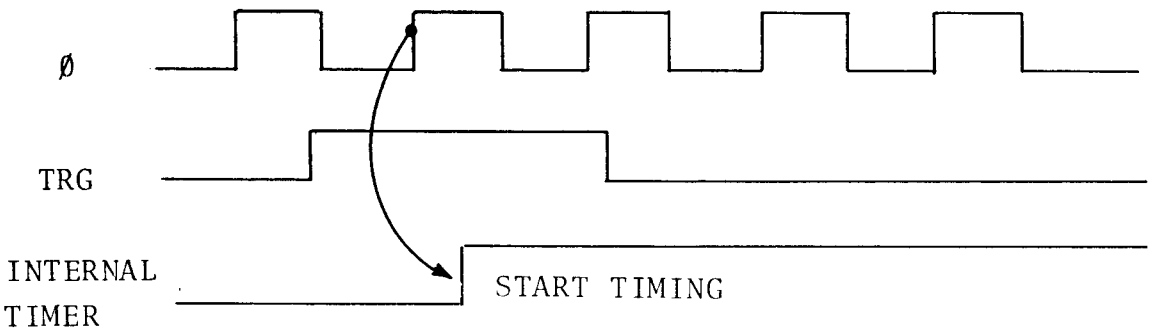


FIGURE 9 MEMORY LATCH TIMING



CTC COUNTING MODE



CTC TIMING MODE

FIGURE 10 CTC TIMING

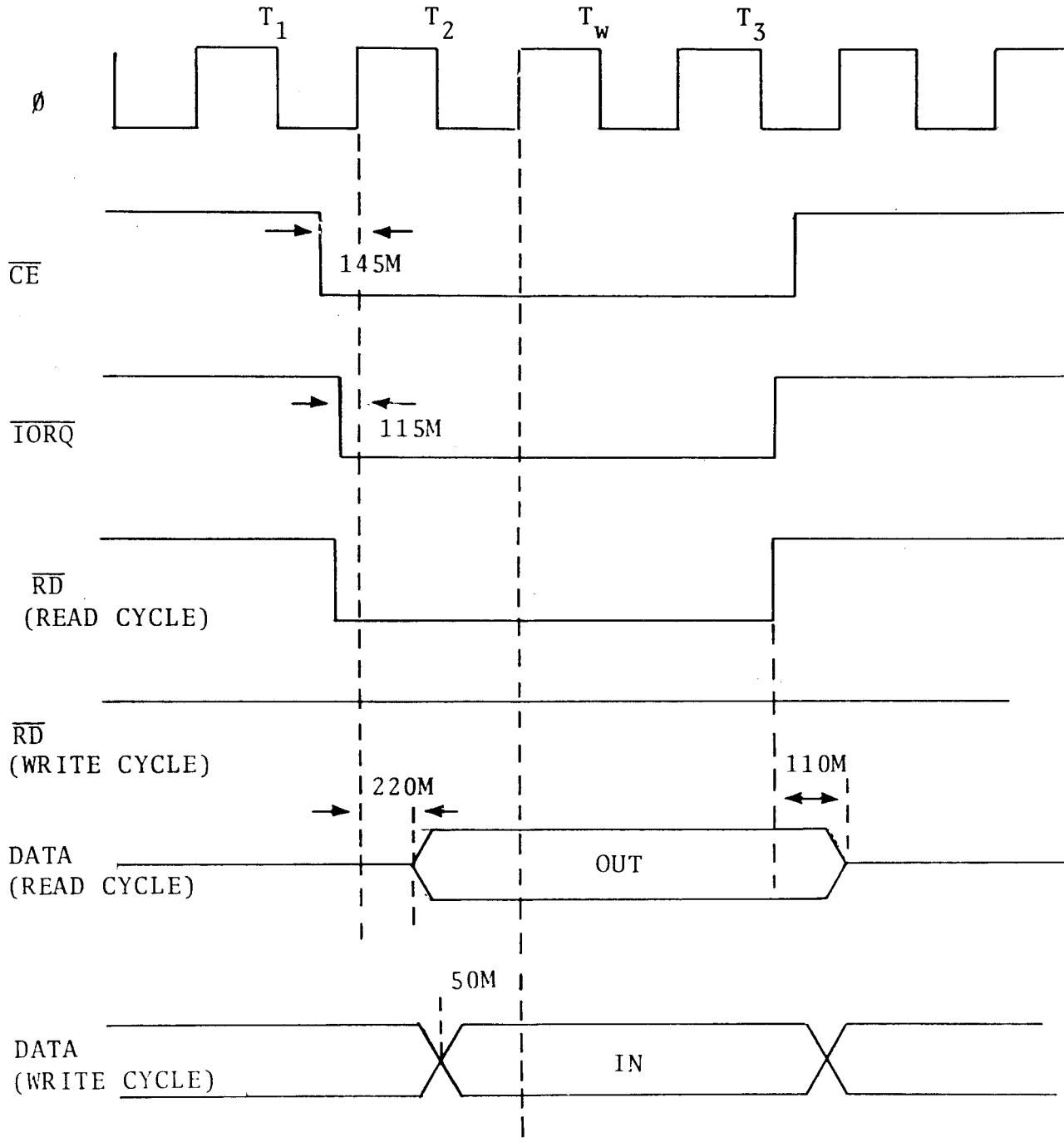


FIGURE 11 SIO READ/WRITE CYCLE

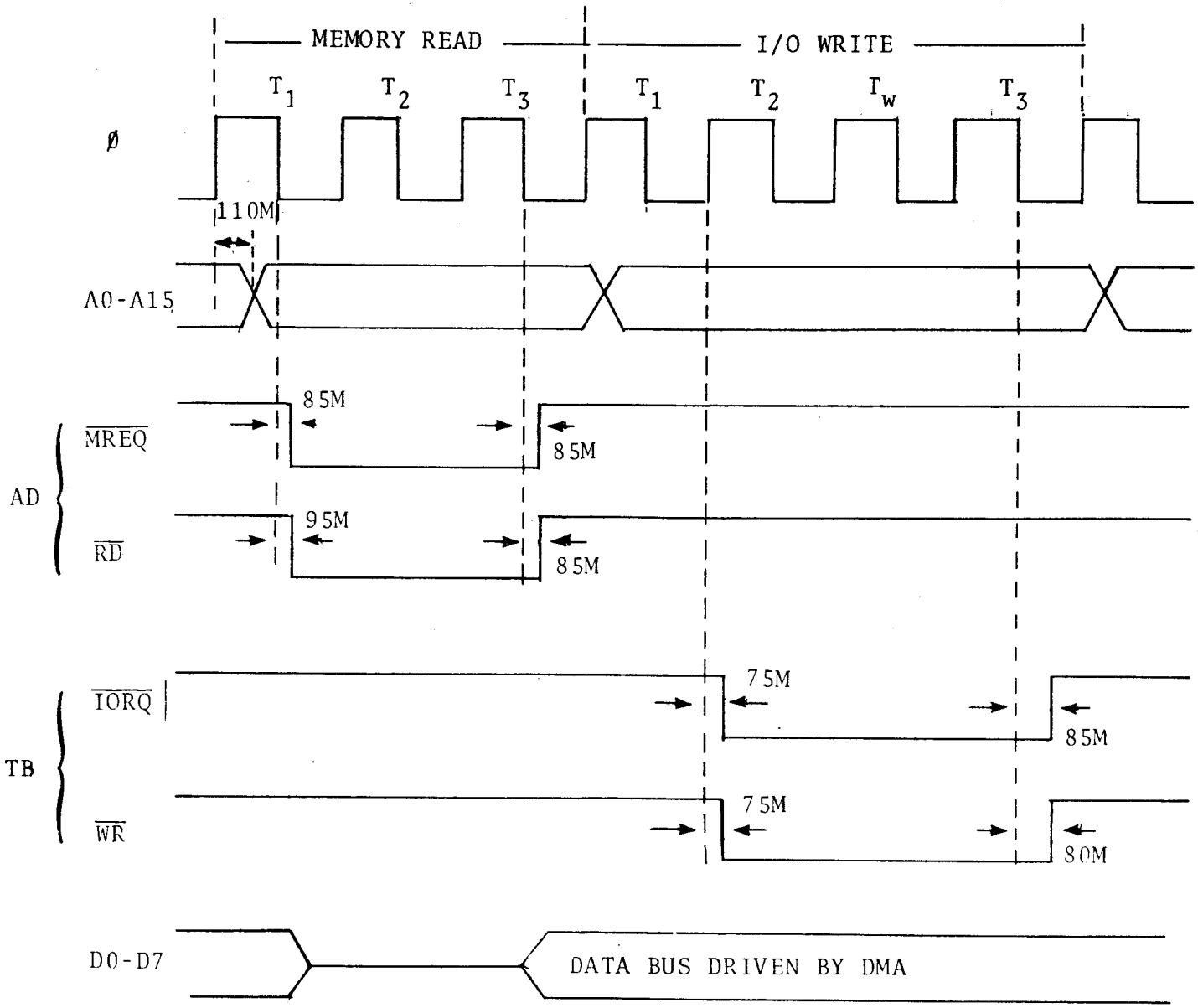


FIGURE 12 DMA MEMORY-TO- I/O TRANSFER

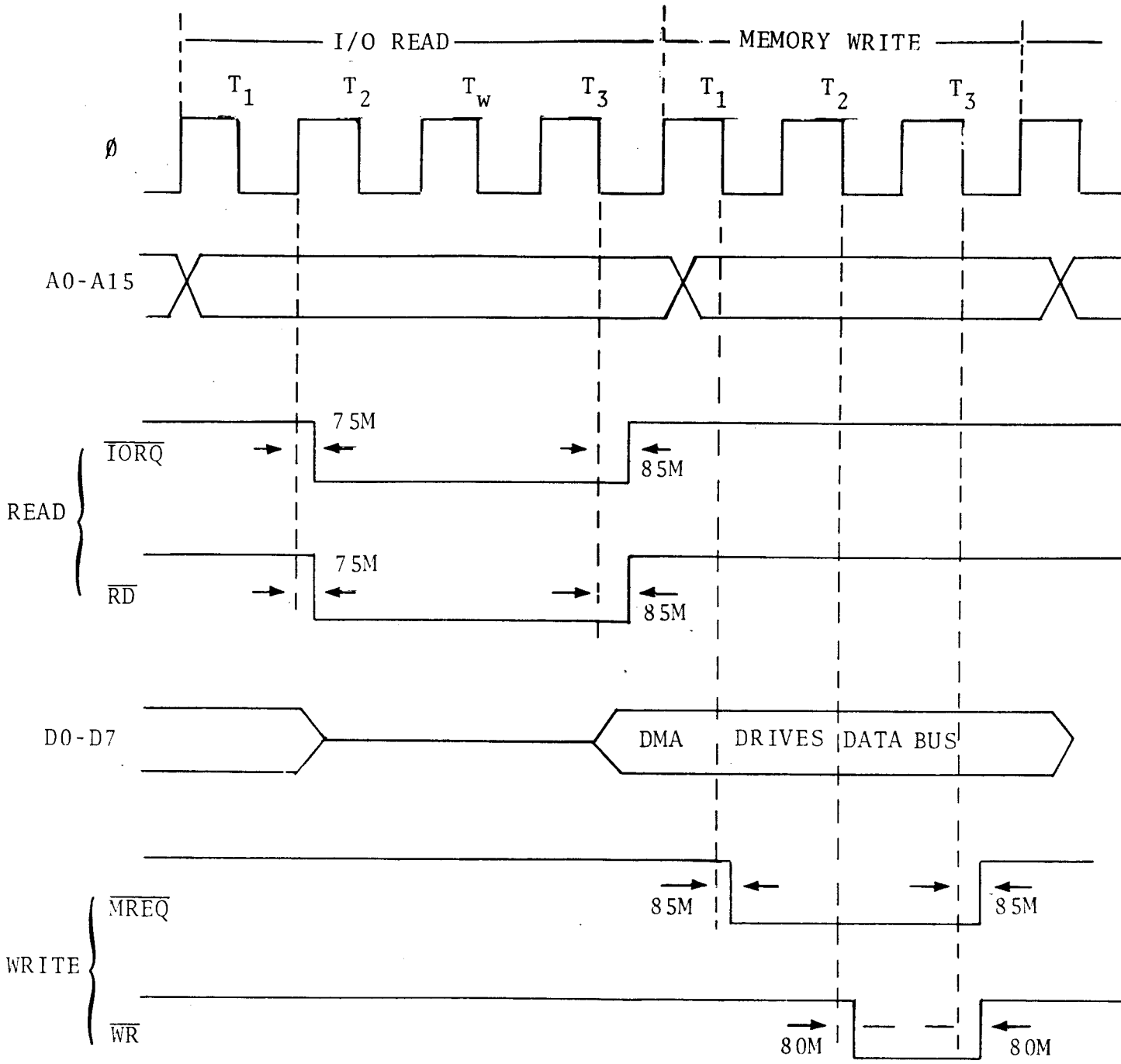


FIGURE 13 DMA I/O-TO-MEMORY TRANSFER

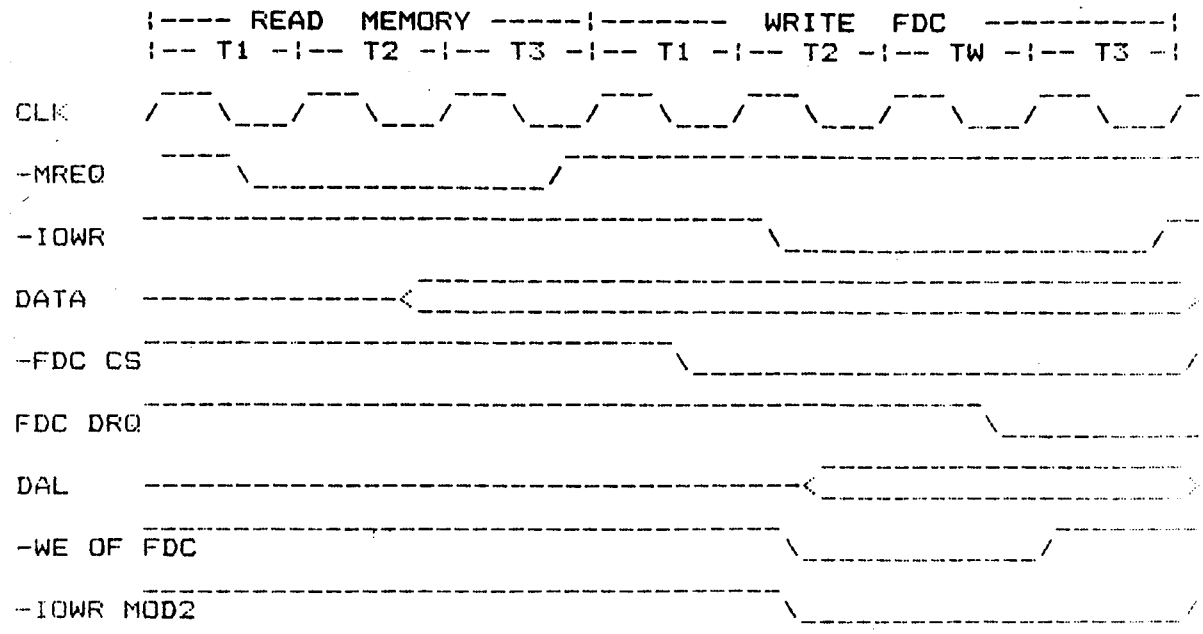


FIG. 14 TIMING DIAGRAM OF MEM. TO FDC TRANSFER (DMA WRITE OPERATION)

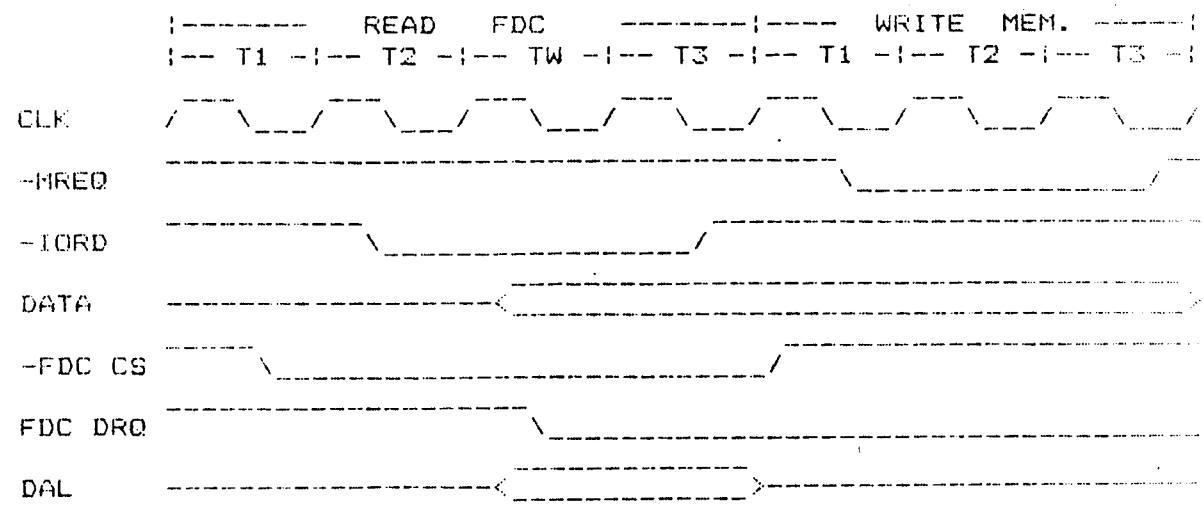


FIG. 15 TIMING DIAGRAM OF FDC TO MEM. TRANSFER (DMA READ OPERATION)

TABLE OF CONTENTS

5.0 CONNECTOR AND SWITCH DESCRIPTION

The positions of all the connectors on the logic board are shown in Figure 16.

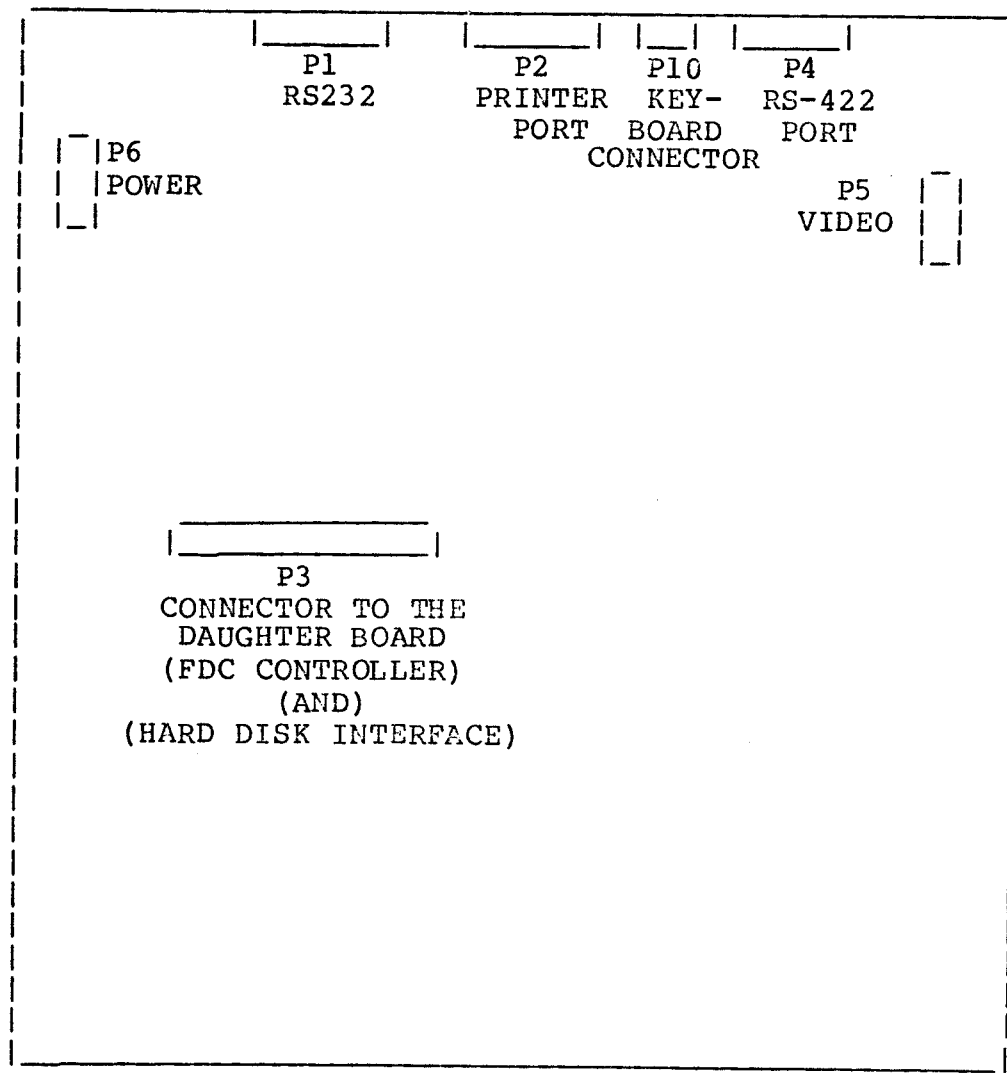


FIGURE 16 CONNECTOR POSITIONS

Table 2 shows the functions of each connector on the logic board.

CONNECTOR #	DESCRIPTION
P6	POWER CONNECTOR
P1	RS-232C MODEM PORT
P3	DAUGHTER BOARD CONNECTOR
P2	SERIAL PRINTER INTERFACE
P5	VIDEO
P4	RS-422 USER CONNECTOR
P10	KEYBOARD CONNECTOR

TABLE 2. CONNECTOR ASSIGNMENT

5.1 The following describes the pin assignment of each connector.

P6 POWER CONNECTOR

PIN #	DESCRIPTION
1	- 12 V
2	UNUSED
3	GROUND
4	+ 5 V
5	+ 12 V

P1 RS232C TERMINAL INTERFACE

PIN #	DESCRIPTION DTE INTERFACE
1	FRAME GROUND
2	TRANSMIT DATA
3	RECEIVE DATA
4	REQUEST TO SEND
5	CLEAR TO SEND
7	SIGNAL GROUND
8	DATA CARRIER DETECT
20	DATA TERMINAL READY
15	DCE SOURCE XMIT SIGNAL (OPT) (see 5.4)
17	DCE SOURCE RCV SIGNAL (OPT) (see 5.4)
24	DTE SOURCE XMIT SIGNAL (OPT) (see 5.4)

P2 SERIAL PRINTER CONNECTOR

PIN #	DESCRIPTION DCE INTERFACE
1	FRAME GROUND
2	RECEIVE DATA
3	TRANSMIT DATA
4	REQUEST TO SEND
5	CLEAR TO SEND
6	DATA SET READY
7	SIGNAL GROUND
8	DATA CARRIER DETECT
20	BUSY

FLOPPY DISK DRIVE CONNECTOR
(ON THE DAUGHTER BOARD)

PIN #	DESCRIPTION
6	DRIVE SELECT 3
8	INDEX/SECTOR
10	DRIVE SELECT 0
12	DRIVE SELECT 1
14	DRIVE SELECT 2
16	MOTOR ON
18	DIRECTION SELECT
20	STEP
22	COMPOSITE WRITE DATA
24	WRITE ENABLE
26	TRACK 0
28	WRITE PROTECTED
30	COMPOSITE READ DATA
32	SIDE SELECT

WDC CONTROLLER CONNECTOR (ON THE DAUGHTER BOARD)

PIN #	DESCRIPTION
1	WDAL 0
3	WDAL 1
5	WDAL 2
7	WDAL 3
9	WDAL 4
11	WDAL 5
13	WDAL 6
15	WDAL 7
17	WA 0
19	WA 1
21	WA 2
23	WCS
25	WWE
27	WRE
29	WWAIT
35	WINTRQ
37	WDRQ
39	WMR

P4 RS-422 USER CONNECTOR

PIN #	DESCRIPTION
1	GROUND
2	TXD +
3	RXD +
4	RTS +
5	CTS +
6	TXCK -
7	RXCK -
8	GROUND
9	TXD -
10	RXD -
11	RTS -
12	CTS -
13	TXCK +
14	RXCK +
15	TEST

5.2 Switch Settings

		(UP) OPEN	(DOWN) CLOSED	
S2 (right)	1			Printer/terminal baud rate* see Table 5.2.2
	2			Printer/terminal baud rate* see Table 5.2.2
	3			Printer/terminal baud rate* see Table 5.2.2
	4	20MEG HARD DISK	10MEG HARD DISK	~~Open TS802, closed TS800A~~
	5			Open TS802/802H/800A user station Closed TS802/802H stand alone
	6	X		TS800A and TS802 must be open Open TS802H, boot from Winchester
			X	Closed TS802H boot from floppy.
	7	X		TS802, 800A, 802H used as terminal for TS806/816
			X	TS802, 800A, 802H used as computer
	8	either		Not used
	9	either		Not used
	10	either		Not used

SWITCH	POSITION	(UP) OPEN	(DOWN) CLOSED	FUNCTION
S1 (left)	1	X		Duplex
			X	Local
	2	X		Blinking
			X	Steady cursor
	3		X	Always closed
	4		X	Always closed
	5		X	Always closed
	6	X		White characters on green

	(UP) OPEN	(DOWN) CLOSED	
		X	Green characters on white
7			See Table 5.2.1
8			See Table 5.2.1
9	X		60 Hertz (115 VAC)
		X	50 Hertz (230 VAC)
10	X		Keyclick off
		X	Keyclick on

TABLE 5.2.1

S2	7	8	FUNCTION
	CLOSED	CLOSED	HALF DUPLEX
	CLOSED	OPEN	FULL DUPLEX (must be for normal operation)
	OPEN	CLOSED	BLOCK
	OPEN	OPEN	LOCAL

TERMINAL BAUD RATE

SWITCH POSITION 1 2 3	BAUD RATE
0 0 0	19200
1 0 0	9600
0 1 0	4800
1 1 0	2400
0 0 1	1200
1 0 1	600
0 1 1	300
1 1 1	150

0 ----- SWITCH CLOSED (down)
1 ----- SWITCH OPEN (up)

5.3 Self-Diagnostics LED Informations.

LED # 1	2	3	4	HARDWARE ERROR			
*	.	.	.	MEMORY	TS-800A	TS-802	TS-802I
.	*	.	.	DMA			
.	.	*	.	CTC			
.	.	.	*	SIO #1			
*	*	.	.	SIO #2			
.	.	*	*	FDC			
*	*	*	*	WDC BOARD			

* --- LED ON
. --- LED OFF

5.4 To activate the options for the modem port (DTE) perform cust and jumps by the following chart at W34.

A..B Using pin 15 cut E & F jumper F & G
C..D Using pin 17 cut C & D jumper B & D
E..F
G.
W34 Using pin 24 connect A & C

The following is the summary of the hardware specifications.

- POWER REQUIRMENT ------ +12V, +5V, -12V
- POWER SUPPLY ------ 150 W
- POWER CONSUMPTION ------ TYPICAL 50 (BOARD ONLY)
- SYSTEM CLOCK ------ 4MHZ
- MEMORY
    - 64 K BYTES OF DYNAMIC RAM
    - 4 K BYTES OF EPROM
- RS-422 COMMUNICATION MODE
    - SDLC MODE
    - 800 K BITS/SEC
- CRT TERMINAL COMMUNICATION MODE
    - ASYNCHRONOUS MODE
    - 150,300,600,1200,2400,4800,9600,19200 BAUD
- RS-232 COMMUNICATION MODE
    - USER DEFINED COMMUNICATION MODE
    - 150,300,600,1200,2400,4800,9600,19200 BAUD
- PRINTER COMMUNICATION MODE
    - ASYNCHRONOUS MODE
- FLOPPY DISK DRIVE
    - 5 1/4 IN. MINI DRIVE
    - DOUBLE SIDE, DOUBLE DENSITY
    - 0.5 MB STORAGE PER DRIVE (UNFORMATTED)
    - 368 KB (FORMATTED)
- WINCHESTER DISK DRIVE
    - 5 1/4 IN MINI DRIVE
    - 9:5 MB STORAGE PER DRIVE (UNFORMATTED)
    - 7:4 MB (FORMATTED)

6.0 GENERAL DESCRIPTION

The floppy disk controller controls all the reading, writing and formatting functions for the two 5 1/4 floppy disk drives. Single side, double side, single density and double density are all programmable by software. The three chip controller provides all the necessary circuit including data separation and write precompensation functions.

6.1 Floppy Disk Read/Write Operation

The floppy disk controller is on a daughter board separated from the main board. They are connected by a short flat cable. The floppy disk controller used in the TS802, TS802H includes four main chips. They are the floppy disk controller and formatter WD1793-02, a data separator and write precompensation circuit WD1691, a four phase clock generator WD2143-01 and a voltage-controlled oscillator 74S124. When reading data from the floppy disk drive, raw data is separated into data and the read clock by the data separator WD1691. The floppy disk controller, WD1793-02, than converts the serial data into the parallel data to interface to the CPU. When writing data to the floppy disk drive, parallel data and the clock are combined into the serial "write data" signal and sent to the floppy drive. The floppy disk controller (WD1793-02) also controls all the floppy disk drive control signals such as the head step signal, head direction signal, track 0 signal, write protect signal, single and double density signal, write precompensation signal and so on. The WD1793-02 can be programmed to handle the seek track,

read sector, write sector, read address, read track, write track and force interrupt functions. The four phase clock generator WD2143-01 is used when write precompensation is desired (it controls the width of write-precompensation). The voltage controlled oscillator 74S124 is used to generate a center frequency (2 MHz) when reading data from the floppy disk drive.

* LATER REVISION USES THE SMC FDC9216/B FLOPPY DISK DATA SEPARATOR.

6.2 Jumper Configuration and Termination for the Floppy Disk Drives.

DRIVE A

1	2	3	4	5	6	7	8
C	C	O	O	O	O	O	O
L	L	P	P	P	P	P	P
O	O	E	E	E	E	E	E
S	S	N	N	N	N	N	N
E	E						

DRIVE B

1	2	3	4	5	6	7	8
C	O	C	O	O	O	O	O
L	P	L	P	P	P	P	P
O	E	O	E	E	E	E	E
S	N	S	N	N	N	N	N
E		E					

NOTE: Only one resistor terminator should be used and that must be on the drive at the end of the cable.

REPAIRS PRICE LIST FOR COMPUTERS

March 1, 1982

REPAIR	Price
Basic Repair Charge	$ 70.00
INDIVIDUAL REPAIR CHARGES	
Logic Board TS800, TS802, TS802H (B900019-001)	150.00
Logic Board TS801 (B900006-001)	175.00
Logic Board TS806 (B900007-001)	250.00
Logic Board TS816 (B900008-001)	350.00
Floppy Controller TS802, TS802H (B900017-001)	50.00
Winchester Disk Controller TS806 (B900010-001)	175.00
Interface Board TS816 (B900009-001)	50.00
Keyboard Repair TS800, TS802, TS802H (K030331-001)	50.00
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Video Module TS800, TS802, TS802H (BC-01643)	50.00
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8" Winchester – Disk Controller	600.00
8" Winchester – Power Amplifier	253.00
Computer Power Supply	110.00
Picture Tube Broken TS800, TS802, TS802H (T300002-002)	214.00
Picture Tube and Top Case TS800, TS802, TS802H	270.00
Top Case Broken TS800, TS802, TS802H	80.00
Bottom Case Broken TS800, TS802, TS802H	100.00
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Out of warranty
Customer to return defective replaceable module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send replacement/repaired module, billing per above price schedule plus return freight.

Prices subject to change without notice.

TeleVideo® Systems, Inc.

TeleVideo Systems, Inc., 1170 Morse Avenue, Sunnyvale, CA 94086 (408) 745-7760 (outside California – 800-538-8725, toll-free)
California: Los Angeles (714) 547-5556; Sunnyvale (408) 745-7760 · *Georgia:* Atlanta (404) 447-1231
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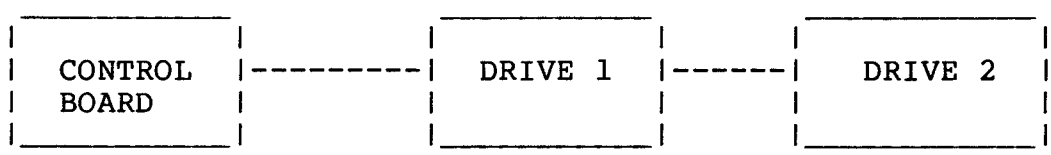
Printed in U.S.A.

EXAMPLE:



Drive 2 must have the resistor terminator.

7.0 WINCHESTER DISK CONTROLLER

7.1 Overview

The WD1000 hard disk controller is a discrete implementation of all functions required to control SA1000/ST506 compatible Winchester hard disk drives via a standard data and control BUS. The controller is fabricated using a mix of high-speed bipolar and NMOS devices contained on a single, 2-sided PC board. The design of the circuitry makes use of a high-speed Microcontroller, the 8X300, newly developed NMOS support devices, Schottky, and low power Schottky devices to achieve low component count and low cost while maintaining high performance and reliability. All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors are provided to permit direct pin-for-pin connection to ST506 compatible 5" drives. All power for the board can be supplied from a single 5 Volt power supply on a separate connector. All host to disk data transfers are buffered by an onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around 5 basic sections:

1. Processor functions
2. Serial data separation
3. Data conversion and checking
4. Serial data generation
5. Host interface functions

7.2 Processor Functions

All functions of the WD1000 controller are ultimately controlled by the onboard processor. Due to the high data rates associated with hard disk drives, processing of data and control of machine functions within the circuitry requires a processor capable of extremely fast execution speed. The processor used is the 8X300, a bipolar microcontroller particularily well suited for handling data efficiently at high rates.

The 8X300 operates at a basic clock rate of 8 MHz and performs all operations within 2 clock cycles giving it a speed of 4 MIPS (Million Instructions Per Second) or one instruction executed every 250 nS. The architecture of the processor is different from most popular microprocessors in that no common data or address BUS is provided to be shared by RAM, ROM or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data BUS. The instruction address BUS (IAO-IA13) is capable of directly accessing 8K words of program storage, however, the WD1000 uses only the first 10 address lines, limiting onboard program storage to 1K words. Program data is input to the 8X300 (U50) on the Instruction Data Operation. All BUS designations utilized by the 8X300 are reversed from the traditional LSB to MSB weighting, so that on the WD1000 these lines have all been renamed on the schematic to provide a more conventional designation system for the board.

7.2.1 Fast IO Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast IO Select" byte, is not processed by the 8X300, rather it is decoded by auxiliary hardware to provide 8 read strobes and 8 write strobes which route data to the various devices distributed along the interface vector BUS.

The Fast IO byte is latched into a 6-bit latch (U27) on the trailing edge of MCLK to ensure the data remains stable during the entire instruction. This data selects a read strobe and write strobe through two 1-of-8 decoders (U20 and U26) which are alternately enabled by the -WC control strobe produced by the 8X300. To provide edges on read strobes during sequential read operations from various ports, the red strobe decoder (U20) is always disqualified at the end of instruction by +MCLK' which is a delayed copy of +MCLK. This delay compensates for timing races through the Fast IO latch (U27) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit BUS called the "IO" BUS. This BUS is active low. It must be noted that this BUS is in no way related to the instruction data BUS and can be thought of as simply an 8-bit bidirectional IO BUS of the 8X300. In fact it has been renamed as I00-I07 to reflect this distinction.

7.2.2 Internal BUS Control

Several BUS control signals are produced by the 8X300 to identify and strobe the data in the IO BUS. WC (write control) is a signal which determines the direction of the data to and from peripherals. When WC is false (during the first half cycle) data is being input to the 8X300 from the IO BUS. When WC is true (during the second half cycle), data is being output from the 8X300 onto the IO BUS. SC (select control) is a signal which becomes active during the second half cycle instead of WC if the IO BUS contains an 8-bit IO address. In the WD1000 both WC and SC are combined by a NOR gate (U24) to indicate all accesses to any port. This arrangement allows 8-bit immediate data moves from the 8X300 to any output port within one instruction, instead of the normal 5-bit immediate moves provided for by the instructions set.

All instruction fetches occur late in the second cycle of the preceeding instruction. This time is marked by the generation of a 65 nS (nominal) active high pulse called MCLK which occurs every instruction. MCLK is also used to latch data prior to being input on the IO BUS to insure stability during reads, and to disqualify read strobes which would otherwise remain true into the second clock cycle of any instruction which does not write to a port.

Two additional BUS control signals are produced by the 8X300. They are RIGHT BANK SELECT (-RB) and LEFT BANK SELECT

(-LB), but are not used in the WD1000 due to the implementation of the Fast IO Select logic.

7.2.3 Reset Circuit

The 8X300 is held reset for approximately 40 mS after initial power on. this is accomplished by an RC network (R42, C68 and CR3) which drives a Schmitt trigger (U31) to provide a proper rise/fall time on the -RESET line of the 8X300. Alternate reset of the processor can be accomplished by dropping -MR (J5 pin 39) whenever the host wishes to reset the controller. A Schmitt trigger (U31) is provided with a 4.7K pull-up (R43) to buffer the -MR input from the host. -RESET also propagates to the drive control latches (U52 and U48) and their associated line drivers (U54-56) and host interface WAIT (U320, DRQ and INTRQ latches (U30), ensuring proper initialization of these functions during power up and subsequent resets from the host.

7.2.4 Processor Power Supply

Power is supplied to the 8X300 from the +5 Volt (Vcc) power BUS. Due to the internal operation of the 8X300 an on-chip voltage reference is provided to produce bias to an external pass transistor (Q4) which drops Vcc to the 8X300 to approximately +3.0 Volts. All signals into and out of the 8X300 are internally level shifted to be TTL compatible.

7.2.5 Read and Write Ports

Throughout the circuit, output ports are formed by D type latches using write strobes (WRO-7) to latch data into the ports. Reading of ports is universally accomplished by using read strobes (RDO, RD2, RD4-6) that enable selected tri-state output devices on the IO BUS. Additionally two read strobes are used to clock the host DRQ and INTRQ latches (U30) and one read strobe is left unused as a "dummy" port for instructions not requiring data from a port. This insures glitchless operation of the Fast IO port decoders.

7.2.6 Read/Write Memory

Since the 8X300 does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the IO BUS. RAM must, therefore, be accessed via the IO BUS by I/O instructions like all other port accesses. To provide for addressing the RAM, three latch/counters (U40, 45 and 46) are connected to the IO BUS to receive and store addresses required to access the RAM (U33 and U39).

7.2.6.1 RAM Addressing

The RAM address BUS (RAO-RA9) uniquely addresses 1 of 1024 memory locations. As each counter chip reaches a count of 0, it will set a borrow condition to the next higher counter which will be decremented at the end of the next access to RAM. When all bits of the address have been reset the -ROVF bit on the last

counter (U40) will be reset providing an overflow status which can be read by the processor on U43. By setting various beginning address values, -ROVF can be used to mark the end of any RAM access loop from 1 to 1024 bytes in length. In the WD1000 this function is used for setting sector buffer lengths of 128, 256, or 512 bytes.

7.2.6.2 Sector Buffering

All data read from the disk or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented which means that effective addresses are stable to the RAM by at least the instruction prior to the actual access. This preselection feature effectively reduces RAM access time to the output enable and propagation time of the RAM for read operations and the width of the minimum -WR strobe pulse for write operations.

7.2.6.3 RAM Accessing

RAM access is initiated by -RCS which is the logical OR (by U25) of -RDO and -WRO which are generated by the Fast IO decoders (U20 and U26). Data to be read from RAM will be placed on the IO BUS whenever - RCS is low and -WC is high. Data is written into a selected RAM cell on the trailing edge of -WC if -RCS is low. During writes, both -WC and -RCS will be low for at least 120 nS so that data setup time requirements are met.

7.2.6.4 Scratchpad Operations

Because the RAM address counters are presettable, direct reads and writes to a specific address are possible. This function is used for scratchpad storage during program execution. This mode of RAM access requires 2 or 3 instruction cycles for each random access to the RAM as opposed to 1 for sequential access using the post-decrement feature.

7.2.7 MAC Control Port

Basic control of the various functional sections of the WD1000 is accomplished by a dedicated 6-bit control port called MAC CNTRL (U34). MAC CNTRL enables the functions of the WAIT control circuitry (-WAEN), CRC generation (-CRCIZ), gating of read data into data separation circuitry (RGATE), selection of read or write functions (-WRITE), control of CRC check word output (-1BLA) and AM detection (SRCH). MAC CNTRL output states are latched into the port by a write strobe (WR7). Additionally, any time MAC CNTRL is loaded with a new byte, the lower 2 data bits (I00-1) are strobed into the upper 2 address counter/latch bits (RA8,9).

All remaining ports are distributed among the basic functional sections of the WD1000 and will be described in detail within the discussion of those functions.

7.3 Serial Data Separation

The WD1000 controller contains onboard circuitry to process incoming MFM data from the drive by a process called data separation. Here, some background information may be helpful:

> In order to provide maximum data recording density and therefore maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of data capacity, hence the term "double density".

The fact that clock bits are not recorded with every data bit cell requires circuitry that can remain in sync with data during the absence of clock bits. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bit timing when clocks are missing and synchronize to clock bits when they are present. This is accomplished by using a phase locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship to the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

TeleVideo Systems, Inc.

TERMINAL SPARE PARTS LIST

May 1, 1982

Quan. Req.	Unit Price	Total Price	Part Number	Description
				Modules
____	$ 91.00	____	BC-01642	Power Supply Module
____	93.00	____	BC-01643	Video Module w/Conn
____	105.00	____	K030330-001	Keyboard Ass'y 912B
____	126.00	____	K030330-002	Keyboard Ass'y 920B
____	105.00	____	K030330-003	Keyboard Ass'y 912C/910
____	126.00	____	K030330-004	Keyboard Ass'y 920C
____	175.00	____	K030331-001	Keyboard 950 w/Housing
____	179.00	____	T300002-001	Tube, CRT B/W
____	179.00	____	T300002-002	Tube, CRT Green
____	458.00	____	B900001-001	Logic Board 912/920
____	539.00	____	B900002-001	Logic Board 950
____	395.00	____	B900011-001	Logic Board 910
____	514.00	____	B900014-001	Logic Board 925
____	200.00	____	Y808000-006	Pattern Generator
				Manuals
____	$ 5.00	____	B300001-001	912/920 Operators Manual
____	50.00	____	B300001-002	912/920 Maintenance Manual
____	5.00	____	B300002-001	950 Operators Manual
____	50.00	____	B300002-002	950 Maintenance Manual
____	5.00	____	B300002-003	950 Customization Manual
____	5.00	____	B300005-001	910 Operators Manual
____	50.00	____	B300005-002	910/910 PLUS Maintenance Manual
____	5.00	____	B300021-001	910 PLUS Operators Manual
____	5.00	____	B300013-001	925 Operators Manual
____	50.00	____	B300013-002	925 Maintenance Manual
				Kits
____	$150.80	____	A300001-001	912/920 Minimum Logic
____	134.28	____	A300001-002	Power Supply/Video Module
____	66.03	____	A300001-003	912/920 Minimum Mechanical
____	202.25	____	A300001-004	Additional Parts
____	183.08	____	A300001-005	950 Minimum Logic
____	54.05	____	A300001-006	925/950 Minimum Mechanical
____	112.22	____	A300001-007	910 Minimum Logic
____	124.19	____	A300001-009	910 Plus Minimum Logic
____	60.23	____	A300001-010	910/910 Plus Minimum Logic
____	135.71	____	A300001-011	925 Minimum Logic
____	35.00	____	A300004-001	912/920 2nd Page Memory
____	43.74	____	A300004-002	950 2nd Page Memory
____	78.73	____	A300004-003	950 3rd/4th Page Memory
____	50.00	____	A300006-001	910/910+ Current Loop Kit
____	60.00	____	A300006-002	925 Current Loop Kit
				Capacitors
____	$ .72	____	C600100-001	Capacitor DIP MICA 10PF 100D03
____	.72	____	C600100-002	Capacitor MICA 20PF 50V
____	.72	____	C600100-004	Capacitor 100PF 50V MICA
____	.72	____	C600100-005	Capacitor 47PF 50 MICA
____	.72	____	C600100-006	Capacitor 150PF
____	.95	____	C600100-007	Capacitor 330PF MICA
____	1.07	____	C600100-008	Capacitor 390PF MICA
____	.72	____	C700100-001	Capacitor Radial Lead 22UF 15V
____	1.74	____	C700100-002	Capacitor Radial Lead .68UF 50V
____	.72	____	C700100-003	Capacitor Radial Lead 22UF 50V
____	1.08	____	C900100-011	Capacitor Radial Lead 100PF
____	2.40	____	C700100-005	Capacitor 3.3UF 50V
____	1.08	____	C700100-006	Capacitor 2.2UF 25V Electrolytic
____	2.33	____	C700100-007	Capacitor .0068UF 50V
____	2.08	____	C700100-008	Capacitor Radial Lead 4.7UF 35V 10%
____	1.98	____	C700100-009	Capacitor 10UF 25V Tantalum
____	.72	____	C700100-010	Capacitor Electrolytic 10UF 16V
____	.96	____	C700100-011	Capacitor Tantalum 4.7UF 16V
____	1.08	____	C700100-013	Capacitor 1.0UF 16V
____	.72	____	C700100-016	Capacitor Radial Lead .22UF 35V
____	.72	____	C800100-001	Capacitor Radial Lead 1UF 15V
____	.72	____	C900100-001	Capacitor Ceramic Disk .01UF+80%-20%-16V
____	$ .72	____	C900100-002	Capacitor Ceramic Disk .01UF 10% 50V-Y5P
____	.72	____	C900100-003	Capacitor Ceramic Disk 330PF 20% 50V
____	.72	____	C900100-004	Capacitor Ceramic Disk 330PF 100V
____	1.08	____	C900100-005	Capacitor 47PF 100V
____	.72	____	C900100-006	Capacitor 22PF 1K V
____	.72	____	C900100-007	Capacitor 68PF 1K V
____	.72	____	C900100-008	Capacitor .1UF 50V
____	.72	____	C900100-009	Capacitor .039UF
____	1.08	____	C900100-010	Capacitor .039UF 50V Mylar
____	.72	____	CC-50221SL	Capacitor 220PF 50V Ceramic
____	.72	____	CE-10107S	Capacitor 100UF 10V Electrolytic
____	.72	____	CE-10226SH	Capacitor 22UF100V Electrolytic
____	2.28	____	CE-10228S	Capacitor 2.2KUF10V Electrolytic
____	6.60	____	CE-16107SH	Capacitor 100UF160V Electrolytic
____	1.27	____	CE-16226SH	Capacitor 22UF160V Electrolytic
____	.72	____	CE-16227S	Capacitor 220UF16V Electrolytic
____	6.91	____	CE-35338S	Capacitor 3.3KUF35V Electrolytic
____	6.56	____	CE-35478S	Capacitor 4.7KUF16V Electrolytic
____	.72	____	CM-16475	Capacitor 4.7UF16V Electrolytic
____	.72	____	CM-20682H	Capacitor .0068UF 200V Mylar
____	.72	____	CM-50102	Capacitor .001UF 50V Mylar
____	.72	____	CM-50103	Capacitor .01UF 50V Mylar
____	.72	____	CM-50473	Capacitor .047UF 50V Mylar
____	1.44	____	CM-50474	Capacitor .47UF 50V Mylar
____	1.35	____	CM-60104H	Capacitor .1UF 600V Mylar
____	4.63	____	CN-15206S	Capacitor 20UF 25V
____	1.86	____	CO-40473H	Capacitor .047UF 400V Mylar
____	1.20	____	CT-35334	Capacitor .33UF 35V Tantalum
____	1.68	____	CT-35338S	Capacitor 470UF 35V Electrolytic
				Diodes–Transistors–Regulator
____	$ 3.96	____	R600000-001	Volt. Reg 78M05
____	34.37	____	R600004-002	Volt Reg LAS15CB 1.5/13.8
____	23.70	____	R600004-003	Volt Reg LAS1605 2A/5V
____	18.60	____	R600005-001	Volt Reg LAS16CB 2.0/13.8
____	3.60	____	S350100-000	2N2219
____	2.02	____	S350100-001	2N4401
____	2.64	____	S350100-002	2N3019
____	.97	____	S350100-003	2N2907A
____	17.04	____	S350100-004	6700 Transistor Array
____	1.80	____	S350100-005	2N5320 Power Transistor
____	4.50	____	S350100-006	2N3094/KTC 1815/2SC372
____	2.07	____	S350100-007	KTC1627A/MPSA06 75V Req.
____	2.59	____	S350100-009	2SC983/2N5551
____	22.80	____	S350100-010	2SC2233/MJE 13006
____	.72	____	S360100-000	IN914
____	.91	____	S360100-001	IN4001 Diode
____	4.20	____	S360100-002	P6KE15A Diode
____	3.00	____	S360100-003	MV55A LED
____	59.40	____	S360100-004	MV1404 Tuning Diode
____	1.20	____	S360100-005	Diode Switching IN4148
____	.72	____	SD-01251	DS135D/IN5391 Rectifier
____	.72	____	SD-01252	DS18/1DS135D Rectifier
____	1.94	____	SD-01253	DSA17C/MR500
____	1.82	____	SD-01254	RD12EB/IN759A Zener
____	6.29	____	SD-01255	DS113A/MRI-1000 Diode
____	1.00	____	SD-01257	DS-130TB/IN4004 Diode
____	.72	____	SD-01258	KDS8513A/IN920 Diode
____	35.00	____	SI-01551	LAS1512
____	35.00	____	SI-01553	LAS1812

7.3.1 Incoming Data Selection

In the WD1000, serial data is input from up to 4 radially connected drives via a quad RS422 differential receiver (U15). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to the data separation circuitry by a 4-section AND/OR/INVERT gate (U23). At this point data and clocks are still combined and appear as 50 nS (nominal) active high pulses spaced at intervals of 1, 1.5 or 2 times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U18) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

7.3.2 Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q3, U17 and associated circuitry). This oscillator uses a fundamental crystal cut to oscillate at 4 times the RCLK frequency. The 4X output is then divided by U17 to produce both a 2X clock (2XDR) which is used as a reference and a 1X clock (WCLK) which is used to produce MFM write data for the disk. The crystal (Y1) frequency is 20.000 MHz for ST506 compatible drives or 17.360 MHz for SA1000 compatible drives.

7.3.3 Clock Gating

The gating of the reference and MFM data into the data separator is dependent on the condition of the read gate (RGATE) signal and the spacing of the data on the serial stream after

RGATE is brought true. Due to the techniques which are employed to separate data from clocks, it is necessary to run the VCO at a rate twice the data clock (RCLK) rate. The VCO is therefore set to an open loop frequency of 2X RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VCO but instantaneous shifts in data due to the effects of adjacent bit cells on the disk and minor noise must be ignored. Also, the response of the VCO must be adjusted to effectively ride over missing clock bis which occur as a result of the MFM recording technique. The resultant compromise between response and reject requirements of the VCO cause the VCO to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at 1.5 or 2 times the actual RCLK time intervals.

To provide protection against this undesirable condition, the VCO is always held locked onto a stable clock running at 2 X RCLK frequency whenever the controller is not actually reading data. Furthermore, great care is taken to switch in read data to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

7.3.4 High Frequency Detector

The switching function is initiated immediately after the RGATE goes true and will only switch read data into the VCO after

16 consecutive ones or zeros (high frequency) are detected by a one-shot (U10) and counter (U12) connected directly to the raw MFM data. The one-shot is adjusted for a pulse width of 1.25 times the RCLK period. This is a 250 +/-10 nS for ST506 compatible drives and 287 +/-10 nS for SA1000 compatible drives. these adjustments of the DRUN one-shot (U10) provide tolerence of up to 1/4 RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.

Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constant, the one-shot remains retriggered. As the one-shot is triggered by data stream bits, so is the up/down counter (U12), whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered the counter counts up. When any data bit fails to reach the one-shot before its time constant is over the one-shot resets and in turn clears the counter. Only when 16 successive retriggers occur can the counter reach its terminal count. At this time, the counter overflow goes true and sets up the -DRUN latch output (U13 pin 8) low which switches read data in and reference clock out. An AND/OR/INVERT gate (U18) performs the switching. -DRUN is read through U42 by the 8X300 to determine the condition of the MFM data stream.

At this point data and clocks have finally been connected to the first stage of the data separator. The heart of the data separator is the VCO (U2 and associated circuitry) and the error amplifier and filter (U1). As previously stated, the VCO runs at a frequency twice that of the RCLK rate.

7.3.5 VCO

RCLK is produced by the VCO thru a divide-by-two counter (U8). The VCO is a discrete LC oscillator with a shunt capacitor formed by a hyper-abrupt tuning diode (CR1). The diode varies its capacitance as a function of the amount of reverse DC bias applied to its PN junction. As bias decreases the capacitance increases pulling the oscillator down in frequency and, conversely as the bias increases, the oscillator frequency rises.

The VCO performs conventionally with one interesting exception. To help the VCO lock onto the incoming signals more quickly, a provision has been made to allow an external timing signal to freeze the output of the VCO in the high state. This is accomplished by disqualifying U2 in the VCO feedback circuit and by removing bias from the transistor (Q2) which provides loop gain in the oscillator. -PHASEUP performs this function and is present just after the switch over from reference clock to MFM data is made.

The width of -PHASEUP is directly related to the difference in timing between the positive going transition of the VCO output and the positive transition of the second data/clock bit of the MFM data stream. -PHASEUP causes the output of the VCO to rise in phase with the MFM data from the drive. This eliminates the need for the VCO to perform a frequency acquisition to lock onto the data stream, but rather only adjust its phase slightly to center data/clocks within the RCLK. The phase acquisition is much faster and easier to acheive and results in vastly improved performance.

7.3.6 Error Amplifier

Control of the VCO is accomplished by the error amplifier and filter. The error amplifier is a balanced differential amplifier whose output sources or sinks current to the filter stage. The output of the error amplifier is pulse width modulated by the phase detector (U6, 7). Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these pulses producing an average increase in the voltage to the cathode of the hyper-abrupt tuning diode (CR1). this effectively increases the reverse bias on the diode which reduces its capacitance and therefore increases the VCO frequency slightly to match the phase of the incoming data. Whenever the VCO is running to fast, the error amplifier produced pump-down pulses to the filter. The diode then receives decreased reverse bias and,therefore more capacitance and lower VCO frequency.

The operating point of the tuning diode (CR1) is initially set for an open loop VCO frequency of two times RCLK by setting -OSC ADJUST and monitoring the VCO output. This adjustment places the initial bias through the bias divider (R18-20, R22 and C8-9) at approximately -2.8 V to -3.2 V. At this setting the most responsive region of the diode is being used giving higher gain in the VCO. To keep the initial bias voltage close to three volts with varying disk data rates, the VCO inductor (L1) is 3.3 UH for 5 MHz drives and 3.9 UH for 4.34 MHz drives.

The VCO is forced to match the phase of the incoming data. Once the VCO is close to the phase of the incoming data, the pump pulses will become very small or missing completely. It must be noted, however, that some slight error will always be present because, without pumps, the filter will float and the VCO will drift. The overall gain of the error amplifier and the VCO will maintain this error very small, resulting in very close tracking between the VCO ouput phase and the incoming data phase.

Previously, we said that great care is taken to insure that the VCO starts on the same phase as the incoming data. If this were not the case, the error amplifier would produce very large pumps in an attempt to pull the VCO onto frequency and phase. Due to the gain of the error amplifier and the required characteristics of the filter, the integrated pump pulses would overcompensate, causing the VCO to overshoot in its attempt to

lock-on. This action would continue in a diminishing fashion until lock on-occurred. Unfortunately, the data sync fields it was trying to acquire would be over by the time the VCO finally acquired lock-on. -PHASEUP is, therefore, extremely important to the overall ability of the data separator to function reliably.

7.3.7 Sample on Phase Detector

The circuitry which feeds the error amplifier is called the Sample on Phase Detector. This circuit consists of several D latches (U7) and a delay line (DL1). The function of the circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 50 nS in length. The windows are initiated by a leading edge of any data bit as it enters the detector. They are terminated by that same data bit, edge-delayed by a net 50 nS (60 nS in the delay line minus approximately 10 nS in propagation delays).

When both the delayed data bit and the nearest VCO edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce a pump-up condition at the error amplifier. The VCO clock edge sets its half of the detector to produce a pump-down condition. When the circuit is balanced, either both pumps are on or both pumps are off, producing no net pump-up or down.

7.3.8 Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. The manner in which this is accomplished is by using a technique called window extention. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles and then to be latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data off the sample on phase detector delay line at the 60 nS tap and inverting the VCO clock to the RCLK divider (U8). The delayed data clocks a pair of latches (U9). The 'data' latch has its D input and CLEAR connected to +RCLK and the 'clock' latch has its D input and CLEAR connected to -RCLK.

If a MFM data bit enters the latches while -RCLK is high, it will be extended as a data bit. If -RCLK is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately 1/4 the RCLK period without being lost. The output of each latch is then further extended by feeding directly into another stage of latches (U3) and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals, one consisting solely of NRZ data, and the other NRZ clocks. NRZ data and clocks are finally in a form suitable for processing by subsequent circuitry within the WD1000.

7.3.9 Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on -RCLK are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U8) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the AM detector (U14) by raising the SEARCH signal. This signal releases a latch (U13) which will remove -DHOLD from the RCLK divider (U8) on the next rising edge of a MFM data bit so that CLOCKS will be on the -RCLK phase and DATA will be on the +RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which are detected by the one-shot (U10) in the DRUN circuit. Once released, the phase of RCLK vs. data and clocks will remain stable throughout the read of an ID field or data field. Whenever SEARCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

7.4 Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X300. This processing consists

of 3 functional circuits.

1) AM detection (U14)
2) Serial to parallel conversion (U29)
3) CRC checking circuit (U19)

Each function will be discussed separately but bear in mind that many interdependencies exist.

7.4.1 AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. Furthermore, it is equally impossible to determine byte boundaries as well. This problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'A1' with a missing clock pattern of HEX 'OA'. Normally a data byte of HEX 'A1' requires a clocking pattern of HEX 'OE'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (Data or ID field) within each sector. Preceeding each AM on the disk there is always a long run of "zero" data. Zeros have a clock bit for every RCLK. When attempting to read information from the disk the WD1000 first acquires phase lock over a field of zeros. After this acquisition is acheived, the

Quan. Req.	Unit Price	Total Price	Part Number	Description
				Diodes-Transistors-Regulators
	$ 4.00		ST-01353	2SC1173/2N6121
	4.28		ST-01354	2SA473/2N6123
	4.38		ST-01361	2SC1166/2N4401
	.91		ST-10351	2SA495/2N3906
				Mechanical
	$ 1.87		1701126	Fuse Holder SN-1301
	19.87		3601536	Power Cord 3 PIN
	7.73		3801541	Speaker w/conn 8 ohm
	10.92		B510000-001	Phone Cord 925/950 Keyboard
	17.34		B510002-001	Cable RJ11 Modem
	25.08		B51003-003	912/920 Kbd Cable
	25.08		B51003-009	910 Keyboard Cable
	4.68		CRT-010138	Pivotshaft minimum 25
	5.70		CRT-010174	E-Ring minimum 25
	97.80		CRT-010267	Upper Case 910/912
	70.20		CRT-010268	Lower Case 910/912/920
	97.80		CRT-010334	Upper Case 920
	25.00		CRT-04001	Upper Kybd Case 925/950
	35.00		CRT-04002	Lower Kybd Case 925/950
	10.00		CRT-04003	Kybd Bezel 925/950
	97.80		CRT-05001	Upper Case 925/950
	70.20		CRT-05002	Lower Case 925/950
	20.00		CRT-05003	Bezel 925/950
	8.88		FC-12503A	3A 125V Fuse minimum 25
	9.00		K0303XX-001	Key Cap 1x1 minimum 25
	18.75		K0303XX-001	Key Cap 1x1¼/1x1½ minimum 25
	.72		K030301-XXX	Key Cap 1X1 Black
	1.52		K030302-XXX	Key Cap 1X1½ Black
	1.52		K030303-XXX	Key Cap 1X1½ Tan
	.72		K030304-XXX	Key Cap 1X1 Tan
	.72		K030305-XXX	Key Cap 1X1 Dark Grey
	1.52		K030306-XXX	Key Cap 1X1½ Dark Grey
	1.52		K030307-XXX	Key Cap 1X1½ Light Grey
	.72		K030308-XXX	Key Cap 1X1 Light Grey
	.72		K030309-XXX	Key Cap 1X1 Light Grey
	2.76		K030310-XXX	Key Cap "L" Light Grey
	1.52		K030311-XXX	Key Cap 1X1¼ Light Grey
	5.52		K030312-XXX	Key Cap 1X8 Dark Grey
	5.52		K030313-XXX	Key Cap 1X8 Black
	.72		K030315-XXX	1X1 Dark Grey Mat
	2.56		K030316-XXX	1X1½ Dark Grey Mat
	2.56		K030317-XXX	1X1½ Light Grey Mat
	.72		K030318-XXX	1X1 Light Grey Mat
	.72		K030319-XXX	1X1 Light Grey Mat Low Profile
	5.58		K030320-XXX	"L" Light Grey Mat
	2.44		K030321-XXX	1X1¼ Light Grey Mat
	5.94		K030322-XXX	1X8 Dark Grey Space Bar Mat
	52.44		K030400-001	912 B Key-Cap Set Blk/Tan
	56.58		K030400-002	920 B Key-Cap Set Blk/Tan
	52.44		K030401-001	912 C Key-Cap Set Gry
	56.58		K030401-002	920 C Key-Cap Set Gry
	79.29		K030402-001	925/950 Key Cap Set Gry
	1.80		K030500-001	Key Guide Equal Assy
	3.60		K030500-004	Key Guide Arm Equal Assy
	3.24		KS-123456	Keyswitches .294 X 83
	6.22		KS-123457	Keyswitches—Alpha Lock
	12.00		KS-123458	Keystopper minimum 100
	.72		M200100-002	Trans Pad Large 3005-A
	4.08		M200100-006	Dip Switch 16 Pin 8 Pos
	3.84		M200101-001	76SB07 Switch Top Adj.
	3.90		M200101-002	76SB10 Switch Top Adj.
	5.70		M200101-003	76PSB10 Switch Side Adj.
	17.88		M200101-004	Pushbutton Switch
	8.88		M200104-001	1A 250V Fuse minimum 25
	7.89		M200107-001	Power switch (SPST)
	6.92		M200108-001	Power select switch (DPDT)
	10.62		M200201-001	RS232 Conn
	$ 20.00		M200201-005	Conn. Straight 25 Pin
	4.44		M200202-001	RJ11 Female Keyboard Con.
	19.80		M200206-001	Conn Recep 'D' 15 Pin
	19.80		M200207-001	15 Pos RS422 Rec.
	12.72		M200208-002	40 Pin Unpro HD R/A
	8.10		M200208-003	Conn R/A Unpro HD 50 Pin
	3.06		M200209-002	16 Pin Unprot. Header
	7.50		M200209-004	Conn Unpro 40 Pin ST HD
	3.93		M200209-005	Conn Unpro 34 Pin ST HD
	5.16		M200209-006	Conn Unpro 20 Pin ST HD
	9.00		M200210-001	16 Pin Socket Conn
	22.14		M200210-003	34 Pin Socket Conn
	21.90		M200210-004	40 Pin Socket Conn
	27.48		M200210-005	50 Pin Socket Conn
	23.10		M200211-001	34 Contact Card Edge Conn
	16.50		M200211-002	20 Cont. Card Edge Conn
	.83		M200301-001	640359-3 18 Pin Socket
	1.10		M200301-002	640361-3 24 Pin Socket
	1.80		M200301-003	640379-3 40 Pin Socket
	.78		M200301-004	640357-3 14 Pin Socket
	1.32		M200301-005	IC Socket 28 Pins
	3.30		M200301-006	Adaptor Plug 14 Pin
	.48		M200301-007	IC Socket 16 Pin
	.72		M200301-008	IC Socket 20 Pin
	6.00		M200303-003	IC Socket Low Profile 16 Pin (Current Loop)
	1.50		M200302-001	50 Pin IC Socket
	.72		M200601-001	640388-2 Plug 2 Pin
	.72		M200601-002	640388-5 Plug 5 Pin
	4.21		M200601-004	1-87543-3 Plug 26 Pin
	.72		M200601-006	09-66-1021 Wafer R/A 2 Pin
	.96		M200601-008	Wafer 5 Pin RT Ang. Molex
	.72		M200602-001	3 Pin Wafer
	1.00		M220000-001	MTG Pad Crystal
	10.00		M400008-001	RS232 Connector Shroud 925/950
	20.00		M400008-002	RS232 Connector Shroud, Modem 925/950
	5.00		M440000-001	16 Pin Cont. Hsng.
	5.00		M440001-001	Housing Contact 16 Pos
	.72		M500001-001	Recp. Contacts
	.72		M500002-001	Keying Plug
	.72		M500003-001	Amp Mate-N-Lok Contact
	7.00		PM-123456	Fuse Holder
	10.00		M400011-001	RS232 Connector Shroud 910/912/920
	20.00		M400011-002	RS232 Connector Shroud, Modem 910/912/920
				Resistors & Potentiometers
	$ .72		R514000-001	Resistor Carbon Film 68 Ω 5% 1/4W
	.72		R514000-002	Resistor Carbon Film 270 Ω 5% 1/4W
	.72		R514000-003	Resistor Carbon Film 330 Ω 5% 1/4W
	.72		R514000-004	Resistor Carbon Film 470 Ω 5% 1/4W
	.72		R514000-005	Resistor Carbon Film 510 Ω 5% 1/4W
	.72		R514000-006	Resistor Carbon Film 1000 Ω 5% 1/4W
	.72		R514000-007	Resistor Carbon Film 1800 Ω 5% 1/4W
	.72		R514000-009	Resistor Carbon Film 3300 Ω 5% 1/4W
	.72		R514000-011	Resistor Carbon Film 4700 Ω 5% 1/4W
	.72		R514000-012	Resistor Carbon Film 180 Ω 5% 1/4W
	.72		R514000-014	Resistor Carbon Film 1M Ω 5% 1/4W
	.72		R514000-015	Resistor Carbon Film 750 Ω 5% 1/4W
	.72		R514000-016	Resistor Carbon Film 1200 Ω 5% 1/4W
	.72		R514000-017	Resistor Carbon Film 100K Ω 5% 1/4W
	.72		R514000-018	Resistor Carbon Film 51K Ω 5% 1/4W
	.72		R514000-024	Resistor Carbon Film 22 Ω 5% 1/4W
	.72		R514000-025	Resistor Carbon Film 47K Ω 5% 1/4W
	.72		R514000-026	Resistor Carbon Film 150 Ω 5% 1
	.72		R514000-027	Resistor Carbon Film 10K Ω 5% 1
	.72		R514000-028	Resistor Carbon Film 200 Ω 5% 1/4W
	.72		R514000-029	Resistor Carbon Film 33 Ω 5% 1/4W
	.72		R514000-030	Resistor Carbon Film 20 Ω 5% 1/4W
	.72		R514000-031	Resistor Carbon Film 100 Ω 1% 1/4W
	.72		R514000-032	Resistor Carbon Film 1500 Ω 1% 1/4W

processor releases the AM detector (U14) by raising the SEARCH control line (SRCH) on the MAC CNTRL port (U34). Due to the circuitry associated with the VCO to RCLK divider, the -RDAT output of the data separator (U3 pin 8) will be high and the -CLKS output (U3 pin 6) will be low. -RCLK will be the shifting clock for -RDAT and +RCLK will be the shifting clock for -CLKS. These 4 signals are routed into the AM detector.

Inside the AM detector, the -RDAT is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of -RCLK. -CLKS are shifted into a similar shift register on the falling edge of +RCLK. The output stage of the -RDAT register is dumped into an 'A1' comparator and the output stage of the -CLKS register is dumped into a 'OA' comparator. AM detection occurs when both detectors are true, thereby relationship between data and clocks is known. It is also known that data is being clocked by -RCLK so -CLKS can actually be discarded; their only purpose was in detecting AM. The -AMDET signal is used as a synchronization signal to start subsequent conversion circuitry. The -AMDET signal remains true until the processor again de-asserts the SEARCH control line.

7.4.2 Serial to Parallel Conversion

After an AM has been detected, the Serial to Parallel converter (U29) takes over. NRZ data and -RCLK are used to shift data bits into an 8-bit serial to parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is

incremented. After every eight bit of data is shifted, the counter produces an overflow pulse, marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the IO BUS using read strobe 4 (RD4) in conjunction with a tri-state buffer (U36). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial to parallel device also include -SHFTCLK and -DOUT. -SHFTCLK is actually -RCLK propagated through the device. -DOUT and -SHFTCLK are tri-stated along with BDONE, and are active only when -WRITE is high, indicating a read mode of operation. -DOUT and -SHFTCLK are routed to the CRC generator checker device.

7.4.3 CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. On the WD1000, a Cyclic Redundancy Check (CRC) is performed on all data transfers from the disk.

The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16 bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator re-computes the riginal CRC bits. After the last two bytes (containing the original recorded CRC) are read, the value in the CRC generator must always be zero. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after is has checked all bytes of the recorded data, then the controller will flag the data as erroneous and enter into a retry condition. If after attemtping to correctly read the data 16 times, the controller still cannot get correct data, the read is aborted and the host is informed that the data in the buffer is questionable.

The WS1000 uses the same device to generate and check CRC's for data being written and read on the disk. The polynomial used is:

X16+X12+X5+1 (commonly called the CRC-CCITT polynomial).

During read operations, the processor polls the condition of the DRUN circuitry. When DRUN is true, it begins to search for an address mark. Once the AM is located, the processor will start to read parallel data which has been converted from NRZ

data by the serial to parallel device. The processor will terminate this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting -CRCIZ low for at least 250 nS during the search for the AM. -CRCIZ is originated on the MAC CNTRL port (U34). Upon receiving the -CRCIZ signal, the CRC generator/checker will preset all 16 of its internal polynomial division shift registers to logic ones and arm an internal latch which will enable the checking function on the leading edge of the first non-zero data to enter the device.

It should be remembered that prior to an AM there is always a field of zeros (all data bits low) so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

Once enabled by the first non-zero data bit, the CRC device will shift succeeding data bits into a feedback shift register string with exclusive OR gates tied to the feedback nodes on the first, fifth, twelvth and sixteenth registers. As each RCLK occurs, the registers will divide the incoming data and a unique pattern of ones and zeros will appear across the registers.

When the last bit of an ID or DATA field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the exclusive OR gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16 bit wide comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U43 to see if a CRC error occurred.

After the CRC bits are processed, the data stream will contain at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers none will be flipped if a constant input of zeros is shifted into the registers. This provides a convenient latching function for the CRCOK flag which will remain true for at least 1 byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock and BDONE are supplied to the CRC device on a 3-bit minibus. During read operations, the Serial to Parallel device (U29) will be sourcing these lines because the WRITE control line from MAC CNTRL (U34) is low which enables tri-state

drivers on these lines. The Parallel to Serial device (U37) will have its tri-state drivers disabled.

7.5 Serial Data Generation

The WD1000 records data on the disk in MFM format. In order to produce the proper data format, the WD1000 uses several specialized devices to process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is essentially the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data generation section are listed below:

1) Parallel to Serial conversion (U37)
2) CRC generation (U19)
3) MFM and precompensation (U30)

7.5.1 Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the Parallel to Serial device (U37). The processor enables this conversion by lowering the -WRITE signal on MAC CNTRL (U34).

-WRITE causes the tri-state buffers present on the parallel to serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the IO bus along with the -WR4 write strobe which latches the data into the parallel port on the trailing edge of the strobe. The write strobe also resets any pending BDONE. Inside the parallel to serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transistion. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U43 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate 1/8 that of the bit rate of the NRZ data stream. For ST506 compatible drives the byte timing is 1.6 us and for SA1000 drives it is 1.84 us.

The output of the last register in the shift string is brought out of the device as a NRZ serial data stream. The shifting clock is also brought out as SHFCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

7.5.2 CRC Generation

The CRC generator/checker (U19) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing -CRCIZ for approximately 250 nS while the parallel to serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero data bit enters the device. The first non-zero bit will be the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it will store a HEX A1 in the parallel to serial device. At the proper time (in sync with BDONE) the parallel to serial device will begin to send the MSB of the AM to the CRC device. This will start the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel to serial device, it will drop the -1BLA (1 Byte Look-

ahead) signal on MAC CNTRL port (U34). This signal will cause the CRC generator to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last date (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. -1BLA is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving -1BLA low for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device.

7.5.3 MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precomp device. This device accepts NRZ data and a complimentary WCLK and produces MFM data and clocks by sending the data through circuitry which decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1) If the current data cell contains a data bit then no clock bit will be generated.

2) If the previous data cell contained a data bit then no clock bit will be generated.

3) If the previous data cell and the present data cell are vacant then produce a clock bit in the current clock cell.

The terms "data cell" and "clock cell" are defined by the state of the WCLK. While WCLk is low it is a data cell and while high it is a clock cell. It can be seen then, that both clock and the data cells are 1/2 the period of WCLK or 100 nS for ST506 compatible drives and 115 nS for SA1000 drives. Also note that by the rules stated above, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be 1, 1.5, or 2 times the WCLK period only. The rules are implemented within the device by shift registers that hold the next two last and present data bits and combinatorial logic. The state of WCLK is considered and the appropriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so it is run through a re-timing latch (U21) to clean it up.

7.5.3.1 Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit a increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as 'dynamic bit shift'.

Quan. Req.	Unit Price	Total Price	Part Number	Description
				Resistors & Potentiometers
	$ .72		R514000-033	Resistor Carbon Film 3920 Ω 1% ¼W
	.72		R514000-034	Resistor Carbon Film 511 Ω 1% ¼W
	.72		R514000-035	Resistor Carbon Film 8250 Ω 1% ¼W
	.72		R514000-036	Resistor Carbon Film 1300 Ω 1% ¼W
	.72		R514000-037	Resistor Carbon Film 51 Ω 5% ¼W
	.72		R514000-038	Resistor Carbon Film 22K Ω 5% ¼W
	.72		R514000-039	Resistor Carbon Film 240 Ω 5% ¼W
	.72		R514000-041	Resistor Carbon Film 2000 Ω 5% ¼W
	.72		R514000-042	Resistor Carbon Film 680 Ω 5% ¼W
	.72		R514000-043	Resistor Cnrbon Film 27K Ω 5% ¼W
	.72		R514000-044	Resistor Carbon Film 560 Ω 5% ¼W
	.72		R514000-045	Resistor Carbon Film 47 Ω 5% ¼W
	.72		R514000-046	Resistor Carbon Film 56 Ω 5% ¼W
	.72		R514000-048	Resistor, Carbon Film 27K Ω 5% ¼W
	.72		R514000-049	Resistor, Carbon Film 90 Ω 5% ¼W
	.72		R514000-050	Resistor, Carbon Film 2.2K Ω 5% ¼W
	.72		R514000-051	Resistor, Carbon Film 3.9K Ω 5% ¼W
	.72		R514000-052	Resistor, Carbon Film 6.8K Ω 5% ¼W
	.72		R514000-053	Resistor, Carbon Film 30K Ω 5% ¼W
	.72		R514000-054	Resistor, Carbon Film 56K Ω 5% ¼W
	1.58		R514000-100	Res Pack 1K Ω Sip
	1.73		R514000-101	Resistor Pack 6.2K Ω
	2.04		R514000-103	Res Pack 10K Ω 8 Pin
	1.20		R514000-104	Res Pack 4.7K Ω Sip
	2.34		R514000-105	Res Pack 68 Ω Dip
	2.64		R514000-106	Res Pack 33 Ω Dip
	2.58		R514000-107	Res Pack 220 Ω Sip
	2.88		R514000-108	Res Pack 330 Ω Sip
	4.20		R514000-109	Res Pack 220/330 Sip
	1.80		R514000-110	Res Pack 150 Ω Sip
	3.00		R514000-111	Res Pack 1K Ω Sip
	5.46		R514000-112	Res Pack 4.7 Ω Sip
	6.60		R514001-000	Trim Pot 5K Ω 3299
	6.60		R514001-001	Trim Pot 50K Ω 3229
	6.60		R514001-002	Trim Pot 100K Ω 3299
	6.00		R514001-003	200 Ω Pot
	6.60		R514001-004	2K Ω Pot
	6.60		R514001-005	10K Ω Pot
	.72		R514003-000	Resistor, Carbon Film 510 Ω 5% ½ W
	.72		R514003-001	Resistor, Carbon Film 220 Ω 5% ½ W
	.72		R514003-002	Resistor, Carbon Film 390 Ω 5% ½W
	.72		R514003-003	Resistor, Carbon Film 820 Ω 5% ½W
	.72		R514003-004	Resistor, Carbon Film 1.5K Ω 5% ½W
	.72		R514003-005	Resistor, Carbon Film 10K Ω 5% ½W
	.72		R514003-006	Resistor, Carbon Film 2.2M Ω 5% ½W
	.72		RC02608J	Res,WW, 0.6 Ω, 2W
	1.06		RF-07104B	Brightness & Vertical Heighth
	1.06		RF-07202B	Vertical Linearity
	1.00		RF-07473B	Video B+ Adjust Pot
	3.86		RV-24205B	Focus
	2.77		RV-24501B	Contrast
				Miscellaneous
	$ 1.44		3312453	Thermister, SDT-100
	2.04		C900100-012	Spark Gap 1KV
	5.24		IC-01462	Linearity Coil (LC-36)
	1.20		IC-01464	Induc. Coil (27UH/.3Pie)
	129.24		IC-01465	Power Trans. w/Con CRT858
	4.08		IC-01466	H. Drive Trans. HDT-19
	55.48		IC-01467	F.B.T./KFS-00093
	31.63		IS-01461	Def. Yoke w/Con KYS-00060
	27.00		I740010-090	IC OSC 16MHz
	11.11		M200401-001	HC18/U-23.814 MHz
	7.85		M200401-002	Crystal 5.7143 MHz
	8.16		M200401-003	Crystal 1.8432 MHz
	4.80		M200401-004	8.000 MHz Crystal
	4.80		M200401-005	20.000 MHz Crystal
	8.70		M200401-006	Crystal 13.608 MHz

Quan. Req.	Unit Price	Total Price	Part Number	Description
				ROMS
	$22.50		I740011-013	KYBD ENCODER A1
	22.50		I740011-020	KYBD ENCODER A1 } 910
	18.90		I800000-015	SYSTEM ROM A45 }
	21.00		I800000-019	KYBD EPROM A2
	34.86		I800000-040	SYSTEM EPROM A45 — 910 Plus
	25.80		I740010-049	SYSTEM ROM A49 B1 }
	25.80		I740010-050	SYSTEM ROM A49 C1 } 912/920
	14.94		I740010-053	CHAR GEN ROM A3-2 }
	37.50		I800000-031	SYSTEM EPROM A50 } 925
	37.50		I800000-033	SYSTEM EPROM A49 }
	18.90		I800000-001	SYSTEM ROM A41
	18.90		I800000-002	CHAR GEN ROM A33
	18.90		I800000-003	CHAR GEN ROM A32
	18.90		I800000-007	SYSTEM ROM A42 } 9
	37.50		I800000-009	8048 KYBD PRO ROM U6
	125.00		I800000-049A	WORDSTAR EMULATION (3 pc.)
	18.90		I800000-016	CHAR GEN ROM } 910/910 + A48
				} 925 A31
				I.C.'s
	$ 2.20		I740010-000	IC 74 S 00
	1.72		I740010-001	IC 74 LS 00
	1.72		I740010-002	IC 74 LS 03
	2.41		I740010-003	IC 74 S 04
	1.80		I740010-004	IC 74 LS 04
	1.80		I740010-005	IC 74 LS 05
	1.80		I740010-006	IC 74 LS 08
	1.80		I740010-007	IC 74 LS 10
	1.72		I740010-008	IC 74 LS 20
	1.86		I740010-009	IC 74 LS 32
	2.55		I740010-010	IC 74 LS 42
	1.80		I740010-011	IC 74 LS 51
	3.58		I740010-012	IC 74 S 74
	1.80		I740010-013	IC 74 LS 74
	2.07		I740010-014	IC 74 LS 86
	2.00		I740010-015	IC 74 LS 109
	3.18		I740010-016	IC 74 LS 139
	2.76		I740010-017	IC 74 LS 157
	4.56		I740010-018	IC 74 LS 163 (TI)
	5.04		I740010-019	IC 74 LS 166
	4.14		I740010-020	IC 74 LS 173
	3.18		I740010-021	IC 74 LS 174
	3.24		I740010-022	IC 74 LS 253
	2.76		I740010-023	IC 74 LS 367
	3.48		I740010-024	IC 74 LS 373
	3.48		I740010-025	IC 74 LS 374
	4.14		I740010-026	IC 75 188N
	4.14		I740010-027	IC 75 189AN
	4.48		I740010-029	IC TIL117(4N37)
	2.58		I740010-031	IC NE555
	17.59		I740010-032	IC DP8304
	13.32		I740010-033	IC AMD2111-4A
	15.52		I740010-034	IC 2502HP,AY-5-1013A
	81.76		I740010-035	IC 5027P,5037,TMS9927
	41.05		I740010-036	IC P8035
	3.45		I740010-051	H11G3
	2.05		I740010-054	IC 7406
	4.32		I740010-055	IC 4N38
	37.08		I740010-056	IC K1114A
	1.92		I740010-057	IC 7414
	9.75		I740010-059	IC 2114-ICB Static RAM
	5.76		I740010-061	IC N8T245N (74LS245)
	2.70		I740010-063	IC 74LS191
	1.56		I740010-067	IC 74LS365
	3.48		I740010-068	IC 74LS273
	8.82		I740010-069	IC 74 S240
	1.74		I740010-070	IC 74LS175
	1.56		I740010-072	IC 74S133
	8.22		I740010-073	IC74S124 (74S629)

Dynamic bit shift comes about as the result of one bit on the disk (a flux reversal) influencing an ajacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. In any event, there is a method which can be applied to reduce the effect of this shift on the data called "write precompensation".

Precompensation is a way of predicting which direction a particular bit will be shifted and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last and the present bits to be written and producing three signals depending on what these bits are. The three signals are EARLY, LATE and NOMINAL. They are used in conjunction with a delay line to cause the leading edge of a data/clock bit to be written early, late or on time. As with MFMW, these signals are subject to decoding slivers and must be retimed by U21.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from the MAC CNTRL port (U34). When RWC is high, precomp is in effect. When RWC is low, no precomp is generated and the NOM output of the device is held true.

The delay line actually performs the precomp with the help of an AND/OR/INVERT gate (U22). MFMW pulses are applied to the input of the delay line and depending on which of the three precomp signals is present the AND/OR/INVERT gate selects a different tap on the delay line. Nominal data is actually tapped from the second tap, early data from the first and late data from the third. From the AND/OR/INVERT gate the MFMW data is sent to the input of an RS422 driver (U16) where it is converted to a differential form and then is sent to the drive. The AND/OR/INVERT gate has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal will be low. This is inverted by U38 and applied to the AND/OR/INVERT gate's fourth section. This resulting high input effectively inhibits the gate from accepting MFMW data.

7.6 Host Interface

All data transfers between the host and the WD1000 take place over an eight bit bi-directional bus (J5) consisting of eight Data Access Lines (DALO-7). The source or destination register inside the WD1000 is selected by the three address lines (A0-2). All accesses to the WD1000 are controlled by Card Select (CS-), Read enable (RE-) or Write Enable (WE-). since the access time for any particular read or write operation will vary, the WD1000 provides a not ready signal (WAIT-). For systems using interrupts and/or DMA, the WD1000 provides INTerrupt reQuest (INTRQ) and Data ReQuest (DRQ).

Accessing the WD1000 is essentially like accessing variable speed RAM. The host must provide a valid address in A0-2 along with a CS-. Immediately or after a short set up time, the host may assert RE- or WE-. If access time on the WD1000 will be over 100 nS, then WAIT- will be asserted. The host must keep all address lines and strobes stable while WAIT- is true. When the WD1000 de-asserts WAIT-, the data has been accepted on a write or the data is on the DAL bus on a read.

7.6.1 Wait Enable

Since most of the registers in the WD1000 are not implemented in hardware, it takes the 8X300 a finite amount of time to actually fetch the requested data on a read or store data on a write. This time varies depending on the amount of processing the 8X300 must do to access the desired register. After the data has been written or read, the WD1000 de-asserts the WAIT- line, allowing the host to terminate the current bus cycle.

The generation of the WAIT- signal is controlled by a bit in the MAC latch (U34) called WAit ENable (WAEN- will be asserted. On each bus access, the host must drop the Card Select (CS-) line on J5. The leading edge of CS- clocks the wait control latch (U32), transferring the WAEN- state through the latch, qualifying the wait drivers (U44, 54). This clocking action is required to insure that WAIT- will not be asserted in the moddle of any bus access already in progress. After the wait latch has been

clocked, CS- [BIC or BOC in some installations] causes WAIT- to be asserted to the host.

The WAIT- line is released on the trailing edge of any read or write strobe to the communications latch (U49). This release is caused by the logical OR of RD6- and WR6- on U25 which presets the wait latch (U32) to a non-wait request condition. The WAIT- signal is stretched to the trailing edge of the RD6- or WR6- by U2.

If WAEN- is de-asserted, the WD1000 generates no waits at all. In this case, the host will read the dummy status written to the communications latch by the 8X300. This feature is used by the microcode to simulate a busy condition when the host reads the status register in non-interrupt driven systems. When the WD1000 becomes un-busy, the WAEN- line will be asserted and operations on the host interface bus will be monitored once again.

7.6.2 Bus Gating

During all accesses by the host, one of two signals will be produced to gate the bus. During read operations, CS- and RE- are ANDed, producing Bus Output Control (BOC-). This signal gates the contents of the communication latch (U49) onto the DAL bus. during write operations, CS- and WE- produce Bus Input Control (BIC). This signal latches the state of the DAL lines into an internal R/S latch.

7.6.3 Register Selection

The combination of a host read or write operation along with the WREQ- signal being asserted, causes a signal, Card Select ACcess (CSAC), to be generated. The 8X300 samples this signal at U43 every 250 nS, and if asserted, reads the status of A0-2 and WE- (U43). The state of A0-2 and WE- determines which register is to be accessed (A0-2) and in what direction that access will take place.

7.6.4 Interrupts and DRQs

The WD1000 produces INTerrupt ReQuests (INTRQ) to signal the end of all disk operations and Data ReQuests (DRQ) to signal data ready to DMA controllers. INTRQ and DRQ originate on the MFM generator (U30) as an auxillary function of the chip. The WD1000 sets INTRQ using INTCLK- and sets DRQ Using DRQCLK-, both of which are produced by U20. Interrupts are cleared by HSAC- (Host Select ACcess) and A0, 1 when the host reads the Status register, issued a command, or accesses the Sector Number register. DRQs are cleared when the host accesses the Data or cylinder Low registers. DRQs will be re-issued for each byte to be transferred. HSAC- is a 200 nS version of the CSAC- signal. during Power On Reset of Master Reset (MR-), INTRQ is set and DRQ is reset.

7.7 Maintenance and Adjustments

The WD1000 requires no scheduled preventative maintenance. There are a few adjustments associated with the data separation circuitry that may need to be adjusted if a drive with a different data rate is installed. Remember, the inductor L1 must be the proper value for the data rate being used and Y1 must be selected for a fundamental frequency of four times the data rate.

7.7.1 VCO Adjustments

Data separation circuitry on the WD1000 uses a voltage controlled oscillator (VCO) which phaselocks onto incoming data and provides a clock suitable for separating data and clock bits on an MFM encoded data stream. The VCO must be adjusted using the following procedures.

Ground the cathode of the tuning diode (CR1) to the closest accessable ground using a low inductance shorting cable. This cable should consist of the shortest piece of wire possible to make the connection.

Connect a frequency counter to the VCO buffered output on TP9.

Apply power to the board. Ensure a logic "1" exists at TP17. A logic "0" on TP17 will inhibit the VCO and make adjustments impossible. If a logic "1" is not present, verify

that the DRUN circuitry (U10-U13) is functioning and adjusted properly. Refer to Section 9.3 for adjustments to DRUN.

Vary the OSC ADJ pot (R22) to verify the range of adjustment values listed in the following table are obtainable. After the range has been verified, adjust R22 to the final setting listed in the table.

Y1 Frequency	Identity	Range	Final Setting
20.000 MHz	L1 = 3.3 uh	9.0-11.0 MHz	10.0 MHz +/-1 KHz
17.360 MHz	L1 = 3.9 uh	7.5-9.5 MHz	8.68 MHz +/-1 KHz

Turn off power to the board. Disconnect all test jumpers and test equipment.

7.7.2 Error Amplifier Adjustments (Static)

The phase detection technique used to correct the frequency and phase of the VCO employs a balanced sample and hold error amplifier. To ensure reliable operation of the data separator, the error amplifier must be properly balanced. The balance adjustment must be made using the following procedures.

Apply power to the board. Ground TP20 or U8 pin 6 to turn off the right half of the error amplifier (U1). In this state current will only flow in the left half of the amplifier.

Connect a 100 ohm resistor between U1 pin 8 and ground.

Adjust the BAL pot (R1) until a reading of 0 V +/- 20 mV is observed on TP5.

Remove the ground from TP20. Install a ground to the PUP1 signal line accessable on U7 pin 1.

Verify a reading of 0 V +/- 50 mV on TP6. This indicates that the side to side balance of the error amplifier is within tolerance.

Re-adjust R1 until the reading at TP5 is 0 V +/- 20 mV.

Turn off power to the board. disconnect all jumpers and test equipment.

7.7.3 Error Amplifier Adjustments (Dynamic)

After static balance adjustments are performed, the error amplifier should be adjusted for balanced dynamic operation.

This adjustment requires that the controller be constantly reading data on the innermost cylinder of a formatted drive. While reading data, monitor TP9 (-OSC) with a frequency counter and adjust the error amplifier balance pot (R2) until the most

stable display reading is obtained. This indicates that the VCO is being locked on every attempt to read data.

Turn off power to the board. Disconnect all test equipment.

7.7.4 DRUN Adjustments

To facilitate the process of aquiring phase lock on data being read from a disk, a hardware detector is utilized to indicate when the read/write head of the drive is over a recorded field of all ones or all zeros. The detector depends on the timing of a one-shot (U10) which is adjustable by the DRUN pot (R26). R26 must be adjusted according to the following procedures:

The DRUN adjustment is made with the WD1000 in an operating test configuration with a host, drive and power source. Once the proper setup is made, apply power to the WD1000 and all test equipment.

Monitor TP14 (-DRUN) with a 10X oscilloscope probe while attempting to read a sector of data from the drive. The scope should be set to trigger on a high to low transition. While observing TP14, adjust R26. The period of the DRUN single shot should be adjusted to 1.25 times the period of RCLK.

Turn off power to the WD1000. Disconnect all test equipment.

8.0 TERMINAL PORTION OPERATION

CPU, Timing and Control

(Refer to Figure 1) The 23.814 Mhz oscillator (Osc 1) is used to generate all timing for the terminal. It is used directly as the dot clock (Shift Clock), divided by 13 to drive the UARTs, and divided by 14 (1.701 Mhz) to drive the CRT controller (CCLK) and the CPU (via the clock stretch circuit).

The clock stretch circuit is capable, upon command, of generating clock periods twice the normal length (588 ns versus 1175 ns) for accessing slow memory or peripheral devices. Its output drives the I_0 input of the 6502 CPU. The CPU then outputs I_2, which controls the timing of the CPU bus. I_2 is a slightly delayed version of I_0.

The result of these circuits are I_2 and CCLK, two signals of identical frequency but opposite phase, (except during clock stretched cycles). The importance of this will be made clear later in our discussion of the display controller.

The CPU fetches its program from the ROMs (Read Only Memory) A41-43. It uses the 6522 (A54) to sense switches S1 and S2 and to generate control signals for the rest of the terminal.

Display Controller

(Refer to Figure 2) Timer T2, part of the 6522, and the 6545 (A55) are used to generate the memory address, in Display RAM, of each character as it is about to be displayed, and the horizontal and vertical synchronization pulses necessary to control the deflection circuits of the monitor.

Timer T2 is used to count horizontal scan lines and interrupt the processor (via NMI) when a specified number of scans has occurred. The processor then loads the memory address of the next data row into the CRT Controller and "sets" this address by generating a carefully-timed reset to the 6545.

At this same time the processor loads a 4 bit value into latch, A61. At the time of the CRT reset this value is transferred to counter A60 and becomes the Row Address of the next data row. This value is then incremented by each horizontal sync pulse until the start of the next data row when it is again preset to a value determined by the CPU.

The CPU and the display controller share access to the System and Display RAM (Random Access Memory). This is done during alternate phases of the I_2 clock. During the positive portion of I_2 the CPU address may be gated onto the RAM address bus by Multiplexers A43-46, and bidirectional transceiver A14 is enabled to pass data between the CPU data bus and the RAM data bus.

Quan. Req.	Unit Price	Total Price	Part Number	Description	Quan. Req.	Unit Price	Total Price	Part Number	Description
				I.C.'s					**I.C.'s**
____	1.80	____	I740010-074	IC 74S32	____	$ 2.16	____	I740010-108	74LS193
____	3.90	____	I740010-075	IC 7416	____	27.06	____	I740010-109	Bipolar PROM 74S472 512x8
____	1.14	____	I740010-076	IC 74LS11	____	5.76	____	I740010-110	96S02
____	27.90	____	I740010-077	IC WD2143L-01	____	1.44	____	I740010-111	74S11
____	41.46	____	I740010-078	IC WD 1691	____	43.74	____	I740011-000	IC 6116 Static RAM 150ns
____	144.00	____	I740010-079	IC FD1793-02	____	28.94	____	I740011-002	IC 6502A Microprocessor
____	6.60	____	I740010-080	IC 93S16PC	____	66.24	____	I740011-003	IC 6545
____	1.68	____	I740010-081	IC 74LS138	____	28.80	____	I740011-004	IC 6551 UART
____	1.14	____	I740010-084	IC 74LS02	____	27.21	____	I740011-005	IC 6522A VIA
____	3.54	____	I740010-086	IC 74LS241	____	18.00	____	I740011-006	IC Z 80 A-P10
____	7.92	____	I740010-088	IC AM26LS31	____	58.00	____	I740011-007	IC Z80A S10/2
____	7.92	____	I740010-089	IC AM26LS32	____	16.80	____	I740011-008	IC Z80A CTC
____	7.50	____	I740010-092	8 Bit I/O Port 8212	____	21.18	____	I740011-009	IC Z80A CPU
____	1.62	____	I740010-093	74LS257	____	56.76	____	I740011-010	IC Z80 DMA
____	1.38	____	I740010-094	7438	____	83.76	____	I740011-012	IC 64K Dynamic RAM
____	2.22	____	I740010-095	74LS123	____	22.50	____	I740011-013	AY-5-3600 KEYBD Encoder (910)
____	3.54	____	I740010-096	74LS240	____	31.50	____	I740011-017	IC 68B045 2MHz
____	5.52	____	I740010-097	74LS244	____	24.00	____	I740011-019	IC SY6551-A-1 2 MHz
____	3.96	____	I740010-099	74S174	____	50.10	____	I740011-018	6545A-1 CRTC
____	3.00	____	I740010-100	74S138	____	39.60	____	I740012-001	Parallel Converter
____	1.98	____	I740010-101	74S86	____	39.60	____	I740012-002	MFM Converter
____	1.56	____	I740010-102	74S64	____	39.60	____	I740012-003	AM Detector
____	1.14	____	I740010-103	74LS54	____	39.60	____	I740012-004	CRC Generator/Checker
____	1.56	____	I740010-104	74S51	____	39.60	____	I740012-005	Parallel/Serial Converter
____	1.44	____	I740010-105	74LS14	____	18.60	____	I740012-006	Delay Line
____	1.29	____	I740010-106	IC 7402					
	24.60	____	I740010-107	Digital Delay Line					

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During the negative portion of I_2 the 6545 address bus is gated onto the RAM address bus allowing the video data to be latched by A24 and held for the display generator.

This alternating access or "interleaved" access allows the processor to operate at normal speed, without waits of any kind, yet prevents degradation of the display quality that could be caused by inadvertant appropriation of the display bus by the processor to access data.

The only penalty for this scheme is the necessity for fast RAM (150 ns or faster).

Video Generation

(Refer to Figure 3) This Display Data and the Row Address (or scan address) are used to obtain the dots for the next character to be displayed from the character generator ROMs A32 and A33.

These dots are then fed in parallel to shift registers A22 and A23 and emerge serially as raw video.

Additionally, bits 0-3 of Display data and bit 7 of A33 are combined to generate the attribute signals Underline, Blink, Blank, and Reverse. ICs A19, 20, 21 and 30 latch and delay the decoded attributes from the previous data row for carry-over into the next.

Bit 6 of A33 controls the intensity of the character to be displayed.

Gates A1, 2, 10 and 11 are used to modify the raw video to the proper intensity and polarity, and gate it on or off in response to the attribute signals and control signals BOW (used to reverse the entire display), cursor, BLI-RATE (used to blink the video) and FORCE BLANK (used to blank the entire screen).

Transistor Q1 is used to drive the video to the proper voltage and current levels to drive the video module and/or an external monitor (using the composite video jumpers).

I/O Circuits

(Refer to Figure 4) UART A49 is used to receive (and optionally transmit) serial data from (and to) the keyboard. The transmit path to the keyboard is normally used to conduct the bell tone from the 6522 (via driver Q4) to the speaker in the keyboard.

UARTs A50 (Main Port, P3) and A51 (Printer Port, P4) are used to send and receive serial data from P3 and P4 via the drivers, receivers and switching circuits A39, 40, 47, 48, 56, 57, 58 and 59.

The UARTs A49, 50 and A51 (6551s) are connected to the CPU Bus and generate IRQ interrrupts when commanded by the CPU to send or receive data. Additionally these parts contain internal baud rate generators that must be programmed by the CPU to control the baud rates.

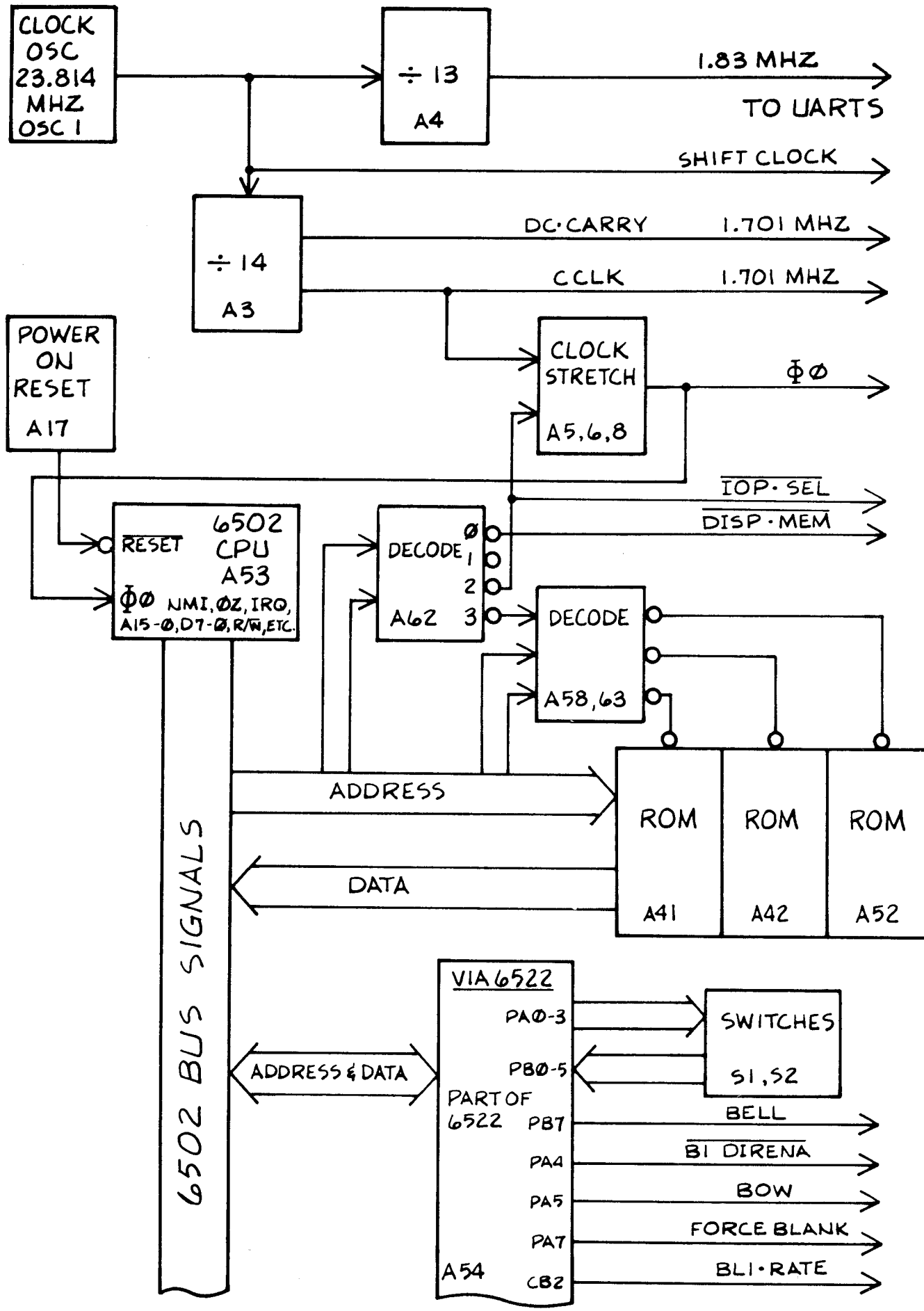


FIG. 1 CPU, TIMING, and CONTROL

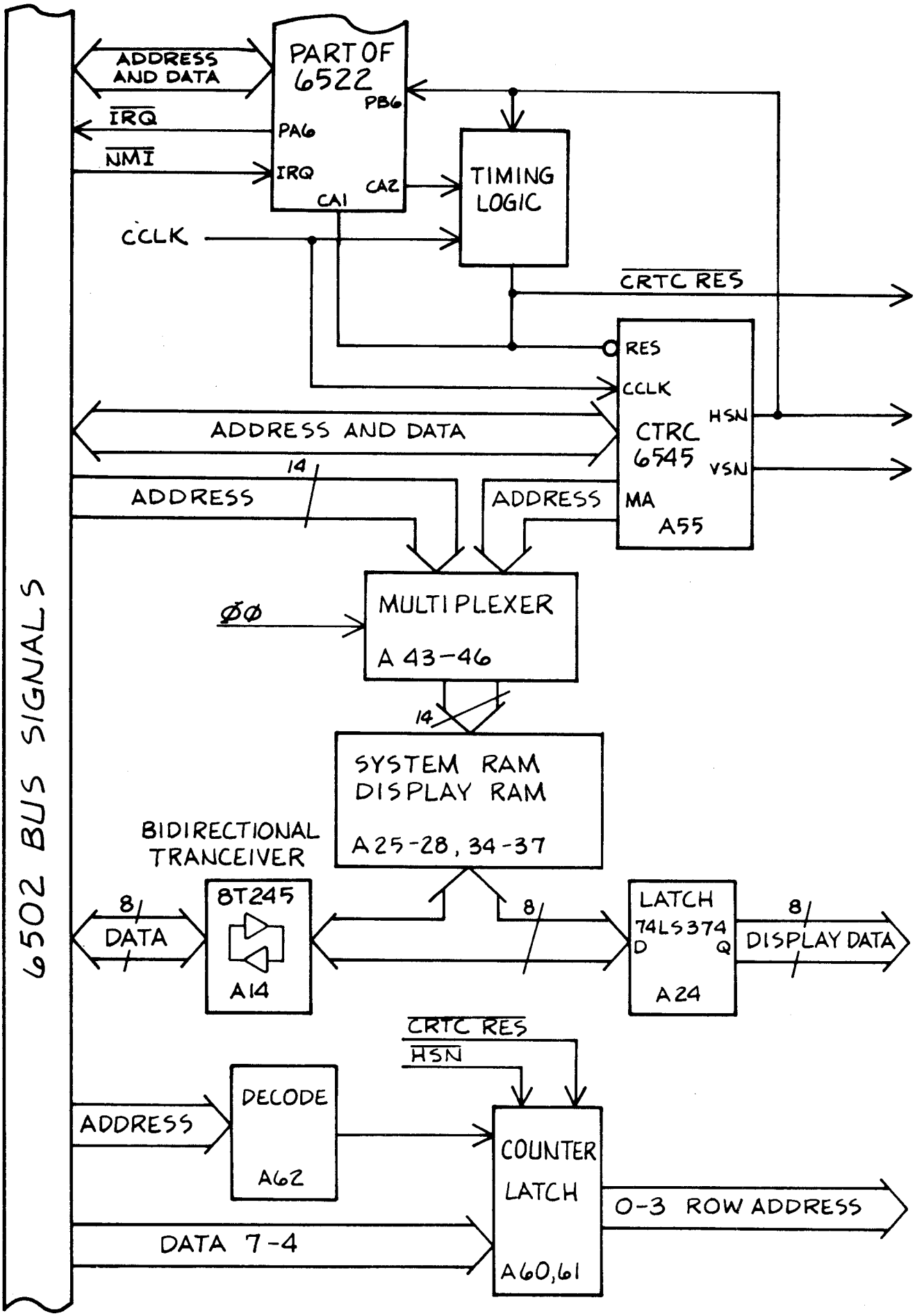


FIG.2 DISPLAY CONTROLLER

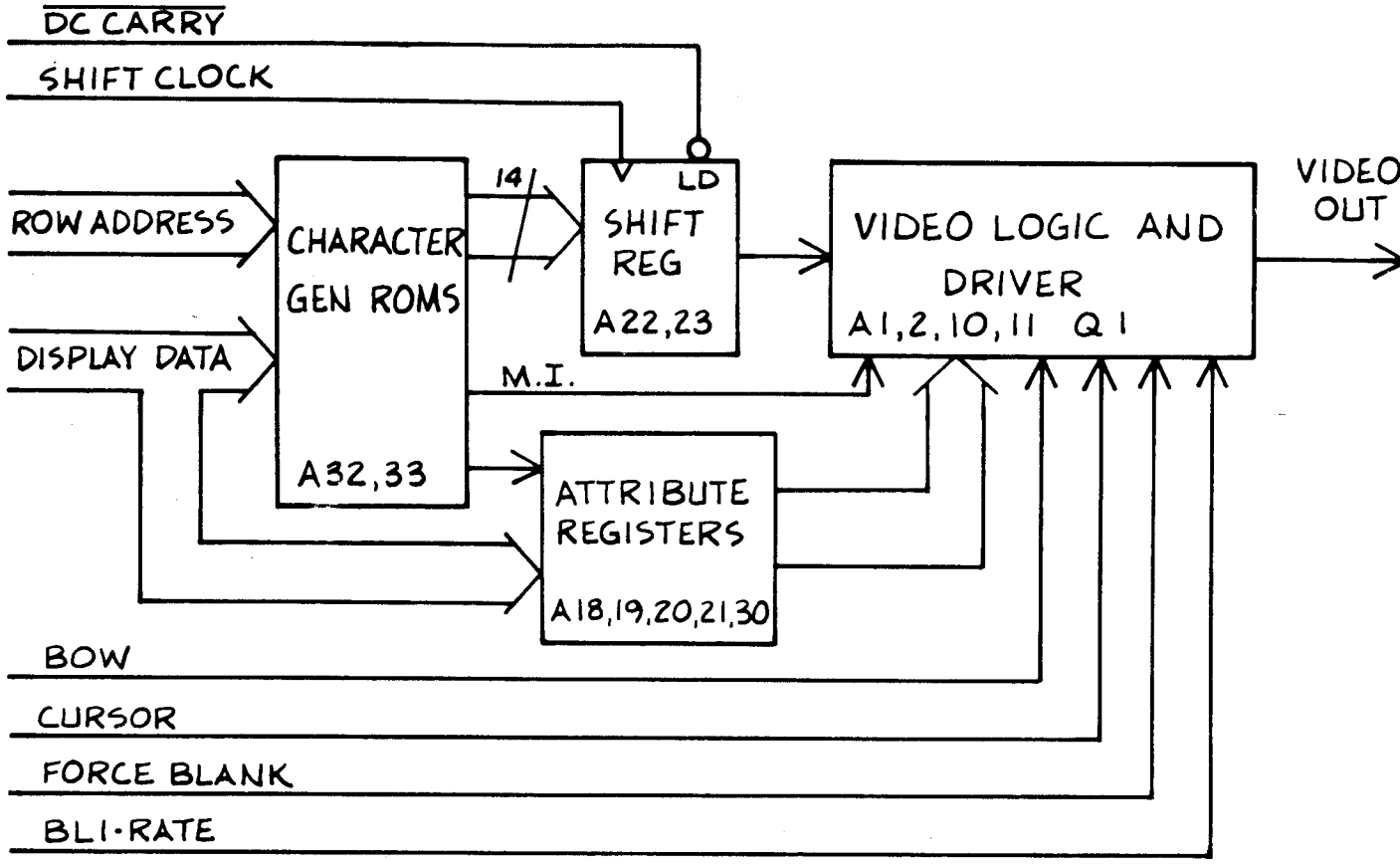


FIG.3 VIDEO GENERATION

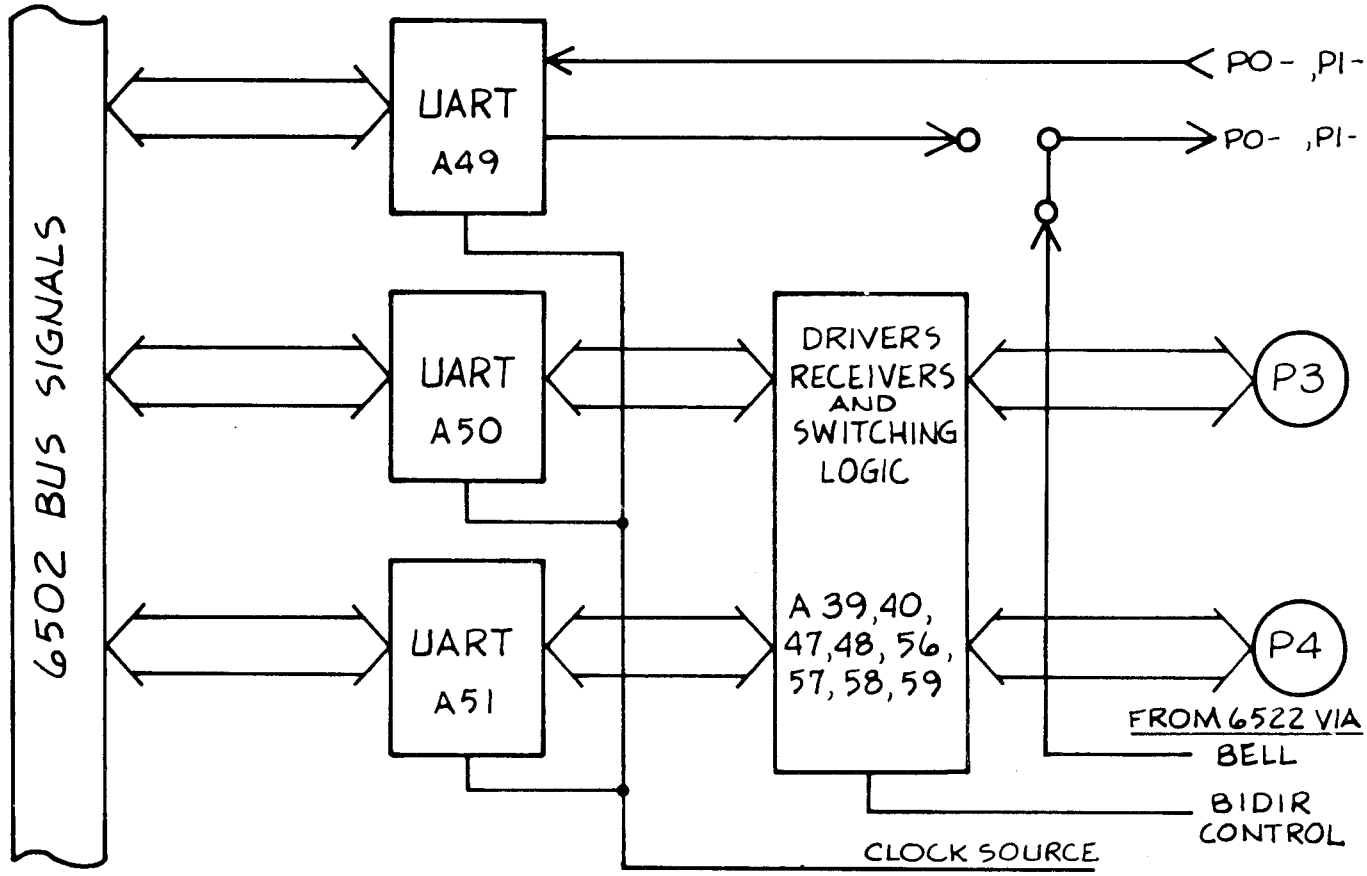


FIG.4 I/O CIRCUITS

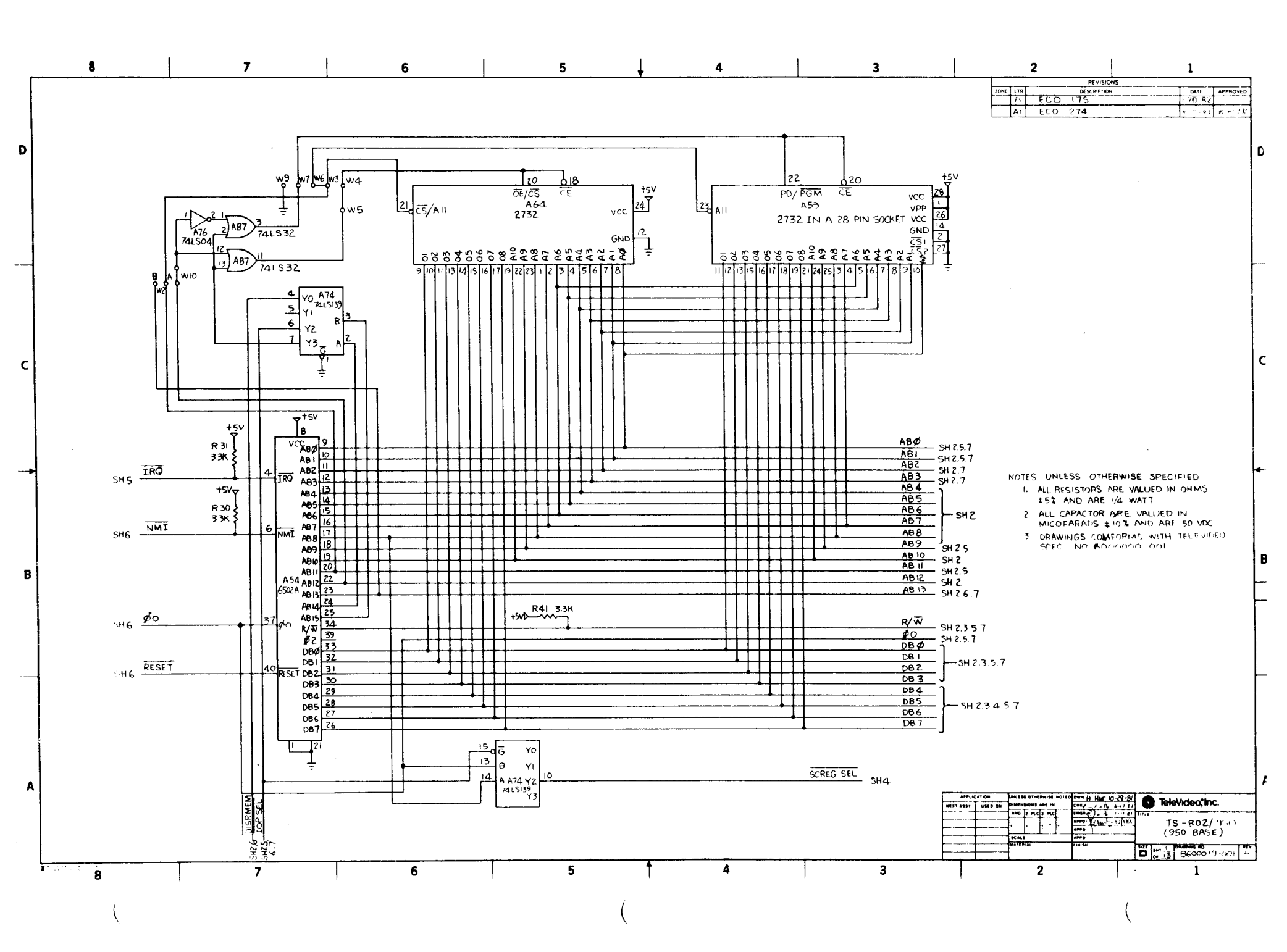
PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
C600100-004	CAP. 100 pf	C12
C900100-004	CAP. 330 pf	C1-11,19
C900100-001	CAP. .01 uf	UNMARKED
C700100-011	CAP. 4.7 uf	C17,20-24
C700100-010	CAP. 10 uf	C16
C700100-003	CAP. 22 uf	C13-15
C900100-008	CAP. .1 uf	C18
I740011-007	IC, Z80A SIO/2	A23,24
I740011-008	IC, Z80A CTC	A25
I740011-009	IC, Z80A CPU	A22
I740011-010	IC, Z80A DMA	A21
I740011-012	IC, MB8264N (200ns)	A13-20
I740010-001	IC, 74LS00	A40,78,86, 99,101
I740010-000	IC, 74S00	A26,105
I740010-004	IC, 74LS04	A27,42,76, 85,91,106
I740010-003	IC, 74S04	A11
I740010-006	IC, 74LS08	A37,45,90, 98
I740010-076	IC, 74LS11	A44
I740010-009	IC, 74LS32	A47,49,87, 104
I740010-074	IC, 74S32	A33
I740010-013	IC, 74LS74	A46,50,75
I740010-012	IC, 74S74	A34,35
I740010-081	IC, 74LS138	A43,48

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
I740010-071	IC, 74S157	A30.38
I740010-080	IC, 93S16	A29,93,94
I740010-018	IC, 74LS163	A8,28
I740010-070	IC, 74LS175	A36
I740010-069	IC, 74S240	A41
I740010-086	IC, 74LS241	A1,31,32
I740010-026	IC, 75188	A4,6
I740010-027	IC, 75189	A3,5
I740010-088	IC, 26LS31	A10
I740010-089	IC, 26LS32	A9
I740010-063	IC, 74LS191	A83
I740010-021	IC, 74LS174	A96
I740010-015	IC, 74LS109	A92
I740010-054	IC, 7406	A103
I740010-014	IC, 74LS86	A102
I740010-016	IC, 74LS139	A74
I740010-017	IC, 74LS157	A51,63,71, 72,97
I740010-019	IC, 74LS166	A81,95
I740010-020	IC, 74LS173	A82
I740010-021	IC, 74LS174	A77,84, 100
I740010-023	IC, 74LS367	A58,59, 66,79
I740010-025	IC, 74LS374	A69
I740011-000	IC, 6116 (2Kx8)	A60-62
I740011-002	IC, 6502A	A54

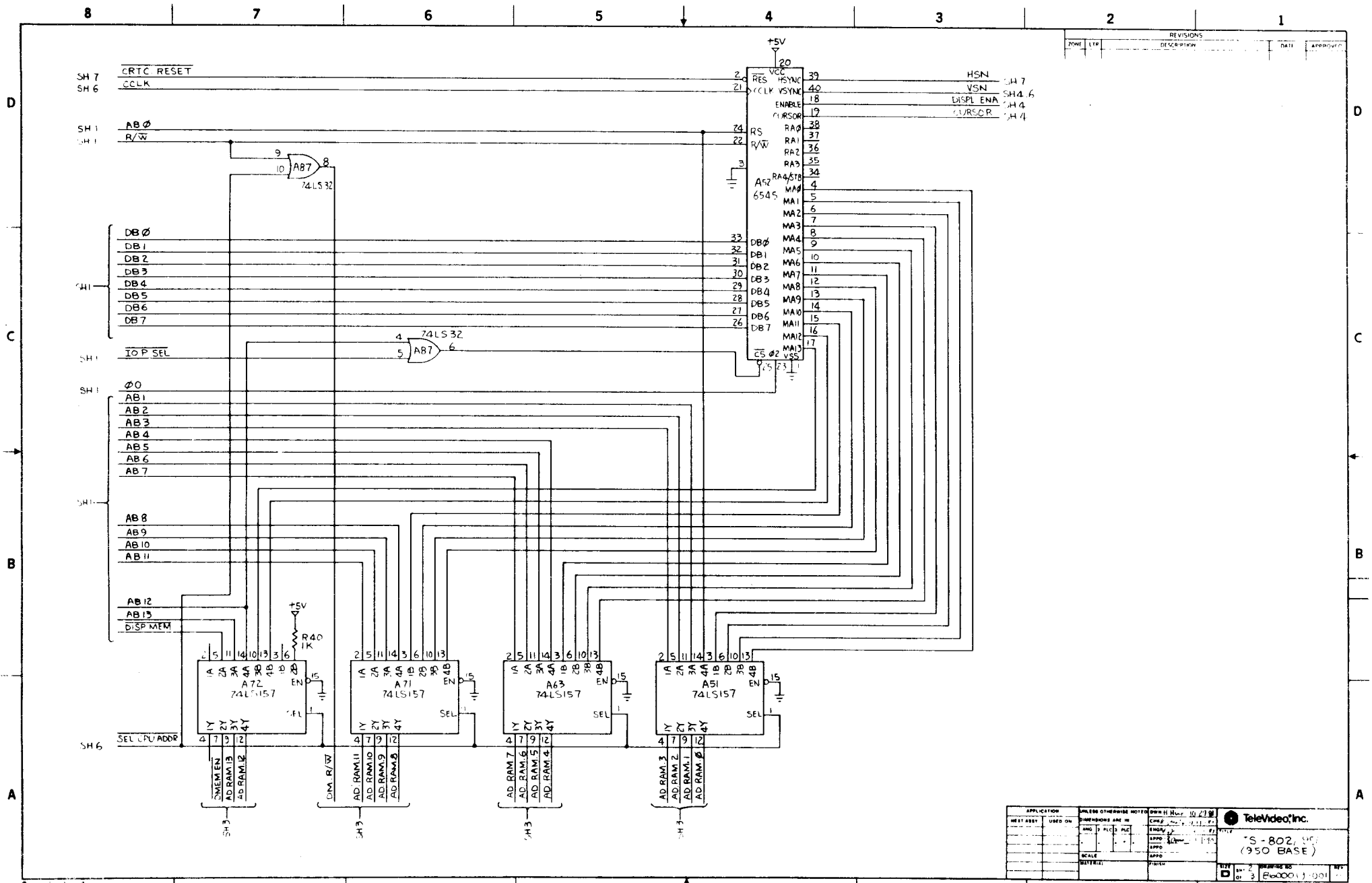
PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
I740011-003	IC, 6545	A52
I740011-004	IC, 6551	A55,56
I740011-005	IC, 6522A	A57
I740010-061	IC, N8T245N	A70
I740010-056	IC, K1114A CRYSTAL OSC	A107
I800000-002	IC, CHAR GEN ROM 2332 (UPPER BYTE)	A67
I800000-003	IC, CHAR GEN ROM 2332 (LOWER BYTE)	A68
I740010-010	IC, 74LS42	A73
I740010-031	IC, NE555	A65
I740010-090	IC, 16 MHZ OSC (LOGO V)	OSC-1
I800000-045	IC, SYSTEM EPROM, Z80 (FOR TS-800A & TS-802)	A39
I800000-050	IC, SYSTEM EPROM, Z80 (FOR TS-802H)	A39
I800000-046	IC, SYSTEM EPROM, LOWER TERMINAL FIRMWARE	A46
I800000-047	IC, SYSTEM EPROM, HIGHER TERMINAL FIRWARE	A53
M200101-003	SWITCH, DIP 20 PIN	SW1,2
M200301-003	SOCKET, 40 PIN	A21-24, 52,54,57
M200301-005	SOCKET, 28 PIN	A25,53, 55,56
M200301-002	SOCKET, 24 PIN	A39,60-62, 64,67,68
M200301-007	SOCKET, 16 PIN	A13-20
M200601-008	PLUG, 5 PIN (RIGHT ANGLE)	P6
M200603-002	PLUG, 2 PIN	P7,9
M200603-005	PLUG, 5 PIN	P5

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
M200202-001	RJ11, FEMALE KEY BD CONN	P10
M200201-001	CONN., 25 PIN RS232 R/A	P1,2
M200207-001	CONN., 15 PIN RS422 R/A	P4
M200209-004	CONN., 40 PIN UNPRO HEADER DOUBLE ROW	P3
R514000-025	RES. 47k ohm	R48
R514000-045	RES. 47 ohm	R14
R514000-031	RES. 100 ohm	R8-10
R514000-001	RES. 68 ohm	R18,19,64
R514000-028	RES. 200 ohm	R13
R514000-003	RES. 330 ohm	R20-23,32,33
R514000-006	RES. Ik ohm	R7,12,15, 17,29,37-40, 42,44,45, 49-58,61, 63,65,66
R514000-011	RES. 4.7k ohm	R2-4,6, 16,24-26, 47,67
R514000-027	RES. 10k ohm	R5,27,28
R514000-015	RES. 750 ohm	R34,60
R514000-002	RES. 270 ohm	R59
R514000-009	RES. 3.3k ohm	R30,31, 41,46
R514000-014	RES. IM ohm	R43
R514000-024	RES. 22 ohm	R11,62
R514000-100	RES. PACK 1k ohm SIP	RP2
R514000-104	RES. PACK 4.7k ohm SIP	RP1
R514000-105	RES. PACK 68 ohm DIP	RP3,4
R514000-112	RES. PACK 4.7K OHM SIP	RP5

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
S360100-003	LED, (SMA TYP)	CR1-4
S360100-000	DIODE, IN914	CR6,7
S360100-001	DIODE, IN4001	CR5
S350100-003	TRANSISTOR, 2N2907	Q1
S350100-000	TRANSISTOR, 2N2219	Q2,3

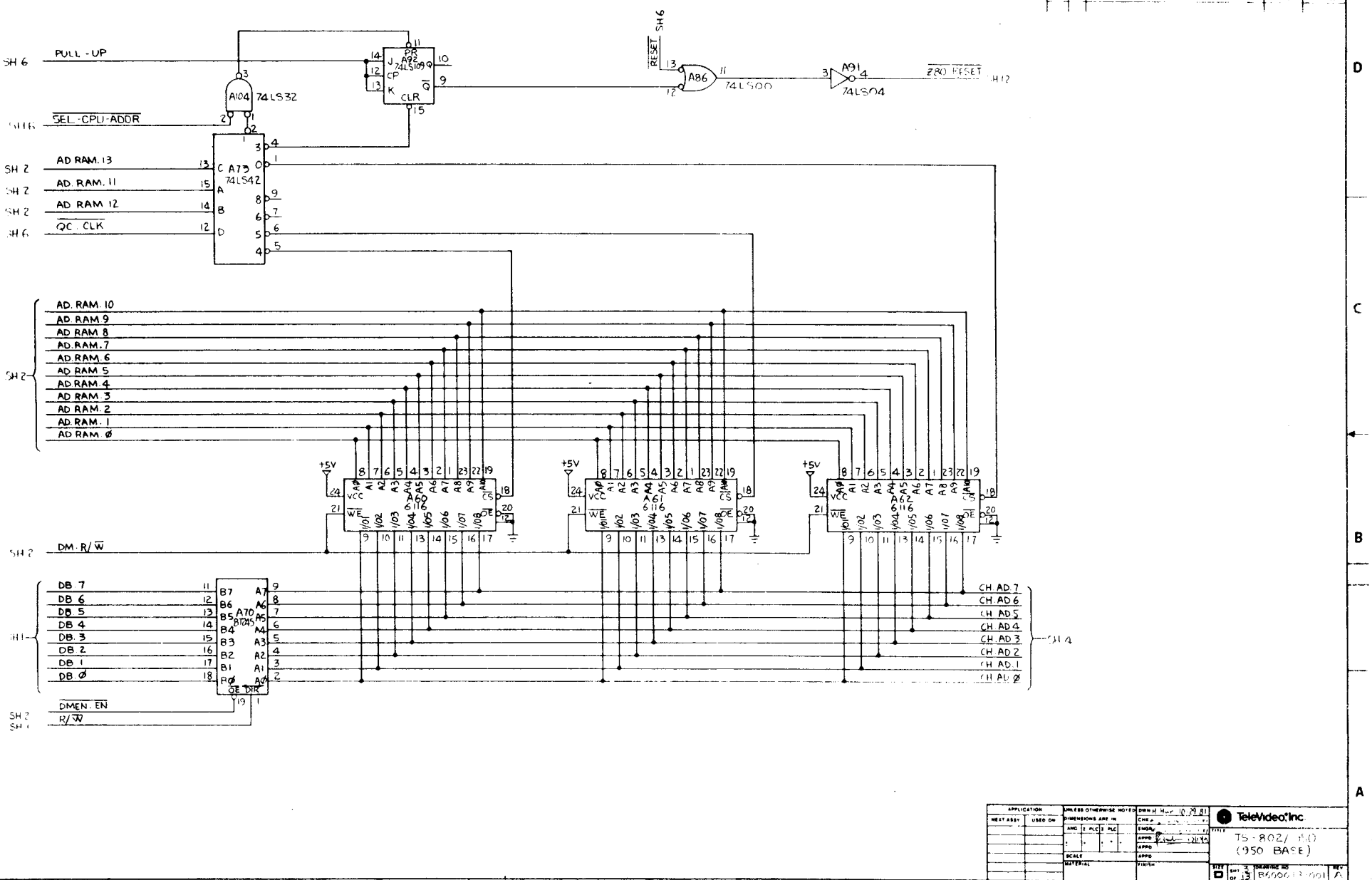

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | ECO 175 | 1/20/82
A1 | ECO 274
A76 74LS04
A87 74LS32
A87 74LS32
W9 W7 W6 W3 W4 W5 W10
A74 74LS139
A64 2732
CS/A11
OE/CS
CE
VCC
GND
A59
2732 IN A 28 PIN SOCKET
PD/PGM
CE
VCC
VPP
VCC
GND
CS1
CS2
A11
+5V
R31 3.3K
R30 3.3K
R41 3.3K
IRQ
NMI
RESET
Ø0
R/W
Ø2
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
A54 6502A
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
SH5
SH6
SH6
SH6
SH2
SH2,5,7
SH2,7
SH2,5
SH2,6,7
SH2,3,5,7
SH2,3,4,5,7
SCREG SEL
SH4
DISPMEM
TOP SEL
SH2,6
SH2,5,6,7
NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT
2 ALL CAPACTOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC
3 DRAWINGS CONFORMS WITH TELEVIDEO SPEC NO 800[illegible]-001
TeleVideo, Inc.
TS-802/'810
(950 BASE)
SIZE D
DRAWING NO 8600013-001
REV A1

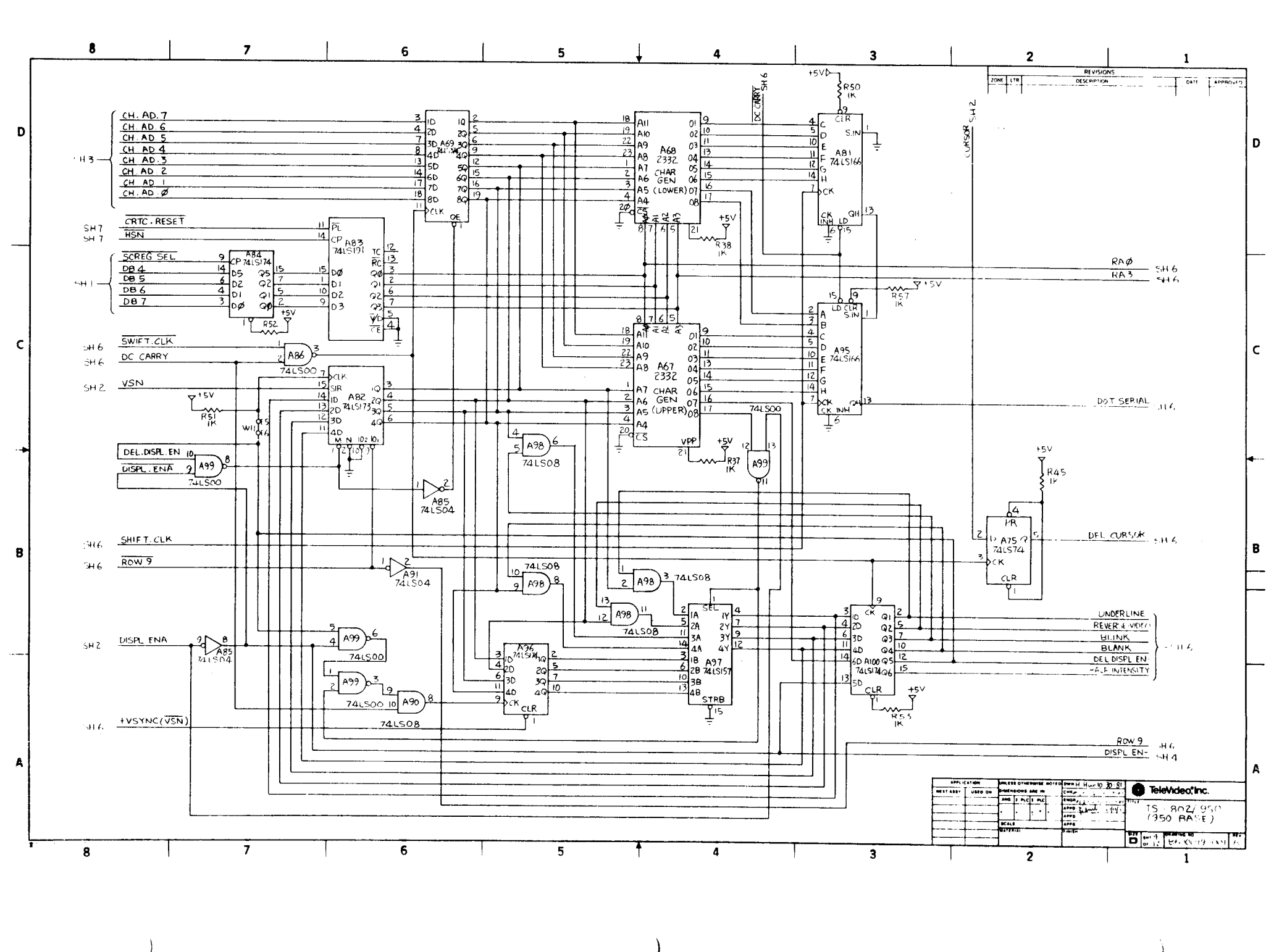
TS800A, TS802, TS802H THEORY OF OPERATION

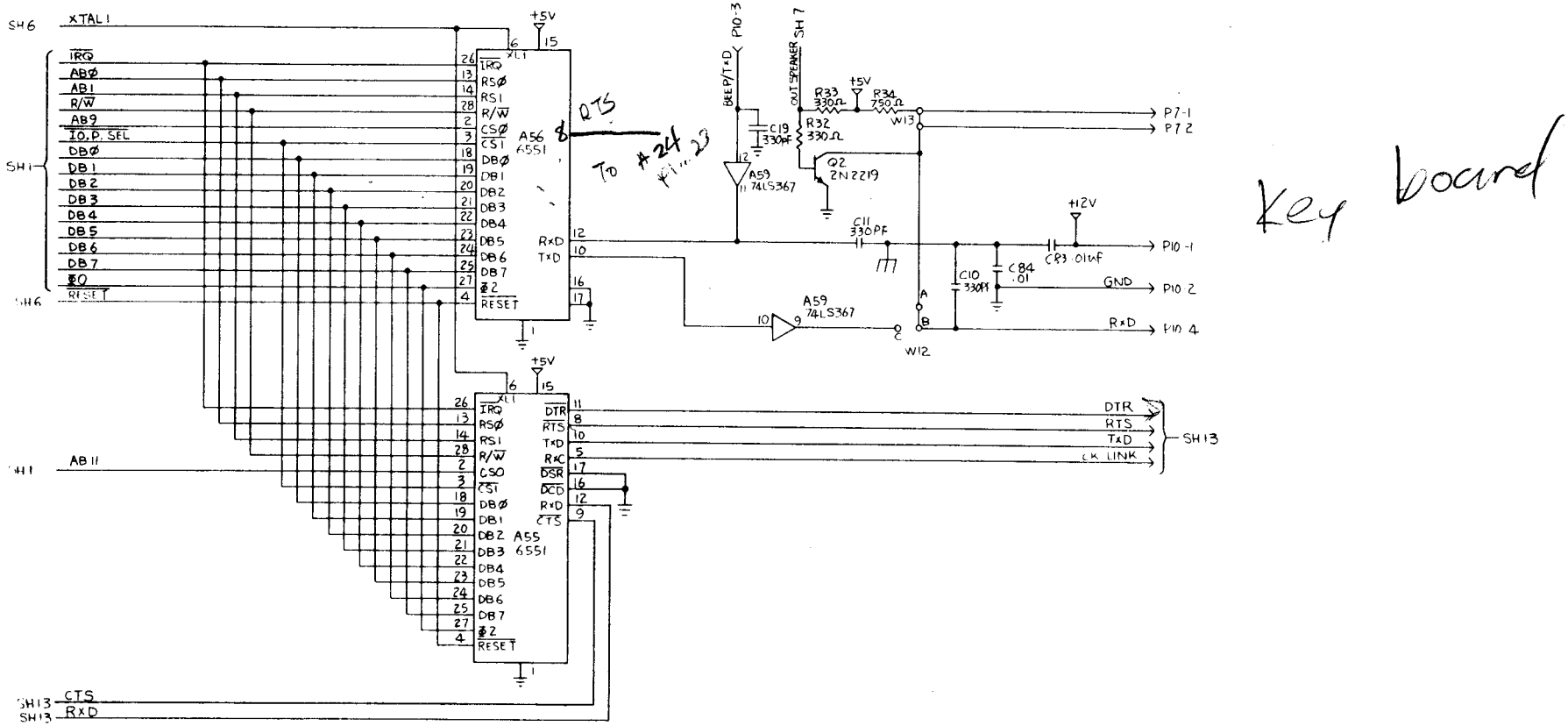


TeleVideo, Inc.

TS-802, SPC
(950 BASE)


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SH 6
PULL - UP
A104 74LS32
SEL - CPU - ADDR
A92 74LS109
RESET
A86 74LS00
A91 74LS04
ZRO RESET
A73 74LS42
AD RAM 13
AD RAM 11
AD RAM 12
QC - CLK
AD RAM 10
AD RAM 9
AD RAM 8
AD RAM 7
AD RAM 6
AD RAM 5
AD RAM 4
AD RAM 3
AD RAM 2
AD RAM 1
AD RAM Ø
+5V
A60-A65 6116
DM - R/W
DB 7
DB 6
DB 5
DB 4
DB 3
DB 2
DB 1
DB Ø
A70 8T245
DMEN - EN
R/W
CH AD 7
CH AD 6
CH AD 5
CH AD 4
CH AD 3
CH AD 2
CH AD 1
CH AD Ø
TeleVideo, Inc.
TS-802/ 810
(950 BASE)


CH. AD. 7
CH. AD. 6
CH. AD. 5
CH. AD. 4
CH. AD. 3
CH. AD. 2
CH. AD. 1
CH. AD. Ø
CRTC. RESET
HSN
SCREG. SEL
DB 4
DB 5
DB 6
DB 7
SWIFT. CLK
DC CARRY
VSN
DEL. DISPL. EN
DISPL. ENA
SHIFT. CLK
ROW 9
DISPL ENA
+VSYNC(VSN)
A68 2332 CHAR GEN (LOWER)
A67 2332 CHAR GEN (UPPER)
A81 74LS166
A95 74LS166
A83 74LS191
A84 74LS174
A82 74LS173
A69 74LS374
A75 74LS74
A96 74LS374
A97 74LS157
A100 74LS174
A85 74LS04
A86 74LS00
A90 74LS08
A91 74LS04
A98 74LS08
A99 74LS00
R50 1K
R51 1K
R52
R37 1K
R38 1K
R45 1K
R55 1K
R57 1K
+5V
DC CARRY SH 6
CURSOR SH 2
RAØ
RA 3
DOT SERIAL
DEL CURSOR
UNDERLINE
REVERSE VIDEO
BLINK
BLANK
DEL DISPL EN
HALF INTENSITY
ROW 9
DISPL EN-
REVISIONS
TeleVideo Inc.
TS-802/950
(350 BASE)



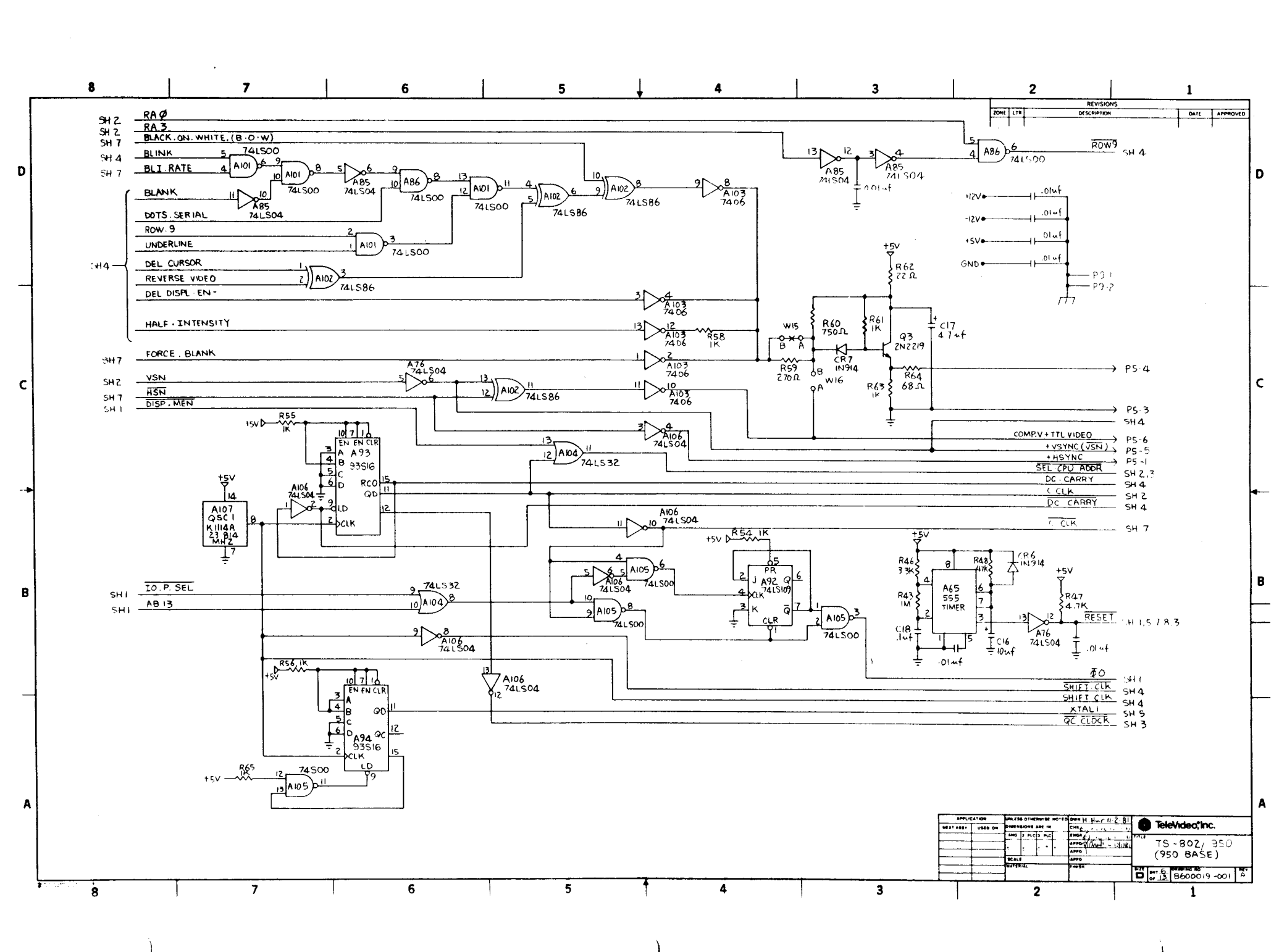
Key board

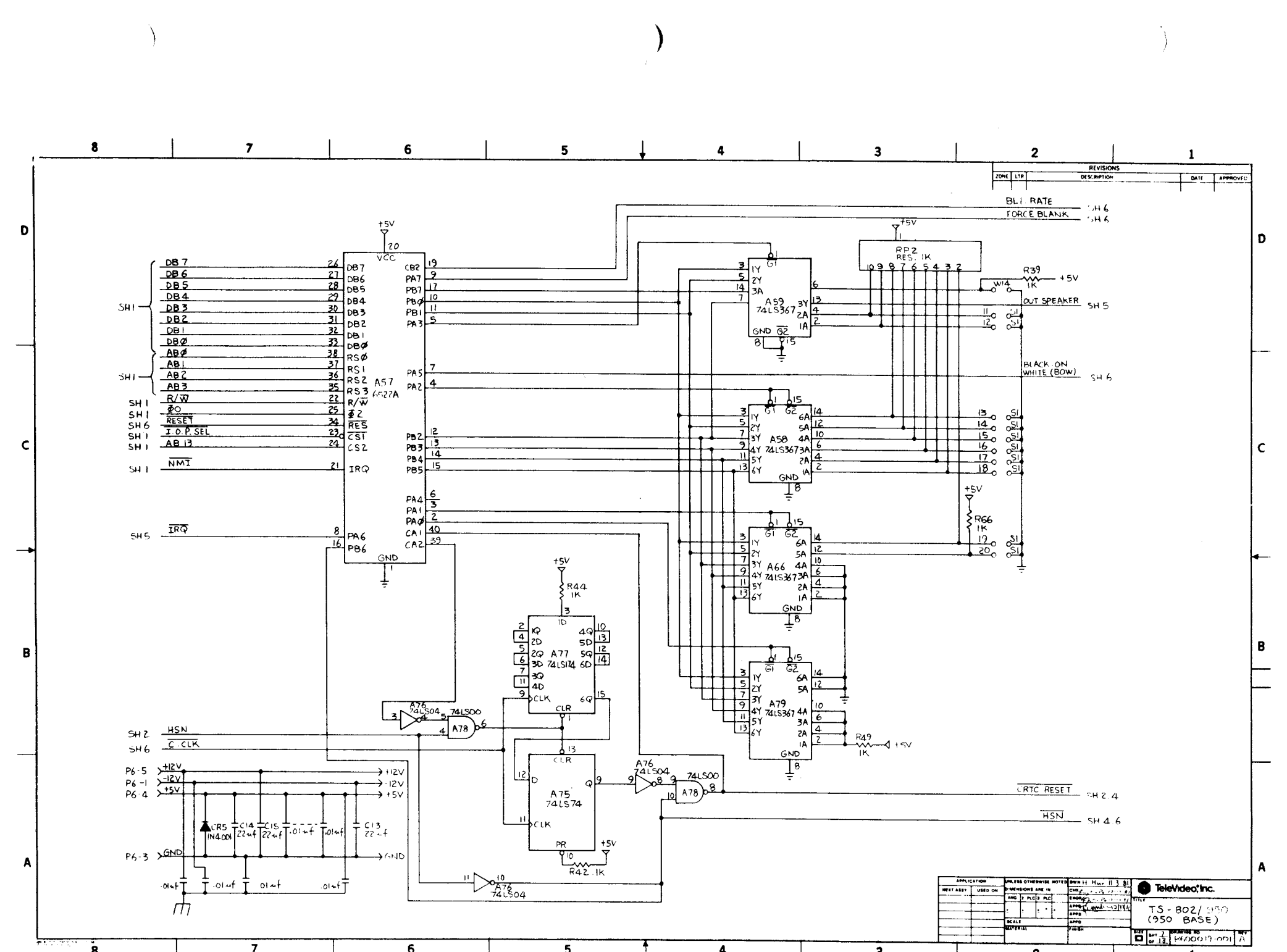
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

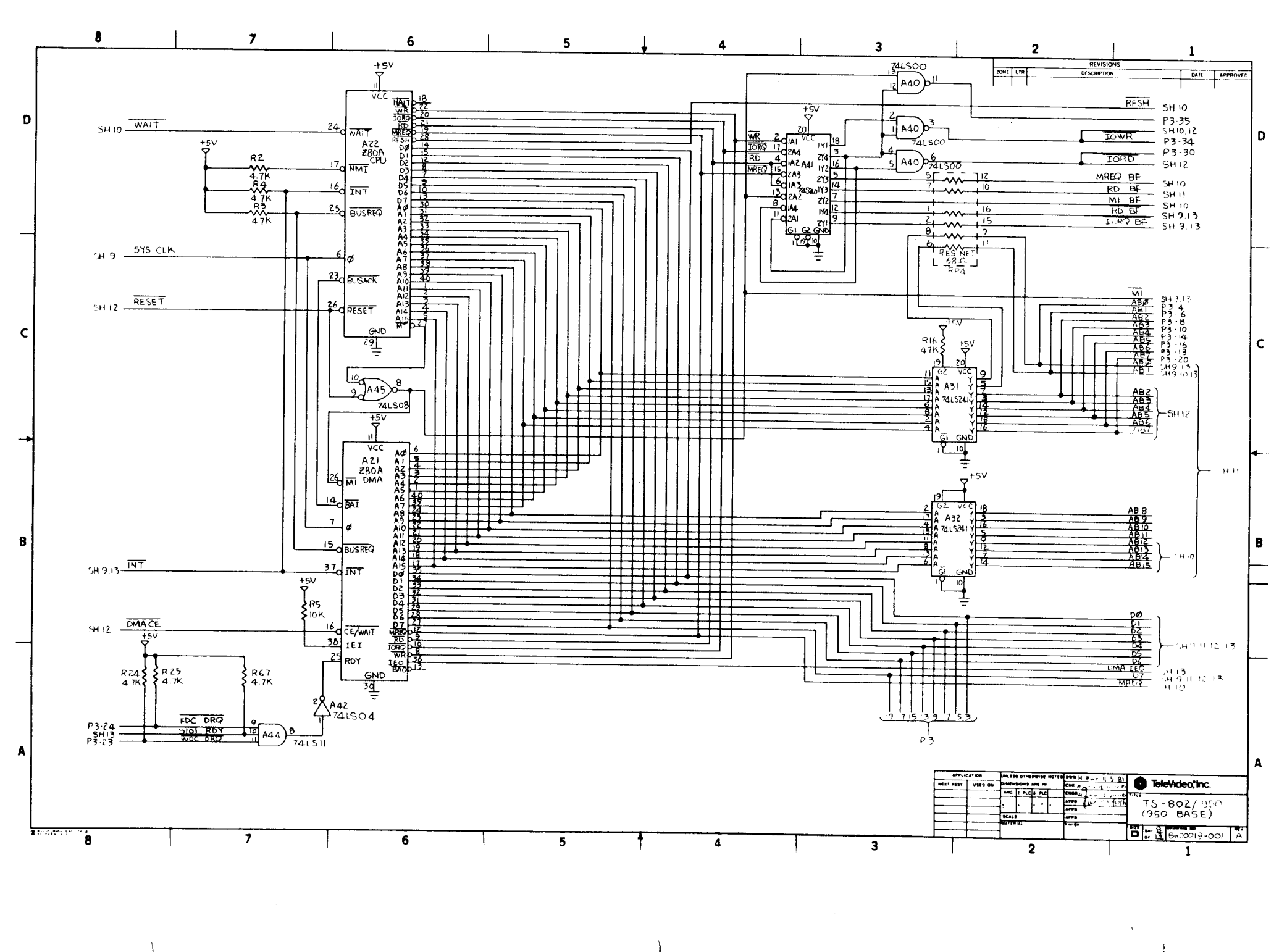
TeleVideo, Inc.

TS-802/950
(950 BASE)

D | SHT 5 OF 13 | A69001B-001 | REV A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
RA Ø
RA 3
BLACK ON WHITE (B·O·W)
BLINK
BLI RATE
BLANK
DOTS SERIAL
ROW 9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
DEL DISPL EN-
HALF · INTENSITY
FORCE BLANK
VSN
HSN
DISP MEN
ROW9
+12V
-12V
+5V
GND
P3-1
P3-2
P5-4
P5-3
P5-6
P5-5
P5-1
COMP V + TTL VIDEO
+VSYNC (VSN)
+HSYNC
SEL CPU ADDR
DC CARRY
C CLK
IO P SEL
AB 13
Ø0
SHIFT CLK
XTAL1
QC CLOCK
RESET
TeleVideo Inc.
TS-802/ 950
(950 BASE)
B600019-001


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
BLT RATE
FORCE BLANK
OUT SPEAKER
BLACK ON WHITE (BOW)
CRTC RESET
HSN
A57 6502A
A59 74LS367
A58 74LS367
A66 74LS367
A79 74LS367
A77 74LS174
A75 74LS74
A76 74LS04
A78 74LS00
RP2 RES. 1K
R39 1K
R66 1K
R44 1K
R42 1K
R49 1K
CR5 IN4001
C14 22uf
C15 22uf
C13 22uf
.01uf
P6-5 +12V
P6-1 -12V
P6-4 +5V
P6-3 GND
TeleVideo, Inc.
TS-802/950
(950 BASE)


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A22 Z80A CPU
A21 Z80A DMA
A31 74LS241
A32 74LS241
A45 74LS08
A42 74LS04
A44 74LS11
A40 74LS00
A41 74LS00
RES NET 68Ω RP4
R2 4.7K
R4 4.7K
R5 4.7K
R5 10K
R16 4.7K
R24 4.7K
R25 4.7K
R67 4.7K
WAIT
SYS CLK
RESET
INT
DMACE
FDC DRQ
SIO RDY
WDC DRQ
RFSH
IOWR
IORD
MREQ BF
RD BF
M1 BF
IORQ BF
P3
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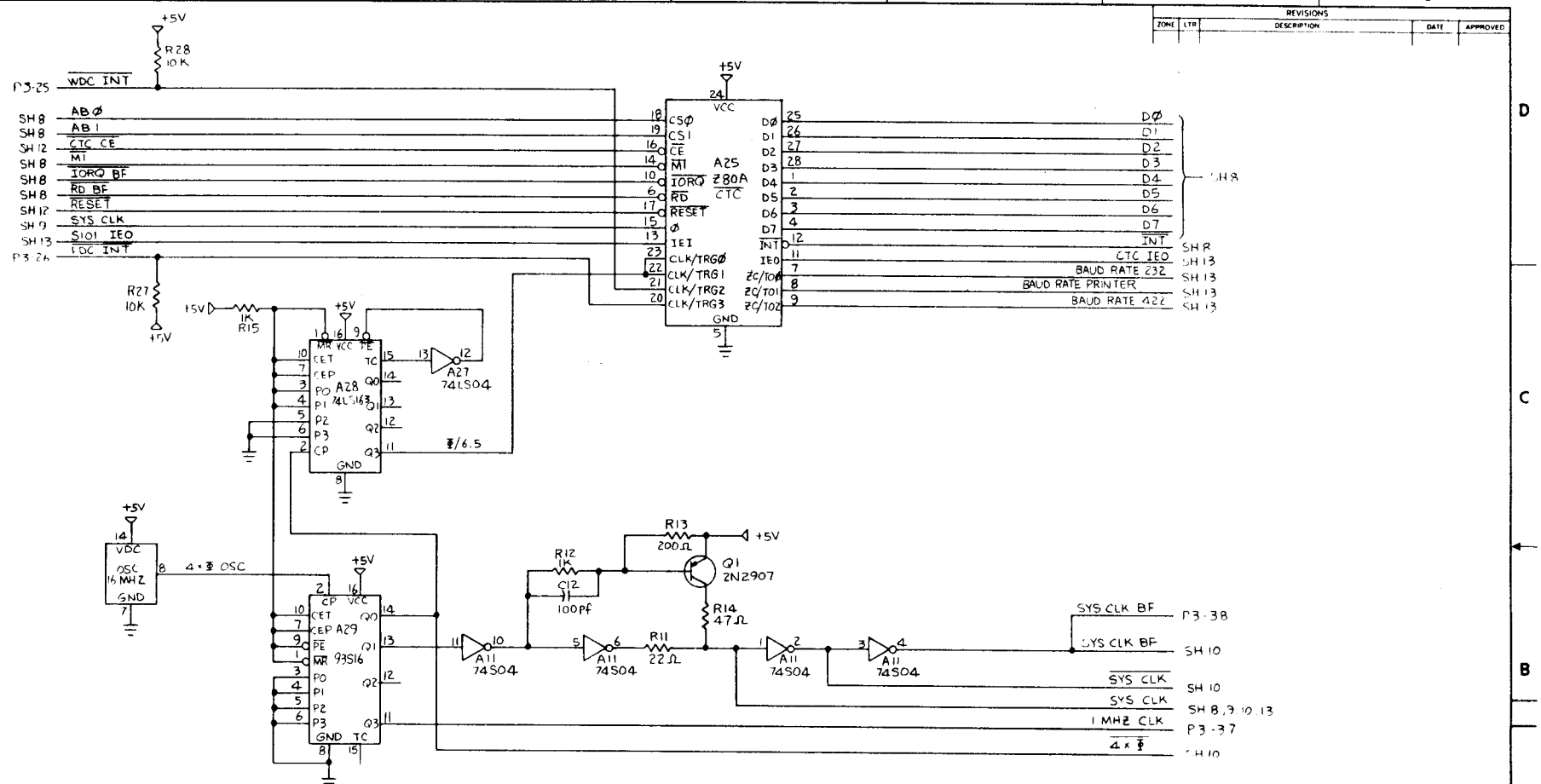
5A0019-001
REV A

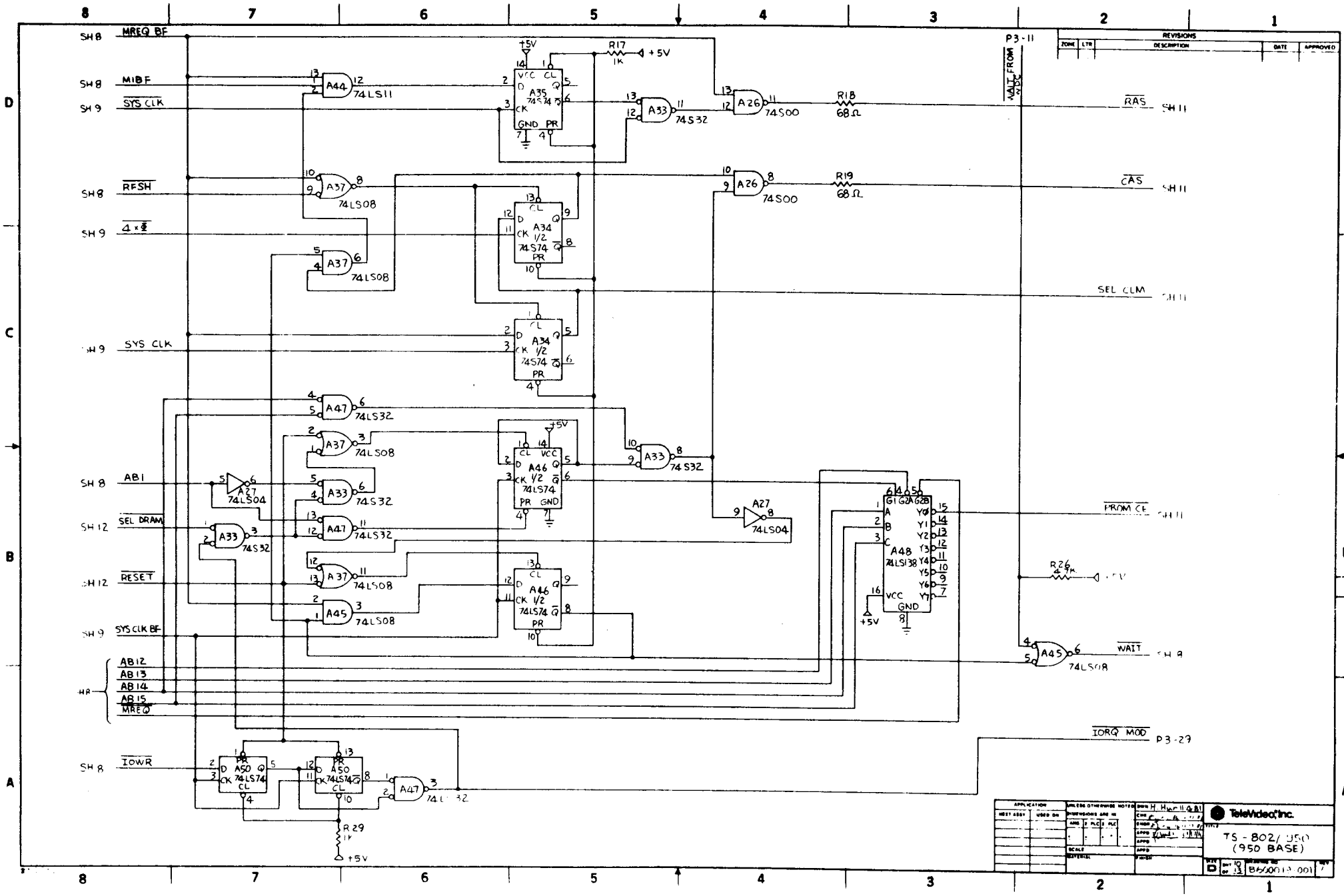


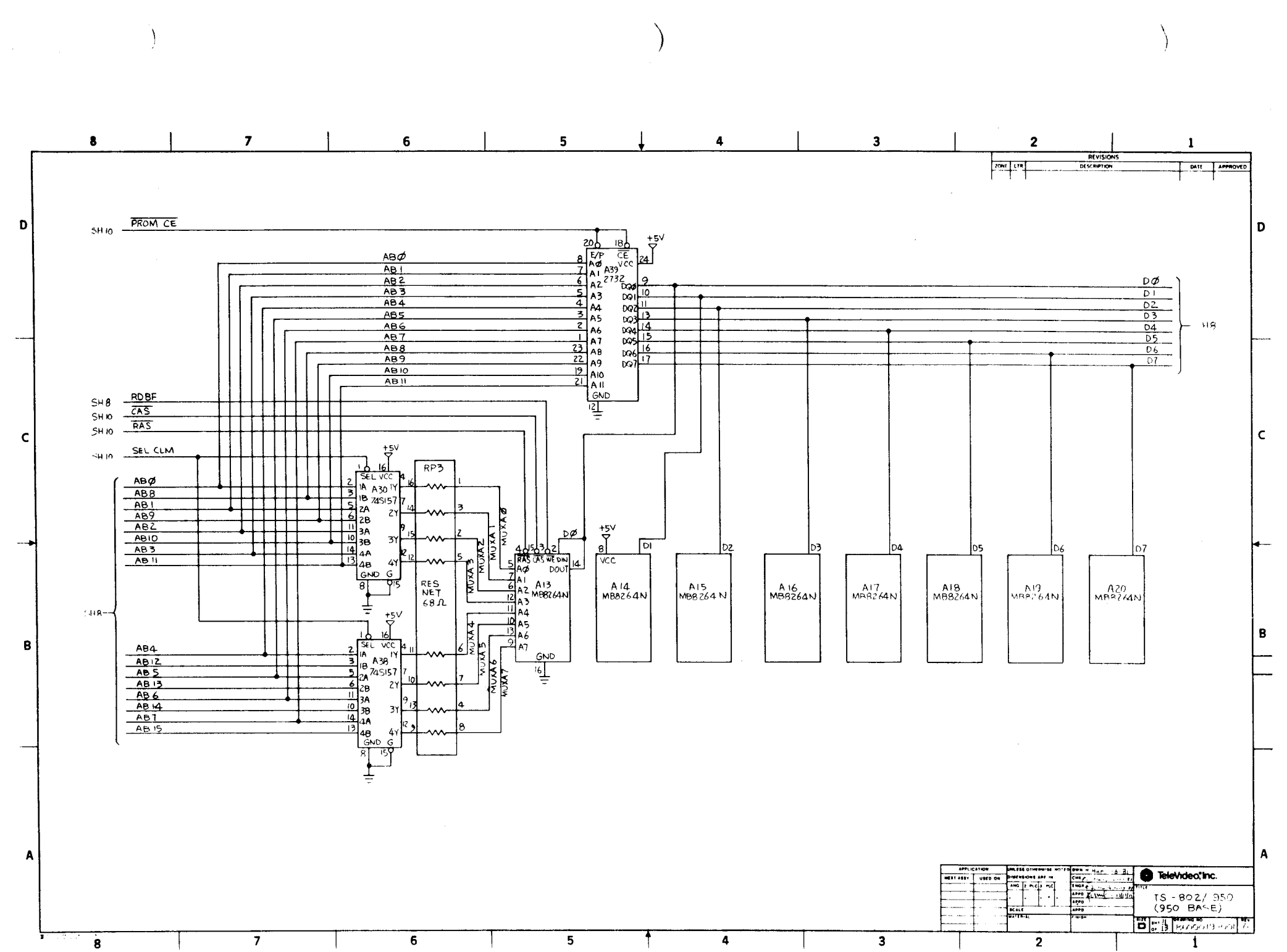
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TeleVideo Inc.

TS-802/950
(950 BASE)

SIZE D | SHT 2 OF 13 | DRAWING NO 8500013-001 | REV F


MREQ BF
MIBF
SYS CLK
RFSH
4 x Φ
SYS CLK
ABI
SEL DRAM
RESET
SYS CLK BF
AB12
AB13
AB14
AB15
MREQ
IOWR
A44 74LS11
A35 74S74
A33 74S32
A26 74S00
R17 1K
R18 68Ω
R19 68Ω
A37 74LS08
A34 1/2 74S74
A47 74LS32
A46 1/2 74LS74
A27 74LS04
A48 74LS138
A50 74LS74
A45 74LS08
R29 1K
+5V
P3-11
WAIT FROM MOD
RAS
CAS
SEL CLM
PROM CE
R26 1K
WAIT
IORQ MOD P3-29
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
TeleVideo, Inc.
TS-802/950
(950 BASE)
B6900013-001


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
PROM CE
SH10
+5V
A39 2732
E/P
CE
VCC
GND
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
D0
D1
D2
D3
D4
D5
D6
D7
D[8]
SH8 RDBF
SH10 CAS
SH10 RAS
SH10 SEL CLM
A30 74S157
A38 74S157
SEL
VCC
GND
RP3
RES NET 68Ω
MUXA0
MUXA1
MUXA2
MUXA3
MUXA4
MUXA5
MUXA6
MUXA7
A13 MB8264N
RAS CAS WE DIN DOUT
A14 MB8264N
A15 MB8264N
A16 MB8264N
A17 MB8264N
A18 MB8264N
A19 MB8264N
A20 MB8264N
TeleVideo, Inc.
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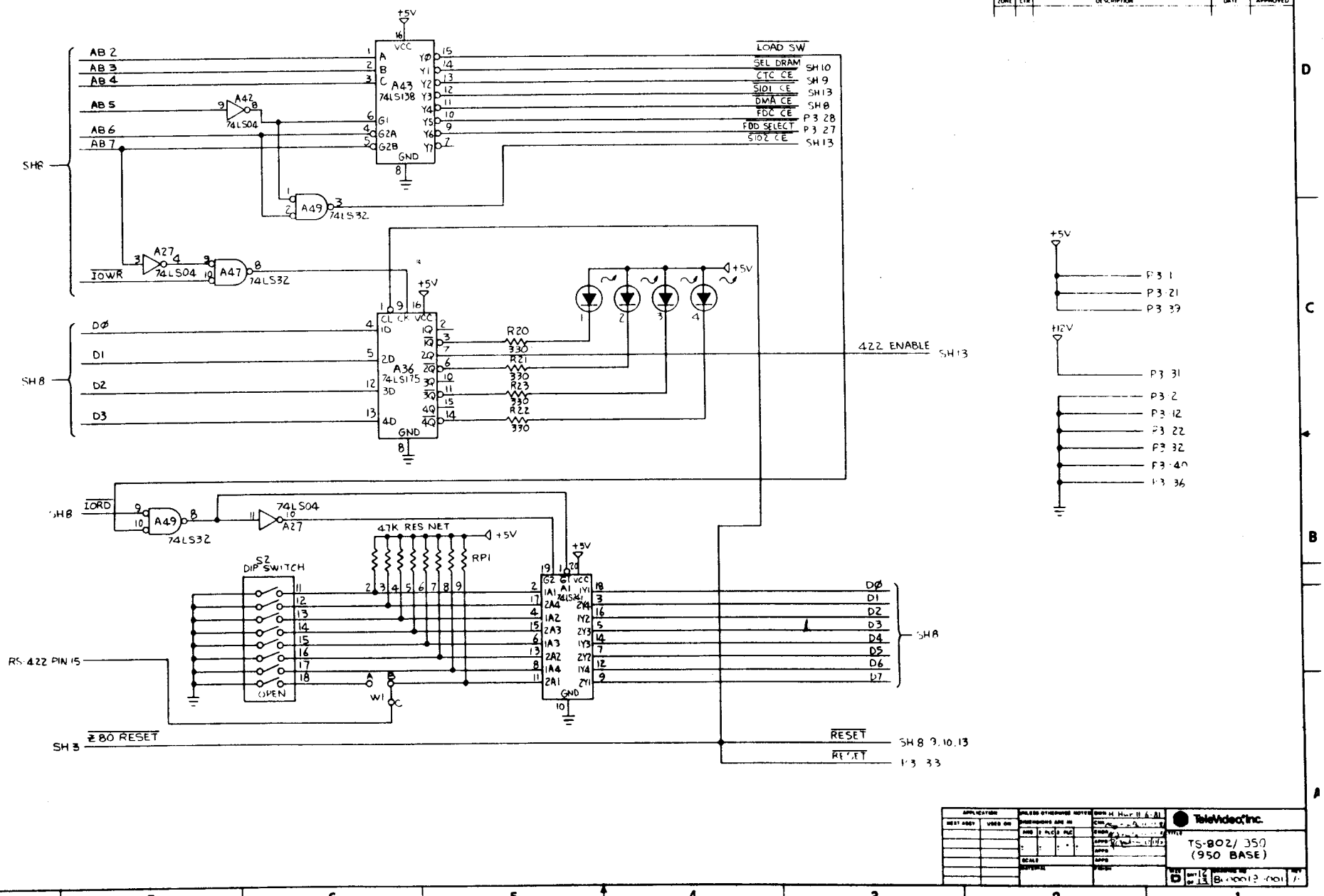
(950 BASE)



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

TeleVideo Inc.

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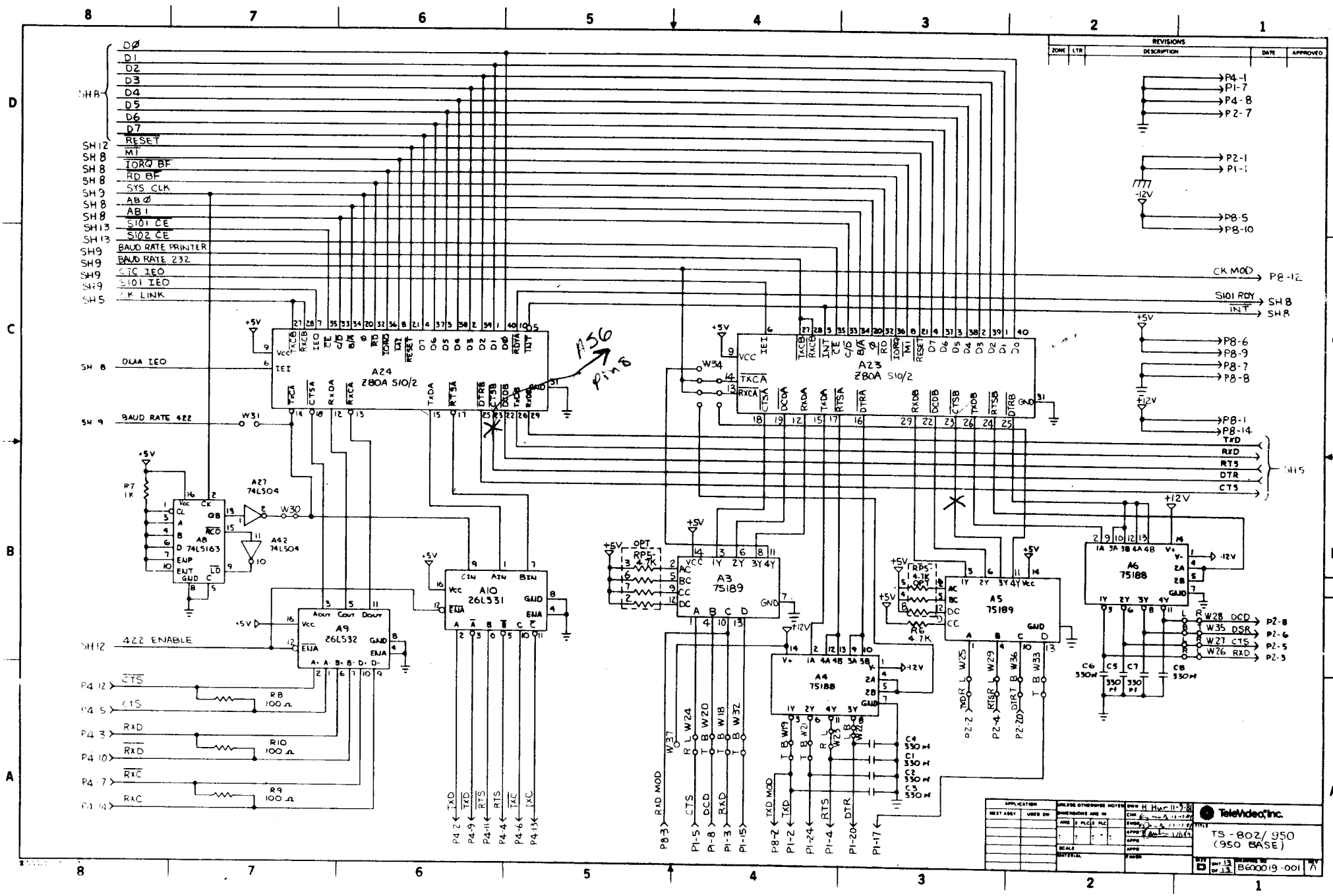
(950 BASE)

SIZE D

402H


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
D0
D1
D2
D3
D4
D5
D6
D7
RESET
M1
IORQ BF
RD BF
SYS CLK
AB0
AB1
S101 CE
S102 CE
BAUD RATE PRINTER
BAUD RATE 232
CTC IEO
S101 IEO
CK LINK
DUA IEO
BAUD RATE 422
422 ENABLE
A24 Z80A SIO/2
A23 Z80A SIO/2
A8 74LS163
A27 74LS04
A42 74LS04
A10 26LS31
A9 26LS32
A3 75189
A4 75188
A5 75189
A6 75188
W30
W31
W34
R7 1K
R8 100Ω
R9 100Ω
R10 100Ω
R6 4.7K
RPS 4.7K
OPT RPF 4.7K
C1 330 pf
C2 330 pf
C3 330 pf
C4 330 pf
C5 330 pf
C6 330 pf
C7 330 pf
C8 330 pf
CK MOD
S101 RDY
INT
TXD
RXD
RTS
DTR
CTS
RXD MOD
TXD MOD
P4-1
P1-7
P4-8
P2-7
P2-1
P1-1
-12V
P8-5
P8-10
P8-12
P8-6
P8-9
P8-7
P8-8
+12V
P8-1
P8-14
W28 DCD
W35 DSR
W27 CTS
W26 RXD
P2-8
P2-6
P2-5
P2-3
P4-12 CTS
P4-5 CTS
P4-3 RXD
P4-10 RXD
P4-7 RXC
P4-14 RXC
P4-2 TXD
P4-9 TXD
P4-11 RTS
P4-4 RTS
P4-6 TXC
P4-13 TXC
P8-3
P1-5 CTS
P1-8 DCD
P1-3 RXD
P1-15
P8-2
P1-2 TXD
P1-24 RTS
P1-4 DTR
P1-20
P1-17
P156 Pin 8
TeleVideo, Inc.
TS-802/950
(950 BASE)
B600019-001
REV A

REVISIONS			
LTR	DESCRIPTION	DATE	
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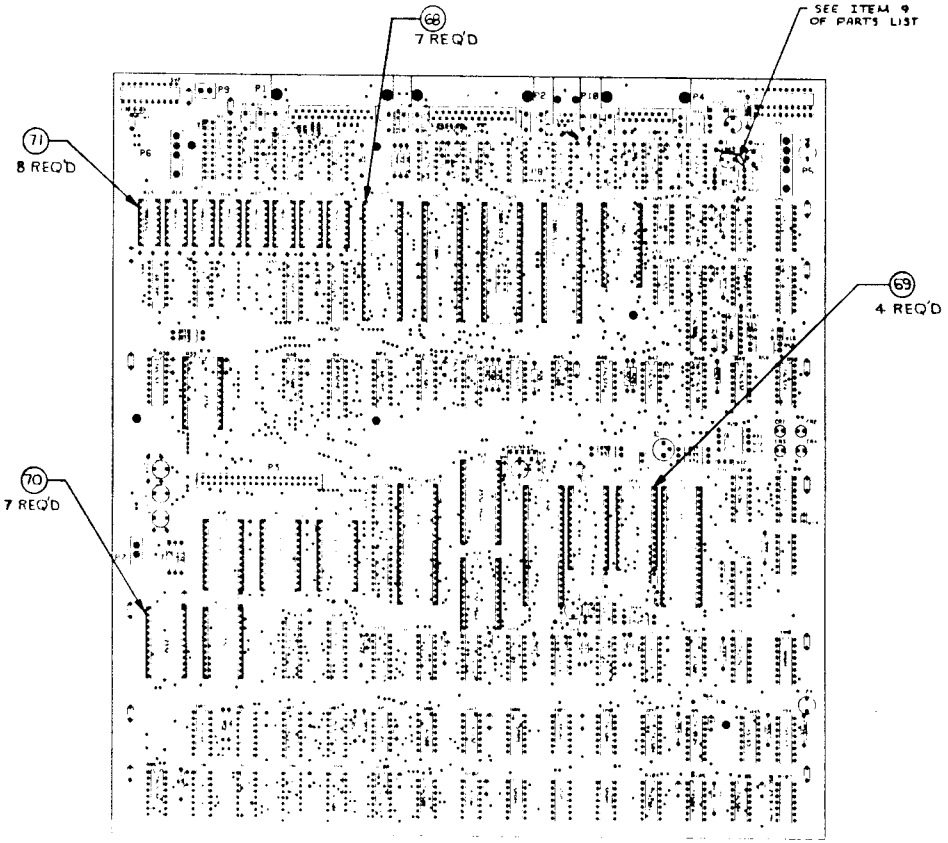
A1	ECO 212, 229		
A2	ECO 228		
A3	ECO 274		



NOTE: UNLESS OTHERWISE SPECIFIED

1. REFER TO SEPARATE PARTS LIST FOR COMPLETE IDENTIFICATION OF REFERENCE DESIGNATION.
2. MADE FROM E109019-001 FAB REV A.
3. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
4. PAPER STAMP REV. LETTER APPROXIMATELY WHERE SHOWN.
5. RES.PACK RPS 4.7K HAS BEEN DELETED FROM ASSEMBLY DWG.

TeleVideo, Inc.

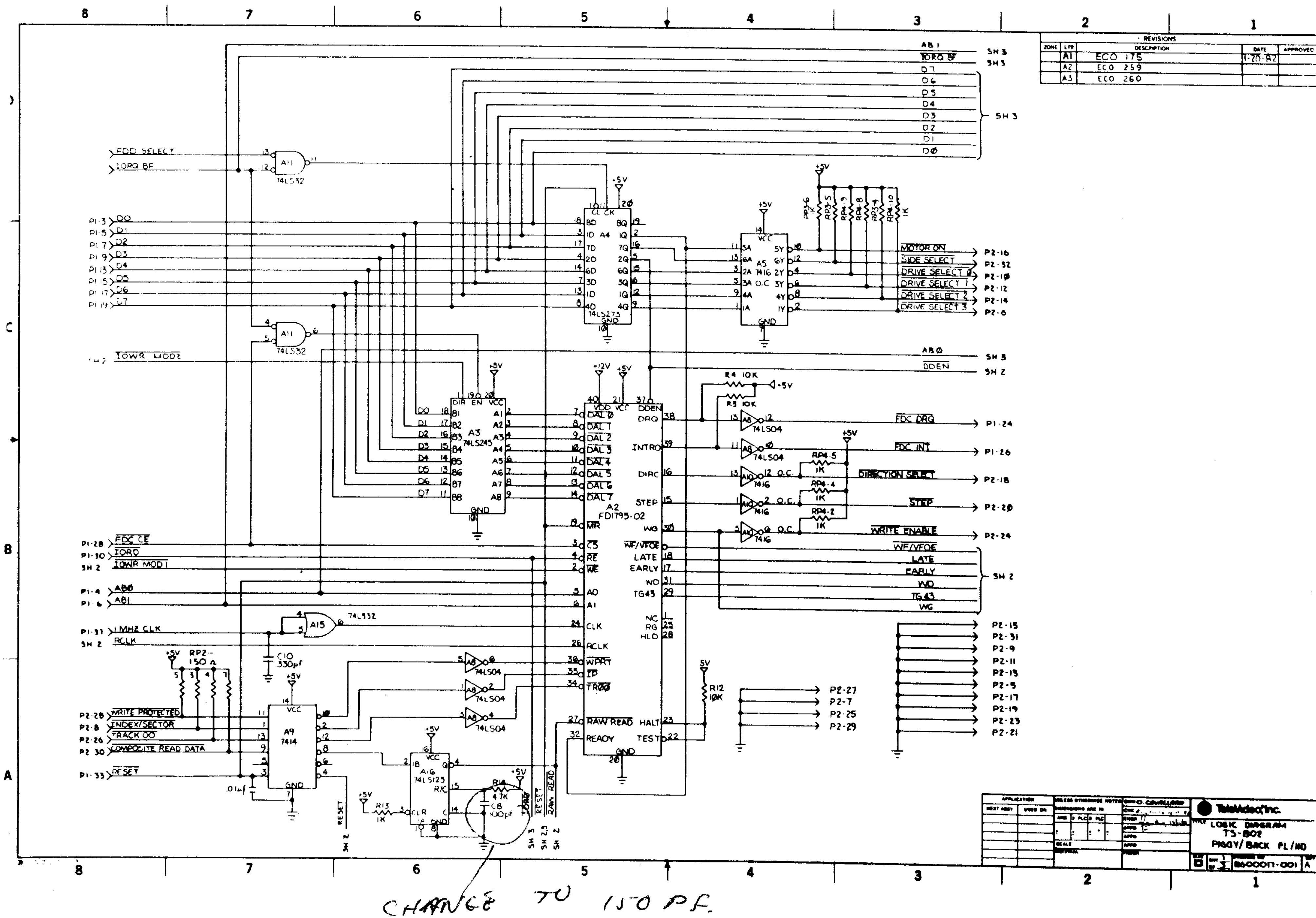
ASSEMBLY DWG
TS-802/950/H

D | 803209-001/002 | A

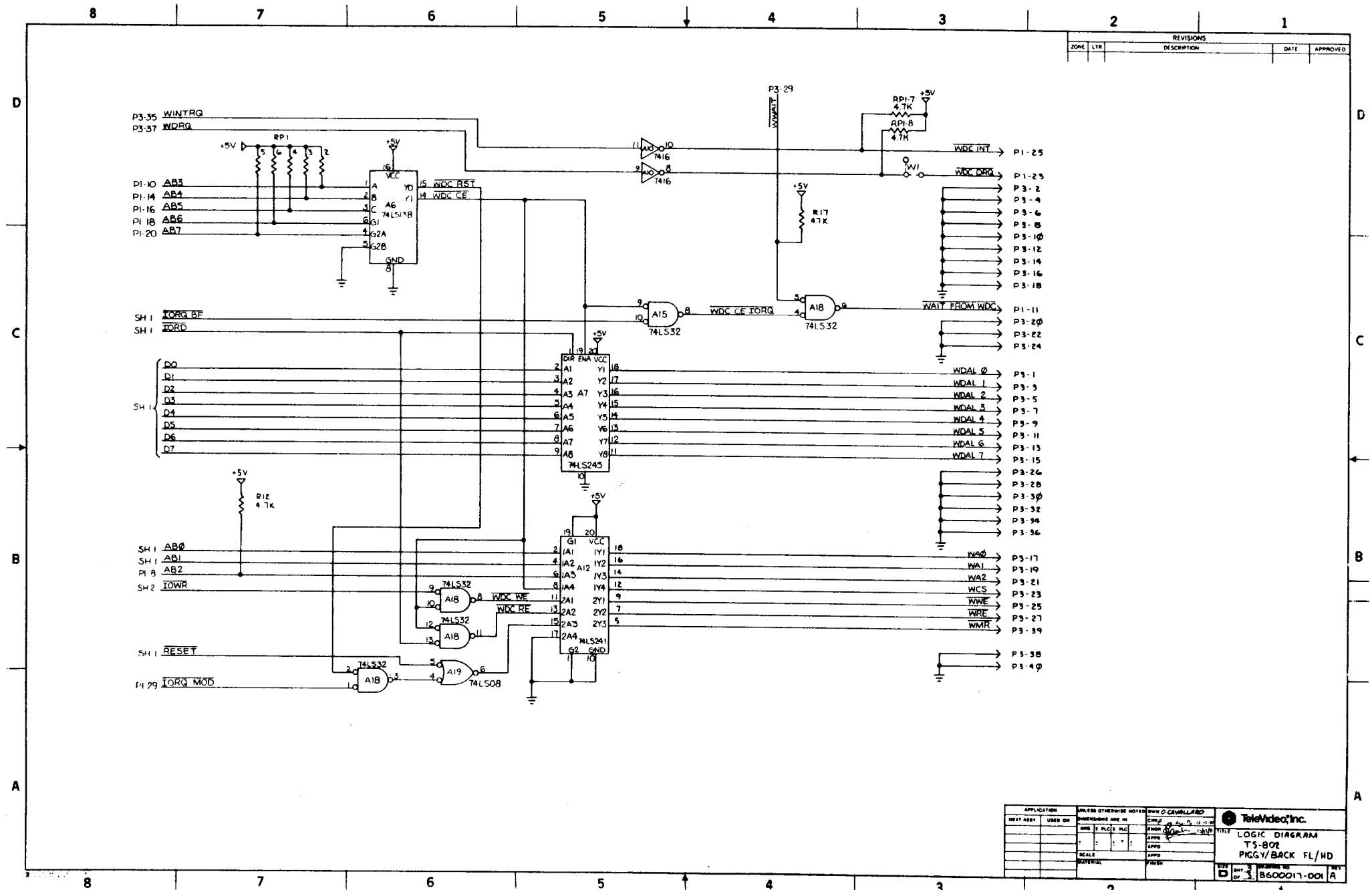
PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
C700100-001	CAP., 22uf 15V	C2,3
C900100-002	CAP., .01uf 50V 10%	UNMARKED
C600100-004	CAP., 100pf 50V 5%	C6,8
C700100-005	CAP., 3.3uf 50V 10%	C5
C900100-008	CAP., 0.1uf 50V 10%	C4,9
C900100-004	CAP., 330pf 100V 20%	C7,10
C700100-002	CAP., .68 uf 50V 10%	C1
I740010-009	IC, 74LS32	A11,15,18
I740010-068	IC, 74LS273	A4
I740010-075	IC, 7416	A5,10
I740010-061	IC, 74LS245	A3,7
I740010-079	IC, FD1793-02	A2
I740010-004	IC, 74LS04	A8
I740010-057	IC, 7414	A9
I740010-095	IC, 74LS123	A16
I740010-078	IC, WD1691	A1
I740010-013	IC, 74LS74	A17
I740010-006	IC, 74LS08	A19
I740010-086	IC, 74LS241	A12
I740010-081	IC, 74LS138	A6
I740010-073	IC, 74S124	A13
I740010-077	IC, WD2143	A14

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A
M200301-003	SOCKET, 40 PIN	A2
M200301-008	SOCKET, 20 PIN	A1
M200301-001	SOCKET, 18 PIN	A14
M200209-007	CONN., HEADER 3 PIN	W1/W3
M200209-005	CONN., HEADER 34 PIN	P2
M200209-004	CONN., HEADER 40 PIN	P1,3
R514000-041	RES. 2K 5% 1/4W	R10
R514000-027	RES. 10K 5% 1/4W	R3,4,12
R514000-031	RES. 100K 5% 1/4W	R5
R514000-025	RES. 47K 5% 1/4W	R2,6
R514000-001	RES. 68ohm 5% 1/4W	R1
R514000-048	RES. 2.7K 5% 1/4W	R9
R514000-029	RES. 33ohm 5% 1/4W	R16
R514000-006	RES. 1K 5% 1/4W	R12,13,15
R514000-011	RES. 4.7K 5% 1/4W	R14,17
R514000-112	RES. PACK 4.7K 8 PIN	RP1
R514000-111	RES. PACK 1K 8 PIN	RP3
R514000-110	RES. PACK 150 ohm 8 PIN	RP2
R514000-100	RES. PACK 1K 10 PIN	RP4
R514001-001	TRIM POT, 50K	R8

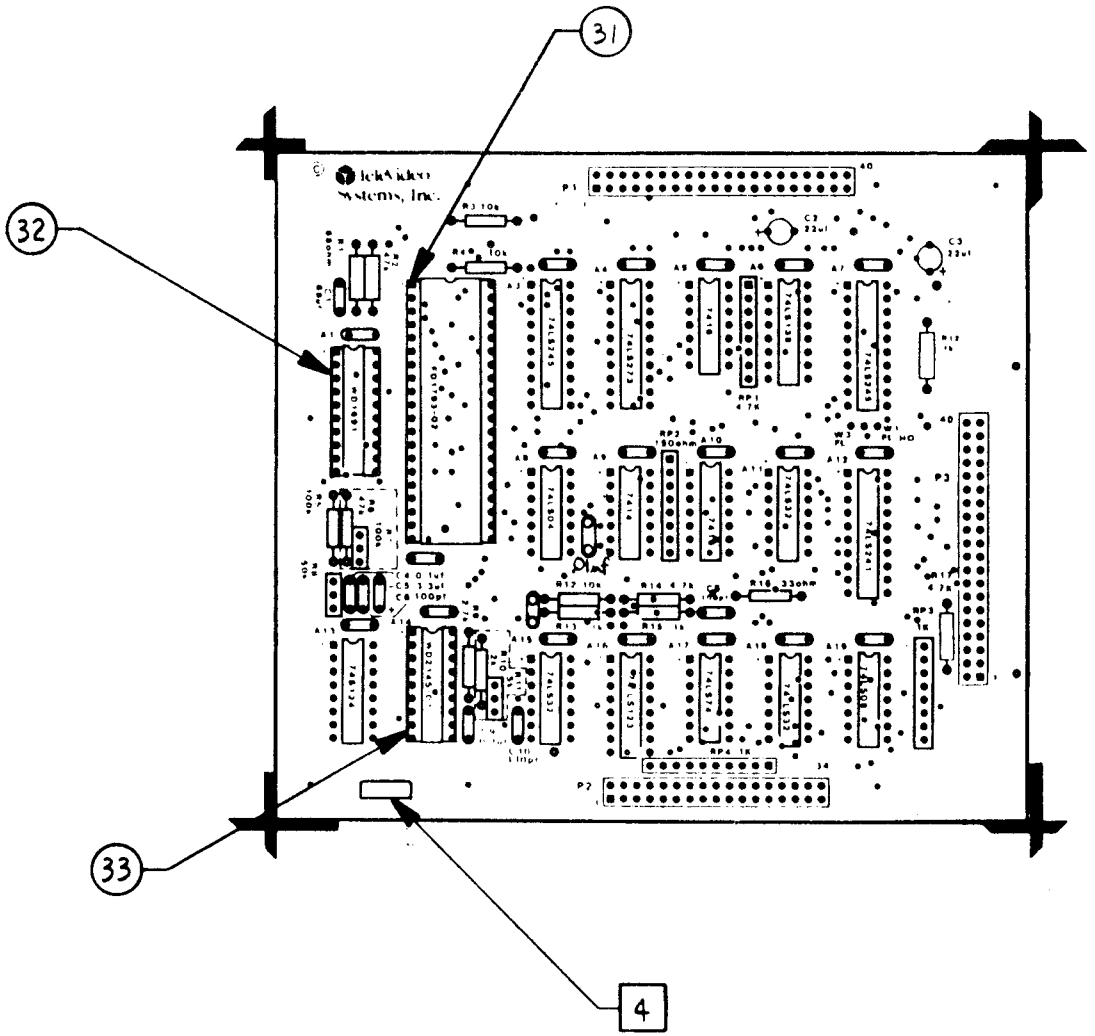
Note: Non-FDC9216 version part list FDC9216 replaces 74S123 and related components



REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A1 | ECO 175 | 1-20-82
A2 | ECO 259
A3 | ECO 260
FDD SELECT
IORQ BF
P1-3 D0
P1-5 D1
P1-7 D2
P1-9 D3
P1-13 D4
P1-15 D5
P1-17 D6
P1-19 D7
IOWR MOD2
P1-28 FDC CE
P1-30 IORD
SH 2 IOWR MOD1
P1-4 AB0
P1-6 AB1
P1-37 1MHZ CLK
SH 2 RCLK
P2-28 WRITE PROTECTED
P2-8 INDEX/SECTOR
P2-26 TRACK 00
P2 30 COMPOSITE READ DATA
P1-33 RESET
RP2- 150 Ω
C10 330pf
A9 7414
A11 74LS32
A15 74LS32
A3 74LS245
A4 74LS273
A5 7416 O.C
A2 FD1793-02
A16 74LS123
A8 74LS04
A10 7416
R13 1K
R14 4.7K
C8 100pf
R12 10K
R4 10K
R3 10K
RP4-5 1K
RP4-4 1K
RP4-2 1K
RP3-6 1K
RP3-5
RP4-9
RP4-8
RP3-4
RP4-10 1K
AB1 SH 3
IORQ BF SH 3
D7 D6 D5 D4 D3 D2 D1 D0 SH 3
AB0 SH 3
DDEN SH 2
MOTOR ON P2-16
SIDE SELECT P2-32
DRIVE SELECT 0 P2-10
DRIVE SELECT 1 P2-12
DRIVE SELECT 2 P2-14
DRIVE SELECT 3 P2-6
FDC DRQ P1-24
FDC INT P1-26
DIRECTION SELECT P2-18
STEP P2-20
WRITE ENABLE P2-24
WF/VFOE LATE EARLY WD TG43 WG SH 2
P2-15 P2-31 P2-9 P2-11 P2-13 P2-5 P2-17 P2-19 P2-23 P2-21
P2-27 P2-7 P2-25 P2-29
SH 2 RESET
SH 3 IORQ
SH 2,3 RESET
SH 2 RAW READ
CHANGE TO 150 PF.
#2 QUESTION.
TeleVideo Inc.
LOGIC DIAGRAM TS-802 PIGGY/BACK PL/ND
O. CAVALLARO
D 1 of 3 B60001-001 A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
P3-35 WINTRQ
P3-37 WDRQ
RP1
+5V
P1-10 AB3
P1-14 AB4
P1-16 AB5
P1-18 AB6
P1-20 AB7
A6 74LS138
WDC RST
WDC CE
7416
P3-29
WAIT
RP1-7 4.7K
RP1-8 4.7K
WDC INT
P1-25
WDC DRQ
P1-23
R17 4.7K
P3-2
P3-4
P3-6
P3-8
P3-10
P3-12
P3-14
P3-16
P3-18
SH1 IORQ BF
SH1 IORD
A15 74LS32
WDC CE IORQ
A18 74LS32
WAIT FROM WDC
P1-11
P3-20
P3-22
P3-24
SH1 D0 D1 D2 D3 D4 D5 D6 D7
A7 74LS245
WDAL 0
WDAL 1
WDAL 2
WDAL 3
WDAL 4
WDAL 5
WDAL 6
WDAL 7
P3-1
P3-3
P3-5
P3-7
P3-9
P3-11
P3-13
P3-15
P3-26
P3-28
P3-30
P3-32
P3-34
P3-36
R12 4.7K
SH1 AB0
SH1 AB1
P1-8 AB2
SH2 IOWR
A12 74LS241
WA0
WA1
WA2
WCS
WWE
WRE
WMR
P3-17
P3-19
P3-21
P3-23
P3-25
P3-27
P3-29
WDC WE
WDC RE
SH1 RESET
P1-29 IORQ MOD
A19 74LS08
P3-38
P3-40
TeleVideo, Inc.
LOGIC DIAGRAM
TS-802
PIGGY/BACK FL/HD
B600017-001
A

REVISIONS			
A1	ECO 175	1-20-82	
A2	ECO 259		



NOTE: UNLESS OTHERWISE SPECIFIED

1. REFER TO SEPARATE PARTS LIST FOR COMPLETE IDENTIFICATION OF REFERENCE DESIGNATION.
2. MADE FROM B800017-001 FAB REV A1
3. COMPLETE HEIGHT OF COMPONENTS NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BD.
4. RUBBER STAMP REV LETTER APPROX. WHERE SHOWN.

B800017-001 1 A1

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

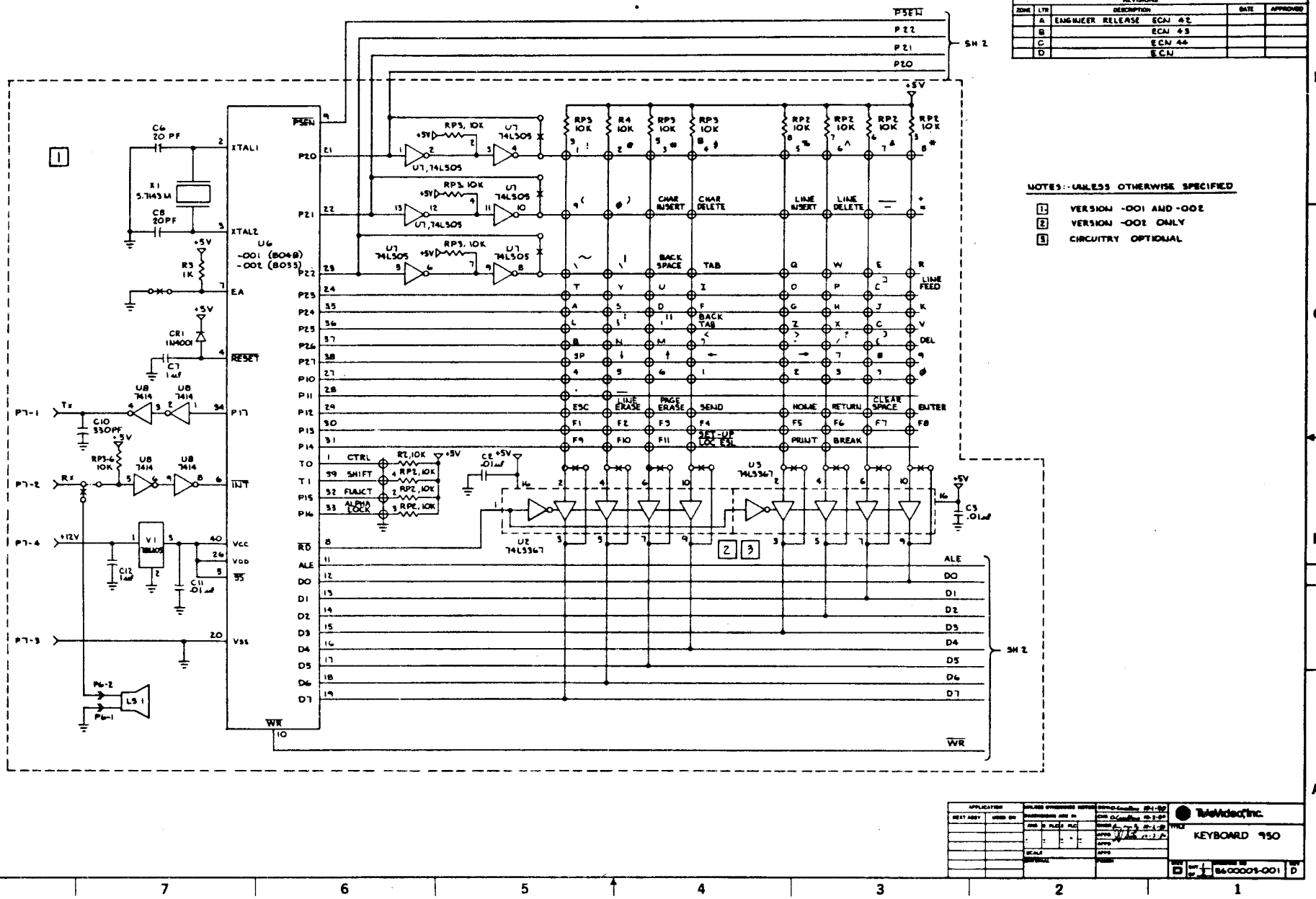
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN

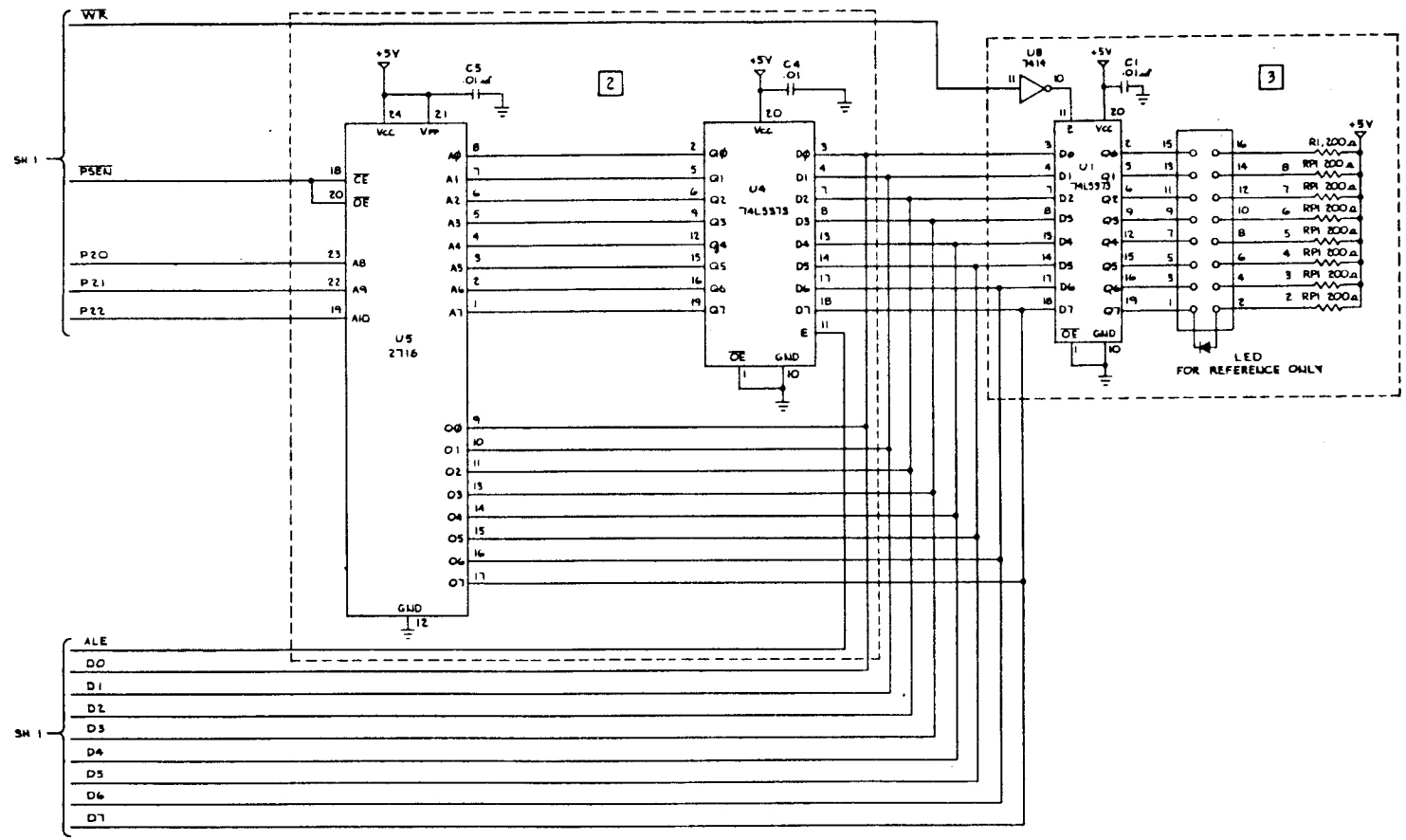
DWN O. CAVALLARO

TeleVideo, Inc.

TITLE ASSEMBLY DWG TS-802 950 FL/HD DAUGHTER BD.

B930017-001 A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A ENGINEER RELEASE ECN 42
B ECN 43
C ECN 44
D ECN
NOTES: UNLESS OTHERWISE SPECIFIED
1 VERSION -001 AND -002
2 VERSION -002 ONLY
3 CIRCUITRY OPTIONAL
U6 -001 (8048) -002 (8035)
U2 74LS367
U3 74LS367
U7 74LS05
RP3, 10K
RP2 10K
R4 10K
RP1, 10K
RP2, 10K
RPE, 10K
R2, 10K
X1 5.7143 M
C6 20 PF
C8 20PF
R3 1K
CR1 1N4001
C7 1 uf
C10 330PF
C12 1 uf
C11 .01 uf
C2 .01 uf
C3 .01 uf
U8 7414
RP3-6 10K
V1 78L05
LS1
SH 2
PSEN
P22
P21
P20
XTAL1
XTAL2
EA
RESET
P17
INT
Vcc
VDD
Vss
WR
RD
ALE
DO
D1
D2
D3
D4
D5
D6
D7
CTRL
SHIFT
FLAUCT
ALPHA LOCK
CHAR INSERT
CHAR DELETE
LINE INSERT
LINE DELETE
BACK SPACE
TAB
BACK TAB
LINE FEED
DEL
ESC
LINE ERASE
PAGE ERASE
SEND
SET-UP LOC ESL
HOME
RETURN
CLEAR SPACE
ENTER
PRINT
BREAK
TeleVideo, Inc.
KEYBOARD 950
B4000001-001
D



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE

TITLE	KEY BOARD 950
DWG NO	840000S-001
REV	D
SHT	2 OF 2

TeleVideo, Inc.

Part Number	Description	Locations REV A			
C600100-005	CAP, DIP MICA 47 pf 50V 5%	C13			
C600100-006	CAP, DIP MICA 150 pf 500V 1%	C4			
C600100-008	CAP, DIP MICA 390 pf 500V 5%	C12			
C700100-009	CAP, R/L, ELECTRO 10 uf 25V 10%	C1,2,10,16,72			
C700100-014	CAP, R/L, ELECTRO .0068 uf 100V 5%	C5			
C700100-015	CAP, R/L, ELECTRO 2.2 uf 25V 10%	C68			
C900100-006	CAP, CERAMIC 22 pf 1KV 20%	C14			
C900100-007	CAP, CERAMIC 68 pf 1KV 20%	C15,17			
C900100-008	CAP, CERAMIC 0.1 uf 50V 10%	SEE NOTE			
I740010-000	IC 74S00	U2			
I740010-003	IC 74S04	U38			
I740010-006	IC 74LS08	U25			
I740010-009	IC 74LS32	U44			
I740010-012	IC 74S74	U3,5,7,8,9,			
		13,17			
I740010-013	IC 74LS74	U32			
I740010-021	IC 74LS174	U34,48			

Part Number	Description	Locations REV A			
I740010-025	IC 74LS374	U42,43			
I740010-054	IC 7406	U6			
I740010-063	IC 74LS191	U40,45,46			
I740010-068	IC 74LS273	U52			
I740010-070	IC 74LS175	U21			
I740010-085	IC 74S02	U24			
I740010-088	IC AM26LS31	U16			
I740010-089	IC AM 26LS32	U15			
I740010-094	IC 7438	U54,55,56			
I740010-097	IC 74LS244	U36			
I740010-099	IC 74S174	U27			
I740010-100	IC 74S138	U20,26			
I740010-101	IC 74S86	U11			
I740010-102	IC 74S64	U23			
I740010-103	IC 74LS54	U22			
I740010-104	IC 74S51	U18			
I740010-105	IC 74LS14	U31			

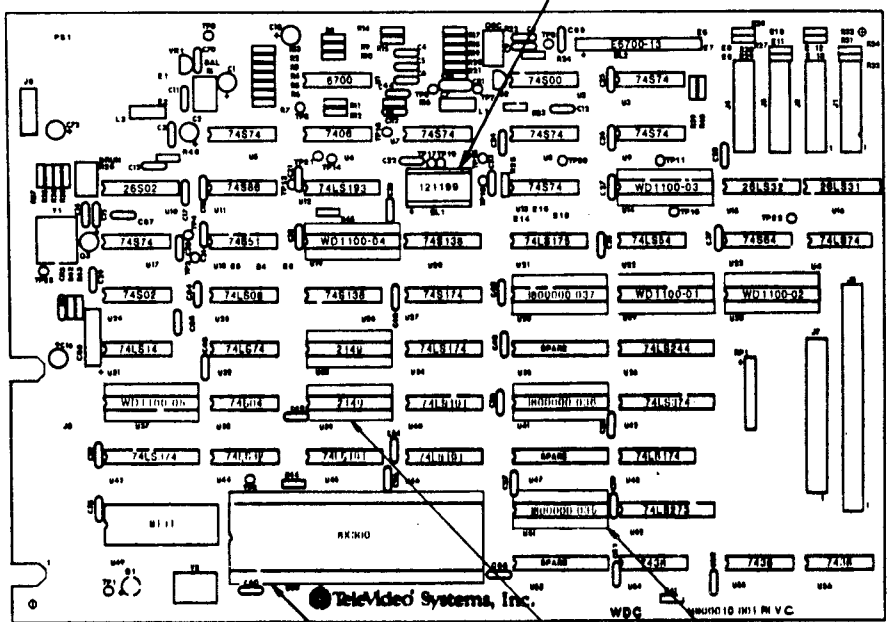
Part Number	Description	Locations REV A			
I740010-107	IC DIGITAL DELAY MODULE	DL1			
I740010-108	IC 74LS193	U12			
I740010-110	IC 96S02/26S02	U10			
I740011-015	IC 8 X 300 MICRO CONTROLLER	U50			
I740011-016	IC 8-BIT BIDIRECTIONAL 8T31	U49			
I740011-022	IC 2149 H/HL	U33,39			
I740012-001	IC PARALLEL CONVERTOR WD1100-01	U29			
I740012-002	IC MFM CONVERTOR WD1100-02	U30			
I740012-003	IC AM DETECTOR WD1100-03	U14			
I740012-004	IC CRC GENERATOR/CHECKER WD1100-04	U19			
I740012-005	IC PARALLEL/SERIAL CONVERTOR WD1100-05	U37			
I740012-006	IC DELAYLINE S/P (60 ns)	DL2			
I800000-028	IC PROG. PROM (L26)	U51			
I800000-029	IC PROG. PROM (FX6)	U28			
I800000-030	IC PROG. PROM (MX6)	U41			
M200209-005	CONN. UNPRO. 34 PIN ST. HEAD	J7			
M200209-006	CONN. UNPRO. 20 PIN ST. HEAD	J1-J4			

Part Number	Description	Locations REV A			
M200301-001	IC SOCKET 18 PIN 640359-3	U33,39			
M200301-008	IC SOCKET 20 PIN	U14,19,28-30, 37,41,51			
M200302-001	IC SOCKET 50 PIN	U50			
M200401-004	CRYSTAL - 8.0000 MHz	Y2			
M200401-005	CRYSTAL-20.000 MHz	Y1			
M200602-001	3 PIN WAFER	J6			
R514000-002	RES. 270 5% ¼W	R37			
R514000-003	RES. 330 5% ¼W	R15,16,17,36			
R514000-006	RES. 1K 5% ¼W	R18,24,25,41			
R514000-011	RES. 4.7K 5% ¼W	R43,46			
R514000-017	RES. 100K 5% ¼W	R19			
R514000-026	RES. 150 5% ¼W	R40			
R514000-027	RES. 10K 5% ¼W	R42, 44			
R514000-028	RES. 200 5% ¼W	R45			
R514000-031	RES. 100 1% ¼W	R4,7,21			
R514000-032	RES. 1.5K 1% ¼W	R3,9			
R514000-033	RES. 3.92K 1% ¼W	R8,12			

Part Number	Description	Locations REV A			
R514000-034	RES. 511 1% ¼W	R6,13			
R514000-035	RES. 8.25K 1% ¼W	R10,11			
R514000-036	RES. 1.30K, 1% ¼W	R2, 5			
R514000-036	RES. 51 5% ¼W	R27-34			
R514000-039	RES. 240 5% ¼W	R39			
R514000-041	RES. 2000 5% ¼W	R20			
R514000-042	RES. 680 5% ¼W	R14			
R514000-043	RES. 27K 5% ¼W	R35,38			
R514000-044	RES. 560 5% ¼W	R23			
R514000-109	RES. PACK 220/330 (SIP) 8 PIN	RP1			
R514001-003	POT, 200	R1			
R514001-004	POT, 2K	R22			
R514001-005	POT, 10K	R26			
R60000-002	VOLT REG 79L05AC	VR1			
R700001-001	INDUCTOR 3.30 UH	L1			
R700001-002	INDUCTOR 4.70 UH R.F. COIL 93T0-28	L2			
S350100-006	TRANS, 2N 3904	Q2			

Part Number	Description	Locations REV A			
S350100-003	TRANS, 2N2907A	Q3			
S350100-004	TRANS, ARRAY-TWO NPN/TWO PNP (6700)	U1			
S350100-005	TRANS, 2N5320	Q1			
S360100-004	DIODE, TUNING MV 1404	CR1			
S360100-005	DIODE, SWITCH IN 4148	CR2-3			

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	D	ECO 138	12 OCT 81	CRB 5/1m
	E	ECO 146	18 Nov 81	CRB 5/1m
	E1	ECO 219		
	E2	ECO 278, 280	25 Apr 82	



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFER TO SEPARATE PARTS LIST FOR COMPLETE IDENTIFICATION OF REFERENCE DESIGNATION.
2. MADE FROM B800010-001 REV B FAB.
3. COMPONENT HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
4. REFER TO B700010-001 REV C FOR COMPLETE PRINTED CIRCUIT ARTWORK.

QTY REQD	ITEM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN

ANG	0 PLC	3 PLC
±	±	±

SCALE: 1:1

MATERIAL

DWN Sunny 10-9-81
CHK
ENGR
APPD
APPD MH 9/16/81
APPD

FINISH

TeleVideo, Inc.

TITLE: PCB ASSY DWG WDC

SIZE C | SHT 1 OF 1 | DRAWING NO. B030010-001 | REV E

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MNEMONIC	MEANING
AMDET	ADDRESS MARK DETECT
A2-AØ	TASK FILE ADDRESS SELECT BITS 2-Ø
BIC	BUS INPUT CONTROL
BOC	BUS OUTPUT CONTROL
CLKS	CLOCK DATA
CRCIZ	CYCLIC REDUNDANCY CHECK WORD INITIALIZE
CROK	CRC OKAY
CS	CARD SELECT
CSAC	CARD SELECT ACCESS CONTROL
DAL7-DALØ	DATA ACCESS LINE
-DIRECTION IN	DIRECTION CONTROL
DHOLD	DATA HOLD
DLYDAT	DELAYED DATA
DRQ	DATA REQUEST
DRQCLK	DATA REQUEST CLOCK
DRSEL	DRIVE SELECT
DRS4-DRS1	DRIVE SELECT BITS 4-1
DRUN	DATA RUN
HFRQ	HIGH FREQUENCY
HSAC	HOST SELECT ACCESS CONTROL
HS2-HSØ	HEAD SELECT BITS 2-Ø
IA9-IAØ	INSTRUCTION ADDRESS LINES BITS 9-Ø
ID15-IDØ	INSTRUCTION DATA BITS 15-Ø
-INDEX	INDEX PULSE FROM DRIVE
INTCLK	INTERRUPT CLOCK
INTRQ	INTERRUPT REQUEST
IO7-IOØ	I/O LINES 7-Ø
IVBØ-IVB7	INPUT VECTOR BUS BITS Ø-7
MCLK	MASTER CLOCK
MFMW	MODIFIED FREQUENCY MODULATION WRITE STREAM
MR	MASTER RESET
OSC	OSCILLATOR OUTPUT
RA9-RAØ	RAM ADDRESS BITS 9-Ø
RCLK	READ CLOCK
RCS	RAM CHIP SELECT
RDAT	READ DATA
RD6-RD4 RD2 RDØ	READ CONTROL LINES
RE	READ ENABLE
-READY	READY STATUS FROM DRIVE
RESET	RESET SIGNAL
RGATE	READ GATE
ROVF	RAM OVERFLOW
RWC	REDUCE WRITE CURRENT

MNEMONIC	MEANING
-SEEK COMPLETE	SEEK COMPLETE STATUS FROM DRIVE
SRCH	SEARCH
-STEP PULSE	STEP PULSE TO DRIVE
TIMCLK	TIMING CLOCK FOR SA1000
TRACK ØØØ	TRACK ØØØ STATUS FROM DRIVE
WAEN	WAIT ENABLE
WAIT	MEMORY NOT READY SIGNAL
WCLK	WRITE CLOCK
WE	WRITE ENABLE
WGI	WRITE GATE INTERNAL
-WRITE FAULT	WRITE FAULT STATUS FROM DRIVE
WR7-WRØ	WRITE CONTROL LINES
1BLA	1 BYTE LOOK AHEAD
2XDR	2 x DATA REFERENCE CLOCK

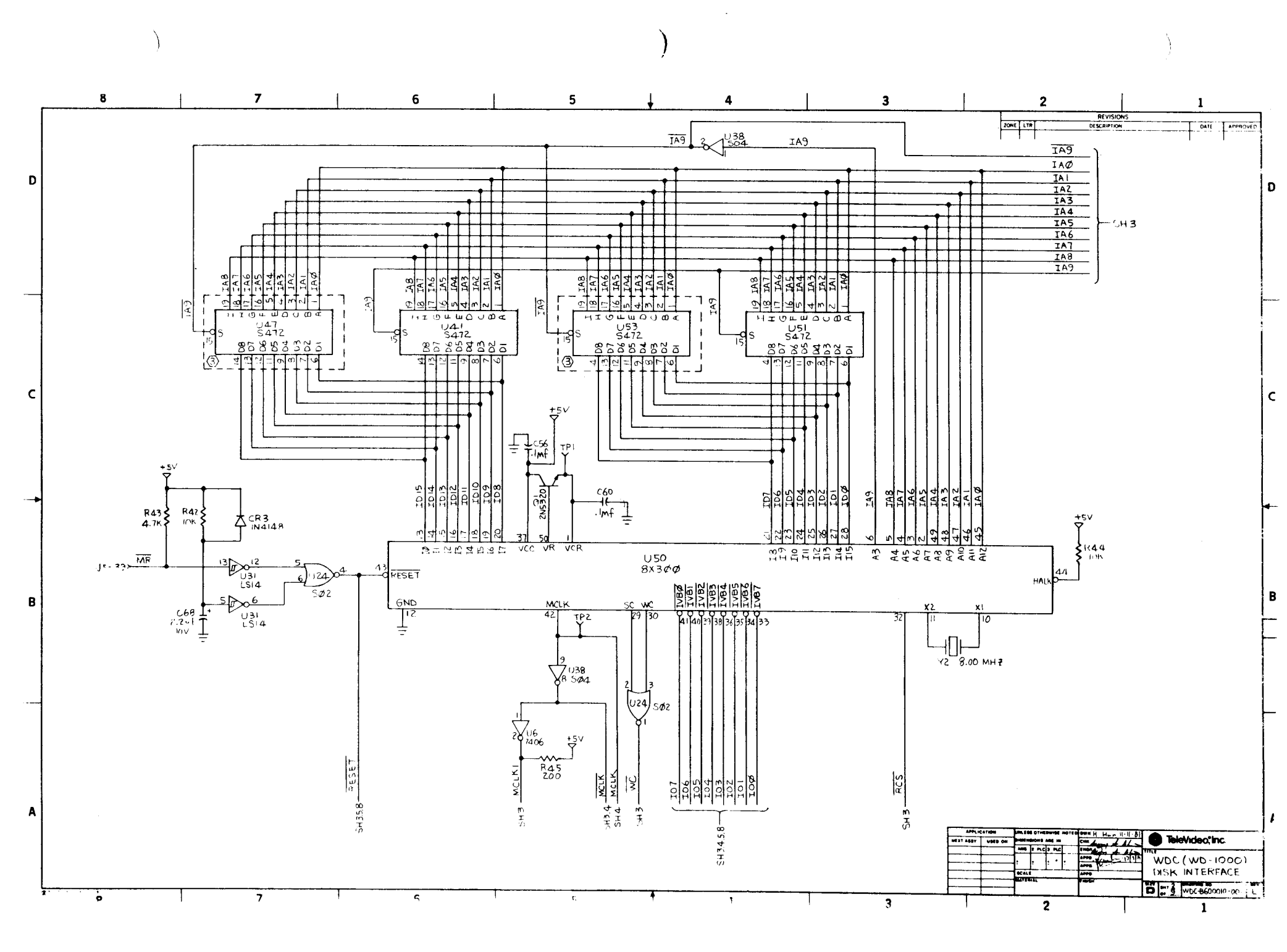
NOTES: UNLESS OTHERWISE SPECIFIED

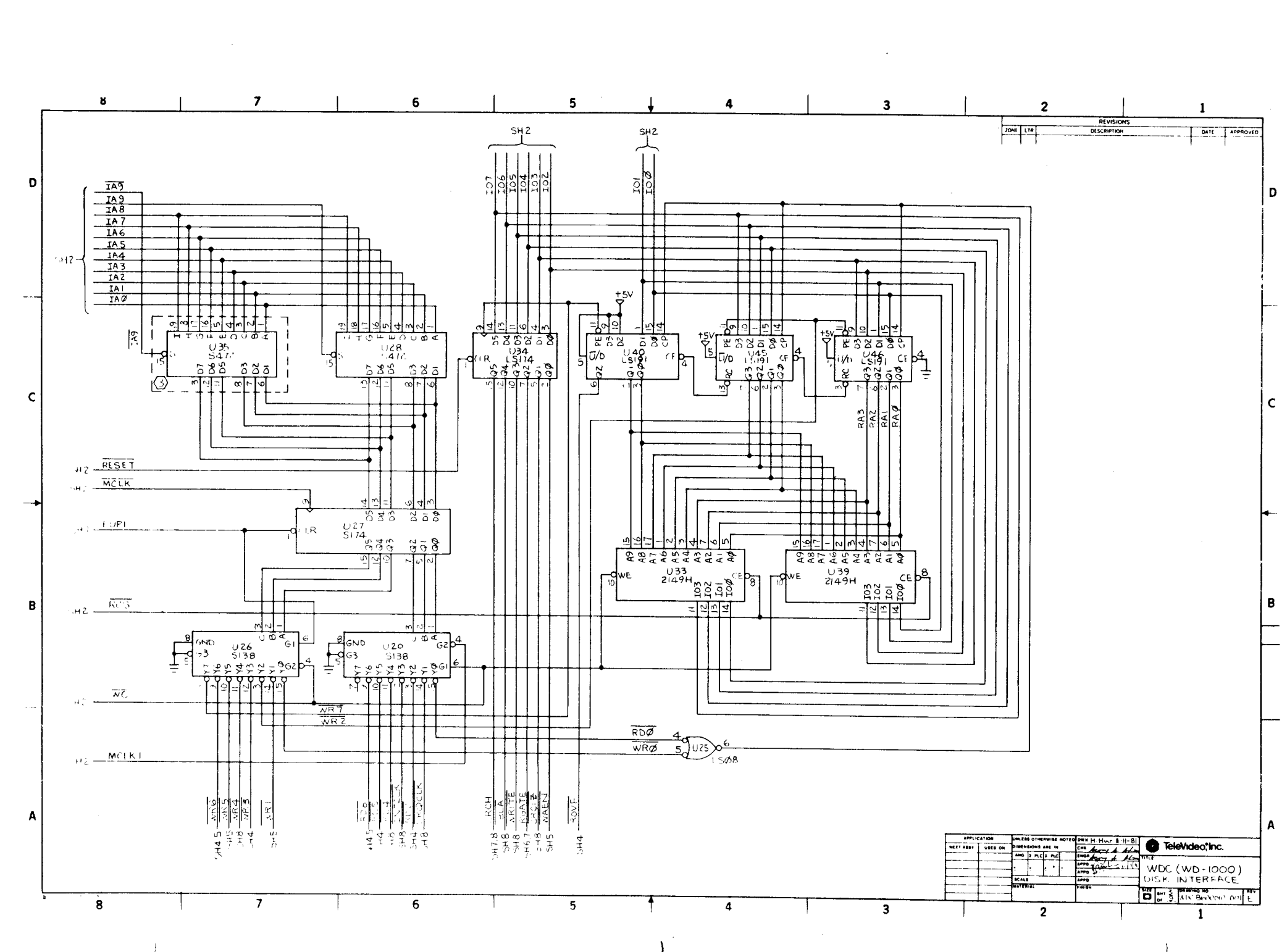
1. RESISTOR VALUES ARE IN OHMS ±5% .1/4 W
2. JUMPER E5 TO E4 TO QUALIFY WAIT BY CS
   JUMPER E3 TO E4 IF BIC-BOC TO QUALIFY WAIT
3. NOT USED, USED ONLY WHEN FOR EXPANDING MEMORY TO 1K.
4. JUMPER E14 TO E16 AND CUT TRACE TO E15 TO ACCOMODATE - 4002, 1 PART IN U30.
5. NOT USED FOR 5 1/4 DRIVE.

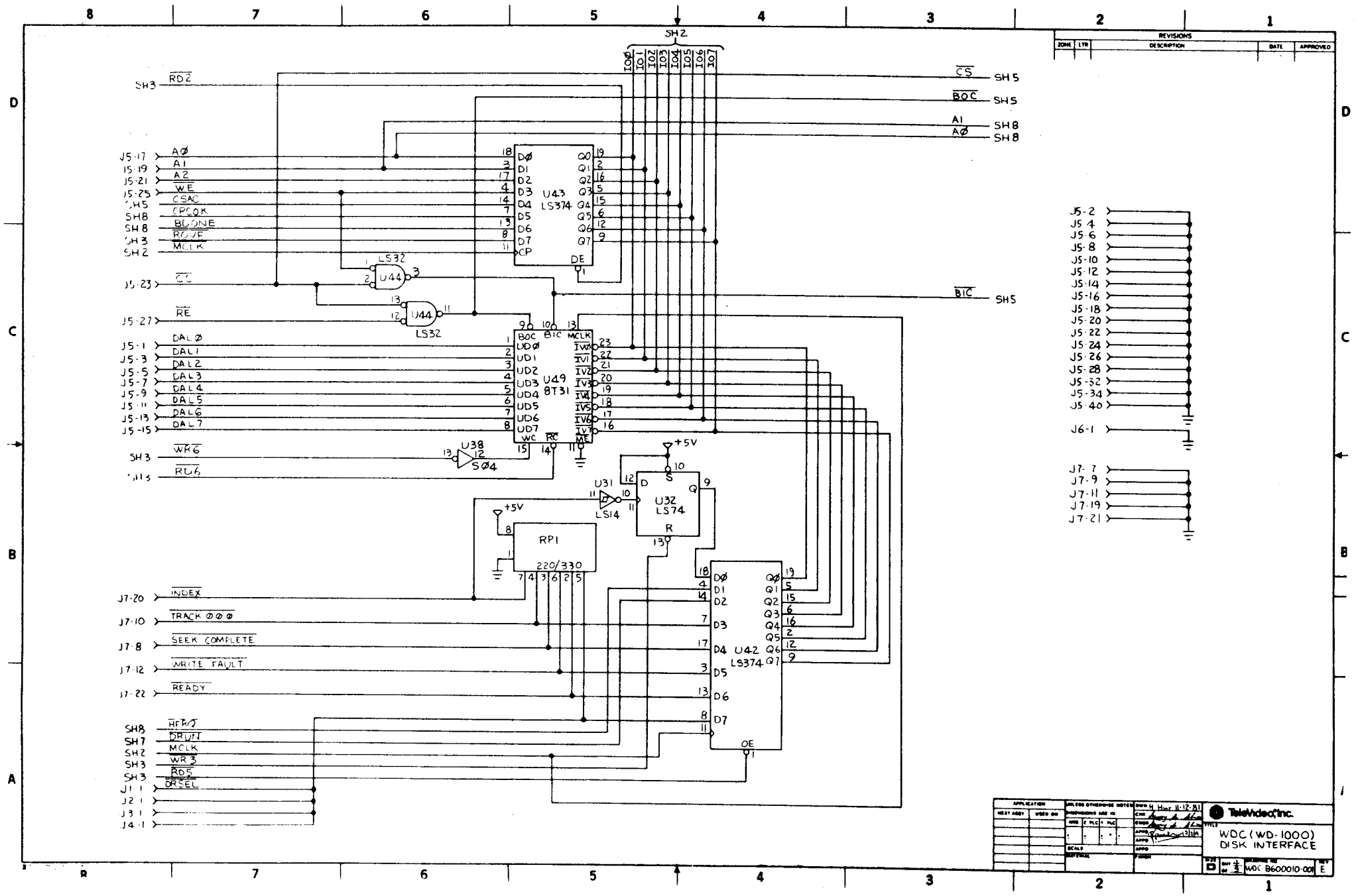
TeleVideo, Inc.

WDC (WD-1000) DISK INTERFACE

B | WDC-860010-001 | E


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
U38 S04
U47 S472
U41 S472
U53 S472
U51 S472
U50 8X30Ø
U31 LS14
U24 SØ2
U6 7406
U38 B SØ4
R43 4.7K
R42 10K
CR3 IN4148
C68 22uf 10V
C56 .1 mf
C60 .1 mf
Q1 2N5320
TP1
TP2
R44 10K
R45 200
Y2 8.00 MHz
RESET
MR
MCLK
WC
RCS
HALT
GND
+5V
SH3
SH4
SH3,4
SH3&8
SH3458
TeleVideo, Inc.
WDC (WD-1000) DISK INTERFACE
WDC-B600010-00


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SH2
IA9
IA8
IA7
IA6
IA5
IA4
IA3
IA2
IA1
IA0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
+5V
U36 S241
U28 S241
U34 S174
U40 S191
U45 S191
U46 S191
RA3
RA2
RA1
RA0
RESET
MCLK
EUPI
U27 S174
U33 2149H
U39 2149H
WE
CE
RDS
U26 S138
U20 S138
WR1
WR2
RDØ
WRØ
U25 1S00
MCLK1
WR1
WR2
RCH
ARATE
RCLK
WAEN
ROVF
TeleVideo, Inc.
WDC (WD-1000) DISK INTERFACE


REVISIONS
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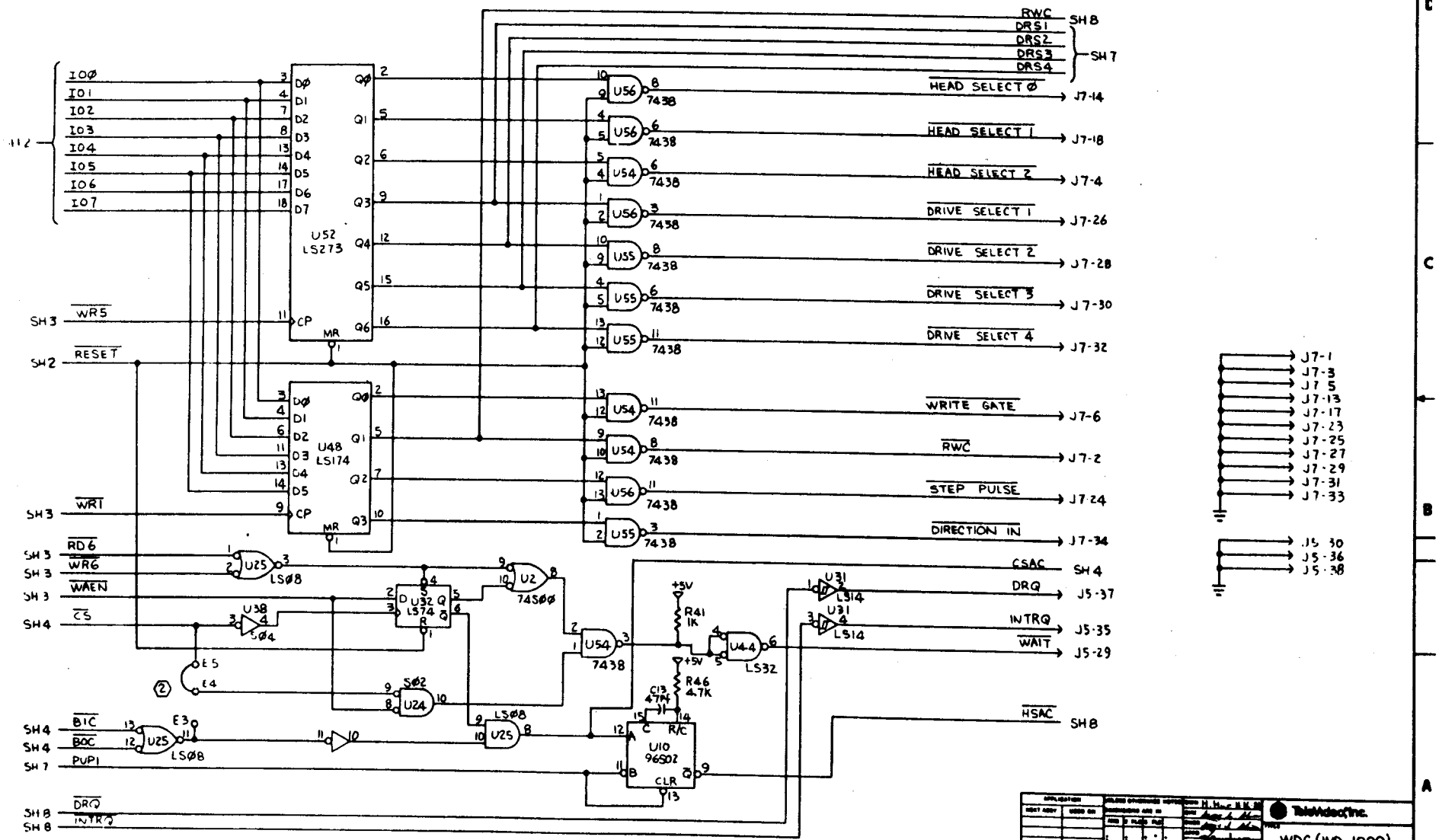
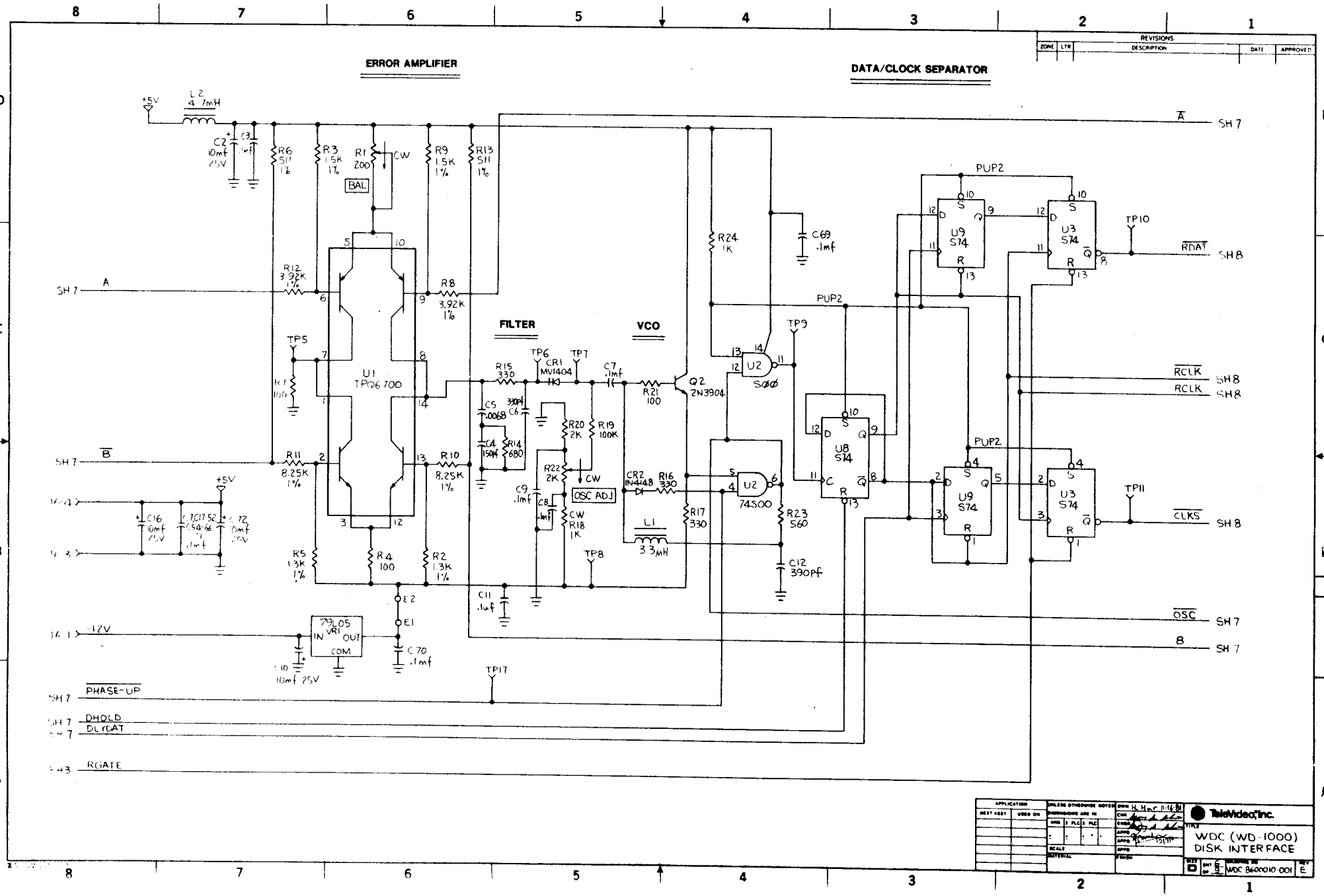
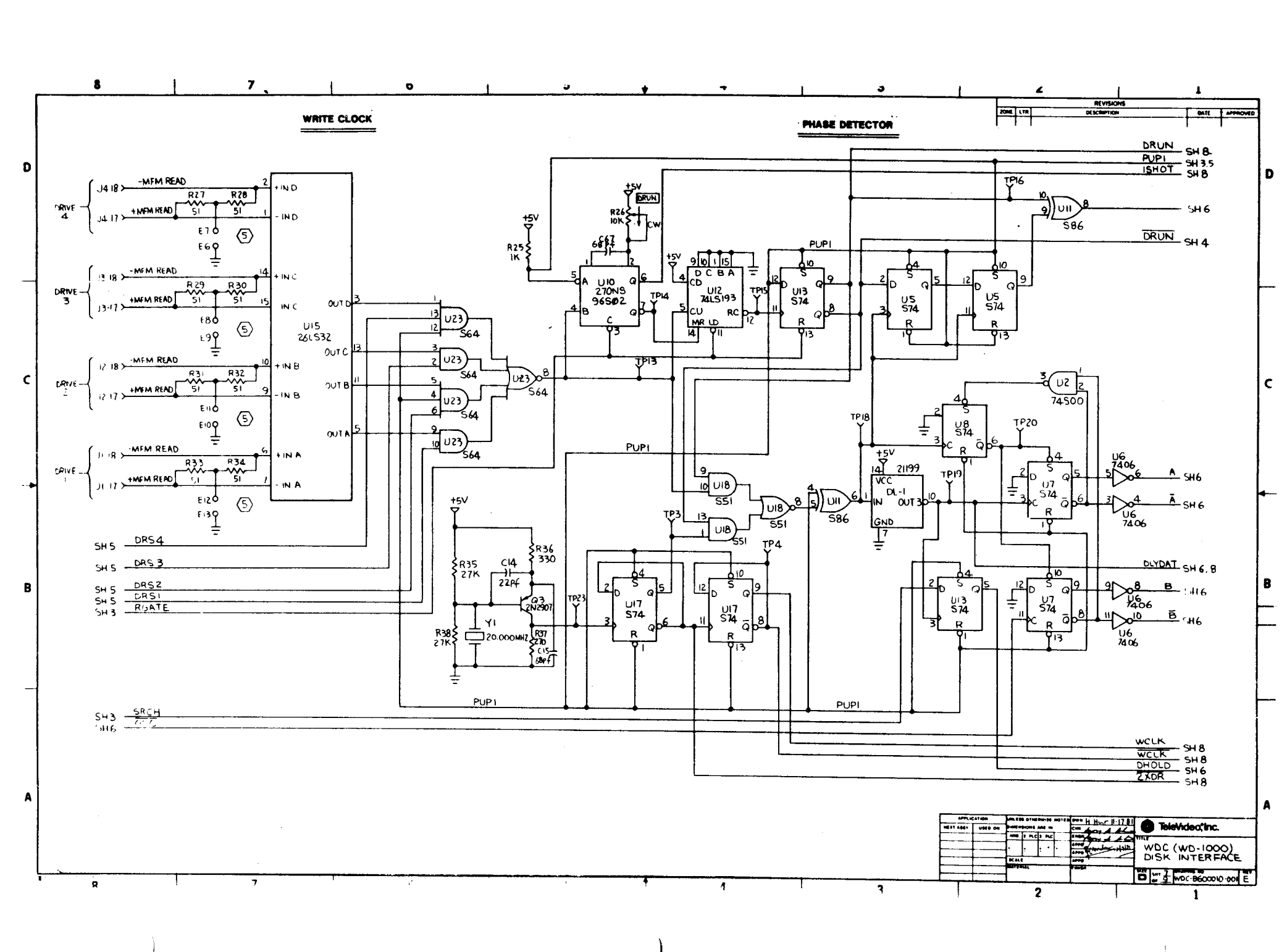
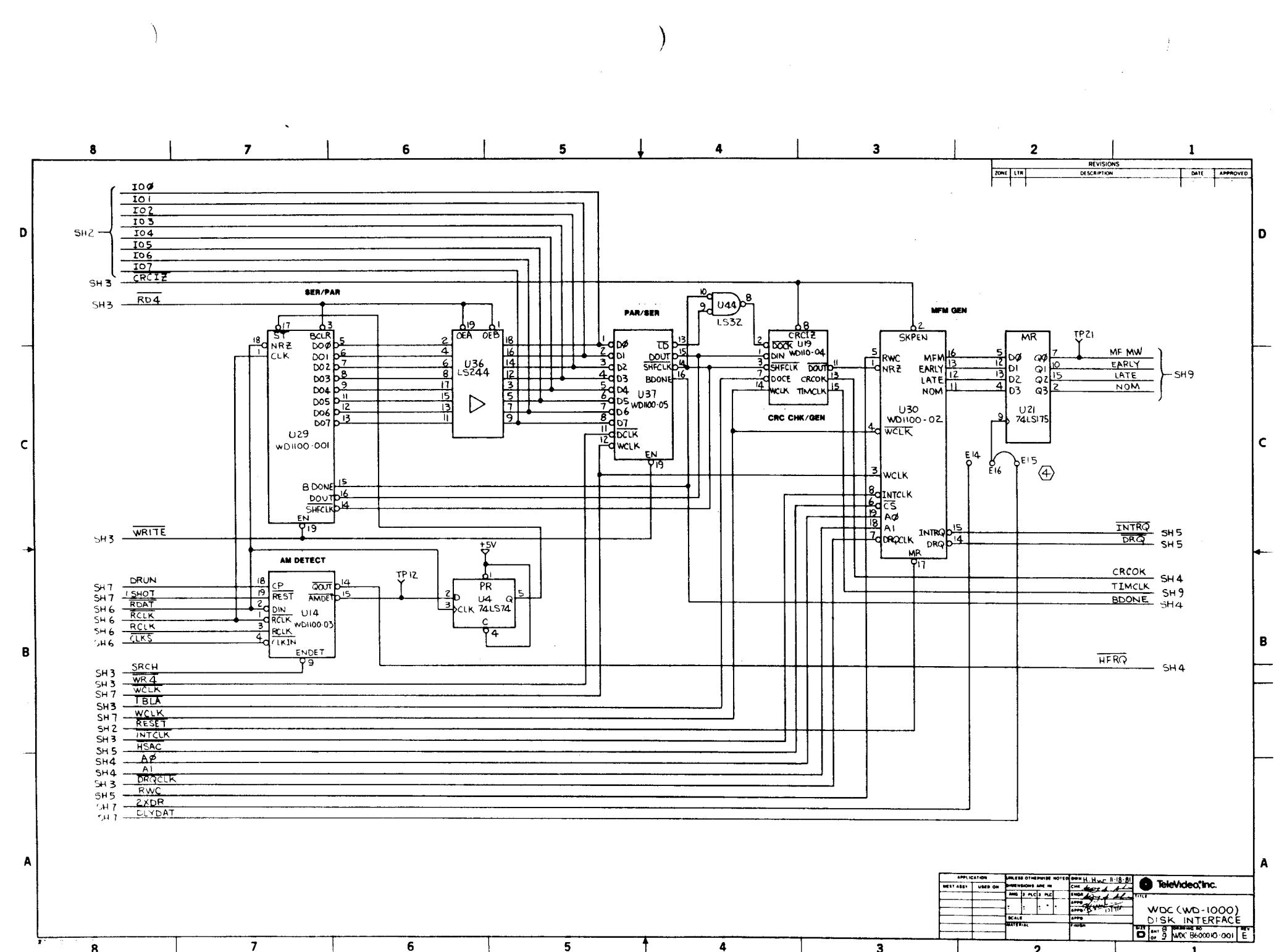
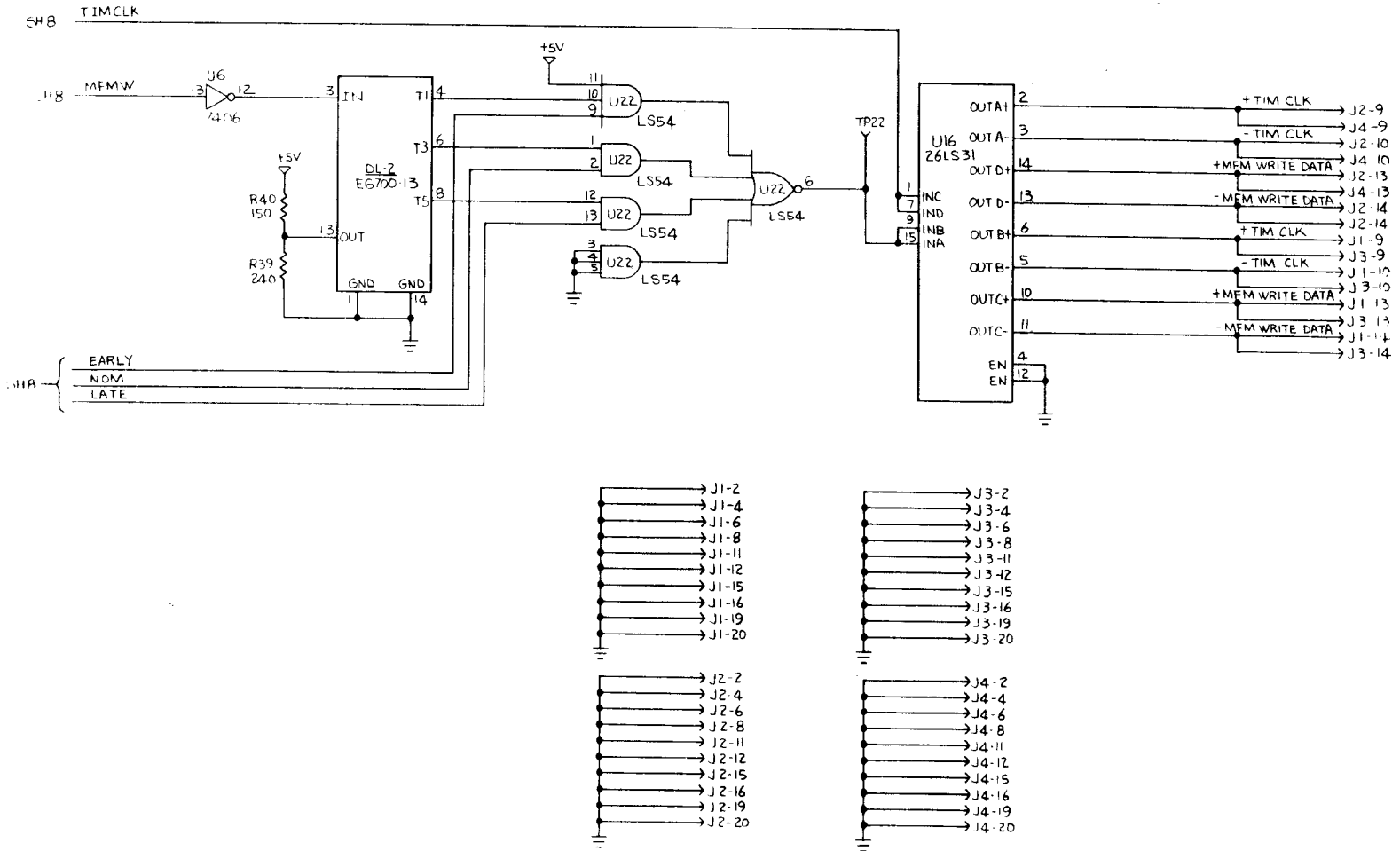
SH2
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
SH3 RD2
CS SH5
BOC SH5
A1 SH8
AØ SH8
BIC SH5
U43 LS374
U44 LS32
U49 8T31
U38 SØ4
U31 LS14
U32 LS74
U42 LS374
RP1 220/330
+5V
J5-17 AØ
J5-19 A1
J5-21 A2
J5-25 WE
J5-23 CS
J5-27 RE
SH5 CSAC
SH8 CPCOK
SH8 BCONE
SH3 ROVF
SH2 MCLK
J5-1 DALØ
J5-3 DAL1
J5-5 DAL2
J5-7 DAL3
J5-9 DAL4
J5-11 DAL5
J5-13 DAL6
J5-15 DAL7
SH3 WR6
SH3 RD6
J5-2 J5-4 J5-6 J5-8 J5-10 J5-12 J5-14 J5-16 J5-18 J5-20 J5-22 J5-24 J5-26 J5-28 J5-32 J5-34 J5-40
J6-1
J7-7 J7-9 J7-11 J7-19 J7-21
J7-20 INDEX
J7-10 TRACK ØØØ
J7-8 SEEK COMPLETE
J7-12 WRITE FAULT
J7-22 READY
SH8 HFRST
SH7 DRUN
SH2 MCLK
SH3 WR3
SH3 RD5
SH3 DRSEL
J1-1 J2-1 J3-1 J4-1
TeleVideo, Inc.
WDC (WD-1000) DISK INTERFACE
WDC B600010-001 E


IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
U52
LS273
SH3 WR5
SH2 RESET
U48
LS174
SH3 WRT
SH3 RD6
SH3 WR6
SH3 WAEN
SH4 CS
U25
LS08
U38
S04
U32
LS74
U2
74S00
U24
S02
U54
7438
R41
1K
+5V
U44
LS32
U31
LS14
R46
4.7K
C13
47PF
U10
96S02
SH4 BIC
SH4 BOC
SH7 PUPI
SH8 DRQ
SH8 INTRQ
RWC
DRS1
DRS2
DRS3
DRS4
SH8
SH7
U56
U55
HEAD SELECT 0
HEAD SELECT 1
HEAD SELECT 2
DRIVE SELECT 1
DRIVE SELECT 2
DRIVE SELECT 3
DRIVE SELECT 4
WRITE GATE
RWC
STEP PULSE
DIRECTION IN
J7-14
J7-18
J7-4
J7-26
J7-28
J7-30
J7-32
J7-6
J7-2
J7-24
J7-34
J7-1
J7-3
J7 5
J7-13
J7-17
J7-23
J7-25
J7-27
J7-29
J7-31
J7-33
J5-30
J5-36
J5-38
CSAC
DRQ
INTRQ
WAIT
HSAC
SH4
J5-37
J5-35
J5-29
SH8
WDC (WD-1000)
DISK INTERFACE
WDC-9600010-001


ERROR AMPLIFIER
DATA/CLOCK SEPARATOR
FILTER
VCO
+5V
L2 4.7mH
C2 10mf 25V
C3 .1mf
R6 511 1%
R3 1.5K 1%
R1 200
CW
BAL
R9 1.5K 1%
R13 511 1%
R12 3.92K 1%
R8 3.92K 1%
U1 TPQ6700
TP5
R7 100
R11 8.25K 1%
R10 8.25K 1%
R5 1.3K 1%
R4 100
R2 1.3K 1%
C5 .0068
C6 330pf
C4 150pf
R14 680
C1 .1mf
C16 10mf 25V
C72 10mf 25V
C70 .1mf
C10 10mf 25V
79L05 IN VR1 OUT COM
E2
E1
TP6
CR1 MV1404
TP7
R15 330
C7 .1mf
R20 2K
R19 100K
R22 2K
CW
OSC ADJ
C9 .1mf
C8 .1mf
CW R18 1K
C11 .1uf
TP8
TP17
Q2 2N3904
R21 100
CR2 IN4148
R16 330
L1 3.3mH
R17 330
R24 1K
C69 .1mf
U2 S00
U2 74S00
R23 560
C12 390pf
TP9
PUP2
U8 S74
U9 S74
U3 S74
TP10
TP11
A
B
RDAT
RCLK
CLKS
OSC
SH 7
SH 8
PHASE-UP
DHOLD
DLYDAT
RGATE
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
TeleVideo, Inc.
WDC (WD-1000) DISK INTERFACE
WDC B600010-001
REV E


WRITE CLOCK
PHASE DETECTOR
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
DRIVE 4
DRIVE 3
DRIVE 2
DRIVE 1
-MFM READ
+MFM READ
R27 51
R28 51
R29 51
R30 51
R31 51
R32 51
R33 51
R34 51
U15 26LS32
+IN D
-IN D
+IN C
-IN C
+IN B
-IN B
+IN A
-IN A
OUT D
OUT C
OUT B
OUT A
U23 S64
DRS4
DRS3
DRS2
DRS1
R/DATE
SRCH
+5V
R25 1K
R26 10K CW
C67 68pf
U10 270NS 96S02
U12 74LS193
U13 S74
U5 S74
U11 S86
TP13
TP14
TP15
TP16
PUP1
DRUN
SH 8
SH 3.5
ISHOT
SH 6
DRUN
SH 4
U2 74S00
U8 S74
TP18
TP19
TP20
21199 DL-1
VCC
IN
OUT 3
GND
U18 S51
U7 S74
U6 7406
A
SH 6
SH 6
DLYDAT
SH 6, 8
B
SH 6
SH 6
R35 27K
C14 22pf
R36 330
Q3 2N2907
Y1 20.000MHZ
R37 270
C15 68pf
R38 27K
TP3
TP4
TP23
U17 S74
WCLK
SH 8
WCLK
SH 8
DHOLD
SH 6
2XDR
SH 8
TeleVideo, Inc.
WDC (WD-1000) DISK INTERFACE
WDC-8600010-004
E


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
IO Ø
IO 1
IO 2
IO 3
IO 4
IO 5
IO 6
IO 7
SH2
SH3
CRCIZ
SH3
RD4
SER/PAR
U29
WD1100-001
U36
LS244
PAR/SER
U37
WD1100-05
U44
LS32
CRCIZ
WD1100-04
CRC CHK/GEN
MFM GEN
SKPEN
U30
WD1100-02
MR
U21
74LS175
TP21
MF MW
EARLY
LATE
NOM
SH9
E14
E15
E16
4
SH3
WRITE
AM DETECT
U14
WD1100-03
TP12
+5V
PR
U4
74LS74
SH7
DRUN
SH7
1 SHOT
SH6
RDAT
SH6
RCLK
SH6
RCLK
SH6
CLKS
INTRQ
DRQ
SH5
SH5
CRCOK
SH4
TIMCLK
SH9
BDONE
SH4
HFRQ
SH4
SH3
SRCH
SH3
WR4
SH7
WCLK
SH3
TBLA
SH7
WCLK
SH2
RESET
SH3
INTCLK
SH5
HSAC
SH4
AØ
SH4
A1
SH3
DRQCLK
SH5
RWC
SH7
2XDR
SH7
CLYDAT
TeleVideo, Inc.
WDC (WD-1000)
DISK INTERFACE
WDC 8600010-001
E



REVISIONS

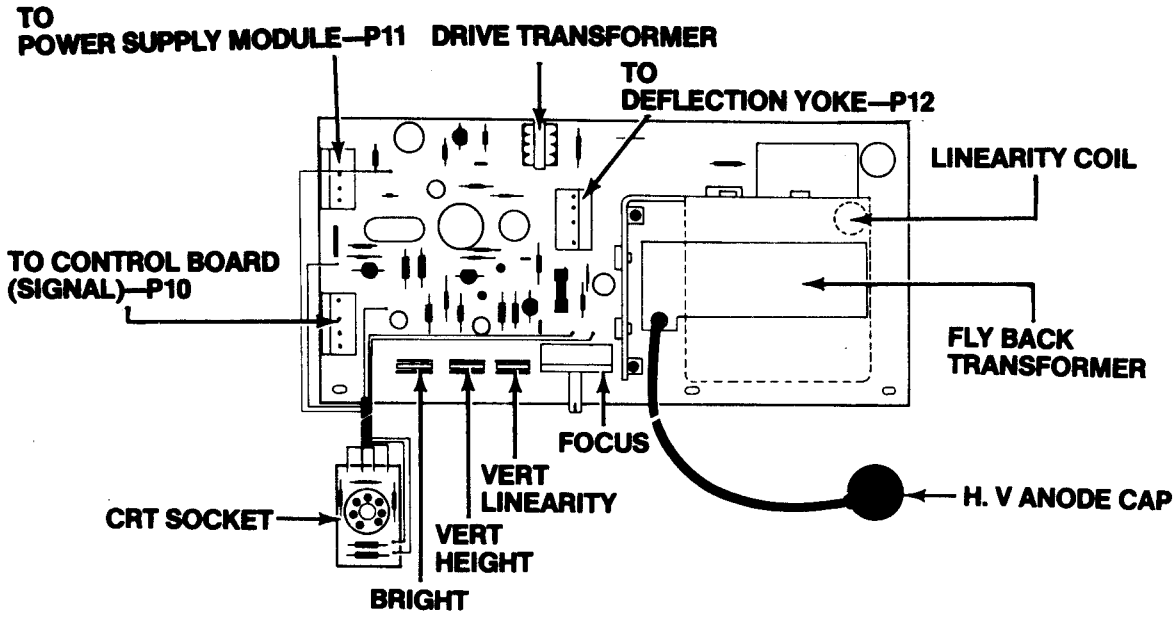
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TeleVideo, Inc.

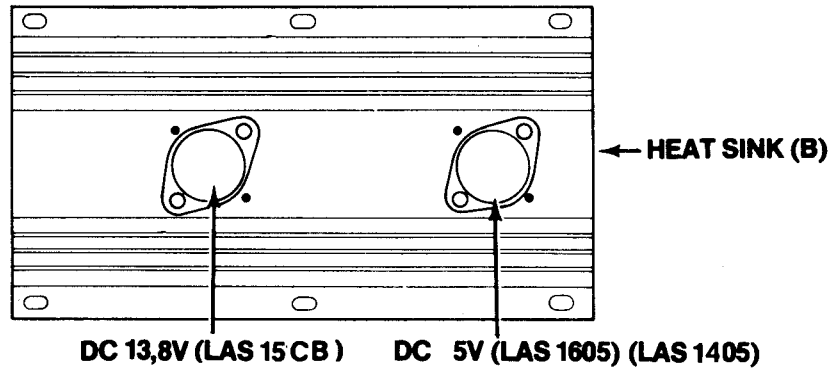
TITLE: WDC (WD-1000) DISK INTERFACE

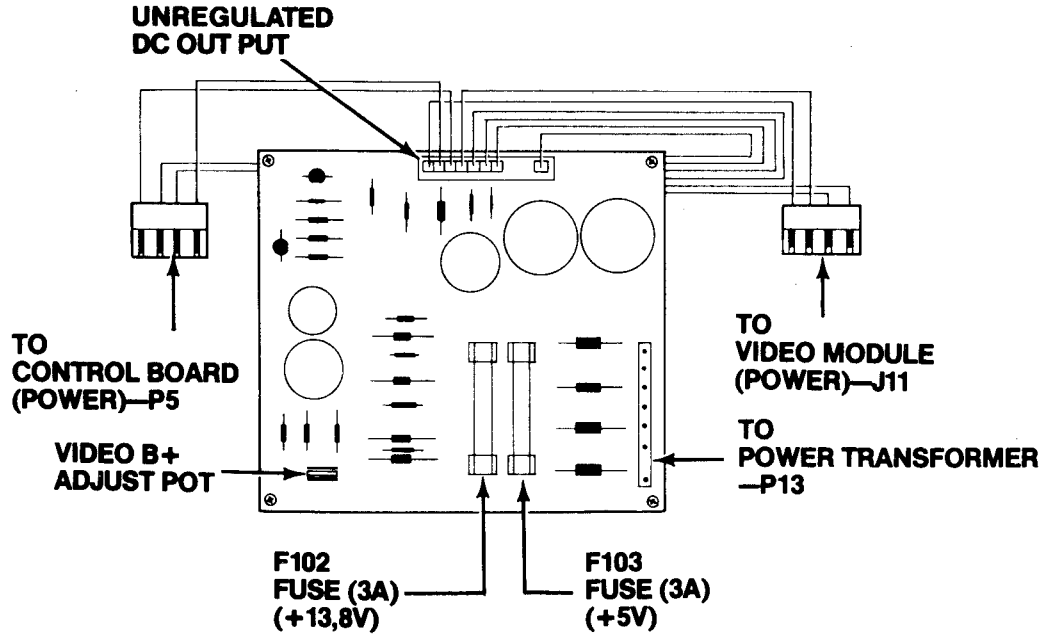
SIZE D | DWG NO WDC-B600010-001 | REV E

SHT OF

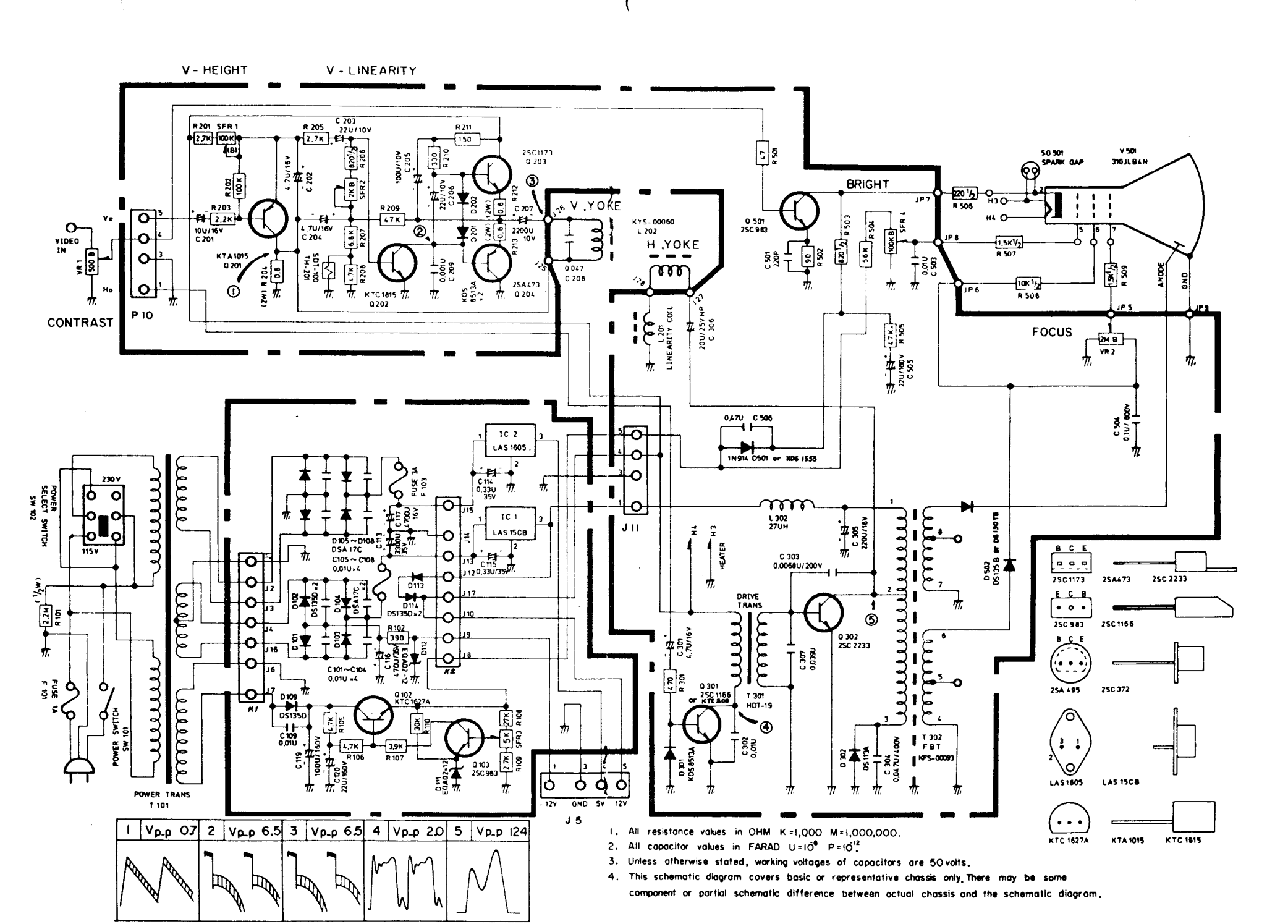


MONITOR BOARD





POWER SUPPLY MODULE



1	Vp-p 0.7	2	Vp-p 6.5	3	Vp-p 6.5	4	Vp-p 2.0	5	Vp-p 12.4

1. All resistance values in OHM K=1,000 M=1,000,000.
2. All capacitor values in FARAD U=10^{-6} P=10^{-12}.
3. Unless otherwise stated, working voltages of capacitors are 50 volts.
4. This schematic diagram covers basic or representative chassis only. There may be some component or partial schematic difference between actual chassis and the schematic diagram.

Part Number	Description	Locations REV A			
BC01642	POWER SUPPLY				
BC01643	CRT MODULE (VIDEO MODULE)				
TRANSISTORS					
S350100-006	KTC 1815/2N3904	Q202			
S350100-007	KTC 1627A	Q102			
S350100-009	2CS 983/2N5551/KTC 2229	Q103, Q501			
S350100-010	2SC 2233/MJE13006	Q302			
ST-10351	KTA 1015/2N3906	Q201			
ST-01353	2SC1/173/2N6121	Q203			
ST-01354	2SA473/2N6123	Q204			
ST-01361	KTC 200 (2SC1166)/2N4401	Q301			
CRT AND DIODE					
S360100-000	IN914/KDS 1553	D501			
SD-01251	DS135D/IN5391	D101, D102, D109, D113			
		D114			
SD-01252	DSA175C/IN5391	D103, D104			
SD-01253	DSA17C/MR500	D105, D106 D107, D108			

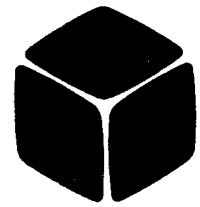
Part Number	Description	Locations REV A			
SD-01254	EQA01-12/IN759A	D111, D112			
SD-01255	DS-113A/MRI-1000	D302			
SD-01257	D130TB/IN4004	D502			
SD-01258	KDS-8513A/IN920	D201, D202			
		D301			
T300002-001	310JLB4 (N)	V501			
COIL AND TRAN					
IC-01365	CRT 858 (EI-858)	T101			
IC-01462	5.4 UH	L201			
IC-01464	27 UH	L302			
IC-01466	HDT-19	T301			
IC-01467	KFS-00093	T302			
IS-01461	KYS-00060	L202			
RESISTORS					
331243	SDT-100 THERMISTER	TH201			
R514000-004	470 OHMS, ¼W	R301			
R514000-011	4.7K OHMS ¼W	R105,106,208			

Part Number	Description	Locations REV A			
R514003-001	220 OHMS ½W	R506			
R514003-002	390 OHMS ½W	R102			
R514003-003	820 OHMS ½W	R206,503,210			
R514003-006	2.2 M ½W	R101			
R514000-017	100K OHMS, ¼W	R202			
R514000-025	47K OHMS, ¼W	R209,505			
R514000-026	150 OHMS, ¼W	R211			
R514000-043	27K OHMS, ¼W	R108			
R514000-045	47 OHMS ¼W	R501			
R514000-048	2.7K OHMS ¼W	R109,201,205			
R514000-049	90 OHMS ¼W	R502			
R514000-050	2.2K OHMS ¼W	R203			
R514000-051	3.9K OHMS ¼W	R107			
R514000-052	6.8K OHMS ¼W	R207			
R514000-053	30K OHMS ¼W	R110			
R514003-054	56K OHMS ¼W	R504			
RC02608J	0.6 OHMS 2W	R204,212,213			

Part Number	Description	Locations			
R514003-004	1.5K OHMS ½W	R507,509			
R514003-005	10K OHMS ½W	R508			
RF-07104B	EVL SOAA00B15 100K OHM POT	HEIGHT BRIGHT SFR1, SFR4			
RF-07202B	EVL SOAA00B23 sK OHM POT	SFR2 LINEARITY			
RF-07473B	EVL SOAA00B53 5K OHM POT	SFR3 75V REG.			
RV-24205B	EVL 26AS10B26 2M OHM POT	VR2 FOCUS			
RV-24501B	EVL GOAF20B52 500 OHM POT	VR1 CONTRAST			
CAPACITORS					
C700100-001	22 uf 16V	C203, 206			
C700100-010	10 uf 16V	C201			
C700100-011	4.7 uf 16V	C202, 204			
C900100-002	0.01 uf 50V	C101,102,103 104,105,106,			
		107,108,109, 503			
C900100-012	1KV SPARKGAP	S501			
CC-50221SL	220 uf 50V	C501			
CE-101075	100 uf 10V	C205			
CE-10226SH	22 uf 100V	C505			

Part Number	Description	Locations REV A			
CE-1607SH	100 uf 160V	C119			
CE16227S	220 uf 16V	C305			
CE-10228S	2200 uf 10V	C207			
CE-16226 SH	22 uf 160V	C120			
CE-35338S	300 uf 35V	C113			
CE-35478S	4700 uf 16V	C117			
CM 16475S	4.7 uf 16V	C301			
CM 20682H	0.0068 uf 200V	C303			
CM 50102	0.001 uf 50V	C209			
CM 50103	0.01 uf 50V	C302			
CM 50473	0.047 uf 50V	C208			
CM 50474	0.47 uf 50V	C506			
CM-60104	0.1 uf 600V	C504			
CN-15206S	20 uf 25V	C306			
CO-40473H	0.047 uf 400V	C304			
CT-35334	0.33 uf 35V	C114, C115			
CT-35338S	470 uf 35V	C116			

Part Number	Description	Locations REV A			
SWITCHES					
M200107-001	SPST 115V 10A/230V 5A	SW101			
M200108-001	DPDT 115V/230V	SW102			
FUSES					
FC-12503A	3A/125V FAST BLOW	F102, F103			
M200104-001	1A/250V FAST BLOW	F101			
SPEAKER					
3801541	8 OHM	S001			



VIDEO BOARD TROUBLESHOOTING GUIDE

I. VISUAL INSPECTION

A. With video module installed, turn off power to terminal and check for the following:

1. Connectors

   a. Loose connectors
   b. Bad crimps
   c. Broken clips on pins at connector
   d. Dirty contacts

2. Broken wires

3. Loose or frayed ground connector (912/920)

4. Overheated, burned or leaking components

Correct and recheck before continuing.

B. Remove video module from terminal and give a detailed visual inspection.

1. Removal instructions:

   a. Turn unit off
   b. On the video module, disconnect
      (1) J10 (signal input)
      (2) J11 (DC power)
      (3) J12 (yoke)
   c. On CRT (tube), disconnect
      (1) CRT socket (small pcb at rear or tube)
      (2) Anode lead (on underside of tube)

CAUTION

Discharge tube before removing anode lead!

      (3) Ground wire
   d. On video module, remove the three securing screws.

d. On video module, remove the three securing screws.
NOTE: When video module is reinstalled, lock tight the securing screws.
e. Carefully remove the video module.

2. Closely inspect the video module for

a. Overheated, burned, or leaking components
b. Missing or broken components
c. Cracked or broken traces
d. Cold solder joints

Correct and recheck before continuing

C. Reinstall video module and apply power.

WARNING!!!

High voltages are present on the video board. USE EXTREME CARE when troubleshooting

NOTE: Adjustments are provided for

Brightness
Height
Linearity
Focus

NOTE: For voltage levels and waveforms, see Attachment 1.

II. MALFUNCTIONS

A. No vertical deflection. Check:

1. Q201 collector

a. If present, proceed to Step 2.
b. If not present, check Q201 base.
c. If present at base, isolate Q201 collector to see if signal is being pulled down. If still no output at Q201, suspect Q201.
d. If not present at Q201 base, troubleshoot between Q201 base and P10 pin 5 (vertical sync signal from logic board).

2. Q202 collector

a. If present, proceed to Step 3.
b. If not present, check Q202 base.
c. If present at base, isolate Q202 collector to see if signal is being pulled down. If still no output, suspect Q202.
d. If not present at Q202 base, troubleshoot from Q202 base back.

3. C207 negative side

   a. If present, the vertical drive section of the video module has checked good. If a vertical problem still exists, areas to check are: connections; the CRT socket; and related components (small pcb at neck of CRT).
   b. If not present at C207, check Q203 emitter.
   c. If not present at Q203 emitter, check Q203 base. If present at base, suspect Q203.
   d. If not present at Q203 base, troubleshoot back.
   e. If Q203 emitter checks good, check Q204 emitter.
   f. If not present at Q204 emitter, check A204 base. If present at base, suspect A204.
   g. If not present at base, troubleshoot back.

   NOTE: If either Q203 or Q204 requires replacement, both should be replaced.

B. No horizontal deflections, check:

1. Q301 collector

   a. If present, proceed to Step 2.
   b. If not present, check Q301 base.
   c. If present at base, isolate Q301 collector to see if signal is being pulled down. If still no output at Q301 collector, suspect Q301.
   d. If not present at Q301 base, troubleshoot between Q301 base and P10 pin 1. (horizontal sync signal from logic board).

2. Q302 collector

   a. If present, proceed to Step 3.
   b. If not present, check Q302 base.
   c. If present at Q302 base base, isolate Q302 collector to see if signal is being pulled down. If still no output, suspect A302.
   d. If not present at Q302 base, suspect T301 (drive transformer) or Q302.

3. If proper signal is present at Q302 collector, suspect areas

   a. C306
   b. L201

C. No video. Suspect areas:

1. L302
2. Q302
3. Q301
4. T302 (FBT)
5. Cracked or broken trace
6. C305
7. Q501

D. Jittery screen. Suspect areas:

1. Dirty yoke connector J12
2. C504
3. Bad crimp
4. Cold solder joint

E. Poor linearity. Suspect areas:

1. Horizontal

    a. L201

2. Vertical

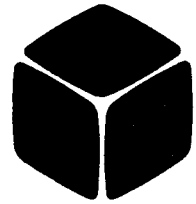
    a. SFT 2 needs adjustment
    b. Q203 and Q204

F. Blows fuses/low voltage. Suspect areas:

1. C504
2. T302 (FBT)
3. Q302
4. T301

G. Arcing/crackling. Suspect areas:

1. T302 (FBT)
2. Cracked or broken traces



POWER SUPPLY TROUBLESHOOTING GUIDE

I. VISUAL INSPECTION

A. With the power supply module installed, disconnect power from the terminal and check for:

1. Connectors

   a. Loose connectors
   b. Bad crimps
   c. Dirty contacts
   d. Depressed pins in connector

2. Broken wires

3. Overheated, burned, or leaking components

4. Bad fuse

   NOTE: Use ohm meter. Do not rely on visual check.

5. Loose fuse holder.

   NOTE: Correct and recheck before continuing.

B. Remove the power supply module from the terminal and give a detailed visual inspection.

1. Removal instructions:

   a. Turn unit off and disconnect power cord
   b. On power supply, disconnect K1 (AC input)
   c. On video module, disconnect J11.
   d. On logic board, disconnect J5.
   e. On power supply module, remove the securing screws.

      NOTE: Lock tight securing screws when the power supply module is reinstalled.

   f. Carefully remove the power supply module.

TeleVideo

2. Closely inspect the power supply module for:

   a. Bad connectors/connections
   b. Bad crimps
   c. Overheated, burned, or leaking components
   d. Disassemble the power supply module and inspect for:

      (1) Cold solder joints
      (2) Broken or cracked traces

3. To disassemble the power supply module:

   a. Remove four securing screws and spacers holding small board on heat sink.
   b. Discharge the capacitors on the pcb.

      NOTE: For voltage levels and waveforms, see Attachment 1.

II. VOLTAGE MANFUNCTIONS

A. No +5V DC

a. Remove F103 and check for +12V on one side of the fuseholder.

   a. If not present, suspect areas:

      (1) C105 through C108
      (2) D105 through D108
      (3) Crimps and connections

   b. If present, suspect areas:

      (1) Fuse (F103)
      (2) LAS1605
      (3) Crimps and connections
      (4) C114
      (5) C113

B. +5V DC is low

1. Suspect areas:

   a. LAS1605
   b. Crimp and connections

C. No +12V DC or 13.8V

1. Remove F102 and check for +24V on one side of the fuseholder.

   a. If not present, suspect areas:

      1. C101 through C104
      2. D101 through D104

b. If present, suspect areas:

(1) LAS15CB
(2) C115
(3) C113
(4) Crimps and Connections
(5) F102 (Fuse)

D. +12V DC or +13.8V DC is low. Suspect areas:

1. LAS15CB
2. C113
3. Crimp and connections

E. No -12V DC. Suspect areas:

1. C101 and C102
2. D101 and D102
3. D112
4. C116
5. Crimps and connections

F No +75V DC. Suspect areas:

1. C109 (Remove only; not required)
2. Q102
3. C119

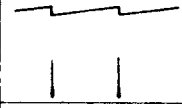
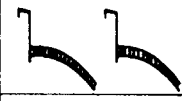
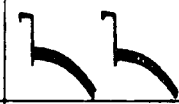
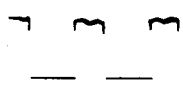
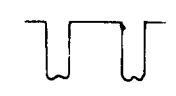
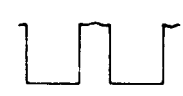
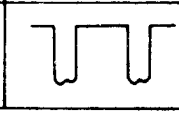
G. +75V DC is low.

1. Adjust SFR3.
2. If +75V DC will not adjust, suspect areas:

a. Q103
b. C109

TR WAVEFORM and VOLTAGE

Attachement 1

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC 1)	LAS1512	Regulation	12	2.5		12	0.0		0.0	0.0	
(IC 2)	LAS1605	〃		1.6		5	0.0		0.0	0.0	
(IC 3)	LAS1812	〃		0.1		-12	0.0		0.0	0.0	
(IC 4)	LAS15CB	〃		1.4		13.8	0.0		0.0	0.0	
Q102	2SC509	〃	78.7	0.0		86.4	1.5		98.0	0.0	
Q103	2SC983	〃	12.0	0.0		75.7	0.0		11.9	0.0	
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0		8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0		8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	
Q501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

MODEL 950/TS800 KEYCAPS

Part No.	Size/Color	Inscription
K030305-001	1x1, Dark Grey	blank
" -002	" "	1, !
" -003	" "	2, @
-004	" "	3, #
-005	" "	4, $
-006	" "	5, %
-007	" "	6, ^
-008	" "	7, &
-009	" "	8, *
-010	" "	9, (
-011	" "	0,)
-012	" "	-, -
-013	" "	+, =
-014	" "	~, `
-015	" "	:, /
-016	" "	back space
-017	" "	1
-018	" "	2
-019	" "	3
-020	" "	4
-021	" "	5
-022	" "	6
-023	" "	7
-024	" "	8
-025	" "	9
-026	" "	0
-027	" "	- (minus)
-028	" "	,
-029	" "	.
-030	" "	Q
-031	" "	W
-032	" "	E
-033	" "	R
-034	" "	T
-035	" "	Y
-036	" "	U
-037	" "	I
-038	" "	O
-039	" "	P
-040	" "	[]
-041	" "	back tab
-042	" "	alpha lock
-043	" "	A
-044	" "	S
-045	" "	D
-046	" "	F
-047	" "	G
-048	" "	H
-049	" "	J
-050	" "	K
-051	" "	L
-052	" "	:, ;
-053	" "	', "
-054	" "	Z

Part No.	Size/Color	Inscription
K030305-055	1x1 Dark Grey	X
" -056	" "	C
" -057	" "	V
" -058	" "	B
" -059	" "	N
" -060	" "	M
" -061	" "	<, ,
" -062	" "	>, .
" -063	" "	?, /
" -064	" "	}, {
" -066	" "	LOC ESC / ESC
K030306-001	1x1½ Dark Grey	blank
" -002	" "	line feed
" -003	" "	tab
K030307-001	1x1½ Light Grey	blank
" -002	" "	shift
" -003	" "	enter
K030308-001	1x1, Lt., Grey	blank
" -002	" "	F1
" -003	" "	F2
" -004	" "	F3
" -005	" "	F4
" -006	" "	F5
" -007	" "	F6
" -008	" "	F7
" -009	" "	F8
" -010	" "	F9
" -011	" "	F10
" -012	" "	F11
" -013	" "	char. insert
" -014	" "	char. delete
" -015	" "	line insert
" -016	" "	line delete
" -017	" "	line erase
" -018	" "	page erase
" -021	" "	control
" -022	" "	break
" -023	" "	delete
" -024	" "	send
" -026	" "	set-up/no scroll
" -0	" "	
K030309-001	1x1, Lt."Grey	L/P, blank
" -003	" "	funct
" -004	" "	home
" -005	" "	→↑↓←
" -006	" "	print
K030310-002	"L" Lt. Grey	return
" -001	" "	blank
K030311-001	1x1¼, Lt. Grey	blank
" -002	" "	clear space
K030312-001	1x8, Dark Grey	space bar

Field Bulletin

March 2 ,1982
Issue No.3

Timely Technical and Sales Information from TeleVideo's Computer Systems Division

A LETTER FROM DAVID WINTERSTEIN

Dear Distributor:

As manager of the Customer Service and Technical Support Department of TeleVideo Computer Systems Division, I would like to take this opportunity to explain to you the organization and functions of our department.

For smoother operation and efficiency, the department is divided into three basic groups: hardware specialists and software specialists who work out of our home office in Sunnyvale, and application engineers who work out of field offices, each of which has a sales manager.

This division of services is designed to give you technical support locally, as well as from our home office.

We are geared to solve technical problems and to answer any complex technical questions regarding the operation or application of our systems. We also aim to insure your satisfaction of our third party maintenance in the services they perform for you.

The home office group handles return material authorization and warranty administration while providing technical support.

Because of our specialized task and teamwork concept, you can start solving a problem with one of our staff members, and if you call us for further information, another individual is also capable of assisting you. In this way, you need not wait for the availability of a specific person to assist you. And we can aid you in arriving at a solution quickly.

At our Sunnyvale headquarters, we are continually seeking new ways to better serve you -- discussing problems, looking for failure trends and exchanging ideas for better applications solving. On a daily basis, we are in touch with each regional application engineer, so that everyone remains current, knowledgeable and informed on the status of our projects.

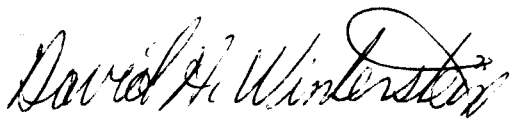
We have a unique team of intelligent, professional and customer-oriented people -- dedicated to supporting you and your business.

Allow me to introduce our team members: Hardware specialists Paul Horvath and Larry McDonald, Software Specialists Eric Carr and John Clark, and Application Specialist Dave Thayer are all based at our Sunnyvale home office.

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

Our regional application specialists are Al Weaser, Los Angeles; Jerry Eubanks, Dallas; Bob Wright, Norcross, Georgia; Ray Inserra, Lombard, Illinois; and Dick Lam, Amsterdam, The Netherlands, who covers Europe. Vacant positions soon to be filled are located in the New York and Boston offices.
If you feel at any time that one of our group has not been effective in helping you, or if you need higher level decision making assistance, please feel free to phone me. I will see to it that the necessary machinery is put into motion to come to a proper and final solution to your specific problem.

Sincerely,



David A. Winterstein

ATTENTION is to mark items that are important and should be read.

FIELD BULLETIN

TS806 Reset at Power On ATTENTION

To consistently have the TS806 reset automatically at "power on", change A2 to become a 74LS03 rather than a 74LS00. This change is being retrofitted into our present stock as of February 12. Please phone us with the number of TS806s you have with this problem and we will send you the appropriate number of components. (This is not a mandatory change.)

Winchester Disk Controller ATTENTION

For a more stable BFO on the Winchester disk controller, replace R23 with a 240 ohm resistor at 5%. (This is not a mandatory change.) Phantom or intermittent hard disk errors, BDOS errors may be corrected by this resistor change. (Also Random format or fixdisk errors.)

LANGUAGES COMPATIBLE WITH MmmOST

TeleVideo's multiuser systems operating under MmmOST can use any CP/M compatible programming language. New TeleVideo COBOL will be available in April. Other CP/M languages require some modifications, as described in the MmmOST Programmer's Manual.

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

MmmOST Enhancements - Release 1.1 to 2.0

Shared Drive Usage

o Shared Files

- o May be extended dynamically (during use) when in N/L or F/L modes. The new portion of a file will be accessible by all other users immediately, and will also be under the control of MmmOST's record and file locking capabilities, if enabled. MmmOST no longer must be reloaded from disk subsequent to extending a shared file. (3.3.3.3 and 3.3.4.1)

- o May be deleted, created and renamed, if no other user has those files open. Again, MmmOST no longer is required to be reloaded. (3.4.1)

- o Commands interpretation of the MULTI.SYS file by MmmOST will now execute approximately 25 times faster. MULTI.SYS commands may no longer have garbage characters, and at most one embedded blank between items is permitted. The command may be enclosed with quotes (' or "). (3.3.2.3)

- o File and record locks will be removed when a program cold or warm boots. The user may maintain locks by first running the program: KEEPLOCK E. The default is restored by running: KEEPLOCK D. Access modes will be maintained. (3.3.3.5)

- o There is no limit, except for free memory space, to the number of filenames in the shared file list.

- o New MULTI.SYS commands are:
  'd:filename.typ(rn,rs) = LCK' , and
  'd:filename.typ(rn,rs) = ULK'
  Where rn is the record number, and rs is the record size in bytes. This will lock multiple records as necessary to accomodate any sector sharing by multiple users; (3.3.2.6)

  and:

  'x = DUMP'
  Where x is in the syntax of a file reference. Upon receiving the command, MmmOST will place the system status in the file DUMP.SYS on the spool drive. This includes space available on the private directory drives and the status on all open or shared files on shared file drives.

- o The MULTI.SYS command '*.* = N/L' is no longer necessary or allowed.

- o Carriage Return and Line Feed are placed in position 127 of record 0 of MULTI.SYS.

  - o Unwritten mailboxes are initialized with blanks.

  - o Better error recovery to the user program.

- o Unshared Files

  - o May be placed in the shared file list by simply specifying an access mode for the file when it is UNOPENED by any user. Its order for hierachical locks is the sequence of becoming shared. The file will remain in the list until the service processor is warm or cold booted. (3.2.3.2)

  - o May be deleted, created, renamed and updated by several users, on different files, simultaneously. (3.4.1)

  - o Become exclusively owned by the first user who writes to it, until warm or cold boot.

- o Spool files are placed on shared drives. (5.2.1)

Private Drive Usage

- o The actual disk space available may be obtained from the MULTI.SYS command 'x = DUMP' mentioned above, or the transient command DSTAT.COM.

- o Since spooling is now done on a shared drive, there is no requirement that a private drive exist in the system. However, there will be a problem if multiple users attempt to use SUBMIT if drive A is not a private drive.

Print Spooling (5.2.1)

- o Named disk files are created by the spooler. This allows considerable manipulation by the user of the file to be printed. Spool file names are: SPLuqnnc.PRt where:

  u is the user's work station alphanumeric id
  q is the queue name - defaults to 0-3 according to iobyte
  nn is the print priority - low numbers first
  c is the number of additional copies
  t is the type:
    N normal
    H print standard forms message and pause
    P pause after 128 characters from the file
      (PRNT M is filled with 128 nulls)

- o Binary characters in the print stream will no longer control the spooler. This will be done by the method above.

- o Top of Form is sent to printer before each print file (default).

o PRNT commands generally apply to the file spooling or the next to spool. (5.3)

GENPARMS

o A totally new, menu-driven program for generating the DPCPARMS.DAT file. (Chapter 6)

Work Station CP/M

o The number of USERCPM.DAT files is now eight (USERCPMn.DAT, where n may to 0 to 7.

o Some error messages may be suppressed with:
  ERRMSG D
  and restored with:
  ERRMSG E. (7.3)

o Multiple user definable functions are now available. USRFNi for i = 1 to 4 are accessible from mailstops 1 to 4.

o New CNFGUSER program allows a smaller CP/M, thereby increasing the size of the user available memory (TPA) to about 54K.

o Sign-on message has new version number and work station identification. (3.5.2)

o Configuration changes that require rerunning CNFGUSER are enforced by a 'generation revision' number.

TS801 Serial Port (RS422) Activation

To activate the RS422 port in order to use the TS801 as an intelligent workstation, perform the following cuts and jumps:

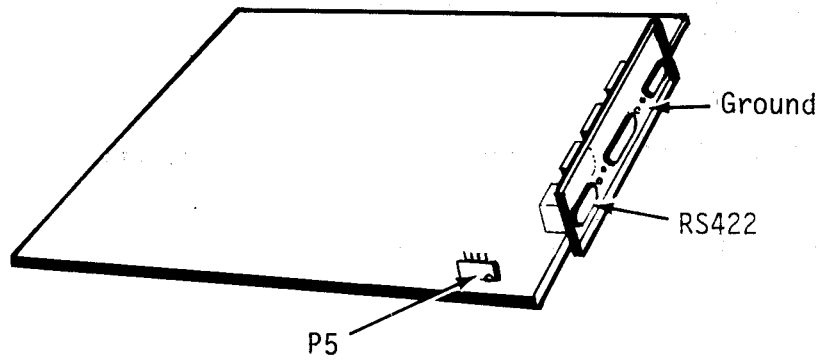
CUT W1, W2, W10, W11, W12, W8, W9	(These are wires and just require removal)
JUMP W3, W4, W5, W6, W7	(Located by A12 on board)

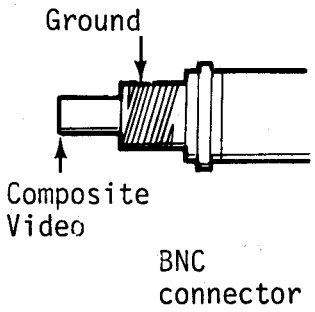
When these cuts and jumps are completed, the RS232 printer port will no longer be functional.

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

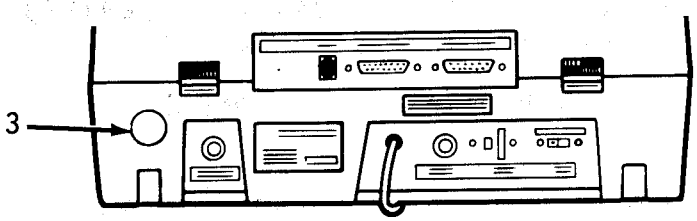
Composite Video Modification

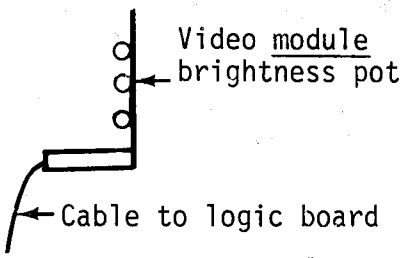
This is the instruction set for modifying the TS800A, TS802(H) logic PCB for the use of composite video.





Keyboard Connector





Instructions:

1. **Cut trace at W15.**
2. **Add jumper to W16.**
3. **Cut hole in connector SHROUD on left side as viewed from rear of terminal.**
4. **Install "BNC" connector (AMP P/N 227169-5) onto shroud assembly.**
5. **Connect center lead of connector to P5-6 as shown above.**
6. **connect Gnd lead of connector to P5-3 as shown.**
7. **Adjust brightness pot as needed.**

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

RMA PROCESS

When it is necessary to return a system to the factory for repair you must have a "Return Material Authorization". This authorization is given by the home office Customer Service Department. When calling for authorization please have the following information ready for us:

1. Serial number/modem number

2. Address to return system to upon completion of repair

3. Phone number and the name of the person to contact if we have further questions regarding the system

4. Description of the failure mode

When shipping the product to us please take care of shipping costs, C.O.D. shipments are refused at our receiving dock. The RMA (return material authorization) number must also be on the shipping label. The system will be repaired and on its way back to you within an average of five days. If more time is required, we will notify you of the difficulty so you can be involved in the decision making process.

After your system is repaired we will burn it in and run it through our Quality Assurance testing for new systems. We will then ship it back best way surface. When and if we received the system within the last 24 hours, warranty repairs will be paid for by TeleVideo. If you wish the system to be shipped to you quicker than surface, you must let us know at the time you call in. We will return the system C.O.D. to you in order to meet your needs for delivery (i.e. overnight, three days).

When the system has been shipped and repairs performed, you will be invoiced for our of warranty repair work based on the attached repair price list. Repair charges are on a fixed rate basis. This takes the guess work out of your repair bill. The exception being systems obviously damaged by the customer. In this case you will be notified of the estimated repair charge. (Do not send a board in with all the pluggable parts bad.)

When the system is returned to you, you will also have a copy of the work performed.

Here is a brief description on how we track a returned system:

1. When it is received the receiving clerk matches the paperwork to the system and pulls a copy for our department.

2. When the system is shipped, our department gets the final copy. This system allows us to tell you the following when

you call and ask about your RMA number:

a. When and if we received the system within the last 24 hours.

b. When the system was shipped and repairs performed.

We can give you information regarding the preceding two items. Any other information requires 24 hours. We keep a constant vigil on returned systems and when we see one in the log book that has been at the plant for five days, we check for causes.

WARRANTY ADMINISTRATION

Warranties are administered by our home office Customer Service Department. Warranty repair is performed at the factory at no charge (other than shipment to factory). We also send replacements for faulty components and do not swap boards as this is ultimately a disservice to the customer. By maintaining the same system boards, the product will have a longer operation time.

Replacement components are shipped within two days as follows: All requests received by 2 PM will be shipped by 5 PM the following day. This system allows for smoother two-day response to components requests.

Another method of warranty repair is to pay the labor rate of our third party maintenance; who gets the replacement component from us at no charge.

The third and best way to insure continued operation of your system is to put it under a service contract at the time of purchase.

THIRD PARTY MAINTENANCE

Customer Service at headquarters insures the smoother operation of our third party maintenance organization. Any time you have a question on site locations or national service, feel free to call us and we will connect you with the right people.

If you have a problem with the third party service, call us and we will help to solve any discrepancies in bills or in lack of response and professionalism.

We have a third party organization to give you a better sales position. If that service does not perform as stated by TeleVideo, then you must notify us. As a valued and respected customer, your satisfaction is our responsbility and our pleasure.

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

SOFTWARE DISTRIBUTION

As new releases of the CP/M BIOS or of MmmOST occur we contact the distributors by phone. When we reach the distributors, we inform them of any charge associated with the new release and request the name of an individual at the distributor office to help coordinate the release. We also notify the distributor of the type of software changes or enhancements and provide a letter for distribution to the customers. Within a week of a blanket no-charge release, we make copies of the new software with the serial numbers of the software sold to distributors up to that time. We then send the distributor appropriate copies for distribution to customers. The distributor retrieves the old diskette and sends it back to TeleVideo so we know that all systems have been updated. If the old diskette is not received within 60 days we must charge the distributor for each unreturned copy.

When the release is a chargeable release we send a copy to the distributor for the appropriate serial number after we have checked on the registration of the software. For this reason it is imperative that you complete the registration form.

REMINDER OF UPCOMING CLASSES

Software Classes - March 29, 30, and April 12, 13 - $200.00

Hardware Classes March 31, and April 1, 2, also on April 14-16 - $350.00

Software class is geared to give general understanding regarding MmmOST and other TeleVideo supplied software packages. Hardware class is geared to give module repair capability and understanding of logic boards for systems.

SERVICE NOTE INDEX

NOTE	DESCRIPTION	REVISION	FIELD BULLETIN ISSUE
1	TS801 Serial Port (RS422) Activation	2	3
2	Reshipping Systems	0	1
3	TS806 Different Baud Rates for RS232 Ports	0	1
4	General Information	0	1
5	Composite Video Modification	1	3
6	Area Code Listing	0	1
7	TS806 Logic Board Interrupt Capability	0	1
8	Cables and CP/M Summary Guide	2	1

Field Bulletin
Timely Technical and Sales Information from TeleVideo's Computer Systems Division

The TRW contract has been signed. June 1st will be when all 30 initial locations will be trained and ready for operation. Attached is a list of locations and phone numbers. TRW will be replacing GE ICES as TeleVideo's third party maintenance organization for TeleVideo Systems.

SCHEDULE OF SERVICE LOCATIONS

A. Service Locations

1. San Francisco, California 1-326
TRW Customer Service Division
3073 Teagarden Street
San Leandro, California 94577

2. Los Angeles, California 1-410
TRW Customer Service Division
1720 Beverly Boulevard
Los Angeles, California 90026
Phone: 213/483-4800

3. San Diego, California 1-210
TRW Customer Service Division
269 W. Washington Street
P.O. Box 3039
San Diego, California 92103
Phone: 714/297-4015

4. Seattle, Washington 1-360
TRW Customer Service Division
13400 Northrup Way
Building B, Suite 32
Bellevue, Washington 98005
Phone: 206/641-6660

5. Phoenix, Arizona 1-311
TRW Customer Service Division
2622 South 24th Street
P.O. Box 20927
Phoenix, Arizona 85036

6. Salt Lake City, Utah 1-267-C
TRW Customer Service Division
960 North 400 East
P.O. Box 213
North Salt Lake, Utah 84054
Phone: 801/292-0408

7. Denver, Colorado 1-267
TRW Customer Service Division
4855 East 41st Avenue
P.O. Box 16083
Denver, Colorado 80216
Phone: 303/388-6307

8. Kansas City, Missouri 4-216
TRW Customer Service Division
3100 Terrace
Kansas City, Missouri 64111
Phone: 816/753-2578

9. Dallas, Texas 1-293
TRW Customer Service Division
1770 Viceroy Drive
P.O. Box 35787
Dallas, Texas 75235
Phone: 214/630-2640

10. Houston, Texas 3-306
TRW Customer Service Division
13240 Hampstead Highway, Suite 21
Houston, Texas 77040
Phone: 713/462-7474

11. St. Louis, Missouri 3-370
TRW Customer Service Division
2212 Welsch Industrial Court
St. Louis, Missouri 63141
Phone: 314/872-9342

12. North Chicago 4-336
TRW Customer Service Division
1325 Wiley Road, Suite 140
Schaumberg, Illinois 60195
Phone: 312/884-0800
or
Chicago, Illinois (South) 4-255
TRW Customer Service Division
100 Bliss Drive
Oak Brook, Illinois 60521
Phone: 312/986-6430

13. Indianapolis, Indiana 4-372
TRW Customer Service Division
5603 West Raymond St., Suite L
Indianapolis, Indiana 46241
Phone: 317/247-9707

14. Atlanta, Georgia 3-320
TRW Customer Service Division
5924 Peachtree Corners East
P.O. Box 763
Norcross, Georgia 30091
Phone: 404/449-4906

15. Baltimore, Maryland 3-374
TRW Customer Service Division
1000 Cromwell Bridge Road
Towson, Maryland 21204
Phone: 301/828-0525

16. Cleveland, Ohio 4-396
TRW Customer Service Division
16528 Commerce Court
Cleveland, Ohio 44130
Phone: 216/243-4055

17. Columbus, Ohio 4-490
TRW Customer Service Division
2208 Hamilton Road South
Columbus, Ohio 43227
Phone: 614/864-5583

18. Cincinnati, Ohio 4-317
TRW Customer Service Division
4511 Reading Road
Cincinnati, Ohio 45229
Phone: 513/242-6720

19. Detroit, Michigan 4-353
TRW Customer Service Division
16250 Northlan Drive, Suite 110
South Field, Michigan 48075
Phone: 313/569-6610

20. Minneapolis, Minnesota 4-287
TRW Customer Service Division
1157 Grey Fox Road
Arden Hills, Minnesota 55112
Phone: 612/484-8319

21. Boston, Massachusetts 2-222
TRW Customer Service Division
1605 Trapelo Road
Waltham, Massachusetts 02154
Phone: 617/890-5600

22. New Jersey Northern 2-397
TRW Customer Service Division
90 Route 22 at Stern Avenue
Springfield, New Jersey 07081
Phone: 201/379-7300

23. Philadelphia Metro 2-218
TRW Customer Service Division
1819 Underwood Boulevard
Unit No. 7
Delran, New Jersey 08075
Phone: 609/764-9082

24. Pittsburg, Pennsylvania 2-398
TRW Customer Service Division
2212 Noblestown Road
Pittsburg, Pennslyvania 15205
Phone: 412/922-6134

25. New York City, New York 2-225
TRW Customer Service Division
144 East 44th Street
New York, New York 10017
Phone: 212/953-9500

26. Hartford, Connecticut 2-399
TRW Customer Service Division
380 Market Street
Hartford, Connecticut 06120
Phone: 203/547-1410

27. Miami, Florida 3-323
TRW Customer Service Division
4824 Northwest 167th Street
Hialeah, Florida 33014
Phone: 305/624-0309

28. Raleigh, North Carolina 3-335
TRW Customer Service Division
1200 Front Street, Suite 110
Raleigh, North Carolina 27609
Phone: 919/821-4655

29. Nashville, Tennessee 3-383
TRW Customer Service Division
4721 Trousdale, Tennessee 37220
Phone: 615/331-5501

30. **Syracuse, New York 2-377-B**
TRW Customer Service Division
2000 Teall Avenue
Syracuse, New York 13206
Phone: 716/442-2965