INSTRUCTION MANUAL

4002A DRAWER UNIT and KEYBOARD MAINTENANCE

PART OF 4002A GRAPHIC COMPUTER TERMINAL

Serial Number _____

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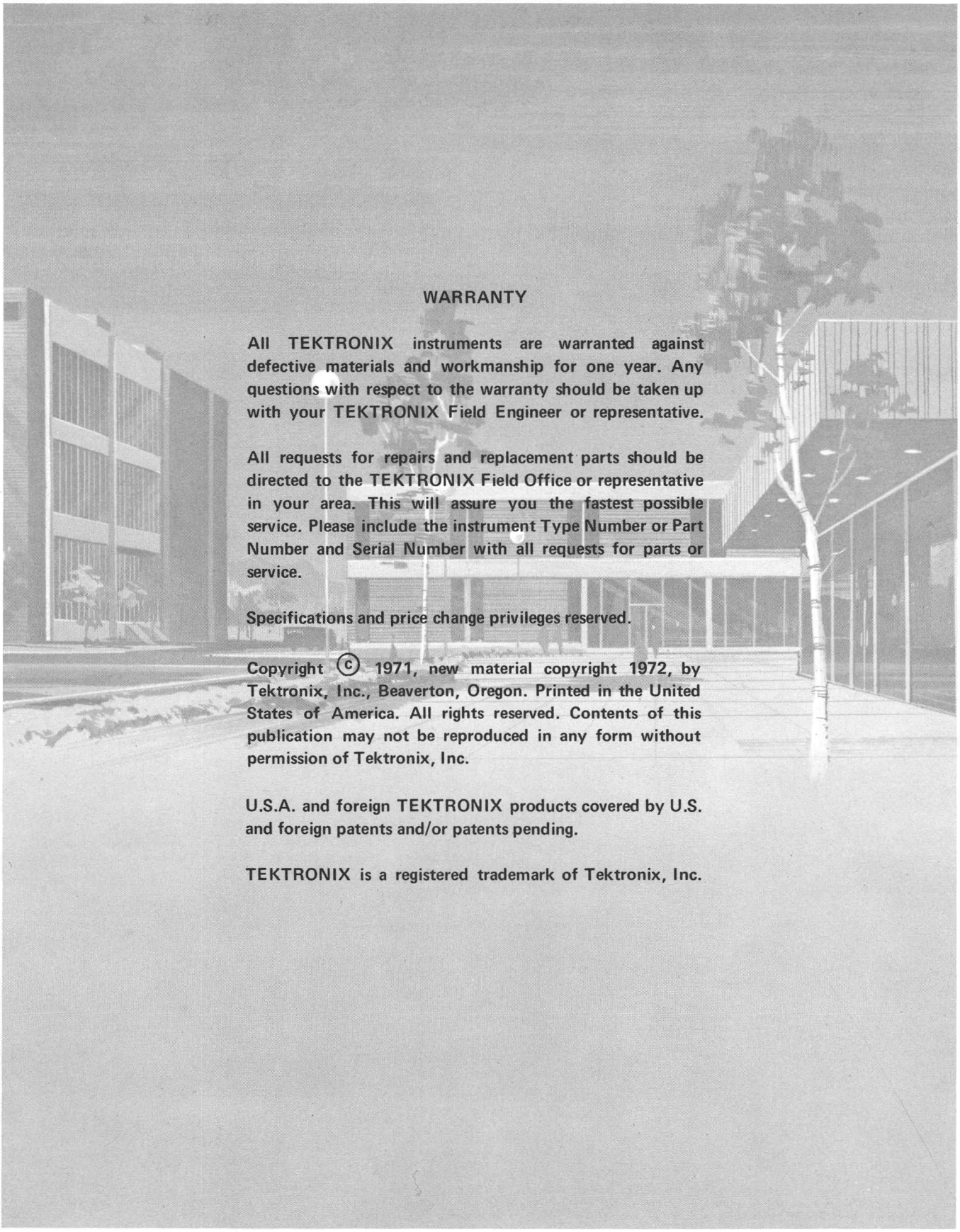

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TABLE OF CONTENTS

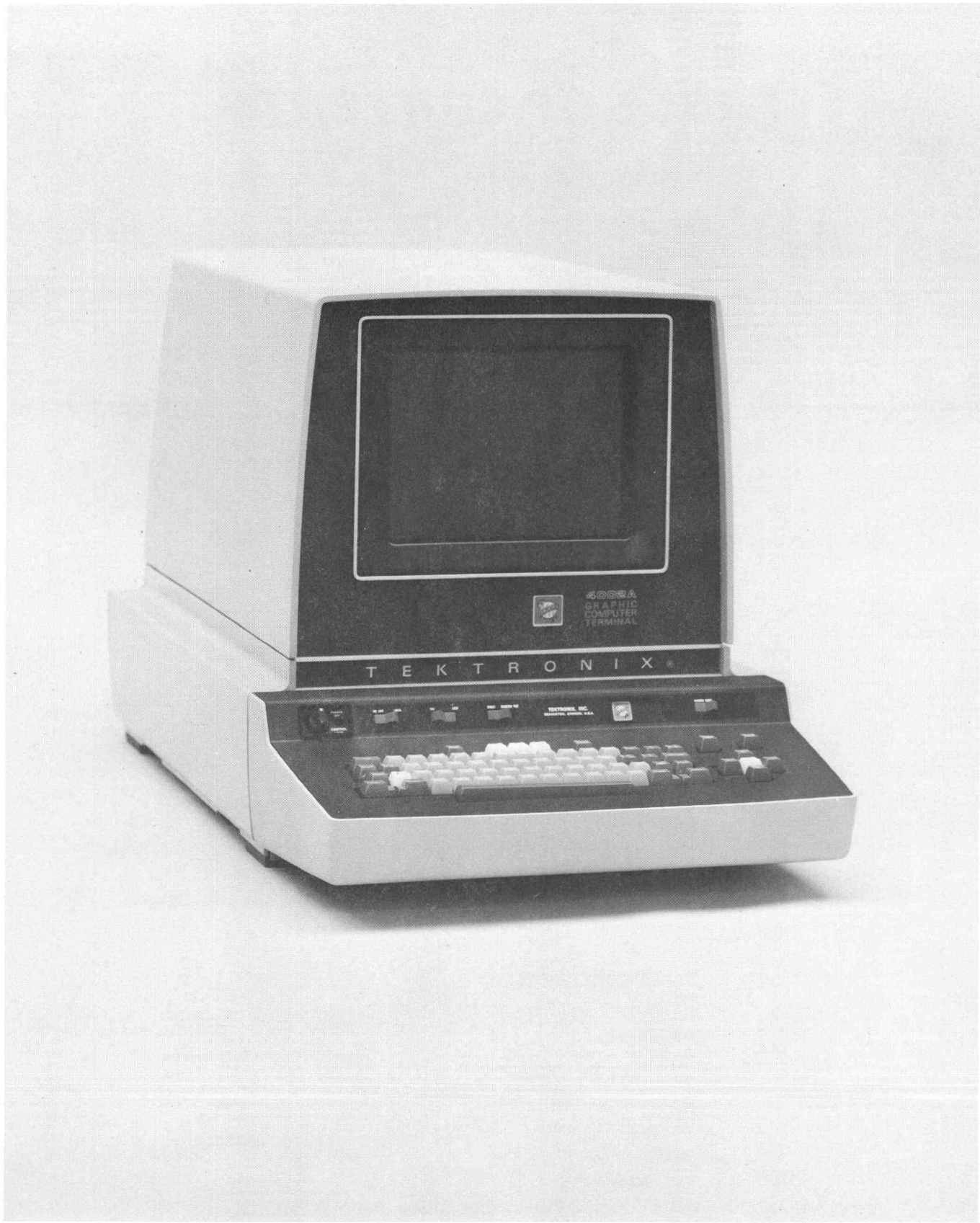

Fig. 1-1. 4002A Graphic Computer Terminal

SECTION 1
GENERAL INFORMATION

INTRODUCTION

The 4002A Drawer Unit is a part of the Tektronix 4002A Graphic Computer Terminal, a device which permits rapid interchange of data between man and computer, whether the 4002A and the computer are geographically separated or located in the same room. The physical relationship of the principal units is shown in Fig. 1-1. Their electrical association appears in Fig. 1-2. A description of the system, its characteristics and operation are contained in the 4002A Specification and Interfacing Data Manual which is supplied with the instrument. That document should be referred to if a further systems understanding is desired.

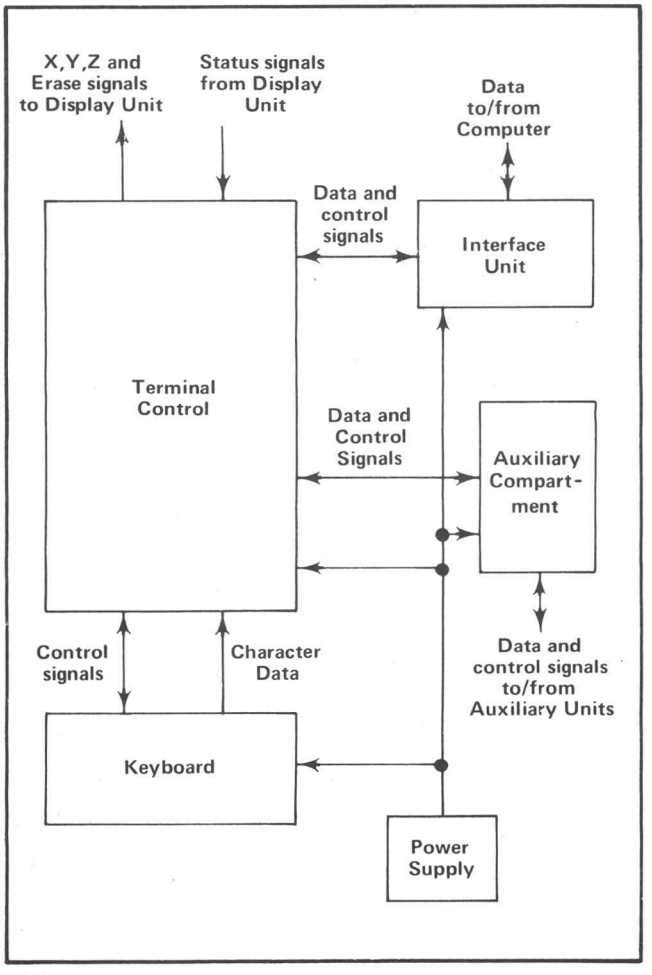

Fig. 1-2. Electrical relationship of Drawer Unit.

The 4002A Drawer Unit contains the following principal sections: Keyboard Interface Unit, Terminal Control, and Power Supply. In addition, a compartment is provided for installation of auxiliary devices, such as the Tektronix 4901 and 4902 Interactive Graphic Units. The location of the various sections is illustrated in Fig. 1-3.

Keyboard. The Keyboard Assembly contains the keys and circuitry necessary for generating characters and commands for operating the Terminal and transmitting data. Individual keys and circuit components are readily accessible for servicing.

Interface Units. The specific Interface Unit used in the 4002A is dependent upon the equipment with which the 4002A is being used. Since any one of several Interface Units may be a part of the Drawer Unit in a given instance, the Interface Units have their separate manuals and are not discussed in detail here.

Terminal Control. This section of the Drawer Unit accepts information from the Interface Unit, the Keyboard, or from any auxiliary device which may be installed and enabled. The Terminal Control then evaluates the information and controls the Terminal as directed by the data. Some of its specific functions are: 1) decode input data; 2) effect mode changes; 3) control position of the display; 4) command an integral character generator to provide beam-unblanking and position-modifying data as necessary to write characters; and 5) indicate readiness condition for sending or receiving data.

Power Supply. The power supply voltages required by the Interface Unit, Terminal Control, Auxiliary Unit, and Keyboard are supplied by the Power Supply unit, which is located in the Drawer Unit. The Drawer Unit does not supply power (other than that required for signal transfer) to the Display Unit.

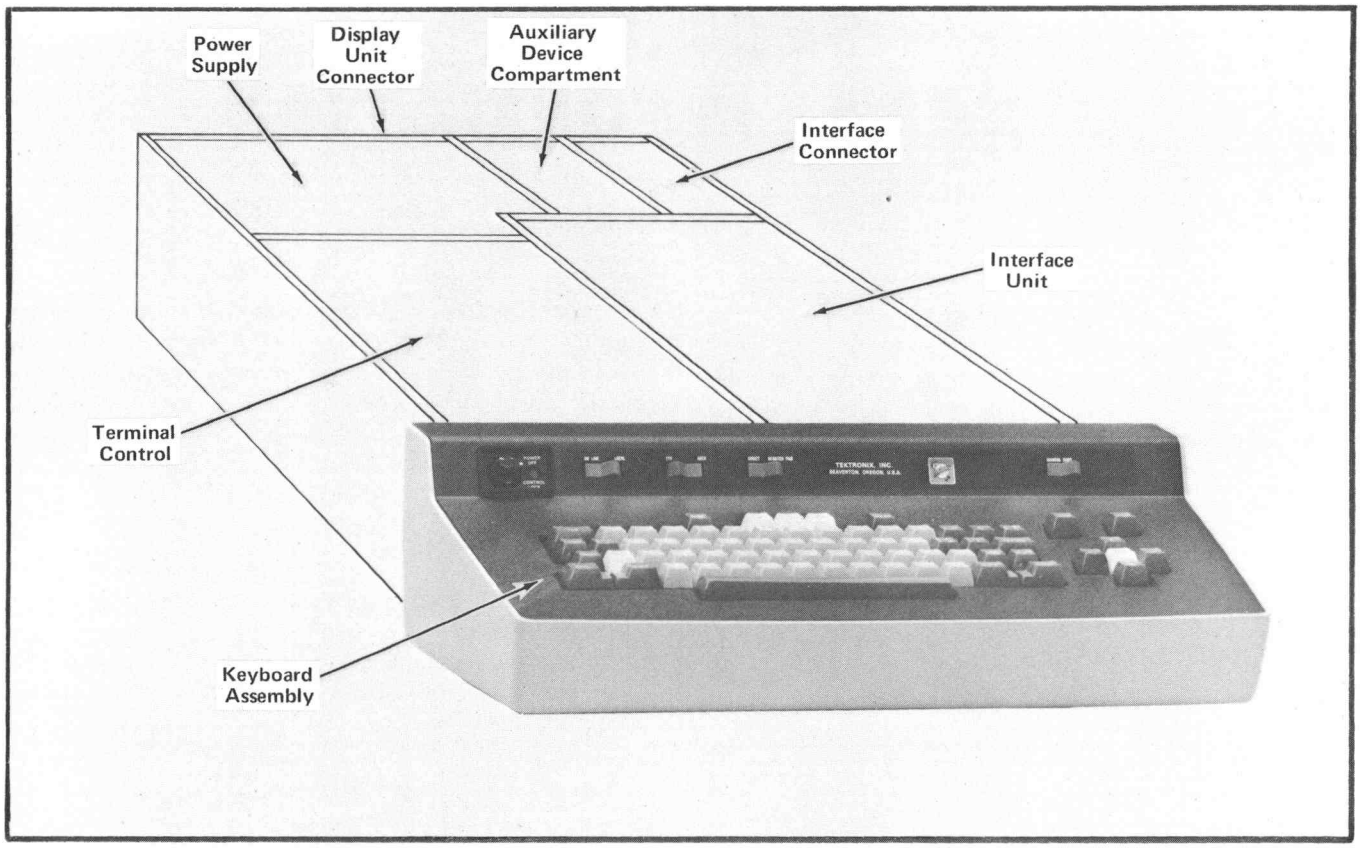

Fig. 1-3. Principal sections of the Drawer Unit.

BLOCK DIAGRAM DESCRIPTIONS

Operation of the Terminal varies with the mode selected. Block diagrams of the principal modes are contained in the Diagrams section of this manual, and include written descriptions as follows:

Transmitting—On Line-Direct; Echoing not in effect

Receiving—On Line-Direct-Incremental Plot Mode

Receiving—On Line-Direct-Point Plot Mode

Receiving—On Line-Direct-Linear Interpolate Mode

Receiving—On Line-Direct-Unrefreshed Scratch Pad Mode

Refreshed Scratch Pad Modes

Transmitting—On Line-Send; Echoing not in effect

Receiving—On Line-Direct-Alphanumeric Mode

Local Echo

Local Mode

CONNECTORS AND WIRE LISTS

A Connectors diagram appears in the Diagrams section to provide interconnecting data for the Drawer Unit. In addition, Wire Lists appear in the Diagrams section. These lists provide information on all connectors which are not included on the detailed schematic.

DICTIONARY OF LINE TITLES

This list appears in the Diagrams section, and is extremely beneficial as an aid to understanding the logic flow between circuit cards. The expanded name of each line and a brief explanation of it is included.

OPTIONS

A picture of each board containing an option or options appears in the Diagrams section. More details regarding these options are provided in the Specification and Interfacing Data Manual.

LOGIC INFORMATION

The logic levels in the Drawer Unit are listed in full in the Specification and Interfacing Data Manual, and are summarized here for convenience:

For inputs, logical 1 is +2.0 to +5.5 V; logical 0 is 0 to +0.8 V.

For outputs, logical 1 is +2.4 to +5.5 V; logical 0 is 0 to +0.4 V.

An exception to this exists in TC-14, where the MOS memory devices use higher levels. Refer to that schematic for actual values.

Examples of integrated circuit functions appear in an illustration in the Diagrams section. In addition, various combinations of these are used in the Drawer Unit to provide registers, counters, etc.

Signal lines are labeled in accordance with the functions they accomplish. The active state of the line is implied by the title given. For example, when in Compose mode, the COMPOSE line is high; when the linear interpolate circuit is busy, the $\overline{\text{LI BUSY}}$ line is low.

NOTES

NOTES

SECTION 2
DETAILED CIRCUIT DESCRIPTION

A detailed description of each circuit card is provided here. Table 2-1 provides a summary of the circuit cards and their functions.

Keyboard Logic TC-1

TC-1 contains keyboard control circuitry. This circuitry is contained on two separate schematics. Refer to TC-1, part 1, where the time delays will be discussed first. Input signals $\overline{\text{MGN SHF PB}}$, $\overline{\text{EDIT KY}}$, $\overline{\text{FULL KY}}$, $\overline{\text{SEND KY}}$, and $\overline{\text{BREAK KY}}$ are applied to sections of U57 and U19A. These time delay circuits normally have a high output. When a low signal is applied at the input, the outputs go low. They remain there until 10 ms after the low input has been removed. This 10 ms delay is a function of the resistor and capacitor connected to these time delay circuits, and is effectively equal to their RC time constant.

Time delay circuits are also associated with the $\overline{\text{CUR LFT KY}}$, $\overline{\text{CUR RT KY}}$, $\overline{\text{CUR DN KY}}$, $\overline{\text{CUR UP KY}}$ lines. When any one of the controlling keys is pressed momentarily, the resulting low causes a high output from either U59A or U59B. This high passes through steering diode CR155 or CR157, where it is felt through C158 into U19B and U19C. The differentiated pulse caused by C158 and R159 causes the U19B output to go high for 10 ms and the U19C output to go high for approximately 300 ms. The transistors at the outputs turn on during this high output pulse. While Q11 is turned on, C165 discharges quite rapidly through CR167. At the end of the 10 ms pulse, Q11 turns off. This causes the collector to go positive, causing a differentiated positive pulse to appear at the top of R166. This in turn causes U19D to put out a positive 2.5 μs pulse. This 2.5 μs pulse ANDs with the positive signal into U39D, U39B, U39A, or U39C to create any one of the four indicated low output signals. The signal duration is slaved to U19D, and therefore is 2.5 μs.

The output of U19C turned Q15 on at the same time that Q11 turned on. With Q15 turned on, a low is applied to the emitter of Q13, holding Q13 cut off. When the U19C 330 ms delay ends, Q15 cuts off. C175 is then permitted to charge through R175 until Q13 conducts. Conduction of Q13 discharges C175, and at the same time provides a positive pulse into pin 13 of U19D. This creates a 2.5 μs output from U19D, occuring approximately 320 ms after the one caused by U19B. If the input signal still exists when this 330 ms time delay elapses, the 2.5 μs pulse from U19D ANDs with a high into one of the four NAND gates to create another 2.5 μs pulse on the appropriate output line. Q15 remains cut off, and Q13 cuts off as soon as C175 has discharged through R178 and the gate junction of Q13. C175 again charges positive until Q13 is again triggered into condution. Another pulse is generated across R178 and sent to U19D to generate another 2.5 μs output. If the input signal still exists, another 2.5 μs output pulse will be generated. This situation continues until the input signal is removed by releasing the control key.

C175 and Q13 continue to generate pulses at a 20 Hz rate as long as the Terminal is turned on. However, the output from this pulse generator can only be used while an input signal exists.

Since the 20 Hz output signal is delayed by U19C for 330 ms following the input of any one of the four previously mentioned signals, it permits an operator to strike one of the cursor keys and have only one position movement occur unless he elects to continue holding the key.

The Cursor Control circuit is designed for cursor right and cursor down operation upon receipt of the $\overline{\text{CUR RT KY}}$ or the $\overline{\text{CUR DN KY}}$ signal. At this time either the $\overline{\text{X CUR PULS}}$ or the $\overline{\text{Y CUR PULS}}$ will be generated. If left or upward movement is desired, two output signals occur. For example, the $\overline{\text{CUR LFT KY}}$ signal causes a $\overline{\text{CUR LFT}}$ signal as well as the $\overline{\text{X CUR PULS}}$ signal. Likewise, the $\overline{\text{CUR UP KY}}$ signal will cause a $\overline{\text{CUR UP}}$ signal as well as a $\overline{\text{Y CUR PULS}}$ signal.

The TC-1 part 2 schematic consists of the following circuits: View/Hold, Strobe and Repeat, KB Click, Bell Circuit, Initial and Home.

The View/Hold circuit is designed to permit viewing of a display for 60 to 120 seconds after the last input data has been processed by the Terminal in all modes except for Compose. (In Compose Mode, viewing is continuous.) When the 60 to 120 second period has elapsed, a $\overline{\text{HOLD}}$ signal is sent out to cause the display intensity to drop below the

TABLE 2-1

Summary of Circuit Cards

Number	Name	Principal Function(s)
TC-1	Keyboard Logic	Provide delays to Keyboard signals; Control repetitive cursor shift signals; Control Keyboard lights, click and bell
TC-2	Output Data Selector	Control which input is to provide output data; Provide clock signal and character strobe signals
TC-4	Scratch Pad Control	Control Scratch Pad operation. A bypass card can be substituted if Scratch Pad operation is not required
TC-5	Scratch Pad Counter	Performs Scratch Pad character and cursor counting functions; controls other details essential to Scratch Pad operation. A bypass card can be substituted if Scratch Pad operation is not required
TC-6	Horizontal Tab	Provides horizontal tab control from keyboard or program; card not essential to Terminal operation
TC-7	Control Function Decoder	Decodes control characters and special functions for use by the Terminal and associated equipment
TC-8	Character Rotator	An optional circuit card which provides character rotation in 90° increments. A bypass card is supplied as standard equipment.
TC-9	Y D/A	Converts the output of the Y data register to analog voltage; also sums it with modifying voltages for character writing
TC-10	Y Data Register	Controls the Y address of the CRT beam position
TC-11	In/Out Data Routing	Directs data to and from Interface Unit; also contains the Graphic Word Assembler
TC-12	X Data Register	Controls the X address of the CRT beam position
TC-13	X D/A	Converts the output of the X Data Register to analog voltage; also sums it with modifying voltage for character writing
TC-14	Internal Data Routing	Contains Scratch Pad memory circuits and devices for routing data around or through the memory
TC-15	Character Generator Control	Controls alphanumeric character and cursor writing
TC-16	Character Generator Memory	Contains ROM and circuitry for generating character matrix
TC-18	Plot Control	Controls the various graphic operations
TC-19	I/O Control	Controls the input and output of the Terminal, interacting with the Interface Unit

viewing level, thus prolonging tube life. Whenever data is processed by the Terminal or whenever appropriate keys are pressed, the $\overline{\text{HOLD}}$ signal is removed and a $\overline{\text{VIEW}}$ signal is generated to permit another 60 to 120 second viewing period. Just before the $\overline{\text{HOLD}}$ signal is generated, the View Lamp pulsates to warn of the impending Hold Mode. This permits the operator to reset the circuit for another 60 to 120 seconds before it drops into the Hold Mode.

Operation is as follows: Assume that either a $\overline{\text{VIEW KY}}$ or a $\overline{\text{RSET VIEW}}$ signal has just been received. It is applied to U95, where it generates a positive 60 to 120 second output pulse. This pulse is applied to U87 to reset that counter circuit, and is also applied to Q93 to hold it in conduction. With Q93 in conduction, its collector holds the gate of Q91 low to keep that device turned off. When the delay period has elapsed, the output of U95 returns low, releasing U87 and turning Q93 off. With Q93 turned off, C20 charges until it places Q91 in conduction momentarily. C20 then discharges through L24 and the gate junction of Q91. Q91 then again turns off, permitting C20 to go into another charge cycle.

Each time Q91 turns on, it applies a positive pulse to U87. The trailing edge of this pulse advances the U87 count by one. The $\overline{\text{VIEW LMP}}$ signal is caused by the ÷ 2 output of U87, and causes the lamp to blink 7 times until all four outputs from U87 go high. The output of U85B then goes low, and applies a high through R12 to Q93. Q93 conducts and shorts out C20, holding Q91 cut off. The low out of U85B becomes the $\overline{\text{HOLD}}$ signal. It is inverted by Q71 to place a high on the $\overline{\text{VIEW}}$ line. The $\overline{\text{VIEW LMP}}$ output is held low until another viewing cycle is commanded.

The Strobe and Repeat circuit operates to provide an RKB STROB signal each time a keyboard character is actuated. If the Repeat key is held down while a key is held down, the circuit causes repetitive RKB STROB signals to be generated at a 20 Hz rate.

When a RAW STROB is received, it is applied to U85A, whose other outputs are normally held high. The low from U85A passes through U1B and becomes RKB STROB. Under this circumstance, the RKB STROB duplicates the RAW STROB. If a Keyboard key is held down continuously, the RAW STROB remains high and holds the RKB STROB high. However, if the Repeat key is held down, the $\overline{\text{RPT KY}}$ input turns Q1 off, placing a high at the Q3 gate. C33 charges through R33 until Q3 goes into conduction. This permits C33 to discharge through L37 and the Q3 gate junction. When C33 discharges sufficiently, Q3 again turns off and C33 starts another charge cycle. The positive pulse that occurs when Q3 goes into conduction is applied to U23A, where its trailing edge causes U23A to change states. The U23A configuration is such that its pin 5 output changes state for each input pulse from Q3. This results in the pin 1 input of U85A going alternately low and high at a 10 Hz rate. This causes the RKB STROB output to be interrupted ten times a second, even though the RAW STROB input signal remains high.

KB Click Circuit. The outputs from U85A are also applied to the input of U5. Each negative input into U5 causes it to deliver a 200 μs (approximate) positive pulse through R5 and R42 to the Bell circuit. This causes the output speaker to emit a short pulse, or "click".

Bell Circuit. The Bell circuit can be separated into three sub-circuits . . . . the Multivibrator, the Gating section and the Amplifier. The Multivibrator is a unijunction diode controlling a D latch to generate push-pull output signals. The pulses from Q45 causes the U23B outputs to continuously change state. The push-pull outputs of U23B are applied to opposite sides of output transistors Q47 and Q49. Except when a Bell signal has been commanded, Q47 and Q49 are without current, and the push-pull outputs from U23B can go no further. However, when a $\overline{\text{BEL X}}$ or a $\overline{\text{RING}}$ signal is received, it causes the U83A output to go low, turning Q53 on. This provides drive to Q51, supplying current to Q47 and Q49. Q47 and Q49 alternately turn on and off, supplying the Bell signal to the operational amplifier circuit. The operational amplifier drives the BELL SPKR line, producing an audible output.

When the $\overline{\text{BEL X}}$ or $\overline{\text{RING}}$ signal is made available to U83B, it not only turns Q53 and Q51 on, it also provides drive to Q63. When Q63 turns on, its low output provides a low to U83A. This causes U83A to produce a high output, which turns Q53 off. During the time that Q53 was turned on, C96 accumulated a charge. With Q53 turned off, the long time constant of C96-R96 holds Q51 in conduction for about one-half second. Then Q51 turns off, ending the audible output.

Initial and Home Circuit. The object of this circuit is to provide an $\overline{\text{INITIAL}}$ signal at turn-on, and to generate a $\overline{\text{HOME}}$ signal whenever a $\overline{\text{HOME KY}}$ signal is received. At turn-on, the +5 V supply builds up, applying a positive voltage to the base of Q41. Until C101 charges, it holds Q41 cut off. This holds Q43 cut off, applying a high to U1C and a low to U81A and U81B. While this condition exists, a $\overline{\text{HOME}}$ and an $\overline{\text{INITIAL}}$ signal occur. Approximately 100 ms later, C101 is charged sufficiently to place Q41 in conduction, causing Q43 to conduct. This removes the high from U1C, ending the output pulses.

Output Data Selector TC-2 (Circuit Card 670-1436-01)

The Output Data Selector circuit card performs several functions. It provides clock signals, develops a KB STROB, a FUNC COMP signal, a DATA STRB signal, and makes data bits available to the rest of the Terminal. The circuits that perform these functions are the Clock circuit, the KB Strobe circuit, the Function Complete circuit, Multiplexer Control circuit, Data Multiplexers, the Data Strobe circuit, and the TTY DEL and Closing Bracket Control circuit.

Clock Circuit. The 4 MHz signal developed by the crystal-controlled multivibrator is applied to U13E, which provides a square wave through U13D to clock the U15A and U15B flip-flops. U15A divides the 4 MHz by 2 to provide a symmetrical 2 MHz clock for the rest of the Terminal. The output of U15A is also sent to U15B, where it is again divided by 2 to provide a 1 MHz clock.

Keyboard Strobe Circuit. When a keyboard character is struck, the RKB STROB line goes high. The low from U11C one-sets U37B. The next negative transition of the 1 MHz clock one-sets U39A, generating KB STROBE. The next 1 MHz negative transition one-sets U39B, causing it to zero-set U37B. The next 1 MHz negative transition zero-sets U39A, placing a low on the J input of U39B. U39B then has lows on the J and K inputs and remains in the one-set condition until zero-set (via U7A) by the Function Complete circuit.

Function Complete Circuit. The Function Complete circuit consists of several negative input OR gates which respond to any one of a number of low input signals. Two outputs are derived from this circuit; one is the FUNC COMP signal, and the other is a signal for resetting the KB Strobe circuit. Any one of the six input signals can cause a reset signal to be sent to the KB Strobe circuit. All except the $\overline{\text{XMIT COMP}}$ signal cause a FUNC COMP signal to be generated.

Multiplexers. These devices are provided with A and B control signals to determine which input data (C0, C1, C2) will control the output of its respective section. BA combinations of 00, 01, 10 will engage C0, C1, C2 respectively.

Multiplexer Control Circuit. This circuit provides two signals to each of the multiplexers, determining which input will control the outputs. When a keyboard signal is entered, the KB STROBE causes a low from U35C, which causes a low from U5B. The U5A output remains high. This combination permits keyboard input data (KB1, etc) to appear at the output of the multiplexers.

During Scratch Pad Send operation, SEND goes high and applies lows to the A and B inputs of the multiplexers, causing Scratch Pad data (SP1, etc) to leave the multiplexers.

In auxiliary operation, $\overline{\text{IN AUX}}$ is low. AUX STROB generates a low from U35A, which places a low on the B inputs while the A inputs remains high. Auxiliary data (A1, etc) then passes through the multiplexers.

Data Strobe Circuit. The Data Strobe Circuit provides a DATA STRB whenever Keyboard or Auxiliary data is being passed through the multiplexers. During Scratch Pad transmission, $\overline{\text{SP XMT STR}}$ must go low to cause DATA STRB.

TTY DEL and Closing Bracket Control Circuit. The purpose of this circuit is to limit the output during TTY operation so that output bit B6 remains low at all times except when the character DEL or Closing Bracket is being transmitted. In essence, the circuit has no effect when TTY is low. Notice that TTY is applied to U35B. If it is low, it causes U35B to have a high output, causing the U5C output to follow the KB6 input. Since the U5C output is applied to the 2C2 input of U27, it has the effect of applying KB6 directly to the multiplexer.

When Teletype Mode is selected, TTY is high. Now U35B is controlled either by the KB7 input or by the U31A output. The B6 output follows the KB6 input as long as KB7 is low. When KB7 is high, the U35B output can only go high when the KB1, KB3, KB4, KB5, and KB6 combination indicates that a DEL or Closing Bracket is being generated. During those times, the U31A output goes low, causing U35B to place a high on U5C, permitting KB6 to again control the B6 output via U5C and U27.

Output Data Selector TC-2 (Circuit Card 670-1436-00)

The Output Data Selector circuit card performs several functions. It provides clock signals, develops a KB STROB, a FUNC COMP signal, a DATA STRB signal, and makes data bits available to the rest of the Terminal. The circuits that perform these functions are the Clock circuit, the KB Strobe circuit, the Function Complete circuit, Gate Enabling circuit, Keyboard Input Gates, AUX Input Gates, Scratch Pad Send Gates, the Data Strobe circuit and the TTY DEL and Closing Bracket Control circuit.

Clock Circuit. The 4 MHz signal developed by the crystal-controlled multivibrator is applied to Q7, which provides a square wave through U7A to clock the U35A and U35B flip-flops. U35A divides the 4 MHz by 2 to provide a symmetrical 2 MHz clock for the rest of the Terminal. The output of U35A is also sent to U35B, where it is again divided by 2 to provide a 1 MHz clock.

KB Strobe Circuit. When a keyboard character is struck, the RKB STROB line goes high and combines with the other three highs on U55 to provide a low output. This causes U13A to become one-set. The next negative-going excursion of the 1 MHz clock pulse causes U15 to become one-set, causing the KB STROB line to go high. The next negative transition of the 1 MHz clock pulse zero-sets U15 and one-sets U13B. The zero output from U13B goes to U15, where it disables U15 in the zero-set condition. U13B now has two low inputs and remains in its one-set condition. The next positive excursion of the 1 MHz clock causes U33D to provide a low output, which zero-sets U13A to prepare it for the next input signal. U13B remains in its one-set condition until such time as the Function Complete circuit provides it with a zero-setting signal.

Function Complete Circuit. The Function Complete circuit consists of several negative input OR gates which respond to any one of a number of low input signals. Two outputs are derived from this circuit; one is the FUNC COMP signal, and the other is a signal for resetting the KB Strobe circuit. Any one of the six input signals can cause a reset signal to be sent to the KB Strobe circuit. All except the $\overline{\text{XMIT COMP}}$ signal cause a FUNC COMP signal to be generated.

Gate Enabling Circuit. The Gate Enabling circuit permits one of the three sets of gates to be enabled at a given time. The SEND input signal takes precedence. Whenever it exists, it enables the Scratch Pad Send Gates and disables the KB Input Gates and the Aux Input Gates.

When the SEND signal is low and IN KB AUX signal exists, U9A has two high inputs. Just before a KB STROB is developed in response to an RKB STROB, U13A applies another high signal to U9A. This sends a high to the KB Input Gates, permitting KB Data bits to pass through the input gates.

Two highs exist on U9C if SEND and $\overline{\text{IN AUX}}$ are low. When an AUX STROB arrives at the circuit, U9C provides a low output, causing U11C to place a high on the Aux Input Gates. The auxiliary data bits are then permitted to pass through.

Data Strobe Circuit. The Data Strobe Circuit provides a DATA STRB whenever data is being passed through any one of the three input gate circuits. When keyboard data is being input, highs are applied to U33A during KB STROB time, sending a low to U51A to generate the DATA STRB signal. When auxiliary inputs are being provided, the AUX STROB causes U33B to generate the DATA STRB. During Scratch Pad transmission, the low SP XMT STR signal causes the DATA STRB.

TTY DEL and Closing Bracket Control Circuit. The purpose of this circuit is to limit the output during TTY operation so that output bit B6 remains low at all times except when the character DEL or Closing Bracket is being transmitted. In essence, the circuit has no effect when TTY is low. Notice that TTY is applied to U9B. If it is low, it causes U9B to have a high output, causing the U7C output to follow the KB6 input. Since the U7C output is applied to U27D, it has the effect of applying KB6 directly to U27D.

When Teletype Mode is selected, TTY is high. Now U9B is controlled either by the KB7 input or by the U1 output. The B6 output follows the KB6 input as long as KB7 is low. When KB7 is high, the U9B output can only go high when the KB1, KB3, KB4, KB5, and KB6 combination indicates that a DEL or Closing Bracket is being generated. During those times, the U1 output goes low, causing U9B to place a high on U7D, permitting KB6 to again control the B6 output via U7D, U7C, and U27D.

Scratch Pad Control TC-4

This circuit card contains most of the circuitry for controlling the Scratch Pad features of the Terminal. When the Scratch Pad has not been selected at the keyboard or by program control, it is essentially a bypass card, and can be represented by the Scratch Pad Bypass drawing which appears on the schematic.

When in Compose Mode, most of the circuitry on the card is interactive, and therefore will be explained as part of an operating sequence rather than an individual circuits.

Refreshed Compose Operation. When the switch on the keyboard is placed in the Compose position, the $\overline{\text{COMP SW}}$ line goes low, placing an enabling voltage on U53B. The first time a character is entered at the keyboard, its KB STROB sends a signal into U53B to create a high output, causing refresh FF U27A to become one-set. This causes several things to happen. One of these is the generation of the REFRSH signal and the placing of a low on the SP KSE line. This disables the generation of KB STROB signals until an $\overline{\text{AGREE}}$ signal is received by the circuit. The Refresh FF also sends out a low which enables the ÷ 256 counter circuit, causes a high on the COMPOSE line, and a low on the $\overline{\text{COMPOSE}}$ line.

One of the functions of the COMPOSE signal is to enable ÷ 256 output gate U37C. Since the counter is being driven by the 1 MHz clock signal, an output pulse is developed once every 256 microseconds. This pulse passes through U11A and U51A to one-set the MOS CLK Enable FF. The next eight 1 MHz pulses cause U15D to generate eight MOS CLK pulses by way of U14B. These pulses are also applied to ÷ 8 counter U58. At the end of the seventh MOS CLK pulse, the inputs to U38B all go high. The U38B output goes low, creating the $\overline{\text{SP EXEC}}$ pulse. This pulse is also applied to U17D, placing a high at the J input of SP Exec Arm FF U18A. When the eighth MOS CLK pulse ends, U58 advances to zero. Feedback from U58 to the MOS CLK Enable FF U13A causes it to become zero-set, disabling the MOS CLK Gate.

The negative-going transition of the 1 MHz clock that ended the eighth MOS CLK pulse also caused U18A to shift to its one-set condition. This placed enabling voltages on the SP EXEC FF U7A and on U39C. It was also applied to U15C, causing a low to appear on the $\overline{\text{CC CNT UP}}$ line. The next positive pulse on the 1 MHz line causes the SP STROB to be generated. When the 1 MHz line again goes low, it one-sets the SP EXEC FF U7A and zero-sets SP EXEC ARM FF U18A. When SP EXEC FF U7A one-sets, it generates a low at pin 13, causing U19A to generate an SP EXEC signal. The zero-setting of U18A causes the enabling voltages to be removed from SP EXEC FF U7A and from U39C. It also causes U18B to become one-set, ending the $\overline{\text{CC CNT UP}}$ pulse. U18B now remains in its one-set condition until more data is inserted, as indicated by the TC IN STRB signal.

As long as no additional data is inserted and no mode changes are made, the Scratch Pad Control card continues to send out 8 MOS CLK pulses every 256 microseconds, and it receives an $\overline{\text{AGREE}}$ pulse each time the Position Counter and Cursor Counter agree. This $\overline{\text{AGREE}}$ signal passes through U38C, U39B, and U59C to create an SP KSE signal which is used to permit the keyboard to generate additional character strobes. In this manner, the keyboard is permitted to insert characters only when the Cursor Position is loaded in the Data Shift Register on TC-14.

Cursor Counter Count-Up Circuit. This circuit controls the device in TC-5 which remembers the cursor position in the Scratch Pad Memory. Each time a character is inserted into memory, a TC IN STRB arrives at U33D, causing a low output from this device. This causes a low into U38A, placing a high on U35A and a low on the CC CNT UP FF U18B. U18B becomes zero-set. At the same time, the TC IN STRB generates a CL SET ARM signal via U33D, U17, U35B and U33B. This CL SET ARM signal permits the character to be stored into the Scratch Pad Memory circuit. The CC CNT UP FF becomes one-set at the end of the series of MOS CLK pulses. This causes the $\overline{\text{CC CNT UP}}$ signal line to return high. When $\overline{\text{CC CNT UP}}$ goes high, the Cursor Counter in TC-5 increments by one to indicate the new cursor position.

Edit Control. When in Compose Mode, a high is applied to the J input of the Edit FF U7B. When Edit Mode is selected, the $\overline{\text{EDIT}}$ line pulses low, causing U5B to produce a low output pulse on the $\overline{\text{CS LOAD}}$ line. This causes the Cursor Counter contents to be stored in the Cursor Storage Register, so that the Cursor position at the time of entering Edit Mode can be remembered. When the $\overline{\text{EDIT}}$ line returns high, the Edit FF becomes one-set, disabling U5B and providing U9B with enabling voltage. When the Edit button is again pushed to exit from the Edit Mode, U5D applies a high to U9B to generate the $\overline{\text{CC LOAD}}$ signal. The information in the Cursor Storage Register (on TC-5) is then loaded into the Cursor Counter Register.

Insert Operation. Assume that the Terminal is in Compose Mode and that Edit Operation has been selected. When the Insert Key is pushed, the $\overline{\text{INSERT}}$ signal into U25B applies a high to U43B. With the Edit FF one-set, U43B has two highs applied. When a keyboard character is entered, the DATA STRB causes the U43B output to go low, generating a COUNT UP signal. This goes to the Cursor Storage Register in TC-5, causing it to increase its count by one. The Cursor Storage Register therefore accounts for the insertion of an additional character in memory. The rest of the circuitry operates just as though a normal character insertion were being made.

Delete Operation. Edit Mode must again exist and the Edit FF must be one-set. With the delete button held down, U43C in the Count Down circuit has two high enabling voltages applied. When a keyboard character is entered and DATA STRB is received, the U43C output goes low, causing a COUNT DWN signal to be generated and sent to TC-5. This causes the Cursor Storage Counter to decrement by one, accounting for the removal of one character from memory. The output of U43C is also applied to U35D, applying a high to CC Count Down gate U35C. U35C then generates a low CC CNT DWN pulse which compensates for the $\overline{\text{CC CNT UP}}$ pulse generated by U18B.

Clearing the Scratch Pad Memory. When a $\overline{\text{FULL}}$ signal is received from the keyboard while in Compose Mode, U19B generates a high output which causes U31 to develop 1 ms high and low output pulses on pins 8 and 6 respectively. The low pulse is felt through MOS CLK Enable Gate U11A and U51A to hold U13A one-set for that period of time, permitting continuous generation of 1 MHz MOS CLK pulses. At the same time, U31 sends its low 1 millisecond pulse out as a $\overline{\text{CLEAR}}$ signal to TC-5. The TC-5 circuitry generates the actual signals necessary for clearing the memory circuit, and also generates an INITIAL signal which is returned to TC-4 to insure that EDIT FF U7B is in its zero-set condition.

The high 1 ms pulse from pin 8 of U31 holds the outputs of ÷ 8 counter U58 at zero, inhibiting $\overline{\text{SP EXEC}}$, SP EXEC and SP STROB signals while the Scratch Pad memory is being cleared.

When the 1 ms clearing pulse ends, it is removed from U13A pin 2. C14 causes a delay in removal of the pulse from U13A pin 3. This zero-sets U13A and inhibits additional MOS CLK pulses.

Send Operation. When the keyboard Send button is pushed, the memory circuit continues to cycle until the first character is in the Shift Register position. TC-4 then receives an $\overline{\text{SP SEND}}$ signal, placing a disabling voltage on SP KSE gate U39B. This prevents characters from being entered at the keyboard. The $\overline{\text{SP SEND}}$ signal also goes to U59F in the SP Send Complete circuit, to place enabling voltage on U9D. $\overline{\text{SP SEND}}$ also is applied to U45A in the Reset circuit placing a high on U25F, causing that device to zero-set the Refresh FF. This causes the COMPOSE line to go low and the $\overline{\text{COMPOSE}}$ line to go high. Since the zero output of the Refresh FF was being applied through U15A to enable the ÷ 256 circuit, that circuit becomes disabled. MOS CLK enabling pulses now are dependent upon the output of U9D in the SP SEND Complete circuit.

As soon as the character in the Shift Register is accepted by the computer (or by the Terminal in case of Local Mode), an $\overline{\text{XMIT COMP}}$ signal is received by TC-4. This causes U25C, U5A, U9A, and U9D to deliver a low pulse to MOS CLK ENABLE GATE U11A. Eight MOS CLK pulses are delivered to cycle the next character in memory into the Shift Register. The process is repeated as often as is necessary to deliver all characters to the computer or Terminal. The $\overline{\text{SP SEND}}$ line then goes high and the Terminal returns to Direct Mode.

Program Control of the Scratch Pad. Program commands can put the Scratch Pad into Unrefreshed Mode. Additional program commands can then shift the Terminal into Refreshed Mode, Refreshed Edit Mode, or can clear the Scratch Pad Memory circuit. It should be noted that these three functions can be programmed into the Terminal only after the Terminal has been placed in the Unrefreshed Scratch Pad Mode.

Assume that the Terminal has just received the character ESC accompanied by the TC IN STRB. The combination of these causes a low output from U21, a high output from U45B, and the one-setting of Arm FF U47B. This places enabling voltages on Unrefreshed SP FF U47A, on EDIT SELECT gate U53D, and on Clear Select gate U53C. If the next input character is US, it causes U47A to clock to its one-set condition, setting up Unrefreshed Scratch Pad operation. The TC IN STRB which accompanies the US character is applied through U45D to return Arm FF U47B to its zero-set condition. The resetting of the ARM FF occurs regardless of the input character. IF the character is not a US, the FF becomes disarmed with no effect on the Program Control circuit. (Note that the Unrefreshed SP FF can also be one-set by a $\overline{\text{LOAD DATA}}$ signal from the Interface Unit, if the Interface Unit is equipped for this type of operation.)

With U47A one-set, highs are applied to SP Exec gate U19A, Refreshed Scratch Pad gate U45C, and flip-flop U49A. At the same time, U47A applies low to U15A and U11B. This causes a COMPOSE signal to be generated, but holds a disabling voltage on the ÷ 256 output gate U11B. Data can now be loaded into the Scratch Pad Memory at a very rapid rate in the following manner: The TC IN STRB which accompanies input data is routed through U33D, U17, U35B, U38A, and U35A to zero-set CC CNT UP FF U18B. This strobe also is routed from U35B through U33B to generate the CL SET ARM signal. This signal goes to TC-5, where it causes the SET signal to be generated and returned to TC-4. When the SET pulse ends, U49A becomes one-set. The next 1 MHz pulse one-sets U49B, generating a low output at pin 8. This low output zero-sets U49A. The output from U49B generates an $\overline{\text{SP COMP}}$ signal which is sent to TC-14. This signal is also used internally on TC-4 in the U11A gate circuit. The resulting high output from U11A causes a low from U51A, which one-sets MOS CLK ENABLE FF U13A. Eight MOS CLK pulses now are generated, after which the $\overline{\text{CC CNT UP}}$ signal is sent to TC-5 to increment the Cursor Counter by one. Although a pulse is applied to SP EXEC gate U19A, no output occurs because pin 3 is held disabled by Unrefreshed SP FF U47A. The circuit remains in this condition until another TC IN STRB and accompanying data is received from the Interface Unit.

When program commands are used to shift the Terminal to Compose Mode (Refreshed Scratch Pad), the control character EOT is sent to the Terminal and detected by EOT Detector U1. U1 sends a signal through U29A, U45C, U51E, and U53A to one-set Refresh FF U27A. Compose operation is then essentially as previously explained.

If it is desired to shift from Unrefreshed Scratch Pad operation to Edit Mode under program control, the characters ESC ? must be sent to Terminal. The ESC character arms the U47B FF as previously explained and the ? character causes a signal to be routed through U2, U53D, and U51F to set the U33A output high. The high is blocked from U29A by CR22. After the ? is loaded into the memory, eight MOS CLK pulses occur and U7A develops a low output which goes to U43A to set the U33A output low. This low is felt at U29A, sending a signal through U45C, U51E and U53A to one-set Refresh FF U27A. The U33A output is also routed through U53D and U51F to the Edit Control circuit to one-set EDIT FF U7B. Edit operation is then as previously explained.

Program command sequence ESC C clears the Scratch Pad memory if in Unrefreshed Mode. ESC arms the U47B FF and the C causes a signal to pass through U23, Clear Select gate U53C, U14A and into U31 where it generates a 1 ms pulse. This 1 ms pulse affects the circuit in the same manner as previously explained.

Certain Interface Units are capable of causing the Unrefreshed Scratch Pad contents to be sent directly to the Terminal screen. This is accomplished by sending a $\overline{\text{SEND SCRN}}$ signal to TC-4 and TC-5. The $\overline{\text{SEND SCRN}}$ signal into TC-4 causes Send Screen FF U27B to one-set, enabling U15B and turning Q5 on. U15B sends out an $\overline{\text{INHIBIT X}}$ signal. Q5 disables U5A and enables U5C. $\overline{\text{SEND SCRN}}$ is also routed through U29A, U45C, U51E, and U53A to one-set Refresh FF U27A. As soon as the first character in memory is contained in the Shift Register, an $\overline{\text{SP SEND}}$ signal is received from TC-5. The $\overline{\text{SP SEND}}$ signal goes through U45A and U25F to zero-set U27A. $\overline{\text{SP SEND}}$ also goes through U59F to place an enabling voltage on U9D.

TC-2 sends a FUNC COMP signal to TC-4 to acknowledge receipt of the data transmitted by the Scratch Pad. This is applied to U5C. The output from U5C is routed through U9A and U9D to place a low pulse on MOS CLK Enable gate U11A. This results in eight MOS CLK pulses, which advance the next character into the Shift Register. An SP STROB and an SP EXEC signal follow the MOS CLK pulses. Another character is transmitted to the SCREEN and the operation is repeated until all characters are transmitted. The $\overline{\text{SP SEND}}$ signal then goes high, causing SEND SCREEN FF U27B to return to its zero-set condition. Q5 cuts off and U5C becomes disabled.

The Terminal can also be switched from the Unrefreshed Scratch Pad Mode to the Direct Mode by pressing the Home button. The $\overline{\text{HOME}}$ signal is applied to U14C. As soon as the Position Counter agrees with the Cursor Counter (on TC-5), $\overline{\text{AGREE}}$ is received by TC-4, causing a signal from U14C and U59E. This is routed to both the Refresh SP FF and the Unrefreshed SP FF, resetting them for Direct Mode operation.

Scratch Pad Counter TC-5

The Scratch Pad Counter circuit contains the Position Counter Registers, the Cursor Counter Registers, and the Cursor Storage Registers which are used in conjunction with the Scratch Pad Memory circuit. Other circuitry dependent upon these counters is also included on this diagram. When the Scratch Pad circuit is not in use, the card can be represented as the Scratch Pad Counter Bypass card, which is also shown on the schematic diagram.

As soon as the Terminal has been initialized, the $\overline{\text{INITIAL}}$ signal received on TC-5 resets the circuitry. When the Terminal is placed in Refreshed Compose Mode, $\overline{\text{SP EXEC}}$ signals are received continuously every 256 microseconds. Each one of these is routed through U43E and U45A to the Position Counter circuit.

The purpose of the Position Counters is to count the Scratch Pad Memory character position which is contained in the Shift Register on TC-14, and it is incremented every time that an $\overline{\text{SP EXEC}}$ signal is received. The Cursor Counter is incremented each time a character is inserted into the Scratch Pad Memory circuit. The $\overline{\text{CC CNT UP}}$ signal is passed through Cursor Count Up Disable gate U47B and through U29C to increment the counter. Assume that thirty characters have been stored in the Scratch Pad Memory. The Cursor Counter would contain the digital equivalent of thirty. Each time the Position Counter reaches that value, the A=B output of comparator U5 would cause U49D to generate the $\overline{\text{AGREE}}$ signal.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-01 and above. If an insert condition does not exist, low pulses are generated by U55B and U13B each time the Position Counters reach one hundred. (If insert conditions exists, U13B generates a low output when the Position Counter reaches 101. This accounts for the added Insert shift register on TC-14.) The U53B output forms the $\overline{\text{RSET INS}}$ signal, while the U13B output is processed through the TC-5 circuit as an "end of memory" signal. This signal causes a high to be applied to the J input of U35A. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal causes U35A to one-set. This causes several things to happen. The one output provides enabling voltage to U55A and U59D. The low from the zero output goes to U55B to disable it, and goes to U13A to reset the position counters to zero. The low from U35A also goes to U5 during this time to inhibit $\overline{\text{AGREE}}$ signals. (With pin 1 high and pin 15 low, the comparator cannot generate an $\overline{\text{AGREE}}$ output.) When $\overline{\text{SP EXEC}}$ returns high, it generates an $\overline{\text{SP RSET X}}$ from U55A and a $\overline{\text{DC PAUSE}}$ from U59D. $\overline{\text{SP RSET X}}$ goes to TC-12 to reset the X registers. $\overline{\text{DO PAUSE}}$ goes to TC-4 to inhibit MOS CLK pulses. It is also used in TC-5 circuitry

to zero-set U35B (to inhibit SP EXEC X pulses) and to one-set U17A if the $\overline{\text{SEND}}$ signal is low. (Send operation is discussed later.) U17A is normally zero-set, supplying enabling voltages to U37D and U55B. The U37D output is thus held low, supplying an $\overline{\text{SP STRIP}}$ signal to hold the display in the scratch pad area of the display. The next $\overline{\text{SP EXEC}}$ pulse ends the $\overline{\text{DO PAUSE}}$ signal from U59D, ends the $\overline{\text{SP RSET X}}$ pulse from U55A, and zero-sets U35A. When $\overline{\text{DO PAUSE}}$ ends, it releases U35B. When U35A zero-sets, its zero output puts a high on U55B. The one output from U35A one sets U51A to permit Send operation, if it had been ordered by a $\overline{\text{SEND}}$ signal. Each subsequent SP EXEC pulse causes a low out of U55B. This low appears at the output of U19 eight 1 MHZ pulses later, generating an EXEC signal to permit writing the character in the Scratch Pad strip.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-00. If an insert condition does not exist, low pulses are generated by U55B and U13B each time the Position Counters reach one hundred. (If insert conditions exists, U13B generates a low output when the Position Counter reaches 101. This accounts for the added Insert shift register on TC-14.) The U55B output forms the $\overline{\text{RSET INS}}$ signal, while the U13B output is processed through the TC-5 circuit as an "end of memory" signal. This signal causes a high to be applied to the J input of U35A. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal causes U35A to one-set. This causes several things to happen. The first of these is that the zero output is applied to U13A to zero-set the Position Counters. This removes the highs from the output gates of the counters and removes the enabling high from pin J or U35A. With U35A one-set, U55A receives enabling voltage and generates an $\overline{\text{SP RSET X}}$ signal which goes to the X-Register to return it to zero position. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal returns U35A to its zero-set condition. This places an enabling voltage on U53B, permitting SP EXEC signals to control the output of that device. It also causes the Send Enable FF U51A to become one-set, thus initiating Send operation with the first character in Scratch Pad memory.

When Edit Mode is selected, a $\overline{\text{CS LOAD}}$ signal causes the Cursor Counter output to be loaded into the Cursor Storage circuit. This records the cursor count at the point where Edit Mode was selected, so that if Edit Send is to be accomplished, it can start from that position. It also occurs when the Terminal is shifted out of Scratch Pad Mode, so that the Cursor Counter can return to this value when the Terminal is switched back to Scratch Pad Mode.

If a character is inserted while the Terminal is in Edit Mode, a COUNT UP signal is applied to the Cursor Storage Register and $\overline{\text{CC CNT UP}}$ is applied to the Cursor Counter, permitting both counters to increment by one. If a character is deleted from memory while in Edit Mode, a COUNT DWN signal is received to decrement the Cursor Storage Register at the same time a $\overline{\text{CC CNT DWN}}$ signal is decrementing the Cursor Counter. Thus the Cursor Storage Registers are compensated for additions or deletions of characters. When the Terminal is switched from Edit to Compose Mode, a $\overline{\text{CC LOAD}}$ signal is applied to the Cursor Counters, causing them to change their values to that contained in the Cursor Storage circuit.

Notice that the Cursor Counter is provided with a Cursor Count Up Disable gate and a Cursor Count Dwn Disable gate. Count up is disabled when the registers contain a digital equivalent of 98, causing a FULL LITE signal to exist as well as the disabling feedback signal. Count down disabling occurs when the Cursor Zero-Position Detect Diodes all have low inputs, indicating that the Cursor Counter has reached a value of zero.

One other circuit associated with insertion of characters into memory is the Clear Set circuit. When a character is to be inserted, the CL SET ARM line goes high, enabling U51B. The next negative transition of the 1 MHz line causes U51B to become one-set, placing enabling voltages on Set and Clear gates U45C and U45D. With the 1 MHz line low, U45D generates a low output, causing the CLEAR signal to be sent to the Shift Registers. (The CLEAR signal insures that the Shift Register contains all zeros before the SET signal loads the new character data.) The next half microsecond finds the 1 MHz line high; U45C generates a low output, causing the SET line to go high.

This paragraph pertains only to TC-5 circuit cards 670-1438-01 and above. When the Position Counter passes through one hundred and reaches the first character position, Send Enable FF U51A becomes one-set. The next low input on the 1 MHz line causes a low pulse out of U53C. This is applied through U49B and U37B to Send FF U17B. If a $\overline{\text{SEND}}$ had previously caused U17A to one-set, U17B would become one-set, causing $\overline{\text{SP SEND}}$ and SEND signals to be sent out. In addition, the pin 9 output of U17B puts an enabling voltage on U33C and U59C. U59C permits SP XMT STR signals to be generated. When an $\overline{\text{AGREE}}$ signal occurs (indicating that the last character has been transmitted), U33C generates a low output and causes U15B to send a reset signal through U57F to the Send Initiate and the Send flip-flops, restoring them to their zero-set condition.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-00. When the Position Counter passes through one hundred and reaches the first character

position, Send Enable FF U51A becomes one-set. The next low input on the 1 MHz line causes a low pulse out of U53C. This is applied to Send Initiate gate U47D. If a $\overline{\text{SEND}}$ signal is present, U47D generates a high output pulse, the leading edge of which one-sets Send Initiate FF U17A, applying a high to the D input of U17B. The low pulse from U53C is also applied to U49B. When it ends, the U49B output goes low, causing a high to appear at the U37B output. This one-sets SEND FF U17B, causing $\overline{\text{SP SEND}}$ and SEND signals to be sent out. In addition, the pin 9 output of U17B puts an enabling voltage on U33C and U59C. U59C permits SP XMT STR signals to be generated. When an $\overline{\text{AGREE}}$ signal occurs (indicating that the last character has been transmitted), U33C generates a low output and causes U15B to send a reset signal through U57F to the Send Initiate and the Send flip-flops, restoring them to their zero-set condition.

If the Terminal is in the Edit Mode when the $\overline{\text{SEND}}$ command is executed, the $\overline{\text{EDIT FF}}$ signal disables U49B and enables Edit Send Execute device U37A. At the time that Edit was selected, the Cursor Counter loaded its contents into the Cursor Storage Register. When the Position Counter reached the first character position, it indirectly caused Send Initiate FF U17A to become one-set. This removed the low from the U37C pin 10 input, permitting that device to come under control of the SP STROB signal. Now each time the Position Counter increments one count, an SP STROB signal and a COUNT DWN signal are received by TC-5, causing the output of U45B to go low. This sends a high COUNT DWN signal into U21. When the Position Counter reaches the value that had been in Cursor Storage, the Cursor Storage contains the complement of 1. (Complement of 0 for TC-5 circuit cards numbered 670-1438-00.) All inputs to U9 are high. This causes the Edit Send Execute gate U9 to send a low to U41A, causing U37A and U37B to deliver a high pulse to U17B, one-setting that device and initiating transmission. Transmission continues until the Cursor Counter and the Position Counter values agree, at which time transmission is terminated and the Scratch Pad Send circuits become reset.

Horizontal Tab TC-6

The purpose of this circuit card is to permit insertion of tab positions, removal of tab positions, and the shifting of beam writing position to pre-determined tab positions. Circuitry consists of the following sections: Control Signal Decoder, Disarming Circuit, Tab Arm flip-flop, Set flip-flop, Clear flip-flop, Master Clear Control Circuit, Read/Write flip-flop, Reset flip-flop, Tab Pulse Control, Random Access Memory, and Master Clear Counters.

Assume that no tab positions have been established, and that it is desired to insert a tab at the position occupied by the beam. The eight most significant bits are routed through Master Clear Counters U55 and U57 and applied to the Random Access Memory U35. There they call up a specific memory location which is coincident with the content of these lines. Upon receipt of a coded character (normally ESC), the Terminal provides an $\overline{\text{SP ARM}}$ signal into the circuit. The trailing edge of this pulse one-sets flip-flop U9B, applying enabling voltages to Set flip-flop U9A, Clear flip-flop U29A and Master Clear Control flip-flop U29B. In order to set a tab, the next input data must provide a low output from U1 in the Control Signal Decoder. As configured on the schematic, the number 1 provides all highs into U1. When the TC IN STRB pulse arrives, it causes a low pulse out of U1 which passes through U27A, is inverted and causes Set flip-flop U9A to become one-set. This applies a low to U31A, causing that device to remove the clear signal from Read/Write flip-flop U11A, at the same time sending a $\overline{\text{TAB BSY}}$ signal out through U53B. The $\overline{\text{TAB BSY}}$ signal is routed back to U51D to reset U9B to its zero-set condition. With the clear voltage removed from Read/Write flip-flop U11A, the next 1 MHz clock pulse one-sets U11A; U11A then applies a high to U51C and a low to U53A. The high at pin 9 of U51C has no effect, since the second input to U51C remains low. U51C therefore maintains a high into pin 12 of U35, holding that input in its tab setting condition. Read/Write gate U53A has coincidence between the low signal from the 1 MHz line and the low from the 0 output of U11A, and therefore provides a high into the R/W input of U35. This high at the R/W input of U35 causes the high at pin 12 to set a tab. Simultaneously, the U35 Data Out signal goes low, indicating that a tab position is contained at the existing address. A tab position has been written and the Tab Arm flip-flop has been reset. The next 1 MHz clock pulse one-sets U11B, resetting Set and Clear flip-flops U9A and U29A.

Let's now consider how the beam can be ordered to the tab position which was just inserted. This is accomplished by receiving an $\overline{\text{HT}}$ signal, which comes in and is applied to U51B to generate a $\overline{\text{TAB}}$ signal which goes to TC-12, the X Data Register. In TC-12, this tab signal causes the register to increment by 12 points, which is the spacing between character positions. As the X Register increments, the bit information coming into U55 and U57 changes, continuously calling up new addresses in the U35 Random Access Memory. The $\overline{\text{HT}}$ signal is also applied through U49B, where its trailing edge causes flip-flop U13A to become one-set. When this one-sets, it provides a $\overline{\text{TAB BSY}}$ signal to inform the Terminal that the circuitry is busy providing tab functions. At the same time, U13A releases the clear signal from U33B, U33A, and U13B. This permits that circuit to start counting from 0 to 8 in response to the 1 MHz input signals.

The X Register is incremented through its 12 points at a 2 MHz rate. Therefore, after 6 microseconds, the X Register completes incrementing to its new position. By this time,

the divide by 8 counter is providing a low to U53C. If the Random Access Memory has not arrived at a tab position, the Data Out connection remains high and U53C continues to provide a low output to U53D. This permits U53D to continue applying a high to the Clear input of U13A. U13A remains one-set and permits the divide by 8 counter to continue counting.

When the divide by 8 counter reaches 8, it applies three highs to U31B. The next time the 1 MHz clock goes high, U31B applies a low to U51B which causes another $\overline{\text{TAB}}$ signal to be sent to the X Register. The X Register increments through another 12 points and again the Random Access Memory indicates whether or not a tab position exists. If none exists, the divide by 8 counter causes another $\overline{\text{TAB}}$ signal to be sent out. This continues until either a tab position is arrived at, or the end of the line is reached and an $\overline{\text{EOL}}$ signal arrives. $\overline{\text{EOL}}$ is processed through U7A and U53D to apply a low to U13A, zero-setting that device. This places a clear signal onto the three flip-flops in the divide by 8 circuit, causing them to become zero-set. They are thus prevented from generating any more $\overline{\text{TAB}}$ signals.

Assume that the circuit is generating $\overline{\text{TAB}}$ signals and the X Register comes to rest in the position that addresses a tab in U35. The U35 Data Out line goes low. This low is joined in U53C by a low from U13B. The high from U53C causes U53D to zero-set U13A. When U13A becomes zero-set, the divide by 8 counter is again locked in a cleared condition, preventing additional $\overline{\text{TAB}}$ signals. It should be noted that at the same time U13A becomes zero-set, the $\overline{\text{TAB BSY}}$ is ended.

Assume now that the X Register is resting in a position that calls up a tab indication from U35, and that it is desired to clear this tab position. It can be done as follows: First, the $\overline{\text{SP ARM}}$ signal must be received to one-set Tab Arm flip-flop U9B. This provides enabling voltages to the Set flip-flop, Clear flip-flop, and the Master Clear flip-flop. The next character input must cause gate U3 to provide a low output. In the configuration shown on the schematic, the number 0 will perform this function. Assuming that a 0 has been received, the low output from U3 causes a high pulse to appear on the Clear flip-flop. The trailing edge of this causes the Clear flip-flop to become one-set, with the zero output causing a $\overline{\text{TAB BSY}}$ signal to be generated. At the same time, U51A applies a high to the Clear Set gate U51C.

Note that in addition to causing $\overline{\text{TAB BSY}}$ signal to be generated, U31A releases U11A from its cleared condition. The next 1 MHz pulse causes U11A to become one-set, applying a high to U51C, and a low to U53A. U51C now has two high inputs, and applies a low to the Data In connection of U35. The next time the 1 MHz clock goes low, two lows are in effect at the input of U53A, causing it to apply a high signal to the R/W input of U35. This high signal writes the low at pin 12 into the RAM, removing the tab indication from that address and the Data Out at pin 14 goes low. It should be noted that the low $\overline{\text{TAB BSY}}$ signal again was fed back to clear U9B, causing it to become zero-set; thus the Set flip-flop, Clear flip-flop and the Master Clear Control flip-flops become disarmed.

Assume now that a number of tabs exist in the Random/Access Memory, and that all these tabs are to be cleared. Again, we must first receive an $\overline{\text{SP ARM}}$ signal which causes Tab Arm flip-flop U9B to become one-set, applying an enabling voltage to Master Clear Control flip-flop U29B. If the next character is an M, it causes the U5 output to pulse low, causing U29B to become one-set. The low transition into U37 causes it to generate a pulse of approximately 1.5 milliseconds duration. The zero output from U37 goes to U51A to place a high on U51C. The zero output from U37 also is processed by U31A to release the clear signal from R/W flip-flop U11A and to generate the $\overline{\text{TAB BSY}}$ signal. As before, the $\overline{\text{TAB BSY}}$ signal goes back to reset the TAB ARM flip-flop to its cleared condition.

The next 1 MHz CLOCK signal to arrive causes R/W flip-flop U11A to become one-set. This cause a high into U51C and a low into U53A. U51C now has two high inputs, causing a low output to be applied to the Data In terminal of U35. While the zero output from U37 is controlling U51A and U31A, the one output from U37 is applying a positive pulse to the Cnt/Load inputs of U55 and U57. This high signal permits U55 and U57 to be disconnected from the X Registered input lines and allows U55 and U57 to advance through one count for each input of the 1 MHz clock signal. The positive excursion of the 1 MHz clock advances the U55 and U57 count by one position. The negative level of the 1 MHz clock is then applied to R/W Gate U53A. The high pulse from U53A writes the low Data In signal into the Random Access Memory. A low is written into each address as the 1 MHz clock carries the U55 and U57 circuits through their entire range.

The U37 output pulse ends at the end of 1.5 ms. Notice that during pulse time, the 0 output from U37 was being fed back to U29B, locking U29B in a cleared condition. When the pulse ends, U29B remains in that condition until it again becomes enabled by the Tab Arm flip-flop and receives another input signal from U5. It should be noted that throughout the clearing of the tabs, the X Register was permitted to remain stationary. The U55, U57 outputs were clocked serially through their entire range by the combination of the high into pin 9 and the repetitive application of 1 MHz pulses.

One more point should be considered—receipt of a character other than those recognizable by U1, U3, or U5

while the SP ARM flip-flop is armed. In such a case, U1, U3, and U5 apply highs to U7B, causing U7B's output to remain low. This causes U49A to apply a high to U7C. When the $\overline{\text{SP ARM}}$ signal elapses, it applies a high to a second input of U7C. When the TC IN STRB signal arrives, this third high causes a low output of U7C, which results in U9B disarming.

Control Function Decoder TC-7

TC-7 is the control character and special function decoder for the Terminal. It consists principally of two Character Decoders, a Control Function Completes Delay circuit, and the special function output circuitry.

The inputs to the decoders consist of data lines DR1 through DR5. DR5 selects the decoder, and DR1 through DR4 determine its outputs. The CF EXEC signal is applied through an inverter to the decoders as an enabling voltage. Inputs 18 and 19 must both be low in order for the device to decode the DR1 through DR4 information. Therefore, when DR5 is low, U7 is enabled by the CF EXEC signal. When DR5 is high, U11 is enabled by the CF EXEC signal. Thus, if DR1 through DR5 were all high, U11 would be selected; when CF EXEC occurred, a low would appear on output pin 17, resulting in a high US control character signal out of the card.

The special function signals are generated whenever appropriate control characters are decoded by U7 or U11. These are then processed by the applicable circuitry and made available as outputs. It should be noted that although standard factory-wired connections are shown to indicate which signals control the special functions, these resistive straps can be moved to connect any of the control characters to any one of the special function control lines.

CF Comp Delay Circuit. The purpose of this circuit is to provide a 64 μs time delay between receipt of the CF EXEC signal and the CF COMP output signal. This 64 μs permits adequate time for any special function or control character to be executed by the Terminal. The details regarding this special function complete delay circuit can be determined from the timing diagram associated with the TC-7 schematic.

Character Rotator TC-8

TC-8 is the character rotator card, and is optional in the Terminal. When the card is not in use, a bypass card must be in its place. With the bypass card in use, the A, B, C, and D signals appear at the output as KR5, KR6, KR7, and KR8, respectively, and the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ signals appear at the output as KR2, KR3, and KR4, respectively. The KR1 output is held low and the $\overline{\text{KR SHIFT}}$ output is held high.

Assume that the Character Rotator card is in use and that U15A and U15B are in their zero-set condition. (This condition could occur as a result of a $\overline{\text{HOME}}$ signal, an $\overline{\text{INITIAL}}$ signal, or a US signal; it could also occur by having a successive number of NAK signals sufficient to leave the two flip-flops in their zero-set condition.) With the flip-flops zero-set, U13B receives two high signals and U13A, U13D, and U13C receive at least one low signal. Under this condition U35C has all high signals applied, causing a high output on the $\overline{\text{KR SHIFT}}$ line. U11D has a low input, causing it to place highs on 2 section input gates U3A, U5, U25, U7, U27, U9, and U31. Notice that the second input to these sections is provided by the A, B, C, D, $\overline{\text{E}}$, $\overline{\text{F}}$, $\overline{\text{G}}$, inputs as follows: U3A is driven by A, U5 is driven by $\overline{\text{E}}$, U25 is driven by B, U7 is driven by $\overline{\text{F}}$, U27 is driven by C, U9 is driven by $\overline{\text{G}}$, and U31 is driven by D. When row 1 is selected by the Character Generator matrix in TC-16, A, B, C, and D are low. By following these signals to the respective 0° gates, it can be seen that they control the KR5, KR6, KR7, and KR8 outputs–which would also be low at this time. When column 1 is selected, $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ are high. Following them through their 0° gates will result in KR2, KR3, and KR4 being high.

Now assume that an NAK has been received. U15A becomes one-set, causing U13C to receive two highs while the other three NAND gates each receive at least one low. The output of U13C goes low, causing a low $\overline{\text{KR SHIFT}}$ signal to be developed. At the same time, highs are received by one input of the 90° AND gates. The second input to these 90° gates is controlled by their respective A, B, C, D, $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ inputs. Now an interchange of functions has been accomplished. Note that KR1 is now put into use to control the X-axis, because the interchange has caused the 10 rows to be applied to the X Registers instead of the usual 8 columns. It should also be noticed that during 90° operation, the KR5 output is disabled, and is held in a low condition. This occurs because the KR6, KR7, and KR8 lines now are handling the column selection and three lines are sufficient. With 90° character rotation selected, the A, B, C, and D input lines control the KR1, KR2, KR3, and KR4 output lines respectively, while the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines control the KR6, KR7, and KR8 lines, respectively.

Receipt of another NAK signal causes 180° character rotation to be selected. At this time, U15A becomes zero-set and U15B becomes one-set. This condition results in U13D providing a low output to cause the $\overline{\text{KR SHIFT}}$ signal. U13D and U11A provide highs to appropriate AND gates. KR1 is now disabled and is held low, while KR5 is put back into use. Operation is similar to 0° condition except that the A, B, C, and D lines control KR8, KR7, KR6, and KR5, respectively. This causes the inverse of that which existed at 0° character rotation. Under these same circumstances, the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines control the KR4, KR3, and KR2 lines, respectively.

One more NAK signal causes U13A to receive two highs, with its low output causing a low $\overline{\text{KR SHIFT}}$ signal and

causing highs to be applied to appropriate AND gates. The operation now is similar to that described for 90° operation except that A, B, C, and D now control KR4, KR3, KR2, and KR1, respectively, while $\overline{E}$, $\overline{F}$, and $\overline{G}$ control KR8, KR7, and KR6, respectively.

Y D/A TC-9

The TC-9 circuit description is essentially the same as that for TC-13. Only the differences will be discussed here.

TC-9 does not contain an Italics circuit. Another difference is that TC-9 does contain a Compose circuit. When the Terminal is not in Compose Mode, the input to pin 6 of U87C is high; Q57 and Q77 are turned on. If S99 is set at BTM, CR84 is back-biased and prevents Q77 from affecting U55.

When Compose is selected, the input to pin 6 of U87C goes low, turning Q77 off and placing a high on the anode of CR84. This high passes through S99 to the negative input of U55, causing the output of U55 to hold the CRT beam in the Scratch Pad strip at the bottom of the display area. The D/A circuits now have no effect upon the vertical position of the beam. However, the beam can still be influenced by the character generator matrix signal coming in through the KR5 through KR8 lines at the bottom of the schematic.

If the tube had been rotated so that the Scratch Pad strip were at the top of the CRT, S99 would be in the Top position. Compose Mode would cause Q57 to turn off, placing a low signal through CR88 to the U55 circuit. This low into the negative input of U55 would result in a positive output, holding the display at the top of the CRT in the Scratch Pad area.

Y Data Register TC-10

The Y register contains the following circuits:

5 Least Significant Bit (LSB) control
5 Most Significant Bit (MSB) control
16 Y Parallel control
512 Y Parallel control
Step control
Line Feed Enable
Line Feed ÷19
Double Size Character Line Feed control
Reset Circuit
Cursor Up
Page Full

These circuits will be discussed in that order.

5 LSB Control. The 5 LSB control circuit can be driven either parallel or serial. Under initial or reset conditions it is driven in parallel manner. Parallel input gates U41D, U41C, and U45D are inhibited by the high signal from U57B. The resulting lows from these gates are applied to U41A, U41B, and U45A. When a horizontally oriented display tube is installed, a low is applied to the second inputs of each of these three OR gates, causing their outputs to be high, applying lows to U21 inputs A, B, and D. U21 pin C is receiving a high from U24C because of the effect of U57B on U45B. The high pulse from U57B also passes through U9B to apply a low to the load input of U21, causing the low-low-high-low at A, B, C, and D respectively, to be felt at outputs 3, 2, 6, and 7. These are inverted to cause $\overline{1Y}$, $\overline{2Y}$, and $\overline{8Y}$ to be high, and $\overline{4Y}$ to be low.

The $\overline{16Y}$ line is controlled by U7A. During resetting, the high signal from U57B is coupled through U9B to U3E, where it causes a high output to be applied to U23D. At this time, U24A is also applying a high to U23D, causing a low from U23D to zero-set U7A. This causes the 1 output to be low, causing the 16Y line to be high.

The condition of the just-described five lines is determined by whether a vertical or horizontal format is in use. The description given was for a horizontally oriented CRT. When a vertically oriented CRT is in use, the inputs to U41A, U41B, and U45A are high during the time that the pulse from U57B is high; this results in highs into U21 A, B, and D, causing the $\overline{1Y}$, $\overline{2Y}$, and $\overline{8Y}$ lines to be low. In addition, the high from U57B is inverted by U29E, applying a low through the strap link to U27A, putting a low on U23D, disabling it. Simultaneously, the low is applied to the preset connection of U7A, causing U7A to one-set. With U7A one-set, the one output is high, putting a low on the $\overline{16Y}$ line. It may be noted that U5B serves no function during this resetting action.

5 MSB Control. This circuit can be analyzed in a manner comparable to that used for the 5 LSB control circuit. It should be noted that during horizontal format reset conditions, the low which was applied to U21 is also applied to U25 pin D. This causes the $\overline{256Y}$ line to be high. When vertical format is selected, $\overline{32Y}$, $\overline{64Y}$, $\overline{128Y}$, $\overline{256Y}$, and 512Y lines are all held low during reset. During reset, U1D, U1C and U5C have no effect on the 5 MSB control circuit.

The two circuits described in the preceding paragraphs are normally reset under one of several conditions; one of these is upon receipt of the $\overline{HOME}$ signal; another is when $\overline{ALFA\ ORG}$ is received by way of U9A and U37B into U57B. A third situation causing reset to occur is when Page Full happens. At that time the $\overline{PF\ PULSE}$ from U35D is coupled back through U57B to cause reset to occur.

While in Graphic Mode, a high on the GRAF 2 line disables the $\overline{ALFA\ ORG}$ input and also disables the Page Full circuit. During this time data can be parallel-loaded

into U21, U7A and their counterparts in the 5 MSB control circuit. The routes for DR1, DR2, DR3, and DR4 can be determined quite easily–they pass through gates and are applied to the inputs of the up-down counters. They are latched into only one counter at a time, the counter being determined by whether a high pulse is applied to the LO Y EN (low Y enable) line or the HI Y EN line. If applied to the LO Y EN line, it causes a low out of U9B, applying a low to the load input of U21. If the high is applied to the HI Y EN input line, it passes through U9D to apply a low to the load input of the 5 MSB counter.

The $\overline{16Y}$ and $\overline{512Y}$ lines are controlled in graphics by the combination of the enable pulse and DR5. If a LO Y EN pulse and a DR5 exist, U23C applies a low to U27A, placing a low at the preset input of U7A, causing U7A to one-set. This applies a low to the $\overline{16Y}$ line. If DR5 and HI Y EN signals exist at the same time, the ANDing is performed by U27B putting a low into U27D, applying a low to the preset input of U7B. This one-sets U7B, applying a low to the $\overline{512Y}$ line.

16Y Parallel Control and 512Y Parallel Control. Although these two are indicated as separate circuits on the schematic, their function was explained with the 5 LSB control and 5 MSB control circuits.

Step Control Circuit. The Step control circuit provides the drive pulse to increment or decrement the 5 LSB control circuit. The direction is determined by U51C, which responds to an $\overline{AUX\ +Y}$ signal from auxiliary units, a $\overline{+Y}$ signal from the Plot control circuit, and a Cursor Up signal from Cursor Up flip-flop U33B. Normally, these three lines are high, providing a low from U51C, disabling U57C and providing an enabling voltage to U5A. Under the described condition, a low pulse at any one of the three inputs to U51B will cause a low pulse out of U5A; this low pulse is accepted by U21, causing it to decrement one count at a time. When U21 decrements through 0, a low pulse appears on the pin 13 Borrow line. If U7A is one-set, it is an indication that a $\overline{16Y}$ exists and the Borrow is taken from this device. With U7A one-set, its 1 output disables U1D, preventing the Borrow pulse from passing through. The Borrow pulse goes through U5B to clock U7A into a zero-set condition, putting a high on the $\overline{16Y}$ line. The next time U21 clocks through 0 position, another Borrow pulse occurs at pin 13. This time it finds U7A zero-set and U1D is enabled. The Borrow pulse ANDs with the low from U7A in U1D to provide a high out of U1D and a low into the count-down input of the 5 MSB control counter, causing it to decrement by one point or one count. The Borrow pulse from U21 again causes U7A to toggle, this time one-setting it. Subsequent Borrow pulses will repeat the described action.

If U51C in the Step Control circuit is receiving a low from any one of its inputs, it will enable U57C and disable U5A. Now, pulses into U51B will cause U57C to generate low output pulses, and U21 will count up. Subsequent action is very similar to that described for counting down, except that a Carry pulse will be provided by U21 and will be acted on by U5B and U1C in a manner very similar to that described for Borrow.

Line Feed Enable Circuit. The Line Feed Enable circuit permits 2 MHz clock pulses to pass through U31A into the Step Control circuit to cause the counter circuit to increment or decrement according to the existing signals. U31A is normally disabled and becomes enabled in response to one of several signals into U59. One of these is a $\overline{LINE\ FEED}$ through U9C and U37C into U59. Another one is an $\overline{EOL}$ signal through the AUTO LF strap into U59. A third is a $\overline{Y\ CUR\ PULS}$ into U59. And a fourth is a $\overline{DBL\ SZ\ CHR}$ command through U37D, U35B, and U39 into U59. Regardless of which signal arrives at U59, it generates a high output into U57A. As long as Page Full condition does not exist, the 2 MHz signal through U37F clocks a pulse out of U57A which one-sets LF Clock Enable flip-flop U33A. U33A applies a high to U31A, enabling that gate. 2 MHz pulses are then permitted to pass through U31A to clock the counter circuit. The number of 2 MHz clock pulses permitted to pass through U31A is limited to either 19 or 38. Limiting to 19 is done by the Line Feed ÷ 19 circuit U11, U13A, U15, U17, U19B, U37A and the U13B flip-flop. When 19 pulses have passed through this countdown circuit, U33A zero-sets, putting a disabling voltage onto U31A.

Line Feed ÷ 19 Circuit. This circuit consists essentially of a divide-by-19 counter which is best explained through a timing diagram, which is provided opposite from the schematic.

Double Size Character Line Feed Control. If a $\overline{DBL\ SZ\ CHR}$ signal is in effect, U35B has an enabling voltage applied. When a $\overline{LINE\ FEED}$ pulse, or an $\overline{EOL}$ pulse is processed through U35A, it causes the U35B output to go low, thus one-setting U39. The low from the 0 output of U39 holds the U59 output high, resulting in a low from U57A. This holds U33A in a one-set condition. Therefore, when the first pulse from U13B reaches U33A, it is overridden by the low on the preset input. However, the pulse from U13B is routed back to U39, causing it to zero-set. Now the 0 output of U39 is high. This permits the U59 output to go low, providing a high output from U57A. The next U13B pulse to reach U33A resets it to a zero-set condition and disables U31A. In this manner, the counter is caused to step 38 counts in response to a $\overline{LINE\ FEED}$ command instead of stopping after the usual 19.

Reset Circuit. The reset circuit was basically discussed in conjunction with the 5 LSB control and the 5 MSB control circuits at the beginning of this discussion and will not be discussed further.

Cursor Up flip-flop Circuit. Cursor Up flip-flop U33B is one-set upon initialization, and remains in this condition until such a time as a $\overline{\text{CUR UP}}$ signal is commanded by the switch on the keyboard. At this time, U33B becomes zero-set, causing count-up pulses to be delivered by the Step Control circuit. Since the $\overline{\text{CUR UP}}$ is accompanied by a $\overline{\text{Y CUR PULS}}$, the U31A NAND gate and the Line Feed Enable circuit becomes enabled at the same time U33B becomes zero-set. Upon completion of the divide-by-19 countdown, U33A becomes zero-set, and its 0 output applies a high to U33B. The next 2 MHz clock pulse one-sets U33B, removing the low from the Step Control circuit.

One more comment. A $\overline{\text{PRNT BSY}}$ signal can be applied to the Page Full circuit to create a pseudo $\overline{\text{PAGE FULL}}$ signal to prevent Terminal operation until hard copy printing has been accomplished.

Page Full. TC-10 circuit cards 670-1443-01 and above. The page Full circuit will be described next. If not in Scratch Pad mode, Page Full is indicated when $\overline{512Y}$ and $\overline{256Y}$ are high and another Borrow pulse is applied to the input of U7B. This Borrow-during-zero condition indicates that the counters have decremented to zero and that the beam is at the bottom of the CRT, the Page Full position. In Alpha Mode, the other three inputs to U49 are high, causing it to generate a low output pulse, placing a low on U27C. This places a low on the K input of U55B. A simultaneous high from U27C goes to U55B. The next 2 MHZ pulse causes U55B to one-set, generating a PF LITE out of U55B. The low from the zero output of U55B passes through U35C and U53D to generate $\overline{\text{PAGE FULL}}$. The PF LITE signal is applied to U55A, permitting the next 2 MHZ pulse to one-set it. When the 2 MHZ pulse ends, U55A zero-sets and disables U35D. The $\overline{\text{PF PULSE}}$ goes to the interface unit and may be returned to TC-10 as a $\overline{\text{PF RESET}}$ signal. This goes into U31C and is applied to U51A to reset the flip-flop circuit. The $\overline{\text{PF PULSE}}$ from U35D is also looped back to U57B to generate a high output signal which resets the 5 LSB and 5 MSB circuits.

It should be noted that U7B disables PF Gate U49 immediately after the just-described action. This occurs when the trailing edge of the pulse from U5C one-sets U7B.

Removing the U49 low from U27C permits the $\overline{\text{PF RESET}}$ pulse to reset the U27C-U51A flip-flop. With U27C and U51A reset, U55B zero-sets in response to the next 2 MHZ pulse. The $\overline{\text{PAGE FULL}}$ line goes high and PF LITE goes low. The input to U55A goes low, disabling U55A in the zero-set state.

During Scratch Pad modes, $\overline{\text{SP STRIP}}$ inhibits U24D. It also holds U55B zero-set, preventing page full signals from being generated.

Page Full. TC-10 circuit cards 670-1443-00 only. The Page Full circuit will be described next. Page Full is indicated when $\overline{512Y}$ and $\overline{256Y}$ are high and another Borrow pulse is applied to the input of U7B. This Borrow during 0 condition indicates that the counters have decremented to 0 and that the beam is at the bottom of the CRT, the Page Full position. In Alpha Mode the other three inputs to U49 are high, causing it to generate a low output pulse, placing a low on U27C. This generates a low $\overline{\text{PAGE FULL}}$ pulse. A simultaneous high from U27C goes to U55B and U55A. The next 2 MHz pulse to occur causes U55B and U55A to one-set, generating a PF LITE out of U55B and a high out of U55A into U35D. When the 2 MHz pulse again goes high, U35D generates a low $\overline{\text{PF PULSE}}$. When the 2 MHz pulse ends, U55A 0-sets and disables U35D. The $\overline{\text{PF PULSE}}$ goes to the interface unit and may be returned to TC-10 as a $\overline{\text{PF RESET}}$ signal. This goes into U31C and is applied to U51A to reset the flip-flop circuit. The $\overline{\text{PF PULSE}}$ from U35D is also looped back to U57B to generate a high output signal which resets the 5 LSB and 5 MSB circuits.

It should be noted that U7B disables PF Gate U49 immediately after the just-described action. This occurs when the trailing edge of the pulse from U5C one-sets U7B.

Removing the U49 low from U27C permits the $\overline{\text{PF RESET}}$ pulse to reset the U27C-U51A flip-flop. With U27C and U51A reset, the $\overline{\text{PAGE FULL}}$ line goes high and the input to U55A goes low, disabling U55A in the zero-set state. Although the output of U27C returns low, the PF LITE flip-flop U55B remains one-set until such time as a $\overline{\text{FULL}}$ pulse is received, permitting the 2 MHz clock to zero-set U55B.

In/Out Data Routing TC-11

TC-11 is the input/output data routing board for the Terminal, and it contains the following principal circuits:

- Output Latches
- Input Latches
- Local Control
- Output Latch Clear
- Graphic Word Assembler

The output latches accept B1 through B8 data from the keyboard, scratch pad, or auxiliary inputs. Upon receipt of a DATA STRB, the data is latched through, making it available on the interface output lines TB1 through TB8. If $\overline{\text{LOCAL ECHO}}$ exists or if ON LINE is low, U27C sends a high to U3B and the Local Control gates U23C through U37C. When a DATA STRB occurs, U3B sends a DROP FLG signal to the interface to prevent data from going to the computer. At the same time, the high on gates U23C through U37C AND with data from the output latches to make the data bits available on the DR1 through DR8 lines. The output latches are cleared upon completion of character processing. For example, if On Line condition exists and data is being transmitted through the interface to the computer, it is followed by an $\overline{\text{LE COMP}}$. This is applied to U5C in the Output Latch Clear circuit, is processed through U27D, U27B, and U45A to clear both Output Latches. If LOCAL Mode exists, ON LINE is low and completion signals are routed through U3A to do the clearing.

Input Latch Circuit. When data is received from the computer and interface, it appears on the RB1 through RB8 lines and is accompanied by RCV STROB. The strobe latches the data bits into U47 and U51, making them available at the output of the latches. From there these bits are routed through inverters and OR gates and are made available to the Terminal circuits on the DR1 through DR8 lines.

Graphic Word Assembler. The purpose of this circuit is to accept bytes of input information during Graphics Mode and route these bytes to the appropriate data registers in five-bit bytes. The sequence in which these bytes is routed is determined by straps R7, R13, and R5. Standard factory connection for these straps requires that bytes be supplied to the Terminal in the following sequence: high Y, low Y, high X, and low X. This discussion will assume that these straps are as shown on the schematics and the given sequence is being presented.

When Linear Interpolate or Point Plot Mode is selected, $\overline{\text{GS+FS}}$ goes low, causing the Graf FF to change states. U3C provides a low to U29C. The accompanying high from U27A serves several purposes—it provides enabling voltage to Byte Decoder U7, and enabling voltage to NAND gate U13A. It also removes the low which had been holding Hi byte flip-flop U11 zero-set. When graphic bytes are clocked into the TC-11 circuitry, the bit 7 and bit 6 configuration is determined by the byte being received. For example, high X byte has bit 7 low and bit 6 high; the low X byte has them high, low; the high Y byte has them low, high; and the low Y byte has them high, high. Upon receipt, these bits are applied to byte decoder U7 along with SYNC STRB, which is applied through U5F. The leading edge of the SYNC STRB clocks bit 7 and 6 through U7, placing a low on either the 4, 6, 5, or 7 output lines. If the high X byte is being received, it causes U7 pin 6 to go low, placing enabling voltages on U29B and A. The high on Pin 4 of U7 holds the LOW Y EN line low and maintains a disabling voltage on the J input of HI BYTE FF U11. Pin 5 of U7 is also high, putting a low disabling voltage on the K input of U11, and on the LO X EN line, In addition, it places a low on U13A, disabling that gate. The high from pin 7 of U7 places a low on U29C to AND with the low from the $\overline{\text{GRAF}}$ flip-flop. The high output from U29C causes a low $\overline{\text{GWA}}$ output command, indicating that the Graphic Word Assembler is being employed.

Go back to Hi Byte flip-flop U11. Prior to the time that the GRAF flip-flop had been put into Graphics Mode, a low from U27A had held U11 zero-set. The low from U11 pin 8 held a low on U29B. When the high Y byte is decoded by U7, the low from pin 6 ANDs with the low from U11 pin 8, causing a HI Y EN pulse from U29B. The HI Y EN also goes through U33D to cause a high out of U13C, placing an enabling voltage on U15A. U15A is negative-edge conscious and when the SYNC STRB input ends, it causes the high at the J input of U15A to clock through and apply a high to the J input of U15B. The next 1 MHz clock pulse finds its negative transition one-setting U15B, causing the $\overline{\text{GWA COMP}}$ signal to go low. This $\overline{\text{GWA COMP}}$ signal is fed back through U13D and U13B to zero-set U15A, causing the U15B J input to go low. The next 1 MHz clock pulse has its negative edge zero-setting U15B, causing $\overline{\text{GWA COMP}}$ to end. This signal is an indication to the Interface Unit that the Graphic Word Assembler has loaded the byte into the appropriate register.

The next byte to arrive is a low Y byte and it contains a high bit 7 and a high bit 6. With pins 3 and 13 of byte decoder U7 high, its pin 4 output goes low when the SYNC STRB pulse arrives. This places a high on the LO Y EN line, at the same time holding lows on the HI Y EN, HI X EN, and LO X EN lines. The high on the LO Y EN line is applied to the J input of U11 and is also applied through U33A and U13C to the J input of U15A. When the SYNC STRB ends, U11 and U15A both become one-set. U11's change of state is a preparatory step towards having the next high byte enabling the HI X EN line. When U15A changed state, it caused a high to be applied to U15B, so that the $\overline{\text{GWA COMP}}$ pulse can be generated by the next 1 MHz pulse just as it did when the high Y byte was loaded.

When the $\overline{\text{GWA COMP}}$ pulse ends and the interface supplies the TC-11 with the high X byte, it is accompanied by a low bit 7 and a high bit 6. This causes a low on pin 6 of U7, providing enabling voltage to U29B and U29A. Since U11 is one-set, U29A now has two lows and generates a HI X EN output pulse. Incidentally, this pulse is of the same width as the Sync Strobe that caused it. This HI X EN pulse passes through U33A, U13C and is applied to the J input of U15A. The end of the SYNC STRB clocks U15A and causes U15B to generate another $\overline{\text{GWA COMP}}$ pulse as before. When the fourth byte (low X) is applied to the

TC-11 circuitry, it has a high bit 7 and a low bit 6. This causes a low on pin 5 of U7 when SYNC STRB occurs. This puts a high on the K input of U11, a high on the LO X EN line, and a high into U13A. The high into U13A ANDs with the high from U27A and causes a low into U31 to generate a low $\overline{\text{STROB DLY}}$ output pulse, which permits the point to be written. When SYNC STRB ends, LO X EN also ends, zero-setting U11. This permits receipt of the high Y byte of the next point to be written. Note that the fourth byte does not enable the GWA Comp flip-flops and no $\overline{\text{GWA COMP}}$ signal is generated. On TC-11 circuit cards 670-1444-01 and above, the end of the fourth pulse (at U13A pin 2) is felt through a network which causes U29D to clear the data latches.

One other item. It should be noted that throughout the loading of these four bytes, pin 7 of U7, the byte decoder, remained high to maintain a low into U29C. Since $\overline{\text{GS+FS}}$ remains low while in Linear Interpolate or Point Plot, U3C also provided a low into U29C. The high output from U29C was inverted by U53F and mainteined a $\overline{\text{GWA}}$ signal to indicate that the Graphic Word Assembler is in its active state. If a control character is received, the bits strobed through U7 cause pin 7 to go low, putting a high on U29C. This causes $\overline{\text{GWA}}$ to go high, permitting the control character to be processed.

X Data Register TC-12

TC-12 is the X Data Register for the Terminal. Its purpose is to control the Terminal's horizontal address. The principal parts of TC-12 are the 5 LSB Control circuit, the 5 MSB Control circuit, the Reset circuit, Bell circuit, Line Start Detector, Line End Detector, EOL Control, Margin Control, and Space Control circuit. These circuits will be discussed in that order.

5 LSB Control. This circuit controls and stores the five least significant bits of the 10-bit X register. Bits $\overline{\text{1X}}$, $\overline{\text{2X}}$, $\overline{\text{4X}}$ and $\overline{\text{8X}}$ are controlled by Up-Down Counter U21; bit $\overline{\text{16X}}$ is controlled by flip-flop U9B. These devices can be controlled in either serial or parallel fashion. In addition, they can be cleared to zero upon command. Clearing the registers is accomplished by placing a high signal on the pin 14 Clear input of U21 and simultaneously applying a low to pin 8 (Clear input) of U9B. This clearing signal is received from U55 in the Reset circuit.

Serial control of the circuit is accomplished by applying a pulse to either the Up or Down input of the Counter circuit. Under normal left to right operation, count up gate U49C is enabled and pulses are applied to the Up input of the counter. These pulses can be the result of $\overline{\text{AUX PLOT X}}$ or $\overline{\text{STEP X}}$ input signals, or of the clock signal from U15C in the Space circuit. Each time a pulse is received, the Up-Down Counter increments its digital output by 1. For example, pin 3 represents bit 1 and pin 2 represents bit 2. When the counter is cleared, both of these outputs are low. After the first pulse arrives, pin 3 goes high. The second pulse causes pin 3 to go low and pin 2 to go high. After 15 pulses have been received, pins 3, 2, 6, and 7 are all high. The next pulse causes them to go low and causes a low pulse to appear on pin 12, the Carry line. This low causes U3C to apply a high pulse to U9B, the 16X flip-flop. This flip-flop had initially been zero-set by the action of the U55 Clear pulse through U1B, U3B, and U3D. When this Carry pulse ends, U9B becomes one-set and applies a low on the $\overline{\text{16X}}$ line.

It should be noted that the 5 MSB Control circuit operates essentially the same as the 5 LSB Control circuit, differing only in its manner of receipt of input pulses. Notice that the zero output of U9B is applied through U11B and U1E to the Up pulse input of U23. Initially, U9B was in its one-set condition and its zero output held U11B disabled. Therefore, when the first Carry pulse from the U21 Up-Down Counter arrives at U11B, it is prevented from affecting the output of that device. However, after U9B has received its first Carry pulse, it becomes one-set. A low is applied from the U9B zero output to U11B, providing that device with an enabling voltage. The next time a carry pulse is received from U21, it causes U11B to develop a high output, which applies a low pulse to pin 5 of the Up-Down Counter. This causes that device to increment by one count. The trailing edge of the pulse which causes this incrementing, causes 16X flip-flop U9B to again become zero-set, removing the enabling voltage from U11B.

Decrementing or down-counting is accomplished in much the same manner. Whenever U51C in the 5 LSB Control circuit is receiving a low input, it provides a high to U33C and U49B. U33C disables U49C, preventing the count up input from receiving any further signals. The stepping commands from U51B are then applied to pin 4 of U49B, causing a low output to be applied to the count down input of Up-Down Counter U21.

Assume that the pin 3, 2, 6, and 7 outputs of the Up-down Counter all contain lows at the time that a count down pulse is received. The 3, 2, 6, and 7 outputs of the Up-Down Counter go high and a low pulse appears on pin 13, the Borrow output. Assume also that the 16X flip-flop U9B has been zero-set prior to the arrival of that count down pulse. Pin 11 of U9B is low, providing U11A with an enabling voltage. When the low borrow pulse arrives at U11A, it causes a high output from U11A, applying a low to the count down input of Up-Down Counter U23. This counter then decrements by 1. The Borrow pulse that causes the U23 Up-Down Counter to decrement is also applied to 16X flip-flop U9B, causing it to become one-set. This applies a disabling voltage to U11A. The next Borrow pulse to be sent from U21 is prevented from passing through U11A but causes U9B to again change states. Essentially, U21 is then borrowing 1 from U9B, the 16X flip-flop.

Parallel control of the register is accomplished simply by applying data bit information on the DR1 through DR5

lines, making it available to both the 5 LSB and the 5 MSB Control circuits. The data is not accepted by the registers until such time as an enabling pulse is applied to the devices. When the 5 LSB Control circuit is to be controlled in parallel fashion, the data bit information is accompanied by a LO X EN input pulse. This is applied through U1C to pin 11, the load input of U21. Whenever this input goes low, the bit information at inputs A, B, C, and D is made available at output pins 3, 2, 6, and 7, supplying the four least significant X bits. The fifth input bit is applied to U3A. If it is high, the LO X EN pulse causes U3A to develop a low output to one-set U9B. At the same time, the low output from U3A disables U3D. However, if the bit 5 input is low, it disables U3A. The LO X EN pulse is then routed through U1C to apply a low to U3B, putting a high on U3D. U3D develops a low output, zero-setting 16X flip-flop U9B. The 5 MSB circuit is parallel loaded in the same fashion, except that a signal must be present on the HI X EN line to cause loading.

Reset Circuit. The Reset circuit causes the register to be set to left or center margin position, depending upon the selection made by the margin control circuit. This resetting is done is response to such signals as $\overline{\text{HOME}}$, $\overline{\text{PF PULSE}}$, $\overline{\text{SP RSET X}}$, $\overline{\text{CAR RTN}}$, $\overline{\text{ALFA ORG}}$, $\overline{\text{IO MGN SHF}}$, and $\overline{\text{MGN SHFT}}$. In addition, strap option AUTO CR permits resetting to occur each time that an END of Line condition is reached. The 5 LSB register and four bits of the 5 MSB register are reset to zero, regardless of the condition of the Margin Control. However, 512X bit flip-flop U9A is set to either of two states upon Reset, depending upon whether U15A or U15B is enabled. If the Left Margin has been selected, Margin Control flip-flop U19B is zero-set, putting an enabling voltage on U15B. When a high pulse is emitted by U55, U15B sends a low pulse to U5B, causing the 512X flip-flop to become one-set. This stores a register address of zero, the left edge of the screen.

If the Margin Control flip-flop had been one-set due to a $\overline{\text{MGN SHFT}}$ command, U15A would be enabled and U15B would be disabled. Reset pulses from U55 would then pass through U15A, applying a low to U7A; this would place a low on the Preset input of 512X flip-flop U9A, causing its zero output to go low, commanding the register to the 512X position. This places the CRT beam at mid-screen.

Bell Circuit. The Bell circuit generates a $\overline{\text{BEL X}}$ signal which causes the Terminal's bell to ring as the register approaches the end of the horizontal line. If the selector straps are set for a horizontal display format, this $\overline{\text{BEL X}}$ signal is generated when the register is in the 78th character writing position and an RKB STROB pulse is received. If the straps are in the vertical position, the $\overline{\text{BEL X}}$ command is generated when the register is in the 67th character position and an $\overline{\text{RKB STROB}}$ signal is received.

Line Start Detector. This circuit consists of NAND gate U29, whose output is used to prevent application of countdown pulses to Up-Down Counter U21 whenever the register is in the first character position while in Alphanumeric Mode. At this time all highs are applied to U29, causing it to send a low to U49B, preventing countdown pulses from passing through that device to U21.

Line End Detect Circuit. This circuit consists of NAND gate U47. If the selector straps are in the horizontal position, the gate receives all high inputs after the 85th character has been written. The resultant low from U47 is applied to count up gate U49C, inhibiting that device. Additional input pulses are thereby prevented from incrementing the circuit.

The Line End pulse is also applied to U11C, causing a high to be placed on the J input of U53B. The next negative-going transition of the 2 MHz signal causes U53B to one-set, placing a high on the J input of U53A. The following negative transition of the 2 MHz clock causes U53A to one-set, putting a low on the $\overline{\text{EOL}}$ line. This low is also sent back to the clear input of U53B to zero-set it. This causes the J input to U53A to again go low. The next negative transition of the 2 MHz clock causes U53A to again zero-set, ending the $\overline{\text{EOL}}$ signal.

If the Auto CR strap is connected to the IN position, the 1/2 μs $\overline{\text{EOL}}$ pulse is also sent to U55, causing a reset pulse to be developed. This resets the X register to the Left or Center margin as determined by U19B in the Margin Control circuit.

Space Circuit. This circuit controls the movement of the register in 12 point increments as required by the character writing positions. It also controls the direction of movement and the $\overline{\text{SPAC COMP}}$ output signal. Assume that Alfa Mode exists and that the COMPOSE line is low. When the character generator finishes with character writing, a $\overline{\text{CHAR COMP}}$ signal is received, causing a high to be applied to U37D. U37D generates a low output and applies it to Space gate U51A. The resultant high produces a low from U11D which causes U57B to generate a high pulse output. This output zero-sets space FF U17A.

The low from pin 15 of U17A places a disabling low on Right Left Control flip-flop U17B. The high from U17A pin 14 is placed on the T input of U16B and also applies a high to U15C and U15D. The outputs of U15C and U15D pulse low for 1/2 μs each time the 2 MHz signal goes high. This causes the register to move one point, and also causes ÷ 12 Counter U13 to increment. Gates U15C and U15D are permitted to pass 12 clock pulses from the 2 MHz line. U13 emits a high pulse which ends when the 12th clock pulse is applied. This causes Space flip-flop U17A to become

one-set, which applies an inhibiting low to ÷ 12 Clock Gate U15D and Space Clock Gate U15C. The negative-going output from pin 14 of the Space flip-flop also causes U16B to become one-set. The next negative transition of the 2 MHz line causes U16A to become one-set, applying a low on the $\overline{\text{SPAC COMP}}$ line. This low is also applied back to U16B, causing it to zero-set. With the high removed from the J input of U16A, the next negative transition of the 2 MHz clock causes U16A to again zero-set, ending the $\overline{\text{SPAC COMP}}$ signal. A similar evolution occurs in response to the TAB input signal. If in COMPOSE Mode, the SP EXEC signal also causes identical circuit reaction.

If the left or right directional shift key is pressed, the $\overline{\text{X CUR PULS}}$ signal line goes low, causing a high to be applied to U59C. If the Terminal is not in Compose Mode, a low is emitted by U59C and applied to U57B to cause Space action essentially the same as that just described. If the left directional shift button has been actuated, the $\overline{\text{X CUR PULS}}$ is accompanied by a $\overline{\text{CUR LFT}}$ signal, which passes through U39D and applies a high to U59B. The resultant low from U59B passes through U37B and U33E to zero-set Right-Left Control flip-flop U17B. The low from pin 11 is applied to U51C, placing a high on U49B to enable that device. The high from U51C is inverted by U33C to place an inhibiting low on U49C. Under this condition, the countup circuit is inhibited and the countdown circuit is actuated. The 12 clock pulses from U15C are then routed through U51B and U49B, causing the counter to decrement 12 points.

Note that Space flip-flop U17A applies an inhibiting low to the J input of the Right-Left Control flip-flop during the time that the counter is decrementing. As soon as the 12 clock pulses have been processed by the circuit, the Space flip-flop becomes one-set, applying a high to the Right-Left Control flip-flop. The next negative transition of the 2 MHz clock causes the Right-Left Control flip-flop to become one-set, removing the countdown command from U51C.

Whenever U11D applies a space enabling signal to U57B, it also is applied to U35D. This places a high on U35A. If a $\overline{\text{DBL SZ CHR}}$ signal is present, U35A generates a low output which one-sets U19A. The resulting low from pin 14 keeps the output of U57B high, holding U17A zero-set. When the ÷ 12 counter completes its cycle, it sends a high pulse to Space flip-flop U17A. However, with that device held in its zero-set condition, the pulse is ignored. The pulse from the ÷ 12 counter is also applied to Double Size flip-flop U19A, causing it to become zero-set. This removes the low from pin 12 of U57B. The ÷ 12 counter continues through a second sequence. When that second sequence is ended, the resultant output pulse is applied to U17A. Since U17A is no longer held zero-set by the Double Size flip-flop, it is permitted to become one-set, ending the space cycle after 24 points rather than 12 points.

When a $\overline{\text{BAK SPAC}}$ command is received, it causes lows to be applied to U35D, U57B, and U37B. This causes a reaction essentially the same as that which results from pushing the left directional shift button at the keyboard.

X D/A TC-13

TC-13 circuit card can be broken into the following sections:

Data Latches

Current Summing

D/A Amplifier

Delta X Control

GDIV Control

GDLI Control

Character Matrix Control

Italics Control

Double Size and Cursor Shift Control

The Data Latches consist of ten D-type latches. When the X ENABLE line goes high, the latch inputs are permitted to control the outputs. When the X ENABLE signal is removed, the outputs remain at the value that exists at the time X ENABLE went low. The combination of highs and lows on the $\overline{\text{1X}}$ through $\overline{\text{512X}}$ lines are therefore made available to the current summing network, which is the input to the D/A Amplifier circuit. Each latch is associated with a pair of steering diodes. For example, if the $\overline{\text{1X}}$ bit were low when X ENABLE strobed it through the latch, it would cause CR1 to conduct, putting a relatively low voltage at the CR1-R1 junction. This would back bias the associated diode in U23. Current would be unable to flow between R1 and U3 in the D/A Amplifier circuit. Suppose that the same X ENABLE pulse strobed in a high $\overline{\text{2X}}$ signal through U61B. CR3 would then be back biased; R3 and R4 would draw current through the appropriate diode in U23, with this current affecting the U5 Amplifier.

The number of diodes in U23 and U25 enabled at any given time determines how much current is being demanded through the feedback resistors of U5, thereby controlling the U5 output. The more diodes that are enabled, the more positive the effect at the negative input of U5, and the more negative the U5 output. This output is applied to U3, where it is again inverted.

Zero position exists at the left of the screen in the X Register. Therefore, when the circuit is zeroed, all input lines will be high, steering diodes CR1 through CR19 will be back biased, the diodes in U23 and U25 will be conducting. A maximum positive signal will exist at the input of U5. This results in a maximum negative output from U5, a maximum positive out of U3, a positive out of U33, and a negative out of U35. (Note that of the four amplifiers mentioned, all except U33 are inverters.) When the beam is positioned to the extreme right of the screen, all of the $\overline{1X}$ through $\overline{512X}$ lines will be low. Diodes CR1 through CR19 will be conducting and the diodes in U23 and U25 will be back biased. This results in a minimum current to U5, which is indicative of a minimum positive signal. Considering this minimum positive as a negative signal into U5, this causes a positive out of U5, negative out of U3, negative out of U33, and a positive out of U35.

The Data Latches just discussed permit the X Register to control the position of the writing beam. However, when characters are being generated, the Data Latches merely determine the starting position or reference position for the character. The positioning of the beam for actual character writing is controlled by the Character Matrix Control circuit at the bottom right of the schematic, and by the Double Size and Cursor Shift circuit. Note that the positive input of U35 is accepting current signals from each of the NAND gates and inverters at the bottom of the schematic, and also from transistors, Q31, Q47, Q49, and Q53.

When the Character Generator Matrix is at row 1—column 1, and the Character Rotator is selecting vertical characters, KR1 is low, KR2, KR3 and KR4 are high. This provides high, low, low, low outputs from the respective inverters. The low outputs generated by KR2, KR3, and KR4 are felt at the positive input of U35, placing U35's output at a reference point for the character matrix.

When row 2 is selected, it is indicated by KR2 going low. This causes the U17D output to go high, having a positive effect at the U35 positive input and at its output. This positive output from U35 causes the display beam position to move 1 dot position to the right. In a similar manner, when KR3 or KR4 go low, their outputs go high, causing the positive effect again at the U35 output.

It should be noticed that this explanation has merely mentioned positive effect. In reality, each time one of the gates has its output go high, it increases the current drive from U35, causing an increase in U35 output in a positive direction.

When character rotation is ordered, a $\overline{\text{KR SHIFT}}$ signal places a high on the U35 input to modify character starting position. With 90° or 270° character writing commanded, KR1, KR2, KR3, and KR4 reflect the output of the column positions from the Character Generator Matrix. During vertical and 180° character writing, KR1 is inactive and KR2, KR3, and KR4 reflect the row position output of the Character Generator Matrix.

The Italics circuit is normally used only during vertical character writing. When italics is commanded, the high ITALIC signal provides lows out of U75B and Q53. These are applied to opposite sides of U35 to compensate each other. As different rows are selected by the A, B, C, and D signals, these signals are also applied to the TC-13 X D/A circuits to cause a slight shift in horizontal position of the dot, proportional to the row which is being written. When the bottom row is being written, no shift occurs. As the rows above are selected, combinations of A, B, C, and D are received, causing low outputs from the respective gates. These low outputs are applied to the negative side of U35, causing a positive output. Therefore, as higher and higher rows are written, the dot placement is moved further and further to the right, giving an overall slanted appearance to the character.

When characters such as a lower case g are received, part of them must be written below the line. A $\overline{\text{SHIFT DOWN}}$ signal is received, causing its gate to apply a high to the minus input of U35, shifting the starting position of the matrix slightly to the left to give a natural appearance to the character.

Double Size and Cursor Shift Circuit. When Cursor Shift and Double Size Character are not commanded, Q31, Q47, and Q49 are conducting. With Q49 conducting, its emitter voltage is applied to the cathode of the Character Matrix Control diodes, thus limiting the positive value to which the gate outputs can go. When a Double Size Character is ordered, $\overline{\text{DBL SZ CHR}}$ cuts off Q47 and Q49, permitting the Character Matrix Control circuit to rise to a higher positive value when commanded by the input gates. This permits a larger signal to be applied to U35, causing the dot displacement to be greater. The net result is that a larger character is written.

Q31 is turned off during Alphanumeric Mode cursor writing whenever $\overline{\text{CUR SHF}}$ is received. At this time, the Q31 output goes positive, causing a positive input to the negative side of U35. This causes the U35 output to go negative, shifting the matrix starting position to the left. If $\overline{\text{DBL SZ CHR}}$ is not in effect at this time, Q49 is conducting and supplying part of the current demanded by R81. If $\overline{\text{DBL SZ CHR}}$ had been commanded, Q47 would be cut off, Q49 would be cut off, and no current would be provided through CR87 to R81. This means that more current is demanded from the U35 circuit, causing a greater displacement of the starting point, as is necessary during double size character writing.

GDIV Control Circuit. Whenever linear interpolate is not in effect, the output from amplifier U3 is felt almost instantaneously through R71 at the positive input of U33. However, when linear interpolate is commanded, the first vector after linear interpolate is selected finds a GDIV signal coming in to turn Q13 on. This causes CR62 to be back biased, and permits Q29 to be turned on quite hard. This permits changes in U3 output voltage to appear directly on the positive input of U33. However, after the first vector has been written, GDIV goes low and GDLI goes high. With GDIV low, CR62 is conducting and the effect of the 15 V being applied to R62 holds Q29 cut off. However, the high GDLI signal turns Q57 on, back biasing CR67. Q59 turns on. Now, any changes in U5 output voltage must charge C69 through R71 and Q59 before the effect can be felt at the positive input of U33. This integration of U3 output signals permits relatively constant vector brightness.

Delta X Control Circuit. The DELTA X output is used on another card in conjunction with beam intensity during vector writing. Its purpose is to permit the Z axis to be turned on as a function of the X or Y vector length, depending upon which is longer. When changes in X Register outputs occur, the U33 output is applied to integrating amplifier U37. The current necessary to charge C52 causes an output voltage proportional to the change of input signal. VR52 and VR53 limit DELTA X output signals to approximately 12 V.

Internal Data Routing TC-14

TC-14 is the Internal Data Routing circuit card for the Terminal. Several functions are performed on this card. One of them is the routing of data directly to the Character Generator in Alphamuneric Mode; another is the routing of data to the Scratch Pad Memory circuit, and the subsequent release of this data from the memory circuit to the Character Generator. In addition, the Internal Data Routing card contains the circuitry for insertion and deletion of data in the Scratch Pad Memory circuit. An Execute circuit is also contained on this card.

The circuitry will be discussed in the following order: Data Select Gates, Execute Circuit, Scratch Pad Memory, Scratch Pad Input/Output, Scratch Pad Delete Circuit, Delete Comp Circuit, Scratch Pad Insert Circuit.

Data Select Gates. When in Direct Mode, the COMPOSE line is low, causing the Data Select Gates to route DR1 through DR8 data directly through this card and out on the DB1 through DB8 lines. When Compose Mode is selected, the DR1 through DR8 bits are blocked from the Data Select Gates; outputs are then taken from scratch pad shift registers U1 and U5. The output lines are sampled by a series of inverters which detect NUL signals. Whenever a character is in process, detected NUL signals and inverted $\overline{\text{CHAR PROC}}$ signals combine in U35B to produce a low $\overline{\text{NUL DET}}$ signal.

Execute Circuit. When in Direct Mode, U35A is inhibited by a low at its pin 1 input. It therefore presents a constant high output, disabling U51A and providing U55B with an enabling voltage. If the $\overline{\text{TC INHIB}}$ line is high and no delete character is present, U55B is permitted to respond to the pin 9 input. If in Alphanumeric Mode and no character is in process, U55A produces a low output in response to an EXEC signal input. If an $\overline{\text{AUX PLOT}}$ condition does not exist, U51C responds to the U55A output, causing U55B to develop a $\overline{\text{CHAR EXEC}}$ signal.

When in Compose Mode, U35A pin 1 goes high. At any time a control character is received into the circuit, it is detected by control character Detector U51B and causes the U35A output to go low. This disables U55B and provides U51A with an enabling voltage. Subsequent EXEC pulses then cause CF EXEC signals to be generated, rather than $\overline{\text{CHAR EXEC}}$ signals.

Scratch Pad Memory Circuit. This consists of two 4000 bit memory devices and a negative 6 volt power supply circuit. Data bits are applied to pin 1 of U37 and are clocked into the device by the MOS CLK signal. Each MOS CLK signal advances the data one position through the memory circuits while clocking in the next data bit. Data moves out of U37 pin 8 and is accepted in U57 on pin 1. The output from U57 pin 8 is applied to U9E for processing by the Scratch Pad Input/Output circuit. An initializing circuit is included on later versions of the circuit card. At turn-on, $\overline{\text{INITIAL}}$ goes low and permits 1 MHz clock pulses to cycle the Memory Circuit. Since $\overline{\text{INITIAL}}$ is also applied to U17C, the memory circuit becomes completely loaded with high bits. Data in the Memory Circuit is the inverse of true data, and its contents thus represent a succession of NUL characters.

Scratch Pad Input/Output Circuit. Assume that Compose Mode exists and a character is to be entered into the Scratch Pad circuit. The data bits appear on the DR1 through DR8 lines, and are applied to the parallel inputs of U1 and U5. Compose Clear gate U13A and Compose Set gate U13C each have two high inputs. A CLEAR signal is received from TC-5 and causes U13A to produce a low output, clearing the U1 and U5 Shift registers. One-half microsecond later a SET signal is received from TC-5 and causes U13C to generate a low output. This applies a high to the preset inputs of U1 and U5. This preset signal permits the content of the parallel input lines to appear at the output lines of U1 and U5. The least significant data bit appears at U1 pin 15, while the most significant data bit appears at pin 13 of U5. This signal at pin 13 of U5 is applied to the Compose Serial Output Gate U31D. The signal at pin 13 of U31D remains high under all except for delete conditions. Therefore, the U31D output is an inverted representation of the bit data at U5 pin 13. U13B and U17C cause the U31D output to be applied to the serial input of U37 in the Scratch Pad Memory circuit. After the data has been loaded into the Scratch Pad Shift Registers, a series of 8 MOS CLK pulse is received by the

circuit. These cause the data bits in U1 and U5 to be sequentially clocked out on pin 13 of U5, with the most significant bit leaving first and the least significant bit leaving last. These data bits are applied to the input of U37 and are sequentially accepted by the memory circuit.

Now assume that the Scratch Pad Memory has data in it and that a character bit 8 is present at U57 pin 8. The effect of this data bit is felt through U9E, U11C, and U29D, making it present at the pin 9 input of U1. The next MOS CLK pulse to arrive causes this bit to be clocked through U1 and appear at the pin 15 output. The MOS CLK pulse also causes the Scratch Pad Memory to make the next data bit (in this case bit 7) available at the U57 pin 8 output. The following MOS CLK pulse will then clock bit 7 in through pin 9 of U1, at the same time advancing the pin 15 output data to pin 14. Bit 7 now appears on pin 15 of U1 and pin 8 appears on pin 14. After six more clock pulses, bit 8 has advanced to pin 13 of U5 and bit 1 appears on pin 15 of U1. The Shift Register has now been loaded with the next character. The bits are felt through the Data Select Gates and appear on the DB1 through DB8 lines. The Scratch Pad Shift Register outputs are also available to the output data selector circuit on TC-2 via the SP1 through SP8 lines. This permits the Scratch Pad to transmit data to the computer in On Line-Send Mode or to the screen in Local Send Mode.

Scratch Pad Delete Circuit. If a character is to be deleted from the Scratch Pad Memory, the Scratch Pad Cursor is placed above this character. Edit Mode is selected and the delete key is pressed. The $\overline{\text{EDIT FF}}$ signal and the output of Delete Detector U45 causes U15D to produce a high output. When the Scratch Pad Shift Register contains the character over which the cursor is placed, an AGREE signal is developed by TC-5. This is applied to U17D, causing it to generate a low output. This one-sets the delete flip-flop U33A. The pin 13 output of U33A disables the Compose Serial Output Gate U31D. It is also applied to U31A to send a disabling voltage to the Compose Serial Gate U11A. The high from the pin 12 output of U33A is applied to the Delete Mode Shunt U31C.

Note the condition that exists. With Compose Serial Output Gate U31D disabled, serial data from U5 is prevented from going to the input of the Scratch Pad Memory circuit. Serial output data from the Scratch Pad Memory circuit is prevented from reaching the serial input of U1 because Compose Serial Input Gate U11A is disabled. With the Delete Mode Shunt Gate U31C enabled, the output from pin 8 of U57 loops through U9E, U31C, U13B, and U17C directly back to the input of the memory circuit. Under this condition, the data to be deleted is contained in the Scratch Pad Shift Register and is isolated from the Scratch Pad Memory circuit. When the next set of eight MOS CLK pulses is received, the data being clocked out of U57 is clocked directly back into U37. The data which is contained in the Scratch Pad Shift Registers is clocked out of pin 13 of U5, but is not received by any circuit and therefore disappears from the Scratch Pad Memory.

At the same time that the character bits are being clocked out of U1 and U5, zeros are being clocked in at U1 pin 9. After the last character in memory has been clocked out of U57 and back into U37, a $\overline{\text{RSET INS}}$ signal is received. U35C and U31B cause delete flip-flop U33A to zero-set. The circuit then returns to normal operation. Note that the character has been removed and that no gap exists in its previous position. Also note that all data in the Scratch Pad Memory which follows the deletion point has been moved one position to the left as viewed on the Scratch Pad display.

Delete Complete Circuit. When the delete signal is received and detected by U45, it disables U55A in the execute circuit and prevents $\overline{\text{CHAR EXEC}}$ or CF EXEC signals from being generated. The Delete Detector output is also inverted by U47F and applied to the J input of U19A. The EXEC signal which accompanies the delete character causes U19A to become one-set. The negative transition of a subsequent 1 MHz clock pulse causes U19B to become one-set, applying a high to U17B. When the 1 MHz signal again goes positive, U17B develops a low output to cause an $\overline{\text{AUX D COMP}}$ signal to leave the circuit. In addition, the output from U17B is fed back to U19A to zero-set that device. This removes the high from J input of U19B. When the 1 MHz again goes low, U19B zero-sets and disables U17B.

Scratch Pad Insert Circuit. When a character is to be inserted, the Insert Shift Registers are brought into use to permit inserting the new character at the desired point in the string of characters in memory. To insert the character, an $\overline{\text{EDIT FF}}$ signal is applied to the circuit. When the Insert button is pushed, the $\overline{\text{INSERT}}$ signal arrives. This causes U15C to generate a high output. When the character over which the cursor appears is present in the Scratch Pad Shift Register, an AGREE signal is received from TC-5. This causes U35D to generate a low output, causing insert flip-flop U33B to become one-set. This causes several things to happen. The low output from pin 8 of U33B is applied through U31A to place an enabling voltage on U11B. U31A also places a high on U9D to send a low to disable the Compose Serial Input Gate U11C. The low from pin 8 of U33B also disables the Compose Set and Compose Clear gates U13C and U13A. At the same time, the high from U33B pin 9 is applied to the Insert Serial Gate U11A to enable it. The high from U33B pin 9 is also sent to U29A and U29B to enable those two devices.

When the character to be inserted is entered at the keyboard, the data bits appear on the DR1 through DR8

lines. This is followed by a CLEAR signal, which causes U29A to clear the Insert Shift Registers U7 and U3. One-half microsecond later, a SET signal arrives and causes U29B to generate a low output. This causes the input bits to be loaded into U7 and U3. The bit 8 data becomes available at the pin 13 output of U7, while the bit 5 data becomes available at pin 10 of U3. Now note the situation that exists. The new character to be inserted is contained in the Insert Shift Registers. The Insert Serial Gate U11A is enabled, making the U7 pin 13 output available to the serial input of Scratch Pad Shift Register U1. The output of the Scratch Pad Memory circuit is routed through U9E, U17A, and U9A making it available to the serial input of Insert Shift Register U3. At this time, the Scratch Pad Memory output is being blocked from Scratch Pad Shift Register U1 by the inhibiting voltage on Compose Serial Input Gate U11A.

When the next set of MOS CLK pulses is received, the data from the Insert Shift Registers is sequentially clocked through U11A and U29D into U1 and U5 while the data contained in U1 and U5 is clocked through U31D, U13B, and U17C into the Scratch Pad Memory circuit. At the same time, the Scratch Pad Memory circuit output is clocked through U9E, U17A, U9A, into U3 and U7. After the last character in memory has been clocked into the Scratch Pad Shift Registers, a $\overline{\text{RSET INS}}$ pulse is received from TC-5, causing the insert flip-flop U33B to return to its zero-set condition. This restores the circuit to its normal Compose condition, and it continues to operate as previously described.

Character Generator Control TC-15

TC-15 initializes the character generator matrix writing and provides clock for advancing the character generator through its matrix. The dot-writing control information is routed through TC-15 and sent from TC-15 to the display unit. One additional function of TC-15 is to provide a cursor shift signal to permit writing the alphanumeric cursor alternately in each of two positions. TC-15 can be broken down into the following circuit areas: Clock Control, 5 μs Delay, Cursor Dot Control, Cursor Shift and Flicker Control, CG Reset, Reset Circuit, Dot-Writing Time, Alfa Written Dot Control, Unwritten Dot Control, and Graf Dot Control.

Alphanumeric Cursor Writing. The first of the circuits to be discussed will include the Clock Control, 5 μs Delay, Cursor Dot Control, and Cursor Shift and Flicker Control circuits. If in the Alfa Direct Mode, the ALFA 2 line is high and the COMPOSE line is low. Under this circumstance the Alphanumeric Cursor is written continuously as long as the display unit is in a "view" condition ($\overline{\text{HOLD}}$ line high). 2 MHz clock pulses are processed through the Clock Control circuit into the 5 μs Delay circuit. Every 5 μs a 1 μs pulse is delivered to U13, causing that device to generate a 50 to 300 nanosecond positive pulse to U35B. This pulse is adjustable by R48. Under the conditions described, U35B has highs on its other two inputs, and therefore generates a low output pulse and applies it to U53B, generating a SCAN CLK pulse. The SCAN CLK pulse is applied to U53A to generate a Z ENABLE pulse. When the SCAN CLK pulse ends, it steps the character generator matrix (on TC-16) to its next position. The 5 μs wait and then write cycle repeats itself until the matrix has been completely written, and then it recycles back through the matrix. This continues until another mode of operation is commanded.

There are two exceptions to the preceding explanation. One is that whenever the matrix generator is scanning the Y10 row, the Y10 signal into TC-15 is high, causing a low at the output of U33C. This disables U53A and prevents Z ENABLE pulses from causing a dot to be written. Therefore, only rows 1 through 9 are written in conjunction with the Alfa Cursor. It should be noted that $\overline{\text{AGREE}}$ is high at all times except when in Compose Mode and the Scratch Pad cursor is commanded to be written. It then overrides the inhibiting Y10 signal.

The second exception is the effect of the Cursor Shift and Flicker Control. This circuit provides a low pulse (of about 400 microseconds duration) to U33D about twenty-four times a second. These low pulses into U33D provide high outputs to enable U53A for the duration of the pulse. With U53A enabled for approximately 400 microseconds, approximately one full matrix is permitted to be written. When the Q12 output of the multivibrator again goes low, U17B changes state, sending a $\overline{\text{CUR SHF}}$ signal to the D/A circuits to cause a change in cursor writing position. The low pulse from Q12 causes U33D to enable U53A to permit one complete matrix to be written in the new position. $\overline{\text{CUR SHF}}$ signal is a symmetrical 12 Hz waveform, and causes the cursor to be written alternately in each of two positions. The net result is a flickering cursor, one rectangle of which appears on the character line and a second rectangle which appears below and to the left. The Cursor Shift and Flicker Control circuit is prevented from affecting U53A during the following conditions: When in graphics and ALFA 2 is low; when in Compose Mode (COMPOSE line high); and whenever a character is being written as indicated by a low on the $\overline{\text{CHAR PROC}}$ line.

Writing Stored Characters. When a character is to be written, a $\overline{\text{CHAR EXEC}}$ signal is received by the CG Reset circuit, causing U31B to put a high pulse on the CG RESET line. This sets the matrix in TC-16 to its starting position. The high pulse out of U31B is also applied to U49D, which generates a low output pulse to U31C. U31C sends a high output pulse to the 5 μs delay circuit and through U29D to the Dot Writing Time circuit, where it clears U7B and U11B. When the $\overline{\text{CHAR EXEC}}$ pulse ends, the pulse out of U31C ends and permits the timing circuit to start counting.

A one microsecond positive pulse out of U7B at the end of the 5 μs delay is applied through U29E and U9D to U11B. When the one microsecond pulse ends, U11B clocks to a one-set condition and applies a high to Alfa Written Dot Control gate U35A.

Assume that a character is in process and that a command is being received to write the dot. Under this circumstance, $\overline{\text{CHAR PROC}}$ is low and Z is high, with these two resulting in high enabling voltages on U35A. The positive signal from Dot-Writing Time flip-flop U11B causes a low out of U35A, which lasts 5 μs. Then the 5 μs Delay circuit again sends a pulse from U7B through U29E and U9D to zero-set U11B. During the time that the 5 μs positive pulse froom U11B is being applied to U35A, that device sends a low to U53B to generate a high SCAN CLK pulse. The high SCAN CLK pulse is applied to U53A to generate a Z ENABLE pulse.

Not all dots in a matrix are written while a character is in process. For the unwritten dots, another circuit is put into effect. During the time that $\overline{\text{CHAR PROC}}$ is low (indicating a character is in process) the Z line goes low whenever dots are not to be written. Under that circumstance, two highs are applied to U33A, causing its output to be low. This low from U33A disables U53A (Z Enable Gate) and at the same time is applied to U31C in the Reset Circuit. As long as this condition exists, U31C will apply a high to the 5 μs delay and a low to the Dot Writing Time circuit, holding flip-flops disabled in their zero-set condition. The low from U33A is also applied to U55C, placing a high on U49C. Each 2 MHz clock pulse is then permitted to pass through U49C, sending a low to the Scan Clock Gate to create a SCAN CLK pulse. The matrix generator in TC-16 is thus advanced at a 2 MHz rate until such a time as another dot is to be written. At that time, the Z line goes high and the Alfa Written Dot Control circuit again takes over.

Writing Scratch Pad Characters. When the Terminal is placed in Compose Mode, the COMPOSE line goes high. This produces a constant high output from U33D (via U55B, U35C, and U55F), and locks out the effect of the Cursor Shift and Flicker Control circuit. It also places a high on U33B to permit $\overline{\text{CHAR PROC}}$ to control the CG RESET Circuit. In addition, it places an enabling voltage on U9C in the Dot Writing Time circuit. Whenever the $\overline{\text{CHAR EXEC}}$ signal is received, CG RESET is generated and the 5 μs Delay and the Dot Writing Time circuits are cleared. When the $\overline{\text{CHAR EXEC}}$ signal ends, the 5 μs delay counts to 5 microseconds, U11B (in the Dot Writing Time circuit) becomes one-set, sending a high pulse to U35A. This causes a low into U53B to generate a SCAN CLK pulse which also generates a Z ENABLE pulse, if the dot in that position is to be written. The high from U11B (in the Dot-Writing Time circuit) is also sent back to U9C, where it places an enabling voltage on that device. With both inputs to U9C high, its output goes low to disable U9B. This low from U9C is also applied to U29F to place a high on U9A. The next high pulse from U7A causes a low pulse from U9A which produces a high pulse from U9D. At the end of the high pulse, U9D zero-sets flip-flop U11B, ending the high pulse from that device. The duration of this pulse is one microsecond. Therefore, SCAN CLK pulse duration and the Z ENABLE pulse duration is one microsecond in Compose Mode. As in Alphanumeric Mode, if a dot is not to be written in the selected position, the Z line is low. This disables U35A (Alpha Written Dot Control Gate) and enables the Unwritten Dot Control circuit. Unwritten dots are therefore processed at a 2 MHz rate as a result of U49C in the Unwritten Dot Control circuit. It should be noticed that when in Compose Mode with $\overline{\text{CHAR PROC}}$ high, U33B applies a low to U31B, causing CG RESET to exist until the next character is to be written and $\overline{\text{CHAR PROC}}$ again goes low.

Writing Graphic Points. Now assume that the Terminal has been switched to Graphics Mode and the ALFA line goes low. This does the following things: It places a low on U49D in the Reset Circuit and on U35B in the Cursor Dot Control circuit, disabling these two devices. It places a low on U31B in the CG RESET circuit to hold the CG RESET line high. It also places a low on U35C in the Curosr Shift and Flicker Control circuit to lock out the effects of the multivibrator. The low on Alfa 2 is inverted by U29B, placing an enabling high on the Graf Dot Control circuitry and on U49B in the Reset Circuit.

When a point is to be written, a GRAF Z signal arrives and causes a low from U49B. This low zero-sets U11A in the Graf Dot Control circuit, and at the same time resets U7B in the 5 μs Delay Circuit and U11B in the Dot Writing Time circuit. When the GRAF Z pulse ends, the 5 μs Delay Circuit goes through a 5 μs count and then one-sets U11B in the Dot Writing Time circuit. This causes a high to be applied to U31A, sending a low to U53B to generate a SCAN CLK pulse, which goes to U53A to generate a Z ENABLE pulse. At the end of 5 μs, U7B sends another transition to U11B to zero-set that device. This applies a low to U31A, which causes a high to go to U53B to end the SCAN CLK pulse. When the SCAN CLK pulse ends, the Z ENABLE pulse also ends. In addition, the end of the SCAN CLK pulse is fed back as a clock pulse to U11A to flip that device to its one-set state. This causes U11A to place a low on U31A, inhibiting further pulses until such a time as another GRAF Z pulse arrives to again zero-set U11A.

Character Generator Memory TC-16

The purpose of TC-16 is to generate an 8 X 10 matrix for character writing purposes. As the matrix is generated, the CRT beam is positioned through eight discrete column positions in each of 10 rows. The TC-16 circuitry makes a

dot-writing determination in each of the eighty positions. Circuits contained on TC-16 include the Matrix Generator, Data Latches, ROM Select, Read Only Memory, ROM Section Select, Z Enable Gates, Character in Process, Character Complete, Shift Down, Control Character Symbol Enable, and Scratch Pad Cursor Gate. They will be discussed in that order. Refer to the TC-16 Block Diagram in the Diagrams section.

Matrix Generator. In Alpha Mode, character writing is initiated by a CG RESET signal and a $\overline{\text{CHAR EXEC}}$ signal. The CG RESET signal sets ÷ 8 device U55 and Column Decoder U37 to column one condition. With the aid of the Alfa Reset circuit, it also sets ÷ 10 device U31 and Row Decoder U29 to row 10 position. After the CG RESET signal ends, the SCAN CLK pulses are permitted to clock the ÷ 8 and Column Decoder devices through the eight column conditions. At the same time, various combinations of highs and lows are sent out on the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines to cause the X D/A Register to move the CRT beam to each of the eight column positions. After the Column Decoder has reached column 8, the next SCAN CLK pulse resets the circuit to column 1. The column 8 pulse is applied to the ÷ 10 circuit to clock the Row Decoder to row 1. Subsequent column 8 signals into the ÷ 10 circuit clock the Row Decoder sequentially through to column 10. Various combinations of highs and lows are sent to the Y D/A circuit on the A, B, C, and D lines to deflect the CRT beam to each of the ten row positions. The column signals are applied to the Z Enable Gates, sequentially enabling them. The outputs from the Row Decoder are applied to the Read Only Memory circuit to address those devices to each of the matrix positions to determine whether or not a dot should be written in the selected point.

The matrix generator is inoperative during Graphics Mode. A constant CG RESET signal is received to hold the matrix locked in its row 1 column 1 position. The low on the ALFA 2 line disables the Alfa Reset circuit and enables the Graphics Reset circuit, causing row 1 (rather than row 10) to be selected.

Data Latches. The $\overline{\text{CHAR EXEC}}$ signal strobes the DB1 through DB7 bits into the Data Latches. DB1 through DB5 are applied to the Read Only memory circuit while DB6 and DB7 are applied to the ROM Select circuit. If DB6 and DB7 indicate that a control character is contained in the code, the ROM Select circuit sends a signal to the Control Character Symbol Enable circuit. Otherwise, the ROM Select circuit enables one of the three Read Only memory devices. The specific device enabled is dependent upon the coding of bits 6 and 7.

Read Only Memory. The Read Only Memory circuit consists of three ROM devices, selection of which is determined by the ROM Select circuit. Each of these ROMs contain two sections, selectable by a signal from the ROM Section Select circuit. One section of these devices is selected when rows 1 through 5 are indicated by the Row Decoder, while the second section is selected while rows 6 through 10 are indicated. Although the rows 1 through 5 signals are contained on the same respective line as the rows 6 through 10 signals, they affect different addresses in the ROMs due to the ROM Section Select signal applied to the devices. With data bits applied to the Read Only Memory circuit, and one of the devices selected by the ROM Select circuit, and a specific section selected by the ROM Section Select circuit, the Row Decoder sequentially enables each of the five row signal lines. The combination of signals into the Read Only Memory results in dot disclosure information on each of the seven output lines.

Z Enable Gate. The column decoder sequentially enables each of the Z Enable Gates. If a dot is to be written in any of the columns, coincidence is obtained with a high from the Read Only Memory circuit and a Z output signal is generated.

Character In Process. When the $\overline{\text{CHAR EXEC}}$ signal is received, it zero-sets Char Proc FF U19A. When the $\overline{\text{CHAR EXEC}}$ signal ends, U39D generates a $\overline{\text{CHAR PROC}}$ signal. The Character in Process circuit then applies enabling voltages to the Scratch Pad Cursor Gate, the Character Complete Gate, and the Shift Down circuit. When matrix writing is complete, a signal from the Character Complete Gate one-sets U19A, ending the $\overline{\text{CHAR PROC}}$ signal.

Character Complete Gate. This circuit is enabled by the Character in Process circuit after the $\overline{\text{CHAR EXEC}}$ signal is received. When the matrix generator circuit completes scanning the matrix, the combination of Y10, column 8 and SCAN CLK signals causes a $\overline{\text{CHAR COMP}}$ signal to be developed. This $\overline{\text{CHAR COMP}}$ signal is routed back to the Data Latches to clear them. The next SCAN CLK pulse to reach the ÷ 8 circuit causes the column 8 signal to be removed from the Character Complete gate, ending the $\overline{\text{CHAR COMP}}$ signal. Removal of the $\overline{\text{CHAR COMP}}$ signal from the Character in Process circuit ends the $\overline{\text{CHAR PROC}}$ signal.

Shift Down. The lower case characters g, j, p, u, and y and the underline symbol must be partially written below the character base line. Therefore, when code representing these characters is received by the Read Only Memory, dots are disclosed in the row 10 position. Writing of these dots is prevented by sending a Y10 signal to the TC-15 circuit. The dot disclosure information and the Y10 signals are both applied to the Shift Down circuit. Coincidence between the two cause this circuit to develop a $\overline{\text{SHIFT DN}}$ signal, which causes the Y D/A circuits to shift the character matrix down sufficiently to present a normal appearing character.

The Shift Down circuit is reset and the $\overline{\text{SHIFT DN}}$ signal removed when the $\overline{\text{CHAR PROC}}$ signal ends.

Control Character Symbol Enable. This circuit operates only in the Scratch Pad Modes, because that is the only time that $\overline{\text{CHAR EXEC}}$ signals accompany coded control character data. Assume that the Terminal is in a Scratch Pad Mode and that a control character is strobed into the Character Generator circuit by the $\overline{\text{CHAR EXEC}}$ signal. The ROM Select circuit sends a Control Character signal through U45A and U45B to enable U59C. While the matrix generator is scanning row 1 through 4, U59C sends an enabling signal through U59D to the Z Enable Gate circuit, causing a Z signal to be sent to TC-15. This results in all dots in rows 1 through 4 being written in the position occupied by the Control Character in the Scratch Pad display. The Row 5—10 Detector disables the Control Character Symbol Enable output while the remainder of the matrix is being scanned. $\overline{\text{A NUL DET}}$ signal is applied to the Control Character Symbol Enable circuit to prevent the symbol from being written when Control Character NUL is being received.

Scratch Pad Cursor Gate. This circuit causes a Scratch Pad Cursor to be written in row 10. The cursor position is kept track of by a cursor counter in the TC-5 circuit. When the Scratch Pad Character Position Counter agrees with the Cursor Counter, an $\overline{\text{AGREE}}$ signal is received by TC-16. If the terminal is in Compose Mode, the Scratch Pad Cursor Gate sends an enabling signal to the Z Enable gates during the time that the matrix generator is clocking through row 10. Y10 provides an enabling voltage to U53A during this time. Dots are thereby written in the column 1 through column 7 positions.

Although this description was written in conjunction with a block diagram of TC-16, it can be re-read while following the schematic for a further understanding.

Plot Control TC-18

TC-18 is the plot control circuit board. It consists of the following circuits:

IP Direction Decoder

IP Enabling

IP Step Control

IP Graph Z Control

Mode Control

G Z Comp Control

Z Control

LI-Z Control

LI Control

Incremental Plot Mode. When an RS is received it causes the U47A-U47B flip-flop in the Mode Control circuit to generate a low output from U47A. This causes a high to be placed on the GRAF 2 line and a low on the ALFA 2 line. The RS signal also causes a low to be applied to U29B in the IP Enabling circuit. The U29B-U27C flip-flop places a high on U51A and on the clear input of U53A, enabling those circuits. The U27C output places a low on U43C, disabling that device.

Incremental Plot commands have a low DR7 and a high DR6. This causes highs to be placed on U51A in the IP Enabling circuit. The low from U51A passes through U45F to place enabling highs on the NAND gates in the IP Enabling circuit.

The status of bits DR1, DR2, and DR3 determine the direction that is to be commanded. This direction is decoded by U41 and its accompanying OR gates. The output from these OR gates is applied to NAND gates and then to the IP Step Control circuit. Circuit arrangement is such that 1, 2, 3, or 4 of the output lines can go low at any one time. For example, if a command to step in a downward direction is received, it is indicated by a 1, 0, 0 on the DR3, DR2, and DR1 lines, respectively. This causes a low at output pin 5 of U41, causing a high from U21C and a low from U23B. This results in a high from U1B which places an enabling voltage on U3A. When the TC IN $\overline{\text{STRB}}$ occurs, it supplies the third high to U3A, causing a $\overline{\text{STEP Y}}$ signal to occur, which causes the Y Register to decrement 1 point.

Now assume that a command to move the beam in a northwest direction is received; this is indicated by a 1, 1, 1 on DR3, DR2, and DR1. This causes a low on pin 9 of U41, resulting in highs from U21A and U43B. These highs cause lows from U23A and U1A. These cause lows to appear on the $\overline{+Y}$ line and on the $\overline{-X}$ line, as well as causing highs to appear at the U1C and U1B outputs. The $\overline{+Y}$ and $\overline{-X}$ signals are used to reverse the stepping direction of the X and Y Registers. The highs from U1C and U1B provide enabling voltages to U3B and U3A, so that when the TC IN STRB arrives, both of these devices generate low outputs on the $\overline{\text{STEP X}}$ and $\overline{\text{STEP Y}}$ lines to cause the actual stepping of the registers.

Whether or not the point is to be written is a function of DR4. If this line is high, then U23D will generate a low output, causing a low from U25A to disable gate U25D. With U25D disabled, GRAF Z pulses cannot be sent out when TC IN STRB occurs. However, if the DR4 line is low (indicating that a point is to be written), it places a high on U25B. This causes a low to be placed on U25A, providing U25D with an enabling voltage. Now when the TC IN STRB occurs, it places a high at pin 14 of U53A. The next negative transition of the 1 MHz line causes U53A to one-set, placing a high at pin 9 of U31C. The next time that the 1 MHz line goes high, U31C places a low on U5B to apply a high to U25D. This generates a low from that device, causing GRAF Z. The next negative transition of the 1 MHz line causes U53A to again zero-set, where it remains until the next TC IN STRB.

It should be noted that when the unwritten point was being plotted, U3C provided a high to U27A. When the TC IN STRB occurred, the U53A action caused the second high to be placed on U27A, providing a low to U9A. This low pulse to U9A caused a high pulse from that device, causing U7B to one-set. The next 1 MHz clock pulse caused U7A to one-set, generating a $\overline{\text{GZ COMP}}$ signal. This signal is fed back to U7B to zero-set the device. With U7B zero-set, the next 1 MHz clock pulse zero-sets U7A, ending the $\overline{\text{GZ COMP}}$ pulse. This pulse indicates that incrementing of the unwritten point has been completed. The GRAF Z pulse is routed to TC-15 and comes back as a Z ENABLE pulse. For written points, the Z ENABLE pulse is generated on TC-15 as a result of actually writing the point. It also goes through U5E to U9A to cause the same action as that which was caused by the signal from U27A.

Point Plot Mode. Point Plot Mode is initiated by the control character FS. When FS is received by U49C, it generates $\overline{\text{GS+FS}}$ which goes to TC-11 to generate GWA and $\overline{\text{GWA}}$. $\overline{\text{GWA}}$ returns to TC-18 where it is applied to U51A to disable the Incremental Plot Mode of operation. It is also applied to U43A to hold the ALFA line low while points are being plotted. GWA also returns to TC-18 where it is applied through U45D to U47B. This generates a low from U47A causing U31D to generate a high on the GRAF 2 line and a low on the ALFA 2 line.

When the last byte of a graphic address is received, a LO X EN signal arrives at TC-18 and is applied to U43C. This signal is accompanied by a TC IN STRB which also goes to U43C. The combination of these two causes a low from U43C, which makes U25C generate a GRAF Z output for TC-15. After 5 μs delay, TC-15 returns a Z ENABLE pulse to TC-18. This is routed through U31A and U9C to generate the Z OUT pulse which causes the display unit to write the point. When the 5 μs Z ENABLE pulse ends, its effect through U5E and U9A causes U7B to become one-set. The next negative excursion of the 1 megahertz line causes U7A to become one-set, generating a $\overline{\text{GZ COMP}}$ pulse. This pulse returns to U7B, zero-setting it. The next negative-going excursion of the 1 MHz signal causes U7A to return to its one-set condition, ending the $\overline{\text{GZ COMP}}$ pulse.

Linear Interpolate Mode. Control character GS initiates this mode by generating a low from U49C and a low from U49B. The low from U49C creates a $\overline{\text{GS+FS}}$ signal which causes TC-11 to return $\overline{\text{GWA}}$ and GWA to TC-18 just as in Point Plot Mode. The low from U49B zero-sets U53B, applying a high to U33C and a low to U33D. The low from U49B also causes the U29A output to go high, generating a GDLI signal through Q15 and providing enabling voltage to U9B. The high from U29A also causes the U27D output to go low, generating a high from U33A. This causes the X ENABLE and Y ENABLE lines to go low, isolating the X and Y D/A circuits from their respective registers.

The Plot Control circuitry remains in this condition until the last byte of an address is received. Then the LO X EN pulse combines with the TC IN STRB to generate a low from U43C. This is felt through U45C, U23C and U5C, causing a high pulse to be placed on U33A to generate X ENABLE and Y ENABLE pulses. The high from U5C is also felt through U9B and U29D, placing highs on U53B, U29C and U51B. U51B responds by generating an $\overline{\text{LI BUSY}}$ pulse and by generating a GDIV pulse by way of U33D and Q35.

When the X ENABLE and Y ENABLE pulses are applied to TC-13 and TC-9 respectively, they cause differentiated signals to return to TC-18 as DELTA X and DELTA Y. The amplitude and polarity of these signals is dependent upon the length of the vector being commanded and upon the direction of the new point with respect to the previous location of the CRT beam. These delta signals are felt through full wave network CR20, CR21, CR22, and CR23, causing Q59 to turn on and/or Q56 to turn off. In any case, a low is felt at the CR26-CR40 junction. This causes a high to be felt at the collector of Q54, causing CR43 to become back-biased. The +5 V applied to R44 is then felt at the pin 4 input of U31B. If it is in response to the first LO X EN to follow a GS command, pin 5 of U31B is low and no effect is felt at the U31B output.

When the LO X EN and TC IN STRB signals end, that effect is felt through U43C, U45C, U23C and U5C, causing the U9B output to return high. This causes the U29C output to go low, turning Q36 off. C67 now charges toward the +15 V being applied to it, until Q37 goes into conduction. This is normally adjusted to be approximately 2.5 ms. When Q37 goes into conduction, it turns Q38 on, causing a low to be applied to U51B, resetting the U51B-U29D flip-flop. At this time the $\overline{\text{LI BUSY}}$ signal returns high and U53B one-sets, remaining that way until

another GS command is received. Note that while U53B was zero-set, U33C was disabled and its low output blocked any signals through U31B.

When $\overline{\text{LI BUSY}}$ returns high, its effect is felt through U9A where it causes U7B to become one-set. This permits U7A to generate a 1 μs $\overline{\text{GZ COMP}}$ pulse as was explained for Point Plot Mode.

After the first vector to follow a GS has been completed, vectors are permitted to be written in the following manner. The LO X EN signal (which accompanies the last byte of the address) combines with the TC IN STRB to generate a low from U43C. This is felt through U45C, U23C, and U5C to generate the X ENABLE and Y ENABLE signals via U33A, U35B and U35C. At the same time, U9B causes the U29D output to go high. This causes the U51B output to go low, thus generating the $\overline{\text{LI BUSY}}$ signal. When the X ENABLE and Y ENABLE signals permit the contents of the X and Y Data Registers to be loaded into the X and Y D/A circuits, the DELTA X and DELTA Y signals are felt at the TC-18 circuit inputs. This causes a high to be placed at pin 4 of U31B as previously explained. With $\overline{\text{LI BUSY}}$ low and U53B one-set, two lows are being applied to U33C, causing it to apply a high to pin 5 of U31B. Therefore, U31B generates a low output which causes U9C to generate the Z OUT signal for unblanking the display beam. At the end of the LO X EN pulse, the U9B output returns high. This causes the U29C output to go low, again causing a 2.5 ms delay to occur. At the end of this 2.5 ms delay, Q38 goes into conduction. U51B generates a high output, ending the $\overline{\text{LI BUSY}}$ pulse. The effect of this transition is again felt through U9A to generate 1 μs $\overline{\text{GZ COMP}}$ pulse.

I/O Control TC-19

TC-19 circuitry consists of the following:

Xmit Ready

Receive Ready

Italics

Double Size

Double Intensity

Strobe Circuits

The purpose of the Xmit Ready circuit is to indicate to the interface that the Terminal has data ready to be sent to the computer. The Xmit Ready circuit goes into action when a DATA STRB is received. If the Terminal is On Line when DATA STRB ends, U3 one-sets, setting XMIT RDY high. When the computer accepts the data, $\overline{\text{XMIT COMP}}$ is received by TC-19. The trailing edge of this pulse causes U3 to zero-set, ending the XMIT RDY signal. If the Terminal is in Local Mode, ON LINE is low, causing U57C to develop a high output. This maintains a low on the clear input of U3, holding XMIT READY low. This same situation is also forced when ON LINE is high and the Terminal is in Compose Mode. At this time, U57A sends a low to U57C, again causing XMIT READY to be held low. If the Send button is pushed while in Compose Mode, $\overline{\text{SP SEND}}$ is received by U57A, permitting a low to leave U57C, releasing U3. DATA STRB and $\overline{\text{XMIT COMP}}$ signals are then permitted to raise and lower the XMIT RDY line, respectively.

Receive Ready Circuit. The purpose of the Receive Ready circuit is to generate a signal for the Interface Unit, indicating that the Terminal is ready to receive data. In order for the RCV RDY line to be high, the following conditions must exist. On Line must be selected at the Rocker switch, the tabulator must not be busy, page full condition must not exist, and $\overline{\text{ERAS INTV}}$ pulse must not be in process. Under these circumstances, the RCV RDY line is set high when ON LINE is initially selected, and can be reset high by a $\overline{\text{HOME}}$ pulse, an $\overline{\text{AUX COMP}}$ pulse, or a FUNC COMP pulse. Any of these cause a low pulse into U29A, causing a high pulse out. The end of this high pulse one-sets U5B, causing a low from U19E and a high RCV RDY signal from U25F. Whenever a RCV STROB arrives (indicating that data is being input). U9A becomes zero-set, causing U59A and U45D to zero-set U5B, locking RCV RDY in its low condition. The same situation results whenever a DATA STRB occurs while in Compose Mode, because of U55A and U55C.

Italics Circuit. The function of the Italic Control circuit is to write slanted characters whenever commanded by an ITAL CMD or a $\overline{\text{COMM ERR.}}$ When turned on, the Terminal generates an $\overline{\text{INITIAL}}$ signal, which passes through U21C and U43A to zero-set U41B. The first FUNC COMP signal to occur ensures that U45A has a high output, disabling U23B. While in Alphanumeric Mode, ALFA 2 is high, putting an enabling voltage on the other input to U23B. When a communication error occurs, $\overline{\text{COMM ERR}}$ goes low, causing the U45A output to go low, causing U23B to generate an ITALIC command. This command will remain as long as $\overline{\text{COMM ERR}}$ exists. When $\overline{\text{COMM ERR}}$ is removed, the next FUNC COMP will reset the U45A-U29B flip-flop, removing the ITALIC command.

If an ITALIC command is generated by a Control Character, the ITAL CMD line pulses high, causing U41B to one-set. This locks the U45A-U29A flip-flop so that a low is applied continuously to U23B, generating a constant ITALIC signal output. This condition remains until a US signal zero-sets U41B, releasing the flip-flop so that the next FUNC COMP signal can cause the ITALIC line to go low.

Double Size Character Circuit. The purpose of this circuit is to cause characters to be written double normal size in response to a Double Size Character command. (Incidentally, the DBL SZ CHR signal also causes double line spacing and double character spacing.) When the Terminal is turned on, the INITIAL signal causes U41A to zero-set, disabling U45B and placing a high on the DBL SZ CHR line. At any time that a double size character command occurs, a pulse on that line one-sets U41A, causing U45B to generate a low signal on the DBL SZ CHR line.

Double Intensity Circuit. The function of this circuit is to increase the intensity when double size characters are being written. The increase in intensity compensates for the increased display area required by double size character writing. When U41A one-sets in response to a DBL SZ CMD signal, lows are applied to U43B and U43C. Whenever a character is in process, the CHAR PROC line goes low, causing U43C to send a high through U43D and U21F to Q1, turning it on. This generates a low on the INTENS 2 line. U43B permits double intensity graphics to be written in response to DBL SZ CMD signals when the ALFA 2 line is low.

Strobe Circuitry. The function of this section of the circuit is to provide either a TC IN STRB or an AUX IN STR in response to inputs from either the DATA STRB line or the RCV STROB line. Let's presume that an RCV STROB has been received. It passes through U59C, placing a low pulse on U55D. This provides a high pulse to U9A, causing that device to become one-set. The high into the J input of U9B permits the 1 MHz clock signal to generate a high output from U9B, which is applied as an enabling voltage to U35A and U35C. The zero output from U9B is applied to U15B and U25E to zero-set U9A. The next negative transition from the 1 MHz clock line therefore causes U9B to return to its zero-set condition, ending the 1 μs output.

The purpose of U35A and U35C is to determine which of the two strobes will be generated. This is done in response to the status of U17A – the Strobe Select flip-flop. U17A is placed in its zero-set condition by the HOME signal upon initialization, thus automatically selecting the TC Input Strobe gate to output the U9B signal.

The Aux Input Strobe gate is selected at any time that graphics are to be written, as indicated by the GWA line going low. This puts a high on U23C, putting a low on the K input of U17A. When either PRNT BSY or AG go low, it places a high on the J input of U17A. Now when a DATA STRB or a RCV STROB occur, they cause U17A to change state and select the Aux Input Strobe gate.

POWER SUPPLY

+15 V Supply

Voltage from a winding of T1 is full-wave rectified by CR14, and developed across C14. Series regulator Q15 reduces the output to +15 V. The output is controlled by applying the 15 V across the R17-R19 circuit, feeding approximately +7 V back to pin 2 of U16, which is the inverting input to an error amplifier. If the +15 V output tends to increase, a positive error signal is sensed, inverted, and applied to the transistor which drives Q15. (The driver transistor is also a part of U16.) This decreases the drive to Q15, limiting the circuit current to a value which maintains the +15 V output within limits.

If the +15 V line accidentally becomes grounded, R15 develops enough voltage across it to turn on an error sense transistor in U16. This causes the driver to decrease the Q15 base voltage, keeping the Q15 current within non-destructive limits.

–15 V Supply

This supply is quite similar to the +15 V Supply, but the feedback circuit differs slightly. Pin 5 of U86 feels the full effect of –15 V changes. This is coupled to the non-inverting input of the error amplifier. The inverting input of the error amplifier (pin 2) feels only a portion of the –15 V Supply changes. If the –15 V output tends to go in a negative direction, the non-inverting input will receive a greater drive signal than the inverting input. The output will be in phase with the change (negative) and will decrease the drive to Q85. Q85 will limit the load current to the value required to keep the –15 V output within design limits. The circuit is protected from short-circuit damage in a manner similar to that in the +15 V Supply.

+5 V Supply

The +5 V Supply is powered by a center-tapped fullwave rectifier, and its output voltage is developed across C32. The load current flows through R75 and series regulator Q65. These components are paralleled by R66 and R67, which provides shunt paths to deliver sufficient current to the load. The circuit can deliver 5 to 10 amps with R67 paralleling R66, and can deliver 2.5 to 7 amps with R67 disconnected.

The output voltage is monitored by the voltage divider in the base circuit of U42A. Errors in the +5 V output thus cause in-phase signals at the Q60 base. Q60 inverts them and applies the out-of-phase results through drivers Q70 and Q72 to Q65. If the supply tends to go positive, the drive to Q65 is decreased. Q65 holds circuit current to a value which keeps the +5 V Supply within limits. Ripple is kept to a minimum by applying it through C59-R59 to the base of Q60, where it performs the same regulatory action as the +5 V SENSE feedback causes.

Two protective circuits exist in the +5 V Supply circuitry. One is for short-circuits and the other for over-voltage protection. If the output becomes short-circuited to ground, the increased Q65 current increases the drop across R75. This develops enough negative voltage at the R76-R77 junction to turn Q64 on. The Q64 collector drops from its normal +5.1 V. This negative signal drives the Q60 collector negative, applying a negative signal to the Q70 base. This decreases the Q65 drive, holding its collector current to a safe value.

CR61 is normally conducting, which holds CR60 back-baised. During short-circuit conditions the U42 collector voltage drops. When it gets near 0 V, CR60 conducts and limits it to that value.

Over-voltage protection is provided by the Q33-Q34 circuit. Sections C and D of U42 form a comparator. The +5 V is applied through a voltage divider to the base of the D section, holding the D section cut off during normal operating conditions. With R41 properly adjusted, the D section goes into conduction if the +5 V output reaches +5.4 V. Then Q34 conducts and applies a positive potential to the gate of Q33. Q33 goes into conduction and rapidly discharges C32 down to about +1 V, holding it there until the power is turned off. The action will repeat itself if the power is turned on before the over-voltage problem is remedied.

POWER ON Circuit

This circuit provides the Interface Unit with an indication of the Terminal power status. Under normal conditions, Q26 is cut off and its collector applies +5 V to the Interface Unit.

Q26 is held cut off as follows: CR11 and CR12 full-wave rectify the transformer voltage, charging C12 positive. This causes Q24 to conduct, holding Q26 cut off. The C12 discharge time is much shorter than the C32 discharge time in the +5 V Supply. If the input power should fail or falter, the C12 voltage drops rapidly. Q24 cuts off and the +5 V Supply pulls up on the Q26 base. Q26 conducts and drops the POWER ON line to a logical zero, informing the Interface Unit that a power disruption has occurred. The Interface Unit then prevents further interchange of data between the computer and the Terminal until normal power conditions are regained.

Primary Circuit

The Primary Circuit of the supply transformer is equipped with a Line Voltage Selector Assembly, Thermal Cutout switch S5, Display Unit Outlet J4, Power Switch S4, Electro-Magnetic Interference Filter FL1, and Power Plug P1. The Line Voltage Selector Assembly contains an external switch which permits easy switching between 115 V AC and 230 V AC operation. Proper fuse selection accompanies the switching. A second switch in the assembly permits selection of low, medium, or high operating range.

Miscellaneous

There are four separate ground circuits contained on the Power Supply circuit board to minimize interactive ground loop effects. Each is referred to chassis ground through separate pin connectors.

The power supply is capable of delivering a large amount of energy in a short time. Precautions listed in the Servicing Section should be observed when working on circuitry within the Terminal.

SECTION 3
SERVICING

Introduction

This section of the manual contains information for use in preventive maintenance, troubleshooting, and component replacement. Refer to the Display Unit Maintenance Manual if information concerning adjustment is required.

The Drawer Unit can either be pulled out to its extended position, or completely removed from the cabinet for servicing. It is held in place by a large slotted screw. This screw is located at the back of the Terminal, above the Drawer Unit. Once the screw is loosened, the Drawer Unit can be pulled out the front until the stop-latches engage, holding the drawer in the extended position.

WARNING

Dangerous potentials exist at several points in the Drawer Unit. Do not touch electrical connections or components while the unit is energized. Disconnect power before cleaning the unit or replacing parts.

To completely remove the drawer from the cabinet, disconnect the Drawer Unit power plug, the Display Unit power plug and interconnecting plug from the back of the Drawer Unit. After the drawer has been pulled out to its extended position, the latches in both side rails must be pushed in before pulling the drawer completely off the tracks.

While replacing the Drawer Unit, the power cables must be pulled through the cabinet opening. Then insert the drawer rails into the slide-out tracks. After the drawer has been partially inserted, the stop-latches must be pushed in to permit them to enter the slide-track assembly. They will again latch the drawer in the extended position. The latches must be pushed in again to fully insert the drawer.

PREVENTIVE MAINTENANCE

General

Preventive maintenance consists of cleaning, visual inspection, etc. Preventive maintenance performed on a regular basis may prevent instrument breakdown and will improve the reliability of this instrument. The severity of the environment to which it is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is preceding recalibration of the instrument.

Cleaning

Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-pressure air. Remove any dirt which remains with a soft-bristled brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces.

Visual Inspection

The unit should be inspected occasionally for such defects as broken connections, damaged or improperly installed circuit boards, and heat-damaged parts. Tightness of bolted-down electrical connectors in the Power Supply section should also be checked.

The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the unit. It is important that the cause of over-heating be corrected to prevent recurrence of the damage.

TROUBLESHOOTING

Introduction

Information contained in other sections of this manual should be used with the following information to aid in locating the defective component. An understanding of the circuit operation is very helpful in locating troubles, particularly where integrated circuits are used. See the Circuit Description section for complete information.

Troubleshooting Aids

Diagrams. Complete circuit diagrams are given on fold-out pages in the Diagrams Section. The component number and electrical value of each component in this unit are shown on the diagrams.

Circuit Boards. Some circuit board pictures are shown in the Diagrams Section. Each electrical component on the boards is identified by its circuit number. These pictures, used with the diagrams, aid in locating the components mounted on the circuit boards.

Semiconductor Lead Identification. A top view of the arrangement of leads for the semiconductors in the Drawer Unit is shown in the Diagrams Section in the back of this manual.

Troubleshooting Equipment

The following equipment is useful for troubleshooting the Drawer Unit:

1. Bypass circuit cards for TC-4, TC-5, and TC-8; Tektronix Part No. 670-1649-00, 670-1650-00, and 670-1441-00 respectively.

2. Circuit Card Extender, Tektronix Part No. 067-0615-00.

3. X, Y, Z Extender Cable for use with TC-9, TC-13, and TC-18; Tektronix Part No. 012-0334-00.

4. Dynamic Transistor Tester; Tektronix Type 576 Transistor Curve Tracer or equivalent.

5. Volt-Ohmmeter; 20,000 ohms/volt input impedance, 0 to 500 volt range, accurate to within 3%.

6. Test Oscilloscope; DC to above 5 MHz frequency response, 5 millivolts to 5 volts/division deflection factor. Use a 10X probe to prevent circuit loading.

COMPONENT REPLACEMENT

WARNING

Disconnect the Terminal from the power source before replacing components.

General

The information provided here should be used in conjunction with the exploded-view drawings in this manual when disassembling or assembling components.

Semiconductor Replacement

Replacement semiconductors should be of the original type or a direct replacement. All transistor sockets are wired for standard basing as used for metal-case transistors. If a replacement transistor is made by a different manufacturer than the original, check the manufacturer's basing diagram for correct basing.

The following semiconductors in the Power Supply section are insulated from the chassis by mica insulators: CR31, CR32, Q15, Q33, Q65, Q72, and Q85. The mica insulators have silicon grease applied to both sides to improve heat dissipation. In addition, silicon grease is applied between Q61 and its heat sink. Replacement components should receive a similar application of silicon grease prior to installation. Adequate safety precautions should be observed in the handling of the silicon grease.

WARNING

Silicon grease can cause severe eye irritation. Wash hands thoroughly after contact with it.

Two semiconductors on the TC-14 card (U37, U57) are equipped with clip-on heat sinks. The Drawer Unit should not be operated without these heat sinks in place.

Circuit Board Pins

A pin replacement kit (which includes necessary tools, instructions, and replacement pins) is available from Tektronix, Inc. Order Tektronix Part No. 040-0542-00.

To replace a pin which is mounted on a circuit board, first disconnect any pin connectors. Then, unsolder the damaged pin and pull it out of the circuit board with a pair of pliers. Be careful not to damage the wiring on the board with too much heat. Ream out the hole in the circuit board with a 0.031-inch drill. Then remove the ferrule from the new interconnecting pin and press the new pin into the hole in the circuit board. Position the pin in the same manner as the old pin. Then, solder the pin on both sides of the circuit board. If the old pin was bent at an angle to mate with a connector, bend the new pin to match the associated pins.

End-Lead Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To replace damaged end-lead pin connectors, remove the old pin connector from the end of the lead and clamp the replacement connector to the lead.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and re-installed as a multi-pin connector. To provide correct orientation of this multi-pin connector when it is replaced, an arrow is stamped on the circuit board or chassis and a matching arrow is molded into the plastic housing of the multi-pin connector. Be sure these arrows are aligned as the multi-pin connector is replaced. If the individual end-lead pin connectors are removed from the plastic holder, note the color of the individual wires for replacement.

Terminal Control Circuit Board Replacement

Entire circuit cards or boards, including all soldered-on components, can be replaced. Part numbers are given in the Mechanical Parts List.

Some of the circuit cards cannot be removed from energized equipment without causing damage. As a general rule, de-energizing of the Terminal is recommended prior to removing or replacing any boards or components.

The plug-in cards can be removed by pulling upward on the inner ends of both tabs attached to each card. When replacing cards, insure that the card is in its guide and properly started in its jack before applying pressure. Cards are keyed to avoid cross-insertion.

The Terminal Control assembly must be taken out of the Drawer Unit to remove the Terminal Control interconnector board. Take the four screws out of the bottom to release the assembly. Then disconnect the cables while removing the assembly out the top. Remove all of the circuit cards, and remove the screws which hold the individual connectors to the assembly frame. The interconnector board should then be free to lift away from the bottom of the frame.

Keyboard Assembly Information

Keyboard Assembly Removal. Release the Drawer Unit locking knob at the rear of the Terminal. Pull the Drawer Unit out until it latches. Remove two screws from the back of the flange on each side of the Keyboard. Hold the Keyboard in place until the screws are all removed. Then pull the Keyboard forward off of the Drawer Unit.

Keyboard Access. After the Keyboard assembly has been removed from the Drawer Unit, remove four screws from the bottom of the unit and lift the bottom off of the assembly.

Keyboard Removal. Remove four nuts from the plate on the underside and lift the Keyboard away from the assembly.

Key Cap Removal. Pull directly up on the cap. The caps are press fits and slide off of the top.

Key Assembly Removal. Remove the solder from the contacts on the bottom of the board, using a vacuum-type solder removing device. When all the solder is removed and the contacts are free, pull the key assembly up through the top. Remove the spacer sleeve (if any) from between the circuit board and the top plate.

ADJUSTMENTS

Terminal Control adjustments are listed here. Details regarding them are provided in the adjustment procedure which is contained in the Display Unit Maintenance Manual.

TC-1	BELL TONE R1
	BELL VOLUME R9
	KEYBOARD CLICK R5
TC-9	Y D/A GAIN R9
	Y D/A OFFSET R7
	SCRATCH PAD POSITION R97
TC-13	X D/A GAIN R9
	X D/A OFFSET R7
TC-15	CURSOR INTENSITY R48
TC-18	LINEAR INTERPOLATE BUSY TIME R70
	LINEAR INTERPOLATE Z INTENSITY R17 and R19

SECTION 4
ELECTRICAL PARTS LIST

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS				
C11	283-0003-00			0.01 µF, Cer, 150 V, +80%-20%
C14	290-0086-00			2000 µF, Elect., 30 V
C31	283-0003-00			0.01 µF, Cer, 150 V, +80%-20%
C32	290-0433-00			160,000 µF, Elect., 12 V, +75%-10%
C33	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C81	283-0003-00			0.01 µF, Cer, 150 V, +80%-20%
C83	290-0086-00			2000 µF, Elect., 30 V
SCD, DIODES				
CR31	152-0274-00			Silicon, replaceable by 1N1200
CR32	152-0274-00			Silicon, replaceable by 1N1200
FUSES				
F4	159-0023-00			2A, 3AG, Slo-blow
F8	159-0041-00			1.25A, 3AG, Slo-blow
F31	159-0045-00			20A, 3AG, Fast-blow
FILTER				
FL1	119-0207-00			Filter, 250VAC, 45 to 66 Hz, 10A
CONNECTORS				
J101	131-0408-00			Receptacle, electrical
J102	131-0569-00			Receptacle, electrical
J103	136-0156-01			Socket, 44 pin
J251	131-0569-00			Receptacle, electrical
P101	131-0422-00			Receptacle, electrical
P102	131-0570-00			Receptacle, electrical
LOUD SPEAKER				
LS108	119-0131-00			Loud Speaker
TRANSISTORS				
Q15	151-0148-00			Silicon, NPN, Tek Spec
Q33	151-0507-00			Silicon, controlled rectifier, 2N3669
Q72	151-0148-00			Silicon, NPN, Tek Spec
Q74	151-0275-00			Silicon, NPN, 2N3771
Q85	151-0148-00			Silicon, NPN, Tek Spec
RESISTORS				
R33	315-0102-00			1 kΩ, 1/4 W, 5%
R73	308-0179-00			5 Ω, 5 W, WW, 5%
R75	308-0575-00			0.06 Ω, 6 W, WW, 10%
R78	308-0205-00			2 Ω, 25 W, WW, 5%
R79	308-0205-00			2 Ω, 25 W, WW, 5%

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SWITCHES				
S4	260-1035-00			Sensitive, POWER OFF/CONTROL LOCK
S5, S8[1]	260-0157-00			Thermostatic, 160° F, ±5°
S101	260-1273-00			Rocker, DPDT, DIRECT/SCRATCH PAD
S103	260-1274-00			Rocker, SPDT, MARGIN SHIFT
S105	260-1273-00			Rocker, DPDT, TTY/ASC11
S107	260-1273-00			Rocker, DPDT, ON LINE/LOCAL
TRANSFORMER				
T1	120-0653-00			Power
ASSEMBLY A1	670-1435-00	B050500	B069999	**KEYBOARD LOGIC TC#1 Circuit Card**
A1	670-1435-01	B070000		**KEYBOARD LOGIC TC#1 Circuit Card**
CAPACITORS				
C6	290-0248-01			150 µF, Elect., 15 V, 20%
C20	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C33	283-0167-00			0.1 µF, Cer, 200 V, 10%
C39	283-0167-00			0.1 µF, Cer, 200 V, 10%
C41	283-0198-00			0.22 µF, Cer, 50 V, 20%
C48	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C51	283-0238-00			0.01 µF, Cer, 50 V, 10%
C60	283-0191-00			0.022 µF, Cer, 50 V, 20%
C62	283-0191-00			0.022 µF, Cer, 50 V, 20%
C66	283-0191-00			0.022 µF, Cer, 50 V, 20%
C68	283-0187-00	B050500	B090000	0.047 µF, Cer, 400 V, 10%
C68	283-0341-00	B100000		0.047 µF, Cer, 100 V, 10%
C96	290-0246-00			3.3 µF, Elect., 15 V, 10%
C101	290-0134-00			22 µF, Elect., 15 V, 20%
C126	283-0198-00			0.22 µF, Cer, 50 V, 20%
C131	283-0198-00			0.22 µF, Cer, 50 V, 20%
C136	283-0198-00			0.22 µF, Cer, 50 V, 20%
C138	283-0198-00			0.22 µF, Cer, 50 V, 20%
C143	283-0198-00			0.22 µF, Cer, 50 V, 20%
C158	283-0176-00			0.0022 µF, Cer, 50 V, 20%
C163	283-0198-00			0.22 µF, Cer, 50 V, 20%
C165	283-0602-00			53 pF, Mica, 300 V, 5%
C168	283-0602-00			53 pF, Mica, 300 V, 5%
C173	290-0246-00			3.3 µF, Elect., 15 V, 10%
C175	283-0167-00			0.1 µF, Cer, 200 V, 10%
C178	283-0602-00			53 pF, Cer, 300 V, 5%
C190	290-0301-00			10 µF, Elect., 20 V, 10%
C192	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C193	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C195	290-0301-00			10 µF, Elect., 20 V, 10%
SCD, DIODES				
CR155	152-0185-00			Silicon, replaceable by 1N4152
CR157	152-0185-00			Silicon, replaceable by 1N4152
CR167	152-0185-00			Silicon, replaceable by 1N4152
CR178	152-0185-00			Silicon, replaceable by 1N4152
VR24	152-0278-00			Zener, 1N4372A, 400 mW, 3 V, 5%
VR37	152-0278-00			Zener, 1N4372A, 400 mW, 3 V, 5%
VR48	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
VR55	152-0278-00			Zener, 1N4372A, 400 mW, 3 V, 5%

[1] See Mechanical Parts List, Line Voltage Selector Body.

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INDUCTORS				
L24	108-0245-00	XB100000		3.9 µH
L37	108-0245-00			3.9 µH
L55	108-0245-00	XB090000		3.9 µH
TRANSISTORS				
Q1	151-0190-00			Silicon, NPN, 2N3904
Q3	151-0504-00			Silicon, unijunction, 2N4851
Q9	151-0190-00			Silicon, NPN, 2N3904
Q11	151-0190-00			Silicon, NPN, 2N3904
Q13	151-0504-00			Silicon, unijunction, 2N4851
Q15	151-0190-00			Silicon, NPN, 2N3904
Q25	151-0190-00			Silicon, NPN, 2N3904
Q27	151-0188-00			Silicon, PNP, 2N3906
Q29	151-0190-00			Silicon, NPN, 2N3904
Q41	151-0188-00			Silicon, PNP, 2N3906
Q43	151-0190-00			Silicon, NPN, 2N3904
Q45	151-0504-00			Silicon, unijunction, 2N4851
Q47	151-0190-00			Silicon, NPN, 2N3904
Q49	151-0190-00			Silicon, NPN, 2N3904
Q51	151-0254-00			Silicon, NPN, 2N5308
Q53	151-0188-00			Silicon, PNP, 2N3906
Q63	151-0190-00			Silicon, NPN, 2N3904
Q71	151-0190-00			Silicon, NPN, 2N3904
Q73	151-0192-00			Silicon, NPN, replaceable by MPS6521
Q91	151-0504-00			Silicon, unijunction, 2N4851
Q93	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R1	311-1289-00			500 kΩ, Var
R2	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R2	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R3	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R3	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R5	311-1287-00			100 kΩ, Var
R6	317-0205-00	B050500	B089999	2 MΩ, 1/8 W, 5%
R6	315-0205-00	B090000		2 MΩ, 1/4 W, 5%
R7	317-0433-00	B050000	B089999	43 kΩ, 1/8 W, 5%
R7	315-0433-00	B090000		43 kΩ, 1/4 W, 5%
R9	311-1287-00			100 kΩ, Var
R10	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R10	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R11	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R11	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R12	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R12	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R13	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R13	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R15	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R15	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R16	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R16	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R18	315-0820-00			82 Ω, 1/4 W, 5%
R20	317-0514-00	B050500	B089999	510 kΩ, 1/8 W, 5%
R20	315-0514-00	B090000		510 kΩ, 1/4 W, 5%
R22	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R22	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R24	317-0101-00	B050500	B089999	100 Ω, 1/8 W, 5%
R24	315-0101-00	B090000	B099999X	100 Ω, 1/4 W, 5%
R28	317-0331-00	B050500	B089999	330 Ω, 1/8 W, 5%
R28	315-0331-00	B090000		330 Ω, 1/4 W, 5%
R29	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R29	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R30	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R30	315-0102-00	B090000		1 kΩ, 1/4 W, 5%
R31	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R31	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R33	317-0474-00	B050500	B089999	470 kΩ, 1/8 W, 5%
R33	315-0474-00	B090000		470 kΩ, 1/4 W, 5%
R35	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R35	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R39	317-0303-00	B050500	B089999	30 kΩ, 1/8 W, 5%
R39	315-0303-00	B090000		30 kΩ, 1/4 W, 5%
R42	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R42	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R43	317-0222-00	B050500	B089999	2.2 kΩ, 1/8 W, 5%
R43	315-0222-00	B090000		2.2 kΩ, 1/4 W, 5%
R45	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R45	315-0102-00	B090000		1 kΩ, 1/4 W, 5%
R48	315-0151-00			150 Ω, 1/4 W, 5%
R51	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R51	315-0473-00	B090000		47 kΩ, 1/8 W, 5%
R53	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R53	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R55	317-0101-00	B050500	B089999X	100 Ω, 1/8 W, 5%
R62	317-0123-00	B050500	B089999	12 kΩ, 1/8 W, 5%
R62	315-0123-00	B090000		12 kΩ, 1/4 W, 5%
R64	317-0123-00	B050500	B089999	12 kΩ, 1/8 W, 5%
R64	315-0123-00	B090000		12 kΩ, 1/4 W, 5%
R66	317-0152-00	B050500	B089999	1.5 kΩ, 1/8 W, 5%
R66	315-0152-00	B090000		1.5 kΩ, 1/4 W, 5%
R67	317-0103-00	B050500	B089999	10 kΩ, 1/8 W, 5%
R67	315-0103-00	B090000		10 kΩ, 1/4 W, 5%
R69	317-0153-00	B050500	B089999	15 kΩ, 1/8 W, 5%
R69	315-0153-00	B090000		15 kΩ, 1/4 W, 5%
R73	301-0510-00	B050500	B069999	51 Ω, 1/2 W, 5%
R73	302-0391-00	B070000		390 Ω, 1/2 W, 10%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R79	301-0510-00	B050500	B069999	51 Ω, 1/2 W, 5%
R79	302-0391-00	B070000		390 Ω, 1/2 W, 10%
R81	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R81	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R83	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R83	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R85	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R85	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R87	317-0331-00	B050500	B089999	330 Ω, 1/8 W, 5%
R87	315-0331-00	B090000		330 Ω, 1/4 W, 5%
R88	317-0331-00	B050500	B089999	330 Ω, 1/8 W, 5%
R88	315-0331-00	B090000		330 Ω, 1/4 W, 5%
R90	317-0682-00	B050500	B089999	6.8 kΩ, 1/8 W, 5%
R90	315-0682-00	B090000		6.8 kΩ, 1/4 W, 5%
R92	317-0182-00	B050500	B089999	1.8 kΩ, 1/8 W, 5%
R92	315-0182-00	B090000		1.8 kΩ, 1/4 W, 5%
R93	317-0432-00	B050500	B089999	4.3 kΩ, 1/8 W, 5%
R93	315-0432-00	B090000		4.3 kΩ, 1/4 W, 5%
R94	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R94	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R96	317-0154-00	B050500	B089999	150 kΩ, 1/8 W, 5%
R96	315-0154-00	B090000		150 kΩ, 1/4 W, 5%
R100	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R100	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R101	317-0101-00	B050500	B089999	100 Ω, 1/8 W, 5%
R101	315-0101-00	B090000		100 Ω, 1/4 W, 5%
R103	317-0103-00	B050500	B089999	10 kΩ, 1/8 W, 5%
R103	315-0103-00	B090000		10 kΩ, 1/4 W, 5%
R105	317-0222-00	B050500	B089999	2.2 kΩ, 1/8 W, 5%
R105	315-0222-00	B090000		2.2 kΩ, 1/4 W, 5%
R106	317-0332-00	B050500	B089999	3.3 kΩ, 1/8 W, 5%
R106	315-0332-00	B090000		3.3 kΩ, 1/4 W, 5%
R107	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R107	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R108	317-0221-00	B050500	B089999	220 Ω, 1/8 W, 5%
R108	315-0221-00	B090000		220 Ω, 1/4 W, 5%
R109	317-0221-00	B050500	B089999	220 Ω, 1/8 W, 5%
R109	315-0221-00	B090000		220 Ω, 1/4 W, 5%
R111	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R111	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R112	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R112	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R114	317-0122-00	B050500	B089999	1.2 kΩ, 1/8 W, 5%
R114	315-0122-00	B090000		1.2 kΩ, 1/4 W, 5%
R116	315-0820-00			82 Ω, 1/4 W, 5%
R117	315-0820-00			82 Ω, 1/4 W, 5%
R118	315-0820-00			82 Ω, 1/4 W,5%
R120	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R120	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R121	317-0273-00	B050500	B089999	27 kΩ, 1/8 W, 5%
R121	315-0273-00	B090000		27 kΩ, 1/4 W, 5%
R123	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R123	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R124	317-0273-00	B050500	B089999	27 kΩ, 1/8 W, 5%
R124	315-0273-00	B090000		27 kΩ, 1/4 W, 5%
R126	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R126	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R128	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R128	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R129	317-0273-00	B050500	B089999	27 kΩ, 1/8 W, 5%
R129	315-0273-00	B090000		27 kΩ, 1/4 W, 5%
R131	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R131	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R133	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R133	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R134	317-0273-00	B050500	B089999	27 kΩ, 1/8 W, 5%
R134	315-0273-00	B090000		27 kΩ, 1/4 W, 5%
R136	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R136	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R138	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R138	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R140	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R140	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R141	317-0273-00	B050500	B089999	27 kΩ, 1/8 W, 5%
R141	315-0273-00	B090000		27 kΩ, 1/4 W, 5%
R143	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R143	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R150	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R150	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R152	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R152	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R154	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R154	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R156	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R156	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
R158	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R158	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R159	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R159	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R161	317-0123-00	B050500	B089999	12 kΩ, 1/8 W, 5%
R161	315-0123-00	B090000		12 kΩ, 1/4 W, 5%
R163	317-0473-00	B050500	B089999	47 kΩ, 1/8 W, 5%
R163	315-0473-00	B090000		47 kΩ, 1/4 W, 5%
R165	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R165	317-0102-00	B090000		1 kΩ, 1/4 W, 5%
R166	317-0123-00	B050500	B089999	12 kΩ, 1/8 W, 5%
R166	315-0123-00	B090000		12 kΩ, 1/4 W, 5%

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R168	317-0223-00	B050500	B089999	22 kΩ, 1/8 W, 5%
R168	315-0223-00	B090000		22 kΩ, 1/4 W, 5%
R171	317-0123-00	B050500	B089999	1Ω kΩ, 1/8 W, 5%
R171	315-0123-00	B090000		12 kΩ, 1/4 W, 5%
R173	317-0104-00	B050500	B089999	100 kΩ, 1/8 W, 5%
R173	315-0104-00	B090000		100 kΩ, 1/4 W, 5%
R175	317-0474-00	B050500	B089999	470 kΩ, 1/8 W, 5%
R175	315-0474-00	B090000		470 kΩ, 1/4 W, 5%
R177	317-0471-00	B050500	B089999	470 Ω, 1/8 W, 5%
R177	315-0471-00	B090000		470 Ω, 1/4 W, 5%
R178	317-0101-00	B050500	B089999	100 Ω, 1/8 W, 5%
R178	315-0101-00	B090000		100 Ω, 1/4 W, 5%
R179	317-0123-00	B050500	B089999	12 kΩ, 1/8 W, 5%
R179	315-0123-00	B090000		12 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U5	156-0072-00			Monostable multi, replaceable by T.I. SN74121N
U7	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U9	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U19	155-0031-01			Quad timing logic
U23	156-0041-00			Dual D flip-flop, replaceable by T.I. SN7474N,
U29	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U39	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U51	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U57	155-0031-01			Quad timing logic
U59	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U81	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U83	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U85	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U87	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U95	156-0081-00			Retriggerable monostable multivibrator, replaceable by Fairchild 9601
ASSEMBLY				
A2	670-1436-00	B050500	B069999	**OUTPUT DATA SELECTOR TC#2 Circuit Card**
CAPACITORS				
C12	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C13	281-0510-00			22 pF, Cer, 500 V, 20%
C18	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C20	283-0187-00			0.047 μF, Cer, 400 V, 10%
C36	281-0510-00			22 pF, Cer, 500 V, 20%
C52	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C53	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C54	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C55	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C56	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C57	283-0177-00			1 μF, Cer, 25 V, +80%-20%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SCD, DIODE				
CR20	152-0185-00			Silicon, replaceable by 1N4152
INDUCTORS				
L13	108-0395-00			64 µH
L50	108-0551-00			14 µH
L52	108-0551-00			14 µH
L54	108-0551-00			14 µH
L56	108-0551-00			14 µH
L58	108-0551-00			14 µH
L60	108-0551-00			14 µH
L62	108-0551-00			14 µH
L64	108-0551-00			14 µH
L66	108-0551-00			14 µH
L68	108-0551-00			14 µH
L70	108-0551-00			14 µH
TRANSISTOR				
Q7	151-0223-00			Silicon, NPN, 2N4275
RESISTORS				
R10	317-0102-00			1 kΩ, 1/8 W, 5%
R11	317-0202-00			2 kΩ, 1/8 W, 5%
R13	317-0431-00			430 Ω, 1/8 W, 5%
R15	317-0621-00			620 Ω, 1/8 W, 5%
R16	317-0182-00			1.8 kΩ, 1/8 W, 5%
R17	317-0102-00			1 kΩ, 1/8 W, 5%
R18	317-0682-00			6.8 kΩ, 1/8 W, 5%
R20	317-0222-00			2.2 kΩ, 1/8 W, 5%
R22	317-0222-00			2.2 kΩ, 1/8 W, 5%
R30	317-0472-00			4.7 kΩ, 1/8 W, 5%
R34	317-0472-00			4.7 kΩ, 1/8 W, 5%
R40	317-0472-00			4.7 kΩ, 1/8 W, 5%
R52	317-0102-00			1 kΩ, 1/8 W, 5%
R53	317-0102-00			1 kΩ, 1/8 W, 5%
R54	317-0102-00			1 kΩ, 1/8 W, 5%
INTEGRATED CIRCUITS				
U1	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U5	156-0033-00			Linear, RF/IF ampl, replaceable by RCA CA3028A
U7	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U9	156-0047-00			Tripple 3-input gate, replaceable by T.I. SN7410N
U11	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U13	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U15	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U23	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U25	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U27	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U29	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U31	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U33	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U35	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U37	156-0156-00			Dual 4-input pos nand buffer, replaceable by T.I. SN74H70N
U43	156-0047-00			Tripple 3-input gate, replaceable by T.I. SN7410N
U45	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U47	156-0047-00			Tripple 3-input gate, replaceable by T.I. SN7410N
U49	156-0047-00			Tripple 3-input gate, replaceable by T.I. SN7410N
U51	156-0036-00			Dual 4-input buffer, replaceable by T.I. SN7440N
U53	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U55	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
CRYSTAL				
Y7	158-0056-00			4 MHz
ASSEMBLY				
A2	670-1436-01	B070000	B099999	**OUTPUT DATA SELECTOR TC#2 Circuit Card**
A2	670-1436-02	B100000		**OUTPUT DATA SELECTOR TC#2 Circuit Card**
CAPACITORS				
C1	281-0546-00			330 pF, Cer, 500 V, 10%
C3	283-0602-00			53 pF, Mica, 300 V, 5%
C5	283-0602-00			53 pF, Mica, 300 V, 5%
C30	290-0530-00			68 µF, Elect., 6 V, 20%
C31	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C32	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C33	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C34	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C37	290-0530-00			68 µF, Elect., 6 V, 20%
C38	283-0177-00			1 µF, Cer, 25 V, +80%-20%
INDUCTORS				
L30	108-0395-00			64 µH
134	108-0395-00			64 µH
L37	108-0395-00			64 µH
L50	108-0551-00			14 µH
L51	108-0551-00			14 µH
L54	108-0551-00			14 µH
L56	108-0551-00			14 µH
L58	108-0551-00			14 µH
L60	108-0551-00			14 µH
L62	108-0551-00			14 µH
L64	108-0551-00			14 µH
L66	108-0551-00			14 µH
L68	108-0551-00			14 µH
L70	108-0551-00			14 µH
RESISTORS				
R1	315-0681-00			680 Ω, 1/4 W, 5%
R3	321-0147-00			332 Ω, 1/8 W, 1%
R5	321-0147-00			332 Ω, 1/8 W, 1%
R7	315-0681-00			680 Ω, 1/4 W, 5%
R10	321-0097-00			100 Ω, 1/8 W, 1%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R25	315-0472-00			4.7 kΩ, 1/4 W, 5%
R30	315-0472-00	XB100000		4.7 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS				
U5	156-0129-00			Dual 2-input gate, replaceable by T.I. SN7408N
U7	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U11	156-0047-00			Tripple 3-input gate, replaceable by T.I.SN7410N
U13	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U15	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U19	156-0156-00			Dual 4-input positive nand buffer, replaceable by T.I. SN74H40N
U21	156-0098-00			Dual 4-line to 1-line data selector w/strobe replaceable by T.I. SN74153N
U23	156-0098-00			Dual 4-line to 1-line data selector w/strobe replaceable by T.I. SN74153N
U27	156-0098-00			Dual 4-line to 1-line data selector w/strobe replaceable by T.I. SN74153N
U29	156-0098-00			Dual 4-line to 1-line data selector w/strobe replaceable by T.I. SN74153N
U31	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U35	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U37	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U39	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
CRYSTAL				
Y10	158-0056-00			4 MHz
A3	670-1649-00			**SCRATCH PAD BYPASS TC#4 (optional)**
A3	670-1437-00	B050500	B089999	**SCRATCH PAD CONTROL TC#4 Circuit C[illegible]d**
A3	670-1437-01	B090000		**SCRATCH PAD CONTROL**
CAPACITORS				
C1	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C3	285-0835-00			0.22 µF, PTM, 100 V, 2%
C14	283-0065-00			0.001 µF, Cer, 100 V, 5%
C25	283-0065-00			0.001 µF, Cer, 100 V, 5%
C30	283-0177-00			1 µF, Cer, 35 V, +80%-20%
C31	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C32	283-0177-00			1 µF, Cer, 25 V, +80%-20%
SCD, DIODE				
CR22	152-0185-00			Silicon, replaceable by 1N4152
TRANSISTOR				
Q5	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R1	315-0472-00			4.7 kΩ, 1/4 W, 5%
R3	315-0302-00			3 kΩ, 1/4 W, 5%
R8	315-0472-00			4.7 kΩ, 1/4 W, 5%
R10	315-0201-00			200 Ω, 1/4 W, 5%
R11	315-0472-00			4.7 kΩ, 1/4 W, 5%
R12	321-0306-00			15 kΩ, 1/8 W, 1%
R14	317-0201-00	B050500	B089999	200 Ω, 1/8 W, 5%
R14	315-0201-00	B090000		200 Ω, 1/4 W, 5%
R20	315-0102-00			1 kΩ, 1/4 W, 5%
R22	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R22	315-0102-00	B090000		1 kΩ, 1/4 W, 5%
R24	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R24	315-0102-00	B090000		1 kΩ, 1/4 W, 5%
R25	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R25	315-0202-00	B090000		2 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS				
U1	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U2	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U5	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U7	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U9	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U11	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U13	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U14	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U15	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U17	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U18	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U19	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U21	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U23	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U25	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U27	156-0041-00			Dual D flip-flop, replaceable by T.I. SN7474N
U29	156-0036-00			Dual 4-input buffer, replaceable by T.I. SN7440N
U31	156-0081-00			Retriggerable monostable multivibrator, replaceable by Fairchild 9601
U33	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U35	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U37	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U38	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U39	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U41	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U43	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U45	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U47	156-0041-00			Dual D flip-flop, replaceable by T.I. SN7474N
U49	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U51	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U53	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U55	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U57	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U58	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U59	156-0058-00			Hex. invert, replaceable by T.I. SN7404N

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY				
A4	670-1650-00			**SCRATCH PAD BYPASS TC#5 (optional)**
A4	670-1438-00	B050500	B079999	**SCRATCH PAD COUNTER TC#5 Circuit Card**
A4	670-1438-01	B080000		**SCRATCH PAD COUNTER TC#5 Circuit Card**
CAPACITORS				
C2	281-0580-00			470 pF, Cer, 500 V, 10%
C4	281-0580-00			470 pF, Cer, 500 V, 10%
C10	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C11	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C12	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C13	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C14	283-0177-00			1 µF, Cer, 25 V, +80%-20%
RESISTORS				
R5	315-0472-00			4.7 kΩ, 1/4 W, 5%
R7	315-0472-00			4.7 kΩ, 1/4 W, 5%
R10	315-0472-00			4.7 kΩ, 1/4 W, 5%
R12	315-0472-00	XB080000		4.7 kΩ, 1/4 W, 5%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R25	315-0102-00			1 kΩ, 1/4 W, 5%
R30	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U3	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U5	156-0123-00			4-bit magnitude comparator, replaceable by T.I. SN7485
U7	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U9	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U13	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U15	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U17	156-0155-00			Dual D-type edge trig flip-flop, replaceable by T.I. SN74H74N
U19	156-0131-00	XB080000		Single 25 MHz 8-bit ser. in/par. out shift reg., replaceable by T.I. SN74164N
U21	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U23	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U25	156-0123-00			4-bit magnitude comparator, replaceable by T.I. SN7485N
U27	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U29	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U31	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U33	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U35	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U37	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U41	156-0092-00			Hex. inverter w/open collector, replaceable by T.I. SN7405N
U43	156-0092-00			Hex. inverter w/open collector, replaceable by T.I. SN7405N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U45	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U47	156-0043-00			Quad,2-input NOR gate, replaceable by T.I. SN7402N
U49	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U51	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U53	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U55	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U57	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U59	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
ASSEMBLY				
A5	670-1439-00			**HORIZONTAL TAB TC#6 Circuit Card (optional)**
CAPACITORS				
C3	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C18	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C50	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C51	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C54	290-0267-00			1 µF, Elect., 35 V
SCD, DIODE				
VR16	152-0306-00			Zener, 1N960B, 400 mW, 9.1 V, 5%
RESISTORS				
R3	315-0512-00			5.1 kΩ, 1/4 W, 5%
R13	315-0202-00			2 kΩ, 1/4 W, 5%
R14	315-0202-00			2 kΩ, 1/4 W, 5%
R16	301-0131-00			130 Ω, 1/2 W, 5%
R20	315-0202-00			2 kΩ, 1/4 W, 5%
R22	315-0202-00			2 kΩ, 1/4 W, 5%
R24	315-0202-00			2 kΩ, 1/4 W, 5%
R26	315-0202-00			2 kΩ, 1/4 W, 5%
R30	315-0202-00			2 kΩ, 1/4 W, 5%
R32	315-0202-00			2 kΩ, 1/4 W, 5%
R34	315-0202-00			2 kΩ, 1/4 W, 5%
R36	315-0202-00			2 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U3	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U5	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U7	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U9	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U11	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U13	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U27	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U29	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U31	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U33	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U35	156-0135-00			Random access mem, replaceable by Intel 1601
U37	156-0081-00			BDC to decimal decoder/drive, replaceable by SN7441AN
U47	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U49	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U51	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U53	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U55	156-0117-00			4-bit binary counter presettable asychronous clear, replaceable by T.I. SN74161N
U57	156-0117-00			4-bit binary counter presettable asychronous clear, replaceable by T.I. SN74161N
ASSEMBLY A6	670-1440-00			**CONTROL FUNCTION DECODER TC#7 Circuit Card**
CAPACITORS				
C22	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C32	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C42	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C60	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C61	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C62	283-0177-00			1 µF, Cer, 25 V, +80%-20%
SCD, DIODES				
CR22	152-0185-00			Silicon, replaceable by 1N4152
CR32	152-0185-00			Silicon, replaceable by 1N4152
CR42	152-0185-00			Silicon, replaceable by 1N4152
TRANSISTORS				
Q35	151-0190-00			Silicon, NPN, 2N3904
Q37	151-0190-00			Silicon, NPN, 2N3904
Q41	151-0190-00			Silicon, NPN, 2N3904
Q59	151-0190-00			Silicon, NPN, 2N3904
Q75	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R2	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R2	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R4	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R4	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R6	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R6	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R8	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R8	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R10	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R10	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R12	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R12	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R14	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R14	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R16	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R16	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R17	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R17	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R18	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R18	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R22	315-0473-00			47 kΩ, 1/4 W, 5%
R23	315-0123-00			12 kΩ, 1/4 W, 5%
R30	315-0472-00			4.7 kΩ, 1/4 W, 5%
R32	315-0473-00			47 kΩ, 1/4 W, 5%
R33	315-0123-00			12 kΩ, 1/4 W, 5%
R42	315-0473-00			47 kΩ, 1/4 W, 5%
R43	315-0123-00			12 kΩ, 1/4 W, 5%
R50	315-0103-00			10 kΩ, 1/4 W, 5%
R54	317-0102-00	B050500	B089999	1 kΩ, 1/8 W, 5%
R54	315-0102-00	B090000		1 kΩ, 1/4 W, 5%
R56	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R56	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R60	315-0102-00			1 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U3	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U7	156-0078-00			4 to 16 line decoder, replaceable by T.I. SN7415N
U9	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U11	156-0078-00			4 to 16 line decoder, replaceable by T.I. SN7415N
U13	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U15	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U17	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U19	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U39	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
ASSEMBLY A7	670-1576-00			**CHARACTER ROTATOR BYPASS TC#8**
	670-1441-00			**CHARACTER ROTATOR TC#8 Circuit Card (optional)**
CAPACITORS				
C20	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C22	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C24	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C26	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C28	282-0177-00			1 μF, Cer, 25 V, +80%-20%
INTEGRATED CIRCUITS				
U3	156-0037-00			Dual 2 wide 2-input and-or-invert gate, replaceable by T.I. SN7451N
U5	156-0031-00			4-wide 2-input, and-or-invert gate, replaceable by T.I. SN7454N
U7	156-0031-00			4 wide 2-input, and-or-invert gate, replaceable by T.I. SN7454N
U9	156-0031-00			4 wide 2-input, and-or-invert gtae, replaceable by T.I. SN7454N
U11	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U13	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U15	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U23	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U25	156-0031-00			4 wide 2-input, and-or-invert gate, replaceable by T.I. SN745N
U27	156-0031-00			4 wide 2-input, and-or-invert gate, replaceable by T.I. SN745N
U29	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U31	156-0031-00			4-wide 2-input, and-or-invert gate, replaceable by T.I. SN7454N
U33	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U35	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
ASSEMBLY A8	670-1442-00			**Y D/A TC#9 Circuit Card**
CAPACITORS				
C52	285-0684-00			0.056 µF, Plastic, 100 V, 5%
C69	285-0753-03			0.01 µF, PTM, 100 V, 3 1/2%
C72	285-0753-03			0.01 µF, PTM, 100 V, 3 1/2%
C130	290-0323-00			270 µF, Elect., 15 V, 20%
C132	290-0286-00			50 µF, Elect., 25 V, +75%-10%
C134	290-0323-00			270 µF, Elect., 15 V, 20%
SCD, DIODES				
CR1	152-0185-00			Silicon, replaceable by 1N4152
CR3	152-0185-00			Silicon, replaceable by 1N4152
CR5	152-0185-00			Silicon, replaceable by 1N4152
CR7	152-0185-00			Silicon, replaceable by 1N4152
CR9	152-0185-00			Silicon, replaceable by 1N4152
CR11	152-0185-00			Silicon, replaceable by 1N4152
CR13	152-0185-00			Silicon, replaceable by 1N4152
CR15	152-0185-00			Silicon, replaceable by 1N4152
CR17	152-0185-00			Silicon, replaceable by 1N4152
CR19	152-0185-00			Silicon, replaceable by 1N4152
CR62	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR67	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR84	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR88	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR100	152-0185-00			Silicon, replaceable by 1N4152
CR103	152-0185-00			Silicon, replaceable by 1N4152
CR106	152-0185-00			Silicon, replaceable by 1N4152
CR109	152-0185-00			Silicon, replaceable by 1N4152
CR112	152-0185-00			Silicon, replaceable by 1N4152
CR115	152-0185-00			Silicon, replaceable by 1N4152
CR118	152-0185-00			Silicon, replaceable by 1N4152
VR52	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
VR53	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
CONNECTOR				
J151	131-1154-00			Link term.
INDUCTORS				
L130	108-0395-00			64 µH
L132	108-0395-00			64 µH
L134	108-0395-00			64 µH

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
TRANSISTORS				
Q15	151-0188-00			Silicon, PNP, 2N3906
Q17	151-1025-00			Silicon, FET, N channel, junction type
Q19	151-0216-00			Silicon, PNP, replaceable by MOT MPS6523
Q37	151-1021-00			Silicon, FET, N channel, junction type
Q39	151-0188-00			Silicon, PNP, 2N3906
Q57	151-0188-00			Silicon, PNP, 2N3906
Q69	151-0190-00			Silicon, NPN, 2N3904
Q77	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R1	315-0205-00			2 MΩ, 1/4 W, 5%
R3	315-0123-00			12 kΩ, 1/4 W, 5%
R4	322-0684-09			1.024 MΩ, 1/4 W, 1%
R5	322-0683-09			512 kΩ, 1/4 W, 1%
R6	315-0512-00			5.1 kΩ, 1/4 W, 5%
R7	311-1168-00			500 Ω, Var
R8	315-0222-00			2.2 kΩ, 1/4 W, 5%
R9	311-1167-00			200 Ω, Var
R10	322-0682-06			256 kΩ, 1/4 W, 1/4%
R12	315-0432-00			4.3 kΩ, 1/4 W, 5%
R14	321-0190-00			931 Ω, 1/8 W, 1%
R15	308-0663-00			128 kΩ, 1/8 W, WW
R17	321-0152-00			374 Ω, 1/8 W, 1%
R18	308-0662-00			64 kΩ, 1/8 W, WW
R20	321-0111-00			140 Ω, 1/8 W, 1%
R21	308-0661-00			32 kΩ, 1/8 W, WW
R23	321-0065-00			46.4 Ω, 1/8 W, 1%
R24	308-0660-00			16 kΩ, 1/8 W, WW
R26	321-0007-00			11.5 Ω, 1/8 W, 1%
R27	308-0659-00			8 kΩ, 1/8 W, WW
R28	308-0658-00			4 kΩ, 1/8 W, WW
R29	321-0204-00			1.3 kΩ, 1/8 W, 1%
R31	321-0126-00			200 Ω, 1/8 W, 1%
R33	321-0177-00			681 Ω, 1/8 W, 1%
R35	321-0356-00			49.9 kΩ, 1/8 W, 1%
R37	321-0264-00			5.49 kΩ, 1/8 W, 1%
R39	321-0356-00			49.9 kΩ, 1/8 W, 1%
R40	321-0356-00			49.9 kΩ, 1/8 W, 1%
R42	321-0208-00			1.43 kΩ, 1/8 W, 1%
R44	321-0240-00			3.09 kΩ, 1/8 W, 1%
R46	321-0356-00			49.9 kΩ, 1/8 W, 1%
R50	321-0385-00			100 kΩ, 1/8 W, 1%
R52	321-0126-00			200 Ω, 1/8 W, 1%
R53	321-0606-00			203 kΩ, 1/8 W, 1/4%
R60	315-0471-00			470 Ω, 1/4 W, 5%
R62	315-0103-00			10 kΩ, 1/4 W, 5%
R63	315-0474-00			470 kΩ, 1/4 W, 5%
R65	315-0471-00			470 Ω, 1/4 W, 5%
R67	315-0103-00			10 kΩ, 1/4 W, 5%
R68	315-0107-00			100 MΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R70	321-0755-03			65 kΩ, 1/8 W, 1/4%
R71	321-0746-02			162.6 kΩ, 1/8 W, 1/2%
R72	321-0755-03			65 kΩ, 1/8 W, 1/4%
R73	321-0279-00			7.87 kΩ, 1/8 W, 1%
R74	321-0289-00			10 kΩ, 1/8 W, 1%
R76	321-0362-00			57.6 kΩ, 1/8 W, 1%
R79	315-0102-00			1 kΩ, 1/4 W, 5%
R81	315-0511-00			510 Ω, 1/4 W, 5%
R82	315-0302-00			3 kΩ, 1/4 W, 5%
R84	321-0447-00			442 kΩ, 1/8 W, 1%
R85	321-0419-00			226 kΩ, 1/8 W, 1%
R87	315-0302-00			3 kΩ, 1/4 W, 5%
R88	321-0329-00			26.1 kΩ, 1/8 W, 1%
R90	315-0472-00			4.7 kΩ, 1/4 W, 5%
R92	321-0289-00			10 kΩ, 1/8 W, 1%
R93	321-0235-00			2.74 kΩ, 1/8 W, 1%
R94	321-0253-00			4.22 kΩ, 1/8 W, 1%
R96	315-0472-00			4.7 kΩ, 1/4 W, 5%
R97	311-0633-00			5 kΩ, Var
R100	315-0472-00			4.7 kΩ, 1/4 W, 5%
R101	321-0452-00			499 kΩ, 1/8 W, 1%
R103	315-0472-00			4.7 kΩ, 1/4 W, 5%
R104	322-0481-00			1 MΩ, 1/4 W, 1%
R106	315-0472-00			4.7 kΩ, 1/4 W, 5%
R107	321-0353-00			46.4 kΩ, 1/8 W, 1%
R109	315-0472-00			4.7 kΩ, 1/4 W, 5%
R110	321-0318-00			20 kΩ, 1/8 W, 1%
R112	315-0472-00			4.7 kΩ, 1/4 W, 5%
R113	321-0347-00			40.2 kΩ, 1/8 W, 1%
R115	315-0472-00			4.7 kΩ, 1/4 W, 5%
R116	321-0376-00			80.6 kΩ, 1/8 W, 1%
R118	315-0472-00			4.7 kΩ, 1/4 W, 5%
R119	321-0405-00			162 kΩ, 1/8 W, 1%
SWITCH				
S99	260-0960-00			Slide
INTEGRATED CIRCUITS				
U3	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U23	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U35	156-0060-00			Volt. follower, replaceable by NSLM302H
U43	156-0106-00			Diode array (6 matched), replaceable by RCA CA3039
U45	156-0106-00			Diode array (6 matched), replaceable by RCA CA3039
U55	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U71	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U83	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U85	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U87	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U93	156-0057-00			Quad 2-input NAND gate w/open coll, replaceable by T.I. SN7401N
U95	156-0057-00			Quad 2-input NAND gate w/open coll, replaceable by T.I. SN7401N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY				
A9	670-1443-00	B050500	B079999	**Y DATA REGISTER TC#10 Circuit Card**
A9	670-1443-01	B080000	B089999	**Y DATA REGISTER TC#10 Circuit Card**
A9	670-1443-02	B090000		**Y DATA REGISTER TC#10 Circuit Card**
CAPACITORS				
C50	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C51	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C52	283-0177-00			1 µF, Cer, 25 V, +80%-20%
RESISTORS				
R10	315-0102-00			1 kΩ, 1/4 W, 5%
R15	315-0472-00			4.7 kΩ, 1/4 W, 5%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R30	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U3	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U5	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U7	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U9	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U11	156-0038 00			J-K flip-flop, replaceable by T.I. SN7472N
U13	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U15	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U17	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U19	156-0036-00			Dual 4-input buffer, replaceable by T.I. SN7440N
U21	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U23	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U24	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U25	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N,
U27	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U29	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U31	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U33	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U35	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U37	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U39	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U41	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U43	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U45	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U47	156-0030 00			Quad 2-input gate, replaceable by T.I. SN7400N
U49	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U51	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U53	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U55	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U57	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U59	156-0035-00			8-input gate, replaceable by T.I. SN7430N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY				
A10	670-1444-00	B050500	B079999	**IN/OUT DATA ROUTING TC#11 Circuit Card**
A10	670-1444-01	B080000	B089999	**IN/OUT DATA ROUTING TC#11 Circuit Card**
A10	670-1444-02	B090000		**IN/OUT DATA ROUTING TC#11 Circuit Card**
CAPACITORS				
C10	283-0239-00			0.022 µF, Cer, 50 V, 10%
C21	283-0000-00			0.001 µF, Cer, 500 V, +100%-0%
C30	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C31	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C32	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C33	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C34	283-0177-00			1 µF, Cer, 25 V, +80%-20%
RESISTORS				
R1	315-0472-00			4.7 kΩ, 1/4 W, 5%
R3	315-0472-00			4.7 kΩ, 1/4 W, 5%
R5	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R5	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R7	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R7	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R10	315-0562-00			5.6 kΩ, 1/4 W, 5%
R13	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R13	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R15	315-0472-00			4.7 kΩ, 1/4 W, 5%
R20	317-0202-00	XB080000	B089999X	2 kΩ, 1/8 W, 5%
R21	317-0102-00	XB080000	B089999X	1 kΩ, 1/8 W, 5%
R31	315-0102-00			1 kΩ, 1/4 W, 5%
R32	315-0102-00			1 kΩ, 1/4 W, 5%
R33	315-0102-00			1 kΩ, 1/4 W, 5%
R34	315-0102-00			1 kΩ, 1/4 W, 5%
R35	315-0102-00			1 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U3	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U5	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U7	156-0110-00			Dual 2-line to 4-line decoders/demultiplexers replaceable by T.I. SN74155N
U11	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U13	156-0030-00			Quad 2-input gate, repalceable by T.I. SN7400N
U15	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U17	156-0039-00	XB090000		Dual J-K flip-flop, replaceable by T.I. SN7473N
U23	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U25	156-0150-00			Quad 2-input pos logic NAND buffer, replaceable by T.I. SN7437N
U27	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U29	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U31	156-0072-00			Monostable multi, replaceable by T.I. SN74121N
U33	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U35	156-0150-00			Quad 2-input pos. logic NAND buffer, replaceable by T.I. SN7437N
U37	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U43	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U45	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U47	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U51	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U53	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U55	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
ASSEMBLY				
A11	670-1445-00	B050500	B079999	**X DATA REGISTER TC#12 Circuit Card**
A11	670-1445-01	B080000		**X DATA REGISTER TC#12 Circuit Card**
CAPACITORS				
C36	283-0220-00	B050500	B079999X	0.01 µF, Cer, 50 V, 20%
C60	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C62	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C64	283-0177-00			1 µF, Cer, 25 V, +80%-20%
RESISTORS				
R3	315-0472-00			4.7 kΩ, 1/4 W, 5%
R5	315-0472-00			4.7 kΩ, 1/4 W, 5%
R10	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R10	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R11	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R11	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R12	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R12	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R13	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R13	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R22	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R22	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R23	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R23	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R24	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R24	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R25	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R25	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R32	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R32	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R35	315-0472-00			4.7 kΩ, 1/4 W, 5%
R36	315-0201-00	B050500	B079999X	200 Ω, 1/4 W, 5%
R38	315-0472-00			4.7 kΩ, 1/4 W, 5%
R42	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R42	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R60	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U3	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U5	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U7	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U9	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U11	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U13	156-0114-00			Divide by twelve counter, replaceable by T.I. SN7492N
U15	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U16	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U17	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U19	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U21	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U23	156-0089-00			Synchronous 4-bit up-down counter, replaceable by T.I. SN74193N
U27	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U29	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U31	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U33	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U35	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U37	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U39	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U41	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U43	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U47	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U49	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U51	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U53	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U55	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U57	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U59	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
ASSEMBLY A12	670-1446-00			**X D/A TC#13 Circuit Card**
CAPACITORS				
C52	285-0684-00			0.056 µF, Plastic, 100 V, 5%
C69	285-0753-03			0.01 µF, PTM, 100 V, 3 1/2%
C72	285-0753-03			0.01 µF, PTM, 100 V, 3 1/2%
C130	290-0323-00			270 µF, Elect., 15 V, 20%
C132	290-0286-00			50 µF, Elect., 25 V, +75%-10%
C134	290-0323-00			270 µF, Elect., 15 V, 20%
SCD, DIODES				
CR1	152-0185-00			Silicon, replaceable by 1N4152
CR3	152-0185-00			Silicon, replaceable by 1N4152
CR5	152-0185-00			Silicon, replaceable by 1N4152
CR7	152-0185-00			Silicon, replaceable by 1N4152
CR9	152-0185-00			Silicon, replaceable by 1N4152
CR11	152-0185-00			Silicon, replaceable by 1N4152
CR13	152-0185-00			Silicon, replaceable by 1N4152
CR15	152-0185-00			Silicon, replaceable by 1N4152
CR17	152-0185-00			Silicon, replaceable by 1N4152
CR19	152-0185-00			Silicon, replaceable by 1N4152

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SCD, DIODES (cont)				
CR62	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR67	152-0246-00			Silicon, low leakage, 250 mW, 40 V
CR87	152-0185-00			Silicon, replaceable by 1N4152
CR100	152-0185-00			Silicon, replaceable by 1N4152
CR103	152-0185-00			Silicon, replaceable by 1N4152
CR106	152-0185-00			Silicon, replaceable by 1N4152
CR109	152-0185-00			Silicon, replaceable by 1N4152
CR112	152-0185-00			Silicon, replaceable by 1N4152
CR115	152-0185-00			Silicon, replaceable by 1N4152
CR118	152-0185-00			Silicon, replaceable by 1N4152
CR121	152-0185-00			Silicon, replaceable by 1N4152
CR124	152-0185-00			Silicon, replaceable by 1N4152
CR127	152-0185-00			Silicon, replaceable by 1N4152
CR130	152-0185-00			Silicon, replaceable by 1N4152
VR52	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
VR53	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
INDUCTORS				
L130	108-0395-00			64 μH
L132	108-0395-00			64 μH
L134	108-0395-00			64 μH
TRANSISTORS				
Q13	151-0188-00			Silicon, PNP, 2N3906
Q29	151-1025-00			Silicon, FET, N channel, junction type
Q31	151-0190-00			Silicon, NPN, 2N3904
Q47	151-0190-00			Silicon, NPN, 2N3904
Q49	151-0216-00			Silicon, PNP, replaceable by MOT MPS 6523
Q53	151-0190-00			Silicon, NPN, 2N3904
Q57	151-0188-00			Silicon, PNP, 2N3906
Q59	151-1021-00			Silicon, FET, N channel, junction type
RESISTORS				
R1	315-0205-00			2 MΩ, 1/4 W, 5%
R3	315-0123-00			12 kΩ, 1/4 W, 5%
R4	322-0684-09			1.024 MΩ, 1/4 W, 1%
R5	322-0683-09			512 kΩ, 1/4 W, 1%
R6	315-0512-00			5.1 kΩ, 1/4 W, 5%
R7	311-1168-00			500 Ω, Var
R8	315-0222-00			2.2 kΩ, 1/4 W, 5%
R9	311-1167-00			200 Ω, Var
R10	322-0682-06			256 kΩ, 1/4 W, 1 /4%
R12	315-0432-00			4.3 kΩ, 1/4 W, 5%
R14	321-0190-00			931 Ω, 1/8 W, 1%
R15	308-0663-00			128 kΩ, 1/8 W, WW
R17	321-0152-00			374 Ω, 1/8 W, 1%
R18	308-0662-00			64 kΩ, 1/8 W, WW
R20	321-0111-00			140 Ω, 1/8 W, 1%
R21	308-0661-00			32 kΩ, 1/8 W, WW
R23	321-0065-00			464 Ω, 1/8 W, 1%
R24	308-0660-00			16 kΩ, 1/8 W, WW
R26	321-0007-00			11.5 Ω, 1/8 W, 1%
R27	308-0659-00			8 kΩ, 1/8 W, WW

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R28	308-0658-00			4 kΩ, 1/8 W, WW
R29	321-0204-00			1.3 kΩ, 1/8 W, 1%
R31	321-0126-00			200 Ω, 1/8 W, 1%
R33	321-0177-00			681 Ω, 1/8 W, 1%
R35	321-0356-00			49.9 kΩ, 1/8 W, 1%
R37	321-0264-00			5.49 kΩ, 1/8 W, 1%
R39	321-0356-00			49.9 kΩ, 1/8 W, 1%
R40	321-0356-00			49.9 kΩ, 1/8 W, 1%
R42	321-0208-00			1.43 kΩ, 1/8 W, 1%
R44	321-0240-00			3.09 kΩ, 1/8 W, 1%
R46	321-0356-00			49.9 kΩ, 1/8 W, 1%
R50	321-0385-00			100 kΩ, 1/8 W, 1%
R52	321-0126-00			200 Ω, 1/8 W, 1%
R53	321-0606-00			203 kΩ, 1/8 W, 1/4%
R60	315-0471-00			470 Ω, 1/4 W, 5%
R62	315-0103-00			10 kΩ, 1/4 W, 5%
R63	315-0474-00			470 kΩ, 1/4 W, 5%
R65	315-0471-00			470 Ω, 1/4 W, 5%
R67	315-0103-00			10 kΩ, 1/4 W, 5%
R68	315-0107-00			100 MΩ, 1/4 W, 5%
R70	321-0755-03			65 kΩ, 1/8 W, 1/4%
R71	321-0746-02			162.6 kΩ, 1/8 W, 1/2%
R72	321-0755-03			65 kΩ, 1/8 W, 1/4%
R73	321-0279-00			7.87 kΩ, 1/8 W, 1%
R74	321-0279-00			7.87 kΩ, 1/8 W, 1%
R76	323-0463-00			649 kΩ, 1/2 W, 1%
R77	323-0478-00			931 kΩ, 1/2 W, 1%
R79	321-0279-00			7.87 kΩ, 1/8 W, 1%
R81	315-0472-00			4.7 kΩ, 1/4 W, 5%
R82	322-0620-00			800 kΩ, 1/4 W, 1%
R83	321-0441-00			383 kΩ, 1/8 W, 1%
R85	315-0472-00			4.7 kΩ, 1/4 W, 5%
R88	315-0472-00			4.7 kΩ, 1/4 W, 5%
R90	315-0472-00			4.7 kΩ, 1/4 W, 5%
R92	321-0235-00			2.74 kΩ, 1/8 W, 1%
R93	321-0289-00			10 kΩ, 1/8 W, 1%
R94	321-0271-00			6.49 kΩ, 1/8 W, 1%
R100	315-0472-00			4.7 kΩ, 1/4 W, 5%
R101	315-0103-00			10 kΩ, 1/4 W, 5%
R103	315-0472-00			4.7 kΩ, 1/4 W, 5%
R104	321-0376-00			80.6 kΩ, 1/8 W, 1%
R106	315-0472-00			4.7 kΩ, 1/4 W, 5%
R107	321-0318-00			20 kΩ, 1/8 W, 1%
R109	315-0472-00			4.7 kΩ, 1/4 W, 5%
R110	321-0347-00			40.2 kΩ, 1/8 W, 1%
R112	315-0472-00			4.7 kΩ, 1/4 W, 5%
R113	321-0376-00			80.6 kΩ, 1/8 W, 1%
R115	315-0472-00			4.7 kΩ, 1/4 W, 5%
R116	321-0353-00			46.4 kΩ, 1/8 W, 1%
R118	315-0472-00			4.7 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R119	321-0318-00			20 kΩ, 1/8 W, 1%
R121	315-0472-00			4.7 kΩ, 1/4 W, 5%
R122	321-0347-00			40.2 kΩ, 1/8 W, 1%
R124	315-0472-00			4.7 kΩ, 1/4 W, 5%
R125	321-0376-00			80.6 kΩ, 1/8 W, 1%
R127	315-0472-00			4.7 kΩ, 1/4 W, 5%
R128	321-0405-00			162 kΩ, 1/8 W, 1%
R130	315-0472-00			4.7 kΩ, 1/4 W, 5%
R131	321-0336-00			30.9 kΩ, 1/8 W, 1%
R135	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U3	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U5	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U23	156-0106-00			Diode array (6 matched), replaceable by RCA CA3039
U25	156-0106-00			Diode array (6 matched), replaceable by RCA CA3039
U33	156-0060-00			Volt. follower, replaceable by NSLM302H
U35	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U37	156-0049-00			Op ampl, replaceable by Fairchild μA741C
U61	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U65	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U67	156-0040-00			Quad latch, replaceable by T.I. SN7475N
U71	156-0057-00			Quad 2-input NAND gate w/open coll, replaceable by T.I. SN7401N
U75	156-0057-00			Quad 2-input NAND gate w/open coll, replaceable by T.I. SN7401N
U79	156-0057-00			Quad 2-input NAND gate w/open coll, replaceable by T.I. SN7401N
ASSEMBLY A13	670-1447-00	B050500	B079999	**INTERNAL DATA ROUTING TC#14 Circuit Card**
A13	670-1447-01	B070000		**INTERNAL DATA ROUTING TC#14 Circuit Card**
CAPACITORS				
C14	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C16	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C18	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C20	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C21	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C22	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C23	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C24	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C25	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C26	283-0177-00			1 μF, Cer, 25 V, +80%-20%
C27	283-0177-00			1 μF, Cer, 25 V, +80%-20%
SCD, DIODE				
VR59	152-0278-00			Zener, 1N4372A, 400 mW, 3 V, 5%
TRANSISTOR				
Q59	151-0208-00			Silicon, PNP, 2N4036

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS				
R1	315-0472-00			4.7 kΩ, 1/4 W, 5%
R3	315-0472-00			4.7 kΩ, 1/4 W, 5%
R6	315-0272-00			2.7 kΩ, 1/4 W, 5%
R8	315-0102-00			1 kΩ, 1/4 W, 5%
R10	315-0102-00			1 kΩ, 1/4 W, 5%
R11	315-0472-00			4.7 kΩ, 1/4 W, 5%
R12	322-0156-00			412 Ω, 1/4 W, 1%
R14	322-0651-00			667 Ω, 1/4 W, 1/2%
R15	308-0706-00			125 Ω, 1 W, WW, 1%
INTEGRATED CIRCUITS				
U1	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U3	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U5	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U7	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U9	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U11	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U13	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U15	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U17	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U19	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U21	156-0037-00			Dual 2 wide 2-input and-or-invert gate, replaceable by T.I. SN7451N
U23	156-0037-00			Dual 2 wide 2-input and-or-invert gate, replaceable by T.I. SN7451N
U25	156-0037-00			Dual 2 wide 2-input and-or-invert gate, replaceable by T.I. SN7451N
U27	156-0037-00			Dual 2 wide 2-input and-or-invert gate, replaceable by T.I. SN7451N
U29	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U31	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U33	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U35	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U37	156-0154-00			Dual 200 bit static shift reg, replaceable by Signetics 2511K

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U43	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U44	156-0092-00			Hex. invert w/open collector, replaceable by T.I. SN7405N
U45	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U46	156-0092-00			Hex. invert w/open collector, replaceable by T.I. SN7405N
U47	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U51	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U53	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U55	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U57	156-0154-00			Dual 200 bit static shift reg, replaceable by Signetics 2511K
ASSEMBLY A14	670-1520-00			**CHARACTER GEN CONTROL TC#15 Circuit Card**
CAPACITORS				
C12	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C16	285-0684-00			0.056 µF, Plastic, 100 V, 5%
C48	281-0504-00			10 pF, Cer, 500 V, 10%
C90	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C91	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C92	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C93	283-0177-00			1 µF, Cer, 25 V, +80%-20%
SCD, DIODE				
CR13	152-0185-00			Silicon, replaceable by 1N4152
TRANSISTORS				
Q10	151-0190-00			Silicon, NPN, 2N3904
Q12	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R12	315-0471-00			470 Ω, 1/4 W, 5%
R14	315-0104-00			100 kΩ, 1/4 W, 5%
R16	315-0102-00			1 kΩ, 1/4 W, 5%
R18	315-0133-00			13 kΩ, 1/4 W, 5%
R20	317-0472-00			4.7 kΩ, 1/8 W, 5%
R46	315-0472-00			4.7 kΩ, 1/4 W, 5%
R48	311-1285-00			25 kΩ, Var
INTEGRATED CIRCUITS				
U7	156-0079-00			Decade counter, replaceable by T.I. SN7490N
U9	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U11	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U13	156-0072-00			Monostable Multi, replaceable by T.I. SN74121N
U17	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U29	156-0058-00			Hex. invert, replaceable by T.I. SN7404N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U31	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U33	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U35	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U49	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U53	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U55	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
ASSEMBLY A15	670-1521-00			**CHARACTER GEN MEMORY TC#16 Circuit Card**
CAPACITORS				
C62	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C67	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C68	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C72	283-0177-00			1 µF, Cer, 25 V, +80%-20%
RESISTORS				
R10	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R10	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R11	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R11	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R12	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R12	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R13	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R13	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R14	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R14	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R20	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R20	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R21	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R21	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R22	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R22	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R23	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R23	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R24	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R24	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R25	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R25	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R30	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R30	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R31	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R31	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R32	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R32	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R33	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R33	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R34	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R34	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R35	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R35	315-0202-00	B090000		2 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R36	317-0202-00	B050500	B089999	2 kΩ, 1/8 W, 5%
R36	315-0202-00	B090000		2 kΩ, 1/4 W, 5%
R41	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R41	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R43	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R43	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R44	317-0472-00	B050500	B089999	4.7 kΩ, 1/8 W, 5%
R44	315-0472-00	B090000		4.7 kΩ, 1/4 W, 5%
R45	317-0512-00	B050500	B089999	5.1 kΩ, 1/8 W, 5%
R45	315-0512-00	B090000		5.1 kΩ, 1/4 W, 5%
R50	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R50	315-0272-00	B090000		2.7 kΩ ,1/4 W, 5%
R52	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R52	315-0272-00	B050500	B089999	2.7 kΩ, 1/4 W, 5%
R54	317-0272-00	B050500	B089999	2.7 kΩ, 1/8 W, 5%
R54	315-0272-00	B090000		2.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0103-00			Read only memory, MOS, replaceable by T.I. TMS4100
U5	156-0104-00			Read only memory, MOS, replaceable by T.I. TMS4100
U7	156-0102-00			Read only memory, MOS, replaceable by T.I. TMS4100
U9	156-0111-00			BCD to decimal decoder/driver 15 volt breakdown replaceable by T.I. SN74145N
U11	156-0113-00			Low power quad 2-input positive logic nand gate replaceable by T.I. SN74L00N
U13	156-0113-00			Low power quad 2-input positive logic nand gate replaceable by T.I. SN74L00N
U15	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U17	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U19	156-0041-00			Dual D flip-flop, replaceable by T.I. SN7474N
U29	156-0111-00			BCD to decimal decoder/driver 15 volt breakdown replaceable by T.I. SN74145N
U31	156-0079-00			Decade conunter, replaceable by T.I. SN7490N
U33	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U35	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U37	156-0061-00			BCD to dec decoder, replaceable by T.I. SN7442N
U39	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U45	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U47	156-0093-00			Hex. invert w/open collector, replaceable by T.I. SN7416N
U49	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U51	156-0073-00			5-bit shift register, replaceable by T.I. SN7496N
U53	156-0035-00			Dual 4-input buffer, replaceable by T.I. SN7440N
U55	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U57	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U59	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY A16	670-1451-00	B050500	B079999	**PLOT CONTROL TC#18 Circuit Card**
A16	670-1415-01	B080000		**PLOT CONTROL TC#18 Circuit Card**
CAPACITORS				
C10	283-0178-00			0.1 µF, Cer, 100 V, +80%-20%
C12	283-0178-00			0.1 µF, Cer, 100 V, +80%-20%
C40	283-0110-00			0.005 µF, Cer, 150 V
C44	283-0116-00			820 pF, Cer, 500 V, 5%
C52	285-0598-00			0.01 µF, PTM, 100 V, 5%
C53	285-0598-00			0.01 µF, PTM, 100 V, 5%
C54	285-0598-00			0.01 µF, PTM, 100 V, 5%
C67	285-0703-00			0.1 µF, PTM, 100 V, 5%
C73	283-0178-00			0.1 µF, Cer, 100 V, +80%-20%
C90	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C91	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C92	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C93	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C94	283-0177-00			1 µF, Cer, 25 V, +80%-20%
CR10	152-0185-00			Silicon, replaceable by 1N4152
CR12	152-0o85-00			Silicon, replaceable by 1N4152
CR20	152-0185-00			Silicon, replaceable by 1N4152
CR21	152-0185-00			Silicon, replaceable by 1N4152
CR22	152-0185-00			Silicon, replaceable by 1N4152
CR23	152-0185-00			Silicon, replaceable by 1N4152
CR26	152-0185-00			Silicon, replaceable by 1N4152
CR28	152-0185-00			Silicon, replaceable by 1N4152
CR32	152-0185-00			Silicon, replaceable by 1N4152
CR40	152-0185-00			Silicon, replaceable by 1N4152
CR43	152-0185-00			Silicon, replaceable by 1N4152
CR52	152-0185-00			Silicon, replaceable by 1N4152
CR71	152-0185-00			Silicon, replaceable by 1N4152
CR81	152-0185-00			Silicon, replaceable by 1N4152
CR82	152-0185-00			Silicon, replaceable by 1N4152
Q15	151-0190-00			Silicon, NPN, 2N3904
Q16	151-0190-00			Silicon, NPN, 2N3904
Q17	151-0188-00			Silicon, PNP, 2N3906
Q35	151-0190-00			Silicon, NPN,. 2N3904
Q36	151-0260-00			Silicon, NPN, 2N5189
Q37	151-0504-00			Silicon, unijunction, 2N3851
Q38	151-0190-00			Silicon, NPN, 2N3904
Q54	151-0188-00			Silicon, PNP, 2N3906
Q55	151-0190-00			Silicon, NPN, 2N3904
Q56	151-0190-00			Silicon, NPN, 2N3904
Q57	151-0188-00			Silicon, PNP, 2N3906
Q58	151-0190-00			Silicon, NPN, 2N3904
Q59	151-0190-00			Silicon, NPN, 2N3904

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS				
R1	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R1	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R2	317-0047-00	B050500	B089999	4.7 Ω, 1/8 W, 5%
R2	315-0047-00	B090000		4.7 Ω, 1/4 W, 5%
R3	315-0103-00			10 kΩ, 1/4 W, 5%
R5	315-0472-00			4.7 kΩ, 1/4 W, 5%
R6	315-0301-00			300 Ω, 1/4 W, 5%
R10	315-0471-00			470 Ω, 1/4 W, 5%
R12	315-0471-00			470 Ω, 1/4 W, 5%
R14	315-0102-00			1 kΩ, 1/4 W, 5%
R16	315-0102-00			1 kΩ, 1/4 W, 5%
R17	311-1280-00			1 kΩ, Var
R19	311-1280-00			1 kΩ, Var
R22	315-0104-00			100 kΩ, 1/4 W, 5%
R24	315-0103-00			10 kΩ, 1/4 W, 5%
R26	315-0222-00			2.2 kΩ, 1/4 W, 5%
R28	315-0104-00			100 kΩ, 1/4 W, 5%
R29	315-0472-00			4.7 kΩ, 1/4 W, 5%
R31	321-0268-00			6.04 kΩ, 1/8 W, 1%
R33	321-0280-00			8.06 kΩ, 1/8 W, 1%
R35	315-0302-00			3 kΩ, 1/4 W, 5%
R40	315-0153-00			15 kΩ, 1/4 W, 5%
R42	301-0222-00			2.2 kΩ, 1/2 W, 5%
R44	315-0472-00			4.7 kΩ, 1/4 W, 5%
R50	315-0223-00			22 kΩ, 1/4 W, 5%
R51	315-0103-00			10 kΩ, 1/4 W, 5%
R52	315-0223-00			22 kΩ, 1/4 W, 5%
R53	315-0472-00			4.7 kΩ, 1/4 W, 5%
R54	321-0283-00			8.66 kΩ, 1/8 W, 1%
R56	321-0257-00			4.64 kΩ, 1/8 W, 1%
R60	315-0222-00			2.2 kΩ, 1/4 W, 5%
R62	315-0221-00			220 Ω, 1/4 W, 5%
R63	315-0150-00			15 Ω, 1/4 W, 5%
R65	315-0242-00			2.4 kΩ, 1/4 W, 5%
R70	311-1285-00			25 kΩ, Var
R71	321-0327-00			24.9 kΩ, 1/8 W, 1%
R73	315-0221-00			220 Ω, 1/4 W, 5%
R90	315-0102-00			1 kΩ, 1/4 W, 5%
R92	315-0102-00			1 kΩ, 1/4 W, 5%
R94	315-0102-00			1 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U1	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U3	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U5	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U7	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U9	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U13	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U21	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U23	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U25	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U27	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U29	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U31	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U33	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U35	156-0150-00			Quad 2 input pos logic NAND buffer, replaceable by T.I. SN7437N
U41	156-0061-00			BCD to dec decoder, replaceable by T.I. SN7442N
U43	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U45	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U47	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U49	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U51	156-0036-00			Dual 4-input buffer, replaceable by T.I. SN7440N
U53	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
ASSEMBLY A17	670-1452-00			**I/O CONTROL TC#19 Circuit Card**
CAPACITORS				
C10	281-0580-00			470 µF, Cer, 500 V, 10%
C40	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C41	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C42	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C43	283-0177-00			1 µF, Cer, 25 V, +80%-20%
TRANSISTOR				
Q1	151-0190-00			Silicon, NPN, 2N3904
RESISTORS				
R1	315-0472-00			4.7 kΩ, 1/4 W, 5%
R3	315-0472-00			4.7 kΩ, 1/4 W, 5%
R5	315-0472-00	XB090000		4.7 kΩ, 1/4 W, 5%
R7	315-0472-00			4.7 kΩ, 1/4 W, 5%
R10	315-0332-00			3.3 kΩ, 1/4 W, 5%
R11	315-0222-00			2.2 kΩ, 1/4 W, 5%
R12	315-0472-00			4.7 kΩ, 1/4 W, 5%
R13	315-0472-00			4.7 kΩ, 1/4 W, 5%
R15	315-0472-00			4.7 kΩ, 1/4 W, 5%
R18	315-0472-00			4.7 kΩ, 1/4 W, 5%
R20	315-0222-00			2.2 kΩ, 1/4 W, 5%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS				
U3	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U5	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U9	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U15	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U17	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U19	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U21	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U23	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U25	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U29	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U35	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U37	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U41	156-0042-00			Dual J-K flip-flop, replaceable by T.I. SN7476N
U43	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U45	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U46	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U55	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U57	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U59	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
ASSEMBLY				
A18	670-0679-00	B010100	B099999	**POWER SUPPLY Circuit Card**
	670-0679-01	B100000		
CAPACITORS				
C12	290-0159-00			2 µF, Elect., 150 V
C15	290-0290-00			10 µF, Elect., 25 V, 20%
C18	281-0580-00			470 pF, Cer, 500 V, 10%
C45	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C59	285-0686-00			0.068 µF, PTM, 100 V, 10%
C63	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C70	285-0702-00			0.033 µF, PTM, 100 V, 5%
C76	290-0105-00			100 µF, Elect., 6 V
C87	281-0580-00			470 pF, Cer, 500 V, 10%
C93	290-0290-00			10 µF, Elect., 25 V, 20%

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SCD, DIODES				
CR11	152-0107-00			Silicon, replaceable by 1N647
CR12	152-0107-00			Silicon, replaceable by 1N647
CR14	152-0200-00			Rectifier bridge, MDA 962-5
CR52	152-0185-00			Silicon, replaceable by 1N4152
CR60	152-0107-00			Silicon, replaceable by 1N647
CR61	152-0107-00			Silicon, replaceable by 1N647
CR65	152-0185-00			Silicon, replaceable by 1N4152
CR82	152-0200-00			Rectifier bridge, MDA 962-5
VR21	152-0168-00			Zener, 1N963A, 400 mW, 12 V, 5%
VR45	152-0212-00			Zener, 1N936, 500 mW, 9 V, 5%
VR63	152-0195-00			Zener, 1N751A, 400 mW, 5.1 V, 5%
TRANSISTORS				
Q24	151-0190-00			Silicon, NPN, 2N3904
Q26	151-0190-00			Silicon, NPN, 2N3904
Q34	151-0188-00			Silicon, PNP, 2N3906
Q60	151-0188-00			Silicon, PNP, 2N3906
Q64	151-0223-00			Silicon, NPN, 2N4275
Q70	151-0223-00			Silicon, NPN, 2N4275
RESISTORS				
R15	308-0587-00			0.9 Ω, 1/2 W, WW, 5%
R17	321-0279-00			7.87 kΩ, 1/8 W, 1%
R18	315-0392-00			3.9 kΩ, 1/4 W, 5%
R19	321-0275-00			7.15 kΩ, 1/8 W, 1%
R21	315-0302-00			3 kΩ, 1/4 W, 5%
R24	315-0512-00			5.1 kΩ, 1/4 W, 5%
R26	315-0511-00			510 Ω, 1/4 W, 5%
R32	315-0621-00			620 Ω, 1/4 W, 5%
R34	315-0470-00			47 Ω, 1/4 W, 5%
R36	315-0202-00			2 kΩ, 1/4 W, 5%
R37	315-0512-00			5.1 kΩ, 1/4 W, 5%
R40	321-0231-00			2.49 kΩ, 1/8 W, 1%
R41	311-0540-00			2.5 kΩ, Var
R42	321-0289-00			10 kΩ, 1/8 W, 1%
R44	315-0512-00			5.1 kΩ, 1/4 W, 5%
R45	315-0102-00			1 kΩ, 1/ 4 W, 5%
R50	321-0193-00			1 kΩ, 1/8 W, 1%
R51	321-0239-00			3.01 kΩ, 1/8 W, 1%
R53	315-0302-00			3 kΩ, 1/4 W, 5%
R54	315-0123-00			12 kΩ, 1/4 W, 5%
R55	315-0103-00			10 kΩ, 1/4 W, 5%
R57	315-0333-00			33 kΩ, 1/4 W, 5%
R59	315-0101-00			100 Ω, 1/4 W, 5%
R60	315-0682-00			6.8 kΩ, 1/4 W, 5%
R62	315-0682-00			6.8 kΩ, 1/4 W, 5%
R63	315-0301-00			300 Ω, 1/4 W, 5%
R65	315-0153-00			15 kΩ, 1/4 W, 5%
R67	321-0216-00			1.74 kΩ, 1/8 W, 1%

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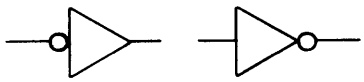
Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R70	315-0102-00			1 kΩ, 1/4 W, 5%
R71	315-0102-00			1 kΩ, 1/4 W, 5%
R76	321-0181-00			750 Ω, 1/8 W, 1%
R77	315-0201-00			200 Ω, 1/4 W, 5%
R85	308-0587-00			0.9 Ω, 1/2 W, WW, 5%
R87	315-0392-00			3.9 kΩ, 1/4 W, 5%
R90	321-0268-00			6.04 kΩ, 1/8 W, 1%
R91	311-0540-00			2.5 kΩ, Var
R93	321-0266-00			5.76 kΩ, 1/8 W, 1%
INTEGRATED CIRCUITS				
U16	156-0053-00			Volt. reg, replaceable by Fairchild μA723C
U42	156-0048-00			Linear, replaceable by RCA CA3046
U86	156-0053-00			Volt. reg, replaceable by Fairchild μA723C
ASSEMBLY				
A19	119-0269-00	B050500	B089999	**KEYBOARD Assembly**
A19	119-0269-01	B090000		**KEYBOARD Assembly**
BULBS				
B1 thru B5	150-0120-00			Incandescent, 5 V, 115 mA
CAPACITORS				
C1	283-0078-00			0.001 μF, Cer, 500 V, 20%
C2	283-0170-00			50 pF, Cer, 200 V, 10%
C3	290-0286-00			50 μF, Elect., 25 V, +75%-10%
C4	283-0013-00			0.01 μF, Cer, 1000 V, +100%-0%
C5	283-0013-00			0.01 μF, Cer, 1000 V, +100%-0%
C6	290-0106-00			10 μF, Elect., 15 V
C7	290-0286-00	XB090000		50 μF, Elect., 25 V, +75%-10%
DIODE				
CR1	152-0185-00	XB090000		Silicon, replaceable by 1N4152
TRANSISTORS				
Q1	151-0164-00			Silicon, PNP, 2N3702
RESISTORS				
R1	316-0562-00			5.6 kΩ, 1/4 W, 10%
R2	316-0562-00	B050500	B089999	5.6 kΩ, 1/4 W, 10%
R2	316-0103-00	B090000		10 kΩ, 1/4 W, 10%
R3	316-0562-00			5.6 kΩ, 1/4 W, 10%
R4	316-0152-00			1/5 kΩ, 1/4 W, 10%
R5	315-0391-00			390 Ω, 1/4 W, 5%
R6	315-0684-00			680 kΩ, 1/4 W, 5%
R7	316-0104-00			100 kΩ, 1/4 W, 10%
R8	316-0562-00			5.6 kΩ, 1/4 W, 10%
R9	302-0271-00			270 Ω, 1/2 W, 10%
R10	316-0472-00	XB090000		4.7 kΩ, 1/4 W, 10%
R11	316-0103-00	XB090000		10 kΩ, 1/4 W, 10%

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SWITCHES				
SW1 thru 27	260-1347-00			Push, SPST, Keyboard Switch
SW1 thru 27	260-1347-00			Push, SPST, Keyboard Switch
29 32				
34 47				
49 69				
SW33	260-1348-00			Push, SPST, Lighted Keyboard Switch
48				
70				
71				
72				
SW28	260-1349-00			Push, DPST, Keyboard Switch
INTEGRATED CIRCUITS				
X1	156-0030-00			Quad 2-input positive nand gate, replaceable by T.I. SN7400N
X2	156-0169-00			Hex. inverter, replaceable by T.I. SN15836N
X3	156-0168-00			Read only memory, MOS
X4	156-0058-00			Hex. inverter, replaceable by T.I. SN7404N
X5	156-0043-00			Quad 2-input positive nor gate, replaceable by T.I. SN7402N
X6	156-0149-00			Dual nand Schmitt triggers, replaceable by T.I. SN7413N
X7	156-0170-00			Quad 2-input positive nand gate, replaceable by T.I. SN15846N
ASSEMBLY				
	670-0857-01			**AUXILIARY INTERCONNECTOR Circuit Board Assembly**
CONNECTORS				
J341	131-0870-00	B050500	B069999	Receptacle, electrical, female
J341	131-0972-00	B070000		Receptacle, electrical, female
J342	131-0870-00	B050500	B069999	Receptacle, electrical, female
J342	131-0972-00	B070000		Receptacle, electrical, female
J343	131-0870-00	B050500	B069999	Receptacle, electrical, female
J343	131-0972-00	B070000		Receptacle, electrical, female
J344	131-0870-00	B050500	B069999	Receptacle, electrical, female
J344	131-0972-00	B070000		Receptacle, electrical, female

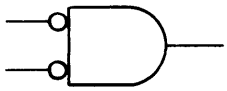
SECTION 5
DIAGRAMS

Contents:

Inverters

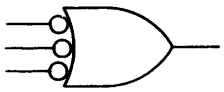


Inverted Input AND



2 lows in = high out

Inverted Input OR

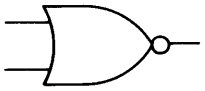


1 or more low inputs = high out

NAND

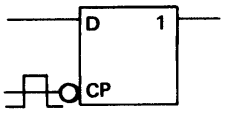
3 high inputs = low output

NOR



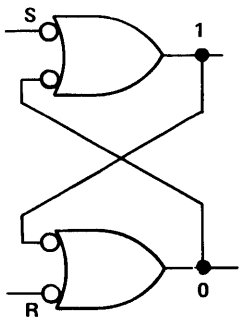
1 or more high inputs = low output

Latch



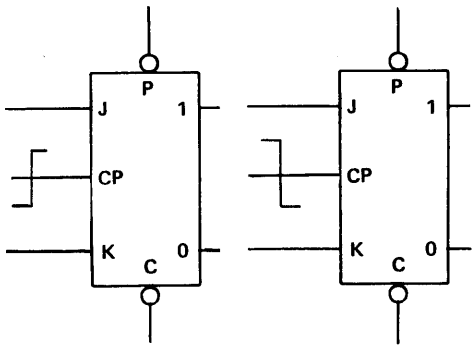
1 follows D with CP high; with CP low, 1 holds state of D which existed at CP switching time

R-S Flip-Flop



One-sets with low into S; zero-sets with low into R; 1 and 0 both high if R and S both low

Clocked J-K Flip-Flop



It is assumed that unspecified inputs are high in each of the following:

One-sets with low level into P; remains one-set with P held low. P over-rides CP.

Zero-sets with low level into C; remains zero-set with C held low. C over-rides CP.

1 and 0 outputs are both high if P and C are both low.

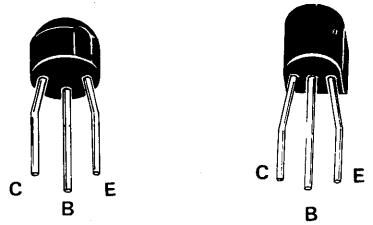
1 and 0 outputs exchange states with indicated transition into CP if J and K are both high.

One-sets with indicated transition into CP if J high, 1 low, (regardless of level at K).

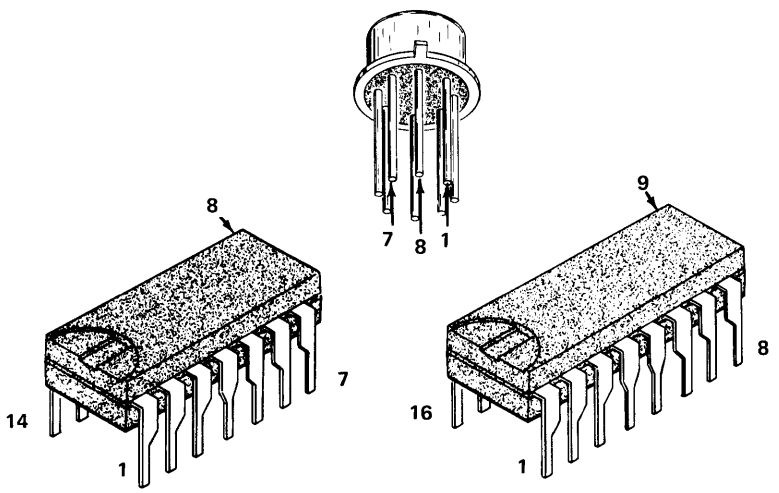
Zero-sets with indicated transition into CP if K high, 0 low, (regardless of level at J).

(A) Integrated circuit logic functions. One-set means that the 1 output is high, 0 output is low. Zero-set means the inverse is true.

TRANSISTORS



INTEGRATED CIRCUITS



(B) Semiconductor pin identification, top views.

Fig. 5-1. Semiconductor information.

4002A DICTIONARY OF LINE TITLES

CODE: L = LEVEL
P = PULSE
S = SOURCE
T = TYPE SIGNAL
* = INDICATES LOW ACTIVE (i.e., LE* = $\overline{LE}$)

NAME	T	SOURCE	DEFINITION
+Y	*P	TC18-C	Controls Y direction during incremental plot
+15V	L	PWR SUP	Power supply voltage
+5V	L	PWR SUP	Power supply voltage
−X	*P	TC18-8	Controls X direction during incremental plot
−12V	L	TC1-11	Power supply voltage modified for Keyboard use
−15V	L	PWR SUP	Power supply voltage
A	P	TC16-AA	D/A modifier for writing characters
ACK	*P	TC7-20	Control character
AG	*L	J342-6	Auxiliary Unit control signal
AGREE	P	TC5-U	Indication that the Scratch Pad cursor counter and character counter agree
AGREE	*P	TC5-V	Indication that the Scratch Pad cursor counter and character counter agree
ALF RSET	*P	TC18-T	Signal for resetting to Alphanumeric Mode
ALFA	L	TC18-9	Indication of Alphanumeric Mode existance
ALFA ORG	*P	TC7-26	"Home" signal, strappable to any control character — normally SOH
ALFA 2	L	TC18-10	Indication of Alphanumeric Mode existance
AUX +Y	*P	J343-11	Auxiliary control of Y register incrementing direction
AUX −X	*P	J343-3	Auxiliary control of X register incrementing direction
AUX COMP	*P	J341-14	Indication that the Auxiliary Unit has completed its assigned function
AUX PLOT	L	TC19-N	Input disabling signal indicating the Auxiliary Unit is controlling the registers
AUX PLOT	*L	J342-12	An indication that the Auxiliary Unit is performing some function
AUX PLT	*L	J342-8	A derivation of $\overline{\text{AUX PLOT}}$
AUX Z	*P	J341-9	Unblanking command from the Auxiliary Unit
AUXDCOMP	*P	TC14-11	A completion signal caused by the Auxiliary Unit or completion of X Register spacing
AUXINSTR	P	TC19-24	Input strobe for Auxiliary Unit; dependent on $\overline{\text{AG}}$/$\overline{\text{PRNT BSY}}$ and DATA STRB/RCV STROB
AUXPLOTX	*P	J343-19	Command from Auxiliary Unit for incrementing X register
AUXPLOTY	*P	J343-21	Command from Auxiliary Unit for incrementing Y register
AUXPLTIO	*L	TC14-21	Indicates Auxiliary Unit is performing a function; dependent on $\overline{\text{AUX PLOT}}$
AUXSTROB	P	J341-33	Data input strobe from Auxiliary Unit
A1	P	J341-18	Data input bits from Auxiliary Unit
A2	P	J341-28	
A3	P	J341-27	
A4	P	J341-25	
A5	P	J341-26	
A6	P	J341-6	
A7	P	J341-7	
A8	P	J341-8	

NAME	T	SOURCE	DEFINITION
B	P	TC16-16	D/A modifier for writing characters
BAK SPAC	*P	TC7-10	Back spacing command dependent on control characters; normally BS
BEL	*P	TC7-19	Control character
BEL SPKR	P	TC1-6	Signal power supply line to the speaker
BEL X	*P	TC12-18	End of line warning signal for actuating bell
BIT 8	P	TC1-2	Most significant data bit; generated in Terminal; normally parity
BREAK	*L	TC1-27	Interrupt signal originated by $\overline{\text{BREAK KY}}$ signal
BREAK KY	*L	J101-11	Source signal for BREAK; originated by Keyboard key
BS	*P	TC7-9	Control character
BUF X GD	L	J152-1	Shield for BUF X LDR
BUF Y GD	L	J151-1	Shield for BUF Y LDR
BUFXLDR	P	J152-2	Unmodified D/A output signal indicative of X Register contents
BUFYLDR	P	J151-2	Unmodified D/A output signal indicative of Y Register contents
B1	P	TC2-4	Data bits originated by Keyboard, Auxiliary Unit, or Scratch Pad
B2	P	TC2-5	
B3	P	TC2-6	
B4	P	TC2-K	
B5	P	TC2-L	
B6	P	TC2-M	
B7	P	TC2-P	
B8	P	TC2-X	
C	P	TC16-17	D/A modifier for writing characters
CAN	*P	TC7-8	Control character
CAR RTN	P	TC7-15	Carriage return signal initiated by control character CR and optionally LF
CAR RTN	*P	TC7-3	Complement of CAR RTN
CC CNTUP	P	TC4-Y	Scratch Pad cursor counter incrementing signal; occurs during Edit Mode character insert
CC LOAD	*P	TC4-L	Scratch Pad cursor counter load signal; occurs when switching out of Edit Mode
CCCNTDWN	P	TC4-Z	Scratch Pad cursor counter decrementing signal; occurs during Edit Mode character delete
CF COMP	*P	TC7-16	Control Function completion signal, occurring 64 μs after CF EXEC occurs
CF EXEC	P	TC14-T	Control Function execute signal occurring upon receipt of control character
CG RESET	P	TC15-DD	Character Generator reset signal which initializes the character matrix generator
CHARCOMP	*P	TC16-19	Character completion signal occurring when writing matrix has been completed
CHAREXEC	*P	TC14-Y	Character execute signal which initiates character writing
CHARPROC	*P	TC16-28	Character in process signal which accompanies character writing
CLEAR	P	TC5-13	Signal which clears data shift register prior to loading data in TC-14
CLEAR	*P	TC4-14	Scratch Pad clearing and resetting signal; clears memory devices
CLRTOSND	L	J121-22	Signal from Interface Unit indicating it can receive data from the Auxiliary Unit
CLSETARM	P	TC4-T	Permits data loading into the TC-14 shift register
COMM ERR	*P	J121-23	Communication error signal which causes italic writing of alphanumeric character
COMP SW	*L	J102-7	Compose Mode signal caused by Keyboard Compose switch
COMPOSE	L	TC4-20	Compose Mode signal
COMPOSE	*L	TC4-19	Compose Mode signal
COUNT UP	P	TC4-9	Scratch Pad cursor storage register incrementing signal
COUNTDWN	P	TC4-K	Scratch Pad cursor storage register decrementing signal
CR	P	TC7-2	Control character for carriage return
CS LOAD	*P	TC4-D	Loading command for cursor storage; occurs when Edit Mode is selected
CUR LFT	*P	TC1-EE	X Register decrementing command resulting from left directional shift key
CUR SHF	*P	TC15-FF	Moves alphanumeric cursor alternately to each of two positions
CUR UP	*P	TC1-DD	Y Register incrementing command resulting from up directional shift key
CURDN KY	*L	J102-13	Signal from down directional shift key
CURLFTKY	*L	J102-19	Signal from left directional shift key
CURRT KY	*L	J102-12	Signal from right directional shift key

NAME	T	SOURCE	DEFINITION
CURUP KY	*L	J102-20	Signal from up directional shift key
D	P	TC16-18	D/A modifier for writing characters
DATASTRB	P	TC2-21	Data processing strobe resulting from Scratch Pad, Auxiliary, or Keyboard strobe
DBLSZCHR	*L	TC19-6	Indicates that a double size character condition exists
DBLSZCMD	P	TC7-18	Double size command initiated by a control character, usually EM
DB1	P	TC14-B	
DB2	P	TC14-C	
DB3	P	TC14-D	
DB4	P	TC14-3	
DB5	P	TC14-4	
DB6	P	TC14-P	
DB7	P	TC14-8	
DB8	P	TC14-9	
DC1	P	TC7-FF	
DC2	P	TC7-Y	
DC3	P	TC7-BB	
DC4	*P	TC7-U	
DELETE	P	TC14-10	Deletion signal for removing character from Scratch Pad memory
DELTA X	P	TC13-17	X D/A rate-of-change signal for controlling unblanking in Linear Interpolate Mode
DELTA Y	P	TC9-Y	Y D/A rate-of-change signal for controlling unblanking in Linear Interpolate Mode
DLE	P	TC7-DD	Control character
DO PAUSE	*P	TC5-28	Initiating command for PAUSE
DROP FLG	*P	TC11-A	Local or Local Echo command for putting RCV RDY low
DR1	P	TC11-10	
DR2	P	TC11-9	
DR3	P	TC11-11	
DR4	P	TC11-12	
DR5	P	TC11-26	
DR6	P	TC11-23	
DR7	P	TC11-25	
DR8	P	TC11-24	
E	*P	TC16-22	D/A modifier for writing characters
EDIT	*L	TC1-X	Edit Mode command signal
EDIT FF	*P	TC4-N	Indication that Edit Mode exists
EDIT KY	*L	J101-16	Initiating command for Edit Mode
EDIT LMP	*L	TC1-10	Lamp drive signal
EM	*P	TC7-N	Control character
ENQ	P	TC7-W	Control character
EOL	*P	TC12-AA	End of line indicator from X Register
EOT	P	TC7-V	Control character; switches Terminal from Unrefreshed to Refreshed Mode
ERASE	*P	TC7-7, TC1-V	Screen-erasing signal generated by Keyboard key or control character, usually CAN; open collector signal
ERASE KY	*L	J102-18	Keyboard erase-command signal
ERASEINTV	*P	J251-7	Indication that the CRT is busy erasing
ESC	*P	TC7-L	Control character
ETB	*P	TC7-T	Control character
ETX	*P	TC7-AA	Control character
EXEC	P	TC5-22	Execution command; derived from TC IN STRB or SP EXEC

DB1–DB8: Data bits used by the Character Generator

DC1–DC4: Control characters

DR1–DR8: Data bits for internal routing

NAME	T	SOURCE	DEFINITION
F	*P	TC16-23	D/A modifier for writing characters
FF	*P	TC7-H	Control character
FS	P	TC7-F	Control character; commands Terminal into Point Plot Mode
FULL	*P	TC1-22	Extinguishes Full lamp in Direct Mode; clears memory in Scratch Pad Mode
FULL KY	*P	J102-11	Initiating command for $\overline{\text{FULL}}$; from Keyboard
FULL LMP	*L	TC1-7	Full lamp drive signal
FULLLITE	L	TC5-W	Control signal for $\overline{\text{FULL LMP}}$
FUNCCOMP	P	TC2-CC	Function complete signal
G	*P	TC16-24	D/A modifier for writing characters
GDIV	P	TC18-CC	Gate Drive Initializing Vector; command which accompanies first Linear Interpolate vector
GDLI	P	TC18-BB	Gate Drive Linear Interpolate; Indication of Linear Interpolate Mode
GND	L	PWR SUP	Ground
GRAF Z	L	TC18-8	Graphic write signal
GRAF 2	L	TC18-X	Indication of being in Graphic Mode
GS	P	TC7-J	Control character; commands Terminal into Linear Interpolate Mode
GS+FS	*P	TC18-P	Graphic Mode signal normally derived from control characters GS or FS
GWA	L	TC11-13	Indicates that the Graphic Word Assembler is in use for Graphic Modes
GWA	*L	TC11-20	Complement of GWA except while control characters are being accomplished in graphics
GWA COMP	*P	TC11-27	Indicates completion of graphic point or vector writing
GZ COMP	*P	TC18-11	Indicates completion of graphic point, vector, or increment
H COPY	L	J251-13	Reserved for HC Target signal
HC GND	L	J251-12	Target coaxial ground
HCU PRNT	*P	TC7-28	Hard Copy Unit print command initiated by control character; usually $\overline{\text{ETB}}$; open collector signal
HI X EN	P	TC11-EE	Parallel loading command for high bit X registers
HI Y EN	P	TC11-21	Parallel loading command for high bit Y registers
HOLD	*L	TC1-17	Drops display unit intensity below viewing level
HOME	*P	TC1-5	Reset signal
HOME KY	*L	J101-18	Initiating signal for $\overline{\text{HOME}}$; from Keyboard
HT	*P	TC7-M	Control character
IN AUX	*L	J341-19	Selects Auxiliary Unit inputs only
IN KBAUX	L	J341-32	Terminal under control of either Keyboard or Auxiliary Unit
INHIBITX	*P	TC4-BB	Prevents Scratch Pad from controlling X Register or Character Generator
INITIAL	L	TC5-10	Cancels Edit Mode in response to $\overline{\text{CLEAR}}$ signal
INITIAL	*L	TC1-D	Terminal initializing command
INSERT	*L	J102-5	Scratch Pad character inserting command
INSERTFF	L	TC14-16	Indicates character can be inserted or deleted
INTENS 2	*L	TC19-B	Double intensity signal used during double size character and bright vector writing; open collector signal
INTENS 3	*L	J343-9	Over-riding intensity signal from Auxiliary Unit
IOMGNSHF	*P	J121-33	Margin shift control signal from Interface Unit
ITAL CMD	P	TC7-17	Italic command generated by control character; usually SO
ITALIC	L	TC19-11	Italic control signal caused by communication error or control character

NAME	T	SOURCE	DEFINITION
KB ENABL	L	J121-32	Keyboard enabling signal from Interface Unit
KB STROB	P	TC2-26	Data strobcaused by $\overline{\text{RKB STROB}}$ from Keyboard
KB1	P	J101-27	Keyboard data bits
KB2	P	J101-26	
KB3	P	J101-25	
KB4	P	J101-24	
KB5	P	J101-30	
KB6	P	J101-29	
KB7	P	J101-28	
KB8	P	J101-9	
KEY SW	*L	J102-8	Ground closure created by Keyboard Power switch
KR SHIFT	*P	TC8-16	Indication that character rotation is in effect
KR1	P	TC8-8	D/A modifier outputs of the Character Rotator
KR2	P	TC8-12	
KR3	P	TC8-H	
KR4	P	TC8-L	
KR5	P	TC8-9	
KR6	P	TC8-N	
KR7	P	TC8-P	
KR8	P	TC8-13	
KSE	P	TC5-DD	Keyboard strobe timing signal for data entry to Scratch Pad
LE	*L	J121-10	Local echo command from Interface Unit
LE COMP	*P	TC19-F	Completion signal generated from $\overline{\text{AUX COMP}}$, FUNC COMP, or $\overline{\text{XMIT COMP}}$
LF	*P	TC7-5	Control character
LI BUSY	*L	TC18-19	Indication that a linear interpolate vector is being drawn
LINEFEED	*P	TC7-4	Line feed command caused by a control character; usually LF
LITE 1	L	J122-3	Keyboard lamp control lines for special applications
LITE 2	L	J122-7	
LITE 3	L	J122-15	
LITE 4	L	J122-17	
LO X EN	P	TC11-2	Parallel loading command for low X register bits
LO Y EN	P	TC11-1	Parallel loading command for low Y register bits
LOADDATA	*P	J121-26	Command from Interface Unit or Auxiliary Unit which permits loading Scratch Pad memory
LOC ECHO	*L	TC19-Y	Internal local echo signal caused by refreshed Scratch Pad Modes, or by $\overline{\text{LE}}$
LOCAL	L	J101-36	Caused by Keyboard rocker switch being in Local
MGN SHFT	*P	TC1-Y	Margin shift command caused by $\overline{\text{MGN SHF PB}}$
MGNSHFPB	*L	J101-15	Ground closure created by Keyboard Margin key
MOS CLK	P	TC4-CC	Shift register serial clock pulses from Scratch Pad
MOS DATA	P	TC14-W	Scratch Pad memory input bit stream
MOS DATA	*P	TC3-27	Scratch Pad memory output bit stream
NAK	P	TC7-X	Control character
NUL	*P	TC7-EE	Control character
NUL DET	*P	TC14-V	Nul signal detection for use in the Character Generator

NAME	T	SOURCE	DEFINITION
ON LINE	L	J101-17	Caused by Keyboard rocker switch being at On Line
PAGEFULL	*P	TC10-BB	Indication of alphanumeric page full; inhibits RCV RDY signal
PANEL LK	*L	TC1-J	Keyboard disabling signal controlled by Keyboard Power switch
PAUSE	*P	TC4-M	Retrace delay occurring when Scratch Pad cycles from last to first memory position
PF LITE	L	TC10-20	Signal to Keyboard and Interface Unit indicating page full; reset by Keyboard Full key
PF PULSE	*P	TC10-DD	Pulse indicating that page full occurred
PF RESET	*P	J122-22	Interface signal used to reset PF LITE and $\overline{\text{PAGE FULL}}$ signals
PRGM GND	L	PWR SUP	Ground
PRNT BSY	*L	J251-10	Hard Copy Unit busy signal
RAWSTROB	P	J101-31	Strobe which accompanies data from keyboard
RB1	P	J122-33	Receive data bits from Interface Unit
RB2	P	J122-32	
RB3	P	J122-31	
RB4	P	J122-13	
RB5	P	J122-12	
RB6	P	J122-10	
RB7	P	J122-16	
RB8	P	J122-11	
RCV RDY	L	TC19-19	Signal to Interface Unit indicating ability to accept data
RCVSTROB	P	J121-34	Signal from Interface Unit which accompanies input data
REFRSH	L	TC4-27	Indication of refreshed Scratch Pad Mode
RESETSND	*P	J122-29	Interface Unit command to re-initiate send operation
RING	*P	TC7-21	Open collector signal caused by control character; usually BEL
RKBSTROB	P	TC1-A	Keyboard strobe signal caused by RAW STROB from Keyboard
RPT KY	*L	J101-34	Keyboard signal caused by Repeat key
RS	P	TC7-B	Control character; commands Terminal into Incremental Plot Mode
RSET INS	*P	TC5-15	Reset signal which follows each insertion or deletion during Edit Mode
RSETVIEW	*P	TC14-12	View restoring signal which accompanies each character input
SCAN CLK	P	TC15-21	Clock signal for advancing character-writing matrix
SEND	P	TC5-26	Scratch Pad send indication
SEND	*P	TC1-Z	Send initiating command caused by Keyboard Send key
SEND KY	*L	J102-4	Result of pressing Keyboard Send key; initiates Scratch Pad send operation
SEND LMP	*L	TC1-8	Keyboard lamp drive signal indicating send is in progress
SENDSCRN	*P	J122-1	Command from Interface Unit causing Scratch Pad memory contents to be displayed
SET	P	TC5-7	Scratch Pad memory character loading command
SHIFT DN	*P	TC16-FF	Character matrix shift command for characters g, j, p, q, y, underline
SI	*P	TC7-D	Control character
SO	*P	TC7-C	Control character
SOH	*P	TC7-25	Control character
SP ARM	*P	TC7-12	Arming signal for program control of Scratch Pad and Horizontal Tab
SP COMP	*P	TC4-13	Unrefreshed Scratch Pad loading complete signal
SP ERASE	*P	TC7-24	Open-collector erase command for Scratch Pad; generated by control character, normally ESC; applicable only to optional stored Scratch Pad
SP EXEC	P	TC4-22	Command for executing Scratch Pad memory data which is in shift register
SP EXEC	*P	TC4-23	Signal for advancing Scratch Pad position counter
SP EXECX	P	TC5-20	Scratch Pad spacing command to X Register
SP KSE	P	TC4-24	Keyboard enabling signal indicating Scratch Pad can accept a character
SP LE	*L	TC19-W	Scratch Pad local echo signal which disables XMIT RDY
SP RSETX	*P	TC5-BB	X Register resetting command occurring when Scratch Pad memory recycles to first character
SP SEND	*P	TC5-FF	Indication that Scratch Pad is in Send Mode
SP STRIP	*L	TC5-2	Sets Y register to Scratch Pad position

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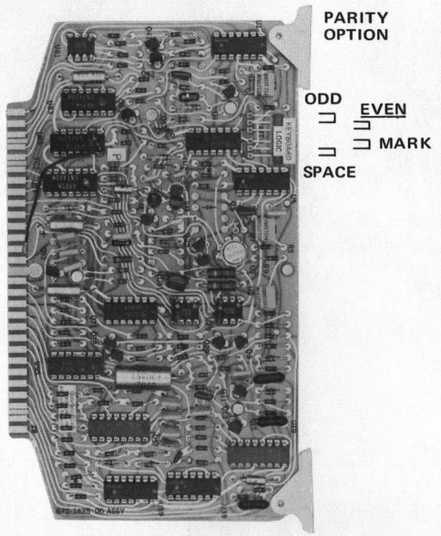
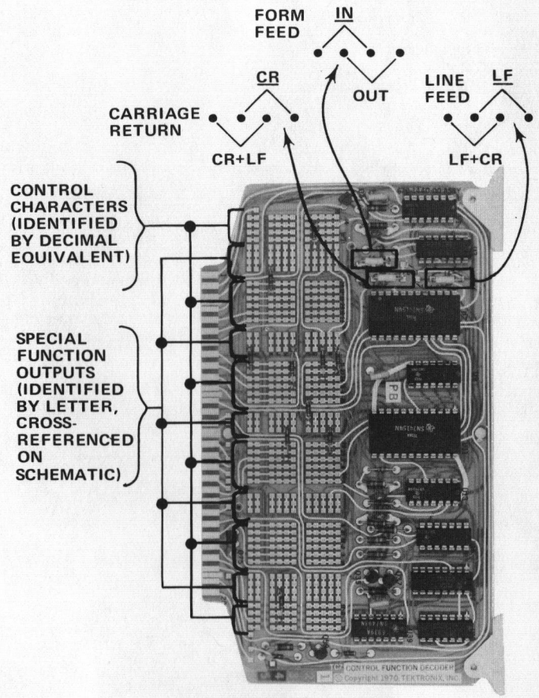
NAME	T	SOURCE	DEFINITION
SP STROB	P	TC4-28	Indication that next memory character has arrived in shift register
SPACCOMP	*P	TC12-19	X Register has arrived at new character position in the X axis
SPXMISTR	*P	TC5-24	Strobe accompanying Scratch Pad character during send operation
SP1	P	TC14-A	Scratch Pad character output bits
SP2	P	TC14-1	
SP3	P	TC14-2	
SP4	P	TC14-E	
SP5	P	TC14-F	
SP6	P	TC14-N	
SP7	P	TC14-7	
SP8	P	TC14-14	
STEP X	*P	TC18-4	Command to increment the X Register one point
STEP Y	*P	TC18-23	Command to increment the Y Register one point
STROBDLY	*P	TC11-17	Delay signal which permits loading of register before generating input strobe
STX	*P	TC7-Z	Control character
SUB	*P	TC7-6	Control character
SYN	*P	TC7-P	Control character
SYNCSTRB	P	TC19-20	Enabling command for loading address bytes into X and Y registers
TAB	*P	TC6-21	Horizontal Tab circuit command for advancing X Register one character space
TAB BSY	*L	TC6-18	Indication that the Horizontal Tab circuit is seeking the next tab position
TB1	P	TC11-J	Transmit bits
TB2	P	TC11-8	
TB3	P	TC11-7	
TB4	P	TC11-H	
TB5	P	TC11-Z	
TB6	P	TC11-AA	
TB7	P	TC11-CC	
TB8	P	TC11-BB	
TC INHIB	*L	J342-35	Signal from Auxiliary Unit which inhibits character execution
TCINSTRB	P	TC19-25	Strobe for processing characters within the Terminal
TTY	L	J101-32	Created by Keyboard switch being in TTY position
US	P	TC7-E	Control character used as an alphanumeric reset command and refreshed Scratch Pad command
VIEW	*P	TC1-16	Open collector signal for restoring viewing intensity to CRT
VIEW KY	*L	J102-17	Caused by Keyboard View key
VIEW LMP	*L	TC1-9	Drive signal for Keyboard View lamp
VT	*P	TC7-K	Control character
X AUX	P	J341-4	Analog output from X D/A circuit, indicative of X Register contents
X AUX GD	L	PWR SUP	Ground
X D/A	P	J152-6	Analog representation of X Register content; integrated during Linear Interpolate Mode
X ENABLE	P	TC18-Y	Enabling voltage for loading the X D/A latches
X GND	L	PWR SUP	Ground
XCURPULS	*P	TC1-CC	Stepping command for X Register, initiated by left or right directional shift key on Keyboard
XMIT RDY	L	TC19-13	Indication that Terminal has data for the Interface Unit
XMITCOMP	*P	J121-27	Indication that the Interface Unit has completed transmission of data

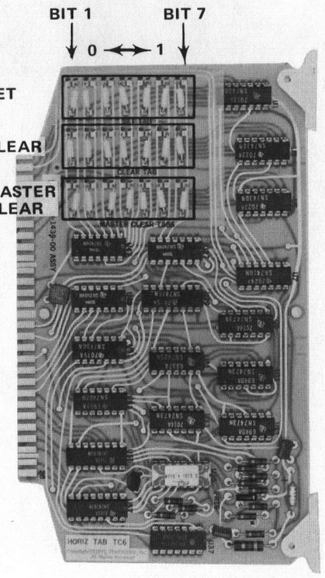
NAME	T	SOURCE	DEFINITION
Y AUX	P	J151-4	Analog output from Y D/A circuit, indicative of Y Register contents
Y AUX GD	L	PWR SUP	Ground
Y D/A	P	J151-6	Analog representation of Y Register content; integrated during Linear Interpolate Mode
Y ENABLE	P	TC18-Z	Enabling voltage for loading the Y D/A latches
Y GND	L	PWR SUP	Ground
YCURPULS	*P	TC1-FF	Stepping command for Y Register; initiated by up or down directional shift key on Keyboard
Y10	*P	TC16-27	Indication that Character Generator is scanning the tenth row of the matrix
Z	P	TC16-21	Point writing command
Z AUX	P	J341-24	Unblanking command to/from Auxiliary Unit
Z AUX GD	L	PWR SUP	Ground
Z ENABLE	P	TC15-EE	Point writing command from Character Generator
Z GND	L	PWR SUP	Ground
Z OUT	P	J153-4	Unblanking command to Display Unit connector
1 MHZ	P	TC2-27	Sub-multiple of 4 MHz internal clock
1X	*P	TC12-3	X and Y Register bits
1Y	*P	TC10-B	
128X	*P	TC12-8	
128Y	*P	TC10-H	
16X	*P	TC12-10	
16Y	*P	TC10-6	
2 MHZ	P	TC2-AA	Sub-multiple of 4 MHz internal clock
2X	*P	TC12-2	X and Y Register bits
2Y	*P	TC10-2	
256X	*P	TC12-7	
256Y	*P	TC10-L	
32X	*P	TC12-9	
32Y	*P	TC10-7	
4X	*P	TC12-4	
4Y	*P	TC10-5	
512X	*P	TC12-11	
512Y	*P	TC10-M	
64X	*P	TC12-6	
64Y	*P	TC10-9	
8X	*P	TC12-5	
8Y	*P	TC10-C	



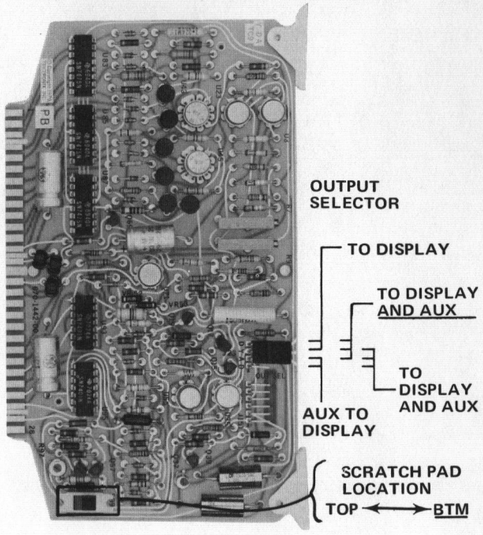
5-4 (A); TC-1



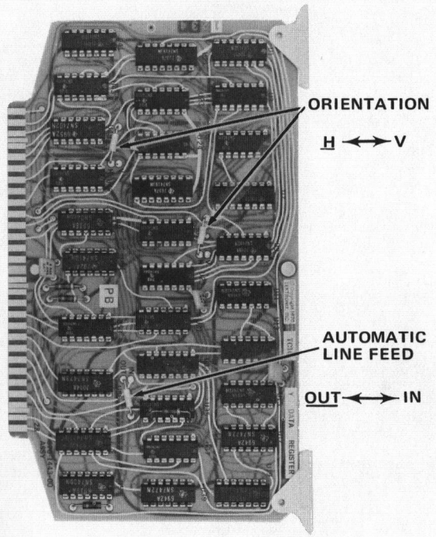
5-4 (C); TC-7



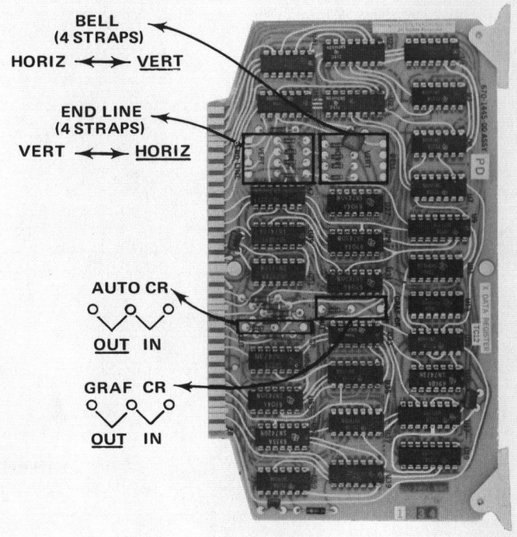
5-4 (B); TC-6



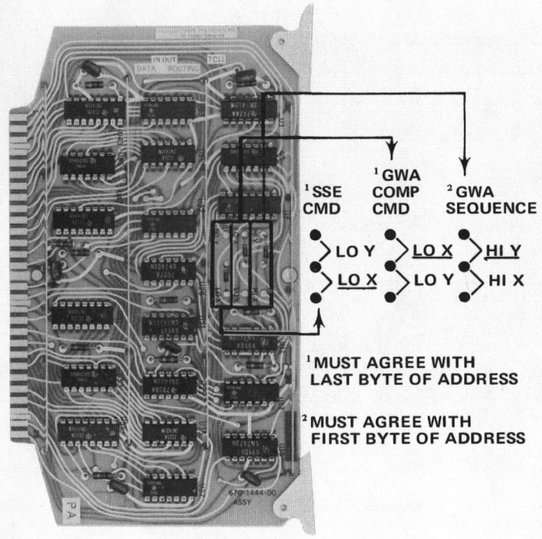
5-4 (D); TC-9



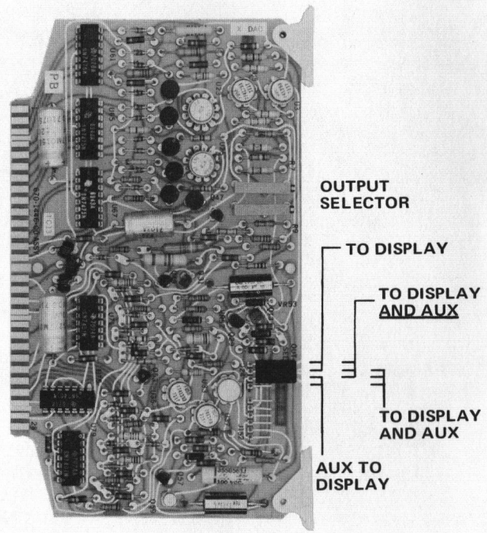
5-4 (E); TC-10



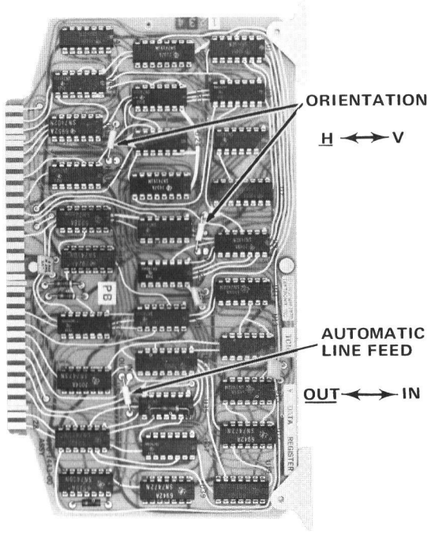
5-4 (G); TC-12



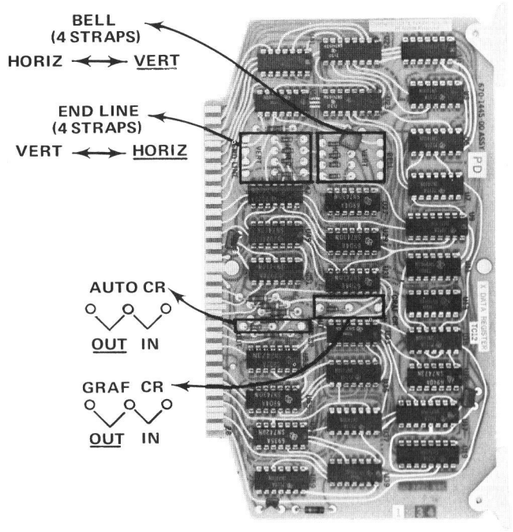
5-4 (F). TC-11



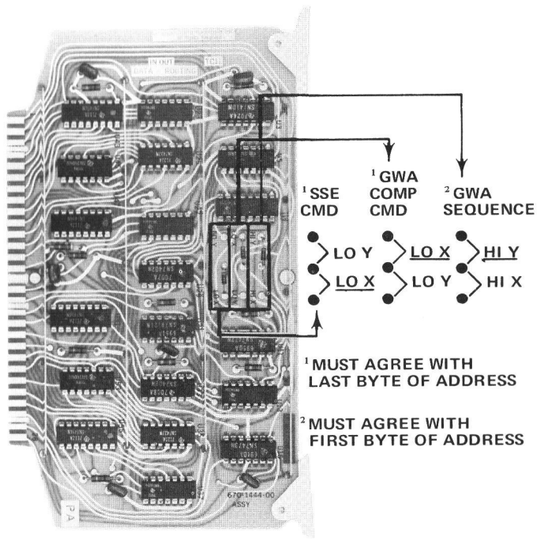
5-4 (H); TC-13



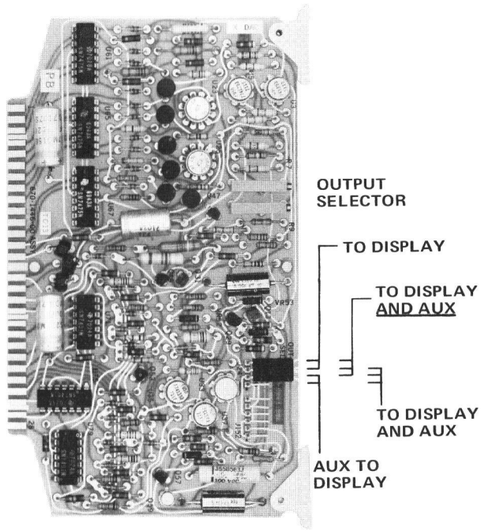
5-4 (E); TC-10



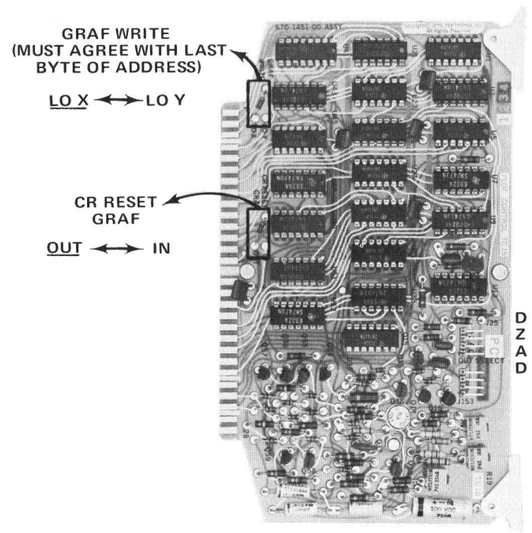
5-4 (G); TC-12



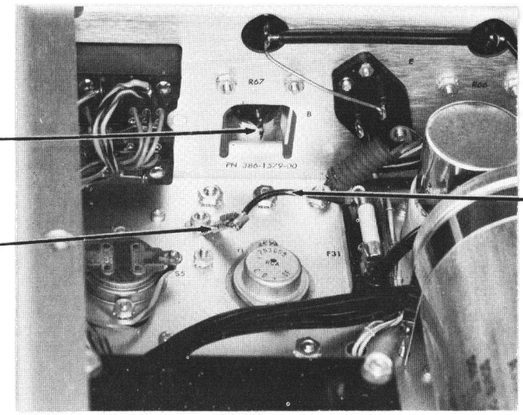
5-4 (F). TC-11



5-4 (H); TC-13



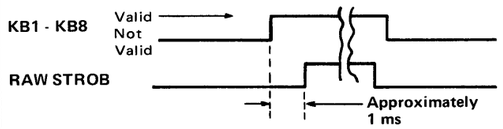
5-4 (I); TC-18



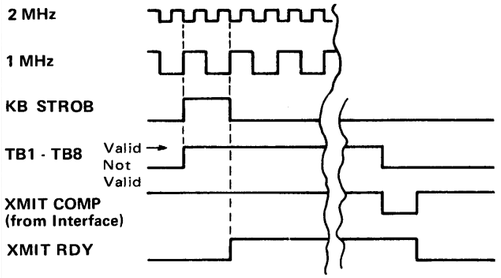
5-4 (J); Power Supply

Fig. 5-4. Strappable options. (Line selector not shown). Factory standard positions are underlined or specified.

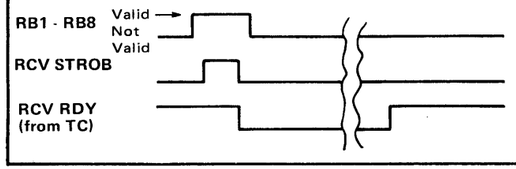
KEYBOARD TO TERMINAL CONTROL



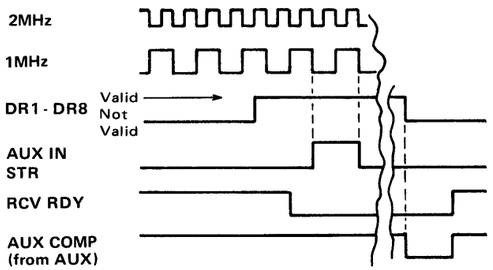
TERMINAL CONTROL TO INTERFACE UNIT



INTERFACE UNIT TO TERMINAL CONTROL



TERMINAL CONTROL TO AUXILIARY UNIT



AUXILIARY UNIT TO TERMINAL CONTROL

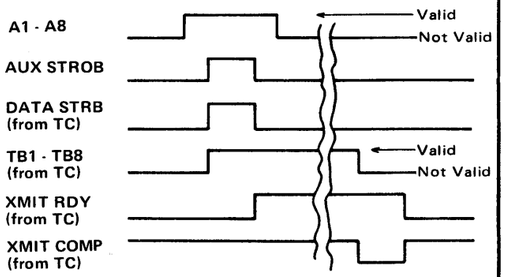
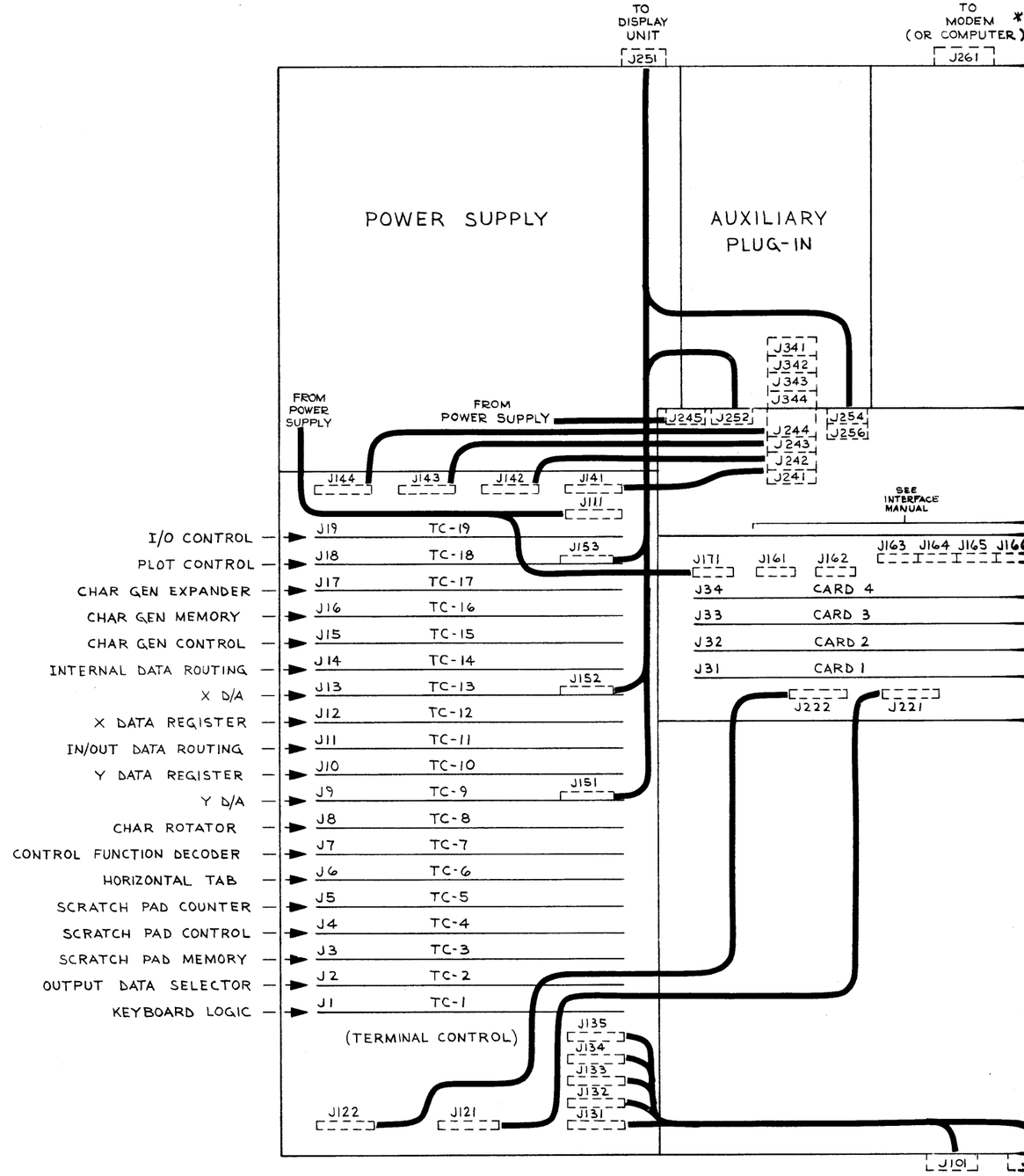
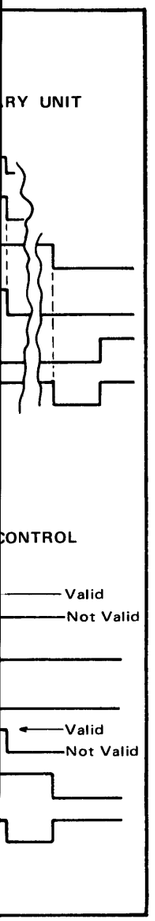
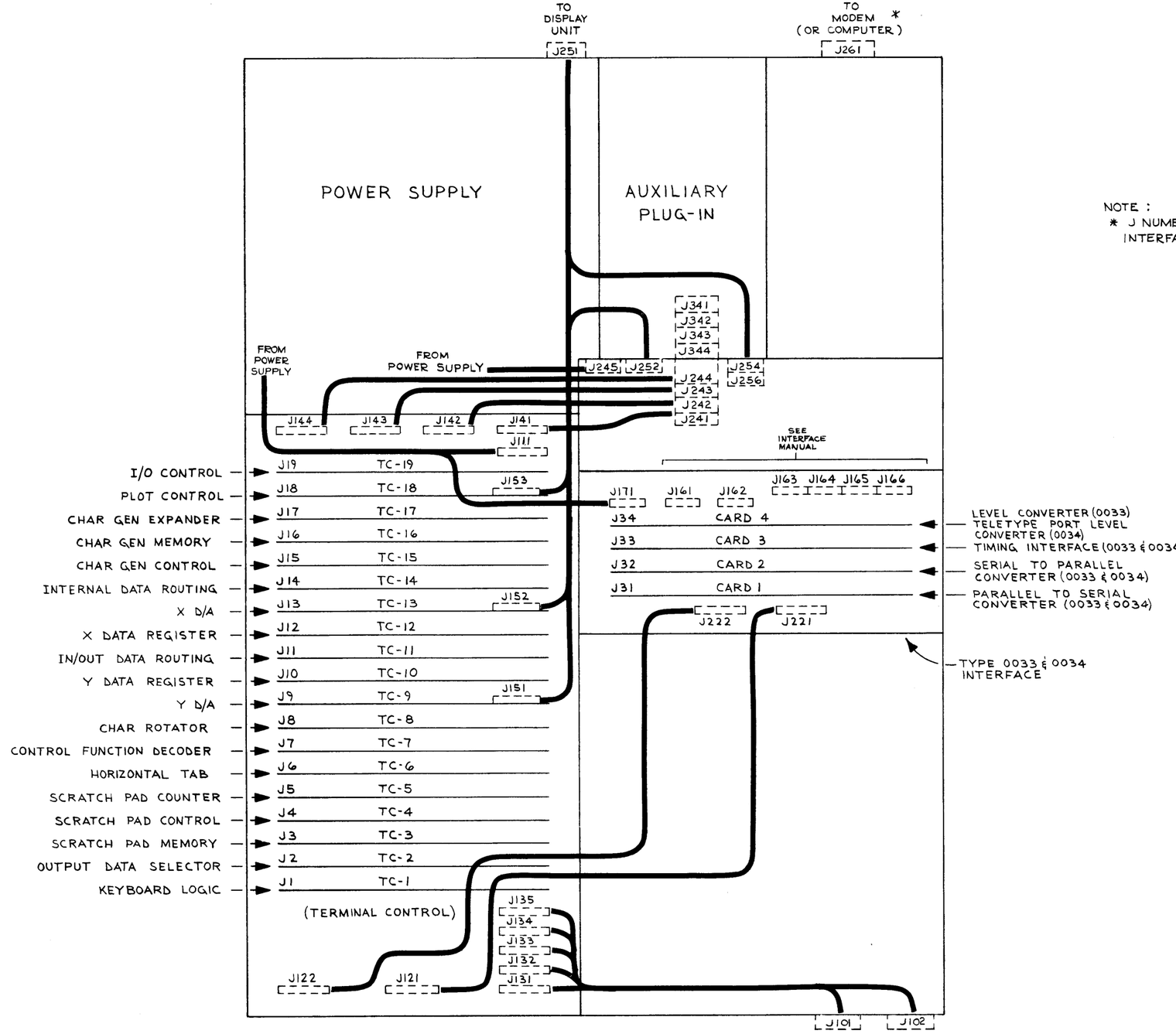


Fig. 5-2. Input/Output timing.

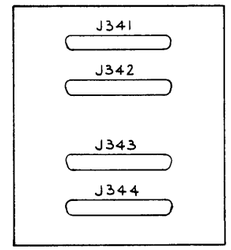


4002A DRAWER

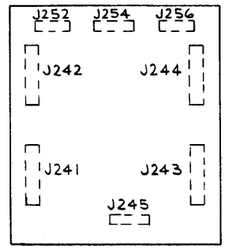




NOTE :
* J NUMBER VARIES WITH INTERFACE UNIT IN USE.



AUXILIARY UNIT OUTPUT CONNECTORS



AUXILIARY CONNECTOR BLOCK

4002A DRAWER

FIG 5-3 CONNECTORS

CONNECTOR WIRE LIST

NOTE

If the signal is input to Terminal Control through the connector, the connector is listed as being the source and all load points are listed. However, if the signal is output from Terminal Control, only the source is listed. All output signals have a fan out capability of at least one.

CODE: L = LEVEL P = PULSE S = SOURCE T = TYPE SIG

* = INDICATES LOW ACTIVE (ei., LE* = $\overline{LE}$)

J101 KEYBOARD CONNECTOR

PIN		NAME	T	CONN
1		+5V	L	PWR SUP
2		+5V	L	PWR SUP
3		GND	L	PWR SUP
4		GND	L	PWR SUP
5		LITE 1	L	J122 03
6		LITE 2	L	J122 07
7		-12V	L	PWR SUP
8		LITE 3	L	J122 15
9	S	KB8	P	J132 9
				TC01 1
10		LITE 4	L	J122 17
11	S	BREAK KY	*L	J134 2
				TC01 18
12				
13				
14		FULL LMP	*L	TC01 07
15	S	MGNSHFPB	*L	J135 2
				TC01 19
16	S	EDIT KY	*L	J135 3
				TC01 20
17	S	ON LINE	L	J121 28
				J135 10
				J144 33
				J342 13
				TC04 12
				TC11 14
				TC19 22
18	S	HOME KY	*L	J134 5
				TC01 E
19				
20				
21				
22				
23				
24	S	KB4	P	J133 8
				TC02 A
25	S	KB3	P	J133 7
				TC02 1
26	S	KB2	P	J134 4
				TC02 3
27	S	KB1	P	J132 10
				TC02 2
28	S	KB7	P	J133 6
				TC02 U
29	S	KB6	P	J132 7
				TC02 B
30	S	KB5	P	J132 8
				TC02 C
31	S	RAWSTROB	P	J134 7
				TC01 H
32	S	TTY	L	J135 9
				TC02 17
33		BEL SPKR	P	TC01 06
34	S	RPT KY	*L	J132 5
				TC01 B
35				
36	S	LOCAL	L	J122 34
				J135 1
37				

CONNECTOR WIRE LIST (cont)

J102 KEYBOARD CONNECTOR

PIN		NAME	T	CONN
1				
2				
3		EDIT LMP	*L	TC01 10
4	S	SEND KY	*L	J135 4
				TC01 21
5	S	INSERT	*L	J133 9
				TC04 8
				TC14 DD
6		SEND LMP	*L	TC01 08
7	S	COMP SW	*L	J134 8
				TC04 W
8	S	KEY SW	*L	J133 2
				TC01 C
9				
10				
11	S	FULL KY	*P	J134 9
				TC01 AA
12	S	CURRT KY	*L	J135 6
				TC01 25
13	S	CURDN KY	*L	J132 6
				TC01 BB
14				
15				
16		VIEW LMP	*L	TC01 09
17	S	VIEW KY	*L	J134 10
				TC01 T
18	S	ERASE KY	*L	J135 8
				TC01 28
19	S	CURLFTKY	*L	J135 7
				TC01 26
20	S	CURUP KY	*L	J135 5
				TC01 24
21				
22				
23				
24				
25				

J111 TERMINAL CONTROL POWER SUPPLY CONNECTOR

PIN	NAME	T	CONN
1	+15 V	L	PWR SUP
2	+5 V	L	PWR SUP
3	+5 V	L	PWR SUP
4	+5 V	L	PWR SUP
5	GND	L	PWR SUP
6	GND	L	PWR SUP
7	−15 V	L	PWR SUP

J121 INTERFACE CONNECTOR

PIN		NAME	T	CONN
1		PF LITE	L	TC10 20
2		KB STROB	P	TC02 2E
3		INITIAL	*L	TC01 0D
4		LTB	*P	TC07 0T
5		PAGEFULL	*P	TC10 BB
6		EOT	P	TC07 0V
7		TB7	P	TC11 CC
8		BREAK	*L	TC01 27
9		AUXPLTIO	*L	TC14 21
10	S	LE	*L	J143 4
				J343 27
				TC19 H
11				
12		RCV RDY	L	TC19 19
13		TB4	P	TC11 0H
14		HOME	*P	TC01 05
15		TB6	P	TC11 AA
16		TB5	P	TC11 0Z
17		TB2	P	TC11 08
18		SEND	*P	TC01 0Z
19		REFRSH	L	TC04 27 ①
20		PF PULSE	*P	TC10 DD
21		TB8	P	TC11 BB
22	S	CLRTOSND	L	J141 32
				J344 37
23	S	COMM ERR	*P	TC19 15
24				
25		IN AUX	*L	J341 19
26	S	LOADDATA	*P	J143 11
				J342 3C
				TC04 16
27	S	XMITCOMP	*P	J144 12
				J342 5
				TC02 22
				TC04 6
				TC19 C
28		ON LINE	L	J101 17
29		LI BUSY	*L	TC18 19
30		XMIT RDY	L	TC19 13
31				
32	S	KB ENABL	L	TC01 13
33	S	IOMGNSHF	*P	TC12 V
34	S	RCVSTROB	P	TC11 19
				TC19 AA

① Not connected on TC-0 number 670-1522-00.

®

CONNECTOR WIRE LIST (cont)

J122 INTERFACE CONNECTOR

PIN		NAME	T	CONN
1	S	SENDSCRN	*P	TC04 E
				TC05 5
				TC19 C
2		TB1	P	TC11 0J
3	S	LITE 1	L	J101 5
				J134 6
4		RS	P	TC07 0B
5		US	P	TC07 0E
6				
7	S	LITE 2	L	J101 6
				J132 2
8		1 MHZ	P	TC02 27
9		2 MHZ	P	TC02 AA
10	S	RB6	P	TC11 U
11	S	RB8	P	TC11 T
12	S	RB5	P	TC11 P
13	S	RB4	P	TC11 N
14				
15	S	LITE 3	L	J101 8
				J132 4
16	S	RB7	P	TC11 18
17	S	LITE 4	L	J101 10
				J132 3
18		SP SEND	*P	TC05 FF
19				
20		CAR RTN	P	TC07 15
21		FS	P	TC07 0F
22	S	PF RESET	*P	TC10 19
23		SEND	P	TC05 26
24				
25		FULL	*P	TC01 22
26		GS	P	TC07 0J
27		RING	*P	TC07 21
28				
29	S	RESETSND	*P	TC05 A
30		TB3	P	TC11 07
31	S	RB3	P	TC11 M
32	S	RB2	P	TC11 L
33	S	RB1	P	TC11 K
34		LOCAL	L	J101 36

J131 KEYBOARD CONNECTOR

PIN	NAME	T	CONN
1	GND	L	PWR SUP
2	GND	L	PWR SUP
3	−12V	L	PWR SUP
4	+5V	L	PWR SUP
5	+5V	L	PWR SUP

J132 KEYBOARD CONNECTOR

PIN	NAME	T	CONN
1	BEL SPKR	P	TC01 06
2	LITE 2	L	J122 07
3	LITE 4	L	J122 17
4	LITE 3	L	J122 15
5	RPT KY	*L	J101 34
6	CURDN KY	*L	J102 13
7	KB6	P	J101 29
8	KB5	P	J101 30
9	KB8	P	J101 09
10	KB1	P	J101 27

J133 KEYBOARD CONNECTOR

PIN	NAME	T	CONN
1	SEND LMP	*L	TC01 08
2	KEY SW	*L	J102 08
3	FULL LMP	*L	TC01 07
4			
5			
6	KB7	P	J101 28
7	KB3	P	J101 25
8	KB4	P	J101 24
9	INSERT	*L	J102 05
10			

CONNECTOR WIRE LIST (cont)

J134 KEYBOARD CONNECTOR

PIN	NAME	T	CONN
1	EDIT LMP	*L	TC01 10
2	BREAK KY	*L	J101 11
3	VIEW LMP	*L	TC01 09
4	KB2	P	J101 26
5	HOME KY	*L	J101 18
6	LITE 1	L	J122 03
7	RAWSTROB	P	J101 31
8	COMP SW	*L	J102 07
9	FULL KY	*P	J102 11
10	VIEW KY	*L	J102 17

J135 KEYBOARD CONNECTOR

PIN	NAME	T	CONN
1	LOCAL	L	J101 36
2	MGNSHFPB	*L	J101 15
3	EDIT KY	*L	J101 16
4	SEND KY	*L	J102 04
5	CURUP KY	*L	J102 20
6	CURRT KY	*L	J102 12
7	CURLFTKY	*L	J102 19
8	ERASE KY	*L	J102 18
9	TTY	L	J101 32
10	ON LINE	L	J101 17

J141 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	IN AUX	*L	J341 19
2			
3			
4	DC1	P	TC07 FF
5	NUL	*P	TC07 EE
6	DLE	P	TC07 DD
7	SOH	*P	TC07 25
8	DC3	P	PWR SUP
9	ETX	*P	TC07 AA
10	STX	*P	TC07 0Z
11	DC2	P	TC07 0Y
12	ACK	*P	TC07 20
13	SUB	*P	TC07 06
14	CAN	*P	TC07 08
15	LF	*P	TC07 05
16	NAK	P	TC07 0X
17	FS	P	TC07 0F
18	IN AUX	*L	J341 19
19	HOME	*P	TC01 05
20	REFRSH	L	TC04 27
21	SEND	*P	TC01 0Z
22			
23			
24			
25			
26			
27	CR	P	TC07 02
28	SI	*P	TC07 0D
29	RS	P	TC07 0B
30	SO	*P	TC07 0C
31			
32	CLRTOSND	L	J121 22
33	BS	*P	TC07 09
34	US	P	TC07 0E

CONNECTOR WIRE LIST (cont)

J142 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	BEL	*P	TC07 19
2	VT	*P	TC07 0K
3	AUXSTROB	P	J341 33
4	ESC	*P	TC07 0L
5	HT	*P	TC07 0M
6	IN KBAUX	L	J341 32
7			
8			
9			
10	ETB	*P	TC07 0T
11	A2	P	J341 28
12	A3	P	J341 27
13	A5	P	J341 26
14	EOT	P	TC07 0V
15	DC4	*P	TC07 0U
16	A6	P	J341 06
17	ENQ	P	TC07 0W
18	FF	*P	TC07 0H
19	GS	P	TC07 0J
20			
21	ALFA	L	TC18 09
22	A1	P	J341 18
23	EM	*P	TC07 0N
24	SYN	*P	TC07 0P
25	A4	P	J341 25
26	AUX Z	*P	J341 09
27	AUXPLOTY	*P	J343 21
28	FULL	*P	TC01 22
29			
30			
31			
32	DR1	P	TC11 10
33	A8	P	J341 08
34	A7	P	J341 07

J143 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	DR5	P	TC11 26
2	DR6	P	TC11 23
3	DR7	P	TC11 25
4	LE	*L	J121 10
5	XMIT RDY	L	TC19 13
6	RCV RDY	L	TC19 19
7	AUXINSTR	P	TC19 24
8	4Y	*P	TC10 05
9			
10	DR8	P	TC11 24
11	LOADDATA	*P	J121 26
12			
13	AUX COMP	*P	J341 14
14			
15	AUXPLOTX	*P	J343 19
16			
17			
18	DR4	P	TC11 12
19	DR3	P	TC11 11
20	DR2	P	TC11 09
21	2Y	*P	TC10 02
22	16Y	*P	TC10 06
23			
24	1Y	*P	TC10 0B
25	FUNCCOMP	P	TC02 CC
26	32Y	*P	TC10 07
27	64Y	*P	TC10 09
28	8Y	*P	TC10 0C
29	128Y	*P	TC10 0H
30	256Y	*P	TC10 0L
31	512Y	*P	TC10 0M
32			
33			
34			

CONNECTOR WIRE LIST (cont)

J144 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	512X	*P	TC12 11
2	256X	*P	TC12 07
3			
4	128X	*P	TC12 08
5	SP ERASE	*P	TC07 24
6	32X	*P	TC12 09
7	16X	*P	TC12 10
8	ERASINTV	*P	J251 07
9	8X	*P	TC12 05
10			
11			
12	XMITCOMP	*P	J121 27
13	GWA	L	TC11 13
14	INTENS 2	*L	J342 02
15	ERASE	*P	TC01 0V
16	HCU PRNT	*P	TC07 28
17	1 MHZ	P	TC02 27
18	TC INHIB	*L	J342 35
19			
20	PRNT BSY	*L	J251 10
21	64X	*P	TC12 06
22	AUX +Y	*P	J343 11
23	4X	*P	TC12 04
24	DATASTRB	P	TC02 21
25	1X	*P	TC12 03
26	2X	*P	TC12 02
27	AUX -X	*P	J343 03
28			
29	AUX PLOT	*L	J342 12
30	MCS DATA	*P	TC03 27
31	AUX PLT	*L	J342 08
32	AG	*L	J342 06
33	ON LINE	L	J101 17
34	VIEW	*P	TC01 16

J151 Y OUTPUT CONNECTOR

PIN		NAME	T	CONN
1	S	BUF Y GD	L	J252 9
				J341 20
2	S	BUFYLDR	P	J252 10
				J341 1
3		Y AUX GD	L	PWR SUP
4		Y AUX	P	J341 03
5		Y GND	L	PWR SUP
6	S	Y D/A	P	J251 15

J152 X OUTPUT CONNECTOR

PIN		NAME	T	CONN
1	S	BUF X GD	L	J252 7
				J341 21
2	S	BUFXLDR	P	J252 8
				J341 2
3		X AUX GD	L	PWR SUP
4		X AUX	P	J341 04
5		X GND	L	PWR SUP
6	S	X D/A	P	J251 1

J153 Z OUTPUT CONNECTOR

PIN		NAME	T	CONN
1		Z AUX GD	L	PWR SUP
2		Z AUX	P	J341 24
3		Z GND	L	PWR SUP
4	S	Z OUT	P	J251 4

J171 INTERFACE UNIT POWER CONNECTOR

PIN	NAME	T	CONN
1	POWER ON	L	PWR SUP
2	+5V	L	PWR SUP
3	-15V	L	PWR SUP
4	+15V	L	PWR SUP
5	GND	L	PWR SUP

CONNECTOR WIRE LIST (cont)

J245 AUXILIARY UNIT POWER CONNECTOR

PIN	NAME	T	CONN
1	+5V	L	PWR SUP
2	GND	L	PWR SUP
3	+15V	L	PWR SUP
4	-15V	L	PWR SUP

J251 DISPLAY UNIT CONNECTOR

PIN		NAME	T	CONN
1		X D/A	P	J152 06
2		X GND	L	PWR SUP
3		Y GND	L	PWR SUP
4		Z OUT	P	J153 04
5		Z GND	L	PWR SUP
6		SP ERASE	*P	TC07 24
7	S	ERASINTV	*P	J144 8
				J256 6
				J342 9
				TC19 FF
8		INTENS 2	*L	J342 02
9		INTENS 3	*L	J343 09
10	S	PRNT BSY	*L	J144 20
				J254 5
				J341 10
				TC10 27
				TC19 27
11				
12		HC GND	L	PWR SUP
13	S	H COPY	L	J254 3
				J343 2
14		X GND	L	PWR SUP
15		Y D/A	P	J151 06
16		Y GND	L	PWR SUP
17		Z GND	L	PWR SUP
18		ERASE	*P	TC01 0V
19		PRGM GND	L	PWR SUP
20		VIEW	*P	TC01 16
21		SEND	*P	TC01 02
22				
23				
24		HCU PRNT	*P	TC07 28
25		HC GND	L	PWR SUP

J252 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	Z AUX	P	J341 24
2	Z AUX GD	L	PWR SUP
3	X AUX GD	L	PWR SUP
4	X AUX	P	J341 04
5	Y AUX GD	L	PWR SUP
6	Y AUX	P	J341 03
7	BUF X GD	L	J152 01
8	BUFXLDR	P	J152 02
9	BUF Y GD	L	J151 01
10	BUFYLDR	P	J151 02

J254 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	SEND	*P	TC01 02
2	INTENS 3	*L	J343 09
3	H COPY	L	J251 13
4	HC GND	L	PWR SUP
5	PRNT BSY	*L	J251 10

J256 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	HCU PRNT	*P	TC07 28
2	ERASE	*P	TC01 0V
3	INTENS 2	*L	J342 02
4	VIEW	*P	TC01 16
5	SP ERASE	*P	TC07 24
6	ERASINTV	*P	J251 07

CONNECTOR WIRE LIST (cont)

J341 AUXILIARY CONNECTOR

PIN		NAME	T	CONN
1		BUFYLDR	P	J151 02
2		BUFXLDR	P	J152 02
3	S	Y AUX	P	J151 4
				J252 6
4	S	X AUX	P	J152 4
				J252 4
5		Z AUX GD	L	PWR SUP
6	S	A6	P	J142 16
				TC02 N
7	S	A7	P	J142 34
				TC02 16
8	S	A8	P	J142 33
				TC02 T
9	S	AUX Z	*P	J142 26
				TC18 AA
10		PRNT BSY	*L	J251 10
11		AUXINSTR	P	TC19 24
12				
13		1 MHZ	P	TC02 27
14	S	AUX COMP	*P	J143 13
				TC14 23
				TC19 A
15				
16				
17				
18	S	A1	P	J142 22
				TC02 F
19	S	IN AUX	*L	J121 25
				J141 1
				J141 18
				TC02 V

PIN		NAME	T	CONN
20		BUF Y GD	L	J151 01
21		BUF X GD	L	J152 01
22		Y AUX GD	L	PWR SUP
23		X AUX GD	L	PWR SUP
24	S	Z AUX	P	J153 2
				J252 1
25	S	A4	P	J142 25
				TC02 10
26	S	A5	P	J142 13
				TC02 11
27	S	A3	P	J142 12
				TC02 J
28	S	A2	P	J142 11
				TC02 H
29				
30				
31				
32	S	IN KBAUX	L	J142 6
				J341 34
32				TC02 18
33	S	AUXSTROB	P	J142 3
				TC02 19
34		IN KBAUX	L	J341 32
35		HOME	*P	TC01 05
36				
37		MOS DATA	*P	TC03 27

CONNECTOR WIRE LIST (cont)

J342 AUXILIARY CONNECTOR

PIN		NAME	T	CONN
1		SEND	*P	TC01 0Z
2	S	INTENS 2	*L	J144 14
				J251 8
				J256 3
				TC19 B
3		DR1	P	TC11 10
4		HCU PRNT	*P	TC07 28
5		XMITCOMP	*P	J121 27
6	S	AG	*L	J144 32
				TC19 28
7				
8	S	AUX PLT	*L	J144 31
9		ERASINTV	*P	J251 07
10				
11		VIEW	*P	TC01 16
12	S	AUX PLOT	*L	J144 29
				TC14 20
13		ON LINE	L	J101 17
14				
15		ERASE	*P	TC01 0V
16		GWA	L	TC11 13
17				
18		DATASTRB	P	TC02 21
19		SP ERASE	*P	TC07 24
20		DR7	P	TC11 25
21		DR4	P	TC11 12
22		DR3	P	TC11 11
23		DR2	P	TC11 09
24				
25		DR6	P	TC11 23
26		DR5	P	TC11 26
27		XMIT RDY	L	TC19 13
28		RCV RDY	L	TC19 19
29		DR8	P	TC11 24
30		LOADDATA	*P	J121 26
31				
32				
33				
34				
35	S	TC INHIB	*L	J144 18
				TC14 Z
36				
37				

J343 AUXILIARY CONNECTOR

PIN		NAME	T	CONN
1		HC GND	L	PWR SUP
2		H COPY	L	J251 13
3	S	AUX -X	*P	J144 27
				TC12 U
4		2X	*P	TC12 02
5		1X	*P	TC12 03
6				
7				
8		PRGM GND	L	PWR SUP
9	S	INTENS 3	*L	J251 9
				J254 2
10		4X	*P	TC12 04
11	S	AUX +Y	*P	J144 22
				TC10 V
12		32X	*P	TC12 09
13		64X	*P	TC12 06
14		128X	*P	TC12 08
15		256X	*P	TC12 07
16		512X	*P	TC12 11
17		16X	*P	TC12 10
18		8X	*P	TC12 05
19	S	AUXPLOTX	*P	J143 15
				TC12 16
20		REFRSH	L	TC04 27
21	S	AUXPLOTY	*P	J142 27
				TC10 T
22		ALFA	L	TC18 09
23		FULL	*P	TC01 22
24				
25		4Y	*P	TC10 05
26				
27		LE	*L	J121 10
28		2Y	*P	TC10 02
29		16Y	*P	TC10 06
30		1Y	*P	TC10 08
31		FUNCCOMP	P	TC02 CC
32		32Y	*P	TC10 07
33		64Y	*P	TC10 09
34		8Y	*P	TC10 0C
35		128Y	*P	TC10 0H
36		256Y	*P	TC10 0L
37		512Y	*P	TC10 0M

CONNECTOR WIRE LIST (cont)

J344 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	ACK	*P	TC07 20
2	SUB	*P	TC07 06
3	CAN	*P	TC07 08
4	LF	*P	TC07 05
5	FS	P	TC07 OF
6	NAK	P	TC07 0X
7	BS	*P	TC07 09
8	US	P	TC07 0E
9	SYN	*P	TC07 OP
10	FF	*P	TC07 0H
11	EM	*P	TC07 0N
12	VT	*P	TC07 0K
13	BEL	*P	TC07 19
14	ESC	*P	TC07 0L
15	HT	*P	TC07 0M
16	ETB	*P	TC07 0T
17	EOT	P	TC07 0V
18	DC4	*P	TC07 0U
19	ENQ	P	TC07 0W
20	GS	P	TC07 0J
21	DC2	P	TC07 0Y
22	STX	*P	TC07 0Z
23	ETX	*P	TC07 AA
24	DC3	P	PWR SUP
25	SOH	*P	TC07 25
26	DLE	P	TC07 DD
27	NUL	*P	TC07 EE
28	DC1	P	TC07 FF
29	CR	P	TC07 02
30	SI	*P	TC07 0D
31	RS	P	TC07 0B
32	SO	*P	TC07 0C
33	−15V	L	PWR SUP
34	+15V	L	PWR SUP
35	GND	L	PWR SUP
36	+5V	L	PWR SUP
37	CLR TO SND	L	J121 22

TC-3 CONNECTOR (J3)

PIN		NAME	T	CONN
A		MOS DATA	P	TC14 0W
R		GND	L	PWR SUP
S		+5V	L	PWR SUP
Y		MOS CLK	P	TC04 CC
14		+15V	L	PWR SUP
15		−15 V	L	PWR SUP
27	S	MOS DATA	*P	J144 30
				J341 37
				TC14 FF

TC-17 CONNECTOR (J17)

PIN	NAME	T	CONN
EE	CHAR EXEC	*P	TC14 0Y
H	DB1	P	TC14 0B
J	DB2	P	TC14 0C
K	DB3	P	TC14 0D
L	DB4	P	TC14 03
M	DB5	P	TC14 04
R	GND	L	PWR SUP
S	+5V	L	PWR SUP
T	DB7	P	TC14 08
U	DB6	P	TC14 0P
V	DB8	P	TC14 09
X	SCAN CLK	P	TC15 21
1	HOME	*L	TC01 05 ①
2	1Y	*P	TC10 0B ①
3	DC4	*P	TC07 0U ①
4	2Y	*P	TC10 02 ①
5	4Y	*P	TC10 05 ①
6	GRAF Z	P	TC18 08 ①
7	L1 BUSY	*P	TC18 19 ①
8	REFRSH	L	TC04 27 ①
14	+15V	L	PWR SUP
15	−15 V	L	PWR SUP
20	CG RESET	P	TC15 DD
22	E	*P	TC16 22
23	F	*P	TC16 23
24	G	*P	TC16 24
25	AGREE	*P	TC05 0V
26	ALFA 2	L	TC18 10
28	CHAR PROC	*P	TC16 28 ①

NOTE ① : Not connected on TC-0 number 670-1522-00.

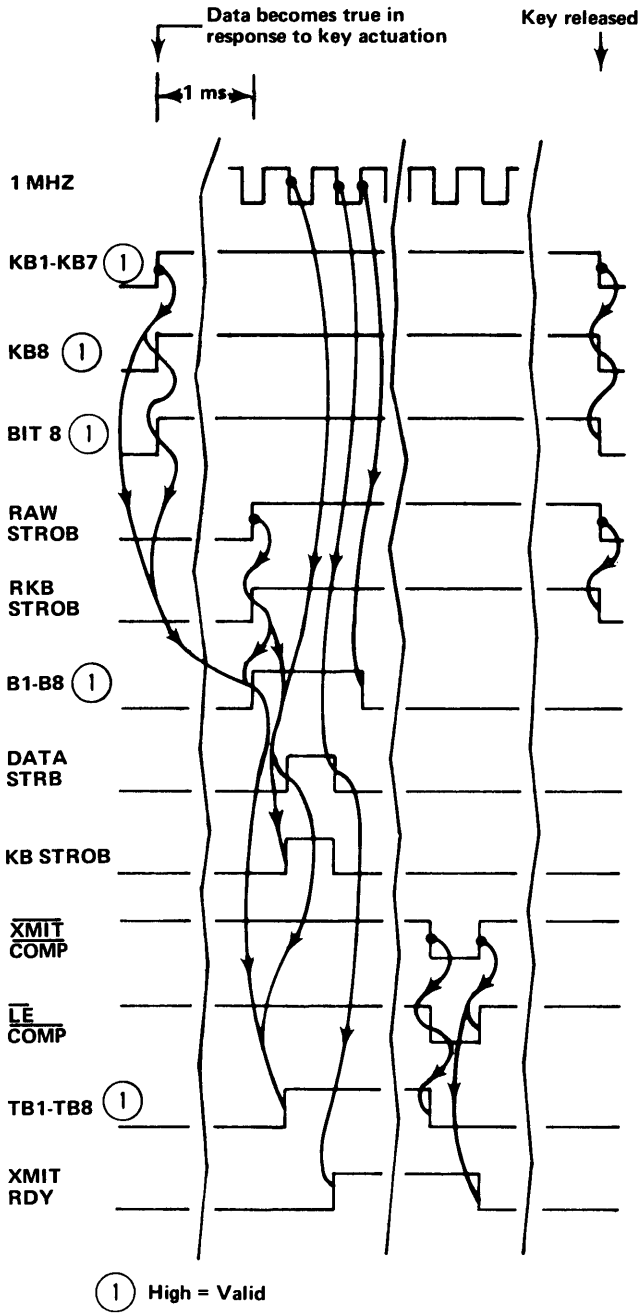


Fig. 5-5. Timing for transmitting Keyboard data.

BLOCK DIAGRAM DESCRIPTION

Transmitting—On Line-Direct; Echoing Not In Effect

General. In this mode, the Terminal converts keyboard characters to ASCII code and makes them available to the Interface Unit for transmission to the computer. The bits are accompanied by a strobe and a high transmit ready signal. When the computer accepts the bits, it causes the Interface Unit to return a transmit complete signal to permit additional transmission.

Description. Refer to the Block Diagram. When a character is entered at a Keyboard, the KB1 through KB7 lines receive bit information and transmit that information to TC-2. In standard factory configuration, KB8 is a parity bit. A selector in TC-1 permits odd or even parity to pass into TC-2 as bit 8, or it permits a mark or space to be selected. The data bits are followed by a RAW STROB signal which causes an audible click from the speaker. The RAW STROB also causes the RKB STROB signal to go to TC-2.

TC-2 sends the data bits to TC-11 via lines B1 through B8. TC-2 also sends a DATA STRB to TC-11 and TC-19. The DATA STRB causes the data bits to pass through TC-11, from where they are applied to the Interface Unit as TB1 through TB8. The DATA STRB into TC-19 causes XMIT RDY to go high, applying it to the Interface Unit. When the computer receives the data, it causes the Interface Unit to send an $\overline{\text{XMIT COMP}}$ signal to TC-19. TC-19 responds by setting the XMIT RDY line low, and sending an $\overline{\text{LE COMP}}$ signal to TC-11 to clear the latches. The circuit is then ready to transmit another character.

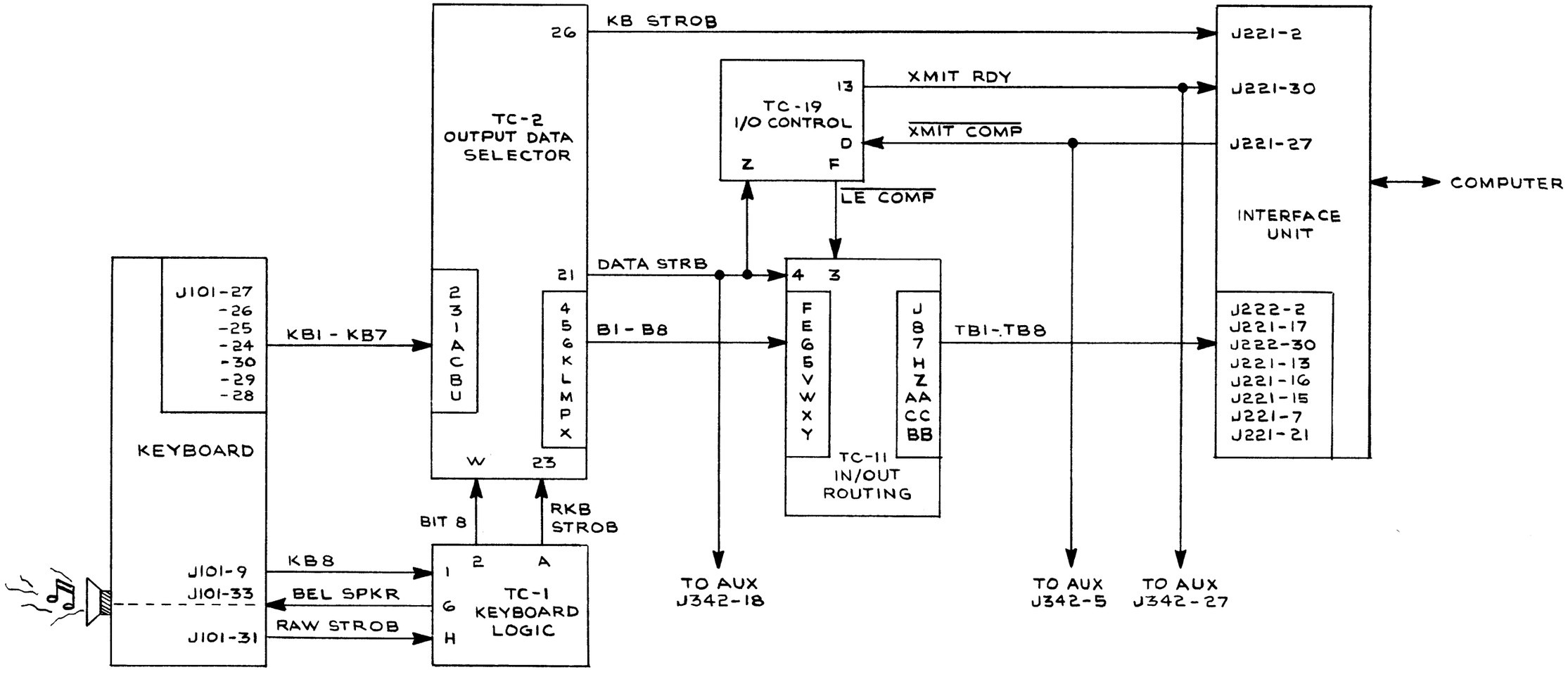
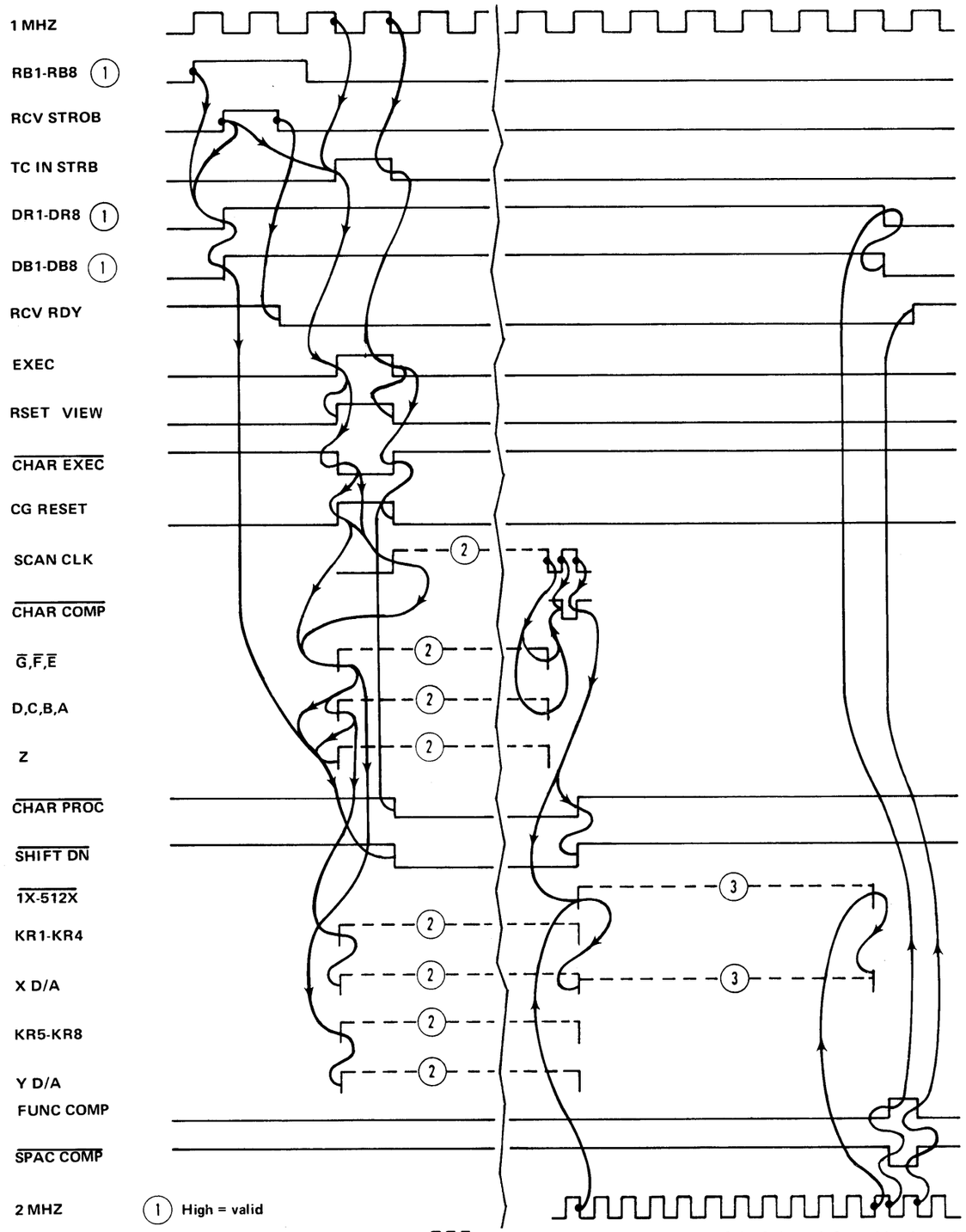


FIG 5-6
BLOCK DIAGRAM
TRANSMITTING
ON LINE - DIRECT 971 EKP

4002A DRAWER

Ⓐ

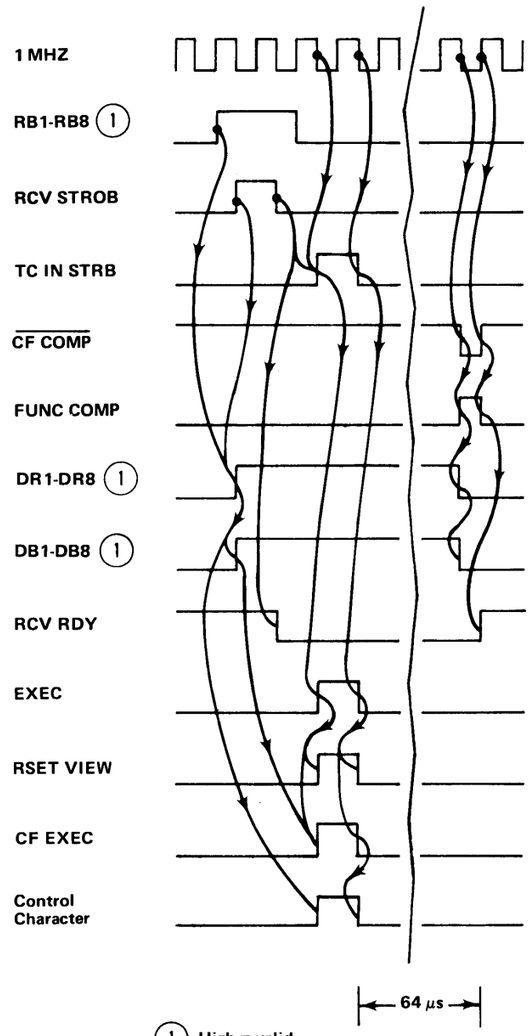


(1) High = valid

(2) During this time SCAN CLK causes G,F,E to count from 0 through 7 at each of the 0 through 9 combinations of D,C,B,A. Z indicates dots for each combination if ordered by DB1-DB8. KR1-KR4 and KR5-KR8 follow G,F,E, D,C,B,A. X D/A and Y D/A respond with 5 mV steps.

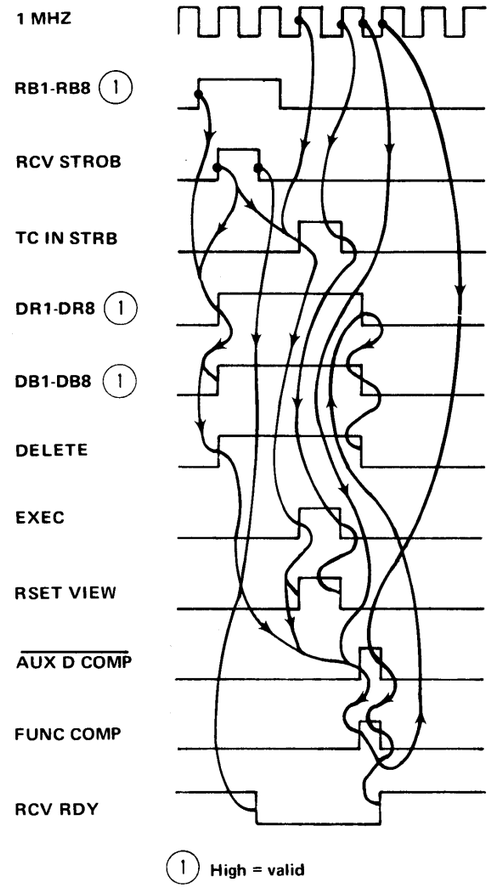
(3) 1X-512X increments 12 points (24 if dobule size is in effect) and X D/A increases by 5 mV for each point.

Fig. 5-7. Timing for Alphanumeric Mode; Written character processing.



(1) High = valid

Fig. 5-8. Alphanumeric Mode—Control Character processing (except DELETE).



(1) High = valid

Fig. 5-9. Timing for Alphanumeric Mode—Delete processing.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Alphanumeric Mode

The following principal functions occur in this mode: Data bits and a strobe are received from the computer; The Terminal puts a low on the RCV RDY line to inhibit inputs; The Terminal examines the data to determine what type of character has been received; The Terminal either executes a control character or writes a character; If it is a control character, a delay circuit is put into effect and the input circuits are reset after 64 μs; If it is a written character, writing is affected by the character generator, the X register is incremented to the next character writing position, and the input circuits are reset.

Refer to the On Line-Direct-Alphanumeric Mode block diagram. The Terminal receives data from the Interface Unit on the RB1 through RB8 lines, accompanied by a RCV STROB. In TC-19, RCV STROB causes RCV RDY to go low and generates a TC IN STRB for TC-4, TC-5, TC-6, and TC-18. In TC-11, the RCV STROB latches the data bits in to generate DR1 through DR8. Various combinations of these bits are applied to TC-4, TC-6, TC-7, TC-10, TC-12, TC-14, and TC-18.

TC-4 uses the TC IN STRB and DR1 through DR7 bits in conjunction with Scratch Pad operation. See the Scratch Pad description for details. TC-5 uses the TC IN STRB to generate an EXEC pulse for TC-14. TC-6 uses the TC IN STRB and the DR1 through DR8 bits for horizontal tab operation. See that circuit description for details. TC-10, TC-12, and TC-18 use the DR bits for graphics operation only.

In TC-14, EXEC generates $\overline{\text{CHAR EXEC}}$ if the bits contain a character to be written; it generates CF EXEC if the bits contain any control character except Delete. If the bits contain a Delete control character, a DELETE signal goes to TC-4 for Scratch Pad use; no $\overline{\text{CHAR EXEC}}$ or CF EXEC signals are generated, but a delayed 1/2 μs $\overline{\text{AUX D COMP}}$ pulse into TC-2 generates the FUNC COMP, which is used by the Scratch Pad in TC-4, clears the latches in TC-11, and resets RCV RDY in TC-19. TC-14 also converts the DR1 through DR8 bits to DB1 through DB8 bits, which are then made available to TC-16 for character generation.

Assume that a control character has been received in the RB1 through RB8 code. The CF EXEC latches the DR1 through DR5 bits into TC-7 and also starts a 64 μs $\overline{\text{CF COMP}}$ delay circuit. The control character is decoded and sent out to be utilized in any of the various circuits (such as to ring the bell). 64 μs after CF EXEC, $\overline{\text{CF COMP}}$ occurs. This goes to TC-2, where it generates a FUNC COMP which is sent to TC-4, TC-11, TC-19, and to the Auxiliary connectors.

In TC-4, the FUNC COMP signal is used during Scratch Pad Mode. (See the Scratch Pad description for details.) In TC-11, FUNC COMP clears the Input Latches. In TC-19, FUNC COMP resets the RCV RDY line high.

Now assume that a written character exists. $\overline{\text{CHAR EXEC}}$ strobes DB1 through DB8 into TC-16, and also generates a $\overline{\text{CHAR PROC}}$ signal there. $\overline{\text{CHAR EXEC}}$ also enters TC-15 to generate a CG RESET pulse to initialize the TC-16 circuits. TC-15 and TC-16 cause character writing. A zero through seven counting sequence occurs on the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines for each combination on the A, B, C, and D lines. Each discrete combination may or may not be accompanied by a Z command from TC-16, and a Z $\overline{\text{ENABLE}}$ command from TC-15. The A, B, C, D, E, F, and G signals go to TC-8, where they may or may not be rotated. (See TC-8 description.) If not rotated, A, B, C, and D emerge as KR5 through KR8 and go to TC-9 to modify the beam positioning voltage on the Y D/A and Y AUX lines; $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ go to TC-13 as KR2, KR3, and KR4 to modify the beam positioning voltage on the X D/A and X AUX lines. (KR1 is used only during character rotation.) The Z ENABLE signal goes to TC-18 to generate the Z OUT and/or Z AUX signals for beam unblanking.

The $\overline{\text{CHAR PROC}}$ signal which was generated by $\overline{\text{CHAR EXEC}}$ goes to TC-14, and TC-19. In TC-14 it inhibits $\overline{\text{CHAR EXEC}}$ and CF EXEC pulses. In TC-15 it inhibits cursor writing. In TC-19 it puts a low on the $\overline{\text{INTENS 2}}$ line. When the character generator finishes with the matrix, $\overline{\text{CHAR PROC}}$ goes high and a $\overline{\text{CHAR COMP}}$ pulse is sent to TC-12. In TC-12, it causes the $\overline{\text{1X}}$ through $\overline{\text{512X}}$ lines to increment 12 units (24 if a $\overline{\text{DBL SZ CHR}}$ signal is in effect). When finished, a $\overline{\text{SPAC COMP}}$ signal goes to TC-2 to generate FUNC COMP, which goes to TC-11 to clear the latches, and to TC-19 to reset the RCV RDY line high.

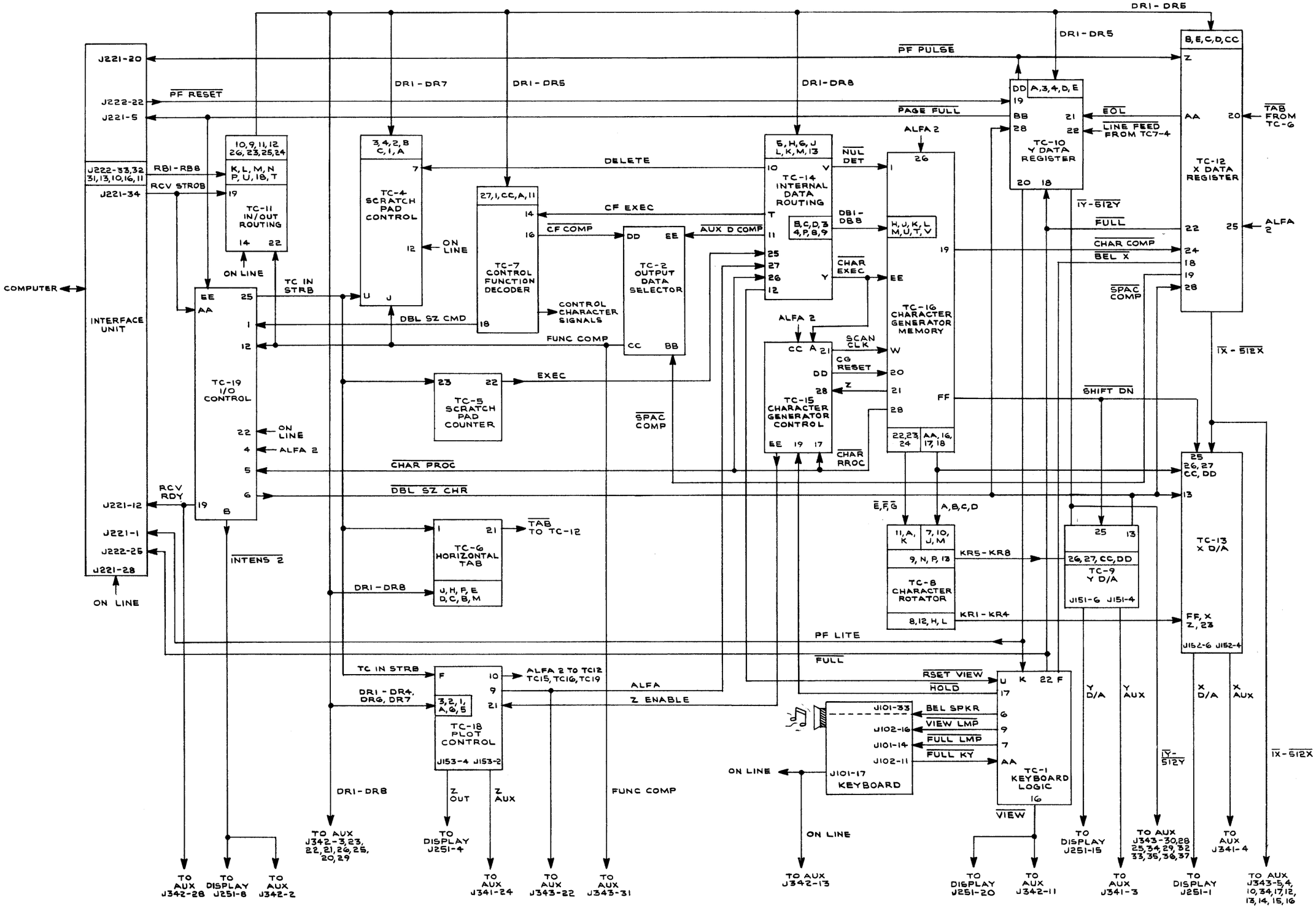
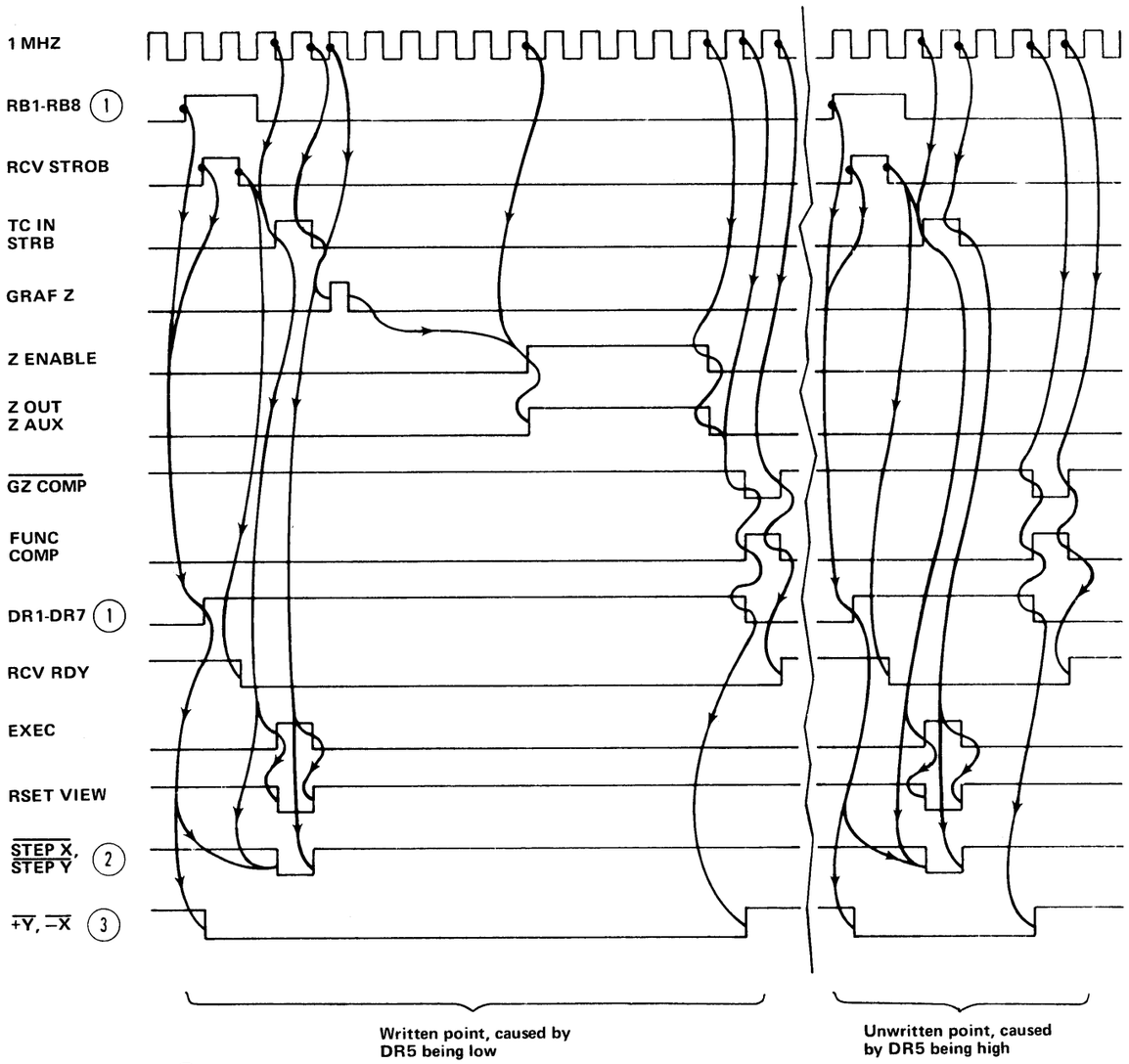


FIG 5-10
BLOCK DIAGRAM
RECEIVING IN ON LINE – DIRECT
ALPHANUMERIC MODE

4002A DRAWER



(1) High = valid

(2) STEP X and/or STEP Y occur whenever X and/or Y movement is commanded

(3) +Y and/or −X occur only when up and/or left movement is commanded

Fig. 5-11. Timing for Incremental Plot Mode.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Incremental Plot Mode

General. An RS command will switch the Terminal from Alphanumeric Mode to Incremental Plot Mode. Then the Terminal accepts single character commands and interprets them as a command to move one point in any of eight directions. Movement is accomplished by causing the X and/or Y registers to increment or decrement one point. Coding incorporated in the incoming character determines whether the point arrived at is written or unwritten.

Description. The RS command is received by TC-18, putting it into Incremental Plot Mode. GRAF 2 goes high and ALFA 2 goes low. GRAF 2 puts TC-10 into Graphics Mode. ALFA 2 puts TC-12 and TC-19 into Graphics Mode. ALFA 2 puts TC-15 into Graphics Mode, causing CG RESET to disable the Character Generator matrix generator. ALFA 2 goes to TC-16 to put it in Graphics Mode and hold the matrix at row 0, column 0.

The DR1, DR2, DR3, DR4, DR6, and DR7 bits from the next received character are applied to TC-18. There they cause a low to appear on either or both of the $\overline{\text{STEP X}}$ and $\overline{\text{STEP Y}}$ lines; in addition, this may be accompanied by a low on either $\overline{+Y}$ or $\overline{-X}$, or both. The $\overline{+Y}$ and $\overline{-X}$ outputs are direct functions of the DR1, DR2, and DR3 bits. The $\overline{\text{STEP X}}$ and $\overline{\text{STEP Y}}$ outputs are functions of the DR1, DR2, and DR3 bits in conjunction with the TC IN STRB. The $\overline{\text{STEP X}}$ and $\overline{\text{STEP Y}}$ signals go to TC-10 and TC-12 to cause movement of the registers one point in the direction commanded by the $\overline{+Y}$ and $\overline{-X}$ lines. Stepping actually occurs when the $\overline{\text{STEP X}}$ and/or $\overline{\text{STEP Y}}$ signals end.

The stepping is followed by a $\overline{\text{GZ COMP}}$ signal if DR4 is high, or by a 1/2 μs GRAF Z signal if DR4 is low. With DR4 high, the $\overline{\text{GZ COMP}}$ command goes to TC-2 to cause FUNC COMP. FUNC COMP zeroes the latches in TC-11 and resets RCV RDY high in TC-19.

With DR4 low, the GRAF Z pulse goes to TC-15 to cause a 5 μs wait followed by a 5 μs Z ENABLE pulse which goes to TC-18 to generate Z OUT. When Z ENABLE ends, it is followed by a 1 μs $\overline{\text{GZ COMP}}$ which goes from TC-18 to TC-2 to generate FUNC COMP. Again, FUNC COMP zeroes the latches in TC-11 and resets the RCV RDY line high in TC-19.

Control Characters. When a control character is received while in any graphic mode, it is detected on TC-11, causing $\overline{\text{GWA}}$ to go high. The combination of lows on DR6 and DR7 plus the high on $\overline{\text{GWA}}$ causes TC-18 to put a high on the ALFA line and disable the graphic circuits. This permits the control character to be executed as explained in Receiving in On Line-Direct-Alphanumeric Mode. However, the Terminal cannot execute control characters GS or RS while in Incremental Plot Mode. It must first be commanded into Alphanumeric Mode with a US (or a CR, if strapped).

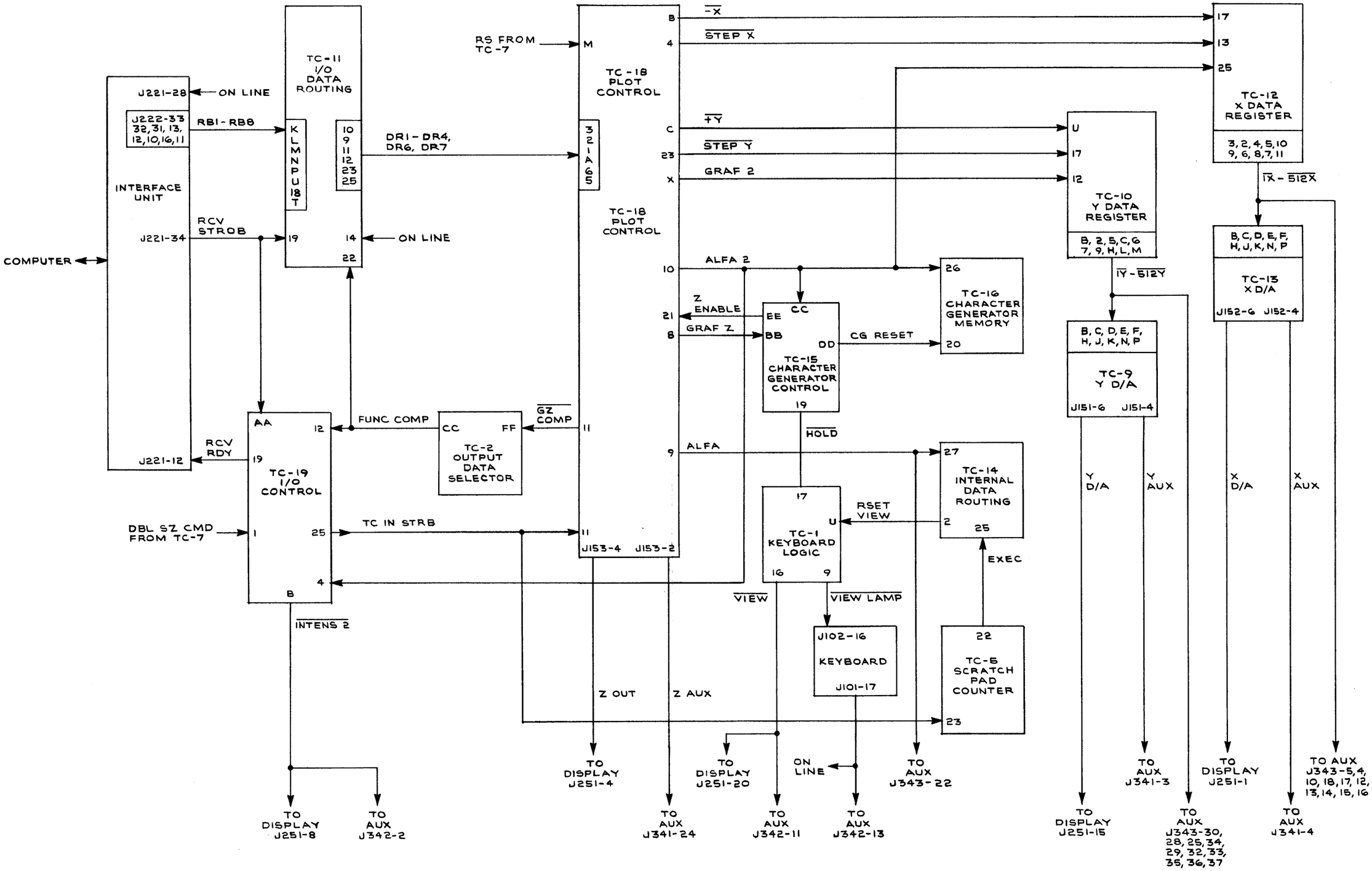
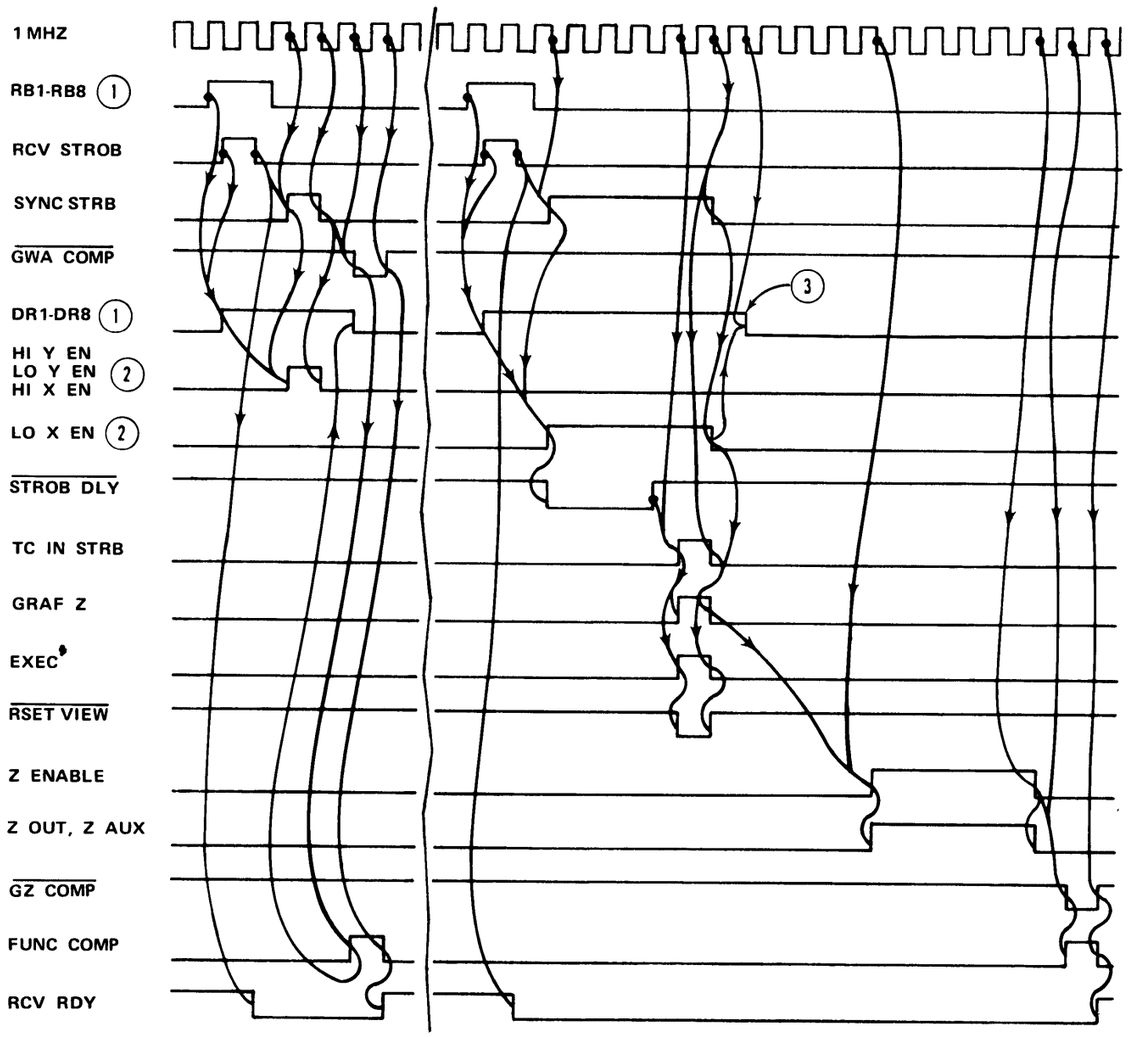


FIG 5-12
BLOCK DIAGRAM
RECEIVING IN ON LINE - DIRECT
INCREMENTAL PLOT MODE

4002A DRAWER



(1) High = valid

(2) Only one of these occurs in response to a specific RCV STROB, determined by DR6 and DR7. Under standard strap configuration they occur in high Y, low Y, high X, low X sequence.

(3) On TC-11 circuit cards 670-1444-00, DR1-DR8 go low at the beginning of FUNC COMP. On TC-11 circuit cards 670-1444-01, DR1-DR8 go low at end of LO X EN, without delay.

Fig. 5-13. Timing for Point Plot Mode. Straps set to write the point in response to a low X byte input.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Point Plot Mode

The Terminal goes into Point Plot Mode in response to receipt of Control Character FS. The five least significant incoming data bits can then be loaded directly into the X and Y registers to control register contents, thus controlling beam position. The registers are loaded by a four byte sequence in response to four input characters. The loading sequence is in accordance with the position of straps in TC-11 and TC-18. These straps are initially set for high Y, low Y, high X, and low X sequence. The Y bits are first loaded into the Y register to control the Y D/A output; then the X bits are loaded into the X register to control the X D/A output. After the last byte is received, the writing beam is unblanked and the point is written. After the point is written, the circuitry is reset to receive the next incoming character.

The Terminal must be in Alphanumeric Mode to receive the FS character which commands Point Plot Mode. Receipt of FS into TC-18 causes GS+FS to go to TC-11, where it enables the graphic word assembly circuitry. This causes GWA to go to TC-18 and $\overline{\text{GWA}}$ to go to TC-18 and TC-19. (Note: GWA and $\overline{\text{GWA}}$ are not direct complements of each other.) $\overline{\text{GWA}}$ into TC-19 presets the circuit for graphics.

When the 64 μs delay ends after receiving FS (see Alphanumeric Block Diagram Description), FUNC COMP goes from TC-2 to TC-19 to disable the TC IN STRB circuit.

In TC-18, the combination of GWA and $\overline{\text{GWA}}$ causes ALFA and ALFA 2 to go low and GRAF 2 to go high. (ALFA 2 and GRAF 2 are complements of each other.)

Now the circuit is set up for Point Plot operation. Assume that the sequence straps are as shown on the schematics, and that the computer will load the Terminal with four graphic bytes in the high Y, low Y, high X, low X sequence. The first byte arrives and is strobed into TC-11 by the RCV STROB. The resulting DR bits are sent to TC-10, TC-12, and TC-18. RCV STROB also goes to TC-19, where it causes RCV RDY to go low and generates a SYNC STRB for TC-11. In TC-11 the SYNC STRB causes HI Y EN to occur. HI Y EN goes to TC-10, where it loads the DR1 through DR5 bit information into the $\overline{\text{32Y}}$, $\overline{\text{64Y}}$, $\overline{\text{128Y}}$, $\overline{\text{256Y}}$, and $\overline{\text{512Y}}$ register positions, changing the Y D/A output. When SYNC STRB ends, so does the HI Y EN pulse. 1/2 μs later, a 1 μs $\overline{\text{GWA COMP}}$ pulse occurs and is sent to TC-2. The $\overline{\text{GWA COMP}}$ pulse causes TC-2 to generate a FUNC COMP pulse, which goes to TC-19 to reset the RCV RDY line high.

The next byte arrives and causes essentially the same action, except that TC-11 generates a LO Y EN pulse instead of a HI Y EN pulse. This causes the DR bits to load into the $\overline{\text{1Y}}$, $\overline{\text{2Y}}$, $\overline{\text{4Y}}$, $\overline{\text{8Y}}$, and $\overline{\text{16Y}}$ register positions. The third byte causes similar action, generating a HI X EN pulse in TC-11 to load the DR bits into the $\overline{\text{32X}}$, $\overline{\text{64X}}$, $\overline{\text{128X}}$, $\overline{\text{256X}}$, and $\overline{\text{512X}}$ register positions in TC-12. The fourth byte causes TC-11 to generate a LO X EN pulse to load $\overline{\text{1X}}$, $\overline{\text{2X}}$, $\overline{\text{4X}}$, $\overline{\text{8X}}$, and $\overline{\text{16X}}$ register positions in TC-12. The LO X EN pulse also goes to TC-18 to enable the GRAF Z circuit. On TC-11 circuit cards 670-1444-01 and above, the ending of the LO X EN pulse causes the data latches to clear, placing lows on the DR1-DR8 lines.

No $\overline{\text{GWA COMP}}$ pulse is generated by the fourth byte. Instead, a $\overline{\text{STROB DLY}}$ pulse goes to TC-19, where it causes the SYNC STRB to last about 100 μs. When STROB DLY ends, it causes a 1/2 μs TC IN STRB to be generated and ends the SYNC STRB. The TC IN STRB goes to TC-5 to generate an EXEC signal, and to TC-18 where it generates a GRAF Z signal. The EXEC signal from TC-5 goes to TC-14 to generate $\overline{\text{RSET VIEW}}$ for TC-1. TC-1 uses the signal to insure that $\overline{\text{VIEW LMP}}$ and $\overline{\text{HOLD}}$ are high and that $\overline{\text{VIEW}}$ is low. The GRAF Z signal from TC-18 goes to TC-15 to generate a Z ENABLE pulse. This goes to TC-18 to create a Z OUT pulse to write the point. When Z ENABLE ends, Z OUT ends and a 1 μs $\overline{\text{GZ COMP}}$ pulse goes from TC-18 to TC-2, where it generates FUNC COMP. As before, FUNC COMP resets the latches in TC-11 and resets the RCV RDY line in TC-19.

If the SSE CMD, GWA SEQ and GWA COMP CMD options in TC-11 and the GRAF WRITE option in TC-18 are set to accept a different byte sequence, essentially the same performance can be expected. Exceptions occur in the sequence in which the Y and X enable pulses (HI Y EN etc.) are generated.

Control Characters. If a control character is received by the Terminal, the low RB7 and RB6 cause $\overline{\text{GWA}}$ in TC-11 to go high. $\overline{\text{GWA}}$ goes to TC-18 to set ALFA high and to TC-19 to enable the TC IN STRB circuits. Subsequent action is essentially the same as explained in the Receiving—On Line-Direct-Alphanumeric Mode block diagram description. When the character is received and RCV RDY goes high, the Terminal returns to normal Point Plot Mode, with $\overline{\text{GWA}}$ low. RS cannot be executed while in Point Plot Mode. The Terminal must first be commanded into Alphanumeric Mode by a US (or a CR if strapped).

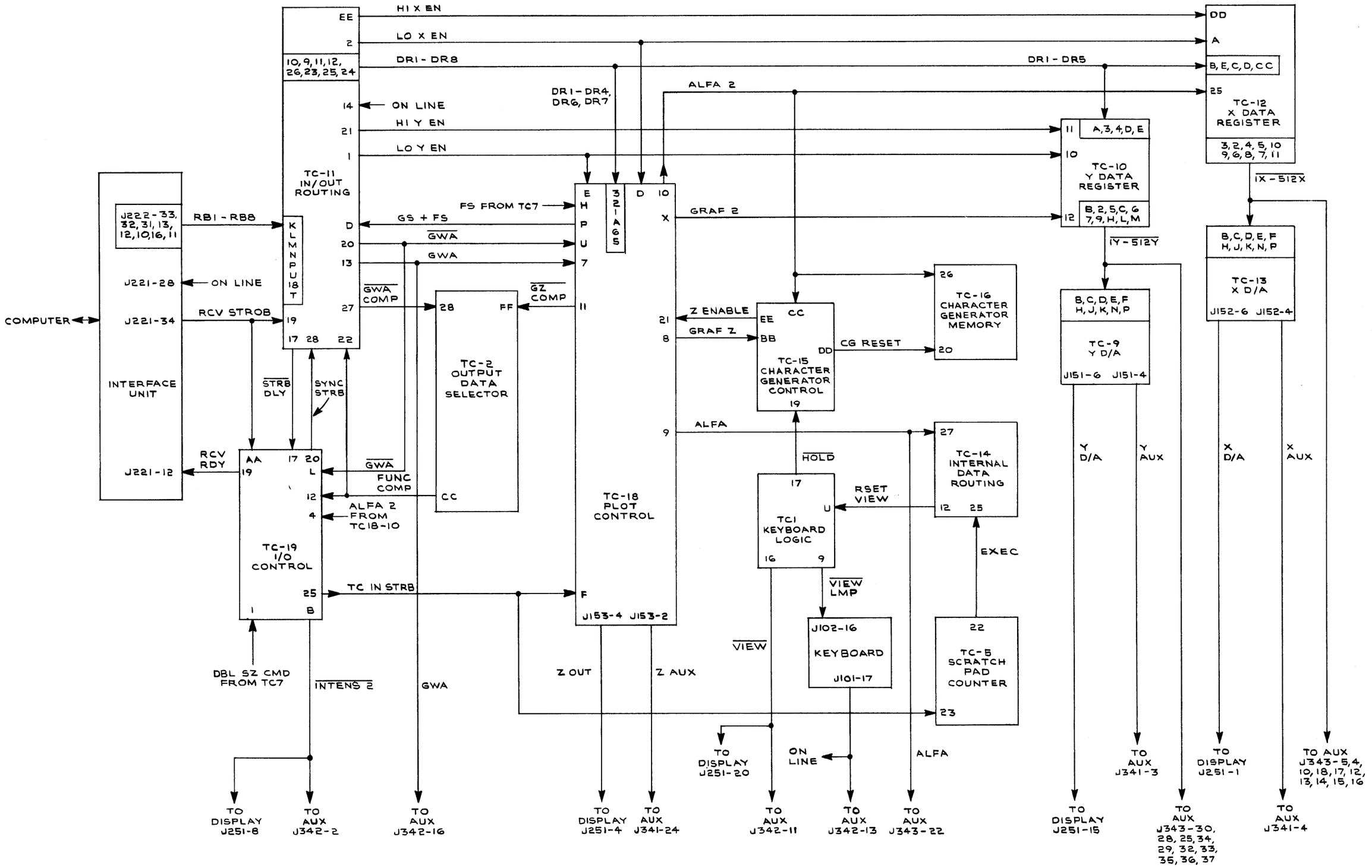
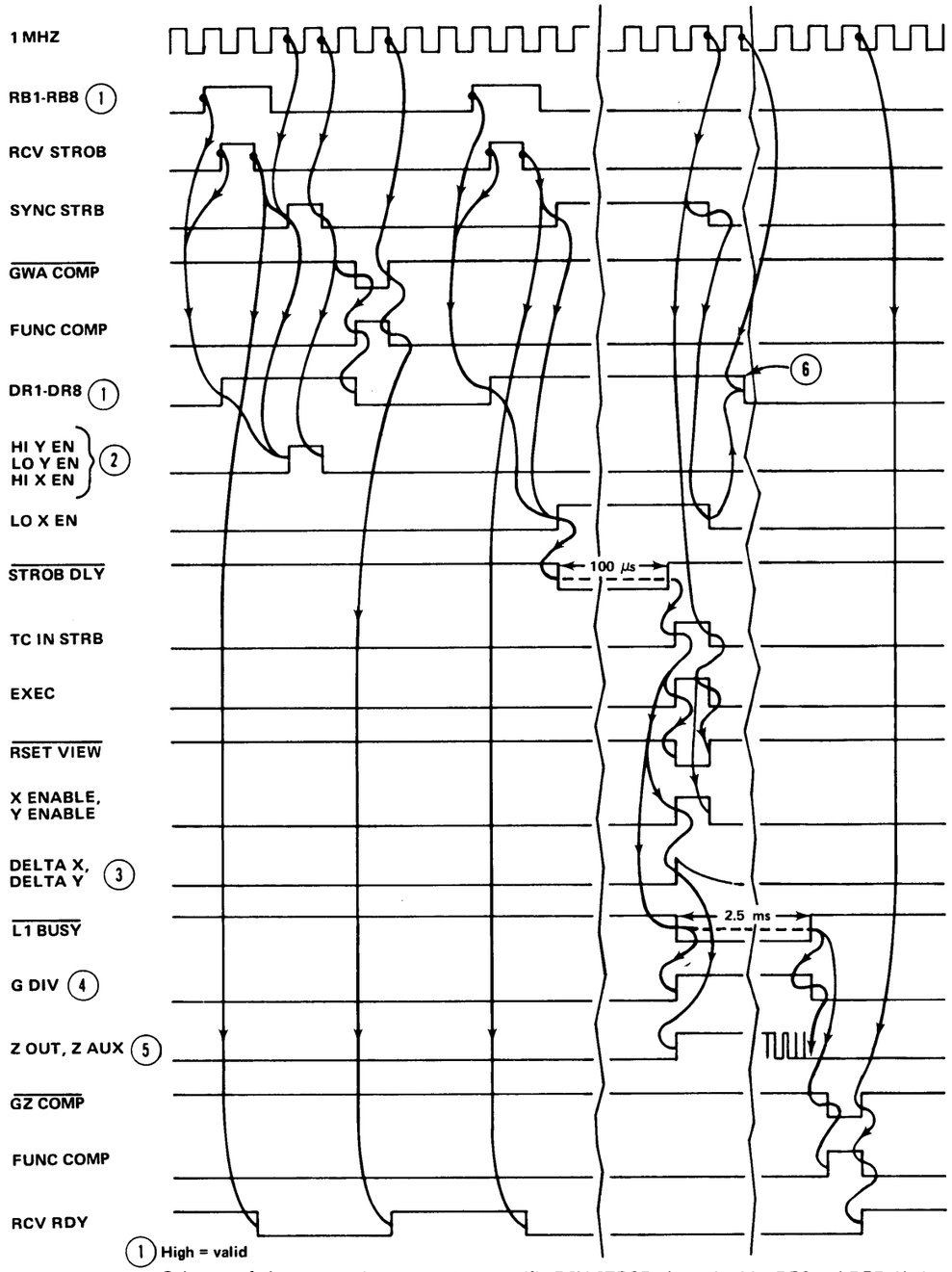


FIG 5-14
BLOCK DIAGRAM
RECEIVING IN ON LINE - DIRECT
POINT PLOT MODE



(1) High = valid

(2) Only one of these occurs in response to a specific RCV STROB; determined by DR6 and DR7. Under standard strap configuration they occur in high Y, low Y, high X, low X sequence.

(3) Amplitude, polarity and duration vary with vector length.

(4) Caused only by first vector following GS.

(5) Width varies with vector length. Does not occur in response to first vector following GS.

(6) On TC-11 circuit cards 670-1444-00, DR1-DR8 go low at the beginning of FUNC COMP. On TC-11 circuit cards 670-1444-01, DR1-DR8 go low at the end of LO X EN, without delay.

Fig. 5-15. Timing for Linear Interpolate Mode. Straps set to execute the vector in response to a low X byte input.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Linear Interpolate Mode

General. The Terminal must be in Alphanumeric Mode to receive the initializing GS control character. The five least significant bits of subsequent characters can then be loaded directly into the X an; Y registers to control their contents, thus controlling beam position. The registers are loaded in a four byte sequence in accordance with the straps in TC-11 and TC-18. Unless otherwise requested, these straps are factory-set for high Y, low Y, high X, low X sequence.

The Y bits are first loaded into the Y Register. Then the X bits are loaded into the X Register. After the last byte is received, the beam is moved to the new position. If it is the first address to follow a GS command, no unblanking occurs. Subsequent addresses have the beam unblanked during movement, causing a line to be drawn between the points. After arriving at the new point, the circuitry automatically resets to receive the next incoming character.

If subsequent dark vectors are to be drawn, an additional GS character can be entered immediately preceding the address while in Linear Interpolate Mode. The Terminal will return to Alphanumeric Mode upon receipt of a US command, or upon receipt of a CR command if the circuitry is strapped to accept it.

Description. Receipt by TC-18 of control character GS puts highs on GS+FS, GDLI, and GDIV. It also puts lows on X ENABLE and Y ENABLE. GS+FS goes to TC-11, where it enables the Graphic Word Assembly circuit. This causes GWA to go to TC-18 and $\overline{\text{GWA}}$ to go to TC-18 and TC-19. (GWA and $\overline{\text{GWA}}$ are not direct complements of each other.) $\overline{\text{GWA}}$ into TC-19 presets the circuit for graphics. The X ENABLE and Y ENABLE lines going low prevent the X and Y registers from affecting the X and Y D/A outputs.

When the 64 µs delay ends after receiving GS (see Alphanumeric Block Diagram Description), FUNC COMP goes from TC-2 to TC-19 to disable the TC IN STRB circuit. In TC-18, the combination of GWA and $\overline{\text{GWA}}$ causes ALFA and ALFA 2 to go low and GRAF 2 to go high. (ALFA 2 and GRAF 2 are complements of each other.)

Now the circuit is set up for Linear Interpolate operation. Assume that the sequence straps are as shown on the schematics, and that the computer will load the Terminal with four graphic bytes in the high Y, low Y, high X, low X sequence. The first byte arrives and is strobed into TC-11 by the RCV STROB. The resulting DR bits are sent to TC-10, TC-12, and TC-18. RCV STROB also goes to TC-19, where it causes RCV RDY to go low and generates a SYNC STRB for TC-11. In TC-11, the SYNC STRB causes HI Y EN to occur. HI Y EN goes to TC-10, where it loads the DR1 through DR5 bit information into the $\overline{\text{32Y}}$, $\overline{\text{64Y}}$, $\overline{\text{128Y}}$, $\overline{\text{256Y}}$, and $\overline{\text{512Y}}$ register positions. No effect is felt on the Y D/A output, because Y ENABLE is low. When SYNC $\overline{\text{STRB}}$ ends, so does the HI Y EN pulse. 1/2 µs later, a 1 µs $\overline{\text{GWA COMP}}$ pulse causes TC-2 to generate a FUNC COMP pulse. FUNC COMP goes to TC-19 to reset the RCV RDY line high, and to TC-11 to clear the data latches.

The next byte arrives and causes essentially the same action, except that TC-11 generates a LO Y EN pulse instead of a HI Y EN pulse. This causes the DR bits to load into the $\overline{\text{1Y}}$, $\overline{\text{2Y}}$, $\overline{\text{4Y}}$, $\overline{\text{8Y}}$, and $\overline{\text{16Y}}$ register positions. The third byte causes similar action, generating a HI X EN pulse in TC-11 to load the DR bits into the $\overline{\text{32X}}$, $\overline{\text{64X}}$, $\overline{\text{128X}}$, $\overline{\text{256X}}$, and $\overline{\text{512X}}$ register positions in TC-12. The fourth byte causes TC-11 to generate a LO X EN pulse to load $\overline{\text{1X}}$, $\overline{\text{2X}}$, $\overline{\text{4X}}$, $\overline{\text{8X}}$, and $\overline{\text{16X}}$ register positions in TC-12. In TC-11 circuit cards 670-1444-01 and above, DR1-DR8 return low after LO X EN ends.

No $\overline{\text{GWA COMP}}$ pulse is generated by the fourth byte. Instead, a $\overline{\text{STROB DLY}}$ pulse goes to TC-19, where it causes the SYNC STRB to last about 100 µs. When $\overline{\text{STROB DLY}}$ ends, it causes a 1/2 µs TC IN STRB to be generated and ends the SYNC STRB. The TC IN STRB goes to TC-5 to generate an EXEC signal, and to TC-18 where it performs several functions. The EXEC signal from TC-5 goes to TC-14 to generate $\overline{\text{RSET VIEW}}$ for TC-1. TC-1 uses the signal to insure that $\overline{\text{VIEW LMP}}$ and $\overline{\text{HOLD}}$ are high, and that $\overline{\text{VIEW}}$ is low.

The TC IN STRB into TC-18 generates high X ENABLE and Y ENABLE pulses, and a low $\overline{\text{LI BUSY}}$ pulse. The X ENABLE and Y ENABLE pulses go to TC-13 and TC-9 respectively, to load the X and the Y Data Register information into the D/A circuits. With GDIV in effect (as occurs for the first address after each GS command), the D/A circuit outputs change rapidly.

When TC IN STRB ends, X ENABLE and Y ENABLE end. A brief time later $\overline{\text{LI BUSY}}$ goes high and GDIV goes low. GDIV then remains low until another GS command is received to command the vector to be dark. When $\overline{\text{LI BUSY}}$ goes high, it causes TC-18 to generate a 1 µs $\overline{\text{GZ COMP}}$ pulse. This goes to TC-2 to generate FUNC COMP, which goes to TC-11 to clear the latches and to TC-19 to reset the RCV RDY line.

When the first address after the GS is executed, the GDIV line goes low and remains there. The next address

receives essentially the same treatment as just explained except that with GDIV low, the data latched into the Y and X D/A circuits (by X ENABLE and Y ENABLE) is confronted by an integrating time constant. The DELTA Y and DELTA X outputs are sent back to TC-18, where the larger of the two amplitudes controls the Z OUT pulse, which unblanks the writing beam. Therefore, the movement from the old to the new address occurs slower than the first (dark) one to follow GS, and the beam is unblanked to permit it to be written. With GDIV low, a 2.5 ms (nominal) timing circuit is put into effect in TC-18, causing the $\overline{\text{LI BUSY}}$ pulse to be of that duration.

If the SSE CMD, GWA SEQ, and GWA COMP CMD options in TC-11 and the GRAF WRITE option in TC-18 are set to accept a different byte sequence, essentially the same performance can be expected. Exceptions occur in the sequence in which the Y and X loading pulses (HI Y EN, etc.) are generated.

Control Characters. If a control character is received by the Terminal, the low RB7 and RB6 cause $\overline{\text{GWA}}$ in TC-11 to go high. $\overline{\text{GWA}}$ goes to TC-18 to set ALFA high and to TC-19 to enable the TC IN STRB circuits. Subsequent action is essentially the same as explained in the Receiving—On Line-Direct-Alphanumeric Mode block diagram description. When the character is received and RCV RDY goes high, the Terminal returns to normal Linear Interpolate Mode, with $\overline{\text{GWA}}$ low.

RS and FS cannot be executed while in Linear Interpolate Mode. The Terminal must first be commanded into Alphanumeric Mode by a US (or a CR, if strapped).

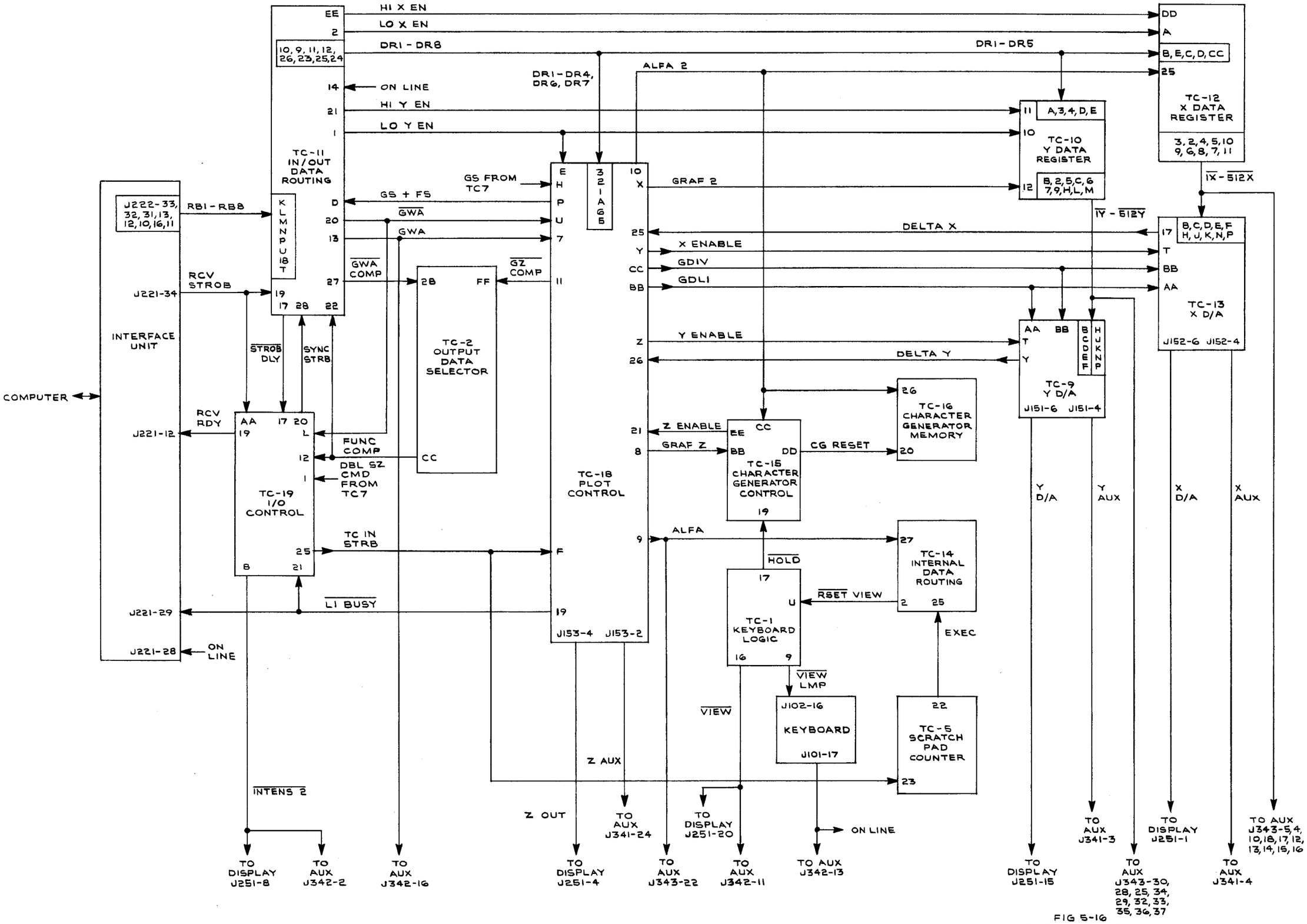


FIG 5-16
BLOCK DIAGRAM
RECEIVING IN ON LINE - DIRECT
LINEAR INTERPOLATE MODE

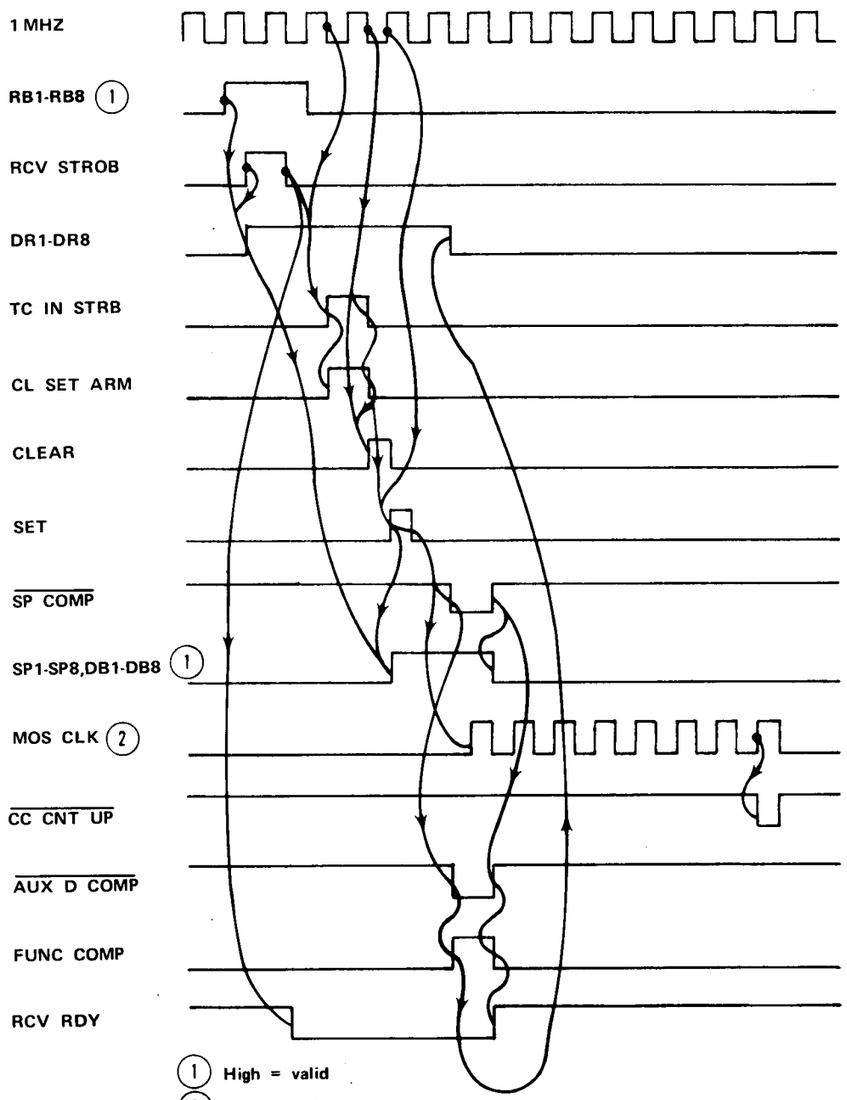


Fig. 5-17. Timing for receiving data in Unrefreshed Mode.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Unrefreshed Scratch Pad Mode

General. In this mode, the Scratch Pad Memory circuit is loaded from the Interface Unit, without displaying the characters on the screen. This permits more rapid reception of a block which can be checked before being displayed. Checking is done by circuitry in the Interface Unit.

Description. When a RCV STROB brings in data bits containing Escape character, the DR1 through DR7 bits are decoded in TC-4 where they arm the Scratch Pad control circuitry. (The same effect can be obtained by sending $\overline{\text{SP ARM}}$ in from TC-7. $\overline{\text{SP ARM}}$ is strappable in TC-7 so that it can be controlled by any control character.) If the next character sent to the Terminal is a US, TC-7 decodes it and sends it to TC-4 where it puts the Terminal in Unrefreshed Scratch Pad Mode. COMPOSE goes high and $\overline{\text{COMPOSE}}$ goes low. $\overline{\text{COMPOSE}}$ goes to TC-1 to disable the bell. COMPOSE goes to numerous circuit cards to establish Scratch Pad operation.

The next character is strobed into TC-11 by the RCV STROB, and the DR bits are routed to TC-4. The RCV STROB also causes TC-19 to put a low on the RCV RDY line, and to generate the TC IN STRB signal for TC-4. TC-4 produces a CL SET ARM signal, and presets the CC CNT UP circuit. The CL SET ARM signal causes TC-5 to produce a 1/2 μs CLEAR signal followed by a 1/2 μs SET signal. CLEAR goes to TC-14 to insure that the shift register is empty, and then SET loads the DR bits. (The bits become available on the DV lines to TC-16 and the SP lines to TC-2, but are not used at this time.)

SET also goes to TC-4. When it ends, TC-4 sends a 1 μs $\overline{\text{SP COMP}}$ pulse and 8 MOS CLK pulses to TC-14. The $\overline{\text{SP COMP}}$ generates an $\overline{\text{AUX D COMP}}$ signal which goes to TC-2 to generate FUNC COMP, which goes to TC-11 to clear the latches and to TC-19 to reset RCV RDY high. The eight MOS CLK pulses serially shift the inserted character into the memory, removing them from the DB and SP lines. TC-4 also sends a $\overline{\text{CC CNT UP}}$ to TC-5 to increment the cursor counter register, and an $\overline{\text{SP EXEC}}$ to TC-5 to increment the position counter. When the Scratch Pad memory is fully loaded, KSE goes low to inhibit KB entry, although no such restraint is put on inputs from the computer.

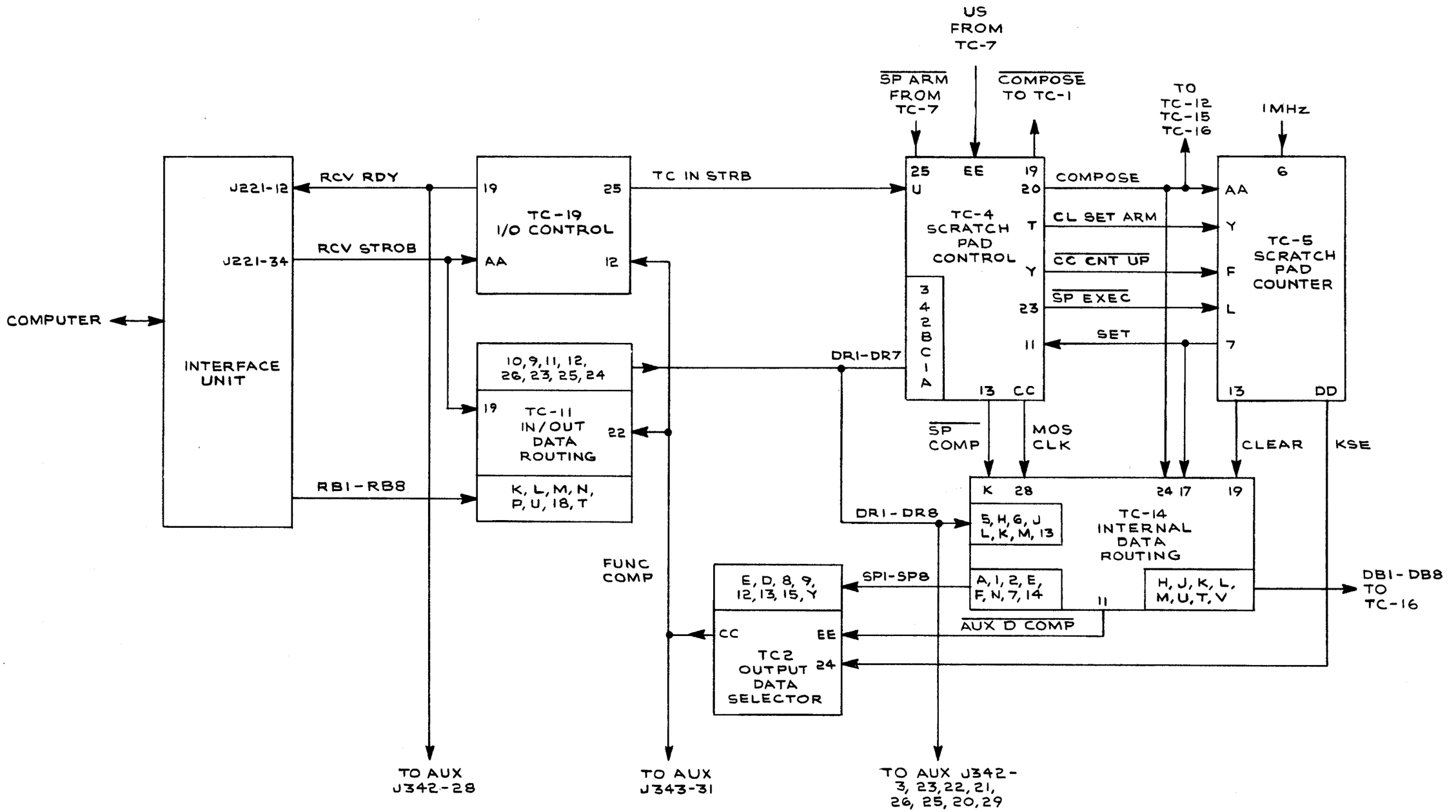
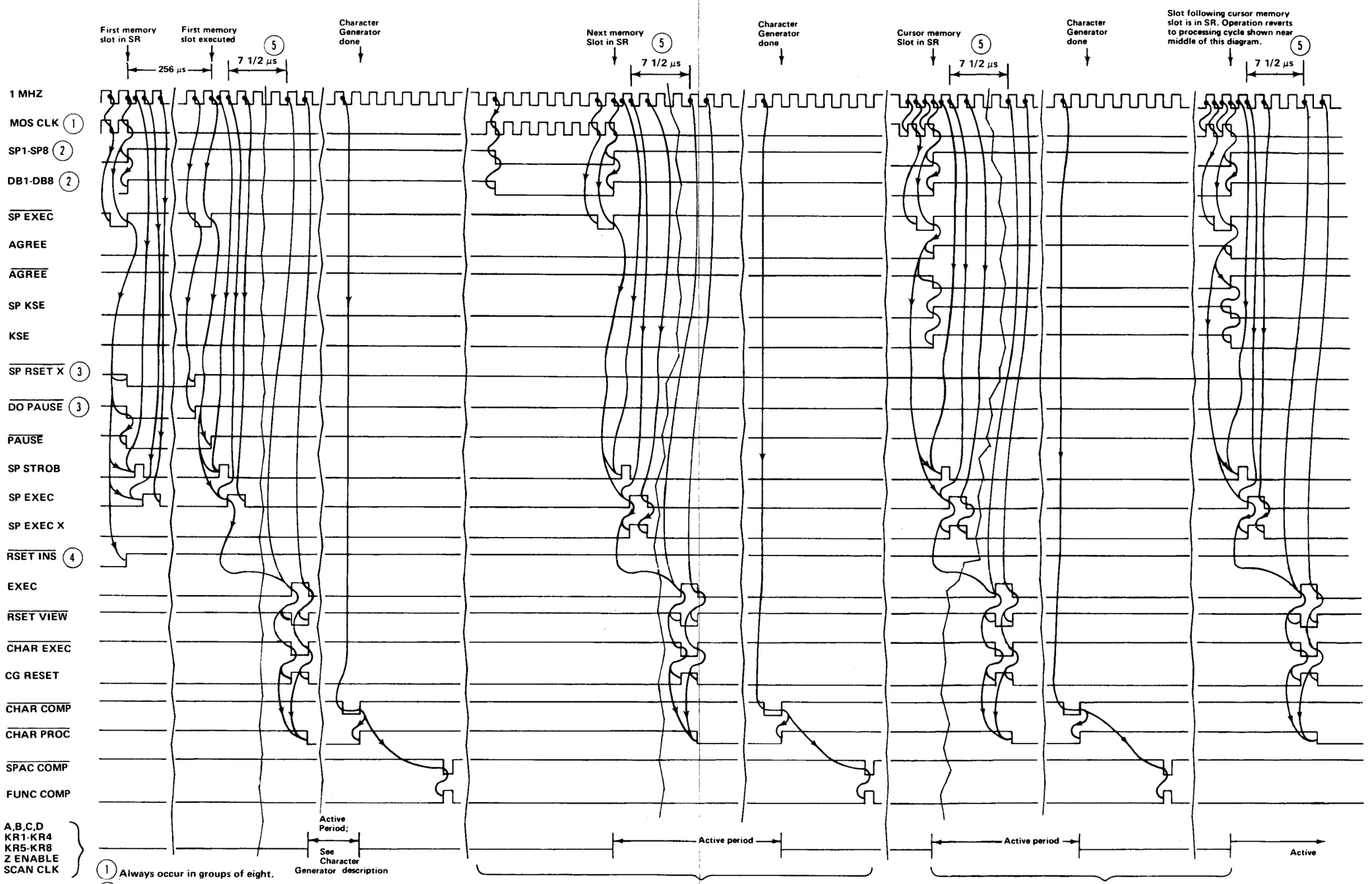


FIG 5-18
BLOCK DIAGRAM
RECEIVING IN UNREFRESHED
SCRATCH PAD MODE

4002A DRAWER



(1) Always occur in groups of eight.

(2) High indicates valid data.

(3) Board number 670-1438-00 does not contain $\overline{\text{DO PAUSE}}$; $\overline{\text{SP RSET X}}$ then controls $\overline{\text{PAUSE}}$.

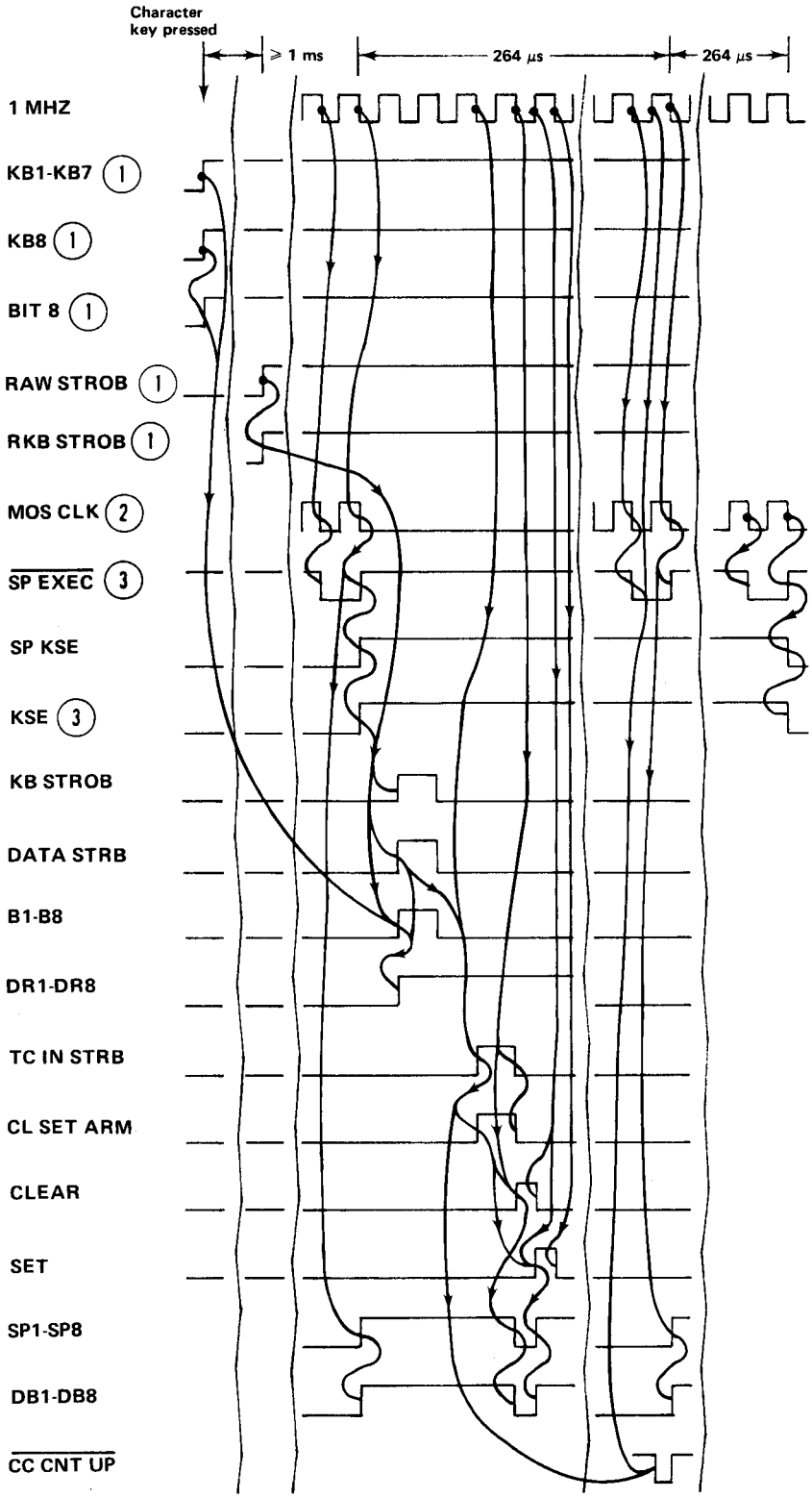
(4) Goes low when last memory slot leaves Shift Register. Returns high when first memory slot is loaded in Shift Register.

(5) This delay does not exist on TC-5 boards numbered 670-1438-00 EXEC is then controlled solely by SP EXEC.

Processing cycle for memory slots other than first slot and cursor slot; Repeats until Cursor Memory slot or First Memory Slot enters Shift Register.

See appropriate diagram for Character Entry Character Insertion or Character Deletion

Fig. 5-19. Refreshed Scratch Pad timing.

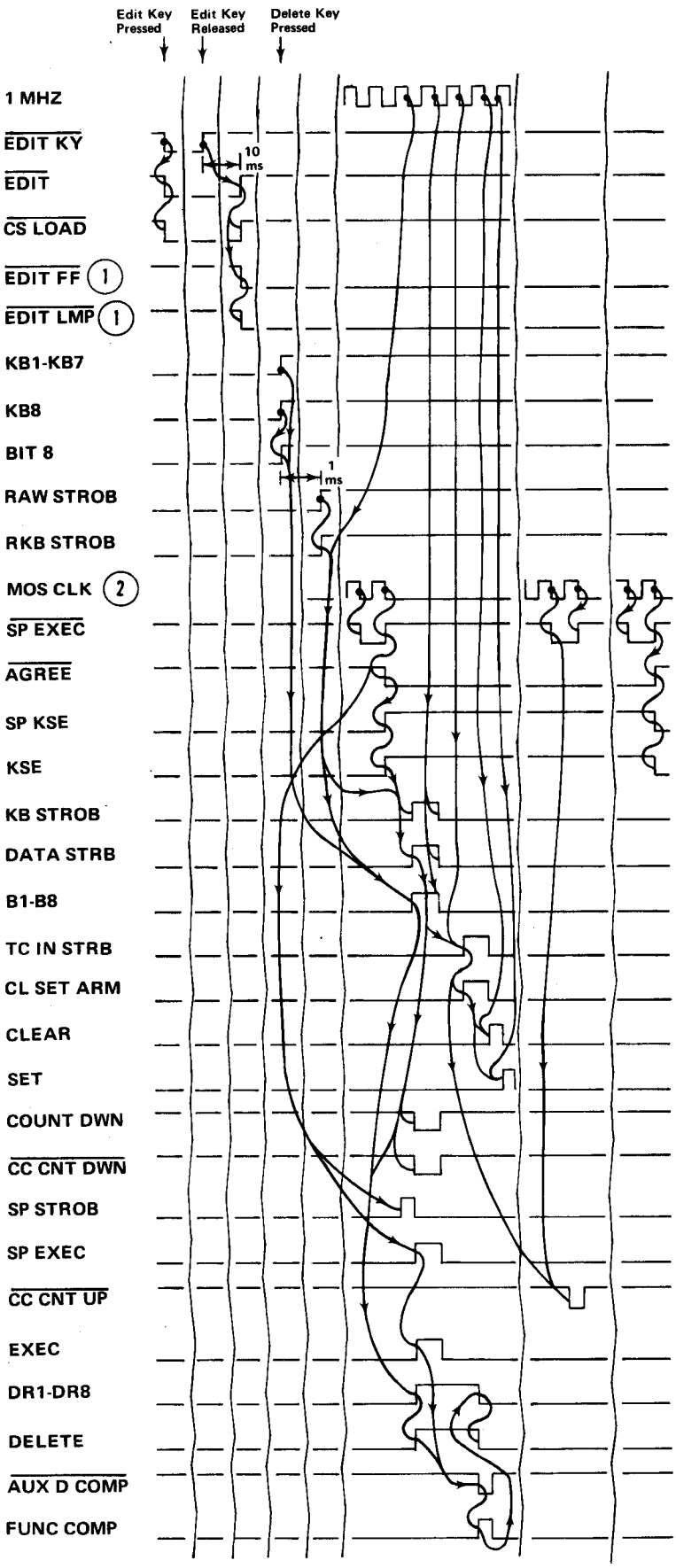


(1) Ends when key is released

(2) Always occur in groups of eight

(3) Referenced to Fig. 5-19.

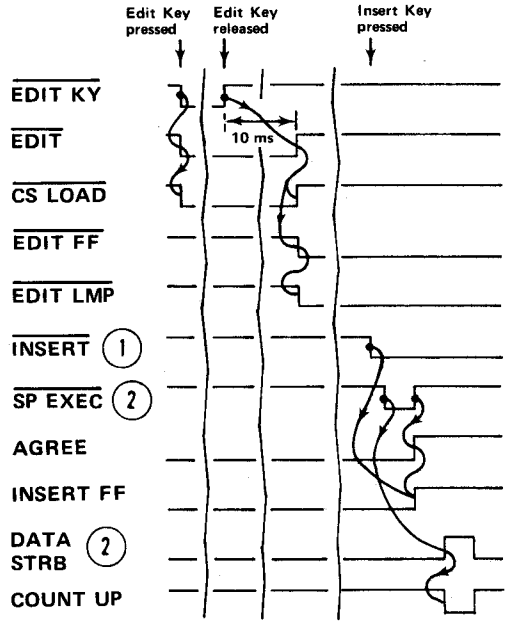
Fig. 5-20. Character Entry variation to Refreshed Scratch Pad timing. Events are additions to or variations of events in area designated on Fig. 5-19.



(1) Ends when Edit key again pressed or upon exiting from Scratch Pad Mode.

(2) Referenced to Fig. 5-19.

Fig. 5-21. Edit Mode, Delete operation. Timing is a variation of Refreshed Scratch Pad timing. Events are additions to or variations of events shown in Fig. 5-19.



(1) Key must be held down during character insertion. Signal ends when key is released.

(2) Referenced to Fig. 5-20.

Fig. 5-22. Edit Mode, Insert operation. Timing shown is in addition to Character Entry timing shown in Fig. 5-20.

BLOCK DIAGRAM DESCRIPTION

Refreshed Scratch Pad Modes

The Refreshed Scratch Pad Block Diagram contains the signal lines (and pin numbers) which are incidental to the various modes of Refreshed Scratch Pad operation. The modes are explained separately in the following paragraphs under these titles: Entering Into Compose Mode; Quiescent Compose Operation; Character Entry; Edit Mode; Delete Operation; and Insert Operation.

Entering Into Compose Mode. If the Keyboard switch is at Scratch Pad, a $\overline{\text{COMP SW}}$ goes to TC-4. When a character is entered at the Keyboard, a RAW STROB signal goes to TC-1 to generate RKB STROB. This goes to TC-2 to generate KB STROB which combines with $\overline{\text{COMP SW}}$ in TC-4 to generate COMPOSE, $\overline{\text{COMPOSE}}$, and REFRSH, putting the Terminal into Compose Mode. If the TC-5 card is numbered 670-1433-01 or above, compose into TC-5 generates $\overline{\text{ST STRIP}}$ which goes to TC-9 to hold the X Register in the Scratch Pad area of the CRT. REFRSH into TC-19 causes RCV RDY to go low and sends $\overline{\text{LOC ECHO}}$ to TC-11 to permit the B1 through B8 bits to go to TC-14 as DR1 through DR8.

Quiescent Compose Operation. In Refreshed Mode, the Scratch Pad continually circulates characters through its memory and shift register. If the memory is empty, a succession of NUL characters (all low bits) is circulated. Circuit effect is as follows: Every 256 μs a series of eight MOS CLK pulses is generated in TC-4 and goes to TC-14 to shift eight bits from memory into the shift register. They are made available to the Character Generator on the DB1 through DB8 lines. They are also made available to TC-2 on the SP1 through SP8 lines, although only used there during Send operation.

After the eight MOS CLK pulses, an $\overline{\text{SP EXEC}}$ goes from TC-4 to TC-5 to increment the position counter. (The position counter keeps count of which Scratch Pad memory character slot is in the TC-14 shift register.) Then an SP STROB goes to TC-5, followed by an SP EXEC. The SP EXEC causes TC-5 to generate an SP EXEC X pulse for TC-12 and an EXEC pulse for TC-14.

TC-12 uses the SP EXEC X pulse to increment the X register to the next character position, after which it sends a $\overline{\text{SPAC COMP}}$ to TC-2. This generates a FUNC COMP from TC-2, which goes to TC-4, TC-11, and TC-19. (FUNC COMP signals are not instrumental in quiescent Compose operation.)

TC-14 uses the EXEC pulse to generate $\overline{\text{RSET VIEW}}$ and $\overline{\text{CHAR EXEC}}$. $\overline{\text{CHAR EXEC}}$ goes to the Character Generator circuit to cause it to scan through its matrix. The Character Generator sends $\overline{\text{CHAR PROC}}$ to TC-14 and TC-19. During matrix scanning, the Character Generator and Rotator circuits send out A, B, C, D, and KR1 through KR4 signals to TC-13, and KR5 through KR8 signals to TC-9 to move the beam position through the character-writing matrix. It also examines the DB1 through DB8 coding and sends out Z ENABLE pulses when dots are to be written. TC-9, TC-13, and TC-18 route the position and unblanking information to the Display Unit. (See the Receiving—On Line-Alphanumeric Mode Block diagram description, or individual circuit card descriptions, if a more detailed description of the Character Generator operation is required.) When through with the matrix, the Character Generator sends $\overline{\text{CHAR COMP}}$ to TC-12 and ends $\overline{\text{CHAR PROC}}$ into TC-14 and TC-19. ($\overline{\text{CHAR COMP}}$ into TC-12 serves no function in Compose Mode.)

The preceding sequence repeats itself every 256 μs, until the last memory character slot is in the shift register in TC-14. Then the Position Counter in TC-5 sends out a $\overline{\text{RSET INS}}$ to TC-14. ($\overline{\text{RSET INS}}$ is not used except during Edit Mode.) After the first character slot is shifted into the TC-14 shift register, the $\overline{\text{SP EXEC}}$ pulse (which follows the eight MOS CLK pulses) ends the $\overline{\text{RSET INS}}$ pulse and causes $\overline{\text{SP RSET X}}$ and $\overline{\text{DO PAUSE}}$, during which time EXEC and SP EXEC X are inhibited. ($\overline{\text{DO PAUSE}}$ occurs only in TC-5 cards number 670-1438-01 and above. In lower numbered cards its function is performed by $\overline{\text{SP RSET X}}$.)

$\overline{\text{SP RSET X}}$ goes to TC-12. TC-4 responds with a $\overline{\text{PAUSE}}$ signal for TC-5, while TC-12 zeroes the X register (sets beam to left edge of screen). 256 μs later, another $\overline{\text{SP EXEC}}$ pulse is emitted by TC-4, after which $\overline{\text{PAUSE}}$ ends. $\overline{\text{PAUSE}}$ is not generated again until 100 MOS CLK groups later, when the first character slot is again in the shift register.

TC-5 contains a Cursor Counter which maintains a record of the cursor position. Whenever that memory slot is in the shift register, TC-5 generates an $\overline{\text{AGREE}}$ signal which causes the Character Generator to print the cursor. If a character is also in that memory slot, both the character and the cursor are written. The $\overline{\text{AGREE}}$ signal also causes TC-4 to produce an SP KSE pulse, which causes TC-5 to generate a KSE pulse for TC-2. This permits character entry into the Scratch Pad through TC-2.

Character Entry. When a character is entered at the Keyboard, KB1 through KB7 go from the Keyboard to TC-2, while KB8 goes to TC-1 and BIT 8 goes from TC-1 to TC-2. The RKB STROB is applied to TC-2. When the Scratch Pad cursor memory slot is in the TC-11 shift register, TC-5 sends an $\overline{\text{AGREE}}$ signal to TC-4. TC-4 sends an SP KSE to TC-5, which sends a KSE to TC-2, permitting it to

generate a KB STROB and a DATA STRB, and permitting the KB1 through KB8 data to go to TC-11 as B1 through B8. The KB STROB goes from TC-2 to TC-4, and DATA STRB goes to TC-11, TC-4, and TC-19. The KB STROB has no effect in TC-4 unless the Terminal is in Direct Mode with the rocker switch at Scratch Pad position. (Under that circumstance, the Terminal switches to Compose Mode as previously described.) The DATA STRB into TC-4 is used in Edit Mode only.

DATA STRB into TC-19 generates the TC IN STRB, while DATA STRB into TC-11 loads the B1 through B8 bits into latches, making them available on the DR1 through DR8 lines to TC-4 and TC-14. The TC IN STRB goes to TC-4 to generate a CL SET ARM signal for TC-5. TC-5 then sends a CLEAR signal to TC-14 to clear the shift register. This is followed by a SET signal from TC-5 to TC-4 and TC-14. (SET affects TC-4 only in Unrefreshed Mode.) In TC-14, SET loads the DR1 through DR8 bits into the shift register. The next set of MOS CLK pulses is followed by a $\overline{\text{CC CNT UP}}$ from TC-4 to TC-5, which increments the cursor counter in TC-5 by one, advancing the cursor to the next character slot in the memory circuit. Subsequent MOS CLK pulses cycle them through the memory circuit as explained for Quiescent Compose operation.

Edit Mode. When the Edit key is pushed at the Keyboard, an $\overline{\text{EDIT KY}}$ signal goes to TC-1, which sends an $\overline{\text{EDIT}}$ signal to TC-4. If in Compose Mode, a $\overline{\text{CS LOAD}}$ goes from TC-4 to TC-5 to load the cursor counter register contents into the cursor storage register. When $\overline{\text{EDIT}}$ ends, TC-4 sends an $\overline{\text{EDIT FF}}$ signal to TC-1, TC-5, and TC-14; TC-1 sends an $\overline{\text{EDIT LMP}}$ signal to the Keyboard to light the Edit lamp; TC-5 uses the $\overline{\text{EDIT FF}}$ signal during Send operation only; TC-14 uses the signal as enabling voltage for Insert and Delete operation.

A Quiescent Edit Operation now exists, which is the same as Quiescent Compose Operation except for the added signals and the lighted Edit lamp.

If the Edit key is pushed again, $\overline{\text{EDIT KY}}$ again causes $\overline{\text{EDIT}}$, which causes TC-4 to generate $\overline{\text{CC LOAD}}$. This causes TC-5 to load the cursor storage contents into the cursor counter. When $\overline{\text{CC LOAD}}$ ends, $\overline{\text{EDIT FF}}$ goes high and $\overline{\text{EDIT LMP}}$ into the Keyboard goes high, extinguishing the Edit lamp.

Delete Operation. If the Delete key is pushed while in Edit Mode, the character under the cursor is removed from memory and a NUL is put in its place. This happens as follows: When Delete is entered at the Keyboard, KB1 through KB7, BIT 8, and RKB STROB go to TC-2. When the cursor memory slot is in the shift register, $\overline{\text{AGREE}}$ goes from TC-5 to TC-4, SP KSE from TC-4 to TC-5, KSE from TC-5 to TC-2. DATA STRB then goes to TC-11, TC-4, and TC-19, while B1 through B8 go to TC-11. DATA STRB into TC-11 causes the B1 through B8 bits to emerge from TC-11 as DR bits, which are used by TC-14. In TC-14 a detector senses the DELETE character, which causes the shift register to be bypassed by the memory loop.

A DELETE signal is also sent from TC-14 to TC-4. DATA STRB and DELETE combine in TC-4 to generate a CC CNT DWN signal and a COUNT DWN signal to make TC-5 decrement the cursor counter and cursor storage registers. An $\overline{\text{AUX D COMP}}$ signal is generated in TC-14 after the DELETE signal ends. This goes to TC-2 to generate FUNC COMP which clears the data register in TC-11.

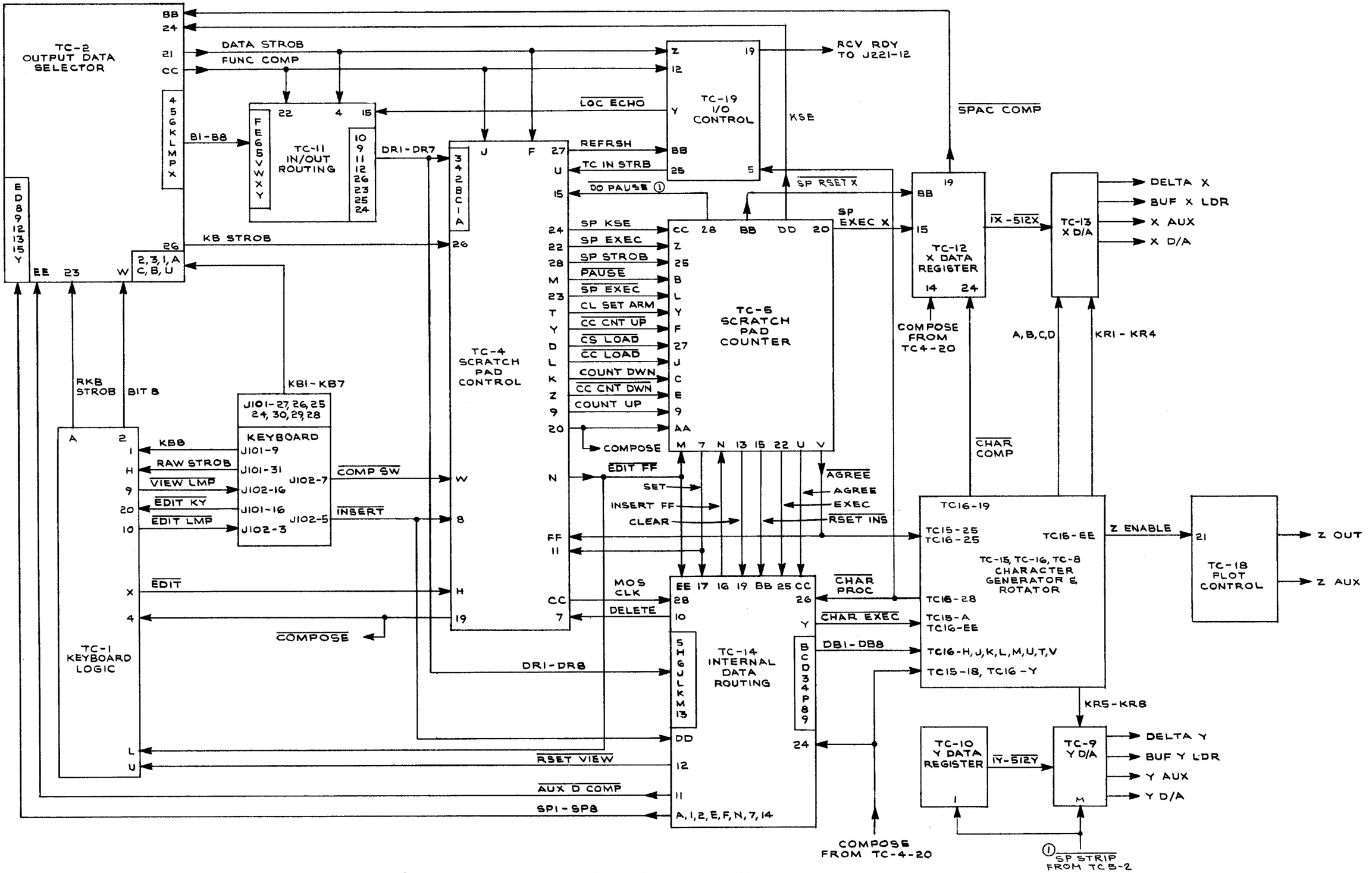
DATA STRB into TC-19 causes TC IN STRB to go to TC-4, where it causes a $\overline{\text{CC CNT UP}}$ signal to go to TC-5 after the next set of eight MOS CLK pulses. This increments the cursor counter by one, restoring it to its previous slot in the Scratch Pad memory.

The Terminal then returns to Quiescent Edit Operation except that the shift register is still bypassed by the memory loop in TC-14. This exists until the last memory slot is shifted past the shift register. Then the $\overline{\text{RSET INS}}$ pulse from TC-5 goes to TC-14 to re-insert the empty shift register into the memory loop. The Terminal then returns to Quiescent Edit Operation, functioning as previously described.

Insert Operation. If a character is to be inserted, the Terminal must be in Edit Mode, the Insert key held down, and a character key pressed. The Insert key generates an $\overline{\text{INSERT}}$ signal for TC-4 and TC-14. It provides TC-4 with an enabling voltage, and causes TC-14 to place an empty "Insert Shift Register" in the memory loop. TC-14 sends an INSERT FF signal to TC-5 to account for the character slot added to the Scratch Pad memory loop. The empty shift register is inserted when the cursor slot is in the shift register, causing a NUL to be inserted in memory immediately following the cursor slot. In addition, parallel entry into the shift register is blocked and parallel entry into the insert shift register is enabled.

When a character is entered at the Keyboard, it waits until an $\overline{\text{AGREE}}$ signal occurs, indicating that the cursor slot is in the shift register. This also indicates that the NUL slot is in the insert shift register. The character being entered is then accepted into the insert shift register in a manner identical to that previously described for Character Entry, except that the DATA STRB which accompanies character entry also causes TC-4 to emit a COUNT UP signal. This causes the cursor storage register in TC-5 to increment to account for the added character.

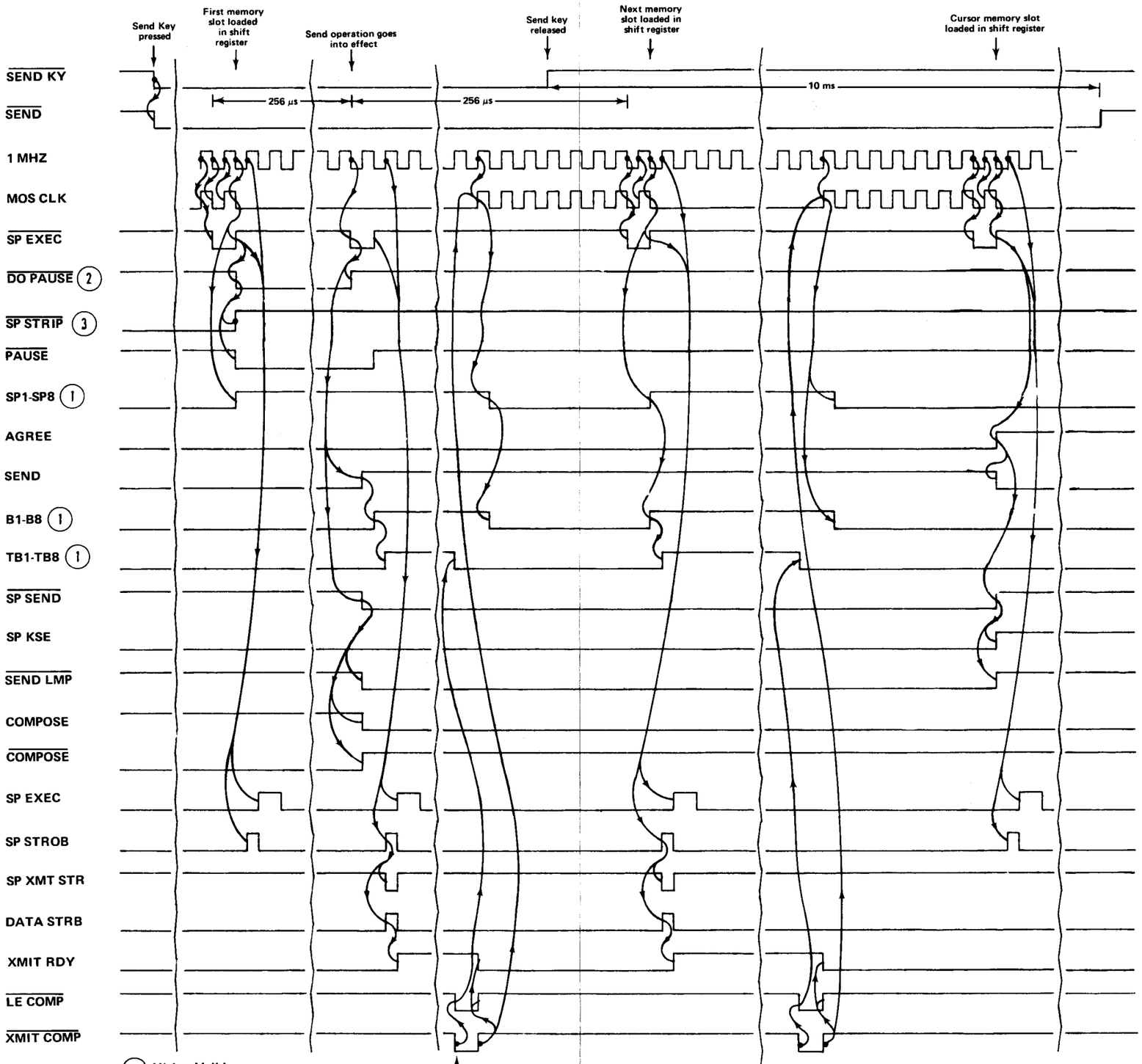
There is one additional character slot in memory when the insert shift register is in the loop, and it must be removed to return to quiescent operation. Therefore, when the last character slot is in the insert shift register, the $\overline{\text{RSET INS}}$ signal goes from TC-5 to TC-14 to remove the insert shift register from the memory loop, restoring Quiescent Edit Operation.



① IF TERMINAL CONTAINS TC-5 BOARD NUMBERED 670-1438-00, THE DO PAUSE FUNCTION IS PERFORMED BY SP RSET X. THE SP STRIP FUNCTION IS PERFORMED BY COMPOSE INTO TC-10 AND BY COMPOSE INTO TC-9.

FIG 5-23
BLOCK DIAGRAM
REFRESHED SCRATCH PAD

Diagrams–4002A Drawer



(1) High = Valid

(2) Performed by $\overline{\text{SP RSET X}}$ in TC-5 cards numbered 670-1438-00.

(3) Does not exist in TC-5 cards numbered 670-1438-00.

Fig. 5-24. Timing for Send operation.

BLOCK DIAGRAM DESCRIPTION

Transmitting—On Line-Send; Echoing Not In Effect

General. Send can be initiated in Unrefreshed Mode, in Compose Mode (Send Operation), or in Edit Mode (Edit Send Operation). Send Operation causes the Scratch Pad memory contents from the first memory slot to the cursor position to be sent. Edit Send Operation sends the data between cursor memory position (the position occupied by the cursor when Edit Mode is selected) and the actual position of the cursor. The basic Send Operation is explained in detail, and the Edit Send Operation is explained as a variation of Send.

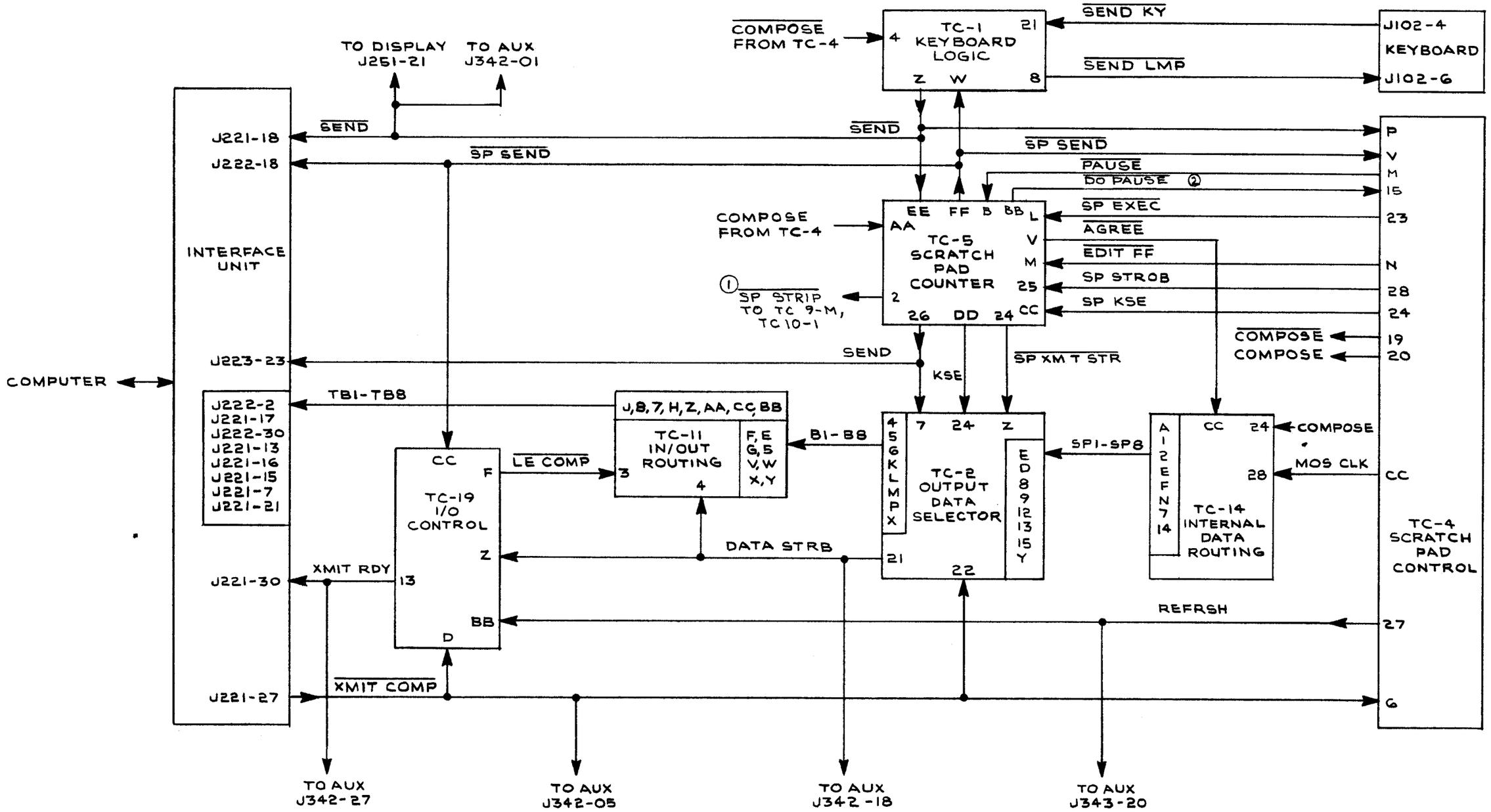
Send Operation. This is initiated by pressing the Send key while in Compose Mode. $\overline{\text{SEND KY}}$ then goes to TC-1. $\overline{\text{SEND}}$ goes from TC-1 to TC-, to TC-5, to the Interface Unit, and to the Display Unit. If in Unrefreshed Mode, $\overline{\text{SEND}}$ into TC-4 puts the Terminal into Compose Mode, putting a high on the REFRSH line. When the Scratch Pad memory first character slot is in the shift register in TC-14, TC-5 routes an $\overline{\text{SP SEND}}$ signal to TC-1, TC-4, the Interface Unit, and TC-19. TC-5 also provides a SEND signal to TC-2 and the Interface Unit. TC-1 routes a $\overline{\text{SEND LMP}}$ signal to the Keyboard to light the Send key. $\overline{\text{SP SEND}}$ into TC-4 ends the COMPOSE, $\overline{\text{COMPOSE}}$, REFRSH, and MOS CLK signals, thus causing TC-14 to hold the first character on the SP1 through SP8 lines to TC-2. TC-2 uses the SEND signal to route the SP1 through SP8 bits to TC-11 as B1 through B8.

1 μs after TC-4 generates the $\overline{\text{SP EXEC}}$ pulse (which caused TC-5 to emit $\overline{\text{SP SEND}}$), TC-4 sends an SP STROB to TC-5. TC-5 routes this to TC-2 as $\overline{\text{SP XMT STR}}$. TC-2 then creates a DATA STRB signal for TC-11 and TC-19. This latches the B1 through B8 bits into TC-11, emitting them from there as TB1 through TB8. The DATA STRB into TC-19 causes XMIT RDY to go high.

When the computer accepts the data bits, the Interface Unit sends $\overline{\text{XMIT COMP}}$ to TC-2, TC-4, and TC-19. TC-19 ends the XMIT RDY signal and sends an $\overline{\text{LE COMP}}$ signal to TC-11 to clear the data latches. TC-2 responds to the $\overline{\text{XMIT COMP}}$ signal by routing a FUNC COMP (not shown) to TC-4, TC-11, and TC-19, although none of these have any effect in this mode. TC-4 uses the $\overline{\text{XMIT COMP}}$ signal to initiate another series of MOS CLK pulses to put the next character in the shift register in TC-14, again putting the bits on the SP1 through SP8 lines. These are followed by the usual $\overline{\text{SP EXEC}}$ and SP STROB signals from TC-4 to TC-5. $\overline{\text{SP EXEC}}$ increments the position counter. SP STROB causes a repeat of the transmission as previously described.

This continues until the cursor slot is in the TC-14 shift register, TC-5 then puts $\overline{\text{SP SEND}}$ high, SEND low, and inhibits future $\overline{\text{SP XMT STR}}$ signals, ending transmission. TC-5 also generates an $\overline{\text{AGREE}}$ signal for TC-4, which restores SP KSE to a high level. TC-5 then sends KSE to TC-2 and the Terminal reverts to Direct-On Line operation.

Edit Send Operation. If in Edit Mode when the Send button is pushed, operation is approximately the same as described for Send Operation. The exception is that the $\overline{\text{EDIT FF}}$ signal from TC-4 to TC-5 causes TC-5 to wait until the cursor memory position slot (slot indicative of the position occupied by the cursor when Edit Mode is selected) before the $\overline{\text{SP SEND}}$ and SEND signals are generated in TC-5. Then the $\overline{\text{EDIT FF}}$ signal ends. The EDIT light goes out and transmission occurs as in Send Operation.



① SP STRIP DOES NOT EXIST IN TC-5 CARDS NUMBERED 670-1438-00. ITS FUNCTION IS THEN PERFORMED BY COMPOSE IN TC-9 AND BY COMPOSE IN TC-10

② DO PAUSE DOES NOT EXIST IN TC-5 CARDS NUMBERED 670-1438-00. ITS FUNCTION IS THEN PERFORMED BY SP RSET X.

FIG 5-25
BLOCK DIAGRAM
TRANSMITTING – ON LINE – SEND

BLOCK DIAGRAM DESCRIPTION

The Effect of Local Echo on the Circuits

With Local Echo selected at the Interface Unit, $\overline{LE}$ exists in TC-19 to produce $\overline{LOC\ ECHO}$ for TC-11. $\overline{LE}$ also permits the DATA STRB to perform the same functions in TC-19 as the RCV STROB does during receiving modes.

In TC-11, $\overline{LOC\ ECHO}$ causes DATA STRB to generate $\overline{DROP\ FLG}$ for TC-19. This makes TC-19 put a low on the RCV RDY line. The $\overline{LOC\ ECHO}$ signal into TC-11 also permits transmit data bits TB1 through TB8 to enter the receive circuits on the DR1 through DR8 lines at the same time they are being made available to the Interface Unit for transmission to the computer.

BLOCK DIAGRAM DESCRIPTION

The Effect of Local Mode on the Circuits

When the Keyboard switch is placed at LOCAL, a low ON LINE signal goes to TC-4, TC-11, and TC-19. The low into TC-4 only affects Send Operation, when it prevents $\overline{XMIT\ COMP}$ from causing MOS CLK pulses and permits FUNC COMP to do it. The low ON LINE into TC-11 permits FUNC COMP signals to clear the output data latches instead of the $\overline{LE\ COMP}$ signals; it also permits the B1 through B8 input bits to enter the receiving circuits on the DR1 through DR8 lines in response to a DATA STRB. The low ON LINE into TC-19 holds the RCV RDY line low and inhibits the RCV STROB circuits, preventing inputs from the Interface Unit; it also permits DATA STRB to perform the same TC-19 functions as the RCV STROB does in receiving modes.

The remaining circuit action is the same as described for On Line receiving modes, except that data is entered at the Keyboard, and the RCV RDY line in TC-19 never gets reset by completion signals.

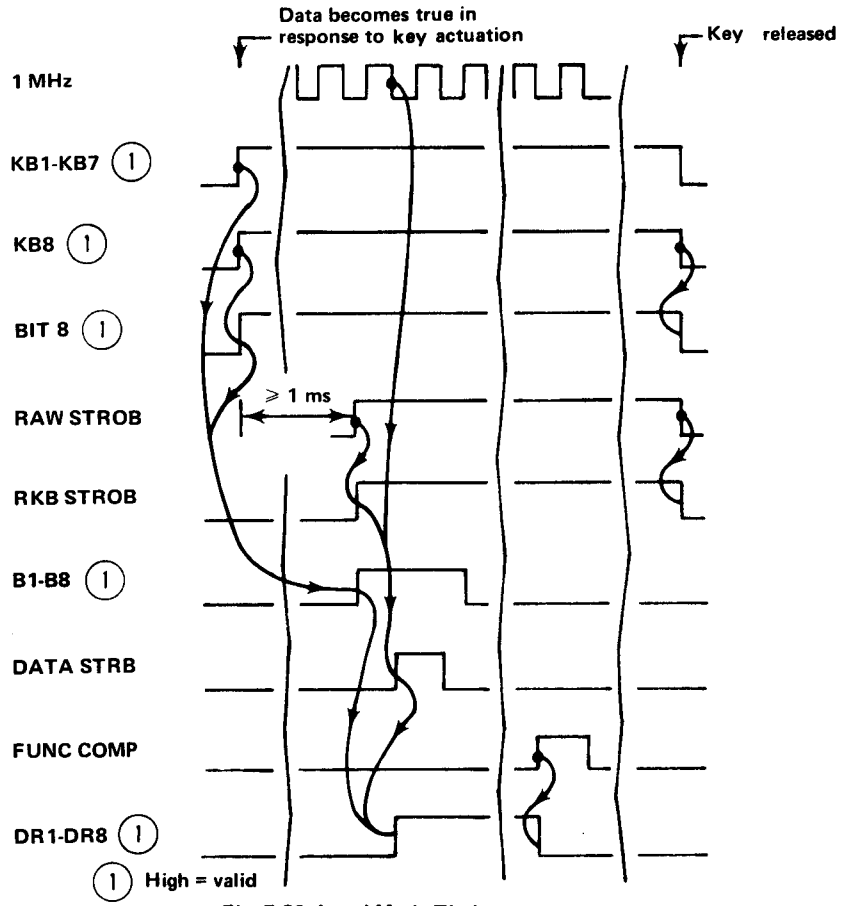


Fig. 5-26. Local Mode Timing.

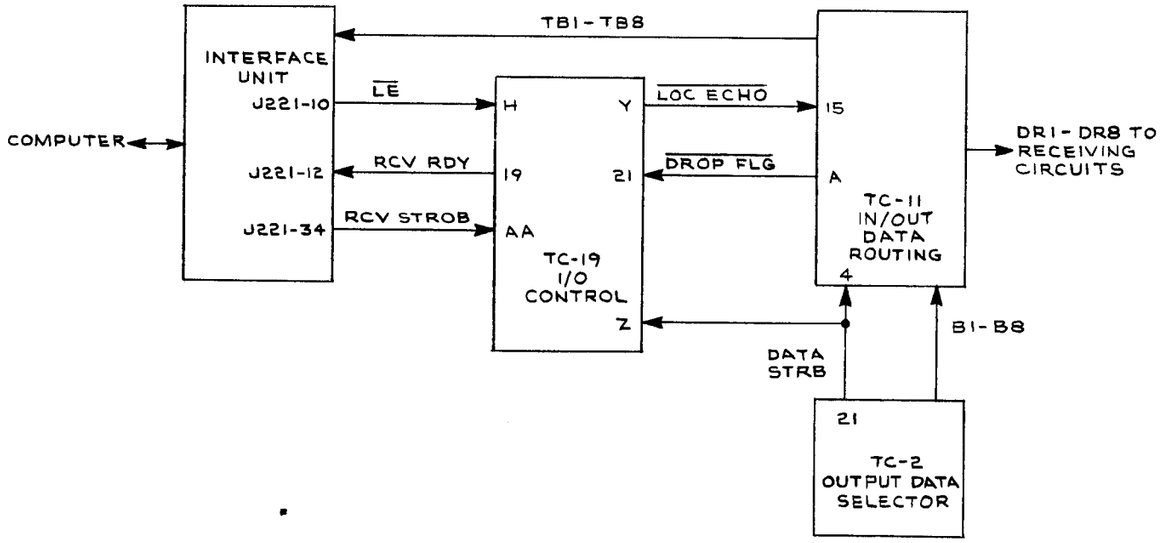


FIG 5-27
BLOCK DIAGRAM
LOCAL ECHO EFFECT 971 EKP

4002A DRAWER Ⓐ

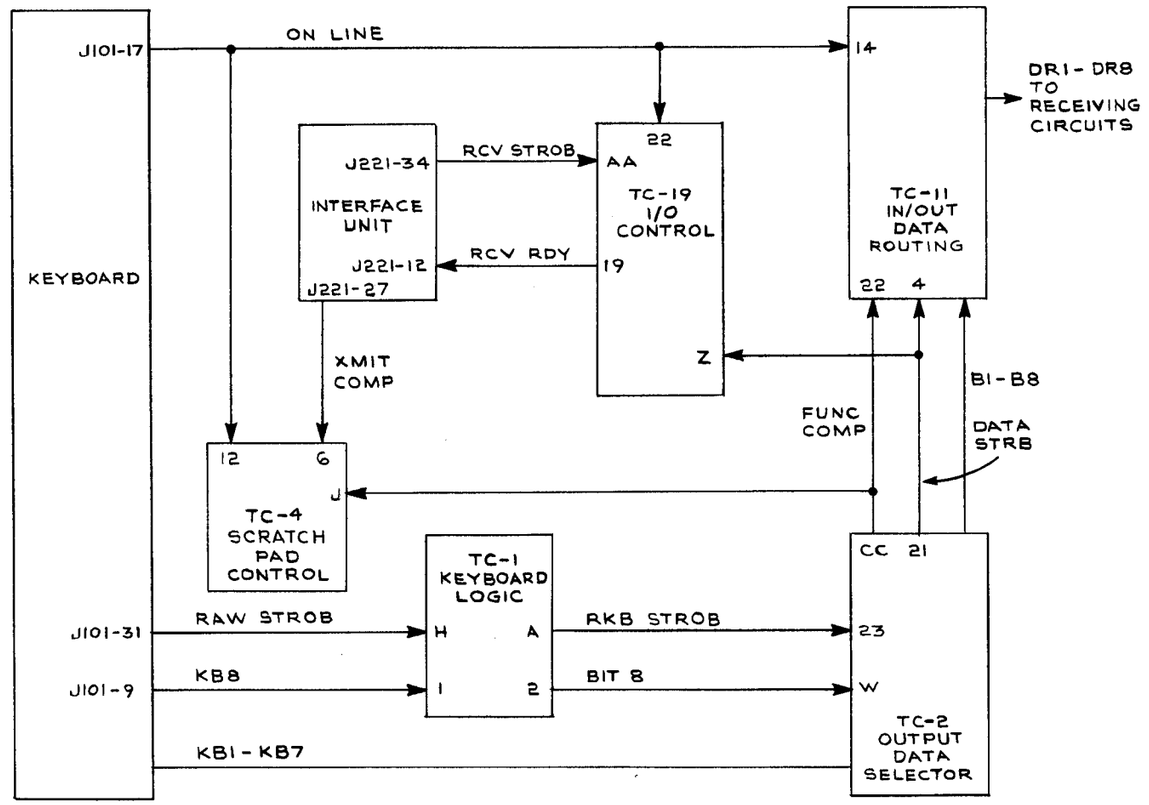
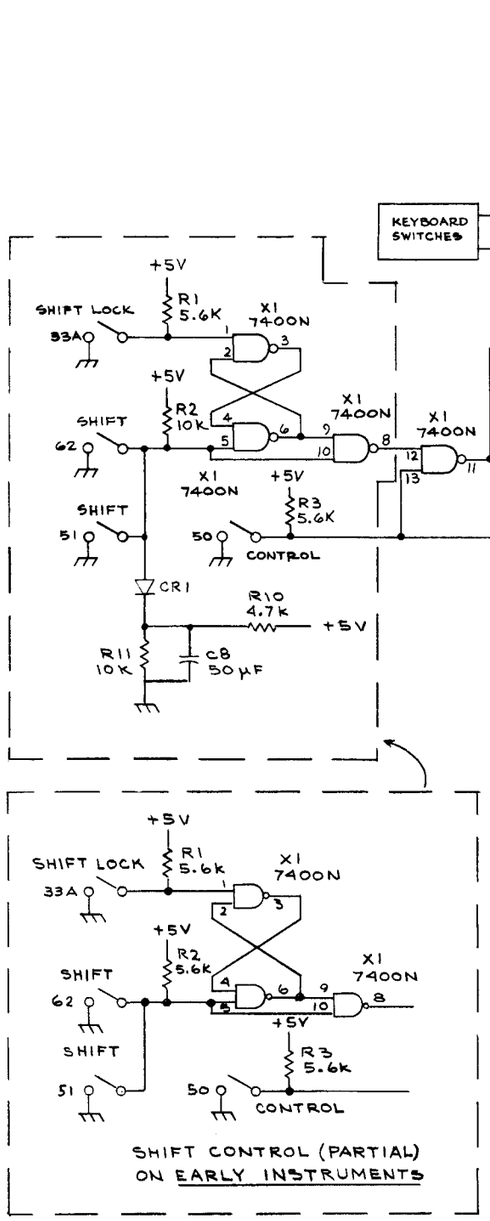
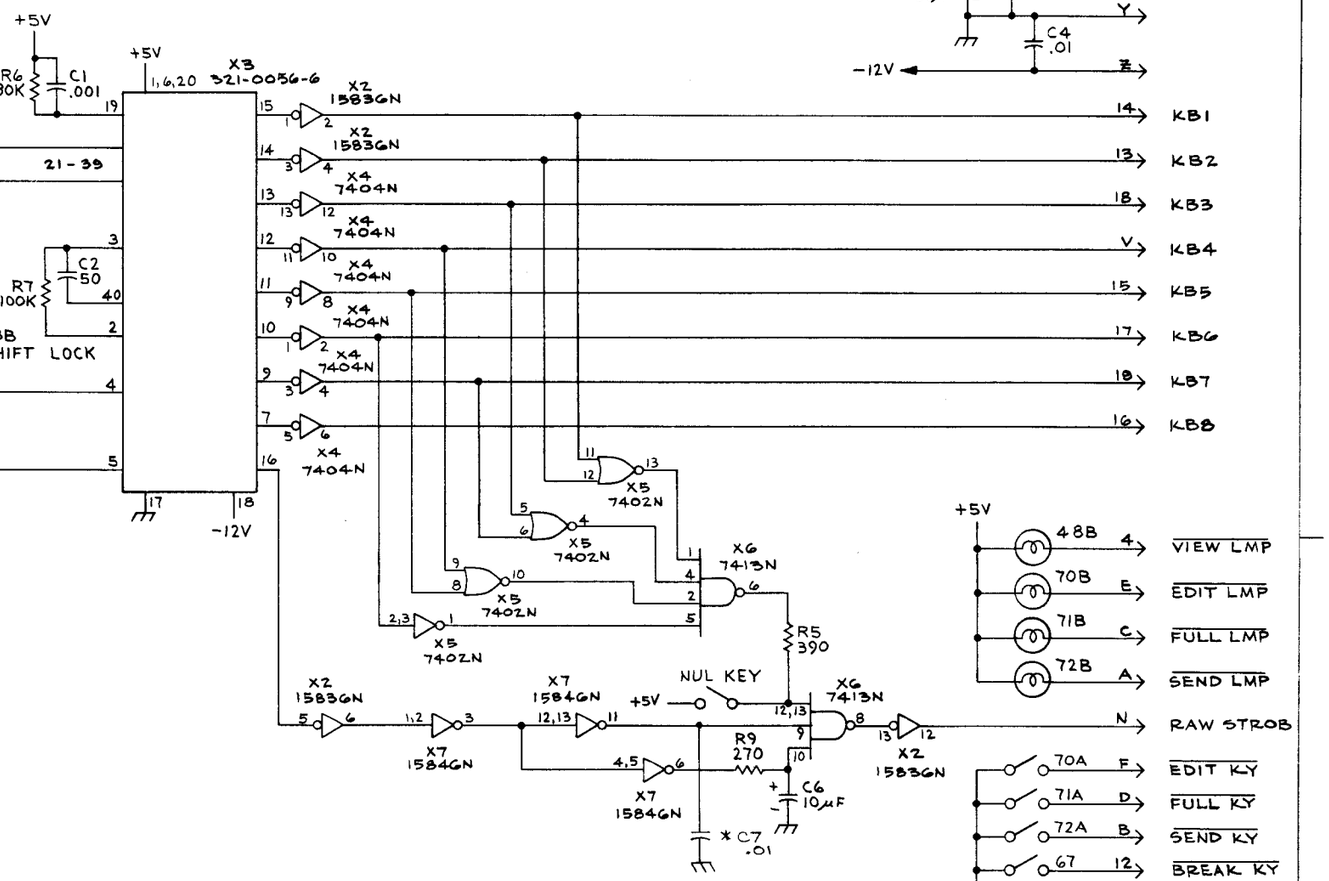


FIG 5-28
BLOCK DIAGRAM OF
LOCAL MODE EFFECT

4002A DRAWER Ⓐ



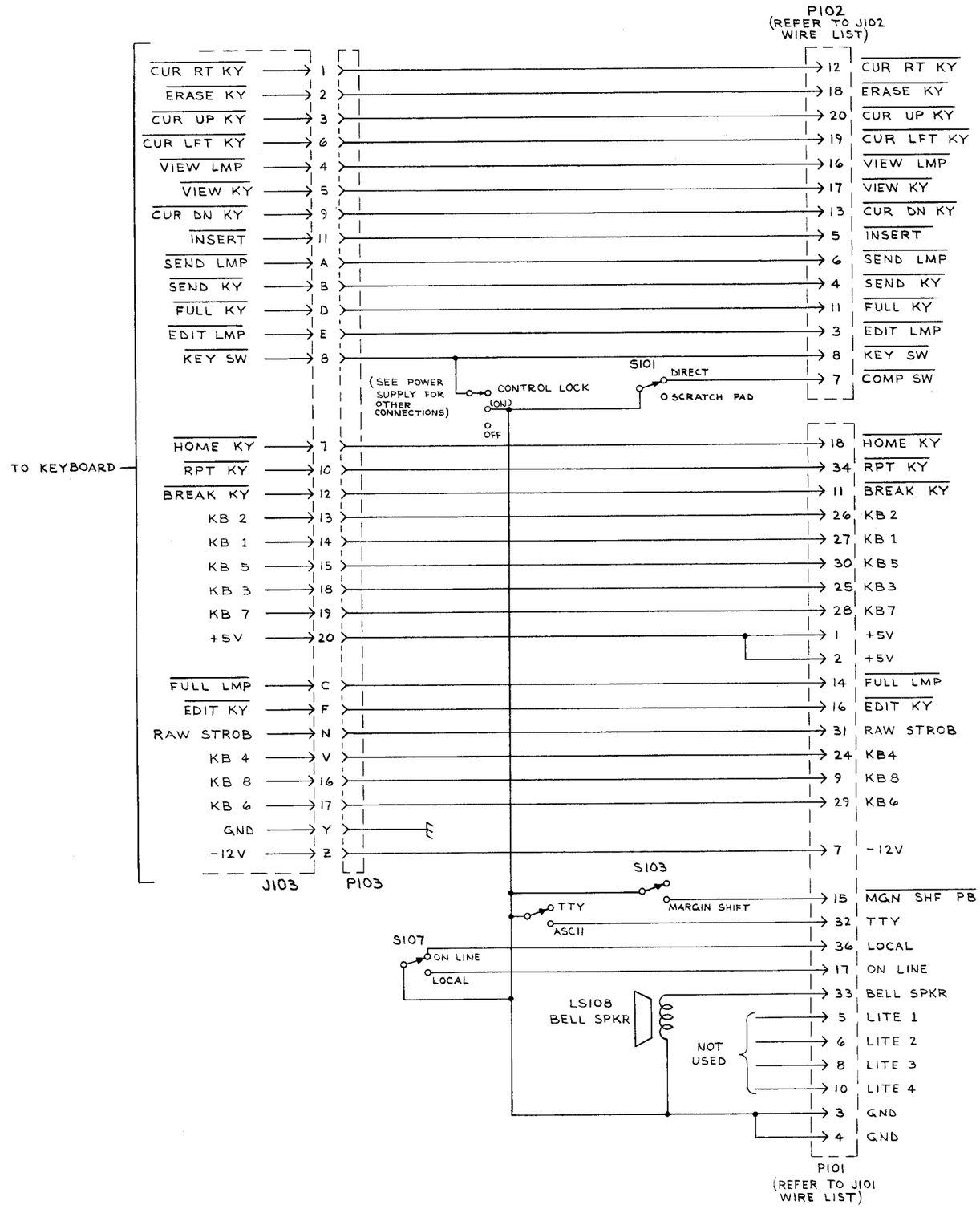
SHIFT CONTROL (PARTIAL)
ON EARLY INSTRUMENTS



* NOT PRESENT IN ALL
EARLY INSTRUMENTS

A19

FIG. 5-29 A19 KEYBOARD



4002A DRAWER

FIG 5-30 KEYBOARD CHASSIS

Ⓐ

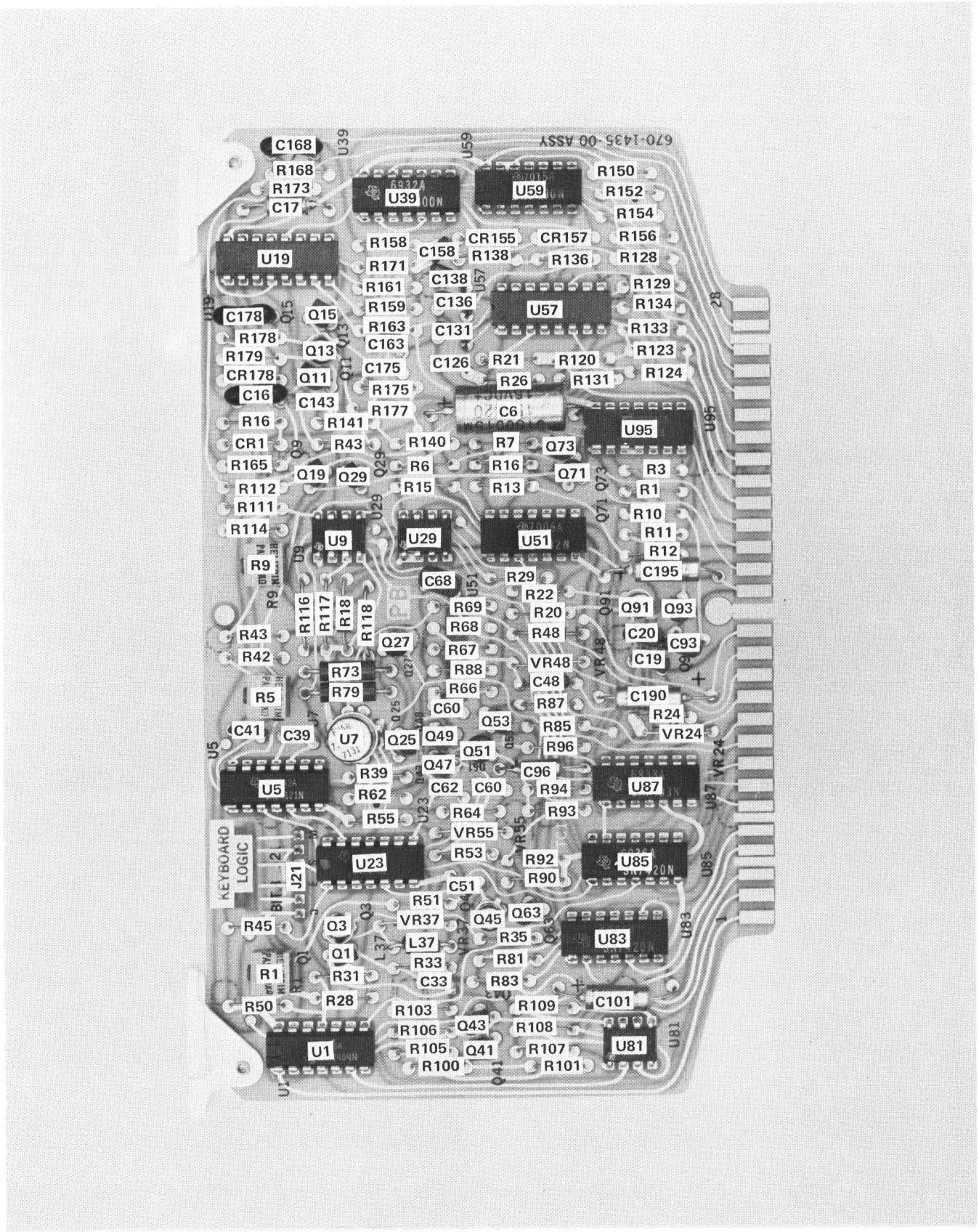
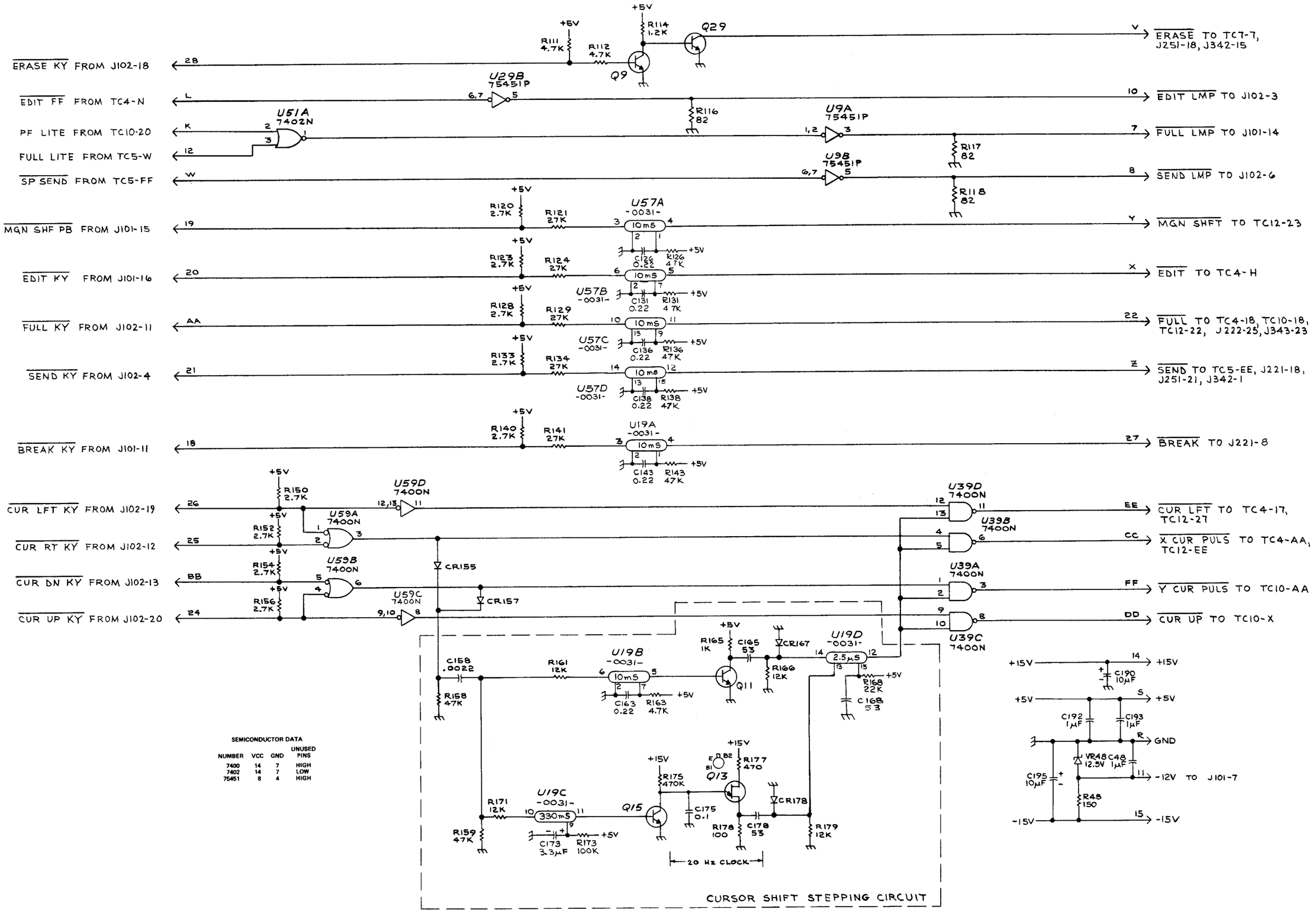


Fig. 5-31. TC1 component illustration.



SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
75451	8	4	HIGH

4002 A DRAWER

P/O A1

FIG. 5-32 KEYBOARD LOGIC TC-1 (PART 1)

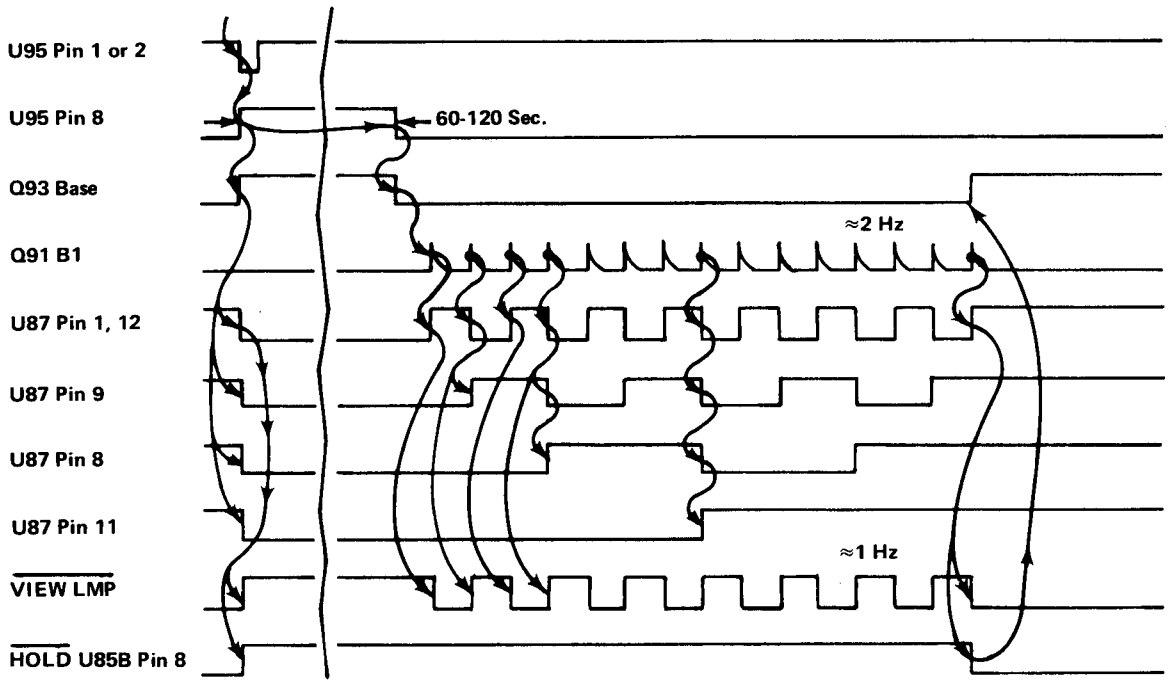


Fig. 5-33. View/Hold timing (TC-1)

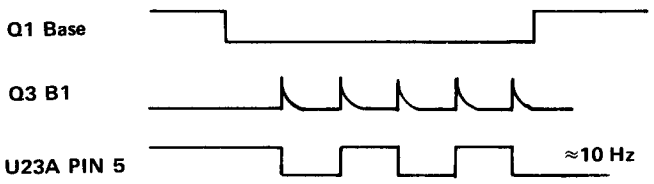


Fig. 5-34. Strobe and Repeat timing (TC-1).

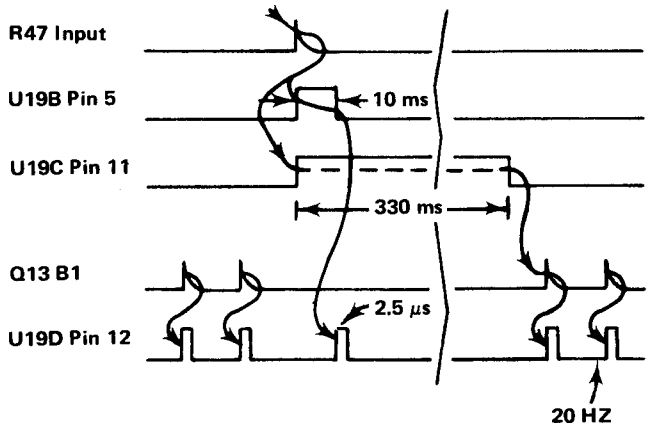
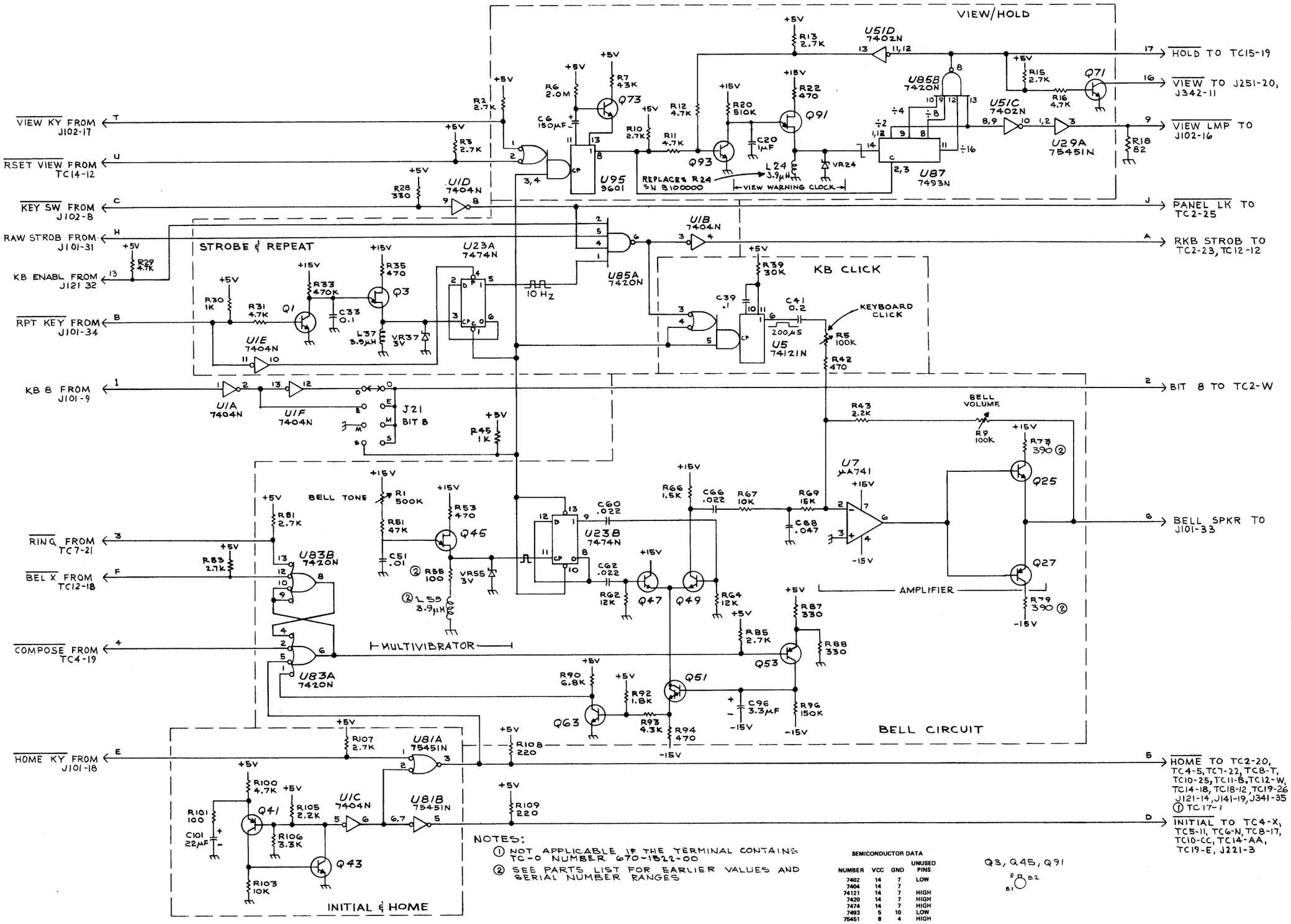


Fig. 5-35. Cursor Shift Step timing (TC-1).



NOTES:

① NOT APPLICABLE IF THE TERMINAL CONTAINS TC-0 NUMBER 670-1822-00

② SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7402	14	7	LOW
7404	14	7	
74121	14	7	HIGH
7420	14	7	HIGH
7474	14	7	HIGH
7493	5	10	LOW
75451	8	4	HIGH

Q3, Q45, Q91

©

4002 A DRAWER

P/O A1

REV. JAN. 1974

FIG. 5-36 KEYBOARD LOGIC TC-1 (PART 2)

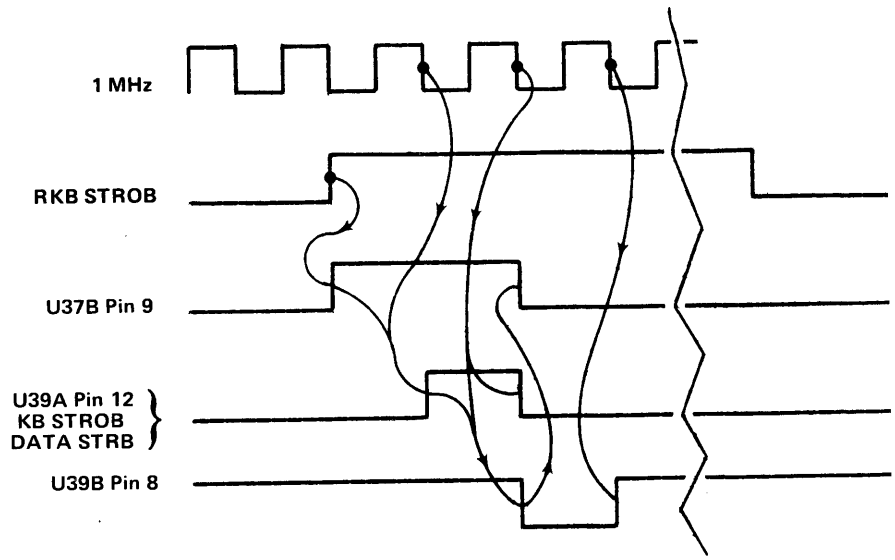


Fig. 5-37. KB STROBE timing. (TC-2 Circuit card 670-1436-01).

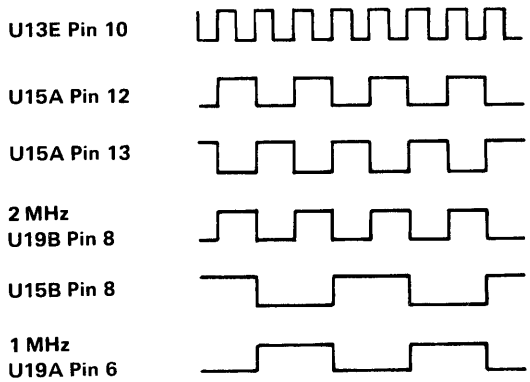
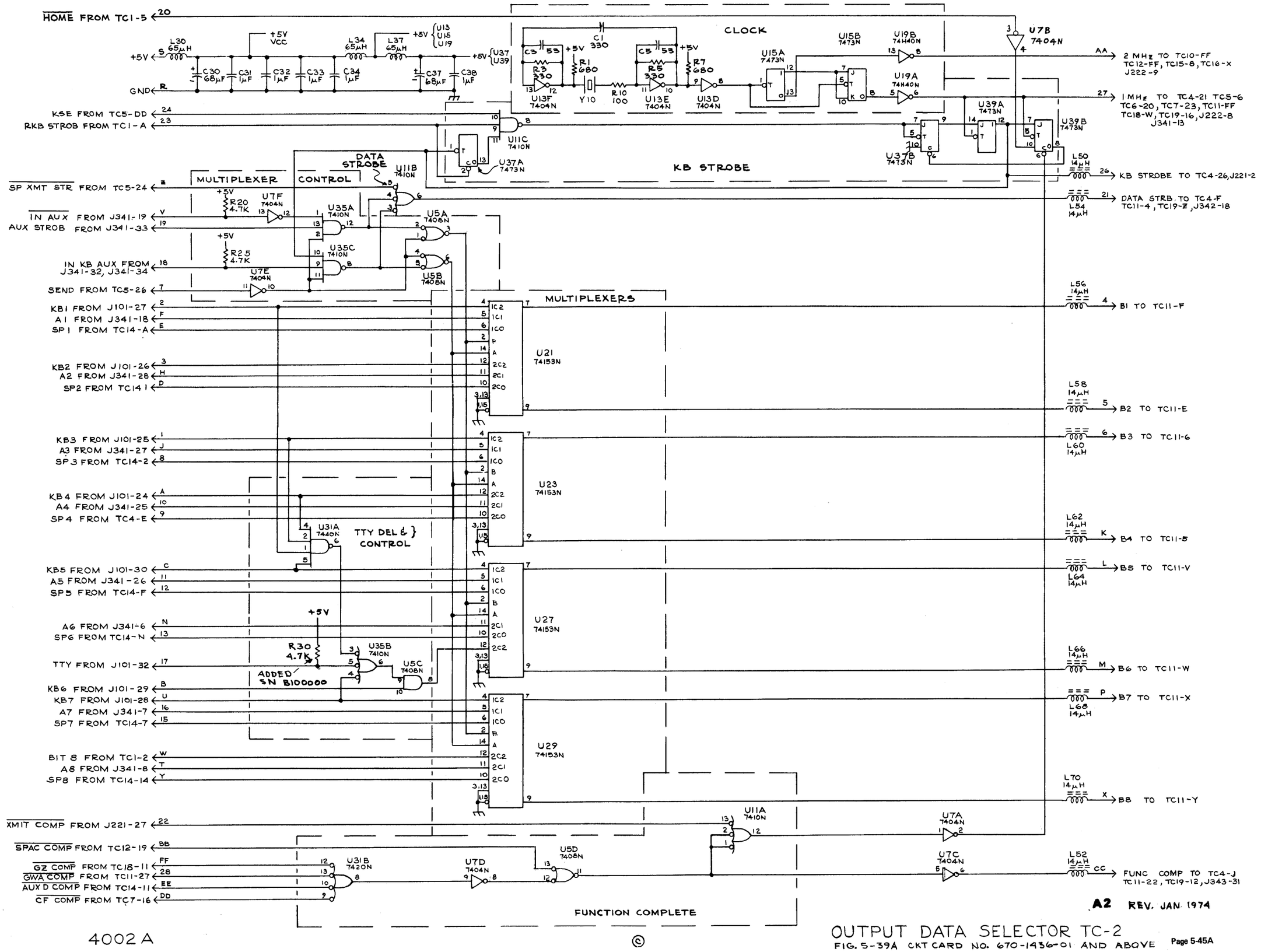


Fig. 5-38. Clock timing (TC-2). Circuit card (670-1436-01).



A2 REV. JAN. 1974

4002 A

OUTPUT DATA SELECTOR TC-2

FIG. 5-39A CKT CARD NO. 670-1436-01 AND ABOVE

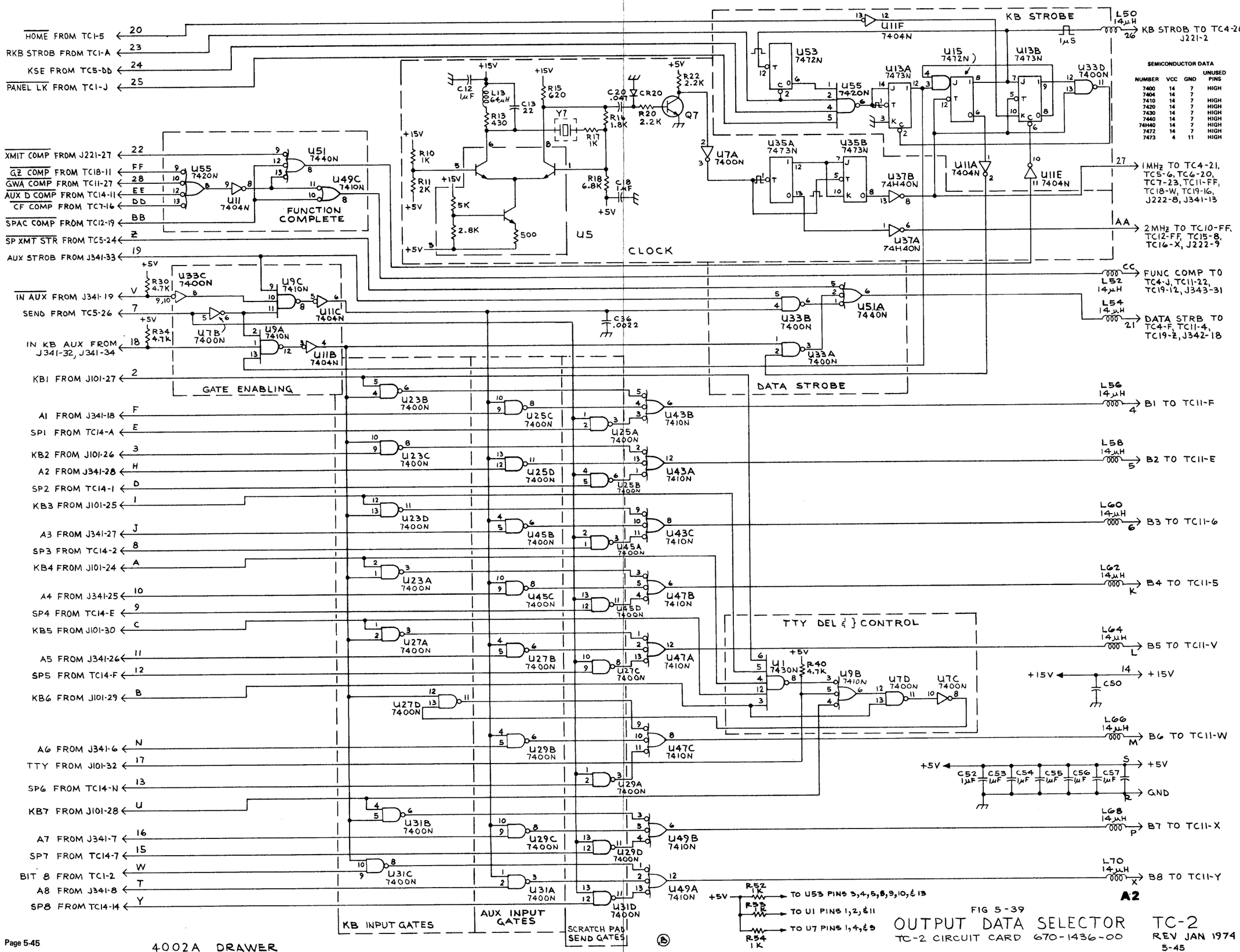


FIG 5-39

OUTPUT DATA SELECTOR TC-2

TC-2 CIRCUIT CARD 670-1436-00

REV JAN 1974

5-45

A2

4002A DRAWER

Page 5-45

TC-2
670-1436-00

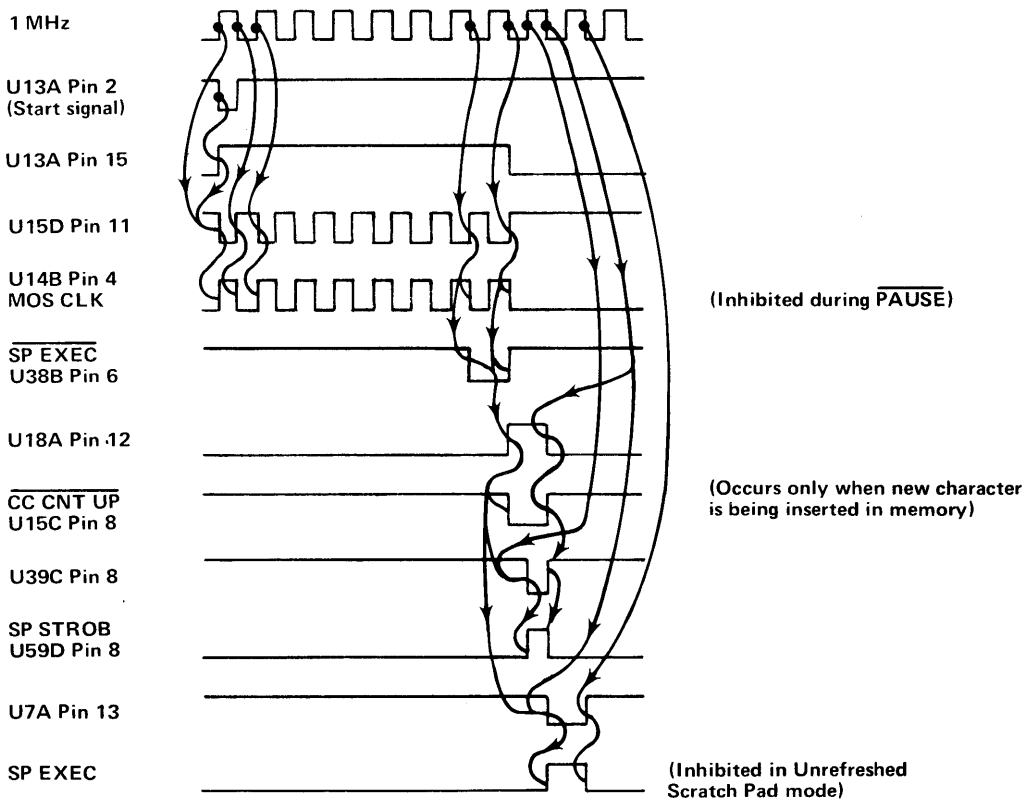


Fig. 5-40. One cycle of MOS CLK circuit operation (TC-4). A 256 μs PAUSE signal occurs every 101 cycles, immediately after the memory first character slot is loaded in the TC-11 shift register. PAUSE starts when U38B pin 6 goes high.

NOTES:
① THIS WIRE ADDED IN LATER BOARD VERSIONS. PIN 1 OF U43A WAS PREVIOSLY CONNECTED TO +5V.
② NOT APPLICABLE IF THE TERMINAL CONTAINS TC-0 NUMBER 670-1522-00
③ PIN 13 IS DRIVEN BY SP RSET X FROM TC5-BB IF TERMINAL CONTAINS TC-0 NO. 670-1522-00
④ CON. BELOW SN B089999
⑤ CON. ABOVE SN B090000

DR7 FROM TC11-25 A
DR6 FROM TC11-23 1
DR5 FROM TC11-26 C
DR4 FROM TC11-12 B
DR3 FROM TC11-11 2
DR2 FROM TC11-9 4
DR1 FROM TC11-10 3
SP ARM FROM TC7-12 25
US FROM TC7-E EE
LOAD DATA FROM J221-26 16
KB STROB FROM TC2-26 26
COMP SW FROM J102-7 W
FUNC COMP FROM TC2-CC J
ON LINE FROM J101-17 12
HOME FROM TC1-5 5
SEND SCRN FROM J222-1 E
XMIT COMP FROM J221-27 6
SEND FROM TC1-Z P
FULL FROM TC1-22 18
SET FROM TC5-7 11
SP LE FROM TC19-W 10
1MHz FROM TC2-27 21
③ DO PAUSE FROM TC5-28 15
INITIAL FROM TC1-D X
AGREE FROM TC5-V FF
SP SEND FROM TC5-FF V
TC IN STRB FROM TC19-25 U
X CUR PULS FROM TC1-CC AA
CUR LFT FROM TC1-EE 17
DELETE FROM TC14-10 7
DATA STRB FROM TC2-21 F
INSERT FROM J102-5 8
EDIT FROM TC1-X H
INITIAL FROM TC5-10 DD

U41A 7404N
U41C 7404N
U41B 7404N
U41F 7404N
U25A 7404N
U41D 7404N
U41E 7404N
U1 7430N EOT DETECT
U23 7430N C DETECT
U2 7430N ? DETECT
U21 7430N ESC DETECT
U45B 7400N
+5V
R11 4.7K
PROGRAM CONTROL
U47B 7474N
ARM FF
U47A 7474N
UNREFRESHED SP FF
R10 200
U25E 7404N
C1 .001
U45D 7400N
ARM FF RESET
U53D 7402N
U25D 7404N
U39A 7400N
U53C 7402N CLEAR SELECT
EDIT SELECT
UNREFRESH SP
U51F 7404N
UNREFRESH SP
UNRFRSH COMPOSE
R1 4.7K +5V
U59B 7404N
U51E 7404N
U53A 7402N
U53B 7402N
U27A 7474N
5 REFRESH SP
REFRESH SP
U45A 7400N
RESET U14C 7402N
U59E 7404N
U25F 7404N
+5V
R8 4.7K
REFRESHED SCRATCH PAD
SEND SCREEN
U27B 7474N
U15B 7400N
R3 3k
Q5
U51C 7404N
U5C 7400N
U25C 7404N
U9A 7400N
U59F 7404N
U5A 7400N
U9D 7400N
U45C 7400N
U29A 7440N
SP SEND COMPLETE
CLEAR
U19B 7402N
U14A 7402N
C3 .22μF
R12 15K +5V
U49A 7473N
U49B 7473N
U31 9601
1 mS
UNREFRSH SCRATCH PAD COMPLETE F.F.
U55 7493N
÷8
÷2
÷4
÷16
U37 7430N
U57 7493N
U17C 7404N
÷256
U14D 7402N
U17F 7404N
U51A 7404N
U11A 7420N MOS CLK ENABLE
U11B 7420N
U15A 7400N
R14 200
C14 .001
COMPOSE
U13A 7476N
MOS CLK GATE
U15D 7400N MOS CLK ENABLE FF
MOS CLK
1MHZ
U43A 7410N
U33A 7400N
R22 1K
R24 1K
R25 2K
CR22
C25 .001
U13B 7476N
U14B 7402N
-U7A 7473N
SP EXEC ARM FF
U17A 7404N
U58 7493N
U17D 7404N
U38B 7410N
U18A 7473N
U18B 7473N
U15C 7400N
U39C 7400N
U59C 7404N
U38C 7410N
U39B 7400N
U59D 7404D
U19A 7402N
KEYBOARD STROBE ENABLE
U33C 7400N
COMPOSE GATE
U59A 7404N
U29B 7440N
COMPOSE
U35C 7400N CC COUNT DOWN
U17 7404N
U35B 7400N
U33D 7400N
U39D 7400N
U35D 7400N
U35A 7400N
U38A 7410N
U33B 7400N
CURSOR COUNTER COUNT UP
COUNT DOWN
U43C 7410N
U43B 7410N
R20 1K
U25B 7404N
U5D 7400N
U9B 7400N
EDIT FF
U7B 7473N
U5B 7400N
U19D 7402N
① EDIT CONTROL
⑧

EITHER A SCRATCH PAD CONTROL OR A BYPASS CARD MUST BE USED.

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7440	14	7	HIGH
7473	4	11	HIGH
7474	14	7	HIGH
7476	8	13	HIGH
7490	8	10	HIGH
7493	8	10	LOW

+5V S → 13 SP COMP
19 COMPOSE
N EDIT FF
GND R → 22 SP EXEC
20 COMPOSE
27 REFRSH
SAME AS BELOW
TC4 SCRATCH PAD BYPASS

+5V S → +5V
C30 1μF C31 1μF C32 1μ
R GND

BB → INHIBIT X TO TC5-18
27 → ② TC17-8, ② J121-19 REFRSH TO TC19-BB
14 → CLEAR TO TC5-12
13 → SP COMP TO TC14-X
M → PAUSE TO TC 5-B
CC → MOS CLK TO TC3-Y TC14-28
9 → COUNT UP TO TC5-9
T → CL SET ARM TO TC5-Y
K → COUNT DWN TO TC5-C
L → CC LOAD TO TC5-J
D → CS LOAD TO TC5-27
N → EDIT FF TO TC1-L, TC14-EE, TC5-M
28 → SP STROB TO TC5-25
Y → CC CNT UP TO TC5-F
22 → SP EXEC TO TC5-Z
24 → SP KSE TO TC5-CC
23 → SP EXEC TO TC5-L
Z → CC CNT DWN TO TC5-E
19 → COMPOSE TO TC1-4, TC9-M
20 → COMPOSE TO TC5-AA, TC10-1, TC12-14, TC14-24, TC15-18, TC16-Y

A3

4002A DRAWER

FIG 5-41 SCRATCH PAD CONTROL

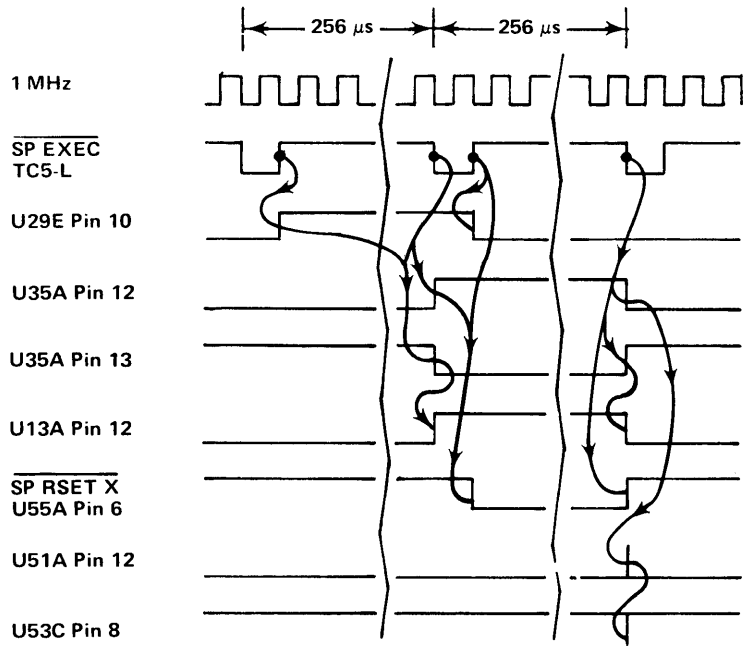


Fig. 5-42. SP RSET X circuit timing (TC-5).

EITHER A SCRATCH PAD CONTROL OR A BYPASS CARD MUST BE USED.

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	
7405	15	7	
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7473	4	11	HIGH
74H74	14	7	HIGH
7485	16	8	LOW
74193	16	8	LOW

TC IN STRB 23 22 EXECUTE

+5V 9 24 SP XMT ST
DD KSE
FF SP SEND
BB SP RSET X
V AGREE

W FULL LIGHT
26 SEND
7 SET
13 CLEAR
GND R U AGREE

TC-5
SCRATCH PAD COUNTER BYPASS

INSERT FF FROM TC14-16 N

SP EXEC FROM TC4-23 L
PAUSE FROM TC4-M B

CURSOR COUNT UP DISABLE

CC LOAD FROM TC4-L J
CC CNT UP FROM TC4-Y F
CC CNT DWN FROM TC4-Z E

CS LOAD FROM TC4-D 27
COUNT UP FROM TC4-9 9
COUNT DWN FROM TC4-K C

RSET INS TO TC14-BB
1MHz FROM TC2-27
CL SET ARM FROM TC4-T
INHIBIT X FROM TC4-BB
DO PAUSE TO TC4-15
SP EXEC 28 FROM TC4-22
COMPOSE FROM TC4-20
TC IN STRB FROM TC19-25
SP KSE FROM TC4-24

KSE TO TC2-24
SP RSET X TO TC12-BB
EXEC TO TC14-25
SP EXEC X TO TC12-15
SET TO TC4-11, TC14-17
CLEAR TO TC14-19
AGREE TO TC4-FF, TC15-25, TC16-25, TC17-25
AGREE TO TC14-CC
SP STRIP TO TC9-M, TC10-1
FULL LITE TO TC1-12
INITIAL TO TC4-DD
SP SEND TO TC1-W, TC4-V, J222-18 TC19-CC
SP XMT STR TO TC2-Z
SEND TO TC2-7, J222-23

EDIT FF FROM TC4-N
INITIAL FROM TC1-D
CLEAR FROM TC4-14
HOME FROM TC1-5
SEND FROM TC1-Z
SEND SCRN FROM J222-1
SP STROB FROM TC4-28
RESET SND FROM J222-29

A4

4002A DRAWER

FIG 5-43 SCRATCH PAD COUNTER TC-5
CIRCUIT CARD #670-1438-01

670-1438-01

EITHER A SCRATCH PAD CONTROL OR A BYPASS CARD MUST BE USED.

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	
7405	15	7	
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7473	4	11	HIGH
74H74	14	7	HIGH
7485	16	8	LOW
74193	16	8	LOW

TC IN STRB 23 → 22 EXECUTE

+5V → 9 → 24 SP XMT ST
DD KSE
FF SP SEND
BB SP RSET X
V AGREE

W FULL LIGHT
26 SEND
7 SET
13 CLEAR
GND → R → U AGREE

TC-5
SCRATCH PAD COUNTER BYPASS

INSERT FF FROM TC14-16 ← N

SP EXEC FROM TC4-23 ← L
PAUSE FROM TC4-M ← B

CC LOAD FROM TC4-L ← J
CC CNT UP FROM TC4-Y ← F
CC CNT DWN FROM TC4-Z ← E

CS LOAD FROM TC4-D ← 27
COUNT UP FROM TC4-9 ← 9
COUNT DWN FROM TC4-K ← C

RSET INS TO TC14-BB
1MHz FROM TC2-27
CL SET ARM FROM TC4-T
INHIBIT X FROM TC4-BB
SP EXEC FROM TC4-22
COMPOSE FROM TC4-20
TC IN STRB FROM TC19-25
SP KSE FROM TC4-24

U55B 7420N
U31D 7400N
U33B 7400N
U33A 7400N
U13B 7410N
U13C 7410N
END OF MEMORY DETECT
U29E 7404N
U51B 7473N
C2 470
U35A 7473N
END OF MEMORY FF
U53B 7410N
U55A 7420N
U57B 7404N
U59D 7400N
U59A 7400N
EXECUTE
U57C 7404N
U53A 7410N
U35B 7473N
U47C 7402N
SP EXEC
POSITION COUNTER RESET
U27 74193N POSITION COUNTER
U7 74193N POSITION COUNTER
CLEAR SET
U45C 7400N
U45D 7400N
U31B 7400N
U47A 7402N
C4 470
U29B 7404N
U13A 7410N
SEND ENABLE FF
U53C 7410N
U51A 7473N
U43E 7405N
R5 4.7K
U45A 7400N
U25 7485N COMPARATOR
U5 7485N COMPARATOR
U57D 7404N
U59B 7400N
U33D 7400N
U57A 7404N
U49D 7400N

DD → KSE TO TC2-24
BB → SP RSET X TO TC4-15 TC12-BB
22 → EXEC TO TC14-25
20 → SP EXEC X TO TC12-15
7 → SET TO TC4-11, TC14-17
13 → CLEAR TO TC14-19
V → AGREE TO TC4-FF, TC15-25, TC16-25, TC17-25
U → AGREE TO TC14-CC

CURSOR COUNT UP DISABLE
U47B 7402N
U29C 7404N
U23 74193N CURSOR COUNTER
U3 74193N CURSOR COUNTER
U31A 7400N CURSOR COUNT DOWN DISABLE
U29D 7404N
FULL DETECT
U15A 7420N
U29F 7404N
CURSOR COUNTER CLEAR
U31C 7400N
R7 4.7K
U41A 7405N
U37A 7400N
U37B 7400N
U49B 7400N
COMPOSE SEND EXECUTE
U43D 7405N
R10 4.7K
EDIT SEND EXECUTE
U9 7430N EDIT SEND EXECUTE
S P SEND
U49A 7400N
U17A 74H74N SEND INITIATE FF
U17B 74H74N SEND FF
SEND INITIATE GATE
U47D 7402N
SP SEND RESET
U15B 7420N
U33C 7400N
U57F 7404N
CURSOR STORAGE COUNT DOWN ENABLE
U37C 7400N
U57E 7404N
U59C 7400N
U21 74193N CURSOR STORAGE
U1 74193N CURSOR STORAGE
U29A 7404N
U45B 7400N
R20 4.7K
R25 1K
R30 4.7K
U43F 7405N
U41D 7405N
U41B 7405N
U43B 7405N
U43C 7405N
U41E 7405N
U41F 7405N
U41C 7405N
U49C 7400N
CURSOR STORAGE CLEAR
CURSOR ZERO POSITION DETECT
C10 1μF
C11 1μF
C12 1μF
C13 1μF
C14 1μF

W → FULL LITE TO TC1-12
10 → INITIAL TO TC4-DD
FF → SP SEND TO TC1-W, TC4-V, J222-18 TC19-CC
24 → SP XMT STR TO TC2-Z
26 → SEND TO TC2-7, J222-23

M EDIT FF FROM TC4-N
11 INITIAL FROM TC1-D
12 CLEAR FROM TC4-14
21 HOME FROM TC1-5
EE SEND FROM TC1-Z
5 SEND SCRN FROM J222-1
25 SP STROB FROM TC4-28
A RESET SND FROM J222-29

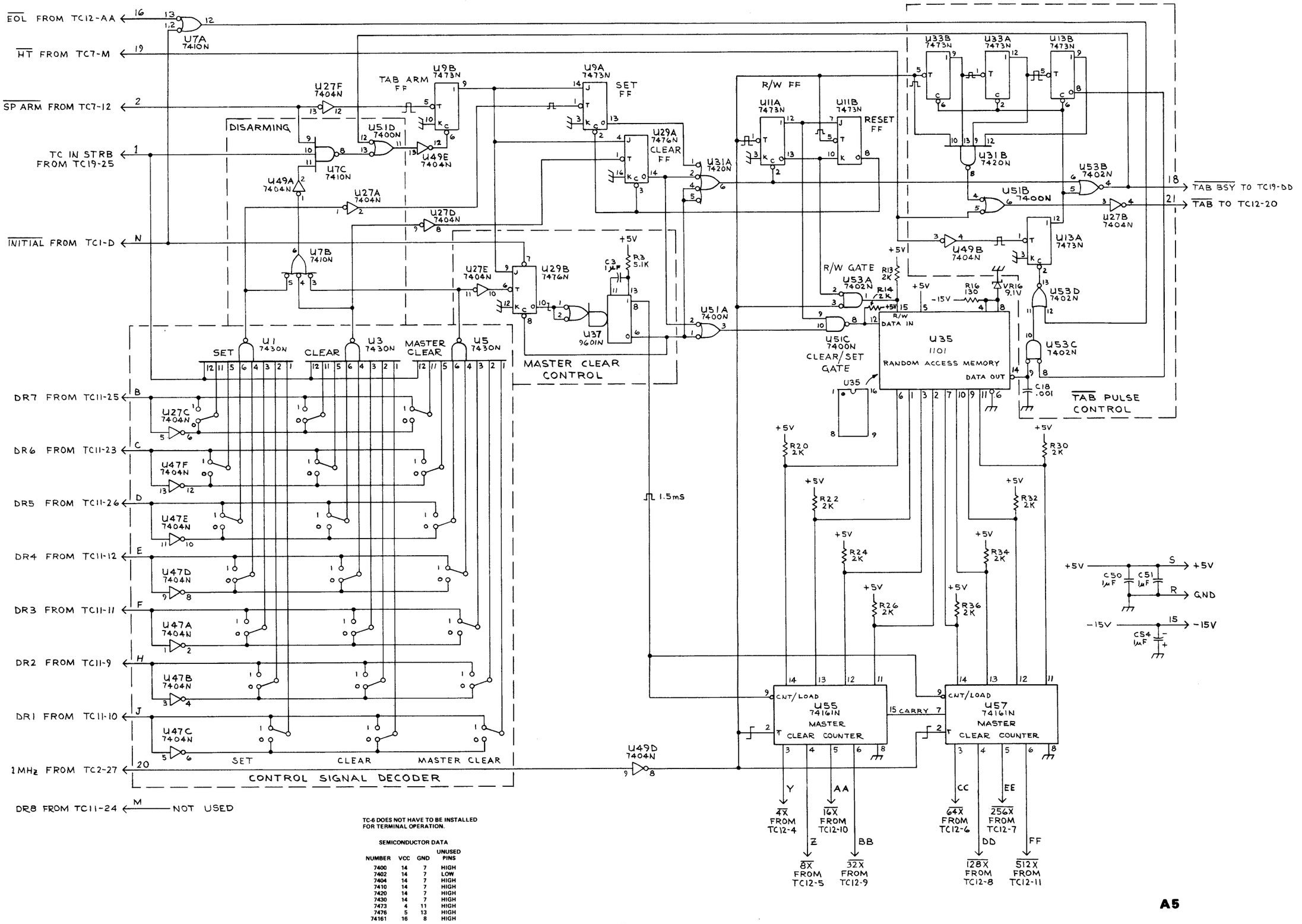
NOTE:
① THESE WIRES NOT CONTAINED ON CIRCUIT CARDS BELOW SN 8070000

A4

Page 5-47A

4002A DRAWER

Ⓐ FIG. 5-43A SCRATCH PAD COUNTER TC-5
CIRCUIT CARD 670-1438-00



TC-6 DOES NOT HAVE TO BE INSTALLED FOR TERMINAL OPERATION.

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH
74161	16	8	HIGH

4002A DRAWER

A5

FIG. 5-44 HORIZONTAL TAB TC-6

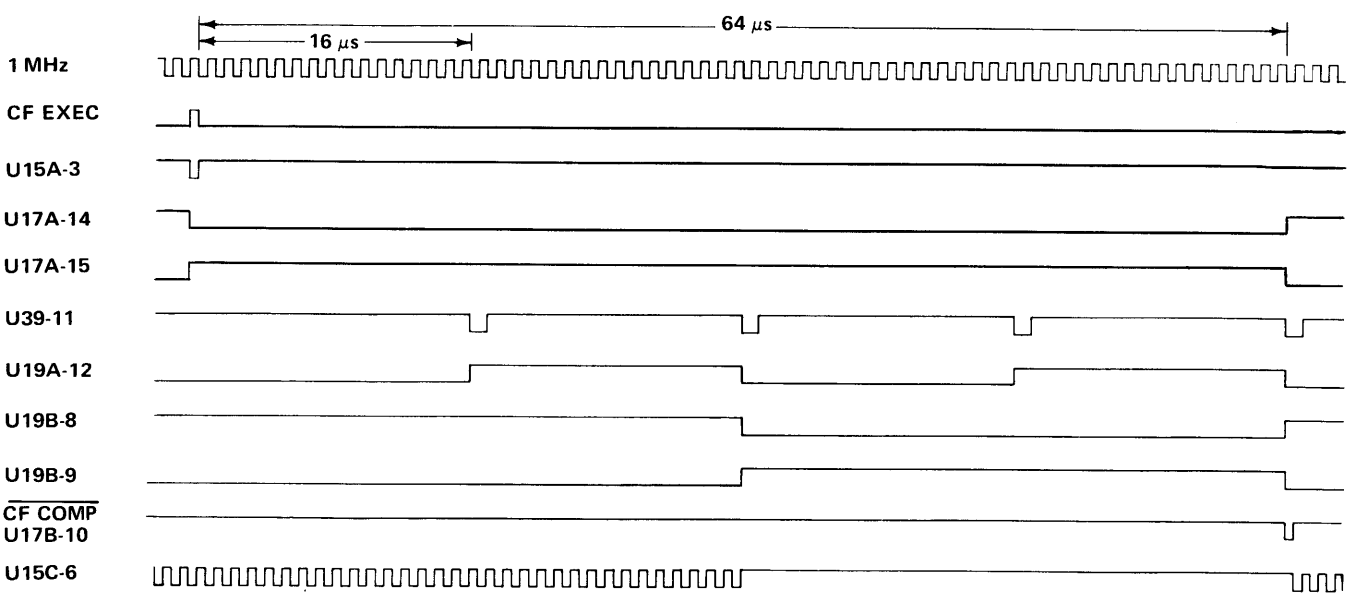
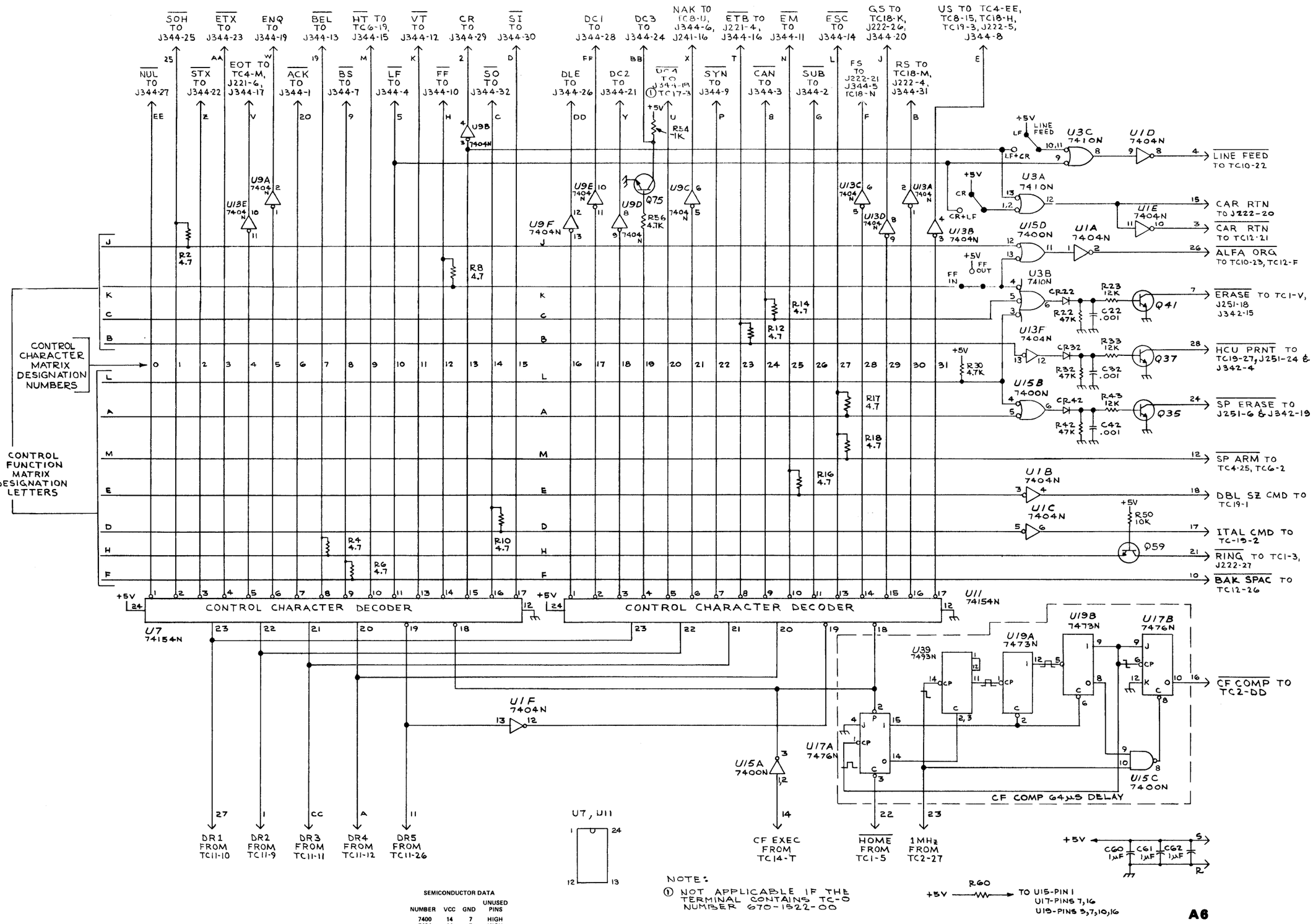


Fig. 5-45. $\overline{\text{CF COMP}}$ 64 μs delay circuit (TC-7).



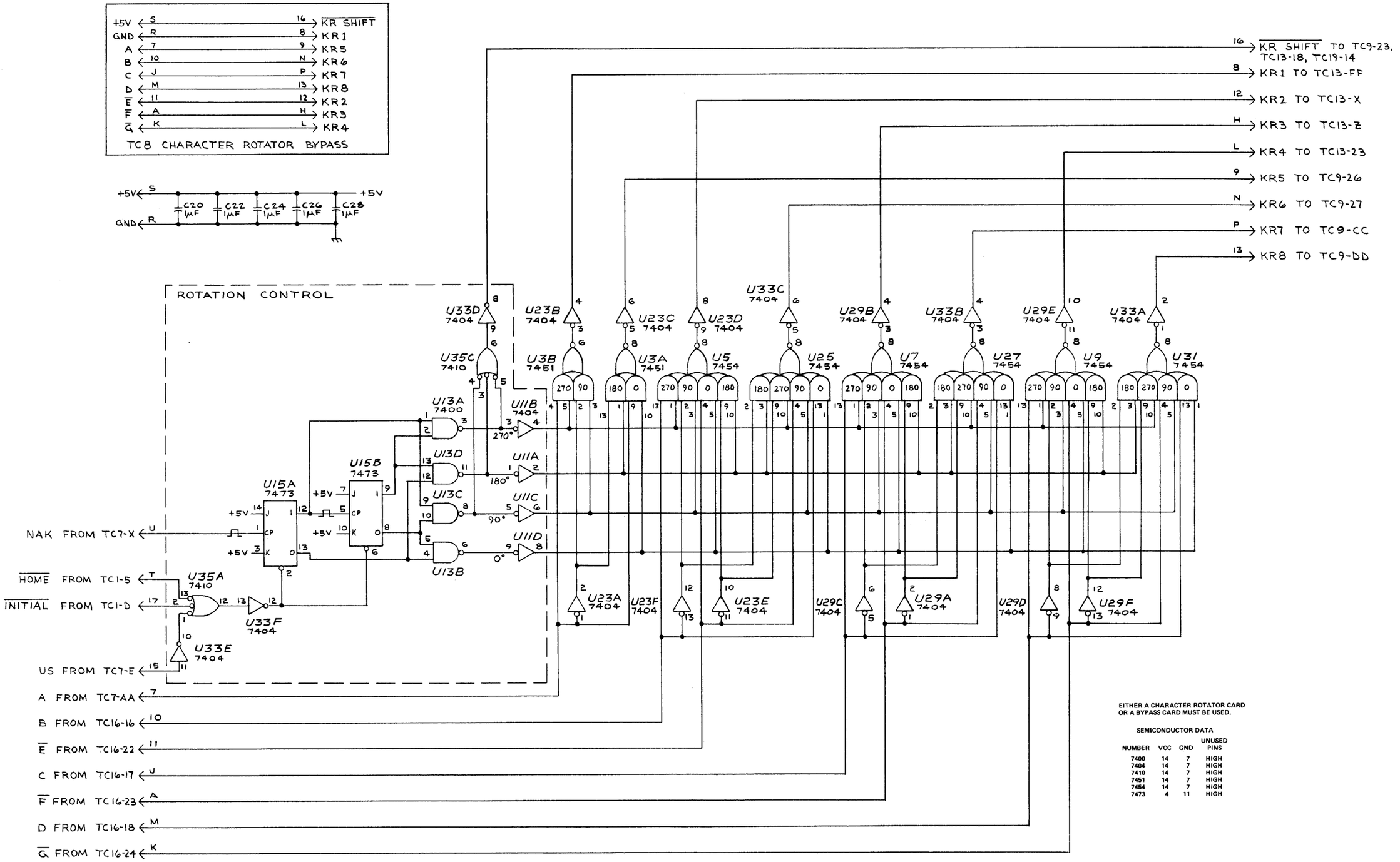
NOTE:
① NOT APPLICABLE IF THE TERMINAL CONTAINS TC-0 NUMBER 670-1522-00

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7404	14	7	HIGH
7410	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH
7493	5	10	LOW
74154	24	12	LOW

4002A DRAWER

FIG 5-46 CONTROL FUNCTION DECODER TC-7



EITHER A CHARACTER ROTATOR CARD OR A BYPASS CARD MUST BE USED.

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7404	14	7	HIGH
7410	14	7	HIGH
7451	14	7	HIGH
7454	14	7	HIGH
7473	4	11	HIGH

A7

4002 A DRAWER

Ⓐ

FIG. 5-47 CHARACTER ROTATOR TC-8

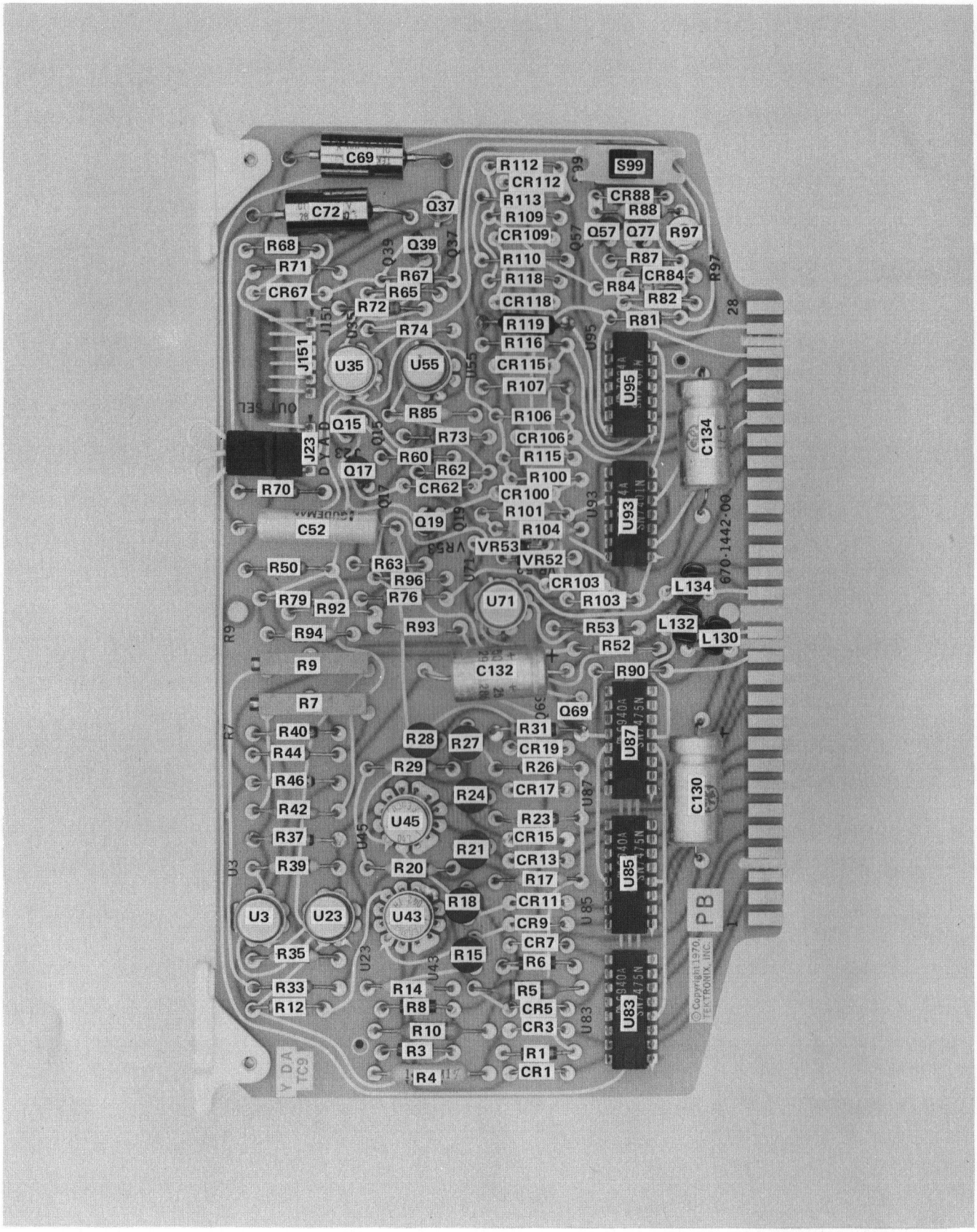
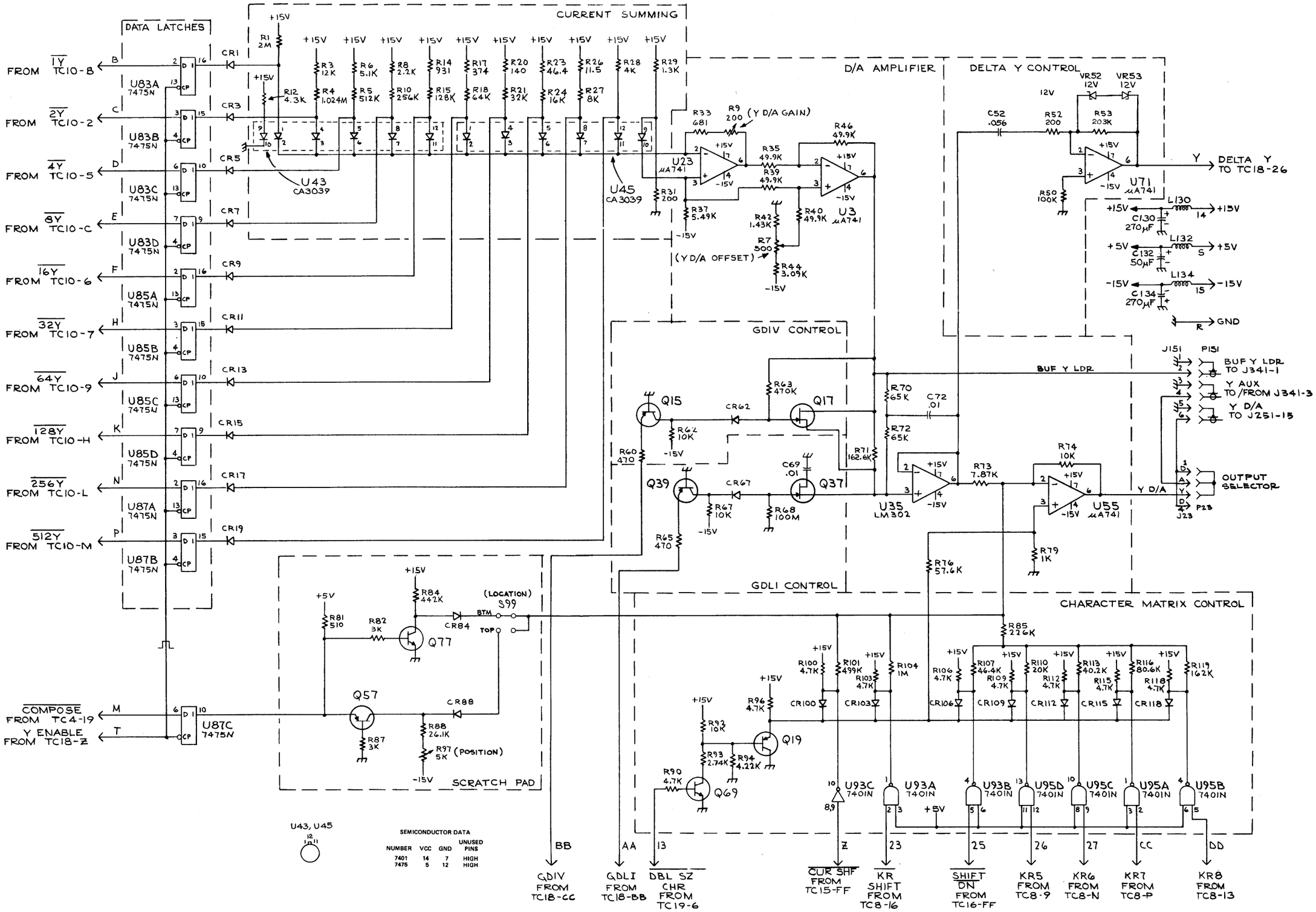


Fig. 5-48. TC9 component illustration.



A8

4002 A DRAWER

Ⓑ

FIG 5-49 Y D/A TC-9

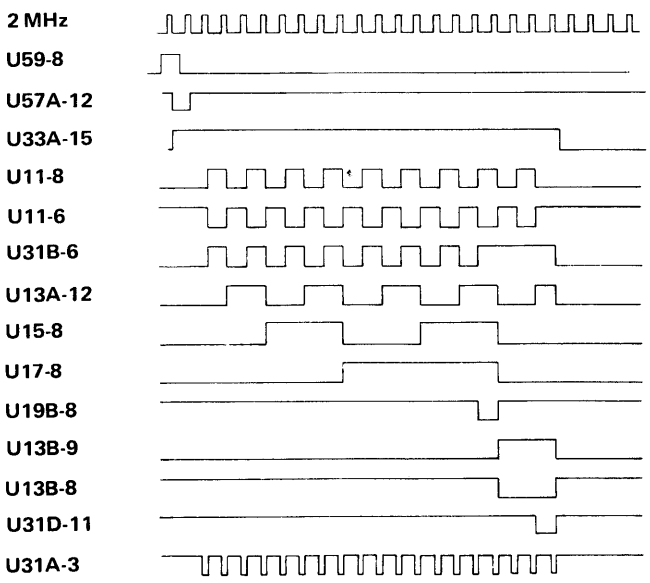
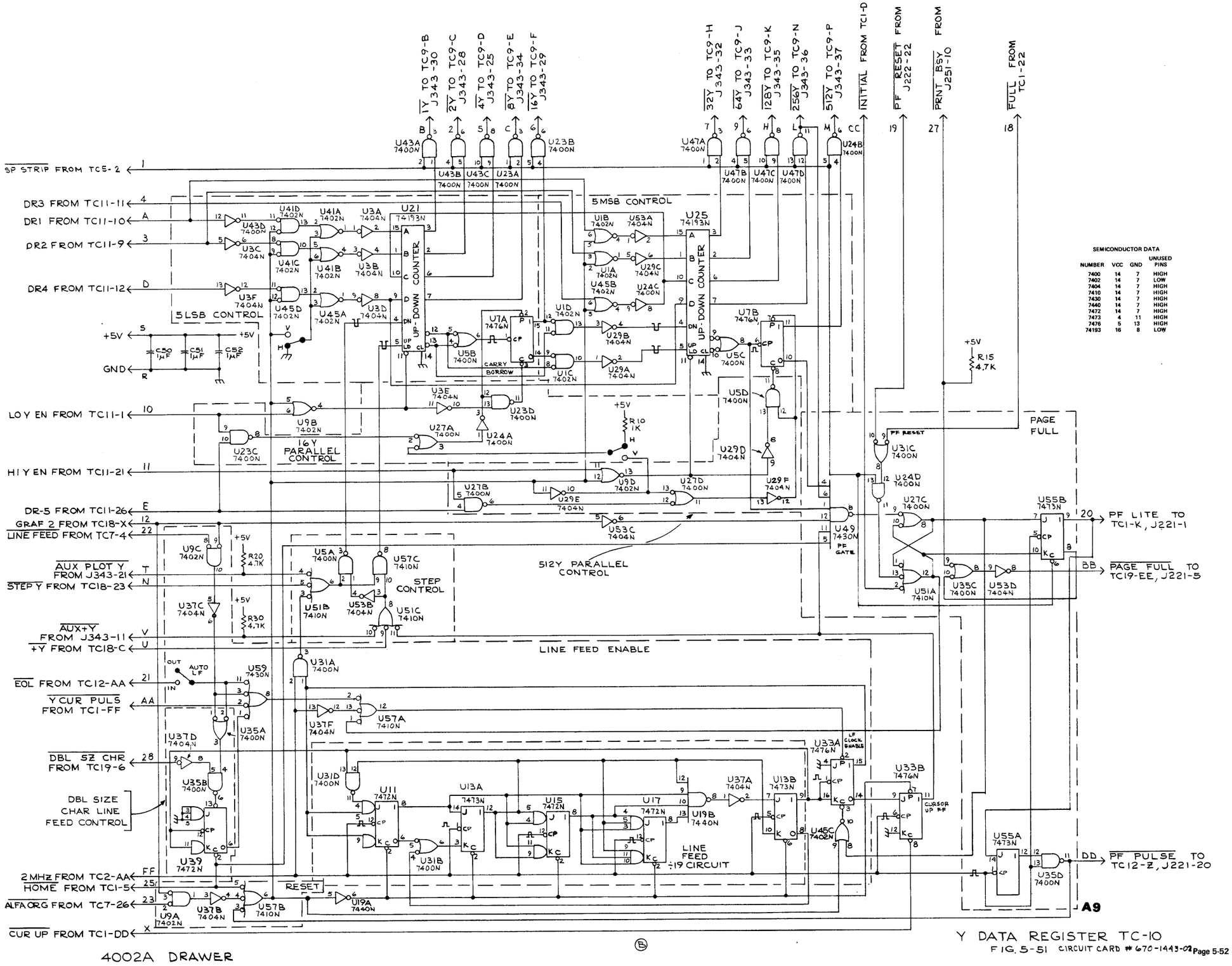


Fig. 5-50. Divide-by-19 counter timing diagram (TC-10).



Y DATA REGISTER TC-10

FIG. 5-51 CIRCUIT CARD # 670-1443-02 Page 5-52

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7430	14	7	HIGH
7440	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH
74193	16	8	LOW

NOTES:
① EXISTS ON CIRCUIT CARD 670-1443-00 ONLY
② EXISTS ON CIRCUIT CARD 670-1443-01 ONLY
③ NOT APPLICABLE IF THE TERMINAL CONTAINS TC-O NUMBER 670-1522-00

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7430	14	7	HIGH
7440	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH
74193	16	8	LOW

TC-10
670-1443-00
670-1443-01

Page 5-52A

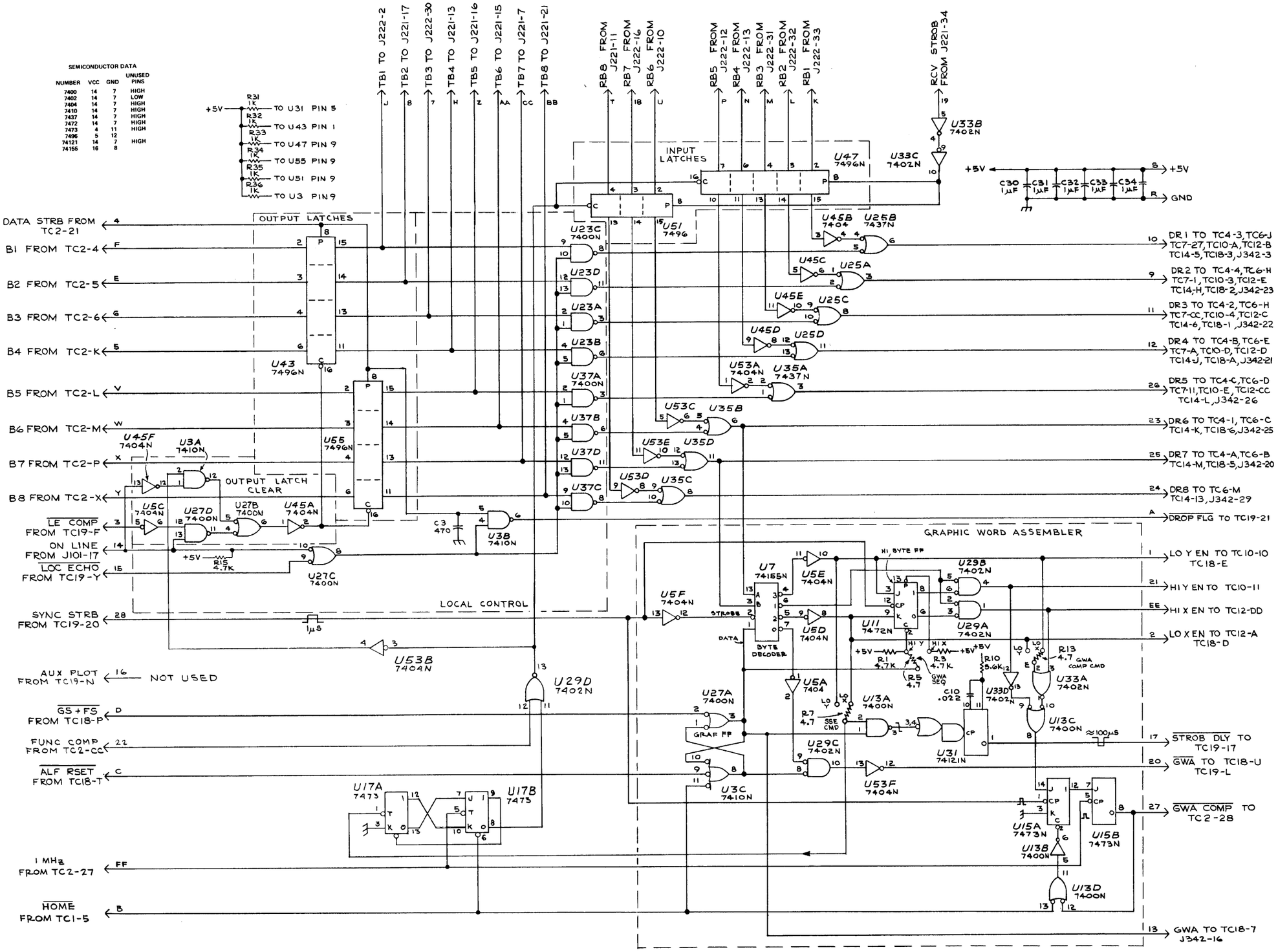
4002A DRAWER

FIG. 5-51A Y DATA REGISTER TC-10
CIRCUIT CARDS 670-1443-00 & 670-1443-01

A9

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7437	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7496	5	12	
74121	14	7	HIGH
74155	16	8	



4002 A DRAWER

A10

IN/OUT DATA ROUTING TC-11 Page 5-53

FIG 5-52 CIRCUIT CARD #670-1444-02 & ABOVE

TC-11
670-1444-02

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7437	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7486	5	12	
74121	14	7	HIGH
74186	16	8	

+5V — R31 1K — TO U31 PIN 5
R32 1K — TO U43 PIN 1
R33 1K — TO U47 PIN 9
R34 1K — TO U55 PIN 9
R35 1K — TO U51 PIN 9
R36 1K — TO 113 PIN 9

TB1 TO J222-2
TB2 TO J221-17
TB3 TO J222-30
TB4 TO J221-13
TB5 TO J221-16
TB6 TO J221-15
TB7 TO J221-7
TB8 TO J221-21

RB8 FROM J221-11
RB7 FROM J222-16
RB6 FROM J222-10
RB5 FROM J222-12
RB4 FROM J222-13
RB3 FROM J222-31
RB2 FROM J222-32
RB1 FROM J222-33

RCV STROB FROM J221-34

INPUT LATCHES

U47 7496N
U51 7496

OUTPUT LATCHES

U43 7496N
U55 7496N

FUNC COMP FROM TC2-CC 22
DATA STRB FROM TC2-21 4
B1 FROM TC2-4 F
B2 FROM TC2-5 E
B3 FROM TC2-6 G
B4 FROM TC2-K S
B5 FROM TC2-L V
B6 FROM TC2-M W
B7 FROM TC2-P X
B8 FROM TC2-X Y
LE COMP FROM TC19-F 3
ON LINE FROM J101-17 14
LOC ECHO FROM TC19-Y 15
AUX PLOT FROM TC19-N 16
SYNC STRB FROM TC19-20 28
GS + FS FROM TC18-P D
ALF RSET FROM TC18-T C
1 MHz FROM TC2-27 FF
HOME FROM TC1-5 B

U45F 7404N
U3A 7410N
U5C 7404N
U27D 7400N
U27B 7400N
U45A 7404N
U5B 7404N
U27C 7400N
U29D 7402N
U3B 7410N
C3 470
1μS
R20 2K
R21 1K
+5V
C21 .001

U23C 7400N
U23D
U23A
U23B
U37A 7400N
U37B
U37D
U37C
U53C U35B
U53E U35D
U53D U35C
U45B 7404 U25B 7437N
U45C U25A
U45E U25C
U45D U25D
U53A 7404N U35A 7437N

U33B 7402N
U33C 7402N

+5V — C30 1μF, C31 1μF, C32 1μF, C33 1μF, C34 1μF — +5V, GND

DR1 TO TC4-3, TC6-J, TC7-27, TC10-A, TC12-B, TC14-5, TC18-3, J342-3 — 10
DR2 TO TC4-4, TC6-H, TC7-1, TC10-3, TC12-E, TC14-H, TC18-2, J342-23 — 9
DR3 TO TC4-2, TC6-H, TC7-CC, TC10-4, TC12-C, TC14-6, TC18-1, J342-22 — 11
DR4 TO TC4-B, TC6-E, TC7-A, TC10-D, TC12-D, TC14-J, TC18-A, J342-21 — 12
DR5 TO TC4-C, TC6-D, TC7-11, TC10-E, TC12-CC, TC14-L, J342-26 — 26
DR6 TO TC4-1, TC6-C, TC14-K, TC18-6, J342-25 — 23
DR7 TO TC4-A, TC6-B, TC14-M, TC18-5, J342-20 — 25
DR8 TO TC6-M, TC14-13, J342-29 — 24
DROP FLG TO TC19-21 — A

GRAPHIC WORD ASSEMBLER

U7 74155N
U5E 7404N
U5F 7404N
U5D 7404N
U11 7472N
U29B 7402N
U29A 7402N
U5A 7404
U13A 7400N
U27A 7400N
GRAF FF
U3C 7410N
U29C 7402N
U53F 7404N
U31 74121N
U33D 7402N
U33A 7402N
U13C 7400N
U15A 7473N
U15B 7473N
U13B 7400N
U13D 7400N

HI Y BYTE FF
STROBE
DATA
BYTE DECODER
R1 4.7K
R3 4.7K
R5 4.7
GWA SEQ
R10 5.6K
R13 4.7 GWA COMP CMD
C10 .022
SSE CMD
≈100μS

LO Y EN TO TC10-10, TC18-E — 1
HI Y EN TO TC10-11 — 21
HI X EN TO TC12-DD — EE
LO X EN TO TC12-A, TC18-D — 2
STROB DLY TO TC19-17 — 17
GWA TO TC18-U, TC19-L — 20
GWA COMP TO TC2-28 — 27
GWA TO TC18-7, J342-16 — 13

4002 A DRAWER

A10 IN/OUT DATA ROUTING TC-11
FIG. 5-52A
CIRCUIT CARD #670-1444-01

TC-11
670-1444-01

5-53A

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7437	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7486	5	12	
74121	14	7	HIGH
74166	16	8	

+5V — R31 1K TO U31 PIN 5; R32 1K TO U43 PIN 1; R33 1K TO U47 PIN 9; R34 1K TO U55 PIN 9; R35 1K TO U51 PIN 9; R36 1K TO U3 PIN 9

TB1 TO J222-2 (L)
TB2 TO J221-17 (B)
TB3 TO J222-30 (J)
TB4 TO J221-13 (Z)
TB5 TO J221-16 (N)
TB6 TO J221-15 (AA)
TB7 TO J221-7 (CC)
TB8 TO J221-21 (BB)

RB8 FROM J221-11 (T)
RB7 FROM J222-16 (R)
RB6 FROM J222-10 (C)
RB5 FROM J222-12 (P)
RB4 FROM J222-13 (N)
RB3 FROM J222-31 (M)
RB2 FROM J222-32 (F)
RB1 FROM J222-33 (K)
RCV STROB FROM J221-34 (19)

U33B 7402N (5, 4, 6)

INPUT LATCHES
U47 7496N
U33C 7402N (9, 10)

+5V — C30 1µF, C31 1µF, C32 1µF, C33 1µF, C34 1µF — S +5V, R GND

U53B 7404N (3, 4)

FUNC COMP FROM TC2-CC (22)
DATA STRB FROM TC2-21 (4)
B1 FROM TC2-4 (F)
B2 FROM TC2-5 (E)
B3 FROM TC2-6 (G)
B4 FROM TC2-K (S)
B5 FROM TC2-L (V)
B6 FROM TC2-M (W)
B7 FROM TC2-P (X)
B8 FROM TC2-X (Y)

OUTPUT LATCHES
U43 7496N
U55 7496N

U51 7496
U23C 7400N (9, 10, 8)
U23D (12, 13, 11)
U23A (2, 1, 3)
U23B (4, 5, 6)
U37A 7400N (2, 1, 3)
U37B (4, 5, 6)
U37D (12, 13, 11)
U37C (9, 10, 8)

U45B 7404 (3, 4); U25B 7437N (4, 5, 6)
U45C (5, 6); U25A (1, 2, 3)
U45E (11, 10); U25C (9, 10, 8)
U45D (9, 8); U25D (12, 13, 11)
U53A 7404N (1, 2); U35A 7437N (2, 1, 3)
U53C (5, 6); U35B (5, 4, 6)
U53E (11, 10); U35D (12, 13, 11)
U53D (9, 8); U35C (9, 10, 8)

10 DR1 TO TC4-3, TC6-J, TC7-27, TC10-A, TC12-B, TC14-5, TC18-3, J342-3
9 DR2 TO TC4-4, TC6-H, TC7-1, TC10-3, TC12-E, TC14-H, TC18-2, J342-23
11 DR3 TO TC4-2, TC6-H, TC7-CC, TC10-4, TC12-C, TC14-6, TC18-1, J342-22
12 DR4 TO TC4-B, TC6-E, TC7-A, TC10-D, TC12-D, TC14-J, TC18-A, J342-21
26 DR5 TO TC4-C, TC6-D, TC7-11, TC10-E, TC12-CC, TC14-L, J342-26
23 DR6 TO TC4-1, TC6-C, TC14-K, TC18-6, J342-25
25 DR7 TO TC4-A, TC6-B, TC14-M, TC18-5, J342-20
24 DR8 TO TC6-M, TC14-13, J342-29
A DROP FLG TO TC19-21

U45F 7404N (X, Y); U3A 7410N (2, 1, 12); OUTPUT LATCH CLEAR

LE COMP FROM TC19-F (3)
ON LINE FROM J101-17 (14)
LOC ECHO FROM TC19-Y (15)
AUX PLOT FROM TC19-N (16)
SYNC STRB FROM TC19-20 (28)

U5C 7404N (5, 6); U27D 7400N (12, 11, 13); U27B 7400N (5, 4, 6); U45A 7404N (1, 2)
+5V — R15 4.7K
U27C 7400N (10, 9, 8); U5B 7404N (3, 4); U29D 7402N (11, 12, 13)
C3 470
U38 7410N (5, 4, 6)
1µs

LOCAL CONTROL

GRAPHIC WORD ASSEMBLER

SELECT A; SELECT B
U7 74155N
U5F 7404N (13, 12); STROBE; DATA; BYTE DECODER
U5E 7404N (11, 10); U5D 7404N (5, 9, 8)
HI BYTE FF
U11 7472N
U29B 7402N (5, 6, 4); U29A 7402N (2, 1, 3)
+5V — R1 4.7K; R3 4.7K; R5 4.7 GWA SEQ; R10 5.6K; R13 4.7 GWA COMP CMD
HI Y; HI X; LO Y; LO X
U5A 7404 (2, 1); U33A 7402N (E, E, 3)
U33D 7402N (13, 12)
C10 .022
U13A 7400N (2, 1, 3); R7 4.7 SSE CMD
U29C 7402N (9, 10, 8); U53F 7404N (13, 12)
U31 7412N (CP)
U13C 7400N (10, 9, 8) ≈100µs
U27A 7400N (2, 1, 3); GRAF FF
U3C 7410N (10, 9, 11)
U15A 7473N (J, CP, K, C); U15B 7473N (J, CP, K, C)
U13B 7400N (6, 5)
U13D 7400N (11, 13, 12)

GS + FS FROM TC18-P (D)
ALF RSET FROM TC18-T (C)
1 MHz FROM TC2-27 (FF)
HOME FROM TC1-5 (B)

1 LO Y EN TO TC10-10, TC18-E
21 HI Y EN TO TC10-11
EE HI X EN TO TC12-DD
2 LO X EN TO TC12-A, TC18-D
17 STROB DLY TO TC19-17
20 GWA TO TC18-U, TC19-L
27 GWA COMP TO TC2-28
13 GWA TO TC18-7, J342-16

4002 A DRAWER

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A10

FIG. 5-52B IN/OUT DATA ROUTING TC-11
CIRCUIT CARD 670-1444-00

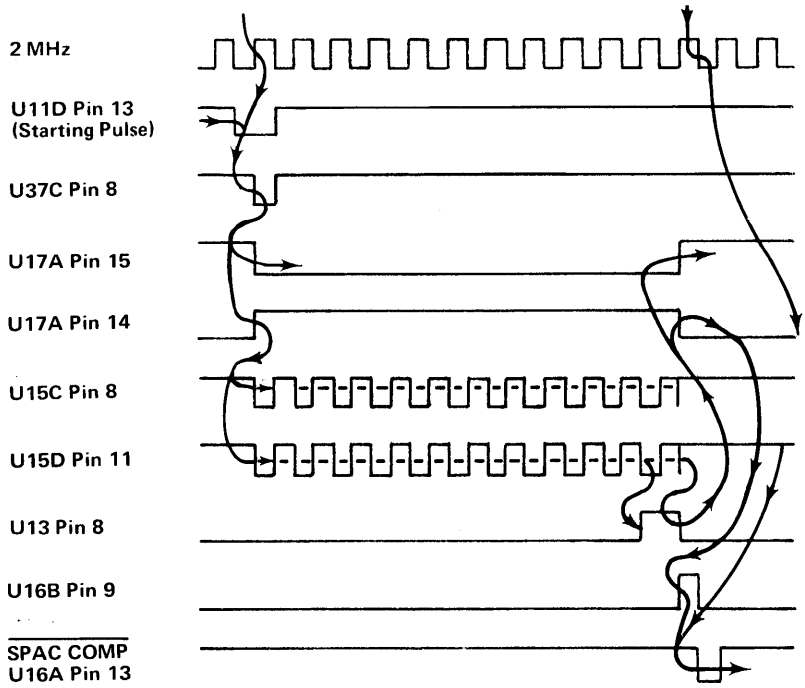
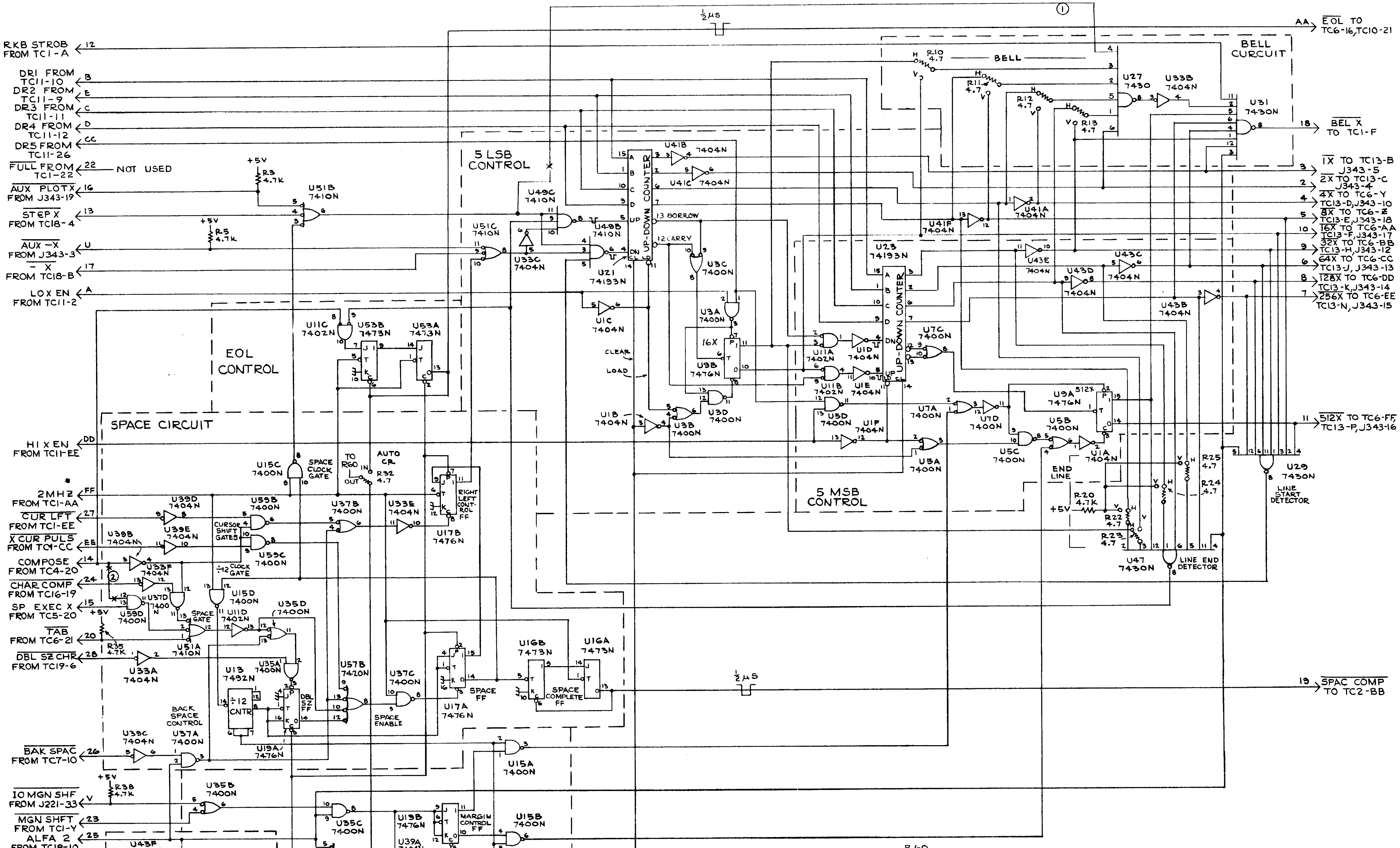
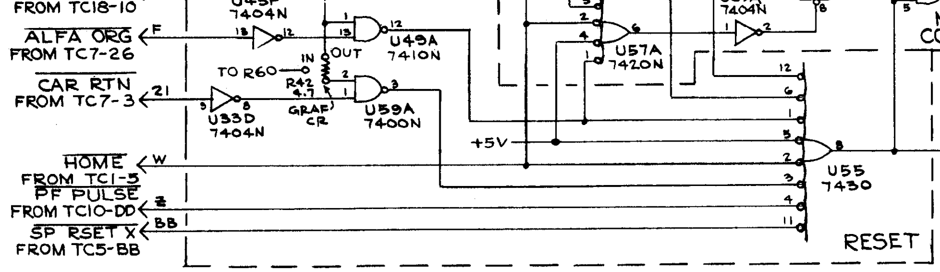
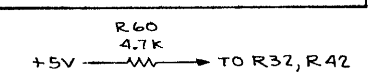
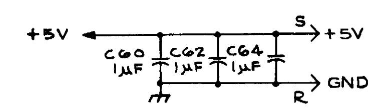


Fig. 5-53. Space circuit timing (TC-12).







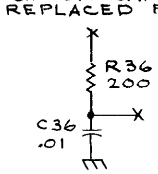


SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH
7492	5	10	LOW
74193	16	8	LOW

① THIS LINE DOES NOT EXIST IN CIRCUIT CARD 670-1445-00. U27 PIN 4 THEN CONNECTS TO +5V.

② ON CIRCUIT CARD 670-1445-00 THIS LINE IS REPLACED BY THE FOLLOWING CIRCUIT:



A11

4002A DRAWER

(B)

FIG. 5-54 X DATA REGISTER TC-12

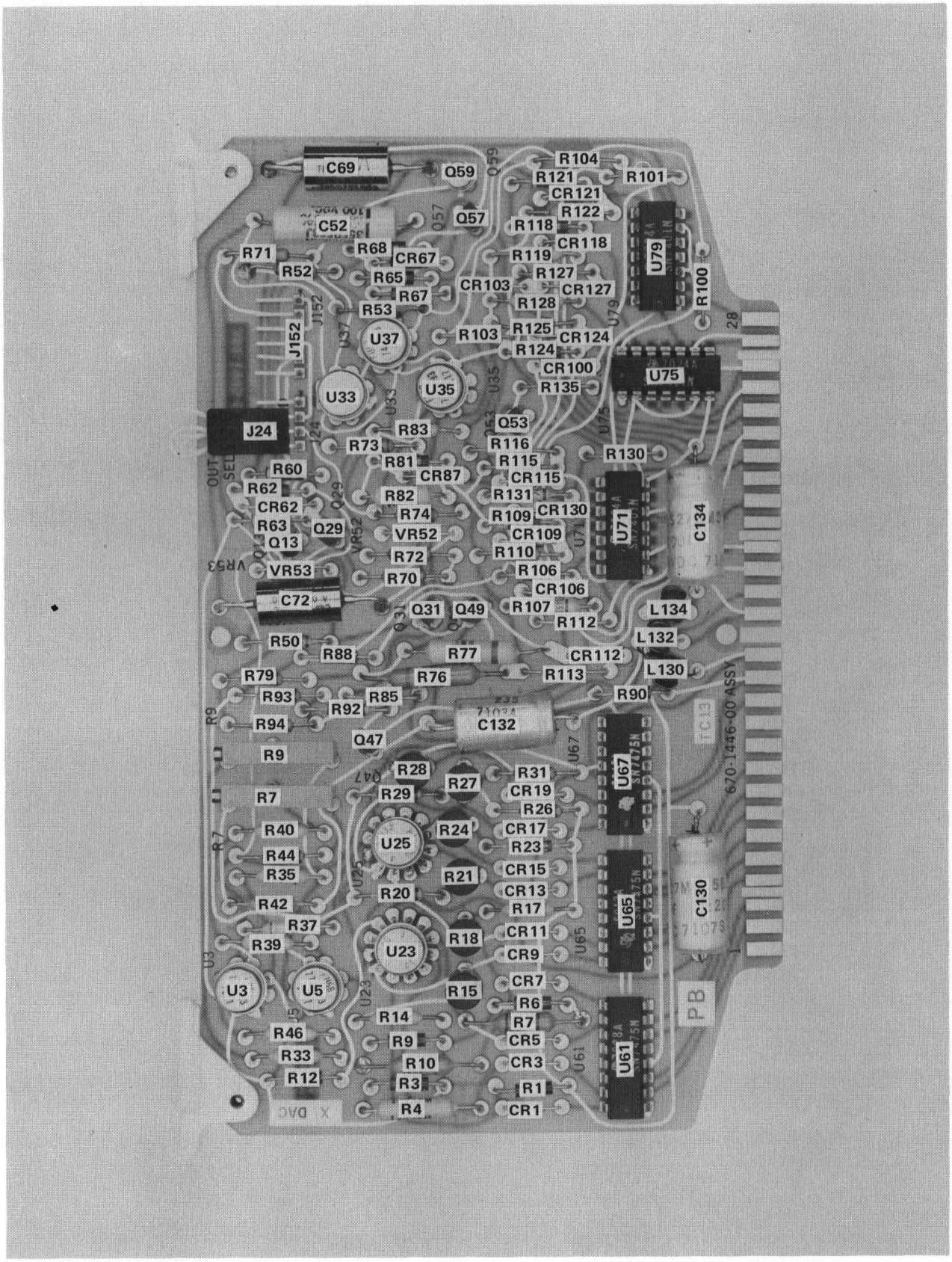


Fig. 5-55. TC13 component illustration.

DATA LATCHES

CURRENT SUMMING

D/A AMPLIFIER

DELTA X CONTROL

GDIV CONTROL

GDLI CONTROL

ITALICS CONTROL

CHARACTER MATRIX CONTROL

DBL SIZE & CURSOR SHIFT CONTROL

FROM $\overline{1X}$ TC12-3 — U61A 7475N

FROM $\overline{2X}$ TC12-2 — U61B 7475N

FROM $\overline{4X}$ TC12-4 — U61C 7475N

FROM $\overline{8X}$ TC12-5 — U61D 7475N

FROM $\overline{16X}$ TC12-10 — U65A 7475N

FROM $\overline{32X}$ TC12-9 — U65B 7475N

FROM $\overline{64X}$ TC12-6 — U65C 7475N

FROM $\overline{128X}$ TC 12-8 — U65D 7475N

FROM $\overline{256X}$ TC12-7 — U67A 7475N

FROM $\overline{512X}$ TC12-11 — U67B 7475N

FROM X ENABLE TC18-Y

FROM GDIV TC18-CC

FROM GDLI TC18-BB

FROM $\overline{CUR\ SHF}$ TC15-FF

FROM $\overline{DBL\ SZ\ CHR}$ TC19-6

U23 CA3039

U25 CA3039

U5 µA741

U3 µA741

U37 µA741

U33 LM302

U35 µA741

DELTA X TO TC18-25

BUF X LDR

BUF X LDR TO J341-2

X AUX TO/FROM J341-4

X D/A TO J251-1

OUTPUT SELECTOR

J152 P152

J24 P24

KR1 FROM TC8-8

$\overline{KR}$ SHIFT FROM TC8-16

KR2 FROM TC8-12

KR3 FROM TC8-H

KR4 FROM TC8-L

SHIFT DN FROM TC16-FF

A FROM TC16-AA

B FROM TC16-16

C FROM TC16-17

D FROM TC16-8

ITALIC FROM TC19-11

U23,U25

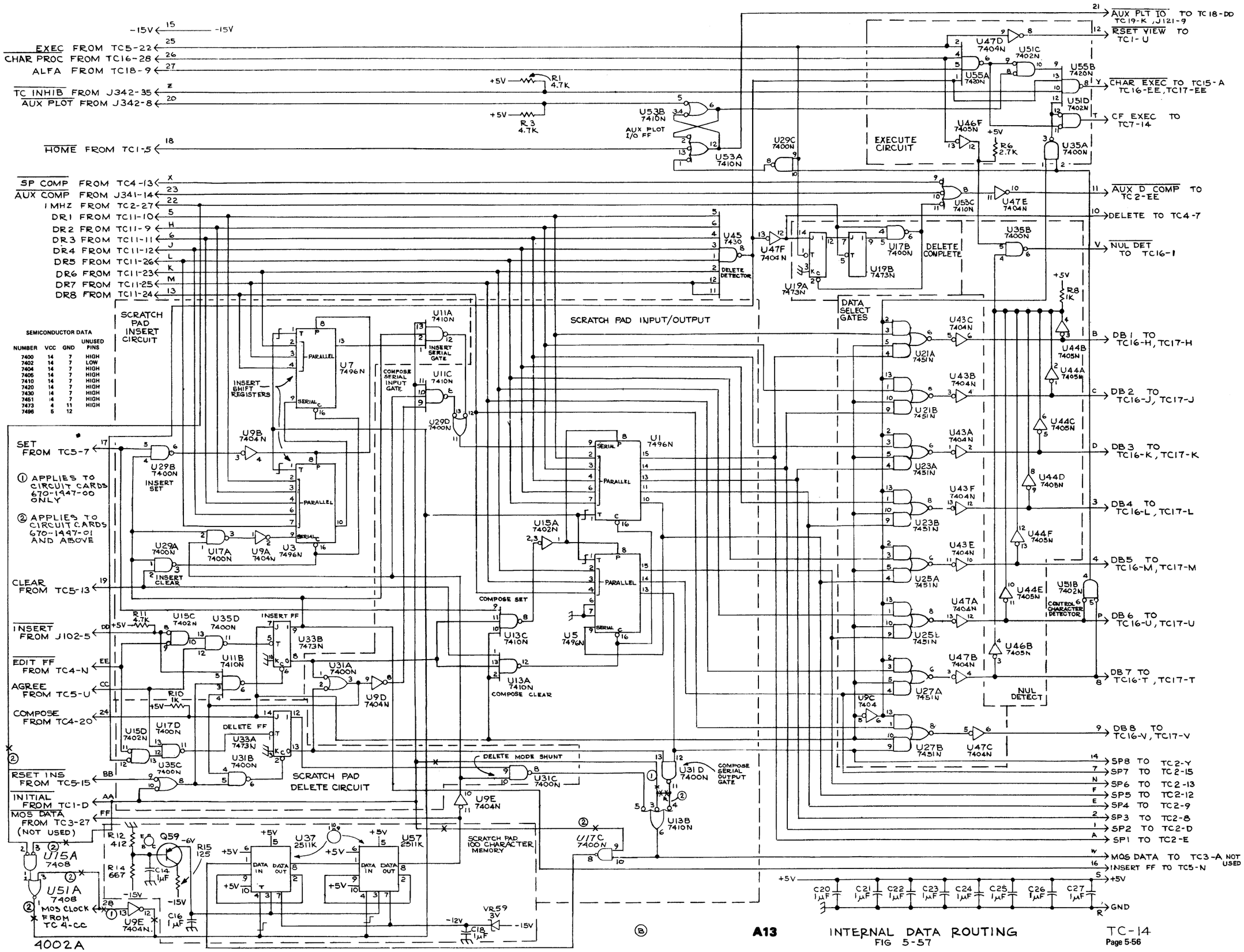
SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7401	14	7	HIGH
7475	5	12	HIGH

A12

4002 A DRAWER

FIG 5-56 X D/A TC13


-15V
EXEC FROM TC5-22
CHAR PROC FROM TC16-28
ALFA FROM TC18-9
TC INHIB FROM J342-35
AUX PLOT FROM J342-8
HOME FROM TC1-5
SP COMP FROM TC4-13
AUX COMP FROM J341-14
1 MHZ FROM TC2-27
DR1 FROM TC11-10
DR2 FROM TC11-9
DR3 FROM TC11-11
DR4 FROM TC11-12
DR5 FROM TC11-26
DR6 FROM TC11-23
DR7 FROM TC11-25
DR8 FROM TC11-24
+5V
R1 4.7K
R3 4.7K
U53B 7410N
AUX PLOT I/O FF
U53A 7410N
U29C 7400N
EXECUTE CIRCUIT
U47D 7404N
U51C 7402N
U55A 7420N
U55B 7420N
U51D 7402N
U46F 7405N
R6 2.7K
U35A 7400N
AUX PLT IO TO TC18-DD
TC19-K, J121-9
RSET VIEW TO TC1-U
CHAR EXEC TO TC15-A
TC16-EE, TC17-EE
CF EXEC TO TC7-14
U53C 7410N
U47E 7404N
AUX D COMP TO TC2-EE
DELETE TO TC4-7
U45 7430
DELETE DETECTOR
U47F 7404N
U19A 7473N
U17B 7400N
U19B 7473N
DELETE COMPLETE
U35B 7400N
NUL DET TO TC16-I
SCRATCH PAD INSERT CIRCUIT
SCRATCH PAD INPUT/OUTPUT
DATA SELECT GATES
R8 1K
U44B 7405N
U44A 7405N
U44C 7405N
U44D 7405N
U44F 7405N
U44E 7405N
U51B 7402N
CONTROL CHARACTER DETECTOR
U46B 7405N
NUL DETECT
U43C 7404N
U21A 7451N
DB1 TO TC16-H, TC17-H
U43B 7404N
U21B 7451N
DB2 TO TC16-J, TC17-J
U43A 7404N
U23A 7451N
DB3 TO TC16-K, TC17-K
U43F 7404N
U23B 7451N
DB4 TO TC16-L, TC17-L
U43E 7404N
U25A 7451N
DB5 TO TC16-M, TC17-M
U47A 7404N
U25B 7451N
DB6 TO TC16-U, TC17-U
U47B 7404N
U27A 7451N
DB7 TO TC16-T, TC17-T
U9C 7404
U27B 7451N
U47C 7404N
DB8 TO TC16-V, TC17-V
SP8 TO TC2-Y
SP7 TO TC2-15
SP6 TO TC2-13
SP5 TO TC2-12
SP4 TO TC2-9
SP3 TO TC2-8
SP2 TO TC2-D
SP1 TO TC2-E
MOS DATA TO TC3-A NOT USED
INSERT FF TO TC5-N
+5V
GND
C20 1µF
C21 1µF
C22 1µF
C23 1µF
C24 1µF
C25 1µF
C26 1µF
C27 1µF
SEMICONDUCTOR DATA
NUMBER VCC GND UNUSED PINS
7400 14 7 HIGH
7402 14 7 LOW
7404 14 7 HIGH
7405 14 7 HIGH
7410 14 7 HIGH
7420 14 7 HIGH
7430 14 7 HIGH
7451 14 7 HIGH
7473 4 11 HIGH
7496 5 12
U7 7496N
U3 7496N
U1 7496N
U5 7496N
PARALLEL
SERIAL
INSERT SHIFT REGISTERS
U11A 7410N
INSERT SERIAL GATE
COMPOSE SERIAL INPUT GATE
U11C 7410N
U29D 7400N
U9B 7404N
U29B 7400N
INSERT SET
U29A 7400N
INSERT CLEAR
U17A 7400N
U9A 7404N
U15A 7402N
COMPOSE SET
U13C 7410N
U13A 7410N
COMPOSE CLEAR
U15A 7402N
U51A 7408
MOS CLOCK FROM TC 4-CC
U9E 7404N
SET FROM TC5-7
CLEAR FROM TC5-13
INSERT FROM J102-5
EDIT FF FROM TC4-N
AGREE FROM TC5-U
COMPOSE FROM TC4-20
RSET INS FROM TC5-15
INITIAL FROM TC1-D
MOS DATA FROM TC3-27 (NOT USED)
R11 4.7K
R10 1K
R12 412
R14 667
R15 125
C14 1µF
C16 1µF
C18 1µF
Q59 -6V
VR59 3V
U15C 7402N
U35D 7400N
INSERT FF
U33B 7473N
U11B 7410N
U31A 7400N
U9D 7404N
U15D 7402N
U17D 7400N
U35C 7400N
DELETE FF
U33A 7473N
U31B 7400N
SCRATCH PAD DELETE CIRCUIT
DELETE MODE SHUNT
U31C 7400N
U9E 7404N
U31D 7400N
COMPOSE SERIAL OUTPUT GATE
U13B 7410N
U17C 7400N
SCRATCH PAD 100 CHARACTER MEMORY
U37 2511K
U57 2511K
DATA IN
DATA OUT
① APPLIES TO CIRCUIT CARDS 670-1447-00 ONLY
② APPLIES TO CIRCUIT CARDS 670-1447-01 AND ABOVE
4002A
Ⓑ
A13
INTERNAL DATA ROUTING
FIG 5-57
TC-14
Page 5-56
TC-14

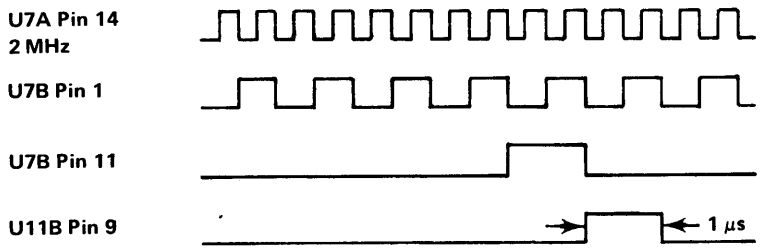
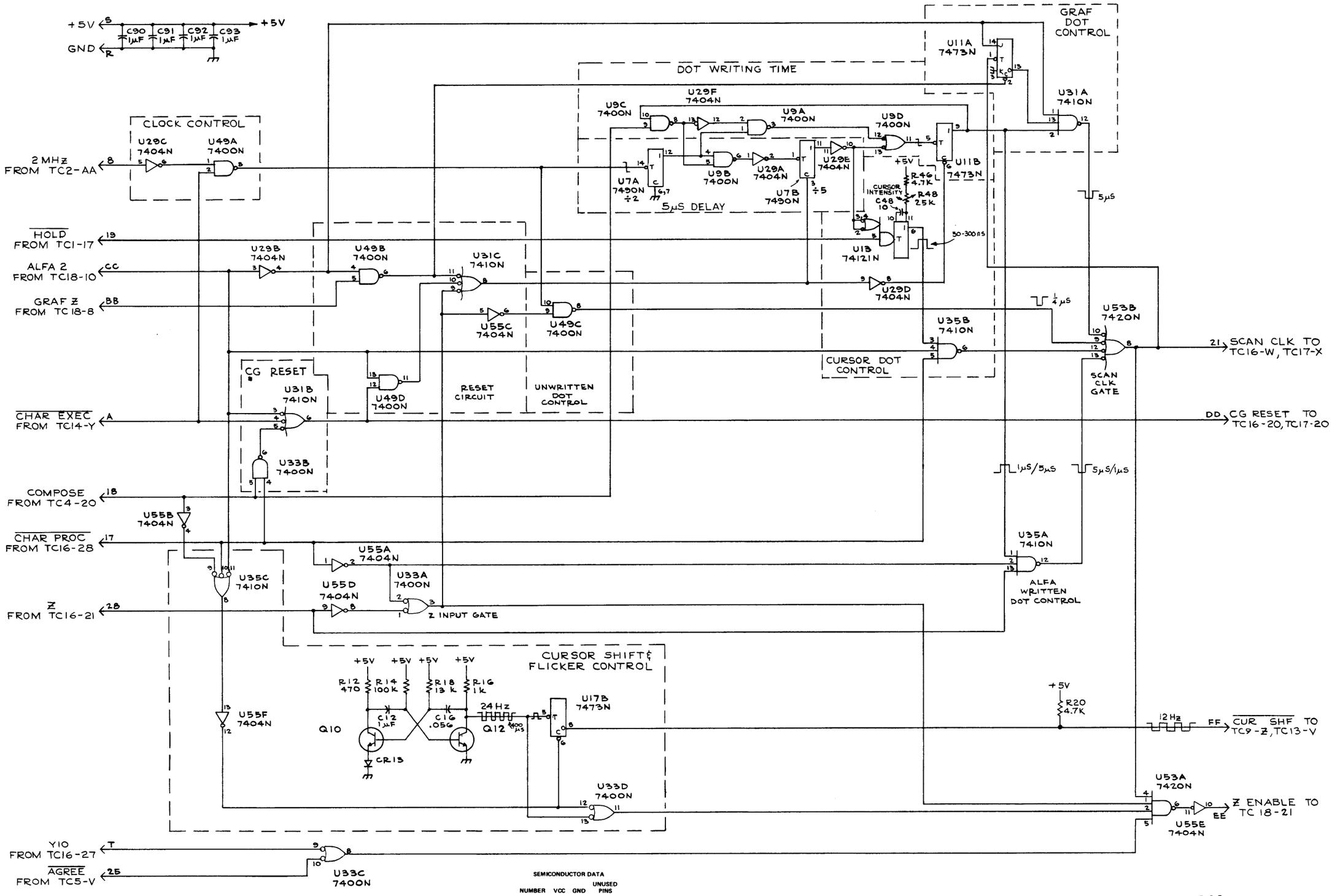


Fig. 5-58. 5μs Delay and Dot Writing time (TC-15).



SEMICONDUCTOR DATA

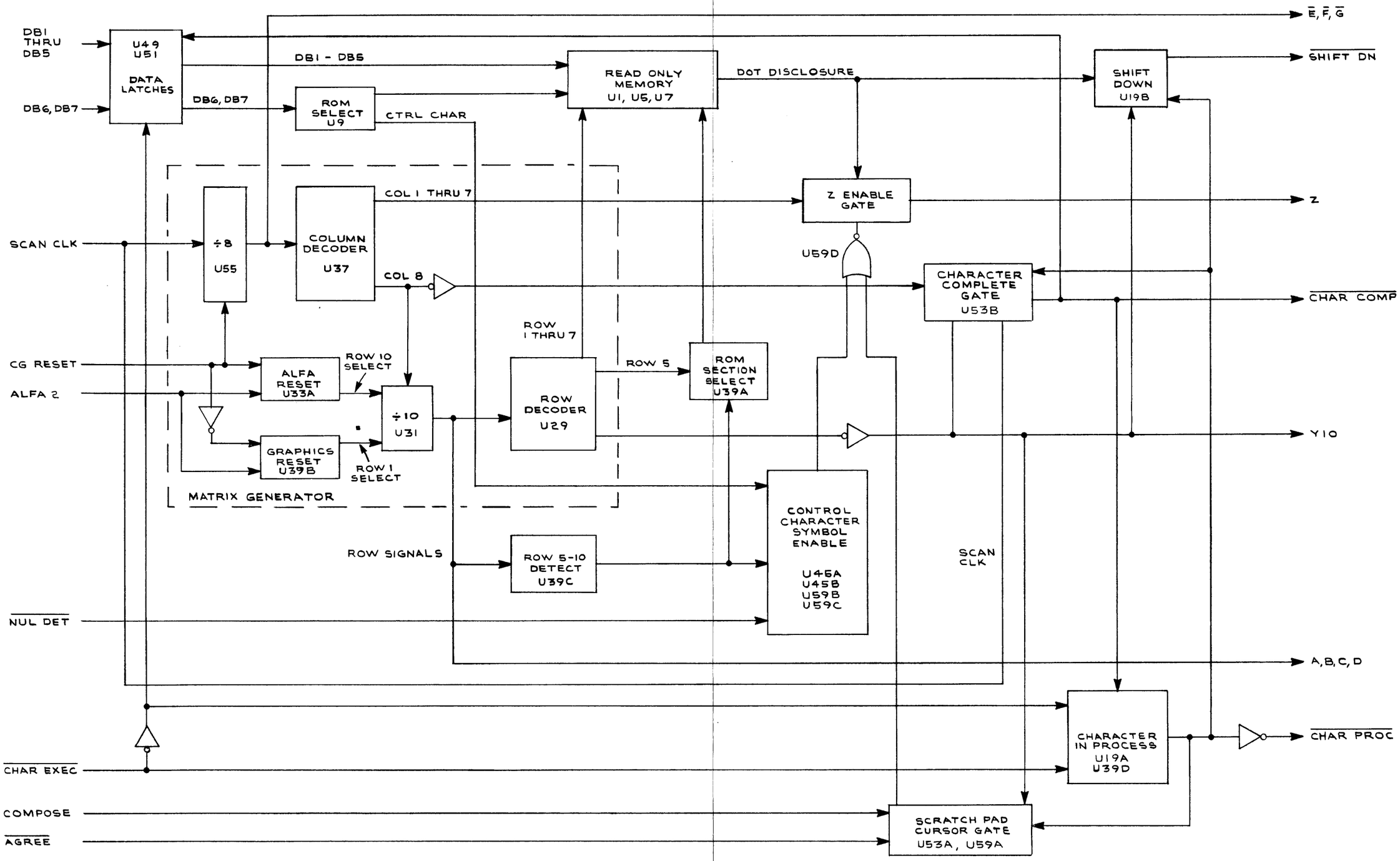
NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7404	14	7	HIGH
7410	14	7	HIGH
7420	14	7	HIGH
7473	14	7	HIGH
7490	5	10	HIGH
74121	14	7	HIGH

A14

4002A DRAWER

CHARACTER GENERATOR CONTROL TC-15

FIG 5-59



4002A DRAWER

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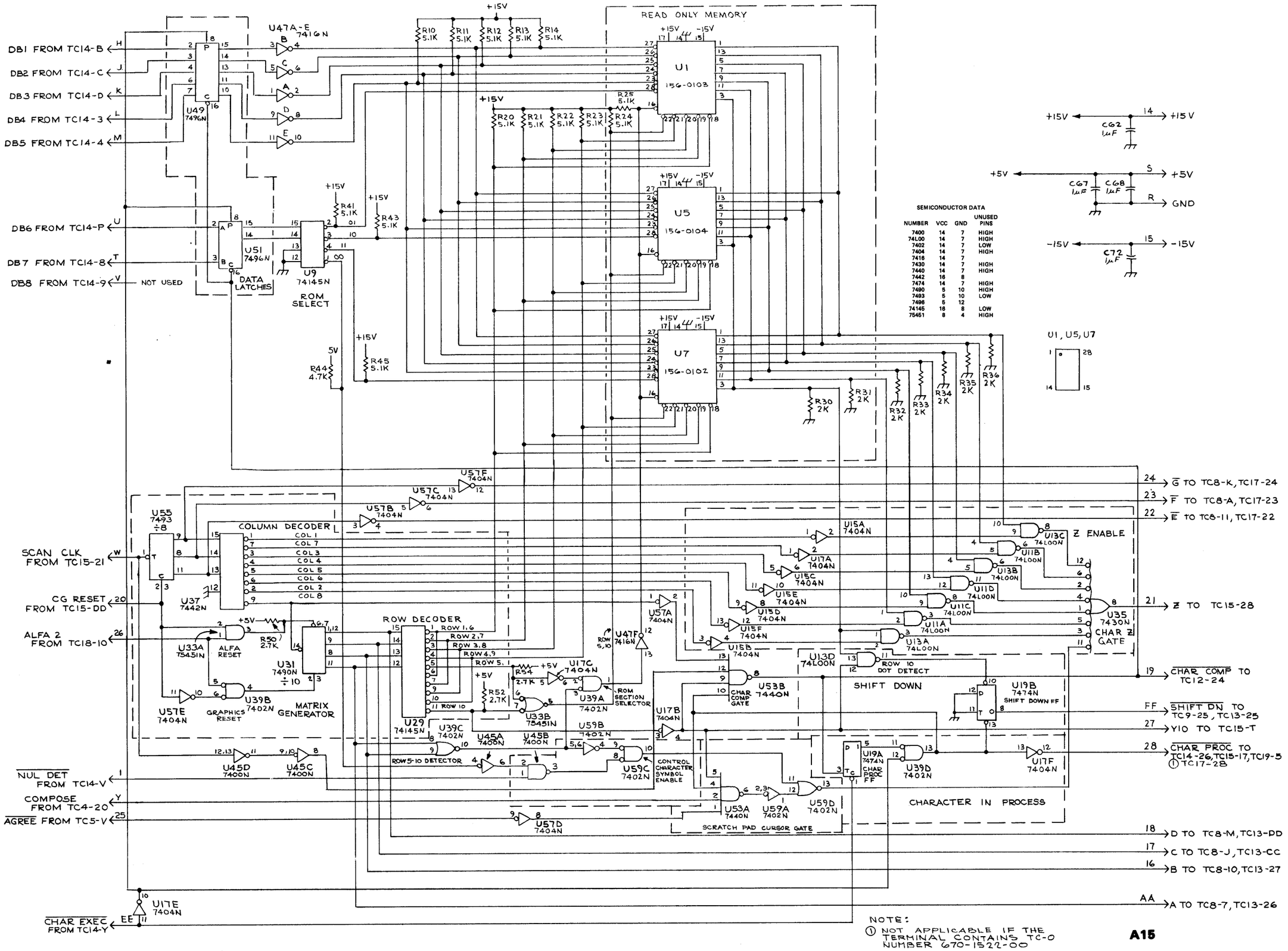
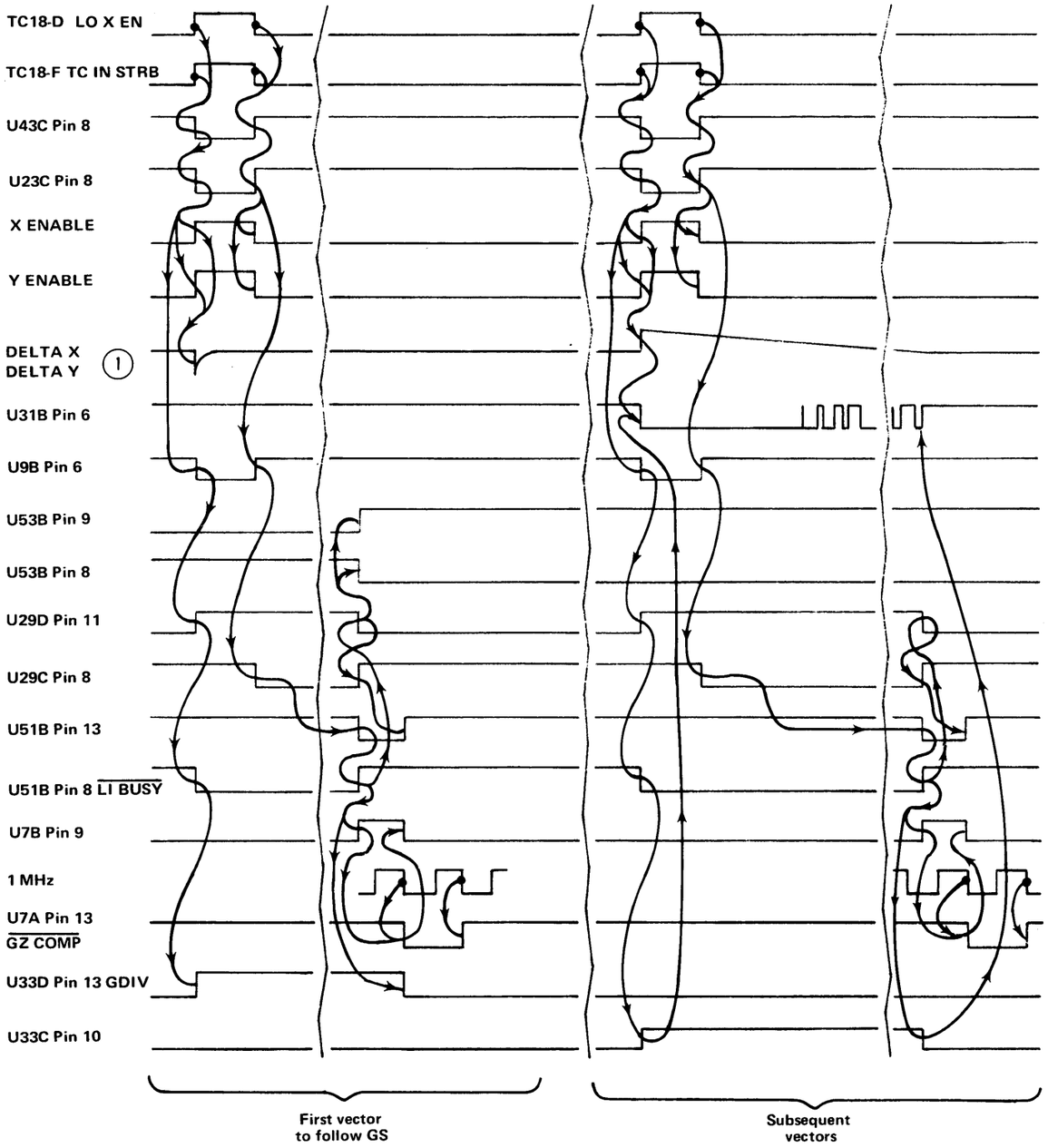
FIG 5-60
BLOCK DIAGRAM
CHARACTER GENERATOR MEMORY (TC-16)



4002A DRAWER

FIG. 5-61 CHARACTER GENERATOR MEMORY – TC16



(1) May be either polarity

Fig. 5-62. Linear Interpolate timing (TC-18).

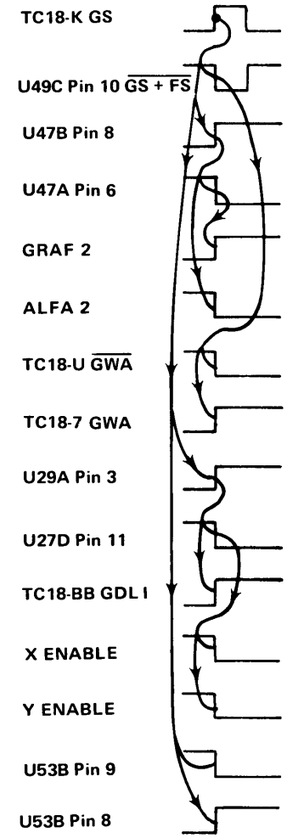


Fig. 5-63. Linear Interpolate initialization (TC-18).

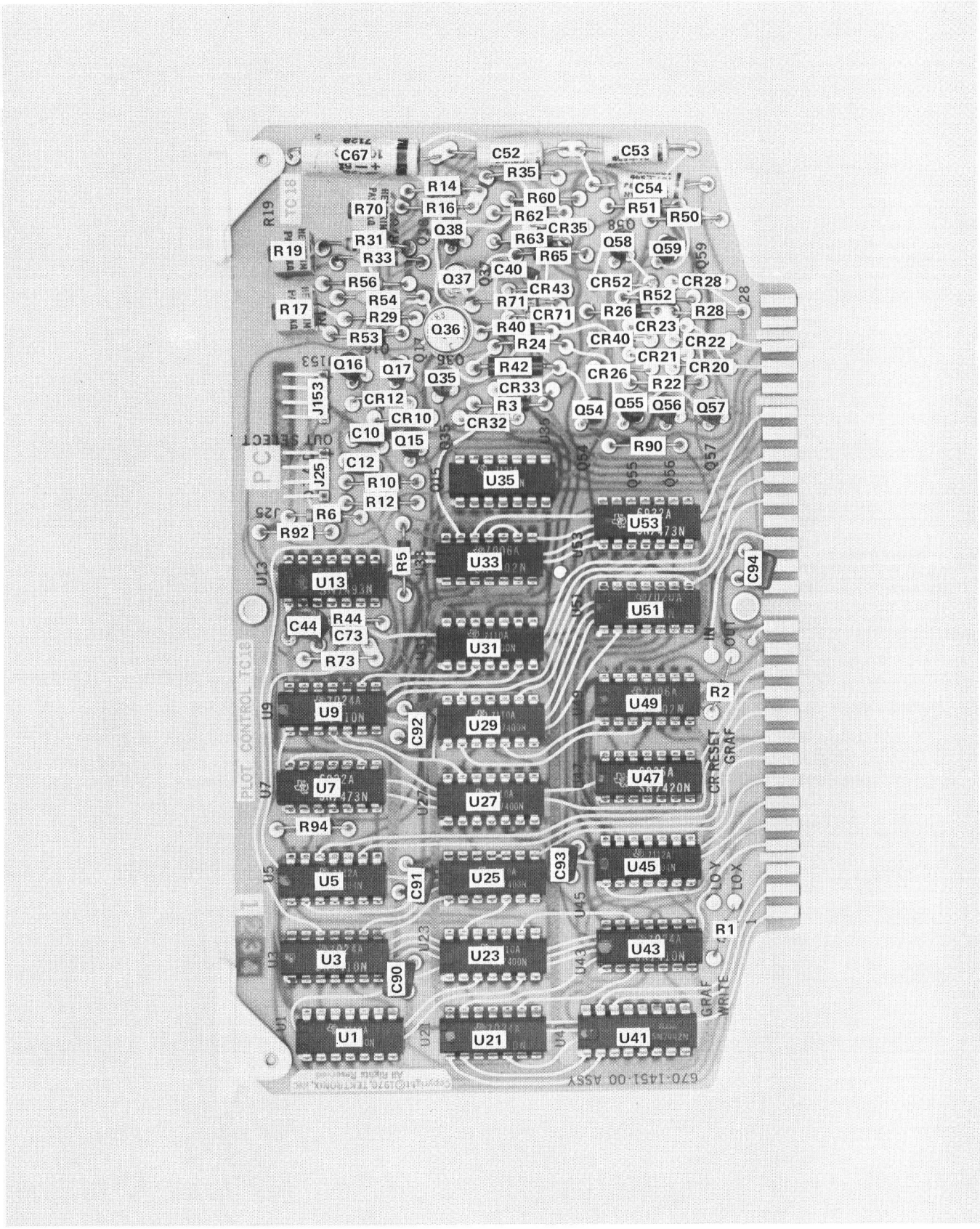


Fig. 5-64. TC18 component illustration.

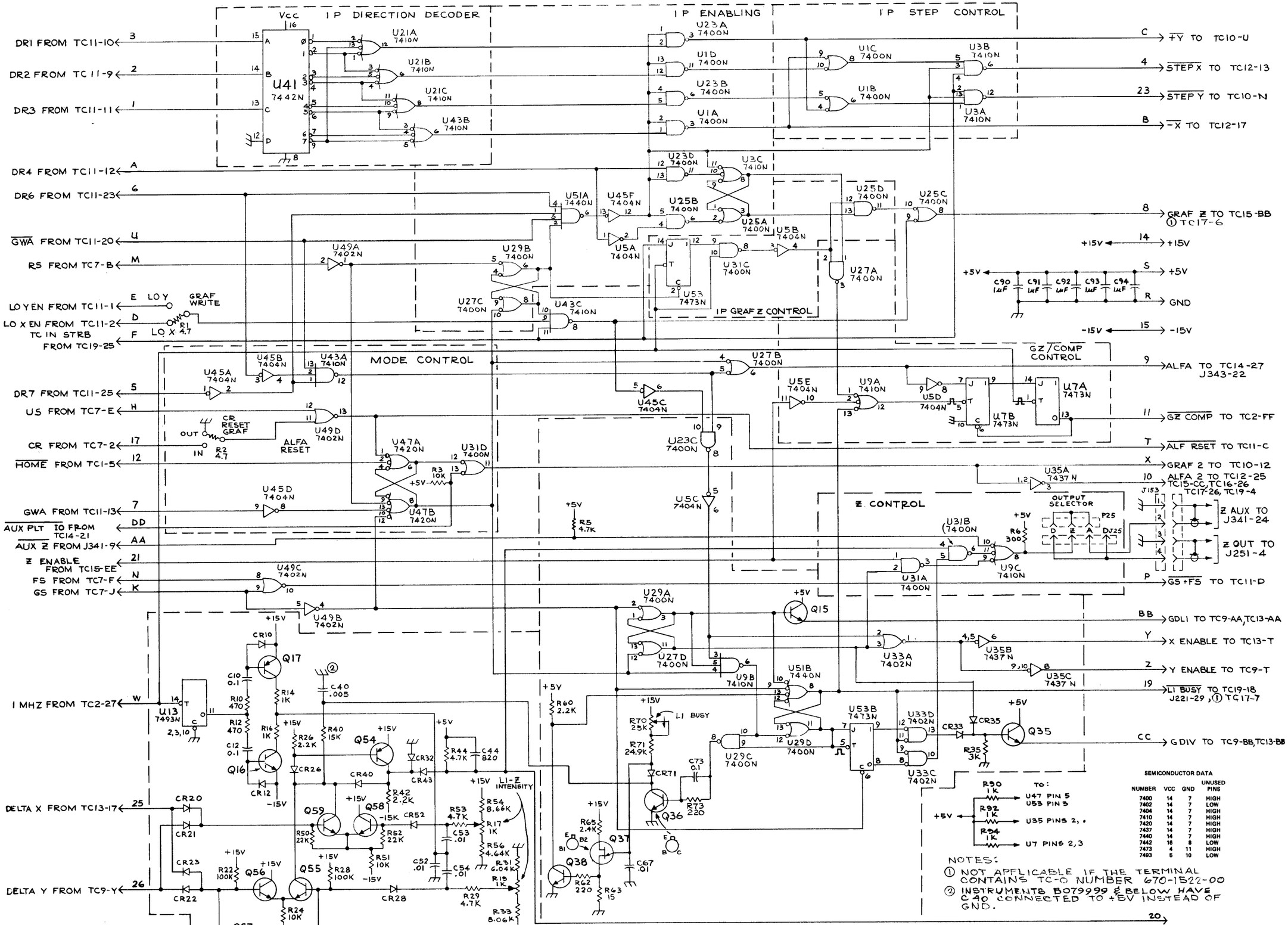


FIG 5-65 PLOT CONTROL TC-18

STROBE CIRCUIT

LE FROM J221-10 H
SP SEND FROM TC5-FF CC
REFRSH FROM TC4-27 BB
DATA STRB FROM TC2-21 Z
XMIT COMP FROM J221-27 D
PRNT BSY FROM J251-10 27
AG FROM J342-6 28
RCV STROB FROM J221-34 AA
GWA FROM TC11-20 L
IMHZ FROM TC2-27 16
LI BUSY FROM TC18-19 18
ON LINE FROM J101-17 22
HOME FROM TC1-5 26
CLEAR FROM TC5-12 23
STROB DLY FROM TC11-17 17
DROP FLG FROM TC11-A 21
AUX COMP FROM J341-14 A
AUX PLT IO FROM TC14-21 K
FUNC COMP FROM TC2-CC 12
COMM ERR FROM J221-23 15
TAB BSY FROM TC6-18 DD
PAGEFULL FROM TC10-BB EE
ERAS INTV FROM J251-7 FF
ITAL CMD FROM TC7-17 2
INITIAL FROM TC1-D E
US FROM TC7-E 3
ALFA 2 FROM TC18-10 4
DBL SZ CMD FROM TC7-18 1
CHAR PROC FROM TC16-28 5
KR SHIFT FROM TC8-16 14

+5V R1 4.7K
U37A 7400N
U37B 7400N
U57A 7410N
U55A 7400N
U55C 7400N
+5V R5 4.7K
+5V R3 4.7K
U15D 7400N
U17A 7473N STROBE SELECT FF
U23C 7402N
U55D 7400N
U15A 7400N
U15C 7400N
1μs
U59C 7420N
U45C 7400N
U9A 7473N STROBE ENABLE FF
U9B 7473N STROBE FF
1μs
U29C 7410N RCV RDY LOCKOUT
U25E 7404N
U15B 7400N
+5V R7 4.7K
U25A 7404N
U5A 7476N STROBE ENABLE
+5V R15 4.7K
U21B 7404N
U23A 7402N
+5V R13 4.7K
U21F 7404N
U45A 7400N
U29B 7410N
ITALIC CONTROL
U41B 7476N
U21C 7404N
U43A 7402N
U45B 7400N
U41A 7476N
U43B 7402N
U43C 7402N
U57B 7410N
U43D 7402N
U21E 7404N
R20 2.2K
Q1
DOUBLE SIZE
DOUBLE INTENSITY

U17B 7473N
TC INPUT STROBE GATE
U35A 7410N
U35C 7410N
AUX INPUT 7410N STROBE GATE U35B
U37C 7400N
U37D 7400N
U21A 7404N
U23D 7402N
U25B 7404N
U3 7472
U46B 7402N
U46A 7402N
U25D 7404N
U57C 7410N
XMIT READY
+5V R11 2.2K
C10 470
U55B 7400N
U29A 7410N
U5B 7476N
U45D 7400N
U19 7430N
U25F 7404N
+5V R12 4.7K
U59A 7420N
RCV READY
U25C 7404N
+5V R18 4.7K

+5V C40 1μF C41 1μF C42 1μF GND

W SP LE TO TC4-10
Y LOC ECHO TO TC11-15
13 XMIT RDY TO J221-30, J342-27
F LE COMP TO TC11-3
25 TC IN STRB TO TC4-U, TC5-23, TC6-1, TC18-F
24 AUX IN STR TO J341-11
20 SYNC STRB TO TC11-28
19 RCV RDY TO J221-12, J342-28
N AUX PLOT TO TC11-16
11 ITALIC TO TC13-EE
6 DBL SZ CHR TO TC9-13, TC10-28, TC12-28, TC13-13
B INTENS 2 TO J251-8, J342-2

SEMICONDUCTOR DATA

NUMBER	VCC	GND	UNUSED PINS
7400	14	7	HIGH
7402	14	7	LOW
7404	14	7	HIGH
7410	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7472	14	7	HIGH
7473	4	11	HIGH
7476	5	13	HIGH

A17

4002A DRAWER

FIG. 5-66 I/O CONTROL TC-19

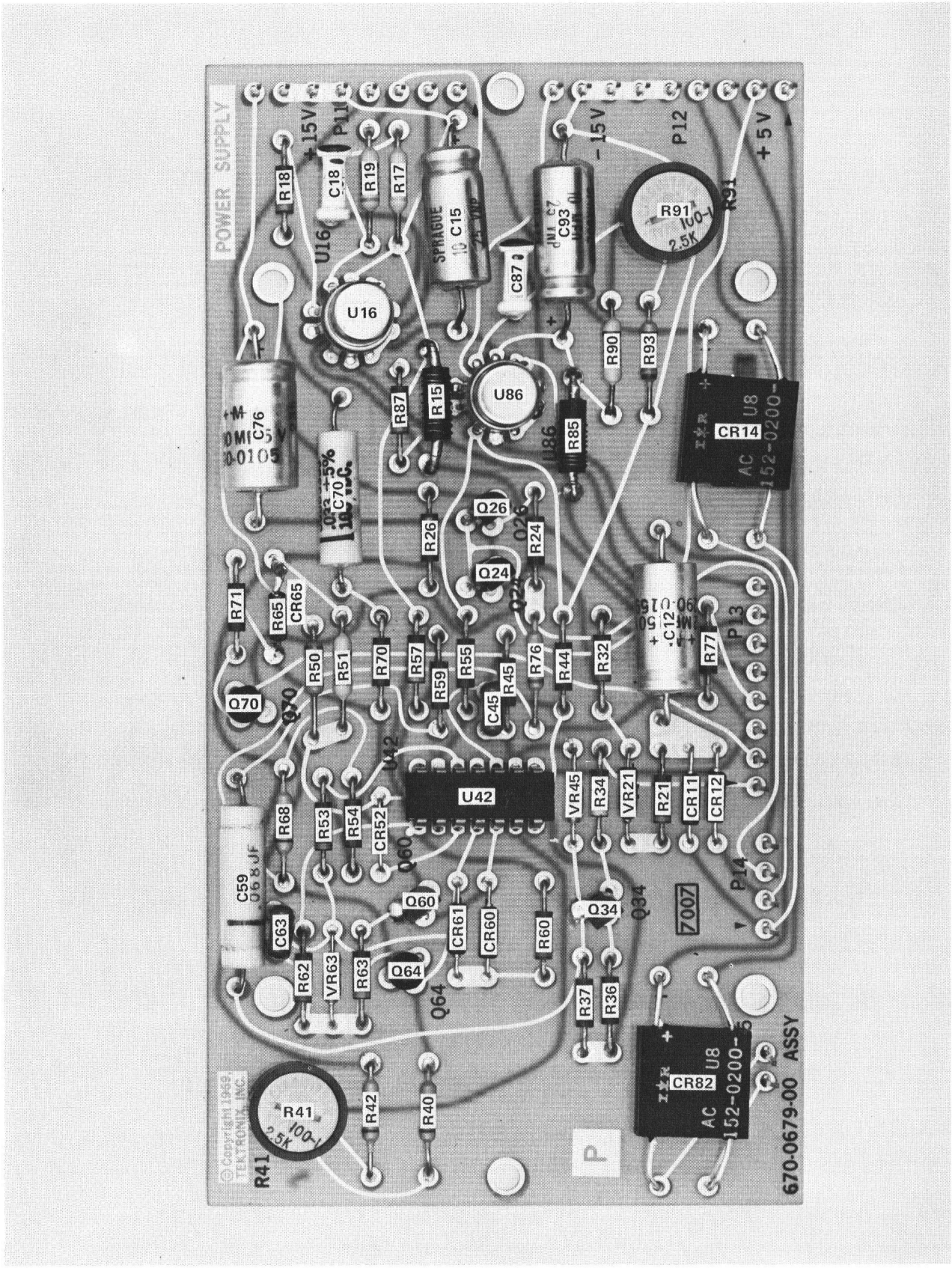
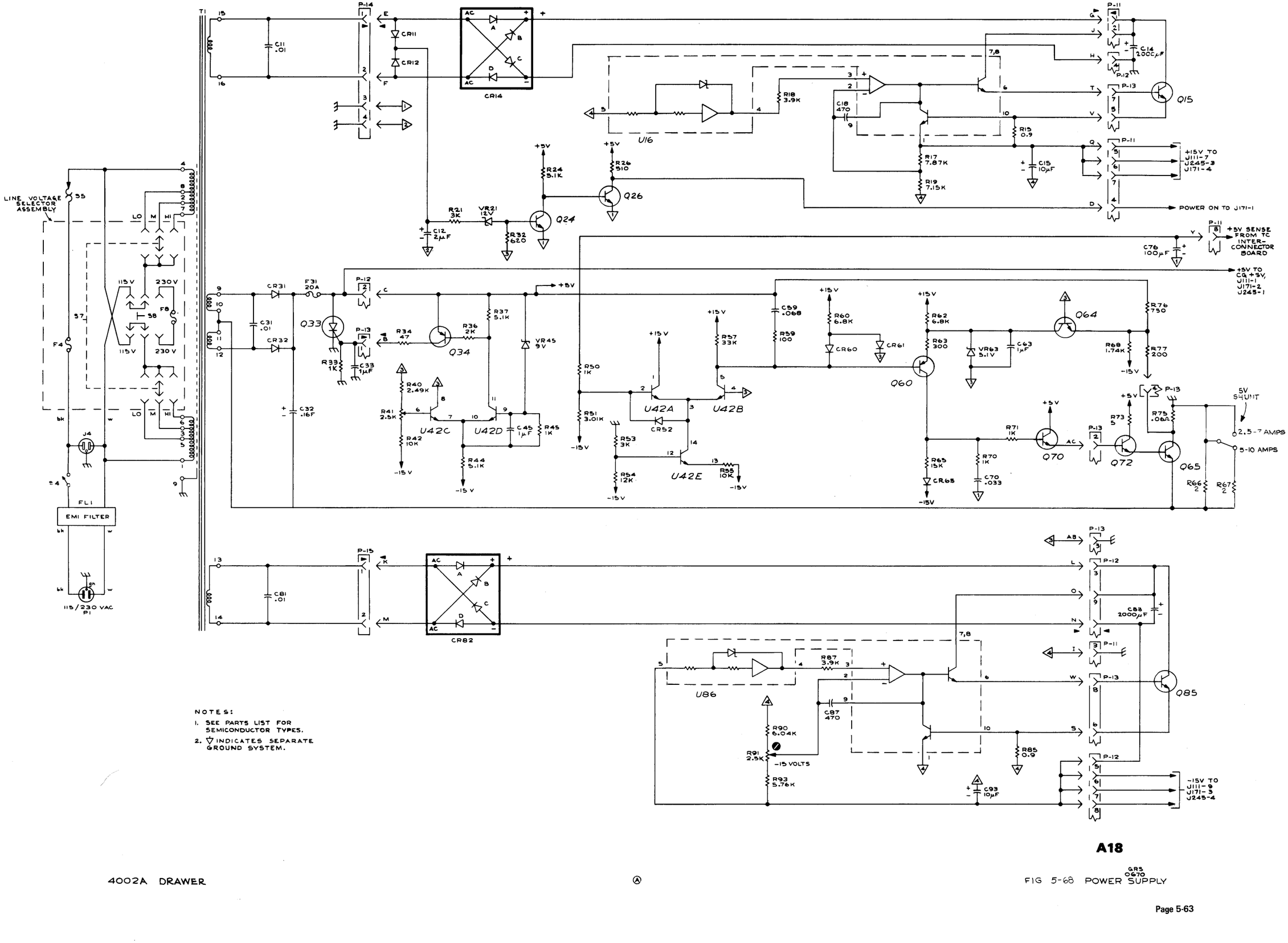


Fig. 5-67. Power Supply board.


LINE VOLTAGE SELECTOR ASSEMBLY
S5
LO
M
HI
115V
230V
S7
S8
F8
F4
J4
FL1
EMI FILTER
115/230 VAC
P1
T1
C11 .01
CR11
CR12
CR14
P-14
U16
R18 3.9K
C18 470
R17 7.87K
R19 7.15K
R15 0.9
C15 10µF
Q15
P-11
P-13
P-12
C14 200µF
+15V TO J111-7 J245-3 J171-4
POWER ON TO J171-1
R24 5.1K
R26 510
Q26
Q24
R21 3K
VR21 12V
R32 620
C12 2µF
C76 100µF
+5V SENSE FROM TC INTER-CONNECTOR BOARD
+5V TO CG +5V, J111-1 J171-2 J245-1
CR31
CR32
F31 20A
C31 .01
C32 .16F
Q33
R33 1K
C33 1µF
R34 47
R36 2K
R37 5.1K
Q34
VR45 9V
R40 2.49K
R41 2.5K
R42 10K
U42C
U42D
C45 1µF
R45 1K
R44 5.1K
R50 1K
R51 3.01K
U42A
U42B
CR52
R53 3K
R54 12K
U42E
R55 10K
R57 33K
C59 .068
R59 100
R60 6.8K
CR60
CR61
Q60
R62 6.8K
R63 300
VR63 5.1V
C63 1µF
Q64
R76 750
R68 1.74K
R77 200
R71 1K
Q70
R65 15K
CR65
R70 1K
C70 .033
Q72
Q65
5V SHUNT
R73 5
R75 .06Ω
2.5-7 AMPS
5-10 AMPS
R66 2
R67 2
C81 .01
CR82
P-15
C83 2000µF
U86
R87 3.9K
C87 470
R90 6.04K
R91 2.5K
-15 VOLTS
R93 5.76K
R85 0.9
C93 10µF
Q85
-15V TO J111-9 J171-3 J245-4
NOTES:
1. SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
2. ▽ INDICATES SEPARATE GROUND SYSTEM.
A18

SECTION 6
MECHANICAL PARTS LIST

FIGURE 1 KEYBOARD

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-1	380-0237-01			1		HOUSING, keyboard
	- - - - - -			-		mounting hardware: (not included w/housing)
-2	211-0607-00			2		SCREW, 6-32 x 2.625 inches, PHS
-3	211-0530-00			2		SCREW, 6-32 x 1.75 inches, PHS
-4	210-0856-00			4		WASHER, flat, 0.15 ID x 0.25 inch OD
	640-0495-00			1		KEYBOARD ASSEMBLY
	- - - - - -			-		keyboard assembly includes:
-5	200-1213-00			1		BEZEL
-6	333-1417-00			1		PANEL, front
-7	260-1273-00			3		SWITCH, push
	- - - - - -			-		mounting hardware for each: (not included w/switch)
	210-0406-00			2		NUT, hex., 4-40 x 0.188 inch
	210-0054-00			2		WASHER, lock, split, 0.118 ID x 0.212 inch OD
	166-0024-00			2		TUBE, spacer, 0.125 ID x 0.188 OD x 0.125 inch long
-8	260-1274-00			1		SWITCH, push--MARGIN SHIFT
	- - - - - -			-		mounting hardware: (not included w/switch)
-9	210-0406-00			2		NUT, hex., 4-40 x 0.188 inch
-10	210-0054-00			2		WASHER, lock, split, 0.118 ID x 0.212 inch OD
-11	166-0024-00			2		TUBE, spacer, 0.125 ID x 0.188 OD x 0.125 inch long
-12	334-1800-00			1		PLATE, identification
	- - - - - -			-		mounting hardware: (not included w/plate)
-13	210-0586-00			2		NUT, keps, 4-40 x 0.25 inch
-14	386-1955-00			1		PANEL, rear
	- - - - - -			-		mounting hardware: (not included w/panel)
-15	210-0457-00			6		NUT, keps, 6-32 x 0.312 inch
-16	366-0491-02			1		KNOB, gray
	- - - - - -			-		knob includes:
	213-0153-00			1		SETSCREW, 5-40 x 0.125 inch, HSS
-17	358-0439-00			1		BUSHING, sleeve, plastic
-18	384-1086-00			1		SHAFT, extension, 1.188 inches long
	214-1315-00			1		ACTUATOR-SWITCH ASSEMBLY
	- - - - - -			-		actuator-switch assembly includes:
-19	214-1312-00			1		INDICATOR, switch position
-20	214-1313-00			1		ACTUATOR, switch indicator
	- - - - - -			-		mounting hardware: (not included w/actuator)
	213-0048-00			1		SETSCREW, 4-40 x 0.125 inch, HSS
-21	260-0760-00			1		SWITCH, sensitive
	- - - - - -			-		mounting hardware: (not included w/switch)
-22	213-0087-00			2		SCREW, thread forming, 2-32 x 0.50 inch, RHS

FIGURE 1 KEYBOARD (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
1-23	352-0225-00			1	HOLDER, switch actuator
-24	214-1314-00			1	ACTUATOR, switch
-25	214-0273-00			1	PIN, roll, 0.062 OD x 0.437 inch long
	- - - - - -			-	mounting hardware: (not included w/actuator-switch
	- - - - - -			-	assembly)
-26	211-0564-00			1	SCREW, 6-32 x 0.375 inch, HSS
-27	211-0559-00			1	SCREW, 6-32 x 0.375 inch, 100° csk, FHS
-28	210-0457-00			2	NUT, keps, 6-32 x 0.312 inch
-29	119-0131-00			1	SPEAKER
	- - - - - -			-	mounting hardware: (not included w/speaker)
-30	210-0457-00			3	NUT, keps, 6-32 x 0.312 inch
-31	210-0202-00			1	LUG, solder, SE #6
-32	354-0366-00			1	RING, retaining, 2.10 ID x 2.875 inches OD
-33	131-0570-00			1	CONNECTOR, plug, male, 25 pin
	- - - - - -			-	mounting hardware: (not included w/connector)
-34	211-0038-00			2	SCREW, 4-40 x 0.312 inch, 100° csk, FHS
-35	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
-36	131-0422-00			1	CONNECTOR, plug, male, 37 pin
	- - - - - -			-	mounting hardware: (not included w/connector)
	211-0038-00			2	SCREW, 4-40 x 0.312 inch, PHS
	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
	361-0433-00			1	SPACER, connector
-37	179-1677-00			1	WIRING HARNESS
-38	136-0156-01			1	SOCKET, circuit board, 44 pin
-39	214-0702-00			1	KEY, connector
-40	119-0269-00	B050500	B089999	1	KEYBOARD A19
	119-0269-01	B090000		1	KEYBOARD A19
	- - - - - -			-	keyboard includes:
-41	260-1347-00			66	SWITCH, pushbutton
-42	260-1348-00			5	SWITCH, pushbutton
-43	260-1349-00			1	SWITCH, pushbutton
-44	119-0312-00			1	SPACE BAR ASSEMBLY
	- - - - - -			-	mounting hardware: (not included w/space bar assy)
-45	211-0105-00			2	SCREW, 4-40 x 0.188 inch, 100° csk, FHS
	- - - - - -			-	mounting hardware: (not included w/keyboard)
-46	210-0457-00			4	NUT, keps, 6-32 x 0.312 inch
-47	166-0032-00			4	TUBE, spacer, 0.18 ID x 0.25 OD x 0.312 inch long
	- - - - - -			-	mounting hardware: (not included w/keyboard assembly)
	212-0045-00			4	SCREW, 8-32 x 0.50 inch, THS, (not shown)

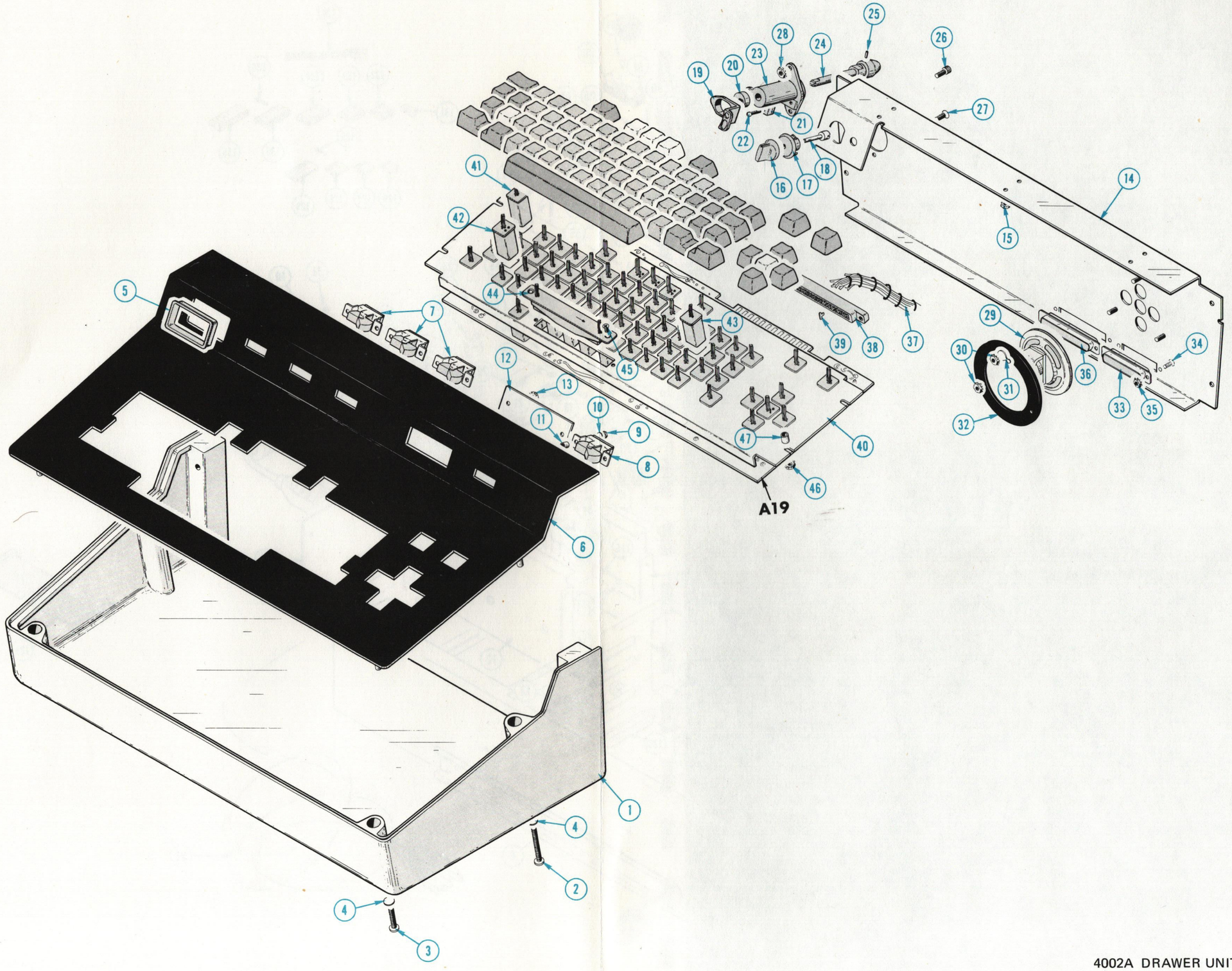
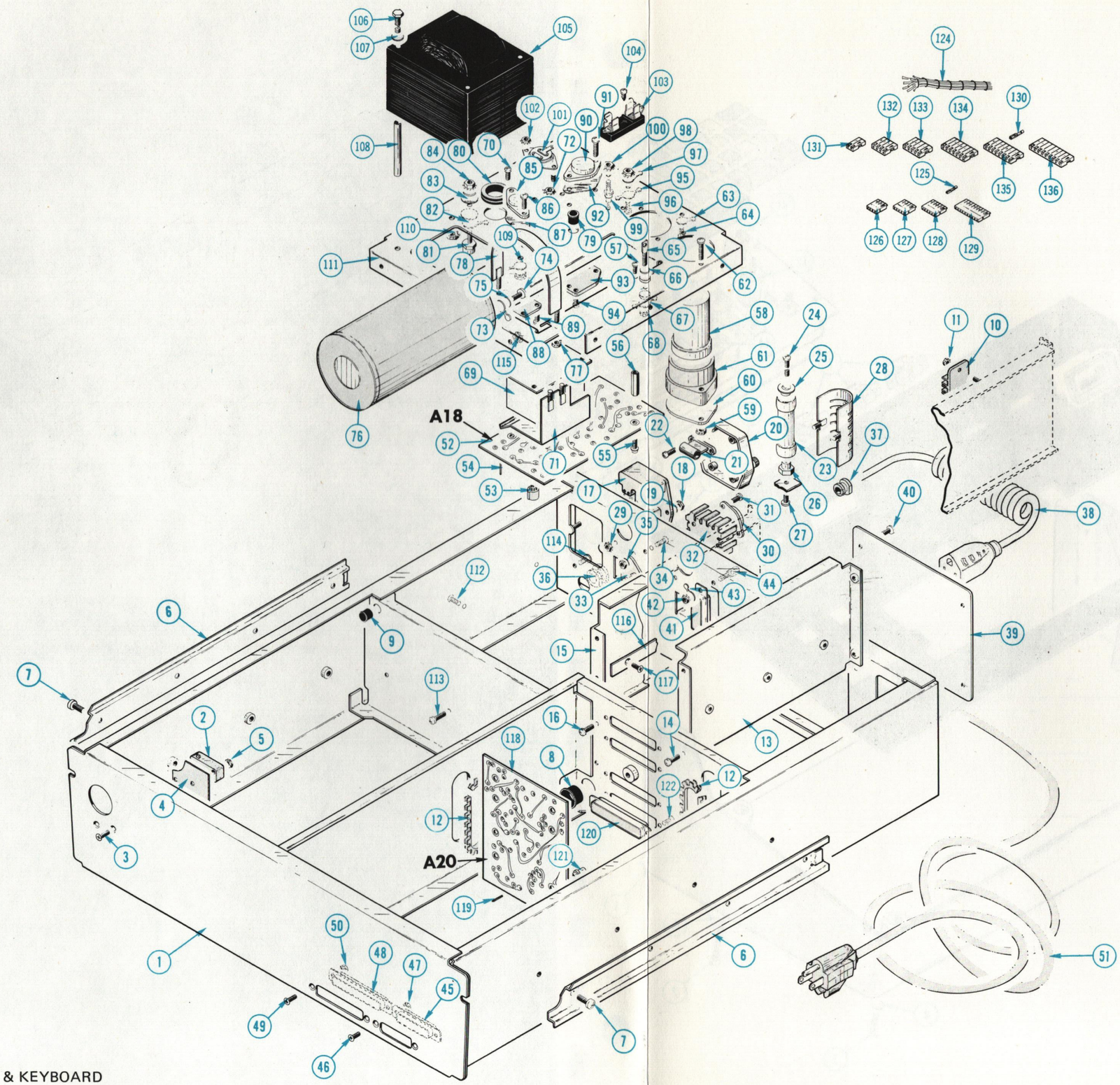
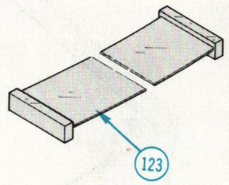

A19

FIG. 2 DRAWER





4002A DRAWER UNIT & KEYBOARD

FIGURE 2 DRAWER

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
2-1	426-0578-00			1		FRAME ASSEMBLY
-2	260-1035-00			1		SWITCH, unwired--POWER
	- - - - - -			-		mounting hardware: (not included w/switch)
-3	211-0174-00			2		SCREW, plastic, 4-40 x 0.625 inch, 100° csk, FHS
-4	342-0013-00			1		INSULATOR, plate, plastic
-5	210-0586-00			2		NUT, keps, 4-40 x 0.25 inch
-6	351-0104-00			1		SLIDE, section (pair)
	- - - - - -			-		mounting hardware for each: (not included w/slide)
-7	212-0518-00			4		SCREW, 10-32 x 0.312 inch, PHS
-8	348-0064-00			1		GROMMET, plastic, 0.50 inch diameter
-9	348-0056-00			2		GROMMET, plastic, 0.375 inch diameter
-10	352-0093-00			1		HOLDER, fuse (spare)
	- - - - - -			-		mounting hardware: (not included w/holder)
-11	210-0586-00			2		NUT, keps, 4-40 x 0.25 inch
-12	255-0334-00			ft		PLASTIC CHANNEL, 36 inches long
-13	426-0511-00			1		FRAME SECTION, auxiliary housing, right
	- - - - - -			-		mounting hardware: (not included w/frame section)
-14	211-0507-00			2		SCREW, 6-32 x 0.312 inch, PHS
-15	426-0510-00			1		FRAME SECTION, auxiliary housing, left
-16	211-0507-00			2		SCREW, 6-32 x 0.312 inch, PHS
-17	204-0279-00			1		BODY, line voltage selector
	- - - - - -			-		mounting hardware: (not included w/body)
-18	210-0407-00			2		NUT, hex., 6-32 x 0.25 inch
-19	210-0006-00			2		WASHER, lock, internal, 0.146 ID x 0.283 inch OD
-20	200-0762-00			1		COVER, line voltage selector
	- - - - - -			-		cover includes:
-21	352-0102-00			2		HOLDER, fuse, plastic
	- - - - - -			-		mounting hardware for each: (not included w/holder)
-22	213-0088-00			1		SCREW, thread forming, 4-40 x 0.25 inch, PHS
-23	- - - - - -			2		RESISTOR
	- - - - - -			-		mounting hardware for each: (not included w/resistor)
-24	212-0037-00			1		SCREW, 8-32 x 1.75 inches, Fil HS
-25	210-0808-00			1		WASHER, centering
-26	210-0462-00			1		NUT, hex., 8-32 x 0.50 inch
-27	212-0004-00			1		SCREW, 8-32 x 0.312 inch, PHS

FIGURE 2 DRAWER (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description
2-28	337-1239-00			2	SHIELD, resistor
	- - - - - -			-	mounting hardware for each: (not included w/shield)
-29	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
-30	- - - - - -			1	TRANSISTOR
	- - - - - -			-	mounting hardware: (not included w/transistor)
-31	211-0511-00			2	SCREW, 6-32 x 0.50 inch, PHS
-32	214-0559-00			1	HEATSINK, transistor
-33	136-0135-00			1	SOCKET, transistor, 2 pin
	- - - - - -			-	mounting hardware: (not included w/socket)
-34	211-0112-00			2	SCREW, 2-56 x 0.375 inch, 100° csk, FHS
	210-0001-00			2	WASHER, lock, internal, 0.092 ID x 0.18 inch OD
-35	210-0405-00			2	NUT, hex., 2-56 x 0.188 inch
-36	358-0025-00			1	BUSHING, strain relief, 0.687 OD x 0.437 inch long
-37	358-0161-00			1	BUSHING, strain relief, plastic
-38	161-0062-00	B050500	B059999	1	CABLE ASSEMBLY, coiled, 3 feet long
	161-0076-00	B060000		1	CABLE ASSEMBLY, coiled, 3 feet long
-39	386-1697-00			1	PANEL, rear, auxiliary unit
	- - - - - -			-	mounting hardware: (not included w/panel)
-40	211-0542-00			4	SCREW, 6-32 x 0.312 inch, THS
-41	131-0569-00			1	CONNECTOR, receptacle, 25 pin
	- - - - - -			-	mounting hardware: (not included w/connector)
-42	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
-43	210-0201-00			1	LUG, solder, SE #4
-44	129-0260-00			2	POST, stud, w/counter sink, 4-40 thread
-45	131-0569-00			1	CONNECTOR, receptacle, 25 pin
	- - - - - -			-	mounting hardware: (not included w/connector)
-46	211-0101-00			2	SCREW, 4-40 x 0.25 inch, 100° csk, FHS
-47	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
-48	131-0408-00			1	CONNECTOR, receptacle, 37 pin
	- - - - - -			-	mounting hardware: (not included w/connector)
-49	211-0101-00			2	SCREW, 4-40 x 0.25 inch, 100° csk, FHS
-50	210-0586-00			2	NUT, keps, 4-40 x 0.25 inch
	210-0201-00			1	LUG, solder, SE #4
-51	161-0057-00			1	CABLE ASSEMBLY, power, 8 feet long
-52	670-0679-00	B050500	B099999	1	CIRCUIT BOARD ASSEMBLY--POWER SUPPLY A18
	670-0679-01	B100000		1	CIRCUIT BOARD ASSEMBLY--POWER SUPPLY A18
	- - - - - -			-	circuit board assembly includes:
	388-1245-00	B050500	B099999	1	CIRCUIT BOARD
	388-1245-01	B100000		1	CIRCUIT BOARD
-53	136-0241-00			2	SOCKET, integrated circuit, 10 contact
-54	131-0589-00			33	TERMINAL, pin, 0.50 inch long
	- - - - - -			-	mounting hardware: (not included w/circuit board assembly)
-55	211-0116-00			4	SCREW, sems, 4-40 x 0.312 inch, PHB
-56	129-0097-00			4	POST, metallic, 0.555 inch long
	- - - - - -			-	mounting hardware for each: (not included w/post)
-57	211-0008-00			1	SCREW, 4-40 x 0.25 inch, PHS

FIGURE 2 DRAWER (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5	Description
2-58	- - - - - -			2		CAPACITOR
	- - - - - -			-		mounting hardware for each: (not included w/capacitor)
-59	210-0457-00			2		NUT, keps, 6-32 x 0.312 inch, PHS
-60	386-0254-00			1		PLATE, fiber, large
-61	432-0048-00			1		BASE, large, plastic
-62	211-0516-00			2		SCREW, 6-32 x 0.875 inch, PHS
-63	210-0201-00			2		LUG, solder, SE #4
	- - - - - -			-		mounting hardware for each: (not included w/lug)
-64	213-0044-00			1		SCREW, 6-32 x 0.875 inch, PHS
-65	214-0012-00			1		BOLT, spade, 6-32 x 0.375 inch
	- - - - - -			-		mounting hardware: (not included w/bolt)
-66	210-0802-00			2		WASHER, flat, 0.15 ID x 0.312 inch OD
	210-1111-00			2		WASHER, plastic, shouldered, 0.247 ID x 0.375 inch OD
-67	210-0204-00			1		LUG, solder, DE #6
-68	210-0457-00			1		NUT, keps, 6-32 x 0.312 inch
-69	- - - - - -			1		LINE FILTER
	- - - - - -			-		mounting hardware: (not included w/filter)
-70	211-0008-00			2		SCREW, 4-40 x 0.25 inch, PHS
-71	337-1268-00			1		SHIELD, line filter
	- - - - - -			-		mounting hardware: (not included w/shield)
-72	210-0586-00			2		NUT, keps, 4-40 x 0.25 inch
-73	210-0273-00			3		TERMINAL, lug
	- - - - - -			-		mounting hardware for each: (not included w/terminal)
-74	212-0518-00			1		SCREW, 10-32 x 0.312 inch
-75	210-0010-00			1		WASHER, lock, internal, 0.20 ID x 0.376 inch OD
-76	- - - - - -			1		CAPACITOR
	- - - - - -			-		mounting hardware: (not included w/capacitor)
-77	210-0457-00			4		NUT, keps, 6-32 x 0.312 inch
-78	346-0071-00			2		STRAP, retaining
-79	348-0067-00			1		GROMMET, plastic, 0.312 inch diameter
-80	348-0006-00			1		GROMMET, rubber, 0.75 inch diameter
-81	- - - - - -			2		DIODE
	- - - - - -			-		mounting hardware for each: (not included w/diode)
-82	210-0224-00			1		LUG, solder, SE #10
	210-0910-00			1		WASHER, plastic, 0.19 ID x 0.281 inch OD
-83	210-0909-00			2		WASHER, plastic, 0.196 ID x 0.625 inch OD
	210-0805-00			1		WASHER, flat, 0.204 ID x 0.438 inch OD
-84	220-0410-00			1		NUT, keps, 10-32 x 0.375 inch
-85	- - - - - -			3		TRANSISTOR
	- - - - - -			-		mounting hardware for each: (not included w/transistor)
-86	213-0104-00			2		SCREW, thread forming, 6-32 x 0.375 inch, THS
-87	386-0143-00			1		PLATE, mica, insulator

FIGURE 2 DRAWER (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
2-88	136-0270-00			3		SOCKET, transistor, 2 pin
	- - - - - -			-		mounting hardware for each: (not included w/socket)
-89	213-0088-00			2		SCREW, thread forming, 4-40 x 0.25 inch, THS
-90	- - - - - -			1		TRANSISTOR
	- - - - - -			-		mounting hardware: (not included w/transistor)
-91	211-0510-00			2		SCREW, 6-32 x 0.375 inch, PHS
-92	386-0978-00			1		PLATE, mica, insulator
-93	136-0135-00			1		SOCKET, transistor, 2 pin
	- - - - - -			-		mounting hardware: (not included w/socket)
-94	213-0113-00			2		SCREW, thread forming, 2-32 x 0.312 inch, RHS
-95	210-0204-00			1		LUG, solder, DE #6
	- - - - - -			-		mounting hardware: (not included w/lug)
-96	211-0507-00			1		SCREW, 6-32 x 0.312 inch, PHS
-97	210-0202-00			1		LUG, solder, SE #6
-98	210-0457-00			1		NUT, keps, 6-32 x 0.312 inch
-99	129-0006-00			3		POST, connecting, insulated
	- - - - - -			-		mounting hardware for each: (not included w/post)
-100	210-0457-00			1		NUT, keps, 6-32 x 0.312 inch
-101	- - - - - -			1		SWITCH, thermostatic
	- - - - - -			-		mounting hardware: (not included w/switch)
-102	210-0586-00			2		NUT, keps, 4-40 x 0.25 inch
-103	352-0031-00			1		HOLDER, fuse, single
	- - - - - -			-		mounting hardware: (not included w/holder)
-104	213-0054-00			1		SCREW, thread cutting, 6-32 x 0.312 inch, PHS
-105	- - - - - -			1		TRANSFORMER
	- - - - - -			-		mounting hardware: (not included w/transformer)
-106	212-0522-00			4		SCREW, 10-32 x 2.50 inches, HHS
-107	210-0812-00			4		WASHER, fiber, 0.188 ID x 0.375 inch OD
-108	166-0434-00			4		TUBE, bolt insulating, plastic
-109	210-0206-00			1		LUG, solder, SE #10
-110	220-0410-00			4		NUT, keps, 10-32 x 0.375 inch
-111	441-0881-00			1		CHASSIS, power supply
	- - - - - -			-		mounting hardware: (not included w/chassis)
-112	211-0541-00			3		SCREW, 6-32 x 0.25 inch, 100° csk, FHS
-113	211-0507-00			4		SCREW, 6-32 x 0.312 inch, PHS
-114	211-0565-00			2		SCREW, 6-32 x 0.25 inch, THS
-115	210-0457-00			1		NUT, keps, 6-32 x 0.312 inch
-116	351-0256-00			2		SLIDE, guide
	- - - - - -			-		mounting hardware for each: (not included w/slide)
	211-0538-00			3		SCREW, 6-32 x 0.25 inch, 100° csk, FHS (right side)
-117	211-0541-00			3		SCREW, 6-32 x 0.312 inch, 100° csk, FHS (left side)

FIGURE 2 DRAWER (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5 Description
2-118	670-0857-01			1	CIRCUIT BOARD ASSEMBLY--AUXILLIARY
	- - - - - -			-	circuit board assembly includes:
	388-1505-01			1	CIRCUIT BOARD
-119	131-0608-00			161	TERMINAL, pin, 0.365 inch long
-120	131-0870-00	B050500	B069999	4	CONNECTOR, receptacle, 37 pin
	131-0972-00	B070000		4	CONNECTOR, receptacle, 37 pin
-121	129-0105-00			8	POST
	- - - - - -			-	mounting hardware: (not included w/circuit board assembly)
-122	211-0101-00			8	SCREW, 4-40 x 0.25 inch, 100°csk, FHS
-123	175-1290-00			2	CABLE ASSEMBLY, 9 inches long
	175-1291-00			2	CABLE ASSEMBLY, 15 inches long
-124	179-1674-00			1	WIRING HARNESS, connector
	- - - - - -			-	wiring harness includes:
-125	131-0707-00			23	CONNECTOR, terminal
	131-0708-00			14	CONNECTOR, terminal
-126	352-0162-00			1	HOLDER, terminal connector, 4 wire (black)
-127	352-0163-00			1	HOLDER, terminal connector, 5 wire (black)
-128	352-0164-00			3	HOLDER, terminal connector, 6 wire (black)
-129	352-0168-00			1	HOLDER, terminal connector, 10 wire (black)
	179-1675-00			1	WIRING HARNESS, power
	- - - - - -			-	wiring harness includes:
-130	131-0621-00			47	CONNECTOR, terminal
-131	352-0198-00			1	HOLDER, terminal connector, 2 wire (black)
-132	352-0200-00			2	HOLDER, terminal connector, 4 wire (black)
-133	352-0201-00			1	HOLDER, terminal connector, 5 wire (black)
-134	352-0203-00			1	HOLDER, terminal connector, 7 wire (black)
-135	352-0204-00			2	HOLDER, terminal connector, 8 wire (black)
-136	352-0205-00			1	HOLDER, terminal connector, 9 wire (black)
	179-1484-00			1	WIRING HARNESS, line voltage
	179-1678-00			1	WIRING HARNESS, keyboard interface
	- - - - - -			-	wiring harness includes:
	131-0707-00			34	CONNECTOR, terminal
	131-0621-00			5	CONNECTOR, terminal
	352-0201-00			1	HOLDER, terminal connector, 5 wire (black)
	352-0168-00			1	HOLDER, terminal connector, 10 wire (black)
	352-0168-03			1	HOLDER, terminal connector, 10 wire (orange)
	352-0168-04			1	HOLDER, terminal connector, 10 wire (yellow)
	352-0168-06			1	HOLDER, terminal connector, 10 wire (blue)
	131-0992-00			1	CONNECTOR, terminal, quick disconnect
	131-1191-00			1	TERMINAL, quick disconnect

FIGURE 3 TERMINAL CONTROL

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description
3-1	386-2016-00			2	SUPPORT, connector bracket, end
	- - - - - -			-	mounting hardware for each: (not included w/support)
-2	211-0504-00			4	SCREW, 6-32 x 0.25 inch, PHS
-3	386-2017-00			4	SUPPORT, side
	- - - - - -			-	mounting hardware for each: (not included w/support)
-4	211-0541-00			1	SCREW, 6-32 x 0.25 inch, 100°csk, FHS
-5	211-0510-00			1	SCREW, 6-32 x 0.375 inch, PHS
-6	255-0334-00			ft	PLASTIC CHANNEL, 3 inches long
-7	351-0303-00			38	GUIDE, circuit card
-8	407-0952-00			1	BRACKET, left
-9	407-0953-00			1	BRACKET, right
-10	670-1522-00	B050500	B089999	1	CIRCUIT BOARD ASSEMBLY--INTERFACE
	670-1522-01	B090000		1	CIRCUIT BOARD ASSEMBLY--INTERFACE
	- - - - - -			-	circuit board assembly includes:
	388-2077-00	B050500	B089999	1	CIRCUIT BOARD
	388-2077-01	B090000		1	CIRCUIT BOARD
-11	131-0608-00			269	TERMINAL, pin, 0.365 inch long
-12	131-0762-01			19	CONNECTOR, receptacle, 56 contact
-13	214-0702-00			57	KEY, connector polarizing
	- - - - - -			-	mounting hardware: (not included w/circuit board assembly)
-14	211-0097-00			8	SCREW, 4-40 x 0.312 inch, PHS
-15	670-1435-00	B050500	B069999	1	CIRCUIT CARD ASSEMBLY--KEYBOARD LOGIC A1
	670-1435-01	B070000		1	CIRCUIT CARD ASSEMBLY--KEYBOARD LOGIC A1
	- - - - - -			-	circuit card assembly includes:
	388-1984-00			1	CIRCUIT CARD
-16	131-0589-00			6	TERMINAL, pin, 0.50 inch long
	131-0993-00			1	LINK, terminal connecting
	- - - - - -			-	link includes:
-17	352-0169-00			1	HOLDER, terminal connector, 2 wire (black)
-18	131-0707-00			2	CONNECTOR, terminal
-19	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
-20	214-1337-00			1	PIN, spring
-21	670-1436-00	B050500	B069999	1	CIRCUIT CARD ASSEMBLY--OUTPUT DATA SELECTOR A2
	670-1436-01	B070000	B099999	1	CIRCUIT CARD ASSEMBLY--OUTPUT DATA SELECTOR A2
	670-1436-02	B100000		1	CIRCUIT CARD ASSEMBLY--OUTPUT DATA SELECTOR A2
	- - - - - -			-	circuit card assembly includes:
	388-1985-00	B050500	B069999	1	CIRCUIT CARD
	388-1985-01	B070000		1	CIRCUIT CARD
-22	337-1454-00			4	SHIELD, electrical
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-23	670-1437-00	B050500	B089999	1	CIRCUIT CARD ASSEMBLY--SCRATCH PAD CONTROL A3
	670-1437-01	B090000		1	CIRCUIT CARD ASSEMBLY--SCRATCH PAD CONTROL A3
	- - - - - -			-	circuit card assembly includes:
	388-1986-00	B050500	B089999	1	CIRCUIT CARD
	388-1986-01	B090000		1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring

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FIGURE 3 TERMINAL CONTROL (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty 1 2 3 4 5	Description
3-24	670-1438-00	B050500	B079999	1	CIRCUIT CARD ASSEMBLY--SCRATCH PAD LOGIC A4
	670-1438-01	B080000		1	CIRCUIT CARD ASSEMBLY--SCRATCH PAD LOGIC A4
	- - - - - -			-	circuit card assembly includes:
	388-1987-00	B050500	B079999	1	CIRCUIT CARD
	388-1987-01	B080000		1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-25	670-1440-00			1	CIRCUIT CARD ASSEMBLY--CONTROL FUNCTION DECODER A6
	- - - - - -			-	circuit card assembly includes:
	388-1989-00			1	CIRCUIT CARD
-26	131-0566-00			3	LINK, terminal connecting
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-27	670-1576-00			1	CIRCUIT CARD ASSEMBLY--CHARACTER ROTATOR BYPASS A7
	- - - - - -			-	circuit card assembly includes:
	388-2135-00			1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware: (not included w/ejector)
	214-1337-00			1	PIN, spring
-28	670-1442-00			1	CIRCUIT CARD ASSEMBLY--Y D/A A8
	- - - - - -			-	circuit card assembly includes:
	388-1991-00			1	CIRCUIT CARD
	131-0589-00			10	TERMINAL, pin, 0.50 inch long
-29	260-0960-00			1	SWITCH, slide
	131-1154-00			1	LINK, terminal connecting
	- - - - - -			-	link includes:
-30	131-0707-00			3	CONNECTOR, terminal
-31	352-0161-00			1	HOLDER, terminal connector, 3 wire (black)
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-32	670-1443-00	B050500	B079999	1	CIRCUIT CARD ASSEMBLY--Y DATA REGISTER A9
	670-1443-01	B080000		1	CIRCUIT CARD ASSEMBLY--Y DATA REGISTER A9
	- - - - - -			-	circuit card assembly includes:
	388-1992-00	B050500	B079999	1	CIRCUIT CARD
	388-1992-01	B080000		1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-33	670-1444-00	B050500	B079999	1	CIRCUIT CARD ASSEMBLY--IN/OUT DATA ROUTING A10
	670-1444-01	B080000	B089999	1	CIRCUIT CARD ASSEMBLY--IN/OUT DATA ROUTING A10
	670-1444-02	B090000		1	CIRCUIT CARD ASSEMBLY--IN/OUT DATA ROUTING A10
	- - - - - -			-	circuit card assembly includes:
	388-1993-00			1	CIRCUIT CARD
	337-1454-00			4	SHIELD, electrical
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-34	670-1445-00	B050500	B079999	1	CIRCUIT CARD ASSEMBLY--X DATA REGISTER A11
	670-1445-01	B080000		1	CIRCUIT CARD ASSEMBLY--X DATA REGISTER A11
	- - - - - -			-	circuit card assembly includes:
	388-1994-00	B050500	B079999	1	CIRCUIT CARD
	388-1994-01	B080000		1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring

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FIGURE 3 TERMINAL CONTROL (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
3-35	670-1446-00			1	CIRCUIT CARD ASSEMBLY--X DA A12
	- - - - - -			-	circuit card assembly includes:
	388-1995-00			1	CIRCUIT CARD
	131-0589-00			10	TERMINAL, pin, 0.50 inch long
	131-1154-00			1	LINK, terminal connecting
	- - - - - -			-	link includes:
	131-0707-00			3	CONNECTOR, terminal
	352-0161-00			1	HOLDER, terminal connector, 3 wire (black)
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-36	670-1447-00			1	CIRCUIT CARD ASSEMBLY--INTERNAL DATA ROUTING A13
	- - - - - -			-	circuit card assembly includes:
	388-1996-00			1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-37	670-1520-00			1	CIRCUIT CARD ASSEMBLY--CHAR GEN CONTROL A14
	- - - - - -			-	circuit card assembly includes:
	388-2075-00			1	CIRCUIT CARD
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-38	670-1521-00			1	CIRCUIT CARD ASSEMBLY--CHARACTER GEN MEMORY A15
	- - - - - -			-	circuit card assembly includes:
	388-2076-00			1	CIRCUIT CARD
-39	136-0252-04			84	SOCKET, pin connector
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-40	670-1451-00	B050500	B079999	1	CIRCUIT CARD ASSEMBLY--PLOT CONTROL A16
	670-1451-01	B080000		1	CIRCUIT CARD ASSEMBLY--PLOT CONTROL A16
	- - - - - -			-	circuit card assembly includes:
	388-2000-00			1	CIRCUIT CARD
	131-0589-00			8	TERMINAL, pin, 0.50 inch long
	131-1154-00			1	LINK, terminal connecting
	- - - - - -			-	link includes:
	131-0707-00			3	CONNECTOR, terminal
	352-0161-00			1	HOLDER, terminal connector, 3 wire (black)
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring
-41	670-1452-00			1	CIRCUIT CARD ASSEMBLY--I/O CONTROL A17
	- - - - - -			-	circuit card assembly includes:
	388-2001-00			1	CIRCUIT CARD
	337-1454-00			4	SHEILD, electrical
	105-0160-00			2	EJECTOR, circuit card
	- - - - - -			-	mounting hardware for each: (not included w/ejector)
	214-1337-00			1	PIN, spring

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5	Description
						STANDARD ACCESSORIES
	070-1167-01			1		MANUAL, instruction
	070-1159-00			1		SPECIFICATIONS MANUAL
						OPTIONAL ACCESSORIES
	067-0615-00			1		CALIBRATION FIXTURE, extender circuit card
	012-0334-00			1		CABLE, interconnecting, 12 inches long
	012-0335-00			1		CABLE, interconnecting, 36 inches long
	670-1649-00			1		CIRCUIT CARD ASSEMBLY–SCRATCH PAD BYPASS
	670-1650-00			1		CIRCUIT CARD ASSEMBLY–SCRATCH PAD BYPASS
	670-1439-00			1		CIRCUIT CARD ASSEMBLY–HORIZONTAL TAB
	670-1441-00			1		CIRCUIT CARD ASSEMBLY–CHARACTER ROTATOR

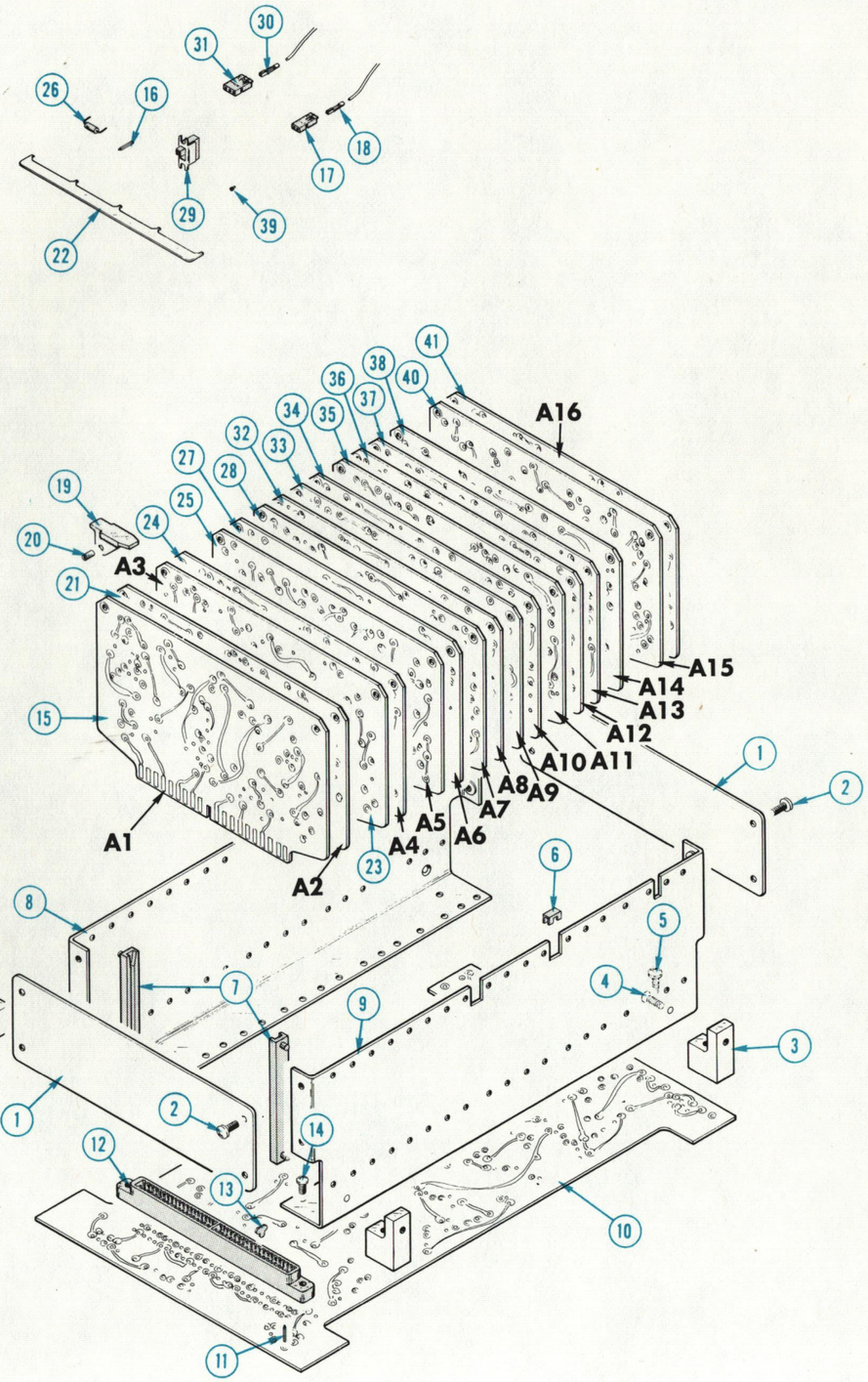

FIG. 3 TERMINAL CONTROL & ACCESSORIES

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

SCHEMATIC CORRECTIONS

Page 5-45, Fig. 5-39	At left-middle, at U31A, change 7440N to 7420N
Page 5-46, Fig. 5-41	Top-right, change U2 to U3
Page 5-47, Fig. 5-43	Top-right, at U53B, change pin 13 to 9 and change pin 9 to 13; change the device number from U53B to U55B.
	At right edge, 2 inches above center, at U47C, delete the 9 at the input.
Page 5-53, Fig. 5-52	At bottom edge, 2 inches to left of center, change U17A to U15A; change U17B to U15B.
	At bottom-right corner, change U15A to U17A; change U15B to U17B.
	In bottom-left quadrant, at U29D, change pin 12 to 11, and pin 11 to 12.
Page 5-56, Fig. 5-57	At center, change U15A to U9F; change 7402N to 7404N; change pins 2, 3 to 13; change pin 1 to 12.
	At bottom-left corner, change U51A and U15A from 7408 to 7402.
Page 5-62, Fig. 5-66	At top-left corner, on U57A, change pin 1 to 2 and pin 2 to 1. Two inches above and to the right of center, change U35B to U57B; delete 4, 5 at its input.
	At bottom-center, change U57B to U35B; at its input, change 3,4 to 5 and change 5 to 4.