Service Manual

SYKES Comm-Stor*

*This manual is for use with Comm-Stor family products.

Comm-Stor ™

SERVICE MANUAL

SYKES ®
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The information in this publication is believed to be accurate in all respects. Additionally, the logic drawings included in this manual may not necessarily be 100% accurate with respect to the boardsets shipped in a particular Comm-Stor unit. Therefore, Sykes Datatronics, Incorporated cannot assume responsibility for any consequences resulting from the use thereof. The information contained herein is subject to change without notice. Revisions of this publication or new editions of it may be issued to incorporate such change.

Comm-Stor SERVICE MANUAL

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CHAPTER 1

INTRODUCTION TO THE Comm-Stor SYSTEM

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1. GENERAL DESCRIPTION

Comm-Stor is a communications storage unit which uses an IBM compatible flexible diskette for storing operator information. Industry standard connectors provide interfacing with a terminal, modem, and line printer. A block diagram of the Sykes Series 8000 Comm-Stor System (CSS) is shown in Figure #1-3. The components of the system are as follows:

A. Flexible Disk Drive (FDD)

The FDD is an IBM compatible self-contained unit which spins the diskette and locates the read/write head in the proper position for accessing tracks. Also included is a printed circuit board which contains read/write electronics, stepper control and status logic.

B. Flexible Disk Controller (FDC)

The FDC is the complete electronics package which interfaces to the FDD and controls all disk operations. For example, it detects the data coming off the diskette, locates desired tracks/sectors automatically, buffers data and responds to commands from the microprocessor.

C. Power Supply

A multiple voltage power supply generates the voltages required for operation of the system from standard AC line voltages.

D. Front Panel

The front panel contains an access door through which the diskette is inserted into the FDD, an illuminating main POWER (on Comm-Stor) or RESTART (on Comm-Stor II, III, IV) switch/indicator, and four LED's indicating the state of the READY, BUSY, CARRIER, and STATUS functions. On Comm-Stor II, III and IV, the POWER switch is located in the center of the rear panel.

E. EIA Interface and I/O Panel

Comm-Stor interfaces with all asynchronous RS-232 terminals, printers and modems by using a printed circuit board which is inserted into the FDC base card, a cable harness to connect the board to

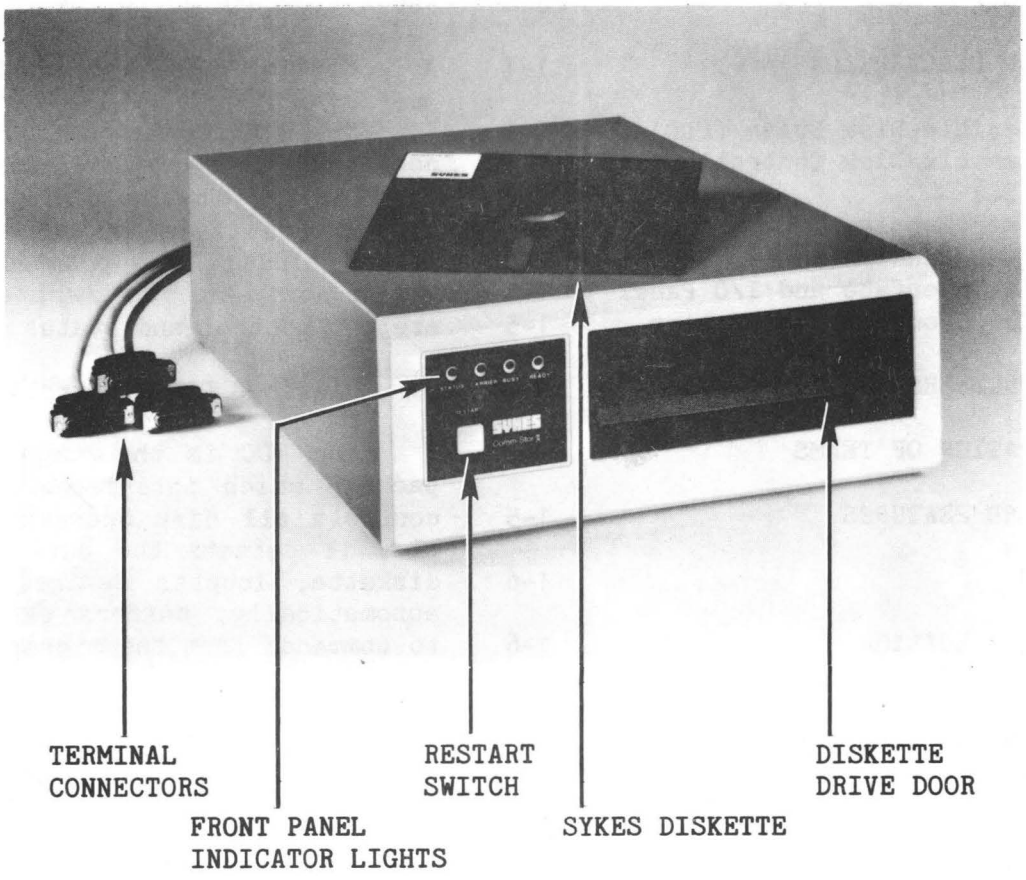
TERMINAL
CONNECTORS
FRONT PANEL
INDICATOR LIGHTS
RESTART
SWITCH
SYKES DISKETTE
DISKETTE
DRIVE DOOR

FIGURE #1-1

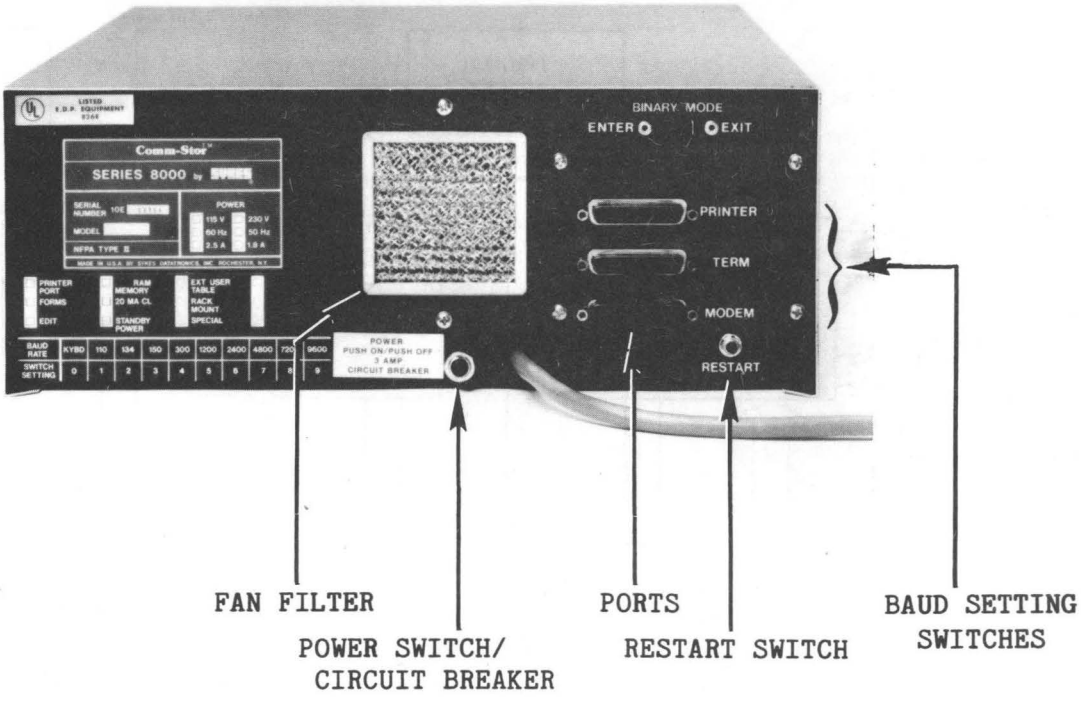
BINARY MODE
ENTER
EXIT
PRINTER
TERM
MODEM
RESTART
Comm-Stor
SERIES 8000
FAN FILTER
POWER SWITCH/
CIRCUIT BREAKER
PORTS
RESTART SWITCH
BAUD SETTING
SWITCHES

FIGURE #1-2

BLOCK DIAGRAM OF Comm-Stor SYSTEM

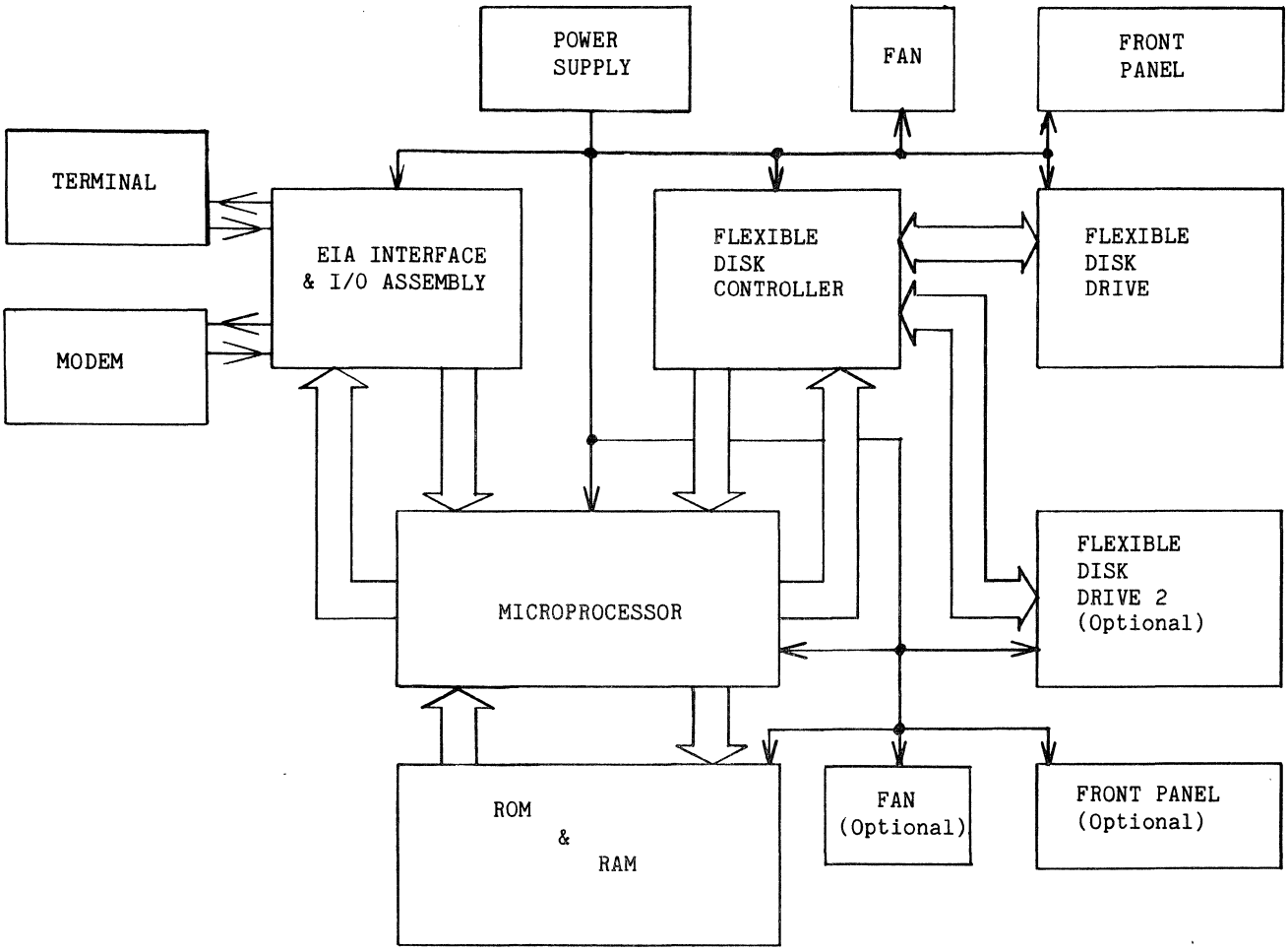

FIGURE #1-3

the I/O panel and multiple connectors on the I/O panel.

F. Microprocessor and Memory

Refer to Chapter 6 for details.

2. MODEL NUMBERS

There are four levels of the Comm-Stor Product: Comm-Stor, Comm-Stor II, Comm-Stor III and Comm-Stor IV. They are available in two basic models: Model 81X0 (Single Drive Unit) and Model 82X0 (Dual Drive Unit). The Comm-Stor product level is identified by replacement of the X with a 0 for Comm-Stor, a 2 for Comm-Stor II, a 3 for Comm-Stor III, and a 4 for Comm-Stor IV.

Available options include:

File Editing
Printer Port
Forms Option
Extended Users Table
3740 Format Program
User Diagnostic Kit
Standby Disk Power
Current Loop Interface
Expanded RAM Memory
Rackmount Cabinet
220 V/50 Hz Power

3. EXPLANATION OF TERMS

DRIVE NUMBER: A number designating a Flexible Disk Drive. In a single drive system the drive number is 1. In a dual drive system the lower drive is number 2 and the upper drive is number 1.

BYTE: A group of 8 binary digits which is the fundamental unit of information written and read to the diskette.

CHARACTER: Same as a Byte.

RECORD: Up to 128 bytes written sequentially on a diskette track. One record of data is contained in one diskette sector. If the record length is less than 128 bytes, the remaining byte positions within the sector are filled in with Fill Bytes by the Series 8000 FDC. A Fill Byte consists of all zeros.

TRACK: A circular band of area on the diskette recording surface that passes beneath the read/write head as the diskette revolves. A diskette has 77 tracks, the outer most track is identified as Track 00 and the inner most track as Track 76.

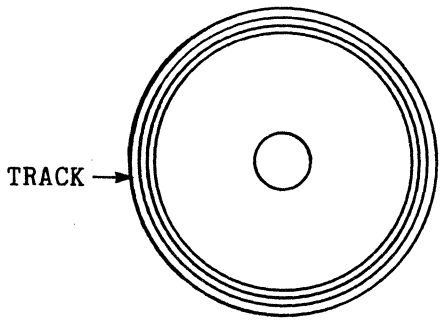

FIGURE #1-4

SECTOR: A record of data preceded and followed by certain control characters and marks essential for the operation of the system. The first sector recorded on a track is identified as Sector 1, and the last as Sector 26.

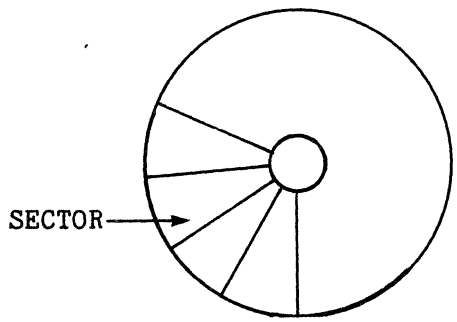

FIGURE #1-5

Figure #1-6 illustrates the Sykes diskette in detail.

4. STANDARD FEATURES

While Comm-Stor has many features, only the more important ones found in the standard system are discussed in this section.

Any storage system must have the capability to store new files. For Comm-Stor, the ENTER command (.E) stores new files from the terminal and the RECEIVE command (.R) stores new files from the modem. Line Cancel and Character Delete editing operations can be performed on files received from the terminal. These editing features are done before the file is stored on the diskette so that the finished file will be error-free.

When these files are stored, the operator assigns each of them a file name which is automatically entered into the Directory. To display the Directory on the terminal, enter a DISPLAY DIRECTORY command (.DD). Similarly, a remote computer can have the Directory sent to it via the modem port (.SD). All or portions of the Directory can be listed, either in the sequence the names appear in the Directory (.SM) or alphabetical order (.AM).

A single file or a group of files may likewise be displayed in sequential order or in alphabetical order. By using the SEND command (.S), files may be sent to the remote computer via the modem port.

A file which is no longer needed is deleted from the system by using the CANCEL command (.CN). This makes space available for new files. Files may also be copied from one diskette to another in a dual drive system (.C).

For operators who frequently change baud rates at different ports, Comm-Stor has the capability to change these baud rates via remote commands (.BM, .BP, .BT) from either the terminal or computer. Any one of fifteen baud rates can be selected in this manner. As Comm-Stor will also perform Auto Answer and Auto Disconnect operations, the ability to change baud rates may be especially important when working under unattended operation and the remote computer desires to change transmission speeds to meet changing line conditions.

5. OPTIONS

A. File Editing

The File Editing option allows the operator to edit an entire file instead of using only Line Cancel and Character Delete features. This option provides character string searches and replacements, as well as line-oriented editing capabilities. A file is stored in a temporary "scratch pad" area on the diskette for editing before it is placed in permanent storage on the diskette. It may be recalled to the scratch pad area at any time for re-editing. Line editing operations consist of:

;List	;Search (and Replace)	;Replace
;Delete	;=Number of Lines	;Append
;Insert	;Number and List	;Clear Buffer

B. Forms Operation

This option provides a forms fill-in capability. Forms are created by the operator and stored on the diskette. They consist of fixed information fields and variable fields to be filled in later.

When a form is requested, it is displayed on the terminal. After the operator enters the variable information, Comm-Stor displays any fixed information up to the next variable field.

When the form is completed, the variable information is stored as a separate file on the diskette. The file, consisting of only the variable information can be sent to a remote computer. This results in a cost savings by reducing transmission time. If desired, however, Comm-Stor will merge the variable information with the fixed information and transmit a completed form.

C. Printer Port

An optional printer port is available for operators with CRT displays who wish to have hard copy printouts of their

files. It is also useful for those operators who have printing terminals but would prefer to use high speed line printers for permanent records. An independent baud rate switch is provided for the line printer.

D. Standby Disk Power

Standby Disk Power allows the operator to turn off disk drive motors if the unit is to be idle for an extended period of time. This is useful particularly when the unit is unattended during evening hours and used only when a computer calls for a data transfer. When Comm-Stor performs the Auto-Answer operation, it automatically starts the disk drive motors. The diskette is up to speed in 2 seconds and ready before the line connections are completed.

E. Current Loop Interface

This option provides a 20 mA Current Loop interface for devices connected to the terminal port. This interface may be connected as either an active interface or as a passive interface. As an active interface, it supplies the 20 mA power source for devices such as a Teletype. As a passive interface, it may be connected to devices such as a computer which provide the necessary power.

F. 220 Volt/50 Hertz Power

Comm-Stor is also available for operation at either or both 220 volts, 50 Hertz operation.

G. Extended Users Table

This option is available for Comm-Stor and Comm-Stor II/IV systems and is <u>standard</u> with Comm-Stor III systems. It provides the ability to create a Macro Command Table up to 256 characters long

SYKE'S DISKETTE

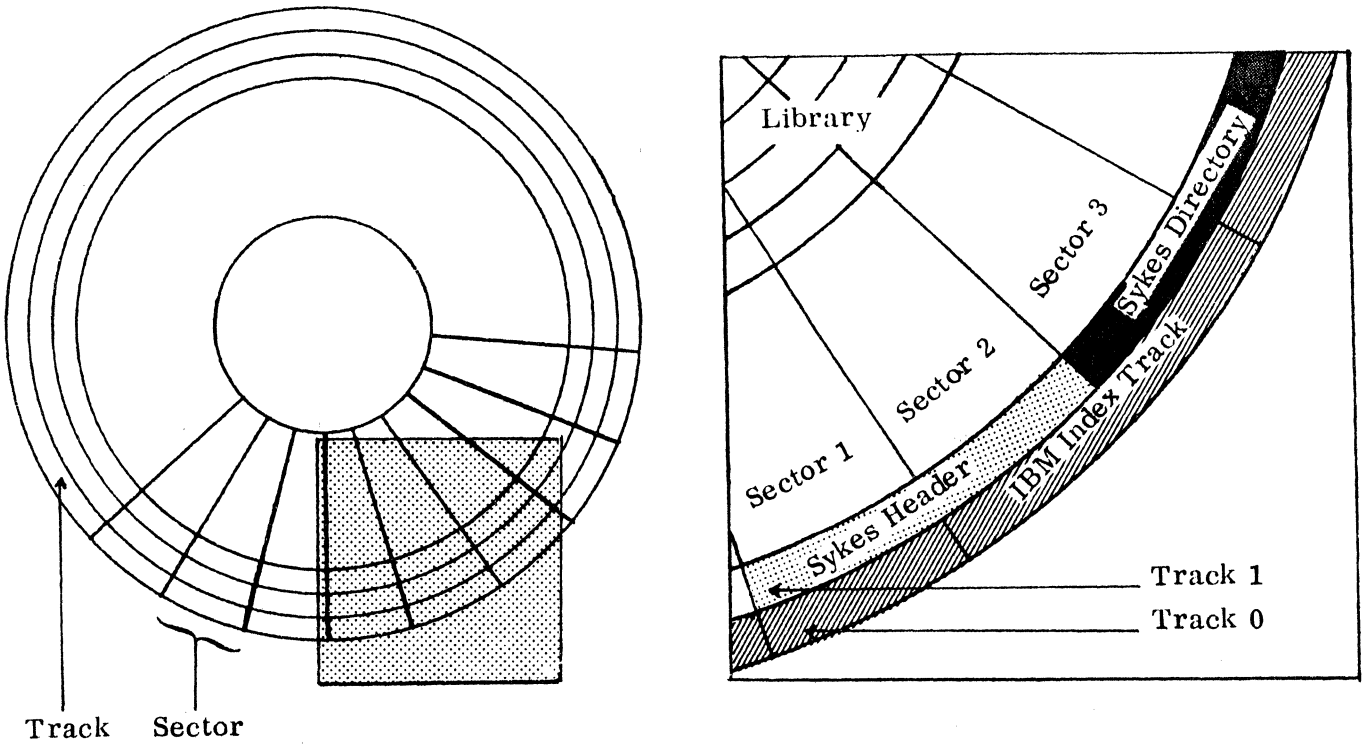

FIGURE #1-6

which may contain several groups of Comm-Stor command strings, each initiated by its own single control character.

H. 3740 Format Program

This option provides compatability between Comm-Stor diskettes and IBM 3740 type equipment. The 3740 Format Program converts files stored on Comm-Stor diskettes to IBM 3740 compatible data sets complete with appropriate data set labels.

6. DISKETTE

A. Data Format

Information is arranged on a diskette in fixed length quantities of data called sectors which are magnetically written on tracks (see Figure #1-6). Each diskette has 77 physical tracks numbered 00 through 76. Track 00, referred to as the Index Track, is the outermost track and Track 76 is the innermost track. The packing density of the data varies from track to track because the amount of data per track remains constant and inner tracks are shorter in length than outer tracks. The packing density of Track 00 is 1,836 bits per inch and of Track 76 is 3,268 bits per inch.

Each track contains 26 sectors numbered 01 through 26. Each sector consists of an Identification (ID) Field and Data Field (see Figure #1-7). The ID Field contains a track and sector value and is preceded by a unique clock/data bit pattern referred to as the Address Mark. The ID Field is terminated by two cyclic redundancy check (CRC) characters that are used by the FDC for verification of this field. The ID Field is followed by the Data Field which contains 128 bytes. The Data Field is preceded by a 17 byte gap then a unique clock/data bit pattern referred to as the Data Mark and is used by the FDC to recognize the beginning of a Data Field. The Data Field is terminated by two CRC characters used by the FDC for the verification of the field.

Only diskettes initialized with the IBM Standard Disk Format can be used in the 8000 System. The initialization process prepares a blank diskette by recording the entire diskette with 2,002 sectors (77 tracks x 26 sectors). The exact data recorded during the initialization process conforms to the IBM Standard Format where Track 00 is the Index Track with data files beginning on Track 01. Diskettes may be initialized with various sector sequences, for example 1,2,3... or 1,3,5, 7... or 1,4,8,12... etc. The Sykes FDC will operate with <u>any</u> sector sequence.

Except for the Index Track, the data recorded during the initialization process is "dummy" data whose purpose is to fill out each sector with 128 bytes. The Index Track (Track 00) is recorded with unique records such as a Volume Label and Data Set Labels.

To maintain IBM compatibility, limit data to tracks 1 through 73. (IBM reserves 3 tracks for diagnostic and spare tracks.) One advantage of maintaining IBM compatibility is the ability to copy the entire diskette off-line using an IBM 3741 type key-to-disk machine. If the user is not concerned with IBM compatibility, data may be written over the entire diskette.

B. Data Capacity

The data capacity of the diskette Figure #1-7, is as follows:

Number of tracks	77
Sectors per track	26
Bytes per sector	128
Bytes per track	3,328
Bytes contained on Tracks 1 through 73	242,944

Address Mark (AM) - Identifies bytes between this Address Mark and the following Data Mark as the ID field of the sector.

ID Field - Identifies the record contained in the Data Field by sector number and track number.

*NOTE: The ID Field and the Data Field are each terminated by two Cyclic Redundancy Check (CRC) characters.

G - 17 byte data gap

Data Mark (DM) - A Data Mark indicates that the Data Field contains a good record.

Data Field - Contains a maximum of 128_{10} data bytes. If less than 128_{10} data bytes comprise the record, the Data field is completed with Fill bytes.

C. Configuration Diskette

The Configuration diskette is supplied by Sykes Datatronics, Inc. It contains prerecorded information for configuring a system and for creating Refresh and User diskettes. Use of the Configuration diskette is covered in the publication "Comm-Stor Configuration Manual."

Any Comm-Stor, Comm-Stor II, III, or IV system parameters can be returned to standard factory configuration using a REV G or higher configuration disk.

D. Refresh Diskette

Once a system is configured, it is possible to store this configuration on a diskette called a Refresh diskette. This is done in conjunction with a Configuration diskette. After a Refresh diskette is created, another Comm-Stor unit can be identically configured by inserting the Refresh diskette and pressing the RESTART button. A Refresh diskette is normally used to configure new systems or to configure systems after maintenance. It may also be used to update a system to a new configuration or to switch between different configurations in the same system.

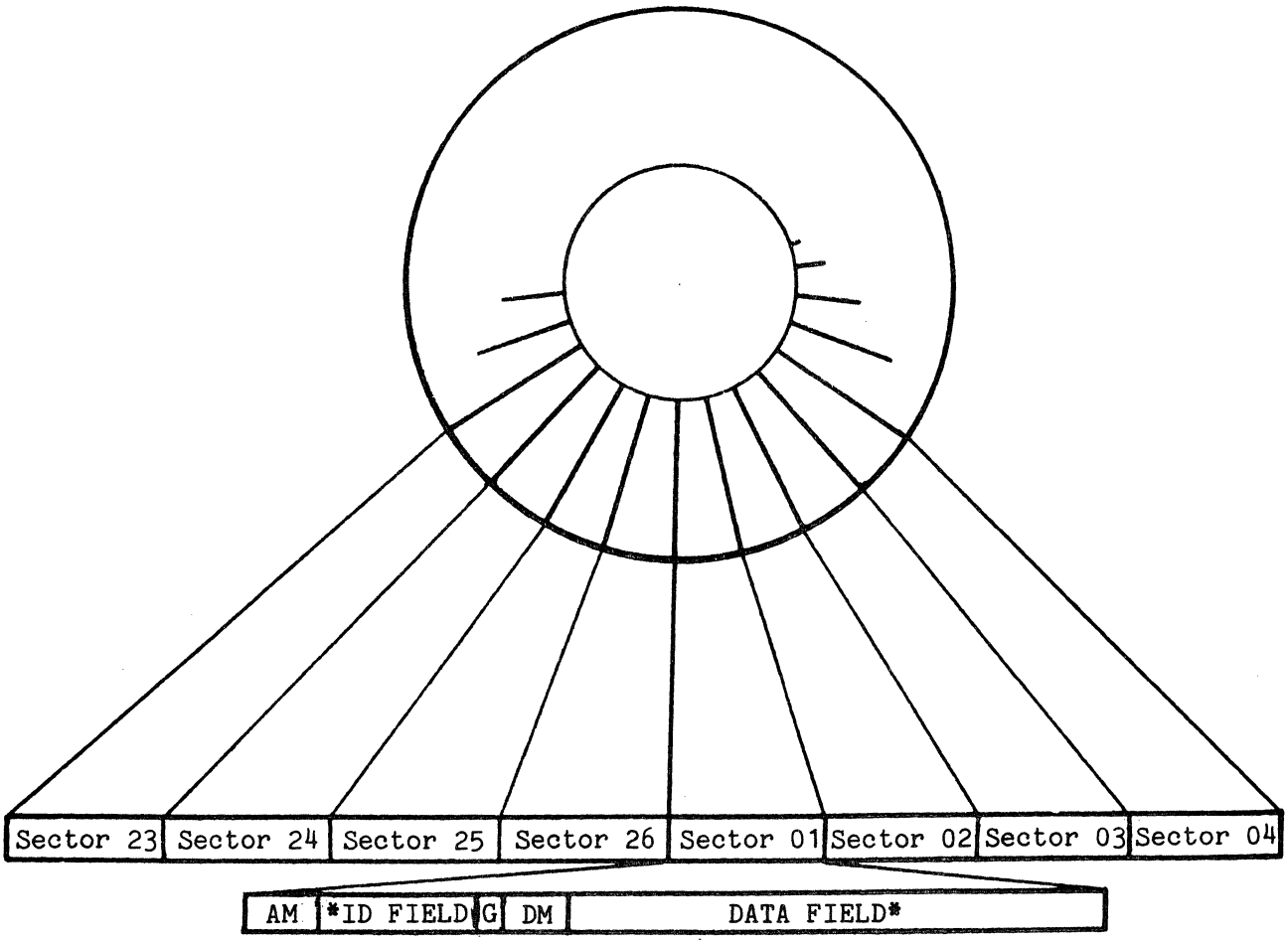

FIGURE #1-7 TRACK FORMAT

E. User Diskette

The User diskette contains a Directory and is used for all normal operations. If not already available, this diskette should be created before proceeding further in the manual.

The User diskette is created using a Configuration diskette. It is initialized with such parameters as the maximum number of characters per file name, the maximum number of characters in the extension, and the maximum file length. Comm-Stor II, III and IV have a Variable Length File feature which makes utmost use of the User diskette. Use of this feature is explained in the "Comm-Stor Configuration Manual."

F. Inserting the Diskette

After powering on Comm-Stor, the diskette is inserted. This is done by raising the front door, inserting the diskette until it can go no further, holding it in the innermost position, and lowering the door. An interlock on the door prevents it from being lowered unless the diskette is fully inserted.

Operators with dual drive units should place the Configuration, Refresh, or User diskette into the upper drive, which is Drive 1; optionally, a second user diskette may be placed in the lower drive.

IT IS IMPORTANT THAT DISKETTES BE INSERTED ONLY WITH POWER ON AS SPINDLE ROTATION ALIGNS THE DISKETTE. A DISKETTE NEED NOT BE REINSERTED IF POWER IS TURNED OFF AND ON AGAIN, PROVIDED THE DOOR OF THE DRIVE IS NOT DISTURBED.

When the drive door is closed, the READY light is lit on the front panel indicating that the respective drive is ready for use.

7. Comm-Stor COMMANDS

Comm-Stor will respond to commands from either the terminal or modem ports. Commands are entered by typing a special character (usually a period) followed by a one-or-two-character abbreviated English language command, and the file name(s) where applicable. All commands are terminated by the End of Line character, usually a carriage return. For a dual drive unit, the number 2 is added to the command to specify the second drive.

Below is a list of Comm-Stor commands and the standard set of abbreviations which are reconfigurable.

.C	Copy	.DD	Display Directory
.CN	Cancel	.DS	Display Status
.D	Display	.E	Enter
.EA	Enter Automatic	.EM	Echo Mode
		.EX	Echo Mode Exit
.LE	Load Extension	.FC	Forms Complete
.LI	Load Initial Value	.FV	Forms Variable
		.FX	Forms Exit
.P	Print	.MM	Monitor Mode
.PD	Print Directory	.MX	Monitor Mode Exit
		.IM	Included Mode
.R	Receive		
.RA	Receive Automatic	.IX	Included Mode Exit
.S	Send	.SB	Standby Mode
.SD	Send Directory	.MV	Move File to Edit Buffer
.SS	Send Status		
.AM	Alphabetical Mode	.SV	Save File in Edit Buffer
.SM	Sequential Mode	.WE	Write Enable
		.WP	Write Protect
.BT	Baud Terminal		
.BM	Baud Modem		
.BP	Baud Printer		

For a complete explanation of Comm-Stor's standard set of commands, control codes and symbols, refer to the appropriate "Comm-Stor Reference Manual".

8. FRONT PANEL INDICATORS

The front panel of Comm-Stor has several indicators to assist the operator. Two of the indicators, READY and BUSY, are duplicated in a dual drive unit to provide information about each drive. When power is turned on, all lamps are illuminated for a short time to allow the operator to

perform a visual lamp test. The function of each indicator is described below.

POWER A switch/indicator to show when power is turned on to the unit (Comm-Stor).

RESTART A switch/indicator to show that power is on and Restarts the system (Comm-Stor II, III, and IV).

READY An indicator which signifies that a diskette has been properly inserted in the drive (when not in Standby Mode).

BUSY An indicator which signifies that data is being transferred to or from the diskette. A diskette should not be removed when the BUSY indicator is illuminated. To interrupt an operation, a Reset command should be entered and the operator should wait until the BUSY lamp extinguishes before removing the diskette.

CARRIER An indication of the presence of a Carrier Detect Signal from the modem. When the modem is in use, the indicator should illuminate continuously with a full duplex modem and while data is being transferred with a half duplex modem.

STATUS This indicator has three purposes: First, it indicates that data is being transferred to or from any of the ports, and Secondly, it indicates the presence of a parity error. The lamp will glow at half brilliance when data is being transferred to or from any port. If a parity error occurs and data is not being transferred through any of the ports, it will illuminate at full brilliance. When a parity error occurs and data is being transferred through a port, the lamp will illuminate at half brilliance but will return to full brilliance after completion of the data transfer. After a parity error, the lamp is extinguished by entering a Reset command.

Thirdly, when Comm-Stor is initially powered on, a check of the Configuration memory is performed. The CMOS memory can be destroyed by loss of battery power or a power surge in the line. Comm-Stor checks a special test byte in CMOS; if it has been altered, the STATUS Light will remain illuminated. The system must be refreshed before normal operations can be performed. The test byte will then return to a normal condition.

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CHAPTER 2

INSTALLATION AND HANDLING

CONTENTS

1. INSTALLATION

A. Unpacking and Inspecting the Unit

After removing Comm-Stor from its shipping container, the operator should visually inspect the unit for any shipping damage. If damage has occurred, an insurance claim is to be made with the carrier immediately.

IT IS NOT NECESSARY TO REMOVE THE COVER TO PERFORM ANY OF THE INSTALLATION OPERATIONS. REMOVING THE COVER AND IMPROPERLY HANDLING THE INTEGRATED CIRCUITS OR OTHER COMPONENTS MAY CAUSE FAILURES IN THESE PARTS.

The operator should retain the shipping container for repacking if service is needed on the unit.

B. Electrical Power

Voltage and frequency requirements are listed on the configuration plate attached to the rear of the unit (see Figure #1-2). Check to be certain that both voltage and frequency agree with local usage.

The units are shipped with a three-prong power plug commonly used in the U.S.A. and Canada. It may be necessary to replace this plug in other areas of the world.

C. Connecting Peripheral Devices

A terminal, printer and modem can be connected to Comm-Stor via industry standard connectors on the rear of the unit. These connectors, commonly called "ports", conform to the Electronic Industries Association (EIA) specification RS-232-C.

Device cables connect to the ports on the rear of Comm-Stor. Except for Current Loop installations, which are discussed later, no special wiring of the cables is necessary and all leads should be wired pin-for-pin.

Terminal Port

The cable from the terminal is connected to the port labeled TERM. This cable should have a male plug in accordance with industry standard procedures.

THE USER MUST PLACE THE TERMINAL IN THE FULL DUPLEX MODE FOR ALL OPERATIONS. THE TERMINAL MUST REMAIN IN THIS MODE FOR BOTH FULL AND HALF DUPLEX MODEM CONNECTIONS.

Printer Port

If the user has the Printer Port option, the cable from the printer is connected to the port labeled PRINTER. This cable should have a male plug in accordance with industry standard procedures.

If the Printer Port is installed but the user does not wish to use it at this time, the connector may be left unterminated.

Modem Port

The cable from the modem is connected to the port labeled MODEM. This cable should have a female plug.

Current Loop Interface Installations

Current Loop Interface installations are made by using pins in the terminal connector not normally used for RS-232-C operation. Four pins carry the necessary Current Loop signals for the terminal. In addition, jumpers are placed between certain pins to make Comm-Stor either an active or a passive Current Loop interface. At any time, the user may disconnect the cable with the jumpers for Current Loop operation and replace it with a standard RS-232-C connector for normal operation. Figure #7-4 contains a wiring diagram for Current Loop operation.

D. Setting Baud Rates

Each port on the rear of Comm-Stor has a corresponding thumbwheel baud rate switch which sets the baud rate for that port. The switches contain the numbers 1 through 9 which relate to a particular rate in accordance with the table on the rear of the unit.

Switch setting 0 is called KYBD rate. In this setting the operator may enter the different baud rates from the terminal keyboard.

The terminal may not have a lower baud rate than the modem; however, the terminal and modem do not need to have equal baud rate settings, even when online operations are desired. It is preferred that the terminal be operated at a higher baud rate than the modem. However, in those cases where batch transmission from the terminal to a remote station is made, the baud rates must be set equal unless terminal input buffering has been implemented in Comm-Stor. Examples of batch transmission equipment are the paper tape reader on a Teletype, or a CRT terminal in the page-transmit mode.

THE RESTART SWITCH MUST BE DEPRESSED AFTER CHANGING ANY OF THE BAUD RATE SWITCHES AS Comm-Stor WILL NOT RECOGNIZE THE NEW BAUD RATE SETTING UNTIL THIS IS DONE.

E. Setting Binary Mode

The BINARY MODE switch on the rear of the unit (see Figure #1-2) should be set to the exit position, except when the Binary Data Mode is used. This is described in detail in the Comm-Stor Reference Manual.

2. MAINTENANCE TOOLS AND MATERIALS

Diskette Carrier Alignment Gauge,
Sykes Part Number 1030B3220
Feeler Gauge Set
Screwdriver, Regular
Screwdriver, Phillips
Digital Volt Meter
Oscilloscope, Dual Trace
Hex Head (Allen Head) Drivers

3. HANDLING AND STORING DISKETTES

Care must be taken to protect diskettes from dust and lint contamination or physical damage. These can prevent proper contact of disk with the read/write head, thus reducing signal strength or obliterating information. Accidental exposure to any magnetic field can produce similar results.

To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

HANDLING PRECAUTIONS:

1. Keep diskettes in the protective storage envelopes provided until actually placed in the FDD; return the diskette to the envelope immediately after use.

2. Store diskettes vertically.

3. Keep diskettes away from magnetic fields and from ferro-magnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.

4. Replace storage envelopes when they become worn, cracked or distorted.

5. Do not write on the diskette with a lead pencil or ball-point pen. Use a felt tip pen.

6. Do not smoke while handling the diskette. Heat and contamination from a carelessly dropped ash can damage the disk.

7. Do not expose diskettes to heat or sunlight. The read/write head cannot properly track a warped disk.

8. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

OPERATIONAL PRECAUTIONS:

1. Do not open diskette carrier door when the BUSY light is on.

2. Do not power-off the system when the BUSY light is on.

3. Do not press the RESTART button when the busy light is on.

4. Always type a Reset character on the terminal to abort a BUSY condition.

CAUTION: FAILURE TO ABIDE BY THE OPERATIONAL PRECAUTIONS COULD RESULT IN ELECTRICAL DAMAGE TO THE DISKETTE.

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CHAPTER 3

ENCLOSURE COMPONENTS

CONTENTS PAGE

REMOVAL/REPLACEMENT PROCEDURES
(See Figure #3-1)

A. Top Cover

1.) Disconnect the Comm-Stor unit from the power source.
2.) Remove the four mounting screws from the bottom of the cover on the underside of the unit.
3.) Slide the cover off from the back of the unit.
4.) Replace in reverse order.

B. Front Panel Assembly

Single Drive Unit

1.) Remove the top cover (above)
2.) Loosen the two screws which connect the front panel to the disk drive. These two screws are located on each side of the disk drive.

NOTE: It may be necessary to remove the circuit board nearest the disk drive in order to loosen the screw on the left side of the drive.

3.) Remove the third screw located on the bottom left side of the front panel. This screw is removed from the topside of the chassis.
4.) Disconnect the two front panel wire harnesses from their corresponding connectors.
5.) The front panel can now be removed by sliding it forward.

Dual Drive Unit

1.) Remove the top cover (above)
2.) Loosen the four screws which connect the front panel to the disk drives.

NOTE: It may be necessary to remove the circuit board nearest the disk drive in order to loosen the screw on the left side of the bottom drive.

3.) Remove the fifth screw located on the bottom left side of the front panel. This screw is removed from the topside of the chassis.
4.) Disconnect the two front panel wire harnesses from their corresponding connectors.
5.) The front panel can now be removed by sliding it forward.

C. LED Assembly

1.) Remove the front panel assembly (section B, above).
2.) Carefully remove metal spring retainer on LED to be replaced.

NOTE: This is done by working each side of the retainer out a little at a time being careful not to break the plastic enclosure.

3.) The LED assembly can now be pulled out of the front panel.
4.) The LED assembly wires can be removed from the harness and connector by cutting the harness tie wrap. The wires should be isolated at the connector and removed by inserting a sharp object in the side of the connector where the wires terminate. The wires can then be pulled out of the connector.
5.) Replace in reverse order.

D. Comm-Stor Power Switch Assembly

1.) Remove the front panel assembly (section B, page 3-1).
2.) Press the power switch out from the wire side of the front panel.
3.) Remove the 22-gauge black and white wires from the harness which includes the LED assembly wires.
4.) Remove the wires from the connector by inserting a sharp object in the side of the connector where the wires terminate. The wires can then be pulled out of the connector.
5.) Disconnect the 18-gauge red and black wires at the remaining connector.
6.) Replace in reverse order.

E. Comm-Stor II/III/IV Restart Switch Assembly

1.) Remove front panel assembly (section B, page 3-1).
2.) Press the Restart switch out from the wire side of the front panel.
3.) Remove the 22-gauge black and white wires from the harness which includes the LED assembly wires.
4.) Remove the wires from the connector by inserting a sharp object in the side of the connector where the wires terminate. The wires can then be pulled out of the connector.
5.) Replace in reverse order.

F. Filter Cover, Air Filter

1.) Remove the two screws which fasten the filter cover.
2.) Remove the filter cover and air filter.
3.) Replace in reverse order.

G. Interface Panel

1.) Remove the top cover (section A, page 3-1).
2.) Remove connector P1 from EIA circuit board (Assembly No. 1030A6051).
3.) Remove connector P2 from printer circuit board (Assembly No. 1030A6175 or 5012 Printer option only).
4.) Remove the four screws from the back of the interface panel.
5.) Replace in reverse order.

H. Air Deflector

1.) Remove the top cover (section A, page 3-1).
2.) Remove the tie wrap which holds the deflector to the fan.
3.) The deflector may be lifted straight up and out of the unit.
4.) Replace in reverse order.

I. Fan Assembly

1.) Remove the filter cover (section F, above).
2.) Remove the air deflector (section H, above).
3.) Remove the four rivets which hold the fan in place. These rivets must be drilled out. AVOID GETTING METAL SHAVINGS INSIDE THE UNIT.
4.) Disconnect the fan wire connector.
5.) Replace in reverse order.

J. Circuit Breaker

1.) Remove the air deflector (section H, above).
2.) Remove the nut which holds the circuit breaker to the back of the chassis.
3.) Disconnect the two wire lugs which are connected to the circuit breaker.
4.) Replace in reverse order.

K. Line Filter Assembly

1.) Remove the top cover (section A, page 3-1).

2.) Remove the two rivets which fasten the line filter to the chassis. These rivets must be drilled out. AVOID GETTING METAL SHAVINGS INSIDE THE UNIT.
3.) Disconnect the line filter wire harness connector.
4.) Replace in reverse order.

L. Power Cord Assembly

1.) Remove the top cover (section A, page 3-1).
2.) Locate the black, white and green power cord wires at the rear of the chassis.
3.) Remove the white wire from the 1-wire connector.
4.) Remove the black wire from the circuit breaker.
5.) Remove the green wire from the chassis ground point.
6.) Remove the rubber grommet which holds the power cord in place at the rear of the chassis.

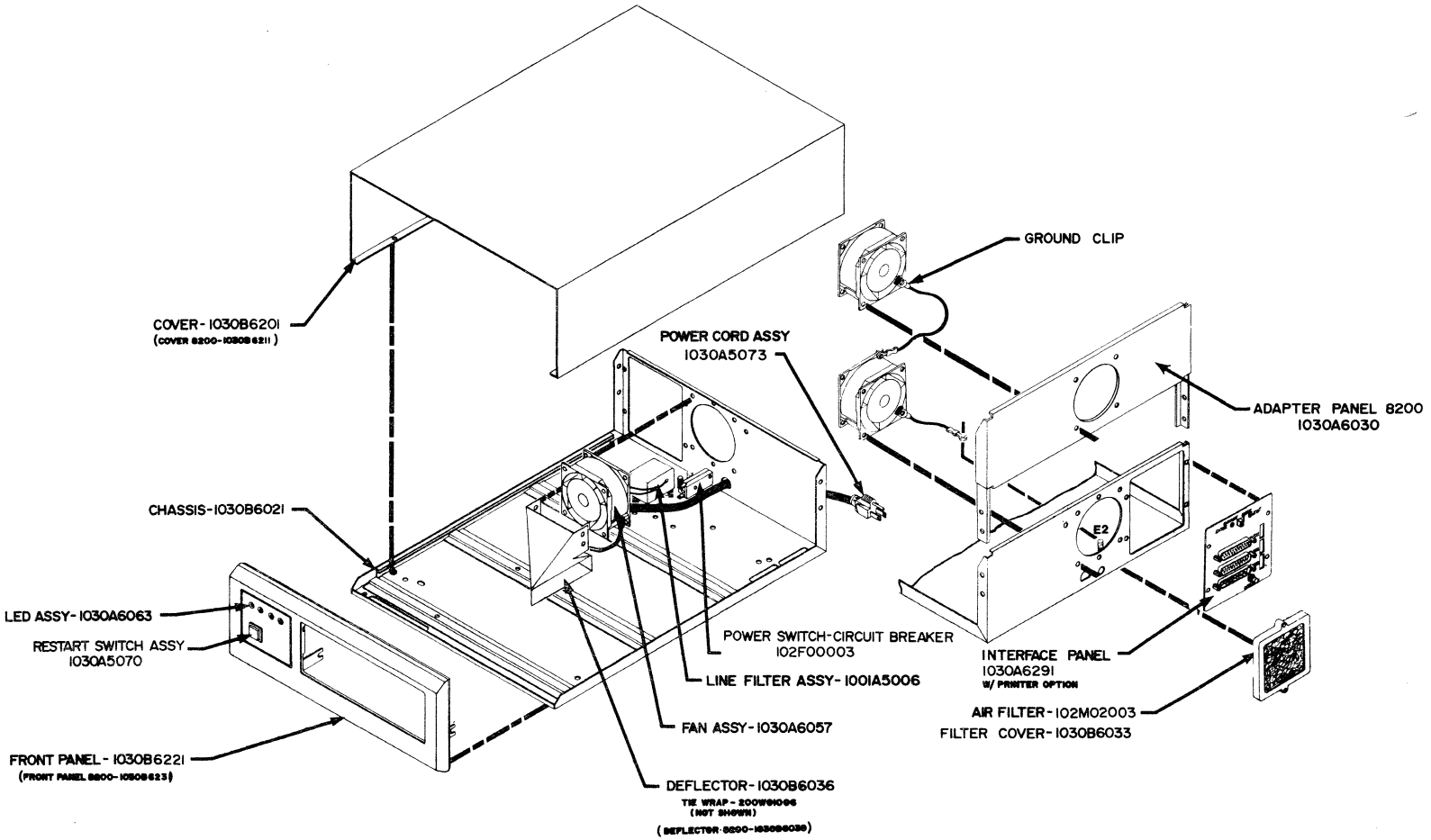


FIGURE #3-1 ENCLOSURE COMPONENTS

CHAPTER 4

FLEXIBLE DISK DRIVE

CONTENTS PAGE

CONTENTS PAGE

1. FLEXIBLE DISK DRIVE

This chapter will discuss the FD 700 Flexible Disk Drive (FDD), Sykes Part Number 1030C3000, which is an integral part of the Sykes Comm-Stor system.

A. General

The FD 700 is a small, portable, direct access, data storage device that interfaces to a host system via a control unit. (See Figure #4-1.)

The FD 700 mechanism positions a read/write head to discrete positions or tracks on the spinning diskette surface. Magnetic data is written on or read from the diskette surface by the read/write head. The drive uses a single, oxide coated mylar disk enclosed in a sealed envelope to form a diskette. The diskette and information are fully IBM compatible.

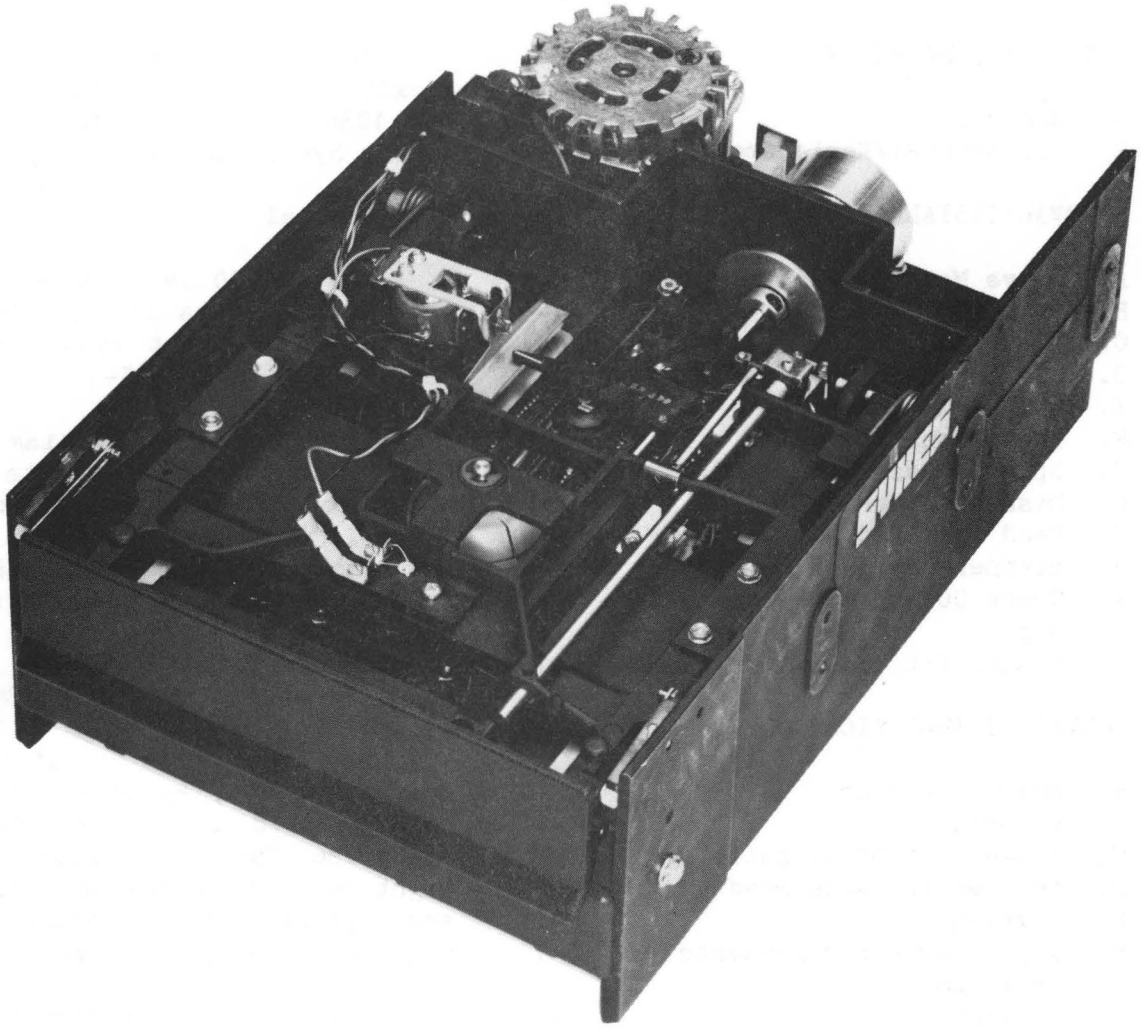
The mechanism consists of a belt driven spindle, spindle motor, read/write head mounted on a stepping motor drive mechanism for track accessing, indexing light emitting diode and phototransistor, and a printed circuit board to provide all required internal electronic functions.

The drive components are mounted in a base-enclosure with a front panel. The front panel contains a cam-operated door mechanically linked to the disk mechanism. The door will remain stationary in the open or closed position.

B. FDD Removal/Replacement

Single Drive Unit

1.) Remove the top cover (section A, page 3-1).



FLEXIBLE DISK DRIVE

FIGURE #4-1

2.) Remove the front panel assembly (section B, page 3-1).
3.) Remove the six retaining screws from the bottom of the chassis.
4.) Slide the drive forward approximately two inches and remove the power connector and disk drive interface cable from the rear of the drive.
5.) Remove drive from unit.
6.) Replace in reverse order.

Model 8200 - Upper Drive

1.) Remove the top cover (page 3-1).
2.) Remove the front panel assembly (page 3-1).
3.) Remove the four drive mounting screws, two on each side of the drive.
4.) Slide the drive forward approximately two inches and remove the power connector.
5.) Disconnect the disk drive interface cable and power supply connector from the Drive board located under the drive.
6.) Remove drive from unit.
7.) Replace in reverse order.

Model 8200 - Lower Drive

1.) Remove the upper disk drive assembly (above).
2.) Remove the six retaining screws from the bottom of the chassis.
3.) Slide the drive forward approximately two inches and remove the power connector.
4.) Disconnect the disk drive interface cable and power supply connector from the Drive board located under the drive.
5.) Remove drive from unit.
6.) Replace in reverse order.

2. REMOVAL/INSTALLATION PROCEDURES

See Figures #4-2, #4-3, #4-4, and #4-5.

Remove the FDD as described on page 4-1.

A. Drive Motor Assembly

1.) Disconnect motor from AC connector.
2.) If applicable, remove screw holding capacitor clamp to the base. Remove plastic caps and disconnect motor leads from capacitor.
3.) Remove belt from drive and motor pulleys.
4.) Remove fasteners holding the motor to the base casting and remove motor.
5.) Replace in reverse order.

Note: Insure ground lead is reinstalled correctly.

B. Motor Drive Pulley

1.) Loosen set screw and remove pulley.
2.) Replace in reverse order.

Note: When installing a new pulley, the drive pulley must be on the motor shaft far enough to clear the bottom of unit.

C. Diskette Carrier Access

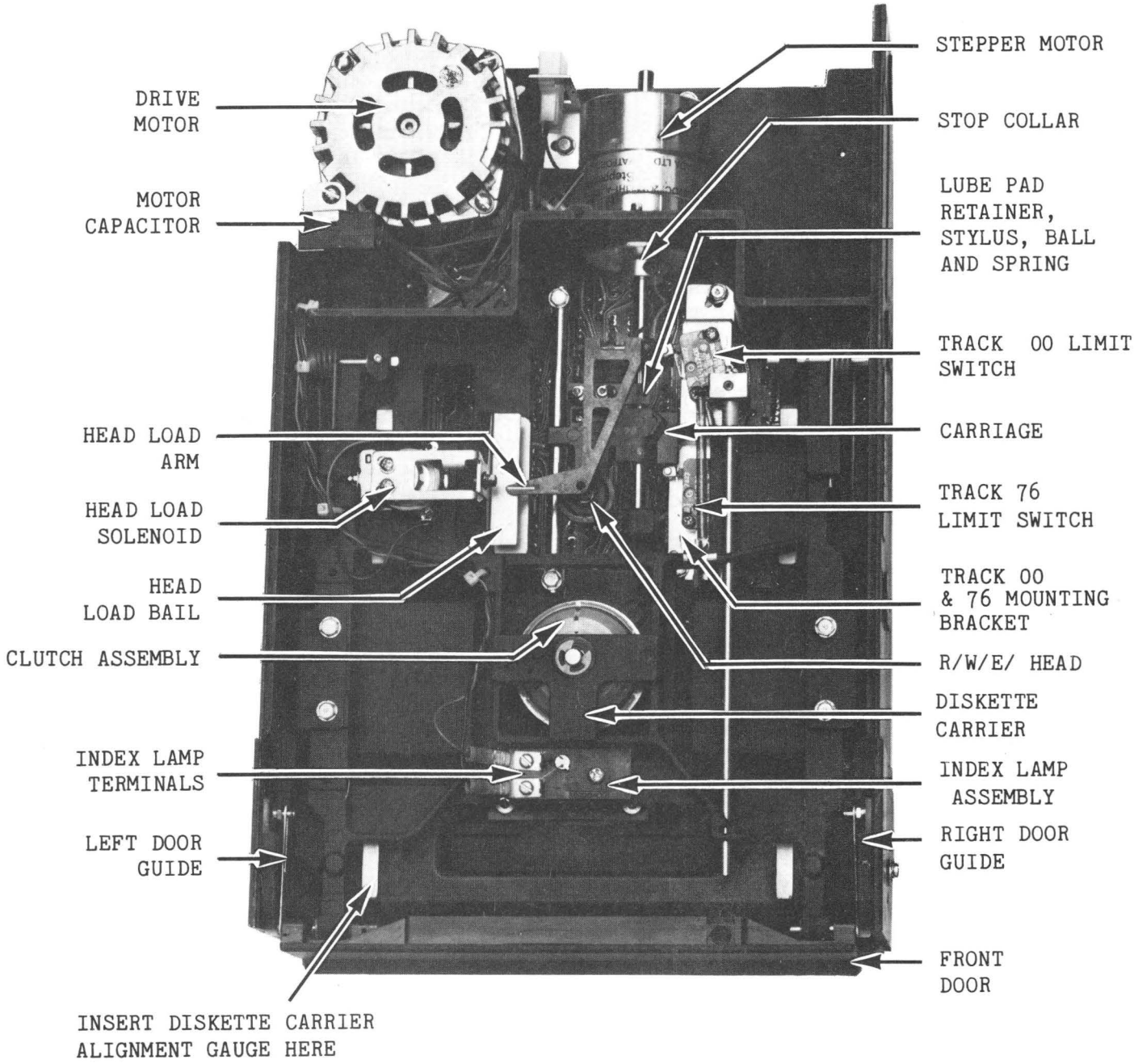
1.) Remove front panel (see page 3-1).
2.) Position head to approximate center of head load bail by turning shaft.
3.) Remove door stop arms from door stop pins by removing E-ring from each and sliding off.
4.) Swing carrier up by carefully closing front door and unlatching it from door guides.

CAUTION: CARRIER IS SPRING LOADED. USE EXTREME CARE WHEN OPENING CARRIER.

5.) Reverse procedure to close carrier. Ensure that both torsion springs on the carrier pivots are correctly positioned and that the door rollers and stop arms are mounted to the pins on the sides of the door. Reconnect door stop arms.

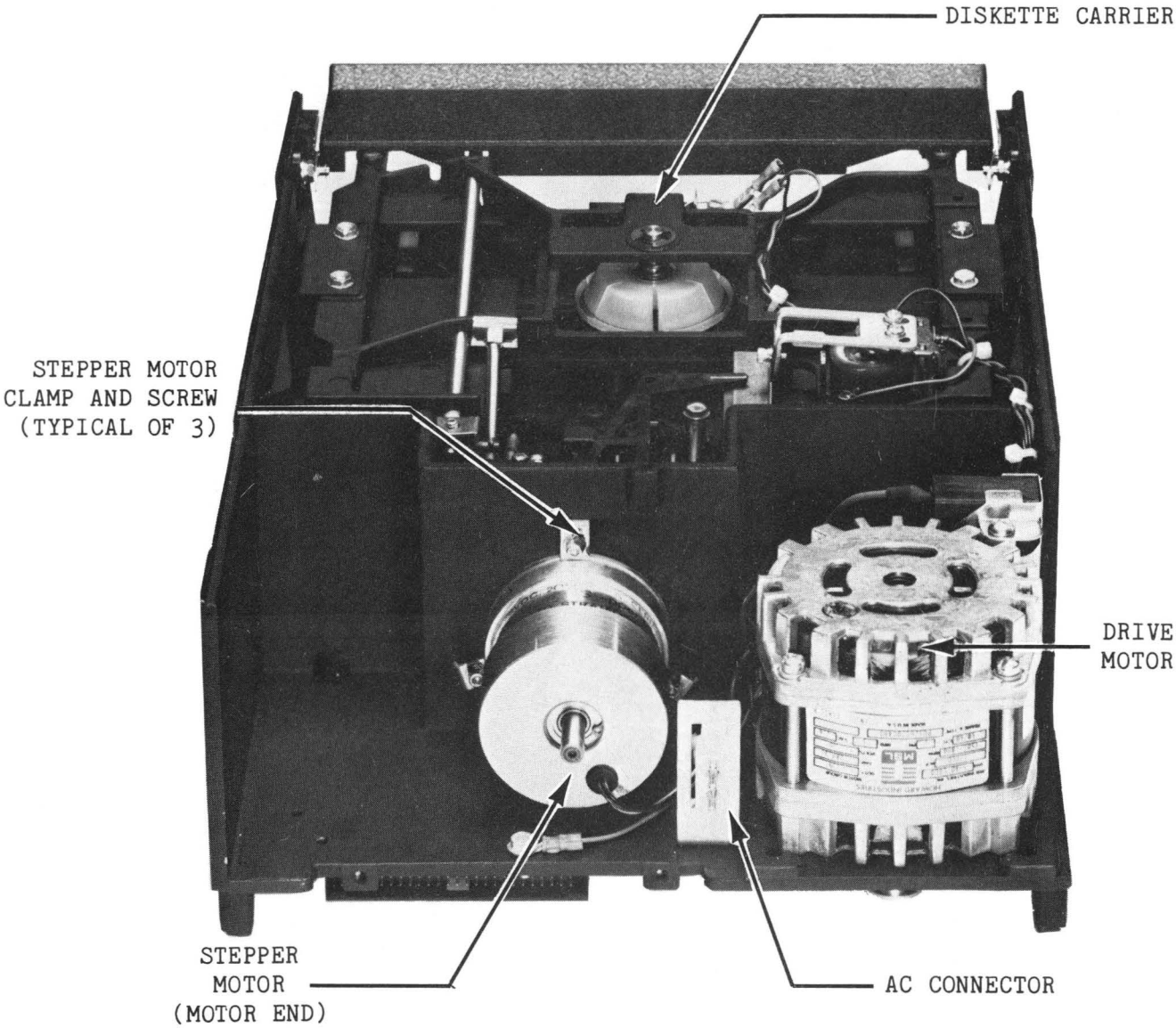
D. Index Sensor Lamp Assembly

1.) Disconnect the wires to the LED terminals (quick disconnects).
2.) Remove the screw and washer holding the assembly to the diskette carrier.
3.) Replace in reverse order.



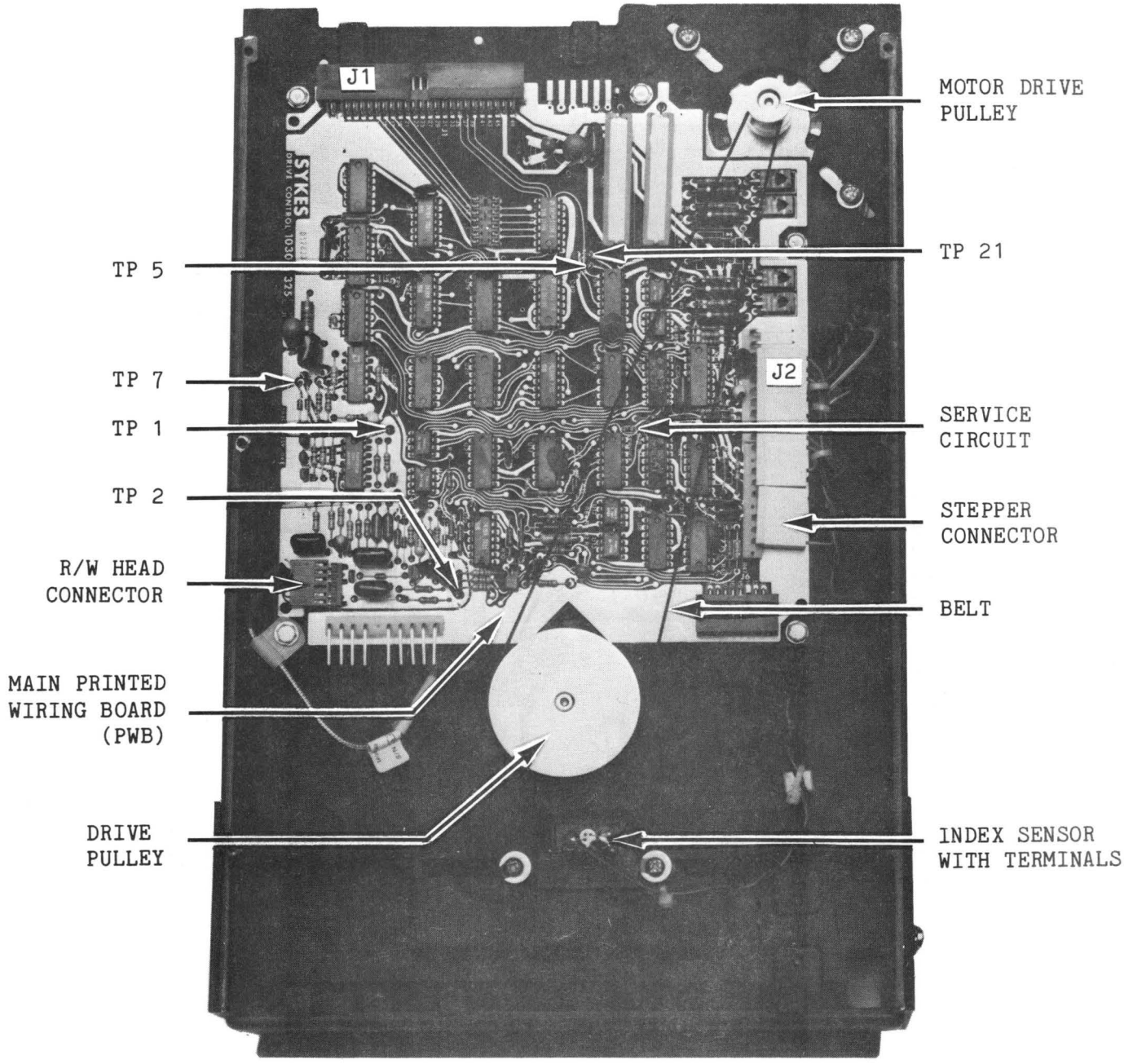
TOP VIEW OF FD 700

EIGURE #4-2



REAR VIEW OF FD 700

FIGURE #4-3



BOTTOM VIEW OF FD 700

FIGURE #4-4

to the cleaned surface. Remove the green paper from the pad and press the white surface against the contact cement and hold.

CAUTION: TAKE EXTREME CARE TO GET THE PAD IN STRAIGHT AND DO NOT GET CONTACT CEMENT ON THE SURFACE OR SIDES OF THE PAD.

5.) Connect system to power source and turn power on. Insert a diskette into the drive; close the door. Load the head by jumpering the black wire on the head load solenoid to ground. Allow the glue to dry for approximately 1 (one) hour.
6.) Turn the power off and disconnect the unit from the power source. Remove the jumper and disk.
7.) From the bottom of the chassis, remove the six phillips head screws which hold the FDD assembly to the chassis.
8.) Without disconnecting the FDD cables, rotate the FDD on its side so the top and bottom of the FDD are accessible.
9.) Connect a true R.M.S.A.C. Voltmeter or an Oscilloscope to TP1 on the Drive Control Circuit Board.
10.) Power up the system. The four front panel LEDS should come on for one second and then go off.
11.) Load a diskette into the system.
12.) Load the head by jumpering the black wire on the head load solenoid to ground.
13.) While observing the voltage at TP1, press down slightly on the head load arm. The amplitude at TP1 should not change by more than 10%. If it does, the media must be flying. This condition can cause Read/Write errors and must be corrected:
    a.) Check the head load bail adjustment (see service manual) and correct if necessary.
    b.) Inspect the pad for any ridges. If necessary, use a fine emery cloth and gently rub the surface of the pad to insure a flat surface.
    c.) Repeat procedure in step 13.
14.) Remove the head load jumper.
15.) Turn power off and disconnect from power source.
16.) Reinstall the FDD and top cover.

J. Stepper/Carriage

1.) Disconnect the connectors from the PWB (PRINTED WIRING BOARD).
2.) Remove screws holding the cable clamp nearest the stepper motor. Remove the stepper cable from the clamp.
3.) Remove screws holding the head cable clamp next to Track 00/76 switch bracket.
4.) Remove two screws on the carriage and carefully remove lube pad retainer, stylus spring and stylus ball.

CAUTION: BE VERY CAREFUL WITH THE STYLUS BALL. IT IS VERY SMALL AND EASY TO MISPLACE.

5.) Loosen three stepper motor clamp screws and rotate clamps away from motor body.
6.) Pull the motor back far enough to allow the shaft to clear the carriage bearings. Carefully remove the carriage assembly.
7.) Add one drop of light machine oil to the lube pad upon reassembly. A small amount of non-silicone grease will hold the stylus ball in place on the stylus spring during reassembly.
8.) Adjust Head/Track alignment (see page 9-3).
9.) Adjust Track 00 stop (see page 9-6).
10.) Adjust Track 00 and 76 switches (see page 9-3).
11.) Adjust index (see page 9-4).
12.) Replace top cover.

K. Track 00 and 76 Switch Assembly

1.) Manually rotate clockwise stepper shaft and move carriage to Track 76.
2.) Remove cable connectors from both switches.

3.) Remove two screws holding bracket to base casting and remove bracket and switches.
4.) Remove screws holding switches to bracket and remove switches.
5.) Replace in reverse order.

L. Clutch Assembly Installation

1.) Open the drive door (both doors in a dual drive unit).
2.) Remove the front panel assembly (page 3-1).
3.) If replacing the clutch assembly for Drive 2, Drive 1 must first be removed (page 4-1).
4.) Position head to approximate center of head load bail (see Figure #4-6) by manually turning the stepper motor shaft.
5.) Swing up the diskette carrier assembly (see Section C, page 4-3).

CAUTION: THE CARRIER ASSEMBLY IS SPRING LOADED. USE EXTREME CARE WHEN OPENING IT.

6.) Remove door rollers and stop arms from door assembly and store them in a safe place.
7.) Locate the Clutch Assembly (see Figure #4-6).
8.) Push up on the clutch pin from the bottom; carefully remove the C-clip which holds the clutch pin to the Carrier Assembly.

CAUTION: THE CLUTCH IS SPRING LOADED AND MUST BE REMOVED SLOWLY.

9.) Assemble new clutch using existing parts and new shims (Item #5) as shown in Figure #4-7.
10.) Reinstall clutch and attach C-clip to clutch pin.
11.) Replace door rollers and stop arms and close the carrier. Be sure both torsion springs on the carrier pivots are correctly positioned. Reconnect stop arms.

Note: Drive door must remain open.

12.) Replace front panel and reconnect cables.

3. EQUIPMENT SPECIFICATIONS

The equipment specifications for the FD 700 Diskette Drive are as follows:

A. Accessing Time

Average Latency	83 ms
Access Time	6 ms track to track; 14 ms Settle
Head Load Time	50 ms

B. Recording

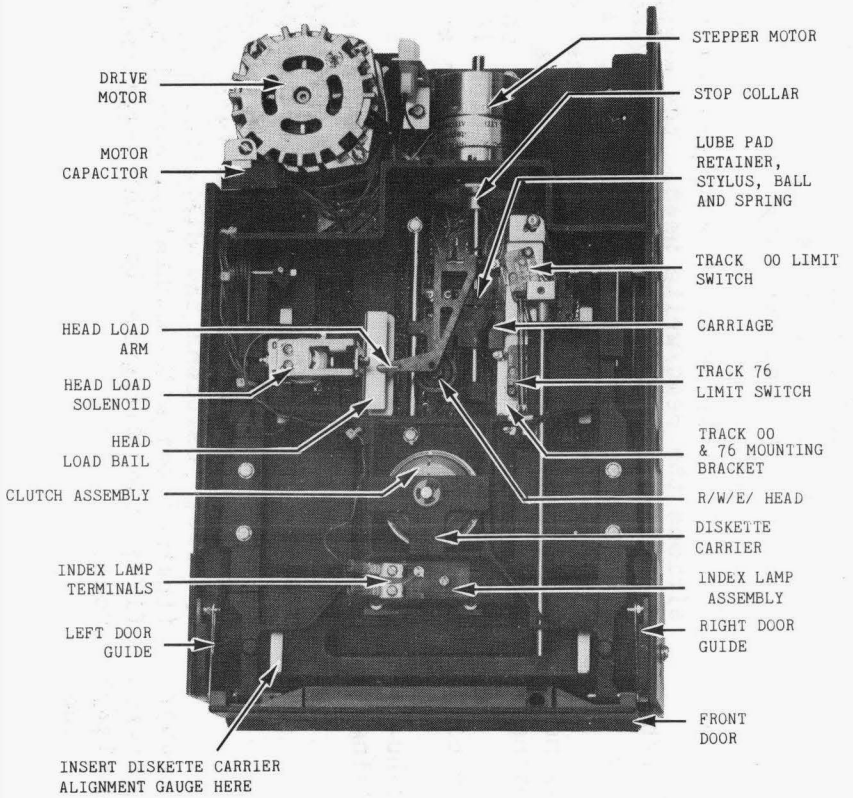
Mode	Double Frequency (Standard)
Density (Nominal)	1836 bpi (outer track) 3268 bpi (inner track)
Data Transfer Rate	250,000 bits/sec nominal
Sectors (soft)	IBM 3740 or equivalent

C. Diskette (IBM Compatible)

Disks/Cartridge	1 (8 x 8 inches including envelope)
Useable Recording Surfaces/Disk Cartridge	1 or 2
Disk Surface Diameter	7.88 inches
Recording Diameters	Track 76 (inner) 2.0290 inches nominal; Track 00 (outer) 3.6123 inches nominal
Disk Surface Coating	Magnetic Oxide
Disk Rotational Speed	360 rpm $\pm$ 2%

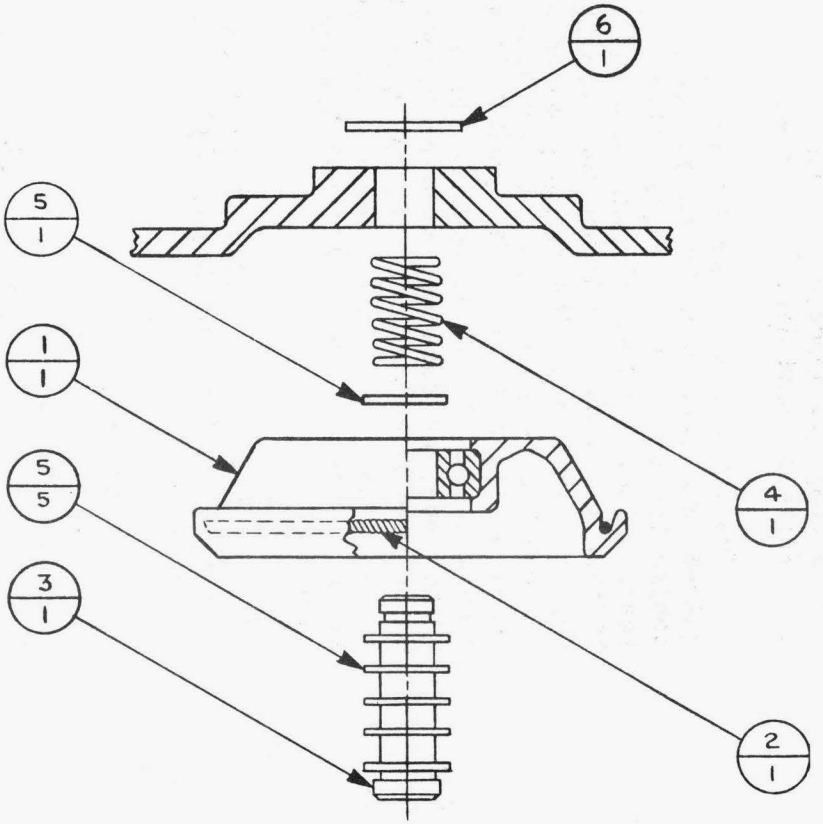
D. Read/Write/Erase Head

Head/Unit	1
Track Width	.014 inch
Track Spacing	0.02083 inch (48 tracks per inch)
Erase to Read/ Write Gap	.033 $\pm$ 0.003 inch



FLEXIBLE DISK DRIVE

FIGURE #4-6



ITEM NO.	QTY.	DESCRIPTION	SYKES P/N
1	1	Clutch/Bearing Assembly	1030A3302
2	1	Spring, Garter	1030B3132
3	1	Pin, Clutch	1030B3120
4	1	Spring, Compression	1030B3194
5	6	Shims	100B03006
6	1	Ring, Retaining	500H60107

CLUTCH ASSEMBLY

FIGURE #4-7

E. **Physical (Figure #4-8)**

Height	4.53 inches
Width	9.01 inches
Depth	14.12 inches
Weight	15 lbs.

F. **Input Power Requirements (Maximum)**

DC +24 volts (±5%) @ 1.5A
+5 volts (±5%) @ 0.75A
-12 volts (±5%) @ 0.10A

AC 100 VAC ± 10% 50/60Hz ± 0.5 Hz
115 VAC ± 10% 60 Hz ± 0.5 Hz
208/230 VAC ± 10% 60 Hz ± 0.5 Hz
240 VAC ± 10% 50 Hz ± 0.5 Hz

The maximum current consumption with this input voltage is as follows:

Operating current (diskette turning, steady-state):

110/115V	1.50A max (motor start)
	1.25A max (run current)
208/230/240V	0.75A max (motor start)
	0.65A max (run current)

G. **Environment**

Operating and storage environments of the FD 700 are as follows:

Operational	50° to 100° F (12° F/hr maximum fluctuation)
	20% to 80% relative humidity (non-condensing)
Non-operational (storage)	(with diskette removed) -30° to +150° F
	5% to 95% relative humidity (non-condensing)

4. THEORY OF OPERATION

A. General

The FDD consists of control and read/write electronics, diskette drive motor, read/write head, track access mechanism, and removable diskette cartridge. The functions of the FDD are:

1.) Receive and generate control signals
2.) Access the appropriate track
3.) Write or read data on command

The functions of the FDD and the required interface signals to and from the controller are shown in Figure #4-9. The Read, Write, and Control Logic are the interface electronics between the Comm-Stor FDC and the drive. The stepping motor positions the read/write head to the desired track on the diskette. The head load solenoid loads the disk against the read/write head and data may then be recorded on or read from the diskette. Each of the logic blocks and signal names shown are later discussed under Logic and R/W Functional Descriptions.

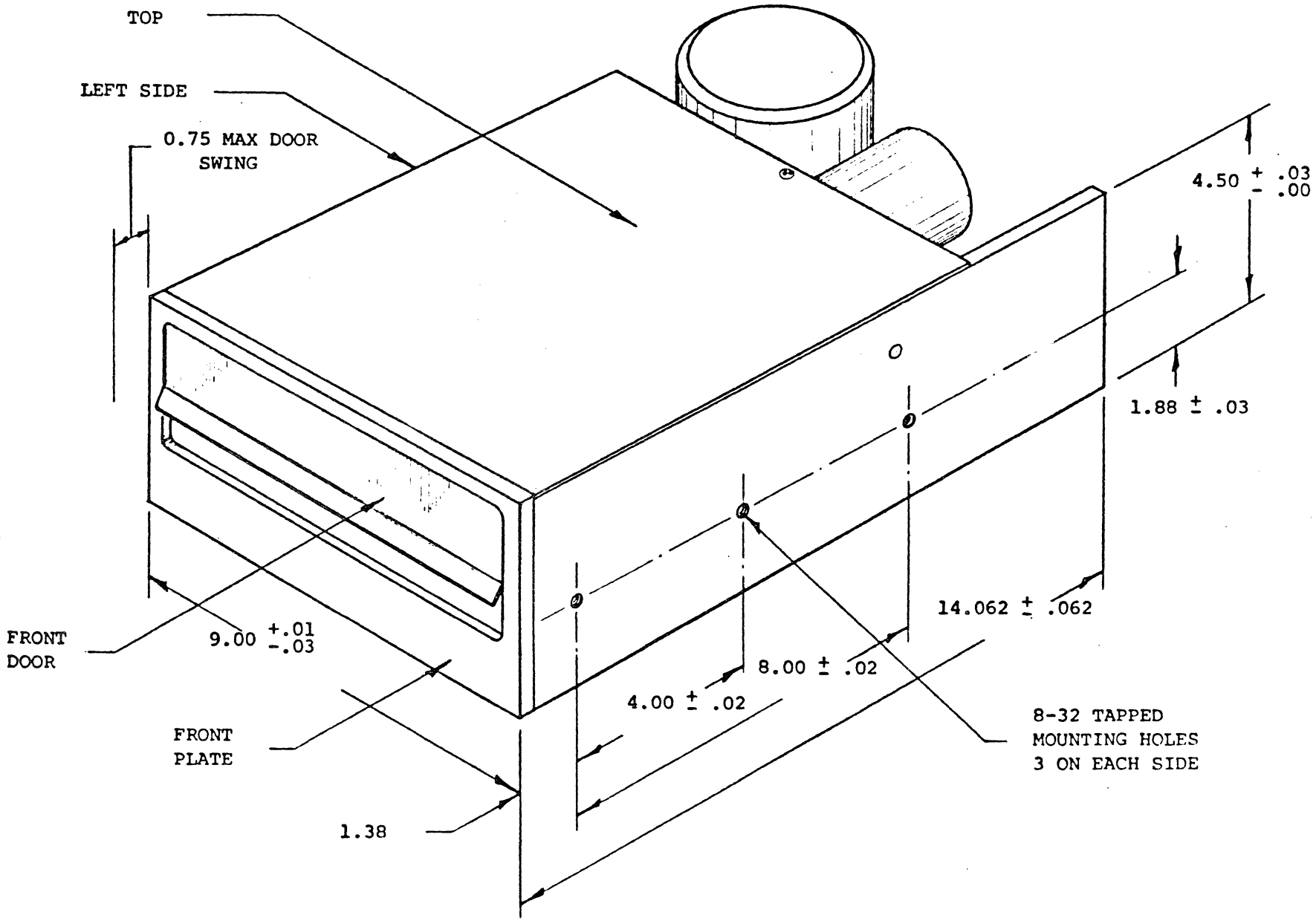
The electronic circuitry is packaged on one Printed Wiring Board (PWB). (See Figure #4-4.)

The PWB contains:

1. Index Transducer Circuit
2. Track Position Stepping Motor Circuits
3. Head Load Circuit
4. Read/Write Circuits
5. Drive Select Circuits

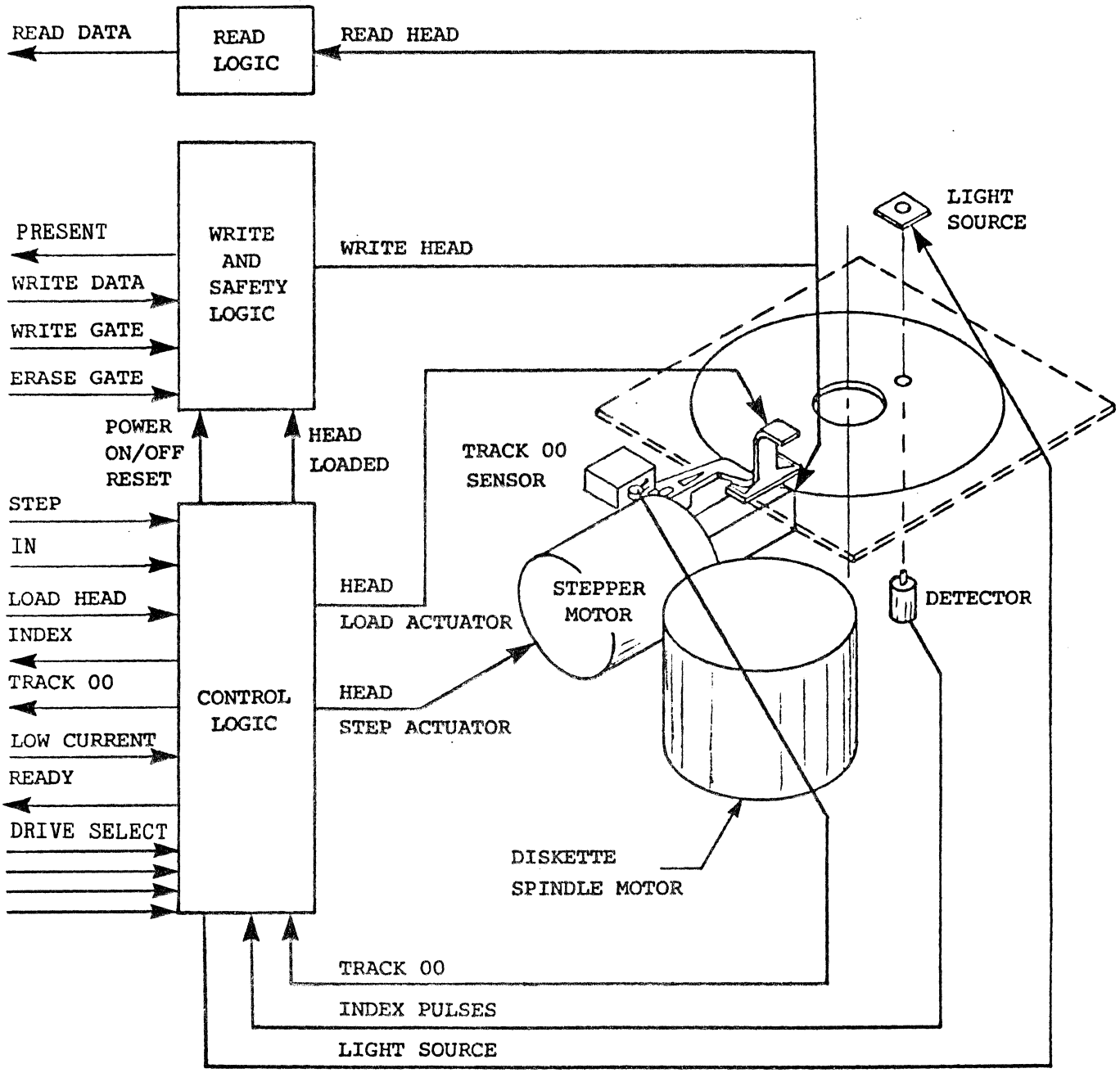
The stepping motor and lead screw positions the read/write head. the stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The Comm-Stor FDC steps the stepping motor to the desired track. Track verification is accomplished by checking track and or sector address.

The diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by means of a pulley change. A registration cone, centered on the face of the spindle, positions the diskette. A clamp (that closes with mechanical door linkage) fixes the diskette to the registration cone.



FD 700 PHYSICAL DIMENSIONS

FIGURE #4-8



FD 700 FUNCTIONAL BLOCK DIAGRAM

FIGURE #4-9

The read/write head is in contact with the diskette when loaded. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the disk with minimum head/diskette wear. The tunnel erase DC erases the inter-track area to improve off track signal-to-noise ratio and permit diskette interchangeabili v from unit to unit.

The read/write head is mounted on a carriage that is moved by the stepper motor drive shaft. Head load is achieved when the diskette is loaded against the rigidly mounted head by moving a load pad against the diskette with the solenoid actuated bail. Head to diskette compliance is achieved by restraining the diskette between the head and the load pad.

B. Interface Description

The interface of the FDD is divided into two categories: Signal/Data Interface and Power Interface. The initial Power Up and Read/Write sequences are shown in Figures #4-10 and #4-11 respectively.

Signal/Data Interface

Input Lines

There are eight low active TTL (Transistor-Transistor Logic) input lines to the FDD: Direction, Step, Load Head, Drive Select Lines, Write Gate, Write Data, Erase Gate and Low Current. Each line has the following characteristics:

Logic 1	Active: 0V to 0.4V
Logic 0	Inactive: +2.5V to +5.5V
Input Impedance	220 ohms to +5V and 300 ohms to GND.

1.) IN Line

This interface signal defines the direction of motion of the R/W head when the Step line is pulsed. A low active level on this line causes the Head Position Mechanism to move the read/write head towards the center of the disk when the Step line is pulsed. With the IN line at an inactive level, a pulse on the Step line causes the Head Position Mechanism to move the read/write head away from the center of the disk. The state of IN line must not change until 200ns after the leading edge of the Step pulse.

2.) Step

A low active level (10 usec) on this line will cause the read/write head to be moved one track. The direction of movement is controlled by the IN line. The state of the IN line is sampled 100 $\pm$ 30 nsec after the leading edge of step. Access timing relationships conform to Figure #4-10.

3.) Load Head

A low active level on this line causes the storage element to be placed in direct contact with the read/write head for data recording or retrieval. Load Head may be activated at any time after power has been applied; however, this line must be activated at least 50ms prior to a read or write operation. During periods of no data transfer this line should be deactivated to provide for maximum storage element and head life.

4.) Drive Select Lines

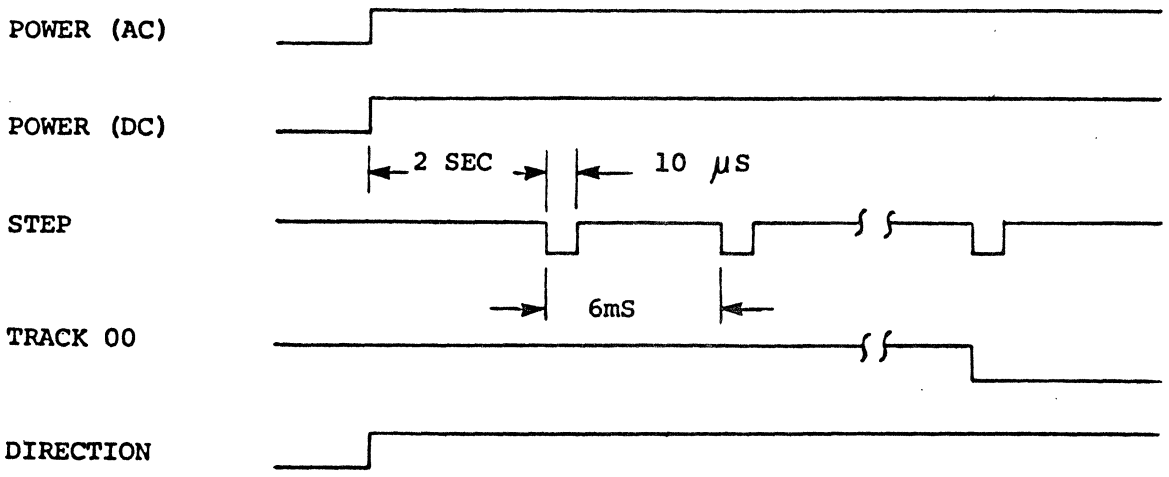
Four input lines, labeled SEL 1,2,3, 4, are used to select the drive number. A high active level on any one of the select lines enables the specified drive.

5.) Write Gate

A low active level on this line enables the write current source, and disables the stepping circuitry.

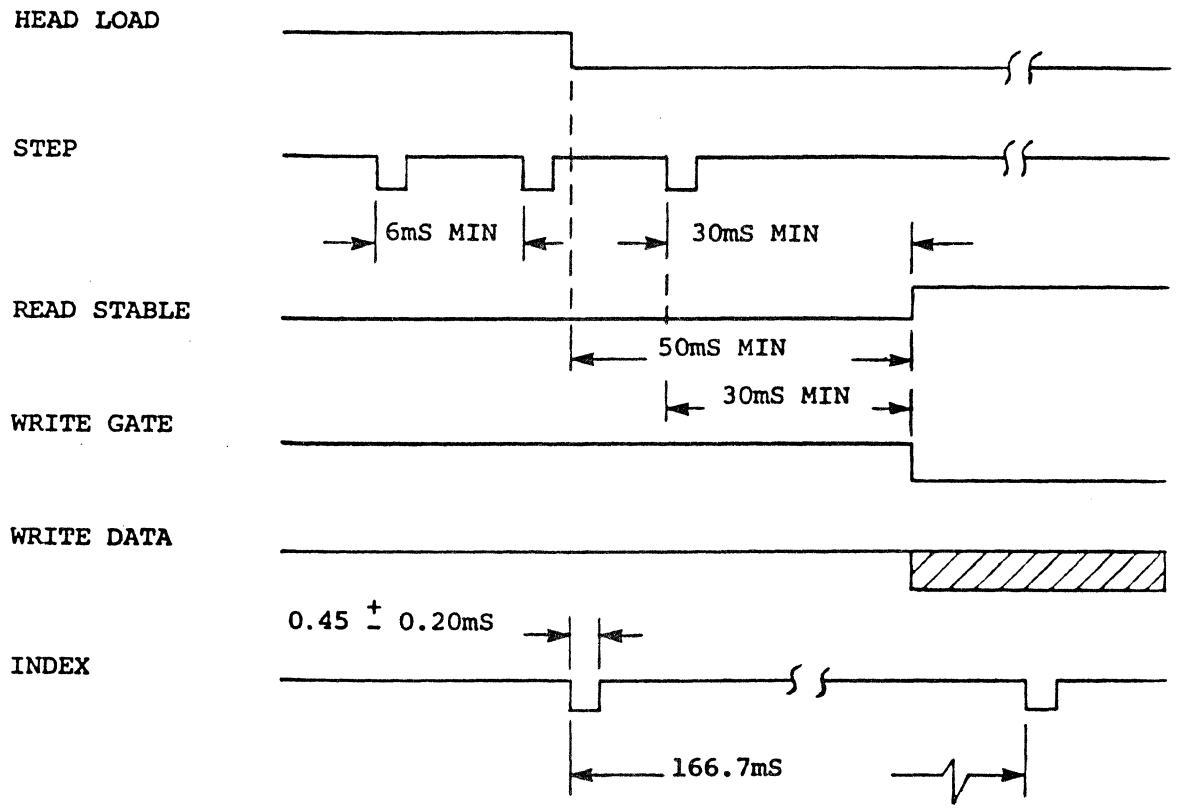
6.) Write Data

This interface line provides the data to be written on the disk. Each transition to a low active level on this line causes write current through the write coils to be reversed. A 200ns wide pulse



POWER UP SEQUENCE

FIGURE #4-10



READ/WRITE SEQUENCE

FIGURE #4-11

is required for each flux reversal to be written.

7.) Erase Gate

The Erase Gate input controls the DC current through the erase element to provide tunnel erase while writing on the disk. A low active level on this line turns on constant current to the erase head. (Refer to Figure #4-12 for timing considerations.)

8.) Low Current

A low active level on this line is present when writing on tracks 48 through 76. This input is used to lower the write current which consequently improves the read output resolution of the inner tracks.

Output Lines

There are five output lines from the FDD: Index, Track 00, Present, Read Data and Ready. Each line has the following characteristics:

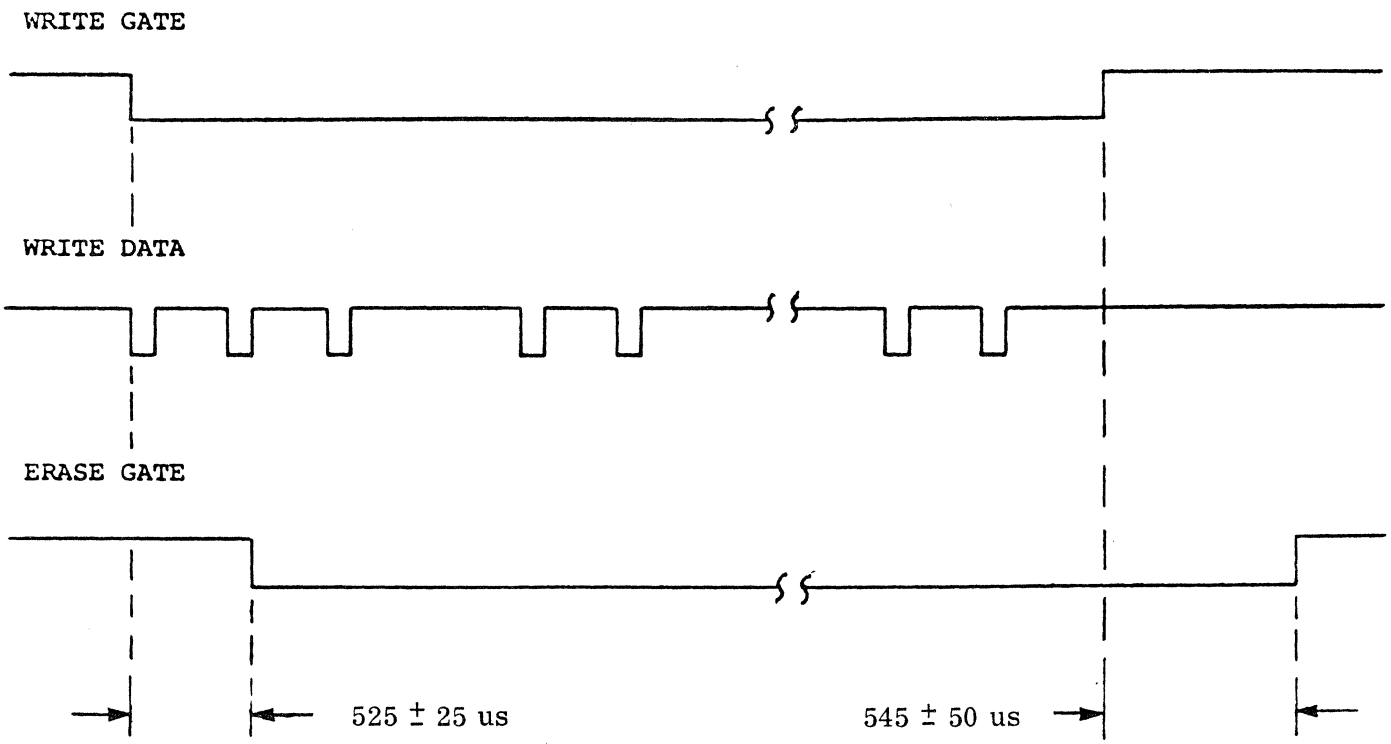
Active	0 to 0.4V
Inactive	4700 ohms to +5V
Maximum Sink	47 mA

1.) Index

This interface signal is provided by the disk drive once each revolution (166.7 ms) to indicate the beginning of the track. This signal makes a transition to a low active level for a period of 0.45 ± 0.20ms (refer to Figure #4-11).

2.) Track 00

A low active level is on this line when the read/write head is positioned at



ERASE GATE TIMING

FIGURE #4-12

track 00 or 01. The signal is valid 10 ms after the last Step command.

3.) Read Data

Data is output to the Comm-Stor FDC in the same form as write data from the FDC. Each flux reversal sensed on the storage element will result in a transition to a low active level for a 200 ns period on this line.

4.) Ready

A low active level on this line indicates that a diskette is loaded and rotating in the drive and that the front door is closed.

5.) Present

A low active level on this line indicates the selected drive is present.

Power Interface

See section 3F, page 4-12.

C. Modes of Operation

The FDD operates in five modes; they are:

1.	Power Up Mode	- Sequence after power up
2.	Seek Mode	- Position read/write head to desired track
3.	Write Mode	- Record data onto storage element
4.	Read Mode	- Retrieve data from storage element
5.	Power Down Mode	- Sequence as power goes down

1.) Power Up Mode (Refer to Figure #4-10)

Applying AC and DC power to the drive can be done in any sequence; however, once ac power has been applied, a two second delay must be completed before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. When dc power is applied, a 10 ms power on reset automatically resets the electronics and inhibits inadvertant writing or erasing on the Diskette. Thus, the drive is ready for operation two sec after application of AC power and 1200ms after application of DC power. Also, initial position of the R/W head with respect to data tracks is indeterminate immediately after application of DC power. In order to assure proper positioning of the R/W head prior to any read/write operation, a Step Out operation should be performed until the Track 00 signal becomes active.

2.) Seek Mode

The Seek Mode positions the read/write head to the desired track for recording or retrieving data. Seeking is accomplished by activating the interface IN line and pulsing the interface line Step once for each track to be traversed.

See Figures #4-10 and #4-11 for track seek timing. Seeking should not take place while writing. Application of a step pulse while write gate is active will cause the following sequence.

a. Deactivation of Write Circuitry
b. Step

Further, the drive will not step further out than Track 00. (The head is automatically unloaded when the door is opened and will not load unless a diskette is present, the door is closed, and the media is rotating.)

3.) Write Mode

The Write Mode records data on the storage element in the form of flux reversals.

4.) Read Mode

The Read Mode retrieves data previously recorded on the storage element.

This is accomplished by the read winding sensing flux reversals on the Diskette. The Read Mode is entered if a Diskette is present and the door is closed by simply activating the interface line Load Head with the Write Gate line at the inactive state. Certain timing relationships are required to assure that the read/write head has stabilized. These timing relationships are defined by Figure #4-11.

5.) Power Down Mode

During dc Power Down, when +5V drops under +3.5V, all write circuitry is deactivated to prevent an inadvertant writing or erasing on the diskette.

5. TYPICAL PARTS LIST

This section contains a typical parts list for the FD 700. Changes to the drive will be made from time to time to improve reliability or to simplify assembly or disassembly. The parts list is intended to be typical of a large number of drives, but not necessarily all. When ordering parts for a specific drive be sure to include the full serial number (eg. 12D0-0150).

The parts list consists of the basic assembly (less PWB and top cover) and its constituent subassemblies. The basic assembly drawing is shown as Figure #4-17.

6. DISKETTE

The Diskette consists of a ferromagnetic coated flexible disk enclosed within a protective plastic jacket. The interior of the jacket is lined with a wiping material to clean the disk of contaminent matter. The diskette should be handled with care at all times. When not in use, the diskette should be retained in a protective storage envelope and stored in a vertical position.

NOTE: Do not load diskette with the power off.

A. Diskette Loading and Unloading

1.) Apply power to the unit.

2.) Carefully remove diskette from the storage envelope and insert into the open mouth of the drive. The index hole should be nearest the operator and the diskette label toward the door. See Figure #4-15.

3.) Maintaining a slight pressure on the diskette to hold it in position, close the door to engage spindle and start diskette rotation. The door will not close if the diskette has not been fully inserted.

4.) To unload, open the door and the diskette will partially push out of the drive in a position convenient for retrieval.

7. SELECTING THE DRIVE NUMBER (DUAL DRIVE UNIT)

The Sykes Drive Control board is shipped with a connector-shunt across pins 2 and 12 of connector J6 on the lower drive (see Figure #4-13). No connector is necessary on drive 1.

NOTE: The connector-shunt is removed by pulling it straight up and off the pins; it is replaced by reversing the procedure.

Terminator Installation

Each Drive Control board is shipped with a 220/300 Terminator at location U18. In dual drive systems, this terminator should reside in the drive which is physically at the end of the cable.

DRIVE ADAPTER

Drive Number	Shunt J6-12 to J6-2
1	No
2	Yes

FIGURE #4-13

PIN ARRANGEMENT OF CONNECTOR J6

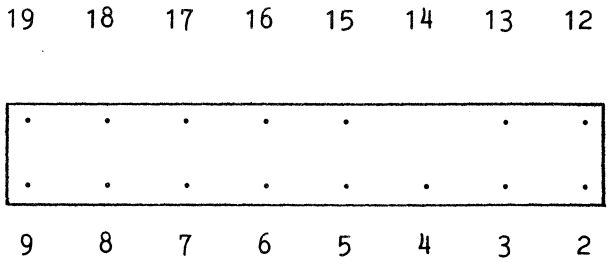
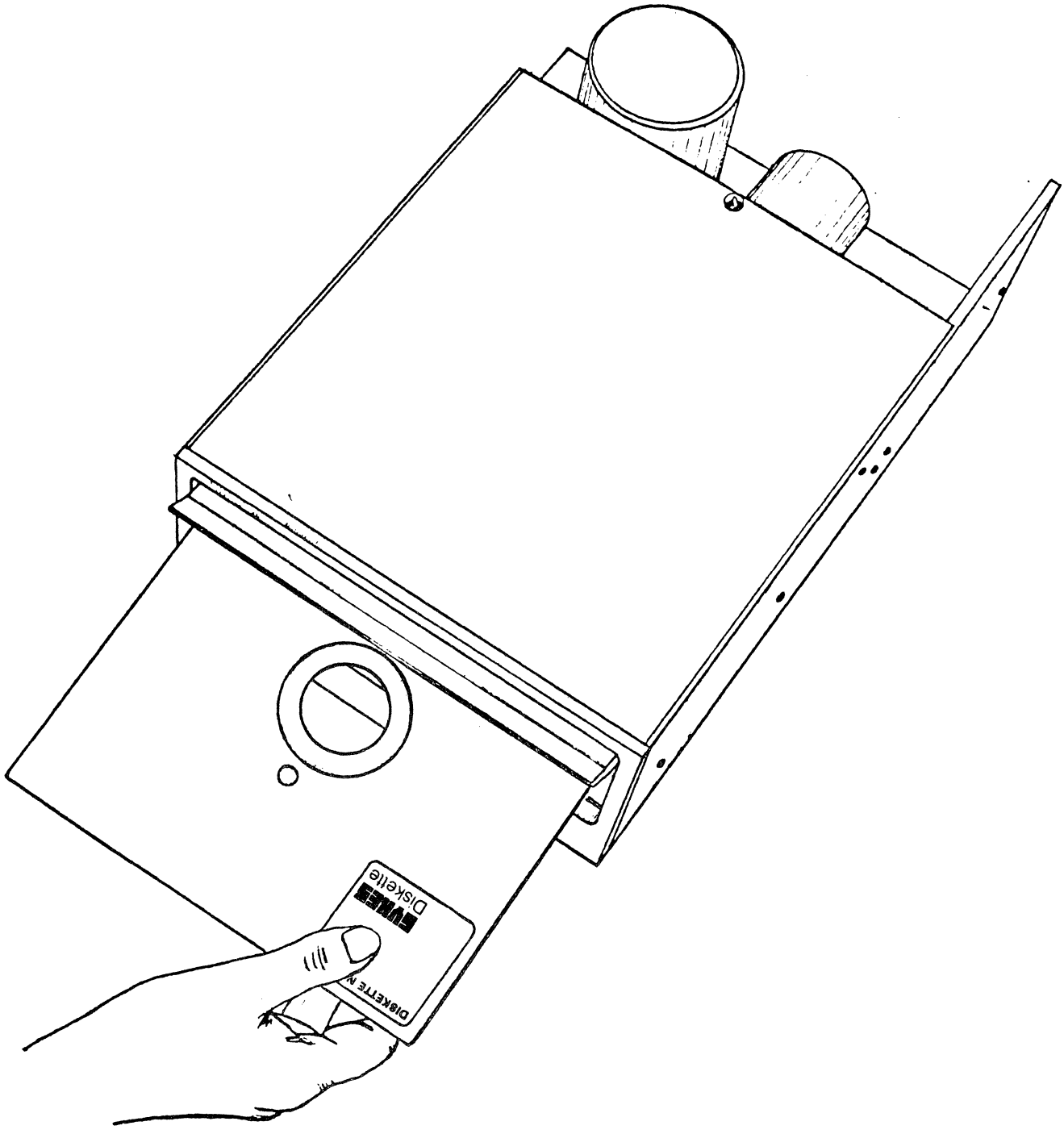


FIGURE #4-14

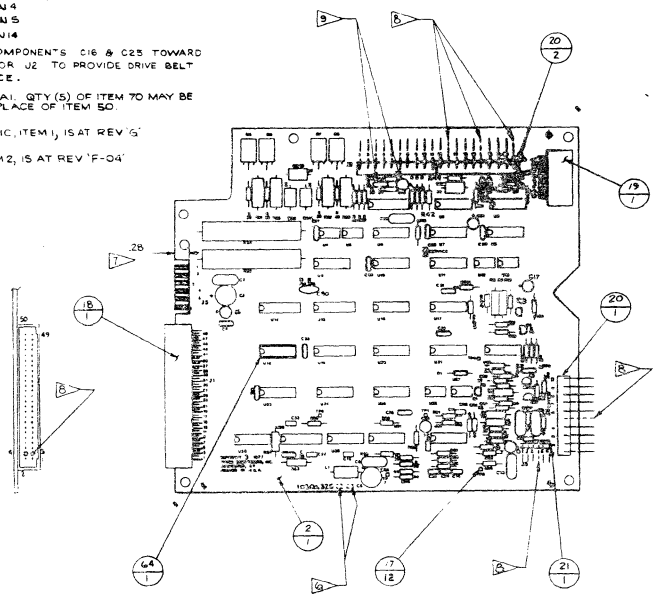


DISKETTE LOADING

FIGURE #4-15

NOTES:

1.
2.
3. REFER TO ENG. STD. ES102-02
4. SOLDER PER ES102-03
5. COMPONENT HEIGHT NOT TO EXCEED .70
6. LAST DIGIT OF ASSY NO. & REVISION LETTER PER ES102-02
7. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
8. REMOVE THE FOLLOWING CONN. PINS AS INDICATED:
   - J1 - PINS 3 & 4
   - J2 - PINS 13, 17 & 21
   - J3 - PIN 4
   - J4 - PIN 5
   - J6 - PIN 14
9. DRESS COMPONENTS C16 & C25 TOWARD CONNECTOR J2 TO PROVIDE DRIVE BELT CLEARANCE.
10. ADDITIONAL QTY (5) OF ITEM 70 MAY BE USED INPLACE OF ITEM 50.
11. SCHEMATIC, ITEM 1, IS AT REV 'G'
12. PWB, ITEM 2, IS AT REV 'F-04'



DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY
	74			
	73			
	72			
	71			
U27	70	100U16073	INT. CKT - 75462	1
C40	69	120C01006I	CAP, DISC, G.P., .001UF	1
C37	68	120C03040	CAP, DISC, L.V., .04UF, 50V	1
R18,20,58	67	100R02144	RES. C.C., 1/4W, 5%, 910K	3
R51	66	100R02131	RES CC 1/4 W, 5% 270K	1
R1,66,62	65	100R02113	RES CC 1/4 W 5% - 47K	3
XU18	64	10HU6002	SOCKET - 14 PIN DIP	1
U6,7	63	100U19056	INT. CKT. - 74LS73	2
U14	62	19018	74LS153	1
U30	61	19013	74LS86	1
U17,28	60	19011	74LS74	2
U11	59	19009	74LS20	1
U16	58	19007	74LS08	1
U9,20	57	19006	74LS04	2
U25	56	100U19005	INT. CKT - 74LS02	1
U10,21	55	100U19004	INT. CKT - 74LS00	2
U15	54	19001	74LS191	1
U19	53	18018	8837	1
U31	52	18012	LM319	1
U2,3,8	51	17005	556	3
U4,5,12,13,26	50	16068	3612	5
U22-24	49	16040	7438	3
U1,29	48	16027	74123	2
U32	47	100U14006	INT. CKT - 739	1
U18	46	103R03003	220/330 TERM DIP	1
R33,34	45	102R07005	RES-W.W, 10W, 10%, 10Ω	2
R2	44	101R01220	RES-M.F, 1/4W, 1%, 2.00K	1
R3	43	310	17.4K	1
R53,54	42	296	12.4K	2
R16,17	41	254	4.53K	2
R9	40	101R01169	RES-M.F., 1/4W, 1%, 562Ω	1
R31,35,37,39	39	100R04057	RES-C.C., 1W, 5%, 220Ω	4
R66	38	100R02073	RES-C.C., 1/4W, 5%, 10K	1
R23	37	100R02121	RES-C.C., 1/4W 5%, 100K	1
R50	36	105	22K	1
R30	35	101	15K	1
R8,9,24,26,41,43,45,46,61,64	34	097	10K	12
R29,56	33	089	4.7K	2
R4,5,11,15, 47,48,55,57	32	085	3.3K	8
R6,7	31	077	1.5K	2
R10,22	30	067	560Ω	2
R32,36,38,40	29	045	470Ω	4
R12-14,42	28	033	180Ω	4
R25,27,28,52,59	27	049	100Ω	5
R21, 44	26	100R02056	RES-C.C., 1/4W, 5%, 200Ω	2
Q1, Q9	25	202Q01001	TRANSISTOR MPS6531	2
Q5-8	24	201Q01003	ZN5193	4
Q2-4	23	201Q01001	TRANSISTOR MPS6534	3
L1	22	300X01001	INJUCTOR 10UH	1
J3	21	100J11813	6 PIN, R.A. WAFER	1
J2(2) J4(1)	20	100J11812	10 PIN, R.A. WAFER	3
J6	19	100J02015	16 POS. RT ANGLE HDR	1
J1	18	100 J02013	50 POS. RT ANGLE HDR	1
TP1-9,21, SERVICE	17	103E02002	POST MOD II	12
CR1,9-11	16	200C02001	DIODE - IN2070	4
CR1-8, 8.13-15	15	200C01001	DIODE - IN4153	10
C2,6,8,9,13	14	130C03025	CAP. MET. POLY, .01UF, 250V	5
C30	13	130C00225	MET. POLY, .068UF, 250V	1
C32	12	120C06017	DISC, NPO, 220PF, 100V	1
C12,15	11	120C06015	NPO, 150PF, 100V	2
C35,2436	10	120C06003	NPO, 22PF, 100V	3
C4,18,19,25-36	9	120C03010	L.V., .05UF, 10V	15
C11,14	8	120C06025	NPO, .001UF, 100V	2
C7	7	120C06009	DISC, NPO, 47PF, 100V	1
C21	6	105C04062	TANT, 10UF, 50V	1
C3,10,17	5	105C04105	TANT, 2.2UF, 15V	3
C1,5	4	105C04103	TANT, 22UF, 35V	2
C16,39	3	105C04077	CAP, TANT, 4.7UF, 50V	2
	2	103B3259	PWB-DRIVE CONTROL	1
	1	103D3259	SCHEMATIC - DRIVE CONTROL	REF
DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASSY
SYKES DRIVE CONT.

DWG SIZE	DWG NO.	REV
D	1030A3251	J
	SHEET 1 OF 1	

FIGURE #4-16

DRIVE CONFIGURATION			VARIABLE PARTS & SUB-ASSEMBLIES							CONFIG CONTROL	
POWER CONFIG	MOTOR TYPE	DOOR COLOR	PULLEY, SQ60HZ 1030T3210	DRIVE MOTOR ASSY	DOOR 1030T3240	230 VAC OPTION KIT				CONTROL NUMBER	REV
700, 115VAC, 60HZ	INDUCTION	LT. TAN	1030B3217	1030A3184	1030A3242					1030C3001	B
115VAC, 50HZ			18							3002	B
230VAC, 60HZ			17			1030A3262				3003	B
230VAC, 50HZ			18			1030A3262				3004	B
115VAC, 60HZ		BLACK	17		1030A3241					3005	B
115VAC, 50HZ			18							3006	B
230VAC, 60HZ			17			1030A3262				3007	B
230VAC, 50HZ			18			1030A3262				3008	B
115VAC, 60HZ	SYNC	LT. TAN	15	1030A3185	1030A3242					3009	B
700, 115VAC, 50HZ	SYNC	LT. TAN	1030B3214	1030A3185	1030A3242					1030C3010	B
700, 230VAC, 60HZ	SYNC	LT. TAN	1030B3213	1030A3185	1030A3242	1030A3262				1030C3011	A
700, 230VAC, 50HZ	SYNC	LT. TAN	1030B3214	1030A3185	1030A3242	1030A3262				1030C3012	A
700, 115 VAC, 60HZ	SYNC	BLACK	1030B3213	1030A3185	1030A3241					1030C3013	A
700, 115 VAC, 50 HZ	SYNC	BLACK	1030B3214	1030A3185	1030A3241					1030C3014	A

NOTES:

1. 1030C3000 IS A REFERENCE CONTROL DOCUMENT COVERING VARIOUS FD700 CONFIGURATIONS. TO IDENTIFY A SPECIFIC CONFIGURATION SEE TABULATION CHART FOR APPROPRIATE SYKES CONTROL NUMBER.
2. ADJUST ITEM 17 TO PROVIDE NOTED CLEARANCE BETWEEN DISKETTE GUIDE RAILS & CARRIER WHEN FRONT DOOR IS FULLY CLOSED.
3. ADJUST DISKETTE LOAD PAD TO NOTED DIMENSION WITH POWER ON CLAPPER RELAY & FRONT DOOR CLOSED. CHECK AT TRACKS 69 & 96.
4. TORSION SPRINGS ITEMS 29 & 30 TO REST IN RECESSES ON FLOOR OF CASTING.
5. INSTALL TWO(2) SET SCREWS (ITEM 44) INTO PULLEY (ITEM 13) WHICH IS TO BE FLUSH WITH END OF SHAFT.
6. SHIM BETWEEN DRIVE MOTOR & FRAME TO MAKE BELT TRACK TRUE ON PULLEYS AS REQUIRED.
7. BEFORE INSTALLING STEPPER MOTOR THOROUGHLY CLEAN BORE IN CASTING AND APPLY SMALL AMOUNT OF GREASE ITEM 55 TO ENTIRE INSIDE SURFACE OF BORE. REMOVE EXCESS GREASE AFTER INSTALLATION.
8. INSURE THAT MOUNTING SCREW DOES NOT PROTRUDE THRU & TOUCH SHAFT.
9. APPLY SHIMS (ITEM 34 & 35) AS REQUIRED TO OBTAIN SET UP DIMENSION FROM C-PLANE (2 PLACES).
10. APPLY WASHERS (ITEMS 51 & 52) AS REQUIRED TO CENTER CARRIER & DOOR TO FRAME (LEFT TO RIGHT).
11. WHEN MOUNTING SYNC MOTOR DISREGARD ITEMS 53, 54 & 72. USE ADDITIONAL QTY'S OF ITEMS 38, 49, 58 AND SPECIFIED QTY OF ITEM 74 (SEE SHEET 2).

ITEM	PART NUMBER	DESCRIPTION	QTY
75	100H11604	SCREW, THREAD FORM 6-32 x 1/4	1
74	1020B4060	WASHER-.400x.191	3
73	500H10801	NUT, HEX #8-32	2
72	200H02101	LOCKWASHER, SPLIT #10	3
71	1030B3271	PAD, DOOR STOP	2
70	200M00012	OIL, LUBRICATING	A/R
69		KIT, 230 VAC OPTION	1
68	1030B3234	BEARING, CARRIAGE	1
67	300C07043	LABEL SERIAL NO.	1
66	800S04001	SPRING COMP	1
65	500H60004	RETAINING RING .125"	2
64	500H10151	NUT HEX 10-32	3
63	200W05104	TIE BASE	2
62	200W01001	CABLE TIE	6
61	200M00305	LOCTITE 290 - CARRIER	A/R
60	200M00302	LOCTITE 242 - PULLEY	A/R
59	200M00015	LUB MAG G	A/R
58	200M00306	LOCTITE-601	A/R
57	800H33008	PIN GROVED	1
56	200H10801	WASHER FLAT CS #8	2
55	200H10601	WASHER FLAT CS #6	4
54	200H10401	WASHER FLAT CS #4	5
53	200H10101	WASHER FLAT CS #10	3

ITEM	PART NUMBER	DESCRIPTION	QTY
52	200H05009	WASHER NYLON-.37x.19x.031	A/R
51	200H05008	WASHER NYLON-.37x.19x.015	A/R
50	200H05007	WASHER NYLON-.375x.156x.031	1
49	200H02801	LOCKWASHER SPLIT #8	2
48	200H02601	LOCKWASHER SPLIT #6	2
47	200H02401	LOCKWASHER SPLIT #4	5
46	100W02004	CLAMP CABLE	2
45	100W02003	CLIP CABLE	1
44	100H256D4	SCREW SET 6-32 X 1/4	4
43	100H15406	SCREW SOC HEAD 4-40 X 3/8	5
42	100H11805	SCREW THREAD FORM 8-32X 5/16	1
41	100H11608	SCREW THREAD FORM 6-32X 1/2	3
40	100H11606	SCREW THREAD FORM 6-32X3/8	7
39	100H05806	SCREW FH 8-32 X 3/8	2
38	100H01808	SCREW FH 8-32 X 1/2	2
37	100H01605	SCREW PH 6-32 X 5/16	2
36	100H01603	SCREW PH 6-32 X 3/16	2
35	100B03006	SHIM BEARING	A/R
34	100B03005	SHIM BEARING	A/R
33	100B03003	BEARING FLANGED	2
32	100A05001	TUBING 1/8"	2
31		PULLEY SQ60 HZ	1
30	1030B3200	SPRING TORS LH	1
29	1030B3199	SPRING TORS RH	1
28	1030B3198	SCR BUTTON HEAD	2
27	1030B3191	BELT DRIVE	1
26	1030B3190	CLAMP SYNC MTG	3
25	1030B3159	CLAMP SPLIT	1
24	1030B3158	BALL STYLUS	1
23	1030B3155	SCALE TRK POS	1
22	1030B3154	ROLLER DOOR	2
21	1030B3150	FRAME MAIN FD	1
20	1030B3149	BRKT AC MTG	1
19	1030B3147	PIN PIVOT	1
18	1030B3146	ROD GUIDE	1
17	1030B3145	GUIDE DOOR L & R	2
16	1030B3141	RETAINER PAD	1
15	1030B3140	PAD LUBE	1
14	1030B3139	SPRING STYLUS	1
13	1030B3138	PULLEY DRIVE	1
12	1030B3136	HUB DRIVE	1
11			
10	1030B0258	DOOR STOP	2
9		ASSY DRIVE MOTOR	1
8	1030A3181	DISC CARRIER ASSY	1
7		DOOR	1
6	1030A3157	SW BRKT ASSY FD	1
5	1030A3148	MOTOR STEPPER	1
4	1030A3281	CARRIAGE ASSY FD	1
3	1030A3105	INDEX SENSOR	1
2	1030A3104	SIGNAL HARNESS FD	1
1	1030A3251	PWB ASSY, SYKES DRIVE CONTROL	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: CONFIGURATION CONTROL FD 700 DISK DRIVE

DWG SIZE: D | DWG NO.: 1030C3000 | REV: E | SHEET 1 OF 3

FIGURE #4-17(A)

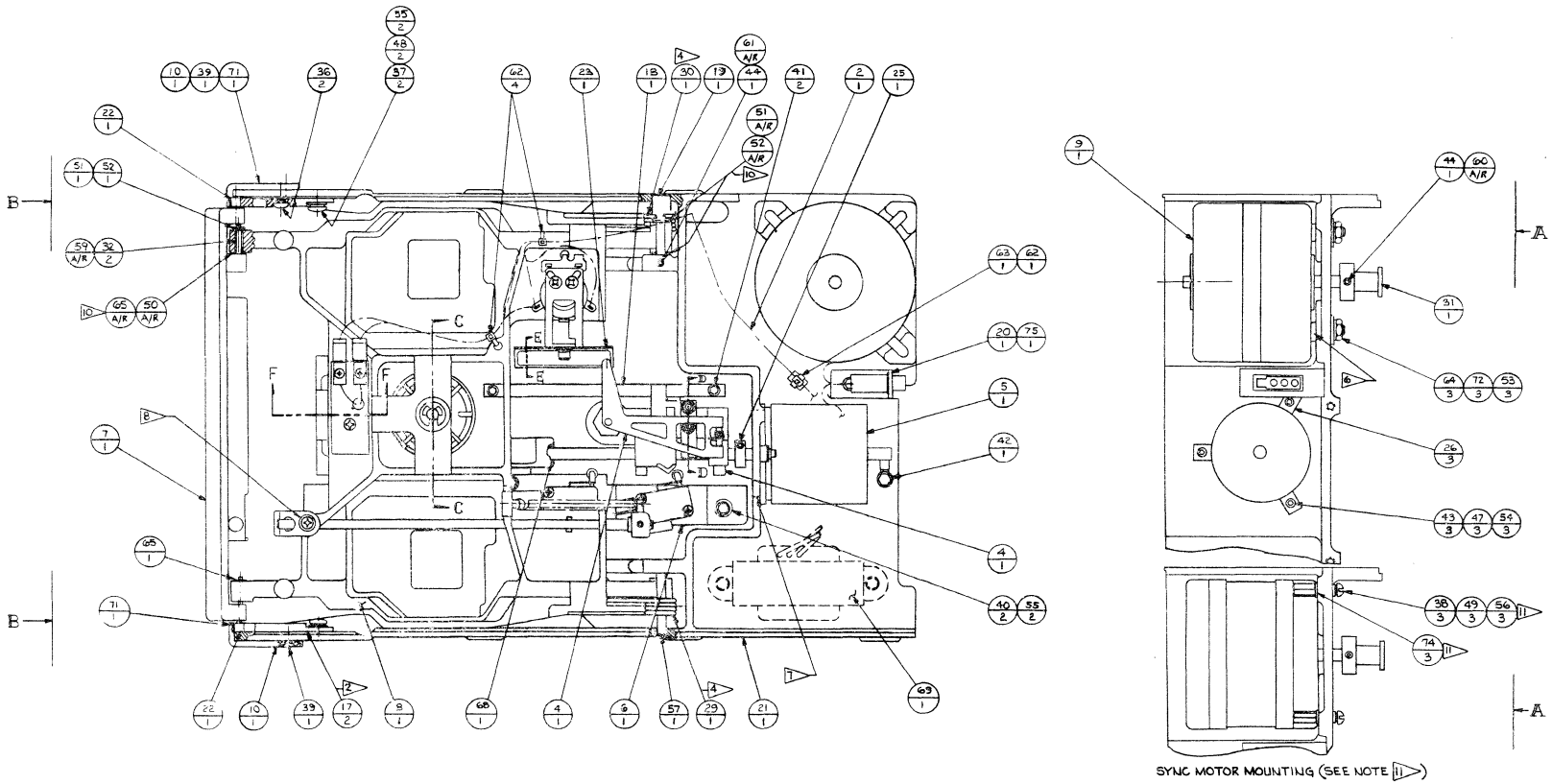

SYNC MOTOR MOUNTING (SEE NOTE 11)
DATATRONICS, INC.
ROCHESTER, NEW YORK
CONFIGURATION CONTROL
FD 700
DISK DRIVE
D
1030C3000
SHEET 2 OF 3

FIGURE #4-17(B)

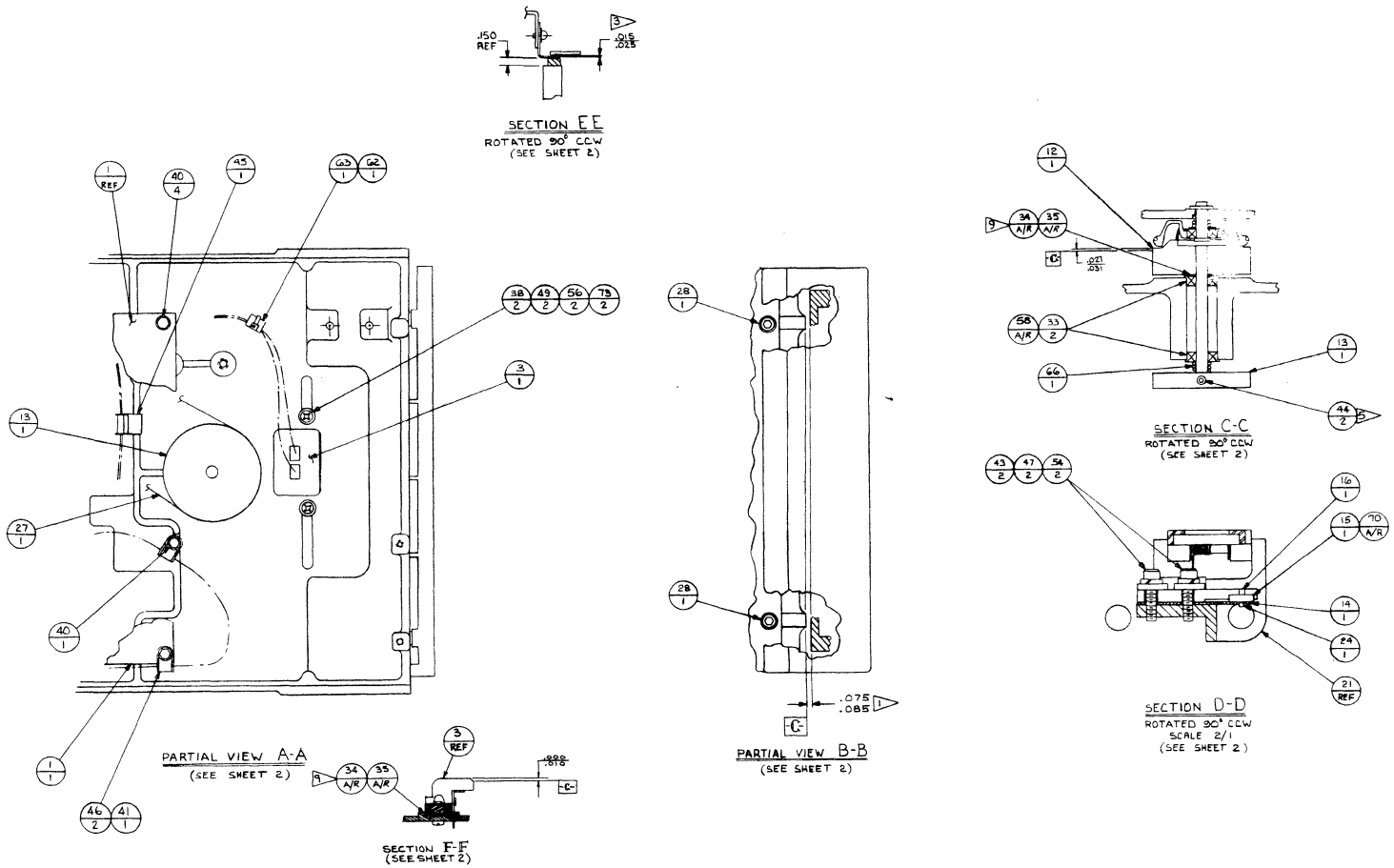

SECTION EE
ROTATED 90° CCW
(SEE SHEET 2)
PARTIAL VIEW A-A
(SEE SHEET 2)
PARTIAL VIEW B-B
(SEE SHEET 2)
SECTION C-C
ROTATED 90° CCW
(SEE SHEET 2)
SECTION D-D
ROTATED 90° CCW
SCALE 2/1
(SEE SHEET 2)
SECTION F-F
(SEE SHEET 2)
SYKES DATATRONICS, INC.
ROCHESTER, NEW YORK
CONFIGURATION CONTROL
FD 700
DISK DRIVE
D
1030C3000
SHEET 3 OF 3

FIGURE #4-17(C)

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CHAPTER 5

MULTIPLE VOLTAGE POWER SUPPLY ASSEMBLY

CONTENTS

1. GENERAL

Two multiple voltage power supply (MVPS) assemblies are discussed in this chapter, one employed in the Comm-Stor single drive unit and another used in dual drive Comm-Stor units.

Refer to Chapter 9 for voltage measurement and adjustment procedures.

Different jumper schemes at the power-in terminal strip allow the Series 8000 Comm-Stor unit to be operated on either 120 or 230 VAC. (Refer to page 5-3 for details.)

2. Comm-Stor SINGLE DRIVE UNIT POWER SUPPLY ASSEMBLY

A. General

The MVPS employed in the Comm-Stor single drive unit is Sykes part number 1030A6022. The MVPS components are mounted on a plate which is retained in the Comm-Stor unit by two philips head screws accessible from the underside of the unit. Drawing numbers 1030A6024 and 1050A0299 illustrate the MVPS assembly.

Refer to Chapter 11 for the schematic of the MVPS and the Power Distribution diagrams.

B. Electrical Inputs

1.) Input Power (PS1TB1, Pin 5)

Power input must be 120 ± 15 VAC or 230 ± 30 VAC, 50 or 60 ± 0.5 Hertz, single phase AC power, 120 watts during normal operation.

2.) AC Neutral (PS1TB1, Pin 4)

AC neutral connection terminal.

C. Electrical Outputs

1.) +5 VDC (PS1J2, Pin 1)
+5 vdc ± 1% at 0.25 to 5 amp, 25 mv p-p ripple, 50 mv p-p noise.

2.) +5 VDC Return (PS1J2, Pin 7)
Return for 5 vdc power.

3.) 12 VDC Return (PS1J2, Pin 9)
Return for +12 vdc and -12 vdc power.

4.) +12 VDC (PS1J2, Pin 10)
+12 vdc ± 0.5% at 0.04 to 0.4 amp, 10 mv p-p ripple, 10 mv p-p noise.

5.) -12 VDC (PS1J2, Pin 11)
-12 vdc ± 0.5% at 0.04 to 0.4 amp, 10 mv p-p ripple, 10 mv p-p noise.

6.) 24 VDC Return (PS1J2, Pin 5)
Return for +24 vdc power.

7.) +24 VDC (PS1J2, Pin 2)
+24 vdc ± 5% at 0.2 to 1.3 amp, 500 mv p-p ripple, 50 mv p-p noise.

8.) Chassis Ground (PS1J2, Pin 8)
The chassis ground connection pin.

9.) 115 VAC Out (PS1TB1, Pin 2)
The 115 volts ac power out connection pin (maximum of 0.5 amperes at 115 vac supplied from tap or primary side of MVPS transformer.

D. **Removal/Replacement**

1.) Disconnect Comm-Stor from the power source.

2.) Remove the top cover from the unit (page 3-1).

3.) Disconnect the following six wires from the terminal block:

2 - red
3 - gray
1 - black

4.) Disconnect P1 from PS1J2 on the MVPS.

5.) Remove the two MVPS mounting screws accessible from the underside of the chassis.

6.) Very carefully lift the MVPS out of the chassis.

7.) Replace in reverse order.

3. Comm-Stor DUAL DRIVE UNIT POWER SUPPLY ASSEMBLY

A. **General**

The MVPS used in the Comm-Stor dual drive unit is Sykes part number 1050A0290. The MVPS components are assembled on a plate which is fastened to the chassis by three nuts and washers. Drawing Figure numbers 1050A0296 and 1050A0299 illustrate the MVPS assembly.

Refer to Chapter 11 for the schematic of the MVPS and the Power Distribution diagrams.

B. **Electrical Inputs**

1.) Input Power (PS1TB1, Pin 5)
Power input (which must be in keeping with Comm-Stor System configuration) may be 120 ± 15 VAC or 230 ± 30 VAC, 50 or 60 ± 0.5 Hertz, single phase AC power, 170 watts during normal operation.

2.) AC Neutral (PS1TB1, Pin 4)
AC neutral connection terminal.

C. **Electrical Outputs**

1.) +5 VDC (PS1J1, Pin 1)
+5 vdc ± 1% at 0.3 to 6.0 amp, 25 mv p-p ripple, 50 mv p-p noise.

2.) +5 VDC Return (PS1J1, Pin 5)
Return for 5 vdc power.

3.) 12 VDC Return (PS1J1, Pin 9)
Return for +12 vdc and -12 vdc power.

4.) +12 VDC (PS1J1, Pin 11)
+12 vdc ± .5% at .04 to .4 amp, 10 mv p-p ripple, 10 mv p-p noise.

5.) -12 VDC (PS1J1, Pin 15)
-12 vdc ± .5% at .04 to .650 amp, 10 mv p-p ripple, 10 mv noise.

6.) 24 VDC Return (PS1J1, Pin 21)
Return for +24 vdc power.

7.) +24 VDC (PS1J1, Pin 24)
+24 vdc ± 5% at 0.2 to 2.5 amp, 500 mv p-p ripple, 50 mv p-p noise.

8.) AC Neutral (PS1J1, Pin 33)
The ac neutral connection pin.

9.) 115 VAC Out (PS1J1, Pin 36)
The 115 volts ac power out connection pin (maximum of 0.8 amperes at 115 vac supplied from tap on primary side of MVPS transformer).

D. **Removal/Replacement**

1.) Disconnect Comm-Stor from the power source.

2.) Remove the top cover from the unit (page 3-1).

3.) Remove both the upper and lower drives (page 4-1).

4.) Unscrew the following eight wires from the terminal block:

3 - red
4 - gray
1 - black

5.) Disconnect P1 from PS1J1 on the MVPS.

6.) Remove the three nuts and washers which hold the power supply in place.

7.) Very carefully lift the MVPS out of the chassis.

8.) Replace in reverse order. Be careful not to pinch the AC wires for the fan motor located behind the supply.

4. MVPS POWER INPUT CONNECTIONS - 120 VAC OR 230 VAC INPUT

The Series 8000 Comm-Stor can be purchased to operate with a 120 vac or a 230 vac power source.

Refer to Reference Diagrams 1030B6008 sheets 2 and 3 found in Chapter 11 when attempting to convert the AC input voltage.

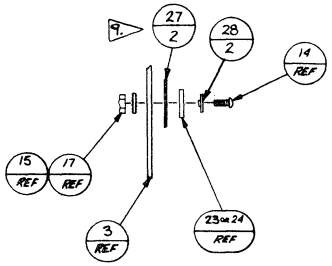
A. Arrangement for 120 VAC Operation

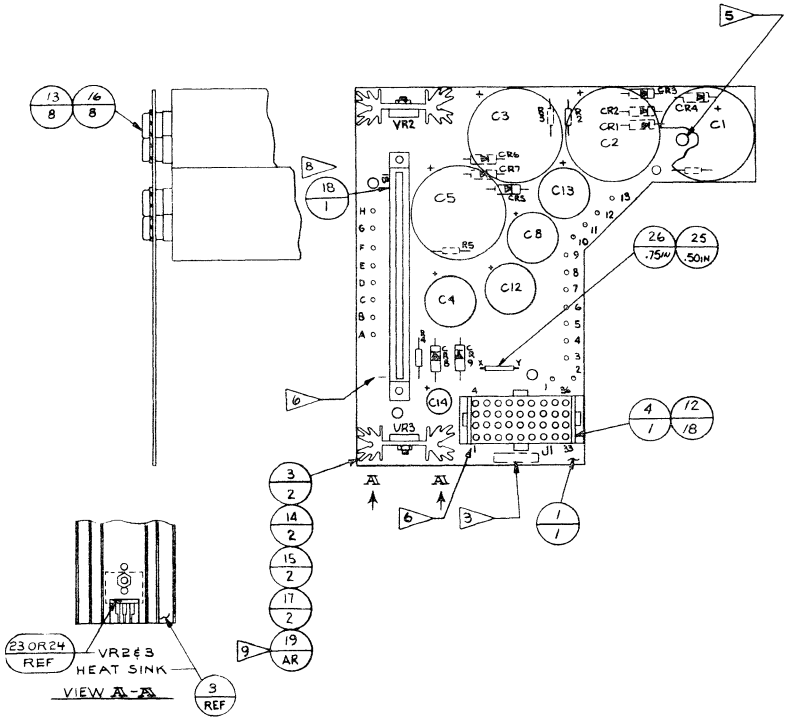
The power-in terminal strip (PS1TB1) on the MVPS has two jumper straps, one connecting terminals 1 and 2, and one connecting terminals 3 and 4. The red and gray power input wires are connected to terminals 1 and 4 respectively.

B. Arrangement for 230 VAC Operation

The power-in terminal strip (PS1TB1) on the MVPS has a jumper strap connected between terminals 2 and 3 and the red and gray power input wires are connected to terminals 1 and 4 respectively. (A suitable 3-wire grounding type plug for the power cable is required.)

NOTES:
1. REFER TO ENG STD ES102-02
2. SOLDER PER ES 102-03
3. REVISION LETTER AND ASSY NO. PER ES102-02
4. CAPACITORS C1-C3 & C5, ITEMS 13 & 16 TO BE ASSEMBLED TO ITEM 1 AFTER FLOW SOLDER
5. POLARITY INSPECTION HOLE
6. ORIENT. J1 & J2 WITH PIN 1 AS SHOWN
8. DUMMY PWB SHOULD BE INSERTED INTO ITEM 18 DURING FLOW SOLDER
9. USING ITEMS 27 & 28 MOUNT VR2 & VR3 AS SHOWN APPLYING ITEM 19 TO BOTH BACKSIDE OF VR2 & VR3 AND AREA AROUND MTG HOLE ON ITEM 3





		28	100A07018	BUSHING, INSULATING	2
		27	100A07017	WASHER, MICA	2
		26	600W05003	18 GA. SOLID WIRE	.75IN
		25	200W50018	18GA. TEFLON SLEEVE	.50IN
VR2		24	100U18015	VOLTAGE REG-MC7905CP	1
VR3		23	100U18014	VOLTAGE REG-MC7805CP	1
R1-3		22	100R02089	RES, 1/4W, 4.7K	3
R5		21	100R02073	" " 1.0K	1
R4		20	100R02095	RES, 1/4W, 8.2K	1
		19	200M00002	CONDUCTIVE COMP.	AR
J2		18	100J13006	CONN-MOD FORK 16 POS	1
		17	500H10401	#4-40 HEX NUT	1
		16	200H03001	#10L WASHER	2
		15	200H03040	#4 WASHER	8
		14	100H01404	#4-40 x 1/4 SCR	2
		13	100H01156	#10-32 x 3/8 SCR	2
		12	100J11554	CONTACT, SOCKET, SOLDER	18
CR1-4		11	200C02010	RECTIFIER-3A-100V	4
CR5-9		10	200C02002	RECTIFIER-1A-50V	5
C14		9	100C03143	CAP.-ELECT 100UF,25V	1
C5		8	101C01002	-CG-10,000-15000	1
C1-3		7	101C01001	-CG-2500-42.00UF	3
C8,12,13		6	100C03196	-ELECT-200-250UF	3
C4		5	100C03175	CAP.-ELECT-700-1000UF	1
J1		4	100J11525	CONNECTOR HSG, 36 POS	1
		3	101A00001	HEAT SINK	2
		2			
	D-02	1	1050B0294	PWB-BASE CARD	1
DESGN	REV	ITEM	PART#	DESCRIPTION	QTY

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

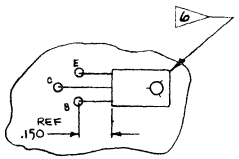
TITLE
PWB ASSY
POWER SUPPLY BASE CARD

DWG. SIZE: C | DWG. NO.: 1050A0296 | REV: C | SHEET 1 OF 1

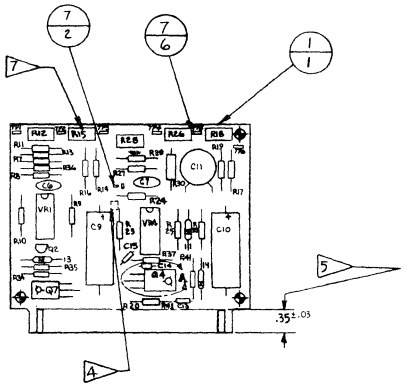
FIGURE #5-1

NOTES:

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .57
4. ASSY NO & REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION.
6. HEAT SINK ON ITEM 8 TO BE FACING DOWN
7. ORIENT POTENTIOMETERS, ITEMS 17, 18, 19 WITH ADJUSTMENT SLOT FACING AWAY FROM CONTACT FINGERS.
8. SEE SHEET 2 FOR REWORK INSTRUCTIONS ITEM 6 ADDED (C13, 14, & 15)



DETAIL A
Q4,7 MOUNTING
AVOID HEAT SINK CONTACT
WITH COMPONENT SIDE TRACES



	CR11	30	200C04205	ZENER - 1N4733, 5.1V, 5%	1
	CR14	29	200C01001	DIODE 1N4153	1
		28			
	R35,37	27	100R02097	RESISTOR 10K, 5%, 1/4W	2
	R34	26	100R02081	RESISTOR, 2.2K, 5%, 1/4W	1
	Q7	25	202Q01007	TSTR, PWR - 2N5191	1
	Q2	24	202Q01001	TSTR - 6531	1
	CR13	23	200C04087	ZENER - 1N5257B, 33V, 5%	1
	R30	22	100R03041	RESISTOR, 470Ω, 1/2W	1
		21	1050B0295	SCHEMATIC -	REF
	VR1,4	20	100U18016	VOLTAGE REG - 723	2
	R26	19	110R05012	POT - 3/8 SQ - 25K	1
	R15,18	18	110R05004	" - 3/8 SQ - 100Ω	2
	R12,28	17	110R05006	POT - 3/8 SQ - 500Ω	2
	R8	16	100R02101	RESISTOR, 15K, 1/4W	1
	R11,23	15	100R02085	" , 3.3K, 1/4W	2
	R10,13,29	14	100R02075	" , 1.2K, 1/4W	3
	R7	13	100R02080	" , 2.0K, 1/4W	1
	R24	12	100R02065	" , 470Ω, 1/4W	1
	R9,25,27	11	100R02061	" , 330Ω, 1/4W	3
	R14,16,17,19,33,41	10	100R02049	" , 100Ω, 1/4W	6
	R20,36	9	100R02053	RESISTOR, 150Ω, 1/4W	2
	Q4	8	202Q01003	TSTR - PWR - 2N5190	1
		7	103E02002	POST - MOD II .025 SQ	8
	C13,C14,C15	6	120C08015	CAP, DISC - 0.1 UF, 100 V	3
	C11	5	120C01086	CAP, DISC - .01UF	1
	C6,7	4	120C01068	CAP, DISC - .0018UF	2
		3			
	C9,10	2	100C01111	CAP, ELECT - 100 UF, 25 V	2
F-05		1	1050B0297	PWB - PWR SUP CONT	1
REV	DESGN	ITEM	PART NUMBER	DESCRIPTION	QTY

SYKES DATATRONICS INC ROCHESTER, NEW YORK

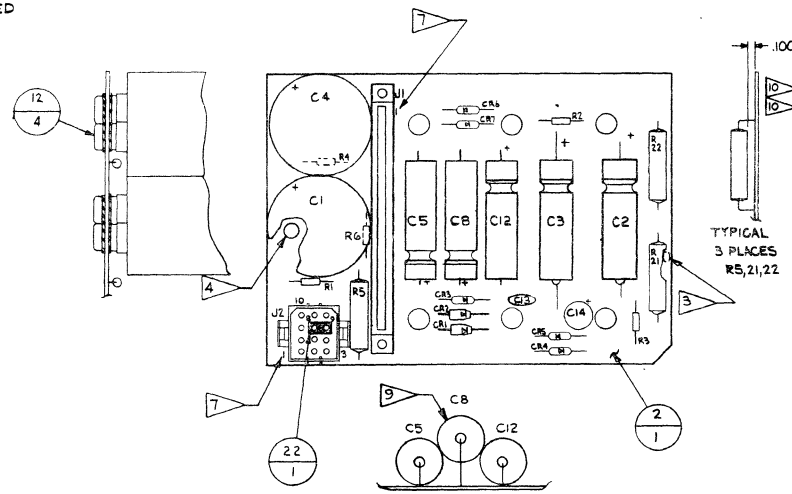
TITLE: PWB ASSY
POWER SUPPLY CONTROL

DWG SIZE: C
DWG. NO.: 1050A0299
SHEET 1 OF 2
G

FIGURE #5-2

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. REVISION LETTER PER ES102-02.
4. POLARITY INSPECTION HOLE
5. DUMMY PWB SHOULD BE INSERTED INTO ITEM 14 DURING FLOW SOLDER
6. CAPACITORS C1&C4, ITEMS 11 & 12 TO BE ASSEMBLED TO ITEM 1 AFTER FLOW SOLDER
7. ORIENT J1 & J2 WITH PIN 1 AS SHOWN
8. ALTERNATE PART
9. CAPACITORS MAY BE ASSEMBLED AS SHOWN WHEN USING ITEM 23
10. ITEMS 23 & 24 SUPPLIED WITHOUT EPOXY END SEALS AND MYLAR SLEEVE SHOULD NOT COME IN CONTACT WITH HALOGENATED CLEANING SOLVENTS.



DESIG	REV	ITEM	PART #	DESCRIPTION	QTY
C2,C3		24	102C01002	CAP, ELECT-500 UF, 35 V	2
C5,8,12		23	102C01001	CAP, ELECT-250 UF, 50V	3
		22	100J11555	COMMONING BAR-2 POS.	1
C13		21	120C03032	CAP, DISC, .033 µF	1
R6		20	100R02080	RESISTOR, ¼ W, 2.0K	1
R5		19	102R07004	RESISTOR, 5W, .5Ω	1
R21,R22		18	102R07003	,5W, .25Ω	2
R2,R3		17	100R02095	,¼W, 8.2K	2
R1		16	100R02089	,¼W, 4.7K	1
R4		15	100R02073	RESISTOR, ¼W, 1.0K	1
J1		14	100J13006	CONN, 18 POS. HDR	1
J2		13	100J11564	CONN, 12 POS. HDR	1
		12	200H03001	LOCKWASHER, #10	4
		11			
CR1,CR2		10	200C02010	RECTIFIER, 3A, 100 V	2
CR3-7		9	200C02002	RECTIFIER, 1A, 50V	5
		8			
C2,C3		7	102C01005	CAP-ELECT, 470 µF	2
C5,8,12		6	102C01004	,220 µF	3
C4		5	101C01002	,10,000 / 15,000 µF	1
C1		4	101C01004	,2400 µF	1
C14		3	100C03143	CAP-ELECT, 100 µF	1
	B-01	2	1030B6025	PWB-BASE CARD	1
		1			

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASSY 8100-BASE CARD

DWG. SIZE: C | DWG. NO.: 1030A6024 | REV: D | SHEET 1 OF 1

FIGURE #5-3

CHAPTER 6

SERIES 8000 CONTROLLER ASSEMBLIES

CONTENTS PAGE

1. DESCRIPTION OF CONTROLLER ASSEMBLIES

The controller assemblies for Comm-Stor, Comm-Stor II/III Systems consist of a base card and four logic boards residing in A1, A2, A3 and A5. Slot A4 is reserved for the Printer Port and/or Expanded RAM option. The controller assemblies for Comm-Stor IV consist of a base card and five logic boards residing in A1, A2, A3, A4, and A6. Slot A5 is reserved for the 24K RAM board.

Drawing number 1030A6043 shows the base board assembly and board slot assignments for the four logic boards and the optional fifth board for Comm-Stor and Comm-Stor II/III. Drawing number 1030A-5010 shows the base board assembly and board slot assignments for the five logic boards and the optional sixth board for Comm-Stor IV.

2. BASE BOARD ASSEMBLY

The base board (motherboard) assembly is a printed circuit card which utilizes five card connectors for Comm-Stor and Comm-Stor II/III, and six card connectors for Comm-Stor IV. Each card connector utilizes dual position connectors and is keyed to eliminate the possibility of inserting a card backwards.

The base board is wired to utilize a bus concept, meaning any board can be inserted into any connector for test purposes. However, because of physical clearances, it is recommended that the logic boards be inserted into their factory assigned slots.

A 4.5-volt alkaline battery and connector are also located on this card.

A. Circuit Boards

1.) Remove the top cover (page 3-1).
2.) Remove the two screws which fasten the circuit board retainer.
3.) Remove the circuit board retainer.
4.) All circuit boards can be removed from the base board assembly with the following exceptions:

1. MP-RAM - Removal of this board requires that the Interface Panel Assembly on the rear of the unit be removed to allow clearance for the baud rate switches as the MP-RAM board is removed from the base board.

2. Disconnect on-board connectors before removing Printer board, EIA board, or Disk Control board.

B. Battery

1.) Remove the top cover (page 3-1).
2.) Remove battery in the front left-hand side of the unit.
3.) Remove the tape and battery connecting clips.
4.) Carefully pop the battery out of its holder.
5.) Replace in reverse order.

C. Base Board Assembly

1.) Remove all circuit boards (see above).
2.) Remove the front panel assembly (page 3-1).
3.) Remove the battery (see above).
4.) Remove the nylon posts by removing corresponding screws on the bottom-side of the chassis.
5.) Remove the power supply connector located on the rear of the base board.
6.) Remove the screw and spacer located near the power supply connector.
7.) The base board can be slid forward until it has been removed from its track.
8.) Replace in reverse order.

3. MICROPROCESSOR AND RANDOM ACCESS MEMORY BOARD (MP-RAM)

Refer to Figure #6-1(A) for the block diagram of the MP-RAM board for Comm-Stor and Comm-Stor II/III. Refer to Figure #6-1(B) for Comm-Stor IV. Figures #6-8 and #6-14 illustrate the component layout for the boards. The schematics of the MP-RAM boards may be found in Chapter 11.

A. Microprocessor Control

Comm-Stor uses the MOS Technology 6502 microprocessor for all system control functions. The 6502 is an eight-bit microprocessor with a one-microsecond cycle time. Figure #6-2 shows the microprocessor's pin assignments. A crystal controlled one MHZ clock, phase 0, is provided to pin 37 of the microprocessor. The microprocessor generates a two-phase clock from this input. Figure #6-3 shows a typical processor cycle during which data is written to memory or hardware registers.

The microprocessor performs the following functions:

1. Locates tracks and sectors on the diskette.
2. Blocks data into logically sequential sectors.
3. Provides control signals needed by the remaining electronics.

Incoming and outgoing data are transferred by an 8-bit bi-directional Data Bus (D0-D7). All outgoing data on the 8-bit bi-directional Data Bus is strobed onto the Data Out Bus (DO0-DO7).

All incoming data to the processor is strobed onto the 8-bit bi-directional Data Bus from the Data In Bus (DB0-DB7).

Whenever data transfers occur, the microprocessor places a 16-bit address on the Address Bus (A0-A15). The address decoder circuits decode part of the address and provide an enable signal which allows data transfer to memory devices and system hardware registers (see Tables #6-1 to #6-3, page 6-7).

The bus structure allows the processor to transfer data directly to and from the EIA controller, the disk drive controller, and all other system devices by addressing them directly on the Address Bus and transferring out-going data on the DO Bus and transferring incoming data on the DB Bus.

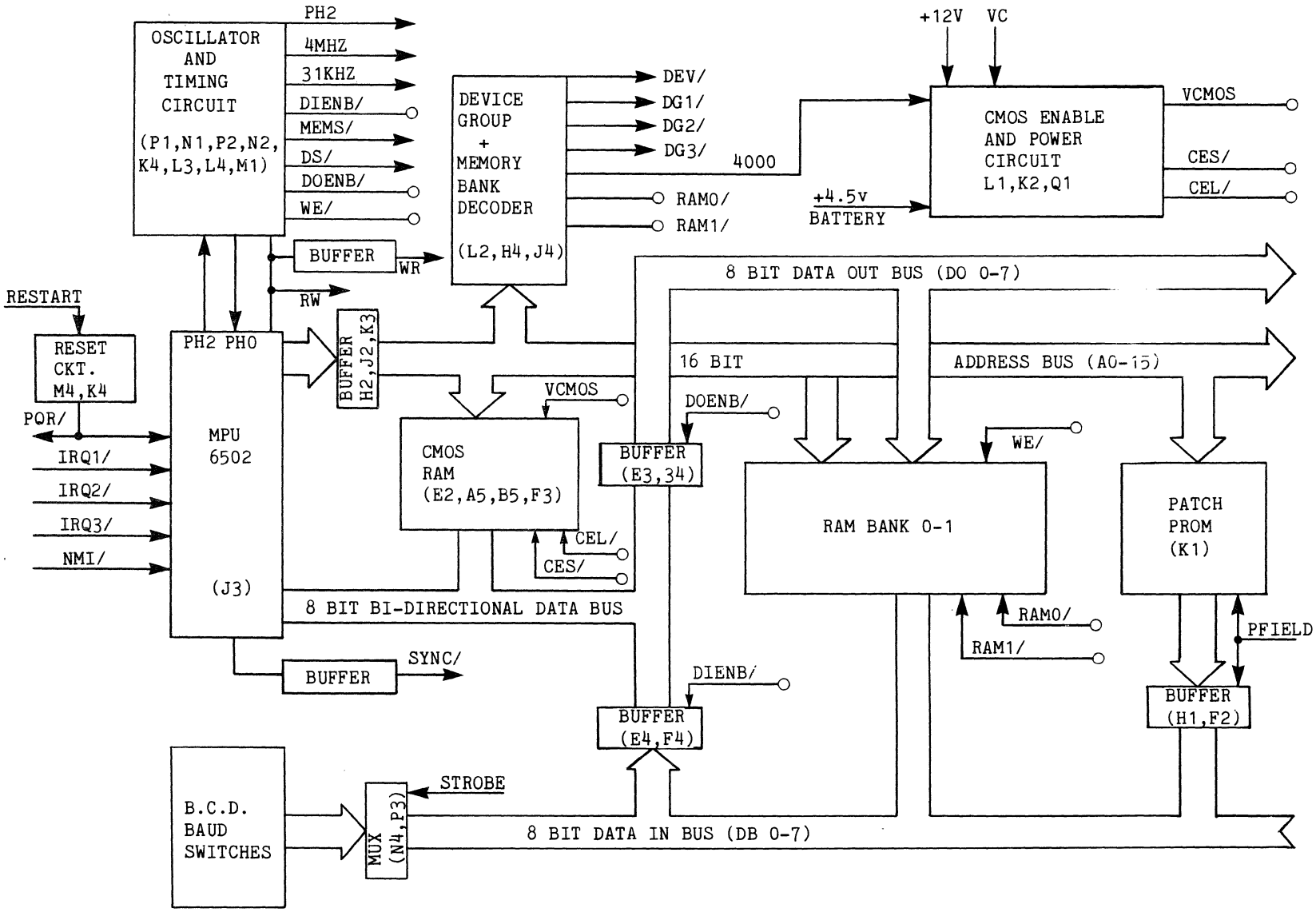


FIGURE #6-1(A) BLOCK DIAGRAM OF THE MP-RAM BOARD FOR Comm-Stor and Comm-Stor II/III

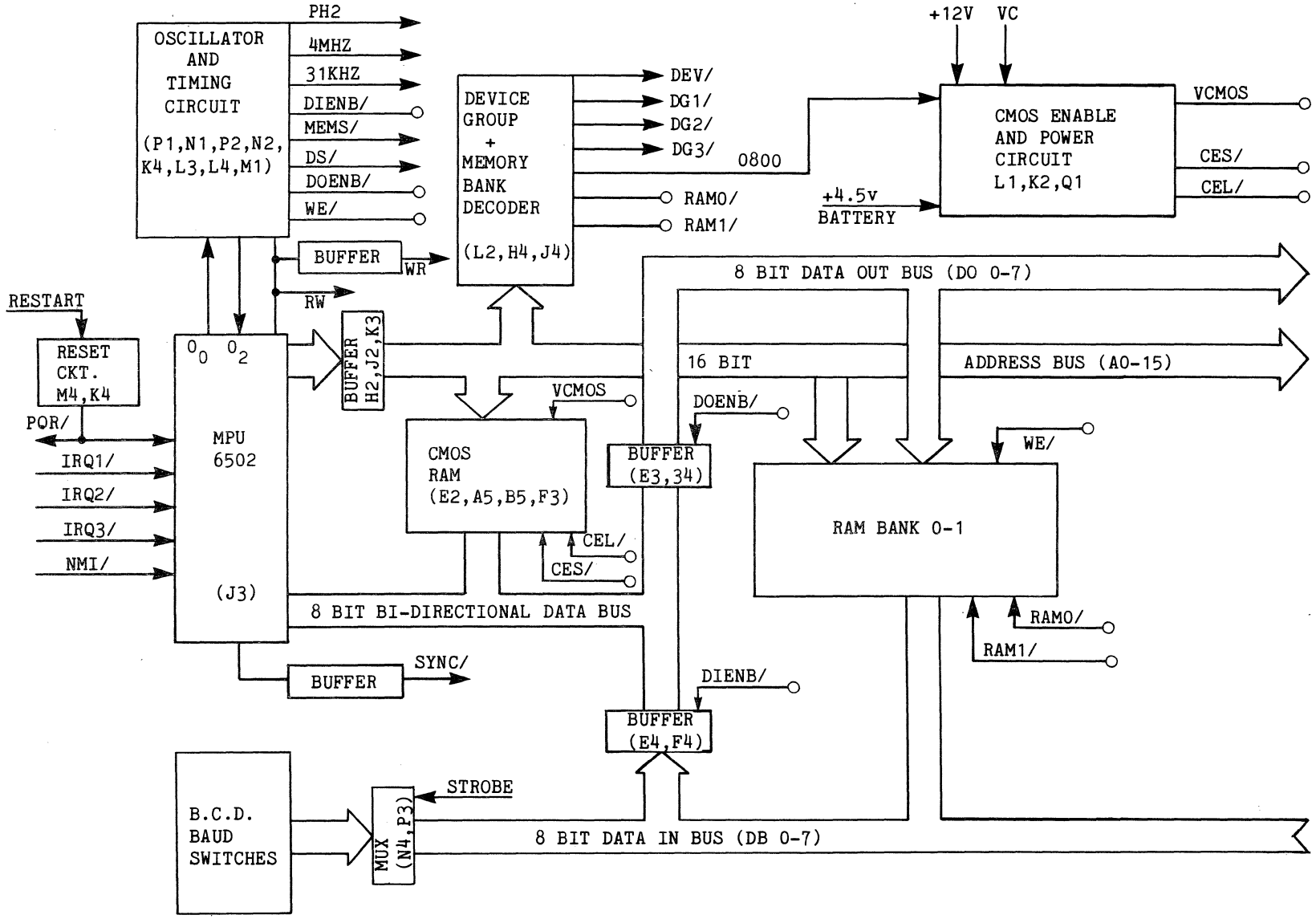
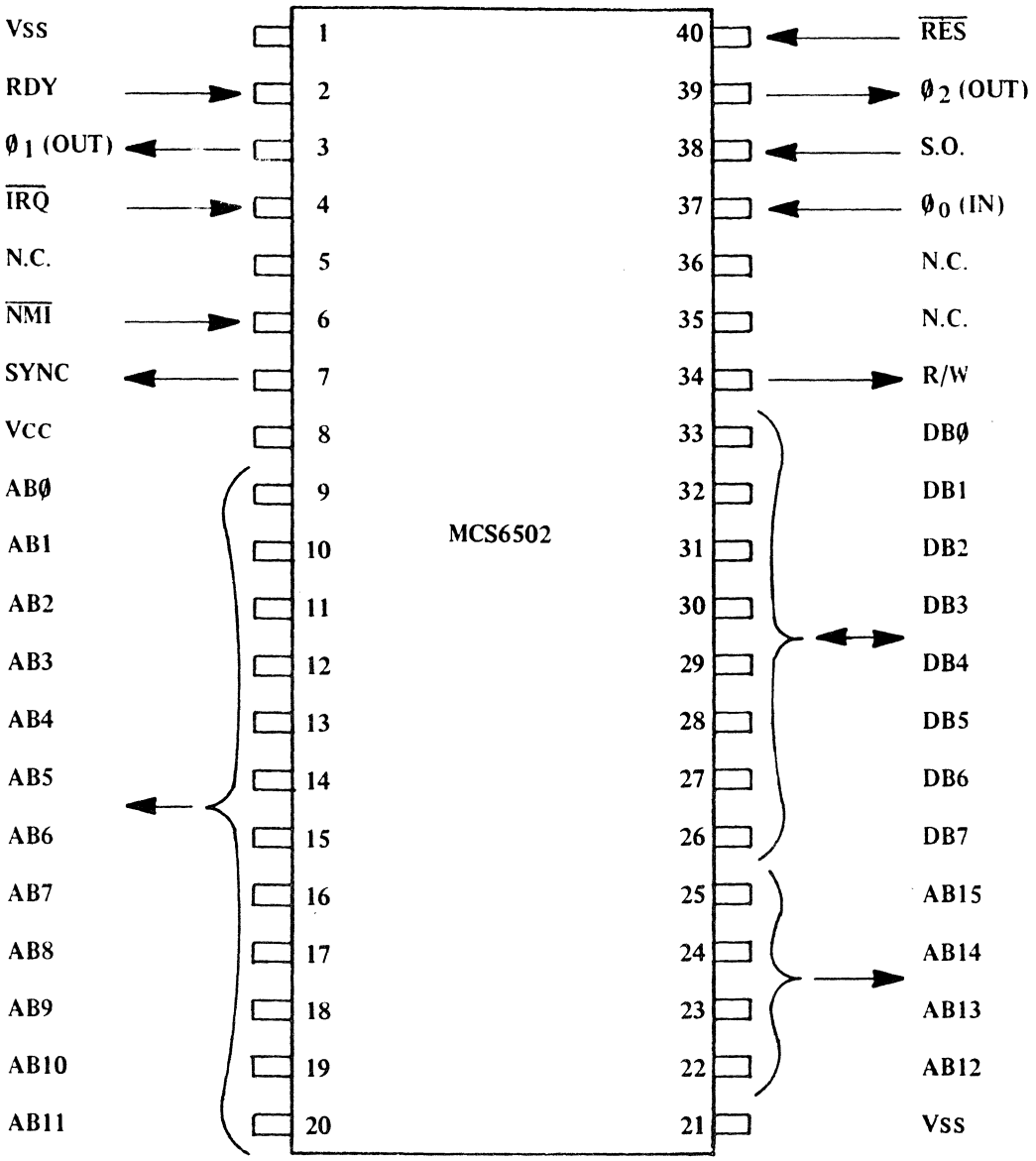


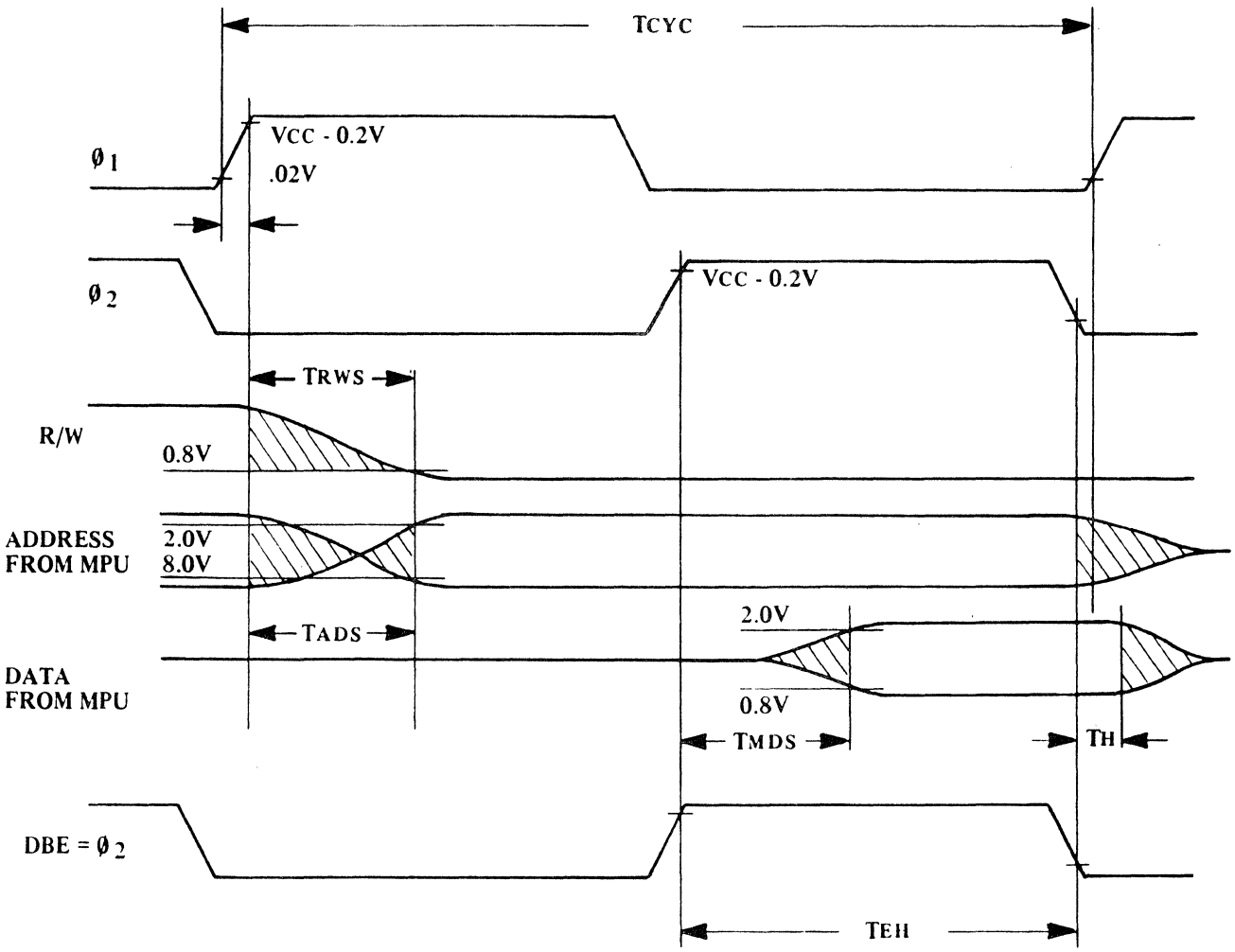
FIGURE #6-1(B) BLOCK DIAGRAM OF THE MP-RAM BOARD FOR Comm-Stor IV



N.C. = NO CONNECTION

MCS6502 PINOUT DESIGNATION

FIGURE #6-2



TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS

FIGURE #6-3

Comm-Stor MEMORY MAP

ADDRESS	FUNCTION	HARDWARE
FFFE-FFFF	IRQ and Break Vector	ROM
FFFC-FFFD	Power Up and Restart Vector	ROM
FFFA-FFFB	NMI Interrupt Vector	ROM
C000-FFF9	System Firmware	ROM
8800-8BFF	Expanded ROM (Patch)	PROM
8000-81FF	Software Patch PROM	PROM
4000-41FF	Configuration Storage	RAM
0400-17FF	Optional System Buffers	RAM
0200-03FF	I/O Buffers	RAM
01DA-01FF	Stack	RAM
0020-01D9	System RAM	RAM
0000-001F	Hardware Device	

TABLE #6-1

Comm-Stor II and III MEMORY MAP

ADDRESS	FUNCTION	HARDWARE
FFFE-FFFF	IRQ and Break Vector	ROM
FFFC-FFFD	Power Up and Restart Vector	ROM
FFFA-FFFB	NMI Interrupt Vector	ROM
6000-FFF9	System Firmware	ROM
4F00-5FFF	Software Patch PROMS	PROM
4000-41FF	Configuration Storage	RAM
1800-37FF	Optional Buffers (Ext. Forms and Comm-Stor III Forms)	RAM
0400-17FF	Optional System Buffers	RAM
0200-03FF	I/O Buffers	RAM
01DA-01FF	Stack	RAM
0020-01D9	System RAM	RAM
0000-001F	Hardware Device Registers	

TABLE #6-2

Comm-Stor IV MEMORY MAP

ADDRESS	FUNCTION	HARDWARE
FFFE-FFFF	IRQ and Break Vector	ROM
FFFC-FFFD	Power Up and Restart Vector	ROM
FFFA-FFFB	NMI Interrupt Vector	ROM
6000-FFF9	System Firmware	ROM
5000-AFFF	Optional System Buffers	RAM*
1000-4FFF	Object Space Buffer	RAM
0F00-0FFF	Software Patch PROMS	PROM
0800-09FF	Configuration Storage	RAM
0200-07FF	I/O Buffers	RAM
01DA-01FF	Stack	RAM
0020-01D9	System RAM	RAM
0000-001F	Hardware Device Registers	

*This RAM overlays system ROMS. Circuitry on the 24K RAM board determines if the processor is requesting RAM or ROM data.

TABLE #6-3

B. Oscillator Circuit

The Oscillator circuit consists of a special CMOS Oscillator which is controlled by an 8-MHz crystal. Supporting circuitry divides the 8-MHz oscillator output frequency to three primary frequencies used in the system. The three frequencies are:

1. 4 MHz - used for bit clock generation in disk control circuitry.
2. 31.25 KHz - master clock frequency for the system timer located on the disk control board.
3. 1 MHz - used for microprocessor cycle timing. This 1 MHz signal is clocked through an 8-bit shift register at an 8 MHz rate. The shift register provides 6 slightly out of phase 1 MHz signals for critical system timing.

C. Restart Circuit

The microprocessor is reset back to its initial start-up sequence when the system is "powered-on" or the RESTART button is depressed.

D. Baud-Rate Switches

The MP-RAM board has space allocated for four BCD (Binary Coded Decimal) switches. The binary information on these switches is transferred through a multiplexer to the processor via the Data In Bus (DB1-DB7).

The basic Comm-Stor is provided with switches for terminal and modem baud rate selection. An additional switch is used for Printer Port option. The fourth location is reserved for future expansion or special applications.

E. Device Group and Memory Bank Decoders

The decoders, located on the MP-RAM board, decode Address Bus lines (A0-A15) to provide "control strobe" signals for memory and data transfer devices within the system. The "control strobe" signals are as follows:

$\overline{\text{DG1}}$ - Terminal and Modem Data Transfer

$\overline{\text{DG2}}$ - Printer Port Data Transfer

$\overline{\text{DG3}}$ - Disk Control Data Transfer

$\overline{\text{CMOS}}$ - 512(256) x 8 - CMOS RAM Data Transfer

RAM0CK - 1024 x 8 - RAM Bank 0 Data Transfer

RAM1CK - 1024 x 8 - RAM Bank 1 Data Transfer

F. Memory Patch Prom

The PROM (Programmable Read-Only Memory), located in position K1, provides the system with the ability to add to or change already existing software subroutines located in the ROMS on the ROM circuit board. In the Comm-Stor II, III and IV systems, this location is vacant.

G. Random Access Memory

The RAM (Random Access Memory) located on the MP-RAM logic card allows the microprocessor to store non-permanent erasable data. The Data In Bus, Data Out Bus and the Address Bus transfer internal system data in and out of RAM. A RAM bank is composed of eight 1024x1 RAM ICs, thus allowing 1024 bytes of memory.

1.) RAM Bank 0

The RAM located at addresses 20_{16} to $3FF_{16}$ provides a scratch pad area for the microprocessor to store internal system data. RAM Bank 0 buffers data which is to be transferred on or off the diskette and data which is to be transferred through the EIA I/O ports. Addresses 00 to $1F_{16}$ are reserved for hardware device registers.

2.) RAM Bank 1 (for Forms Option on Comm-Stor, standard on Comm-Stor II/III and Comm-Stor IV)

The RAM located at addresses 400_{16} to $7FF_{16}$ provides a storage area for operations performed with Comm-Stor options.

3.) CMOS RAM

CMOS RAM, stores the variable Configuration and User Table information. Unlike RAM Banks 0 and 1, CMOS RAM is directly connected to the microprocessor 8-bit bi-directional Data Bus. The tri-state data I/O lines can either read, write or ignore data on the 8-bit bi-Data Bus. Each CMOS RAM package stores 256 4-bit words.

When Comm-Stor is powered down, CMOS RAM data is maintained by a circuit which automatically switches the CMOS RAM over to a 4.5 volt battery supply

when "power-off" is sensed. The battery is a non-rechargeable alkaline cell.

4. FIRMWARE BOARDS

Only one of the following boards will be in a Comm-Stor system.

A. ROM Board

The ROM board is made up of eight ROMS (2048 x 8) which store the standard 16K bytes of system firmware. In addition, the ROM board has sockets and decoding for eight PROMS which can be used for firmware expansion. Refer to Figure #6-4 for the block diagram of the ROM board. Drawing number 1030A6159 illustrates the component layout of the ROM board. The schematic for this board is found in Chapter 11.

Address decoding for the ROM section of memory is handled at two levels:

1.) Address lines A11, A12, A13, and A15 are decoded by a one-of-eight Half-Field decoder. This decoder provides a ROM Enable signal for each of the eight ROMS.
2.) Address lines A14, A0-A10 are decoded internally in each ROM and are capable of accessing 1 of 2048 bytes.

Address decoding for the PROM section of memory is handled at three levels:

1.) The Half-Field decoder output signals are used to select the appropriate section of PROM memory. The specific address range is determined by two jumpers on the ROM board.
2.) Address lines A9, A10, and A14 are decoded by two "one-of-four" decoders in each of the two fields. The one-of-four decoder signal output acts as a PROM Enable signal in the selected field. Logic strobe ICs provide current amplification for the PROM Enable signal.
3.) Address lines A0-A8 are internally decoded by the selected PROM to access 1 of 512 bytes.

B. ROM II Board

The ROM II board is made up of ROMS (2048 x 8) which store the standard Comm-Stor II/III and IV program. In addition, the ROM board has sockets and decoding for five PROMS which can be used for firmware expansion. Refer to Figure #6-5 for the block diagram of the ROM II board. Drawing number 1030T6480 illustrates the component layout of the ROM II board. The schematic for this board is found in Chapter 11.

Address decoding for the ROM section of memory is handled at three levels:

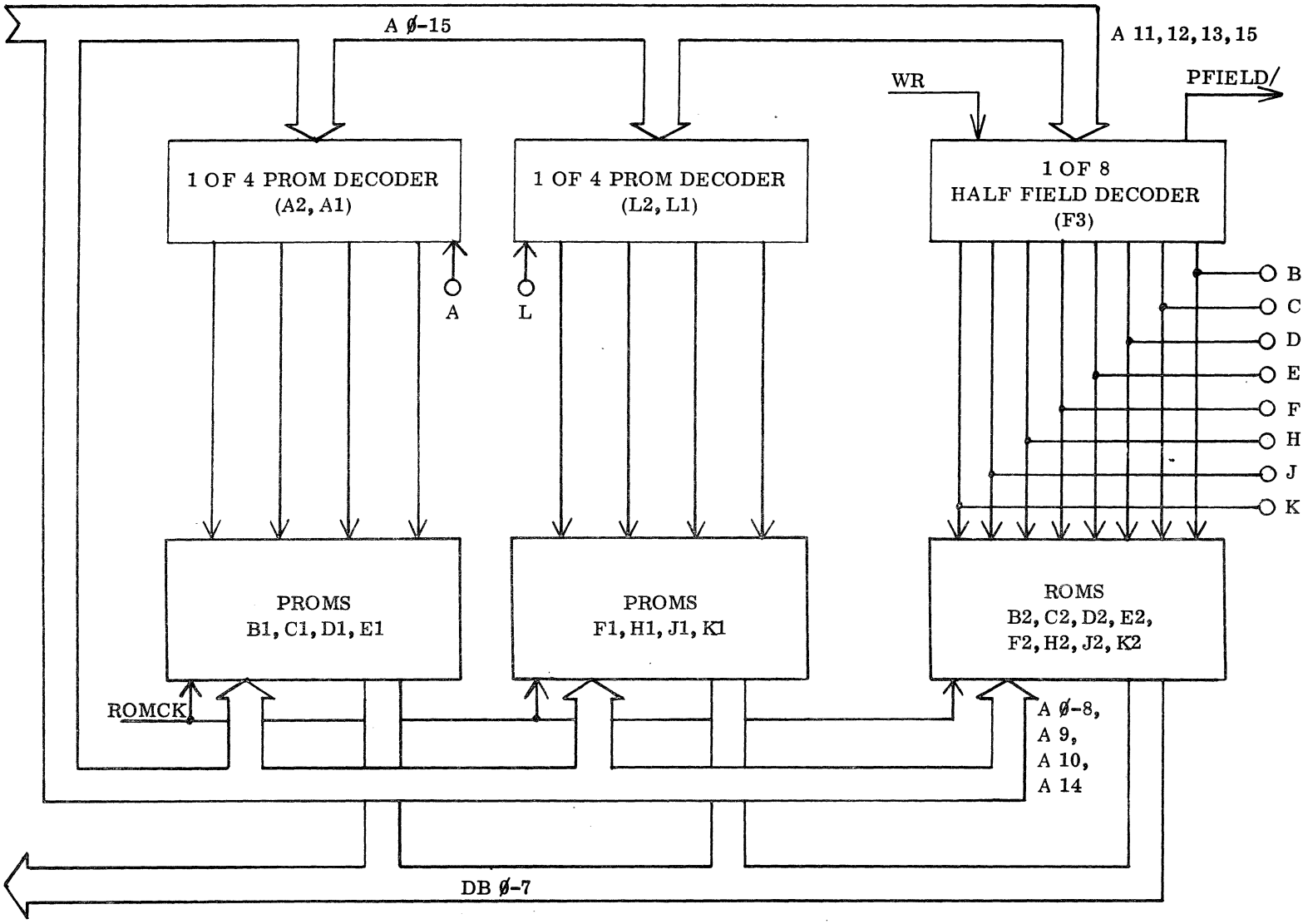
1.) Address lines A15, A14 and A13 are decoded by a 3 to 8 line decoder. This provides five distinct Enable signals. Each signal enables 4 out of 20 possible ROM locations.
2.) Address lines A12 and A11 are then used to select one of the four ROMS to be read.
3.) Address lines A0-A10 are decoded internally, by each ROM, to select 1 of 2048 locations.

Address decoding for the PROMS is also handled at three levels:

1.) Address lines A15, A14 and A13 are decoded and enable the bank of 4 PROMS.

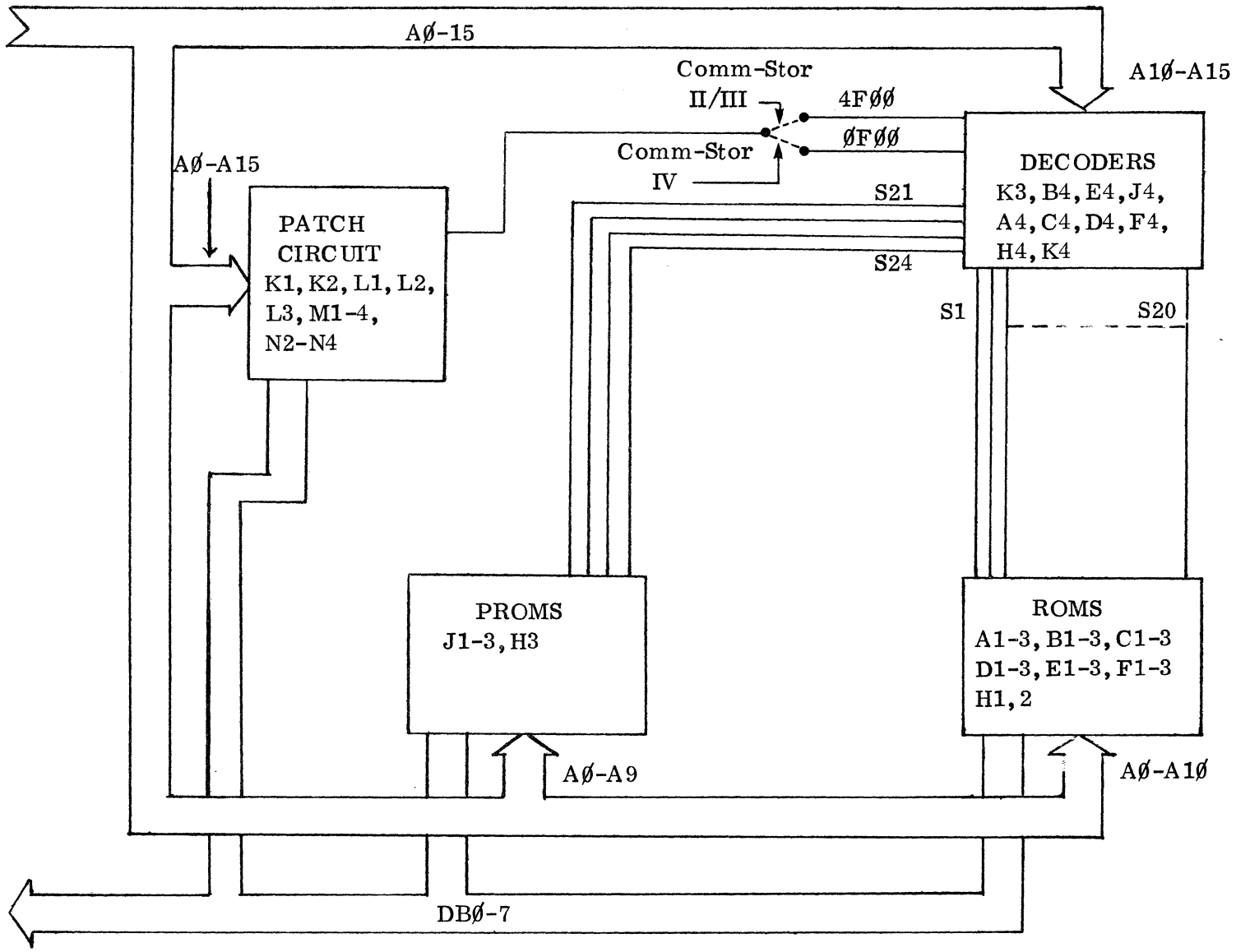
2.) Address lines A12, A11 and A10 then select one of the four PROMS.
3.) Address lines A0-A9 are decoded internally, by each PROM, to enable 1 of 1024 locations.

The Patch PROM address locations vary for Comm-Stor II/III systems and Comm-Stor IV. A strapping option is provided for



BLOCK DIAGRAM OF THE ROM BOARD

FIGURE #6-4



BLOCK DIAGRAM OF THE ROM II BOARD

FIGURE #6-5

this change. Instructions may be found on the schematic drawing for the ROM II board in Chapter 11.

System Firmware Patching

This circuit allows PROM data to be substituted for ROM data. This gives Comm-Stor the ability to patch changes and additions into the system without changing the ROMS.

PROM location K1 contains the higher order address at which a change is to be made. This byte is located at the lower order address at which the change is to be made within the PROM. Whenever that lower order address appears on the bus, the higher order byte of the current address is compared to the byte within the PROM. If they are equal, a "Jump" instruction is forced onto the bus and the jump address is pulled from PROM K1. The processor then jumps to that address which is in one of the remaining four PROMS and executes the patch rather than the ROM routine.

5. DISK CONTROLLER ASSEMBLY

The primary function of the Disk Controller Board (DCB) is to search for the proper track and sector on the diskette and to allow data to be read or written at that location. The circuitry must also convert serial disk data to parallel data for processing on the Data In Bus and the Data Out Bus. Refer to Figure #6-6 for the block diagram of the DCB. Drawing number 1030A6054 illustrates the component layout of the DCB. The schematic for this board is found in Chapter 11.

Refer to Chapter 1 for diskette layout and format information.

A. Read/Write Address Decoders

The decoders allow the microprocessor to address individual devices on the DCB for direct data transfer on the Data In and Data Out Bus or binary command control of Read/Write operations from the DO lines.

B. Disk Sequence Register

When selected by the Read/Write address decoder, the Disk Sequence Register interprets binary information on lines DO4-DO7 and provides a sequence of commands for disk control Read/Write operations.

C. Bit Clock Phase-Control Circuit

Whenever the Read/Write head is activated, or the head is moved from one track to another, there is a 50-50 change it will begin reading the composite clock/data information in sync or out of sync. Out of sync can be defined as recognizing clock pulses as data pulses and data pulses as clock pulses. Therefore the Bit Clock Phase-Control Circuit must be capable of recognizing an out of phase condition and adjusting itself by as much as 180^{o} to establish sync.

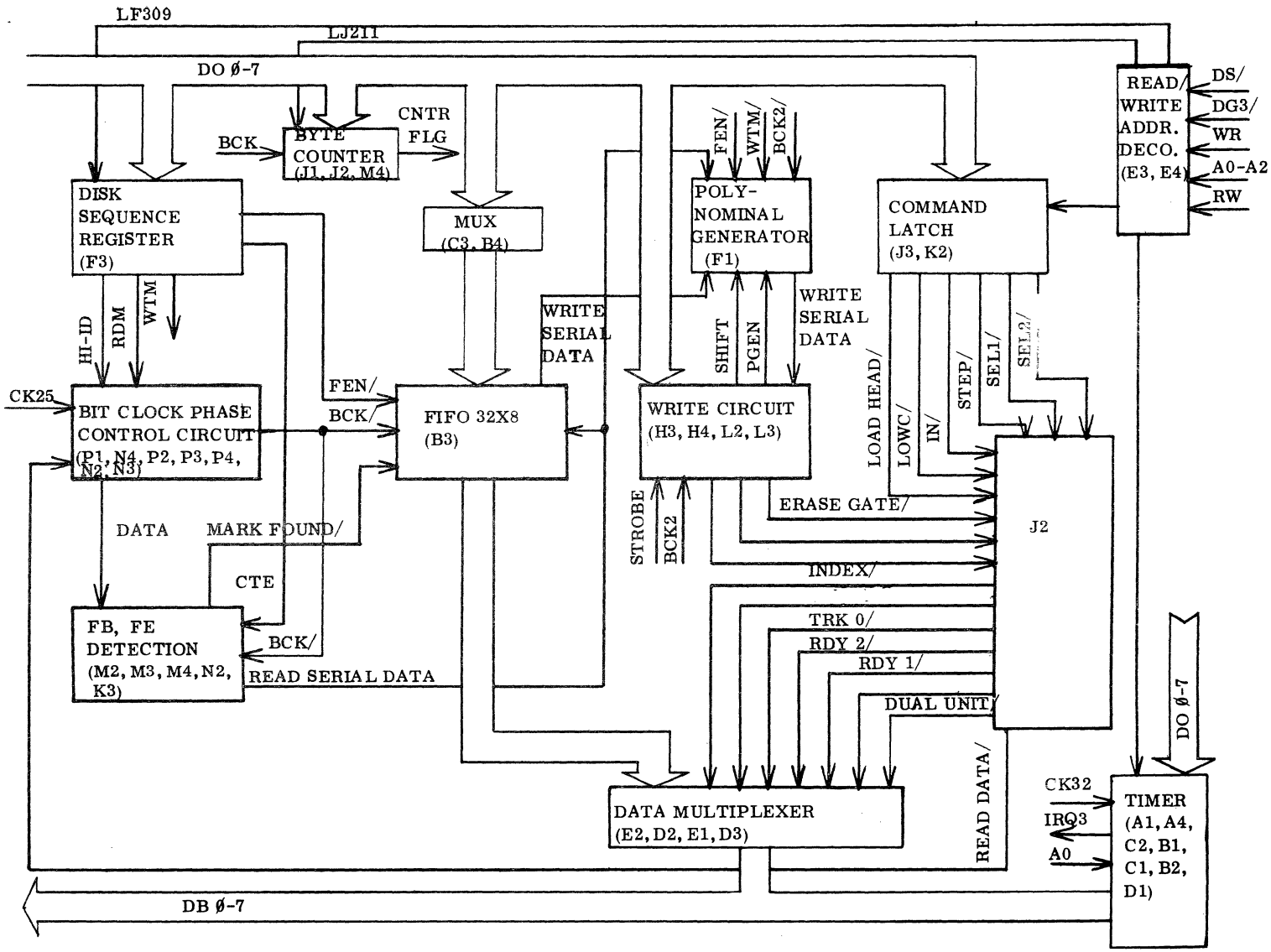
Refer to Figure #6-7 for the Bit Clock Generation timing diagram. Also reference the diskette layout shown in Chapter 1. Bit Clock Sync is established in the gap of six 00_{16} bytes which proceeds each sector. 00_{16}'s are recorded on the disk as clock pulses with absence of interwoven data pulses.

If the bit clock phase is initially out of sync, the read data is read as all "1"s with missing clock pulses. If this situation exists for four serial data bits, a missing clock pulse counter automatically resets the Bit Clock Generator causing the needed phase reversal.

D. Address/Data Mark Detection Circuit

After proper bit sync has been established, the Address/Data Mark Circuit begins checking data pulses for an appropriate Address Mark (FE_{16}) and/or Data Mark (FB_{16}). At the same time, the Bit Clock Phase Circuit is checking clock pulses for missing clocks.

Refer to Figure #6-7. If exactly three missing clock pulses are counted ($C7_{16}$ clock) and an FE_{16} data byte is re-



BLOCK DIAGRAM OF THE DISK CONTROLLER BOARD

FIGURE #6-6

quested and detected, the Mark Found signal goes high indicating the start of a data block.

E. Bit/Byte Count Circuit

All bytes read off the diskette are counted by a Bit/Byte Count Circuit. A desired byte count number is loaded into a parallel 4-bit register from DO lines 0-3. When the appropriate byte count is reached, a flip-flop is latched high raising the Counter Flag (CNTR FLG) signal.

If the microprocessor has been put in a mode by the firmware to recognize Non-Maskable Interrupts, the presence of the CNTR FLG signal immediately causes a Non-Maskable Interrupt to take place.

F. Serial to Parallel Conversion Circuit

During a read operation, this circuit converts serial data being read off the diskette to 8-bit parallel data; during a write operation, the circuit converts parallel data to serial data for transfer to the diskette. This is accomplished by the use of a 32 x 8 FIFO (first in/first out) memory. During a read operation, serial data fills the input register and is strobed out of the output register of the FIFO as parallel 8-bit bytes; during a write operation, parallel 8-bit bytes are strobed into the FIFO input register from the Data Out Bus. Subsequently, data is shifted out serially, one bit at a time, until every byte in the FIFO has been transferred.

G. Write Circuit

Data which is about to be written on the diskette is combined with Bit Clock data and is output directly to the Disk Drive Assembly as Composite Data. This circuit also provides control of data being shifted out of the FIFO, and CRC generation.

H. CRC Generation and Check

CRC generation and checking is performed mainly by a special purpose Polynominal Generator IC. In the write mode, this circuitry calculates a 16-bit CRC character and writes it onto the diskette at the end of each data block. In the read mode, this circuitry looks at each byte being read off the diskette and calculates a CRC character which is then compared to the CRC character read off the diskette at the end of each data block.

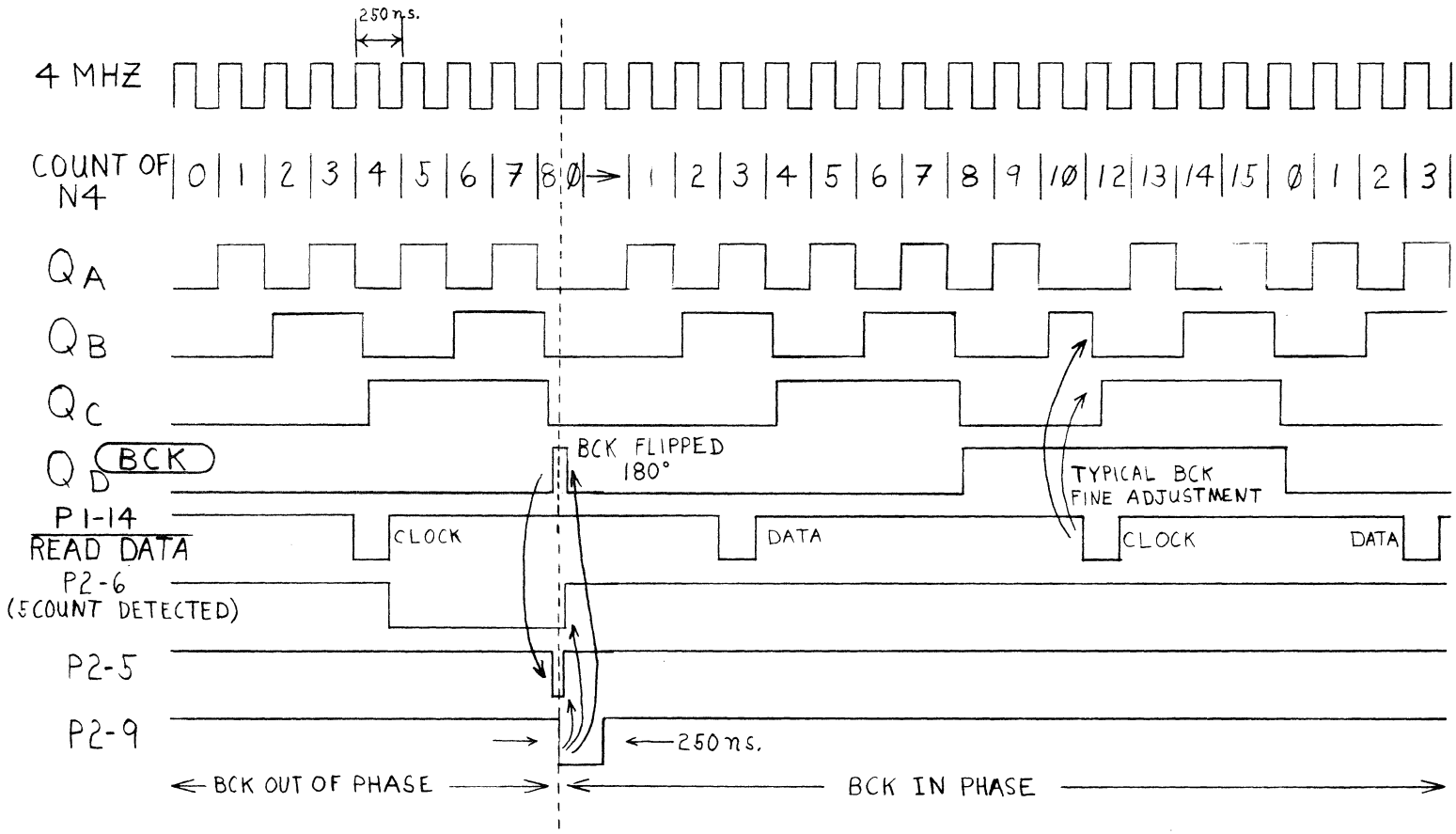
I. Disk Drive Interface Circuit

1.) Command Latch - eight signals which control electromechanical operations on the Disk Drive Assembly are strobed into an eight-bit data latch. The signals then are transferred off the Disk Control Board to the Disk Drive Assembly through the Ribbon Wire Connector (J2) located on the top of the board.

2.) Status Register Multiplexor - eight other signals which indicate the condition or status of the Disk Drive Assembly are multiplexed onto the Data In Bus when requested by the microprocessor.

J. Timer Circuit

The timer circuitry provides Comm-Stor with the ability to initiate operational time delays up to 2.0 seconds and check the timing of critical system functions.

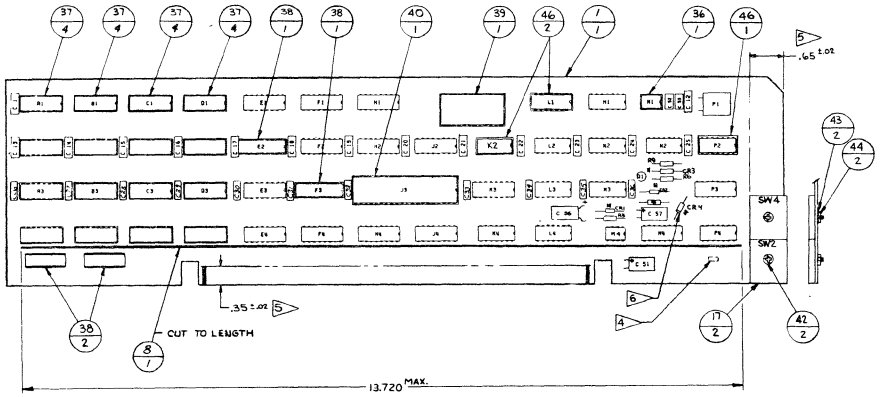


BIT CLOCK GENERATION TIMING DIAGRAM

FIGURE #6-7

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. CAPACITORS C37 & C58 HAVE BEEN REMOVED ASSEMBLE CR4 ORIENTED AS SHOWN IN THE BOTTOM LEG COMPONENT HOLES VACATED BY C37 & C58 (SEE SHEET 2)
7. SEE SHEET 2 FOR ADDITIONAL REWORK INSTRUCTIONS



	M4	47	100U17004	INT CKT-555	1
	XK2, XL1, XP2	46	101U16002	SKT-14 POS	3
	L1, K2	45	100U18038	INT CKT-74C00, CMOS	2
		44	500H10201	NUT, HEX, #2	2
		43	200H03020	LOCKWASHER, INT., #2	2
		42	100H01206	PAN HEAD, #2-56x3/8	2
	P1	41	100Y01007	XTAL 8.000 MHZ	1
	XJ3	40	101U16006	SKT-40 POS	1
	XK1	39	101U16005	SKT-24 POS	1
	XA5, XB5, XE2, XF3	38	101U16004	SKT-18 POS	4
	XA1-A4, XB1-B4, XC1-C4, XD1-D4	37	101U16003	SKT-16 POS	16
	XN1	36	101U16001	SKT-8 POS	1
	E1, F1	35	100U19034	INT CKT - 74LS85	2
	P2	34	100U19033	74LS393	1
	L2	33	100U19029	74LS260	1
	P3, N4, F2, H1	32	100U19028	74LS257	4
	N2	31	100U19022	74LS164	1
		30			
	H4	29	100U19016	74LS139	1
	J4	28	100U19015	74LS138	1
	L3	27	100U19008	74LS10	1
	L4	26	100U19007	74LS08	1
	K4, M2	25	100U19006	74LS04	2
	M1	24	100U19004	74LS00	1
	N1	23	100U18036	7209	1
	E2, F3	22	100U18035	74C921	2
		21			
	A1, A3, B1, B3, C1, C3, D1, D3	20	100U18023	9LO2 8/21024	8
	J3	19	100U18017	6502	1
	E3, E4, F4, H2, J2, K3	18	100U16072	INT CKT-8T97	6
	SW2, SW4	17	107S01001	MINI THUMBWHEEL SW.	2
	M3, P4	16	103R01012	RES DIP PKG, 4.7K Ω, 2%	2
		15			
	R5, R6	14	100R02121	RES-100K, 1/4W, 5%	2
	R3	13	100R02097	RES-10K, 1/4W, 5%	1
	R9	12	100R02067	RES-560Ω, 1/4W, 5%	1
	CR4	11	200C02009	RECTIFIER-IN5818	1
	Q1	10	201Q01001	TRSTR, MPS-6534	1
	CR1, CR2, CR3	9	200C01001	DIODE IN4153	3
		8	108E01001	BUS BAR	1
	C1,2-36	7	120C03010	CAP CER DISC .05UF	25
	C52, C53	6	120C01012	CAP, CRD 22 PF	2
		5			
		4			
	C51, C56, C57	3	105C04105	CAP, TANT, 22UF	3
L		2	1030B6046	SCHEMATIC MP RAM	REF
F-04		1	1030B6047	PWB MP RAM	1
REV	DESIGNATION	ITEM	PART #	DESCRIPTION	QTY

SYNEC DATATRONICS, INC. ROCHESTER, NEW YORK

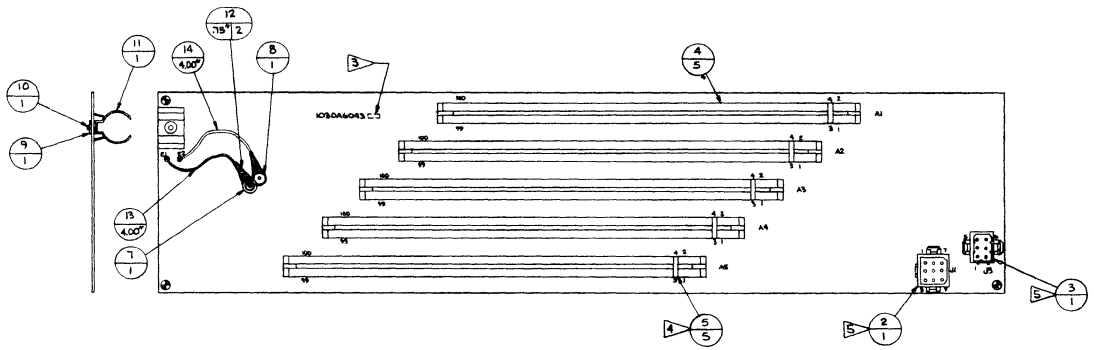
TITLE: PWB ASSY MP-RAM

DWG SIZE: D | DWG NO.: 1030A6045 | SHEET 1 OF 2 | REV: N

FIGURE #6-8

NOTES:

1. REFER TO ENG. STD. ES102-02.
2. SOLDER PER ES102-03.
3. REVISION LETTER PER ES102-02.
4. ON CONTACT KEY ITEM 5 TO BE IN POSITION 3 & 4 IN CONNECTORS A1 - A5.
5. ORIENT CONNECTORS J1, & J3 AS SHOWN.



DESGN	ITEM	PART #	DESCRIPTION	QTY
	14	600W01609	WIRE, WHT #24 GA.	4.00"
	13	600W01600	WIRE, BLK #24 GA.	4.00"
	12	200W30005	SHRINK TUBING	1.50"
	11	10308692 1	COMPONENT CLIP	1
	10	500H52012	POP RIVIT	1
	9	200H11008	WASHER #5 PLAIN	1
	8	102E62005	BATTERY CLIP - SOCKET	1
	7	102E62002	BATTERY CLIP - STUD	1
	6			
	5	100J13005	KEYING PLUG, ON CONTACT	5
A1 - A5	4	100J13003	HSG ASS'Y, TWIN LEAF, 50 SOLDER POS	5
J3	3	100J11562	HEADER, 6 POS, MR	1
J1	2	100J11558	HEADER, 9 POS, MR	1
	1	1030B6044	PWB 8000 BASE CARD	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

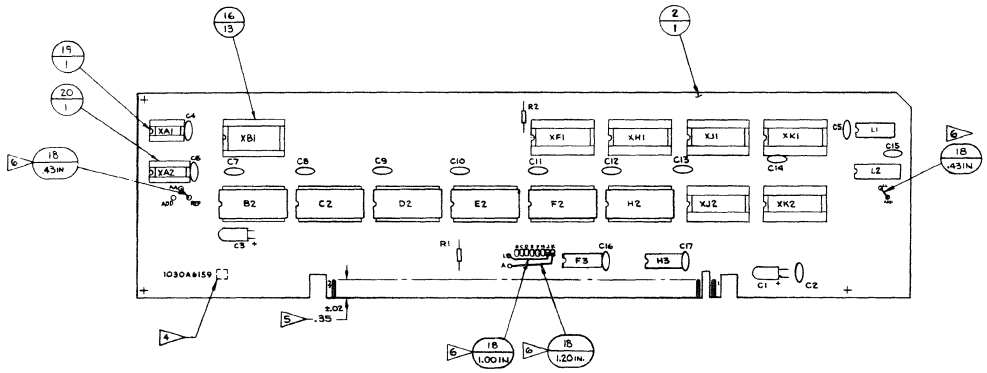
TITLE: PWB ASSY
8000 BASE CARD

SIZE D | DWG NO. 1030A6043 | REV C | SHEET 1 OF 1

FIGURE #6-9

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. APPLY JUMPERS ITEM 18 TO SPECIFIED LOCATIONS AS SHOWN



DESIGNATION	ITEM	PART #	DESCRIPTION	QTY
XA2	20	101U116003	SOCKET, DIP-14 POS	1
XA1	19	101U116002	SOCKET, DIP-14 POS	1
	18	600W06405	WIRE, 26GA. SOLID GRN	3.06 IN.
R2	17	100R02073	RESISTOR-1.0K, 5%, 1/4W	1
XB1,F1-XK1,X2-XK2	16	101U116005	SOCKET, DIP-24 POS	15
R1	15	100R02049	RESISTOR-100Ω, 5%, 1/4W	1
C2, C4-17	14	120C03011	CAP, DISC-0.1UF, 10V	15
C1, C3	13	105C04105	CAP, TANT-22UF, 15V	2
H3	12	100U13004	INT CKT-74LS00	1
F3, L2	11	100U18015	" -74LS138	2
	10			
L1	9	100U18034	" -VD 6605	1
H2	8	1030B6146	" -ROM, D000	1
F2	7	1030B6145	" -" ,D800	1
E2	6	1030B6144	" -" ,E000	1
D2	5	1030B6143	" -" ,E800	1
C2	4	1030B6142	" -" ,F000	1
B2	3	1030B6141	INT CKT-ROM, F800	1
	2	1030B6161	PWB-ROM 2316AN	1
	1	1030B6160	SCHEMATIC-ROM	REF

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASSY ROM-2316AN

DWG SIZE: D | DWG NO.: 1030A6159 | REV: B | SHEET 1 OF 1

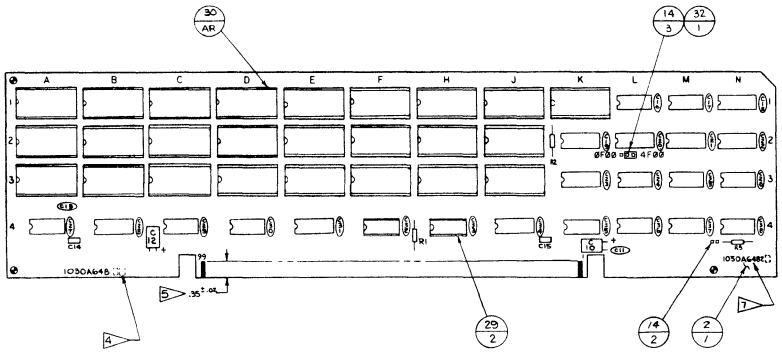
FIGURE #6-10

NOTES:

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-02
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER & LAST DIGIT OF ASSY NUMBER PER ES102-02 & CHART BELOW (NOTE 6)
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. 1030T6480 IS A REFERENCE ASSY COVERING ALL ROM II PWB ASSEMBLIES. FOR A SPECIFIC ASSEMBLY PARTS LIST SEE CHART BELOW:

	DESCRIPTION	PART NUMBER	PATCH LOCATION STRAP SETTING	USED ON	REMARKS
7	ROM II/ XTENDED	1030A6482	4FØØ	COMM-STOR II, III & IV	USED TO MAKE HIGHER ASSYS
4	ROM II	6481	4FØØ	COMM-STOR II	MAKE FROM 1030A6482
4	ROM II EXT FORMS	6483	4FØØ	COMM-STOR II OPTIONS	MAKE FROM 1030A6482
4	ROM II/ARITHMETIC	6484	4FØØ	COMM-STOR III	MAKE FROM 1030A6482
4	ROM II/ BASIC	1030A6485	ØFØØ	COMM-STOR III	MAKE FROM 1030A6482

7. ASSY NUMBER & REVISION LETTER PER ES102-02 SHOULD APPEAR ON EACH ASSY IN LOCATION SHOWN



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: REFERENCE PWB ASSEMBLY ROM II / 40K

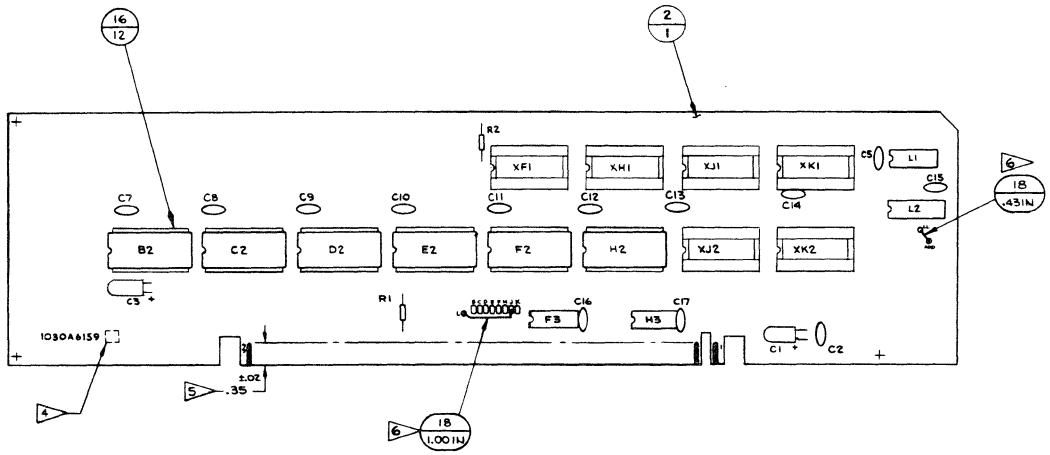
DWG SIZE	DWG NO.	REV
D	1030T6480	M

SHEET 1 OF 1

FIGURE #6-11

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. APPLY JUMPERS ITEM 18 TO SPECIFIED LOCATIONS AS SHOWN



DESIGNATION	ITEM	PART #	DESCRIPTION	QTY
	18	600W06405	WIRE, 26GA-SOLID GRN	1.43 IN
R2	17	100R02073	RESISTOR-1.0K,5%,1/4W	1
XF1-XK1, XB2-XK2	16	101U16005	SOCKET, DIP-24 POS	12
R1	15	100R02049	RESISTOR-100Ω,5%,1/4W	1
C2,C5,C7-17	14	120C03011	CAP, DISC-0.1UF,10V	13
C1,C3	13	105C04105	CAP, TANT-22UF,15V	2
H3	12	100U19004	INT CKT-74LS00	1
F3, L2	11	100U19015	" - 74LS138	2
	10			
L1	9	100U18034	" - HD 6605	1
H2	8	1030B6146	" - ROM, D000	1
F2	7	1030B6145	" - " , D800	1
E2	6	1030B6144	" - " , E000	1
D2	5	1030B6143	" - " , E800	1
C2	4	1030B6142	" - " , F000	1
B2	3	1030B6141	INT CKT-ROM, F800	1
	2	1030B6161	PWB-ROM 2316AN	1
	1	1030B6160	SCHEMATIC-ROM	REF

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASSY ROM-2316AN

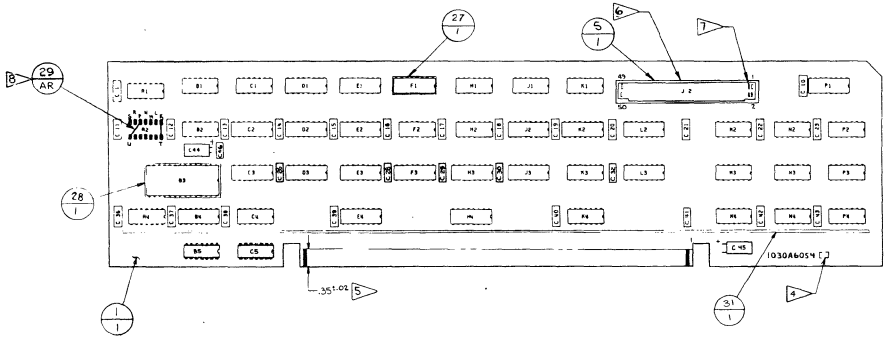
DWG SIZE: D | DWG NO.: 1030A6159 | REV: A | SHEET 1 OF 1

FIGURE #6-12

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. MOUNT CONN J2 WITH INSPECTION SLOTS FACING CUT BOARD.
7. REMOVE CONNECTOR PINS 3 & 4 ON J2, ITEM 5
8. A2 WIRING CHART

WIRE ITEM	FROM	TO
1	A2-P	A2-U
2	A2-K	A2-T



DESIGNATION	ITEM	PART #	DESCRIPTION	QTY
	40			
	39			
	38			
	37			
	36			
	35			
	34			
	33			
	32			
	31	108EC1001	BUS BAR	1
C42, C36	30	120C01030	CAP, DISC-150 PF	2
	29	600W06905	WIRE, SOLID-26 GA GRN	AR
	28	101U16007	SOCKET-28 POS	1
	27	101U16003	SOCKET-16 POS	1
A1, A4, M4	26	100U19033	INT. CKT. 74LS393	3
D2, D3, E1, E2	25	100U19028	74LS257	4
N4	24	100U19027	74LS197	1
F2, N3	23	100U19025	74LS11	2
F3, H3, H4	22	100U19024	74LS175	3
C2	21	100U19023	74LS174	1
M2	20	100U19022	74LS164	1
B4, C3	19	100U19020	74LS157	2
E3, E4	18	100U19015	74LS138	2
B1, B2, C1, C4, J1, K3, N2, P3	17	100U19011	74LS74	8
H1, M3, P4	16	100U19006	74LS04	3
H2, K4, P2, B5	15	100U19004	74LS00	4
J2, P1	14	100U19001	74LS191	4
F1	13	100U18025	8506P	1
B3	12	100U18021	2812A	1
L3	11	100U16067	74151A	1
L2	10	100U16062	74165	1
C5	9	100U19013	74LS86	1
D1	8	100U16060	7414B	1
J3, K2	7	100U16028	INT. CKT. 7417S	2
K1	6	103R03003	RES: TERM PAK 220/330Ω	1
J2	5	100J11408	HEADER, 50 POS, STR. IN	1
C1, 10-23, 26, 28-30, 32, 37-41, 43	4	120C03010	CAP, CER, DISC, 0.05 UF	26
C44, 45	3	105C04105	CAP, TANT, 22UF	2
	2	103086055	SCHEMATIC, DISK CONT.	REF
	1	103086056	PWB DISK CONT.	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

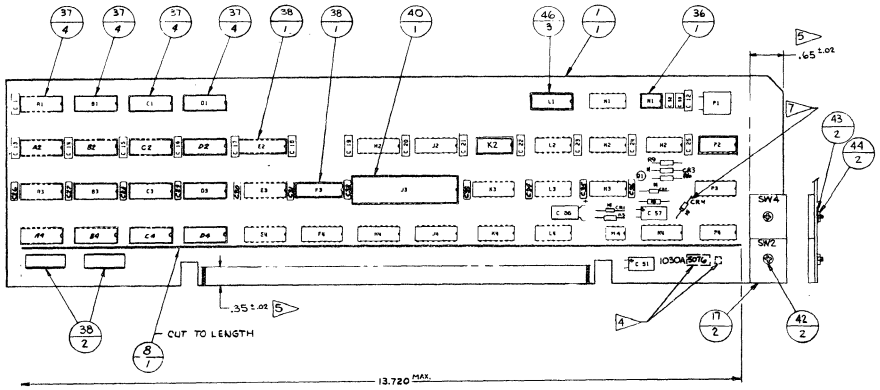
TITLE: PWB ASSY
DISK CONTROLLER

SIZE D | DWG NO. 1030A6054 | REV C | SHEET 1 OF 1

FIGURE #6-13

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER AND ASSY NO. PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. SEE CIRCUITRY MODIFICATION INSTRUCTIONS ON SHT 2
7. CAPACITORS C37 & C58 HAVE BEEN REMOVED ASSEMBLE CR4 ORIENTED AS SHOWN IN THE BOTTOM LEG COMPONENT HOLES VACATED BY C37 & C58 (SEE SHEET 2)



DESIGNATION	ITEM	PART #	DESCRIPTION	QTY
M4	47	100U17004	INT CKT-555	1
XK2, XL1, XP2	46	101U16002	SKT-14 POS	3
L1, K2	45	100U18038	INT CKT-74C00, CMOS	2
	44	500H10201	NUT, HEX, #2	2
	43	200H03020	LOCKWASHER, INT, #2	2
	42	100H01206	PPAN HEAD, #2-56x3/8	2
P1	41	100Y01007	XTAL 8.000 MHZ	1
XJ3	40	101U16006	SKT-40 POS	1
	39			
XA5, XB5, XE2, XF3	38	101U16004	SKT-18 POS	4
XA1-A4, XB1-B4, XC1-C4, XD1-D4	37	101U16003	SKT-16 POS	16
XN1	36	101U16001	SKT-8 POS	1
	35			
P2	34	100U19033	INT CKT 74LS393	1
L2	33	100U19029	74LS260	1
P3, N4	32	100U19028	74LS257	2
N2	31	100U19022	74LS164	1
	30			
H4	29	100U19016	74LS139	1
J4	28	100U19015	74LS138	1
L3	27	100U19008	74LS10	1
L4	26	100U19007	74LS08	1
K4, M2	25	100U19006	74LS04	2
M1	24	100U19004	74LS00	1
N1	23	100U18036	7209	1
E2, F3	22	100U18035	74C921	2
	21			
A1-4, B1-4, C1-4, D1-4	20	100U18023	9LO28/2102AL	16
J3	19	100U18017	6502	1
E3, E4, F4, H2, J2, K3	18	100U16072	INT CKT-8T97	6
SW2, SW4	17	107S01001	MINI THUMBWHEEL SW	2
M3, P4	16	103R01012	RES DIP PKG, 4.7K Ω, 2%	2
	15			
R5, R6	14	100R02121	RES-100K, 1/4W, 5%	2
R3	13	100R02097	RES-10K, 1/4W, 5%	1
R9	12	100R02047	RES-5.1Ω, 1/4W, 5%	1
CR4	11	200C02009	RECTIFIER 1N5318	1
Q1	10	201Q01001	TRSTR, MPS-6534	1
CR1, CR2, CR3	9	200C01001	DIODE 1N4153	3
	8	108E01001	BUS BAR	1
C1-36	7	120C03010	CAP, CER DISC .05 UF	25
C52, C53	6	120C01012	CAP, CRD 22 PF	2
	5			
	4			
C51, C56, C57	3	105C04105	CAP, TANT, 22 UF	3
	2	103085077	SCHEMATIC, MP RAM IV	REF
	1	103086047	PWB MP RAM	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

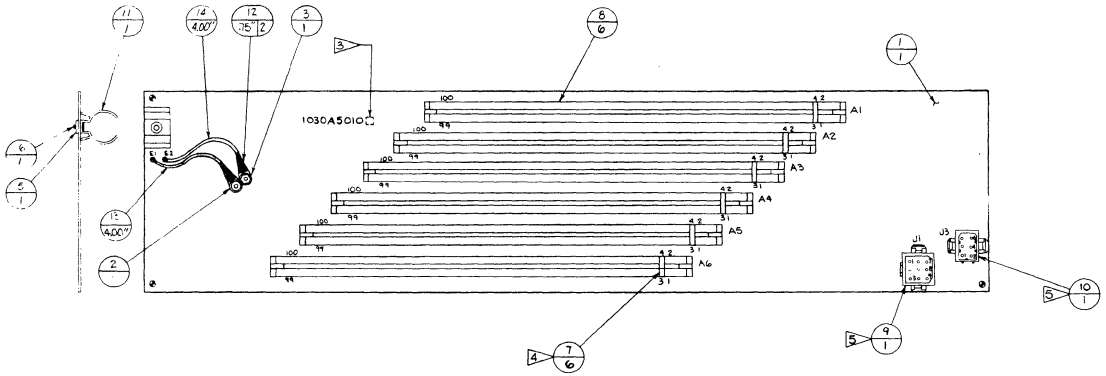
TITLE: PWB ASSY MP-RAM IV

SIZE D | DWG NO. 1030A5076 | SHEET 1 OF 2 | REV 3

FIGURE #6-14

NOTES:

1. REFER TO ENG. STD. ES 102-02.
2. SOLDER PER ES 102-03.
3. REVISION LETTER PER ES 102-02.
4. ON CONTACT KEY, ITEM 9, TO BE IN POSITION 3 & 4 IN CONNECTORS A1-A6.
5. ORIENT CONNECTORS J1 & J3 AS SHOWN



	14	600W01609	WIRE, WHT #24 GA	4.00IN
	13	600W01600	WIRE, BLK #24 GA	4.00IN
	12	200W30005	SHRINK TUBING	1.50IN
	11	[illegible]	COMPONENT CLIP	1
J3,	10	100J11562	HEADER, 6 POS, MR	1
J1	9	100J11558	HEADER, 3 POS, MR	1
A1-A6	8	100J13009	HSG ASSY, TWIN LEAF, 50 DUAL POS	6
	7	100J13005	KEYING PLUG ON CONTACT	6
	6	500H52012	POP RIVET	1
	5	200H11008	WASHER #5 PLAIN	1
	4			
	3	102E62003	BATTERY CLIP-SOCKET	1
	2	102E62002	BATTERY CLIP-STUD	1
	1	103085011	PWB 8000 BASE CARD-G BOARD	1
DESGN	ITEM	PART NUMBER	DESCRIPTION	QTY

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASSY
8000 BASE CARD-G BOARD

DWG SIZE: D | DWG NO.: 1030A5010 | REV:

SHEET 1 OF 1

FIGURE #6-15

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CHAPTER 7

EIA PORTS, I/O PANELS, AND RAM MEMORY

CONTENTS PAGE

1. EIA INTERFACE AND PRINTER PORT BOARDS CIRCUIT DESCRIPTION

The EIA Interface and Printer Port boards provide the circuitry to transfer data in and out of Comm-Stor to peripheral terminals, modems, and printers. All data transfers performed at the I/O ports are controlled and sequenced by the microprocessor via the Data Out Bus (DO0-DO7) and the Data In Bus (DB0-DB7). Refer to Figure #7-1 for the block diagram of the Communications Ports board. Drawing number 1030A6051 illustrates the component layout of the EIA board. Refer to Figure #7-2 for a block diagram of the Printer Port board. Drawing number 1030T6140 illustrates the component layout of the Printer board. The schematics for these two boards can be found in Chapter 11.

A. Device Strobe Address Decoders

The Decoder allows the microprocessor to address individual devices on the EIA board for direct data transfer on the Data In Bus and the Data Out Bus. The Decoder also allows the microprocessor to address binary command latches.

B. Baud Rate Generator

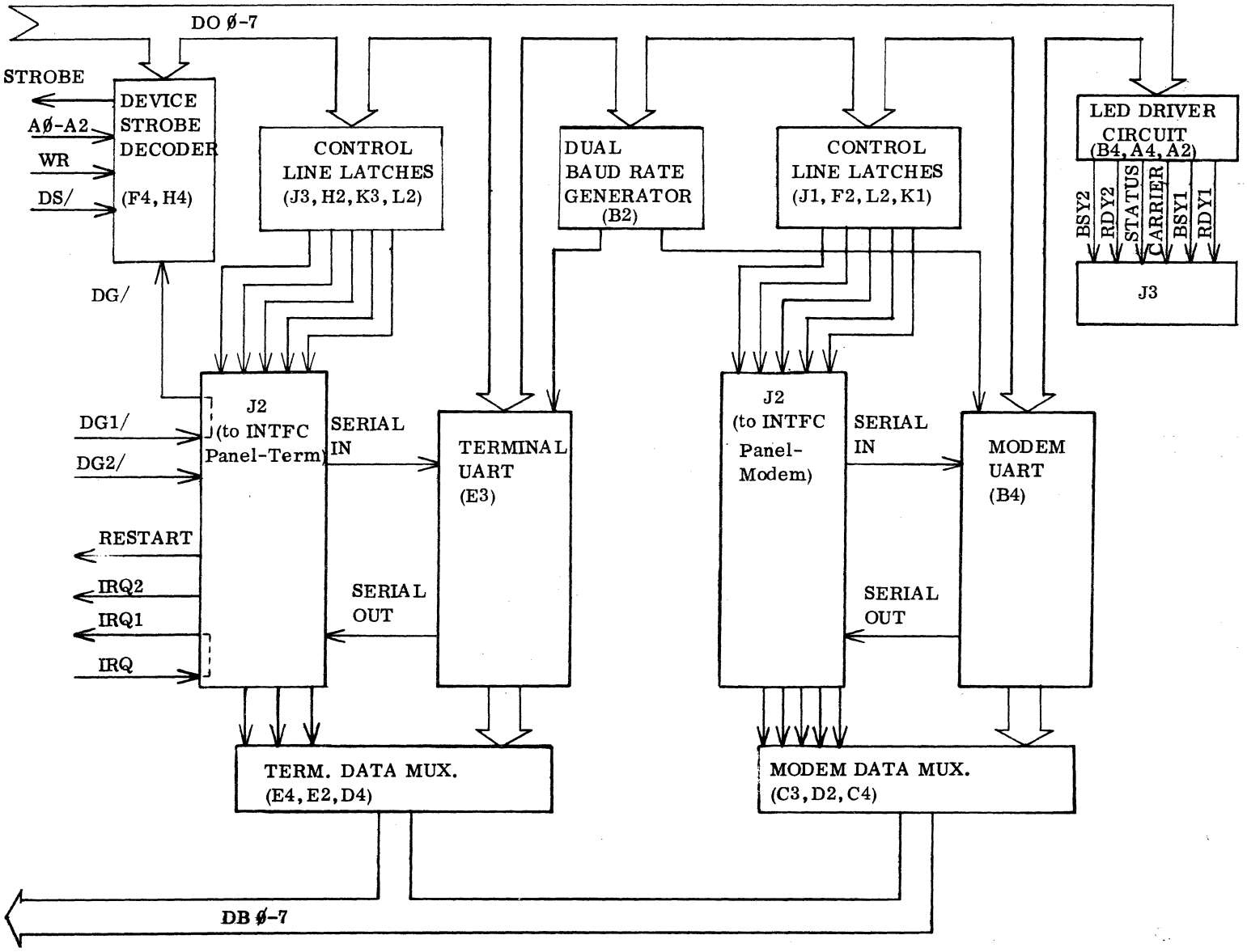
The Dual Baud Rate Generator is a special purpose IC which consists of a crystal controlled oscillator and a binary programmable divider. Any one of 15 frequencies can be selected which establish the clock frequency for the appropriate baud rate.

The Dual Baud Rate Generator is addressed by the Device Strobe Decoder, and the Data Out Bus provides the binary command which selects the desired baud rate.

C. Terminal, Modem, and Printer Universal Asynchronous Receiver/Transmitters (UART)

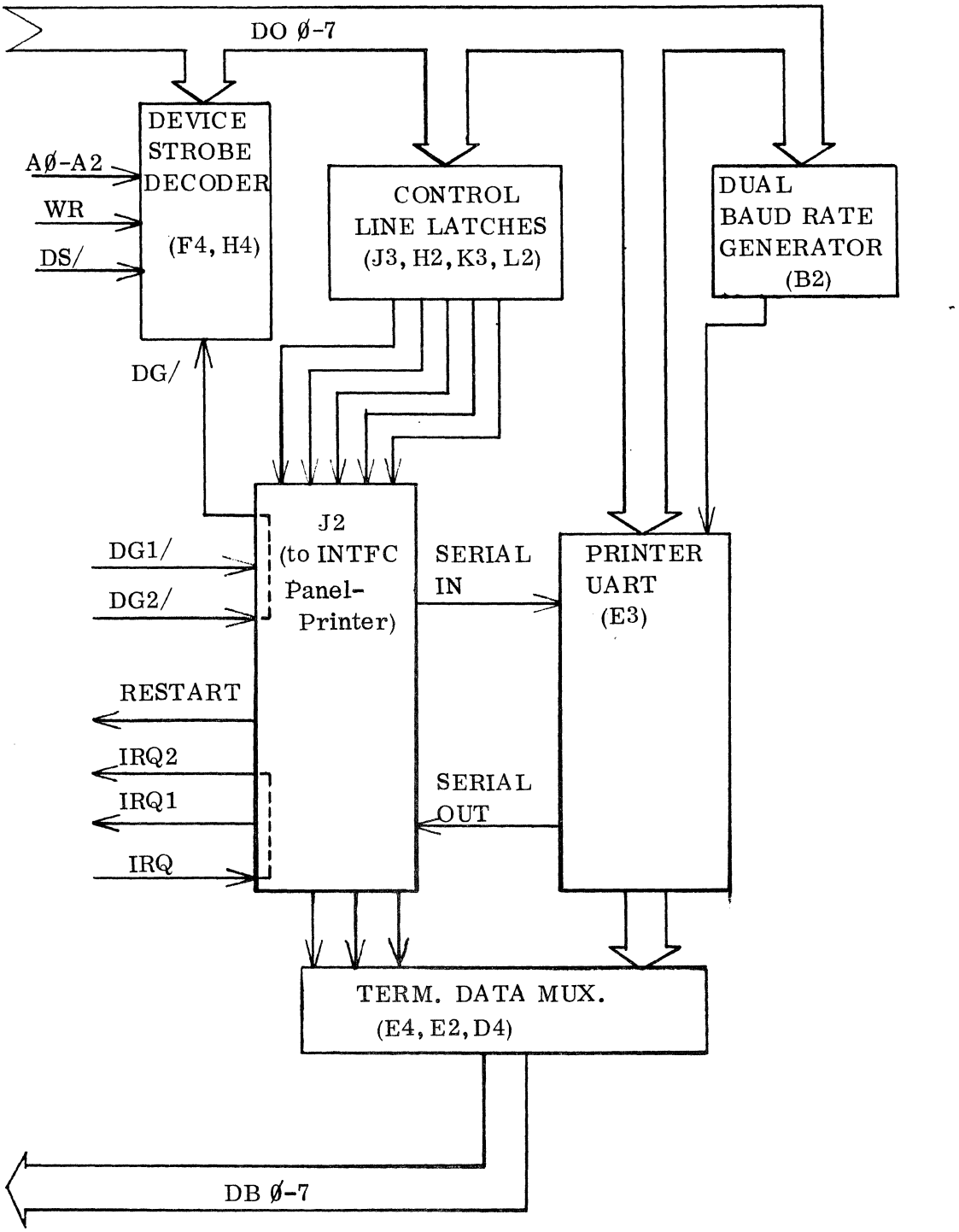
The EIA Standard RS232 specification requires that the data be sent and received by serial data lines. Therefore it is necessary to convert parallel system data to serial data so it can be transferred in and out of Comm-Stor. This is accomplished by a MOS LSI circuit called a Universal Asynchronous Receiver/Transmitter (UART).

Outgoing data is strobed into the appropriate UART from the 8-bit Data Out Bus and converted to serial form and is transmitted at a frequency determined by the Baud Rate Generator. Incoming serial data arrives at the UART where it accumulates



BLOCK DIAGRAM OF THE COMMUNICATIONS PORTS BOARD

FIGURE #7-1



BLOCK DIAGRAM OF PRINTER PORT BOARD

FIGURE #7-2

in a register and is strobed out of the UART as a parallel 8-bit character onto the Data In Bus.

D. Terminal, Modem, and Printer Port Control Lines

Comm-Stor's terminal, modem, and printer ports, operating totally independent of each other, are controlled by the microprocessor via five control lines.

The logic state of each control signal is stored in a latch. The microprocessor addresses the control line latches through the Device Strobe Decoder and controls the logic level of each control line by outputting a binary word on the DO Bus. Standard EIA Driver ICs provide isolation and amplification for the outgoing control line signals.

The microprocessor also monitors the state of incoming terminal and modem control lines. These control lines are received by standard EIA Receiver ICs. The status of the incoming control line signals are sampled by the microprocessor by multiplexing the signals onto the Data In Bus.

E. Front Panel LED Driver Circuit (EIA Interface Board Only)

The purpose of this circuitry is to light the LEDs on the Comm-Stor front panel displaying the STATUS, CARRIER, BUSY and READY signals.

The LED Driver Circuit is addressed by the Device Strobe Decoder which strobes binary command words into six latches from the DO Bus. The LEDs are actually driven by an open collector circuit and current limited by a DIP resistor network.

2. EIA I/O INTERFACE PANEL ASSEMBLY

The I/O panel, located at the rear of the chassis (see Figure #3-1) has cutouts for two or three baud rate selector switches which provide rate selection as required by the associated equipment.

The standard I/O panel has two RS-232-C compatible connectors (one for terminal and one for modem). If the Printer Port option is installed, a third RS-232-C connector is provided. Additionally, an ENTER/EXIT slide switch for Binary Data is provided on the rear panel.

A. Baud Rate Selection

Switch Position	Baud Rate
0	Keyboard
1	110
2	134
3	150
4	300
5	1200
6	2400
7	4800
8	7200
9	9600

Additional baud rates can be selected by keyboard command; refer to the appropriate Comm-Stor Reference Manual.

B. I/O Panel Removal/Replacement

The I/O Interface panel is mounted on the chassis by four screws and lockwashers. To remove the panel assembly, proceed as follows:

1.) Turn the power switch OFF.
2.) Remove the four screws and lockwashers.
3.) Position the panel away from the chassis and remove harness connector P1 from the EIA board. If the Printer Port option is installed, also remove harness connector P2 from the Printer board.
4.) Replace in reverse order.

Note: Be careful not to reverse P1 and P2.

3. TERMINAL, MODEM AND PRINTER I/O CONNECTOR PIN ASSIGNMENTS

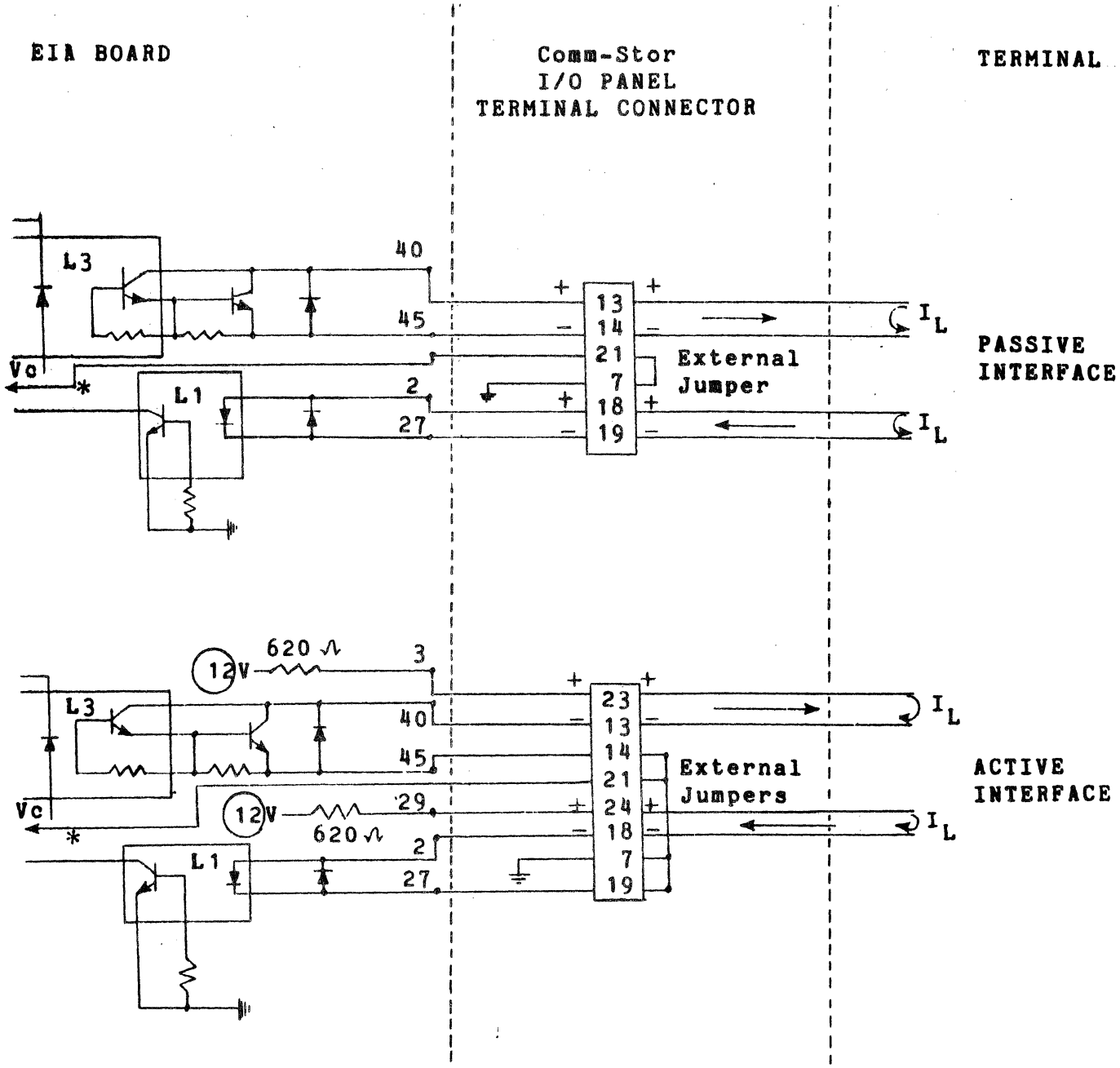
The terminal, modem and printer I/O pin assignments are listed in Figure #7-3.

PIN	DESCRIPTION	TERMINAL PORT		MODEM PORT		PRINTER PORT	
		USED	DIRECTION	USED	DIRECTION	USED	DIRECTION
1	Chassis Ground	X	-	X	-	X	-
2	Transmitted Data	X	in	X	out		
3	Received Data	X	out	X	in	X	out
4	Request to Send	X	in	X	out		
5	Clear to Send	X	out	X	in		
6	Data Set Ready	X	out	X	in	X	out
7	Circuit Ground	X	-	X	-	X	-
8	Carrier Detect	X	out	X	in	X	out
11	Secondary Request to Send	X	in	X	out	X	in
12	Secondary Carrier Detect	X	out	X	in		
20	Data Terminal Ready	X	in	X	out	X	in
22	Ring Indicator	X	out	X	in		

Notes: 1. Direction refers to signal direction with respect to Comm-Stor at each port, e.g., transmitted data is out of Comm-Stor on Pin 2 at the modem port.
2. Unused pins in the terminal EIA connector are assigned for usage with the Current Loop option.

EIA RS-232-C INTERFACE CONNECTIONS

FIGURE #7-3



* Ground: Current Loop ON
Open: Current Loop OFF

FIGURE #7-4 CURRENT LOOP CONNECTIONS (20 mA)

RS-232-C ELECTRICAL SPECIFICATIONS AND VOLTAGE LEVELS

. Driver output logic levels with 3K to 7K load	15 volts $> V_{OH} >$ 5 volts -5 volts $> V_{OL} >$ -15 volts
. Driver output voltage with open circuit	$\lvert V_o \rvert < 25$ volts
. Driver output impedance with power off	$Z_o > 300$ ohms
. Output short circuit current	$\lvert I_o \rvert < .5$ amps
. Driver slew rate	$\frac{dv}{dt} < 30$ Volts / usec
. Receiver input impedance	7K ohms $> R_{in} >$ 3K ohms
. Receiver input voltage	$\pm$ 25 volts compatible with driver
. Receiver output with open circuit input	mark
. Receiver output with 300 ohms to ground on input	mark
. Receiver output with +3 volt input	space
. Receiver output with -3 volt input	mark

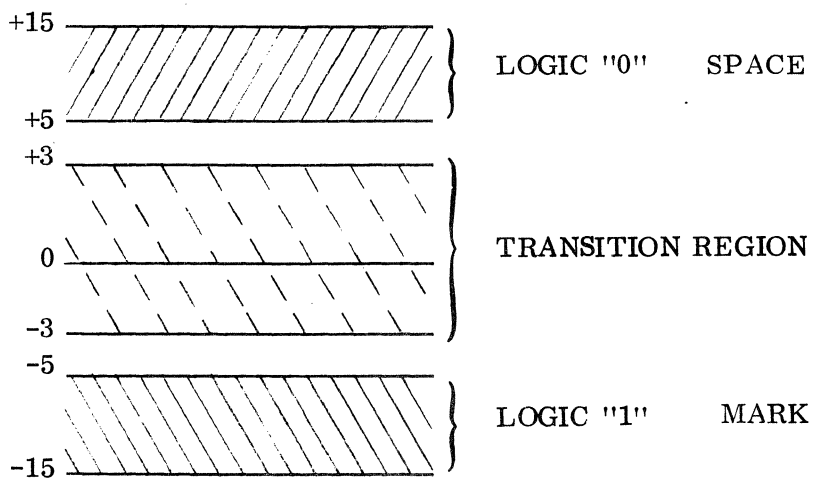


FIGURE #7-5

Current Loop connections for an active or passive interface are listed in Figure #7-4.

4. RS-232-C INTERFACE SPECIFICATIONS

This section will define the operation of the RS-232-C interface control lines. A summary of the RS-232-C electrical specification is given in Figure #7-5.

Modem port signals describe all the control lines which interface to modems.

Terminal port signals describe all control lines which interface to terminals.

Printer port signals may be referenced to terminal port signals as these ports are identical pin-for-pin. However, they may not be used interchangeably.

A. Modem Port Signals

1.) Chassis Ground - Pin 1

2.) Transmitted Data - Pin 2
Serial data output from Comm-Stor.

3.) Receive Data - Pin 3
Serial data input from modem.

4.) Request to Send - Pin 4
This signal is an output from Comm-Stor. During half duplex operation, Request to Send is active when Comm-Stor is in the Send mode or when data from the terminal port is being passed through the system to the modem port.

5.) Clear to Send - Pin 5
This input signal from the modem must be active for Comm-Stor to transmit data in half duplex operation.

6.) Data Set Ready - Pin 6
This input signal from the modem must be positive in order for Comm-Stor to transfer data. If this signal is not provided by the modem, Comm-Stor can be configured (Configuration Parameter #60) to operate in its absence.

7.) Signal Ground - Pin 7
This pin is connected to the chassis at one common ground point.

8.) Carrier Detect - Pin 8
This input signal from the modem indicates the presence of Carrier on the line. Whenever this signal is present, the CARRIER light will be illuminated.

9.) Secondary Request to Send - Pin 11
This signal is used by 202 type modems for circuit assurance. Comm-Stor will hold this line positive for half duplex operation when secondary channel is in use.

10.) Secondary Carrier Detect - Pin 12
This signal is used by 202 type modems for circuit assurance and transmission control. Comm-Stor can be configured to utilize this signal as follows (Configuration Parameter #46):

a. Ignore the signal.
b. Reset Comm-Stor upon loss of the signal.
c. Stop sending data upon loss of the signal.

Comm-Stor will continue to send a maximum of two characters after this signal drops out.

11.) Data Terminal Ready - Pin 20

Comm-Stor will normally keep this line positive whenever power is on. Additionally, the system will hold this line down for 300 ms to perform an Auto Disconnect operation. This occurs after failure to establish a proper telephone connection (Carrier Detect, Data Set Ready) 20 seconds after a ring indicator signal has occurred or after the inactivity timer times out.

12.) Ring Indicator - Pin 22

Signal from the modem which indicates the presence of Ring Signal on the line.

B. Terminal Port Signals

Comm-Stor is designed to operate with full duplex terminals only.

1.) Chassis Ground - Pin 1

2.) Transmitted Data - Pin 2

Serial data input from the terminal.

3.) Received Data - Pin 3

Serial data output from Comm-Stor.

4.) Request to Send - Pin 4

Comm-Stor ignores this input signal from the terminal.

5.) Clear to Send - Pin 5

Comm-Stor normally asserts this signal unless configured to deassert the signal (Parameter #39).

6.) Data Set Ready - Pin 6

Comm-Stor normally asserts this signal unless configured to deassert this signal (Parameter #39).

7.) Signal Ground - Pin 7

This pin is connected to the chassis at one common ground point.

8.) Carrier Detect - Pin 8

Comm-Stor normally asserts this signal unless configured to deassert the signal (Parameter #39).

9.) Secondary Request to Send - Pin 11

This signal is ignored by Comm-Stor.

10.) Secondary Carrier Detect - Pin 12

This signal is normally deasserted unless it is configured to be asserted (Parameter #39).

11.) Data Terminal Ready

Comm-Stor normally does not check for this signal unless configured to do so (Parameter #40).

12.) Ring Indicator

This signal is normally deasserted unless it is configured to be asserted (Parameter #39).

5. Comm-Stor RAM MEMORY BOARDS

A. General

The RAM Memory Boards allow Read/Write memory of Comm-Stor to be expanded. In Comm-Stor and Comm-Stor II systems the standard 1K of RAM memory may be expanded to 5K. In Comm-Stor III systems the standard 5K of RAM memory may be expanded to 13K. In Comm-Stor IV systems, memory may be expanded to 40K.

There are three boards used in RAM memory expansion:

A. 4K Expanded RAM Board
B. 16K Expanded RAM Board
C. 24K Expanded RAM Board

The 16K RAM board has replaced the 4K board in Comm-Stor production. The Comm-Stor II/III addressing scheme allows only 12K of the available 16K on the board to be addressed. Therefore, a full Comm-Stor II/III System will contain a 16K RAM board with one vacant row of IC's. Comm-Stor IV can use the entire 16K on this board.

B. 4K Expanded RAM Board

The 4K Expanded RAM Board is made up of 32 1024X1 Random Access Memory devices. Refer to Figure #7-6 for a block diagram of the 4K Expanded RAM Board. Drawing 1030T6140 illustrates the board component

4K EXPANDED RAM BOARD

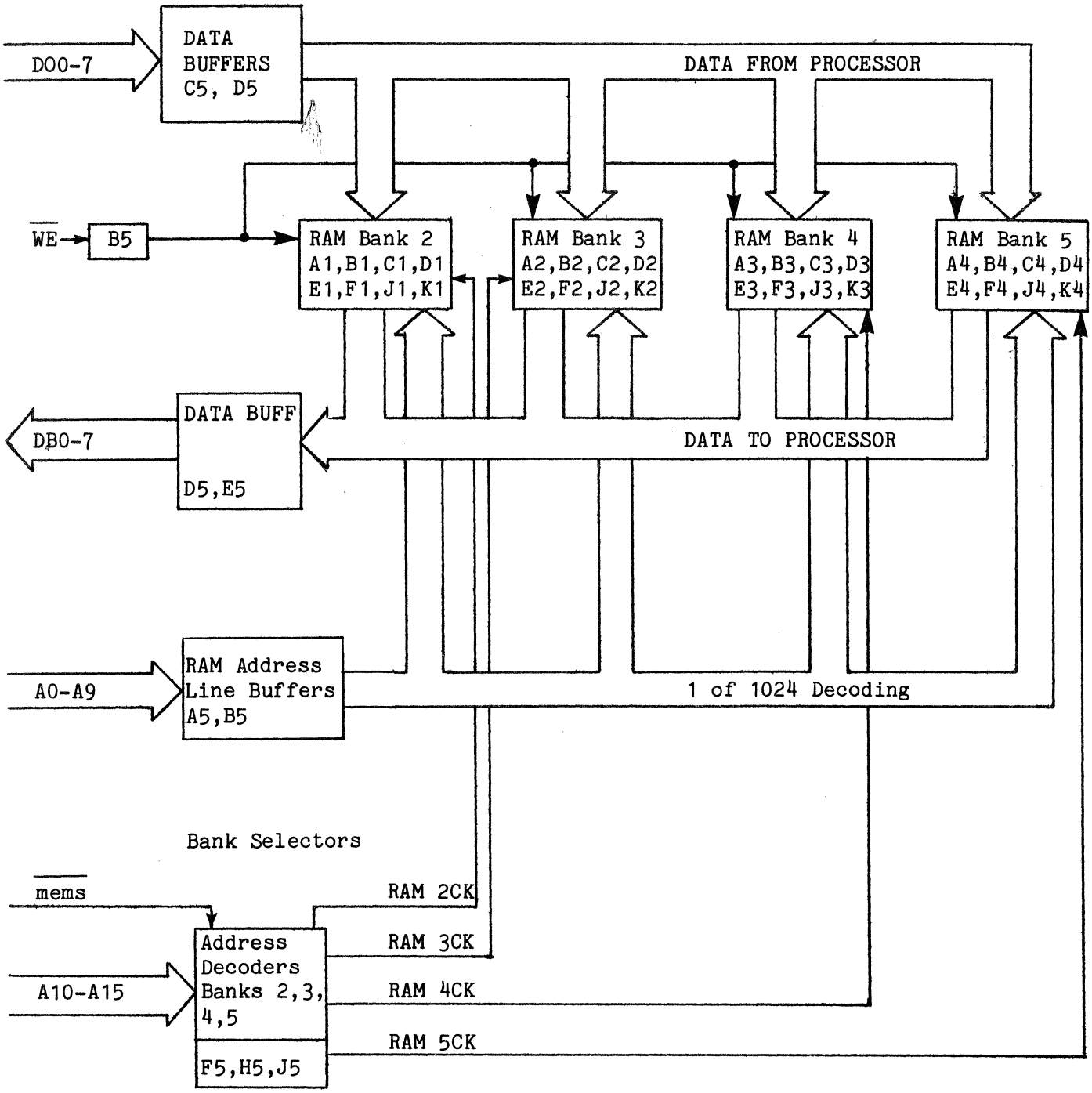
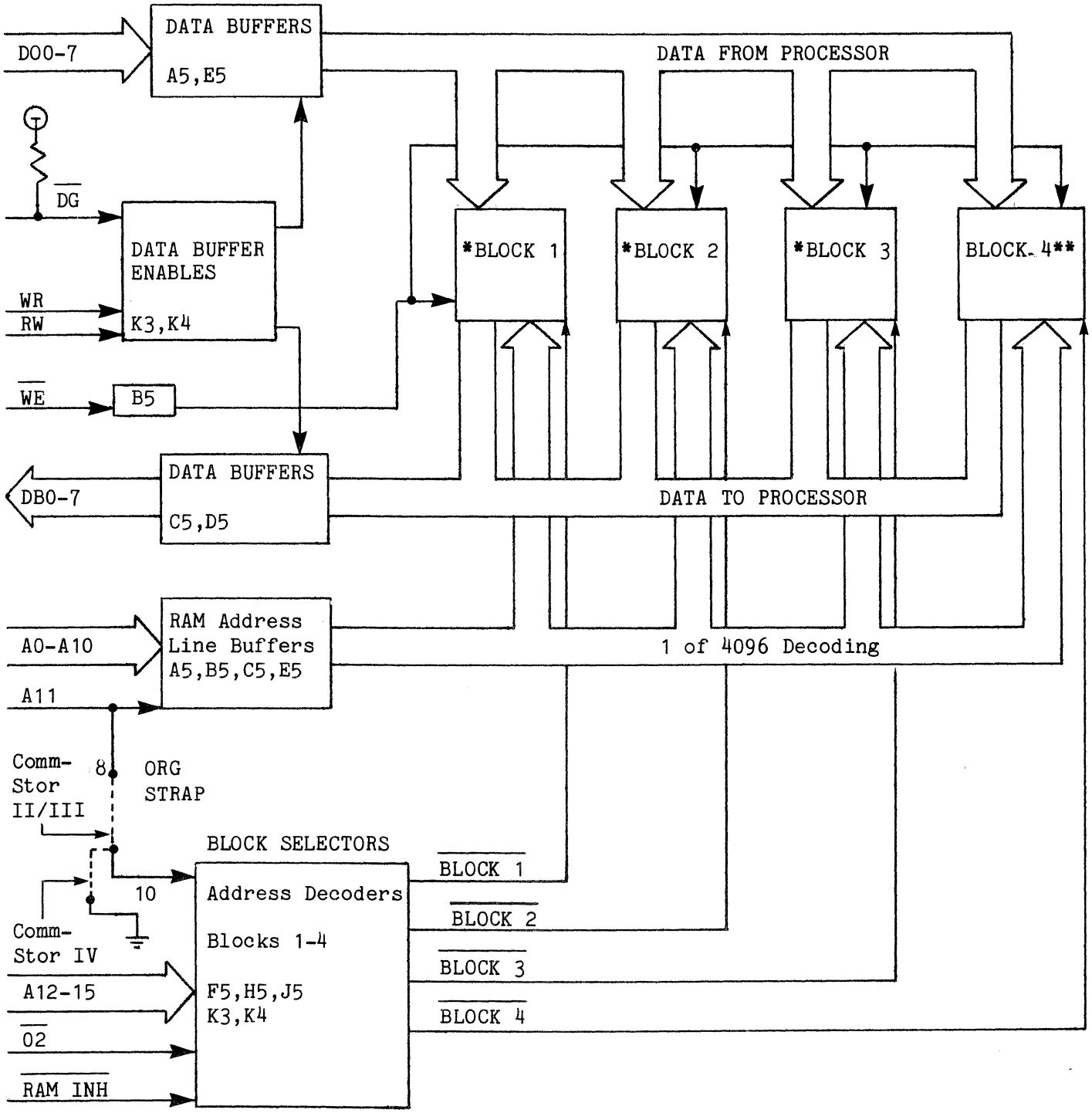


FIGURE #7-6

16K EXPANDED RAM BOARD



* Block 1 = Banks 2-5
Block 2 = Banks 6-9
Block 3 = Banks 10-13
Block 4 = Banks 14-17

** Unused in Comm-Stor II/III.

FIGURE #7-7

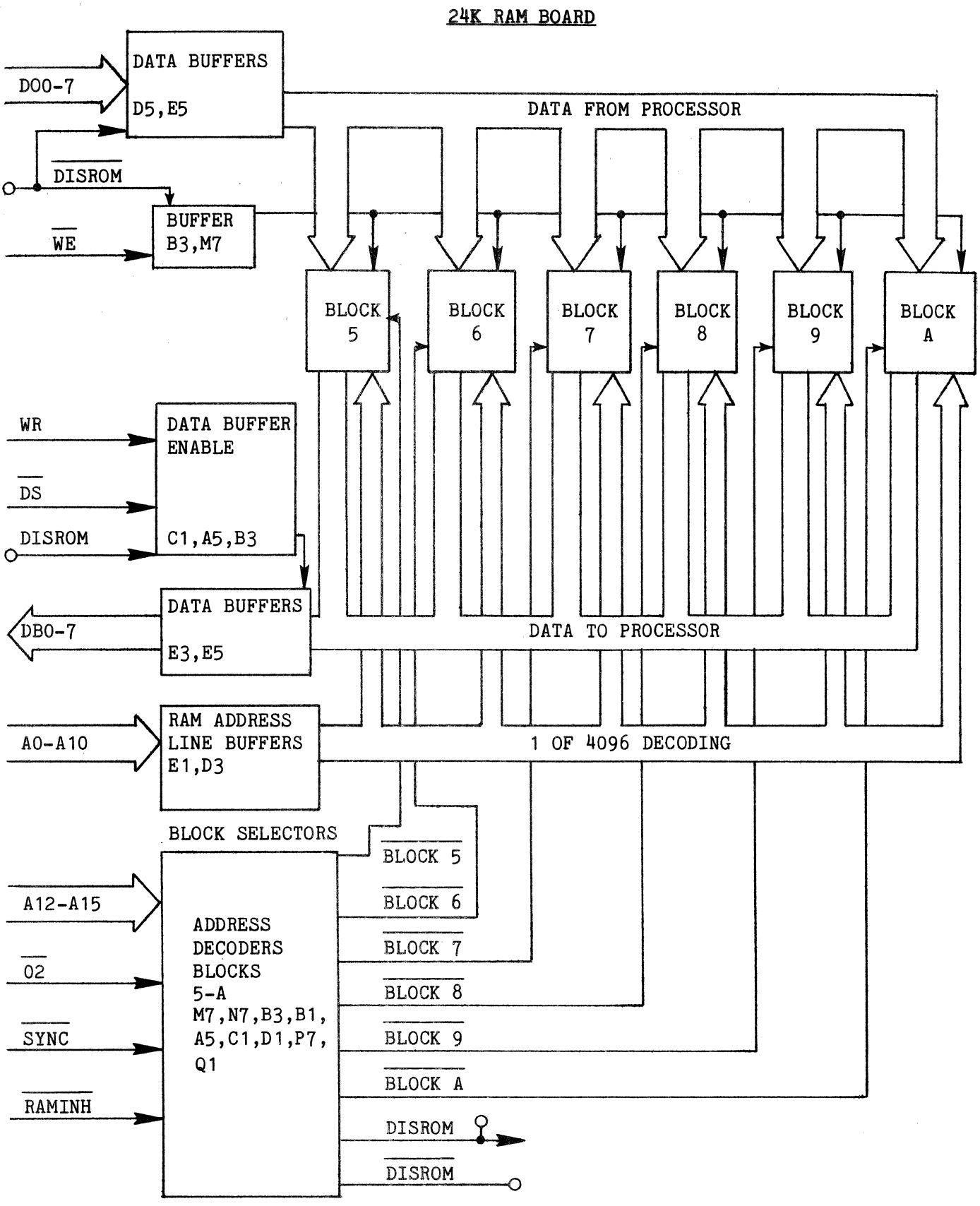

24K RAM BOARD
DATA BUFFERS
D5,E5
D00-7
DATA FROM PROCESSOR
DISROM
BUFFER
B3,M7
WE
BLOCK 5
BLOCK 6
BLOCK 7
BLOCK 8
BLOCK 9
BLOCK A
WR
DATA BUFFER ENABLE
DS
DISROM
C1,A5,B3
DATA BUFFERS
DB0-7
E3,E5
DATA TO PROCESSOR
A0-A10
RAM ADDRESS LINE BUFFERS
E1,D3
1 OF 4096 DECODING
BLOCK SELECTORS
A12-A15
02
SYNC
RAMINH
ADDRESS DECODERS BLOCKS 5-A
M7,N7,B3,B1, A5,C1,D1,P7, Q1
BLOCK 5
BLOCK 6
BLOCK 7
BLOCK 8
BLOCK 9
BLOCK A
DISROM
DISROM

FIGURE #7-8

ORG STRAPPED TO 8
(Comm-Stor II/III)

	A15	A14	A13	A12	A11	$\overline{\text{RAM INIT}}$	$\overline{02}$
$\overline{\text{BLOCK 1}}$	0	0	0	0	1	1	0
$\overline{\text{BLOCK 2}}$	0	0	0	1	1	1	0
$\overline{\text{BLOCK 3}}$	0	0	1	0	1	1	0
$\overline{\text{BLOCK 4}}$	0	0	1	1	1	1	0

ORG STRAPPED TO 10
(Comm-Stor IV)

	A15	A15	A13	A12	$\overline{\text{RAM INIT}}$	$\overline{02}$
$\overline{\text{BLOCK 1}}$	0	0	0	1	1	0
$\overline{\text{BLOCK 2}}$	0	0	1	0	1	0
$\overline{\text{BLOCK 3}}$	0	0	1	1	1	0
$\overline{\text{BLOCK 4}}$	0	1	0	0	1	0

TABLE #7-1

layout. The schematic for this board is found in Chapter 11.

The data out and data in busses and address lines A0-A9 are buffered and presented directly to each memory device.

Bank selection is accomplished by decoding address lines A10-A15 into four RAM CK lines (RAM 2CK - 5CK). Output 4 of F5 is low whenever an address of 0800 - 17FF is present on the buss and mems is low. This signal enables the second half of F5 which develops the RAM CK outputs. The RAM CK leads will be low (enabling the selected bank) according to Table #7-2 below.

	A11	A10	F5 PIN 4
RAM CK2	1	0	0
RAM CK3	1	1	0
RAM CK4	0	0	0
RAM CK5	0	1	0

TABLE #7-2

Data is read from the device when $\overline{WE}$ is high and written when $\overline{WE}$ is low.

C. 16K Expanded RAM Board

The 16K Expanded RAM Board is made up of 32 4096 X 1 Random Access Memory devices. Refer to Figure #7-7 for a block diagram of the 16K Expanded RAM Board. Drawing 1030T5009 illustrates the board component layout. The schematic for this board is found in Chapter 11 of the Comm-Stor Service Manual.

The data out and data in busses and address lines A0 - A11 are buffered and presented directly to each memory device.

Block selection is accomplished by decoding Address Lines A12-A15 into four $\overline{Block}$ Lines ($\overline{Block}$ 1 - $\overline{Block}$ 4). The $\overline{Block}$ leads will be low (enabling the selected block) according to Table #7-1.

The ORG STRAP selects the starting address for RAM memory. The strap is set to 8 for Comm-Stor II/III, and 10 for Comm-Stor IV. Refer to Table #7-1.

Data is read from the device when $\overline{WE}$ is high and written when $\overline{WE}$ is low.

D. 24K RAM Board

The 24K RAM board consists of 48 4096 x 1 Random Access Memory devices. Refer to Figure #7-8 for a block diagram of the 24K RAM Board. Drawing 1030A5023 illustrates the board component layout. The schematic for this board is found in Chapter 11.

The data out and data in busses and address lines A0 - A11 are buffered and presented directly to each memory device.

Block selection is accomplished by decoding Address Lines A12-A15 into six $\overline{Block}$ Lines ($\overline{Block}$ 5 - $\overline{Block}$ A). The $\overline{Block}$ lines will be low (enabling the selected block) according to Table #7-3.

Data is read from the device when $\overline{WE}$ is high and written when $\overline{WE}$ is low.

Part of the RAM on this board (6000 - AFFF) is at the same address as the system firmware. The board determines if the processor is fetching an OP code from the ROM II board ($\overline{SYNC}$ low) and disables the RAM memory. If the processor is not fetching an OP code ($\overline{SYNC}$ high) and the address range is between 6000 - AFFF, the RAM is enabled and the ROM II board is disabled (DISROM goes high).

E. Expanded RAM Memory Allocation

Comm-Stor, Comm-Stor II and Comm-Stor III use the Expanded RAM option for several different operations. The individual Comm-Stor systems that use the option and the methods of handling different operations are defined below:

Comm-Stor Operation

A. 3740 Format Option
B. Expanded Forms Option

Comm-Stor II, III Operation

A. 3740 Format Option
B. Expanded Forms Option
C. Terminal - Modem Buffering
D. Variable Length File - "RESTORE" Operation

Memory Requirements of Specific Operations (Refer to the Expanded RAM Memory Allocation Chart on page 7-24.)

3740 Format Option

The 3740 Format Option uses all of the 4K Expanded RAM option. Forms larger than 1024 characters should not be loaded when the 3740 format is loaded. In Comm-Stor II, III units, terminal and modem buffering (Parameter #144) must be reconfigured for zero buffer space or an error message will be displayed when an attempt is made to load the "3740 Format" disk.

Expanded Forms Operations

Forms larger than 1024 characters will occupy part of the 4K Expanded RAM. This will result in loss of the 3740 Format. In Comm-Stor II, III units, a disk "RESTORE" operation always results in a loss of the form. Also, if Comm-Stor is configured for terminal-modem buffering, the amount of memory allocated for buffering must be subtracted from 4K memory which normally could be used for Expanded Forms Operations.

Terminal-Modem Port Buffering (Comm-Stor II, III only)

If Comm-Stor II, III is configured (Parameter #144) for buffering, the 3740 Format Option cannot be used unless the system is reconfigured or refreshed. Expanded Forms operations will be limited by the amount of memory allocated for buffering.

Example: If the total amount of memory allocated for buffering is 3K, 1K of the Expanded RAM will be available for Forms.

The RAM memory in Comm-Stor IV is available for user BASIC programs and buffering.

RESTORE Operation - (Comm-Stor II,III only)

A disk "RESTORE" operation will always result in the loss of the 3740 Format or the current form loaded in memory. The system will not buffer terminal data when a RESTORE operation is performed. Modem buffering is limited to 1K characters during a RESTORE operation.

	A15	A14	A13	A12	$\overline{02}$	$\overline{\text{RAMINH}}$	$\overline{\text{SYNC}}$
$\overline{\text{BLOCK 5}}$	0	1	0	1	0	1	1
$\overline{\text{BLOCK 6}}$	0	1	1	0	0	1	1
$\overline{\text{BLOCK 7}}$	0	1	1	1	0	1	1
$\overline{\text{BLOCK 8}}$	1	0	0	0	0	1	1
$\overline{\text{BLOCK 9}}$	1	0	0	1	0	1	1
$\overline{\text{BLOCK A}}$	1	0	1	0	0	1	1

TABLE #7-3

ITEM NO.	QUANTITY REQUIRED	UNIT MEAS	PART NUMBER	DESCRIPTION	ELECT REF DESIG	LINE REV
1	1		1030B5018	PWB-16K RAM MEMORY/PRINTER PORT		
2	REF		1030B5017	SCHEMATIC-16K RAM MEMORY		
3	REF		1030B5016	SCHEMATIC-PRINTER PORT		
4	REF		1030T5009	PWB REF ASSY-16K RAM MEMORY/ PRINTER PORT		
5	3		105C04105	CAP-TANT-22UF, 15V	C10, 12, 14	
6	4		120C01044	CAP-DISC-GP-470PF	C18-21	
7	38		120C03010	CAP-DISC-LV-.05UF, 10V	C11,22-29,38-45,55-63,65-76	A1
8	4		120C03032	CAP-DISC-LV-.033UF, 25V	C1 3, 15-17	
9	2		200C01001	DIODE-1N4153	CR1, 2	
10	1		108E01001	BUSS BAR		
11	1		100J11408	CONN-50POS HDR, STR	J2	
12	5		100R02089	RESISTOR-4.7K, $\frac{1}{4}$W, 5%	R1-4, 7	A1
13	1		100U16060	INT. CKT-74148	P3	
14	5		100U16072	INT CKT-8T97	A5, B5, C5, D5, E5	
15	1		100U18002	INT CKT UART TR1402A	M1	
16	2		100U18003	INT CKT-1488	M2, N2	
17	1		100U18004	INT CKT-1489	P4	
18	1		100U18048	INT CKT-K1135A	K1	C
19	1		100U19007	INT CKT-74LS08	K3	B
20	1		100U19006	INT CKT-74LS04	L2	
21	1		100U19008	INT CKT-74LS10	F5	
22	1		100U19011	INT CKT-74LS71	P2	
23	1		100U19013	INT CKT-74LS86	J5	
24	2		100U19015	INT CKT-74LS138	L3, L4	
25	1		100U19016	INT CKT-74LS139	H5	
26	1		100U19023	INT CKT-74LS174	K2	
27	4		100U19028	INT CKT-74LS257	M3, M4, N3, N4	

C REV
2 SHEET

PREP BY K. Weisser 3/31/78 DATE
CHECKED T. Shibuya 4.6.78 DATE
APPD S Conrad 9/78 DATE
APPD DATE

CODE IDENT

TITLE
PWB ASSY
16K RAM MEMORY-4K EXT
PRINTER PORT

SYKES DATATRONICS

NOTES:
1. REF ASSY IS AT REV C
SEE ITEM 4
2.

LATEST EO

SIZE A

PL 1030A5014
SHEET 1 OF 2

REV C

FIGURE #7-9(A)

ITEM NO	QUANTITY REQUIRED	UNIT MEAS	PART NUMBER	DESCRIPTION	ELECT REF DESIG	LINE REV
28	1		100U19032	INT CKT-74LS32	K4	
29	32		101U16004	SOCKET-18 POS	XA1-4, XB1-4, XC1-4	C
					XD1-4, XE1-4, XF1-4	
					XH1-4, XJ1-4	
30	1		101U16006	SOCKET-40 POS	XM1	
31	3		103E02002	POST, MOD II, .025 SQ		A1
32						C
33	8		100U18047	INT CKT, RAM, STATIC, 4K x 1	A1 - J1	A1
34	1		100J02008	CONN ASSY, SHUNT, 2 POS		A1
35	2		100R02067	RESISTOR, 560 Ω, 1/4 W, 5%	R5, 6	A1
36	1		100R02073	RESISTOR, 1.0 K, 1/4 W, 5%	R8	B
37	1		120C01012	CAPACITOR, DISC, GP, 22 pf	C77	B
38	1		1030B6916	INSULATOR, 18 POS DIP		C

SYKES DATATRONICS

CODE IDENT	SIZE	PL 1030A5014 SHEET 2	REV
	A		C

FIGURE #7-9(B)

ITEM NO	QUANTITY REQUIRED	UNIT MEAS	PART NUMBER	DESCRIPTION	ELECT REF DESIG	LINE REV
25	1		100U19011	INT. CKT. - 74LS74	N3	
26	1		100U19013	" - 74LS86	H5	
27	2		100U19015	" - 74LS138	K3,L3	
28	1		100U19016	" - 74LS139	F5	
29	1		100U19023	" - 74LS174	K2	
30	4		100U19028	INT. CKT. - 74LS257	K4,L4,M4,N4	
31						F
32	1		120C03032	CAPACITOR, DISC - .033 μF, 25 V	C42	E
33	1		1030B6916	INSULATOR, 18 PIN DIP		F

CANCEL

SYKES DATATRONICS	CODE IDENT	SIZE	PL 1030A6179 SHEET 2	REV
		A		G

FIGURE #7-10

ITEM NO.	QUANTITY REQUIRED	UNIT MEAS	PART NUMBER	DESCRIPTION	ELECT REF DESIG	LINE REV
1	1		1030B6182	PWB-RAM MEMORY/PRINTER PORT		
2	REF		1030T6140	REF. ASSY-RAM MEMORY/PRINTER PORT		
3	1		100J11408	CONN-50 POS, HDR, STR	J2	
4	32		101J16003	SOCKET-16 POS	XA1-4, XB1-4, XC1-4	
					XD1-4, XE1-4, XF1-4	
					XH1-4, XJ1-4	
6	1		101J16006	SOCKET-40POS	XM1	
7	060	IN	600W05005	WIRE, BUSS, 22GA.		
8	REF		1030B6180	SCHEMATIC - RAM MEMORY		
9	REF		1030B6181	SCHEMATIC - PRINTER PORT		
10	3		105C04105	CAP-TANT-22UF, 15V	C1, C3, C4	
11	4		120C01044	CAP-DISC-G.P.-470PF	C5-C8	
12	33		120C03010	CAP-DISC-L.V.-.05UF, 10V	C2, C9-32, 34-41	F
13	2		200C01001	DIODE-1N4153	CR1-CR2	
14	2		100R02089	RESISTOR-4.7K, 1/4W, ±5%	R1, R2	
15	1		100U16060	INT. CKT. - 74148	P3	
16	5		100U16072	- 8T97	A5, B5, C5, D5, E5	D
17	1		100U18002	- UART TR1402A	M1	
18	2		100U18003	- 1488	M2, N2	
19	1		100U18004	- 1489	P4	
20	1		100U18048	- KI135A	K1	F
21	32		100U18023	- 91L02B/2102AL	A1-4, B1-4, C1-4,	B
					D1-4, E1-4, F1-4	
					H1-4, J1-4	
22	1		100U19004	- 74LS00	L2	
23	1		100U19006	- 74LS04	M3	
24	1		100U19008	INT. CKT. - 74LS10	U5	

CANCEL

	REV 5	DRAWN [illegible] 4/77 DATE
	SHEET 2	CHECKED TS 9-77 DATE
CODE IDENT		APPD DATE
		APPD DATE

TITLE: PWB ASSY RAM MEMORY/ PRINTER PORT

SYKES DATATRONICS

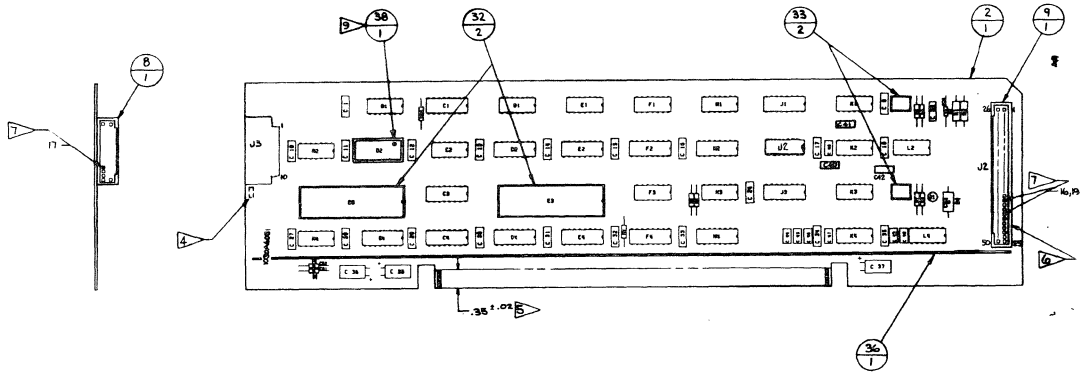
NOTES:
1. REF ASSY IS AT REV E
2. FOR REWORK INSTRUCTIONS SEE 1030T6140

LATEST EO	SIZE	PL 1030A6179	REV
963	A	SHEET 1 OF 2	G

FIGURE #7-11

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. MOUNT CONN J2 WITH INSPECTION SLOTS FACING OUT BOARD
7. REMOVE CONNECTOR PINS 1 & 19 FROM J2, ITEM 9, & PIN 7 FROM CONNECTOR J3, ITEM 8
8. FOR REWORK INSTRUCTIONS SEE ZONE A-7 THIS SHEET
9. APPLY ITEM 38 UNDER CASE OF B2



	ITEM	PART #	DESCRIPTION	QTY
	40			
	39			
	38	1030B6916	INSULATOR, 18 PIN DIP	1
C50	37	120C03032	CAPACITOR-.033MF, 25V	1
	36	108E0100I	BUSS BAR	1
	35			
	34			
	33	101U16009	6 POS-SKT	2
	32	101U16006	40 POS-SKT	2
C3,C4,D2,D4,E2,E4	31	100U19028	INT CKT-74LS257	6
F2,H2,J1,J3	30	100U19024	74LS175	4
B4	29	100U19023	74LS174	1
F4,H4	28	100U19015	74LS138	2
B1,E1	27	100U19011	74LS74	2
F1	26	100U19007	74LS08	1
D1,H3	25	100U19006	74LS04	2
C2,F3,H1	24	100U19004	74LS00	3
B2	23	100U18048	K1135A	1
J2	22	100U16072	ST97	1
K2,K4,L4	21	100U18004	1489	3
K1,K3,L2	20	100U18003	1488	3
B3,E3	19	100U18002	UART TR1402A	2
C1	18	100U16060	74148	1
A4	17	100U16056	INT CKT-7416	1
A2	16	103R07021	RES P/G -150Ω	1
R1,2	15	100R03068	RES-620Ω, 1/2W, 5%	2
R8	14	100R02061	330Ω, 1/4W, 5%	1
R3,4,9,10	13	100R02059	4.7K, 1/4W, 5%	4
R5,7	12	100R02121	100K, 1/4W, 5%	2
R6	11	100R02097	RES-10K, 1/4W, 5%	1
Q1	10	202Q01801	TRST-2N6531	1
J2	9	100J11408	CONN-50POS,HDR,STRT. IN	1
J3	8	100J02014	CONN-20POS,HDR,RT ANG	1
CR4	7	200C02001	DIODE-1N2070	1
CR1-3	6	200C01001	DIODE-1N4153	3
CL9-15,24,27-35,39	5	120C03010	CAP-DISC-.05μF, 10V	22
C40-49	4	120C01044	CAP, DISC-470 PF	10
C36,37,38	3	105C04105	CAP, TANT-2.2μF, 15V	3
	2	1030B6053	PWB-EIA INTFC	1
	1	1030B6052	SCHEMATIC-EIA INTFC	REF

ROCHESTER, NEW YORK

TITLE: PWB ASSY EIA INTFC

SIZE: D | DWG NO. 1030A6051 | REV F | SHEET 1 OF 1

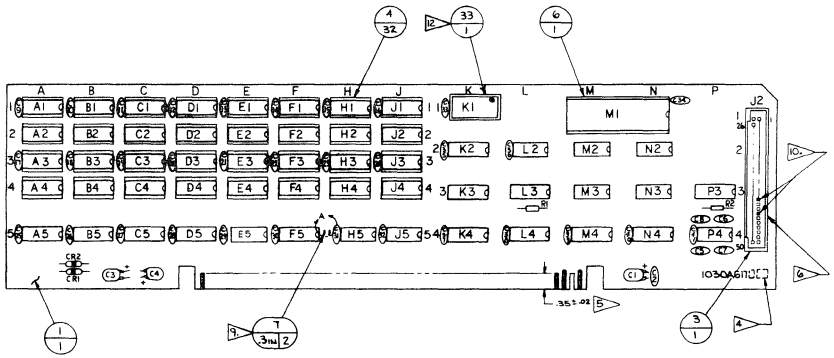
FIGURE #7-12

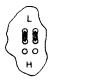
NOTES:

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .58
4. REVISION LETTER (LAST DIGIT OF ASSY NUMBER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. MOUNT CONN. J2 WITH INSPECTION SLOTS FACING OUT BOARD
7. THIS ASSEMBLY DRAWING IS FOR REFERENCE ONLY
8. THERE ARE NO INDIVIDUAL ASSEMBLY DRAWINGS FOR EACH OPTION. SEE P/L & SCHEMATIC LISTING BELOW

OPTION IDENT.	PARTS LIST	SCHEMATIC
RAM MEMORY/PRINTER PORT	1030A6179	1030B6180 1030B6181
RAM MEMORY	1030A6174	1030B6180
PRINTER PORT	1030A6175	1030B6181

9. UNLESS OTHERWISE SPECIFIED ADD JUMPER WIRE (ITEM 30) SEE DETAIL A
10. REMOVE CONNECTOR PINS 16 & 19 FROM J2, ITEM 3
11. REWORK INSTRUCTIONS FOR 1030A6178 & 1030A6179 ONLY
12. APPLY ITEM 33 UNDER CASE OF K1





DETAIL ENLARGED
LOCATED BETWEEN F5-H5
DETAIL A

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK			
TITLE: PWB REFERENCE ASSY RAM MEMORY/PRINTER PORT			
DWG SIZE: D	DWG NO.: 1030T6140 SHEET 1 OF 1	REV: F	

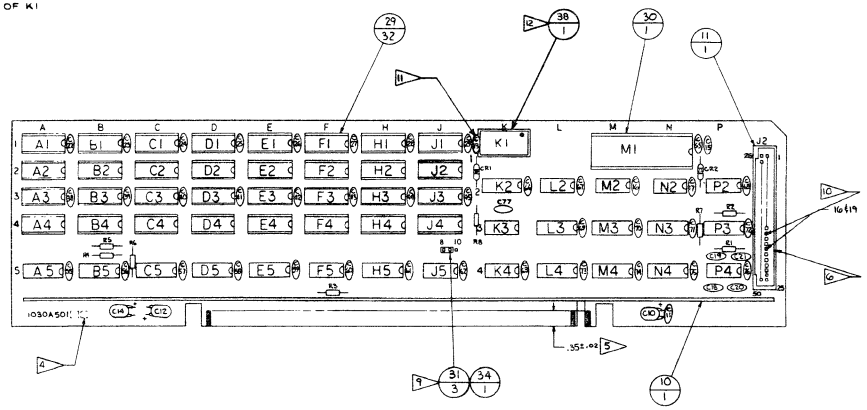
FIGURE #7-13

NOTES:

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .45
4. REVISION LETTER & LAST DIGIT OF ASSY NUMBER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION
6. MOUNT CONN. J2 WITH INSPECTION SLOTS FACING OUT BOARD
7. THIS ASSEMBLY DRAWING IS FOR REFERENCE ONLY
8. THERE ARE NO INDIVIDUAL ASSEMBLY DRAWINGS FOR EACH OPTION. SEE P/L & SCHEMATIC LISTING BELOW

OPTION IDENT.	PARTS LIST	SCHEMATIC
16K RAM MEMORY/PRINTER PORT	1030A5014	1030B5016 1030B5017
16K RAM MEMORY	1030A5013	1030B5017
PRINTER PORT	1030A5012	1030B5016

9. INSERT ITEM 34 OVER ITEM 31 IN LOCATION SHOWN, SEE SCHEMATIC 1030B5017 FOR ORG. STRAP SETTING (SHOWN STRAPPED ORG. 800)
10. REMOVE CONNECTOR PINS 16 & 19 FROM J2, ITEM 11
11. APPLY SLEEVING OVER LEADS OF C13 TO PREVENT SHORTING TO CASE OF K1 AS REQUIRED
12. APPLY ITEM 38 UNDER CASE OF K1

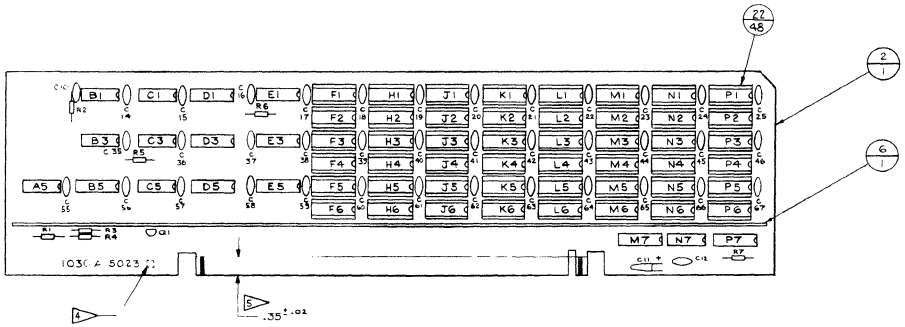


SYKES DATATRONICS, INC. ROCHESTER, NEW YORK			
TITLE: PWB REFERENCE ASSY 16K RAM MEMORY/PRINTER PORT			
DWG SIZE: D	DWG NO.: 1030T5009	SHEET 1 OF 1	REV: C

FIGURE #7-14

NOTES

1. REFER TO ENG STD ES102-02
2. SOLDER PER ES102-03
3. COMPONENT HEIGHT NOT TO EXCEED .45
4. REVISION LETTER PER ES102-02
5. PRINTED CONTACTS SHALL BE FREE OF SOLDER TO LINE OF DEMARCATION



DESIGNATION	ITEM	PART #	DESCRIPTION	QTY
XF1-XF6, XH1-XH6 XJ1-XJ6, XK1-XK6, XL1-XL6 XM1-XM6, XN1-XN6, XP1-XP6	22	101U18004	SOCKET-18 PCS	48
B3	21	100U19032	INT CKT 74LS32	1
C3	20	29	74LS260	1
B5, P7	19	15	74LS138	2
N7	18	13	74LS86	1
C5	17	11	74LS74	1
A5	16	09	74LS20	1
B1	15	07	74LS08	1
C1	14	06	74LS04	1
D1	13	100U19001	74LS131	1
D3, D5, E1, E3, E5, M7	12	100U16072	INT CKT 8T97	6
R1, R3, R5, R6	11	100R02089	RESISTOR, 4.7K, 1/4W, 5%	4
R2	10	100R02073	RESISTOR, 1K 1/4W 5%	1
R4	9	100R02036	RESISTOR, 332, 1/4W, 5%	1
R7	8	100R02033	RESISTOR, 22 Ω, 1/4W, 5%	1
Q1	7	202Q01001	TRANSISTOR, MPS653	1
	6	0BE01001	BUSS BAR	1
C11	5	105C04105	CAP-TANT-22 UF, 5 V	1
C12, C14-25, C35-48, C55-67	4	120C03010	CAP-DISC-LV, 0.05UF, 50V	35
C10	3	120C01007	CAP-DISC-GP, 10 PF	1
	2	1030B5025	PWB-24K RAM MEMORY	1
	1	1030B5024	SCHEMATIC-24K RAM MEM	REF

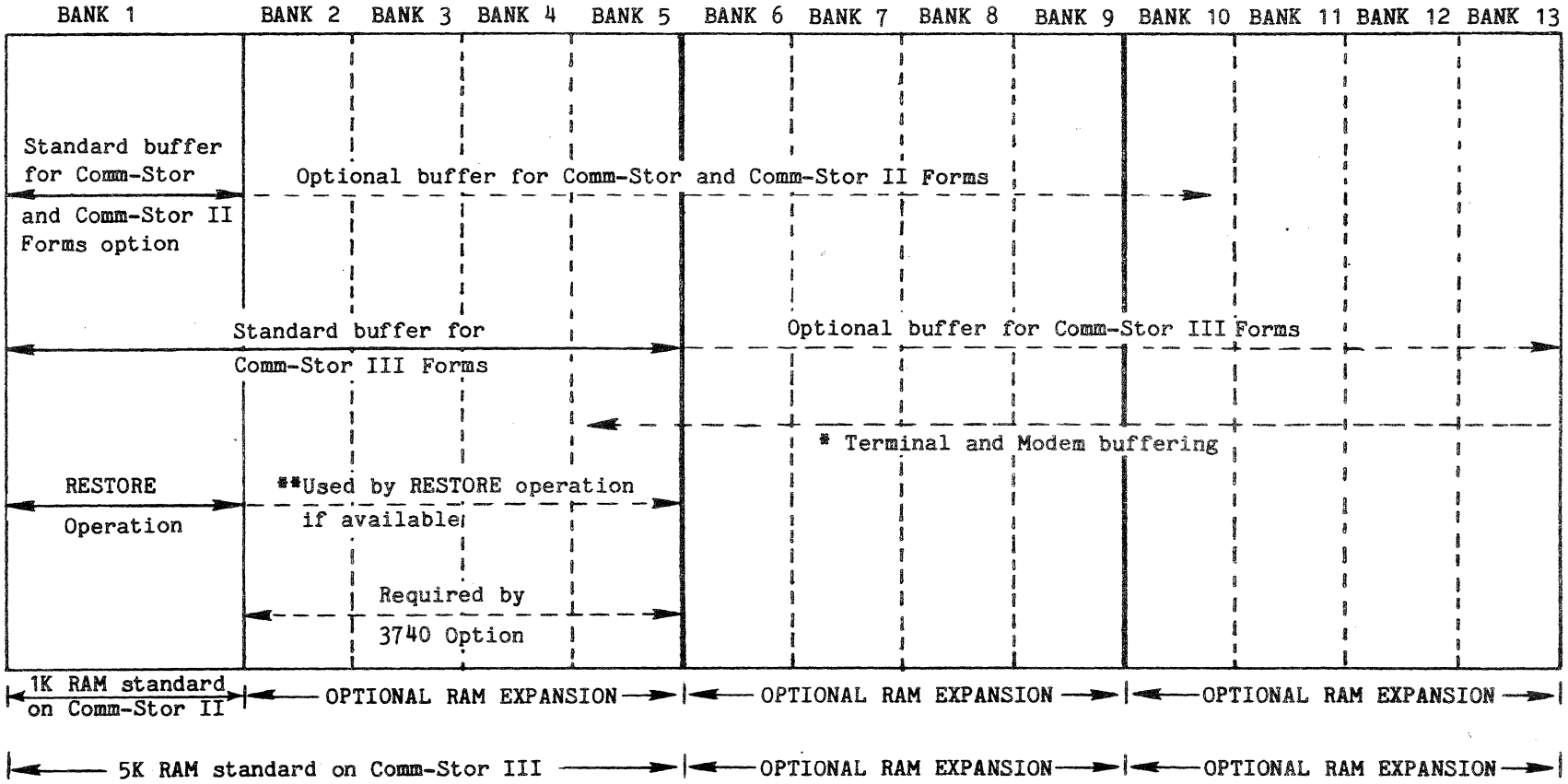
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: PWB ASS'Y 24K RAM MEMORY

DWG SIZE: D | DWG NO.: 1030A5023 | SHEET 1 OF 1 | REV: A1

FIGURE #7-15

Comm-Stor II, III - EXPANDED RAM MEMORY ALLOCATION



* Terminal and Modem buffering will reduce the amount of RAM available for the Forms Options Terminal and/or modem buffering is assigned starting with the highest Bank and working down. The combined maximum is 4K which may be divided between the terminal and modem in any combination of 1K increments.

**If additional RAM is available, the RESTORE command will automatically use BANKS 2, 3 and 4. It will also use BANK 5 if BANK 5 is not assigned as the modem buffer area.

CHAPTER 8

TROUBLE SHOOTING AND USER DIAGNOSTIC GUIDE

CONTENTS PAGE

TROUBLE SHOOTING AND USER DIAGNOSTIC GUIDE

If operational difficulties are experienced with a Comm-Stor unit, peripheral devices such as a terminal, modem, and printer should be checked with respect to the area of difficulty. Also, a check of Comm-Stor's Configuration program parameters should be made and changed if required. The parameters should then be rechecked after the unit has been off for several hours.

If difficulties are encountered during data transfer to or from a diskette, other diskettes should be tried and a check should be made of diskette handling procedures (refer to Chapter 9).

1. USER DIAGNOSTIC DESCRIPTION

An effective Comm-Stor system diagnostic is available from Sykes. The User Diagnostic (Sykes part number 1030A6198, Rev. D) consists of a special diagnostic program diskette and a 3-port EIA connector plug. The test program is automatically loaded from the diskette into Comm-Stor's memory when the test is performed. In the first half of the test interval, tests are performed on Comm-Stor's memory, Disk Drive, and other internal system devices.

In the second half of the test, the 3-port EIA connector plug is installed on the back of Comm-Stor. Comm-Stor can then test its own terminal, modem and printer ports.

All test indications are displayed on the front panel LEDS, allowing the tests to operate independent of the terminal. (Note: The User Diagnostic will not run on Comm-Stor IV systems.)

2. USER DIAGNOSTIC TESTS

Test A - LED/Switch Test
Test B - Internal Tests: Memory, Disk Read/Write
Test C - Terminal and Modem Port Tests
Test D - Terminal Current Loop Test
Test E - Printer Port Test
Test M - RAM Memory Test Run
Test V - Drive/Disk Verify Test with terminal
Test CM - CMOS/Volatility Test

3. BASIC TROUBLE SHOOTING PROCEDURE

To simplify troubleshooting, begin all troubleshooting procedures by loading or attempting to load the User Diagnostic diskette (section 4 below).

Because of the complicated interconnection of Comm-Stor circuitry, it is recommended that a spare set of modules be used to swap/verify the operation of questionable areas as described in the User Diagnostic Procedure.

If the unit is completely dead, or will not load and execute the User Diagnostic Program, refer to Checklist #1 (page 8-14).

If the unit passes all of the tests in the User Diagnostic Procedure but other difficulties are still experienced, refer to Checklist #2 - "Other Types of Difficulties" (page 8-15).

4. USER DIAGNOSTIC PROCEDURE

If a Comm-Stor malfunction prevents reading of the User Diagnostic diskette, the READY light will blink. In certain cases when the incorrect test sequence is used or the switch settings are incorrect, the STATUS light will blink.

The diagnostic test plug (8000 TEST PLUG, #1030A6193) has two switches, numbered "1" and "2", for simulating the peripheral cabling. Below is a top-view diagram of the test plug as mounted on the rear panel of Comm-Stor.

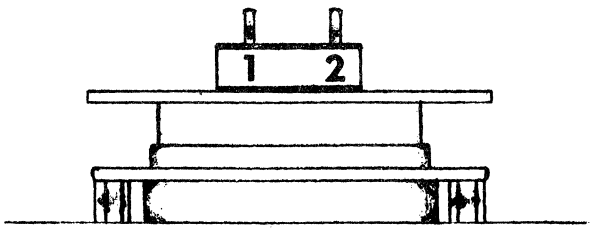


FIGURE #8-1

A. Test A - LED/Binary Mode and Baud Rate Switch Tests

1.) Set all Baud Rate switches on the Comm-Stor unit to zero and Binary Mode switch to EXIT.

2.) Power OFF the Comm-Stor unit.

3.) Open the drive(1) door.

4.) Power ON the Comm-Stor unit.

5.) Load a Refresh diskette into the drive (1); depress the RESTART button.

6.) Load the User Diagnostic diskette into the drive (1); depress the RESTART BUTTON.

7.) LED Test:

The following pattern/information is displayed immediately:

a. All the LEDS are lighted (one second).

b. BUSY (1) and READY (1) are lighted (one second).

c. The revision level of the User Diagnostic program is displayed (one second). Table #8-1 gives the revision level equivalents for the display. Note that revision level A is indicated by all LEDS off.

d. Walking lights: each LED is lit independently and in sequence (one second each).

e. Refer to Table #8-2 for failure interpretation.

8.) Switch Tests:

Note that the switch values are inclusively-ORed and the result then displayed.

a. At this time, the LED lights should be off (not lit).

b. When the Binary Mode switch is moved to ENTER, the STATUS light should be lit; when set to EXIT, it should be off (not lit).

LED DISPLAY - TEST A

BAUD SWITCH SETTING	LED DISPLAY				PROGRAM REVISION LEVEL
	STATUS	CARRIER	BUSY(1)	READY(1)	
0	OFF	OFF	OFF	OFF	A
1	OFF	OFF	OFF	ON	B
2	OFF	OFF	ON	OFF	C
3	OFF	OFF	ON	ON	D
4	OFF	ON	OFF	OFF	E
5	OFF	ON	OFF	ON	F
6	OFF	ON	ON	OFF	G
7	OFF	ON	ON	ON	H
8	ON	OFF	OFF	OFF	I
9	ON	OFF	OFF	ON	J
-	ON	OFF	ON	OFF	K
-	ON	OFF	ON	ON	L
-	ON	ON	OFF	OFF	M
-	ON	ON	OFF	ON	N
-	ON	ON	ON	OFF	O
-	ON	ON	ON	ON	P

TABLE #8-1

FAILURE INTERPRETATION

TEST FAILURE	PROBABLE CAUSES
LED TEST	Defective LED Defective EIA board (LED driver circuit).
Baud Switch	Defective BCD switch on MP-RAM board. Defective MP-RAM board (BCD switch multiplexer).
Binary Switch	Defective "ENTER/EXIT" switch on I/O panel. Defective EIA board.

TABLE #8-2

c. Move the PRINTER baud switch, if equipped, through its settings of zero to nine (be sure that the other baud switches are set to zero). Examine the LEDs at each setting and compare the values displayed with Table #8-1 (each baud switch value should generate a corresponding LED display). Return PRINTER switch to zero and follow the same procedure for the TERM and MODEM baud switches.

d. Refer to Table #8-2 for failure interpretation.

B. Test B - Internal Tests: Memory/Disk

1.) Power OFF the Comm-Stor unit.

2.) Open the drive(1) door.

3.) Remove the diagnostic test plug or any cables from the rear panel.

4.) Power ON the Comm-Stor unit.

5.) Load a Refresh diskette into the drive(1); depress the RESTART button.

6.) Load the User Diagnostic diskette into the drive(1); depress the RESTART button.

7.) The program will immediately perform the visual LED test; the operator may perform the remaining Switch Test of Test A, or go directly to step 8 below.

8.) Set the MODEM switch in accordance with the system's configuration; refer to Table #8-3.

9.) Open and close the drive (1) door. The program will begin to execute Test B.

* Comm-Stor will currently only test the initial 4K of the expanded RAM.

** Comm-Stor II and Comm-Stor III systems must always specify YES in this column.

10.) Wait for Test B to be completed: all the LED lights wiil blink in unison.

11.) Dual Drive 8200 System only: Upon completion of the Disk Test for drive 1, the READY (1) and BUSY (1) lights are blinked in unison. Remove the User Diagnostic diskette from the upper drive (1); insert it into the lower drive (2) and close the drive door. All LED lights will blink in unison.

12.) The test results are now available by opening and closing the drive (1) door (or drive (2) door in a dual drive system). The first set of results displayed in the LED lights corresponds with Table #8-4. When the door is opened and closed a second time, the LED light display corresponds with Table #8-5. Repeat the open-and-close door procedure to obtain the results of Tables #8-6, 8-7 and 8-8. Finally, open and close the door to complete the display of the test results. All the LED lights will blink in unison.

If at any time no further fault conditions exist for displaying, the test will terminate with all the LED lights blinking in unison. A fault table will be by-passed by the program if it contains no reportable results.

OPTIONS' SPECIFICATION

Extended User Table	Expanded RAM Option*	Forms**	MODEM Switch Setting
-	-	-	0
-	-	YES	1
-	YES	YES	2
-	YES	-	3
YES	-	-	4
YES	-	YES	5
YES	YES	YES	6
YES	YES	-	7

If one or more options are installed, set the switch accordingly.

TABLE #8-3

RAM FAULTS

Light	Interpretation	Probable Cause
READY	RAM Bank 0 Main Memory	MP-RAM board - ICs: A1,B1,C1, D1,A3,B3,C3,D3
BUSY	RAM Bank 1 Forms Memory	MP-RAM board - ICs: A2,B2,C2, D2,A4,B4,C4,D4
CARRIER or STATUS	RAM Banks 2,3, 4, or 5	Expanded RAM board

NOTE: If RAM faults are experienced in this test and the system has a terminal, perform Test M for more specific test results.

TABLE #8-4

CMOS-RAM FAULTS

Light	Interpretation	Probable Cause
READY	RAM Bank 10 Main Configuration Memory	MP-RAM board - ICs: E2,F3,K2, L1
BUSY	RAM Bank 10 Extended User Table	MP-RAM board - ICs: A5,B5,K2, L1

TABLE #8-5

ROM FAULTS

Light	Interpretation	Probable Cause
READY	Main Firmware	Defective ROM board

TABLE #8-6

DRIVE 1 FAULTS

Light	Interpretation	Probable Cause
READY or BUSY	Drive 1-Read	Defective Disk Drive Assy. or Disk Drive Control board (check calibration). Defective Disk Controller board, defective cable. Bad User Diagnostic diskette.
CARRIER or STATUS	Drive 1-Write	(same as above)

TABLE #8-7

DRIVE 2 FAULTS

Light	Interpretation	Probable Cause
READY or BUSY	Drive 1 - Read	Defective Disk Drive Assy. or Disk Drive Control board (check calibration). Defective Disk Controller board, defective cable. Bad User Diagnostic diskette.
CARRIER or STATUS	Drive 2 - Write	(same as above)

Note: To further verify disk drive operation, refer to Test V (page 8-12).

TABLE #8-8

C. **Test C - Terminal & Modem Ports Test**

1.) Power OFF the Comm-Stor unit.

2.) Open the drive (1) door.

3.) Mount the diagnostic test plug on the I/O Interface panel. Set switch 1 up (EIA) and switch 2 down (TERM).

4.) Power ON the Comm-Stor unit.

5.) Load a Refresh diskette into the drive (1); depress the RESTART button.

6.) Load the User Diagnostic diskette into the drive(1); depress the RESTART button.

7.) The program will immediately perform the visual LED test; the operator may perform the remaining Switch Test of Test A, or else go directly to step 8 below.

8.) Set the TERM and MODEM baud switches; refer to Tables #8-9 and #8-10. Set the PRINTER switch to zero (if the option is installed).

9.) Open and close the drive (1) door. The program will begin to execute Test C. (If Test D is being performed, it will now be executed.)

10.) Wait for the test to be completed; all LED lights will blink in unison.

11.) The test results are now available by opening and closing the drive (1) door. The first set of results displayed in the LED lights corresponds with Table #8-11. When the door is opened and closed a second time, the LED light display corresponds with Table #8-12. Repeat the open-and-close door procedure to obtain the results of Tables #8-13 and #8-14. Finally open and close the door to end the display of the test results. All the LED lights will blink in unison.

If at any point no further fault conditions exist for displaying, the test will be terminated with all the LED lights blinking in unison. A fault table will be by-passed by the program if it contains no reportable results.

If all recommended probable causes have been checked and the problem is still not isolated, replace the I/O Panel Assembly.

BAUD RATE SPECIFICATION

DESIRED BAUD RATE	TERM SWITCH SETTING
110	1
134	2
150	3
300	4
1200	5
2400	6
4800	7
7200	8
9600	9

This table specifies both the terminal and modem port baud rates. If the rates are different, run the test twice (once at each baud rate).

TABLE #8-9

CHARACTER STRUCTURE SPECIFICATION

DESIRED CHARACTER STRUCTURE	MODEM SWITCH SETTING
7 bits + even parity	0
7 bits + odd parity	1
7 bits without parity	2
8 bits + even parity	3
8 bits + odd parity	4
8 bits without parity	5

TABLE #8-10

TERMINAL RECEIVE/TRANSMIT FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSES
READY/ BUSY	Terminal cannot receive and/or transmit characters properly.	Defective EIA board - ICs: B2,E3,L2,K2,E2, E4
CARRIER	1. false indication of parity error. 2. terminal port cannot send Break. 3. terminal port does not respond to a Break.	Defective EIA board - ICs: E3,E2,E4
STATUS	(not used)	

TABLE #8-11

TERMINAL EIA CONTROL FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSES
Any light	Terminal port control faulty.	Defective EIA board - ICs: F4, H4,J3,H2,K3,L2, K4,K2,E4,E3

TABLE #8-12

MODEM RECEIVE/TRANSMIT FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSE
READY or BUSY	Modem cannot receive or transmit character properly.	Defective EIA board - ICs: B2,B3,K1,L4,D2, C4
CARRIER	1. false indication of parity error. 2. modem port cannot send a Break. 3. modem port does not respond to a Break.	Defective EIA board - ICs: B3,D2,C4
STATUS	When Comm-Stor is configured for direct path transmission, serial data from the modem through Comm-Stor to the terminal will be faulty.	Defective EIA board - ICs: F2,F3,F1,H3

TABLE #8-13

MODEM PORT CONTROL FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSE
Any light	Modem port control faulty.	Defective EIA board - ICs: F4, H4,J1,F2,L2,K1, K2,L4,K4,D2,C4

TABLE #8-14

D. **Test D - Terminal Port/Current Loop Test**

1.) Power OFF the Comm-Stor unit.

2.) Open the drive (1) door.

3.) Mount the diagnostic test plug on the I/O Interface panel and set switches 1 and 2 both down (CL and TERM).

4.) Follow the procedure in Test C, steps 4 through 11.

Note: The Current Loop Test will not run above 2400 baud.

E. **Test E - Printer Port Test**

1.) Power OFF the Comm-Stor unit.

2.) Open the drive (1) door.

3.) Mount the diagnostic test plug on the I/O Interface panel and set switches 1 and 2 both up (EIA and PRINTER).

4.) Power ON the Comm-Stor unit.

5.) Load a Refresh diskette into the drive (1); depress the RESTART button.

6.) Insert the User Diagnostic diskette into the drive (1) door; depress the RESTART button.

7.) The program will immediately perform the visual LED test; the operator may perform the remaining Switch Test of Test A, or else go directly to step 8 below.

8.) Set the TERM and MODEM switches; refer to Tables #8-9 and #8-10. Set the PRINTER switch to one.

9.) Open and close the drive (1) door. The program will execute Test E.

10.) Wait for Test E to be completed; all LED lights will blink in unison.

11.) The test results are now available by opening and closing the drive (1) door. The first set of results, displayed in the LED lights, correspond with Table #8-15. When the door is opened and closed a second time, the LED light display corresponds with Table #8-16. Finally, open and close the door to end the display of the test results. All the LED lights will blink in unison.

If at any point no further fault conditions exist for displaying, the test will be terminated with all the LED lights blinking in unison. A fault table will be by-passed by the program if it contains no reportable results.

If all recommended probable causes have been checked and the problem is still not isolated, replace the I/O Panel Assembly.

PRINTER RECEIVE/TRANSMIT FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSE
READY/ BUSY	Printer port cannot transmit character properly.	Printer Board ICs: K2, M1,M2,P4, L4,N4
CARRIER	Printer port may not be able to send a Break (i.e., long space) to the printer.	Printer Board ICs: M1, L4,N4
STATUS	The STATUS light is not used.	

TABLE #8-15

PRINTER EIA CONTROL FAULTS

LIGHT	INTERPRETATION	PROBABLE CAUSE
Any light	The printer port is faulty.	Printer Board ICs: K1, K2,K3,K4, L2,L3,L4, M1,M2,M3, M4,N2,N3, N4,P3,P4

TABLE #8-16

5. TERMINAL SUPPORTED TESTS

A. Test M - Special Memory Test

The purpose of this test is to provide qualified service personnel with a detailed analysis of the problem area in RAM memory (refer to Table #8-17). This test need only be run if a RAM failure existed during Test B in Table #8-4 or #8-5.

Procedure

1.) Connect a terminal to Comm-Stor's terminal port and set the terminal baud rate switch for the appropriate baud rate.

2.) Power ON the Comm-Stor unit.

3.) Insert the User Diagnostic diskette into drive (1) and close the drive door.

4.) Depress the RESTART button. Comm-Stor will automatically perform the LED test.

5.) Type the letter "M" on the terminal. After a slight delay, the letter M will be echoed back to the terminal and the following statement will be displayed:

FORMS

At this point, the user should type "Y" if the Forms option is installed; type an "N" if it is not. For Comm-Stor II and Comm-Stor III systems, the user must always type Y.

6.) The system will respond by printing the following message at the terminal:

EXP RAM

Respond with "Y" if the optional 4K RAM board is installed or "N" if it is not. The memory test will now execute beginning at Bank 00.

Test Results

1.) The following table will be displayed at the terminal:

GLOBAL W/R TEST

BANK	LOC	WRITE	READ
XX	XX	XX	XX
XX	XX	XX	XX

Where: BANK = hexadecimal RAM Bank number
LOC = hexadecimal memory address
WRITE = a 1 or a 0, indicating the logic level of each data bit written into RAM.
READ = a 1 or a 0, indicating the logic level of each data bit read from RAM.

The Global W/R test writes a unique value (an ascending number) into each memory location. After the entire memory is written into, each location is read and compared to the expected value. This test will detect addressing faults in both the address logic and in the memory chips themselves. Only the first error in each bank is reported.

2.) After completing the above test, Comm-Stor will print GLOB PAT and begin execution. This test writes a unique pattern into memory. After the entire memory is written into, it is read back and a comparison is made. The test is repeated 7 times with a different pattern each time. All errors are stored in a table and printed at the end of the test. This test will detect pattern sensitivity and addressing faults.

3.) After completing the Global Pattern Test, Comm-Stor will respond with the following message:

TYPE KEY

Striking any key will cause the system to perform the final test, W/R ALL V.

This performs a write/read test at each location, writing and reading four different hexadecimal values in the following sequence:

a. Write the value.
b. Read the location (up to 6 attempts) until the correct value is read.
c. If the correct value cannot be read, go back and write it again.
d. If it still cannot be read (6 attempts), repeat the cycle up to 6 times until the correct value is read.

USER DIAGNOSTIC MEMORY TEST

BANK	ADDRESS RANGE	FUNCTION	PCB	IC LOCATION 0 1 2 3 4 5 6 7
00	0020 - 03FF	STANDARD SYSTEM	MP-RAM	A1 A3 B1 B3 C1 C3 D1 D3
01	0400 - 07FF	1K FORMS	MP-RAM	A2 A4 B2 B4 C2 C4 D2 D4
02	0800 - 0BFF	4K RAM	4K RAM/PRINTER	A1 B1 C1 D1 E1 F1 H1 J1
03	0C00 - 0FFF	4K RAM	4K RAM/PRINTER	A2 B2 C2 D2 E2 F2 H2 J2
04	1000 - 13FF	4K RAM	4K RAM/PRINTER	A3 B3 C3 D3 E3 F3 H3 J3
05	1400 - 17FF	4K RAM	4K RAM/PRINTER	A4 B4 C4 D4 E4 F4 H4 J4
10	4000 - 40FF	STANDARD CMOS RAM	MP-RAM	F3 F3 F3 F3 E2 E2 E2 E2

1. Test M performs read/write test on all memory addresses. Note that the test program is loaded and executed in Bank 00. If Forms and EXP RAM questions are answered No, then Banks 01-05 are not tested.

2. Should an error occur, the following information will be displayed: the bank number, the first address which failed within that bank, the value written, and the value read. The bits within these values are organized as follows: 7654. 3210. Note that bit 7 is the MSB.

3. The first 4K of RAM may be tested only on the 16K RAM board. If a failure occurs, use the table above and change the device in Row 1 even if 2, 3, or 4 is indicated.

TABLE #8-17

When an error is found (even if it disappears during retry), no more locations in that bank are tested. The program advances to the next bank.

A typical error display is:

BANK	LOC	WRITE	READ		
02	0801	1100.0010	1100.0000	5	4

The number of write tries.

The number of read tries after the last write.

If the value cannot be read after 6 read-write cycles, an H (HARD ERROR) is displayed in place of the retry numbers.

At the completion of this test it will loop to the beginning.

B. **Test V - Drive/Disk Verify Test**

Description

This test provides qualified service personnel with a means of reading and verifying Track/Sector ID's and data CRC characters for every sector on the diskette.

The main purpose of this test is to check the Disk Drive and the Disk Drive electronics ability to read. If marginal problems exist, it is imperative that the test be run with several other diskettes or a known good diskette.

This test can also be used to check and verify diskettes. After the Disk Drive and electronics have been verified by successfully reading known good diskettes, the Verify Test can be used to verify questionable diskettes. Marginal or bad sectors are indicated by a display which indicates the track number (00-76), the sector number (01-26) and an "S" which indicates a Search Error or "CC" which indicates a CRC or data error.

Procedure

1.) Connect a terminal to Comm-Stor's terminal port and set the terminal baud rate switch for the appropriate baud rate.

2.) Power ON the Comm-Stor unit.

3.) Insert the User Diagnostic diskette into drive (1); close the door.

4.) Depress the RESTART button. Comm-Stor will automatically perform the LED test.

5.) Type the letter "V" on the terminal. After a slight delay, the letter V will be echoed back to the terminal and the following statement will be displayed:

INSERT IN

At this point, the System's ability to read a diskette can be tested by inserting a known good scratch diskette into Drive (1) or Drive (2). Conversly, marginal diskettes can be tested in known good systems using the same procedure.

After the scratch diskette has been inserted, the following message will be displayed on the terminal:

TRK

Answer this prompting message with the decimal number of the track to be tested (0-76), or answer it with an upper case "A" which designates all

tracks and sectors on the diskette.

Type a Carriage Return; the following prompting statement will be displayed on the terminal:

ID REVS (I.D. Revolutions)

Answer this prompting message with a "C". The "C" results in the same search retry sequence used by Comm-Stor in normal operation (up to 12 search retries). If marginal diskettes are being tested, a number 1 through 9 can be entered to limit the number of search retries.

Limiting the number of retries will greatly increase the probability of an error indication when the diskette or Disk Drive electronics are marginal. However, it should be noted that it is normal to have some search errors when ID REVS equals 1 or 2.

The test will begin automatically after a Carriage Return has been entered following the ID REVS number.

The following table will be displayed:

	TRK	SEC	TRK = track number
			SEC = sector number
RUN1			RUN1 = test cycle 1
	XX	YY ZZ	If Read errors occur, see below.

Test Results

Read errors are indicated in the above table by the track (XX) and sector (YY) numbers where the error occurred. The third column (ZZ) describes the type of error: S = "search" or "diskette" type I.D. error; CC = "CRC" or "Bad Read" type data error.

The beginning of each read cycle is indicated by the display RUN1, RUN2, RUN3, etc.

The test will run continuously until interrupted. Striking the space bar on the terminal stops the test and brings the program back to the TRK message. Striking the character "I" brings the program back to the INSERT IN message.

C. Test CM - CMOS Volatility Test

The CMOS Volatility Test will confirm the following:

1. The ability of CMOS memory devices to be addressed and read.
2. The ability of CMOS memory and associated devices to retain information when main power is disconnected.

The purpose of this test is to provide qualified service personnel with information pertaining to Comm-Stor's ability to retain all configurable parameters. This test should be run if the unit fails to configure properly or loses parameters after refresh.

Test Description

The test program will:

1.) Read the previous CMOS page 0 (and 1 if equipped) into RAM memory from the disk.

2.) Compare this image with the contents of page 0 (and 1 if equipped) beginning at location 4000.

3.) Report if the comparison was "Good" or "Bad" for page 0 (and 1 if equipped).

4.) Write the contents of both CMOS pages out to the disk.

Procedure

1.) Connect a terminal to Comm-Stor's terminal port and set the terminal baud rate switch for the appropriate rate.

2.) Power ON the Comm-Stor unit.

3.) Insert the User Diagnostic diskette into drive (1); close the drive door.

4.) Depress the RESTART button. Comm-Stor will automatically perform the LED test.

5.) Type the letter "C" on the terminal. After a slight delay, the letter C will be echoed back to the terminal and the following statement will be displayed:

EXT TABLE?

Type "Y" if the system contains the Extended User CMOS RAM option or "N" if it does not.

Test Results

1.) The test will now execute and print the following information:

PAGE 0 (GOOD) or (BAD)
EXT TABLE (GOOD) or (BAD)

2.) The test results should be ignored the first time the test is run. This enables the system to write the contents of CMOS memory onto the disk.

3.) When the question "EXT TABLE?" is asked again, the results will now be valid.

4.) Two test sequences are possible:

Sequence 1: Run the test.
Turn power OFF, wait 5 seconds, restore power.
Repeat the test immediately.

Sequence 1 will confirm the following hardware components:

a. The CMOS chips in their power down mode.
b. The CMOS support chips.
c. The on-board filter capacitor (which acts as a short term power source for the CMOS system).

Sequence 2: Run the test.
Turn power OFF.
Wait until the next day to repeat the test.

Sequence 2 will confirm the previous hardware as well as the operation of the battery on the mother board.

The CMOS test will not alter CMOS memory.

6. **CHECKLIST #1 - USER DIAGNOSTIC PROGRAM DOESN'T RUN**

A. Unit Completely Dead - cooling fan not spinning, drive motor not spinning, no illumination of power switch, no front panel LED illumination.

1.) On Comm-Stor units, reset the circuit breaker by pushing the orange button on the back panel. On Comm-Stor II and Comm-Stor III units, the circuit breaker is reset by pushing the power switch/circuit breaker button on the back panel.

2.) Check the power outlet for 115 VAC.

3.) Remove the top cover (see page 3-1). Check the power harness connectors to make sure they are mated together properly and there are no loose wires.

4.) Check the AC power connections at the power supply (red and gray wires).

5.) With the unit unplugged, check the continuity of the power switch, the circuit breaker, and the harnessing.

B. No Power Indication - no illumination of power switch no illumination of LEDS when system powered on or restarted.

1.) Check DC power supply voltages at base card edge connectors:

+5.0 VDC ±	@ pins 5,6
+24.0 VDC ±	@ pins 7,8
+12.0 VDC ±	@ pins 99,100
-12.0 VDC ±	@ pins 97,98
Ground	@ pins 1,2,66

If one or more of the DC voltages are not present at the base card edge connector, refer to Chapter 9 for power supply adjustment procedure.

2.) If one or more of the power supply voltages are low, the power supply may be defective; or a defective component on one of the circuit boards could be loading down a particular voltage. Swap/verify the power supply. Swap/verify the circuit boards one at a time.

C. No one-second illumination of LEDS when system restarted. No Head Load Solenoid activity when system restarted with Disk Inserted.

1.) Check DC voltages (see previous section B) at base card edge connector.

2.) Check battery voltage 3.5 VDC MINIMUM.

3.) Check battery connections.

4.) Check front panel LED harness connection at EIA board.

5.) If all the DC voltages appear to be normal, follow the sequence below:

a. Power-off, remove Disk Controller board, power-on. If LEDS come on, problem is in Disk Controller board or Disk Drive Assembly. Swap/verify these assemblies one at a time.

b. Power-off, remove Printer option board if installed, power on. If LEDS come on, problem is in Printer option board.

c. Power-off, swap/verify MP-RAM board.

d. Power-off, swap/verify ROM board, including Patch PROM on MP-RAM board.

e. Power-off, swap/verify base card.

D. LEDS light for one second and go off, but User Diagnostic Program does not load off the diskette.

1.) Check User Diagnostic diskette on another system.

2.) Check for drive motor rotation.

3.) Swap/verify drive ribbon wire cables.

4.) Swap out the Disk Drive Assembly and restart the test.

5.) Swap/verify the Disk Controller board.

6.) Swap/verify the remaining circuit boards one at a time.

7. CHECKLIST #2 - OTHER TYPES OF DIFFICULTIES

Note: This section only applies to units which have passed the User Diagnostic without failure.

A. System will not respond properly to certain keyboard commands.

1.) Using a Configuration diskette, display all parameters and check for valid configuration responses. Change invalid parameters if necessary and recheck. This can be done by "Refreshing" the unit. If over the course of time Configuration parameters change, check the battery voltage; if OK, replace MP-RAM board.

2.) Swap/verify ROM board and Patch PROM (K1 on MP-RAM board).

B. Unit does not respond with "Carriage Return", "Line Feed", "Asterisk" (*) when restarted.

1.) Terminal baud rate not set the same as terminal.

2.) Parity of terminal and Comm-Stor not set the same.

3.) System not Refreshed after MP-RAM board removal/replacement.

4.) Check Configuration parameters as described above in section A.

C. "Error-Diskette" Message

1.) Probable worn or damaged diskette. Check system with other diskettes.

2.) Check Disk Drive Assembly head-to-track alignment. (Refer to Chapter 9.)

3.) Swap/verify Disk Controller board.

D. "Error - Bad Read" Message

1.) Probable worn or damaged diskette. Check system with other diskettes.

2.) Check head-to-track alignment of system that wrote data on the diskette and the system which is reading diskette.

3.) Swap/verify Disk Controller board of system that wrote on diskette as well as system reading the diskette.

4.) Check read/write compatibility. Write (.E - file name) and then read (.D - file name) a diskette. If successful, attempt reading the same diskette on another system. Check FDD Head/Track alignment.

E. "Error-System" Message

1.) Caused by a User diskette with a bad directory.

2.) Swap/verify ROM board and Patch PROM.

3.) Swap/verify MP-RAM board.

4.) Swap/verify Disk Controller board.

5.) Swap/verify EIA board.

F. Erroneous data transfer between Comm-Stor and peripheral terminal, modem or printer.

1.) Check for proper baud rate adjustment of Comm-Stor and peripheral device.

2.) Check for proper parity adjustment of Comm-Stor and terminal.

3.) Swap/verify EIA board for terminal or modem data transfer problems.

4.) Swap/verify Printer board for Printer option data transfer problems.

5.) Swap/verify MP-RAM board if erroneous data transfer exists through <u>all</u> I/O ports.

CHAPTER 9

MAINTENANCE AND ALIGNMENT

CONTENTS

1. FDD MAINTENANCE PROCEDURES

A. General

Under normal circumstances preventative maintenance is not required on the FD 700. If severely dirty environments are encountered, an occasional cleaning of the drive may be performed to assure continued reliable performance.

If a drive malfunctions, it is recommended that it be inspected and cleaned as described below. Visual inspection is the first step in any maintenance operation. Always look for corrosion, dirt, wear,

INSPECTION AND MAINTENANCE PROCEDURES

UNIT	OBSERVE	CLEANING PROCEDURE
Read/Write Head	Oxide build up and scratches	Clean Read/Write Head ONLY IF NECESSARY
Stepper Motor Shaft and Carriage	Inspect for nicks and burrs	Clean off all dust, dirt, and excess lubricant
Belt	Frayed or weakened areas	
Mainframe	Inspect for loose screws, connectors, switches, etc.	Clean Main Frame
Read/Write Head	Check for proper alignment	

TABLE #9-1

binds, and loose connections. Noticing these items may save downtime later.

Inspection and maintenance operations are listed in Table #9-1. During normal maintenance, perform only those operations listed on the chart. Details on adjustments and service checks are found in the following section. Observe all safety procedures.

Cleanliness cannot be overemphasized in maintenance of the FDD. Do not lubricate the drive except as noted in the carriage assembly procedure. Oil will allow dust and dirt to accumulate. The read/write head should be cleaned, but only when signs of oxide build-up are present.

B. Inspect and Clean Read/Write/Erase Head (Figure #4-2)

1.) Remove AC power and let the motor come to a stop.

2.) Remove the top cover (page 3-1).

Note: Use a suitably bright and directional light during the following steps.

3.) Inspect head as follows (carriage must be fully retracted to Track 00):

CAUTION: DO NOT SMOKE WHILE INSPECTING. USE EXTREME CARE NOT TO DAMAGE THE HEAD.

4.) Inspect face of head for reddish-brown oxide deposits. Clean head only if deposits exist (see Step 5).

5.) Clean heads (only if required) as follows:

CAUTION: DO NOT SMOKE WHILE CLEANING. DO NOT TOUCH THE HEAD FACE WITH FINGERS. DO NOT LEAVE RESIDUE OR LINT ON THE HEAD FACE. TRAPPED RESIDUAL PARTICLES CAN RE-SULT IN IRREVERSIBLE DAMAGE TO THE HEAD AND/OR A SCORED DISKETTE.

a. If oxide deposits are found, use recommended brand/type lint-free cloth to lightly drybuff head face. Cleaning is completed when deposits are removed.

b. Dampen (do not soak) gauze with head cleaning solution and wipe head face if oxide deposits were not removed in Step a. Use dry gauze to lightly buff head face if deposits are not removed.

c. Install a new head carriage assembly if oxide deposits still exist.

2. FLOPPY DISK DRIVE ALIGNMENT PACKAGE OPTION

The FDD Alignment Package Options, Sykes part numbers 1030A6294 (Comm-Stor), 1030A5177 (Comm-Stor II/III) and 1030A5181 (Comm-Stor IV), consist of a CE Alignment Diskette (1030A3261), Drive Alignment Patch Prom (1030A6305 Comm-Stor, 1030A-6399 Comm-Stor II/III and 1030A6398 Comm-Stor IV) and Alignment Procedures (9991A-0064). This option allows for precise adjustment of three critical drive parameters.

1. Head/Track Alignment
2. Track 00/76 Switch Adjustment
3. Index/Sector Adjustment

A. System Preparation

1.) Remove the screw which holds the front panel to the chassis.

2.) From the bottom of the chassis, remove the six phillips head screws which hold the FDD assembly to the chassis.

3.) Without disconnecting the FDD cables, rotate the FDD on its side so the bottom and top of the FDD are accessible.

4.) On Comm-Stor, remove the MP-RAM Circuit board. Carefully remove the Patch Prom located at position K1 on the MP-RAM board and insert the Drive Alignment Patch Prom (1030A6305) in its place. Be careful not to bend

any pins when inserting the PROM and make certain that the PROM is in the same direction as the socket key indicates.

5.) On Comm-Stor II,III and IV remove the ROM II board. Carefully remove the Patch Prom from location K1 on the ROM II board and insert the Drive Alignment Patch Prom (1030A6399 for Comm-Stor II/III, or 1030A6398 for Comm-Stor IV) in its place. Be careful not to bend over any pins when inserting the Prom and be certain that the Prom is in the same direction as the socket key indicates.

6.) Connect a standard terminal to the terminal port.

B. **Alignment Procedure**

The following steps must be followed in sequence.

Head/Track Alignment and Track 00/76 Switch Adjustment

NOTE: The service terminals on the drive board must be jumpered together to align the drive.

1.) Slightly loosen the three stepper motor clamp screws.

2.) Rotate the Stepper Motor housing so that the wires are positioned at the bottom of the motor.

3.) Manually move the carriage assembly out until it makes contact with the stop collar.

4.) Connect a True R.M.S.A.C. Voltmeter or an Oscilloscope to TP1 on the Drive Control Circuit board.

5.) Power up the system. The four front panel LEDS should come on for one second and then go off.

6.) Load the CE Alignment diskette. The alignment diskette should be at room temperature for at least twenty minutes before alignment.

7.) Load the head by jumpering the black wire on the head load solenoid to ground.

8.) While observing the AC voltage at TP1, turn the stepper motor housing clockwise (from motor end) until no signal is seen. Turn the housing counterclockwise (in) until a maximum signal is observed at Track 00.

9.) Type a 1 on the terminal for Drive 1 calibration or a 2 for Drive 2 calibration. The Carriage Assembly should immediately move in.

10.) Again, while observing the AC voltage at TP1, very carefully peak the signal by slowly rotating the stepper motor housing.

Tighten the three stepper motor screws while observing TP1. Make certain the amplitude does not change.

NOTE: Do not power down the system until instructed to do so.

11.) While observing the voltage at TP1, press down slightly on the head load arm. The amplitude at TP1 should not change by more than 10%. If it does, the media is flying. This condition can cause Read/Write errors and must be corrected.

a. Check the head load bail adjustment (see service manual) and correct if necessary.
b. Inspect the pad and replace if worn beyond the point where the bail adjustment cannot be made correctly.
c. Inspect the pad for any ridges or excessive oxide build-up. If necessary, use a fine emery cloth and gently rub the surface of the pad to insure a flat surface.
d. Repeat procedure in step 11.

12.) Remove the head load jumper.

13.) Remove the CE Alignment diskette and load a scratch diskette. At this point, the head should automatically move to Track 02.

14.) The Track 00 switch will be adjusted at this time. Slightly loosen two mounting screws for the Track 00 switch.

15.) Connect an oscilloscope or voltmeter to TP 5 to determine the logic level of the Track 00 switch.

16.) Slide the switch inward to the carriage assembly and then back it out until the contacts just open. This transition will be indicated by a change in the logic level at TP 5 from a high to a low.

17.) Check the logic levels at TP 5 by performing the following sequence. It will be necessary to type an "O" for a STEP-OUT command and an I for a STEP-IN command. Refer to the table below to test the switch.

TRACK	COMMAND	LEVEL AT TP 5
Initial - 02		Low
- 01	Step-Out	High
- 00	Step-Out	High
- 01	Step-In	High
- 02	Step-In	Low
- 03	Step-In	Low

TABLE #9-2

18.) If the pattern in Step 17 is not observed, repeat Step 16 until the pattern is the same.

19.) Type an asterisk on the terminal (*). This should cause the head to move to Track 76. While observing carriage movement, type several I's and note the number of times the carriage steps in. The carriage should step in one track but not more than two tracks. If necessary, adjust the Track 76 switch by slightly loosening the two mounting screws and moving it in the appropriate direction. Adjustment of this switch should limit carriage movement inward beyond Track 76.

20.) Remove jumper across service terminals on drive board.

Index/Sector Adjustment

Note: Refer to FIGURE #9-1 to verify proper waveforms throughout the procedure.

1.) With power off, manually position the Carriage Assembly off Track 00.

2.) Remove any diskettes from the carrier and power up the unit. All four front panel LEDS should come on for one second and go off.

3.) Insert the CE alignment diskette.

4.) Load the head by jumpering the black wire on the head load solenoid to ground.

5.) Connect channel A to TP4 and trigger positive.

6.) Connect channel B to TP1 (data).

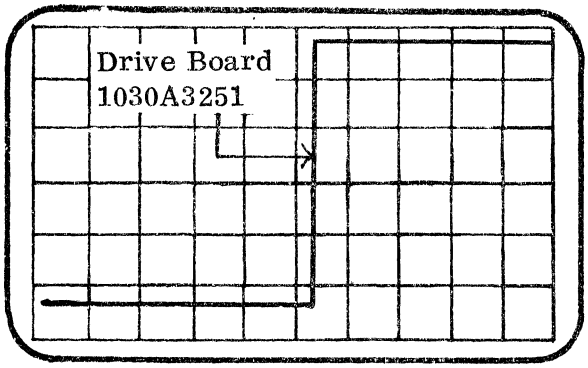
7.) Adjust trigger to obtain waveform.

8.) Adjust index sensor to cause data to be coincident with leading edge of Index pulse ($\pm$5 us). Sensor is adjusted by slightly loosening both screws and moving sensor from the bottom with a screwdriver blade.

9.) Open and close the front door several times. Ensure that the adjustment made in Step 8 above repeats within $\pm$ 25 us.

Procedures for the Remaining FDD Adjustments

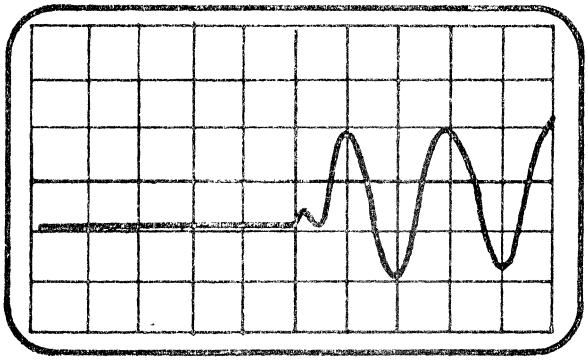
This section will describe the remaining less frequent and less critical adjustments.



CHANNEL A ONLY

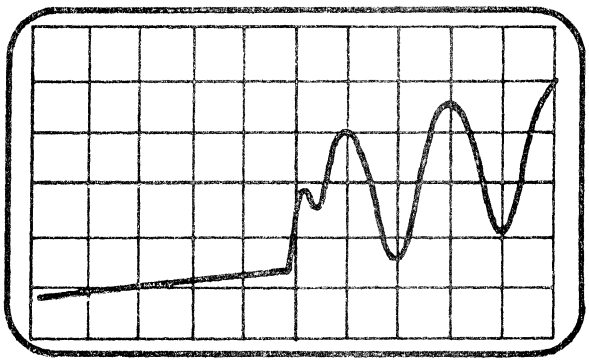
Vert. Sens.: 1V/div.

Adjust Trigger



CHANNEL B ONLY

Vert. Sens.: 1V/div.



DISPLAY (A + B)

Vert. Sens.: 1V/div.

Time Scale: 5 µS/div.

FIGURE #9-1 - OSCILLOSCOPE WAVEFORMS - INDEX/SECTOR ADJUSTMENT

Head Load Actuator Physical Adjustment

1.) With unit powered off, manually position carriage at Track 00 and power on the unit. The carriage should lock in at Track 00.

2.) Adjust the armature to pole clearance of the solenoid using a .035 inch diameter drill (#65 drill).

3.) Energize solenoid coil either using tester or manually grounding pin 15 on connector J2.

4.) Loosen bail screw on Head Load Bail.

5.) Using a .02 inch feeler gauge adjust bail so that Head Load Arm just touches the gauge. Tighten screw until just snug. Insure that the load arm is over bail when carriage is at Track 00.

6.) Step carriage to Track 76 and check that arm still just touches the gauge. (This will result in the correct Head Load Bail to Head Load Arm clearance.) Insure that load arm is over bail when carriage is at Track 76.

7.) Tighten Head Load Bail screw.

Head Load and Settle Timing

1.) Connect oscilloscope Channel A to trigger negative on J2-15 or Head Load (Black or gray wire on solenoid).

2.) Connect oscilloscope Channel B to TP1 on the PWB.

3.) Position head on Track 00 and load a scratch diskette.

4.) Place unit on its side with the head load solenoid down.

5.) Load the head. Data envelope should become stable at 90% amplitude 50 milliseconds from leading edge of Head Load signal.

6.) With Head Load activated, open door and remove diskette. Head should not load. If this is not met, continue the procedure.

7.) Bend the back stop on the solenoid slightly away from frame. Tighten screws.

8.) Repeat Step 5.

Diskette Carrier Adjustment

1.) Insert the Diskette Carrier Alignment Gauge between bottom surface of carrier and left guide rail on mainframe, 1" behind front door.

2.) Remove left door stop arm by carefully removing the E-ring from door stop pin and sliding it off. Loosen left door guide on main frame and adjust downward until carrier just squeezes the gauge. Tighten the door guide. Replace the door stop arm and E-ring.

3.) Repeat steps 1 and 2 on right side.

4.) Recheck both sides with the gauge and readjust if necessary.

Stop Collar Adjustment

1.) Step carriage to Track 00 (verify that Track 00 signal is active).

2.) Loosen screw on Stop Collar.

3.) Place the Stop Collar Alignment Gauge, .01 inch feeler gauge, between the stop and the back of the carriage.

4.) Slide the stop forward against the carriage and tighten the stop screw. Remove the gauge.

5.) Power-off the unit and move the carriage back against the stop.

6.) Power-on and insure that the carriage moves forward (in) to provide the required clearance (see Step 3). Check

the clearance with the gauge and repeat the alignment if necessary.

3. CONTROLLER ADJUSTMENTS

There are no controller adjustments.

4. POWER SUPPLY

The voltage adjustments should be within ±5% of the nominal voltage as shown in Figure #9-2. Refer to Chapter 5 for full power supply specifications.

5. CLEANING THE COOLING FAN FILTER

The Comm-Stor unit must not be operated without the filter as it provides protection against entry of air-borne dust and lint through the cooling fan. Routine cleaning of the filter is recommended as follows: every six months for a Comm-Stor unit operated in a "clean room" environment, or at three-month intervals if conditions are less ideal. A clogged filter will result in possible overheating of the unit. This may cause damage to the unit itself or any diskettes in the drive. Clean the filter as follows:

1.) Turn the Comm-Stor power OFF. (Indicator not illuminated).

2.) Remove the two screws which fasten the filter cover.

3.) Remove the filter cover and air filter.

4.) Vacuum clean the frame to remove any dust dislodged by filter removal. Also, vacuum clean the fan to remove all dirt accumulated on the fan blades. If possible, blow out the fan assembly from inside the unit with compressed air.

5.) Wash the filter in a detergent solution; then rinse and let air dry.

6.) Replace filter in reverse order.

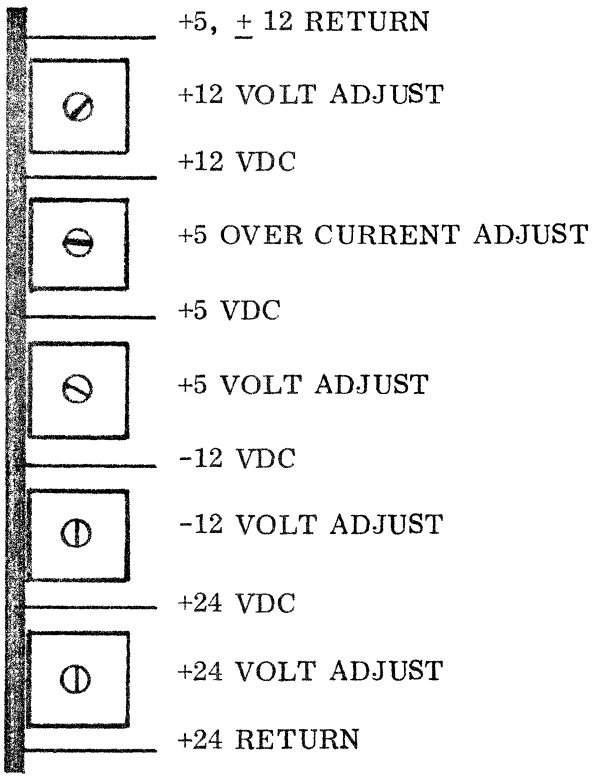


FIGURE #9-2

POWER SUPPLY VOLTAGE ADJUSTMENTS

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CHAPTER 10

DISK DRIVE SCHEMATIC DIAGRAMS

This chapter contains detailed schematic diagrams which describe the performance of the FD 700 Disk Drive.

NOTES

1. UNLESS OTHERWISE SPECIFIED :
   ALL RESISTOR VALUES ARE IN OHMS AND ARE 5%, 1/4 WATT
   ALL CAPACITOR VALUES ARE IN MICROFARADS
   ALL DIODES ARE IN4153

2 INTEGRATED CIRCUIT POWER DISTRIBUTION :

DESIGNATION	+5	GRD	+24 VF	LINEAR GRD
U1, U14, U15, U19, U29	16	8		
U2, U3, U8, U9, U10, U11, U16, U18, U20, U21, U22, U23, U24, U25, U28, U30, U17	14	7		
U4, U5, U12, U13, U26, U27	8	4		
U6, U7	4	11		
U31			11	6

3. CONNECTOR IDENTIFICATION :

DESIGNATION	FUNCTION	DESCRIPTION
J1	CONTROLLER INTFC I/O	RT ANGLE HEADER - 50 POS
J2	SENSOR / STEPPER	(2) RT ANGLE WAFERS - 10 POS
J3	HEAD	RT ANGLE WAFER - 6 POS
J4	FIRM SECTOR OPTION	RT ANGLE WAFER - 10 POS
J5	DC POWER	PWB FINGERS - 6 POS
J6	INDICATOR/SWITCH PANEL	RT ANGLE HEADER - 16 POS

4. TEST POINT IDENTIFICATION :

TP 1 - READ AMPLIFIER
TP 2 - ERASE
TP 3 - WRITE LEVEL
TP 4 - INDEX
TP 5 - OUT LIMIT
TP 6 - INDEX PULSE
TP 7 - LIMIT AMPLIFIER
TP 8 - LINEAR GRD
TP 9 - PEAK POSITION PULSE
TP 21 - IN LIMIT

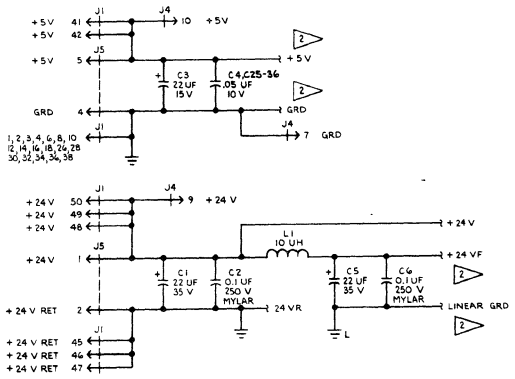
5. DRIVE SELECT JUMPER SEQUENCE :

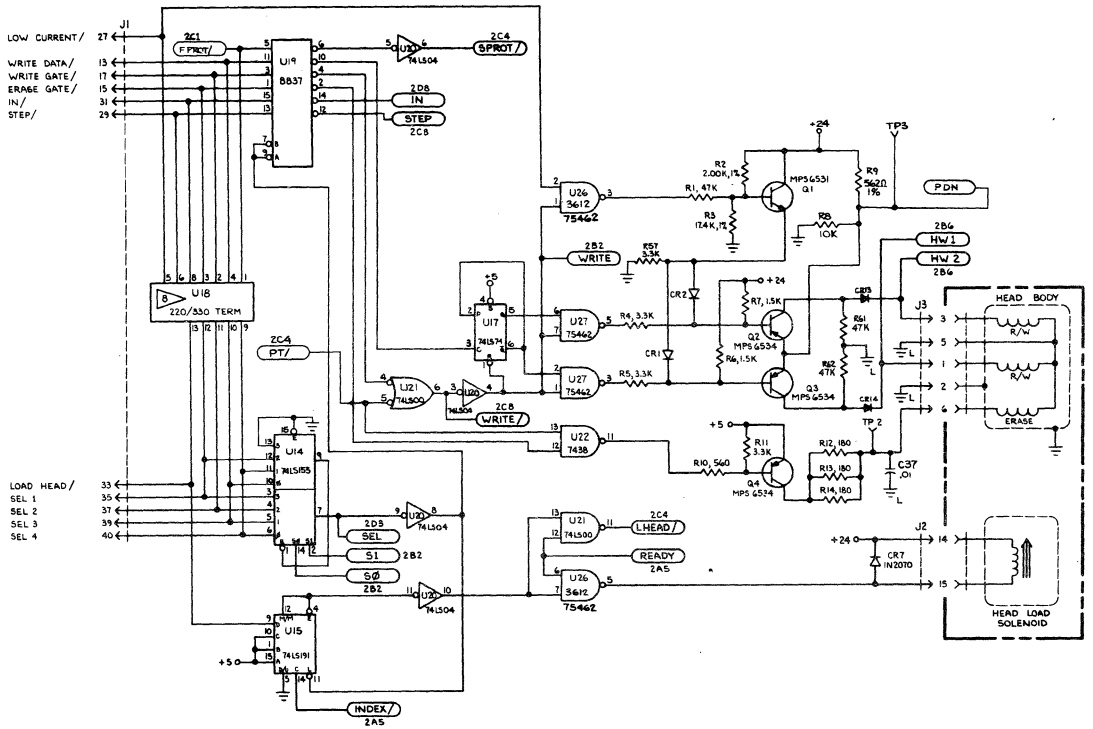
	JUMPER* FROM/TO	DR 1	DR 2	DR 3	DR 4
S0	CONN J6-12 To J6-2	OUT	IN	OUT	IN
S1	CONN J6-13 To J6-3	OUT	OUT	IN	IN

* FOR USE IN 7000 CARD CAGE SYSTEMS NO JUMPER REQUIRED

6. ORIGINS AND DESTINATIONS OF INTERSHEET SIGNAL NETWORKS ARE SHOWN ADJACENT TO THEIR CORRESPONDING SIGNAL CALLOUT AND REFERS TO SHEET NO. AND ZONE. EXAMPLE : 2B7 IS FOUND IN ZONE B7 ON SHEET 2

7 8 REMOVE INTEGRATED CIRCUIT U18 FOR ALL DRIVES IN A MULTIPLE SYSTEM EXCEPT THE LAST DRIVE IN THE CHAIN.

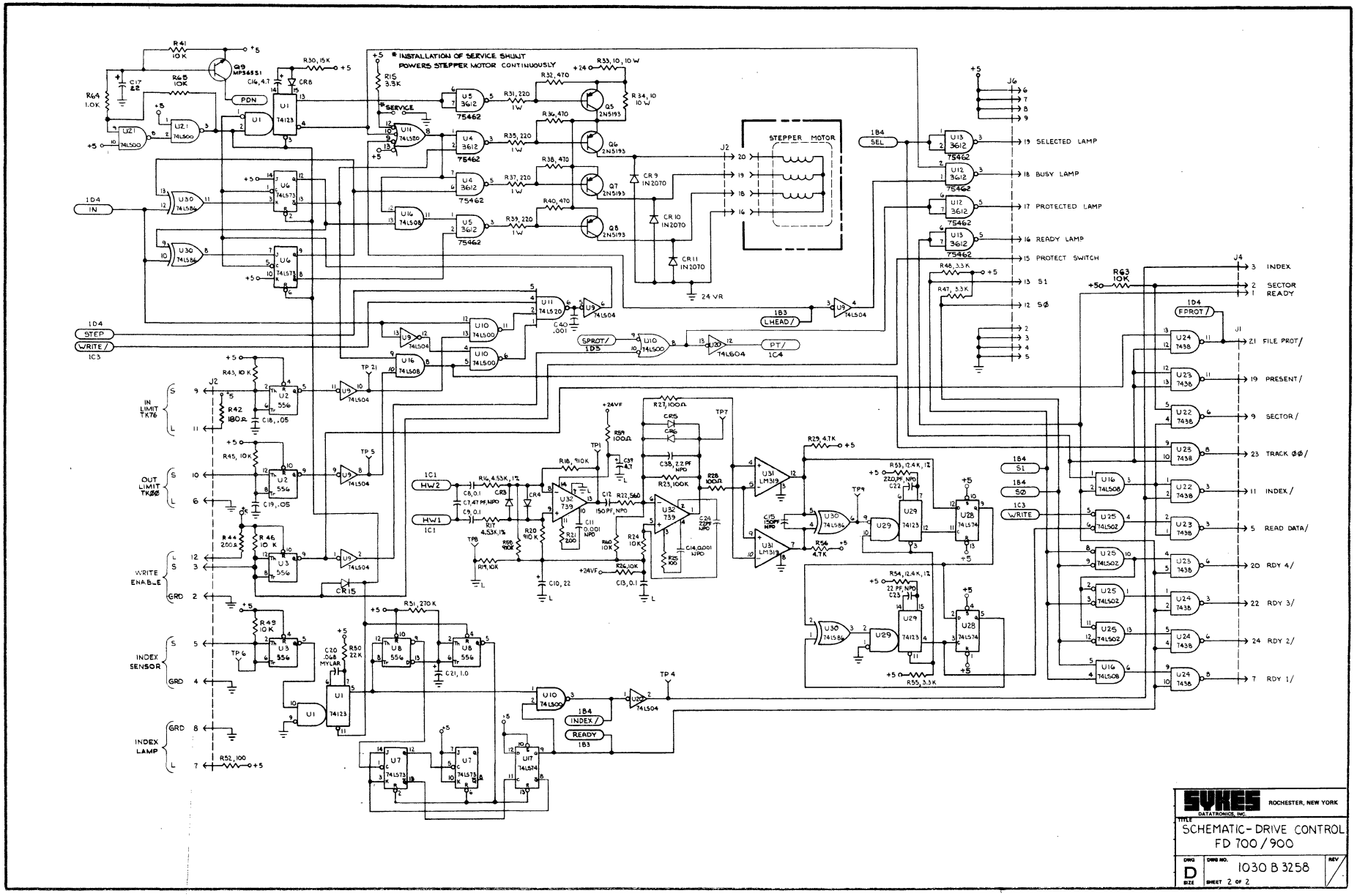




SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC - DRIVE CONTROL FD 700/900

DWG	DWG NO.	REV
D	1030 B 3258	6
SIZE	SHEET 1 OF 2	


* INSTALLATION OF SERVICE SHUNT POWERS STEPPER MOTOR CONTINUOUSLY
STEPPER MOTOR
24 VR
SELECTED LAMP
BUSY LAMP
PROTECTED LAMP
READY LAMP
PROTECT SWITCH
INDEX
SECTOR READY
FILE PROT/
PRESENT/
SECTOR/
TRACK ØØ/
INDEX/
READ DATA/
RDY 4/
RDY 3/
RDY 2/
RDY 1/
IN LIMIT TK76
OUT LIMIT TKØØ
WRITE ENABLE
INDEX SENSOR
INDEX LAMP
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK
SCHEMATIC- DRIVE CONTROL FD 700/900
1030 B 3258
SHEET 2 OF 2

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CHAPTER 11

SYSTEM INTERCONNECTION DIAGRAMS & SCHEMATICS

This chapter contains reference diagrams showing power distribution, base card interconnections, and general information for the Comm-Stor system. It also contains schematics for the Comm-Stor Flexible Disk Controller.

MP-RAM Board Signals

Mnemonic	Signal Point	Connection Point
CK 32	32.125 KHZ Clock	B-16
CK 1	1 MHZ Clock	
CK .25	4 MHZ Clock	B-14
IRQ1	Terminal, Modem Interrupt	B-19
IRQ2	Printer Interrupt	B-18
IRQ3	Timer Interrupt	B-24
NMI	Non-Maskable Interrupt	B-50
STROBE 13	Baud Rate Switch Enable	B-13
MEMS/	Memory Strobe	B-23
DS/	Data Strobe	B-25
DOENB/	Data Out Enable	
WR/	Write/Read	B-28
RW/	Read/Write	B-31
WE/	Write Enable	B-89
CMOS/	CMOS Memory Strobe	B-44
RAMØCK	RAM Bank Ø Strobe	
RAM1CK	RAM Bank 1 Strobe	
DG1/	Term., Modem Device Group Decoder Enable	B-58
DG2/	Printer Device Group Decoder Enable	B-60
DG3/	Disk Controller Device Group Decoder Enable	B-62
PFIELD/	PROM Enable	B-26
ROMCK/	ROM, PROM Clock	B-21

PROM/ROM Board Signals

Mnemonic	Signal Point	Connection Point
ROMCK	PROM/ROM Clock	B-21
WR/	Write/Read	B-28
PFIELD/	PROM Enable	B-26
XJ311	PROM Field Enable	
XJ31Ø	PROM Field Enable	

EIA Board Signals

Mnemonic	Signal Point	Connection Point
WR/	Write/Read	B-28
DS/	Data Strobe	B-25
DG/	Device Group Decoder Input	J2-43
DG1/	Terminal, Modem Device Group Decoder Input	B-58, J2-20
DG2/	Printer Device Group Decoder Input	B-60, J2-42
IRQ/	Interrupt Out (EIA)	J2-1
IRQ1/	Terminal, Modem Interrupt Signal	J2-50, B-19
IRQ2/	Printer Interrupt Signal	J2-25, B-18
STROBE 13	Baud Rate Switch Strobe	B-13, J2-18
POR	Power On Reset (EIA)	
RESTART	Restart	J2-49, B-15
CLOP	Current Loop Operation	J2-37
BUSY2	Busy-Drive 2	J3-3
RDY2	Ready-Drive 2	J3-8
STATUS	Status	J3-6
CARRIER	Modem Carrier	J3-10
BUSY1	Busy-Drive 1	J3-1
RDY1	Ready-Drive 1	J3-5

Terminal Signals

Signal Point	EIA Board Connection Point
Ring Indicator	J2-39
Sec. Rec. Line Sig. Det.	J2-38
Rec. Line Sig. Det.	J2-24
Data Set Rdy.	J2-41
Clear to Send	J2-32
Received Data (to TERM)	J2-31
Request to Send	J2-23
Sec. Request to Send	J2-22
Data Term. Rdy.	J2-6
Transmitted Data (from TERM)	J2-30
Binary Switch	J2-44

Modem Signals

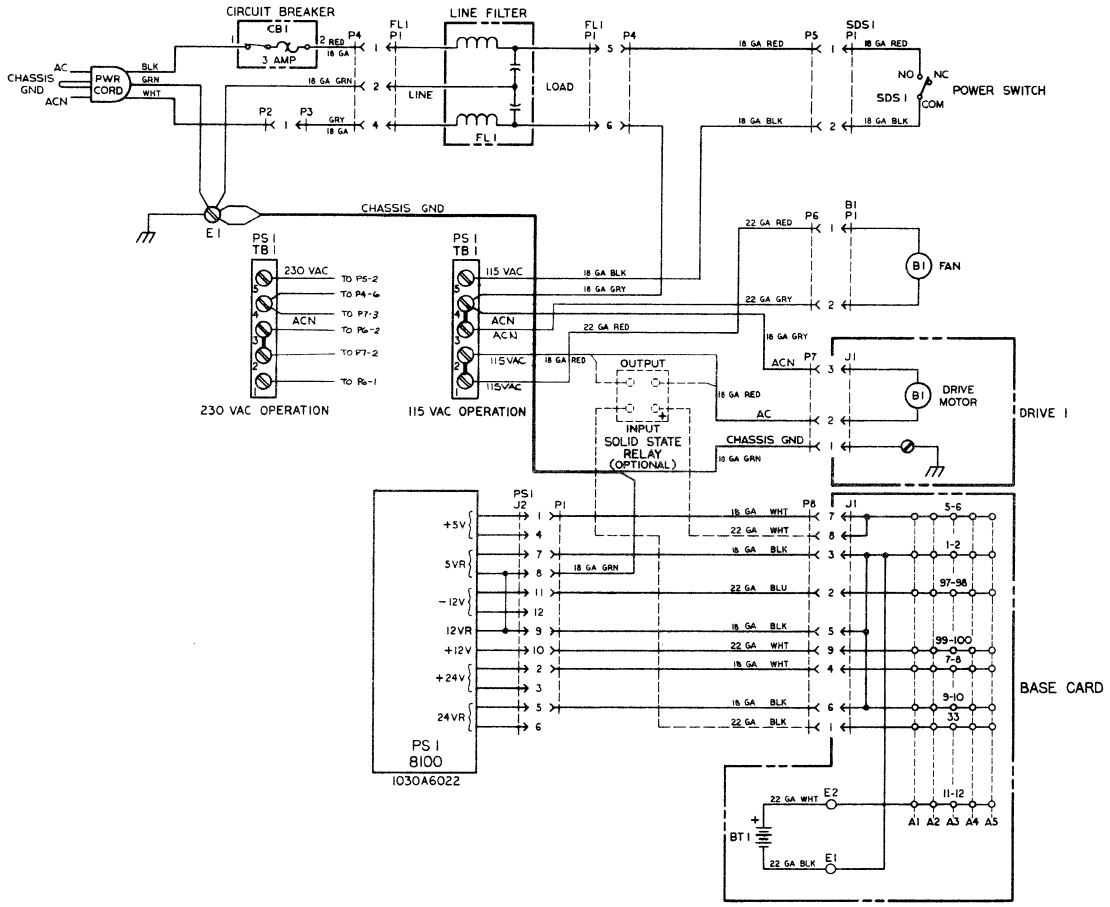
Signal Point	EIA Board Connection Point
Data Set Rdy.	J2-36
Rec. Line Sig. Det.	J2-48
Sec. Rec. Line Sig. Det.	J2-46
Ring Indicator	J2-33
Clear to Send	J2-28
Rec. Data (from Modem)	J2-47
Data Term. Rdy.	J2-34
Sec. Req. to Send	J2-35
Req. to Send	J2-21
Trans. Data (to Modem)	J2-4

Disk Controller Signals

Mnemonic	Signal Point	Connection Point
DG3/	Disk Control Decoder Signal	B-62
WR	Write/Read	B-28
RW	Read/Write	B-31
DS/	Data Strobe	B-25
LJ211	Byte Counter Load	
LF3Ø9	Disk Sequence Register Load	
LC2Ø9	Timer Load	
POR	Power On Reset (D.C.B.)	
FEN	FIFO Enable	
WTM	Write Mode	
RDM	Read Mode	
CP	Clock Pulse	
BCK	Bit Clock	
STR	2 us Write Strobe	
SER DAT	Serial Data	
CNTR-FLG	Counter Flag	
IRQ3	Timer Interrupt	B-24
MKFD	Mark Found	
LD215	Timer Output Enable	
CK.25	4 MHZ Clock	B-14
CRY	Character Ready	
RESET/	Reset	J2-25
IN/	Step Direction	J2-31
LOW CUR/	Low Write Current	J2-27
LOAD HEAD/	Load Head Solenoid	J2-33
WG/	Write Gate	J2-17
EG/	Tunnel Erase Gate	J2-15
WRITE DATA/	Write Data	J2-13
INDEX/	Index Signal	J2-11
FILE P./	File Protect	J2-21
TRK Ø/	Track ØØ Signal	J2-23
RDY2/	Drive 2 Ready	J2-24
RDY1/	Drive 1 Ready	J2-7
FILE UNS/	File Unsafe	J2-19
DUAL UNIT	Dual Unit	J2-22
READ DATA/	Read Data	J2-5

B - represents connections on the Bus.

J(x) - represents connectors on PCB's.

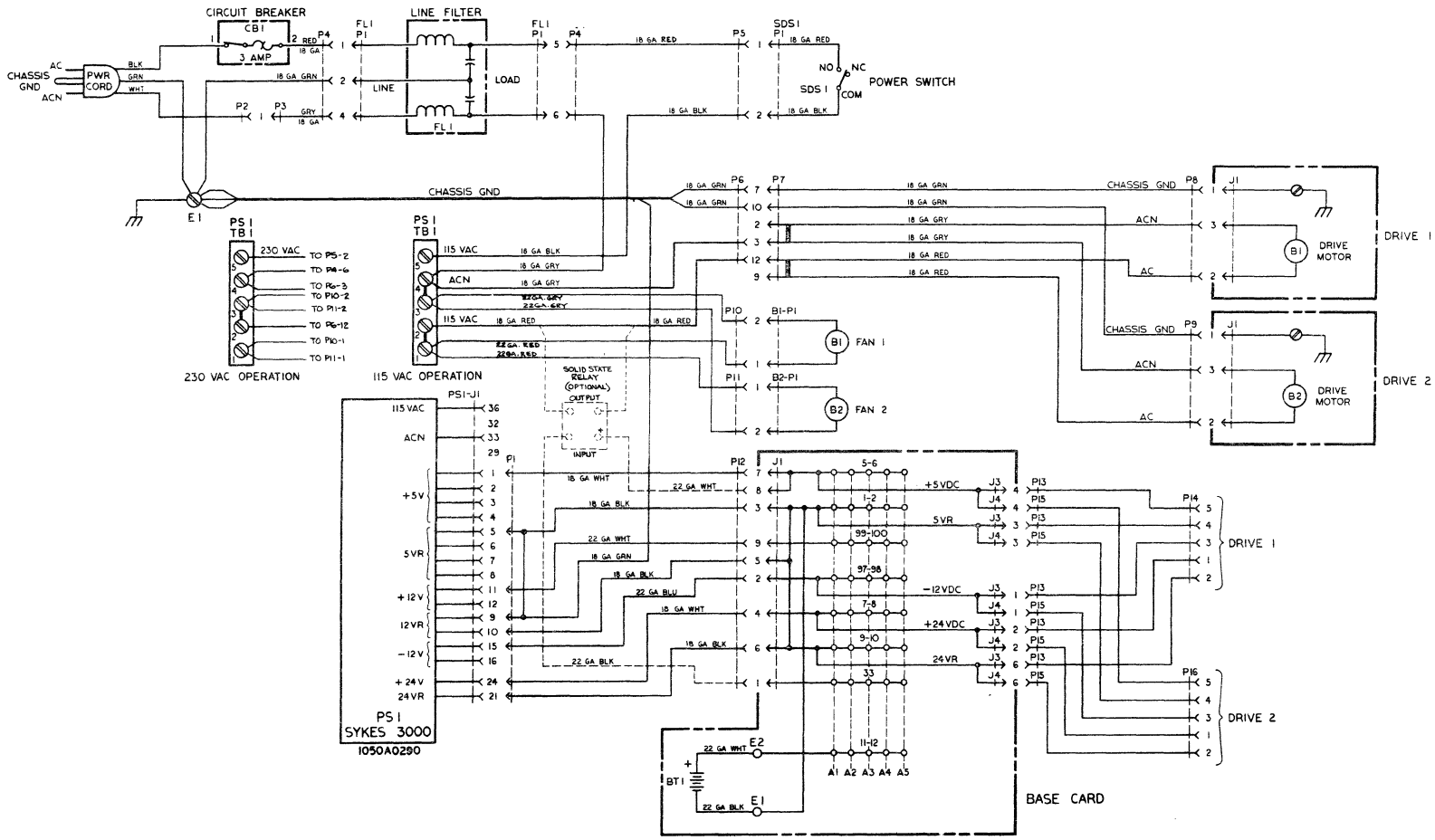


HI/LOW LEVEL POWER DISTRIBUTION
SYKES 8100 SYSTEM

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE
REFERENCE DIAGRAMS
8000 SYSTEMS

DWG SIZE	DWG NO.	REV
D	1030 B 6008	
	SHEET 2 OF 4	

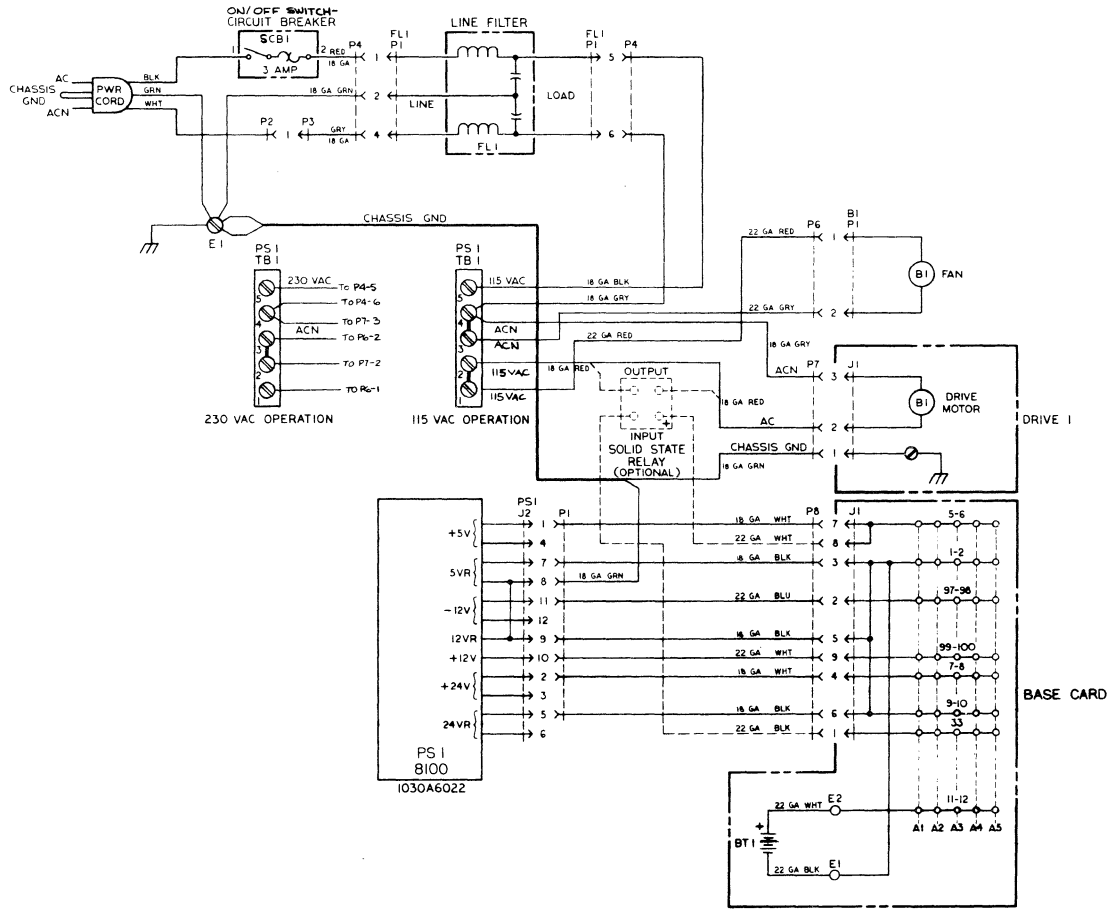


HI/LOW LEVEL POWER DISTRIBUTION
SYKES 8200 SYSTEM

SYKES DATAPRONICS, INC. ROCHESTER, NEW YORK

TITLE
REFERENCE DIAGRAMS
8000 SYSTEMS

DWG SIZE	DWG NO.	REV
D	1030B6008	
	SHEET 3 OF 4	



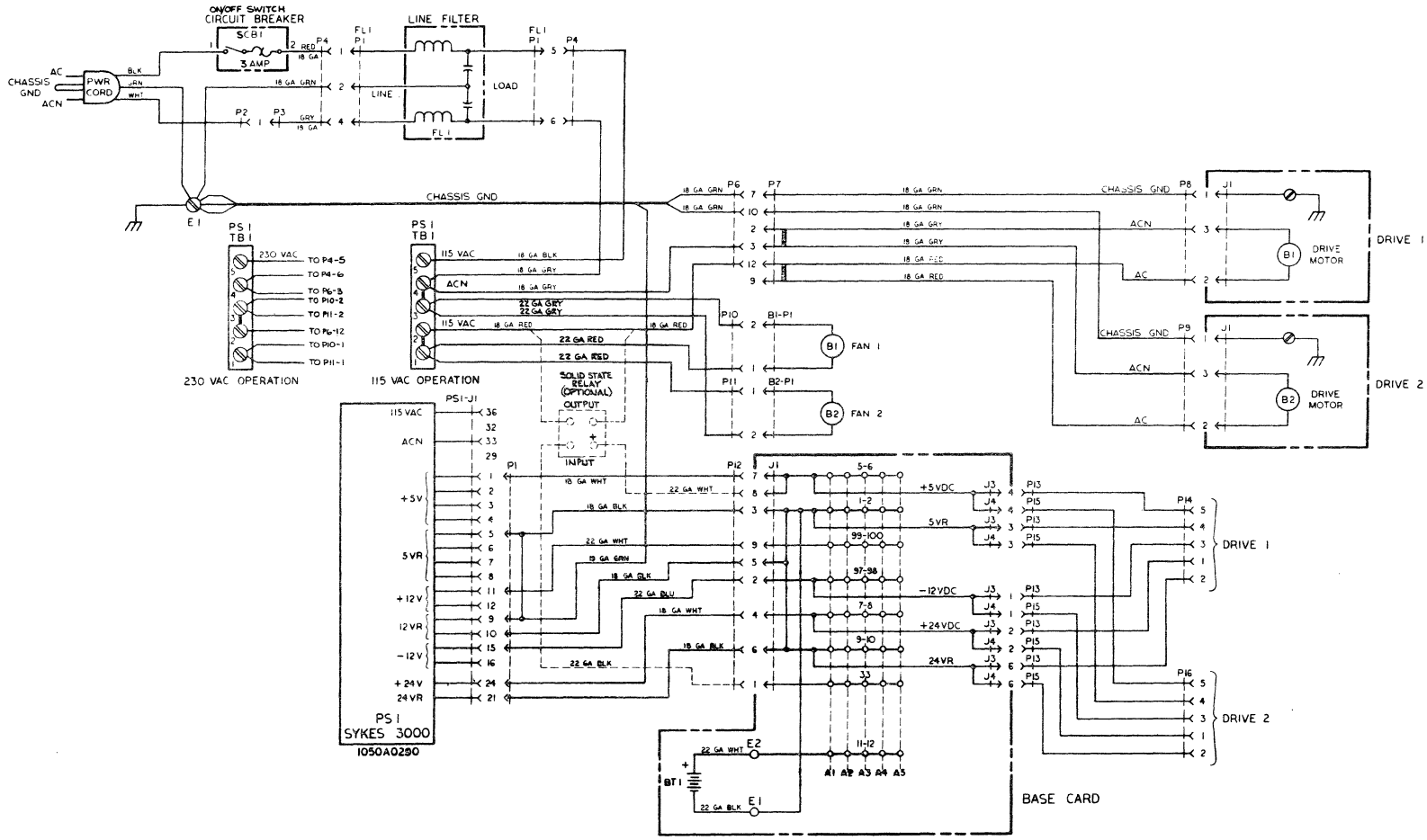
HI/LOW LEVEL POWER DISTRIBUTION
SYKES 8120,8130,8140 SYSTEMS

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SYSTEM SCHEMATIC
COMM-STOR II, III, & IV

SIZE: D | DWG NO. 1030 B5089 | REV

SHEET 2 OF 4

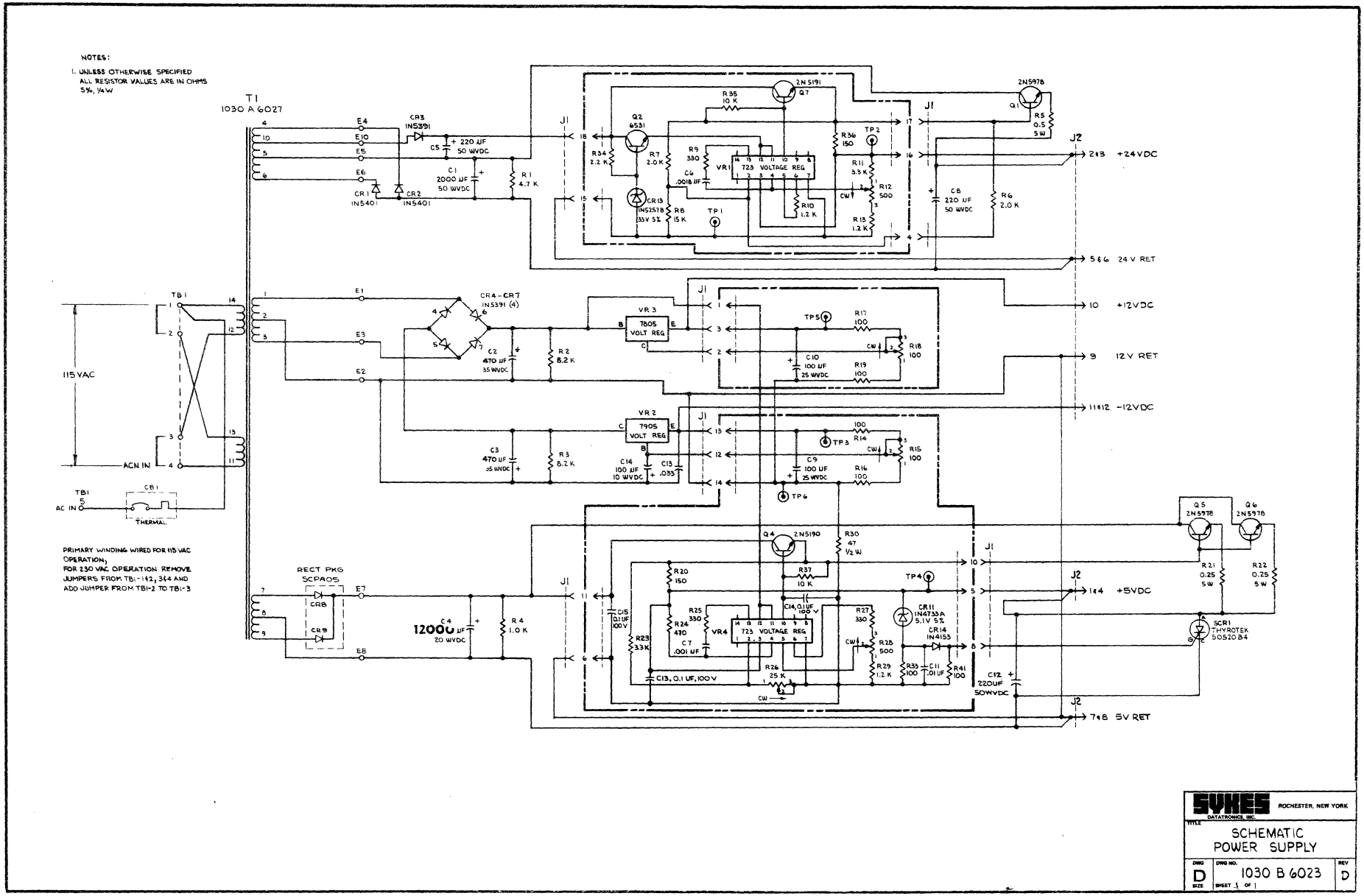


HI/LOW LEVEL POWER DISTRIBUTION
SYKES 8220, 8230, 8240 SYSTEMS

DATATECHNICS, INC. ROCHESTER, NEW YORK

TITLE
SYSTEM SCHEMATIC
COMM-STOR II, III, & IV

SIZE D | DWG NO. 1030B5089 | SHEET 3 OF 4 | REV



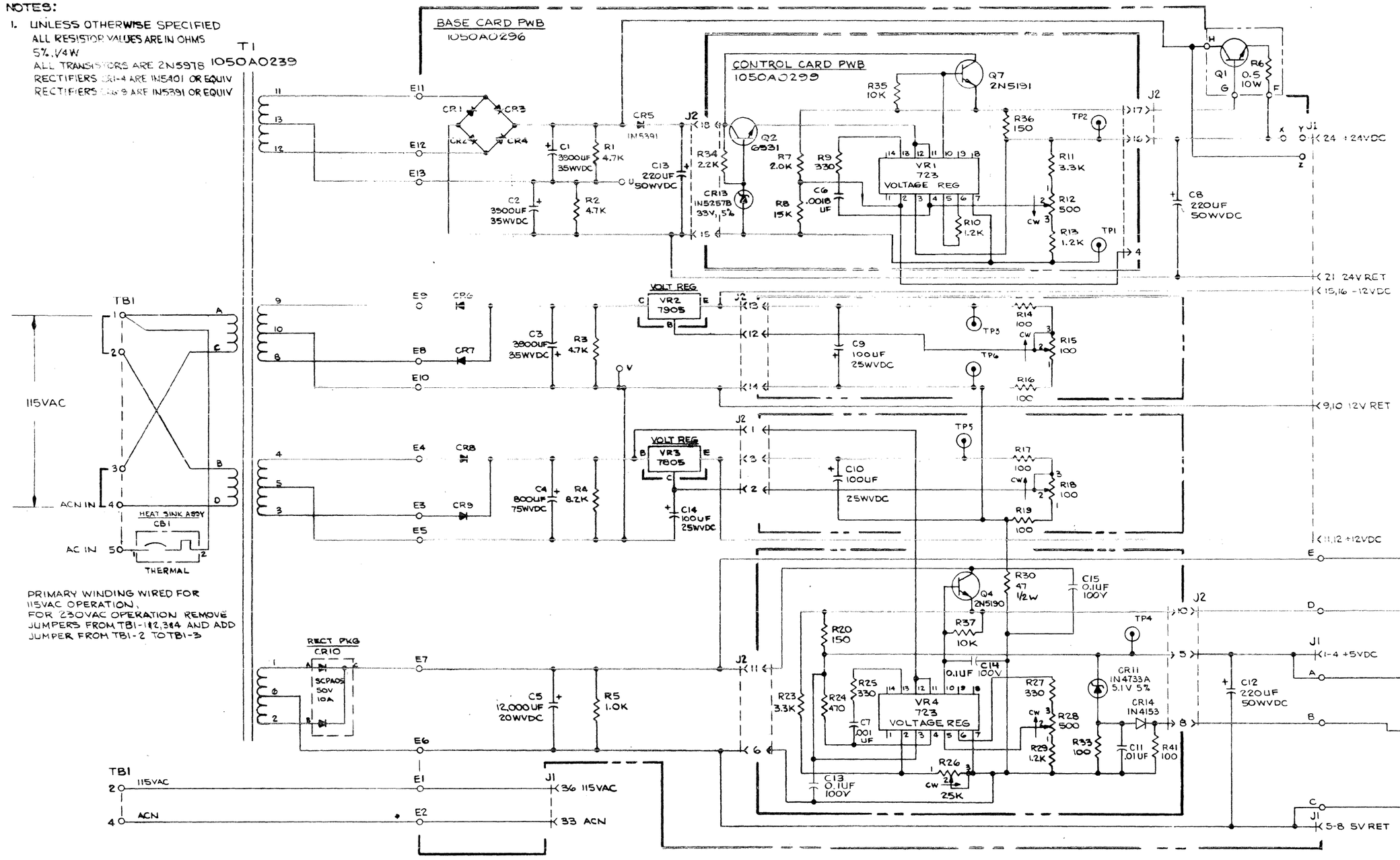
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC POWER SUPPLY

DWG SIZE	DWG NO.	REV
D	1030 B 6023 SHEET 1 OF 1	D

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ARE IN OHMS
   5%, 1/4W
   ALL TRANSISTORS ARE 2N5978
   RECTIFIERS CR1-4 ARE IN5401 OR EQUIV
   RECTIFIERS CR5-9 ARE IN5391 OR EQUIV



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE SCHEMATIC
POWER SUPPLY
INT. HEAT SINK

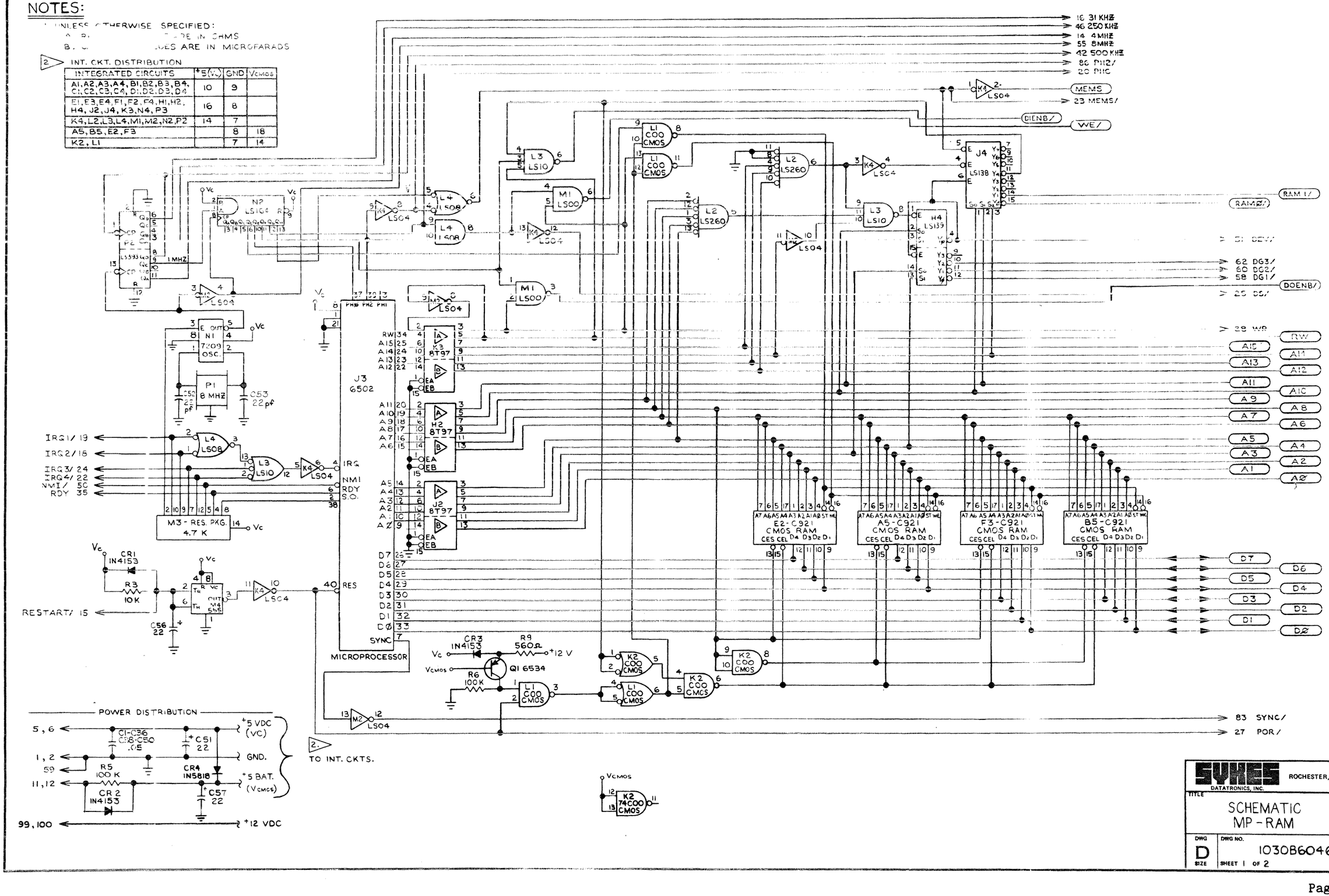
DWG SIZE	DWG NO.	REV
D	1050B0295	E
	SHEET 1 OF 1	

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS
   B. CAPACITORS ARE IN MICROFARADS

2. INT. CKT. DISTRIBUTION

INTEGRATED CIRCUITS	+5 (Vc)	GND	Vcmos
A1,A2,A3,A4,B1,B2,B3,B4, C1,C2,C3,C4,D1,D2,D3,D4	10	9	
E1,E3,E4,F1,F2,F4,H1,H2, H4, J2, J4, K3, N4, P3	16	8	
K4, L2, L3, L4, M1, M2, N2, P2	14	7	
A5, B5, E2, F3		8	18
K2, L1		7	14



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC MP - RAM

DWG SIZE	DWG NO.	REV
D	1030B6046 SHEET 1 OF 2	L

D6 D7 D4 D5 D2 D3 DØ D1 DOENB/ RAMØ/ RAM1/
AØ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 WE/ RW MEMS
PFIELD/ 26

SW1 AUX. SW2 MODEM SW3 PRINTER SW4 TERM

P4 4.7K PULLUP M3 4.7K PULLUP

SEL N4 LS257 SEL P3 LS257

E3 BT97 E4 BT97 F4 BT97

M1 LS00 M2 LS04 L4 LS08

F1 LS85 E1 LS85

K1 3624 PROM M3 4.7 K PULLUP

F2 LS257 H1 LS257

D3 91L02B/2102AL BANKØ-BIT 7
D4 91L02B/2102AL BANK1-BIT 7
BIT6 D1 BIT5 C3 BIT4 C1 BIT3 B3 BIT2 B1 BIT1 A3 BITØ A1
BIT6 D2 BIT5 C4 BIT4 C2 BIT3 B4 BIT2 B2 BIT1 A4 BITØ A2

31 RW
96 DO7
81 DO6
85 DO5
84 DO4
80 DO3
75 DO2
79 DO1
78 DOØ
95 AØ
94 A1
93 A2
54 A3
56 A4
87 A5
88 A6
90 A7
92 A8
91 A9
52 A10
53 A11
32 A12
34 A13
40 A14
36 A15
89 WE/
21 ROMCK

STROBE 13
DIENB/
DB7 82
DB6 77
DB5 66
DB4 70
DB3 74
DB2 73
DB1 72
DBØ 68

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC MP - RAM

DWG SIZE: D | DWG NO.: 1030B6046 | SHEET 2 OF 2 | REV

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTOR VALUES ARE IN OHMS
   B. CAPACITOR VALUES ARE IN MICROFARADS

2 ▷ INT. CKT. DISTRIBUTION

USED CKTS	+5 (Vc)	GND	Vcmos
A1, A2, A3, A4, B1, B2, B3, B4, C1, C2, C3, C4, D1, D2, D3, D4	0	9	
E3, E4, F4, F2, F4, G2, G4, H3, J1, J2, J3	6	8	
K1, K2, K3, K4, L1, L2, L3, L4, M1, M2, N2	2	7	
P1, P3, P2, P3		8	8
N1		7	2

42 500 KHZ
16 31 KHZ
14 4 MHZ
55 8 MHZ
46 250 KHZ
86 PH2/
20 PHG

MEMS
23 MEMS/
DIENB/
WE/
RAM 1/
RAM 0/
51 DEV/
62 DG3/
60 DG2/
58 DG1/
DOENB/
25 DS/
28 WR
31 RW
76 A15
40 A14
34 A13
32 A12
53 A11
52 A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
83 SYNC/
27 POR/

IRQ1/ 19
IRQ2/ 5
IRQ3/ 24
IRQ4/ 22
NMI/ 5
RDY 35
IRQ
NMI
RDY
S.O.
RESTART/ 15
RES/
SYNC
(MICROPROCESSOR)

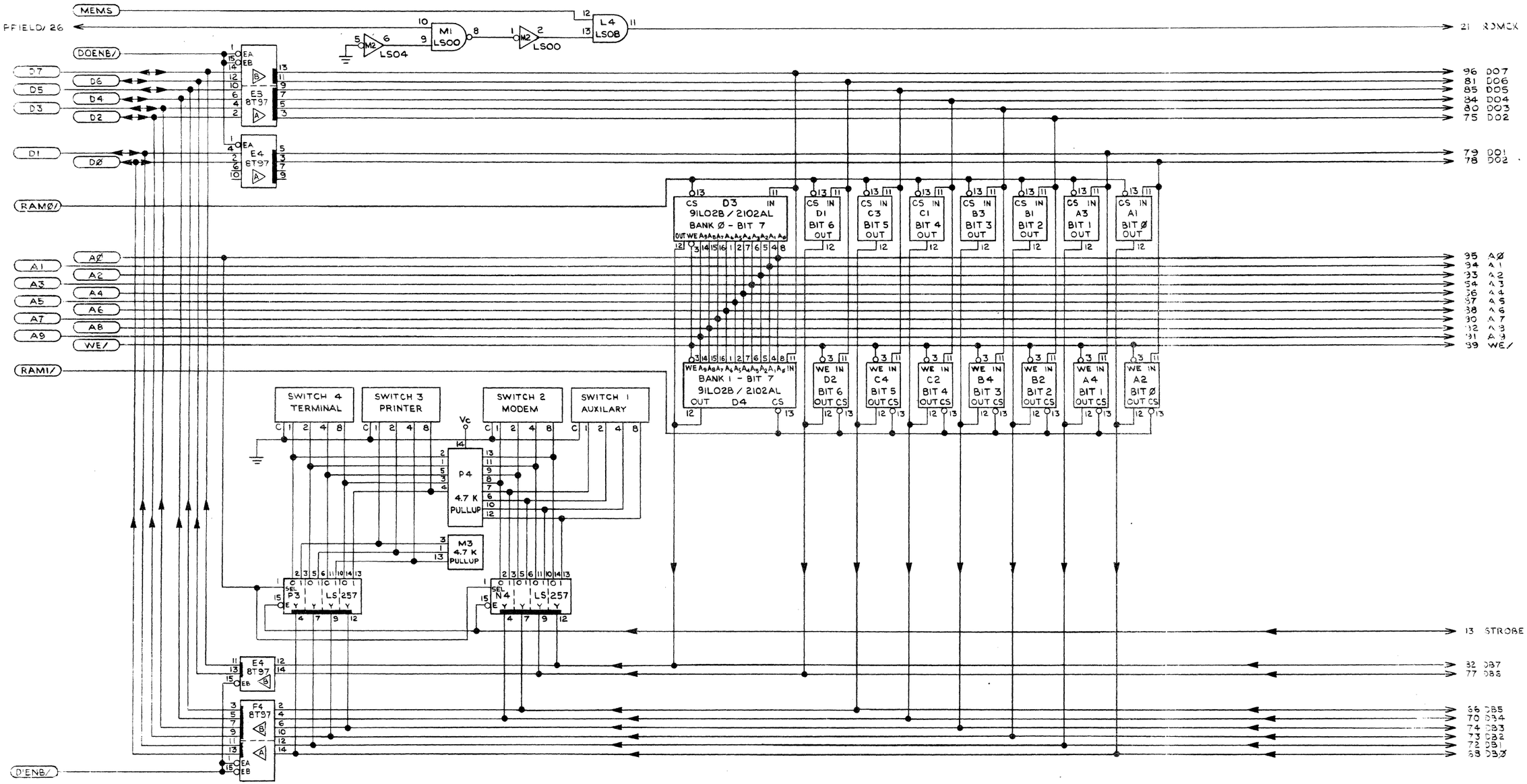
POWER DISTRIBUTION
5, 6 — +5 VDC (Vc)
1, 2 — GND.
11, 12 — +5 BAT. (Vcmos)
99, 100 — +12 VDC
2 ▷ TO INT. CKT'S

SPARE

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC MP - RAM IV

DWG SIZE	DWG NO.	REV
D	1030B5077	E
	SHEET 1 OF 2	



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC MP-RAM IV

DWG SIZE: D

DWG NO.: 1030B5077

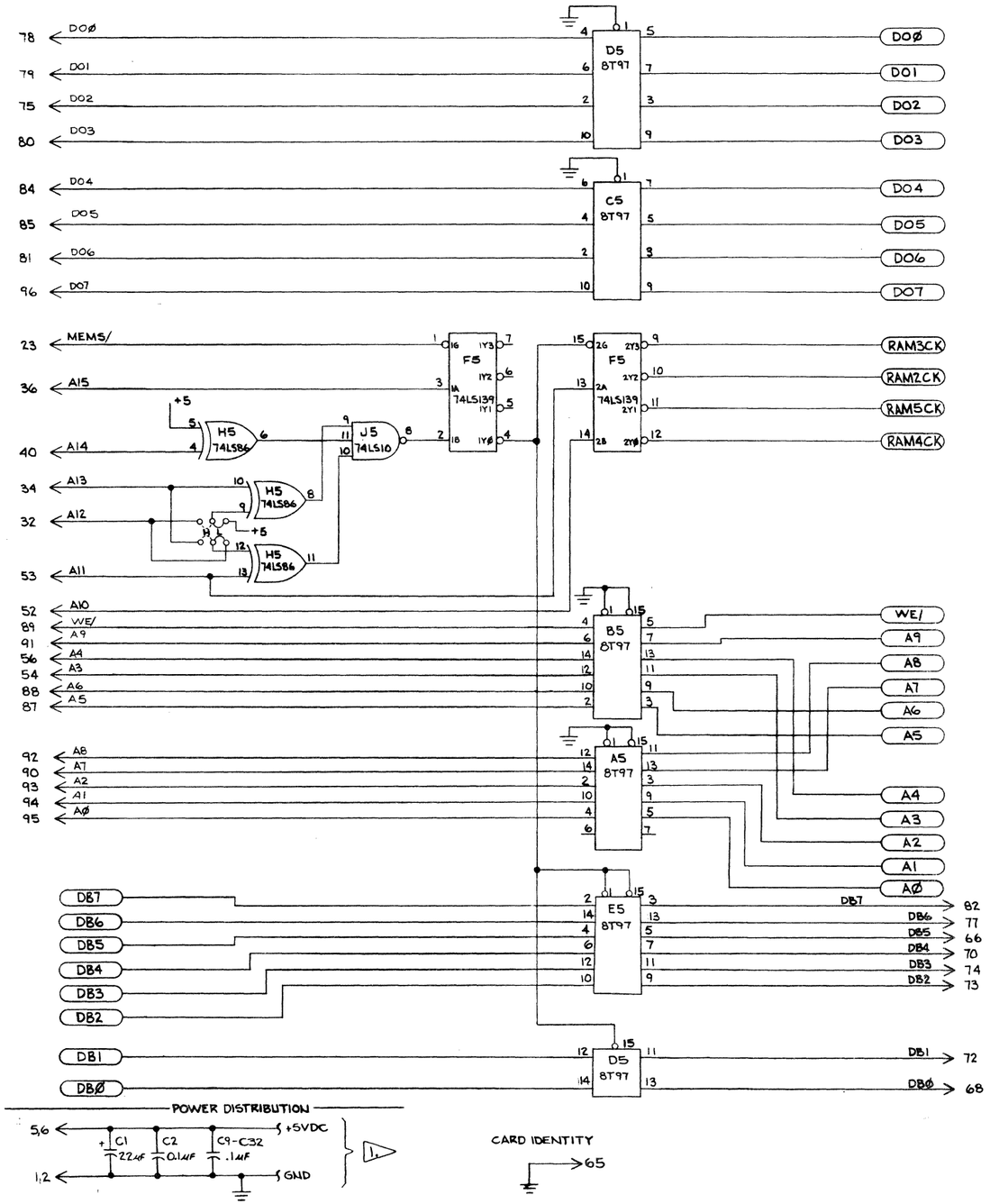
SHEET 2 OF 2

REV: /

NOTES:

1. INT. CKT. POWER DISTRIBUTION

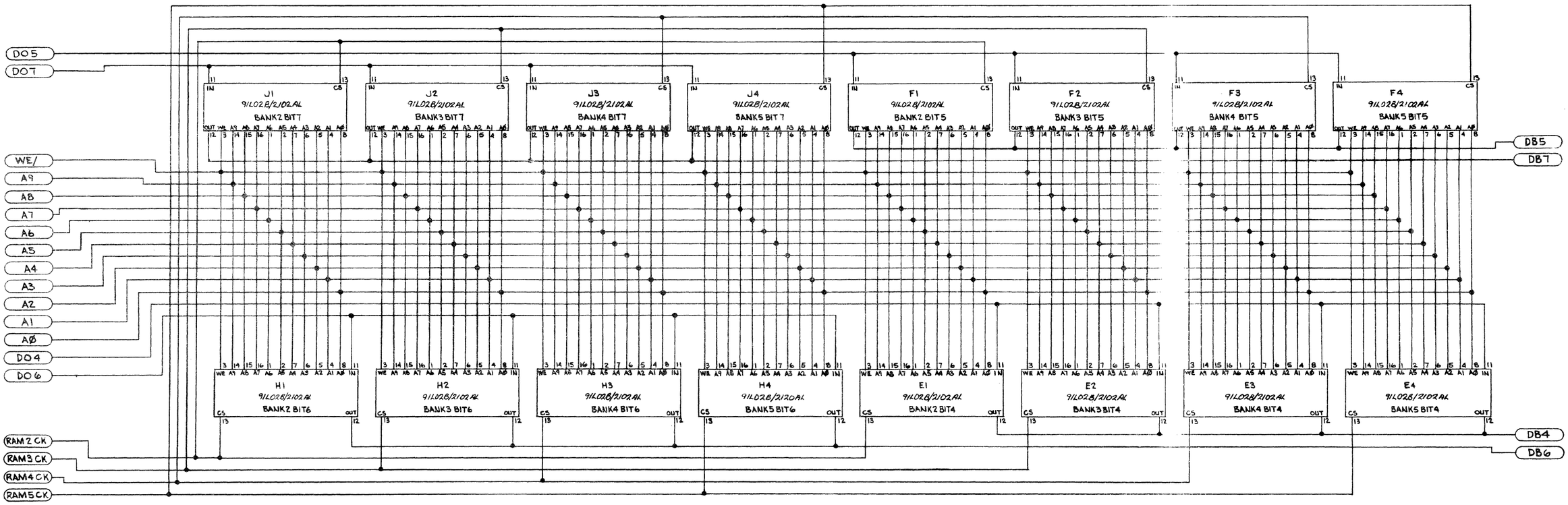
DESIGNATION	+5V	GND
A1-4, B1-4, C1-4, D1-4, E1-4 F1-4, H1-4, J1-4	10	9
A5, B5, C5, D5, E5, F5	16	8
H5, J5	14	7



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC RAM/MEMORY

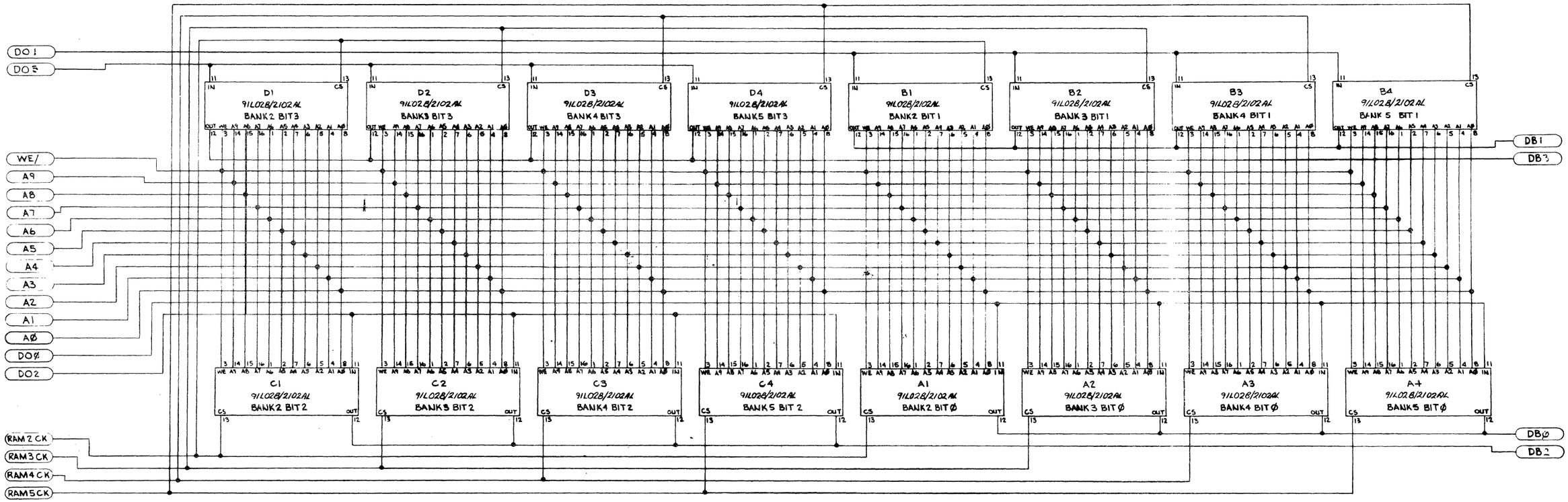
DWG SIZE	DWG NO.	REV
D	1030B6180	D
	SHEET 1 OF 3	



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE
SCHEMATIC
RAM/MEMORY

DWG SIZE	DWG NO.	REV
D	1030B6180	
	SHEET 2 OF 3	



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC RAM/MEMORY

DWG SIZE: D | DWG NO. 1030B6130 | REV | SHEET 3 OF 3

F4 LS138 DEVICE STROBE DECODER

J3 LS175 · H2 LS175 · J1 LS175 · F2 LS175 · B4 LS174 · A4 7416 OPEN COL.

K3 EIA DRIVER 1488 · L2 EIA DR. 1488 · L2 EIA DR. 1488 · K1 EIA DRIVER 1488

A2 150Ω SERIES RESISTORS DIP

B2 K1135A BAUD GEN.

J3 CONNECTOR: LEDS + POWER PILOT

J2 TO TERMINAL PORT

J2 TO MODEM PORT

E3 TERMINAL UART TR1402A

B3 MODEM UART TR1402A

E1 LS74 · B1 LS74

E4 LS257 · E2 LS257 · D4 LS257 · C3 LS257 · D2 LS257 · C4 LS257

E C1 ENCODER 74148

H4 LS138 DEVICE STROBE DECODER

STROBE FOR BAUD SWITCHES

4 EIA REC. 1489A

IN ENTER POSITION BINARY SWITCH SHOULD GROUND THIS LINE

TRANSMITTED DATA

RECEIVED DATA

LOW FOR FORCED SPACE

LOW FOR MARKING

MODEM DIALCT PATH

MARKING

TERM BAUD SIGNAL

CL. TO SEND

MOD. REC FLAG

MOD. TRANS. FLAG

REC. DATA (TEST)

POWER DISTRIBUTION

99,100 ← C38 22µf · CR2 IN4153 → +12V, +11V

97,98 ← C36 22µf · CR1 IN4153 → −12V, −11V

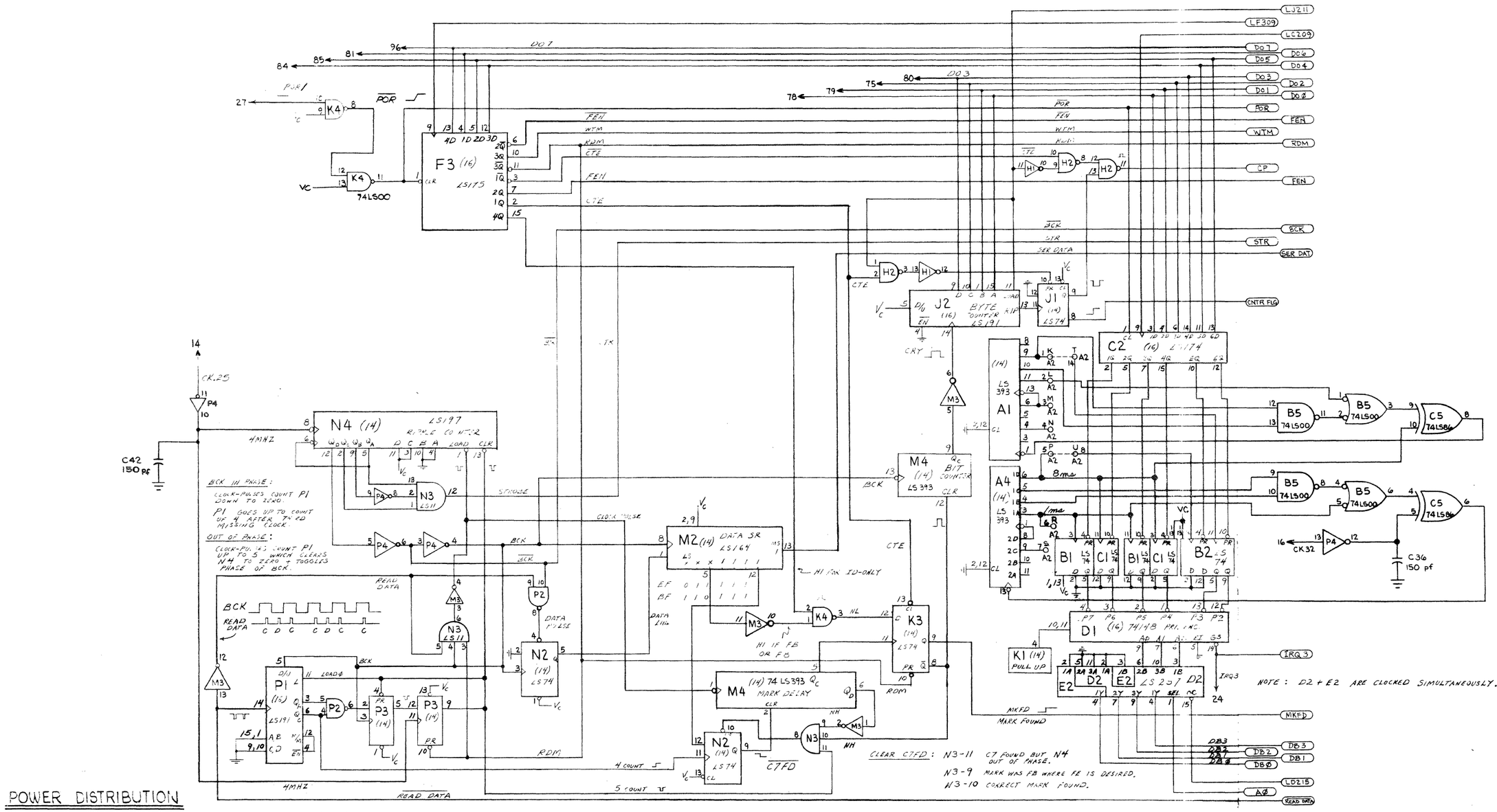
5,6 ← C37 22µf · C1–35 .05µf → VCC (+5V)

1,2 ← 61 → GND

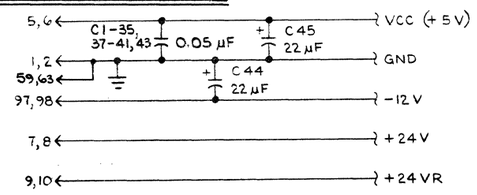
SUKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC EIA PORTS

DWG SIZE: D · DWG NO. 1030 B 6052 · SHEET 1 OF 1 · REV F



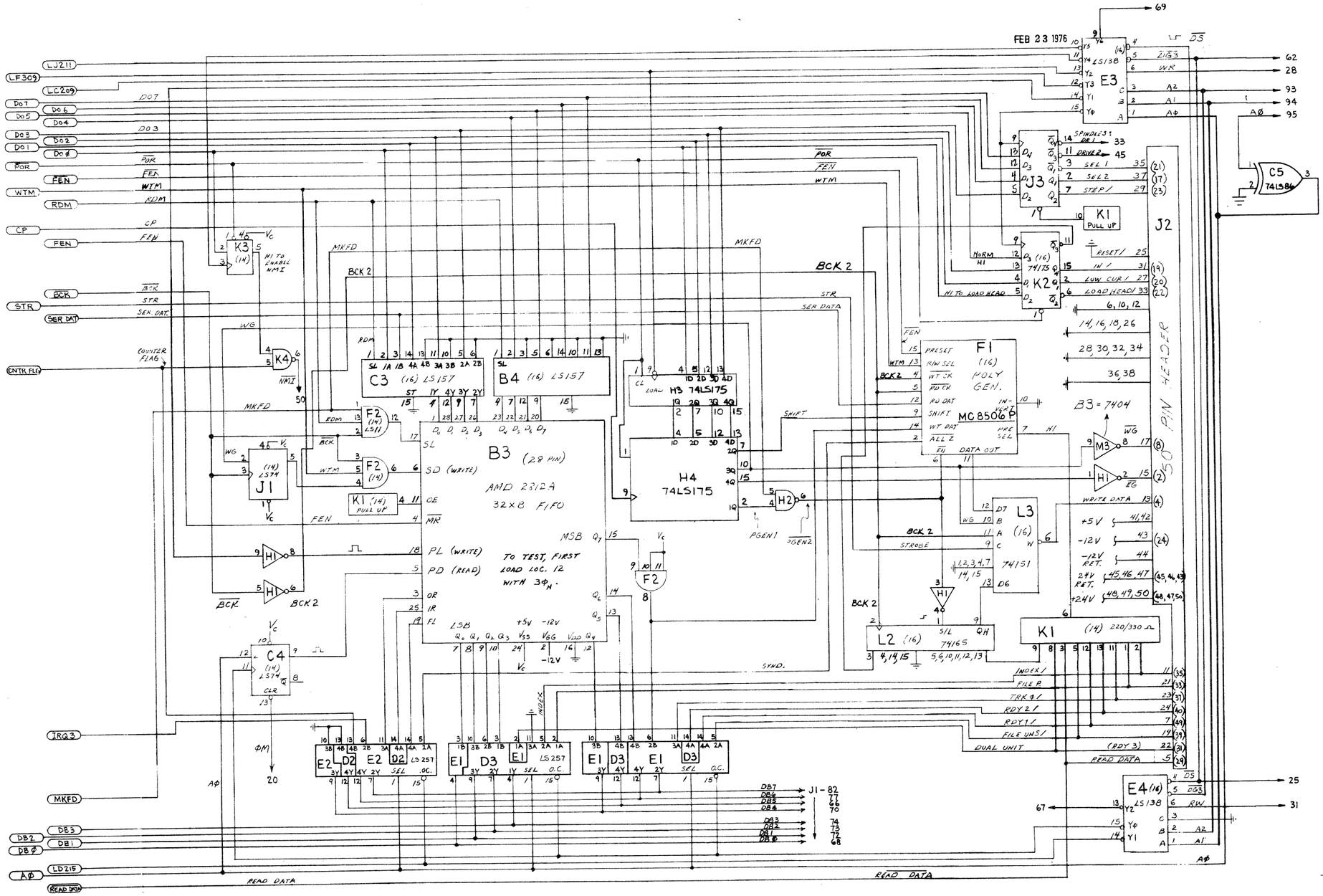
POWER DISTRIBUTION



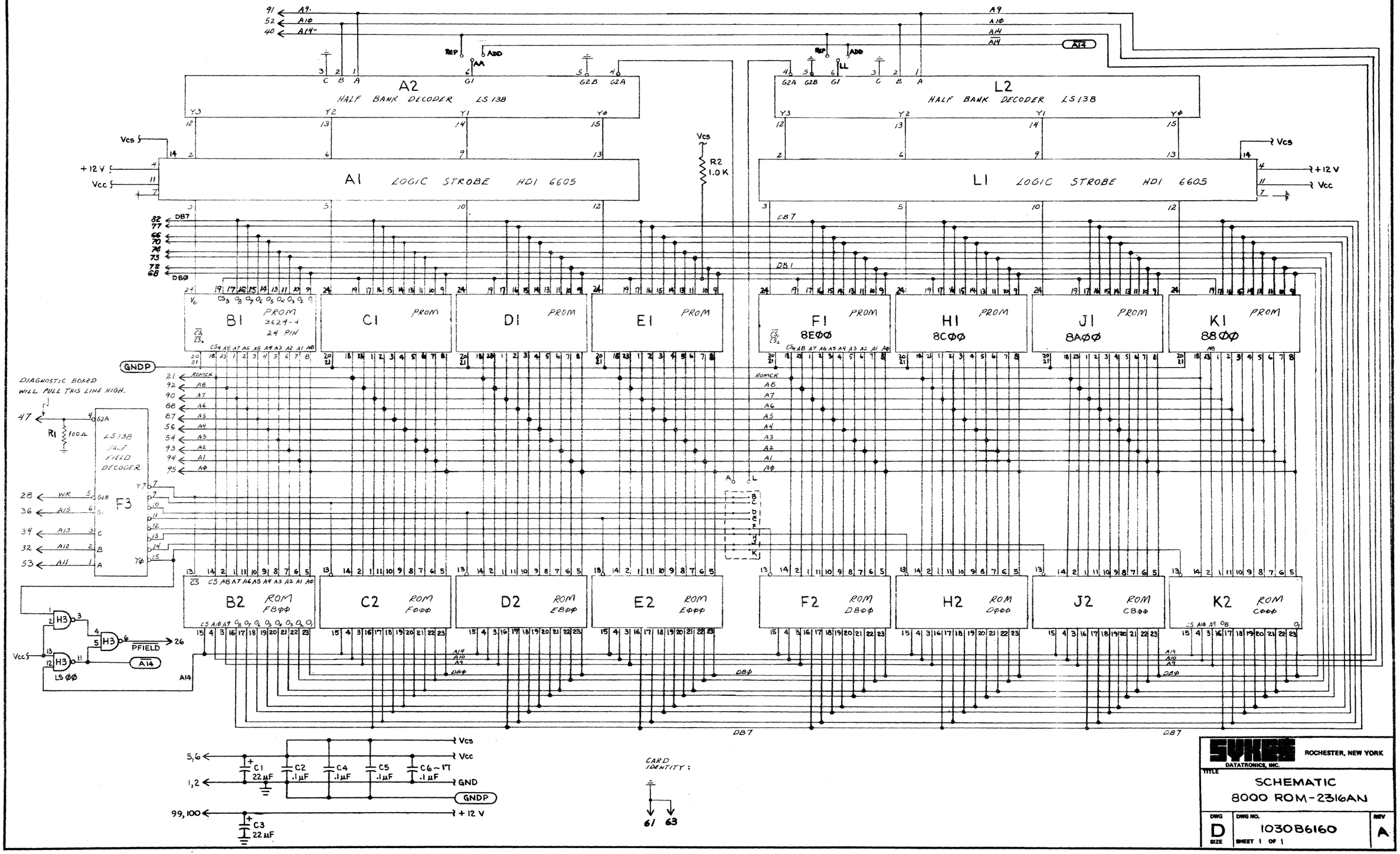
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC DISK CONTROLLER

DWG SIZE: D | DWG NO.: 1030 B 6055 | SHEET 1 OF 2 | REV: F



SYKES DATATRONICS, INC.	ROCHESTER, NEW YORK		
TITLE	SCHEMATIC DISK CONTROLLER		
DWG SIZE D	DWG NO. 1030 B 6055	SHEET 2 OF 2	REV 1



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC 8000 ROM-2316AN

DWG SIZE	DWG NO.	REV
D	1030B6160	A
	SHEET 1 OF 1	

NOTES:

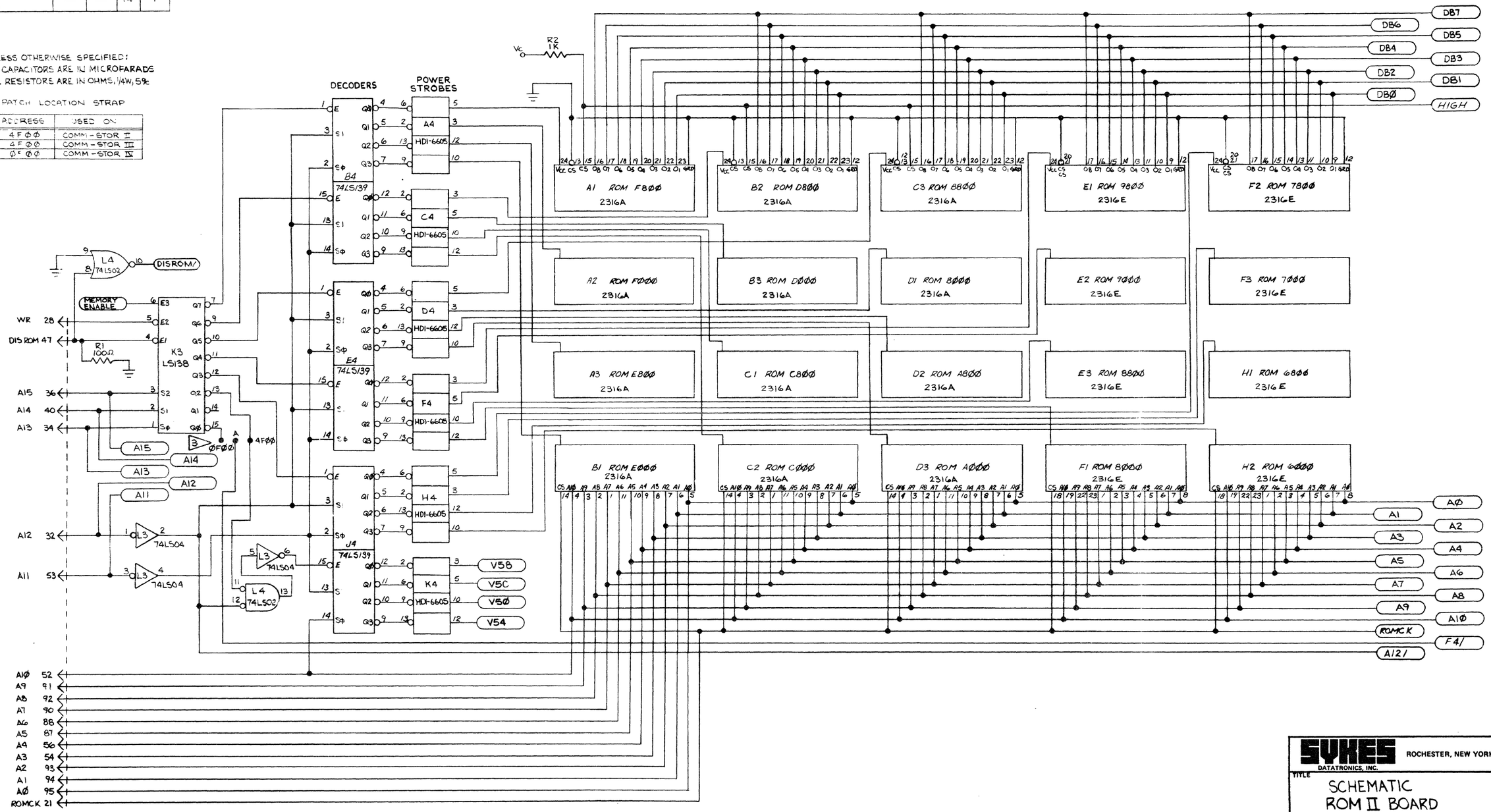
1. POWER DISTRIBUTION TO INT CKT'S

INT. CKT.	+12V	VCS	VC	GRD
A4, C4, D4, F4, H4, K4	4	14	11	7
B4, E4, J4, K2, K3, L2, M2, N2	—	—	16	8
L1, L3, L4, M1, M3, M4, N3, N4	—	—	14	7

2. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE IN MICROFARADS
ALL RESISTORS ARE IN OHMS, 1/4W, 5%

3. PATCH LOCATION STRAP

ADDRESS	USED ON
4FØØ	COMM-STOR II
4FØØ	COMM-STOR III
ØFØØ	COMM-STOR IV



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE
SCHEMATIC
ROM II BOARD

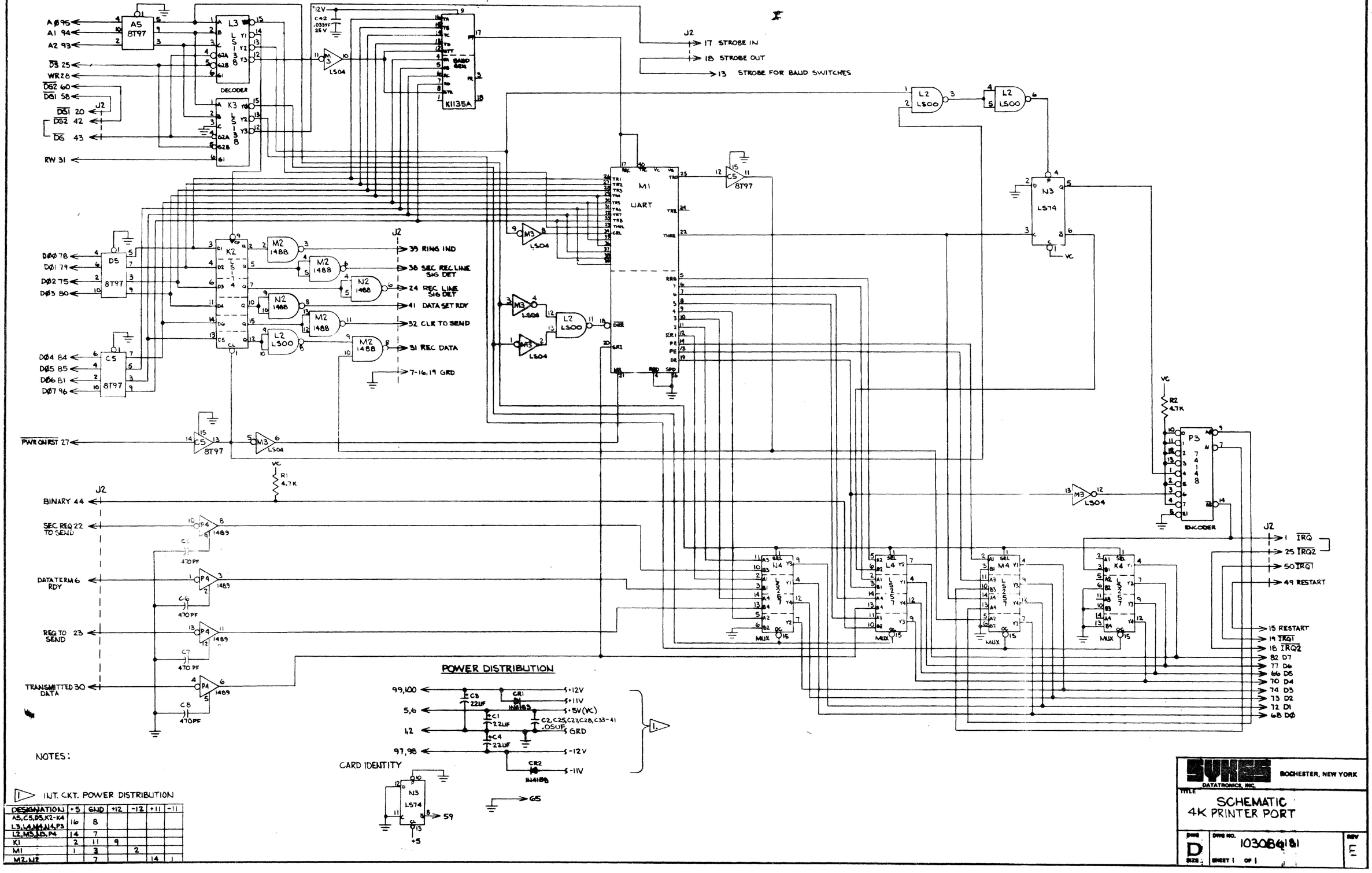
DWG SIZE	DWG NO.	REV
D	1030B6490	C
	SHEET 1 OF 2	

Ø2/ 86
SYNC/ 83
F4/
A11
A12
A13
A14
A15
DISROM/
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
V58
V5C
HIGH
ROMCK
A9
A8
A7
A6
A5
A4
A3
A2
A1
AØ
V54
V5Ø
A12/
A1Ø
N1 74LS08
L3 74LS04
M3 74LS30
N2 LS85
M2 LS85
H3 PROM 5CØØ 3628
J1 PROM 58ØØ 3628
K1 PATCH VECTORS 4FØØ 3628
J2 PROM 54ØØ 3628
J3 PROM 5ØØØ 3628
L4 74LS02
N4 74LS10
SEQUENCE COUNTER
N3 74LS74
M4 74LS00
TRAPPING
L1 74LS30
M1 74LS260
ALL ONES
ALL ZEROS
R3 1K
NO PATCHES
K2 LS257
L2 LS257
MEMORY ENABLE
POR/ 27
MEMS/ 23
POWER DISTRIBUTION
99,100
1,2,63,64,65
5,6
+12VDC
GND
+5VDC(VC)
+5VDC(VCS)
C12 22
C14 0.1
C15 0.1
C11,16-38 .05
C10 22
C13 .05
SPARES
82 D87
77 D86
66 D85
70 D84
74 D83
73 D82
72 D81
68 DBØ
26 PFIELD/

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC ROM II BOARD

DWG SIZE: D
DWG NO.: 1030B6490
REV:
SHEET 2 OF 2

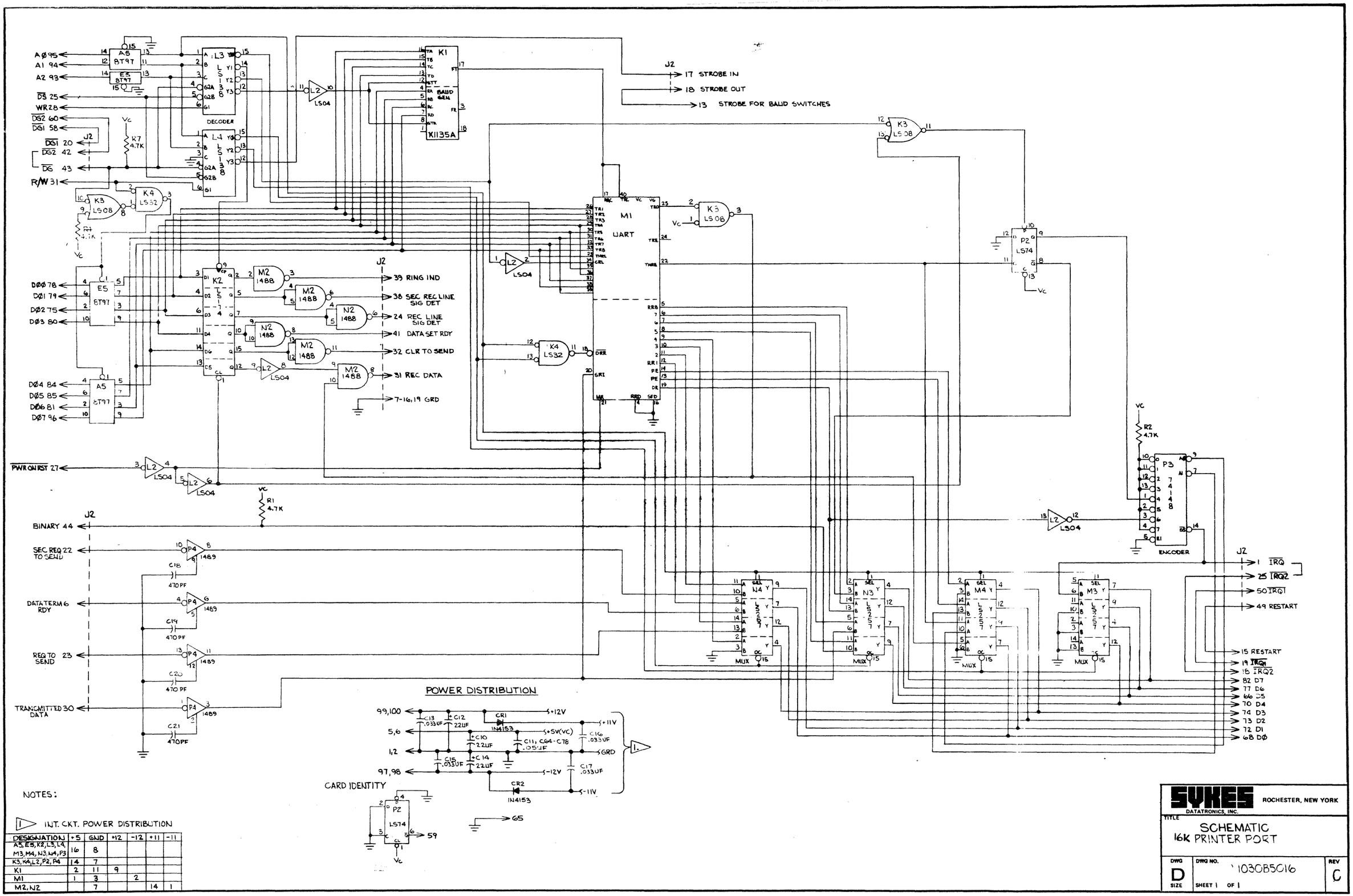


DESIGNATION	+5	GND	+12	-12	+11	-11
A5, C5, D5, K2-K4	16	8				
L3, L4, M4, N4, P3						
L2, M3, N3, P4	14	7				
K1	2	11	9			
M1	1	3		2		
M2, N2		7			14	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC 4K PRINTER PORT

SIZE D | DWG NO. 10308-4181 | REV E | SHEET 1 OF 1



DESIGNATION	+5	GND	+12	-12	+11	-11
A5, E5, K2, L3, L4, M3, M4, N3, N4, P3	16	8				
K3, K4, L2, P2, P4	14	7				
K1	2	11	9			
M1	1	3		2		
M2, N2		7			14	1

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC 16K PRINTER PORT

DWG SIZE	DWG NO.	REV
D	1030B5016	C
	SHEET 1 OF 1	

NOTES:

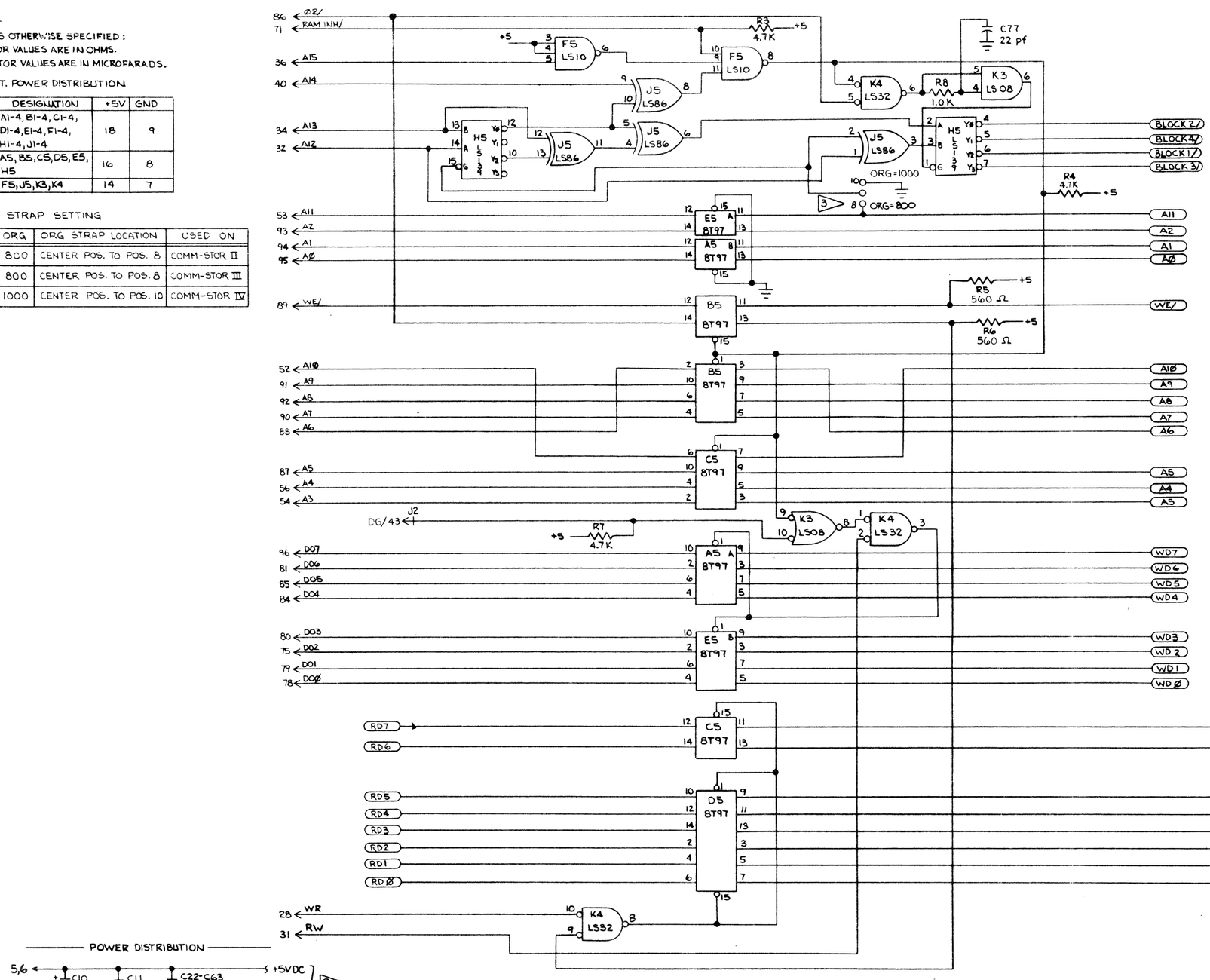
1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS.
   CAPACITOR VALUES ARE IN MICROFARADS.

2. INT. CKT. POWER DISTRIBUTION

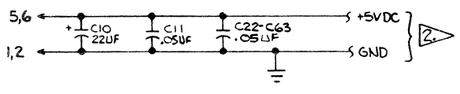
DESIGNATION	+5V	GND
A1-4, B1-4, C1-4, D1-4, E1-4, F1-4, H1-4, J1-4	18	9
A5, B5, C5, D5, E5, H5	16	8
F5, J5, K3, K4	14	7

3. ORG STRAP SETTING

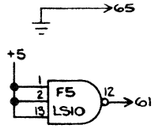
ORG.	ORG STRAP LOCATION	USED ON
800	CENTER POS. TO POS. 8	COMM-STOR II
800	CENTER POS. TO POS. 8	COMM-STOR III
1000	CENTER POS. TO POS. 10	COMM-STOR IV



POWER DISTRIBUTION



CARD IDENTITY



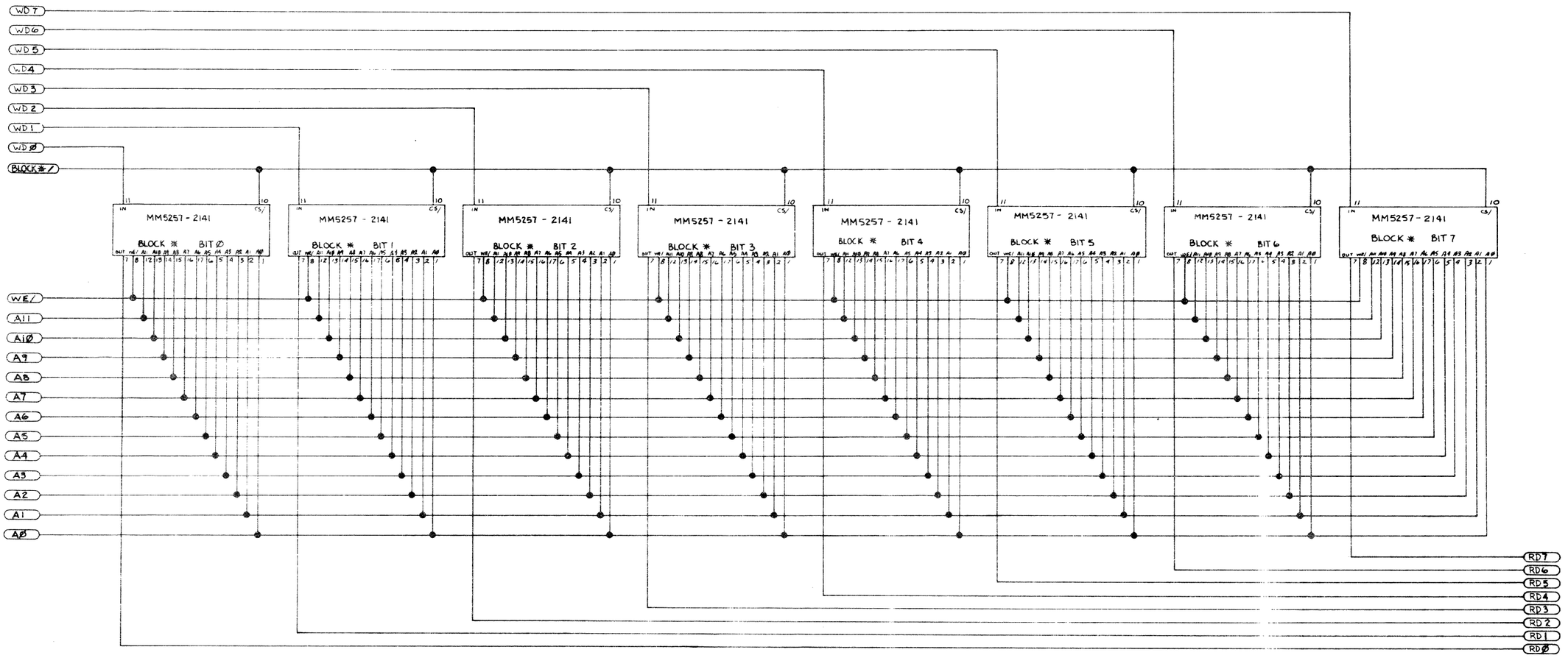
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC 16K RAM/MEMORY

DWG SIZE: D | DWG NO.: 1030B5017 | SHEET 1 OF 2 | REV: C

RAM MEMORY TABULATION

BLOCK *	STARTING ADDRESS	BIT Ø INT. CKT. LOCATION	BIT 1 INT. CKT. LOCATION	BIT 2 INT. CKT. LOCATION	BIT 3 INT. CKT. LOCATION	BIT 4 INT. CKT. LOCATION	BIT 5 INT. CKT. LOCATION	BIT 6 INT. CKT. LOCATION	BIT 7 INT. CKT. LOCATION
1	Ø8ØØ	J1	H1	F1	E1	D1	C1	B1	A1
2	18ØØ	J2	H2	F2	E2	D2	C2	B2	A2
3	28ØØ	J3	H3	F3	E3	D3	C3	B3	A3
4	38ØØ	J4	H4	F4	E4	D4	C4	B4	A4



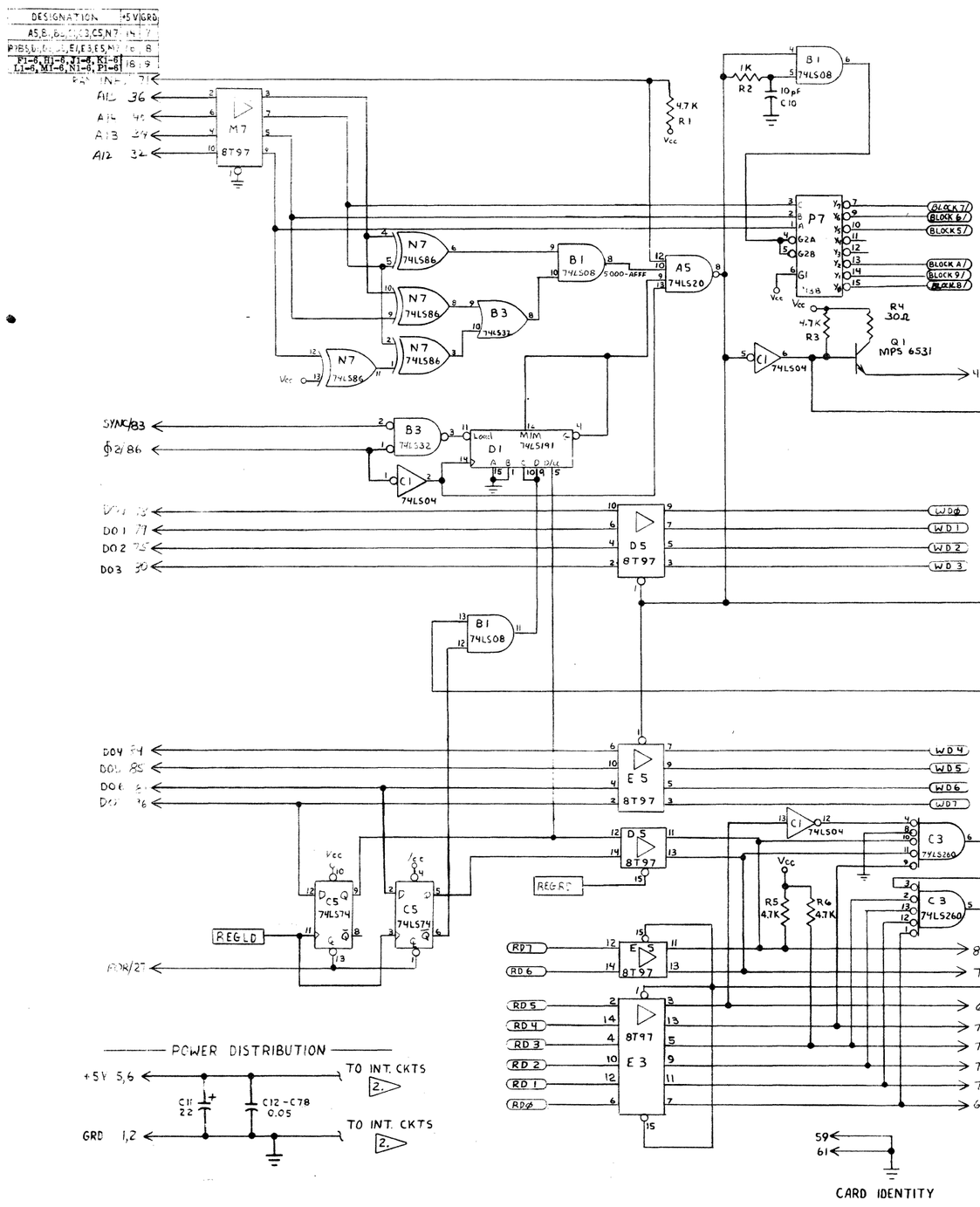
SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE
SCHEMATIC
16K RAM MEMORY

DWG SIZE	DWG NO.	REV
D	1030 B 5017	/
	SHEET 2 OF 2	

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS
   CAPACITOR VALUES ARE IN MICROFARADS
2. INT CKT DISTRIBUTION

DESIGNATION	+5V	GRD
A5,B5,C5,D5,E3,E5,M7	16	8
F1-8, H1-8, J1-8, K1-8, L1-8, M1-8, N1-8, P1-8	16	9



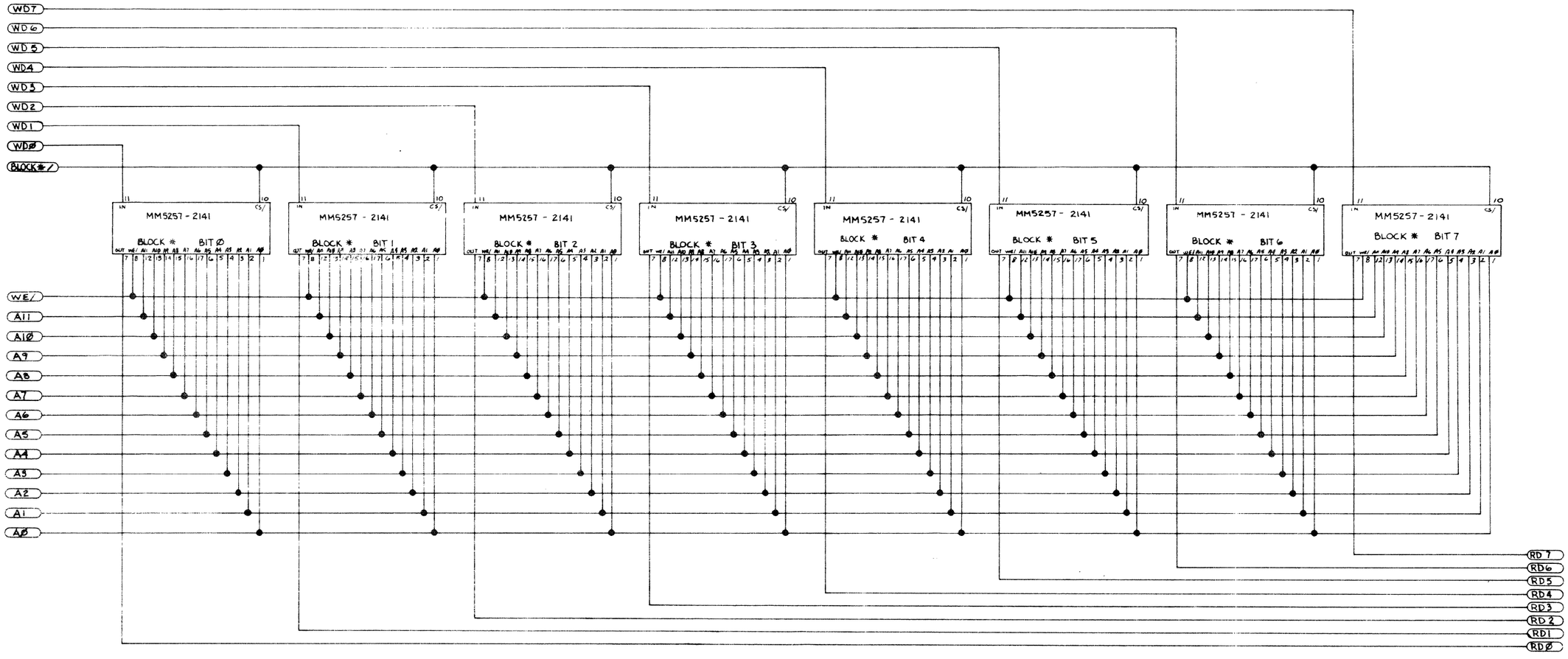
POWER DISTRIBUTION

SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE
SCHEMATIC
24K RAM MEMORY

DWG SIZE	DWG NO.	REV
D	1030B5024 SHEET 1 OF 2	A

BLOCK *	BIT Ø		BIT 1		BIT 2		BIT 3		BIT 4		BIT 5		BIT 6		BIT 7	
	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS	INT CKT LOCATION	STARTING ADDRESS
5	P1	5ØØØ	N1	5ØØØ	M1	5ØØØ	L1	5ØØØ	K1	5ØØØ	J1	5ØØØ	H1	5ØØØ	F1	5ØØØ
6	P2	6ØØØ	N2	6ØØØ	M2	6ØØØ	L2	6ØØØ	K2	6ØØØ	J2	6ØØØ	H2	6ØØØ	F2	6ØØØ
7	P3	7ØØØ	N3	7ØØØ	M3	7ØØØ	L3	7ØØØ	K3	7ØØØ	J3	7ØØØ	H3	7ØØØ	F3	7ØØØ
8	P4	8ØØØ	N4	8ØØØ	M4	8ØØØ	L4	8ØØØ	K4	8ØØØ	J4	8ØØØ	H4	8ØØØ	F4	8ØØØ
9	P5	9ØØØ	N5	9ØØØ	M5	9ØØØ	L5	9ØØØ	K5	9ØØØ	J5	9ØØØ	H5	9ØØØ	F5	9ØØØ
A	P6	AØØØ	N6	AØØØ	M6	AØØØ	L6	AØØØ	K6	AØØØ	J6	AØØØ	H6	AØØØ	F6	AØØØ



SYKES DATATRONICS, INC. ROCHESTER, NEW YORK

TITLE: SCHEMATIC — 24K RAM MEMORY

DWG SIZE: D | DWG NO. 1030B5024 | REV A | SHEET 2 OF 2

APPENDIX A

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

Bits b_7 b_6 b_5					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	ROW / COLUMN	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

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APPENDIX B

COMMANDS, CONTROL CODES AND SPECIAL CHARACTERS

TABLE A
STANDARD SYSTEM OPERATIONS

OPERATION	COMMAND NAME	USER ASSIGNED NAME
Alpha Mode	.AM	
Baud Setting Modem	.BM	
Baud Setting Printer	.BP	
Baud Setting Terminal	.BT	
Cancel (File)	.CN	
Copy	.C	
Display Directory	.DD	
Display (File)	.D	
Display Status	.DS	
Enter Automatic	.EA	
Enter (File)	.E	
Echo Mode	.EM	
Echo Mode Exit	.EX	
Included Mode	.IM	
Included Mode Exit	.IX	
Load Extension	.LE	
Load Initial	.LI	
Monitor Mode	.MM	
Monitor Mode Exit	.MX	
Print Directory	.PD	
Print (File)	.P	
Receive Automatic	.RA	
Receive (File)	.R	
Rename (File)	.RE	
Restore (Diskette)	.RE	
Send Directory	.SD	
Send (File)	.S	
Send Status	.SS	
Sequential Mode	.SM	
Standby Mode	.SB	
Write Enable	.WE	
Write Protect	.WP	

CONTROL CODE FUNCTION	STANDARD CODE	USER ASSIGNED CODE
Character Delete	RUBOUT	_____
End of Line	RETURN	_____
ETX (End of Text)	[^C]	_____
Hold	[^S]	_____
Line Cancel	[^X]	_____
Reset	[^T]	_____
Resume	[^Q]	_____
*Directory/Extension Exclusion Character	[^N]	_____

SPECIAL CHARACTERS	STANDARD SYMBOL	USER ASSIGNED SYMBOL
Directory Boundary Specification	* (see Note)	_____
"Don't Care"-for Extension	?	_____
End "Enter Automatic" Incrementing Field	>	_____
Operator Response to "SURE?" Message	Y	_____
Select Drive 1	1	_____
Select Drive 2	2	_____
Separate Command and Attached Instruction	#	_____
Separate Command and Argument	Space	_____
Separate File Name and Extension	+ (see Note)	_____
Separate File Names	/	_____
Start "Enter Automatic" Incrementing Field	<	_____
Syntax Error Response	?	_____
System Command (Modem only)	,	_____
System Command (Terminal & Modem)	.	_____

Note: These characters are also used in the File Editing (Edit) option with character string searches. See Text References.

* This character is also used in the forms operation to load files from Drive 2.

TABLE B
EDIT OPERATIONS

OPERATION	STANDARD COMMAND NAME	USER ASSIGNED NAME
Edit (into scratch pad)	.ED	_____
Append	;A	_____
Clear Buffer	;Q	_____
Delete	;D	_____
Highest Used Line #	;=	_____
Insert	;I	_____
List	;L	_____
Number & List	;N	_____
Replace	;R	_____
Search	;S	_____
Save (from scratch pad)	.SV	_____

SPECIAL CHARACTERS	STANDARD SYMBOL	USER ASSIGNED SYMBOL
Character String Delimiter	/	_____
Edit Command	;	_____
Line Number Separator	,	_____

TABLE C
FORMS OPERATIONS

OPERATION	STANDARD COMMAND NAME	USER ASSIGNED NAME
Forms Complete	.FC	_____
Forms Mode Exit	.FX	_____
Forms Variable	.FV	_____

CONTROL CODE FUNCTION	STANDARD CODE	USER ASSIGNED CODE
Character String Search	[^Y]	_____
Line Cancel	[^Z]	_____
Load Message (Drive 1)	[^O]	_____
Load Message (Drive 2)	[^N]	_____
Right Justification	Leading Space	_____
Tab (Advance Fields)	[^I]	_____

SPECIAL CHARACTERS	STANDARD SYMBOLS	USER ASSIGNED SYMBOLS
Start Forms Variable Field	]	_____
End Forms Variable Field	[	_____
Start Forms Literal Field	[^L]	_____
End Forms Literal Field	[^L]	_____

APPENDIX C

ERROR MESSAGES

Number	Message	Description
1	NOT RDY	Indicates an attempt to access a drive when a diskette was either not inserted or improperly inserted, or an attempt to access Drive 2 in a single drive system.
2	DISKETTE	Indicates the system was unable to locate the proper location on a diskette where a file is stored or will be stored. The probable cause of this error is a bad diskette.
3	BAD READ	Indicates a file or part of a file could not be read without CRC errors in twelve attempts to read the file.
4	PROTECT	Indicates an attempt to write on a protected diskette or cancel a protected file.
5	WRONG DK	Indicates the diskette is not a User Diskette or it is a bad User Diskette.
6	PREP SYS	Indicates the baud switch was not set to KYBD position when a Baud command was input. or A form was not properly loaded by the operator prior to using Forms Operations.
7	FULL DSK	Indicates the Directory is full. Either a file must be canceled from the diskette before entering a new file or a new diskette must be used.
8	NO FIND	Indicates a requested file does not exist in the Directory. Check to see that file name and extension completely agree with the Directory entry. or A search string was not found in the Forms Mode.

Number	Message	Description
9	ILLEGAL	An illegal operation has been attempted. Examples: 1.) Edit (.ED) a binary file, 2.) When in the Forms Mode, attempting to Enter a non-forms file, 3.) Requesting an Edit or Forms operation without the option installed, 4.) Don't Care or Reject character used in Alpha Mode, 5.) An Enter Automatic command issued without an Auto-Name (.LI command) loaded.
10	BAD SIZE	In Edit Mode: An attempt to Save a file with no data. In Forms Mode: The number of entries in the data file exceeds the number of variable fields in the form. The wrong form was probably loaded into the forms buffer, or The form is too big for the buffer.
11	USR TABL	Indicates the system detected an improper command from the User Command Table. The User Command Table must be corrected using the Configuration Diskette.
12	MODEM	Indicates an improper condition has been detected at the modem interface. One of the following conditions exist: 1.) Clear To Send was not asserted within 400 msec after Request To Send was asserted,

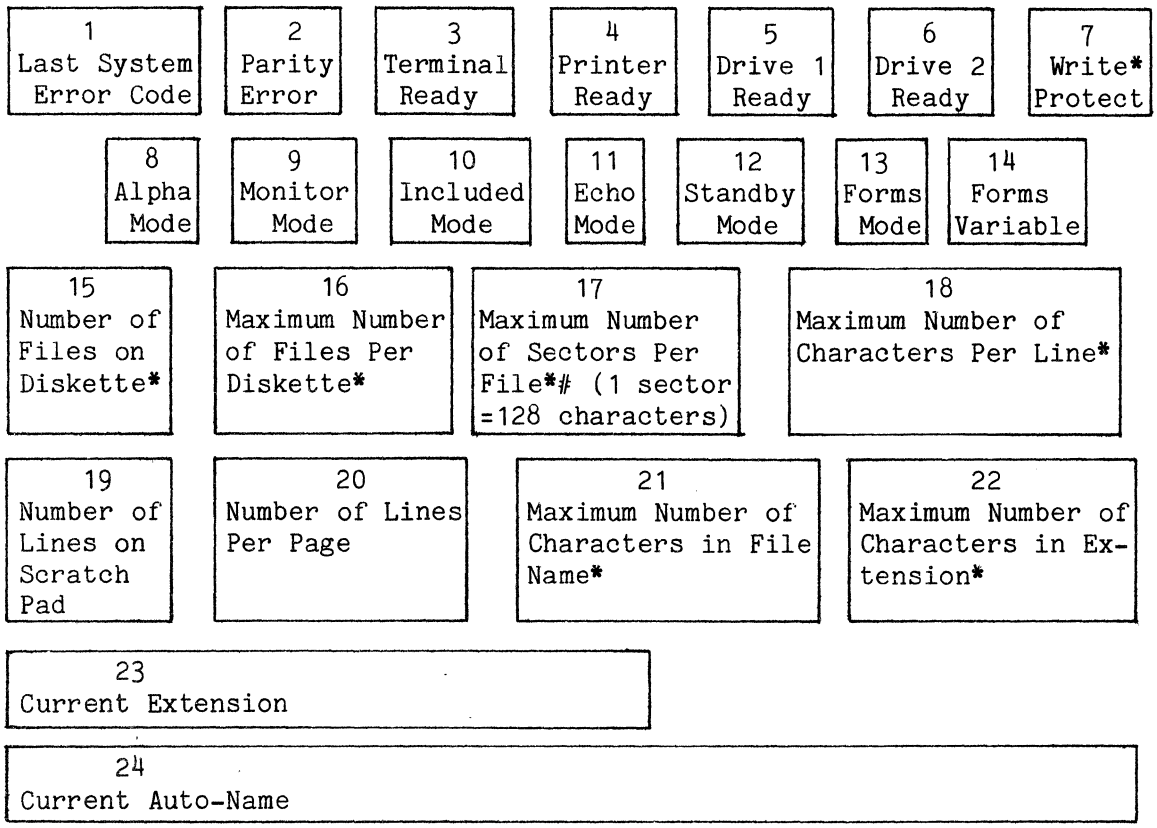
Number	Message	Description
		2.) Data Set Ready was not asserted when attempting to perform a Send, Send Directory or Send Status command.
13	NO ROOM	Indicates a file being Edited or Saved from the scratch pad is larger than the configured maximum file length. or An attempt was made to exceed the capacity of the scratch pad with an Edit, Insert, Replace or Append command. or When merging a file in the Forms Mode, the forms data field is too small for the forms data. or An attempt was made to Edit a file on a diskette which was not configured to have a scratch pad. or A Search/Replace operation results in a line length exceeding the configured value.
14	OVERRUN	Input data in either the Enter or Receive Mode has exceeded the input rate or file capacity of the system and data is lost. or The modem or terminal buffer has been filled beyond its configured capacity. or An illegal buffer configuration exists.
0	SYSTEM	Indicates that the system has detected an equipment problem, or a diskette with a bad Directory.

Number	Message	Description
		If the error occurs when another diskette is used, the operator should note the conditions which created the error and contact maintenance personnel.
—	?	An improper command has been entered. Example: .CM was entered instead of .CN. or A variable length file command (.DS S, .SS S, or .RE with no file name/extension arguments) is entered for a fixed length file diskette.
		A character was entered at the terminal and sent to the modem port when Data Set Ready was not present. This error usually occurs when the operator forgets to enter a period to symbolize the start of a command.
		Note: The bell signal is also used to indicate the completion of an Enter or Enter Automatic operation.
15		Reserved for future expansion.

APPENDIX D

STATUS

STATUS DISPLAY FORMAT
(For Both Send Status and Display Status)



*These items are controlled by the particular User Diskette in use. See "Configuration Manual" for instruction in building User diskettes.

#This field will contain "+" characters if a variable length file type diskette is being used.

STATUS DISPLAY EXPLANATION

1. LAST SYSTEM ERROR CODE

Indicates the number of the last system error message if any system errors have occurred. If no errors have occurred, the response is "N" for None.

2. PARITY ERROR

A response of "Y" for Yes indicates that a parity error has occurred at either the modem or terminal port while data was being received by Comm-Stor. This condition can be cleared only by issuing a Reset command from either modem or terminal, or by depressing the RESTART button. A response of "N" for No indicates that no parity error has occurred since the last Reset command was issued. Note that Comm-Stor may be configured to consider a framing error to be the same as a parity error. See "Configuration Manual."

3. TERMINAL READY

A response of "Y" indicates that the terminal is on-line and ready to send/receive data. A response of "N" indicates that the terminal is not ready. Probable causes: terminal not switched on-line; terminal does not have a Data Terminal Ready signal (see "Configuration Manual"); incorrect cable from terminal to Comm-Stor; terminal power off.

4. PRINTER READY

Similar to TERMINAL READY above but applies to printer only.

5. DRIVE 1 READY

A response of "Y" indicates that a diskette is in place in Drive 1, the door is closed and the diskette is spinning at the proper speed. A response of "N" indicates that the above is not true. Probable causes: door is open and/or diskette not in place; unit is in Standby Mode (also indicated in status display); hardware malfunction.

6. DRIVE 2 READY

As above but applies to Drive 2.

7. WRITE PROTECT

The diskette whose status is being displayed (.DS or .DS2) is Write Protected. The user must unprotect the diskette before any operation which writes data on the disk can be performed. The .WE (Write Enable) command is used for this purpose. This does not reflect the individual file status. Therefore, each file must be individually Write Enabled (if it is Write Protected) in order to write data into it.

8. ALPHA MODE

A response of "Y" indicates that Comm-Stor is in the Alpha Mode. A response of "N" indicates that it is not in the Alpha Mode and therefore is in the Sequential Mode.

9. MONITOR MODE

A response of "Y" indicates that Comm-Stor is currently in the Monitor Mode. A response of "N" indicates that Comm-Stor is not currently in this mode (.MX).

10. INCLUDED MODE

A response of "Y" indicates that Comm-Stor is currently in the Included Mode. A response of "N" indicates that Comm-Stor is not currently in this mode (.IX).

11. ECHO MODE

A response of "Y" indicates that Comm-Stor is currently in the Echo Mode. A response of "N" indicates that Comm-Stor is not currently in this mode.

12. STANDBY MODE

A response of "Y" indicates that Comm-Stor is currently in the Standby Mode. A response of "N" indicates that Comm-Stor is not currently in this mode.

CAUTION: Diskettes must NEVER be inserted in the disk while the unit is in Standby Mode since this may cause permanent damage to the diskette!

13. FORMS MODE

A response of "Y" indicates that Comm-Stor is currently operating in either the Forms Variable or Forms Complete Mode. A response of "N" indicates that the above is not the case (.FX).

14. FORMS VARIABLE

If the response to Item 13 above is "Y", the FORMS VARIABLE response is used to distinguish between Forms Variable (response = "Y") and Forms Complete (response = "N") modes.

15. NUMBER OF FILES ON DISKETTE

This value indicates the number of files currently stored on the diskette and corresponds exactly to the number of file names in the Directory of the diskette.

16. MAXIMUM NUMBER OF FILES PER DISKETTE

This value indicates the maximum number of files that can be stored on the diskette. This may be different for different diskettes. Item 16 minus Item 15 equals the number of files that can be added to the diskette before it becomes full.

17. MAXIMUM NUMBER OF SECTORS PER FILE

Fixed Length Files:

Comm-Stor stores files on the diskette in groups of 128 characters called sectors. Item 17 indicates the maximum number of sectors each file may occupy. To convert this to the maximum number of characters allowable in any file, multiply the number of sectors by 128.

Example: 5 sectors x 128 characters/ sector = 640 characters. This may be different for different diskettes.

Variable Length Files:

Since files stored on a diskette configured for variable length files are not restricted to a certain size (other than the capacity of the diskette) this field will contain "+" characters rather than a numeric value. This provides the user with a quick means of determining if a diskette is configured for fixed length or variable length files.

18. MAXIMUM NUMBER OF CHARACTERS PER LINE

This value is used to set up the scratch pad when the Edit option is used and to determine by how many characters per line the Editor will accept. This value may vary from diskette to diskette.

19. NUMBER OF LINES ON SCRATCH PAD

This specifies the maximum number of lines of characters the scratch pad area can accept. An attempt to exceed this value will result in an error message. This number varies from diskette to diskette.

20. NUMBER OF LINES PER PAGE

This indicates the number of lines that Comm-Stor will output to the terminal or printer before pausing to allow the operator to examine the screen (page). The next page will be displayed when the operator strikes any key on the terminal.

21. MAXIMUM NUMBER OF CHARACTERS IN FILE NAME

This value indicates the maximum number of characters in any file name. Specifying a name longer than this will cause an error.

22. MAXIMUM NUMBER OF CHARACTERS IN THE EXTENSION

This value indicates the maximum number of characters in any extension. Specifying an extension longer than this will cause an error.

23. CURRENT EXTENSION

Indicates the current extension for new files. Any new file created will have this extension until the extension is changed by using the Load Extension (.LE) command. If no extension has been entered, no output will appear. If an extension is specified (and allowed) in the command string (ex. .R ABLE+DEPT B.), then that extension will be used instead of the current extension. The current extension will, however, remain intact.

24. CURRENT AUTO-NAME

Indicates the next file name that will be used when the Enter Automatic or Receive Automatic command is used. If no Auto-Name has been entered, no output will appear.

STATUS STRING FORMAT

Sequence of characters sent to modem or terminal during a Send or Display Status operation. All multiple character strings may contain leading spaces.

```
2 Character String - Status Item #1
Space
1 Character        - Status Item #2
Space        .            .
  .          .            .
  .          .            .
  .          .            .
1 Character        - Status Item #7
Carriage Return
Space
Character String   - Status Item #8
Space
1 Character        - Status Item #9
Space        .            .
  .          .            .
  .          .            .
  .          .            .
1 Character        - Status Item #14
Carriage Return
5 Character String - Status Item #15
5 Character String - Status Item #16
5 Character String - Status Item #17
5 Character String - Status Item #18
Carriage Return
5 Character String - Status Item #19
5 Character String - Status Item #20
5 Character String - Status Item #21
5 Character String - Status Item #22
Carriage Return
Character String   - Status Item #23
(length =1 maximum configured file name
length)
Carriage Return
Character String   - Status Item #24
(length =1 maximum configured extension
length)
Carriage Return
```

Notes:

1) All Carriage Returns at the terminal port are followed by a line feed. Line feed characters are added at the modem port for certain configurations.

2) Items 15 through 22 have a minimum of 1 leading space within the 5 character string.

3) Items 23 and 24 have a single space when no Auto-Name or extension exist.

APPENDIX E

DISKETTE CAPACITY CHART

FOR FIXED LENGTH FILES

The following chart has been prepared to give the operator typical data concerning diskette capacity for diskettes configured for fixed length files. The first column is the maximum number of characters in any file, the second is the maximum number of characters or range of characters in the file name, and the third is the maximum number of characters or range of characters in the extension. Numerous additional combinations of these variables are also possible. The "Configuration Manual" should be consulted for additional information. Note that the above data is for diskettes using only tracks 1 through 73. Those operators who do not use these diskettes with IBM equipment and elect to use tracks 1 through 76 can expect approximately 4 to 5 per cent additional file capacity.

Characters/File	File Name	Extension	Number of Files
128	4	0	1742
128	12	4	1586
128	20	12	1404
250	4	0	910
250	12	4	858
250	20	12	806
500	4	0	461
500	20	12	435
1000	4	0	234
1000	20	12	227
2000	4	0	117
2000	20	12	115
4000	4-20	0-12	58
8000	4-20	0-12	29
16000	4-20	0-12	14
32000	4-20	0-12	7

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APPENDIX F

SYSTEM DELAYS

Comm-Stor has a Directory which contains a cross-reference between user assigned file names and file addresses on the diskette. Being disk-based, the system requires address searching on the diskette before either reading or writing can take place anywhere on the diskette. Delays thus occur before Comm-Stor responds to certain commands, and the operator or remote computer must insert delays where required.

Comm-Stor BUFFER OPTION

Comm-Stor systems equipped with the Buffer option can be configured with buffer areas large enough to allow data input to continue during Directory searches and diskette accesses. For example, a Receive command (.R) entered from the modem port may be immediately followed by the data to be received. As it is received, this data will be automatically buffered within Comm-Stor while the diskette is being prepared to write this file. The longer this preparation takes (usually directly proportional to the number of files currently residing on the diskette) and the higher the modem baud rate, the larger the modem buffer must be configured. For Comm-Stor systems operating at baud rates of 1200 or less, a 1K modem buffer will usually be adequate. (Refer to Appendix D in the Configuration Manual.)

Comm-Stor DELAYS

1. Delays after an Enter or Receive Command

After Comm-Stor receives an Enter, Enter Automatic, Receive or Receive Automatic command, a certain amount of time is required for the system to locate a vacant entry in the Directory and to find the starting position on the diskette where the data will be stored. Systems not equipped with the buffer option must be provided with a delay before data transfer begins to allow the Directory look up operation. The amount of delay depends on the number of files on the diskette, the maximum number of files and the maximum number of characters in the file name. Because these values can vary from diskette to diskette, it is not practical to determine them for each case. Therefore, two alternate approaches are considered.

First, when working from a terminal, the system withholds the Return and Line Feed until it is ready to accept data. Second, when the data is to be received from a modem, the Attached Instruction (see Chapter 6) is not sent out until after this delay, thus using it as a prompt to the remote computer. If this is not possible, a delay of 14 seconds should be allowed to cover the worst case, although typically a delay of less than a second is required.

2. Delays after an Enter or Receive Operation:

After the ETX character is received, signifying termination of an Enter or Receive Mode, Comm-Stor must "close out" the file by entering certain parameters in the Directory. When data is entered from the terminal, the bell will sound on the terminal when the system is ready for the next command. When data is received from the modem port, the remote computer should allow 14 seconds to cover the worst case. As an alternate Comm-Stor may be configured (Parameter #2) to transmit an EOT character out the modem port after completion of any operation initiated by a command received at that port. In addition, the remote computer may "test" Comm-Stor to see if the system is ready by repeatedly sending a Display Status command to the system. When status information is received by the computer, that is an indication that Comm-Stor has closed out the Enter or Receive Mode. The computer may issue a Reset command to halt the Display Status operation or wait until the Status operation has been completed. 350 msec after the Reset command, the system will

be in an idle state, capable of receiving the next command.

3. **Delays after a Display, Send or Print Command:**

When Comm-Stor receives a Display, Send or Print command, there is a maximum pause of up to 14 seconds before data is sent. This is a maximum, and typical delays are less than one second. There may also be a delay within the Send, Display or Print Directory operations, even though initial data is sent as soon as the command is received.

4. **Delays after a Display, Send or Print File Operation:**

No delay is necessary after the last character of a Display, Send or Print operation. The next command may be issued immediately.

5. **Delays During the Reception of Data:**

Under normal conditions, Comm-Stor receives a continuous stream of data without requiring pauses in the data stream. However, if a search error occurs while Comm-Stor is looking for a diskette address, the system may be unable to handle the incoming data. If data is lost, an Overrun Error occurs. To prevent this error, the system may be configured to send a Stop Send character to the computer, and send a Start Send character after Comm-Stor has "caught up". Refer to the "Configuration Manual" for details concerning these commands.

Comm-Stor
SERVICE MANUAL

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