SCD-DLV11E
Asynchronous Serial Line Interface
Manual

Σ Sigma Information Systems

MA400360 REV. A

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Asynchronous Serial Line Interface
Manual

ANAHEIM, CALIFORNIA - AUGUST 1984

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Section 1 - General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and program the SCD-DLV11E Asynchronous Serial Line Interface, which replaces DEC's* DLV11-E module. The SCD-DLV11E is manufactured by Sigma Information Systems located in Anaheim, California.

The material in this manual is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the SCD-DLV11E. Specifications are included.

Section 2 - INSTALLATION. This section explains the procedures for equipment installation. Switch settings and jumper installations that control system configuration are defined.

Section 3 - PROGRAMMING CONSIDERATIONS. This section contains register data bit functions for programming the SCD-DLV11E.

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1.2 GENERAL DESCRIPTION

The SCD-DLV11E is an asynchronous line interface between the LSI-11 bus and a serial communication device. It replaces DEC's* DLV11-E and is software compatible with operating systems and diagnostics designed for the DEC module.

The dual-wide module converts parallel data from the LSI-11 bus to serial data for peripheral devices, and it converts serial data from peripheral devices to to parallel data for the LSI-11 bus. It provides full modem control and an EIA-type interface.

The SCD-DLV11E module has switch selectable baud rates from 50 to 19.2K; the baud rate can be either common or split (independent transmit and receive speeds). The module also provides a switch selectable data word format that defines parity type, character length, and stop/start bits.

1.3 FEATURES

- Full modem control
- External clock input for user-defined baud rate control
- Switch selectable device address and vector interrupt
- Switch selectable baud rates and data format
- Can be used as console interface
- Full duplex operation

1.4 INTERFACE SIGNALS

Table 1-1 is defines the interface signals for the SCD-DLV11E.

	BURG		3M BURG	
3M	PIN	SIGNAL	PIN	SIGNAL
40	A	Protective Ground	23 V	Request to Send
39	B	Signal Ground	22 X	Ring Indicator
38	C	Force Busy	17 BB	Carrier
36	E	EIA Interlock	15 DD	Data Terminal Ready
35	F	Transmitted Data	13 FF	Secondary Transmitted Data
33	J	Received Data	11 JJ	Secondary Received Data
30	M	EIA Interlock	2 UU	Signal Ground
25	T	Clear to Send	1 VV	Protective Ground

TABLE 1-1: SCD-DLV11E INTERFACE SIGNALS

1.5 SPECIFICATIONS

Power Requirements:	+ 5VDC @ 1.0A +12VDC @ 1.18A
Interface:	Standard EIA RS-232-C/CCITT V.24 with full modem control (Bell 103, 113, 202C, 202D, and 212)
Operating Mode:	Full duplex
Device Address:	Switch selectable: 160000 through 177770 Shipped at 175610. Console address at 177560
Vector Interrupt:	Switch selectable: 000 through 770 Shipped at 300 (receive), 304 (transmit) Console interrupts at 60 and 64
Baud Rate:	Switch selectable: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, or 19.2K
Data Format:	
Character Bits:	5, 6, 7 or 8
Parity:	Odd, even, or none
Stop Bits:	1, 1-1/2 (5 level codes only), or 2
Start Bits:	1
Bus Load:	1
Installation:	Plugs directly into any dual-wide Q bus slot
Cabling:	Requires 40-conductor cable (not included) to peripheral device.
Temperature	
Operating:	5°C to 50°C
Storage:	-45°C to 85°C
Humidity:	10% to 95% noncondensing
Altitude	
Operating:	0 ft. to 10,000 ft.
Storage:	0 ft. to 30,000 ft.

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SCD-DLV11E is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SCD-DLV11E and visually inspect for physical damage that might have occurred during shipment. If any damage has occurred, notify the factory immediately.

2.2 FACTORY-SET PARAMETERS

The SCD-DLV11E is shipped configured with DEC standard operating parameters as defined in Table 2-1. The location of the jumpers and switches that determine these parameters is shown in Figure 2-1.

SWITCH PARAMETER	SELECTION	JUMPER PARAMETER	SELECTION
Device Address	175610	Baud Type	Common
Interrupt Vector	300	Boot ROM	Disabled
Transmit/Receive Baud Rate	19.2K	DTR	Controlled by RCSR
Programmable Baud Rate	Enabled		Cleared by RESET
Data Bits/Stop Bits	8/1	RTS	Connected to RTS pin
Parity	Disabled		

TABLE 2-1: FACTORY-SET PARAMETERS

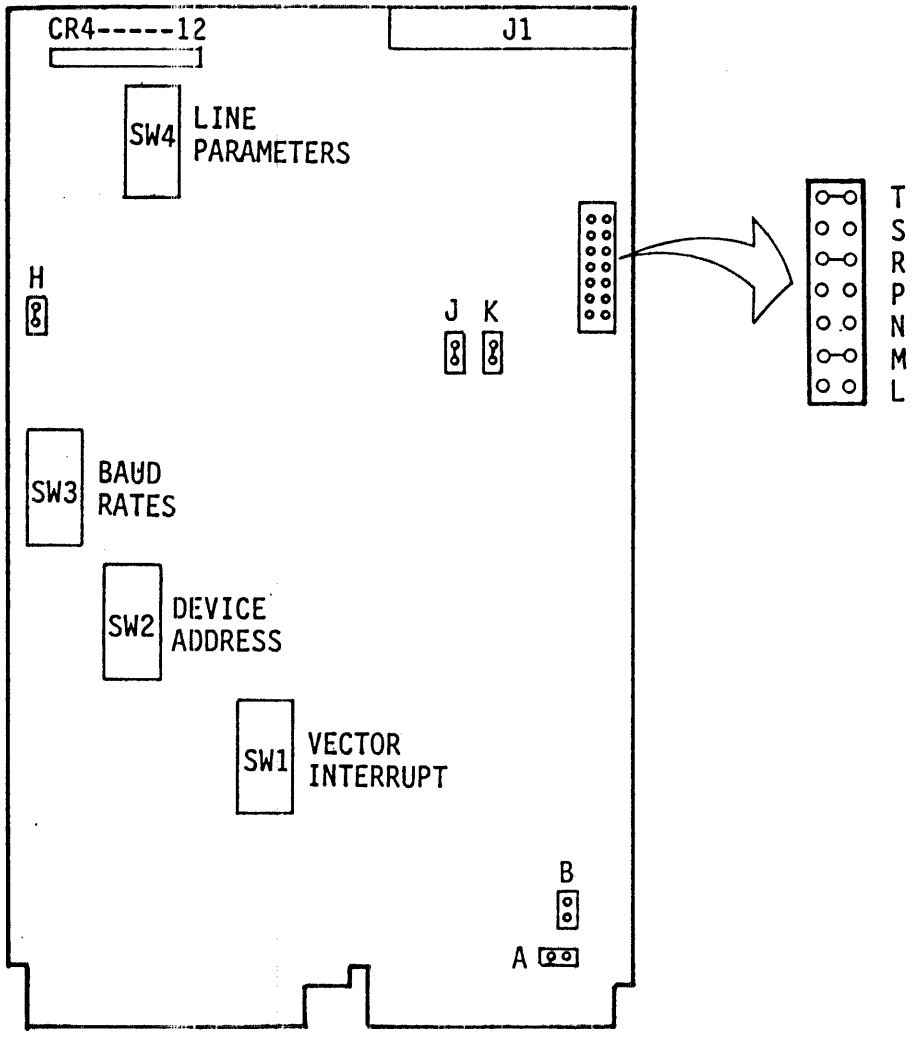


FIGURE 2-1: FACTORY-SET JUMPER & SWITCH LOCATIONS

Before installing modules, verify that these configurations are properly installed. The following sections describe the procedures to verify and/or reconfigure these operating parameters.

2.3 SWITCH SELECTABLE PARAMETERS

The interrupt vector, device address, baud rates, and line parameters are set by switches SW1, SW2, SW3, and SW4, respectively.

2.3.1 Device Address Selection

The device address lies in the range of 160000 to 177770 and is selected by setting switch SW2. The SCD-DLV11E is shipped with DEC standard device address 175610. If the SCD-DLV11E is to be used as the console device, the device address should be reset to 177560.

Address bits A12 through A03 are determined by SW2 . Bits A02 and A01 are hard-wired to implement four device registers defined in Table 2-2.

REGISTER	MNEMONIC	CONSOLE	STANDARD
Receiver Control/Status	RCSR	177560	175610
Receiver Data Buffer	RBUF	177562	175612
Transmit Control/Status	XCSR	177564	175614
Transmit Data Buffer	XBUF	177566	175616

TABLE 2-2: STANDARD REGISTER ADDRESSES

Use the following examples to set SW2. Notice that OFF = 1 and ON = 0.

Set default standard address 175610.

ADDRESS BITS	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
SW2 POSITIONS:	10	9	8	7	6	5	4	3	2	1
SW 2 SETTINGS:	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF
SW2 VALUES	1	1	0	1	1	1	0	0	0	1
ADDRESS: 1	7		5			6			1	0

Set address 177560.

ADDRESS BITS	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
SW2 POSITIONS:	10	9	8	7	6	5	4	3	2	1
SW2 SETTINGS:	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
SW2 VALUES	1	1	1	1	1	0	1	1	1	0
ADDRESS: 1	7		7			5			6	0

EXAMPLE 2-1: ADDRESS SELECTION (SW2)

2.3.2 Interrupt Vector Selection

Interrupt bits V8 through V3 are determined by setting switch SW1 positions 8 through 3. The vectors can range from 000 through 770. The default vector is 300, which implements receive interrupts at 300 and transmit interrupts at 304. If the SCD-DLV11E is used as the console device, the receive interrupt should be set to 060, which implements a transmit interrupt at 064.

If a DRV11 parallel interface is installed that starts at address 300, the SCD-DLV11E should be assigned vectors following 300.

Use the following examples to set SW1. Notice that OFF = 1 and ON = 0.

Set default interrupt vector 300.

VECTOR BITS	V8	V7	V6	V5	V4	V3	
SW1 POSITIONS:	8	7	6	5	4	3	
SW1 SETTINGS:	ON	OFF	OFF	ON	ON	ON	
SW1 VALUES:	0	1	1	0	0	0	
VECTOR INTERRUPT:		3			0		0

Set console interrupt vector 60.

VECTOR BITS	V8	V7	V6	V5	V4	V3	
SW1 POSITIONS:	8	7	6	5	4	3	
SW1 SETTINGS:	ON	ON	ON	OFF	OFF	ON	
SW1 VALUES:	0	0	0	1	1	0	
VECTOR INTERRUPT:		0			6		0

Set vector interrupt 240.

VECTOR BITS	V8	V7	V6	V5	V4	V3	
SW1 POSITIONS:	8	7	6	5	4	3	
SW1 SETTINGS:	ON	OFF	ON	OFF	ON	ON	
SW1 VALUES:	0	1	0	1	0	0	
VECTOR INTERRUPT:		2			4		0

EXAMPLE 2-2: VECTOR INTERRUPT SELECTION (SW1)*

*NOTE: SW1 positions 1 and 2 are not used.

2.3.3 Baud Rate Selections

The SCD-DLV11E is shipped with baud rate at 19.2K for both transmit and receive speeds. The transmit baud rate can be set independently of the receive baud rate providing jumpers P, R, S, and T (Section 2.4) are installed correctly. Table 2-3 defines switch SW3 settings for baud rates.

BAUD RATE	------RECEIVE SPEED------- SW3-1 | SW3-2 | SW3-3 | SW3-4 ------TRANSMIT SPEED------ SW3-5 | SW3-6 | SW3-7 | SW3-8			
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
300	ON	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	ON	OFF	OFF	OFF
1800	OFF	ON	ON	ON
2000	OFF	ON	ON	OFF
2400	OFF	ON	OFF	ON
3600	OFF	ON	OFF	OFF
4800	OFF	OFF	ON	ON
7200	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
*19.2K	OFF	OFF	OFF	OFF

*Factory set.

TABLE 2-3: BAUD RATE SELECTION (SW3)

Use the following example to set SW3.

Set transmit baud to 9600 and receive baud to 2400

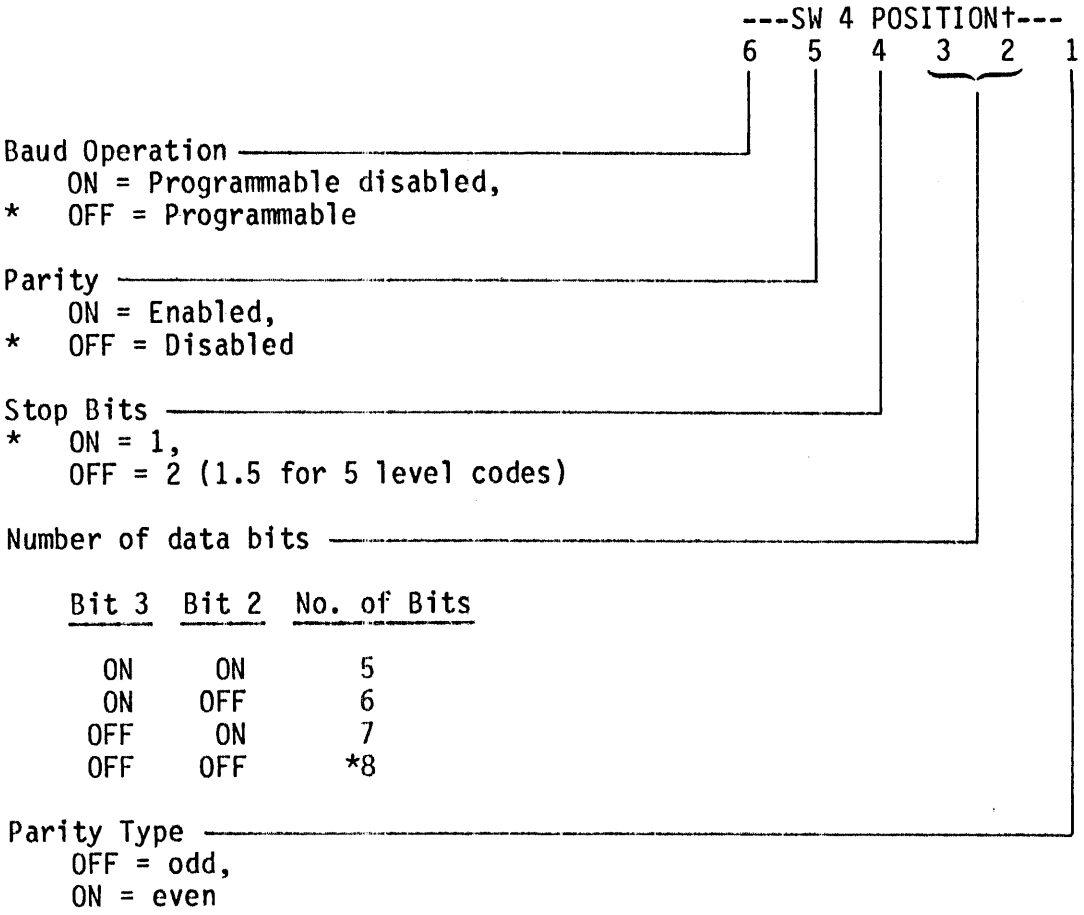
SW3 POSITIONS	8	7	6	5	4	3	2	1
SW3 SETTINGS:	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
BAUD RATE:	9600 TRANSMIT				2400 RECEIVE			

EXAMPLE 2-3: BAUD RATE SELECTION (SW3)

The SCD-DLV11E is shipped with programmable baud rate enabled (Section 2.3.4). Baud rates can be set by bit 15 through bit 12 of the XCSR (Section 3.4), which overrides the switch selected baud rates.

2.3.4 Data Word Format Selection

The data word format is set by switch SW4 as defined below.



Bit 3	Bit 2	No. of Bits
ON	ON	5
ON	OFF	6
OFF	ON	7
OFF	OFF	*8

*Factory set.

†NOTE: SW4 positions 7 and 8 are not used.

2.4 SYSTEM CONFIGURATION JUMPERS

The configuration jumpers shown in Figure 2-1 determine system operation such as interface signal function and split/common baud. These jumpers are defined in Table 2-4.

JUMPER	STATUS	DESCRIPTION
A	IN	Halt on framming error
B	IN	Boot on framing error
H	*IN OUT	Disable boot ROM Enable boot ROM
J	*IN OUT	DTR controlled by bit of RCSR DTR forced true
K	*IN OUT	DTR bit cleared by RESET DTR bit unaffected by RESET
L	IN	Connects RTS to Force Busy line
M	*IN	Connects RTS to RTS pin
N	IN	Enables transmit baud out
P	IN	Enables split baud operation
R	*IN	Enables common baud operation
S	IN	Enables split baud operation
T	*IN	Enables commond baud operation

*Factory set.

TABLE 2-4: CONFIGURATION JUMPERS

2.5 LED INDICATORS

The SCD-DLV11E module contains eight LED indicators (Figure 2-1). When the LED is off, the line is in mark state. When the LED is lit, the line is in the space state. The LEDs and their associated signals are shown in Table 2-5.

LED	SIGNAL	MNEMONIC
CR4	Received Data	RCV DATA
CR5	Transmitted Data	XMIT DATA
CR6	Request to Send	RTS
CR7	Data Terminal Ready	DTR
CR8	Secondary Transmitted Data	SEC XMIT
CR9	Ring	RING
CR10	Secondary Received Data	SEC REC
CR11	Clear to Send	CTS
CR12	Carrier	CAR

TABLE 2-5: LED INDICATOR SIGNALS

Section 3 - Programming Considerations

3.1 INTRODUCTION

Communications between the processor and the SCD-DLV11E are executed via programmed I/O operations or interrupt-driven routines. This section describes the programming instructions for the following registers:

RCSR	Receiver Control/Status
RBUF	Receiver Data Buffer
XCSR	Transmit Control/Status
XBUF	Transmit Data Buffer

The RCSR and the XCSR are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

The RBUF and XBUF provide double-buffering; one byte of data can be held while another byte is entering or exiting. This permits asynchronous, full-duplex operation. Data is manipulated in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF; it also sends a status bit to the RCSR and a framing error bit to the break logic.

3.2 RECEIVER CONTROL STATUS REGISTER (RCSR)

The register word format for the receiver control status register is:

15	14	13	12	11	10	9 8	7	6	5	4	3	2	1	0
DATA SET INT	RING	CLR TO SEND	CAR DET	RCVR ACT	SEC REC	RESERVED	RCVR DONE	RCVR INT ENB	DSET INT ENB		SEC XMIT	REQ TO	DTR	

DATA SET INT — DATA SET INTERRUPT. Initiates an interrupt sequence if DSET INT ENB is also enabled.

This bit is set whenever CAR DET, CLR TO SEND, or SEC REC chanages state (from 0 to 1 or from 1 to 0); it is also set when RING changes from 0 to 1. Cleared by INIT or by reading the RCSR. Since reading the register clears DATA SET INT bit, this bit is effectively a "read-once" bit.

RING — RING. When set, this bit indicates that a ringing signal is being received from the data set. The ringing signal is not a level, but rather an EIA control with a duty cycle of 2 seconds ON and 4 seconds OFF. Read only.

CLR TO SEND — CLEAR TO SEND. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition. The ON or OFF state is dependent on the state of the clear to send signal from the data set. Read-only.

CAR DET — CARRIER DETECT. This bit is set when the data carrier is received. It is cleared at the end of the current transmission or when an error condition occurs. Read only.

RCVR ACT — RECEIVER ACTIVE. When the SCD-DLV11E receiver is active this bit is set at the center of the start bit, which is the beginning of the serial input data. Cleared by the leading edge of RCVR DONE H (bit 7) or by INIT. Read only.

SEC REC — SECONDARY RECEIVED DATA. Provides a receive capability for the reverse channel of a remote station where a space (+6V) is read as a 1. Read only.

RCVR DONE — RECEIVER DONE. Set when an entire character has been received and is ready for transfer to the CPU. It initiates an interrupt sequence when set, provided RCVR INT ENB is also set. Cleared by INIT or when RBUF is addressed. Read only.

RCVR INT ENB RECEIVER INTERRUPT ENABLE. When set, it permits an interrupt sequence to begin if RCVR DONE is also set. Cleared by INIT. Read/write.

DSET INT ENB DATA SET INTERRUPT ENABLE. When set, it permits an interrupt sequence to begin if DATA SET INT is also set. Cleared by INIT. Read/write.

NOTE

Set the appropriate CPU status bit = 1 before clearing an interrupt enable bit. When the interrupt enable bit at the device is cleared, the CPU may be returned to its normal priority.

SEC XMIT SECONDARY TRANSMIT. Provides a transmit capability for a reverse channel of a remote station. When set, a space (approximately +11.5V) is transmitted. Cleared by INIT. Read/write.

REQ TO SEND REQUEST TO SEND. A control lead to the data set, which is required for transmission. This bit is connected to the RTS lead (jumper M) or to the Force Busy lead (jumper L) in the data set. See Section 2.4 for jumper definitions. Cleared by INIT. Read/write.

DTR DATA TERMINAL READY. A control lead for the data set. The channel is connected when this bit is set, and is disconnected when this bit is cleared. See Section 2.4 for DTR jumper functions. Cleared by the program or by RESET (if jumper K is installed). Read/write.

NOTE

The state of this bit is not defined after power-up.

3.3 RECEIVER DATA BUFFER (RBUF)

The word format for the receiver data buffer register is:

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
ERR	OR ERR	FR ERR	P ERR	RESERVED	RECEIVED DATA BITS

ERR — ERROR. Indicates that an error condition has occurred. This bit is the logical OR of OR ERR, FR ERR, and P ERR bits, which cause ERROR to be set. Not connected to the interrupt logic. Cleared by removing the error condition.

NOTE

Error indicators remain in effect until the next character is received, at which time the error bits are updated. Error bits are cleared by INIT.

OR ERR — OVERRUN ERROR. Is set when the previously received character was not completely read (RCVR DONE not cleared) prior to receiving a new character. Cleared by INIT. Read only.

FR ERR — FRAMING ERROR. When set, indicates that the character that was read had no valid stop bit. Cleared by INIT. Read only.

P ERR — PARITY ERROR. When set, indicates the received parity does not match the expected parity. Always 0 if no parity is selected. Cleared by INIT. Read only.

BITS 7-0 — RECEIVED DATA. Holds the most recent character that has been read. If data is less than eight bits, the buffer is right-justified into the least significant bit positions, with the high bits read as 0's. Not cleared by INIT. Read only.

3.4 TRANSMIT CONTROL STATUS (XCSR)

The word format for the transmit control status register is:

15	14	13	12	11	10 9 8	7	6	5 4 3	2	1	0
PBR SEL 3	PBR SEL 2	PBR SEL 1	PBR SEL 0	PBR SEL ENB	RESERVED	XMIT RDY	XMIT INT ENB	RESERVED	MAIN	RE SERV ED	BRK

PBR SEL — PROGRAMMABLE BAUD RATE SELECT. When set (bit = 1), these bits select a baud rate from 50 to 19.2K baud.

BAUD RATE	BIT 15	14	13	12
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2000	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600	1	1	1	0
19.2K	1	1	1	1

Setting bits 15 through 12 overrides SW3 baud rate selection (Section 2.3.3). Bit 11 (PBR SEL ENB) must be set for these value to be effective. Write only.

PBR SEL ENB — PROGRAMMABLE BAUD RATE ENABLE. This bit must be set for the baud rates defined by bits 12 through 15 to be effective. Also, switch SW4-6 must be OFF (Section 2.3.4). Write only.

XMIT RDY — TRANSMITTER READY. This bit is set when XBUF can accept another character, at which time it initiates an interrupt sequence if XMIT INT ENB is also set.

XMIT INT ENB — TRANSMITTER INTERRUPT ENABLE. When set, permits an interrupt sequence to start when XMIT RDY is set. Cleared by INIT. Read/write.

NOTE

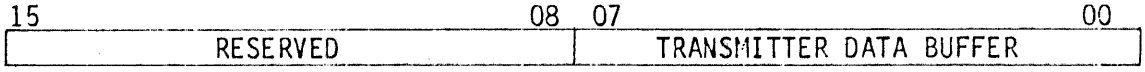
Set the appropriate CPU status word bit = 1 before clearing an interrupt enable bit. When the interrupt enable bit at the device is cleared, the CPU may be returned to its normal priority.

MAIN MAINTENANCE. Used for maintenance function. When set, the transmitter serial output is connected to the receiver serial input, and the external device is disconnected from the receiver serial input. Also forces the receiver to run at transmitter baud rate when split speed operation is enabled. Cleared by INIT. Read/write.

BRK BREAK. When set, transmits a continuous space to the external device. Cleared by INIT. Read/write.

3.5 TRANSMIT DATA BUFFER (XBUF)

The word format for the transmit data buffer is:



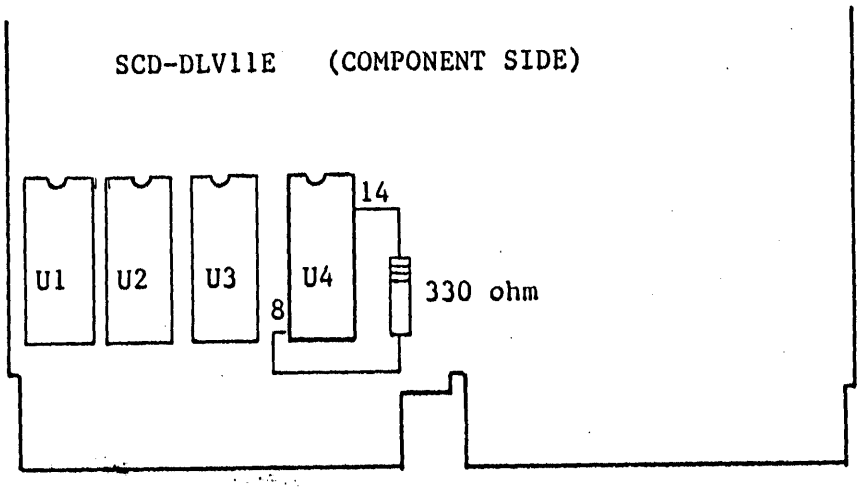
Bits 07 through 00 hold the character to be transferred to the external device. If the character is less than eight bits, it is right-justified into the least significant bits. Read as 0's. Write only.

Technical Bulletin

NUMBER	PRODUCT: SCD-DLV11E	RELEASED BY	PAGE 1 OF 1
TB145	PREVENTING ODD-NUMBERED INTERRUPTS ON 11/73	B. TRUJILLO	4/10/86

If the SCD-DLV11E is used with LSI-11/73, the CPU will trap on odd-numbered vector interrupts.

To prevent the SCD-DLV11E from generating odd-numbered interrupts solder a 330 ohm, 1/4 watt resistor from U4 pin 8 to U4 pin 14. The resistor should be soldered on the component side of the module. (U4 is a 16-pin IC.)



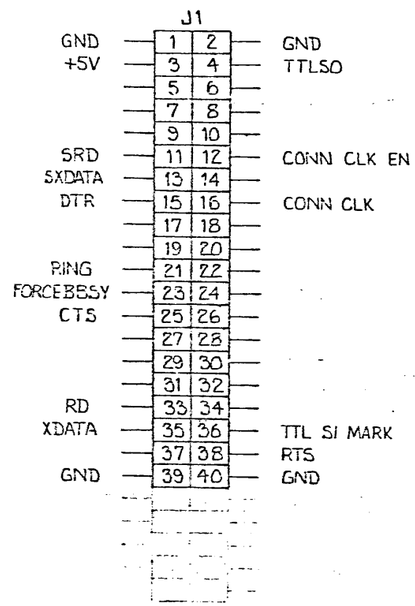
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

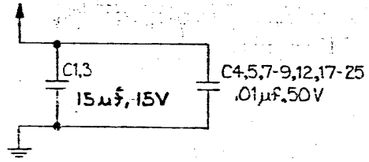
LAST REFERENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U63
CAPACITOR	C26
RESISTOR	R20
RESISTOR MODULE	RM5
DIODE	CR12
CONNECTOR	J1

REFERENCE DESIGNATION NOT USED	

REF. DESIG.	GATES USED PER TOTAL	PART NO.
U17	2 / 4	SN74125
U18	3 / 4	SN7408
U35	1 / 4	AM26LS33
U40	5 / 6	SN7404
U44	3 / 4	SN7400
U45	1 / 2	SN7474
U62	3 / 4	SN7408

SIDE 2		SIDE 1	
+5V	A	BIRL05 L	SOLDER SIDE CONNECTOR A
	B	BIRQ6 L	
GND	C	BDAL16 L	
	D	BDAL17 L	
BDOUT L	E		
BRPLY L	F		
BDIN L	H		
BSYNC L	J		
BWTBT L	K		
BIRQ4 L	L		
BIAK1 L	M		
BIAK0 L	N	BDMR L	
BBS7 L	P		
BDMGI L	R		
BDMGO L	S		
BINIT L	T	GND	
BDAL0 L	U		
BDAL1 L	V		
+5V	A	BDCOK H	COMPONENT SIDE CONNECTOR B
	B	BPOK H	
GND	C		
	D		
BDAL02 L	E		
BDAL03 L	F		
BDAL04 L	H		
BDAL05 L	J		
BDAL06 L	K		
BDAL07 L	L		
BDAL08 L	M		
BDAL09 L	N	BSACK L	
BDAL10 L	P	BIRQ7 L	
BDAL11 L	R		
BDAL12 L	S		
BDAL13 L	T	GND	
BDAL14 L	U		
BDAL15 L	V		





NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ±.020 ±0°30' .XXX±.010	THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO SIGMA INFORMATION SYSTEMS, INC. AND MAY NOT BE REPRODUCED OR USED FOR OTHER THAN MAINTENANCE PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM AN OFFICER OF THE ABOVE FIRM.
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MATERIAL / FINISH

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CHECKED		
ENGINEER		
APPROVED		
APPROVED		

Sigma Information Systems Inc.

TITLE: SCHEMATIC DIAGRAM – DLV11E ASYNCHRONOUS INTERFACE

SIZE	CODE IDENT. NO.	DRAWING NO.	REV
D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 1 OF 6	

DWG NO 400360 REV 0 SH 1

FORM NO. 001

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

BDALØØ L AU2
BDALØ2 L BE2
BDALØ6 L BK2
BDALØ7 L BL2
BDALØ3 L BF2
BDALØ4 L BH2
BDALØ5 L BJ2
BDALØI L AV2
BDALØ8 L BM2
BDAL09 L BN2
BDAL1Ø L BP2
BDAL11 L BR2
BDAL12 L BS2
BDAL13 L BT2
BDAL14 L BU2
BDAL15 L BV2
AR2
AS2
BRPLY L AF2
BIAKO AN2
BIRQ AL2
BHALT AD1
BSYNC L AJ2
BDIN L AH2
BOUT L AE2
BIAKI AM2
BINIT L AT2
BDCOK L BA1
BBS7 L AP2
BWTBT L AK2

DS8641 U4: DØØ H, DALØØ H, DØ2 H, DAL02 H, DØ6 H, DAL06 H, DØ7 H, DAL07 H
DS8641 U3: DØ3 H, DALØ3 H, DØ4 H, DAL04 H, DØ5 H, DAL05 H, DØ1 H, DALØ1 H
DS8641 U2: DØ8 H, DALØ8 H, DØ9 H, DAL09 H, DI0 H, DAL1Ø H, D11 H, DAL11 H
DS8641 U1: D12 H, DAL12 H, D13 H, DAL13 H, D14 H, DAL14 H, D15 H, DAL15 H

U4 pin 9 → U16 (7408) → RDXCSRL
U3 pin 9 → U16 (7408) → RDRDBR L
U2 pin 9 → U16 (7408) → VECT L ⑥
U16 (7408) → RDRCSR L ⑤, ROM L ③
U1 pin 9 → U44 (7400) → U18 (7405) → RD RDBRL

330Ω R15, R16, R17, R20

+5V
RM2 4.7K
SW2
8136 s U12: DAL12 H, DAL11 H, DAL1Ø H, DAL09 H, DAL08 H, DAL07H
RM1 4.7K → MATCH H ⑤

+5V
RM2 4.7K
SW2
8136 s U13: DAL06 H, DAL05 H, DAL04H, DAL03H

+5V
R4 390Ω
R3 680Ω
A/B

DS8641 U1Ø: RPLYH ⑥, BIAKØ ⑥, BR ⑥, FE ④

DS8640 U9: SYNCL ③, DIN H ③⑤⑥, DOUT H ⑤⑥
U40 (7404)
R2 390Ω, +5V, R1 680Ω
BIAKI ⑥

DS8640 U8: INIT L ④⑥③, DCOK ⑤, BBS7H ③, WTBTH ⑤
U37 (7404)

+5V
RM1 4.7K
74LS244 U5: DØ8 H, DØ7 H, DØ6 H, DØ5 H, DØ4 H, DØ3 H, DØ2 H, DØ1 H
SW1
VECTØ ⑥
VECTL ⑥

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 2 OF 6	

FORM NO. 002

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

74LS373 U24
DAL01H
DAL02H
DAL03H
DAL04H
DAL05H
DAL06H
DAL07H
DAL08H
CLK
OE
PU
DALØØH
U46 7474
INTL ②
74LS373 U48
DAL09H
DAL10H
DAL11H
DAL12H
DALØØH
SYNCL
DINH
U40 7404
U42 7400
BBS7H
DAL12H
DAL11H
DAL10H
DAL09H
U56 7430
+5V
RM3 4.7K
LAØ2H ⑤⑥
LAØ1H ⑤
U33 74S472
D15H
D14H
D13H
D12H
D11H
D10H
DØ9H
DØ8H
U34 74S472
DØ7H
DØ6H
DØ5H
DØ4H
DØ3H
DØ2H
DØ1H
DØØH ②
LOAD ROM ⑥
LAØØH ⑤
ROMSEL ⑥
ROM L ②⑥

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 3 OF 6	

DWG. NO. SD400360 REV. B SH

FORM NO. 802

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

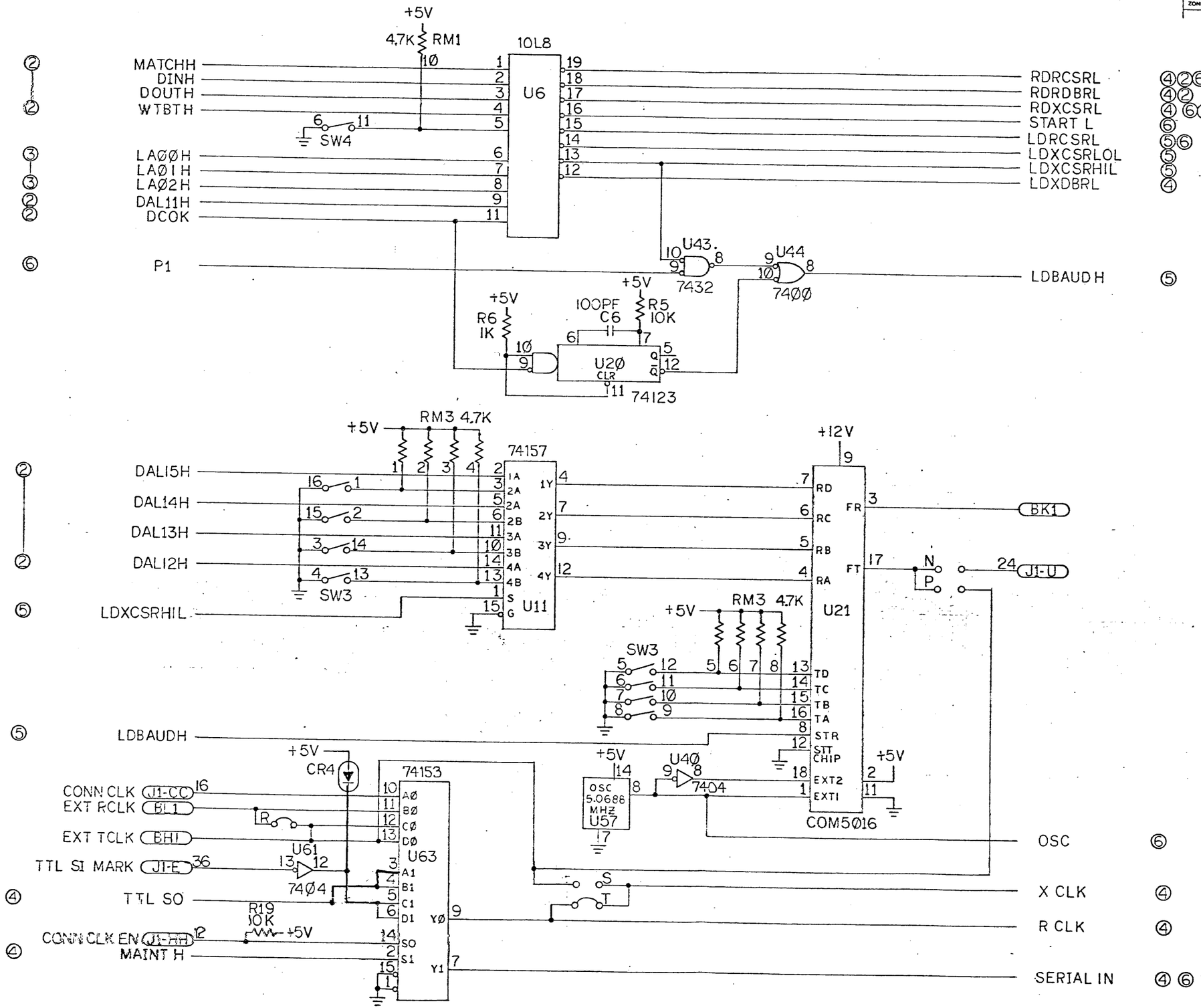
COM8017 U58
DAL07H
DAL06H
DAL05H
DAL04H
DAL03H
DAL02H
DAL01H
DAL00H
RDRDBRL
R CLK
SERIAL IN
LDXDBRL
XCLK
DI7 DI6 DI5 DI4 DI3 DI2 DI1 DIO
R DAR
R CLK
SI
STB STPTUS
STB RD
DS
TCP
DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0
OR FE PE SO
RDA
TBMT
+5V
OPEN
MR
74LS244 U49
74LS244 U52
74LS244 U51
D07H D06H D05H D04H D03H D02H D01H D00H
D15H D14H D13H D12H
FE
RM5 1K
SW4
SB NB NB PE POE
U40 7404
INITL
DSINT
U61 7404
U43 7432
7474 U54
RD RDY
TBMT
7432 U43
RIE H
U42 7400
RINT REQH
74175 U59
DAL06H
DAL05H
DAL03H
DAL02H
LDRCSRL
INIT L
DAL01H
DAL00H
DAL02H
LDXCSRLOL
RDXCSR L
4.7K RM5
R8 1K
RM5 4.7K
CR5-8
7408 U62
U60
D07 H D06 H D05 H D04 H D03 H D02 H D01 H D00 H
RDRCSRL
J1-V RTS
J1-C FORCEBBSY
J1-DD DTR
J1-FF SXDATA
J1-F XDATA
J1-SS
TTLSØ
D00 H D02 H D07 H
R18 10K
MAINTH

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 4 OF 6	

DWG. NO. SD400360 REV. B

FORM NO. 002

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 5 OF 6	

DWG. NO. SD400360 REV. B SH

FORM NO. 002

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

BIAKI ②④
RINTREQH ④
TBMT ④
LAØ2H ③
P2H ⑥
DØ6H ②
LDRCSRL ⑤
RIEH ④
LDXCSRLOL ⑤
DALØ6H ②
LDRCSRL ⑤
LDXCSRLOL
RDXCSRL ⑤
INITL ②
DINH ②

U7 BIAKI, RO, RI, R2, R3, SO, SI, D, LD, OE, R, DIN, BIAKO
R7 1K, RM1 4.7K, +5V
U37 7404
U17 74125, U18 7408, U62 7408, U62 7400
R13 150Ω, C26 100 pf
BR ②
VECTL ②⑥
VECTØ ②
BIAKO ②

RD J1-J 33
J1-II +5V
RING J1-X 21
J1-VV
CAR J1-BB 17
J1-UU
CTS J1-T 25
J1-B
SRD J1-JJ 11
J1-A

-12V RM4 10K
RM4 10K
RM4 10K
RM4 10K
AM26LS33
U35, U27, U27, U27
CR1Ø

PU 74175 U26
U25 16R6
D15H ②
D14H
D13H
D12H
D11H
D1ØH
② INITL
U45 7474
DS INT ④

RDRDY ④
SERIAL IN ⑤
OSC
RD RCSR L

START L ⑤
U37 7404
U28 74123, U28 74LS123
C1Ø 100, R11 10K, C11 100, R1Ø 10K, +5V
PUI
R9 1K
U46 7474
DOUTH ②
ROMSEL ③
DINH ②
U44 7400, U42 7400
U37 7404
R PLY H ②
P1 ⑤
P2H ⑥
LOAD ROM ③

INITL ②
ROML ③⑤
VECTL ⑤
+12V CAD2

C2 2.2UF 20V
U37 7404
R14 470Ω, R12 470
U37 7404
MMHØØ26 U39
C14 1UF 35V
C15 1UF 35V
CR1, CR3, CR2
C13 2.2UF 20V
-12V
C12 .01
+5V
OSC ⑤ U47 74393

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D		SD400360	B
SCALE NONE	WORK ORDER NO.	SHEET 6 OF 6	

SD400360 REV B SH DWG NO.

FORM NO. 002