SHARP

MICROCOMPUTER DATABOOK

1996

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■ The devices in this publication are designed for use in general electronic equipment designs, such as :

- Personal computers
- Office automation equipment
- Telecommunication equipment (except for trunk lines)
- Test and measurement equipment
- Industrial control
- Audio visual equipment
- Consumer electronics

■ Measures such as fail-safe function and redandant design should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that reguires higher reliablity such as :

- Main frame computers
- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
- Traffic signals
- Gas leakaga sensor breakers
- Alarm equipment
- Various safety devices etc.

■ SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as :

- Military and aerospace applications
- Telecommunication equipment (trunk lines)
- Nuclear power control equipment
- Medical and other life suport equipment (e.g. scuba)

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PREFACE

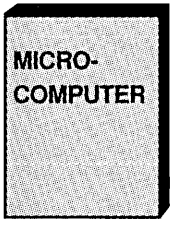
As we become more and more an infomation-oriented society, microcomputers have come to play a major role in both home and office equipment. On the one hand, computer-related services are growing ever more sophisticated and diverse; on the other, they are becoming much more accessible to each of us in our daily lives. Along with this increase in the importance of the information processing in our lives, we are faced with a growing demand for microcomputers using the most advanced technology.

To keep pace with this rapid progress, we at Sharp will continue to direct our efforts at understanding the crucial trends of the moment in this area and supply our customers with products that truly meet their needs. In short, to contribute to a better life for all of us in this age of expanding technology.

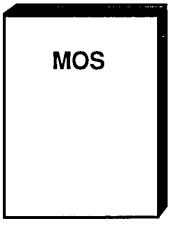
Sharp has developed a wide range of microcomputer units including 4-bit, 8-bit and 16-bit microcomputers and 32-bit RISC microcomputer for use in numerous areas of application. Sharp microcomputer units are used extensively in home appliances, PDAs and multimedia-related products, as well as in communicaton equipment.

This data book has been especially compiled for the use of our customers. Listed here is the major microcomputers products developed and manufactured by Sharp, with detailed explanations of their many functions and outstanding features. We hope that you find this book useful in determining which Sharp products are best suited to your needs. Please contact us directly if you have any further questions.

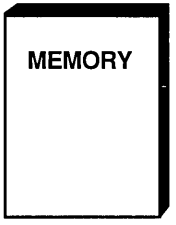
SHARP'S INTEGRATED CIRCUIT DOCUMENTATION



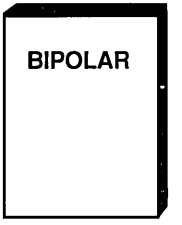
- 32-Bit RISC Microcomputer
- 16-Bit Single-Chip Microcomputer
- 8-Bit Single-Chip Microcomputers
- 4-Bit Single-Chip Microcomputers
- 4-Bit Single-Chip Microcomputers (For Data Bank Use)
- Development Support Systems etc.



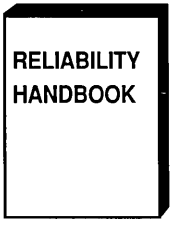
- CCDs/CCD Peripherals
- Display Drivers
- A/D · D/A Converters
- Facsimile MODEMs
- Telecommunications



- Pseudo-Static RAMs
- Dynamic RAMs
- Static RAMs
- Mask-Programmable ROMs
- FIFO Memories
- Applicaton Notes



- Operational Amplifiers/Comparators
- Transistor Arrays, Voltage Regulators
- A/D · D/A Converters
- ICs for Audio/Visual Equipment
- CCD Peripherals, ICs for Telephone, etc.



- Quality and Reliability Assurance System
- How Sharp Views Semiconductor Device Reliability and Reliability Prediction
- Reliability Testing
- Failure Analysis
- Proper Handing of Semiconductor Devices

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GENERAL INFORMATION

Alphanumeric Index

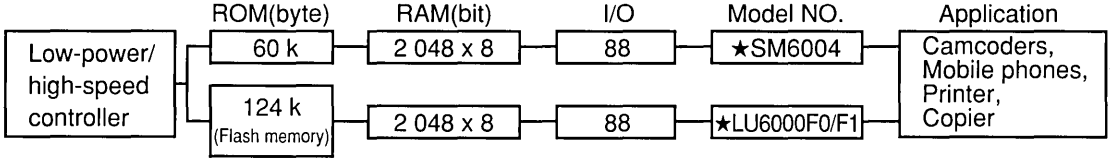
PRODUCT LINEUP

32-Bit RISC Microcomputer (ARM Series)

★ Under development

Model No.	Configuration	Operating frequency (MHz) MAX.	Power consumption (mW) MAX.	Supply voltage (V)	Package
★LH77790	ARM7D CPU + Cache Memory (2 kB) + RAM (2 kB) + Timer + UART (3-ch) +INTC + PIO + DRAMC + PWM + MEM I/F + LCDC + WDT	25 (at 5 V) 16.5 (at 3.3 V)	600 (at 5 V) 90 (at 3 V)	2.7 to 5.5	160QFP

16-Bit Single-Chip Microcomputers



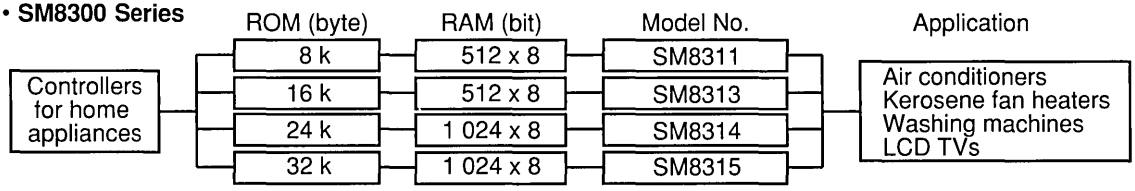
Model No.	Memory (bit)		I/O	Instruction cycle (µs) MIN.	Supply current (mA) TYP.	OSC	Supply voltage (V)	Operating temp. (°C)	Package	Remarks
	ROM	RAM								
★SM6004	60 k x 8	2 048 x 8	88	0.133	65	Crystal/ Ceramic	2.5 to 5.5*2 4.5 to 5.5*3	– 20 to 70	100QFP 100LQFP*4	16-bit timer unit, 10-bit A/D, 8-bit D/A, UART, SIO, PWM output
★LU6000F0/F1	124 k x 8*1	3 584 x 8	88	0.133	TBD	Crystal/ Ceramic	2.7 to 3.6*2 4.5 to 5.5*3	– 20 to 70	100QFP 100LQFP*4	16-bit timer unit, 10-bit A/D, 8-bit D/A, UART, SIO, PWM output

*1 Flash memory
*2 Main clock 20MHz
*3 Main clock 30MHz
*4 0.5mm pin-pitch

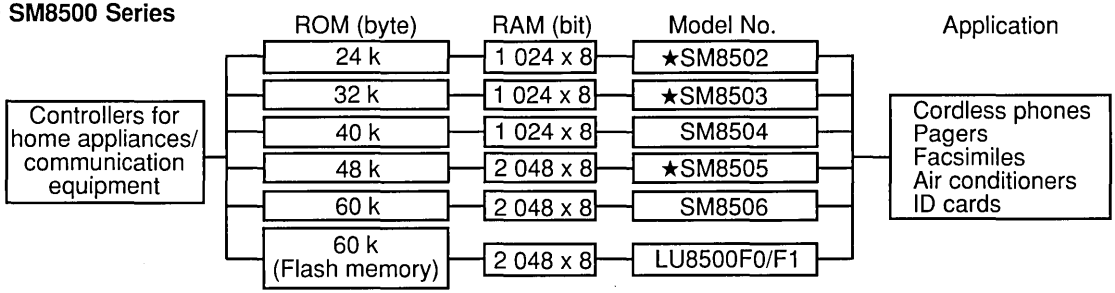
8-Bit Single-Chip Microcomputers

★ Under development

• **SM8300 Series**



• **SM8500 Series**



SM8300, SM8500 Series

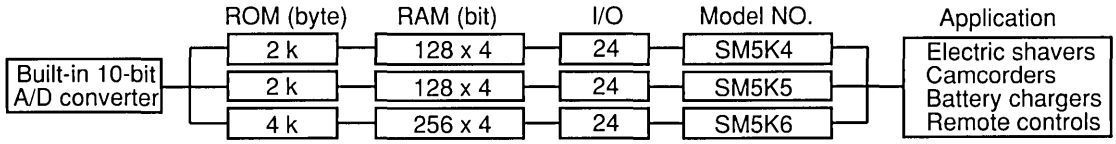
Model No.	Memory (bit)		I/O	Instruction cycle (µs) MIN.	Supply current (mA) TYP.	OSC	Supply voltage (V)	Operating temp. (°C)	Package	Remarks
	ROM	RAM								
SM8311	8k x 8	512 x 8	52	0.5	6 (at 1 µS)	Crystal/ Ceramic	2.7 to 5.5	–20 to 70	64SDIP/ 64QFP	PWM output, LED direct drive, Built-in A/D, SIO
SM8313	16k x 8	512 x 8	52	0.5	6 (at 1 µS)	Crystal/ Ceramic	2.7 to 5.5			
SM8314	24k x 8	1 024 x 8	52	0.5	6 (at 1 µS)	Crystal/ Ceramic	2.7 to 5.5			
SM8315	32k x 8	1 024 x 8	52	0.5	6 (at 1 µS)	Crystal/ Ceramic	2.7 to 5.5			
★SM8502	24k x 8	1 024 x 8	84	0.33*2	10	Crystal	1.8 to 5.5	–20 to 70	100QFP/ 100QFP*3	Built-in wave form generator (2-ch), 10-bit A/D, D/A, SIO
★SM8503	32k x 8	1 024 x 8	84	0.33*2	10	Crystal	1.8 to 5.5			
SM8504	40k x 8	1 024 x 8	84	0.33*2	10	Crystal	1.8 to 5.5			
★SM8505	40k x 8	2 048x 8	84	0.33*2	10	Crystal	1.8 to 5.5			
SM8506	60k x 8	2 048x 8	84	0.33*2	10	Crystal	1.8 to 5.5			
LU8500F0/F1	60k*1 x 8	2 048x 8	84	0.33*2	20	Crystal	2.7 to 3.6 4.5 to 5.5			

*1 Flash memory

*2 System clock speed is switchable on programming.

*3 0.5 mm pin-pitch

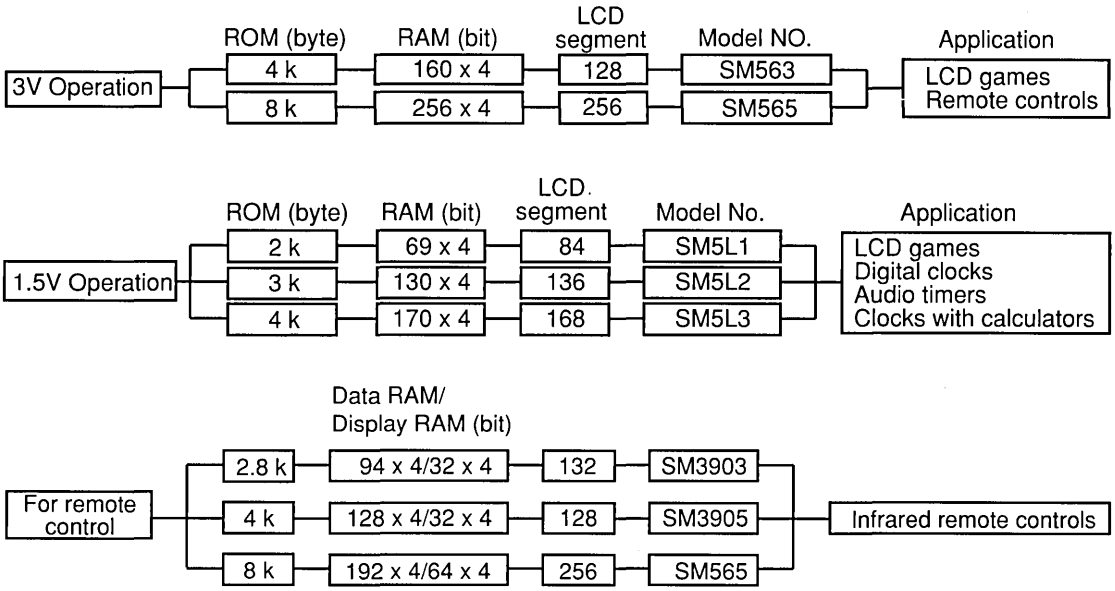
4-Bit Single-Chip Microcomputers



Controller Series

Model No.	Memory (bit)		I/O	A/D conversion	Instruction cycle (µs) MIN.	Supply current (mA) TYP.	OSC	Supply voltage (V)	Operating temp. (°C)	Package
	ROM	RAM								
SM5K4	2 048 x 8	128 x 4	17*1 23*2 24*3	10-bit 4-ch	1.2	1.2	Resistor	2.7 to 5.5	–20 to 85	30SDIP/ 24SSOP/ 32SOP/ 36QFP
SM5K5	2 048 x 8	128 x 4	20*4 23*2 24*3	10-bit 4-ch	1	1.2	Crystal/ Ceramic	2.2 to 5.5	–20 to 70	30SDIP/ 28SOP/ 32SOP/ 36QFP
SM5K6	4 096 x 8	256 x 4	24	10-bit 8-ch	1	1.6	Crystal/ Ceramic	2.0 to 5.5	–20 to 70	30SDIP/ 32SOP/ 36QFP

*1 24-pin SSOP
*2 30-pin SDIP
*3 32-pin SOP or 36-pin QFP
*4 28-pin SOP

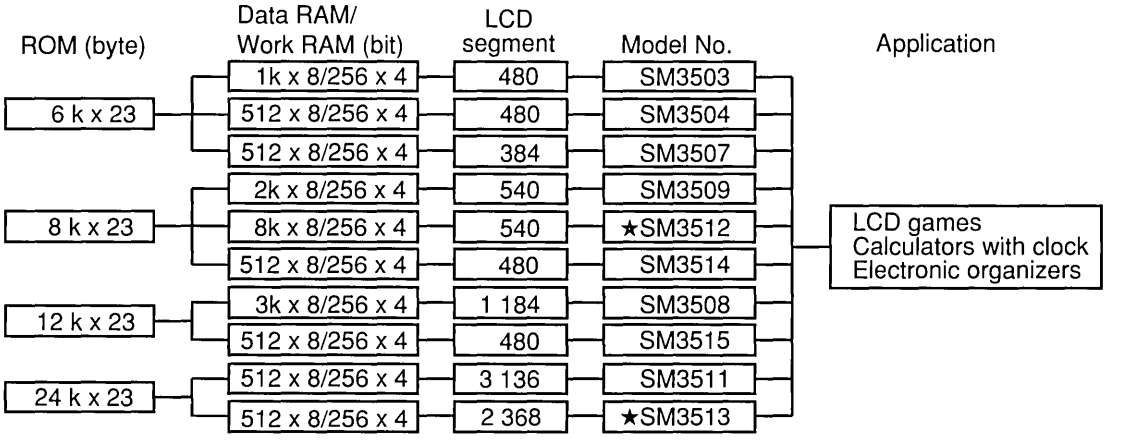


LCD Driver Series

Model No.	Memory (bit)		I/O	Instruction cycle (µs) MIN.	Supply current (mA) TYP.	OSC	Supply voltage (V)	Operating temp. (°C)	Package
	ROM	RAM							
SM563	4 096 x 8	128 x 4*3 32 x 4*4	30	2 (at 5 V) 6.7 (at 3 V)	400 (at 3 V)	Resistor	2.7 to 5.5	–20 to 70	64QFP
SM565	8 192 x 8	192 x 4*3 64 x 4*4	31	2 (at 5 V) 8.79 (at 3 V)	160 (at 3 V)	Ceramic	2.4 to 5.5	–20 to 70	100QFP
SM5L1	2 048 x 8*1 160 x 6*2	48 x 4*3 21 x 4*4	14	61	8 (at 122 µs)	Crystal/ Resistor	1.5 ± 20%	0 to 50	60QFP
SM5L2	3 072 x 8*1 256 x 6*2	96 x 4*3 34 x 4*4	14	61	10 (at 122 µs)	Crystal/ Resistor	1.5 ± 20%	0 to 50	72QFP*5/ 80QFP
SM5L3	4 096 x 8*1 256 x 6*2	128 x 4*3 42 x 4*4	14	61	12 (at 122 µs)	Crystal/ Resistor	1.5 ± 20%	0 to 50	80QFP
SM3903	2 772 x 8	96 x 4*3 32 x 4*4	16	52.8	40	Ceramic	2.6 to 3.2	0 to 50	60QFP
SM3905	4 096 x 8	128 x 4*3 32 x 4*4	30	8.79	160	Ceramic	2.4 to 3.6	–20 to 70	64QFP

*1 Program ROM *3 Data RAM *5 0.5 mm pin-pitch

*2 Melody ROM *4 Display RAM (Usable for Data RAM)



For Data Bank Use

Model No.	Memory (bit)		I/O	Instruction cycle (μs) MIN.	Supply current (TYP.)		OSC	Supply voltage (V)	Operating temp. (°C)	Package
	ROM	RAM			Operating (μA)	Standby (μA)				
SM3503	6 144 x 23	1 024 x 8 256 x 4	8	12	85	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 100QFP
SM3504	6 144 x 23	512 x 8 256 x 4	8	12	85	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 80QFP
SM3507	6 144 x 23	512 x 8 256 x 4	18	12	85	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 80QFP
SM3509	8 192 x 23	2 048 x 8 256 x 4	18	12	85	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 100QFP
★SM3512	8 192 x 23	8 192 x 8 256 x 4	18	12	85	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 100QFP
SM3514	8 192 x 23	512 x 8 256 x 4	8	10	100	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 100QFP
SM3508	12 288 x 23	3 072 x 8 256 x 4	19	3	270 (at 3 V)	40*1 (at 3 V)	Built-in OSC*2/ Ceramic	2.5 to 5.5	–10 to 60	Chip/ 128QFP
SM3515	12 288 x 23	512 x 8 256 x 4	8	10	100	20*1	Built-in*2 OSC	2.5 to 3.4	–10 to 60	Chip/ 100QFP
SM3511	24 576 x 23	512 x 8 256 x 4	20	3	600 (at 5 V)	50*1 (at 5 V)	Built-in OSC*2/ Ceramic	3.8 to 6.0	–10 to 60	Chip
★SM3513	24 576 x 23	512 x 8 256 x 4	20	3	600 (at 5 V)	50*1 (at 5 V)	Built-in OSC*2/ Ceramic	3.8 to 6.0	–10 to 60	Chip

RAM Upper : Data RAM
Lower : Work RAM

*1 Specifications at LCD displaying conditions

*2 Usable with a crystal oscillator (32.768 kHz) for clocks

QUALITY ASSURANCE

Quality Assurance System

Sharp develops and produces a wide range of consumer and industrial-use semiconductor products.

In recent years, the applications of ICs have expanded significantly, into fields where extremely high levels of quality are critical.

In response, Sharp has implemented a total quality assurance system that encompasses the entire production process from planning to after-sales service. This system ensures that quality is a priority in the planning development and production and guarantees product reliability through rigorous reliability testing. We compiled the "Sharp Semiconductor Reliability Handbook, IC Edition" to introduce you to the results of some of our research and to our quality and reliability philosophy and programs. We hope that it is informative and that it will help Sharp customers develop and refine their quality and reliability assurance and control activities. We will introduce a part of this system here.

Sharp's quality and reliability assurance activities are based on the following guidelines :

- All personnel should participate in quality assurance by continually cultivating a higher level of quality awareness.
- In the design and development stages of new products, create reliable designs that consider reliability in every respect.
- Quality control in all production processes, all working environments, materials, equipment, and measuring devices should be carefully monitored to ensure quality and reliability from the very beginning of the production process.
- Confirm long-term reliability and obtain a thorough understanding of practical limits through reliability testing.
- Continually work to improve quality through application of data from process inspections, reliability testing, and market surveys.

Quality Assurance During New Product Development

New product development ***(Fig. 1)*** begins with an accurate grasp of the purpose, environment, and manners in which customers will use the product as well as the required reliability. A development plan is then drafted, clarifying the price, quantity, sales period and target reliability of the product to be manufactured.

Quality and reliability are built into the product from the beginning of the product cycle by introducing design review (DR) and reliability planning in the development and design stage. The first tasks undertaken in this stage are process development and circuitry design, by which a prototype, or technical sample (TS), is made. An evaluation of the technical sample is conducted, centering on the function and performance of the sample under conditions in which the final product will be used (TS evaluation).

Next, an engineering sample (ES) is made, based on the results of the TS evaluation, and it is subjected to ES evaluation. The ES evaluation consists of determining, under mass production conditions, whether the product functions and performs as intended during development and design. Reliability testing is also used to decide whether the engineering sample has the required degree of reliability.

In the final stage, the transfer of the product to mass production is discussed-based on the results of the TS and ES evaluations. Once TS and ES are accepted, preproduction begins. At this time, it is determined whether the quality and reliability obtained during development and design can be maintained, whether there are any discrepancies in the production process and what yields will be. The manufacturability of the product is determined, based on these results.

DR (Design Review) is performed to prevent faulty operation and to enhance the functions, usability, quality and reliability, upon completion of structural design, logic design, software design, circuit design, TS/ES evaluation and reliability tests.

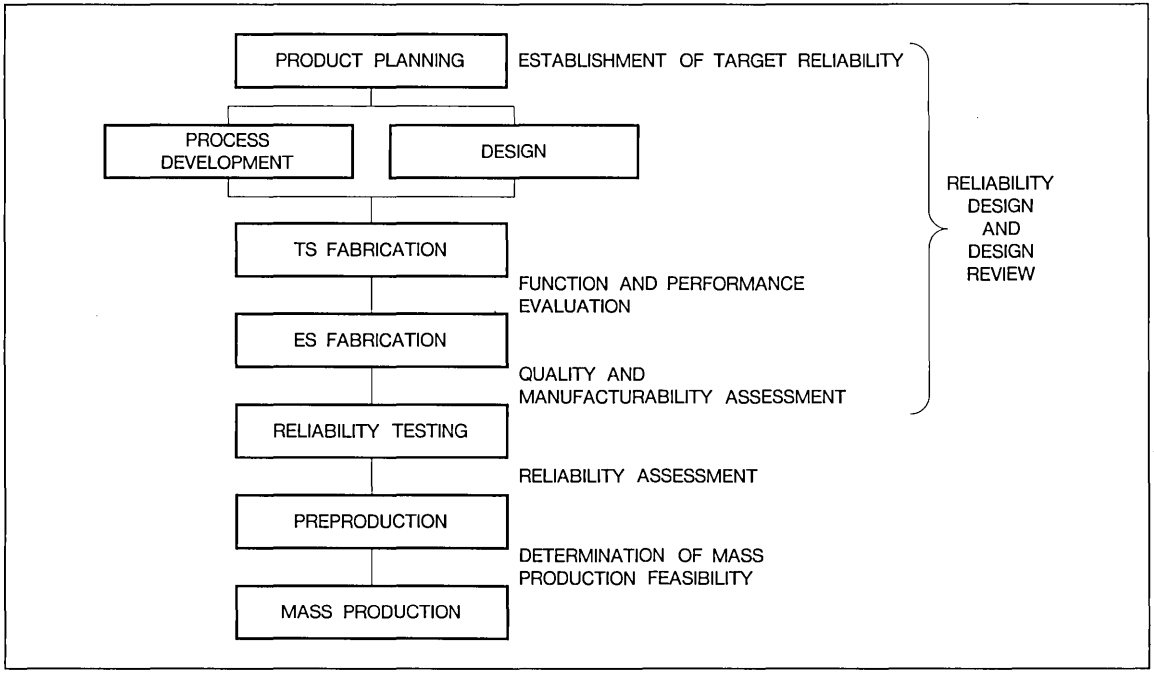


Fig. 1 New Product Development Steps

PROCESS	CHARACTERISTIC(S) CONTROLLED	PURPOSE OF CONTROL
SILICON WAFER INCOMING INSPECTION	EXTERNAL APPEARANCE, DIMENSIONS, SHEET RESISTIVITY	REMOVE PRODUCTS HAVING IMPROPER DIMENSIONS, FLAWS AND CRYSTAL DEFECTS. ENSURE PROPER SHEET RESISTANCE VALUES
OXIDATION		
OXIDE INSPECTION MONITORING	EXTERNAL APPEARANCE, FILM THICKNESS, SURFACE CLEANLINESS	FIND PINHOLES, CHECK SURFACE CLEANLINESS AND CONTROL FILM THICKNESS
PHOTOLITHOGRAPHY		
VISUAL INSPECTION MONITORING	DEVELOPABILITY, ETCHABILITY, LINE WIDTH	CHECK FOR PROPER DEVELOPMENT AND ETCHING. CONTROL LINE WIDTH
ION IMPLANTATION		
ELECTRICAL INSPECTION OF CHIP MONITORING	ELECTRICAL CHARACTERISTICS, MAJOR DEVICE CHARACTERISTICS	REMOVE PRODUCTS HAVING POOR ELECTRICAL CHARACTERISTICS. ENSURE PROPER DEVICE CHARACTERISTICS
DICING		
FRAME BREAK, SORTING		
DIE INSPECTION	EXTERNAL APPEARANCE	REMOVE CRACKED AND CHIPPED ITEMS.
DIE BONDS		
WIRE DIE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE ADHESIVE STRENGTH	ENSURE QUALITY OF DIE BONDS
WIRE BONDS		
MOLDING COMPOUNDS WIRE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE TENSILE STRENGTH	CHECK POSITION AND SHAPE OF BONDS. ENSURE PROPER WIRE TENSILE STRENGTH
ENCAPSULATION/MOLD MONITORING	TEMPERATURE, TIME, STRESS WIRE CONDUCTIVITY	ENSURE MOLDABILITY. ENSURE PROPER WIRE CONFIGURATION
STABILIZED BAKE		
LEAD SURFACE FINISHING	INGREDIENTS, TEMPERATURE, CONTAMINATION	MAINTAIN FINISH QUALITY
FINISHING INSPECTION MONITORING	THICKNESS, UNIFORMITY (SOLDERABILITY) PLATED LAYER COMPOSITION PLATED LAYER THICKNESS	REMOVE PRODUCTS HAVING PLATING IRREGULARITIES. MAINTAIN PLATING QUALITY
MARKING	TEMPERATURE, TIME, MARKING MATERIAL	MAINTAIN MARK QUARITY
LEAD CUT FORMING	TOOLING SHARPNESS TOOLING DIMENSIONS	PREVENT ABNORMAL STRESS ON PLASTIC MOLD RESULTING IN DAMAGE

Fig. 2 Example of the Quality Control Process

Raw Materials Control

The level of product quality and reliability is largely governed by the quality of the materials originally making up the production process and environment.

It is the responsibility of the vendor to execute the quality assurance of basic materials purchased by Sharp. Raw material quality assurance is conducted according to the following system :

- Initial selections of a raw material manufacturer.
- Quality qualification for each new material put into use (quality and reliability assessments of devices in which such new materials are used).
- Periodic quality consultations based on quality information obtained during mass production.

Acceptance inspections are carried out as necessary based on acceptance criteria derived from product specifications and approved drawings.

Control of the Manufacturing Environment

Integrated circuit devices are manufactured in a clean room where there is minimal airborne particulates. The use of ultrapure water also aids cleanliness. Such conditions are necessary due to the adhesion of even small bits of foreign particles (0.1 μm or less), no more than 1/5-1/10 the size of the smallest IC pattern, can result in defects later in the process.

Particulates not only affects chip yields, but can also have a lethal affect on the quality and reliability of a device. Therefore, the cleanliness of every piece of equipment and facility in the plant as well as that of work clothes and work articles are controlled. Degree of cleanliness is usually expressed numerically as the number of particles over 0.5 μm per cubic foot of air.

The degree of cleanliness maintained in Sharp clean rooms, where wafers come in direct contact with air, is Class 1. Temperature and humidity are maintained at constant levels by continuous computer-controlled monitoring ***(Table 1)***.

The ultrapure de-ionized (DI) water used in the wafer process is manufactured with an ultrapurification equipment, employing ion-exchange treatment, ultraviolet irradiation and ultrafiltration systems.

Table 1

Clean Room Temperature & Humidity Standards

Temperature	24±0.5°C
Humidity	45±5% RH

Control of Facilities and Instrumentation

Intregrated circuit device technology is experiencing rapid revolutionary change, and advances in IC production facilities and equipment are equally impressive.

Process automation is promoted by using the latest CIM (Computer Intregrated Manufacturing) system to create devices having stable quality and to reduce variance of characteristics. In addition, production facilities maintenance control, and precision control for various instrumentation devices are implemented by both daily and periodic spot inspections.

Facilities' control is conceptually based on Total Productive Maintenance (TPM), in which all concerned employees systematically participate in facilities maintenance activies. Sharp's goal is to create a highly skilled human resource through activities such as :

- operator-initiated maintenance;
- scheduled maintenance;
- corrective maintenance.

Control of instrumentation devices is in accordance with Japanese national standards. Regular calibration by overseeing public agencies also helps maintain a high level of accuracy in these devices.

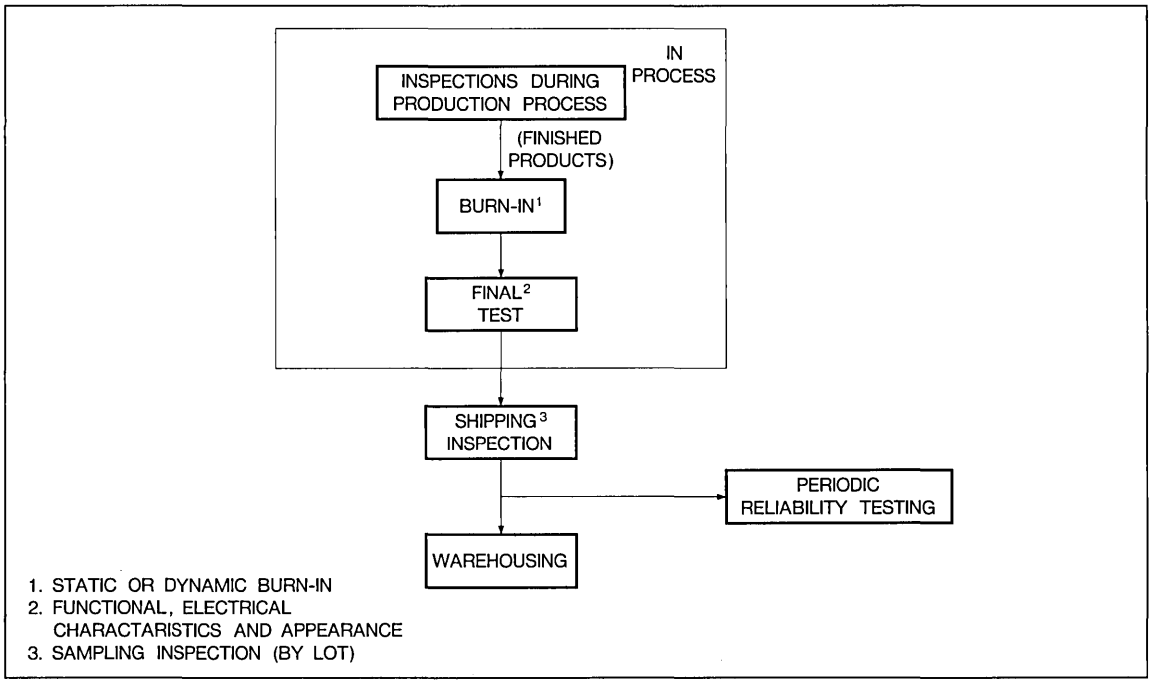


Fig. 3 Product Inspection System

Quality Control During the Production Process

Designed-in quality and reliability must be faithfully built into a device during production to manufacture consistently high-quality and high-reliability products.

Production Operations are therefore based on specific, established operational standards. Checks are performed at each process step to decide whether specific characteristics have been obtained and quality has been built in. Each process is monitored to ensure that defectives are not sent to the next process. This is done by rigorously carrying out various standardized controls, appropriate to each process, such as monitoring, visual inspections and sampling inspections.

Sharp strongly promotes the automaition of production facilities and equipment. Sharp works to prevent quality problems before they occur and to stabilize quality. Operations that required human skills in the past are now automated. Computer Integrated Manufacturihg (CIM) is being introduced into the wafer process. CIM is used to implement comprehensive production control, including conveyance within a process, equipment monitoring and progress control. CIM enables several types of process data to be processed together. Control charts and process capacity index (Cpk) are computed in real time for individual pieces of equipment. Even minute fluctuations in characteristics are fed back to improve control.

Reliability is also being assessed by periodic sampling. This test is a long-term reliability assessment, and the results are fed back to the related divisions.

While quality assurance tests and inspections are conducted for improving and maintaining quality, they are also used to predict the probable reliability a product will have in the marketplace. They provide a multi-faceted approach to ensuring product quality.

Table 2
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE & CONDITIONS	REFERENCE STANDARDS
Thermal Environment Tests	Soldering Heat	To determine soldering heat resistance. Standard test conditions : Solder bath temperature : 260±5°C Time : 10±1 s Solder composition : Pb : Sn =4 : 6	JIS C 7022 : A-1 MIL-STD-750 2031 IEC Pub. 68 Test Tb
	Temperature Cycling	To determine resistance to high and low temperatures and to temperature chenges between these extremes. Standard test conditions : Ta=Tstg MIN. to Tstg MAX. [gas phase]	JIS C 7022 : A-4 MIL-STD-883 1010 IEC Pub. 68 Test Na, Nb
	Thermal Shock	To determine resistance to sudden chengs in temperature. Standard test conditions : Ta=Tstg MIN. to Tstg MAX. [liquid phase]	JIS C 7022 : A-3 MIL-STD-883 1011 IEC Pub. 68 Test Nc
	Temperature and Humidity Cycling	To destermine resistance to conditions of high temperature and high humidity Standard test conditions : −10 to 65°C, 90 to 96% RH, one (1) cycle every 24 hours	JIS C 7022 : A-5 MIL-STD-883 1004 IEC Pub. 68 Test Z/AD
Mechanical Environment Tests	Variable Frequency Vibration	To determine resistance to vibration during transportation and use. Standard test conditions : Cycle : 100 to 2 000 Hz in 4 min. Peak acceleration : 200 m/s² {20 G} Orientation : four (4) times in each of the orientations ±X, ±Y, and ±Z	JIS C 7022 : A-10 MIL-STD-883 2007 IEC Pub. 68 Test Fc
	Mechanical Shock	To determine resistance to shocks during transportation and use. Standard test conditions : Peak acceleration : 15 000 m/s² {1 500 G} Pulse duration : 0.5 ms Orientation : three (3) pulses in each of the orientations ±X, ±Y, and ±Z	JIS C 7022 : A-7 MIL-STD-883 2002 IEC Pub. 68 Test Ea
	Constant Acceleration	To determine resistance to constant acceleration. Standard test conditions : Stress level : 200 000 m/s² {2 000 G} Orientation : applied for one (1) min. in each of the orientations ±X, ±Y and ±Z	JIS C 7022 : A-9 MIL-STD-883 2001 IEC Pub. 68 Test Ga

Table 2 (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE & CONDITIONS	REFERENCE STANDARDS
Mechanical Environment Tests	Lead Integrity	To determine resistance to installation and handling such as wiring. (1) Tensile strength. Standard test conditions : A specified load is applied in a direction parallel to the lead axis for 10±1 s (2) Bending strength. Standard test conditions : A specified load is applied to the tip of each lead and the lead is bent once each through a + and −90° arc and back. (The specified load is determined by nominal cross section or nominal section modulus.) *TCP (tape carrier package) : N/A	JIS C 7022 : A-11 IEC Pub. 68 Test U
	Solderability	To determine the solderability of leads which are connected by soldering. Standard test conditions : Solder bath temperature : 230±5°C Dip time : 5±0.5 s Solder compotisition : Pb : Sn=4 : 6, used with rosin flux.	JIS C 7022 : A-2 MIL-STD-883 2003
	Seal (Hermeticity)	To determine the effectiveness of the seal of hermetically sealed devies. (1) Fine leak detection (helium) : measured with a helium detector after storage in an He atmosphere at a prescribed pressure for a designated time period. (2) Gross leak observation (bubbles) : observation of bubbles formed by a fluorocarbon or silicone oil.	JIS C 7022 : A-6 MIL-STD-883 1014 IEC Pub. 68 Test Q
	Salt Atmosphere (Corrosion)	To determine resistance to corrosion in a salt fog. Standard test conditions : Exposure to salt spraying conditions of salt concentration, 5±1wt%. Spray rate : 0.5 to 3 ml/80 cm^3/h Salt fog temperature : 35±2°C for a designated period of time.	JIS C 7022 : A-12 MIL-STD-883 1009 IEC Pub. 68 Test Ka
Life Tests	High Temperature Operation	To determine resistance to prolonged operating stress, electrical and thermal. Standard test conditions : Ta=Topr MAX. Operating source voltage=MAX. specified operating source voltage	JIS C 7022 : B-1 MIL-STD-883 1005

Table 2 (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE & CONDITIONS	REFERENCE STANDARDS
Life Tests	High Temperature Storage	To determine resistance to prolonged high temperature storage. Standard test conditions : Ta=Tstg MAX.	JIS C 7022 : B-3 MIL-STD-883 1008
	Low Temperature Storage	To determine resistance to prolonged low temperature storage. Standard test conditions : Ta=Tstg MIN.	JIS C 7022 : B-4 IEC Pub. 68 Test A
	High Temperature/ High Humidity Bias	To determine resistance to prolonged temperature, humidity and electrical stress. Standard test conditions : 85°C, 85% RH Applied source voltage=MAX. specified source voltage	JIS C 7022 : B-5 IEC Pub. 68 Test C
	High Temperature/ High Humidity Storage	To determine resistance to prolonged storage at high temperature and humidity. Standard test conditions : (1) 60°C, 90% RH (2) 85°C, 85% RH	JIS C 7022 : B-5 IEC Pub. 68 Test C
Miscellaneous	Pressure Cooker (PCT)	To evaluate moisture resistance in a short period of time. Standard test conditions : 121°C,100% RH, 2×10^5 Pa {2 atm}, no electrical load.	EIAJ IC-121 : 18
	Series Test	Several tests (selected from those listed above) performed in series to effectively evaluate product. Example : for a surface mount device : High-temperature/High-humidity Storage → Soldering heat Resistance → Pressure cooker (PCT)	EIAJ ED-4701 : B-101
	Electrostatic Discharge Strength	To determine resistance to electrostatic stress. Standard test conditions : (1) Human body model : Earth capacity C=100 pF, equivalent Resistance R=1.5 kΩ (2) Machine model : Earth capacity C=200 pF, equivalent Resistance R=0 Ω	MIL-STD-883 3015 EIAJ ED-4701 : C-111
	Latch-Up Strength	To determine resistance to latch-up. Standard test conditions : (1) Condenser charge (2) Current application (3) Vcc overvoltage application	EIAJ ED-4701

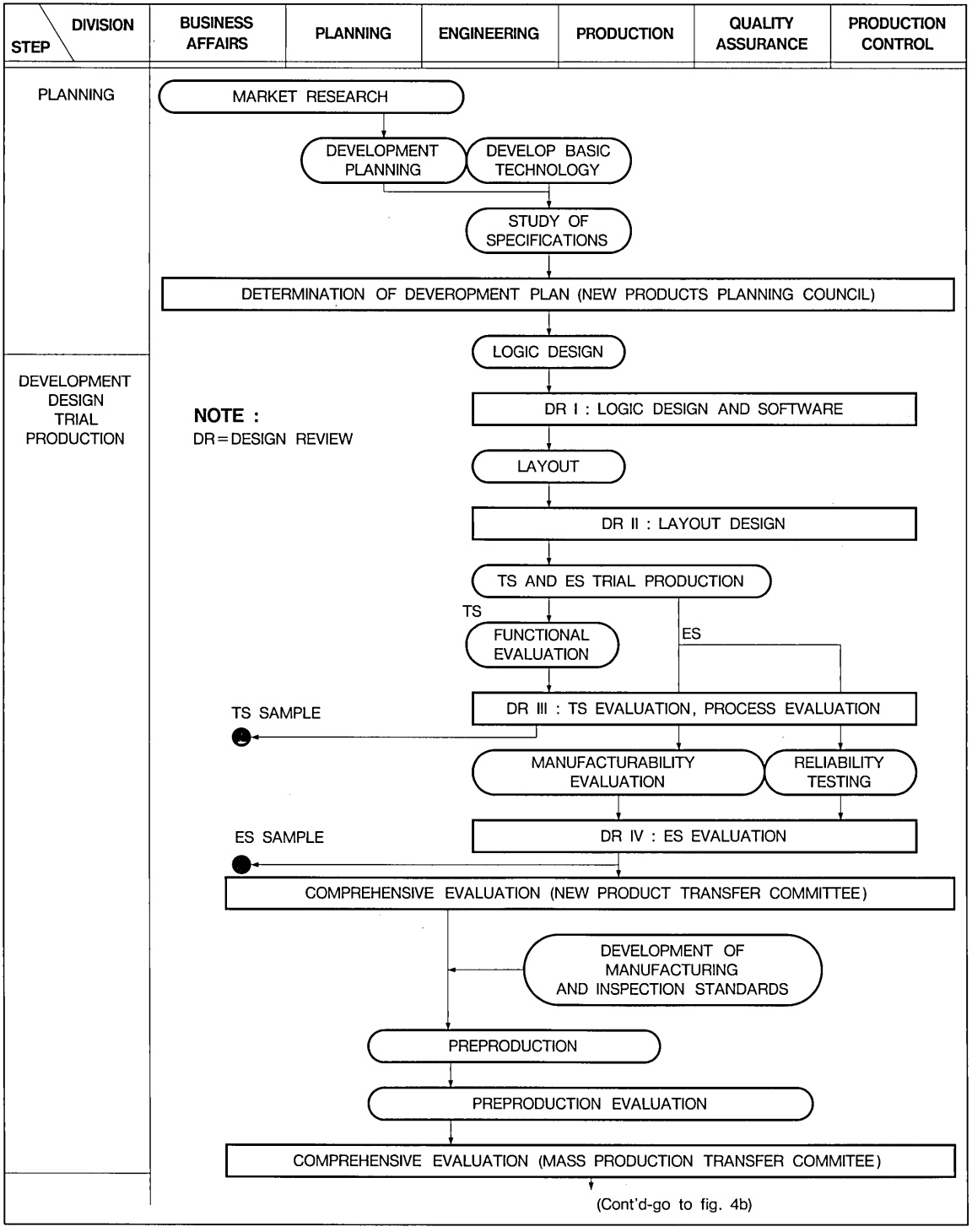


Fig. 4a Quality Assurance System

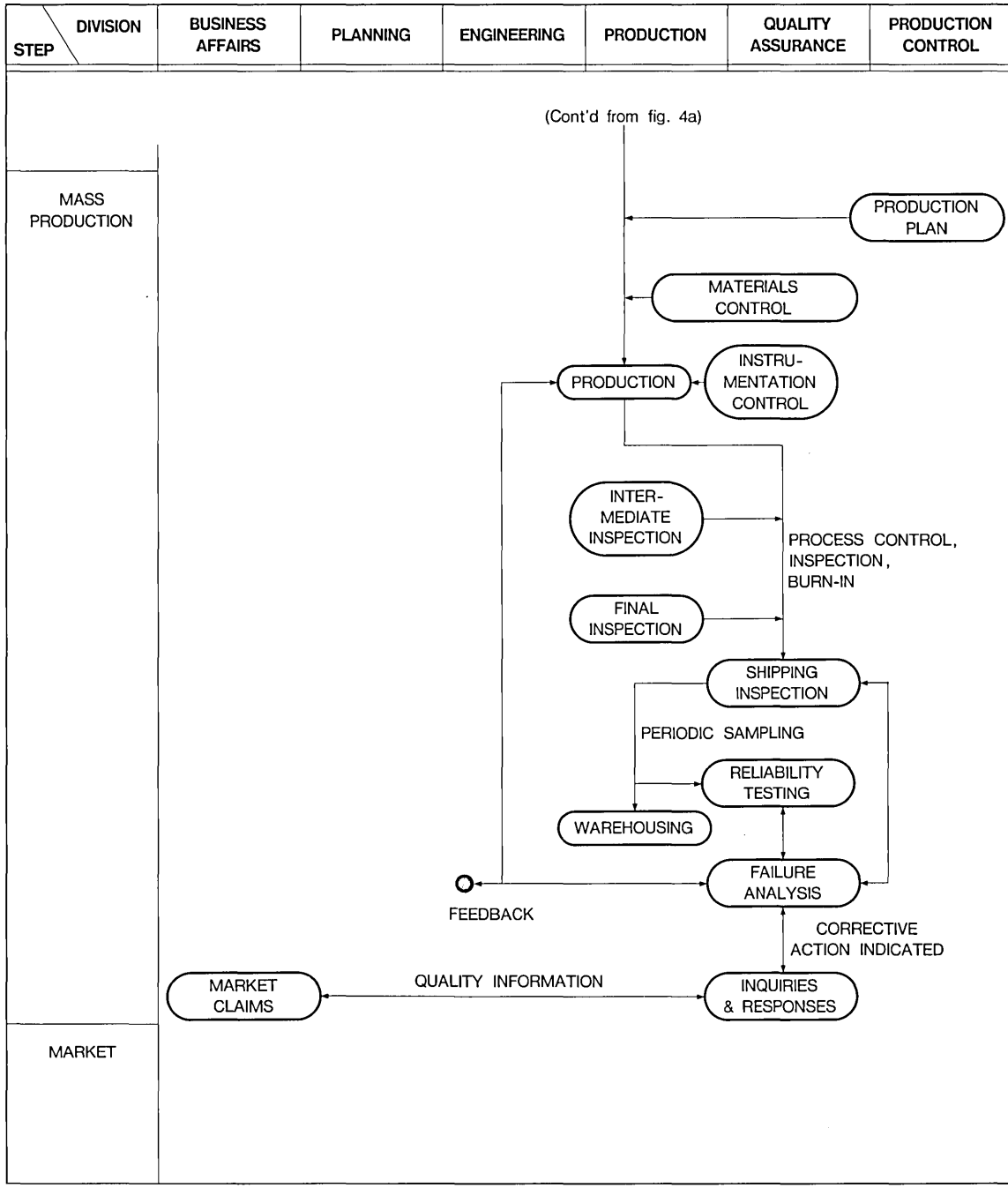


Fig. 4b Quality Assurance System

Reliability Tests

Reliability Tests Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based on standardized test methods. Such uniform testing standards include those established by JIS (Japanese Industrial Standard), MIL (U.S.MILitary Standard), EIAJ (Electronic Industries Association of Japan) and IEC (International Electrotechnical Commission). As indicated in ***Table 2***, however, Sharp has established its own testing method based on these standards.

Advances in semiconductor device technology are astonishing, and they call for higher quality and reliability standards. Improved failure analysis techniques are, therefore, necessary to ensure semiconductor device reliability.

The causes of semiconductor device failure are becoming increasingly diverse. This diversity is the result of element and interconnect miniaturization required for higher integration. It is also due to an increasingly complex manufacturing process with an increased number of steps from the wafer fabrication process to the assembly process.

Failure analysis is the use of human, physical and electrical analytical procedures to clarify the failure mechanisms of defective parts. It is used to evaluate defective items appearing throughout the life of parts : during the semiconductor manufacturing process, outgoing inspections and reliability testing; during the user's incoming inspections, processing and reliability testing; and during operation in the field.

The ultimate goal of failure analysis is to prevent the recurrence of failure. It is necessary to establish various measures based on the results of failure analysis and to feed those measures back to the manufacturing process and product users.

Sharp has an on-going program of supplying users with our own quality data, reliability test data, etc., upon request. It is just one of Sharp's efforts to maintain a high degree of user service. ***Fig. 5*** illustrates Sharp's Quality Information Routes.

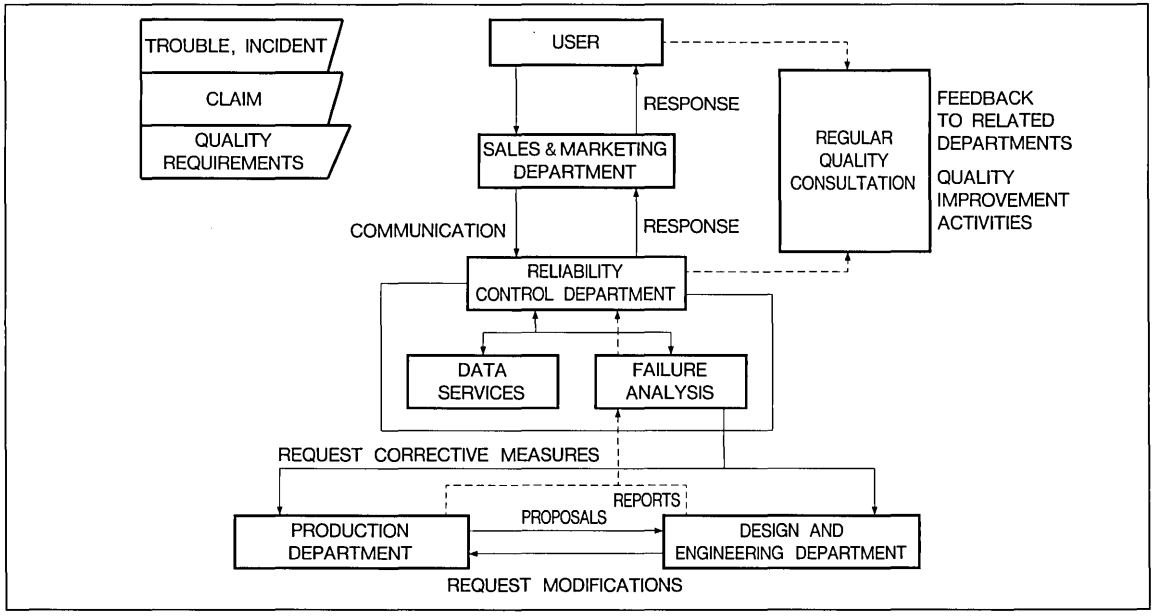


Fig. 5 Routes through which malfunctions outside the company are handled

Handling Precautions

All the semiconductor products listed in this data book are manufactured based on exacting designs and under comprehensive quality control. However, to take full advantage of the features offered and to assure each products' long-life service, please refer to the following items.

Maximum Ratings

It is generally known that the failure rate of semiconductor products increases as the temperature increases. It is, therefore, necessary that the ambient temperature be within the maximum rated temperature. Further, it is desirable from the standpoint of reliability that the ambient temperature be lowered as much as possible. The voltage, current, and electric power used are also factors that significantly influence the life of semiconductor products. Voltage or current that exceeds the rated level may damage the semiconductor product; even if applied only momentarily and the unit continues to operate properly, excessive voltage or current will likely increase the failure rate.

Therefore, in actual circuit design, it is important that the semiconductor products have an allowance with respect to the voltage, current and temperature conditions under which they will be used. The greater this allowance, the fewer the failures that will occur.

To keep failures to a minimum, the circuit should be designed so that under all conditions to absolute maximum, the ratings are not exceeded even momentarily and so that the maximum values for any two or more items are not achieved simultaneously. In addition, remember that the circuit functions of semiconductor products are guaranteed within the operating temperature range (Topr) or the absolute maximum ratings, but that storage temperature (Tstg) is the range in a nonoperating condition.

Storage Precautions

General Storage Precautions

a. Storing product in the packing in which it is shipped is recommended. If transferred to a different container, use one that will not readily carry an electrostatic charge.

b. Store at conditions of normal tempetature (5-35°C) and normal humidity (45-75% RH).

c. Avoid storing product in the presence of corrosive gases or dusty areas.

d. Avoid storing product in areas of direct sunlight or where sudden temperature changes will occur.

e. Avoid stacking product or otherwise applying heavy loads.

f. In the case of extended storage, take particular care against corrosion and deterioration in lead solderability. Inspecting such product before use is recommended.

Basic Electrostatic Discharge Countermeasures

Semiconductor device mounting requires exacting precautions to avoid applying excessive static electricity to the semiconductor.
Item (a)-(c) below are basic electrostatic discharge countermeasures.

a. Use humidifiers and the like to ensure against excessively low relative humidity in the work environment. (Maintaining relative humidity consistently above 50% is ideal).

b. To prevent sudden electrostatic discharge, spread high-resistance electroconductive mats (about 10^6 Ω) over workbenches and have workers wear wrist (ground) straps.

   Have workers wear clothing made of charge-resistant cotton, noncharging materials (10^9-10^{14} Ω) or static electricity dissipating materials (10^5-10^9 Ω). Anti-static foot apparel is also effective.

c. Ionizers (ionized air blowers) are effective when it is difficult to discharge static electricity from mounting equipment, contacting dielectrics and semiconductors.

Sharp recommends using static electricity measuring devices to quantify electrostatic charges and develop effective countermeasures.

When forming the lead wires of semiconductor products to be mounted, forceps or a similar tool that will prevent stress from being applied to the base of the wires should be used.

To prevent the input terminals of semiconductor products on completed printed circuit boards from becoming open during storage or transport, the terminals of the circuit board should be shortcircuited or the entire circuit board itself should be wrapped in aluminium foil.

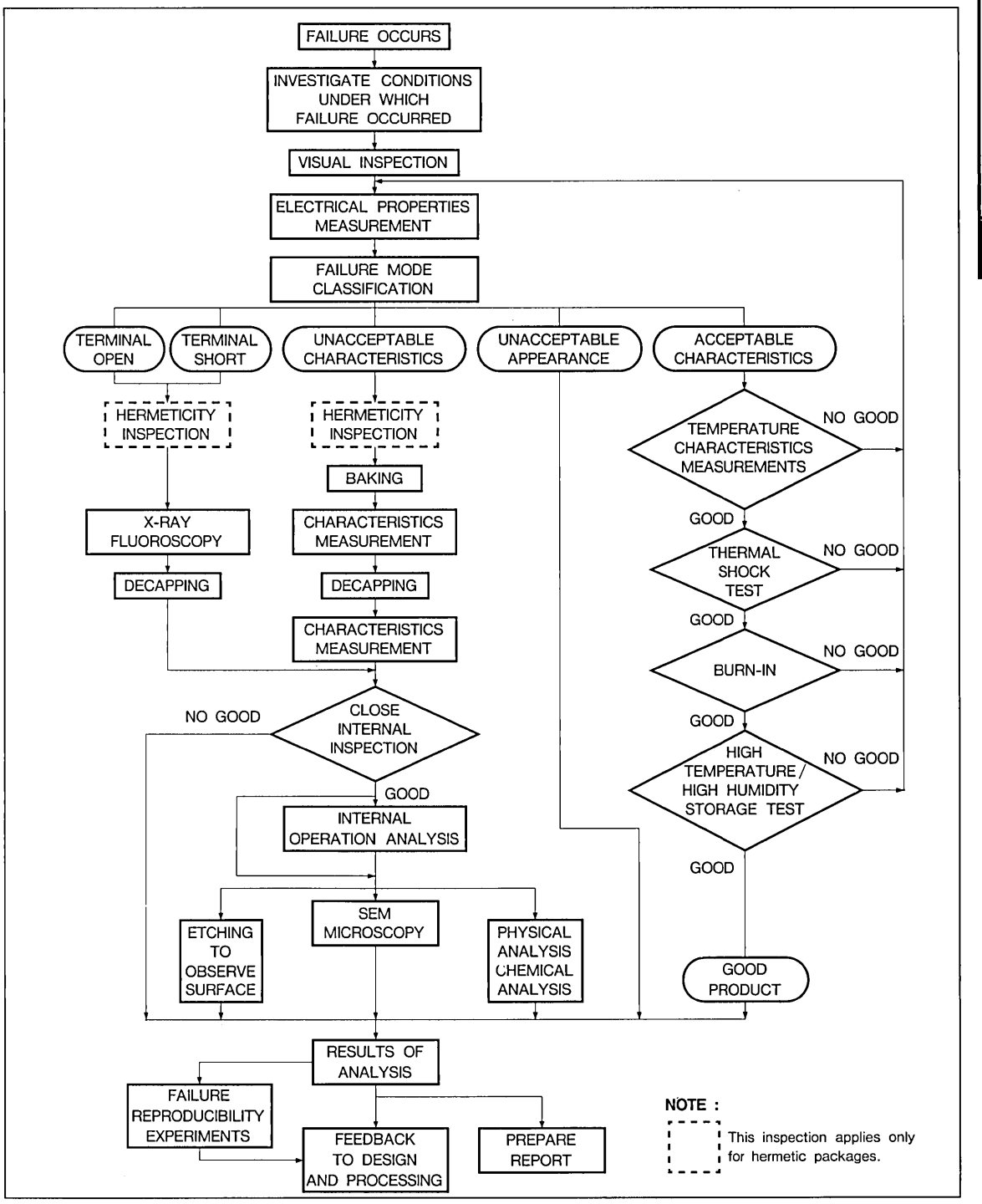


Fig. 6 Failure Analysis Procedure

Soldering and Cleaning

When a semiconductor product is solder-bonded, specify the best conditions according to ***Table 4***. If using a soldering iron, use one that doesn't leak from the soldering tip. An 'A Class' soldering iron with an insulation resistance of less than 10 MΩ is recommended. When using a solder bath, it should be grounded to prevent an unstable electric potential.

Using a strongly acidic or alkaline flux for soldering can cause corrosion of the lead wires. A rosin flux is ideal for this type of soldering.

To assure the reliability of a system, removal of the solder flux is generally required.

To prevent stress of semiconductor products and circuit boards when using ultrasonic cleaning, a cleaning method must be used that will shadow the main unit from the vibrator and specify the best conditions according to the following :

Table 3
Recommended Conditions for PC Board Cleaning

Ultrasonic Power	less than 25 W/l
Cleaning Conditions	less than one minute total
Cleaning Solution Temperature	15 to 40°C

Adjustment and Tests

When the set is to be adjusted and tested upon completion of the printed circuit board the printed circuit board must be checked to ensure that there are no solder bridges or cracks before the power is turned on. Also, if the market-rated voltage and current are to be used, it is wise to use a current limiter.

Whenever a printed circuit board is to be removed or mounted, or mounted on a socket, the power must be turned off.

When testing with a probe, care must be taken to assure that the probe does not come in contact with other signals or the power supply. If the test location has been decided beforehand, it is wise to set up a specially designed test-pin for testing.

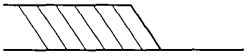
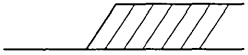
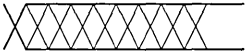
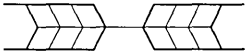
When testing in high and low temperatures, the constant-temperature bath must be grounded and measures taken to protect the set inside the bath from static electricity.

Table 4 outlines the semiconductor bonding and testing methods.

Table 4
Semiconductor Bonding and Testing Methods

BONDING METHOD	TEMPERATURE AND TIME	TEST POSITION
Infrared reflow	Peak temp. 240°C or less 230°C or more within 15 s Heating speed : 1 to 4°C/s	Surface IC package
Flow dipping	245°C or less Within 3 s/cycle Within 5 s in total	Solder bath
VPS	215°C or less 200 to 215°C within 40 s	Steam
Hand soldering (Using a soldering iron)	260°C or less, within 10 s	IC outer lead

TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM	INPUT FUNCTIONS	OUTPUT FUNCTIONS
	HIGH or LOW	HIGH or LOW
	HIGH-to-LOW transitions allowed	HIGH-to-LOW transitions during designated interval
	LOW-to-HIGH transitions allowed	LOW-to-HIGH transitions during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Centerline is high-impedance

32-BIT RISC MICROCOMPUTER

2

LH77790

Embedded Microcontroller

FEATURES

- Highly integrated single chip
- 32-bit ARM7D CPU core
- 2 kB (B : byte) data/instruction cache
- 2 kB Static RAM (4 kB without cache)
- Low power
- High performance
- Programmable clock and power management
- Programmable monochrome LCD controller
- On-chip interrupt controller
- Three UARTs - 16C450-class
- IrDA/DASK infrared interface
- Three pulse width modulator channels
- Simplified no glue memory interface
- On-chip DRAM controller
- 24-bit Programmable Peripheral Interface (PPI)
- Three 16-bit counter/timer channels
- Hardware watchdog timer
- Dual range operation
  5 V TTL / 25 MHz
  3.3 V LVTTL / 16.7 MHz
- Package : 160-pin TQFP (1.4 mm thinner type package)

DESCRIPTION

The LH77790 Embedded microcontroller is an ARM7D-based system on chip with a high level of integration. In addition to the CPU, it consists of a number of essential peripherals, instruction/data cache, and Static RAM. The targeted applications are handheld, battery operated devices that require performance greater than that available from 16-bit and 32-bit CISC-based controllers. These devices include all monochrome LCD displays, keyboards, non-volatile memory (typically Flash), Static RAM, and other communications ports and external peripherals. The Embedded controller provides the features required in these systems, including an LCD controller, no-glue memory (SRAM / DRAM / EEPROM / Flash) interface, and other peripherals that eliminate all external components, except for memory and buffers (i.e. RS232 level converters). The LH77790 allows an external bus master to take control of the external as well as the internal interface (address bus, data bus, controls).

APPLICATIONS

- Hand-held personal equipment (GPS, PDA, communication, games)
- Point-of-sale (barcode scanners, portable inventory controllers)
- Industrial instrumentation (portable oscilloscopes, analyzers)

DEVELOPMENT TOOLS

The ARM software development toolkit 2.0 provides a complete integrated environment for software development. The toolkit provides a complete toolset for :

- Software simulation via ARMulator
- Debugging via ARMs Embedded ICE JTAG debug tool
- ANSI C optimized compiler
- ARM assembler

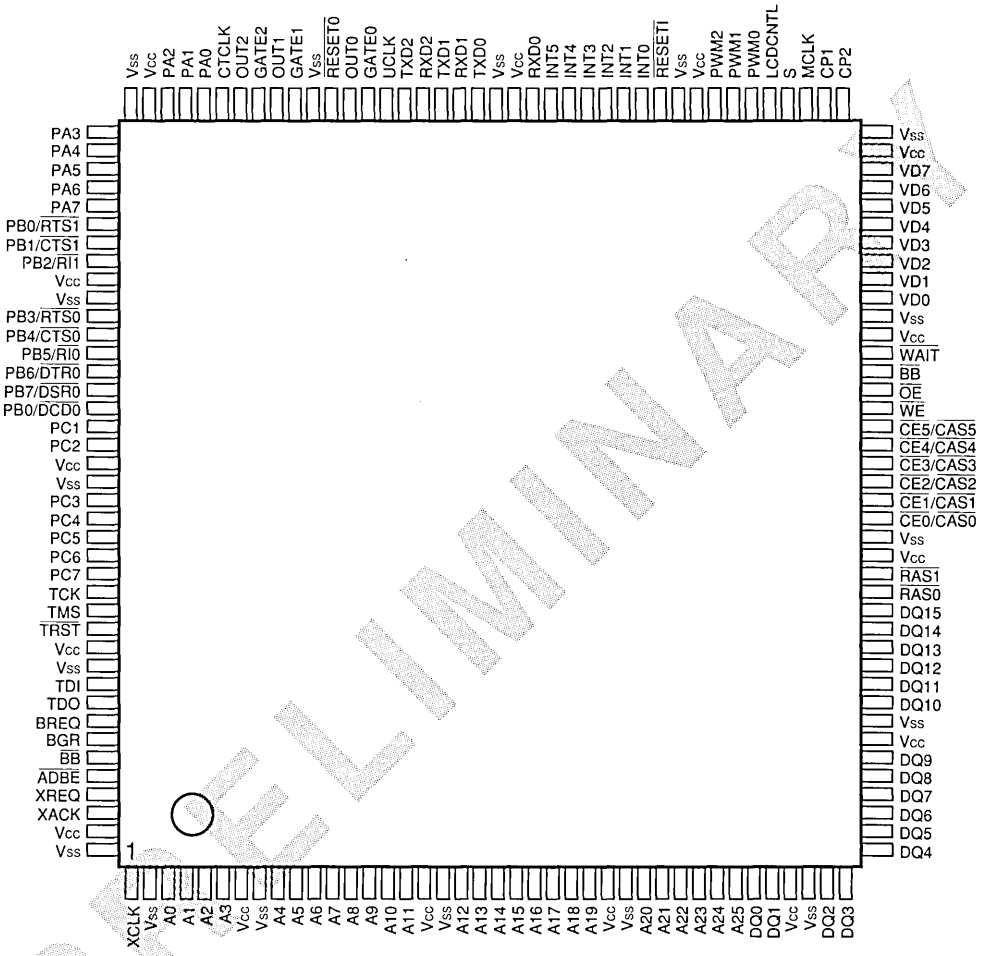
The ARM software development toolkit 2.0 is available on the following platforms :

- Windows 95
- Window 3.1x
- Windows NT (Intel and Alpha)
- MS DOS 6.x
- SunOs 4.1x

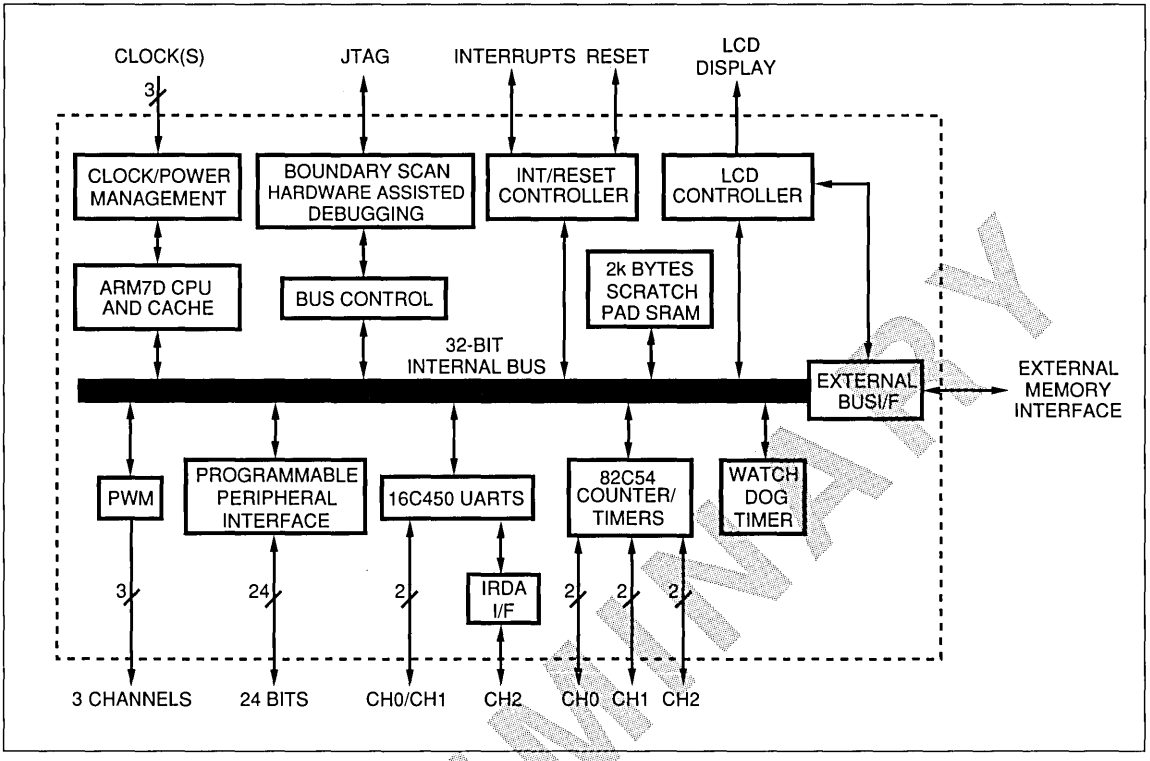
TM

PIN CONNECTIONS

160-PIN TQFP (1.4 mm thinner type package) TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	OPERATIONAL MODE#		DESCRIPTION
	MASTER	SLAVE	
EXTERNAL BUS INTERFACE			
A[25:0]*	O	I	**Master mode :** External address bus. The Embedded microcontroller will provide a 26-bit address to external memories and peripherals. **Slave mode :** External address bus. The external bus master will provide a 26-bit address to the Embedded microcontroller. The High order six bits of the address are provided by an internal programmable register giving the external bus master full access a 32-bit address space. The Embedded microcontroller tristates the address bus in Slave mode.
DQ[15:0]*	I/O	I/O	External 16-bit data bus. The Embedded microcontroller tristates the data bus in Slave mode.
$\overline{OE}$*	O	I	**Master mode :** Output enable for external memory and peripherals. $\overline{OE}$ allows external memory and peripherals to drive the data bus and is asseted Low during a read operation. **Slave mode :** Output enable for Embedded microcontroller. $\overline{OE}$ should be driven Low during a read operation by the external bus master. The Embedded microcontroller tristates $\overline{OE}$ in Slave mode.
$\overline{WE}$*	O	I	**Master mode :** Write enable for external memory and peripherals. During a write operation, this pin is driven Low. During a read operation, this pin is driven High. **Slave mode :** Determines the direction data transfer. Low indicates a write operation (External bus master --> Embedded microcontroller) and High indicates a read operation (Embedded microcontroller --> External bus master). The Embedded microcontroller tristates $\overline{WE}$ in Slave mode.
$\overline{CE}$[5:0]/ $\overline{CAS}$[5:0]	O	O	These pins provide the chip enables/column address select to directly connect to standard external memory/peripheral devices. The pins act as $\overline{CAS}$ when interfacing to DRAMs and $\overline{CE}$ otherwise. They are fully programmable by the system designer and can support byte enables.
$\overline{RAS}$[1:0]	O	O	Row address select pins for DRAM Bank 0 and Bank 1. Embedded microcontroller refreshes the external DRAM in both Master and Slave modes.
$\overline{WAIT}$	I	I	External memory wait. Allows the use of slow memories.
$\overline{BW}$*	O	I	**Master mode :** Byte wide access. The ARM-CPU indicates to external memory and peripherals the data size of the data transfer. When Low, the data transfer is a byte length. Can be used by an external address decoder to generate extra chip/byte enables. **Slave mode :** Size transfer. The external bus master indicates the transfer size. Low indicates a byte transfer and High indicates a halfword transfer. The Embedded microcontroller tristates $\overline{BW}$ in Slave mode.

$\overline{BB}$	I	O	**Master mode :** Byte boot selects between x8 or x16 for the boot memory. It is sampled when $\overline{RESETI}$ transitions from Low to High. **Slave mode :** The external bus master can provide its own address to the Embedded microcontroller on the address bus in which case this pin should be Low. The external bus master can also use an internal counter to the Embedded microcontroller as an address source in which case this pin should be High. In Slave mode, the High order six bits of the address are provided by an internal programmable register.
BREQ	I	I	Bus master request. An external bus master can request control of the external as well as internal interfaces (data bus, address bus, controls) by asserting this pin High. When the Embedded microcontroller is ready to release the Interface, it will drive High BGR. By asserting BREQ LOW, the external bus controller indicates to the Embedded microcontroller it is releasing the interface.
BGR	O	O	Bus master grant. Upon detecting BREQ=High, the Embedded microcontroller grants and allows the external bus master to take control of the external as well as internal interfaces by asserting this pin High, and releasing the data bus, address bus and controls. The Embedded microcontroller will operate in Slave mode. The external bus master has control as long as BGR is driven High. In Slave mode, the Embedded microcontroller will continue to refresh the DRAM banks as programmed. The Embedded Microcontroller can takeover (operate in Master mode) the interface by asserting BGR Low.
XREQ	I	I	**Master mode :** No function **Slave mode :** Transfer request. The external bus master can request access the Embedded microcontroller internal SRAM, cache, registers, DRAM controller, or SRAM controller by asserting this pin High during BFR=High, and providing address, data, and controls as necessary. Burst access is not supported.
XACK	O	O	Transfer acknowledge. Upon detecting XREQ=High, the Embedded microcontroller acknowledges the transfer request by asserting XACK HIGH, latching address, data, and controls. The Embedded microcontroller will take control of the interface by asserting BGR Low. Upon completing the transfer, the Embedded microcontroller will drive XACK Low, drive the data bus on a read operation and continue to assert BGR Low as long as XREQ is High. When XREQ is driven Low, the Embedded microcontroller assets BGR High giving the external bus master control of the Interface.
COUNTERS/TIMERS INTERFACE			
GATE[2:0]	I	I	Counter/timer control gate input signals.
OUT[2:0]	O	O	Counter/timer output signals may be connected to interrupt input signals.
INTERRUPT INTERFACE			
INT[5:0]	I	I	External interrupt input signals.

LCD CONTROLLER INTERFACE			
CP_2	O	O	Display data shift clock to LCD display.
CP_1	O	O	Display data latch pulse and scan signal transfer clock signal.
MCLK	O	O	LCD display frame signal.
S	O	O	Scan line start pulse to LCD display.
LCDCNTL	O	O	LCDC output control to LCD.
VD[7:0]	O	O	Video data to LCD display.
PROGRAMMABLE PERIPHERAL INTERFACE			
PA[7:0], PB[7:0], PC[7:0]	I/O	I/O	Parallel ports A, B, and C signals. Signals have programmable operation and can function as input, output or controls. PB[7:0] and PC0 are multiplexed with UART's MODEM signals.
PWM INTERFACE			
PWM[2:0]	O	O	Pulse width modulator output signals.
UARTS INTERFACE			
RxD[2:0]	I	I	UART serial data input signals. RxD2 also doubles as the digital input for the IrDA interface.
TxD[2:0]	O	O	UART serial data output signals. TxD2 also doubles as the digital output for the IrDA interface.
$\overline{RTS}$[1:0]	O	O	Request To send for UARTs 0 & 1. multiplexed with PB0 & PB3 respectively
$\overline{CTS}$[1:0]	I	I	Clear To send for UARTs 0 & 1. multiplexed with PB1 & PB4 respectively
$\overline{RI}$[1:0]	I	I	Ring indicator for UARTs 0 & 1. multiplexed with PB2 & PB5 respectively
$\overline{DTR_0}$	O	O	Data terminal ready for UART 0 only. multiplexed with PB6
$\overline{DSR_0}$	I	I	Data set ready for UART 0 only. multiplexed with PB7
$\overline{DCD_0}$	I	I	Data carrier detect for UART 0 only. multiplexed with PC0
RESET & EXTERNAL CLOCKS			
$\overline{RESETI}$	I	I	Chip reset Input. It should be driven Low for at least 6 cycles to guarantee a proper reset. $\overline{RESETI}$ has a built-in glitch detector. $\overline{RESETO}$ will be driven Low after a valid reset is detected for as long as $\overline{RESETI}$ is driven Low.
$\overline{RESETO}$	O	O	Chip reset output. It will be driven Low during : (1) Chip reset (2) WDT timeout reset (8 cycles) (3) Software controlled reset
XCLK	I	I	The Embedded microcontroller external clock input pin
UCLK	I	I	UART/DASK demodulator external clock input signal
CTCLK	I	I	Counter/timer external clock input signal.
JTAG INTERFACE			
TCK	I	I	JTAG test clock input signal. This pin is not part of the scan chain
TMS	I	I	JTAG test mode select input signal. This pin is not part of the scan chain
$\overline{TRST}$	I	I	JTAG test scan reset input. This pin is not part of the scan chain
TDI	I	I	JTAG test data input signal. This pin is not part of the scan chain
TDO	O	O	JTAG test data output signal. This pin is not part of the scan chain

TEST INTERFACE			
$\overline{\text{ADBE}}$	I	I	Test Pin. For normal operation, this pin should be Low. This pin is not part of the scan chain

N/A : Not Available

Master mode : The Embedded microcontroller is the bus master (BGR = 0)

Slave mode : An external device is the bus master (BGR = 1)

*Tristated in slave mode

FUNCTIONAL DESCRIPTION

CPU Core

The CPU core is the ARM7D. The ARM7D is comprised of the ARM7 processor, with Debugging (D) features provided with access via the JTAG test port.

FEATURES

- ARM7D 32-bit RISC CPU
- Low power consumption
- High performance
- Fast interrupt response with minimal context switching
- 25 MHz at 5 V, 16.7 MHz at 3.3 V
- Excellent High-level language support
- Simple but powerful instruction set
- Little endian operation Mode
- Fully static design for power sensitive applications

Cache

The 2 kB on-chip cache provides for zero wait state operation on cache hits. It is a combined data/instruction cache.

FEATURES

- 2 kB cache
- 4-way associative
- Line size = 1 word, 128 sets
- Combined instruction/data
- Write-Back Policy
- Least recently used replacement policy
- Four modes of operation :
  - 2 kB cache
  - 2 kB SRAM (giving a total of 4 kB local SRAM)
  - Flush mode
  - Invalidate mode

Local SRAM

The 2 kB local SRAM provides zero wait state operation and is ideal for fast access to critical data or code (such as interrupt service routines).

FEATURES

- 2 kB expandable to 4 kB (See Cache section)
- Read/write programmable

Memory and Peripheral Interface

The Embedded microcontroller supports standard x8 and x16 SRAM, DRAM, EEPROM, and Flash memory devices. It also supports memory mapped peripherals through a programmable external bus controller with little or no glue logic, resulting in lower power consumption and cost savings in device count and board area.

FEATURES

- Supports 26-bit address bus
- Supports 16-bit data bus
- Memory management
- SRAM controller
  - Six SRAM banks
- DRAM controllers
  - Two DRAM banks
- Programmable properties:
  - Six multiplexed chip enables/nCAS pins
  - Two RAS pins
  - 0-7 wait states
  - 8/16-bit bus width
  - Half word access
  - Access privilege for user/system
- External memory mapped I/O support
- LCD frame buffer support

Memory Management

The ARM CPU can address up to 4 GB of address space (32-bit internal address). The Embedded microcontroller can address up to 64 MB (26-bit external address). The Embedded microcontroller supports up to eight programmable segments (0-7). Each segment can address 64 MB of external memory. This will give a total of 512 MB external addressable space.

FEATURES

- Supports eight programmable segments
- Supports one default segment
- Each segment consists of :
  - START register
  - STOP register
  - Segment descriptor register (SDR)
- SDR contains information on :
  - System/user privileges
  - Cacheability
  - Cache write policy
  - 16/32-bit mode
  - Memory bank selection
- Supports eight memory banks
  - Six SRAM banks and two DRAM banks
  - Each bank has a bank configuration register (BCR)
  - BCRs reflect external memory properties

Logical To Physical Mapping

When the external bus controller receives an internal address for a memory access, it maps the address to the appropriate segment (or default segment) and performs all the necessary check for cacheability and privileges as programmed in the SDR. Once all the checks are passed, the external bus controller accesses the appropriate memory bank, BCR, as programmed in the SER. BCR tells the external bus controller which external device to select and its properties. The lower 26 bits of the address are used to address the external device.

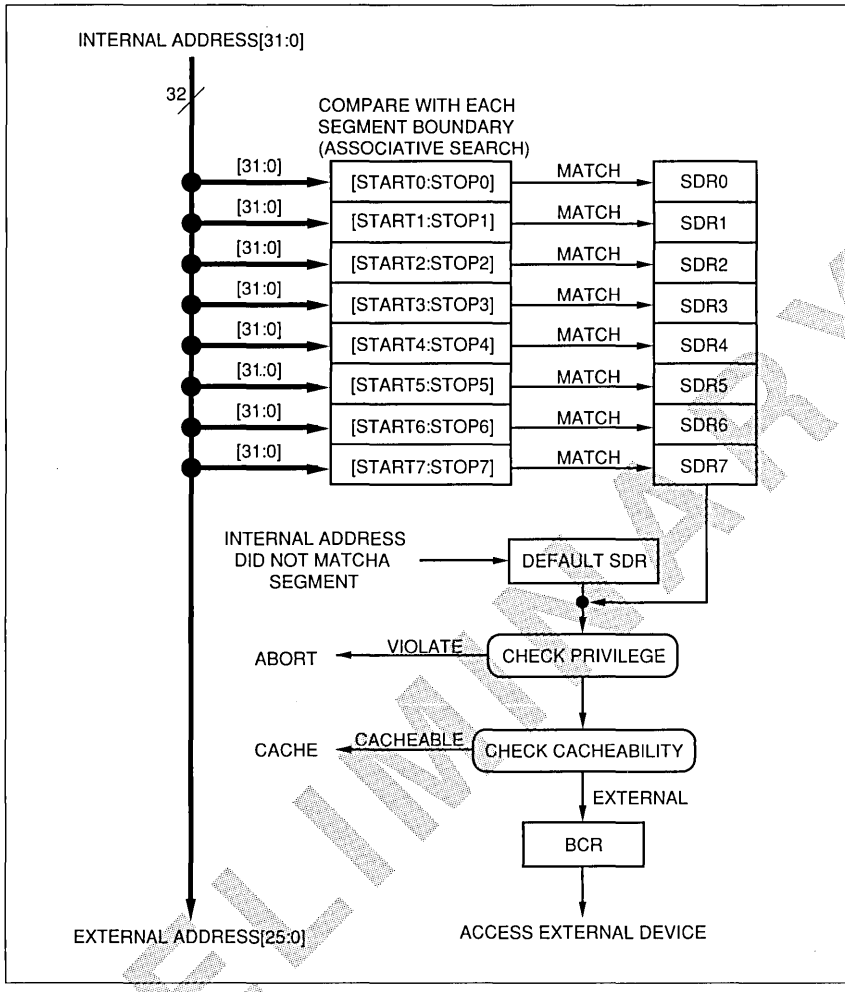


Fig. 1 Logical to Physical Address Mapping

DRAM Controller

The Embedded microcontroller supports a wide range of x8, and x16 DRAMs. The On-chip DRAM controller eliminates the need for an external DRM controller, and simplifies the design of the system.

FEATURES

- Supports x8 and x16 DRAM
- Supports up to 2 banks
- Each bank can be programmed for :
  - Device size (256 kB-64 MB)
  - Device width (8, 16 bits)
  - Fast page mode
  - Refresh rate (One RR for both banks)
  - Memory protection
- CAS before RAS refresh

UART

The Embedded microcontroller provides three 16C450-class UART macrocells (Universal Asynchronous Receiver/Transmitter). UART_0 supports a nine-wire interface (TxD, RxD, $\overline{RTS}$, $\overline{CTS}$, $\overline{DTR}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{RI}$, and GND). UART_1 supports a six-wire interface (TxD, RxD, $\overline{RTS}$, $\overline{CTS}$, $\overline{RI}$, and GND). UART_2 supports a three-wire interface (TxD, RxD, and GND) and is IrDA-IR and SHARP DASK-IR compliant.

FEATURES

- Double buffering
- 16-bit programmable baud rate generator
- Independently controlled interrupts
  - Receive, transmit, line status, and MODEM status
- Fully-prioritized interrupt system control
- Programmable interface characteristics
  - 5 to 8-bit data
  - Even, odd, no parity
  - 1, 1-1/2, 2 stop bits
- Complete status reporting
- False start bit detection
- Line break generation and detection
- Full MODEM support on UART_0
- Loop back mode on UART_0
- UART_2 supports three modes of operation :
  - Pass through : Gives a total of three UARTs
  - IrDA SIR : Gives a total of two UARTs + one infrared Port
  - DASK SIR : Gives a total of two UARTs + one infrared port

Serial Infrared (SIR) Interface

The Embedded microcontroller has a serial infrared (SIR) interface that is IrDA and SHARP-DASK compatible. The interface connects to UART_2 and performs format encoding/decoding between UART format and IrDA/DASK SIR format. The SIR interfaces directly to any external IrDA/DASK transceiver module.

FEATURES

- IrDA SIR (version 1.0) compatible
- SHARP DASK SIR compatible
- Adds IR port to UART_2
- 2.4 Kbps to 115.2 kbps IrDA data rate
- 2.4 Kbps to 57.6 Kbps DASK data rate
- Sleep mode to save power
- Three modes of operations :
  - Pass through : Three serial ports
  - IrDA SIR : Two serial ports + one infrared port
  - DASK SIR : Two serial ports + one infrared port
- UART format ↔ SIR format

APPLICATIONS

The SIR interface is an important feature that allows wireless communications and data exchange between hand-held devices, office equipment, and office networks. It is an ideal solution for compact, low-power, cost-sensitive applications.

Pulse Width Modulator (PWM)

The Embedded microcontroller supports three fully independent pulse width modulator channels (PWM0, PWM1, PWM2) with the frequency range shown in Table 1.

Table 1 PMW Channels

SYSTEM CLOCK FREQUENCY	PWM PULSE FREQUENCY RANGE	
	16-BIT RESOLUTION	8-BIT RESOLUTION
16.7 MHz	4.10 Hz - 4.17 MHz or DC	1.05 kHz - 4.17 MHz or DC
25 MHz	6.15 Hz - 6.25 MHz or DC	1.58 kHz - 6.25 MHz or DC

FEATURES

- Each PWM channel is independent
- Frequency range :
  - DC High or Low
  - 4.10 Hz : 6.25 MHz
- Easy to program
- One 16-bit resolution PWM and two 8-bit resolution PWMs
- Programmable Synchronous mode support
  - This will produce a synchronized sequence of PWM pulses
- Programmable pulse width (Duty Cycle) and interval (frequency)
  - Static programming : PWM is stopped/disabled
  - Dynamic programming : PWM is runnint/enabled
    - Double buffering allows dynamic programming
    - Updates to duty cycle and frequency are done at end of a PWM cycle
- Enable/disable PWM
  - Disable PWM output at end of a PWM cycle
- Sleep mode to save power
- PWM output connected to on-chip counters
  - This feature simplifies building applications like A/D
- Ability to invert the PWM output on the fly

APPLICATIONS

Pulse Width Modulation (PWM) is used in a variety of applications, such as :

- LED intensity control
- LCD gain and contrast
- Automotive engine control
- DC motor speed
- D/A and A/D conversion
- Sound synthesis
- Laser applications
- Servo motor control

LCD Controller

The LCD controller provides control and pixel data for directly driving LCD displays. The Video frame buffer resides in the CPU main memory, eliminating the need for additional pins for a frame buffer memory interface and memory component(s) for the buffer. The LCD controller supports two primary modes : Binary mode (on, off) and Gray mode (on, off, or two gray shades).

FEATURES

- Frame buffer resides in CPU main memory
- LCD Display modes :
  - Binary mode : Pixels are On or Off (1 bit/pixel)
  - Gray mode : Pixels are On, Off, or one of two intermediate gray shades (2 bits/pixel)
- LCD panel :
  - Single (4-bit and 8-bit data transfer)
  - Double (4-bit data transfer)
- Panel division or OR function in Single panel mode
- Maximum resolution :
  - Horizontal : 2048 pixels in Binary mode, 1024 pixels in Gray Mode
  - Vertical : 1024 lines in single scan, 2048 lines in dual scan
- Virtual display screen
- Smooth vertical scrolling
- DMA data transfers for panel refresh from main memory to maximize system performance
  - CPU can be running out of cache with no interference from the LCD controller

Counters/Timers

The Embedded microcontroller provides three independent 16-bit counter/timer (CNT/TMR) channels. Each channel can operate in one of six modes and works with either Binary or BCD counting. The current counter value, control word, and current state of each OUT signal are available to the CPU.

FEATURES

- Six modes of operation:
  - Mode 0 : Interrupt on terminal count
  - Mode 1 : Hardware retriggerable one-shot
  - Mode 2 : Rate generator
  - Mode 3 : Square wave Mode
  - Mode 4 : Software triggered strobe
  - Mode 5 : Hardware triggered strobe
- Binary or BCD counting
- CPU has access to the following :
  - Current counter value
  - Control word
  - Current state of OUT signals
- Selectable Input clock
  - System clock
  - External clock
- Power management
  - Scale down system clock
  - Halt input clock

APPLICATIONS

- Accurate time delays
- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Motor control

Programmable Peripheral Interface (PPI)

The Embedded microcontroller provides an 8225-class Programmable Peripheral Interface (PPI). It is a general-purpose I/O unit to interface peripherals to the Embedded microcontroller with no external glue logic. It has three 8-bit ports which can be programmed as inputs or outputs. The inputs and outputs can be read or written directly, or they can be strobed by external signals providing handshaking and interrupt signals.

FEATURES

- 24 programmable I/O signals
  - Three 8-bit ports : Port A, Port B, and Port C
- Bit set/reset capability
- Read/write control register
- Three modes of operation
  - Basic input/output
  - Strobed input/output
  - Strobed bidirectional I/O
- Data, control, and status bits

APPLICATIONS

The Programmable Peripheral Interface (PPI) can be used for :

- Printer interface
- Keyboard and display interface
- D/A and A/D interface
- Basic floppy disk interface

Interrupt Controller

The on-chip interrupt controller supports both internal and external interrupt sources. Internally there are six peripheral interrupt sources (three UARTs and three counters/timers). Externally there are six interrupt sources (INT[5:0]).

FEATURES

- Each interrupt Source is programmable :
  - Enabled
  - Cleared
  - Active High or Low
  - Drive $\overline{IRQ}$ or $\overline{FIQ}$ (ARM7D Interrupts)
  - Level or edge triggered
- In Sleep mode, the CPU clock is restarted when an interrupt is detected

Clock and Power Management

The clock and power management unit (C&PM) distributes the clock to the CPU core and peripherals, and provides a programmable clock divider to the CPU and peripherals that serves to reduce power. The CPU and peripheral can have their clocks stopped to further reduce power. The CPU clock, when halted, restarts at the fastest speed when an interrupt to the CPU is detected (either IRQ or FIQ).

FEATURES

- Clock control and power management
- Provide clocks to the CPU core and peripherals
- Provide a programmable clock divider to the CPU
- Provide a programmable clock dividers to UARTs and counters/timers (LCD controller and PWMs have built-In programmable clock dividers)
- Stop clocks to CPU and/or peripherals
- CPU clock is restarted when an interrupt is detected

Watchdog Timer

The watchdog timer is a hardware protection against malfunctions. It is a programmable timer that is reset by the software at regular intervals. Failure to do so causes the Embedded microcontroller to interrupt/reset. As long as the system is operating properly, the software that is executing clears the timer on a regular basis.

FEATURES

- Selectable input clock
  - System clock
  - System clock/8
- Selectable Timeout interval
  - Four intervals
- Freeze option
- Protection mechanism
- Selectable Timeout action
  - Non-maskable interrupt
  - Chip reset
- Power management

I/O Configuration

The Embedded microcontroller has a 24-bit input/output configuration register (IOCR) that allows the system designer to program multifunctional pins, select between internal and external clocks for the UARTs and counter/timers, and control the GATE signals to the counter/timers.

Reset

The Embedded microcontroller uses the **RESETI** input signal to generate a global chip reset. This signal must be held Low upon system power-up and remain Low for at least six clock cycles after V_{CC} has stabilized. **RESETI** is a level sensitive signal. A Low level causes the instruction being executed to terminate abnormally. When **RESETI** becomes High for at least one clock, the ARM CPU restarts from address 0 in supervisor mode and all peripherals are reset. During the Low period, the processor performs dummy instruction fetches with the address incrementing from the point where reset was activated.

In addition to holding the **RESETI** Low, the boundary scan reset input, **TRST**, must be pulsed or driven low to achieve normal device operation upon power-up. If the boundary scan interface is used, then **TRST** must first be driven Low, then High. If the boundary scan interface is not used, then **TRST** input may be tied permanently Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to 6.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	T_{OPR}	0 to 70	°C
Storage temperature	T_{STG}	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	3.0 to 3.6	3.3 / 5.0	4.5 to 5.5	V	1
Input High voltage	V_{IH}	2.0		V_{DD}+0.5	V	1
Input Low voltage	V_{IL}	−0.5		0.8	V	1
Operating temperature	T_{OPR}	0		+70	°C	

NOTE :

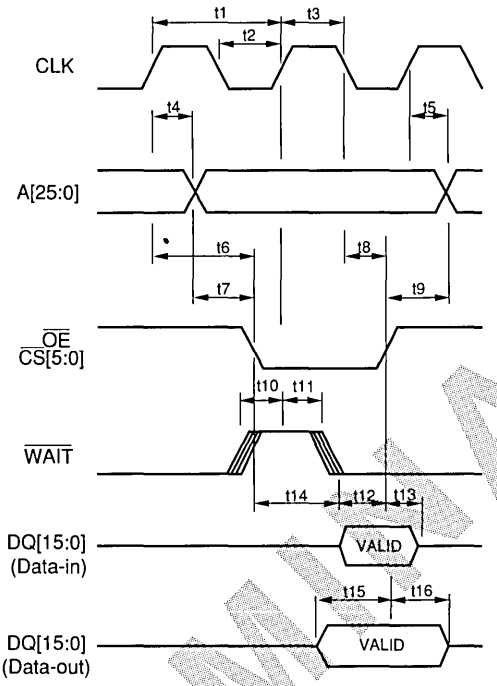
1. The applicable voltage on any pin with respect to V_{SS} (0 V).

DC ELECTRICAL SPECIFICATIONS

(Ta = 0 to +70°C)

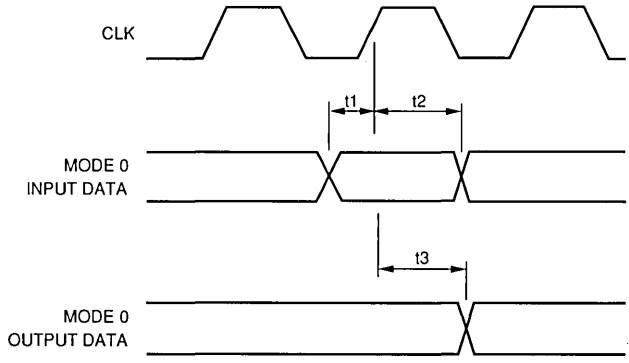
PARAMETER	SYMBOL	CONDITIONS	V_{CC} = 3.0 to 3.6 V		V_{CC} = 4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Input Low voltage	V_{IL}		−0.3	0.8	−0.3	0.8	V
Input High voltage	V_{IH}		2.0	V_{CC}+0.3	2.0	V_{CC}+0.3	V
Output Low current	I_{OL}	V_{OL} = 0.4 V	2.0		8.0		mA
Output High current	I_{OH}	V_{OH} = 2.4 V	−4.0		−8.0		mA
Input leakage current	I_{IL}	V_{IN} = 0 to V_{CC} MAX.	−2	2	−2	2	µA
Output, input/output leakage current	I_{OZ}	V_{IN} = 0 to V_{CC} MAX.	−2	2	−2	2	µA
Average active operating current	I_{CC} (Active)	F = $F_{MAX.}$		30		115	mA
Average halt current	I_{CC} (Halt)	F = $F_{MAX.}$		1		2	mA

AC SPECIFICATIONS
• Memory I/F Timing



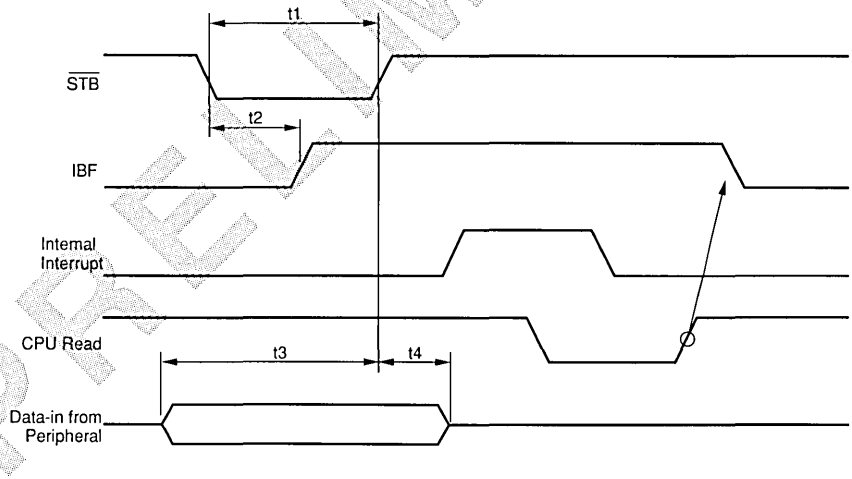
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Clock period			40		ns
t_2	Clock High			20		ns
t_3	Clock Low			20		ns
t_4	Clock High to address valid				15	ns
t_5	Address hold from clock			5		ns
t_6	Clock High to control active - $\overline{WR}$, $\overline{OE}$, $\overline{CE}$ (5:0)				15	ns
t_7	Address to control setup			3		ns
t_8	Clock Low to control inactive - $\overline{WR}$, $\overline{OE}$, $\overline{CE}$ (5:0)			5	15	ns
t_9	Address hold from control inactive			3		ns
t_{10}	$\overline{WAIT}$ setup to clock High			5		ns
t_{11}	$\overline{WAIT}$ hold from clock High			5		ns
t_{12}	Data-in setup to control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			5		ns
t_{13}	Data-in hold from control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			0		ns
t_{14}	Control active to data-in valid - (memory access time)			25		ns
t_{15}	Data-out setup to control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			20		ns
t_{16}	Data-out hold from control ($\overline{WR}$, $\overline{CE}$ (5:0))			5		ns

• Parallel I/O Port Timing - Mode 0 Input & Output



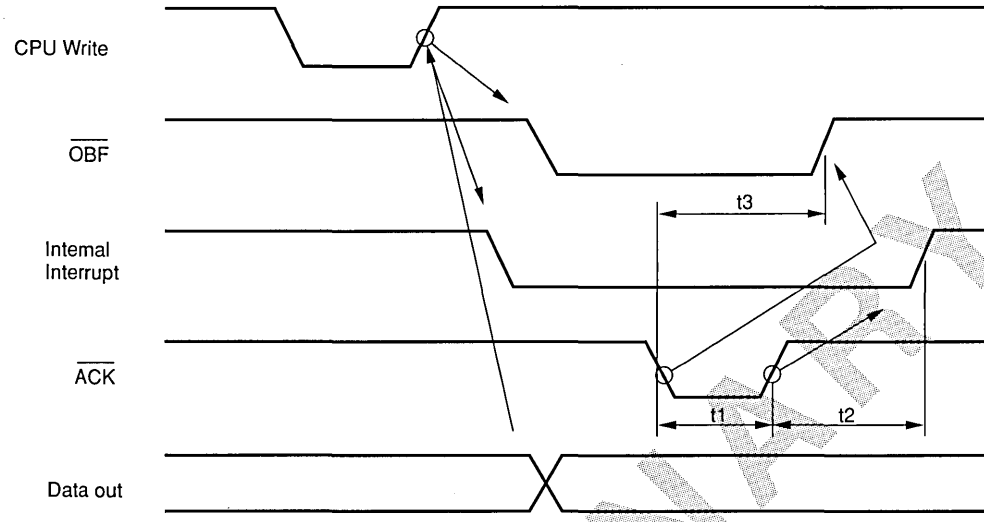
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Data-in set-up to CLK	12		7		ns
t_2	Data-in hold from CLK	0		0		ns
t_3	CLK to data-out valid		34		20	ns

• Parallel I/O Port Timing - Mode 1 Strobed Input



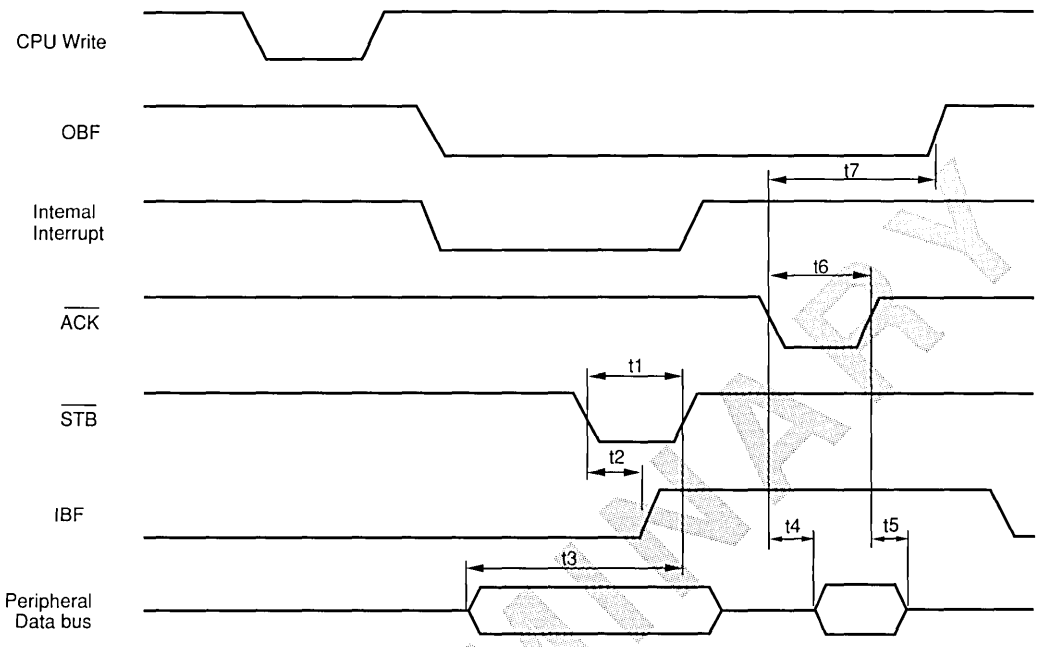
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{STB}$ pulse width	45		25		ns
t_2	$\overline{STB}$ falling edge to IBF active	0	35	0	20	ns
t_3	peripheral data-in set-up to $\overline{STB}$ High	20		10		ns
t_4	peripheral data-in hold from $\overline{STB}$ High	0		0		ns

• Parallel I/O Port Timing - Mode 1 Strobed Output



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{ACK}$ pulse width	40		25		ns
t_2	$\overline{ACK}$ High to interrupt disable	TBD		TBD		ns
t_3	$\overline{ACK}$ Low to $\overline{OBF}$ High delay		35		20	ns

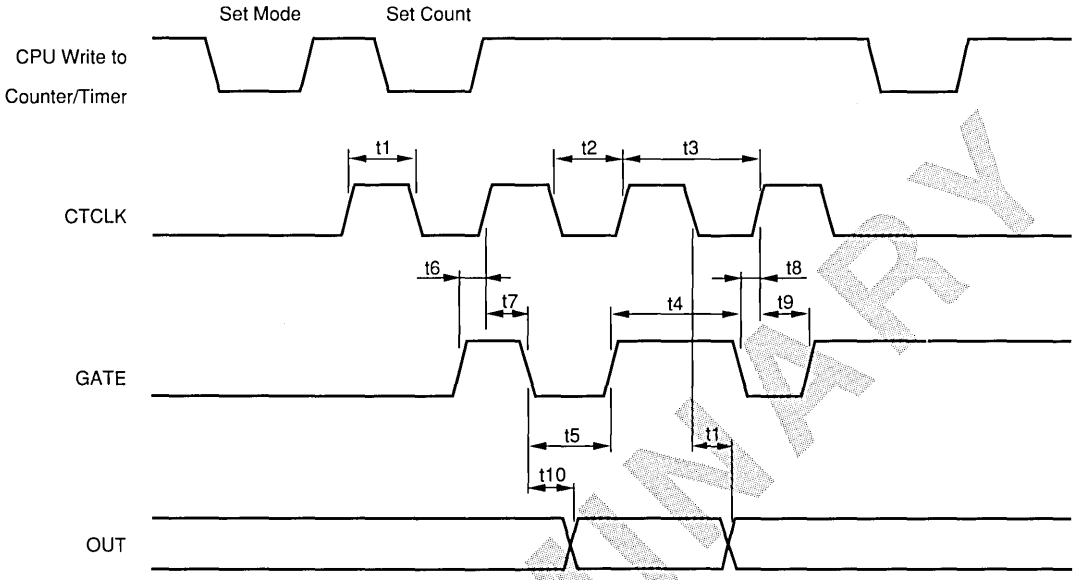
• Parallel I/O Port Timing - Mode 2 Bi-Directional Data Transfer



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{STB}$ pulse width	40		25		ns
t_2	$\overline{STB}$ Low to IBF High delay		35		20	ns
t_3	Peripheral data-in set-up to $\overline{STB}$ High	20		10		ns
t_4	$\overline{ACK}$ Low to data-out valid delay		35		20	ns
t_5	$\overline{ACK}$ High to data-out Hi-Z delay		35		20	ns
t_6	$\overline{ACK}$ pulse width	40		25		ns
t_7	$\overline{ACK}$ Low to $\overline{OBF}$ High delay		35		20	ns

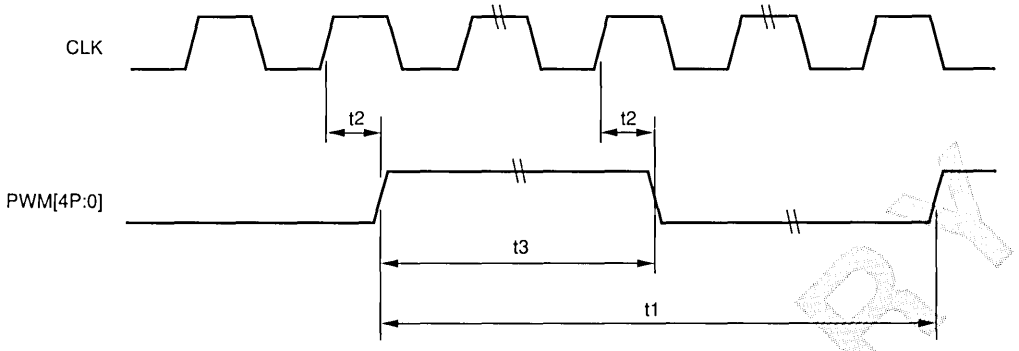
Hi-Z = High impedance

• Counter/Timer Timing



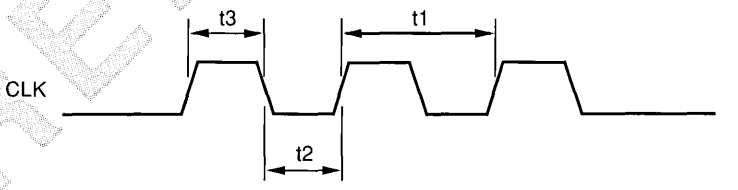
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	CTCLK High time	30		20		ns
t_2	CTCLK Low time	30		20		ns
t_3	CTCLK period	60		40		ns
t_4	GATE High time	40		25		ns
t_5	GATE Low time	40		25		ns
t_6	GATE High set-up to CLTCLK	15		10		ns
t_7	GATE High hold from CTCLK	0		0		ns
t_8	GATE Low set-up to CTCLK	15		10		ns
t_9	GATE Low hold from CTCLK	0		0		ns
t_{10}	GATE to OUT delay	0	35	0	20	ns
t_{11}	CTCLK to OUT delay	0	35	0	20	ns

• PWM Timing



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	PWM pulse period	CLK / prescale		CLK / prescale		CLK periods
t_2	CLK to PWM delay	0	15	0	12	ns
t_3	PWM active pulse width		34		20	CLK periods

• Clock Timing

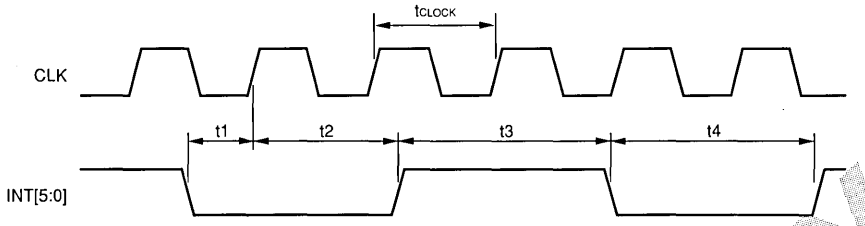


PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Clock cycle time	60		50		ns
t_2	Clock Low time	24		20		ns
t_3	Clock High time	24		20		ns

NOTE :

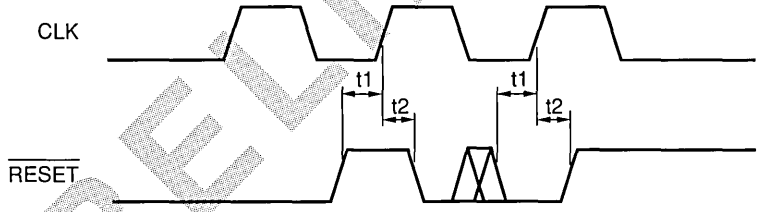
CLK timings are measured to 50% V_{CC}.

• External Interrupt Timing



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	External interrupt set-up time. (only used to insure capture on next active clock edge)	20		10		ns
t_2	External interrupt hold time. (only used to insure capture on next active clock edge)	20		10		ns
t_3	External interrupt active High interval	3 x t_{CLOCK}		3 x t_{CLOCK}		
t_4	External interrupt active Low interval	3 x t_{CLOCK}		3 x t_{CLOCK}		ns

• Reset Timing



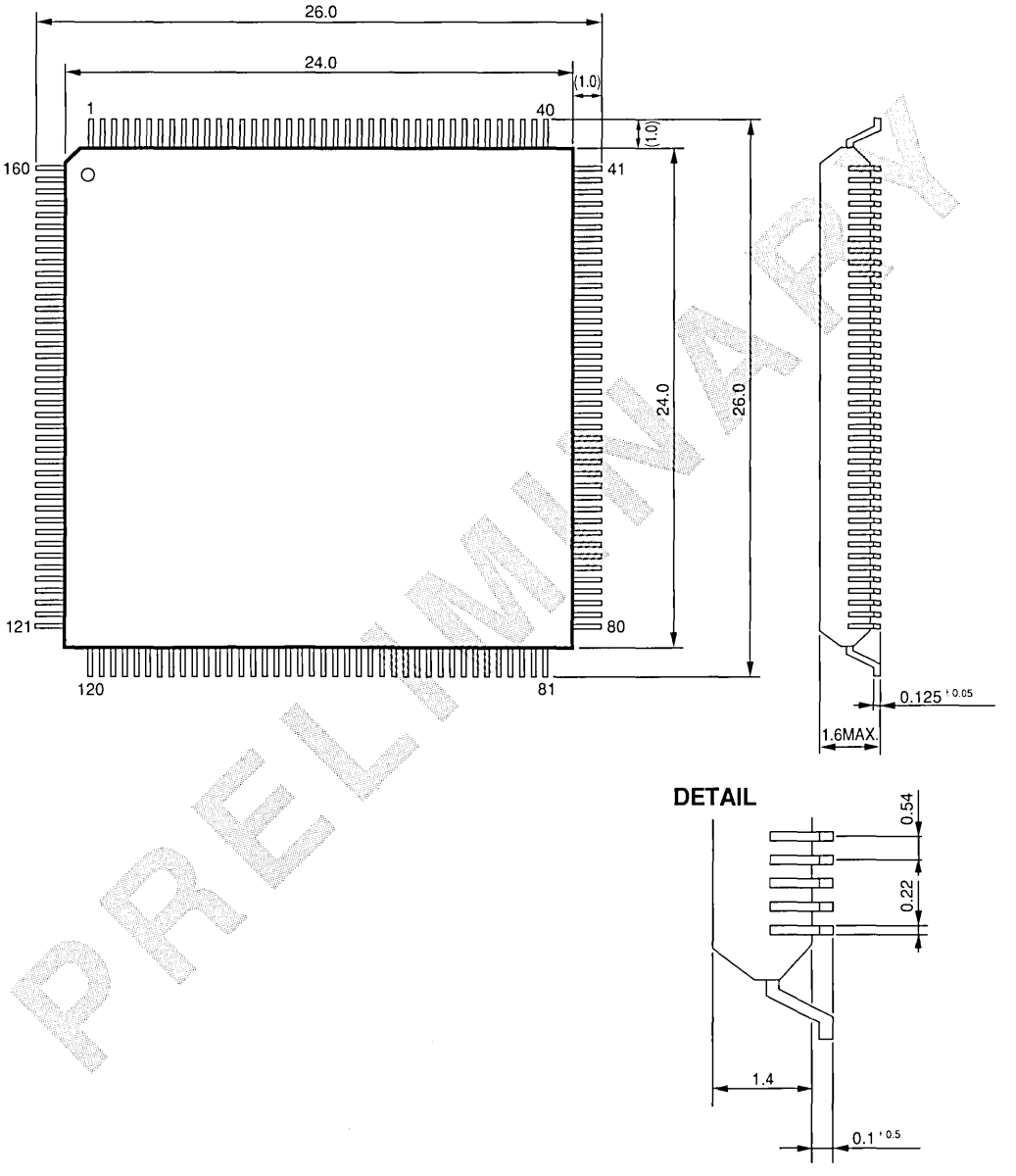
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_1	$\overline{\text{RESET}}$ setup to CLK	60		50		ns	1, 2
t_2	$\overline{\text{RESET}}$ setup to CLK	24		20		ns	1, 2

NOTES :

1. $\overline{\text{RESET}}$ is an asynchronous input, setup and hold times only ensure the signals are captured at the specified clock edge.
2. $\overline{\text{RESET}}$ must remain Low for 16 CLK periods after the power supply and clock have stabilized.

PACKAGE DIMENSION

160-PIN TQFP (1.4 mm thinner type package)



Development Environment for ARM Microprocessors

The RISC development environment requires an advanced high-level language compiler that allows the advantages of RISC microprocessors to be exploited fully.

The software development toolkits for ARM microprocessors are offered by ARM and GH*.

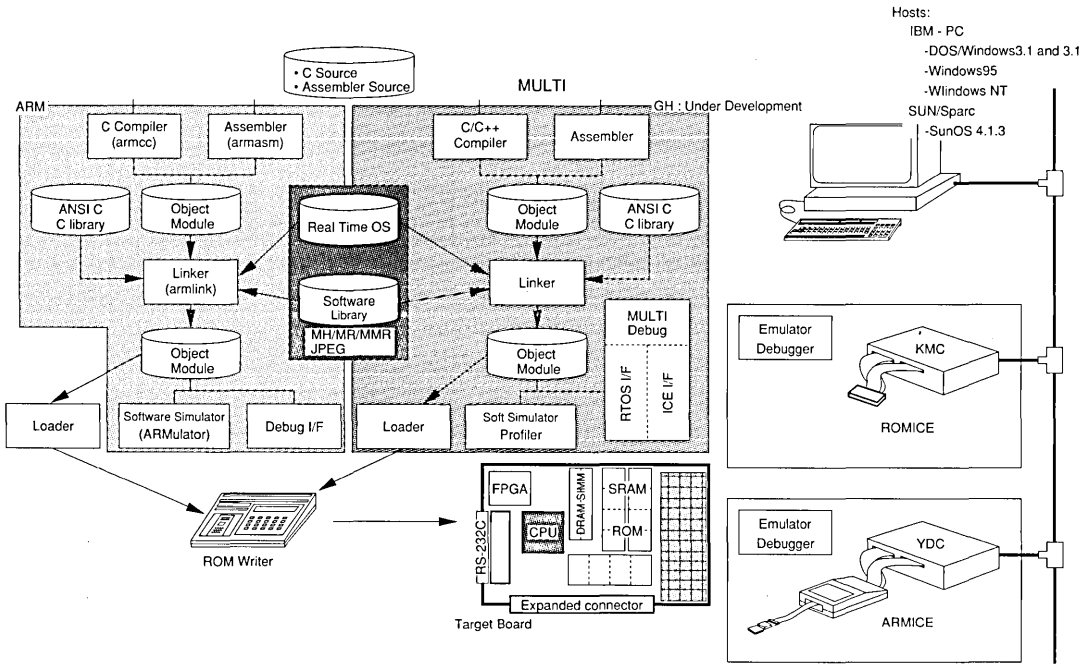
We hope that system engineers who develop software for 32-bit RISC Microcomputer LH77790 will make full use of these advanced tools.

* Under development

ARM : Advanced Risc Machines, Ltd.

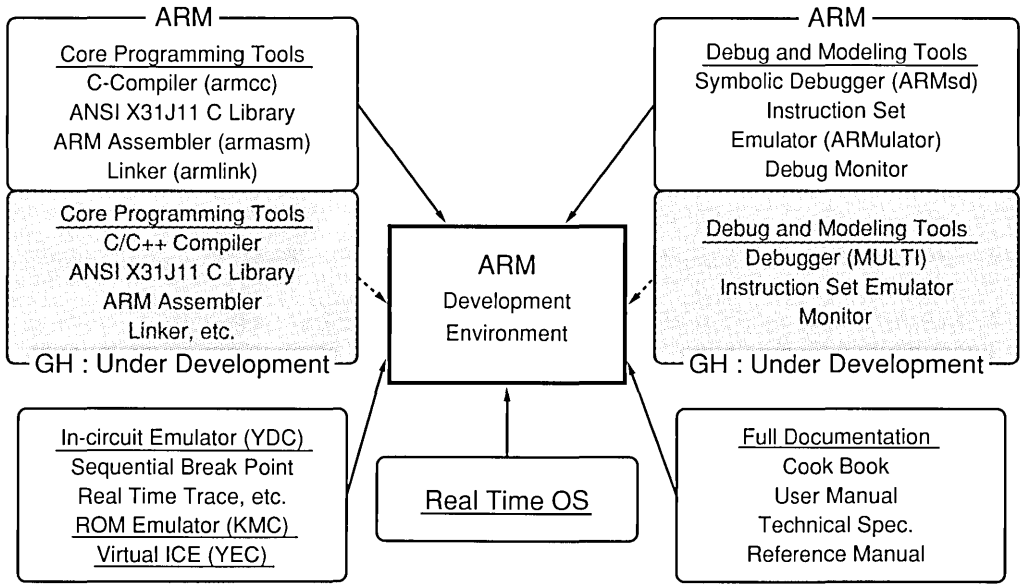
GH : Green Hills Software, Inc.

SOFTWARE DEVELOPMENT ENVIRONMENT



SOFTWARE DEVELOPMENT TOOLKIT

The ARM cross-development toolkit has five key components:



16-BIT SINGLE-CHIP MICROCOMPUTER

SM6004

Low-Voltage High-Speed 16-Bit Single-Chip Microcomputer

DESCRIPTION

The SM6004 is a 16-bit single chip microcomputer incorporating a 16-bit CPU core, ROM, RAM, timer unit, watch dog timer, serial interface (UART, SIO), PWM output, real time output, A/D converter, D/A converter and bus controller.

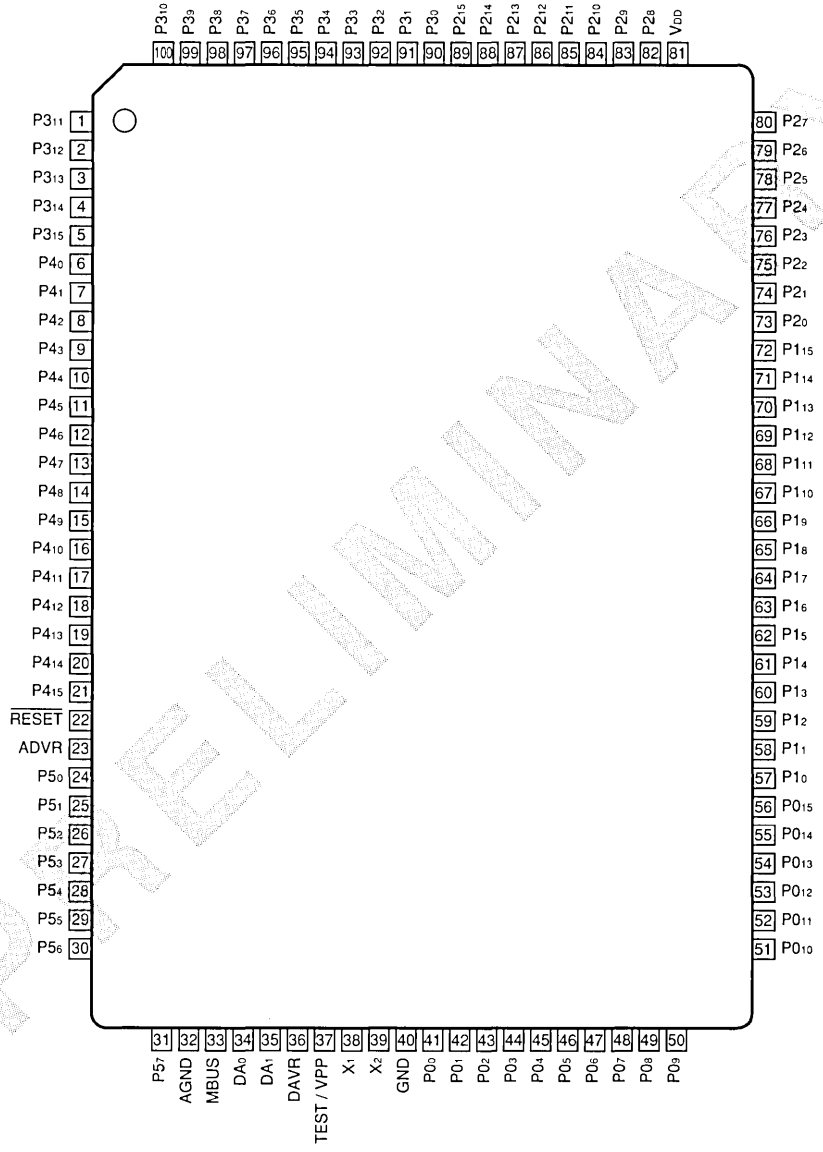
FEATURES

- ROM capacicity : 61 440 x 8 bits
- RAM capacicity : 2 048 x 8 bits
- Versatile timer units : 16 bits counter x 6
  - Timer 0: 16 bits counter x 1; Capture register x 5; Compare register x 2
  - Timer 1: 16 bits counter x 1; Capture register x 1; Capture/compare register x 1
  - Timer 2: 16 bits counter x 1; Capture register x 1; Capture/compare register x 1
  - Timer 3: 16 bits counter x 1; Compare register x 1
  - Timer 4: 16 bits counter x 1; Compare register x 1
  - Timer 5: 16 bits counter x 1; Compare register x 2; PWM output available
- Watch dog timer : 8 bits x 1
- Serial interface :
  - UART/SIO x 2 (built-in baud rate generator)
  - SIO x 1
- PWM outputs :
  - 14 bits x 2
  - (14, 12, 10, 8 bits selectable)
- Real time outputs : 4 bits x 2
- A/D converter :
  - Resolution 10 bits
  - Channels 8
- D/A converter : 8 bits x 2
- Bus controller
  - External bus access function
  - Multi-/nonmulti- address and data selectable
  - Selectable bus width, 8 and 16 bits
  - Auto-wait function
- I/O ports :
  - Input 8 bits x 1 (also used as A/D input)
  - Input/output 16 bits x 5
- Supply voltage :
  - 2.5 to 5.5 V (at 20 MHz main clock)
  - 4.5 to 5.5 V (at 30 MHz main clock)
- Package :
  - 100-pin QFP (QFP100-P-1420)
  - 100-pin LQFP (LQFP100-P-1414)

PIN CONNECTIONS

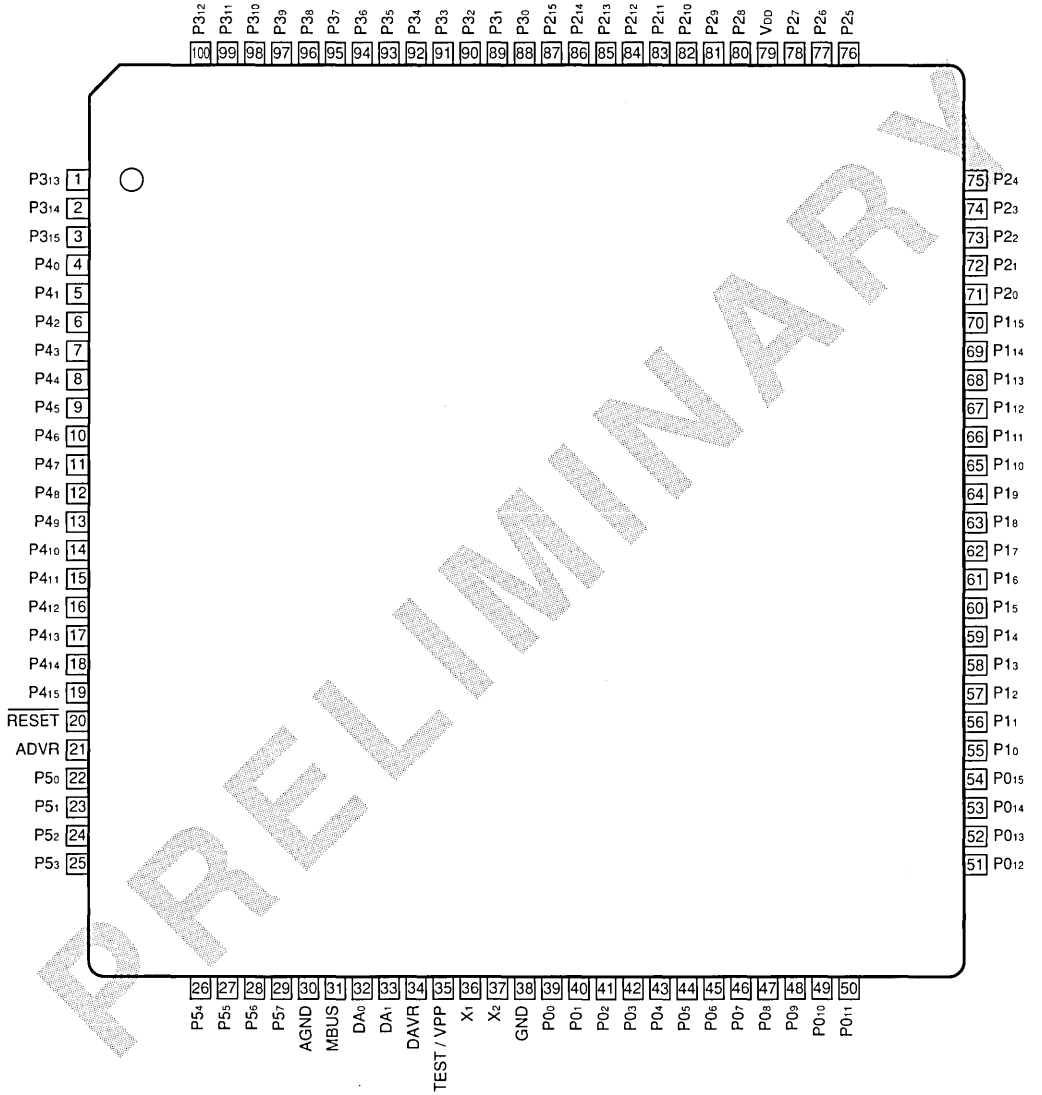
100-PIN QFP

TOP VIEW



100-PIN LQFP

TOP VIEW



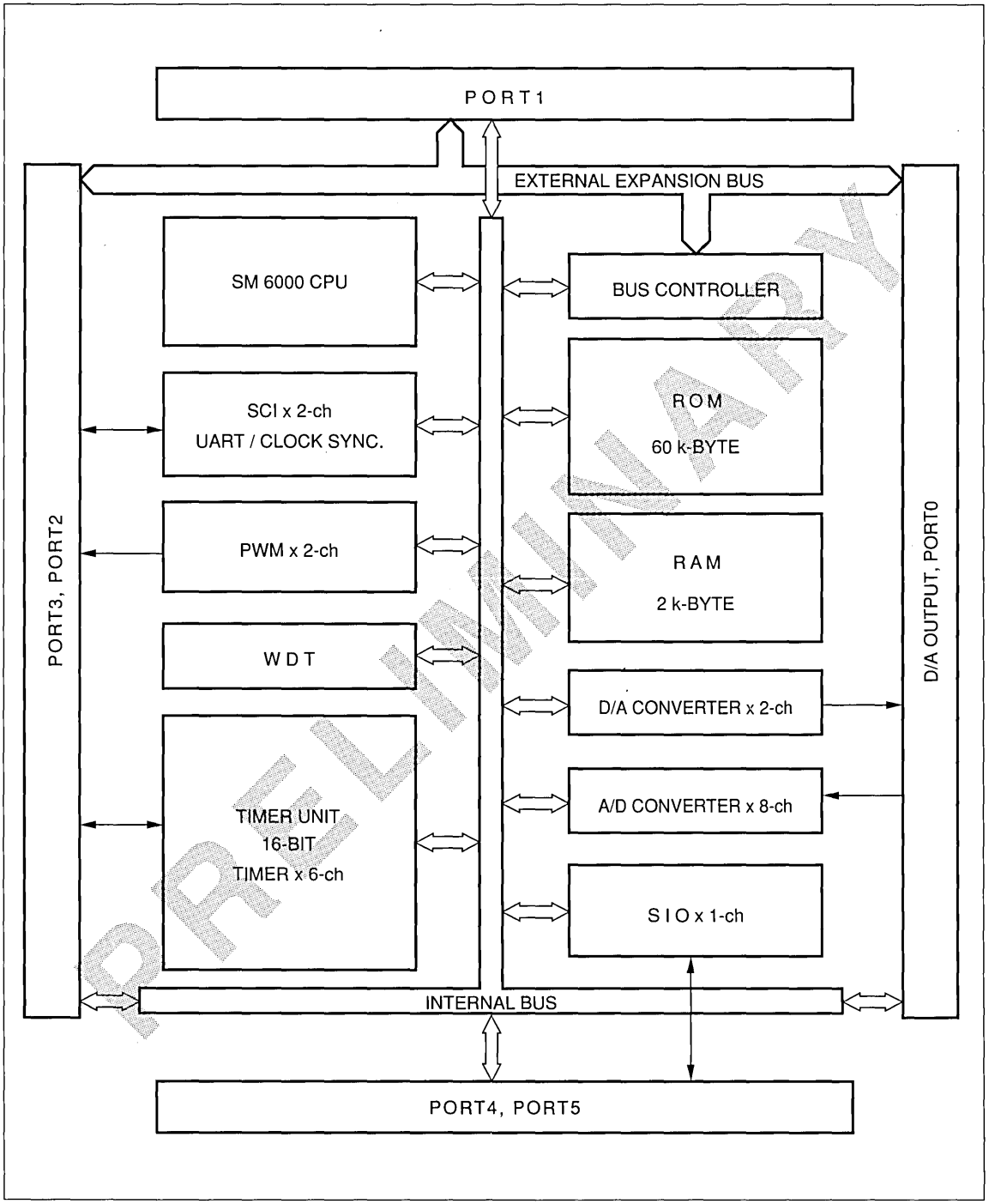
PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$ / EAD0 / EADB0	I/O	I/O port / address output (EAD0) / address · data I/O (EADB0)
$P0_1$ / EAD1 / EADB1	I/O	I/O port / address output (EAD1) / address · data I/O (EADB1)
$P0_2$ / EAD2 / EADB2	I/O	I/O port / address output (EAD2) / address · data I/O (EADB2)
$P0_3$ / EAD3 / EADB3	I/O	I/O port / address output (EAD3) / address · data I/O (EADB3)
$P0_4$ / EAD4 / EADB4	I/O	I/O port / address output (EAD4) / address · data I/O (EADB4)
$P0_5$ / EAD5 / EADB5	I/O	I/O port / address output (EAD5) / address · data I/O (EADB5)
$P0_6$ / EAD6 / EADB6	I/O	I/O port / address output (EAD6) / address · data I/O (EADB6)
$P0_7$ / EAD7 / EADB7	I/O	I/O port / address output (EAD7) / address · data I/O (EADB7)
$P0_8$ / EAD8 / EADB8	I/O	I/O port / address output (EAD8) / address · data I/O (EADB8)
$P0_9$ / EAD9 / EADB9	I/O	I/O port / address output (EAD9) / address · data I/O (EADB9)
$P0_{10}$ / EAD10 / EADB10	I/O	I/O port / address output (EAD10) / address · data I/O (EADB10)
$P0_{11}$ / EAD11 / EADB11	I/O	I/O port / address output (EAD11) / address · data I/O (EADB11)
$P0_{12}$ / EAD12 / EADB12	I/O	I/O port / address output (EAD12) / address · data I/O (EADB12)
$P0_{13}$ / EAD13 / EADB13	I/O	I/O port / address output (EAD13) / address · data I/O (EADB13)
$P0_{14}$ / EAD14 / EADB14	I/O	I/O port / address output (EAD14) / address · data I/O (EADB14)
$P0_{15}$ / EAD15 / EADB15	I/O	I/O port / address output (EAD15) / address · data I/O (EADB15)
$P1_0$ / EAD16	I/O	I/O port / address output (EAD16)
$P1_1$ / EAD17	I/O	I/O port / address output (EAD17)
$P1_2$ / EAD18	I/O	I/O port / address output (EAD18)
$P1_3$ / EAD19	I/O	I/O port / address output (EAD19)
$P1_4$ / EAD20	I/O	I/O port / address output (EAD20)
$P1_5$ / EAD21	I/O	I/O port / address output (EAD21)
$P1_6$ / EAD22	I/O	I/O port / address output (EAD22)
$P1_7$ / EAD23	I/O	I/O port / address output (EAD23)
$P1_8$ / EWRB	I/O	I/O port / write signal output (EWRB)
$P1_9$ / ERDB	I/O	I/O port / read signal output (ERDB)
$P1_{10}$ / EBYTEB	I/O	I/O port / byte signal output (EBYTEB)
$P1_{11}$ / ECK	I/O	I/O port / system clock 1 output (ECK)
$P1_{12}$ / EALE	I/O	I/O port / address latch signal output (EALE)
$P1_{13}$	I/O	I/O port
$P1_{14}$	I/O	I/O port
$P1_{15}$	I/O	I/O port
$P2_0$ / EDB0	I/O	I/O port / data I/O (EDB0)
$P2_1$ / EDB1	I/O	I/O port / data I/O (EDB1)
$P2_2$ / EDB2	I/O	I/O port / data I/O (EDB2)
$P2_3$ / EDB3	I/O	I/O port / data I/O (EDB3)
$P2_4$ / EDB4	I/O	I/O port / data I/O (EDB4)
$P2_5$ / EDB5	I/O	I/O port / data I/O (EDB5)
$P2_6$ / EDB6	I/O	I/O port / data I/O (EDB6)
$P2_7$ / EDB7	I/O	I/O port / data I/O (EDB7)

PIN NAME	I/O	FUNCTION
$P2_8$ / EDB8	I/O	I/O port/data I/O (EDB8)
$P2_9$ / EDB9	I/O	I/O port/data I/O (EDB9)
$P2_{10}$ / EDB10	I/O	I/O port/data I/O (EDB10)
$P2_{11}$ / EDB11	I/O	I/O port/data I/O (EDB11)
$P2_{12}$ / EDB12	I/O	I/O port/data I/O (EDB12)
$P2_{13}$ / EDB13	I/O	I/O port/data I/O (EDB13)
$P2_{14}$ / EDB14	I/O	I/O port/data I/O (EDB14)
$P2_{15}$ / EDB15	I/O	I/O port/data I/O (EDB15)
$P3_0$ / TxD0	I/O	I/O port/SCI0 transmit data output
$P3_1$ / RxD0	I/O	I/O port/SCI0 receive data input
$P3_2$ / SCK0	I/O	I/O port/SCI0 clock I/O
$P3_3$ / TxD1	I/O	I/O port/SCI1 transmit data output
$P3_4$ / RxD1	I/O	I/O port/SCI1 receive data input
$P3_5$ / SCK1	I/O	I/O port/SCI1 clock I/O
$P3_6$ / T5PWM	I/O	I/O port / Timer 5 PWM output
$P3_7$ / PWM0	I/O	I/O port/PWM0 output
$P3_8$ / PWM1	I/O	I/O port/PWM1 output
$P3_9$ / T0C0	I/O	I/O port/ Timer 0 capture input 0
$P3_{10}$ / T0C1	I/O	I/O port/ Timer 0 capture input 1
$P3_{11}$ / T0C2	I/O	I/O port/ Timer 0 capture input 2
$P3_{12}$ / T0C3	I/O	I/O port/ Timer 0 capture input 3
$P3_{13}$ / T0C4	I/O	I/O port/ Timer 0 capture input 4
$P3_{14}$ / T0O0	I/O	I/O port/ Timer 0 output compare output 0
$P3_{15}$ / T0O1	I/O	I/O port/ Timer 0 output compare output 1
$P4_0$ / T1C0 / T1E	I/O	I/O port/ Timer 1 capture input 0 / Timer 1 clock
$P4_1$ / T1O / T1C1	I/O	I/O port/ Timer 1 output compare output / Timer 1 capture input 1
$P4_2$ / T2C0 / T2E	I/O	I/O port/ Timer 2 capture input 0 / Timer 2 clock
$P4_3$ / T2O / T2C1	I/O	I/O port/ Timer 2 output compare output / Timer 2 capture input 1
$P4_4$ / RTO00	I/O	I/O port / real time output 00
$P4_5$ / RTO01	I/O	I/O port / real time output 01
$P4_6$ / RTO02	I/O	I/O port / real time output 02
$P4_7$ / RTO03	I/O	I/O port / real time output 03
$P4_8$ / RTO10	I/O	I/O port / real time output 10
$P4_9$ / RTO11 / SI	I/O	I/O port / real time output 11 / SIO receive data input
$P4_{10}$ / RTO12 / SO	I/O	I/O port / real time output 12 / SIO transmit data output
$P4_{11}$ / RTO13 / SCK	I/O	I/O port / real time output 13 / SIO clock I/O
$P4_{12}$ / INT0	I/O	I/O port / external interrupt 0
$P4_{13}$ / INT1	I/O	I/O port / external interrupt 1
$P4_{14}$ / INT2	I/O	I/O port / external interrupt 2
$P4_{15}$ / INT3	I/O	I/O port / external interrupt 3

PIN NAME	I/O	FUNCTION
$P5_0$ / AIN_0	I	I/O port / analog input 0
$P5_1$ / AIN_1	I	I/O port / analog input 1
$P5_2$ / AIN_2	I	I/O port / analog input 2
$P5_3$ / AIN_3	I	I/O port / analog input 3
$P5_4$ / AIN_4	I	I/O port / analog input 4
$P5_5$ / AIN_5	I	I/O port / analog input 5
$P5_6$ / AIN_6	I	I/O port / analog input 6
$P5_7$ / AIN_7	I	I/O port / analog input 7
ADVR	I	A/D converter reference voltage input
DA_0	O	D/A converter output 0
DA_1	O	D/A converter output 1
DAVR	I	D/A converter reference voltage input
AGND	I	A/D, D/A converter referense voltage (GND level)
$\overline{RESET}$	I	Reset input
TEST	I	Test input : connected to GND
MBUS	I	Bus mode select input
X_1, X_2		For clock oscillation
V_{DD}	I	Power supply
GND	I	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.3 to 6.5	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Max. output current	I_{OH}	All output pins but DA_0, DA_1	−4	mA
	I_{OL1}	$P3_0$, $P3_3$, $P4_{11}$	6	mA
	I_{OL2}	All output pins but $P3_0$, $P3_3$, $P4_{11}$, DA_0, DA_1	4	mA
Total output current	ΣI_{OH}	All output pins but DA_0, DA_1	−40	mA
	ΣI_{OL1}	$P3_0$, $P3_3$, $P4_{11}$	12	mA
	ΣI_{OL2}	All output pins but $P3_0$, $P3_3$, $P4_{11}$, DA_0, DA_1	40	mA
Operating temperature	T_{OPR}		−20 to +70	°C
Storage temperature	T_{STG}		−50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT	NOTE
Supply voltage	V_{DD}		2.5 to 5.5	V	
A/D supply voltage	ADVR		2.5 to V_{DD}	V	
D/A supply voltage	DAVR		2.5 to V_{DD}	V	
Analog GND potential	AGND		GND	V	
Minimum instruction cycle	Tsys	V_{DD} = 4.5 to 5.5 V	133	ns	
		V_{DD} = 2.5 to 5.5 V	200	ns	
Maximum system clock frequency	Fsmax	V_{DD} = 4.5 to 5.5 V	15	MHz	1
		V_{DD} = 2.5 to 5.5 V	10	MHz	1
Maximum main clock frequency	Fmax	V_{DD} = 4.5 to 5.5 V	30	MHz	
		V_{DD} = 2.5 to 5.5 V	20	MHz	
Operating temperature	T_{OPR}		−20 to +70	°C	

NOTE :

1. When system clock is divided-by-2 main clock.

DC CHARACTERISTICS

(V_{DD} = 2.5 to 3.3 V, Ta = –20 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage		V_{IH1}		0.7 x V_{DD}		V_{DD}	V	1
		V_{IL1}		0		0.3 x V_{DD}		
Input current		I_{H1}	V_{IN} = V_{DD}, V_{DD} = 3 V			10	µA	2
		I_{L1}	V_{IN} = 0 V, V_{DD} = 3 V			–10		
Output voltage		V_{OH1}	I_{OH} = –1 mA, V_{DD} = 3 V	V_{DD}–0.5			V	3
		V_{OL1}	I_{OL} = 1 mA, V_{DD} = 3 V			0.5		4
		V_{OL2}	I_{OL} = 2 mA, V_{DD} = 3 V			0.5		5
A/D converter	Resolution		ADVR = V_{DD} = 3 V		10		bits	
	Differential linear error				± 2	± 4	LSB	
	Linear error				± 4	± 6		
	Total error				± 5	± 8		
D/A converter	Resolution				8		bits	
	Output resistance		At resistance output		6		kΩ	6
	Total error				± 0.03	± 0.06	V	
Supply current		I_{DD}			25	50	mA	7
		I_{STOP}			1	10	µA	8

NOTES :

1. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
2. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
3. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
4. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_1$, $P3_2$, $P3_4$-$P3_{15}$, $P4_0$-$P4_{10}$, $P4_{12}$-$P4_{15}$, $\overline{RESET}$.
5. Applicable pins : $P3_0$, $P3_3$, $P4_{11}$.
6. At R-2R resistance output.
7. No-load condition, V_{DD} = 3 V, main clock 20 MHz.
8. No-load condition, V_{DD} = 3 V, ADVR = DRVR = AGND = GND, fixed input signal.

(V_{DD} = 4.5 to 5.5 V, Ta = –20 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage		V_{IH1}		0.7 x V_{DD}		V_{DD}	V	1
		V_{IL1}		0		0.3 x V_{DD}		1
Input current		I_{H1}	V_{IN} = V_{DD}, V_{DD} = 5 V			10	μA	2
		I_{L1}	V_{IN} = 0 V, V_{DD} = 5 V			–10		2
Output voltage		V_{OH1}	I_{OH} = –2 mA, V_{DD} = 5 V	V_{DD}–0.5			V	3
		V_{OL1}	I_{OL} = 2 mA, V_{DD} = 5 V			0.5		4
		V_{OL2}	I_{OL} = 4 mA, V_{DD} = 5 V			0.5		5
A/D converter	Resolution		ADVR = V_{DD} = 5 V		10		bits	
	Differential linear error				± 1	± 2.5	LSB	
	Linear error				± 3	± 5	LSB	
	Total error				± 4	± 6	LSB	
D/A converter	Resolution		DAVR = V_{DD} = 5 V (at AMP output)		8		bits	
	Output voltage range			0.8		V_{DD}–0.8	V	6
	Total error				± 0.05	± 0.10	V	
	Output resistance		At resistance output		6		kΩ	7
	Total error				± 0.05	± 0.10	V	
Supply current		I_{DD}			65	130	mA	8
		I_{STOP}			1	20	μA	9

NOTES :

1. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
2. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
3. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_0$-$P3_{15}$, $P4_0$-$P4_{15}$, $\overline{RESET}$.
4. Applicable pins : $P0_0$-$P0_{15}$, $P1_0$-$P1_{15}$, $P2_0$-$P2_{15}$, $P3_1$, $P3_2$, $P3_4$-$P3_{15}$, $P4_0$-$P4_{10}$, $P4_{12}$-$P4_{15}$, $\overline{RESET}$.
5. Applicable pins : $P3_0$, $P3_3$, $P4_{11}$
6. At AMP output
7. At R-2R resistance output
8. No-load condition, V_{DD} = 5 V, main clock 30 MHz.
9. No-load condition, V_{DD} = 5 V, ADVR = DRVR = AGND = GND, fixed input signal.

8-BIT SINGLE-CHIP MICROCOMPUTERS

SM8502★/SM8503★/ SM8504/SM8505★/ SM8506

8-Bit Single-Chip Microcomputer (Controllers For General Purpose)

★ Under development

DESCRIPTION

SM8500 series is a 1-chip microcomputer containing SM85CPU core and the required peripheral functions for system. SM85CPU is an 8-bit high performance CPU with various addressing modes and high-efficiency instructions set. SM85CPU is featured by allocating general registers on RAM to reduce overhead when calling subroutines.

The peripheral functions and memory of SM8500 series contain ROM, RAM, timer/event counter, serial interfaces (SIO, UART), A/D converter, and D/A converter and waveform generator.

The SM8500 series are offered by a variety of models with different capacity of memory. These are SM8502, SM8503, SM8504, SM8505, and SM8506.

FEATURES

- ROM capacity : 24 576 x 8 bits (SM8502)*
  32 768 x 8 bits (SM8503)*
  40 960 x 8 bits (SM8504)
  49 152 x 8 bits (SM8505)*
  61 440 x 8 bits (SM8506)
- RAM capacity : 1 024 x 8 bits (SM8502*/SM8503*/SM8504)
  2 048 x 8 bits (SM8505*/SM8506)
- A RAM area is used as subroutine stack
- I/O ports :

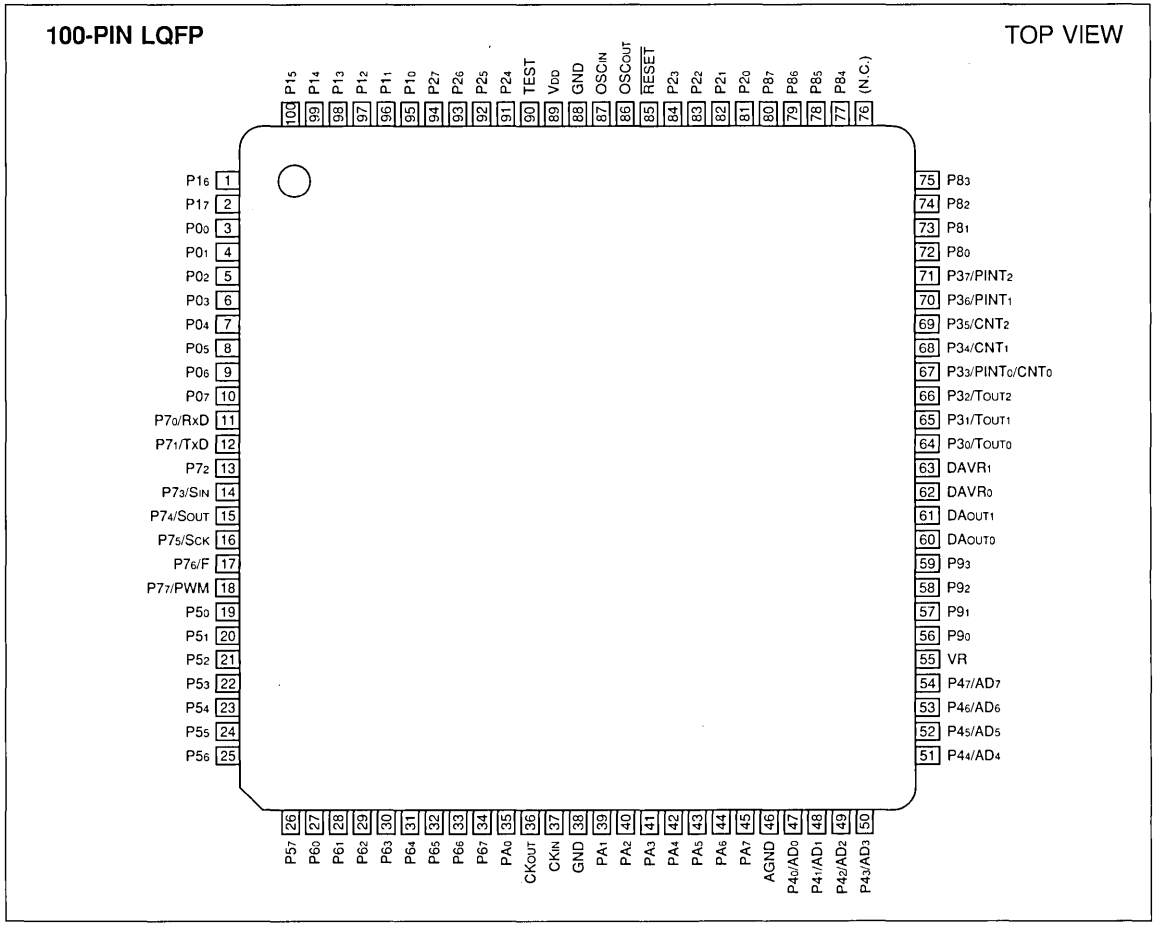
Input	16 (8 inputs also used as A/D input pins)
Output	16
Input / Output	52
D/A output	2

- Interrupts :
  Non-maskable interrupts x 2
  (watch dog timer / illegal instruction trap)
  Maskable interrupts x 14
  (internal interrupts x 10 / external interrupts x 4)
- A/D converter :
  Resolution 8 bits
  Channel 8 channels
- D/A converter :
  Resolution 8 bits
  (4 bits for waveform generator)
  Channel 2 channels
- Waveform generator :
  Channel 2 channels
  16 level tone, 32 step / 1 period waveform output.
  Combined with external circuit, DTMF waveform can be output.
  ✻ Waveform generator can be used by combining with D/A converter.
- Timer/counter : 16 bits x 1, 8 bits x 5
  PWM output available
  Watch dog timer : 8 bits x 1
  Clock timer : 8 bits x 1
- Input capture function
- Clock output (also used as buzzer output)
- Serial interface :
  SIO 8 bits clock synchronous x 1
  UART 8 bits clock asynchronous x 1
- External memory expansion
- Memory configuration (SM8505/SM8506) :
  Setting of external memory accessing address range.

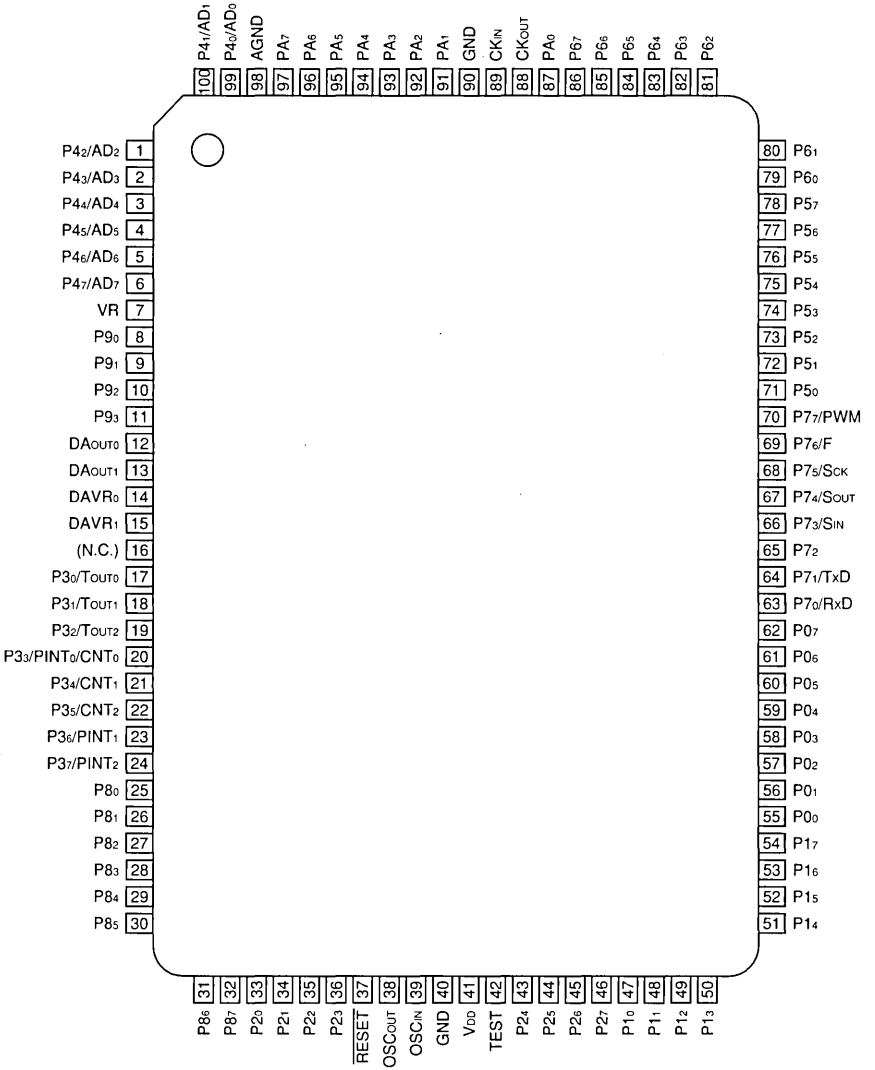
- CPU core :
  8 bits x 8 ports (or 16 bits x 4 ports) and 16 bits x 4 ports general purpose register are used as accumulator, register pointer, and register index.
  Instruction sets 67
  (multiplication / division / bit manipulation instruction)
  Addressing mode 23 types
  System clock cycle 0.17 µs (MIN.) at 12 MHz main clock cycle
  System clock is variable by software (system clock can be optioned to 1/2, 1/4, 1/8, 1/16, 1/32 of main-clock and 1/2 of sub-clock.)
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Standby modes : halt mode / stop mode
- Supply voltage :
  4.5 to 5.5 V ;
  system clock frequency 6 MHz(MAX.)
  2.7 to 3.6 V ;
  system clock frequency 3 MHz(MAX.)
  1.8 to 2.7 V ;
  system clock frequency 750 kHz(MAX.)
  ✻ The system clock frequency must be switched to above given ratings by program.
- Packages :
  100-pin LQFP (LQFP100-P-1414)
  100-pin QFP (QFP100-P-1420)

PIN CONNECTIONS

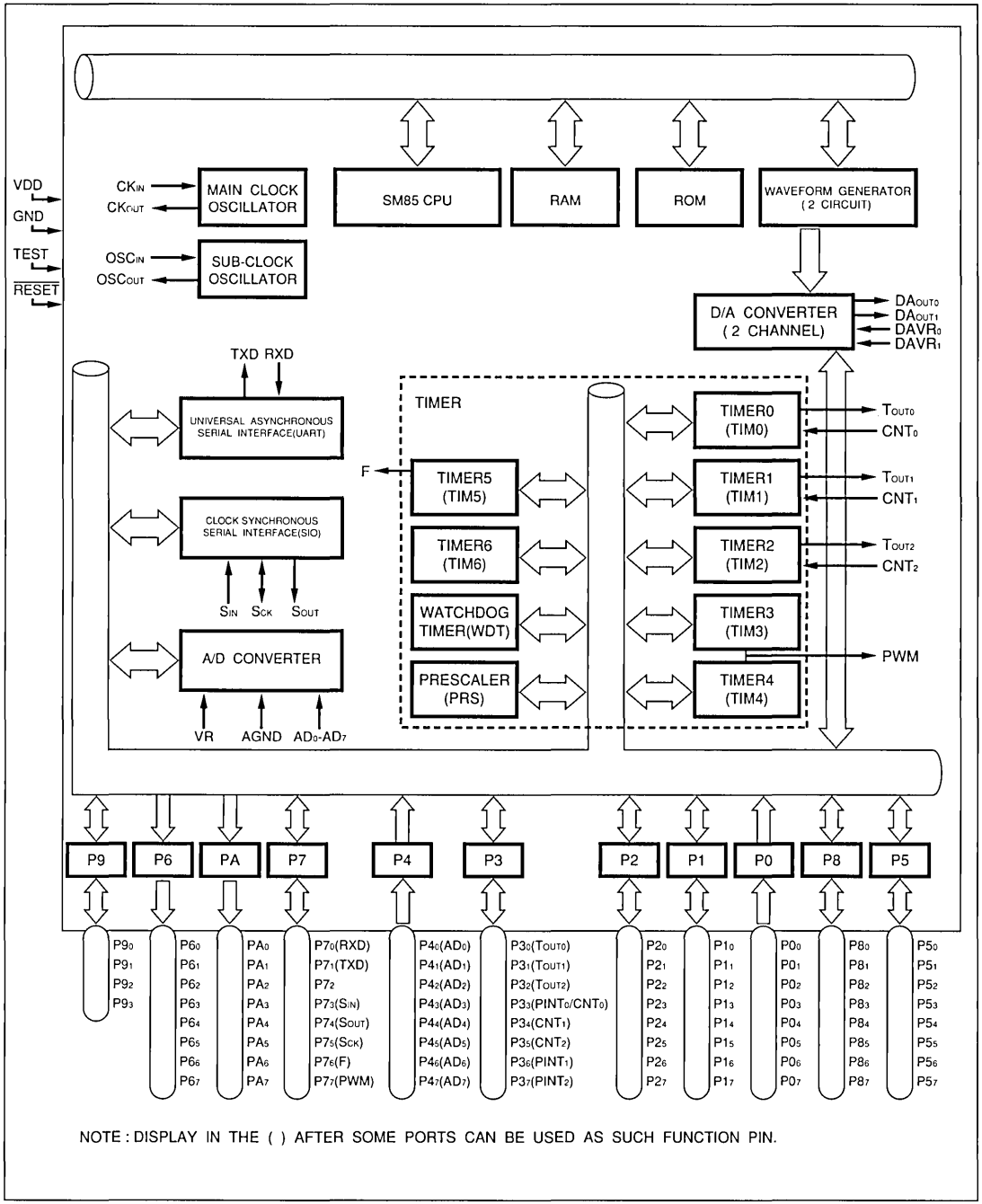
100-PIN LQFP TOP VIEW



100-PIN QFP TOP VIEW



BLOCK DIAGRAM



NOTE : DISPLAY IN THE ( ) AFTER SOME PORTS CAN BE USED AS SUCH FUNCTION PIN.

PIN DESCRIPTION

TYPE	PIN NAME	I/O	FUNCTION
Power supply	V_{DD}	Input	**Power supply** Applied to +1.8 V to 5.5 V
	GND	Input	**Ground** Applied to 0 V. Also serving as the D/A ground pin.
	VR	Input	**A/D converter reference voltage** Set it to V_{DD} level when not in use.
	$DAVR_0$	Input	**D/A converter low-level reference voltage** Set it to V_{DD} level when not in use.
	$DAVR_1$	Input	**D/A converter high-level reference voltage** Set it to V_{DD} level when not in use.
	AGND	Input	**Analog Ground** The ground pin for A/D converter. Applied to 0 V
Clock	CK_{IN}, CK_{OUT}	I/O	**Oscillator pin for main clock** Connecting crystal oscillator.
	OSC_{IN}, OSC_{OUT}	I/O	**Oscillator pin for subclock** Connecting 32.768 kHz crystal oscillator.
System	$\overline{RESET}$	Input	**External Reset** When setting pin to low level, the hardware reset will be initiated.
	TEST	Input	**Test** Don't be released for user, connect to GND.
Interrupt	$PINT_0$, $PINT_1$, $PINT_2$	Input	**External interrupt $PINT_0$-$PINT_2$** These are external interrupt input pins and sharing with the $P3_3$, $P3_6$ and $P3_7$. $PINT_0$ pin is able to detect for falling edge, rising edge and the both edge. PINT1, PINT2 pins are low level and able to detect for falling edge, rising edge and the both edge.
	$P0_0$-$P0_7$	Input	**External interrupt $P0_0$-$P0_7$** Pins of Port 0 can be used in an interrupt by falling edge.

TYPE	PIN NUMBER	I/O	FUNCTION
Port	$P0_0$-$P0_7$	Input	**Port 0** An 8 bit input port. By port pull-up setting register (PPC), the pull-up resistance of the port can be set to ON/OFF in 8 bit unit.
	$P1_0$-$P1_7$	I/O	**Port 1** An 8 bit I/O port. The port can be set as I/O port by P1 control register (P1C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 1 bit unit by P1 pull-up setting register (P1PC) .
	$P2_0$-$P2_7$	I/O	**Port 2** An 8 bit I/O port. The port can be set as I/O port by P2 control register (P2C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 1bit unit by P2 pull-up setting register (P2PC) .
	$P3_0$-$P3_7$	I/O	**Port 3** An 8 bit I/O port. The port can be set as I/O port by P3 control register (P3C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 8bit unit by port pull-up setting register (PPC) .
	$P4_0$-$P4_7$	Input	**Port 4** An 8 bit input port.
	$P5_0$-$P5_7$	I/O	**Port 5** An 8 bit I/O port. The port can be set as I/O port by P5 control register (P5C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 8 bit unit by port pull-up setting register (PPC) .
	$P6_0$-$P6_7$	Output	**Port 6** An 8 bit output port with large current (10mA) [the total output (sink) current of $Port_6$ and $Port_A$ are 100mA] . By mask option, the port can be configured as a N-ch open drain pin.
	$P7_0$-$P7_3$	I/O	**Port 7** An 8 bit I/O port. The port can be set as I/O port by P7 control register (P7C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 8 bit unit by port pull-up setting register (PPC) .
	$P8_0$-$P8_7$	I/O	**Port 8** An 8 bit I/O port. The port can be set as I/O port by P8 control register (P8C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 8 bit unit by port pull-up setting register (PPC) .

TYPE	PIN NUMBER	I/O	FUNCTION
Port	$P9_0$-$P9_3$	I/O	**Port 9** An 8 bit I/O port. The port can be set as I/O port by P9 control register (P9C) in 1 bit unit. For input mode, the pull-up resistance can be set to ON/OFF in 4bit unit by port pull-up setting register (PPC) .
	PA_0-PA_7	Output	**Port A** An 8 bit output port with large current (10mA) [the total output (sink) current of Port6 and PortA are 100mA]. By mask option, the port can be configured as a N-ch open drain pin.
Timer	$TOUT_0$, $TOUT_1$, $TOUT_2$	Output	**Timer output 0 to 2** These are output pin for timer/counter 0 to 2. Each pin is shared with pin $P3_0$, $P3_1$ and $P3_2$, respectively. ($P3_0/TOUT_0$, $P3_1/TOUT_1$, $P3_2/TOUT_2$)
	CNT_0, CNT_1, CNT_2	Input	**Timer event count input 0 to 2** These are output pin for timer/counter 0 to 2. Each pin is shared with pin $P3_3$,$P3_4$ and $P3_5$, respectively. ($P3_3/PINT_0/CNT_0$, $P3_4/PINT_1/CNT_1$, $P3_5/PINT_2/CNT_2$) CNT_0 can also be used as a capture trigger input of timer/counter 0.
	$PINT_0$, $PINT_1$, $PINT_2$	Input	**External interrupt input 0 to 2** Each pin is shared with pin $P3_3$, $P3_6$ and $P3_7$. ($P3_3/PINT_0/CNT_0$, $P3_6/PINT_1$, $P3_7/PINT_2$)
	PWM	Output	**PWM output** This is PWM output pin of timer/counter 3 to 4 and shared with pin $P7_7$ ($P7_7$ /PWM).
	F	Output	**Clock (buzzer) output** This is clock output pin for the buzzer of timer/counter 5 and shared with pin $P7_6$ ($P7_6$ /F).
SIO	SIN	Input	**SIO data input** This is an input pin for SIO data and shared with pin $P7_3$ ($P7_3/SIN$).
	$SOUT$	Output	**SIO data output** This is an output pin for SIO data and shared with pin $P7_4$ ($P7_4/SOUT$)
	SCK	I/O	**SIO transfer clock I/O** This is an I/O pin for SIO data and shared with pin $P7_5$ ($P7_5/SCK$).
UART	RxD	Input	**UART data input** This is an input pin for UART data and shared with pin $P7_0$ ($P7_0$/RxD).
	TxD	Output	**UART data output** This is an output pin for UART data and shared with pin $P7_1$ ($P7_1$/TxD).

TYPE	PIN NUMBER	I/O	FUNCTION
A/D converter	AD_0-AD_7	Input	**Analogue input 0 to 7** These are an analogue input pin for A/D and shared with pin $P4_0$-$P4_7$ ($P4_0$/AD_0-$P4_7$/AD_7) respectively.
D/A converter	DA_{OUT0}, DA_{OUT1}	Output	**D/A converter output 0,1** These are output pins for D/A (2 channel).
External memory expansion	A_0-A_7	Output	**Address bus (lower bit)** In external memory expansion mode, $P5_0$-$P5_7$ pins will be address bus. It will output the lower 8bit address, while accessing the external memory expansion area*.
	A_8-A_{15}	Output	**Address bus (upper bit)** In external memory expansion mode, $P2_0$-$P2_7$ pins will be address bus. It will output the upper 8bit address while accessing the external memory expansion area*.
	DB_0-DB_7	I/O	**Data bus** In external expansion mode, $P1_0$-$P1_7$ pins will be data bus.
	$\overline{RD}$	Output	**Read** In external memory expansion mode, $P0_0$ pin will be $\overline{RD}$ pin. This pin will be low level when reading external memory.
	$\overline{WR}$	Output	**Write** In external memory expansion mode, P01 pin will be $\overline{WR}$ pin. This pin will be low level when writing external memory.

* External memory expansion area depends on models. For more details, please refer to [Memory map] .

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	CONDITION	RATING	UNIT
Power supply voltage		V_{DD}		−0.3 to 6.5	V
Input voltage		V_I		−0.3 to V_{DD} + 0.3	V
Output voltage		V_O		−0.3 to V_{DD} + 0.3	V
Maximum output current	High level	I_{OH}	All output pins	−4	mA
	Low level	I_{OL1}	$P6_0$-$P6_7$, PA_0-PA_7	+30	mA
	Low level	I_{OL2}	All output pins except $P6_0$-$P6_7$, PA_0-PA_7	+4	mA
Tatal output current	High level	Σ_{OH}	All output pins	−20	mA
	Low level	Σ_{OL1}	$P6_0$-$P6_7$, PA_0-PA_7	+100	mA
	Low level	Σ_{OL2}	All output pins except $P6_0$-$P6_7$, PA_0-PA_7	+20	mA
Operating temperature		T_{OPR}		−20 to 70	°C
Store temperature		T_{STG}		−50 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT	NOTE
Power supply voltage	V_{DD}		1.8 to 5.5	V	
A/D voltage	VR		1.8 to +V_{DD}	V	
D/A voltage	DAVR		1.8 to +V_{DD}	V	
System clock cycle	t_{SYS}	V_{DD} = 4.5 to 5.5 V	0.17 to 61	µs	
		V_{DD} = 2.7 to 4.5 V	0.33 to 61	µs	
		V_{DD} = 1.8 to 2.7 V	1.33 to 61	µs	
System clock frequency	f_{SYS}	V_{DD} = 4.5 to 5.5 V	16.384 k to 6.0 M	Hz	
		V_{DD} = 2.7 to 4.5 V	16.384 k to 3.0 M	Hz	
		V_{DD} = 1.8 to 2.7 V	16.384 k to 750 k	Hz	
Maximum main clock frequency	f_{MAIN} (f_{CK})	V_{DD} = 4.5 to 5.5 V	12.0	MHz	
		V_{DD} = 2.7 to 4.5 V	6.0	MHz	1
		V_{DD} = 1.8 to 2.7 V	1.5	MHz	1
Subclock frequency	f_{SUB}	V_{DD} = 1.8 to 5.5 V	32.768	kHz	
Operating temperature	t_{OPR}		−20 to +70	°C	

NOTE :

System clock is the rating value when set to maximum speed (1/2 of main-clock). Actually, 12 MHz main clock can be used in power supply voltage range (1.8 to 5.5 V). Under this case, however, corresponding to the operating voltage, the system clock frequency must be set in above given ratings. The setting can be done by program.

DC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V, Ta = –20 to +70°C)

PARAMETER		SYMBOL	CONDITION	RATINGS			UNIT	NOTE
				MIN.	TYP.	MAX.		
Input voltage		V_{IH1}		0.8 x V_{DD}		V_{DD}	V	1
		V_{IL1}		0		0.2 x V_{DD}		
		V_{IH2}		V_{DD} – 0.3		V_{DD}	V	2
		V_{IL2}		0		0.3		
Input current		I_{IH1}	V_{IN} = V_{DD}, V_{DD} = 5 V			10	µA	3
		I_{IL1}	V_{IH} = 0 V, V_{DD} = 5 V			–10	µA	3
		I_{IL2}	V_{IN} = 0 V, V_{DD} = 5 V	–40	–75	–150	µA	4
Output current		V_{OH1}	I_{OH} = –1 mA, V_{DD} = 5 V	V_{DD} – 0.5			V	5
		V_{OL1}	I_{OL} = 10 mA, V_{DD} = 5 V			2		
		V_{OH2}	I_{OH} = –1 mA, V_{DD}= 5 V	V_{DD} – 0.5			V	6
		V_{OL2}	I_{OL} = 1 mA, V_{DD} = 5 V			0.5		
A/D	resolution		VR = V_{DD} = 5 V, f_{MAIN} = 12 MHz		10		bits	
	differential linear tolerance		VR = V_{DD} = 5 V, f_{MAIN} = 12 MHz		± 1	± 2.5	LSB	
	linear tolerance		VR = V_{DD} = 5 V, f_{MAIN} = 12 MHz		± 3	± 5	LSB	
	combined tolerance		VR = V_{DD} = 5 V, f_{MAIN} = 12 MHz		± 4	± 6	LSB	
D/A	resolution		DAVR = V_{DD} = 5 V		8		bits	8
	output resistance		DAVR = V_{DD} = 5 V			6	kΩ	
	combined tolerance		DAVR = V_{DD} = 5 V		± 0.05	± 0.10	V	
Supply current		I_{DD}	f_{SYS} = 6 MHz		10	20	mA	9
		I_{DDH}	f_{SYS} = 6 MHz, HALT mode		3	6		
		I_{DDS1}	f_{SUB} oscillate, STOP mode		30	60	µA	10
		I_{DDS2}	f_{SUB} stop, STOP mode		1	10	µA	11

NOTES :

1. Applicable pins : $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_2$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_1$, $P7_2$, $P7_4$, $P7_6$, $P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$, CK_{IN}
2. Applicable pins : $\overline{RESET}$, OSC_{IN}, $P0_0$-$P0_7$, $P3_3$-$P3_7$, $P7_0$, $P7_3$, $P7_5$
3. Applicable pins : (separated pull-up resistant status) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$
4. Applicable pins : $\overline{RESET}$ (connected pull-up resistant status) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$
5. Applicable pins : $P6_0$-$P6_7$, PA_0-PA_7
6. Applicable pins : $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$. $P0_0$ ($\overline{RD}$), $P0_1$ ($\overline{WR}$) (During external memory expansion mode)
7. Applicable pins : DA_{OUT0}, DA_{OUT1}
8. No load condition, V_{DD} = 5 V, main-clock frequency = 12 MHz
9. No load condition, V_{DD} = 5 V, f_{SYS} oscillating status (32.768 kHz), VR = GND, input signal fixed.
10. No load condition, V_{DD} = 5 V, OSC_{IN} = GND, VR = GND, input signal fixed.

(V_{DD} = 2.7 to 3.3 V, Ta = –20 to +70°C)

PARAMETER		SYMBOL	CONDITION	RATINGS			UNIT	NOTE
				MIN.	TYP.	MAX.		
Input voltage		V_{IH1}		0.8 x V_{DD}		V_{DD}	V	1
		V_{IL1}		0		0.2 x V_{DD}		
		V_{IH2}		V_{DD} – 0.3		V_{DD}	V	2
		V_{IL2}		0		0.3		
Input current		I_{IH1}	V_{IN} = V_{DD}, V_{DD} = 3 V			10	µA	3
		I_{IL1}	V_{IH} = 0 V, V_{DD} = 3 V			–10	µA	3
		I_{IL2}	V_{IN} = 0 V, V_{DD} = 3 V	–10	–25	–50	µA	4
Output current		V_{OH1}	I_{OH} = –1 mA, V_{DD} = 3 V	V_{DD} – 0.5			V	5
		V_{OL1}	I_{OL} = 10 mA, V_{DD} = 3 V			1		
		V_{OH2}	I_{OH} = –1 mA, V_{DD}= 3 V	V_{DD} – 0.5			V	6
		V_{OL2}	I_{OL} = 1 mA, V_{DD} = 3 V			0.5		
A/D	resolution		VR = V_{DD} = 3 V, f_{MAIN} = 6 MHz		10		bits	
	differential linear tolerance		VR = V_{DD} = 3 V, f_{MAIN} = 6 MHz		± 1	± 2.5	LSB	
	linear tolerance		VR = V_{DD} = 3 V, f_{MAIN} = 6 MHz		± 3	± 5	LSB	
	combined tolerance		VR = V_{DD} = 3 V, f_{MAIN} = 6 MHz		± 4	± 6	LSB	
D/A	resolution		DAVR = V_{DD} = 3 V		8		bits	7
	output resistance					6	kΩ	
	combined tolerance				± 0.03	± 0.06	V	
Supply current		I_{DD}	f_{SYS} = 3 MHz		4	8	mA	8
		I_{DDH}	f_{SYS} = 3 MHz, HALT mode		1	2		
		I_{DDS1}	f_{SUB} oscillate, STOP mode		20	40	µA	9
		I_{DDS2}	f_{SUB} stop, STOP mode		1	6	µA	10

NOTES :

1. Applicable pins : $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_2$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_1$, $P7_2$, $P7_4$, $P7_6$, $P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$, CK_{IN}
2. Applicable pins : $\overline{RESET}$, OSC_{IN}, $P0_0$-$P0_7$, $P3_3$-$P3_7$, P70, $P7_3$, $P7_5$
3. Applicable pins : (separated pull-up resistant status) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$
4. Applicable pins : $\overline{RESET}$ (connected pull-up resistant status) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$
5. Applicable pins : $P6_0$-$P6_7$, PA_0-PA_7
6. Applicable pins : $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$ $P0_0$ ($\overline{RD}$), $P0_1$ ($\overline{WR}$) (During external memory expansion mode)
7. Applicable pins : DA_{OUT0}, DA_{OUT1}
8. No load condition, V_{DD} = 3 V, main-clock frequency = 6 MHz
9. No load condition, V_{DD} = 3 V, f_{SUB} oscillating sataus (32.768 kHz), VR = GND, input signal fixed.
10. No load condition, V_{DD} = 3 V, OSC_{IN} = GND, VR = GND, input signal fixed.

SM85CPU

The SM85 CPU is an 8-bit CPU with an unique architecture, developed by SHARP, and the following features.

General purpose register architectures

- There are eight 8-bit general purpose registers (also serve as four 16-bit general purpose registers) and four 16-bit general purpose registers serve as accumulator, index register, or the pointer registers.

General purpose register allocated at RAM

- The general purpose register access the RAM location by the register pointer RP. So pushing the register during an interrupt and passing parameter to subroutine can be executed in high speed.

Refined instruction set

- The instruction set contains total 68 members : 8 load instructions, 19 arithmetic instructions, 7 logic instructions program control (branch) instruction, 8 bit manipulation instructions, 8 rotate & shift instructions and 9 CPU control instructions.
- There are powerful bit manipulation instructions includes plural bits transfer, logical operation between bits, and the bit test and jump instructions that incorporates a test and condition branch in the same instruction. (Ref. to Table 1)
- There are data transfer, arithmetic and conditional branch instructions for 16 bit. It can rapidly process the word-sized and long jump.
- There are 8-bit x 8-bit→16 bit multiplication and 16 bit x 16 bit→16 bit remaining 8-bit division instructions. (Unsigned arithmetic)

23 address modes

- The rich address modes provides optimal access to ROM, RAM and the register files.

Illegal instruction detecting function

- When an error code is detected, a non-maskable interrupt (NMI) will be generated.

Standby function

- There are two standby modes, HALT and STOP mode, and the mode can be change by HALT instruction or STOP instruction, respectively.

Table 1 Instruction summary

TYPE	INSTRUCTION	NUMBER
Load instruction	CLR, MOV, MOVM, MOVW, POP, POPW, PUSH, PUSHW	8
Arithmetic instruction	ADC, ADCW, ADD, ADDW, CMP, CMPW, DA, DEC, DECW, DIV, EXTS, INC, INCW, MULT, NEG, SBC, SBCW, SUB, SUBW	19
Logic instruction	AND, ANDW, COM, OR, ORW, XOR, XORW	7
Program control instruction	BBC, BBS, BR, CALL, CALS, DBNZ, IRET, JMP, RET	9
Bit manipulation instruction	BAND, BCLR, BCMP, BMOV, BOR, BTST, BSET, BXOR	8
Rotate & shift instruction	RL, RLC, RR, RRC, SLL, SRA, SRL, SWAP	8
CPU control instruction	COMC, CLRC, DI, EI, HALT, NOP, SETC, STOP	8
		Total 67

Table 2 Addressing mode summary

TYPE	ADDRESSING MODE	SYMBOL	ACCESS TARGET
Register direct	Register	r	General purpose register R0, R1, R2...R7
	Register pair	rr	General purpose register RR0, RR2, RR4...RR14
Register indirect	Register indirect	@r	Memory (0000H-00FFH)
	Register indirect auto increment	(r)+	
	Register indirect auto decrement	-(r)	
	Register pair indirect	@rr	Memory (0000H-FFFFH)
	Register pair indirect increment	(rr)+	
	Register pair indirect decrement	-(rr)	
Index	Register index	n(r)	Memory (0000H-00FFH)
	Register pair index	nn(rr)	Memory (0000H-FFFFH)
Register file	Register file	R	Register file (0000H-007FH) and memory (0080H-00FFH)
	Register file pair	RR	
	Port	p	Register file (0010H-0017H)
Direct	Direct	DA	Memory (0000H-FFFFH)
	Direct short	DAs	Program memory (1000H-1FFFH)
	Direct special page	DAp	Memory (FF00H-FFFFH)
Memory indirect	Index indirect	@nn(r)	Memory (0000H-FFFFH)
	Direct indirect	@DA	
PC relative	Relative	RA	Program memory (PC-128 and PC+127)
Bit	Bit	b	Any bit in register file (0000H-007FH) and memory (0080H-00FFH, FF00H-FFFFH)
Immediate	Immediate	IM	Immediate data included in the operand
	Immediate long	IML	
Implied	Implied	–	Carry (C), interrupt mask (I), etc.

Register Lineup

Fig. 1 shows the SM85CPU register lineup. The CPU internal register consists of eight 8-bit general purpose registers (R0-R7), four 16bit general purpose registers (RR8-RR14), a program counter (PC) and four other control registers. (The R0-R7 can be also used as four 16-bit general purpose registers (RR8-RR14).)

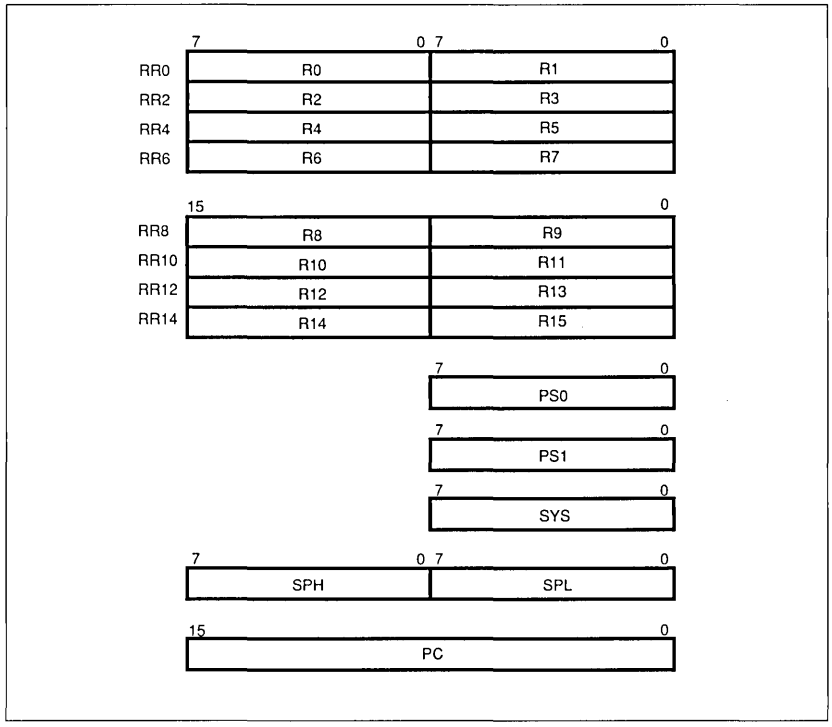


Fig. 1 Register lineup

GENERAL PURPOSE REGISTER

The eight 8-bit general purpose registers R0-R7 and all eight 16-bit general purpose registers (RR0-RR14) are available for use as accumulator, index register and pointer registers. (The R0 and RR0 cannot be used as index register)

The other eight 8-bit registers R8-R15 cannot be used as 8-bit general purpose register.

The feature of the SM8500CPU architecture is that general purpose registers are virtually allocated at 16-byte internal RAM. Actually, if the CPU accesses general purpose registers, the designated RAM will be accessed by the 8-bit register pointer (RP)*. When RP=00000B, the registers occupy the first 16 bytes starting at 0000H. Incrementing the field, RP = 00001B, shifts the mapping by eight bytes so that the registers start at 0008H. As a result, the general purpose registers can be switch in 8-byte unit to any RAM location within 0000H-00FFH.

Although the general purpose registers are members of the register file, which stores the data onto actual RAM, is different from the other members (control registers).

That is, general purpose registers can be referred as registers, as register file (allocated at 0000H-000FH) and as RAM accessing by all addressing modes.

* About register pointer (RP), please refer to [processor status (PS0)].

CPU CONTROL REGISTER

The SM8500CPU has the following control register : processor status PS0, processor status PS1, system configuration register SYS,stack pointer SPH, SPL and program counter PC. All control register except the program counter PC are members of the register file and accessible by the register file R and the register file pair RR addressing modes.

Processor status 0 (PS0)

The processor status PS0 is an 8-bit readable/ writable register containing 2 fields, the upper 8-bit is register pointer (RP) and the lower 8-bit is interrupt mask.

Bit 7 0

PR4	PR3	PR2	PR1	PR0	IM2	IM1	IM1

Bit 7-3 : Register pointer (RP)

This gives, in 8 bytes unit, the starting address in RAM for general purpose registers.

Bit 2-0 : Interrupt mask bit (IM)

BIT	CONTENT
000	All maskable interrupts recognized
001	
010	Maskable interrupts with level 1 to 12 recognized
011	Maskable interrupts with level 1 to 10 recognized
100	Maskable interrupts with level 1 to 8 recognized
101	Maskable interrupts with level 1 to 6 recognized
111	Maskable interrupts with level 1 tto 4 recognized
111	Maskable interrupts with level 1 to 2 recognized

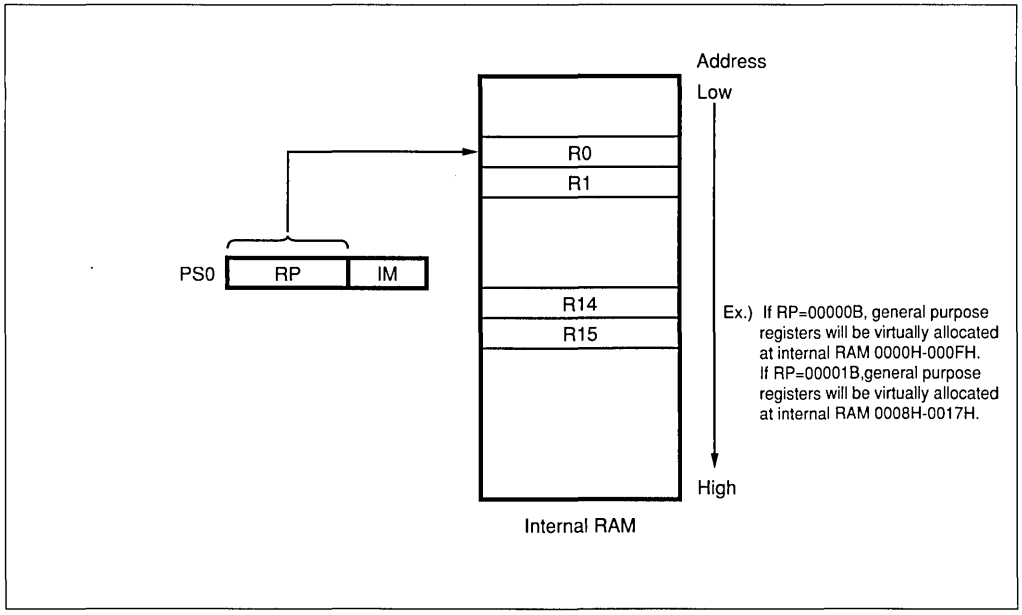


Fig. 2 Register pointer (RP) setting example

Processor status 1 (PS1)

The processor status PS1 is an 8-bit readable/ writable register and consists of eight flag bits. These flags can be use as the condition codes for the conditional branch instructions. When CPU generates an interrupt, the content of processor status PS1 and the value of program counter PC automatically are pushed onto stack.

Bit 7 0

C	Z	S	V	D	H	B	I

Bit 7 : Carry (C)

It indicates that generated a carry in operation.

Bit 6 : Zero (Z)

It indicates that the operation result is zero.

Bit 5 : Sign (S)

It indicates that the operation result is negative (Sign bit = [1]).

Bit 4 : Overflow (V)

Executes the operation with the signed value. If the operation result cannot indicate to '2' complete, then the bit will be '1'.

Bit 3 : Decimal adjustment (D)

It indicates that the last arithmetic operation was a subtract.

Bit 2 : Half carry (H)

It indicates that generated a carry between bit 3 and 4.

Bit 1 : Bit (B)

It indicates that the result of the last bit manipulation.

Bit 0 : Interrupt enable (I)

This is a flag which enables / disables all maskable interrupt.

System configuration register (SYS)

The system configuration register SYS is an 8-bit readable / writable register which sets the external memory expansion modes and selects 8-bit / 16-bit stack pointer.

Bit 7 0

-	SPC	-	AW	-	MCNF2	MCNF1	MCNF1

Bit 6 : Stack pointer configuration (SPC)

0	8 bit (SPLonly)
1	16 bit (both SPL, SPH)

Bit 4 : AW bit

Alougth this bit is readable / writable. It must clear '0'.

Bit 2-0 : Memory configuration (MCNF2-0)

BIT	CONTENT
000	External memory expansion disable.
011	External memory expansion (256 bytes, FF00H-FFFFH)
110	External memory expansion mode (64k bytes *)
Other combination	Do not use.

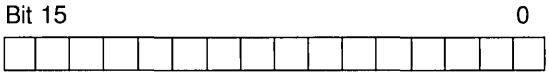
* : In ROM space (60k bytes), the field beyond the internal ROM is the external memory access field. For example, in SM8504, the external memory access field is B000H-FFFFH.

Stack pointer (SPL, SPH)

The stack pointer SPL, SPH are 8-bit readable/ writable register and show the stack address. The bit SPC of the system configuration (SYS) specifies whether the stack pointer is 8 (SPL only) or 16 (both SPL and SPH) bits long.

Program counter (PC)

The program counter (PC) is a pointer for program memory and contains the starting address for the next instruction.



The program counter PC is initialized to 1020H after hardware reset. That is, the application program starts executing from the address 1020H after hardware reset.

Memory configuration register (MCF) only use in SM8505/SM8506

This is a register which sets the accessible address range of internal memory within internal ROM field (1000H-FFFFH). The outside field which set by this register can be used as the access field of external memory. Had set this register as soon as the setting memory field becomes valid. The internal memory beyond the setting field cannot be accessed. To access the external memory, it is necessary to switch the SM8505/SM8506 to external memory expansion mode by setting the bits MCNF2-MCNF0 (bit 2-0 : SYS). The initial value of the register is in the all build-in ROM accessible state. This register is only valid for SM8505/SM8506.

For all others SM8500 series, other than SM8505/SM8506, the operation for the register read/write does not affect to microcomputer internal action.

Internal / external overlap memory field is accessible by program switching. While the program switches to access internal memory from external memory, only if sets the external memory expansion mode to be invalid by setting system configuration register SYS, the overlap internal memory is impossible to access. The access field also is necessary to change by register MCF. In addition, if sets the bits MC3-MC0 to '0000' and the corresponding pins is in the state, same as external memory expansion mode, then all internal ROM will be accessible.

Bit 7 0

-	-	-	-	MC3	MC2	MC1	MC0

Bit 3-0 : Build-in memory accessing field selection bit

BIT	BUILD-IN MEMORY ACCESSING FIELD		EXTERNAL MEMORY FIELD	
0000	60k bytes	1000H-FFFFH	Nothing	
0001	56k bytes	1000H-EFFFH	4k bytes	F000H-FFFFH
0010	52k bytes	1000H-DFFFH	8k bytes	E000H-FFFFH
0011	48k bytes	1000H-CFFFH	12k bytes	D000H-FFFFH
0100	44k bytes	1000H-BFFFH	16k bytes	C000H-FFFFH
0101	40k bytes	1000H-AFFFH	20k bytes	B000H-FFFFH
0110	36k bytes	1000H-9FFFH	24k bytes	A000H-FFFFH
0111	32k bytes	1000H-8FFFH	28k bytes	9000H-FFFFH
1000	28k bytes	1000H-7FFFH	32k bytes	8000H-FFFFH
1001	24k bytes	1000H-6FFFH	36k bytes	7000H-FFFFH
1010	20k bytes	1000H-5FFFH	40k bytes	6000H-FFFFH
1011	16k bytes	1000H-4FFFH	44k bytes	5000H-FFFFH
1100	12k bytes	1000H-3FFFH	48k bytes	4000H-FFFFH
1101	8k bytes	1000H-2FFFH	52k bytes	3000H-FFFFH
1110	4k bytes	1000H-1FFFH	56k bytes	2000H-FFFFH
1111	disable			

Address Space

Fig. 9 shows the SM8500CPU address space. The 64k bytes address space is divided into RAM (0000H-0FFFH) and ROM (1000H-FFFFH) areas. The address 0000H-007FH are both shared by RAM and register file.

The amounts of RAM and ROM physically present are different between SM8500 series number. For more details, please refer to [Memory Map].

The RAM and register file, which allocated at 0000H-007FH, can be selected by the addressing mode, designated by instructions.

ROM Area

ROM area starts at the address 1000H of the space address. The first portion (1000H-101FH) is reserved for the interrupt vector table. Each 2 bytes entry in the vector table contains the address of interrupts. When an interrupt encountered, the CPU jumps to the corresponding branch address of vector table for program executing. The address 1020H marks the start of the user program area itself. Executing always starts at 1020H after hardware reset.

Register File Area

The register file is allocated between 0000H and 007FH. The first 16 bytes (0000H-000FH) area are general registers. The remainder is for CPU control registers, peripherals control register and data register.

The accessing manipulation for register file is based on the addressing mode, (1) register file R, (2) register file pair RR, and (3) port P.

RAM Area

The RAM area starts at the beginning 0000H of the address space. It overlaps the register file for the address 0000H-007FH.

This arrangement is to shorten the instruction length as much as possible and to permit the use with both RAM and the register file for faster execution.

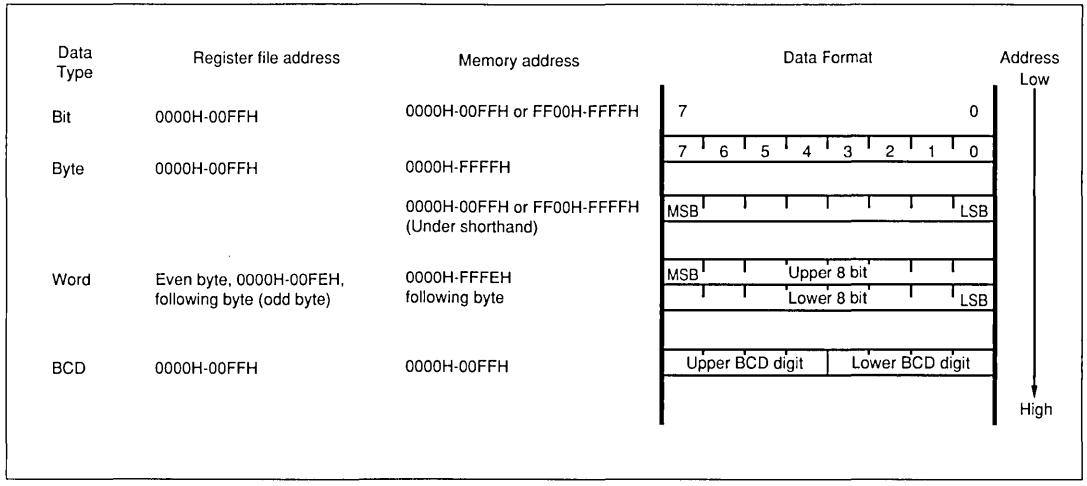


Fig. 3 Register file / memory data formats

Data Format

The SM85CPU supports four data types : bit, 4-bit BCD, byte, and word data.

REGISTER FILE DATA FORMATS

The register file (0000H-007FH) and RAM (0080H-00FFH) accessible with register file R and register file pair RR addressing support processing for all 4 data types : bit 4-bit BCD, byte, and word data. Fig. 3 shows the data layout in the register file.

Bit data (register file)

Bit manipulation instructions access bit data in the register by register file R addressing, which gives the byte address in the register file (0000H-007FH), or RAM (0080H-00FFH), and the operand b, which gives the bit number within the byte.

Byte data (register file)

Instructions access the byte data in the register file by register file R addressing, which gives the byte data address in the register file (0000H-007FH) or RAM (0080H-00FFH).

Word data (register file)

Instructions access word data in the register file by register file pair RR addressing, which gives the word address, even and 2 bytes address, in the register file (0000H-007FH) or RAM (0080H-00FFH). The address must be even (0, 2, 4,..., 254). Specifying an odd address leads to unreliable results.

BCD data (register file)

The decimal adjust instruction (DA), used to adjust BCD digits after an odd or substract, accesses a BCD data byte in the register file by register file R addressing.

Notice for the general register on register file

The general registers are the first 16 bytes (0000H-000FH) in the register file. They can be accessed as byte-sized by register file R addressing and as word-sized by register file pair RR addressing.

MEMORY DATA FORMATS

The memory area (ROM and RAM 0000H-FFFFH) supports processing for all 4 data types :bit , 4-bit BCD, byte, and word data. However, bit data is limited to the ranges (0000H-00FFH, FF00H-FFFFH), and 4-bit BCD data to the ranges 0000H-00FFH. Fig. 3 shows the data layout in memory.

Bit data (memory)

Bit manipulation instructions access bit data in memory by register index n(r) addressing, which gives the byte address in the range (0000H-00FFH), or by direct special page DAp addressing, which gives the byte address in the range (FF00H-FFFFH), and the operand b, which gives the bit number within the byte.

Byte data (memory)

Instructions access the byte data in memory by shorthand (0000H-00FFH or FF00H-FFFFH or full (0000H-FFFFH) address.

Word data (memory)

Instructions access the word data, continue 2 bytes, in memory by shorthand (0000H-00FFH or FF00H-FFFFH) or full (0000H-FFFFH) address. Unlike word data in the register file, the address can be even or odd.

BCD data (memory)

The decimal adjust instruction (DA), used to adjust BCD digits after an odd or substract, accesses a BCD data byte in memory by register index @r addressing.

Notice for general register on memory

The general registers are actually in a RAM area specified by register pointer RP, so they can be read and modify directly as RAM. While programming, the programmer must take care to arrange program data so that other RAM operations do not destroy general registers content.

Bus Timing

The SM85CPU is variable for system clock. The bit FCPUS2-FCPUS0 (bit5-3 : CKKC) of the clock changing register CKKC can select system clock to 1/2, 1/4, 1/8, 1/16, 1/32 of the main clock and 1/2 of sub-clock. The CPU operates at 1/32 clock of the main clock after hardware reset.

INTERNAL MEMORY ACCESS TIMING

The read cycle of internal RAM is 2 cycles. The internal RAM supports 2 cycles for reading or writing.

EXTERNAL MEMORY ACCESS TIMING

The external memory supports 2 cycles for reading or writing. Fig. 5 shows the read timing and Fig. 6 shows the write timing.

INSTRUCTION PREFETCH

The SM8500 CPU, which execution cycle overlaps with the OP code, fetches next instruction OP code during one instruction execution cycle. For example, the execution time for 2 bytes instructions (MOV R, r) of transferring the RAM contents to a register is 4 cycles.

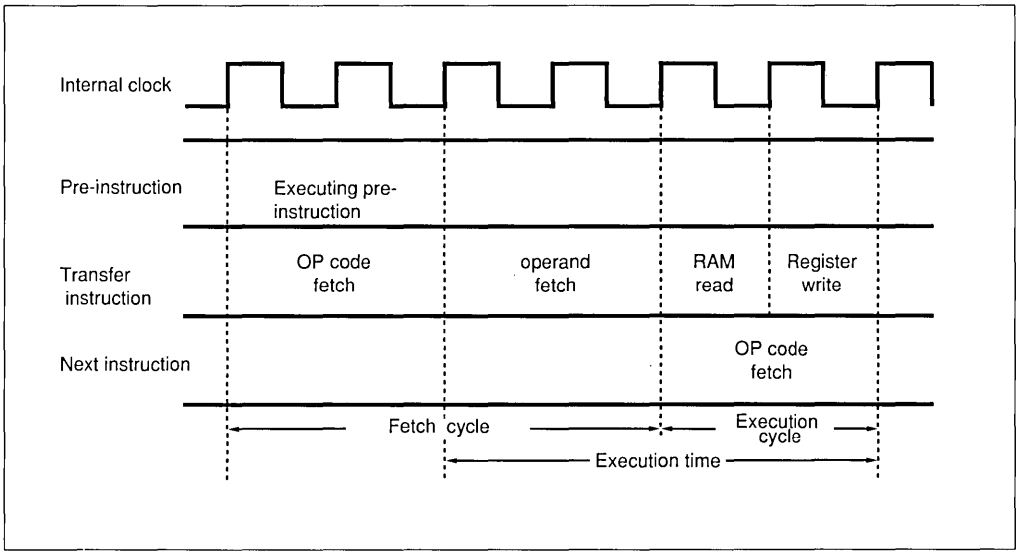
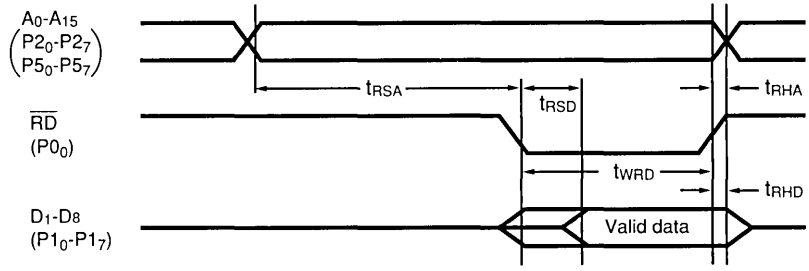


Fig. 4 Instruction execution for transfer instruction (2 bytes)

External memory access timing (read timing)



t_{RSA} : The time between address firm and $\overline{RD}$ signal falling low level firm.

t_{RSD} : The time between $\overline{RD}$ signal firm and input valid data firm.

t_{WRD} : $\overline{RD}$ signal low level width.

t_{RHA} : The time between $\overline{RD}$ signal rising high level firm and address change.

t_{RHD} : The time between $\overline{RD}$ signal rising high level firm and output data floating.

Load capacitance is 50 pF.

Fig. 5 External memory access timing (read timing)

• Operating condition (V_{DD} = 4.5 V to 5.5 V, T_{OPR}= –20 to 70°C)

ITEM	SYMBOL	RATINGS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Address setup time	t_{RSA}		t_{SYS}	t_{SYS} + 50	ns	1
Read data setup time	t_{RSD}			(t_{SYS}/2) – 30	ns	1
$\overline{RD}$ signal pulse width	t_{WRD}	t_{SYS} – 50		t_{SYS}	ns	1
Address hold time	t_{RHA}	0			ns	
Read data hold time	t_{RHD}	0			ns	

NOTE :

1. t_{SYS} : The system clock period (main clock x 1/2) when the bits FCPUS2-FCPUS0 = [100].

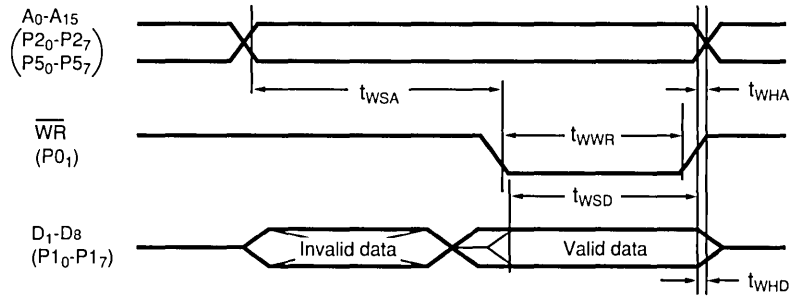
• Operating condition (V_{DD} = 2.7 V to 5.5 V, T_{OPR}= –20 to 70°C)

ITEM	SYMBOL	RATINGS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Address setup time	t_{RSA}		t_{SYS}	t_{SYS} + 80	ns	1
Read data setup time	t_{RSD}			(t_{SYS}/2) – 60	ns	1
$\overline{RD}$ signal pulse width	t_{WRD}	t_{SYS} – 80		t_{SYS}	ns	1
Address hold time	t_{RHA}				ns	
Read data hold time	t_{RHD}				ns	

NOTE :

1. t_{SYS} : The system clock period which set by the bits FCPUS2-FCPUS0 setting to a value other than [100] under V_{DD} = 4.5 V to 5.5 V. Or, the system clock period which under V_{DD} = 2.7 V to 5.5V.

External memory access timing (write timing)



t_{WSA} : The time between address firm and $\overline{WR}$ signal falling low level firm.

t_{WSD} : The time between $\overline{WR}$ signal firm and input valid data firm.

t_{WRD} : $\overline{WR}$ signal low level width.

t_{WHA} : The time between $\overline{WR}$ signal rising high level firm and address change.

t_{WHD} : The time between $\overline{WR}$ signal rising high level firm and output data floating.

Load capacitance is 50 pF.

Fig. 6 External memory access timing (write timing)

• Operating condition (V_{DD} = 4.5 V to 5.5 V, T_{OPR}= –20 to 70°C)

ITEM	SYMBOL	RATINGS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Address setup time	t_{WSA}		t_{SYS}	t_{SYS} + 50	ns	1
Data setup time	t_{WSD}	t_{SYS} – 50	t_{SYS} + 10		ns	1
$\overline{WR}$ signal pulse width	t_{WWR}	t_{SYS} – 60		t_{SYS}	ns	1
Address hold time	t_{WHA}	10			ns	
Data hold time	t_{WHD}	10			ns	

NOTE :

1. t_{SYS} : The system clock period (main clock x 1/2) when the bits FCPUS2-FCPUS0 = [100].

• Operating condition (V_{DD} = 2.7 V to 5.5 V, T_{OPR}= –20 to 70°C)

ITEM	SYMBOL	RATINGS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Address setup time	t_{WSA}		t_{SYS}	t_{SYS} + 80	ns	1
Data setup time	t_{WSD}	t_{SYS} – 80	t_{SYS} + 20		ns	1
$\overline{WR}$ signal pulse width	t_{WWR}	t_{SYS} – 100		t_{SYS}	ns	1
Address hold time	t_{WHA}	10			ns	
Data hold time	t_{WHD}	10			ns	

NOTE :

1. t_{SYS} : The system clock period which set by the bits FCPUS2-FCPUS0 setting to a value other than [100] under V_{DD} = 4.5 V to 5.5 V. Or, the system clock period which under V_{DD} = 2.7 V to 5.5V.

SYSTEM CONTROL

Oscillator Circuit

The SM8500 builds in the main-clock and sub-clock oscillator circuits for generating clock signal. The main-clock oscillator circuit is applied to 1.5 to 12 MHz. The sub-clock oscillator circuit is applied to 32.768 kHz.

Clock System

The SM8500 uses the main-clock and sub-clock oscillator circuits to generate the required clock.

The system clock, lead CPU operation, is one of the five clocks which dividing the main-clock (f_{CK}) into 1/2, 1/4, 1/8, 1/16, 1/32. It also selects from sub-clock (f_{32K}). In addition, the clocks supplied to the peripheral functions are fc_1-fc_{10} divided by the prescaler PRS0 and derived from the 1/2 clock of main-clock, ($f_{CK}/2$). It is also are fx_1-fx_8 divided by the prescaler PRS1 and derived from the sub-clock.

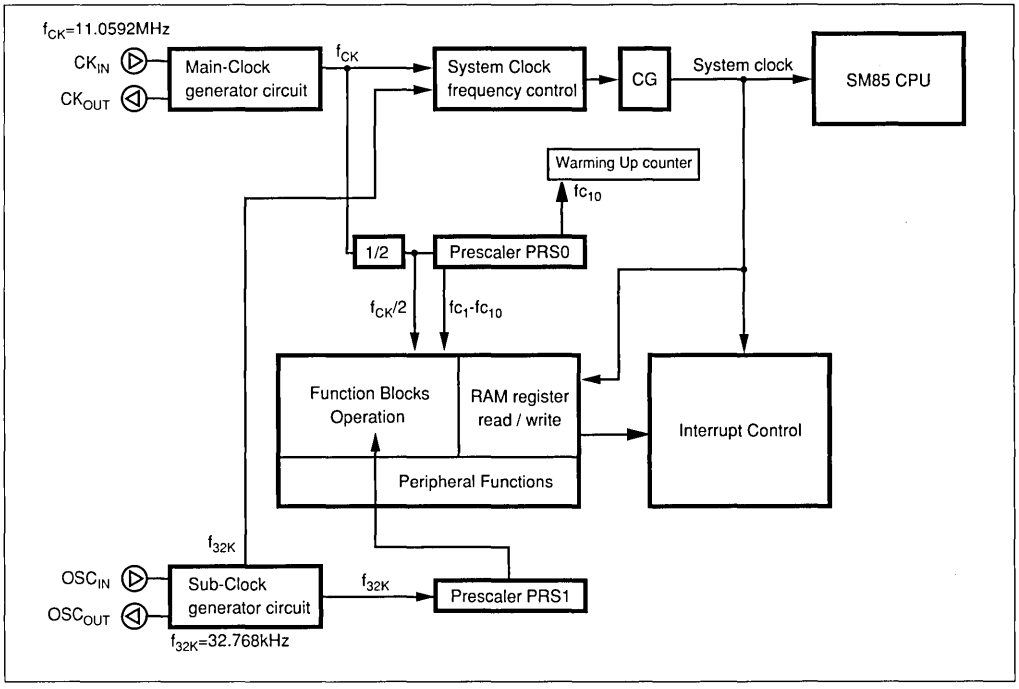


Fig. 7 SM8500 clock system

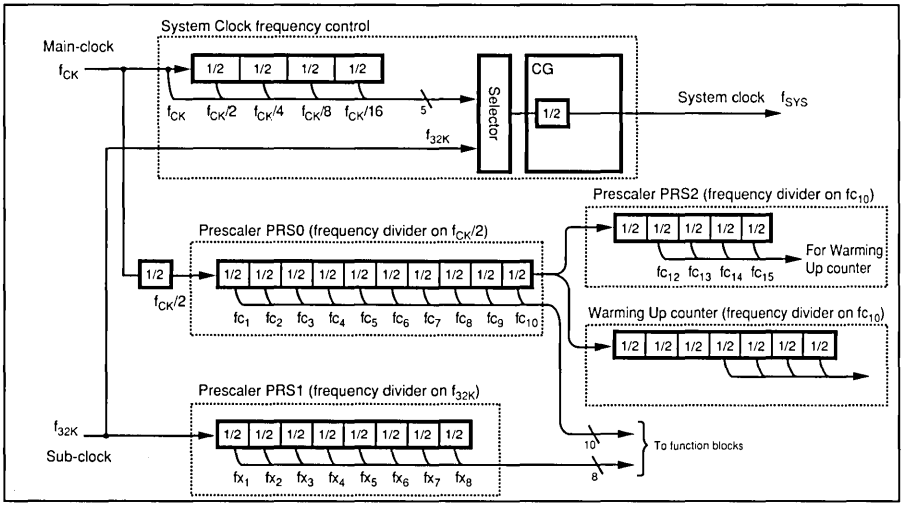


Fig. 8 SM8500 clock system (equivalent circuit for clock system peripheral blocks)

Clock change register (CKKC)

Clock change register CKKC is an 8-bit readable/writable register containing the control of system clock change and the setting of warming up period after waking up from the STOP mode.

Clock change register CKKC is initialized to 00H after hardware reset.

Bit 7 0

FCPUEN	MCKSTP	FCPUS2	FCPUS1	FCPUS0	TFCPU	WUPS1	WUPS0

Bit 7 : Clock change enable bit (FCPUEN)

0 | disable system clock speed change

1 | enable system clock speed change

Bit 6 : Main-clock stopped bit (MCKSTP)

Main-clock stopped allows switching to sub-clock used as system clock.

0 | Main-clock operation

1 | Main-clock stop

Bit 5-3 : System clock selection bit (FCPUS2-FCPUS0)

Under the bit FCPUEN = [1], if executes the STOP instruction, the bits will be valid.

BIT	SYSTEM CLOCK FREQUENCY
000	system clock = (1/32) x main-clock
001	system clock = (1/16) x main-clock
010	system clock = (1/8) x main-clock
011	system clock = (1/4) x main-clock
100	system clock = (1/2) x main-clock
101, 110	disable
111	system clock = (1/2) x sub-clock

Bit 2 : Reserved bit (TFCPU)

Always write '0' to this position. Writing a '1' produces unrealiable operation.

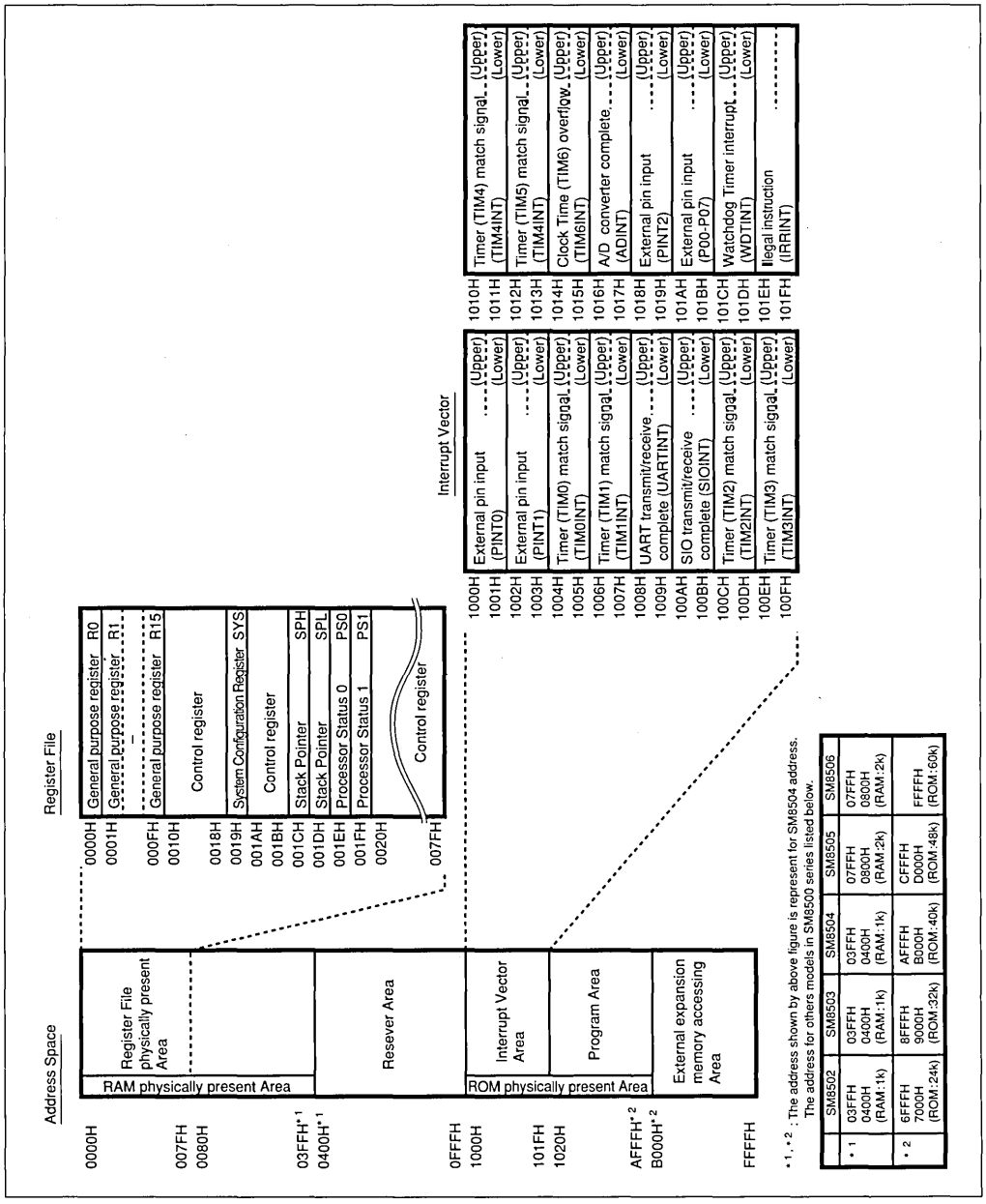
Bit 1-0 : Warming up selection bit (WUPS1-WUPS10)

The bits are able to set the warming up period of after wake up from STOP mode

BIT	WARMING UP PERIOD AFTER STOP MODE RELEASES (when main-clock (f_{CK}) = 11.0592 MHz)
00	2^{18} x main-clock period (23.70 ms)
01	2^{17} x main-clock period (11.85 ms)
10	2^{16} x main-clock period (5.9326 ms)
11	2^{15} x main-clock period (2.963 ms)

Memory Map

Fig.9 shows the SM8500 memory map.



*1, *2 : The address shown by above figure is represent for SM6504 address.
The address for others models in SM8500 series listed below.

	SM8502	SM8503	SM8504	SM8505	SM8506
*1	03FFH 0400H (RAM:1k)	03FFH 0400H (RAM:1k)	03FFH 0400H (RAM:1k)	07FFH 0800H (RAM:2k)	07FFH 0800H (RAM:2k)
*2	6FFFH 7000H (ROM:24k)	8FFFH 9000H (ROM:32k)	AFFFH B000H (ROM:40k)	CFFFH D000H (ROM:48k)	FFFFH (ROM:60k)

Fig. 9 SM8500 memory map (1)

Address	Register name			R/W	Initial value
0000H	General purpose register	R0	RR0	R/W	Undefined
0001H	General purpose register	R1		R/W	Undefined
0002H	General purpose register	R2	RR2	R/W	Undefined
0003H	General purpose register	R3		R/W	Undefined
0004H	General purpose register	R4	RR4	R/W	Undefined
0005H	General purpose register	R5		R/W	Undefined
0006H	General purpose register	R6	RR6	R/W	Undefined
0007H	General purpose register	R7		R/W	Undefined
0008H	General purpose register	R8	RR8	R/W	Undefined
0009H	General purpose register	R9		R/W	Undefined
000AH	General purpose register	R10	RR10	R/W	Undefined
000BH	General purpose register	R11		R/W	Undefined
000CH	General purpose register	R12	RR12	R/W	Undefined
000DH	General purpose register	R13		R/W	Undefined
000EH	General purpose register	R14	RR14	R/W	Undefined
000FH	General purpose register	R15		R/W	Undefined
0010H	Interrupt enable register 0		IE0	R/W	00H
0011H	Interrupt enable register 1		IE1	R/W	00H
0012H	Interrupt flag register 0		IF0	R/W	00H
0013H	Interrupt flag register 1		IF1	R/W	03H
0014H	External interrupt mode register		EXIN	R/W	00H
0015H	SIO Control register		SRC	R/W	00H
0016H	SIO Data register		SRD	R/W	Undefined
0017H	A/D Data register		ADCD	R/W	00H
0018H	A/D Control register		ADCC	R/W	00H
0019H	System configuration register		SYS	R/W	*0000000
001AH	Clock change regsiter		CKKC	R/W	00H
001BH	Reverse (access disable)			-	-
001CH	Stack pointer H	SPH	SP	R/W	Undefined
001DH	Stack pointer L	SPL		R/W	Undefined
001EH	Processor status 0		PS0	R/W	Undefined
001FH	Processor status 1		PS1	R/W	*******0

Address	Register name		R/W	Initial value
0020H	P0 (Input) register	P0	R	Undefined
0021H	P1 (Input/Output) register	P1	R/W	00H
0022H	P2 (Input/Output) register	P2	R/W	00H
0023H	P3 (Input/Output) register	P3	R/W	00H
0024H	P4 (Input) register	P4	R	Undefined
0025H	P5 (Input/Output) register	P5	R/W	00H
0026H	P6 (Output) register	P6	R/W	00H
0027H	P7 (Input/Output) register	P7	R/W	00H
0028H	P8 (Input/Output) register	P8	R/W	00H
0029H	P9 (Input/Output) register	P9	R/W	F0H
002AH	PA (Output) register	PA	R/W	00H
002BH	UART Transmit data register	URTT	W	FFH
002CH	UART Receive data register	URTR	R	00H
002DH	UART Status register	URTS	R	0*000010
002EH	UART Control register	URTC	R/W	00H
002FH	UART Baud rate setting register	URTB	R/W	00H
0030H	P0 Control register	P0C	R/W	00H
0031H	P1 Control registe	P1C	R/W	00H
0032H	P2 Control registe	P2C	R/W	00H
0033H	P3 Control registe	P3C	R/W	00H
0034H	P4 Control registe	P4C	R/W	00H
0035H	P1 Pull-up setting register	P1PC	R/W	00H
0036H	P2 Pull-up setting register	P2PC	R/W	00H
0037H	P7 Control registe	P7C	R/W	00H
0038H	P8 Control registe	P8C	R/W	00H
0039H	P9 Control registe	P9C	R/W	F0H
003AH	P5 Control registe	P5C	R/W	00H
003BH	Port Pull-up setting register	PPC	R/W	00H
003CH	Waveform generator scale data registe 0	WGSD0	R/W	00H
003DH	Waveform generator scale data registe 1	WGSD1	R/W	00H
003EH	Waveform generator scale control registe	WGC	R/W	11H
003FH	D/A Control registe	DACC	R/W	33H

Fig. 9 SM8500 memory map (2)

NOTES :

- R/W indicates that there is at least one bit in the register is capable of read/write.
  (The register indicated by R/W includes the bit of special-purpose register for read). R indicates that the register is only for read.
- * indicates that the corresponding bit is ubdefined.

Address	Register name			R/W	Initial
0040H	Timer0 counter H	TM0H	TM0	R	00H
0041H	Timer0 counter L	TM0L		R	00H
0042H	Timer0 modular register H	TM0MH	TM0M	R/W	FFH
0043H	Timer0 modular register L	TM0ML		R/W	FFH
0044H	Timer0 capture register H	TM0PH	TM0P	R	00H
0045H	Timer0 capture register L	TM0PL		R	00H
0046H	Timer0 control register 0		TM0C0	R/W	C0H
0047H	Timer0 control register 1		TM0C1	R/W	1FH
0048H	Timer counter		TM1	R	00H
0049H	Timer1 modular register		TM1M	R/W	FFH
004AH	Timer1 control register		TM1C	R/W	07H
004BH	Timer2 counter		TM2	R	00H
004CH	Timer2 modular register		TM2M	R/W	FFH
004DH	Timer2 control register		TM2C	R/W	07H
004EH	Timer1/2 clock select register		TM12CT	R/W	00H
004FH	Reverse (access disable)			-	-
0050H	Timer4 counter		TM4	R	00H
0051H	Timer3 counter		TM3	R	00H
0052H	Timer3 control register		TM3C	R/W	00H
0053H	Reverse (Only use for flash memory version) *1			-	-
0054H	Timer4 modular register		TM4M	R/W	FFH
0055H	Timer3 modular registe		TM3M	R/W	FFH
0056H	Timer4 control register		TM4C	R/W	00H
0057H	Memory configuration register *2		MCF	-	-
0058H	Timer5 counter		TM5	R	00H
0059H	Timer5 modular register		TM5M	R/W	FFH
005AH	Timer5 control register		TM5C	R/W	10H
005BH	Reverse (Only use for flash memory version) *1			-	-
005CH	Timer6 counter		TM6	R	00H
005DH	Timer6 control register		TM6C	R/W	38H
005EH	Watchdog timer register		WDT	R	00H
005FH	Watchdog timer control register		WDTC	R/W	38H

Address	Register name		R/W	Initial
0060H	Waveform memory 0 Step00/01	WGM00	R/W	Undefined
0061H	Waveform memory 0 Step02/03	WGM01	R/W	Undefined
0062H	Waveform memory 0 Step04/05	WGM02	R/W	Undefined
0063H	Waveform memory 0 Step06/07	WGM03	R/W	Undefined
0064H	Waveform memory 0 Step08/09	WGM04	R/W	Undefined
0065H	Waveform memory 0 Step10/11	WGM05	R/W	Undefined
0066H	Waveform memory 0 Step12/13	WGM06	R/W	Undefined
0067H	Waveform memory 0 Step14/15	WGM07	R/W	Undefined
0068H	Waveform memory 0 Step16/17	WGM08	R/W	Undefined
0069H	Waveform memory 0 Step18/19	WGM09	R/W	Undefined
006AH	Waveform memory 0 Step20/21	WGM0A	R/W	Undefined
006BH	Waveform memory 0 Step22/23	WGM0B	R/W	Undefined
006CH	Waveform memory 0 Step24/25	WGM0C	R/W	Undefined
006DH	Waveform memory 0 Step26/27	WGM0D	R/W	Undefined
006EH	Waveform memory 0 Step28/29	WGM0E	R/W	Undefined
006FH	Waveform memory 0 Step30/31	WGM0F	R/W	Undefined
0070H	Waveform memory 1 Step00/01	WGM10	R/W	Undefined
0071H	Waveform memory 1 Step02/03	WGM11	R/W	Undefined
0072H	Waveform memory 1 Step04/05	WGM12	R/W	Undefined
0073H	Waveform memory 1 Step06/07	WGM13	R/W	Undefined
0074H	Waveform memory 1 Step08/09	WGM14	R/W	Undefined
0075H	Waveform memory 1 Step10/11	WGM15	R/W	Undefined
0076H	Waveform memory 1 Step12/13	WGM16	R/W	Undefined
0077H	Waveform memory 1 Step14/15	WGM17	R/W	Undefined
0078H	Waveform memory 1 Step16/17	WGM18	R/W	Undefined
0079H	Waveform memory 1 Step18/19	WGM19	R/W	Undefined
007AH	Waveform memory 1 Step20/21	WGM1A	R/W	Undefined
007BH	Waveform memory 1 Step22/23	WGM1B	R/W	Undefined
007CH	Waveform memory 1 Step24/25	WGM1C	R/W	Undefined
007DH	Waveform memory 1 Step26/27	WGM1D	R/W	Undefined
007EH	Waveform memory 1 Step28/29	WGM1E	R/W	Undefined
007FH	Waveform memory 1 Step30/31	WGM1F	R/W	Undefined

Fig. 9 SM8500 memory map (3)

*1 : These two address are only valid with flash memory version [LU8500F0/F1] and do not exist in SM8500 series.
Executing read/write operation at these address do not effect to the SM8500 operation.

*2 : Only exist for SM8506 and flash memory version [LU8500F0/F1].

Hardware Reset

The hardware reset is an initial function for SM8500 system and comes from the following sources.

(1) External reset

If the $\overline{\text{RESET}}$ pin is applied to low level in SM8500 operating, the hardware resets.

(2) Watchdog timer overflow

While watchdog timer overflows, the hardware resets.

The above 2 hardware reset sources initializate the system.

OPERATING EXPLANATIONS

Hardware reset operation

When the SM8500 is operating, a built-in pull-up resistor keeps the RESET pin at High level. If external circuit (like as reset IC, etc.) applies Low level voltage to RESET pin, the SM8500 is reset by hardware after approximately two instruction cycles. To ensure hardware reset execution keeps the RESET pin at Low level over two instruction cycles of system clock.

The pin back to High level from Low level starts the warming up counter built in SM8500. When the counter overflows, about 2^{18} x main-clock (23.70 ms : 11.0592 MHz), leaves its hardware reset state and begins the program execution from the instruction at address 1020H. In the warming up interval, SM8500 is in HALT mode state.

Same as watchdog Timer overflow case, the CPU leaves the hardware reset behind warming up period.

System initial state

Immediately after hardware reset, the system is initializated as following.

- The registers listed below are undefined for their contents.
  - General register R0-R15
  - Stack pointer SPH, SPL
  - Processor status PS0, PS1 [other than bit I (bit 0 : PS1)]
  - Waveform memory WGM00-WGM1F
  - Internal RAM
  - The read value of P0, P4 (input) register

- The I/O pins are in the following states.
  - The port function shared by port/peripheral function is selected.
  - I/O ports are in input state.
  - I/O ports and input only ports are in the pull-up resistance 'OFF' state.
  - Output only ports are in Low level state.

- The Interrupt control register are in the following states
  - Bit I (bit 0 : PS1) is cleared to '0', all maskable interrupts are in disable state.
  - All bits of the interrupt enable registers IE0 , IE1 are cleared to '0', every maskable interrupt is in disable state.

- All built-in peripheral functions all stop. About the initial value for other control registers on the register fill, please refer to [Fig. 9 memory map].

Interrupt Function

The SM8500 supports 16 interrupt sources.

In these interrupts, watchdog timer and illegal instruction trap interrupts are belong to non-maskable interrupt, the others, however, are maskable interrupts

16 interrupt sources are shared to independent interrupt vector, respectively, in the ROM address area between 1000H-101FH. And, the maskable interrupts are set to 14 steps with priority level.

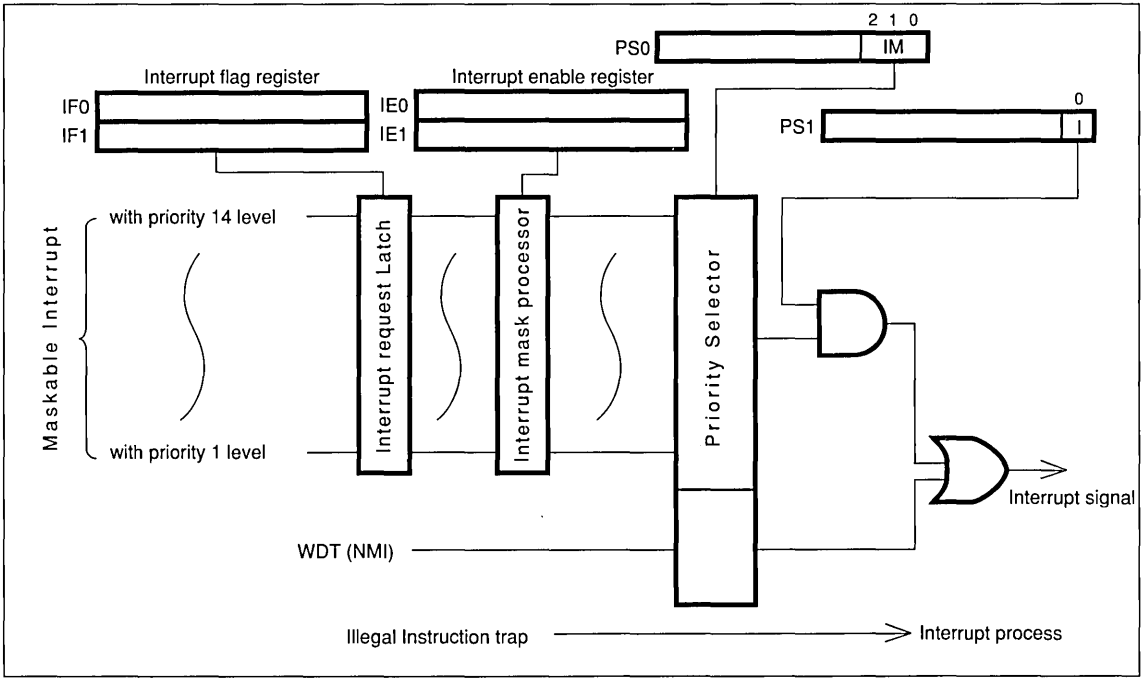


Fig. 10 Interrupt block diagram

Table 3 SM8500 interrupt vectors location and their priority

VECTOR LOCATION	INTERRUPT SOURCE	SYMBOL	PRIORITY*
1000H	External pin input ($P3_3$/$PINT_0$/$CINT_0$)	PINT0	1
1002H	External pin input ($P3_6$/$PINT_1$)	PINT1	2
1004H	Timer (TIM0) match signal	TIM0INT	3
1006H	Timer (TIM1) match signal	TIM1INT	4
1008H	UART transmit/receive complete	UARTINT	5
100AH	SIO transmit/receive complete	SIOINT	6
100CH	Timer (TIM2) match signal	TIM2INT	7
100EH	Timer (TIM3) match signal	TIM3INT	8
1010H	Timer (TIM4) match signal	TIM4INT	9
1012H	Timer (TIM5) match signal	TIM5INT	10
1014H	Clock Timer (TIM6) overflow	TIM6INT	11
1016H	A/D converter complete	ADINT	12
1018H	External pin input ($P3_7$/$PINT_2$)	PINT2	13
101AH	External pin input ($P0_0$-$P0_7$)	KYINT	14
101CH	Watchdog timer overflow	WDTINT	–
101EH	Illegal instruction	IRRINT	–

* The priority levels determine the order in which the chip process simultaneous interrupts. It also denotes the priority level of mask interrupts by setting the bits IM2-IM0 (bit 2-0 : PS0).

Register Explanations

interrupt mask bit (IM) of processor status 0 (PS0)

The bits IM2-IM0 can set the acceptable level for interrupt. The maskable interrupt requested by CPU is set to 1 to 14 priority level. These bits IM2-IM0 determine processing interrupts which priority level.

Bit 2-0 : Interrupt mask bit (IM2-IM0)

BIT	CONTENT
000	All maskable interrupts recognized.
001	All maskable interrupts recognized.
010	Maskable interrupts with 1 to 12 level recognized.
011	Maskable interrupts with 1 to 10 level recognized.
100	Maskable interrupts with 1 to 8 level recognized.
101	Maskable interrupts with 1 to 6 level recognized.
110	Maskable interrupts with 1 to 4 level recognized.
111	Maskable interrupts with 1 to 2 level recognized.

* When an interrupt enables by interrupt mask bit, if all interrupt conditions are setup, then the CPU starts to the interrupt processing.

Interrupt enable bit (I) of processor status 1 (PS1)

The bit I (bit 0 : PS1) enables/disables all maskable interrupts. After hardware reset, the bit I is cleared to '0' and so all maskable interrupts are in disable state.

Bit 0 : Interrupt enable (I).

BIT	CONTENT
0	Disable to accept all maskable interrupts
1	Enable to accept maskable interrupt. For each maskable interrupt can be enabled/ disabled by interrupt enable register IE0, IE1 and bits IM2-IM0.

Except that write to processor status PS1 directly, the bit I can be set/cleared by the following special-purpose instructions. (Under normal case, the special-purpose instructions are used.)

DI instruction : bit I is cleared to '0'.

EI instruction : bit I is set to '1'.

Interrupt enable register 0 (IE0)

The interrupt enable register IE0 is an 8-bit readable/writable register containing the settings for enable/disable to accept interrupt sources.

Bit 7 0

IE07	IE06	IE05	IE04	IE03	IE02	IE01	IE00

Bit 7 : PINT0 Interrupt Enable bit
Bit 6 : PINT1 Interrupt Enable bit
Bit 5 : Timer 0 Interrupt Enable bit
Bit 4 : Timer 1 Interrupt Enable bit
Bit 3 : UART Interrupt Enable bit
Bit 2 : SIO Interrupt Enable bit
Bit 1 : Timer 2 Interrupt Enable bit
Bit 0 : Timer 3 Interrupt Enable bit

BIT	CONTENT
0	disable
1	enable

Interrupt enable register 1 (IE1)

The interrupt enable register IE1 is an 8-bit readable/writable register containing the settings for enable/disable to accept interrupt sources.

Bit 7 0

IE17	IE16	IE15	IE14	IE13	IE12	-	-

Bit 7 : Timer 4 Interrupt Enable bit
Bit 6 : Timer 5 Interrupt Enable bit
Bit 5 : Timer 6 Interrupt Enable bit
Bit 4 : A/D Interrupt Enable bit
Bit 3 : PINT2 Interrupt Enable bit
Bit 2 : P0 Interrupt Enable bit

BIT	CONTENT
0	disable
1	enable

The bit 1 and bit 0 are readable/writable bits. To manipulate these bits also do not affect others operation of the microcomputer.

The interrupt enable register IE0 and IE1 also are used to wake up the chip from standby mode (STOP mode, HALT mode) by setting the interrupt to enable. If the interrupt enabled by the interrupt enable register IE0 and IE1 occurs, the chip will wake up from standby mode. But also there is interrupt source which cannot use to wake up from STOP mode.

Interrupt flag register 0 (IF0)

The interrupt flag register IF0 is an 8-bit readable/writable register. If the interrupt occurs, the corresponding bit will be set to '1'.

Bit 7 0

IF07	IF06	IF05	IF04	IF03	IF02	IF01	IF00

Bit 7 : PINT0 Interrupt Request bit
Bit 6 : PINT1 Interrupt Request bit
Bit 5 : Timer 0 Interrupt Request bit
Bit 4 : Timer 1 Interrupt Request bit
Bit 3 : UART Interrupt Request bit
Bit 2 : SIO Interrupt Request bit
Bit 1 : Timer 2 Interrupt Request bit
Bit 0 : Timer 3 Interrupt Request bit

BIT	CONTENT
0	-
1	request

Interrupt flag register 1 (IF1)

The interrupt flag register IF0 is an 8-bit readable/writable register. If the interrupt occurs, the corresponding bit will be set to '1'.

Bit 7 0

IF17	IF16	IF15	IF14	IF13	IF12	-	-

Bit 7 : Timer 4 Interrupt Request bit
Bit 6 : Timer 5 Interrupt Request bit
Bit 5 : Timer 6 Interrupt Request bit
Bit 4 : A/D Interrupt Request bit
Bit 3 : PINT2 Interrupt Request bit
Bit 2 : P0 Interrupt Request bit

BIT	CONTENT
0	-
1	request

P0 control register (P0C)

The control register P0C is an 8-bit readable/writable register and enables/disables the external interrupt $P0_0$-$P0_7$ in bit unit.

The external internal $P0_0$-$P0_7$ occurs with falling edge of each input pin and is shared to same interrupt vector (101AH-101BH). The bit IE12 (bit 2 : IE1) can disable all the external internal $P0_0$-$P0_7$.

Bit 7 0

P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0

Bit 7 : $P0_7$ Interrupt Enable bit
Bit 6 : $P0_6$ Interrupt Enable bit
Bit 5 : $P0_5$ Interrupt Enable bit
Bit 4 : $P0_4$ Interrupt Enable bit
Bit 3 : $P0_3$ Interrupt Enable bit
Bit 2 : $P0_2$ Interrupt Enable bit
Bit 1 : $P0_1$ Interrupt Enable bit
Bit 0 : $P0_0$ Interrupt Enable bit

BIT	CONTENT
0	enable
1	disable

External interrupt mode register (EXIN)

The register is use for setting external interrupt ports (PINT0/$P3_3$, PINT1/$P3_6$, PINT2/$P3_7$).

Table 4 Interrupt control register

Interrupt Source		Interrupt Control Register			
		Mask Enable	Priority Level	Enable Register	Other
External pin input ($P3_3$/$PINT_0$/CNT_0) (including capture input)		Bit 1 (bit0:PS1)	Bit IM (bit2-0:PS0)	IE07 (bit7 : IE0)	EXS00-01 (bit7-6 : EXIN) (Sampling clock selection) EX00-01 (bit5-4 : EXIN) (Detect edge selection)
External pin input ($P3_6$/$PINT_1$)				IE06 (bit6 : IE0)	EX10-11 (bit3-2 : EXIN) (Low level detect, detect edge selection)
Timer (TIM0) match signal				IE05 (bit5 : IE0)	
Timer (TIM1) match signal				IE04 (bit4 : IE0)	
UART transmit/receive complete				IE03 (bit3 : IE0)	
SIO transmit/receive complete				IE02 (bit2 : IE0)	
Timer (TIM2) match signal				IE01 (bit1 : IE0)	
Timer (TIM3) match signal				IE00 (bit0 : IE0)	
Timer (TIM4) match signal				IE17 (bit7 : IE1)	
Timer (TIM5) match signal				IE16 (bit6 : IE1)	
Clock Timer (TIM6) overflow				IE15 (bit5 : IE1)	
A/D converter complete				IE14 (bit4 : IE1)	
External pin input ($P3_7$/$PINT_2$)				IE13 (bit3 : IE1)	EX20-21 (bit1-0 : EXIN) (Low level detect, detect edge selection)
External pin input (P0)	$P0_7$			IE12 (bit2 : IE1) (All of P0 pins enable / disable)	P0C7 (bit7 : P0C) $P0_7$ pin enable / disable
	$P0_6$				P0C6 (bit6 : P0C) $P0_6$ pin enable / disable
	$P0_5$				P0C5 (bit5 : P0C) $P0_5$ pin enable / disable
	$P0_4$				P0C4 (bit4 : P0C) $P0_4$ pin enable / disable
	$P0_3$				P0C3 (bit3 : P0C) $P0_3$ pin enable / disable
	$P0_2$				P0C2 (bit2 : P0C) $P0_2$ pin enable / disable
	$P0_1$				P0C1 (bit1 : P0C) $P0_1$ pin enable / disable
	$P0_0$				P0C0 (bit0 : P0C) $P0_0$ pin enable / disable
Watchdog timer overflow					WDTRN (bit6:WDTC) select the operation as an interrupt occurs
Illegal instruction trap					

Standby Function

The standby function is a function which temporarily stops program execution so as to conserve power. The standby mode is the chip enters temporary stop state from the operating state, executing program. It contains STOP mode and HALT which can selects it according to your desired.

If the CPU executes the STOP mode or HALT mode, the chip will switch to standby mode from an operating mode. If the wake up source of the standby mode, like as interrupt, encounters, the chip returns to operating mode from the standby mode. Fig. 11 shows its state transition diagram.

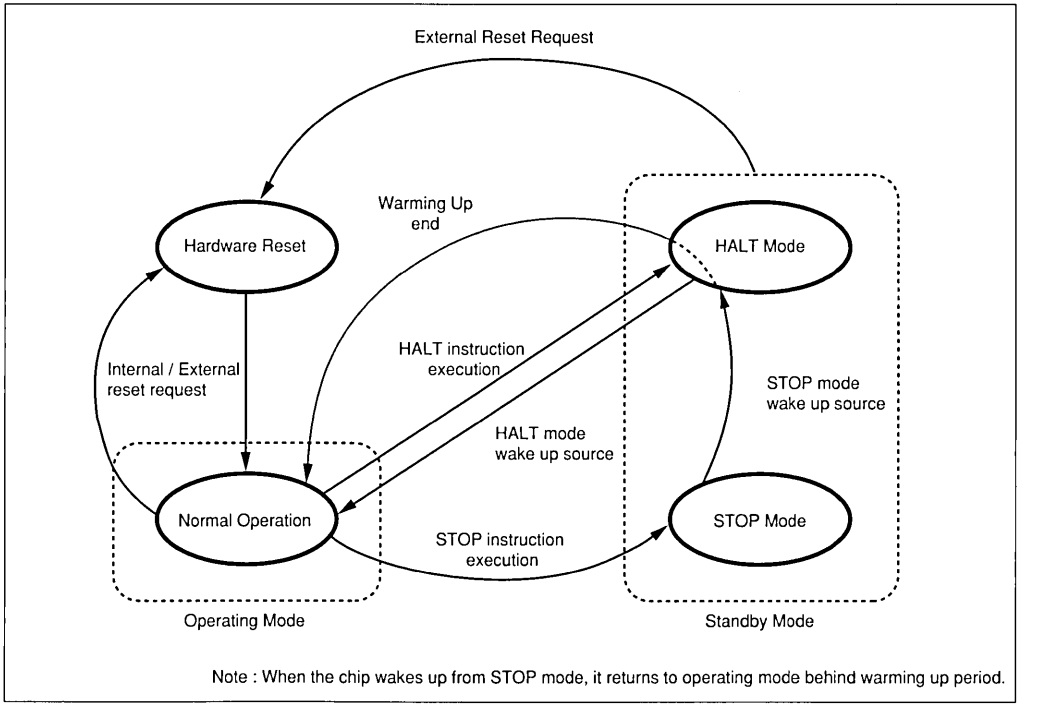


Fig. 11 State transition diagram

NOTE :

The STOP instruction also is used for clock change function, which its operation is different from switching the chip to STOP mode, please take care to use it.

Table 5 System state at standby mode

		HALT MODE	STOP MODE
Transition method		HALT instruction execution	STOP instruction execution
Wake up method		Hardware reset, interrupt	Hardware reset, interrupt *1
Function blocks	CPU	stop	stop
	Main-clock	operating	stop
	Sub-clock	operating	operating
	RAM, register	remain*2	remain*2
	I/O Port	remain	remain
	$P3_3$/$PINT_0$/CNT_0 sampling circuit	operating	stop
	Timer	operating	The timer used main-clock as counter clock is stop. It used external clock as counter clock can still operate.
	Capture trigger	operating	stop
	UART	operating	stop
	SIO	operating	If SIO transfer clock is set to T_{OUT1} and Timer1 counter clock was selected from external clock or sub-clock divider frequency clock (fx_S), it can still operate.
	A/D converter	operating	stop
	Waveform generator, D/A converter	operating	stop

*1 The interrupts used to wake up the chip from STOP mode only have the external interrupts and the internal interrupts generated by operatible Timer, and SIO.

*2 General registers , control registers, and the other memory content all are remained. But something will be changed for the operatable blocks at STOP mode (for example, interrupt flag register IF0, IF1 content, etc.)

About how to use HALT mode and STOP mode

Switches back to the operating mode from the HALT mode immediately after the wake up sources are encounter. For this reason, the HALT mode is suitable for the system need to immediately be waked up by key input frequently. And, all interrupt sources (other than illegal instruction trap) can wake up the chip from the HALT mode.

Switching back to the operating mode from the STOP mode after the wake up sources are encounter must pass a warming up period. In addition, the function blocks used by the main-clock cannot be used in the wake up from STOP mode. Since the sampling circuit is stopped, it do not accept the $PINT_0$ input, too.

For this reason, the STOP mode, conserving more power than the HALT mode, is suitable for the system that the program stop time is more long and the time, back to the operating mode (warming up period), is enough.

In standby mode, I/O ports setting and output level for output ports are remained.
Before switches to standby mode, in order to reduce to the current through every pins, please set with program.

I/O PORTS

The SM8500 supports two 8 bit input ports (Port 0, 4), two 8 bit large current output ports (Port6, A) , and six 8bit and one 4-bit input/output ports (Port 1, 2, 3, 5, 7, 8, 9).

Table 6 Ports function overview

PORTS	PIN	FUNCTION	RELATED CONTROL REGISTER
Port 0	$P0_0$-$P0_7$	8 bit input port Available to ON/OFF pull-up resistor in 8 bit unit Shared with external interrupt pins ($P0_0$-$P0_7$) $P0_0$, $P0_1$ pin serve as $\overline{RD}$ and $\overline{WR}$ pin, respectively, in external memory expansion mode.	P0 (0020H) P0C (0030H) PPC (003BH)
Port 1	$P1_0$-$P1_7$	8 bit I/O port (preventive buffer for through current) Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 1-bit unit, in input mode. $P1_0$-$P1_7$ pins serve as data bus in external memory expansion mode.	P1 (0021H) P1C (0031H) P1PC (0035H)
Port 2	$P2_0$-$P2_7$	8 bit I/O port (preventive buffer for through current) Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 1-bit unit, in input mode. $P2_0$-$P2_7$ pins serve as upper address bus (A_8-A_{15}) in external memory expansion mode.	P2 (0022H) P2C (0032H) P2PC (0036H)
Port 3	$P3_0/T_{OUT0}$ $P3_1/T_{OUT1}$ $P3_2/T_{OUT2}$ $P3_3/PINT_0/CNT_0$ $P3_4/CNT_1$ $P3_5/CNT_2$ $P3_6/PINT_1$ $P3_7/PINT_2$	8 bit I/O port Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 8 bit unit, in input mode. Shared with Timer output pins ($P3_0$-$P3_2$) Shared with external interrupt input/capture trigger input/ event counter input pin ($P3_3$) Shared with event counter pin ($P3_4$) Shared with external interrupt input pin ($P3_6$, $P3_7$)	EXIN (0014H) P3 (0023H) P3C (0033H) PPC (003BH) TM0C0 (0046H) TM0C1 (0047H) TM1C (004AH) TM2C (004DH) TM12CT (004EH)

Table 6 Ports function overview (cont'd)

PORTS	PIN	FUNCTION	RELATED CONTROL REGISTER
port 4	$P4_0$/AD_0-$P4_7$/AD_7	8 bit input port (preventive buffer for through current) Shared with analog input pins ($P4_0$-$P4_7$)	P4 (0024H) P4C (0034H)
port 5	$P5_0$-$P5_7$	8 bit I/O port Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 8bit unit, in input mode. $P5_0$-$P5_7$ pins serve as lower address bus (A_0-A_7) in external memory expansion mode.	P5 (0025H) P5C (003AH) PPC (003BH)
port 6	$P6_0$-$P6_7$	8 bit large current output port Available for corresponding to N-ch open drain by mask option.	P6 (0026H)
port 7	$P7_0$/RxD $P7_1$/TxD $P7_2$ $P7_3$/SIN $P7_4$/SOUT $P7_5$/SCK $P7_6$/F $P7_7$/PWM	8 bit I/O port Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 8 bit unit, in input mode. Shared with UART pin ($P7_0$, $P7_1$) Shared with SIO pin ($P7_3$, $P7_4$, $P7_5$) Shared with clock (Buzzer) output pin ($P7_6$) Shared with PWM pin ($P7_7$)	P7 (0027H) P7C (0037H) PPC (003BH) URTC (002EH) URTB (002FH) SRC (0015H) TM5C (005AH) TM3C (0052H) TM4C (0056H)
port 8	$P8_0$-$P8_7$	8bit I/O port Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 8 bit unit, in input mode.	P8 (0028H) P8C (0038H) PPC (003BH)
port 9	$P9_0$-$P9_3$	4-bit I/O port Available to set input/output in 1-bit unit Available to ON/OFF pull-up resistor in 4-bit unit, in input mode.	P9 (0029H) P9C (0039H) PPC (003BH)
Port A	PA_0-PA_7	8 bit large current output port Available for corresponding to N-ch open drain by mask option.	PA (002AH)

P0 (input) Register (P0)

P0 is an 8 bit read only register for reading input data from the port 0.

P0 Control Register (P0C)

P0 control register P0C is an 8 bit readable/writable register which enables/disables the P00-P07, shared to port 0, interrupts (KYINT).

P1 (input/output) Register (P1)

P1 is an 8 bit readable/writable register for reading input data from the port 1 and storing output data to the port 1.

P1 Control Register (P1C)

P1 control register is an 8 bit readable/writable register which controls the I/O of port 1 in 1-bit unit.

P1 Pull-up Setting Register (P1PC)

P1PC is an 8 bit readable/writable register which ON/OFF pull-up resistor of port 1 in 1-bit unit. This register setting is valid when the corresponding bit is set as input pin. (The pins which are set as output pins are in the pull-up resistor OFF state and regardless of this register setting.)

P2 (input/output) Register (P2)

P2 is an 8 bit readable/writable register for reading input data from the port 2 and storing output data to the port 2.

P2 Control Register (P2C)

P2 control register is an 8 bit readable/writable register which controls the I/O of port 2 in 1-bit unit.

P2 Pull-up Setting Register (P2PC)

P2PC is an 8 bit readable/writable register which ON/OFF pull-up resistor of port 2 in 1-bit unit. This register setting is valid when the corresponding bit is set as input pin. (The pins which are set as output pins are in the pull-up resistor OFF state and regardless of this register setting.)

P3 (input/output) Register (P3)

P3 is an 8 bit readable/writable register for reading input data from the port 3 and storing output data to the port 3.

P3 Control Register (P3C)

P3 control register is an 8 bit readable/writable register which controls the I/O of port 3 in 1-bit unit. When the port 3 is used as input/output for built-in peripheral functions (Timer, etc.), the I/O direction of the corresponding pins for using function must be set by this register.

External Interrupt Mode Register (EXIN)

The external interrupt mode register EXIN is an 8 bit readable/writable register which selects a valid edge of the external interrupts (PINT0-PINT2), and a sampling clock of the external interrupt (PINT0).

Bit 7 0

EXS00	EXS01	EX00	EX01	EX10	EX11	EX20	EX21

Bit 7-6 : PINT0/$P3_3$ Sampling clock selection bit

BIT	SAMPLING CLOCK
00	f_{c2} (1 382.4 kHz*)
01	f_{c6} (345.6 kHz*)
10	f_{c4} (86.4 kHz*)
11	f_{c8} (21.6 kHz*)

* : main-clock = 11.0592 MHz

Bit 5-4 : PINT0/$P3_3$ Valid edge selection bit

BIT	VALID EDGE
00	Invalid
01	rising edge detected
10	falling edge detected
11	both edge detected

Bit 3-2 : PINT1/$P3_6$ Valid edge selection bit

BIT	VALID EDGE
00	both edge detected
01	falling edge detected
10	rising edge detected
11	Low level detected

Bit 1-0 : PINT0/$P3_7$ Valid edge selection bit

BIT	VALID EDGE
00	both edge detected
01	falling edge detected
10	rising edge detected
11	Low level detected

P4 (input) Register (P4)

P4 is an 8 bit read only register for reading input data from the port4.

P4 Control Register (P4C)

P4 control register is an 8 bit readable/writable register which switches in 1-bit unit to analog pins (AD0-AD7), shared to port4, for A/D converter .

P5 (input/output) (P5)

P5 is an 8 bit readable/writable register for reading input data from the port5 and storing output data to the port5.

P5 Control Register (P5C)

P5 control register is an 8 bit readable/writable register which controls the I/O of port5 in 1-bit unit.

P6 (output) Register (P6)

P6 register is an 8 bit readable/writable register for storing the output data to the port6.

P7 (input/output) Register (P7)

P7 is an 8 bit readable/writable register for reading input data from the port7 and storing output data to the port7.

P7 Control Register (P7C)

P7 control register is an 8 bit readable/writable register which controls the I/O of port7 in 1-bit unit. When the port7 is used as input/output for built-in peripheral functions (SIO, etc.), the I/O direction of the corresponding pins for using function must be set by this register.

P8 (input/output) Register (P6)

P8 is an 8 bit readable/writable register for reading input data from the port8 and storing output data to the port8.

P8 Control Register (P8C)

P8 control register is an 8 bit readable/writable register which controls the I/O of port8 in 1-bit unit.

P9 (input/output) Register (P6)

P9 is a 4-bit readable/writable register for reading input data from the port4 and storing output data to the port4. The upper 4-bit do not exist. If the CPU reads this register, these bits will be read with '1'.

P9 Control Register (P9C)

P9 control register is a 4-bit readable/writable register which controls the I/O of port9 in 1-bit unit. The upper 4-bit do not exist. If the CPU reads this register, these bits will be read with '1'.

PA (output) Register (PA)

PA is an 8 bit readable/writable register for storing output data to the portA.

Port Pull-up Setting Register (PPC)

PPC is an 8 bit readable/writable register which ON/OFF pull-up resistor of P0, P3, P5, P7, P8, P9 in port unit. This register setting is valid when the corresponding bit is set as input pin. (The pins which are set as output pins are in the pull-up resistor OFF state and regardless of this register setting.)

TIMER / COUNTERS

The SM8500 supports five 8 bit timer/event counter clock timer port, and one 8 bit watchdog timer port. ports, one 16-bit timer/event counter port, one 8bit

Table 7 Timer function overview

Timer No.	Up counter		Select clock or count clock		Timer output		Interrupt source	Others
	Free-run operation*1	Compare operation*2	Internal clock	External clock	Square wave output	PWM output		
TIM0 (16bit timer/counter)	O	O	fc_1 , fc_2 , fc_3 , fx_5	$P3_3/PINT_0/CNT_0$ (rising edge, fallingedge, both edge)	O ($P3_0/T_{OUT0}$)	O ($P3_0/T_{OUT0}$) (Duty variable)	. Timer match *3 . Capture trigger input	. with input capture function . counter stopped function (counter cleared)
TIM1 (8bit timer/counter)	O	O	fc_1 , fc_2 , fc_3 , fc_4 , fc_5 , fc_6 , fc_7 , fx_5	$P3_4/CNT_1$ (rising edge, fallingedge)	O ($P3_1/T_{OUT1}$)	O ($P3_1/T_{OUT1}$) (Duty variable)	. Timer match	. counter stopped function (counter cleared)
TIM2 (8bit timer/counter)	O	O	fc_1 , fc_2 , fc_3 , fc_4 , fc_5 , fc_6 , fc_7 , fx_5	$P3_5/CNT_2$ (rising edge, fallingedge)	O ($P3_2/T_{OUT2}$)	O ($P3_2/T_{OUT2}$) (Duty variable)	. Timer match	. counter stopped function (counter cleared)
TIM3 (8bit timer/counter)	O	O	fc_1 , fc_2 , fc_3 , fc_4 , fc_5 , fc_6 , fc_7 , fx_5	-	O ($P7_7$/PWM)	O ($P7_7$/PWM) (Period or Duty variable)	. Timer match	. Combining timer3 and timer4 is used as 16bit Timer. . counter stopped function (counter cleared)
TIM4 (8bit timer/counter)			fc_4 , fc_5 , fc_6 , fc_7 , fc_8 , fc_9 , fx_5 , TIM3 overflow					
TIM5 (8bit timer/counter)	O	O	fc_3 , fc_4 , fc_5 , fc_6 , fc_7 , fc_8 , fc_9 , fx_5	-	O ($P7_6$/F) (Buzzer output)	-	. Timer match	. counter stopped function (counter cleared)
TIM6 (8bit Clock timer)	O	-	fc_7 , fc_8 , fc_9 , fc_{10}, fx_5 , fx_6 , fx_7 , fx_8	-	-	-	. Counter overflow (seventh step / eighth step overflow can be selected)	. counter stopped function (counter cleared) . clearable in counter operating
WDT (8bit Watchdog timer)	O	-	fc_{12} , fc_{13} , fc_{14} , fc_{15} , fx_5 , fx_6 , fx_7 , fx_8	-	-	-	. Counter overflow (hardware reset / non-maskable interrupt can be selected)	. counter stopped function (counter cleared) . clearable in counter operating

*1 Counter cleared by counter overflow *2 Counter cleared by matching with the modular register *3 when counter matches with the modular register

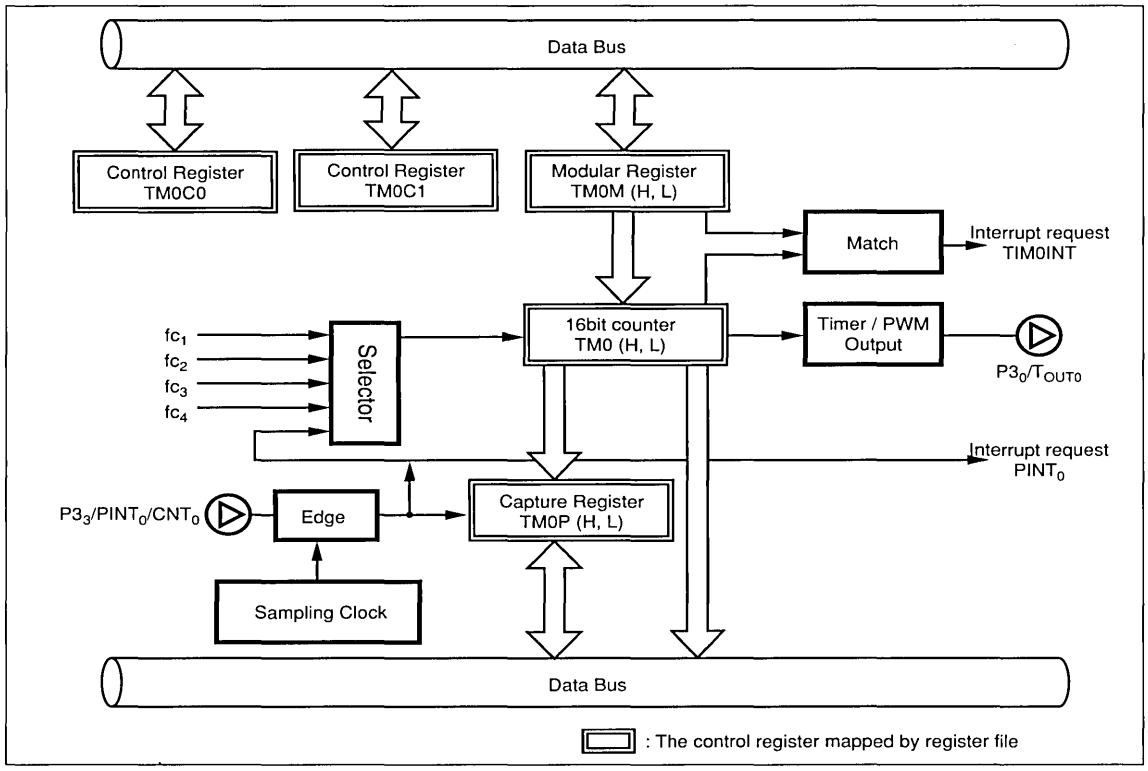


Fig. 12 Timer 0 (TIM0) block diagram

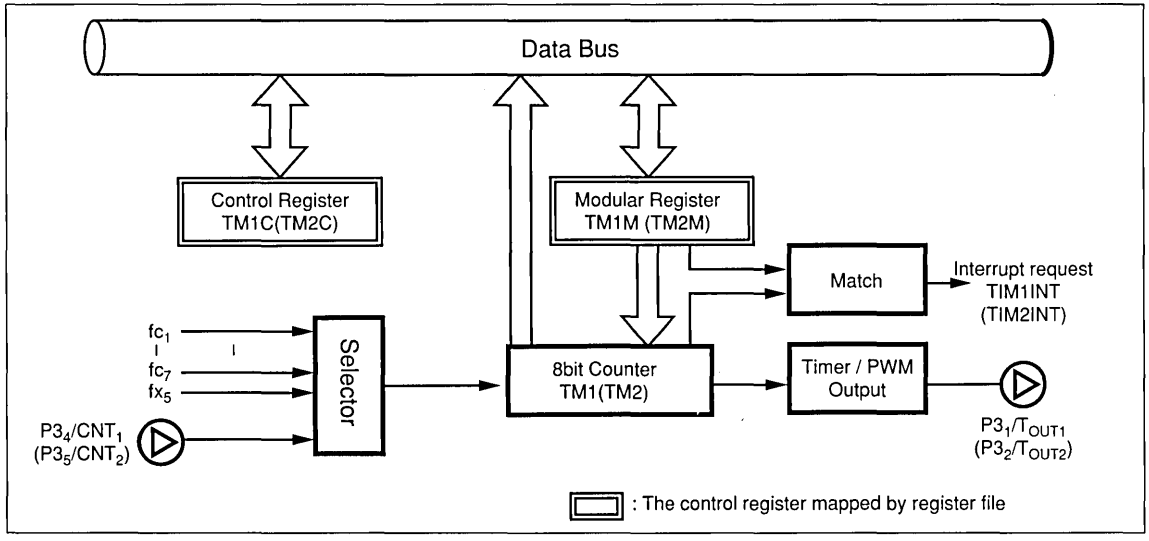


Fig. 13 Timer 1, 2 (TIM1, TIM2) block diagram

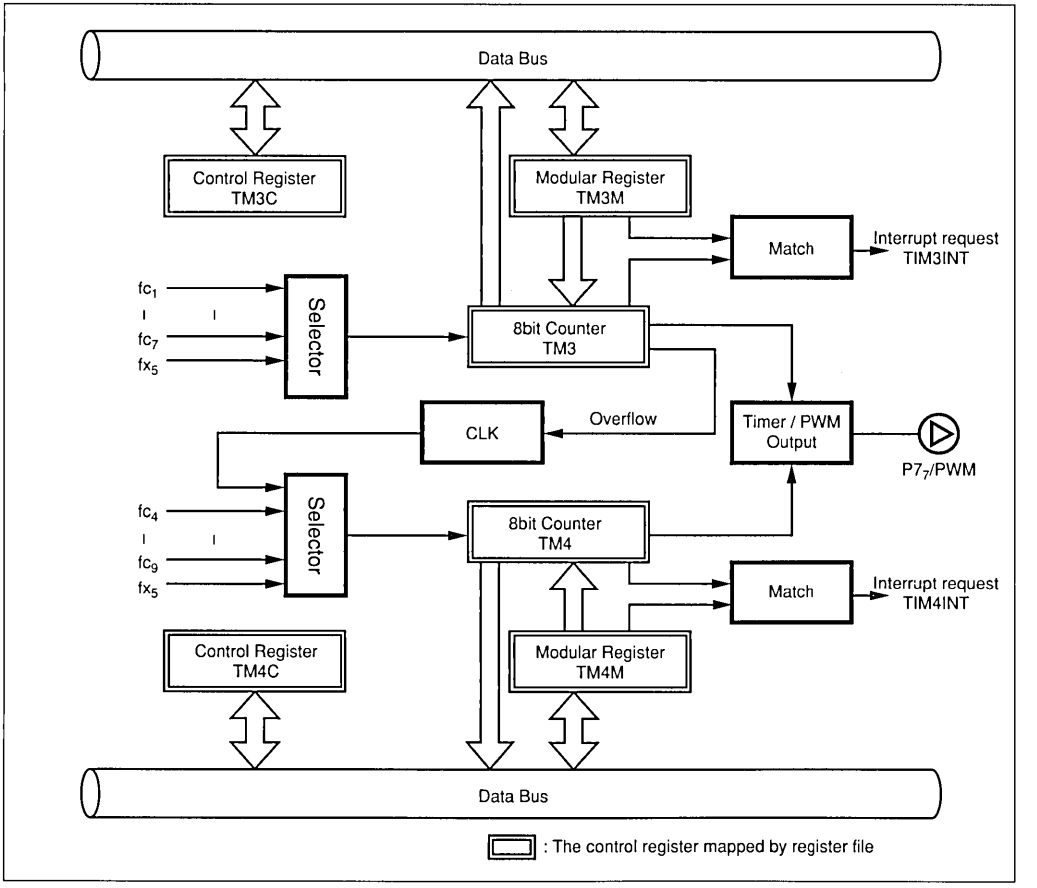


Fig. 14 Timer 3, 4 (TIM3, TIM4) block diagram

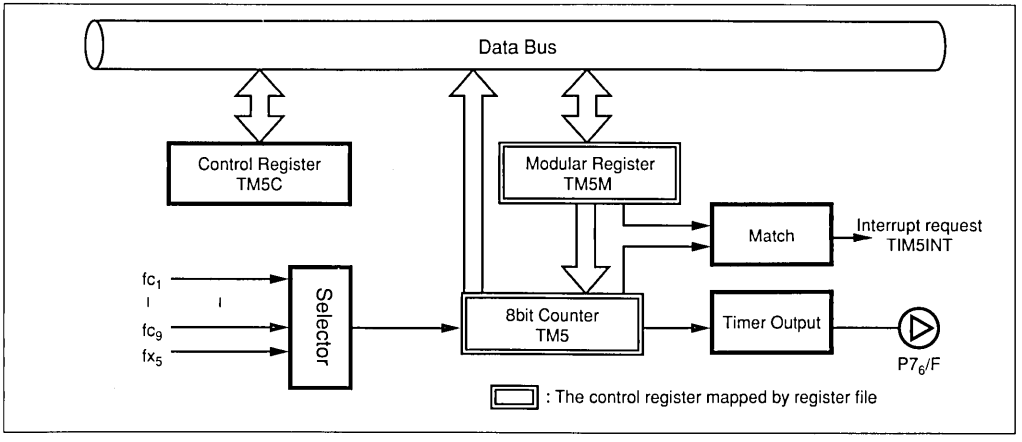


Fig. 15 Timer 5 (TIM5) block diagram

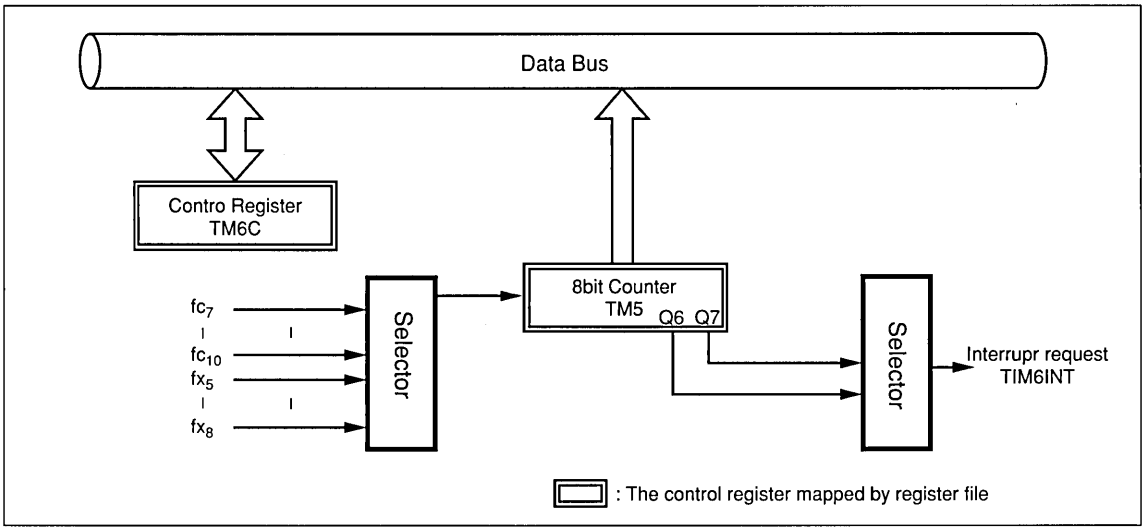


Fig. 16 Clock timer (TIM6) block diagram

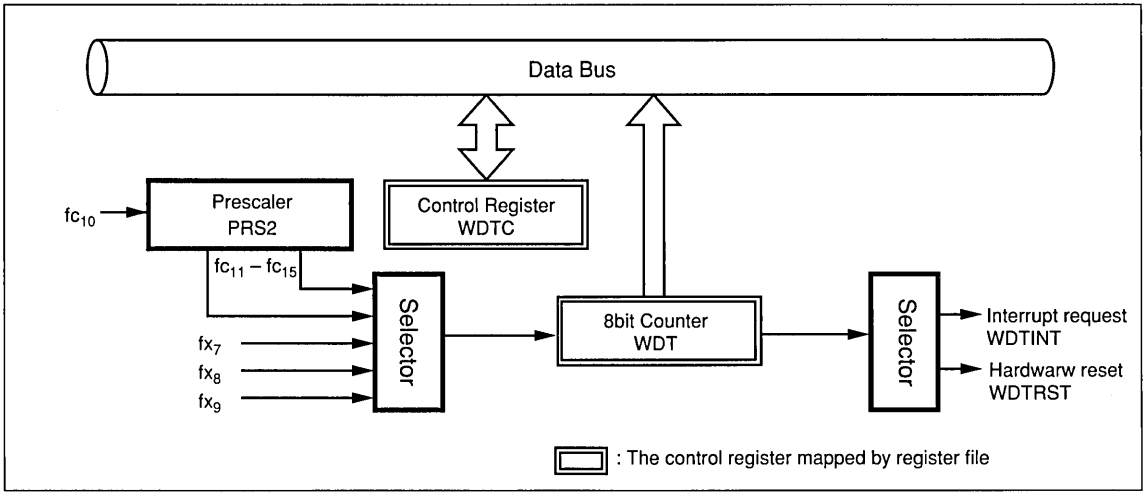


Fig. 17 Watchdog timer (WDT) block diagram

Relative Register Summary

TIMER NO.	ADDRESS	NAME	SYMBOL		R/W	INITIAL
TIM0	0040H	Timer 0 counter register H	TM0H	TM0	R	00H
	0041H	Timer 0 counter register L	TM0L		R	00H
	0042H	Timer 0 modular register H	TM0MH	TM0M	R/W	FFH
	0043H	Timer 0 modular register L	TM0ML		R/W	FFH
	0044H	Timer 0 capture register H	TM0PH	TM0P	R	00H
	0045H	Timer 0 capture register L	TM0PL		R	00H
	0046H	Timer 0 control register 0	TM0C0		R/W	C0H
	0047H	Timer 0 control register 1	TM0C1		R/W	1FH
TIM1	0048H	Timer 1 counter register	TM1		R	00H
	0049H	Timer 1 modular register	TM1M		R/W	FFH
	004AH	Timer 1 control register	TM1C		R/W	07H
TIM2	004BH	Timer 2 counter register	TM2		R	00H
	004CH	Timer 2 modular register	TM2M		R/W	FFH
	004DH	Timer 2 control register	TM2C		R/W	07H
TIM1, 2	004EH	Timer 1/2 clock selection register	TM12CT		R/W	00H
TIM3	0051H	Timer 3 counter register	TM3		R	00H
	0055H	Timer 3 modular register	TM3M		R/W	FFH
	0052H	Timer 3 control register	TM3C		R/W	00H
TIM4	0050H	Timer 4 counter register	TM4		R	00H
	0054H	Timer 4 modular register	TM4M		R/W	FFH
	0056H	Timer 4 control register	TM4C		R/W	00H
TIM5	0058H	Timer 5 counter register	TM5		R	00H
	0059H	Timer 5 modular register	TM5M		R/W	FFH
	005AH	Timer 5 control register	TM5C		R/W	10H
TIM6	005CH	Timer 6 counter register	TM6		R	00H
(use for clock)	005DH	Timer 6 control register	TM6C		R/W	38H
WDT	005EH	Watchdog timer counter register	WDT		R	00H
	005FH	Watchdog timer control register	WDTC		R/W	38H

Timer 0 (TIM0) Register Explanation

Timer 0 counter register TM0 (TM0H, TM0L)

Counter TM0 is a 16-bit read only register and counts up by input clock.

Timer 0 modular register (TM0ML, H)

Modular register TM0M is a 16bit readable/writable register. A necessary value, corresponding to timer0 operation, is set to the register.

An interrupt will occur if the counter TM0 matches with the value of modular register TM0M.

TM0MH : 00H-FFH

TM0ML : 01H-FFH

Timer 0 capture register (TM0PL, H)

Capture register TM0P is a 16-bit read only register. It captures the content of counter TM0 from the external trigger input ($P3_3$/$PINT_0$/CNT_0). The bits EX00-EX01 (bit 5-4 : EXIN) of external interrupt mode register EXIN can set the valid edge of $P3_3$/$PINT_0$/CNT_0 pin. (Refer to [External Interrupt Mode Register EXIN]).

Timer 0 control register (TM0C0)

Control register TM0C0 is an 8bit readable/writable register which selects the operating mode and count clock of timer0.

Control register TM0C0 is initializated to C0H after hardware reset.

Bit 7 0

-	-	TM0D2	TM0D1	TM0D0	CNT02	CNT01	CNT00

Bit 5-3 : Timer 0 operating mode selection bits (TM0D2-TM0D0)

BIT	OPERATING MODE	COUNTER OPERATION
000	Interval timer/counter	Compare operation
001		Free-run operation
010	PWM (Start : Low level)	Free-run operation
011	PWM (Start : High level)	Free-run operation
100	Pulse width measured	Compare operation
101		Free-run operation
110-111	Not to use.	-

Bit 2-0 : Timer count clock selection bits (CNT02-CNT00)

BIT	COUNT CLOCK
000	fc_1 (0.362 µs*1)
001	fc_2 (0.723 µs*1)
010	fc_3 (1.447 µs*1)
011	fx_5 (0.975 ms*2)
100	valid edge of $P3_3$/$PINT_0$/CNT_0 input pin
101-111	Not to use.

*1 The value in ( ) is the period when main-clock is 11.059 MHz.

*2 The value in ( ) is the period when sub-clock is 32.768 KHz.

Timer 0 control register 1 (TM0C1)

Control register TM0C1 is an 8 bit readable/writable register which sets the timer0 to start/stop, timer output or not, and indicates the counter overflow state.

Control register TM0C1 is initializated to 1FH after hardware reset.

Bit 7 0

TM0ST	TM0OV	TM0OE	-	-	-	-	-

Bit 7 : Timer 0 start/stop bit (TM0ST)

BIT	CONTENT
0	stop (counter cleared)
1	start

Bit 6 : Timer 0 overflow flag (TM0OV)

BIT	CONTENT
0	no overflow
1	overflows

Bit 5 : Timer 0 output control bit (TM0OE)

BIT	CONTENT
0	disable output
1	enable output

Timer 1, 2 (TIM1, TIM2) Register Explanation

Timer 1, 2 (TIM1, TIM2) have the same function.

Timer 1, 2 counter register (TM1, TM2)

Counters1, 2 (TM1, TM2) are 8 bit read only registers, respectively, which count up from input clock.

Timer 1, 2 modular register (TM1M, TM2M)

Modular registers TM1M, TM2M are 8 bit read only registers respectively which set the necessary value, corresponding to timer 1, 2 operation.

An interrupt will generate while the value of counter TM1 (TM2) matches with modular register's TM1M (TM2M).

Modular register is set during the timer count stopping.

The setting value of modular register is in the following range.

TM1M, TM2M = 01H-FFH

Timer 1/2 clock selection register (TM12CT)

Clock selection register TM12CT is an 8bit readable/ writable register which both select count clock of timer 1 and timer 2.

Bit 7 0

CNT23	CNT22	CNT21	CNT20	CNT13	CNT12	CNT11	CNT10

Bit 7-4 : Timer 2 count clock selection bits (CNT23-CNT20)

Bit 3-0 : Timer 1 count clock selection bits (CNT13-CNT10)

BIT	COUNT CLOCK
0000	fc_1 (0.362 μs*1)
0001	fc_2 (0.723 μs*1)
0010	fc_3 (1.447 μs*1)
0011	fc_4 (2.894 μs*1)
0100	fc_5 (5.787 μs*1)
0101	fc_6 (11.57 μs*1)
0110	fc_7 (23.15 μs*1)
0111	fx_5 (0.975 ms*2)
1000	rising edge of external input pin*3
1001	falling edge of external input pin*3
1010-1111	Not to use.

*1 The value in ( ) is the period when the main-clock is 11.0592 MHz.

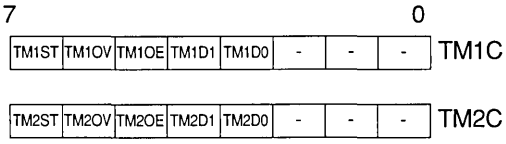
*2 The value in ( ) is the period when the main-clock is 32.768 kHz.

*3 For an external clock, the is input from $P3_4/CNT_1$ pin and timer2 is input from $P3_5/CNT_2$.

Timer 1, 2 control register (TM1C, TM2C)

Control registers TM1C, TM2C are 8 bit readable/writable registers respectively which set the timers 1, 2 to start/stop, timer output or not, and indicates the counter overflow state.

Control registers TM1C, TM2C are initializated to 07H respectively after hardware reset.



Bit 7 (TM1C) : Timer 1 start/stop (TM1ST)
Bit 7 (TM2C) : Timer 2 start/stop (TM2ST)

BIT	CONTENT
0	Timer stop [Counter TM1 (TM2) is cleared.]
1	Timer start

Bit 6 (TM1C) : Timer 1 overflow flag (TM1OV)
Bit 6 (TM2C) : Timer 1 overflow flag (TM2OV)

BIT	CONTENT
0	No overflow
1	Overflow

Bit 5 (TM1C) : Timer 1 output control (TM1OE)
Bit 5 (TM2C) : Timer 2 output control (TM2OE)

BIT	CONTENT
0	Timer output disable [The content of P31 (bit 1 : P3) is output from $P3_1/T_{OUT1}$ pin]. [The content of P32 (bit 2 : P3) is output from $P3_2/T_{OUT2}$ pin]
1	Timer output enable [Waveform set by timer operating mode is output]

Bit 4-3 (TM1C) : Timer 1 operating mode selection bits (TM1D1-TM1D0)
Bit 4-3 (TM2C) : Timer 2 operating mode selection bits (TM2D1-TM2D0)

BIT	OPERATING MODE	COUNTER
00	Interval timer/counter	Compare operation
01		Free-run operation
10	PWM (Start : Low level)	Free-run operation
11	PWM (Start : High level)	Free-run operation

Timer 3, 4 (TIM3, TIM4) Register Explanation

Timer 3, 4 (TIM3, TIM4) can be combinated to serve as 16 bit timer/counter except that is used as two 8 bit independent timer/counter. And, by using the combination which timer 3, 4 counters match with modular registers, it can output the PWM wave which its period and duty are variable.

Timer 3, 4 counter register (TM3, TM4)

Counter registers TM3, 4 (TM3, TM4) are 8 bit read only registers, respectively, which count up from input clock. When they are used as 16 bit timer, the counter TM3 is the lower 8-bits and TM4 is the upper 8-bits for 16-bit counter register.

Timer 3, 4 modular register (TM3M, TM4M)

Modular registers TM3M, TM4M are 8 bit read only registers, respectively, which set the necessary value, corresponding to timer 3, 4 operation.

An interrupt will generate while the value of counter TM3 (TM4) matches with modular register's TM3M (TM4M).

Modular register is set during the timer count stopping.

Timer 3, 4 control register (TM3C, TM4C)

Control registers TM3C , TM4C are 8 bit readable/writable register respectively which set the timer 3, 4 to start/stop, timer output or not, select the count clock, and indicate the counter overflow state.

Bit 7 0

TM3ST	TM3OV	TM3OE	TM3D1	TM3D0	CNT32	CNT31	CNT30	TM3C

TM4ST	TM4OV	TM4OE	TM4D1	TM4D0	CNT42	CNT41	CNT40	TM4C

Bit 7 (TM3C) : Timer 3 start/stop bit (TM3ST)
Bit 7 (TM4C) : Timer 4 start/stop bit (TM4ST)

BIT	CONTENT
0	Timer stop [Counter TM3 (TM4) is cleared.]
1	Timer start

Bit 6 (TM3C) : Timer 3 overflow flag (TM3OV)
Bit 6 (TM4C) : Timer 4 overflow flag (TM4OV)

BIT	CONTENT
0	No overflow
1	Overflow

Bit 5 (TM3C) : Timer 3 output control bit (TM3OE)
Bit 5 (TM4C) : Timer 4 output control bit (TM4OE)

TM4OE	TM3OE	CONTENT
0	0	Timer output disable [The content of bit P77 (bit : 7 : P7) is output]
0 (1)	1 (0)	Timer output enable (square wave output signal generated by reversing while timer 3 (4) modular register match with its counter)
1	1	Timer output enable (PWM signal by timer 3, 4)

Bit 4-3 (TM3C) : Timer 3 operating mode selection bits (TM3D1-TM3D0)
Bit 4-3 (TM4C) : Timer 4 operating mode selection bits (TM4D1-TM4D0)

BIT	OPERATING MODE	COUNTER
00	Interval timer/counter	Compare operation
01		Free-run operation
10	PWM (start : Low level)	Compare operation
11	PWM (start : High level)	Compare operation

Bit 2-0 (TM3C) : Timer 3 count clock selection bits (CNT32-CNT30)

BIT	COUNT CLOCK
000	fc_1 (0.362 μs*1)
001	fc_2 (0.723 μs*1)
010	fc_3 (1.447 μs*1)
011	fc_4 (2.894 μs*1)
100	fc_5 (5.787 μs*1)
101	fc_6 (11.57 μs*1)
110	fc_7 (23.15 μs*1)
111	fx_5 (0.975 ms*2)

*1 The value in ( ) is the period when main-clock is 11.0592 MHz.
*2 The value in ( ) is the period when main-clock is 32.768 kHz.

Bit 2-0 (TM4C) : Timer 4 count clock selection bits (CNT42-CNT40)

BIT	COUNT CLOCK
000	fc_4 (2.894 μs*1)
001	fc_5 (5.787 μs*1)
010	fc_6 (11.57 μs*1)
011	fc_7 (23.15 μs*1)
100	fc_8 (46.03 μs*1)
101	fc9 (92.59 μs*1)
110	fx_5 (0.975 ms*2)
111	Timer 3 overflow

*1 The value in ( ) is the period when main-clock is 11.0592 MHz.
*2 The value in ( ) is the period when main-clock is 32.768 kHz.

Timer 5 (TIM5) Register Explanation

Timer 5 counter register (TM5)

Counter TM5 is an 8 bit read only register which counts up from input clock.

Timer 5 modular register (TM5M)

Modular register TM5M is an 8 bit readable/writable which sets the interval time of timer5.
An interrupt will generate while the value of counter TM5 matches with modular register's TM5M.
Modular register is set during the timer count stopping.

Timer control register (TM5C)

Control register TM5 is an 8 bit readable/writable register which sets the timer5 to start/stop, timer output or not, selects the count clock, and indicates the counter overflow state.

Bit 7 0

TM5ST	TM5OV	TM5OE	-	TM5D0	CNT52	CNT51	CNT50

Bit 7 : Timer 5 start/stop bit (TM5ST)

BIT	CONTENT
0	Timer stop (Counter TM5 is cleared)
1	Timer start

Bit 6 : Timer 5 overflow flag (TM5OV)

BIT	CONTENT
0	No overflow
1	Overflow

Bit 5 : Timer 5 output control bit (TM5OE)

BIT	CONTENT
0	Timer output disable [The content of P76 (bit6 : P7) is output]
1	Timer output enable

Bit 3 : Timer 5 operating mode selection bit (TM5D0)

BIT	OPERATING MODE	COUNTER
0	Interval timer/counter	Compare operation
1		Free-run operation

Bit 2-0 : Timer 5 count clock selection bits (CNT52-CNT50)

BIT	COUNT CLOCK
000	fc_3 (1.447 μs*1)
001	fc_4 (2.894 μs*1)
010	fc_5 (5.787 μs*1)
011	fc_6 (11.57 μs*1)
100	fc_7 (23.15 μs*1)
101	fc_8 (46.30 μs*1)
110	fc_9 (92.59 μs*1)
111	fx_5 (0.975 ms*2)

*1 The value in ( ) is the period when main-clock is 11.0592 MHz.

*2 The value in ( ) is the period when main-clock is 32.768 kHz.

Timer 6 (TIM6) [Clock Timer] Register Explanation

Timer 6 counter register (TM6)

Counter TM6 is an 8 bit read only register which counts up from input clock.

Timer 6 control register (TM6C)

Control register TM6 is an 8 bit readable/writable register which sets the timer 6 to start/stop, counter step number of interrupt, counter clear designation, and selects the count clock.

Bit 7 0

TM6ST	TM6OV	-	-	TM6CR	CNT62	CNT61	CNT60

Bit 7 : Timer 6 start/stop bit (TM6ST)

0 | Timer stop (Counter TM6 is cleared)

1 | Timer start

Bit 6 : Counter step number of interrupt selection bit (TM6OV)

0 | Interrupt occurs at counter the eighth step overflow.

1 | Interrupt occurs at counter the seventh step overflow.

Bit 3 : Counter clear bit (TM6CR) [Write only bit]

0 | No clear.

1 | Counter TM6 is cleared only in writting operation.

Bit 2-0 : Timer 6 count clock selection bits (CNT62-CNT60)

BIT	COUNT CLOCK
000	fc_7 (23.15 μs*1)
001	fc_8 (46.30 μs*1)
010	fc_9 (92.59 μs*1)
011	fc_{10} (185.2μs*1)
100	fx_5 (0.975 ms*2)
101	fx_6 (1.95 ms*2)
110	fx_7 (3.91 ms*2)
111	fx_8 (7.81 ms*2)

*1 The value in ( ) is the period when main-clock is 11.0592 MHz.

*2 The value in ( ) is the period when main-clock is 32.768 kHz.

Watchdog Timer (WDT) Register Explanation

Prescaler 2 (PRS2)

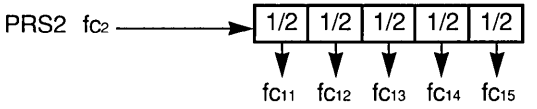
Prescaler PRS2 generates the count clock to watchdog timer counter WDT.

The following conditions is to clear all bits of prescaler PRS2.

When hardware reset.

When watchdog timer counter WDT stopped.

When counter WDT is cleared by writting '1' to the bit WDTCR (bit3 : WDTC).



Prescaler PRS2 divides the frequency derived from input clock fc10 (185.3 ms : main-clock = 11.0592 MHz) then fc_{11}-fc_{15} is output.

Watchdog timer counter register (WDT)

Watchdog timer counter WDT is an 8 bit read only register which count up from input clock.

Watchdog timer control register (WDTC)

Watchdog timer control WDTC is an 8 bit read only register which sets watchdog timer to start/stop, counter clear designation, and selects the count clock.

Bit 7 0

WDTST	WDTRN	-	-	WDTCR	WCNT2	WCNT1	WCNT0

Bit 7 : Watchdog timer start/stop bit (WDTST)

0 | Timer stop [Counter WDT is cleared]

1 | Timer start

Bit 6 : Operation select while watchdog timer overflow (WDTRN)

0 | Hardware reset.

1 | Non-maskable interrupt.

Bit 3 : Counter clear bit (WDTCR) [write only bit]

0 | No clear.

1 | Only in writting operation, counter WDT is cleared.

Bit 2-0 : Watchdog timer counter clock selection bits (WCNT2-WCNT0)

BIT	COUNT CLOCK
000	fc_{12} (740.7 μs*1)
001	fc_{13} (1.481 ms*1)
010	fc_{14} (2.963 ms*1)
011	fc_{15} (5.926 ms*1)
100	fx_5 (0.975 ms*2)
101	fx_6 (1.95 ms*2)
110	fx_7 (3.91 ms*2)
111	fx_8 (7.81 ms*2)

*1 The value in ( ) is the period when main-clock is 11.0592 MHz.

*2 The value in ( ) is the period when main-clock is 32.768 kHz.

OPERATING EXPLANATIONS OF TIMER / COUNTERS

Free-run Operation and Compare Operation

Timer 0-5 (TIM0-TIM5) can select to operate in a free-run operation or compare operation.

Input Capture Function

Timer 0 (TIM0), which the edge detected of external input pin ($P3_3$/$PINT_0$/CNT_0) serves as a trigger, can capture the content of counter TM0 to the capture register TM0P. Based on this function, it is easy to measure the pulse width. Fig. 19 shows the input capture timing.

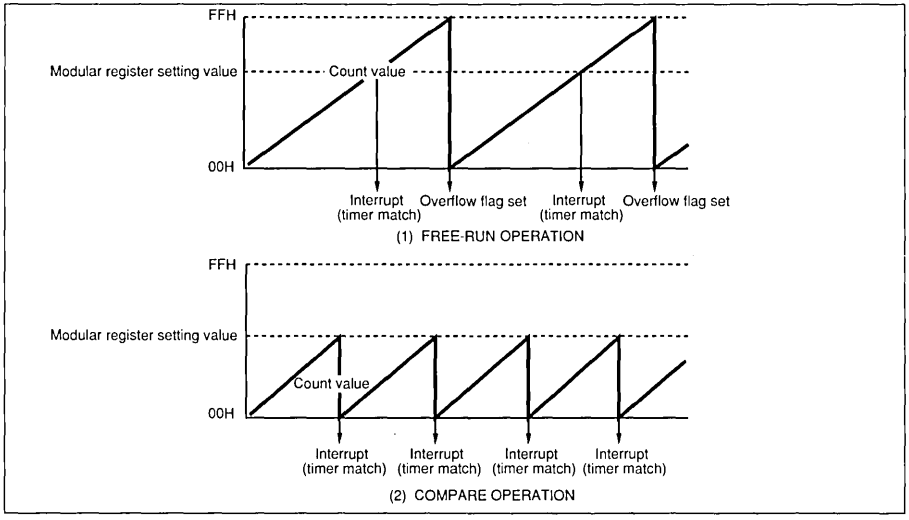


Fig.18 Free-run operation and Compare operation

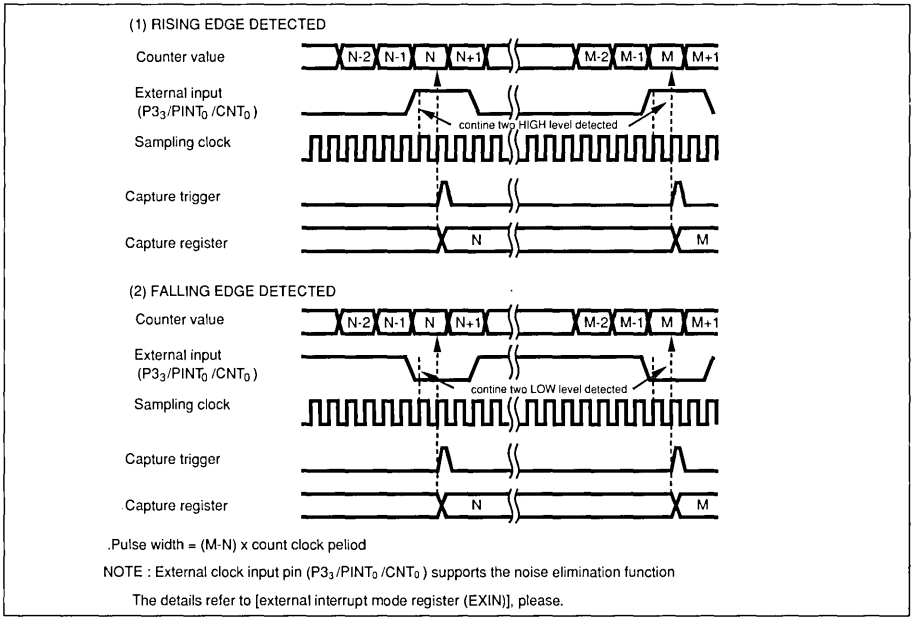


Fig.19 Input capture timing

Square Wave Output Operation (Timer output)

Timer 0-5 (TIM0-TIM5) can output the wave with duty variable and duty 50% by reversing the output while the counter's value matches with modular register. In this manual, they are named as [square wave output] or [timer output]. In partically, the square wave output of timer5 is named as [buzzer output].

PWM Output Operation

Timer 0-2 (TIM0-TIM2) can output PWM wave with the duty variable. Combinating with timer 3-4 (TIM3-TIM4) can output PWM wave with the duty and period variable.

PWM output operation with duty variable

The output level mutually changes while the counter value matches with modular register and the counter overflows. Since the counter is free-run operation, the wave will be the 2^8 (2^{16} for 16-bit timer) x count clock period. Modular register sets a High level or Low level interval of the wave.

PWM output operation with period and duty variable

The PWM output with period and duty variable is to use timer 3 and timer 4 simultaneously. Timer 4 sets the period and timer 3 sets the duty. Since the counters of timer 3, 4 are together cleared matched with modular register, the timer 4 match period is the period of PWM wave and the timer 3 match period). Control register TM3C and TM4C is used to process the controls.

Timer Connection (timer/counter 3, 4)

If selects the overflow of counter TM3 to serve as the count clock of counter TM4, the connection of timer 3, 4 will be a 16 bit timer/counter.

For 16-bit timer, an interrupt is generated by timer 4 interrupt request while both counter TM3 and counter TM4 timer match are valid. (But, timer 3 interrupt request also occurs while counter TM3 timer match.)

Watchdog Timer Operation

Watchdog timer is used to detect the program runaway. Starts the counter and counting up for every input clock. When the counter overflows, hardware resets or a non-maskable interrupt occurs. Thus, the counter is cleared periodly by program before overflows. Table 8 shows watchdog timer overflow period.

Table 8 Watchdog timer overflow period

COUNT CLOCK SELECTION				OVERFLOW PERIOD
BIT 2-0 : WDTC			COUNT PERIOD	
WCNT2	WCNT1	WCNT0		
0	0	0	fc_{12} (741.2 µs)	189.7 ms
0	0	1	fc_{13} (1.482 ms)	379.4 ms
0	1	0	fc_{14} (2.965 ms)	759.0 ms
0	1	1	fc_{15} (5.930 ms)	1 518 ms
1	0	0	fx_5 (0.975 ms)	250 ms
1	0	1	fx_6 (1.95 ms)	500 ms
1	1	0	fx_7 (3.91 ms)	1.00 s
1	1	1	fx_8 (7.81 ms)	2.00 s

NOTE :

The numerical value is in main-clock = 11.0592 MHz, sub-clock = 32.768 kHz.

Relation Between System Clock (CPU clock) and Timer Count Clock

The internal clock input to counters TM0-TM6 and WDT are selected from fc_1-fc_{10} which prescaler PRS0 divided the clock frequency derived from main-clock, fx_1-fx_8 which prescaler PRS1 divided the clock frequency derived from sub-clock, and fc_{11}-fc_{15} which prescaler PRS2 divided the clock frequency derived from fc_{10}. These clock periods don't be affected when changes system clock (CPU clock) by the clock change register CKKC, and are determined by the oscillation frequencies of main-clock and sub-clock.

Counters TM0-TM6 and WDT are counted up from the input falling edge of internal clock. Since an interrupt is accept at the rising edge of system clock (CPU clock), when system clock is low speed, timer continuously counts during the interval from modular register matched to interrupt occurred. (Refer to Fig. 20)

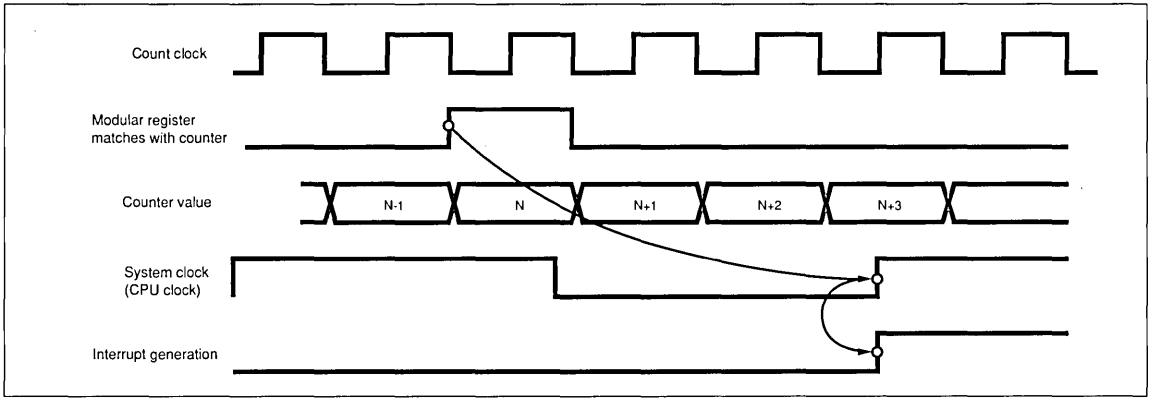


Fig. 20 The relation of system clock (CPU clock) and timer count clock

INTERRUPT

Table 9 shows the timer/counter interrupt sources.

Table 9 Timer/counter interrupt sources summary

TIMER NO.	INTERRUPT SOURCES	SYMBOL	VECTOR ADDRESS	INTERRUPT REQUEST FLAG	INTERRUPT ENABLE FLAG	PRIORITY LEVEL
TIM0	capture trigger input	PINT0	1000H	bit 7 : IF0	bit 7 : IE0	1
	counter match with modular register	TIM0INT	1004H	bit 5 : IF0	bit 5 : IE0	3
TIM1	counter match with modular register	TIM1INT	1006H	bit 6 : IF0	bit 6 : IE0	4
TIM2	counter match with modular register	TIM2INT	100CH	bit 1 : IF0	bit 1 : IE0	7
TIM3	counter match with modular register	TIM3INT	100EH	bit 0 : IF0	bit 0 : IE0	8
TIM4	counter match with modular register	TIM4INT	1010H	bit 7 : IF1	bit 7 : IE1	9
TIM5	counter match with modular register	TIM5INT	1012H	bit 6 : IF1	bit 6 : IE1	10
TIM6	counter overflow	TIM6INT	1014H	bit 5 : IF1	bit 5 : IE1	11
WD1	counter overflow	WDTINT	101CH	-	-	-

A/D CONVERTER

SM8500 has a built-in A/D converter with the features shown as below.

- **Conversion resolution : 10-bit**

- **Analog input channel : 8 channels ($P4_0/AD_0$-$P4_7/AD_7$ pins)**

  $P4_0/AD_0$-$P4_7/AD_7$ pins are able to switch to Port input pin (digital input pin) or A/D input pin (analog input pin) by control register P4C in 1-bit unit.

- **Two conversion modes**

  A/D conversion mode : It converts the analog input voltage into the digital value by sequential comparison type.

  Comparison mode : It compares the analog input voltage with the voltage value preset by user and stores the result of the comparison.

- **Conversion speed**

  A/D conversion mode :

  main-clock period x 488 (44.1 µs : main-clock = 11.0592 MHz)

  Comparison mode :

  main-clock period x 200 (18.1 µs : main-clock = 11.0592 MHz)

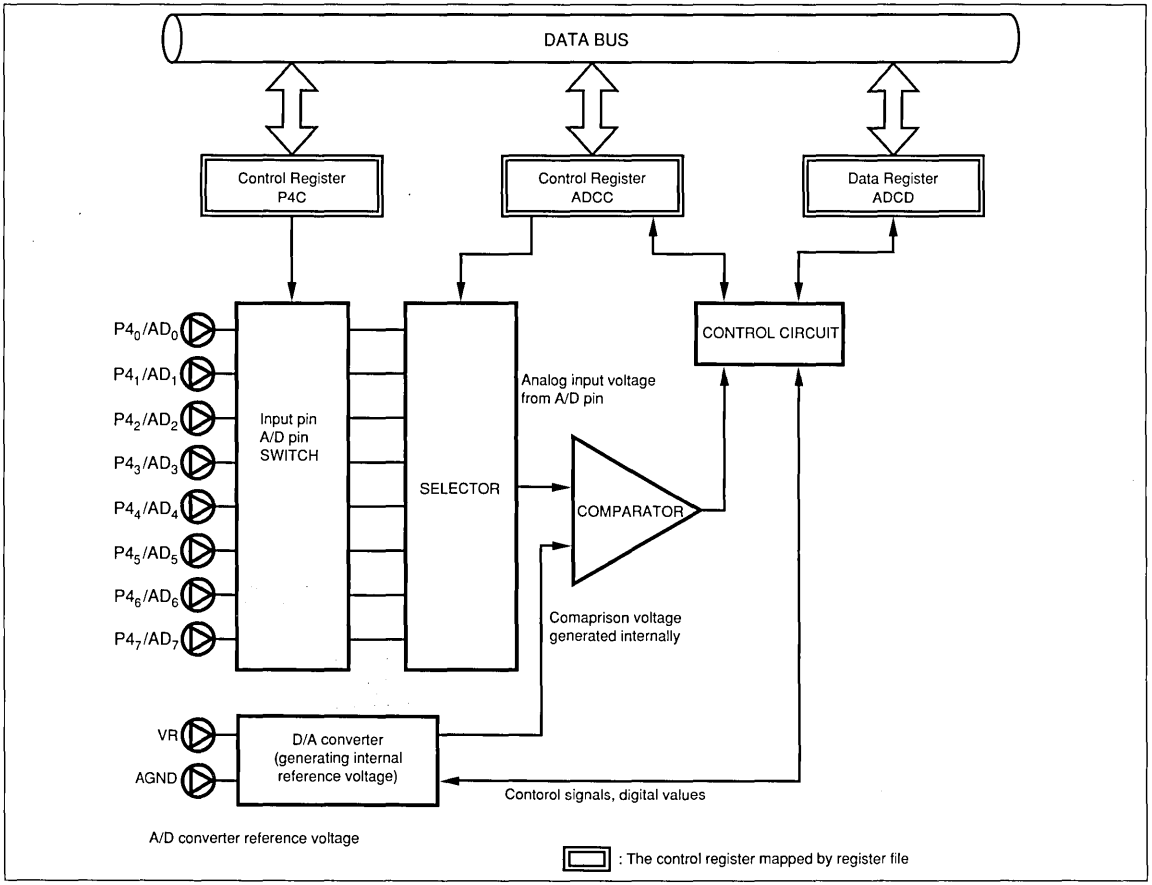


Fig. 21 A/D converter block diagram

A/D Converter Data Register (ADCD)

Data register ADCD is an 8bit readable/writable register which stores the upper 8 bits of 10-bit A/D data.

In A/D conversion mode, while A/D conversion is complete, then the digital value (the upper 8 bits of 10-bit) of corresponding to the analog input voltage is stored into this register.

In comparison mode, the comparison reference voltage value (the upper 8 bits of 10-bit) is set to this register before A/D conversion.

A/D Converter Control Register (ADCC)

Control register ADCC is a register with 7 bits readable/writable and 1 bit read only. The register is for storing the lower 2 bits of 10-bit A/D data, selecting the operating mode, storing the comparison result in comparison mode , controlling to start/stop A/D converter, and selecting the input channel.

Bit 7 0

ADCC7	ADCC6	ADMD	CO	S/S	SEL2	SEL1	SEL0

Bit 7-6 : A/D conversion stored bits (ADCC7-ADCC6)

Stores the lower 2 bits of 10-bit A/D data.

In A/D conversion mode, while A/D conversion is complete, then the digital value (the lower 2 bits of 10-bit) of corresponding to the analog input voltage is stored into these bits.

In comparison mode, the comparison reference voltage value (the lower 2 bits of 10-bit) is set to these bits before A/D conversion.

Bit 5 : Operating mode selection bit (ADMD)

0	A/D conversion mode
1	Comparison mode

Bit 4 : Comparison result stored bit (CO)

0	Input level < 10-bit A/D data (preset D/A level).
1	Input level > 10-bit A/D data (preset D/A level).

Bit 3 : start/stop bit (S/S)

Controls the A/D converter to start/stop and uses to monitor the operating state.

0	Read : A/D converter is in end state. Write : A/D converter is forced to end.
1	Read : A/D converter is in operating state. Write : A/D converter starts.

Bit 2-0 : A/D input channel selection bits (SEL2-SEL0)

BIT	A/D INPUT PIN
000	$P4_0/AD_0$ pin
001	$P4_1/AD_1$ pin
010	$P4_2/AD_2$ pin
011	$P4_3/AD_3$ pin
100	$P4_4AD_4$ pin
101	$P4_5/AD_5$ pin
110	$P4_6/AD_6$ pin
111	$P4_7/AD_7$ pin

P4 Control Register (P4C)

Control register P4C is an 8 bit readable/writable register which is able to switch in 1-bit unit to analog input pin, shared to Port4, of A/D converter.

Bit 7 0

P4C7	P4C6	P4C5	P4C4	P4C3	P4C2	P4C1	P4C0

Bit i : P4i Input mode selection bit (P4Ci) i = 7 to 0

0	digital input (P4i)
1	analog input (ADi)

When A/D converter starts, the bits SEL2-SEL0 (bit 2-0 : ADCC) select one input pin to use among these analog input pins which set by control register P4C.

D/A CONVERTER AND WAVEFROM GENERATOR

SM8500 supports two channels (max.) D/A converter with 8 bit resolution. D/A converter is to convert the digital value written into the waveform RAM of waveform generator to the D/A value which is output to DA_{OUT0} pin or DA_{OUT1} pin. If the two of channels D/A converter are output to the external OP amplifier, they are available for DTMF output.

D/A converter has two output modes as following.

- **Waveform generator mode : output wave from designated by user from waveform generator**
  - One period, 32 steps setting
  - Wave peaking value 4 bit / 1 step
  - 16 step tone data output
  - Waveform data set to waveform memory (WGM)
  - Setting frequency by waveform generator scale data register (WGSD)
  - VDA (output voltage) = (DAVR/8) + (DAVR x 8n/256) (n = 0 to 15)

- **8 bit D/A converter mode : output the content of waveform RAM designated by the address (Do not use waveform generator).**
  - 8 bit data output
  - Output data (Max. 16 bytes) set to waveform memory and switched by program.
  - VDA (output voltage) = DAVR x n/256
    (n = 0 to 255)
    DAVR : the reference voltage of D/A converter (applied to DAVR0, DAVR1 pin)
    n : the digital value set to waveform RAM (decimal)

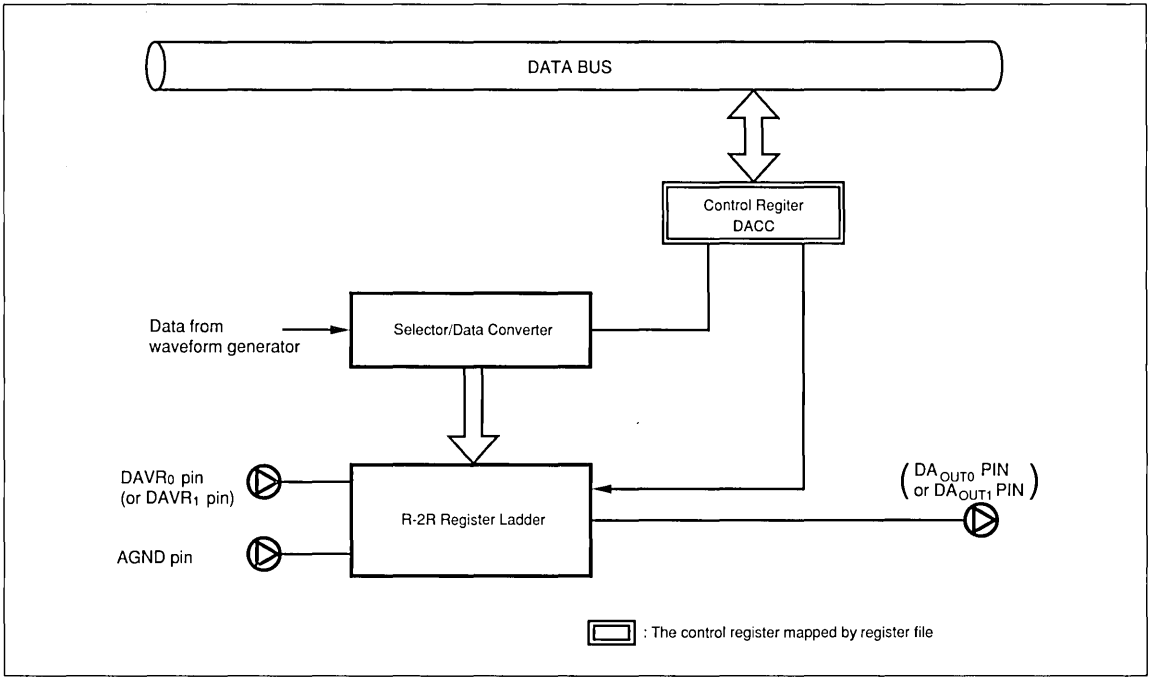


Fig. 22 D/A converter block diagram (1 channel)

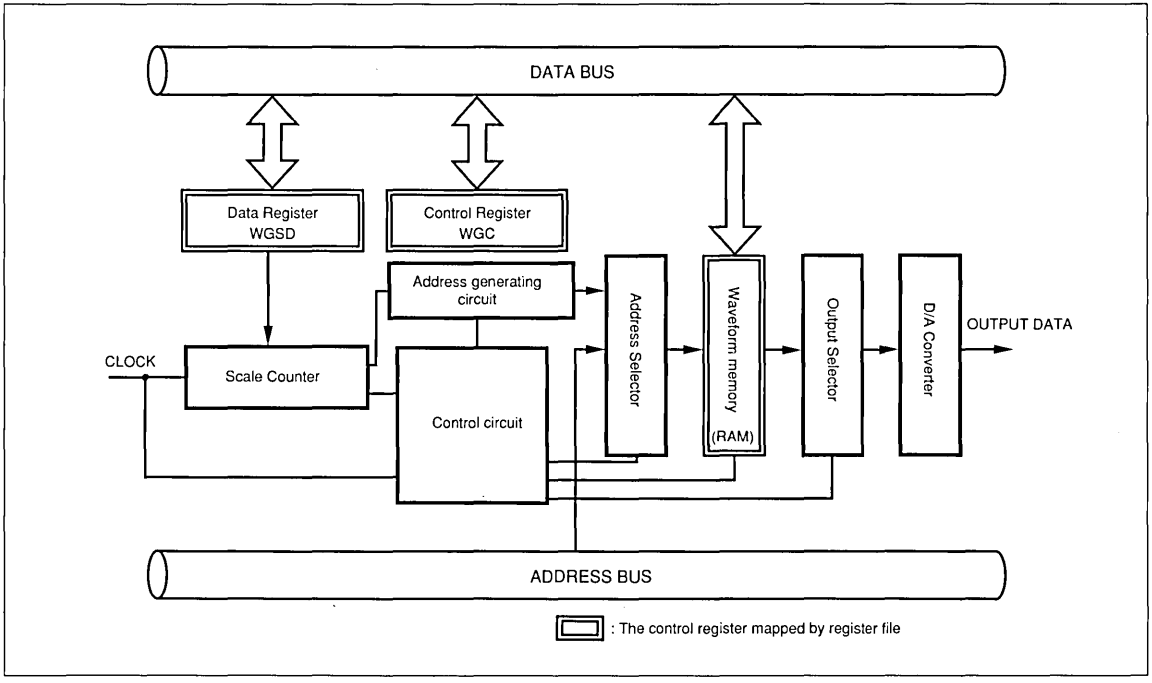


Fig. 23 Waveform generator block diagram (1 channel)

Waveform Memory (WGM)

Waveform memory WGM0 is allocated at the register file area 0060H-006FH and stores the DA_{OUT0} pin output level with digital value. However, waveform memory WGM1 is allocated at register file area 0070H-007FH and stores the DA_{OUT1} pin output level. Waveform memory is undefined after hardware reset.

Waveform generator mode

Waveform memory WGM0, WGM1 are configurated by 16 bytes (32 steps x 4-bit) respectively. (Refer to Fig. 24). The data set to waveform memory represents a wave peaking value. The peaking value of one step has 4bit resolution (16 steps tone, center value 8H). These peaking values of one channel are stored into 16 byte waveform memory, so one period is set by 32 steps (One byte of waveform data is representative of two step wave peaking values.). The peaking value is output in sequence by the upper 4 bits, then the lower 4 bits of one byte from smaller address of waveform memory. If starts the waveform generator, the data is output starting from step 0 in sequence. When the step 31 data is output, it returns to step 0 and outputs it again. (It always starts from step 0 when starts the waveform generator.)

In waveform generator mode, if the bit WGWEN is '1' (enable to write) and bit WGST is '0' (stop waveform generator), then a data can be written into waveform memory.

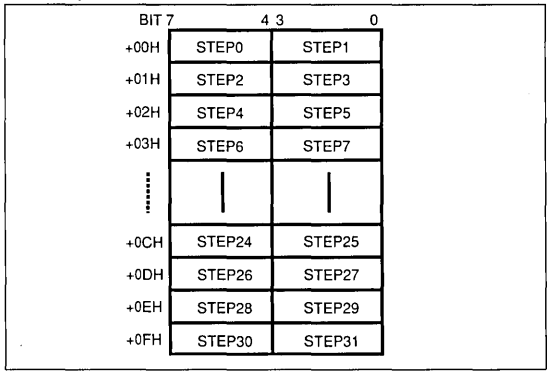


Fig. 24 Waveform memory setting (waveform generator mode)

8 bit D/A converter mode

The data given in waveform memory is representative of D/A conversion output level. Waveform memory WGM0, WGM1 can be set by the digital values of 8 bit x 16 bytes, respectively.

In 8 bit D/A converter mode, When the bit WGWEN of control register WGC is '1' (enable to write), then the data can be written into waveform memory (regardless of the bit WGST).

If starts the D/A converter, a digital value in the address last written to waveform memory is output to D/A converter. In addition, under the bit WGWEN = [0] (disable to write) state, the used waveform memory address can be changed by writting dummy data to waveform memory.

Waveform Generator Scale Data Register 0, 1 (WGSD0, WGSD1)

Data register WGSD0, WGSD1 are 8 bit readable/writable register, respectively, and sets to one step time in waveform generator mode. (WGSD0 , WGSD1 are corresponding to the channel 1 , channel 2 output of waveform generator , respectively.)

One step time = fc_1 (0.362 µs) x (100H - waveform generator scale data register value*)

NOTE :

0.362 µs is the value as main-clock = 11.0592 MHz.

One period time = one step time x 32 (step numbers)

* The scale data register WGSD0, WGSD1 are able to be set to a value between 00H and FEH, respectively.

Waveform Generator Control Register (WGC)

Waveform generator WGC is an 8 bit readable/writable register which is for controlling waveform generator to start/stop, selecting the operating mode, and enabling/disabling to write into waveform memory.

Bit 7 0

WGST1	WGWEN1	WGMOD1	-	WGST0	WGWEN0	WGMOD0	-

Bit 7 : Waveform generator 1 start/stop bit (WGST1)

Bit 3 : Waveform generator 0 start/stop bit (WGST0)

Controls the waveform generator channel 1 or channel 0 to start/stop (The data of waveform memory is transferred to D/A converter.). This bit setting is valid only in waveform generator mode (It does not affect to the operation in 8 bit D/A converter mode.)

0	Read : Waveform generator is in the stop state. Write : Waveform generator is designated to stop.
1	Read : Waveform generator is operating. Write : Waveform generator is designated to start operation.

In waveform generator mode, sets the bit WGST to '1' such that the scale counter starts counting and the data of waveform memory is transferred to D/A converter channel 1.

If writes a '0' value to the bit WGST in the interval of waveform generator channel 1 operating, the waveform generator channel 1 will stop at the end of one period (i, e step 31 is processed completely). And, the bit WGST is not cleared to '0' until the waveform generator channel 1 stops.

Bit 6 : Waveform memory 1 written enable bit (WGWEN1)

Bit 2 : Waveform memory 0 written enable bit (WGWEN0)

In D/A converter mode, if writes data to waveform memory 1 when this bit is '0', the data of waveform memory 1 is not renewed and only renews the address of waveform memory (The address represents the location of the 8 bit data sent to D/A converter.)

0	Disables to write data into waveform memory
1	Enables to write data into waveform memory

Bit 4 : Waveform memory 1 operating mode selection bit (WGMOD1)

Bit 1 : Waveform memory 0 operating mode selection bit (WGMOD0)

0	Waveform generator mode (4 bit data mode).
1	8-bit D/A converter mode (8 bit data mode).

D/A Converter Control Register (DACC)

Control register DACC is an 8 bit readable/writable register and is for enabling/disabling D/A converter (2 channels) to output, and controlling to supply the reference voltage.

Bit 7 0

DAVR1	-	-	-	DAVR0	-	-	-

Bit 7 : D/A converter 1 reference voltage supplied

0 | OFF (Cutoff DAVR1 pin voltage from D/A converter 1)

1 | ON (supply DAVR1 pin voltage to D/A converter 1)

Bit 3 : D/A converter 0 reference voltage supplied

0 | OFF (Cutoff DAVR0 pin voltage from D/A converter 0)

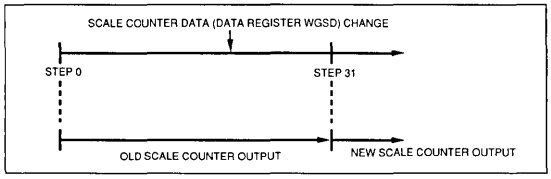
1 | ON(supply DAVR0 pin voltage to D/A converter 0)

NOTES :

1. The bit 2, 6 are readable/writable bits, but the read/write operation of these bits do not affect to microcomputer operation
2. The output circuit of D/A converter do not support the buffer. Please add a buffer to D/A converter output.

Scale Counter Data Changed in The Waveform Generator Operating

If the data register WGSD0 is changed in the operating, the new data of step time and period are output after one period was complete (the output end of step 31).



If a '0' value is written into the bit WGST0 (bit 3 : WGC) in the waveform output operating, it will request to stop the waveform generator 0 operation. But the operation does not stop immediately. The waveform generator 0 operates continously until one period of waveform output is end (the output end of step 31). After a '0' value is written into the bit WGST0, the bit is not '0' until waveform generator stops.

Application Example to DTMF

Tone output frequency example

By the setting of data register WGSD, Table 10 shows that the tone output frequency is able to be set. (When one period set by 32 steps).

Table 10 DTMF output frequency

	STANDARD DTMF (Hz)	SM8500 (Hz)	TOLERANCE (%)
Low frequency group	697	696.8	–0.03
	770	771.4	+0.18
	852	855.5	+0.41
	941	939.1	–0.20
High frequency group	1 209	1 216.9	+0.65
	1 336	1 329.2	–0.51
	1 477	1 489.7	+0.86

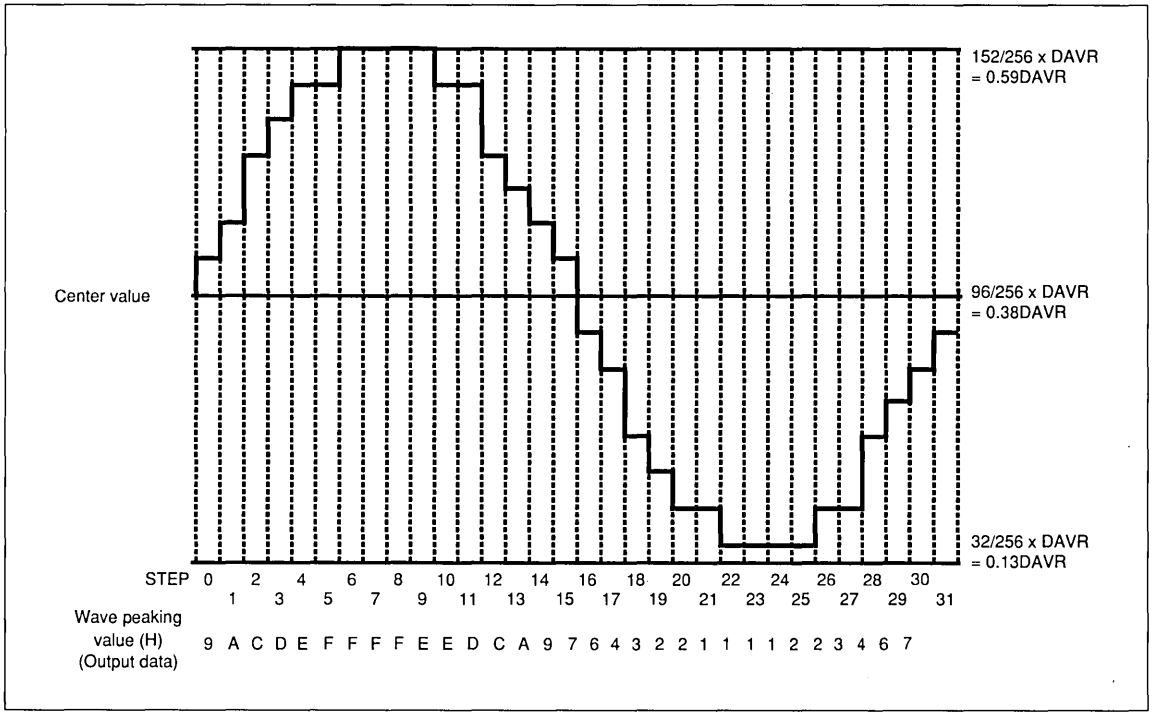


Fig. 25 Output waveform example

The connection example

Low frequency group and high frequency group is use channel 0 and channel 1, respectively, to output by program, connects with external OP amplifier and the buffer to DAOUT0 pin and DAOUT1 pin, then we can get DTMF output. (Refer to Fig. 26).

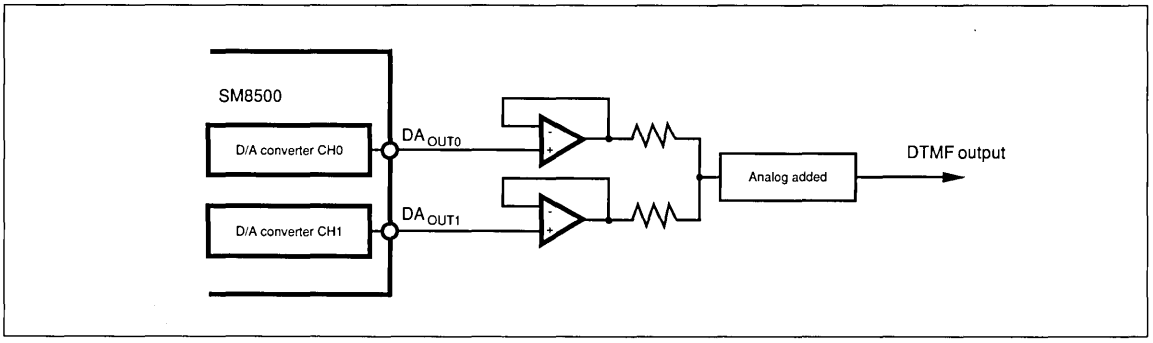


Fig. 26 DTMF output connection example

CLOCK SYNCHRONOUS SERIAL INTERFACE (SIO)

SM8500 supports 1-channel Clock Synchronous Serial Interface SIO .

The SIO interface has the following features.

- **It is able to switch the transmit/receive data width (8 bit transfer/4 bit transfer) for every time transfer operation.**
- **It is able to switch the transfer direction (LSB first / MSB first)**
- **It is able to select 6 kinds of transfer clock sources, such as internal clock (prescaler PRS0 output), timer1 output, external clock or $P7_5$ pin output.**
  - Internal clock : fc_4, fc_5, fc_6, fc_7, fc_8, fc_9
  - Timer 1 output : Timer1 (TM1) output is used as transfer clock.
  - External clock : $P7_5/S_{CK}$ pin serves as transfer clock input pin.
  - $P7_5$ output : $P7_5/S_{CK}$ pin output is used as simulate transfer clock by program.

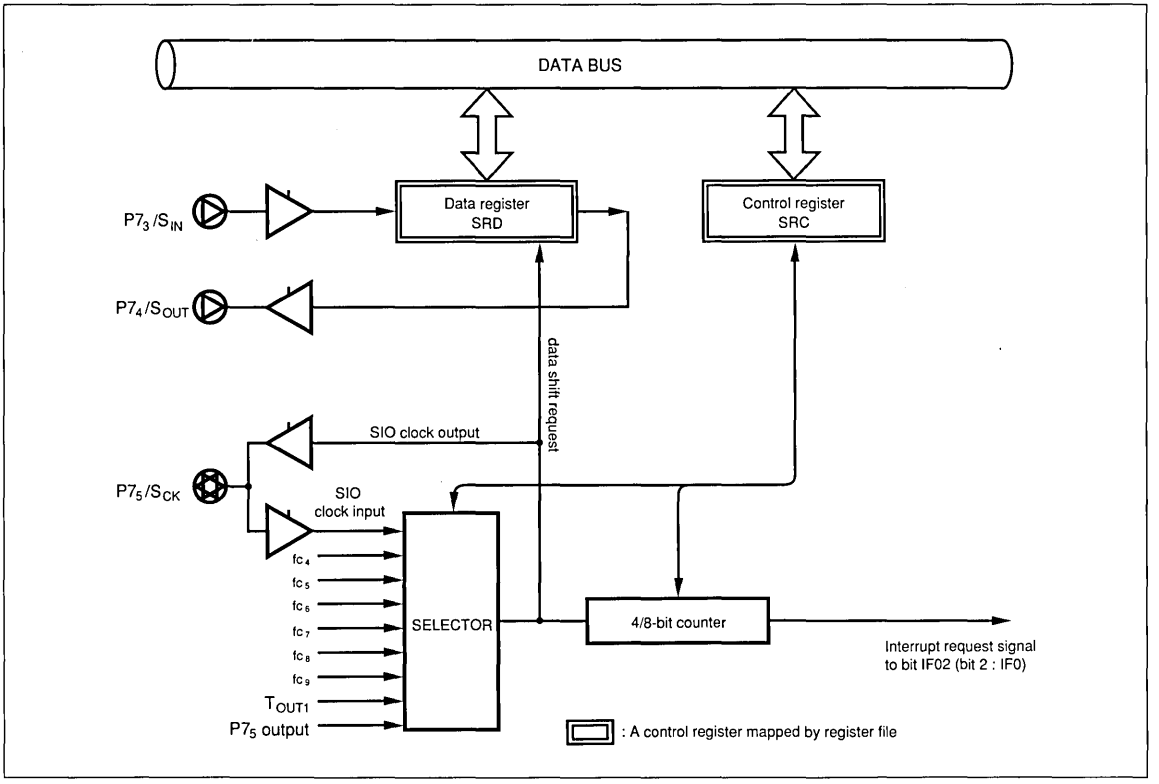


Fig. 27 SIO Block diagram

SIO Data Register (SRD)

Data register SRD is an 8 bit writable/readable register which stores the SIO transfer data.

SIO Control Register (SRC)

Control register SRC is an 8 bit writable/readable register which controls the SIO operations.

Bit 7							0
EN	S/S	MD1	MD0	-	SEL2	SEL1	SEL0

Bit 7 : Interface enable (EN) bit

0 | disable SIO interface.

1 | enable SIO interface. P73/SIN, P74/SOUT, P75/SCK pins can be used as the SIO pins.

Bit 6 : Start/Stop (S/S) bit

0 | read : SIO in stop status.
Write : Designating SIO to stop.

1 | read : SIO in operating status.
Write : Designating SIO to start.

Bit 5 : Transfer direction selection (MD1) bit

BIT	TRANSFER DIRECTION
0	MSB LSB S_{IN} pin → Data register SRD → S_{OUT} pin
1	MSB LSB S_{OUT} pin ← Data register SRD ← S_{IN} pin

Bit 4 : Transfer data width selection (MD0) bit

Selects the numbers of the SIO transmit/receive bits at every time.

0 | 8 bit transfer

1 | 4 bit transfer

Bit 2-0 : Transfer clock selection (SEL2-SEL0) bit

BIT	TRANSFER CLOCK
000	T_{OUT1} (Timer output)
001	fc_4 (345.6 kHz)
010	fc_5 (172.8 kHz)
011	fc_6 (86.4 kHz)
100	fc_7 (43.2 kHz)
101	fc_8 (21.6 kHz)
110	fc_9 (10.8 kHz)
111	External clock or $P7_5$ output

The number indicated in ( ) is the value when the main-clock is 11.0592 MHz.

When the interface starts to operate by designating the bit S/S (bit6 : SRC), please set the control register SRC as following procedures.

(1) To set all bits of the control register under the bit S/S = [0].

(2) After (1) was set, renews the bit S/S to '1' such that starts the SIO interface. (The other bits do not change please other than for the bit S/S.)

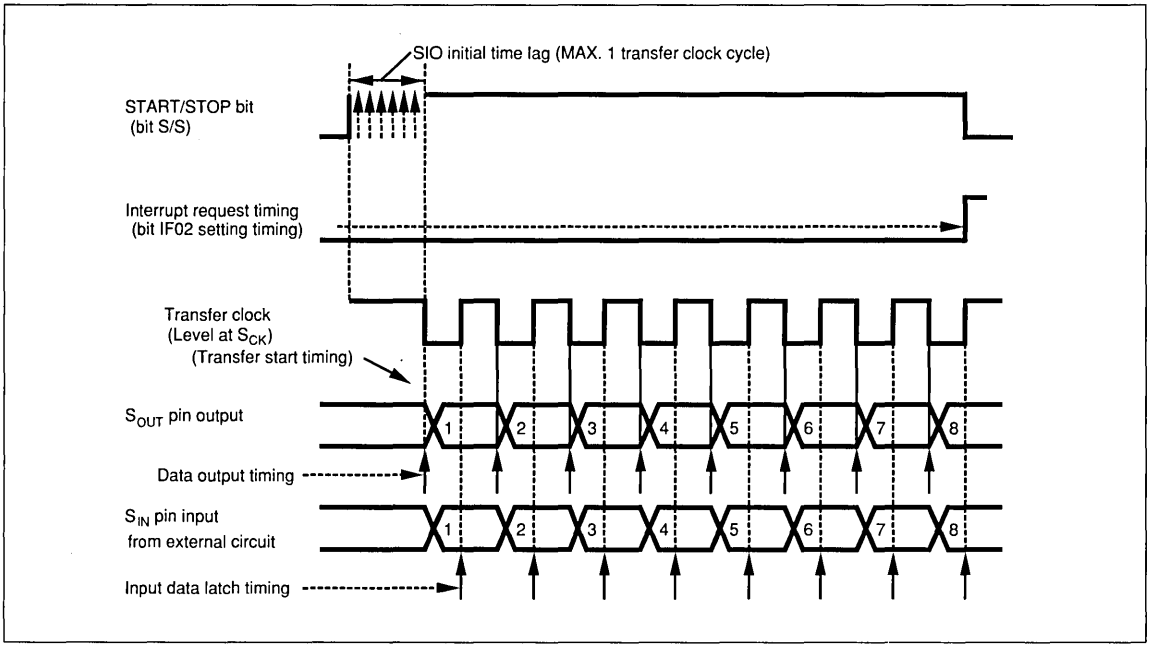


Fig. 28 SIO Transfer timing

UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER (UART) INTERFACE

SM8500 supports 1-channel Universal Asynchronous Receiver and Transmitter interface (UART)
The UART interrupt has the following features.

- **Transmitter and Receiver are independent each other, full duplex communication possible.**
- **Receiver is consisted of duplex buffer, able to receive data continuously.**
- **The dedicated register for Baud Rate Generator is built in.**
- **It is possible to choose transfer format as following.**
  - Stop bit : 1-bit / 2-bit
  - Parity bit : even parity / odd parity / no parity
  - 8-bit / 9-bit transfer : available to configurative multiple CPUs system (the 9-bit mode)
- **Receive error can be detected.**
  - Frame Error
  - Parity Error
  - Overrun Error

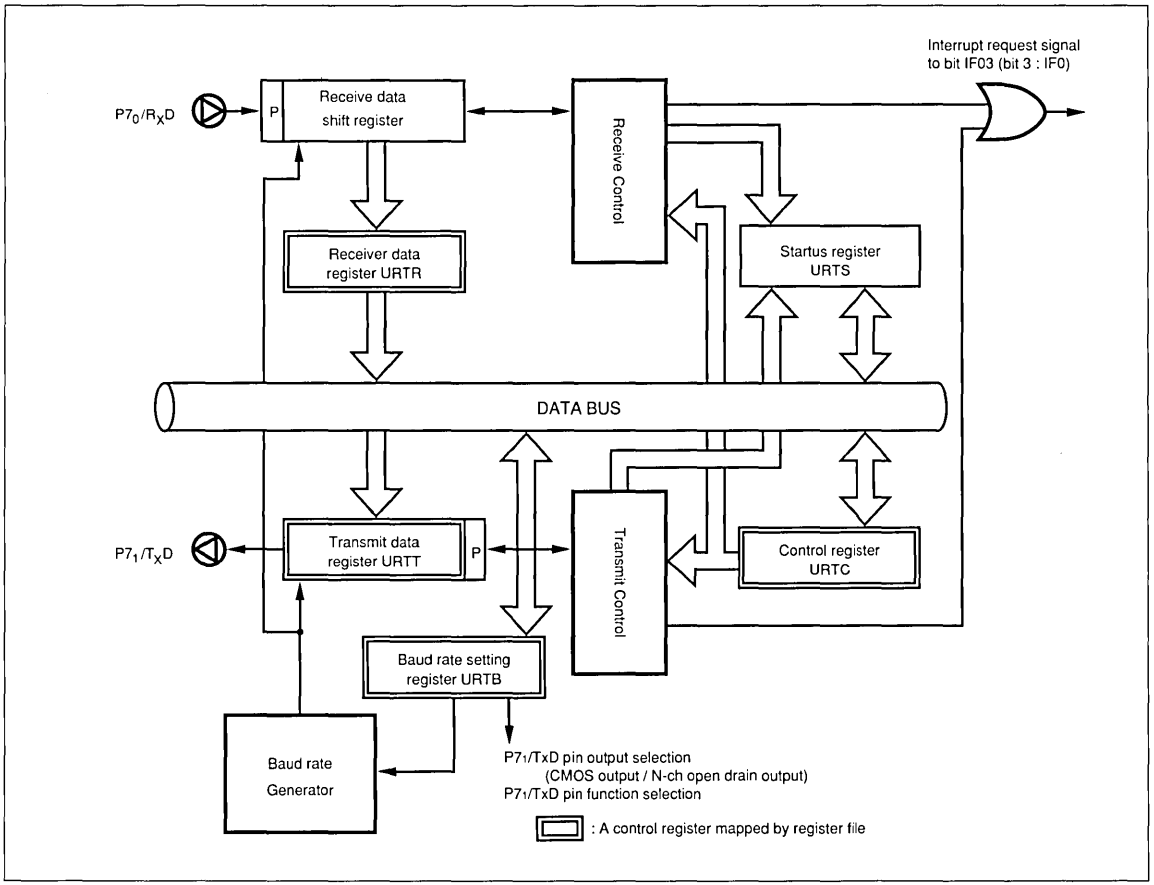


Fig. 29 UART Block diagram

UART Transmit Data Register (URTT)

Transmit data register URTT is an 8-bit write only register which stores the UART transmit data.
When the transmission operation starts, the content of this register LSB first is output from $P7_1$/TxD pin.

UART Receive Data Register (URTR)

Receive data register URTR is an 8-bit read only register which stores the UART receive data.
When the receive operation starts, the receive data LSB first will be moved into the receive data shift register from $P7_0$/RxD pin. Once the receive operation is complete, the content of the receive data shift register is loaded into this receive data register URTR (duplex buffer).

UART Status Register (URTS)

Status register (URTS) is an 8-bit read only register containing the flags of the UART interface transmit/ receive status.

Bit 7 0

RB8	-	RBSY	OR	FE	PE	TDRE	TDRE

Bit 7 : Receiver Bit8 (RB8) bit (9 th bit of received data for 9-bit mode)

Bit 5 : Receiver Busy (RBSY) bit

0 | UART receiver is other than the following.

1 | UART receiver processing incoming data.

Bit 4 : Overrun Error (OR) bit

0 | Clear condition
(1) while reading the status register URTS.
(2) hardware reset

1 | Set condition
(1) while overrun error occurs (the next receive is complete under the bit RDRF = [1]) at receive data.

Bit 3 : Frame Error (FE) bit

0 | Clear Condition
(1) while reading the status register URTS
(2) hardware reset

1 | Set Condition
(1) while frame error occurs (stop bit = [0] was detected) at receive data.

Bit 2 : Parity Error (PE) bit

0 | Clear Condition
(1) while reading the status register URTS
(2) hardware reset

1 | Set Condition
(1) parity error occurs at receive data

Bit 1 : Transmit Data Register Empty (TDRE) bit

0 | Clear Condition
(1) while writting to transmit data register URTT.

1 | Set Condition
(1) while having finished transmitting operation.
(2) hardware reset

Bit 0 : Receiver Data Register Full (RDRF) bit

0 | Clear Condition
(1) while reading from receive data register URTR
(2) hardware reset

1 | Set Condition
(1) while receive data is transferring to receive data register URTR from receive data shift register

UART Control Register (URTC)

Control register URTC is an 8-bit readable/writable register specifying to transfer format setting and transmission/receive operation controlling.

Bit 7 0

TB8	WU	FL	TE	RE	PEN	EOP	SBL

Bit 7 : Transmitter Bit8 (TB8) bit

In 9-bit mode, the Transmitter Bit 8 (TB8) bit holds the 9th bit of the transmit data.

Bit 6 : Wake-Up (WU) bit

0 | All data accepted (regardless of the bit RB8 value) in 9-bit mode.

1 | Only data with RB8 = [1] accepted (the data with RB8 = [0] ignored) in 9-bit mode.

Bit 5 : Frame Length (FL) bit

Multiple CPUs system can be configurated in the 9-bit mode.

0 | 8-bit data length

1 | 9-bit data length (9-bit mode)

Bit 4 : Transmit Enable (TE) bit

Setting the bit TE to '1', starts the built-in Baud Rate Generator and the interface enters transmissible status. In such status, if a transmit data is wrote to the transmit data register URTT, then will start the transmission operation. If the bit TE clears to '0', the transmitter will be initiated.

0 | transmitter disable

1 | transmitter enable (built-in Baud Rate Generator operates)

Bit 3 : Receive Enable (RE) bit

Setting the bit RE to '1', starts the built-in Baud Rate Generator and the interface enters receivable status. In such status, if the start bit (= '0') is detected, then will start the receive operation

0 | receiver disable

1 | receiver enable (built-in Baud Rate Generator operates)

If the bit RE clears to '0', the receiver will be initializated.

Bit 2 : Parity Enable (PEN) bit

0 | transmit : the data with parity bit.
receive : parity enable

1 | transmit : the data without parity bit.
receive : parity disable

Bit 1 : Even/Odd Parity (EOP) bit

0 | even parity

1 | odd parity

Bit 0 : Stop Bit Length (SBL) bit

0 | stop bit : 1 bit

1 | stop bit : 2 bits

UART Baud Rate Setting Register (URTB)

Baud rate setting register URTB is an 8-bit readable/writable register specifying to the baud rate setting and $P7_1$/TxD pin function setting.

Bit 7 0

TXDOE	TXDNO	-	-	-	BSEL2	BSEL1	BSEL0

Bit 7 : $P7_1$/TxD pin function selection bit

0 | I/O port ($P7_1$)

1 | transmit data output pin (TxD)*2

Bit 6 : $P7_1$/TxD pin output selection bit

0 | CMOS output

1 | N-ch open drain output

Bit 2-0 : Baud rale selection bit*1

BIT	BAUD RALE (BPS)
000	38 400
001	19 200
010	9 600
011	4 800
100	2 400
101	1 200
110	600
111	T_{OUT2} (Timer2 output)/16

NOTE :

the numberical value in above table is the value when the main-clock=11.0592 MHz.

*1 : The setting values are set by the bits BSEL2-BSEL0 when the main-clock is 11.0592M Hz.
To get the general baud rate value has to select the ocillator of 11.0592 MHz/2n.
If the ocillator frequency devides by 2, above table will be 1/2 of the baud rate.

*2 : When $P7_1$/TxD pin is set as transmit output pin by the bit TXDOE (bit7 : URTB), $P7_1$/TxD pin also must be set as an output port by P7 control register (P7C).

Transfer Format

According to setting stop bit, parity bit and the 9-bit mode by control register URTC, transfer format indicated by Fig. 30 can be select.

URTC		
FL (bit 5)	PEN (bit 2)	SBL (bit 0)
0	0	0
0	0	1
0	1	0
0	1	1
1	*	0
1	*	1

TRANSFER FORMAT

(TRANSFER DIRECTION)

ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	P	STP	
ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	P	STP	STP
ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	STP		
ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	STP	STP	
ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	RB8	STP	
ST	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	RB8	STP	STP

ST : start bit, P : parity bit, STP : stop bit

RB8 : The ninth bit of a data in 9bit mode, * : Don't care

NOTE : In mode, the parity bit does not be added, irrespective of the setting for bit PEN (bit 2 : URTC)

Fig. 30 Transfer format

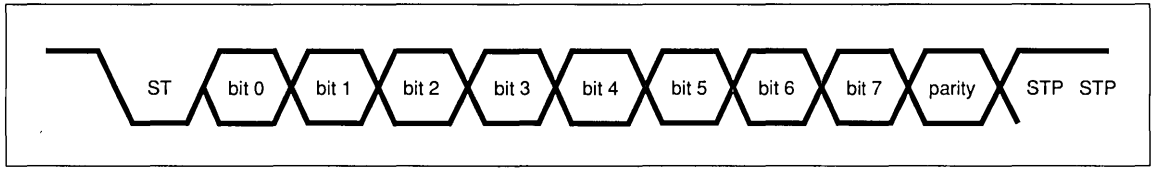


Fig. 31 8-bit mode transfer format (Example for parity added and 2 stop bits)

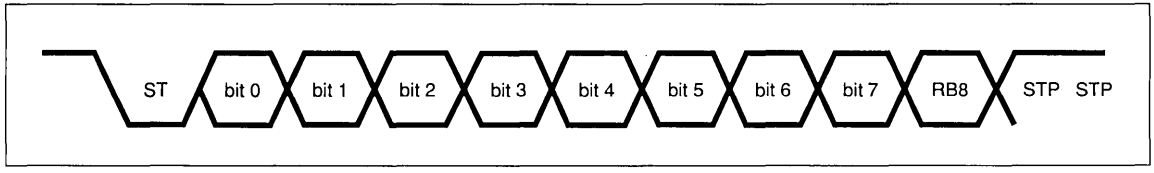


Fig. 32 9-bit mode transfer format (example for 2 stop bits)

INSTRUCTION SET

The instruction set of the SM85CPU has the following characteristics :

- **The instruction set is the result of subtle design and consists of 67 types of basic instructions.**
  - There are powerful bit manipulation instructions includes plural bits transfer, logical operation between bits, and the bit test and jump instructions that incorporates a test and condition branch in the same instruction.
  - There are transfer, operation and conditional branch instructions for 16 bit. The actions of transfer, operation and long jump for word data can be processed in high speed.
  - There are aristhmetic instructions for multiplication and division.
    Multiplication : 8 bit x 8 bit→16 bit
    Division : 16 bit x 16 bit→16 bit remainning 8 bit

- **23 types of memory addressing mode**
  - By variety of memory addressing modes, the accessing to RAM, ROM, and register file can be operated .

Definition of Symbols

SP ; Stack pointer
@SP ; Indirect stack pointer
PC ; Program counter
C ; Carry [bit 7 of processor status 1 (PS1)]
BF ; The value of Bit flag(B) [bit 1 of processor status 1 (PS1)]
I ; Interrupt enable [bit 0 of processor status 1 (PS1)]

Instruction Summary

Load instruction

INSTRUCTION	OPERAND	FUNCTION
CLR	dst	dst←0 (Clear)
MOV	dst, src	dst←src (Move)
MOVM	dst, IM, src	dst←(dst AND IM) or src (Move Under Mask)
MOVW	dst, src	dst←src (Move Word)
POP	dst	dst←@SP, SP←SP+1 (Pop from Stack)
POPW	dst	dst←@SP, SP←SP+2 (Pop Word from Stack)
PUSH	src	SP←SP–1, @SP←src (Push to Stack)
PUSHW	src	SP←SP–2, @SP←src (Push Word to Stack)

Arithmetic operation instruction

INSTRUCTION	OPERAND	FUNCTION
ADC	dst, src	dst←dst+src+C (Add With Carry)
ADCW	dst, src	dst←dst+src+C (Add Word With Carry)
ADD	dst, src	dst←dst+src (Add)
ADDW	dst, src	ds←dst+src (Add Word)
CMP	dst, src	dst−src (Compare)
CMPW	dst, src	dst−src (Compare Word)
DA	dst	dst←DA dst (Decimal Adjust)
DEC	dst	dst←dst−1 (Decrement)
DECW	dst	dst←dst−1 (Decrement Word)
DIV	dst, src	dst←dst/src, src←dst MOD src (Divide)
EXTS	dst	extend sign (Extend Sign)
INC	dst	dst←dst+1 (Increment)
INCW	dst	dst←dst+1 (Increment Word)
MULT	dst, src	dst←dst x src (Multiply)
NEG	dst	dst← −dst (Negate)
SBC	dst, src	dst←dst−src−C (Subtract With Carry)
SBCW	dst, src	dst←dst−src−C (Subtract Word With Carry)
SUB	dst, src	dst←dst−src (Subtract)
SUBW	dst, src	dst←dst−src (Subtract Word)

Logical operation instruction

INSTRUCTION	OPERAND	FUNCTION
AND	dst, src	dst←dst AND src (Logical And)
ANDW	dst, src	dst←dst AND src (Logical And Word)
COM	dst	dst←NOT dst (Complement)
OR	dst, src	dst←dst OR src (Logical Or)
ORW	dst, src	dst←dst OR src (Logical Or Word)
XOR	dst, src	dst←dst XOR src (Logical Exclusive Or)
XORW	dst, src	dst←dst XOR src (Logical Exclusive Or Word)

Program control instruction

INSTRUCTION	OPERAND	FUNCTION
BBC	src, dst	if src = 0 then PC←PC+dst (Branch on Bit Clear)
BBS	src, dst	if src = 1 then PC←PC+dst (Branch on Bit Set)
BR	cc, dst	if cc = true then PC← PC+dst (Branch)
CALL	dst	SP←SP−2, @SP←PC, PC←dst (Call Subroutine)
CALS	dst	SP←SP−2, @SP←PC, PC←dst (Short Call Subroutine)
DBNZ	r, dst	r←r−1, if r ≠ 0 then PC←PC+dst (Decrement and Branch on Non-Zero)
IRET		PS1←@SP, SP←SP+1, PC←@SP, SP←SP+2 (Return from Interrupt)
JMP	cc, dst	if cc = true , then PC←dst (Jump)
RET		PC←@SP, SP←SP + 2 (Logical Exclusive Or Word)

Bit operation instruction

INSTRUCTION	OPERAND	FUNCTION
BAND	BF, src	BF←BF AND src (Bit And)
BCLR	dst	dst←0 (Bit Clear)
BCMP	BF, src	BF–src (Bit Compare)
BMOV	dst, src	dst←src (Bit Move)
BOR	dst, src	dst←BF OR src (Bit Or)
BSET	dst	dst←1 (Bit Set)
BTST	dst, src	dst AND src (Bit Test)
BXOR	BF, src	BF←BF XOR src (Bit Exclusive Or)

Rotate and Shift instruction

INSTRUCTION	OPERAND	FUNCTION
RLC	dst	(Rotate Left through Carry)
RR	dst	(Rotate Right)
RRC	dst	(Rotate Right through Carry)
SLL	dst	(shift Left Logical)
SRA	dst	(shift Right Arithmetic)
SRL	dst	(shift Right Logical)
SWAP	dst	(Swap Nibbles)

CPU Control Instruction

INSTRUCTION	OPERAND	FUNCTION
CLRC		C←0 (Clear Carry Flag)
COMC		C←NOT C (Complement Carry Flag)
DI		I←0 (Disable Interrupt)
EI		I←1 (Enable Interrupt)
HALT		Move to HALT mode (Halt CPU)
NOP		No Opreration (No Opreration)
SETC		C←1 (Set Carry Flag)
STOP		Go to STOP mode (Stop CPU)

Addressing Mode

There are 23 types of addressing mode to perform memory accessing in SM85CPU. The relationships between the addressing modes and the operand are shown in the following table 10.

Table 10 Addressing mode summary

NAME	SYMBOL	Range	Operand
Implied			To specify the carry(C) and interrupt enable (I) in the instruction code.
Register	r	r = R0-R7	General register [byte]
Register pair	rr	r = RR0, RR2, ... ,RR14	General register [word]
Register file	R	R = 0 to 255 (R0 - R15)	Register file (0000H-007FH) and (0080H-00FFH) [byte]
Register file pair	RR	R=0, 2, ... 254 (RR0, RR2, ... ,RR14)	Register file (0000H-007FH) and (0080H-00FFH) [byte]
Register indirect	@r	r=R0-R7	Memory (0000H-00FFH) [byte]
Register indirect auto increment	(r) +	r = R0-R7	Memory (0000H-00FFH) [byte]
Register indirect auto decrement	–(r)	r = R0-R7	Memory (0000H-00FFH) [byte]
Register index	n (r)	n = 00H-FFH, r = R1-R7*2	Memory (0000H-00FFH) [byte]
Register pair indirect	@ rr	rr = RR0, RR2, ... ,RR14	Memory (0000H-FFFFH) [word/byte]
Register pair indirect auto increment	(rr) +	rr = RR0, RR2, ... ,RR14	Memory (0000H-FFFFH) [word/byte]
Register pair indirect auto decrement	–(rr)	rr = RR0, RR2, ... ,RR14	Memory (0000H-FFFFH) [word/byte]
Register pair index	nn (rr)	nn = 0000H-FFFFH rr = RR0, RR2, ... ,RR14*3	Memory (0000H-FFFFH) [word/byte]
Index indirect	@ nn (r)	nn = 0000H-FFFFH r = R1-R7*2	Memory (0000H-FFFFH) [word]*1
Immediate	IM	IM = 00H-FFH	The immediate data in the instruction code [byte]
Immediate long	IML	IML = 0000H-FFFFH	The immediate data in the instruction code [word]
Bit	b	b = 0 to 7	Register file (0000H-007FH) and memory (0080H-00FFH, FF00H-FFFFH) [bit] (1bit of 1 byte pointed by R, n (r) and DAp)
Port	p		Register file (0010H-0017H) [byte]
Relative	RA	PC – 128 to PC + 127	Program memory (1000H-FFFFH)
Direct	DA	DA = 0000H-FFFFH	Memory (0000H-FFFFH) [byte]*1
Direct short	DAs	DAs = 1000H-1FFFH	Program memory (1000H-1FFFH)
Direct special page	DAp	DAp = FF00H-FFFFH	Program memory (FF00H-FFFFH) [byte]*1
Direct indirect	@DA	DA = 0000H-FFFFH	memory (0000H-FFFFH)

*1 The data indicated by [byte] is the unit of possible to use in Load and Arithmetic instruction.

*2 R0 can not be used.

*3 RR0 can not be used.

Address	Register name			R/W	Initial value
0000H	General purpose register	R0	RR0	R/W	Undefined
0001H	General purpose register	R1		R/W	Undefined
0002H	General purpose register	R2	RR2	R/W	Undefined
0003H	General purpose register	R3		R/W	Undefined
0004H	General purpose register	R4	RR4	R/W	Undefined
0005H	General purpose register	R5		R/W	Undefined
0006H	General purpose register	R6	RR6	R/W	Undefined
0007H	General purpose register	R7		R/W	Undefined
0008H	General purpose register	R8	RR8	R/W	Undefined
0009H	General purpose register	R9		R/W	Undefined
000AH	General purpose register	R10	RR10	R/W	Undefined
000BH	General purpose register	R11		R/W	Undefined
000CH	General purpose register	R12	RR12	R/W	Undefined
000DH	General purpose register	R13		R/W	Undefined
000EH	General purpose register	R14	RR14	R/W	Undefined
000FH	General purpose register	R15		R/W	Undefined
0010H	Interrupt enable register 0		IE0	R/W	00H
0011H	Interrupt enable register 1		IE1	R/W	00H
0012H	Interrupt flag register 0		IF0	R/W	00H
0013H	Interrupt flag register 1		IF1	R/W	03H
0014H	External interrupt mode register		EXIN	R/W	00H
0015H	SIO Control register		SRC	R/W	00H
0016H	SIO Data register		SRD	R/W	Undefined
0017H	A/D Data register		ADCD	R/W	00H
0018H	A/D Control register		ADCC	R/W	00H
0019H	System configuration register		SYS	R/W	*0000000
001AH	Clock change regsiter		CKKC	R/W	00H
001BH	Reverse (access disable)			-	-
001CH	Stack pointer H	SPH	SP	R/W	Undefined
001DH	Stack pointer L	SPL		R/W	Undefined
001EH	Processor status 0		PS0	R/W	Undefined
001FH	Processor status 1		PS1	R/W	*******0

Address	Register name		R/W	Initial value
0020H	P0 (Input) register	P0	R	Undefined
0021H	P1 (Input/Output) register	P1	R/W	00H
0022H	P2 (Input/Output) register	P2	R/W	00H
0023H	P3 (Input/Output) register	P3	R/W	00H
0024H	P4 (Input) register	P4	R	Undefined
0025H	P5 (Input/Output) register	P5	R/W	00H
0026H	P6 (Output) register	P6	R/W	00H
0027H	P7 (Input/Output) register	P7	R/W	00H
0028H	P8 (Input/Output) register	P8	R/W	00H
0029H	P9 (Input/Output) register	P9	R/W	F0H
002AH	PA (Output) register	PA	R/W	00H
002BH	UART Transmit data register	URTT	W	FFH
002CH	UART Receive data register	URTR	R	00H
002DH	UART Status register	URTS	R	0*000010
002EH	UART Control register	URTC	R/W	00H
002FH	UART Baud rate setting register	URTB	R/W	00H
0030H	P0 Control register	P0C	R/W	00H
0031H	P1 Control registe	P1C	R/W	00H
0032H	P2 Control registe	P2C	R/W	00H
0033H	P3 Control registe	P3C	R/W	00H
0034H	P4 Control registe	P4C	R/W	00H
0035H	P1 Pull-up setting register	P1PC	R/W	00H
0036H	P2 Pull-up setting register	P2PC	R/W	00H
0037H	P7 Control registe	P7C	R/W	00H
0038H	P8 Control registe	P8C	R/W	00H
0039H	P9 Control registe	P9C	R/W	F0H
003AH	P5 Control registe	P5C	R/W	00H
003BH	Port Pull-up setting register	PPC	R/W	00H
003CH	Waveform generator scale data registe 0	WGSD0	R/W	00H
003DH	Waveform generator scale data registe 1	WGSD1	R/W	00H
003EH	Waveform generator scale control registe	WGC	R/W	11H
003FH	D/A Control registe	DACC	R/W	33H

NOTES :

- R/W indicates that there is at least one bit in the register is capable of read/write.
  (The register indicated by R/W includes the bit of special-purpose register for read). R indicates that the register is only for read.
- * indicates that the corresponding bit is ubdefined.

Address	Register name			R/W	Initial
0040H	Timer0 counter H	TM0H	TM0	R	00H
0041H	Timer0 counter L	TM0L		R	00H
0042H	Timer0 modular register H	TM0MH	TM0M	R/W	FFH
0043H	Timer0 modular register L	TM0ML		R/W	FFH
0044H	Timer0 capture register H	TM0PH	TM0P	R	00H
0045H	Timer0 capture register L	TM0PL		R	00H
0046H	Timer0 control register 0		TM0C0	R/W	C0H
0047H	Timer0 control register 1		TM0C1	R/W	1FH
0048H	Timer counter		TM1	R	00H
0049H	Timer1 modular register		TM1M	R/W	FFH
004AH	Timer1 control register		TM1C	R/W	07H
004BH	Timer2 counter		TM2	R	00H
004CH	Timer2 modular register		TM2M	R/W	FFH
004DH	Timer2 control register		TM2C	R/W	07H
004EH	Timer1/2 clock select register		TM12CT	R/W	00H
004FH	Reverse (access disable)			-	-
0050H	Timer4 counter		TM4	R	00H
0051H	Timer3 counter		TM3	R	00H
0052H	Timer3 control register		TM3C	R/W	00H
0053H	Reverse (Only use for flash memory version) *1			-	-
0054H	Timer4 modular register		TM4M	R/W	FFH
0055H	Timer3 modular registe		TM3M	R/W	FFH
0056H	Timer4 control register		TM4C	R/W	00H
0057H	Memory configuration register *2		MCF	-	-
0058H	Timer5 counter		TM5	R	00H
0059H	Timer5 modular register		TM5M	R/W	FFH
005AH	Timer5 control register		TM5C	R/W	10H
005BH	Reverse (Only use for flash memory version) *1			-	-
005CH	Timer6 counter		TM6	R	00H
005DH	Timer6 control register		TM6C	R/W	38H
005EH	Watchdog timer register		WDT	R	00H
005FH	Watchdog timer control register		WDTC	R/W	38H

Address	Register name		R/W	Initial
0060H	Waveform memory 0 Step00/01	WGM00	R/W	Undefined
0061H	Waveform memory 0 Step02/03	WGM01	R/W	Undefined
0062H	Waveform memory 0 Step04/05	WGM02	R/W	Undefined
0063H	Waveform memory 0 Step06/07	WGM03	R/W	Undefined
0064H	Waveform memory 0 Step08/09	WGM04	R/W	Undefined
0065H	Waveform memory 0 Step10/11	WGM05	R/W	Undefined
0066H	Waveform memory 0 Step12/13	WGM06	R/W	Undefined
0067H	Waveform memory 0 Step14/15	WGM07	R/W	Undefined
0068H	Waveform memory 0 Step16/17	WGM08	R/W	Undefined
0069H	Waveform memory 0 Step18/19	WGM09	R/W	Undefined
006AH	Waveform memory 0 Step20/21	WGM0A	R/W	Undefined
006BH	Waveform memory 0 Step22/23	WGM0B	R/W	Undefined
006CH	Waveform memory 0 Step24/25	WGM0C	R/W	Undefined
006DH	Waveform memory 0 Step26/27	WGM0D	R/W	Undefined
006EH	Waveform memory 0 Step28/29	WGM0E	R/W	Undefined
006FH	Waveform memory 0 Step30/31	WGM0F	R/W	Undefined
0070H	Waveform memory 1 Step00/01	WGM10	R/W	Undefined
0071H	Waveform memory 1 Step02/03	WGM11	R/W	Undefined
0072H	Waveform memory 1 Step04/05	WGM12	R/W	Undefined
0073H	Waveform memory 1 Step06/07	WGM13	R/W	Undefined
0074H	Waveform memory 1 Step08/09	WGM14	R/W	Undefined
0075H	Waveform memory 1 Step10/11	WGM15	R/W	Undefined
0076H	Waveform memory 1 Step12/13	WGM16	R/W	Undefined
0077H	Waveform memory 1 Step14/15	WGM17	R/W	Undefined
0078H	Waveform memory 1 Step16/17	WGM18	R/W	Undefined
0079H	Waveform memory 1 Step18/19	WGM19	R/W	Undefined
007AH	Waveform memory 1 Step20/21	WGM1A	R/W	Undefined
007BH	Waveform memory 1 Step22/23	WGM1B	R/W	Undefined
007CH	Waveform memory 1 Step24/25	WGM1C	R/W	Undefined
007DH	Waveform memory 1 Step26/27	WGM1D	R/W	Undefined
007EH	Waveform memory 1 Step28/29	WGM1E	R/W	Undefined
007FH	Waveform memory 1 Step30/31	WGM1F	R/W	Undefined

*1 : These two address are only valid with flash memory version [LU8500F0/F1] and do not exist in SM8500 series.
Executing read/write operation at these address do not effect to the SM8500 operation.

*2 : Only exist for SM8506 and flash memory version [LU8500F0/F1].

SM8311/SM8313/ SM8314/SM8315

8-Bit Single-Chip Microcomputer (Controllers For Home Appliances)

DESCRIPTION

The SM8311/13/14/15 is a CMOS 8-bit single-chip microcomputer incorporating an 8-bit CPU core (SM83), ROM, RAM, timer/counter, serial interface, watch dog timer and A/D converter.

It facilitates complex timing control by providing 5 timers, 10 interrupts and a pulse width measuring feature. It also has a watch dog timer to detect program overrun, enabling the chip to be used for high reliable applications including household apparatus and office equipment.

FEATURES

- ROM capacity : 8 192 x 8 bits (SM8311)
  16 384 x 8 bits (SM8313)
  24 576 x 8 bits (SM8314)
  32 768 x 8 bits (SM8315)
- RAM capacity : 512 x 8 bits (SM8311/SM8313)
  1 024 x 8 bits (SM8314/SM8315)
- Instruction sets : 74
- A RAM area is used as subroutine stack
- I/O ports :

Input	12 (also used as analog input pins)
Output	16 (high current outputs)
Input/output	24 (include double function pins)

- Interrupts :
  Non-maskable interrupt x 1 (watch dog timer)
  Maskable interrupts;
  Internal interrupts x 7 (timer x 4, serial I/O x 1, A/D converter x 1, pulse width measurement x 1)
  External interrupts x 2 (KI pin, KH pin)
- A/D converter :

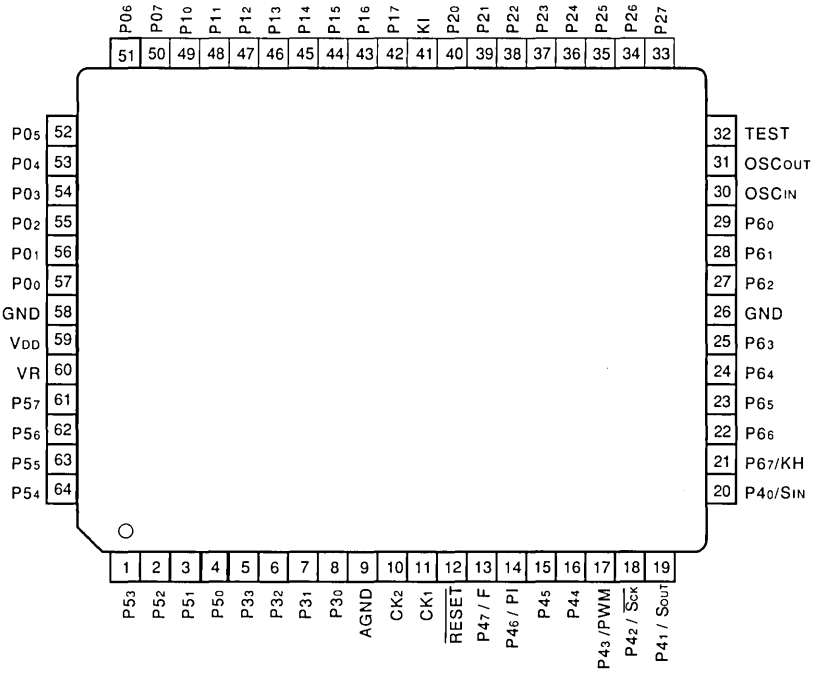
Resolution	8 bits
Channels	12 (including P3 and P5 ports)

- Timer/counter :
  8 bits x 3 (modulo register, input clock selectable)
  16 bits timer x 1 (timer 3)
  Watch dog timer : 8 bits x 1
  Free running counter : 12 bits x 1
  (w/internal 10 bits prescaler)
- Serial interface : 8 bits synchronous x 1
- PWM output circuit x 1 (also used as timer / counter)
- Pulse width measuring circuit x 1 (also used as timer/counter)
- Zero cross detector : 1 ch (KI input)
- Sound output (F pin) : 4 kHz pulse (at 8 MHz main clock)
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Built-in 15 stages divider
- Instruction cycle time :
  1 µs (MIN.) at 4 MHz main clock V_{DD} = 2.7 to 5.5 V
  0.5 µs (MIN.) at 8 MHz main clock V_{DD} = 4.5 to 5.5 V
- Supply voltage : 3.0 V ± 10% at 4 MHz main clock
  5.0 V ± 10% at 8 MHz main clock
- Packages : 64-pin SDIP (SDIP064-P-0750)
  64-pin QFP (QFP064-P-1420)

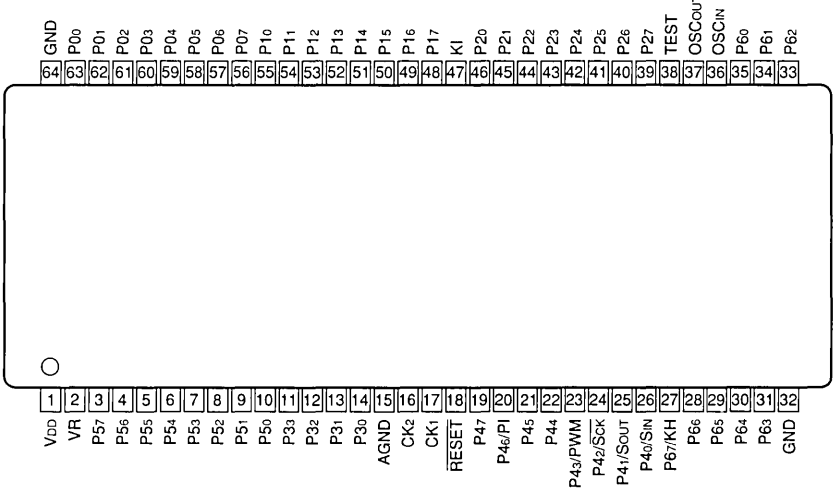
PIN CONNECTION

64-pin QFP

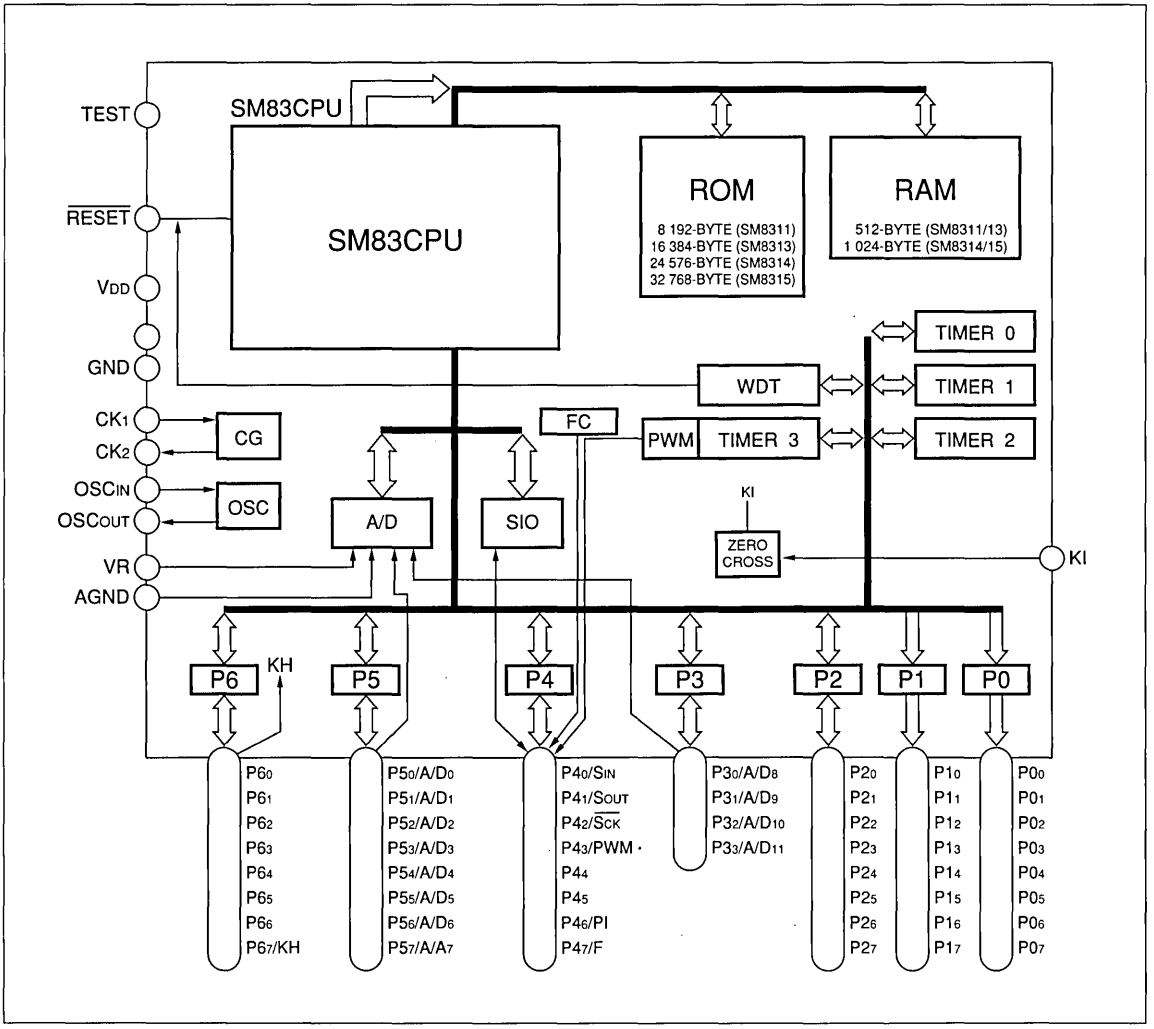
TOP VIEW



64-pin SDIP



BLOCK DIAGRAM



Nomenclature

A	: Accumulator
A/D	: A/D convertor unit
ALU	: Arithmetic logic unit
B, C, D, E	: General-purpose register
CG	: System clock generator
CTRL	: System control unit
FC	: F port control flag
H, L	: RAM address register
IE	: Interrupt enable register
IME	: Interrupt master enable flag
INST/DEC	: Instruction decoder
INT	: Interrupt control unit
PC	: Program counter
P0-P6	: Port register
PWM	: Pulse width modulator
SIO	: Serial interface
SP	: Stack pointer
TIMER 0-TIMER 3	: Counter/timer
WDT	: Watchdog timer
ZERO CROSS	: Zero cross unit

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$-$P0_7$	O	Output
$P1_0$-$P1_7$	O	Output
$P2_0$-$P2_7$	I/O	I/O
$P3_0$-$P3_3$	I	Input pin, analog voltage input
$P4_0$/S_{IN}	I/O, I	I/O, serial interface input
$P4_1$/S_{OUT}	I/O, O	I/O, serial interface input
$P4_2$/$\overline{S_{CK}}$	I/O	I/O, serial interface, clock I/O
$P4_3$/PWM	I/O, O	I/O, PWM wave output
$P4_4$, $P4_5$	I/O	I/O
$P4_6$/PI	I/O, I	I/O, pulse input
$P4_7$/F	I/O, O	I/O, audio output
$P5_0$-$P5_7$	I	Input, analog voltage input
$P6_0$-$P6_6$	I/O	I/O
$P6_7$/KH	I/O, I	I/O, external interrupt input
KI	I	External interrupt input, zero cross comparing voltage input
$\overline{\text{RESET}}$	I	Reset signal input
CK_1	I	System clock OSC pins (ceramic OSC : 8 MHz)
CK_2	O	
OSC_{IN}	I	Measuring clock OSC pins (crystal OSC : 32.768 kHz)
OSC_{OUT}	O	
TEST	I	Test pin (connect to GND)
VR, AGND	I	A/D converter reference voltage input
V_{DD}, GND	I	Power supply

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Power supply	V_{DD}		−0.3 to +6.5	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Max. output current	I_{OH}	High-level output current	−4	mA
	I_{OL1}	Low-level output current ($P0_0$-$P0_7$, $P1_0$-$P1_7$)	+30	mA
	I_{OL2}	Low-level output current (all but $P0_0$-$P0_7$, $P1_0$-$P1_7$)	+4	mA
Total output current	ΣI_{OH}	High-level output current (all outputs)	−20	mA
	ΣI_{OL1}	Low-level output current ($P0_0$-$P0_7$, $P1_0$-$P1_7$)	+100	mA
	ΣI_{OL2}	Low-level output current (all but $P0_0$-$P0_7$, $P1_0$-$P1_7$)	+20	mA
Operating temperature	T_{OPR}		−20 to +70	°C
Storage temperature	T_{STG}		−55 to +150	°C

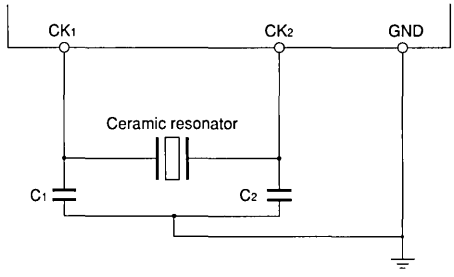
RECOMMENDED OPERATING CONDITIONS

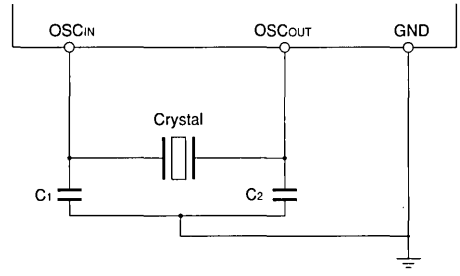
PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Power supply voltage	V_{DD}		2.7 to 5.5	V
Instruction cycle	ts	V_{DD} = 2.7 to 5.5 V	1.0 to 4.0	µs
		V_{DD} = 4.5 to 5.5 V	0.5 to 4.0	

NOTE :

The V_{DD} must be a single supply in the range between 3 V and 5 V. When changing the voltage, do while in SM831 x is in the stop mode.

Oscillation Circuit





DC CHARACTERISTICS

(V_{DD} = 2.7 to 5.5 V, Ta = –20°C to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage		V_{IH1}		0.8 x V_{DD}		V_{DD}	V	1
		V_{IL1}		0		0.2 x V_{DD}		
		V_{IH2}		V_{DD}–0.5		V_{DD}	V	2
		V_{IL2}		0		0.5		
Input current		I_{IL}	V_{IL} = 0 V, V_{DD} = 5 V		–50		µA	3
		I_{IH}	V_{IH} = 5 V, V_{DD} = 5 V		50		µA	4
		I_I	V_{IN} = V_{DD}			10	µA	5
Output current		V_{OH1}	I_{OH} = –1 mA, V_{DD} = 5 V	V_{DD}–0.5			V	6
		V_{OL1}	I_{OL} = –10 mA, V_{DD} = 5 V			2		
		V_{OH2}	I_{OH} = –1 mA, V_{DD} = 5 V	V_{DD}–0.5			V	7
		V_{OL2}	I_{OL} = 1 mA, V_{DD} = 5 V			0.5		
A/D conversion	Resolution		V_R = V_{DD} = 5 V		8		bits	
	Accuracy		fs = 1 MHz			± 2.5	LSB	
Zero cross comparison voltage			fs = 1 MHz, V_{DD} = 5 V	0.5 x V_{DD}–0.1 V	0.5 x V_{DD}	0.5 x V_{DD}+0.1 V	V	
Supply current		I_{DD}	fs = 1 MHz		6		mA	8
		I_{DDH}	fs = 1 MHz, HALT mode		2			
		I_{DDS}	Transmit-stop, STOP mode		1	10	µA	9

NOTES :

1. Applicable pins : $P2_0$-$P2_7$, $P3_0$-$P3_3$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, CK_1, TEST, $P4_1$, $P4_3$, $P4_4$, $P4_5$, $P4_7$.
2. Applicable pins : $\overline{RESET}$, OSC_{IN}, KI, KH, $P4_0/S_{IN}$, $P4_2/\overline{S_{CK}}$, $P4_6$/PI.
3. Applicable pins : $\overline{S_{CK}}$, $\overline{RESET}$.
4. Applicable pins : $P2_0$-$P2_7$, $P4_0$-$P4_7$, $P6_0$-$P6_7$, TEST.
5. Applicable pins : $P3_0$-$P3_3$, $P5_0$-$P5_7$.
6. Applicable pins : $P0_0$-$P0_7$, $P1_0$-$P1_7$.
7. Applicable pins : $P2_0$-$P2_7$, $P4_0$-$P4_7$, $P6_0$-$P6_7$, CK_2, OSC_{OUT}.
8. No load condition, V_{DD} = 5 V.
9. No load condition, V_{DD} = 5 V, OSC_{IN} = GND, VR = GND, constant input.

SYSTEM CONFIGURATION

Instruction Executing Timing

The SM83 CPU core uses pipeline method to speed instruction execution. With this method, OP code fetching cycle and execution cycle are overlapping, i.e. while the current instruction is being executed, the OP code of the next instruction is fetched.* The instruction executing time is the sum of the OP code fetching time and the net instruction executing time necessary to process the job directed by the instruction. The overlapping cycle time can shorten "operation time" of the microcomputer to "net instruction executing time" by its amount. The program can ignore OP code fetching time except for the first fetching time after hardware reset.

Exceptions are the memory access instruction and jump instruction : while in the execution cycle of these instructions, the OP code of the next instruction is not fetched. Therefore, OP code fetch cycle of the next instruction follows the execution cycle of the previous instruction.
Figure 1 shows instruction executing timing.

* Transferring of ROM content to the instruction decoder which translates the content as instruction.

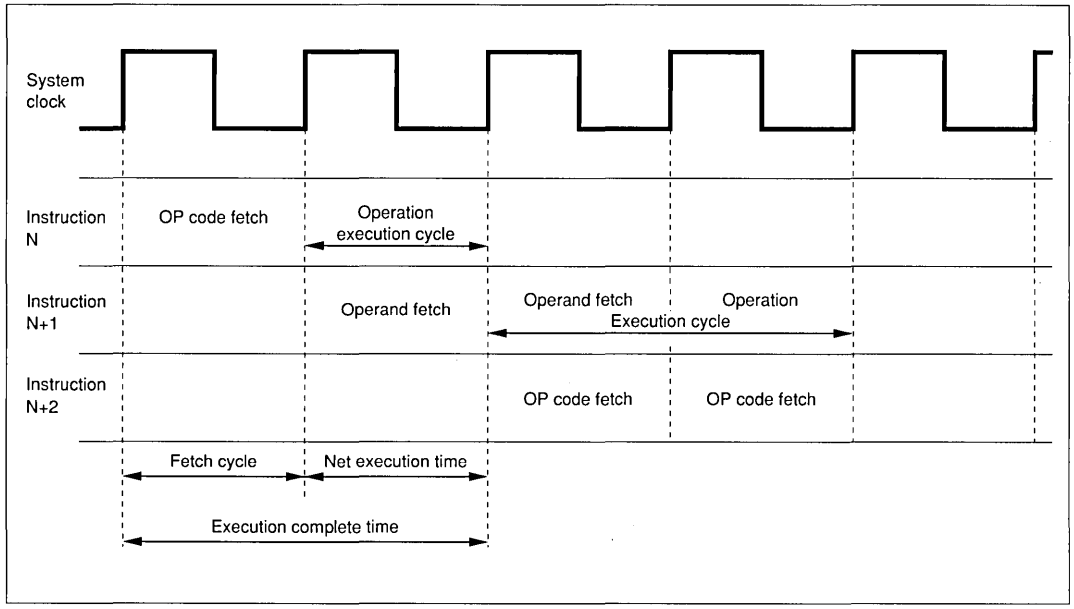


Fig. 1 Fundamental Instruction Execution Timing Diagram

Address Space

An address space of the SM831x occupies 64 k-byte in total.

Do not use address locations reserved for the system. Otherwise correct operation of the microcomputer will not be guaranteed.

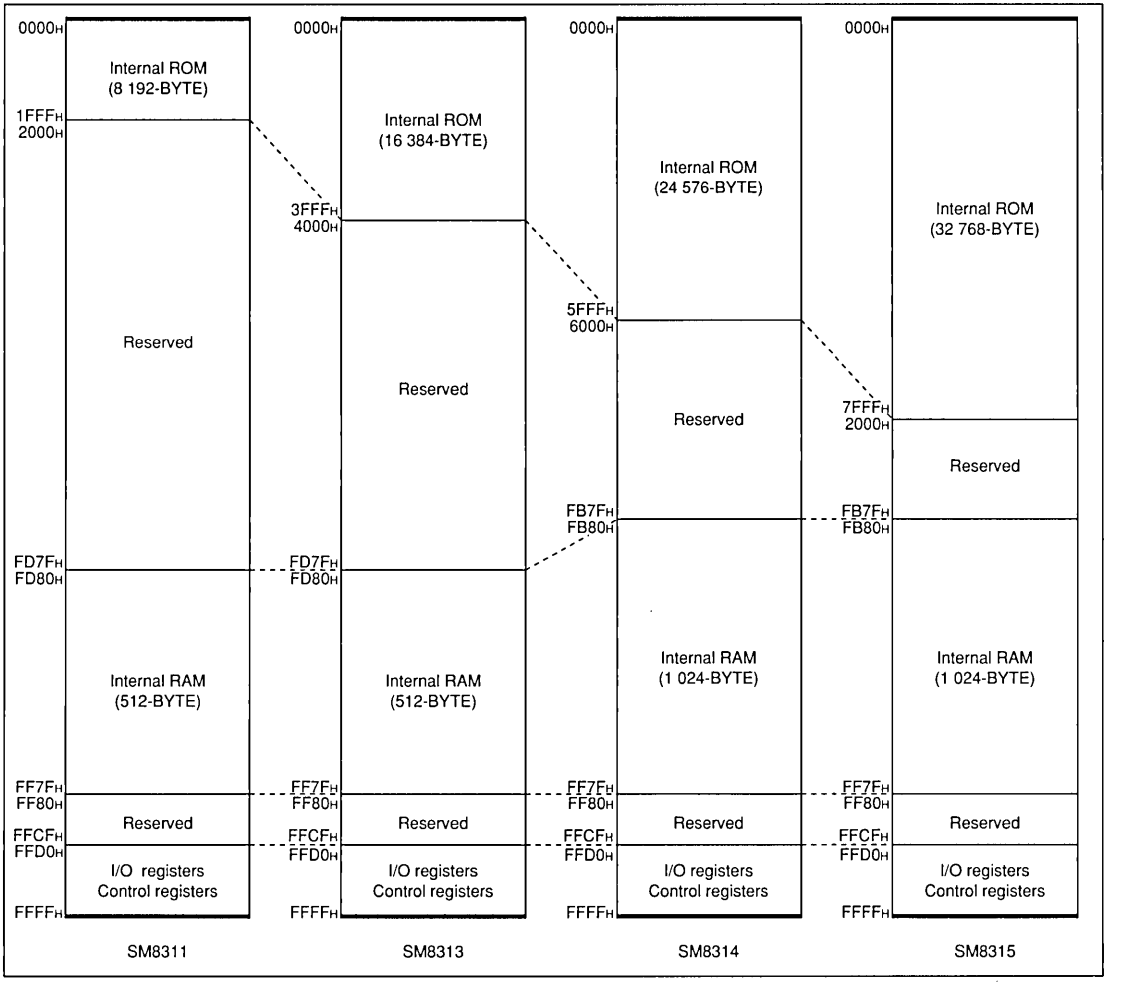


Fig. 2 Address Space

Program Memory (ROM)

The program memory (ROM) stores the user programs. It occupies 8 192-byte (SM8311), 16 384-byte (SM8313). Upon hardware-reset, user program will start at address 0000H.

The internal ROM is assigned with 9-interrupt vector address and the jump addresses of RST instruction.

Table 1 Vector Addresses

ADDRESS	VECTOR
0000	Start address upon reset/RST0
0008	RST1
0010	RST2
0018	RST3
0020	RST4
0028	RST5
0030	RST6
0038	RST7
0040	INT0 : External input pin (KI) interrupt
0048	INT1 : Timer 0 overflow interrupt
0050	INT2 : Timer 1 overflow interrupt
0058	INT3 : Timer 2 overflow interrupt
0060	INT4 : External input pin (KH) interrupt
0068	INT5 : Timer 3 overflow/pulse width measurement completion interrupt
0070	INT6 : Serial interface interrupt
0078	INT7 : A/D converter interrupt
0080	NMI : Non-maskable interrupt (watch dog timer)

Data Memory (RAM)

Address locations FD80H through FF7FH are assigned for the data memory (RAM) which stores data such as operation results and stack. The memory capacity of the RAM of the SM8311/8313 is 512-byte.

The memory capacity of the RAM of the SM8314/8315 is 1 024-byte.

Control Registers

Control registers including I/O registers perform special control. These registers are located at address locations from FFD0H to FFFFH. Most of functions of the SM831x is controlled by manuplating bits of these control registers.

Do not access the reserved addresses, or proper microcomputer operation is not expected.

CPU Core Structure

The CPU core incorporates the instruction decoder (INST. DEC.), arithmetic logic unit (ALU), accumulator (A), general purpose registers (B, C, D, E, H, L), program counter (PC), stack pointer (SP), flag register (F), interrupt control unit (INT), interrupt master enable flag (IME), interrupt enable register (IE) and interrupt flag register (IF).

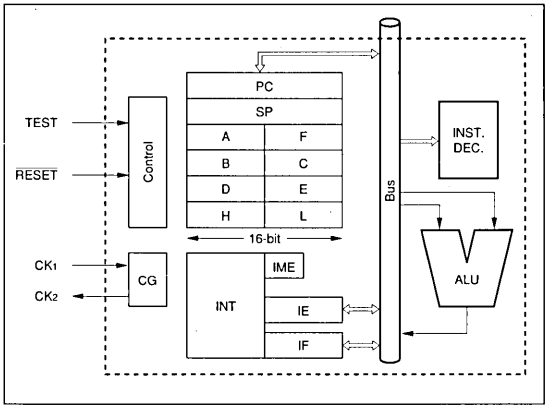


Fig. 3 SM83 CPU Core Internal Structure

• Accumulator (A)

This is an 8-bit register used to hold arithmetic operation results and data. Sometimes referred to as A register.

• General purpose registers (B, C, D, E, H, L)

These are 8-bit registers used as auxiliary registers to accumulator, and also used as register pair (BC, DE, HL) to function as data pointer.

• **Flag register (F)**

bit	7	6	5	4	3	2	1	0
	Z	N	H	Cy	–	–	–	–

Consists of 4 types of flags, each of which is set or clear as a result of execution of respective instruction.

Z : Zero flag
N : Negative flag
H : Half-carry flag
Cy : Carry flag

Clock Generator

The SM831x is provided with two clock generators : the system clock generator (CG) and real time clock generator OSC. The 12-bit prescaler following the CG divides the system clock and provides 4-timing clock for timers and counters. Recommended main clock frequency is 8 MHz (4 MHz) for SM8311 (13/14/15) to obtain the 2 MHz (1 MHz) system clock. Connecting a 32.768 kHz crystal across OSC_{IN} and OSC_{OUT} pin generates the clock for the real time clock which can drive Timers 0 and 1 to count out at every second.

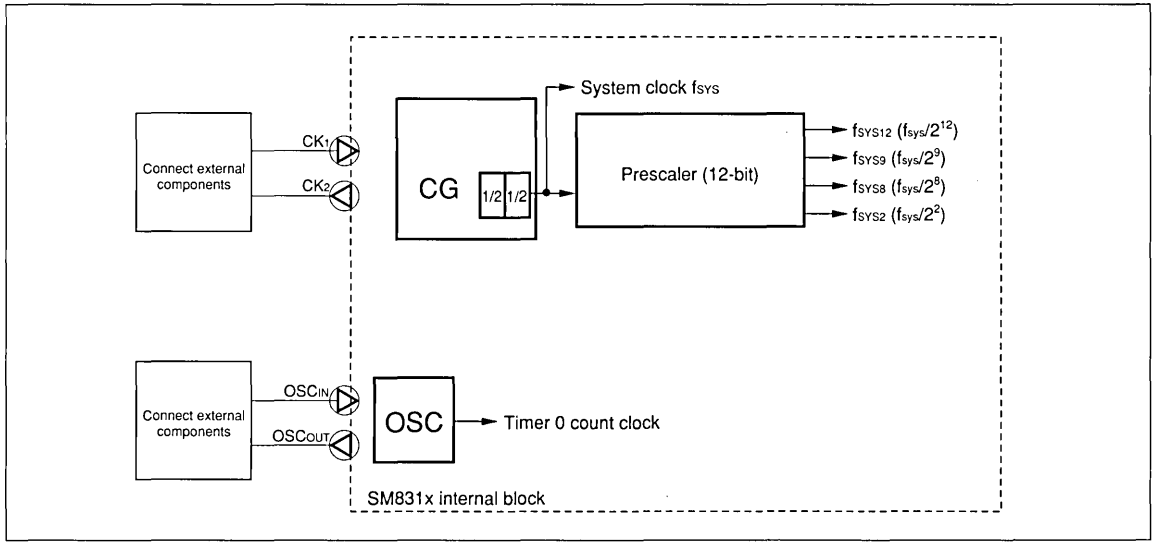


Fig. 4 Clock Generators

I/O Ports

The SM831x has 52-I/O port. They are :

12-input port
16-output port
24-I/O port

These ports have dual functions for various data inputs or/and outputs.

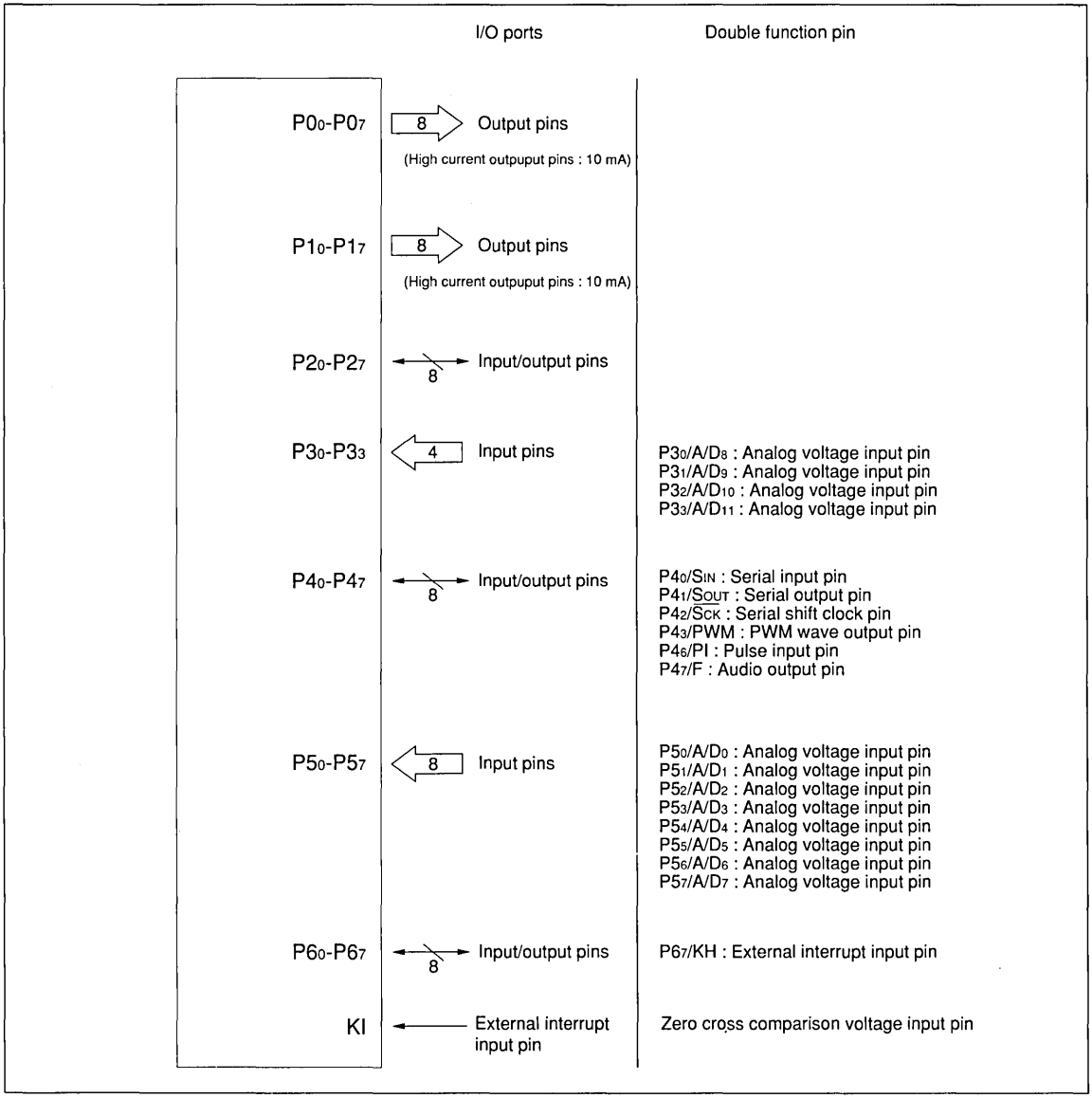


Fig. 5 Port Function

• **P0 port**

Each pin of this 8-bit port outputs a high current. CMOS process, operates from 5 V and flows approx. 10 mA sink current.

The data register P0 (memory address FFD0H) is connected to P0 port.

Table 2 Output from P0 Port

BIT SETTING OF DATA REGISTER P0 P0i	STATE OF P0i PIN
0	Low level
1	High level

(i = 0 to 7)

• **P1 port**

Each pin of this 8-bit port outputs a high current. CMOS process, operates from 5 V and flows approx. 10 mA sink current.

The data register P1 (memory address FFD1H) is connected to P1 port.

Table 3 Output from P1 Port

BIT SETTING OF DATA REGISTER P1 P1i	STATE OF P1i PIN
0	Low level
1	High level

(i = 0 to 7)

• **P2 port**

This is an 8-bit I/O port with each pin provided with a pull-down resistor.

The data register P2 (memory address FFD2H) is connected to P2 port. Selection of the direction of each bit of this port is by means of the bit setting of the control register P2C (address FFE2H). The bits in the P2C ($P2C_0$ to $P2C_7$) correspond to pins $P2_0$ to $P2_7$ of the P2 port in that order.

Table 4 Direction Setting of P2 Port

BIT SETTING OF CONTROL REGISTER P2C P2Ci	STATE OF P2i PIN
0	Input pin
1	Output pin

(i = 0 to 7)

• **P3 port**

P3 pin can also serve as analog voltage input. The pins serving as analog voltage input are called "A/D pins". Otherwise, they are called "digital input pins". Pins $P3_0$ to $P3_3$ are usually called A/D_8 to A/D_{11} pins.

The data register P3 (memory address FFD3H) is connected to port P3. This is a read only register. Selection of the direction of each bit of this port is by means of the bit setting of the control register P3C (address FFE3H). The bits in the P3C ($P3C_0$ to $P3C_3$) correspond to pins $P3_0$ to $P3_3$ of the P3 port in that order.

Table 5 Function Setting of Port P3

BIT SETTING OF CONTROL REGISTER P3C P3Ci	STATE OF P3i PIN
0	A/D pin
1	Digital input pin

(i = 0 to 3)

• P4 port

The port includes 8-I/O pin. Each I/O pin is provided with a pull-down resistor. In some setting, however, $P4_2$ pin is connected to a pull-up resistor. The port also assumes the following :

Serial interface pins (See "Serial Interface")

$P4_0 \rightarrow S_{IN}$

$P4_1 \rightarrow S_{OUT}$

$P4_2 \rightarrow \overline{S_{CK}}$

PWM wave output pin (See "PWM WAVEFORM OUTPUT" in Timer/Counter)

$P4_3 \rightarrow$ PWM

Pulse input pin (See "PULSE WIDTH MEASUREMENT" in Timer/Counter)

$P4_6 \rightarrow$ PI

Sound output pin

$P4_7 \rightarrow$ F

Control registers SRC, PLSC and TMC1 set the function of each port pin.

The data register P4 (memory address $FFD4_H$) is connected to port P4. Selection of the direction of each bit of this port is by means of the bit setting of the control register P4C (address $FFE4_H$). The bits in the P4C ($P4C_0$ to $P4C_7$) correspond to pins $P4_0$ to $P4_7$ of the P4 port in that order.

Using P4 pin as sound output pin

$P4_7$ pin can be used as sound output pin (F pin). Setting bit 6 of the control register TMC1 to "1" cuases the $P4_7$ pin to function as a sound output pin. Pulse selection for sound is by means of the setting of the bit 5 of the control register TMC1.

Table 6 Function Selection of $P4_7$

BIT 5 OF REGISTER TMC1	PULSE TO BE OUTPUT
0	f_{SYS9} (divided-by-2^9 system clock : 4 kHz when main clock is 8 MHz)
1	PWM wave output pulse (same pulse as PWM wave from pin $P4_3$)

To use $P4_7$ as normal input pin, set the bit 6 of the control register TMC1 to "0".

• P5 port

The port is a set of input (digital) only 8-bit pin. P5 pin can also serve as analog voltage input. The pins serving as analog voltage input are called A/D pins. Otherwise, they are called digital input pins. Pins $P5_0$ to $P5_7$ are usually called A/D_0 to A/D_7 pins. The configuration of this port is same as P3. The data register P5 (memory address $FFD5_H$) is connected to port P5. This is a read only register. Selection between the functions (normal and A/D pins) of each bit of this port is by means of the bit setting of the control register P5C (address $FFE5_H$). The bits in the P5C ($P5C_0$ to $P5C_7$) correspond to pins $P5_0$ to $P5_7$ of the port P5 in that order.

Table 7 Function Setting of Port P5

BIT SETTING OF CONTROL REGISTER P5C P5Ci	STATE OF P5i PIN
0	A/D pin
1	Digital input pin

(i = 0 to 7)

• P6 port

This is an 8-bit I/O port with each pin provided with a pull-down resistor.

The data register P6 (memory address $FFD6_H$) is connected to port P6. $P6_7$ serves also as external interrupt input pin (KH). Selection of the direction of each bit of this port is by means of the bit setting of the control register P6C (address $FFE6_H$). The bits ($P6C_0$ to $P6C_7$) in the P6C correspond to pins $P6_0$ to $P6_7$ of port 6 in that order.

Table 8 Direction Setting of Port P6

BIT SETTING OF CONTROL REGISTER P6C P6Ci	STATE OF P6i PIN
0	In
1	Out

(i = 0 to 7)

Setting as external input pin (KH)

Pin $P6_7$ can be used as an external interrupt input (KH). Set pin $P6_7$ to input and set the external interrupt control register EXTC, interrupt enable register IE and IME flag.

Table 9 External Interrupt Input Pin (KH = $P6_7$)

PIN NAME	SETTING OF INTERRUPT ENABLE REGISTER (IE)	SETTING OF EXTERNAL INTERRUPT CONTROL REGISTER (EXTC)		INTERRUPT CONDITION
$P6_7$	Bit IE4 = 1	Bit EXTC4 = 0	Bit EXTC3 = 0	Rising edge
			Bit EXTC3 = 1	Falling edge
		Bit EXTC4 = 1	Bit EXTC3 = 0	High level
			Bit EXTC3 = 1	Low level

• KI port

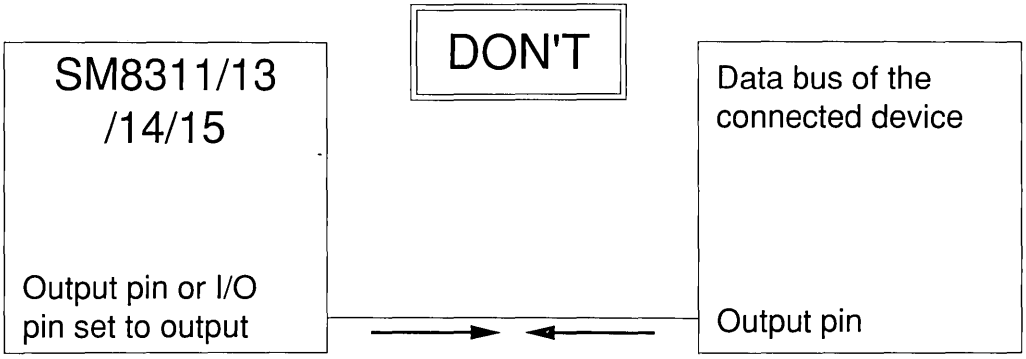
This is an 1-bit external interrupt input port.
KI pin is a 1-bit input having schmitt trigger circuit.
It assumes the following pin functions.

1. External interrupt input (standby mode release)
2. Zero-cross detection
   KI pin is used in conjunction with interrupt operation.

CAUTION :

Connecting considerations of I/O port

When using an I/O port as bidirectional bus such as data bus, avoid setting the I/O port to output when the target pin is also set to output.
Whenever the both output data conflict each other, system failure will be causes due to damage to circuits or instantaneous supply voltage drop.



FUNCTIONAL DESCRIPTION

Hardware Reset Function

Hardware reset is a function to restore the SM831x to its initial state. A Low level on the $\overline{\text{RESET}}$ pin resets the chip and the program is started at address 0000H. Other functions of hardware reset are as follows :

- Clear the interrupt master enable flag IME, interrupt mask register IE and interrupt flag IF and disables all maskable interrupts.
- Set the predetermined registers and ports to their initial state as shown in Table 10. Status of the remaining registers and ports are undefined.

SECTIONS TO BE INITIALIZED UPON HARDWARE RESET

The following registers and ports are put into the state as shown below when the hardware reset sequence completes.

Table 10 State of SM831x after Hardware Reset

PIN NAME	LEVEL AFTER RESET	I/O SETTING
P0, P1	Low level	Output
P2, P4, P6	Low level (with pull-down resistor)	Input

REGISTER NAME	CONTENT OF REGISTER AFTER RESET
P0, P1, P2, P4, P6	00H
P2C, P4C, P6C	00H
KC	E0H
SRC	C0H
ADCC	20H
TMC0	40H
TMC1	00H
STPR	A0H
IE	00H
IF	00H
IME	0
PC	0000H

NOTES :

1. Initialization

The status of the devices shown Table 10 are unknown when reset by hardware and should be correctly set through the program as earlier as possible.

Refer to SM831x User's manual for necessary operations.

- Control register P3C (sets the mode of pin 3)
- Stack pointer SP (specifies the start address of the stack area)

2. Pin initialization time

The mode of and level on pins are definitely set upon hardware reset release (except for pin P3). The following specific operations must be taken into designing considerations.

- Direct reset

When the supply voltage is applied (the level on $\overline{\text{RESET}}$ pin goes High), the mode and the output level (set by the pull-down resistor) of that pin are established. This condition applies to most of input only pins.

- Clocked reset (indirect reset)

After power-on and the system clock generator (CG) starts, the mode and output level of certain pins are established after the period equal to several clocks has elapsed. The output pins and the I/O pins containing the direction register are included in this category.

HARDWARE RESET PROCEDURE

Apply a Low level (GND level) to $\overline{\text{RESET}}$ pin for a period longer than the specified value. The SM831x is then clear and the predetermined flags, registers and ports are put into the initial state.

HARDWARE RESET RELEASE PROCEDURE

When the $\overline{\text{RESET}}$ pin goes High, the SM831x starts counting the main clock pulses. Upon counting the system clock pulses for the specified period, it exits hardware reset condition and executes the program at address 0000_H.

Release of hardware reset can be automatically done by just removing the Low input since the $\overline{\text{RESET}}$ pin level is pulled up by a resistor.

POWER-ON RESET CIRCUIT

Power-on reset circuit must be established to automatically hardware reset the SM831x upon power-on. A power-on reset circuit is shown in Fig. 6.

Typical capacitor is 0.1 µF. Exact value should be determined on the actual board.

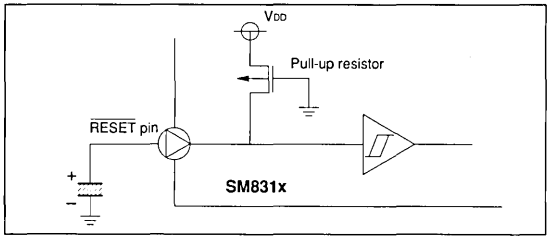


Fig. 6 Power-On Reset Circuit

Standby Feature (Halt/Stop)

Standby feature saves power by pausing the program. The mode which allows the program to run is called the operation mode and the mode which does not allow the program to run is called the standby mode. The standby mode is further divided into two modes : "HALT" mode during which only the system clock is turned off and "STOP" mode during which the main clock is turned off, disabling almost of all system functions.

In either of the standby modes, the output ports, internal registers and internal RAMs are allowed to retain their contents.

Transition from operation mode to a standby mode is started by implementing HALT or STOP instruction.

Return from the halt mode is made possible by a setting of the interrupt enable register IE; and return from the stop mode by the bit setting of the stop cancel register STPR. Alternative to these returning means is the entry of the reset signal.

The SM831x is provided with 9-event (including reset input) that are used to return from the halt mode, and 7 (also including reset input) to return from stop mode.

Table 11 Comparison Between of Halt and Stop Modes

DIFFERENCE	HALT MODE	STOP MODE
What stopped	Functions that do not require system clock.	Functions that do not require external clock or clock generated across OSC_{IN} and OSC_{OUT} pins.
Conditions for entering standby mode	Register IE is set. The bit of the register IF corresponding to standby release event is reset.	Register STPR is set. Registers IE and IF are reset.
Conditions for exiting standby mode	Reset input Halt mode release event set in the register IE. Interrupt condition set in the flag IME	Reset input Stop release event set in the register STPR
Standby release events	9 (including reset)	7 (including reset)

HALT MODE

Execution of the halt instruction puts the SM831x into the halt mode and the system clock is turned off, stopping the current program. Since the main clock oscillator connected across CK_1 and CK_2 pins is active during the halt mode, devices requiring no system clock are kept in-operation. These devices are serial I/Os and timers.

The halt mode is disabled by one of the following means and the program will start again.

• Release by reset input

A Low level on the $\overline{\text{RESET}}$ pin will cause the SM831x to exit halt mode and start program at address 0000_H, the same way as with normal resetting.

• Release by interrupt

When an interrupt event occurs, the SM831x exits the halt mode.

When a bit in the enable flag IE is set, the SM831x exits the halt mode if the interrupt request corresponding to the bit is generated. The action of the SM831x after exiting the halt mode is determined by the setting of the IME flag.

- IME = 0

  The program will start at the location following the halt instruction address. Note that the bit in the interrupt flag register IF that caused the previous interrupt is kept set.

- IME = 1

  After returning from the halt mode, the program will start at the vectored address. This is the same as with the normal interrupt handling process.

STOP MODE

Executing the STOP instruction puts the SM831x to the stop mode and turns off the main clock and system clock. All operations stop. Exception are serial I/Os, timers operating on external clock and clock generated across pins OSC_{IN} and OSC_{OUT}.

The stop mode is canceled by the following factors and the program starts after the specified time (return time).

• Reset input

A Low level on the $\overline{\text{RESET}}$ pin will cause the SM831x to exit the stop mode and start program at address 0000_H, quite the same as with normal resetting. For detailed description of reset, refer to "Hardware Reset Function"

• Interrupt request

While operating on the external clock or clock generated across pins OSC_{IN} and OSC_{OUT}, an interrupt from a serial I/O, timer, or external input pin KI or KH causes the program to continue at the address following the STOP instruction.

• Stop release register STPR

(STPR, $FFFD_H$, R/W)

Bit	7	6	5	4	3	2	1	0
STPR	–	SR6	–	SR4	SR3	SR2	SR1	SR0

The stop release register STPR determines interrupts that are used to release the stop mode. This register will not be effective during the halt mode. There are 6-interrupt sources for releasing the stop mode.

Table 12 Stop Mode Release Bits

STPR BIT	STOP MODE RELEASE EVENT 1 : Enable 0 : Disable
SR0	Low level input from KI pin (generation of interrupt request signal IRQ0)
SR1	Timer 0 overflow (generation of interrupt request signal IRQ1)
SR2	Timer 1 overflow (generation of interrupt request signal IRQ2)
SR3	Timer 2 overflow (generation of interrupt request signal IRQ3)
SR4	Interrupt request from KH pin ($P6_7$) (generation of interrupt request signal IRQ4)
–	
SR6	Interrupt request upon end of serial I/O (generation of interrupt request signal IRQ6)
–	

Interrupt

The SM831x is designed to accommodate 9-independent maskable interrupt (7-internal and 2-external) which can be assigned to 9-interrupt vector address.

One nonmaskable interrupt is available with the SM831x for use with a watch dog timer.

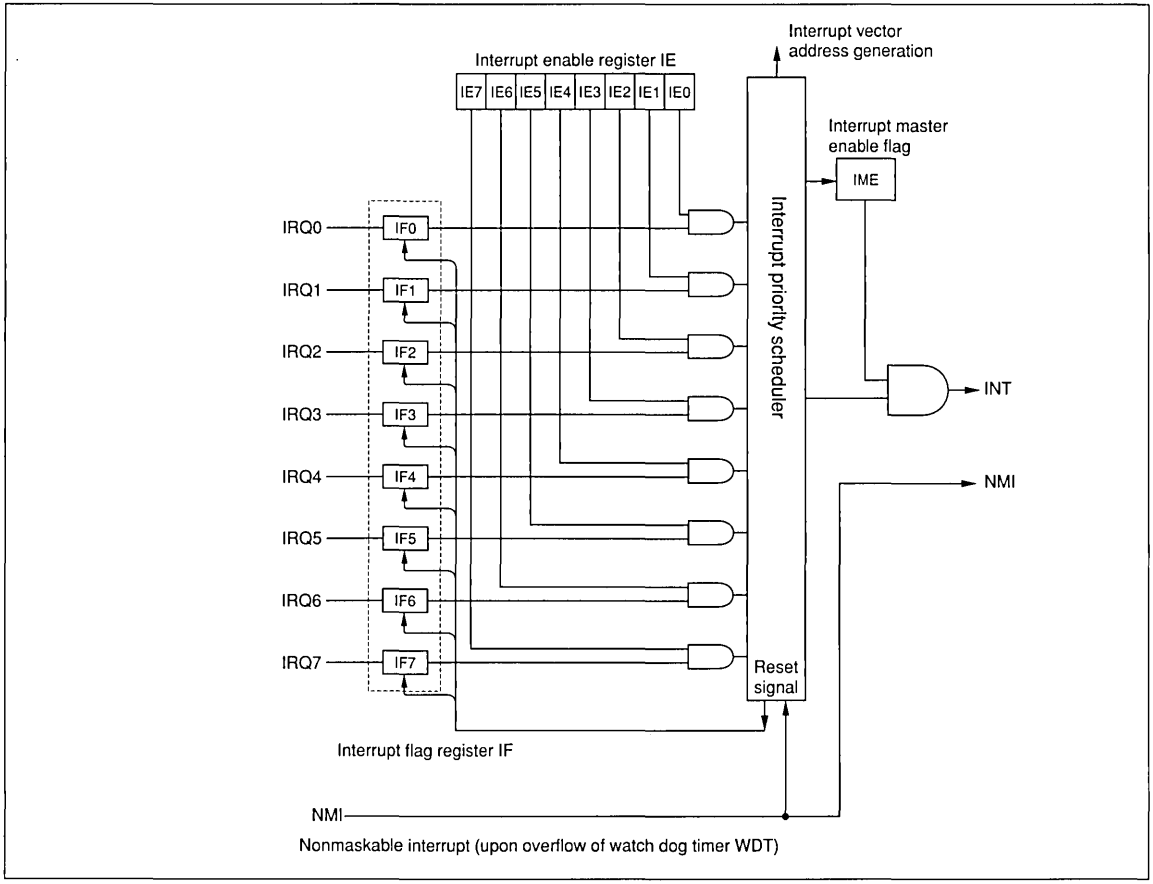


Fig. 7 Interrupt Control Block

INTERRUPT PRIORITY AND VECTOR ADDRESS

PRIORITY LEVEL	ADDRESS	INTERRUPT EVENT	MASKABLE
1	0080	NMI : nonmaskable interrupt; Overflow of watch dog timer	No
2	0040	IRQ0 : External interrupt (KI) or zero cross detect input	Yes
3	0048	IRQ1 : Timer 0 overflow interrupt	Yes
4	0050	IRQ2 : Timer 1 overflow interrupt	Yes
5	0058	IRQ3 : Timer 2 overflow interrupt	Yes
6	0060	IRQ4 : External interrupt ($P6_7$/KH)	Yes
7	0068	IRQ5 : Timer 3 overflow interrupt or end of pulse width measurement ($P4_6$)	Yes
8	0070	IRQ6 : Serial interface	Yes
9	0078	IRQ7 : End of A/D conversion	Yes

INTERRUPT FLAGS, REGISTER

• Interrupt master enable flag IME

This register is used to enable or disable all the maskable interrupts simultaneously.

Executing the EI instruction sets the master enable flag IME, enabling the maskable interrupts. Executing DI instruction resets the IME, disabling the maskable interrupts.

STATE OF IME FLAG	INTERRUPT
1	Enable
0	Disable

• Interrupt flag register IF

(IF, $FFFE_H$, R/W)

Bit	7	6	5	4	3	2	1	0
IF	IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0

When interrupt event (IRQ0 to IRQ7) occurs, corresponding bit (IF0 to IF7) in the interrupt flag register IF is set to "1". At the end of the interrupt process, the bit in the interrupt flag register IF is automatically clear. If the interrupt event is left unprocessed, the bit remains "1" until it is forced to clear by a program.

• Interrupt enable register IE

(IE, $FFFF_H$, R/W)

Bit	7	6	5	4	3	2	1	0
IE	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0

This register is used to individually enable or disable 9-maskable interrupt. Setting a bit in this register to "1" enables corresponding interrupt; and "0" disables the interrupt. The setting of the interrupt enable register is made effective when the interrupt master enable flag IME is set.

The IE register also sets the halt mode release conditions.

STATE OF REGISTER IE BIT	INTERRUPT
1	Enable (as well as halt mode release enable)
0	Disable (as well as halt mode release disable)

MASKABLE INTERRUPTS

Maskable interrupts are selectively enabled or disabled. When a maskable interrupt occurs, it sets the corresponding bits in the flag register IF to 1 level. If the following 2 conditions are met, the microcomputer processes the interrupt, starting with the cycle following the end of the execution of the current instruction sequence.

- Interrupt master enable flag IME is set.
- Corresponding interrupt enable register IE bit is set at 1 level.

IF the above conditions are not met, the interrupt flag register IF bit remains 1 level. Setting flag IME and IE bit forces the microcomputer to immediately start the interrupt processing.

• Simultaneous interrupts

In the flag register IF, the bits corresponding to the interrupts are set to 1 level. The interrupt having the highest priority only is accepted.

Other interrupt(s) is suspended until one of the following conditions is satisfied.

- Upon finishing the current interrupt processing, RET1 instruction is executed to return to the main routine and to set the master enable flag IME to "1" again. This starts the processing of a suspended interrupt.
- Master enable flag IME is set to "1". And a suspended interrupt is processed. Because two interrupts are simultaneously processed, 2 more stack stages are used.

NON-MASKABLE INTERRUPT NMI

Non-maskable interrupt (NMI) is an interrupt which cannot be masked by a program. The SM8311/8313 is provided with a NM1 (upon overflowing of the watch dog timer).

The SM831x treats the NM1 in a similar way as with maskable interrupt, except that any other interrupt is disabled while the program is in the NMI interrupt process routine. Another NMI is also ignored. Trying EI instruction while in the routine cannot set IME flag : multiple interrupt is impossible.

Only RETI instruction or a reset input allows to return from the non-maskable interrupt routine. When the control returns to the main routine, the interrupt master enable flag IME returns to the condition that was maintained before accepting the non-maskable interrupt provided that the neither EI nor DI has been executed in the non-maskable interrupt routine.

If EI or DI instruction has been executed during the non-maskable interrupt routine, the interrupt master enable flag IME is unchanged. If the EI instruction is executed during the non-maskable interrupt routine, the IME flag will be set upon returning to the main routine. If the DI instruction is executed during the non-maskable interrupt routine, the IME flag will be clear.

The SM831x will follow the normal reset sequence when returning from non-maskable interrupt routine when a reset signal is entered, resetting all flags and registers associated with that interrupt, ignoring all processes made to them.

Timer/Counter

The SM831x contains 12-bit prescaler, 3-set of 8-bit timer/counters, a 16-bit timer/counter and an 8-bit watch dog timer. These timer/counters handle periodic interrupt, interval timer operation, counting process, PWM waveform output and real time clock.

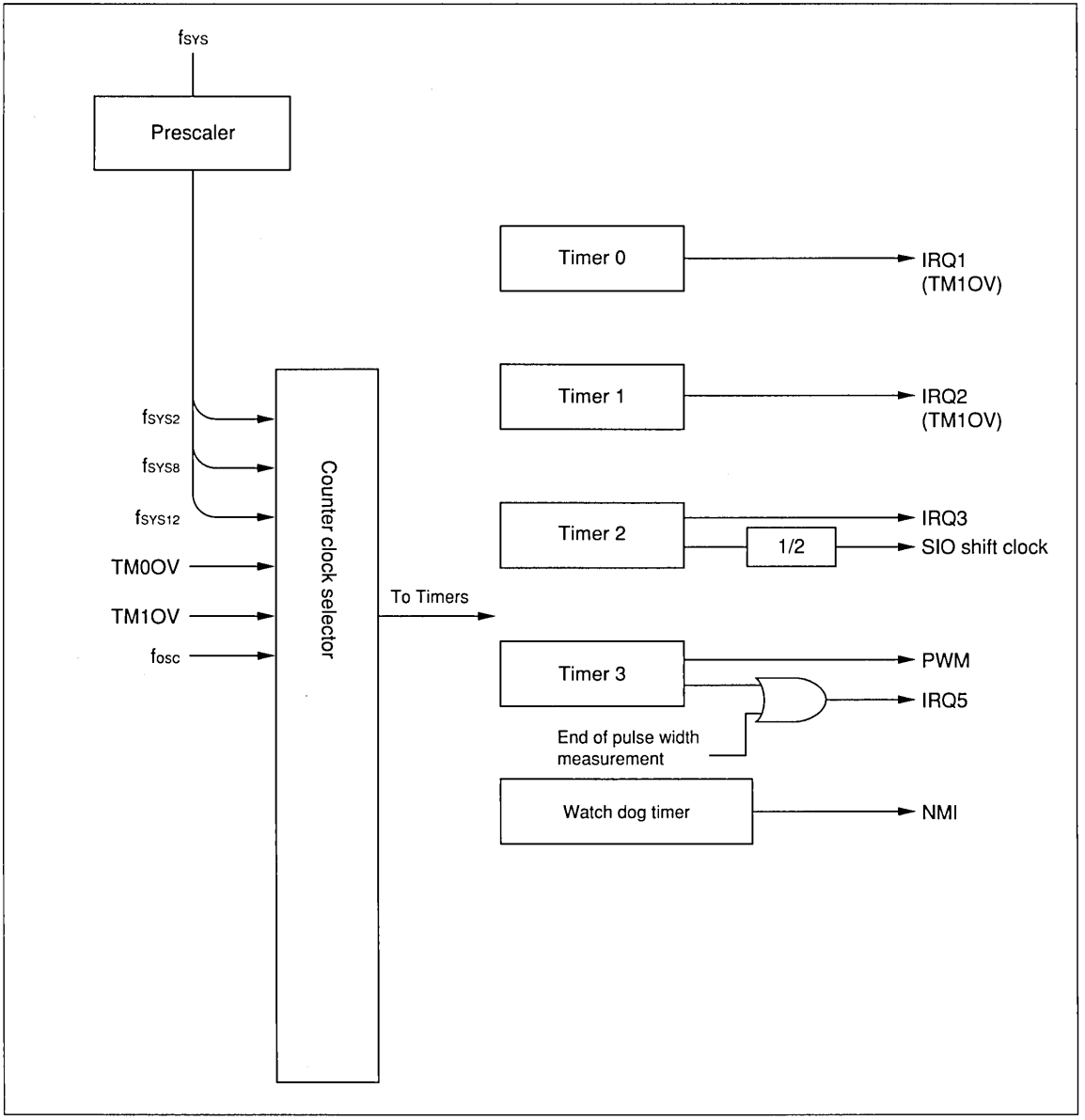


Fig. 8 Timer/Counter Block Diagram

SUMMARY OF TIMER/COUNTER FUNCTIONS

The timer/counters have the following functions.

• **Prescaler**

Functions as a 12-bit prescaler.
Generates the count clock to be fed to the timers.
Resets itself when the CPU is reset or in the stop mode, or when bit 6 of the control register TMC0 is clear.
The prescaler generates the following clocks.

CLOCK	CLOCK FREQUENCIES AVAILABLE FROM THE PRESCALER (8 MHz source clock)
f_{SYS2}	500 kHz
f_{SYS8}	7 812 Hz
f_{SYS9}	3 806 Hz (not use count clock)
f_{SYS12}	488 Hz

• **Timer 0**

Consists of 8-bit up counter TM0 and modulo register TM0M. Can be used as an interval timer or counter. Selection of the count clock to be applied to the up counter TM0 is through the control register TMC0. Selecting f_{OSC} as the count clock can generate 1 second signal by linking Timer 0 and Timer 1. The interrupt request signal IRQ1 will be generated by the overflow of the up counter TM0.

• **Timer 1**

Consists of 8-bit up counter TM1 and modulo register TM1M. Can be used as an interval timer and counter. Control of the Timer 1 including selection of the count clock to be applied to the up counter TM1 is through the control register TMC0. The interrupt request signal IRQ2 is generated by the overflow of the up counter TM1.

• **Timer 2**

Consists of up counter TM2 and modulo register TM2M. Can be used as an interval timer and counter. Selection of the count clock to be applied to the up counter TM2 is through the control register TMC0. The interrupt request signal IRQ3 will be generated by the overflow of the up counter TM2.

• **16-bit timer (Timer 3)**

Consists of up counters (TM3L, TM3H) and modulo registers (TM3LM, TM3HM). Can be used as a 16-bit timer by selecting the overflow of the counter TM3L as the count clock of the counter TM3H. TM3H is upper byte and TM3L lower byte. The control of the up counter TM3 including the selection of count clock to be applied to TM3 is through the control register TMC1. The interrupt request signal IRQ5 will be generated by the overflow of the up counter TM3.

• **PWM waveform output mode (Timer 3)**

The Timer 3 can generate PWM waveform, when the control register TMC1 is set to do so, and outputs to PWM pin ($P4_3$). The circuit configuration during PWM waveform output is similar to that of the Timer 3. The Timer 3H determines the High duration of waveform; Timer 3L Low duration.

High duration = (100_H – content of register TM3HM) x f_{SYS2}

Low duration = (100_H – content of register TM3LM) x f_{SYS2}

• **Pulse width measurement mode (Timer 3)**

The Timer 3 can be used to measure the pulse width by the setting of control registers TMC1 and PLSC. The measurement pulse can be put into pin PI($P4_6$). The High and Low durations of the input pulse are set from the control register PLSC.

Measurements = (times of Timer 3 overflows x 2^{16} +Timer 3 value) x f_{SYS2}

The interrupt request IRQ5 will be generated upon completion of pulse width measurement.

• 8-bit watch dog timer

Can be configured using 8-bit up counter WDT and modulo register WDTM. The watch dog timer is controlled by the setting of the control register TMC1. A write instruction to the watch dog timer transfers content of modulo register to the counter. The overflowing counter generates NMI (non-maskable interrupt) signal.

PRESCALER

The prescaler consists of 12-bit counter.

The prescaler divides the system clock and provides clocks to timers.

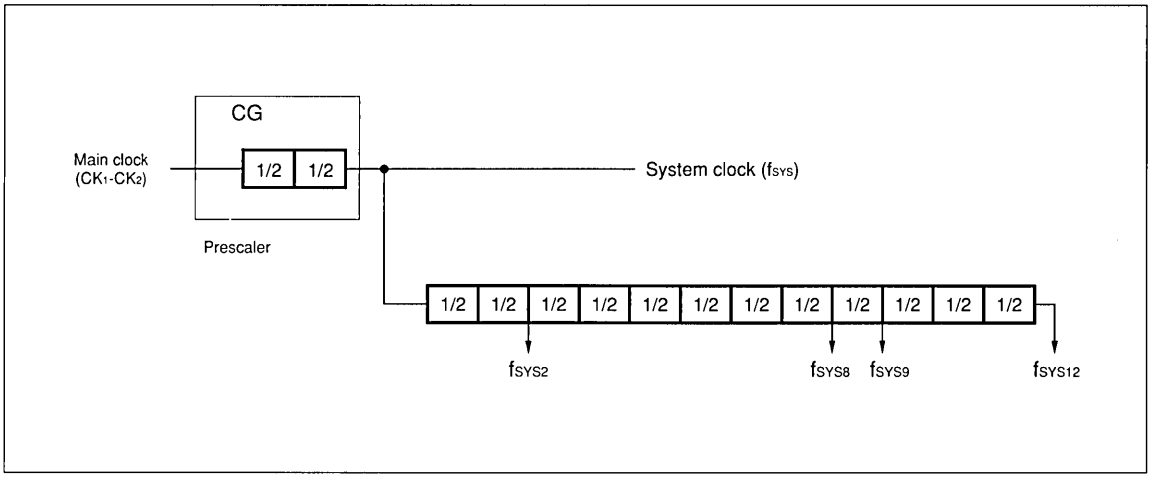


Fig. 9 Prescaler

• Clocks from the prescaler

The prescaler provides the following 3-clock frequency depending on dividing factors.

Table 13 Clocks from Prescaler

CLOCK	FREQUENCY
f_{SYS2}	Divided-by-2^2 system clock (f_{SYS})
f_{SYS8}	Divided-by-2^8 system clock (f_{SYS})
f_{SYS12}	Divided-by-2^{12} system clock (f_{SYS})

TIMER 0

Timer 0 is an 8-bit timer/counter and functions as an interval timer. It consists of the up counter TM0 and modulo register TM0M. Two registers are located at the same address (FFF0H.) During read operation, the up counter is automatically accessed; during write operation the modulo register.

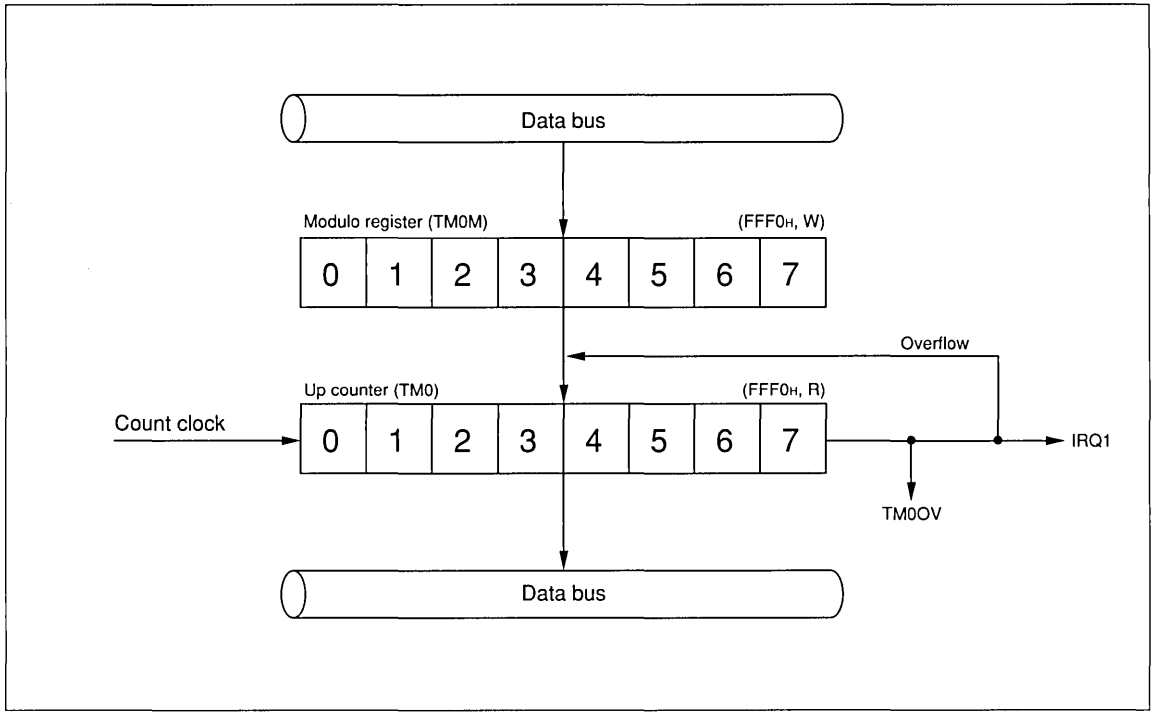


Fig. 10 Timer 0 Block Diagram

• Count operation

The up counter TM0 counts up the internal clock or external event clocks. When the TM0 overflows (TM0 = 00H), it reloads the content of modulo register TM0M as the initial value before starting the next cycle.

• Setting initial value of the up counter TM0

The initial value of the up counter TM0 is set to a value of the modulo register TM0M. The value is written into modulo register TM0M (constant register) and loaded to the up counter TM0 when TM0M write instruction is executed. The number of counts from the initial value to the final value (overflow) can be set from 1 to 256.

* The number of counts before overflow at the up counter TM0 = (100H–content of modulo register TM0M)

• Selection of count clock

The count clock to be applied to the up counter TM0 is selected by the lower two bits of the control register TMC0.

Table 14 Selection of Count Clock to Timer 0

BITS IN REGISTER TMC0		COUNT CLOCK SELECTED FOR TIMER 0
1	0	
0	*	None (no count operation)
1	0	f_{SYS2} (system clock/2^2)
1	1	f_{OSC} (clock from OSC_{OUT} pin)

* Don't care

• Count start/stop

To start the count, select the clock from control register TMC0 bits 0 and 1. The count clock applied to the counter TM0 is not synchronized with the counter start timing, the counter output will deviate up to one clock counting cycle in the first counts (until it causes overflow).

To force the Timer 0 to stop, clear the bit 1 of the control register to 0.

• Interrupt upon overflowing of up counter TM0

The up counter TM0 will generate an interrupt request (IRQ1) upon overflow. To do so, bit 1 of the interrupt enable register IE and interrupt master enable flag should be set to use the Timer 0 for the interrupt handling.

TIMER 1

Timer 1 is an 8-bit timer/counter consisting of the up counter TM1 and modulo register TM1M. These 2-register share the same address ($FFF1_H$). The up counter is accessed automatically during reading and the modulo register during writing.

• Selection of count clock

The count clock to be applied to the up counter TM1 is selected by bits 2 and 3 of the control register TMC0.

Table 15 Selection of Count Clock for Timer 1

BITS IN REGISTER TMC0		COUNT CLOCK SELECTED FOR TIMER 1
3	2	
0	0	None (no count operation)
0	1	Timer 0 overflow (TM0OV)
1	0	f_{SYS2} (system clock/2^2)
1	1	f_{SYS8} (system clock/2^8)

TIMER 2

Timer 2 is an 8-bit timer/counter consisting of the up counter TM2 and modulo register TM2M. These 2-register share the same address (FFF2H). The up counter is accessed automatically during reading and the modulo register during writing.

• Selection of count clock

The count clock to be applied to the up counter TM2 is selected by bits 4 and 5 of the control register TMC0.

Table 16 Selection of Count Clock for Timer 2

BITS IN REGISTER TMC0		COUNT CLOCK SELECTED FOR TIMER 2
5	4	
0	0	None (no count operation)
0	1	Timer 1 overflow (TM1OV)
1	0	f_{SYS2} (system clock/2^2)
1	1	f_{SYS8} (system clock/2^8)

16-BIT TIMER (TIMER 3)

This 16-bit timer/counter configuration is achieved by connecting two 8-bit timers. The 16-bit counter can be used as a 16-bit interval timer or for PWM signal generation or pulse width measurement. The Timer 3 consists of up counters TM3L and TM3H and modulo registers TM3LM and TM3HM. TM3L and TM3LM share the same address FFF3H and TM3H and TM3HM share FFF4H. During read sequence, up counters are automatically accessed, and during write sequence modulo registers.

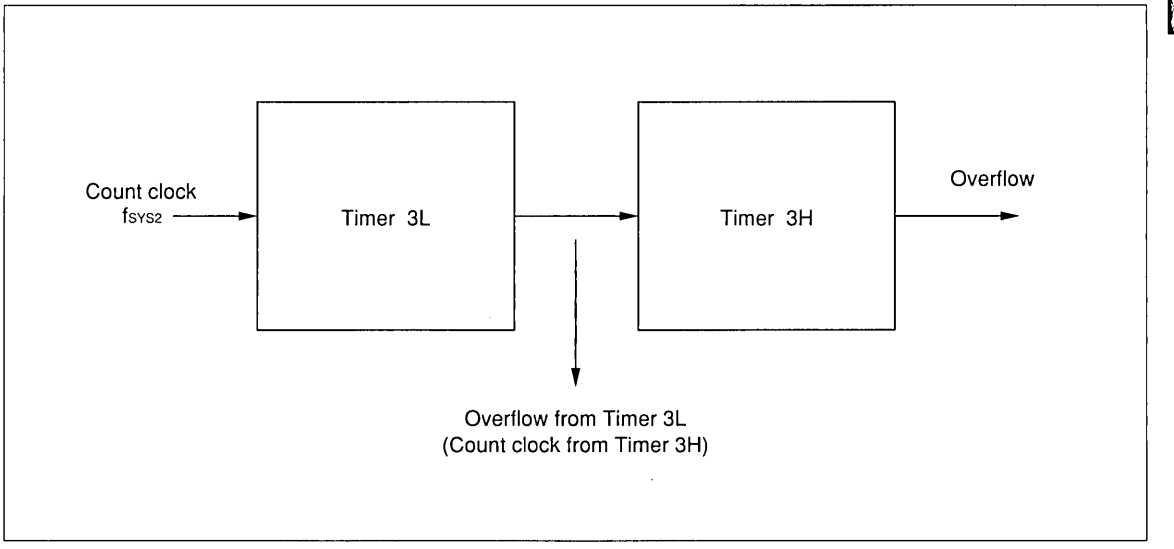


Fig. 11 Configuration of 16-Bit Timer

PWM WAVEFORM OUTPUT

The following describes the PWM waveform generation using Timers 3L and 3H. By using these timers, High period and Low period of clocks of a PWM waveform can be independently set. The resulting waveform is output through pin $P4_3$. The High and Low periods of the PWM waveform are determined by the settings of modulo registers TM3LM and TM3HM.

The Timers 3L and 3H cannot be used as timer/counter while they are used to generate PWM waveform.

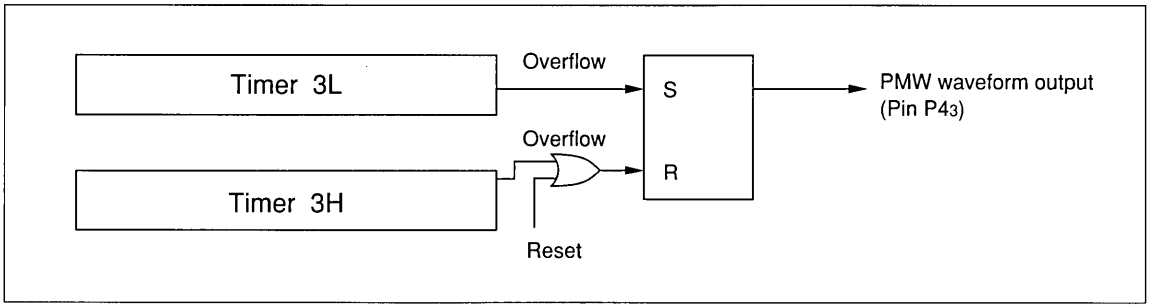


Fig. 12 PWM Waveform Output

• Setting to PWM waveform output mode

To enter PWM waveform output mode, set bit 1 of the control registers TM1C to 0 and bit 3 to 1. Set bit 4 of the control register SRC to 1 to force the pin $P4_3$ to PWM waveform output mode.

• Setting High period and Low period

The High and Low periods of the PWM waveform are determined by the contents of modulo registers TM3HM and TM3LM and selection of count clock.

High period = (100_H−content of TM3HM) x f_{SYS2}

Low period = (100_H−content of TM3LM) x f_{SYS2}

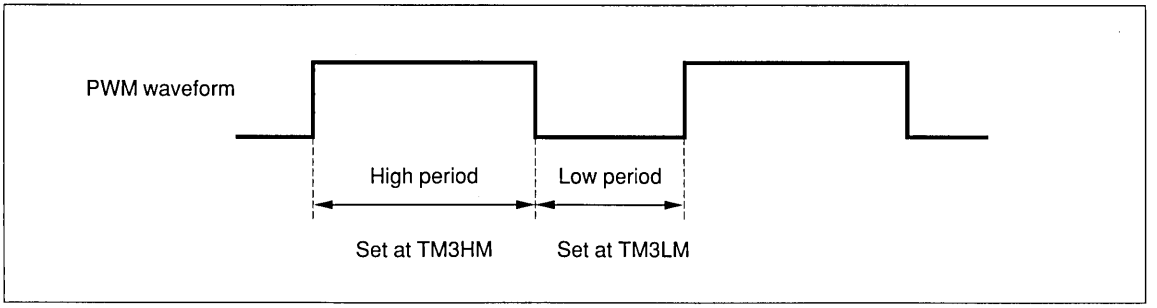


Fig. 13 Modulo Register vs PWM Waveform

• Outputting PWM waveform

The pin $P4_3$ starts outputting PWM waveform upon setting Timer 3 to count enable state and $P4_3$ to PWM waveform output pin. That is, set bits 0 and 7 of the control register TMC1 to 1.

The first half cycle of the PWM wave (High or Low duration) will contain error of up to one count clocks.

To stop PWM waveform, clear the bit 0 of the control register TMC1 to 0.

PULSE WIDTH MEASUREMENT

The pulse width measuring feature determines the High duration and Low duration of the input pulses from the $P4_6$ pin.

• Entering the pulse width measurement mode

To put the microcomputer to the pulse width measuring mode, set bits 0, 1, 3 and 7 of the control register TMC1 to "0". Set the bit 0 of the control register PLS to "1" to set the pin $P4_6$ to the pulse width input.

• Selecting High level or Low level duration

The selecting bit is the bit 1 of the control register PLSC.

BIT 1 OF REGISTER PLSC	PERIOD TO BE MEASURED
0	High half
1	Low half

• Starting/stopping pulse width measurement

Setting the bit 2 of the control register PLSC to "1" puts the microcomputer ready for pulse width measurement*. When the computer detects the rising (falling) edge of the input pulse from pin $P4_6$, the Timer 3 starts counting, and stops on the falling (rising) edge of the input pulse.
The counts indicates the pulse width.

* Rising edge to falling edge - High level duration measurement; falling edge to rising edge - Low level duration measurement.

• Calculating the measurements

The measurements can be obtained from the following equation.

Pulse width = (No. of overflows of Timer 3 x 2^{16}+ counts of Timer 3) x f_{SYS2}

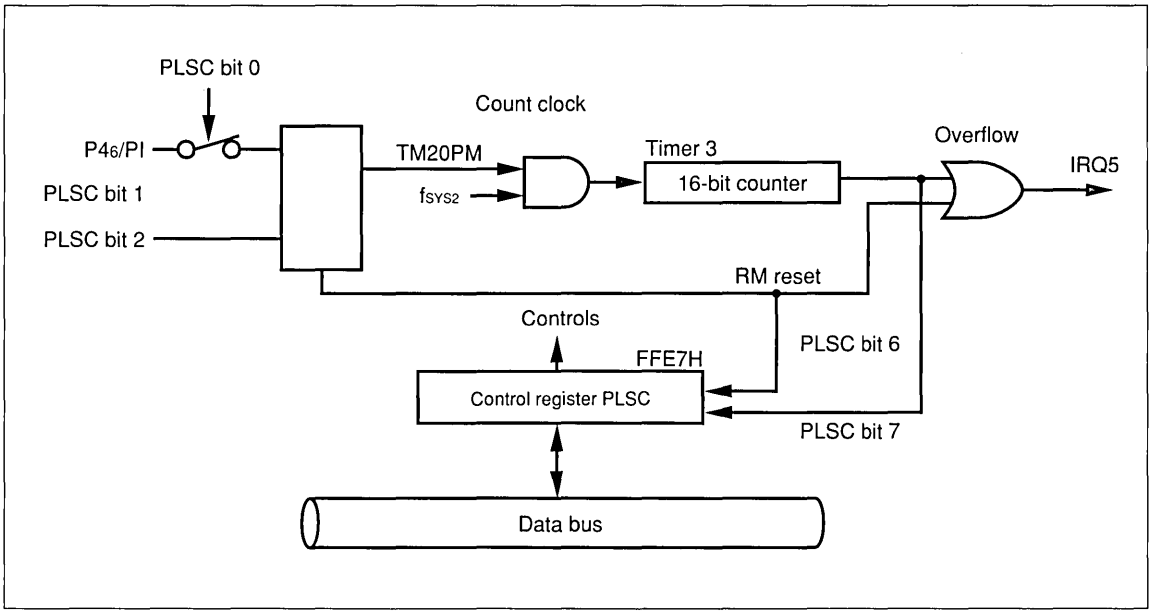


Fig. 14 Timer 3 Configured as Pulse Width Measurement

8-BIT WATCH DOG TIMER

SM831x is provided with a watch dog timer which will help the CPU to escape from program disturbance or infinite loop. The watch dog timer consists of the up counter WDT and modulo register WDTM. These two registers share the same address FFF5H.

• Operation of watch dog timer

The watch dog timer will inform the CPU when the CPU is running in an infinite loop due to miss programing or similar error. The watch dog timer will indicate this condition by generating NMI (non-maskable interrupt request) upon overflowing. Therefore, the user program should have the provision to periodically write into the up counter WDT to prevent the watch dog timer from overflowing.

If the program enters an infinite loop, the write program cannot be executed and the watch dog timer will overflow and produce NMI that shows uncontrolled program run.

A/D Converter

This is an 8-bit analog to digital converter (ADC) having 12-analog input and multiplexer. The ADC operates in either A/D conversion mode or comparison mode. To operate the ADC, first set any number of pins among $P3_0$ to $P3_3$ and $P5_0$ to $P5_7$ as A/D inputs (*) and then select one of these pins as analog data input to the A/D converter. Fig. 15 shows the configuration of the ADC.

Control of the ADC is through the bit manupulation of the A/D conversion control register ADCC (address FFFBH). Whether to use the P3 and P5 pins as standard input pin or A/D input is selected by bit setting of the control registers P3C and P5C (address FFE3H, FFE5H).

* Pins of P3 and P5 set up as analog voltage input are called A/D pins.

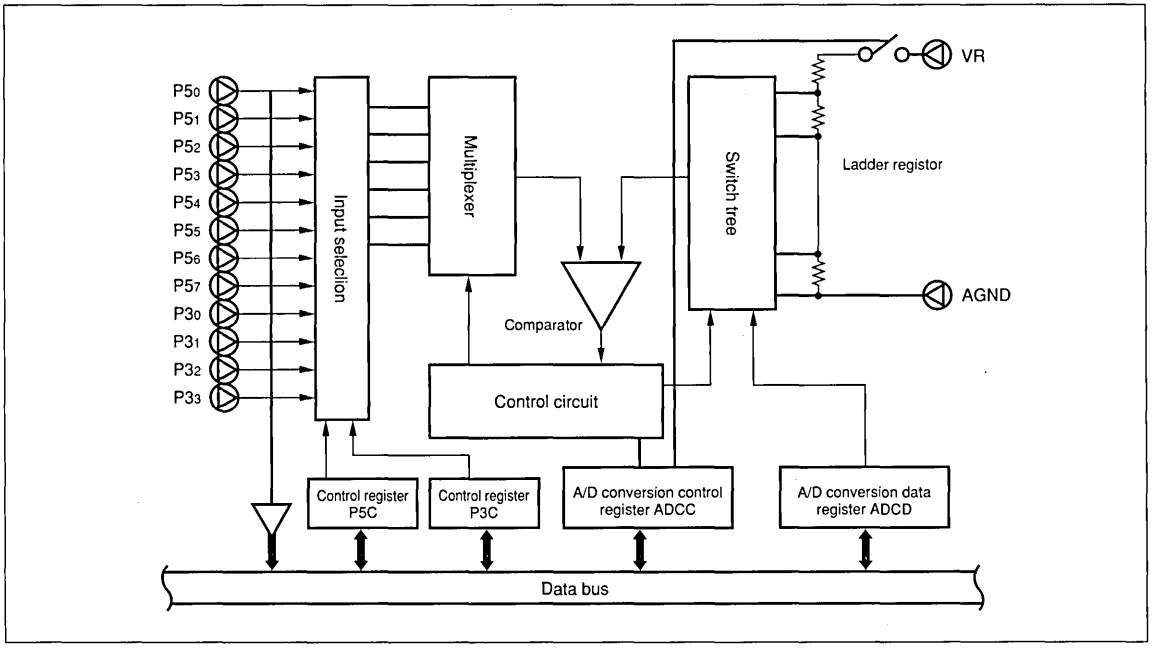


Fig. 15 A/D Converter Block Diagram

CAUTION :

1. Do not write a value other than "0" into the bit 7 place of the control register ADCC.
2. Bit 5 of the control register ADCC is read only. Write operation into this bit place will not affect the A/D converter.
3. The A/D converter remains idle during a standby mode (halt/stop) and therefore the end of A/D conversion cannot be used as a standby mode release event.

A/D CONVERSION MODE

In A/D conversion mode, analog voltage applied to the A/D pin is converted to the digital equivalent. The input analog voltage is sequentially compared with voltages of ladder resistors connected across the A/D reference voltage VR and AGND until approximation of digital value of 8-bit is obtained.

Conversion time : 34 µs (when main clock is 8 MHz and conversion clock is 250 kHz)

• Storing digital value

The ADed value is stored into the A/D data register ADCD (address FFFA$_H$).

Input voltage =

$$\frac{\text{Value of A/D data register ADCD}^{*}-0.5}{256} \times \text{VR (V)}$$

* To be converted to decimal value before calculation.

Note that if the input voltage is 0 V, then the content of the A/D data register ADCD is 00$_H$, different from that obtained from the calculation. Also note that even if the value is equivalent to VR, the result differs from that obtained from the equation above.

• Interrupt upon completion of A/D conversion storing digital value

At the end of A/D conversion, the interrupt request signal IRQ7 is generated when the bit 7 of the interrupt enable register IE and interrupt master enable flag IME have been set.

LEVEL COMPARISON MODE

During this mode, the analog input is compared with the voltage set by the A/D conversion data register ADCD. It takes the following time for the input analog voltage to be fully compared with the reference voltage.

Comparison time : 8 µs (when main clock is 8 MHz and conversion clock is 250 kHz)

• Setting reference voltage

Before starting the level comparison, set the reference voltage. Store the desired voltage value into the data register ADCD by referring to the equation shown below.

Comparison reference voltage =

$$\frac{\text{Value of A/D data register ADCD}^{*}-0.5}{256} \times \text{VR (V)}$$

* To be converted to decimal value before calculation.

If 0 V is desired as the comparison reference voltage, set 00$_H$ into the A/D data register ADCD. Note that this is not an decimal value.

• Result of level comparison

The result is stored into the bit 5 of the control register ADCC. The bit indicates the result as shown below.

BIT 5	LEVELS
0	Input voltage < reference voltage
1	Input voltage ≥ reference voltage

• Interrupt upon completion of comparison

At the end of comparison, the interrupt request signal IRQ7 is generated when the bit 7 of the interrupt enable register IE and interrupt master enable flag IME have been set.

Serial Interface

The SM831x is provided with a serial interface which transfers data in 8-bit serial format in synchronization with the selected transfer clock. The serial interface is controlled by the control register SRC (address FFE9H). Serial data is stored into the data shift register SRD (address FFF8H).

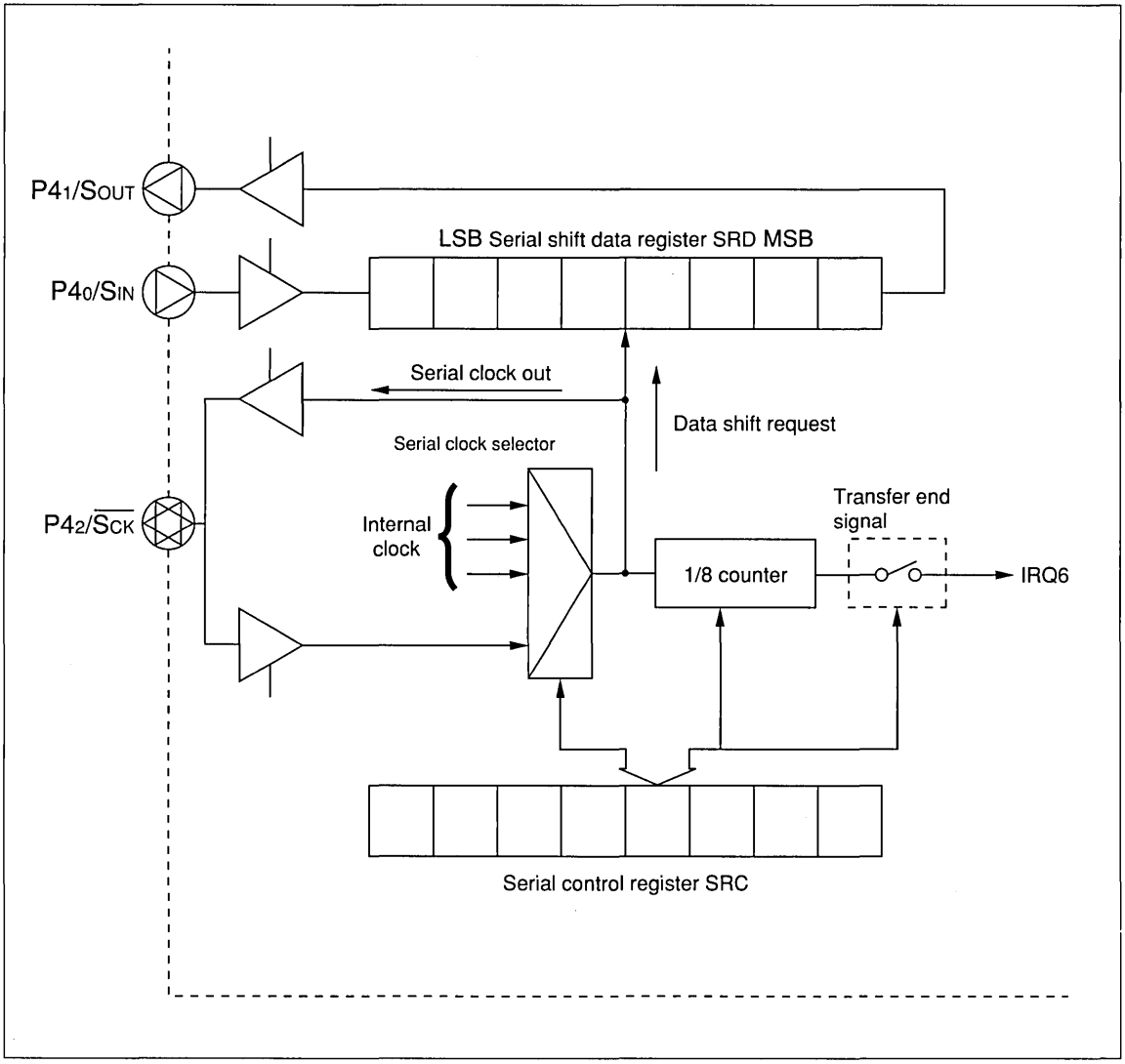


Fig. 16 Serial Interface

SUMMARY OF SERIAL INTERFACE

- Transfer 8-bit data string in serial format in synchronize with the shift clock.
- Set pins $P4_0$ to $P4_2$ pins to serial interface pins from the control registers P4C and SRC.
- The control register SRC controls functions of the interface.
- The serial shift data register SRD stores transmitted and receive data.
- One of the following clocks can be selected as the transfer clock;
  - f_{SYS2}
  - Timer 2 overflow (TM2OV)
  - External clock
- Content of the data register SRD is output to the S_{OUT} in synchronous with the falling edge of the shift clock. The SRD stores the S_{IN} pin level on the next rising edge of the shift clock.
- With or without the interrupt request handling is selectable.

NOTE :

When the serial interface starts transfer, the SM831x output the data from the register SRD, data at MSB first, at the same time placing the received external data to the register, LSB position first. This process is repeated until the 1st bit of the external data is shifted to the MSB position of the SRD.

SERIAL DATA TRANSFER TIMING

The data output timing in the chart below is the time where a bit in the data register SRD is output to pin S_{OUT}.

The data latching timing is the time where pin S_{IN} level is latched and stored into the data register SRD.

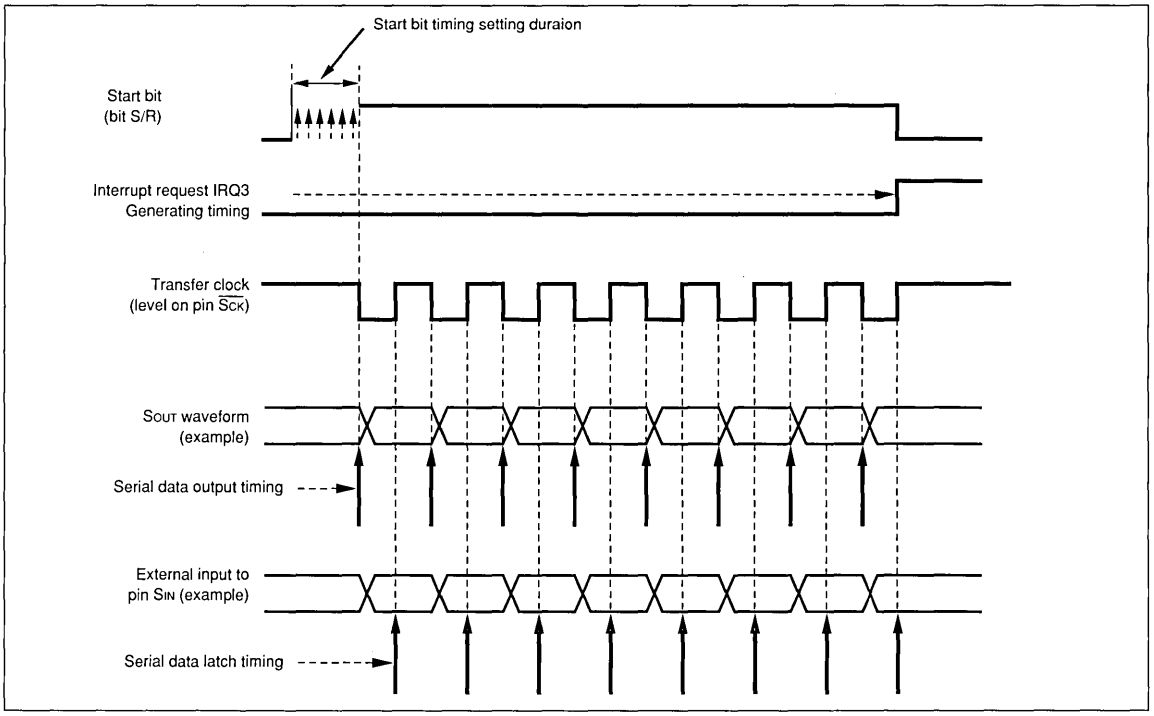


Fig. 17 Serial Data Output Timing

Zero Cross Detection

The SM831x has built-in zero cross detect circuit which compares the input voltage from the KI pin with the $V_{DD}/2$. An interrupt request signal may be issued as a result of the comparison (larger or smaller than the reference voltage). The below describes the control procedure.

• Assigning a pin for zero cross detect input

Use KI pin as zero cross detect input. The KI may also be used as an external interrupt input, KI pin acts like KH ($P6_7$) pin.

• Setting interrupt request signal (IRQ0) generating condition

The interrupt request signal (IRQ0) can be generated upon occurence of one of the following during zero cross detection.

- Rising of zero cross
  IRQ0 is generated when the level on the KI pin increases from GND level to $V_{DD}/2$.
- Zero cross High level
  IRQ0 is generated when the KI pin level reaches $V_{DD}/2$.
- Falling of zero cross
  IRQ0 is generated when the level on the KI pin decreases from $V_{DD}/2$ to GND.
- Zero cross Low level
  IRQ0 is generated when the KI pin level reaches GND.

Selection among these four conditions is through the control register EXTC. Upon selection, KI pin changes to zero cross input.

• Setting interrupt

To process the IRQ0 set the bit 0 of the interrupt enable register IE to "1" and IME flag to "1".
After setting, the KI pin is ready for accommodate the zero cross input as shown in the table below.

Table 17 External Interrupt Conditions at KI

PIN NAME	SETTING OF INTERRUPT ENABLE REGISTER (IE)	SETTING OF EXTERNAL INTERRUPT CONTROL REGISTER (EXTC)			INTERRUPT CONDITION
KI	Bit 0 = 1	Bit 0 = 0	Bit 1 = 0	Bit 2 = 0	Rising edge
				Bit 2 = 1	High level
			Bit 1 = 1	Bit 2 = 0	Falling edge
				Bit 2 = 1	Low level
		Bit 0 = 1	Bit 1 = 0	Bit 2 = 0	Zero cross, rising edge
				Bit 2 = 1	Zero cross, High level
			Bit 1 = 1	Bit 2 = 0	Zero cross, falling edge
				Bit 2 = 1	Zero cross, Low level

CONTROL REGISTER SETS

Total 29 addresses are provided for these 35 registers. This means that some addresses are shared by two or more registers. Almost of all functions of the SM831x are controlled by the settings of the register(s).

The description first lists all the control registers in alphabetical order and then explains them in that order.

Table 18 Register Summary (Alphabetical Order)

ADDRESS	SYMBOL	NAME	R/W	INITIAL VALUE
FFFB$_H$	ADCC	(A/D converter) Control register	R/W	20$_H$
FFFA$_H$	ADCD	(A/D converter) Data register	R/W	–
FFEE$_H$	EXTC	(External interrupt) Control register	R/W	00$_H$
FFFF$_H$	IE	Interrupt enable register	R/W	00$_H$
FFFE$_H$	IF	Interrupt flag register	R/W	00$_H$
FFD0$_H$	P0	(P0 output) Data register	R/W	00$_H$
FFD1$_H$	P1	(P1 output) Data register	R/W	00$_H$
FFD2$_H$	P2	(P2 I/O) Data register	R/W	00$_H$
FFE2$_H$	P2C	(P2) Control register	R/W	00$_H$
FFD3$_H$	P3	(P3 input) Data register	R	–
FFE3$_H$	P3C	(P3) Control register	R/W	–
FFD4$_H$	P4	(P4 I/O) Data register	R/W	00$_H$
FFE4$_H$	P4C	(P4) Control register	R/W	00$_H$
FFD5$_H$	P5	(P5 input) Data register	R	–
FFE5$_H$	P5C	(P5) Control register	R/W	–
FFD6$_H$	P6	(P6 I/O) Data register	R/W	00$_H$
FFE6$_H$	P6C	(P6) Control register	R/W	00$_H$
FFE7$_H$	PLSC	(Pulse input) Control register	R/W	38$_H$
FFF9$_H$	SRC	(Serial interface) Control register	R/W	C0$_H$
FFF8$_H$	SRD	(Serial interface) Data register	R/W	–
FFFD$_H$	STPR	Stop release register	R/W	A0$_H$
FFF0$_H$	TM0	(Timer 0) Up counter	R	00$_H$
FFF0$_H$	TM0M	(Timer 0) Modulo register	W	–
FFF1$_H$	TM1	(Timer 1) Up counter	R	–
FFF1$_H$	TM1M	(Timer 1) Modulo register	W	–
FFF2$_H$	TM2	(Timer 2) Up counter	R	–
FFF2$_H$	TM2M	(Timer 2) Modulo register	W	–
FFF4$_H$	TM3H	(Timer 3H) Up counter	R	–
FFF4$_H$	TM3HM	(Timer 3H) Modulo register	W	–
FFF3$_H$	TM3L	(Timer 3L) Up counter	R	–
FFF3$_H$	TM3LM	(Timer 3L) Modulo register	W	–
FFF6$_H$	TMC0	(Timer) Countrol register (0)	R/W	40$_H$
FFF7$_H$	TMC1	(Timer) Countrol register (1)	R/W	00$_H$
FFF5$_H$	WDT	(Watch dog timer) Up counter	R	–
FFF5$_H$	WDTM	(Watch dog timer) Modulo register	W	–

* When reading write only bit(s) of any of the control registers, "1" is always returned.

ADCC (Control register)

Related block : A/D converter

Overview : Control A/D converter

Bit 7							0
SEL	S/R	CO	ADMD	SEL3	SEL2	SEL1	SEL0

Bit 7 : This bit is reserved and non-user bit. Do not write a value other than 0 into this place.

Bit 6 : Start/reset bit

BIT	CONTENT
0	In stop state
1	Starts operation. Do not read/write into this position during A/D operation. The bit is automatically clear at the end of operation.

Bit 5 : Comparison result storing bit position (Stores the result of comparision in the level comparison mode.)

BIT	CONTENT
0	Level on input pin < D/A level of register ADCD
1	Level on input pin ≥ D/A level of register ADCD

Bit 4 : Operation mode select bit

BIT	CONTENT
0	Level comparision
1	A/D conversion

Bit 3 to 0 : Analog input pin select bit*

BIT	CONTENT
0000	$P5_0$
0001	$P5_1$
0010	$P5_2$
0011	$P5_3$
0100	$P5_4$
0101	$P5_5$
0110	$P5_6$
0111	$P5_7$
1000	$P3_0$
1001	$P3_1$
1010	$P3_2$
1011	$P3_3$
1100	No pin is specified.
1101	No pin is specified.
1110	No pin is specified.
1111	No pin is specified.

* Before accepting analog input through the port 5 or 3, a particular P5 or P3 pin must be set as A/D input pin. For detail, see control register P5C or P3C section.

ADCD (Data register)

Related block : A/D converter

Overview : Store A/D conversion or comparison voltage data

Bit 7							0

• Equation

Input voltage or comparson voltage =

$$\frac{\text{Value of A/D data register ADCD*} - 0.5}{256} \times \text{VR (V)}$$

* To be converted to decimal value before calculation. If the input voltage or comparison voltage is 0 V, then this value is 00_H. Even if the input voltage is equal to VR, the calculated value is not VR.

EXTC (Control register)

Related block : Pins KI and KH, interrupt block

Overview : Generate an event for the interrupt request signal IRQ0 or IRQ4 when the input signal is fed to pin KI or KH.

Bit 7							0
–	–	–	MD4	MD3	MD2	MD1	MD0

Bit 7 to 5 : Unused

Bit 4 to 3 : KH pin interrupt event selection bit

BITS 43	INTERRUPT EVENT	STOP MODE RELEASE CONDITION	COUNT EDGE
00	Rising edge	Don't set	
01	Falling edge	Don't set	
10	High level	Rising edge	
11	Low level	Falling edge	

Bit 2 to 0 : KI pin interrupt event selection bit

BITS 210	INTERRUPT EVENT	STOP MODE RELEASE CONDITION	COUNT EDGE
000	Rising edge	Don't set	
001	Zero cross rising edge	Don't set	
010	Falling edge	Don't set	
011	Zero cross falling edge	Don't set	
100	High level	Rising edge	
101	Zero cross High level	Don't set	
110	Low level	Rising edge	
111	Zero cross Low level	Don't set	

IE (Interrupt enable register)

Related block : Maskable interrupt sections and standby (halt mode) sections

Overview : Enable or disable individual maskable interrupt request (Note 1).
To make the enabled maskable interrupt effective, set the interrupt master enable flag ME to "1".

Bit 7							0
IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0

Bit 7 : A/D converter end interrupt enable bit (Note 2)
Bit 6 : Serial interface interrupt enable bit
Bit 5 : Timer 3, pulse width measurement end interrupt enable bit
Bit 4 : External interrupt (KH) enable bit (Note 2)
Bit 3 : Timer 2 interrupt enable bit
Bit 2 : Timer 1 interrupt enable bit
Bit 1 : Timer 0 interrupt enable bit
Bit 0 : External interrupt (KI) enable bit

BIT	CONTENT
0	Disable
1	Enable

NOTE :

The interrupt enable register IE is used to wake up the chip from standby mode (HALT mode) by setting the interrupt to enable.

This register is also used for the release setting to enable/disable halt mode. The following block disabled in halt mode, however, do not applied to the above setting.

- A/D converter
- Zero cross detector (uses external interrupt enable bit; IE)

When the external interrupt enable bit (KI pin) is used as a external interrupt input not as a zero cross detector, this pin can be used for the release setting.

IF (Input flag register)

Related block : Maskable interrupt sections
Overview : Latch interrupt request signal coming from a block.

Bit 7							0
IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Bit 7 : A/D converter end interrupt request bit
Go "1" level when the A/D conversion ends.
Bit 6 : Serial interface interrupt request bit
Go "1" level when the serial interface finishes transmission.
Bit 5 : Timer 3, pulse width measurement end interrupt request bit
Go "1" level when the Timer 3 overflows or at the end of pulse width measurement.
Bit 4 : External interrupt (KH) request bit
Go "1" level upon input from pin KH (pin $P6_7$).
(Refer to control register EXTC.)
Bit 3 : Timer 2 interrupt request bit
Go "1" level upon Timer 2 overflow.
Bit 2 : Timer 1 interrupt request bit
Go "1" level upon Timer 1 overflow.
Bit 1 : Timer 0 interrupt request bit
Go "1" level upon Timer 0 overflow.
Bit 0 : External interrupt (KI) request bit
Go "1" level upon input from pin KI.
(Refer to control register EXTC.)

NOTE :
Each bit in the IF, once set to "1", remains "1" until the interrupt is accomodated, or software-reset. These bits are non-software-settable.

P0 (Data register)

Related block : Port 0
Overview : Access port 0

Bit 7							0
P07	P06	P05	P04	P03	P02	P01	P00

Bits P07 to P00 correspond to ports $P0_7$ to $P0_0$ which output Low level when the bit is "0" and High when "1".

P1 (Data register)

Related block : Port 1
Overview : Access port 1

Bit 7							0
P17	P16	P15	P14	P13	P12	P11	P10

Bits P17 to P10 correspond to ports $P1_7$ to $P1_0$ which output Low level when the bit is "0" and High when "1".

P2 (Data register)

Related block : Port 2
Overview : Access port 2

Bit 7							0
P27	P26	P25	P24	P23	P22	P21	P20

Bits P27 to P20 correspond to ports $P2_7$ to $P2_0$. When pins are set to input, these bits are set to "0" when the corresponding pin is at Low level and "1" when High level. When these pins are set to output, they output Low level when the corresponding bit is set to "0", and High level when the bit is "1".

P2C (Control register)

Related block : Port 2
Overview : Set pins of port 2 individually

Bit 7 0

P2C7	P2C6	P2C5	P2C4	P2C3	P2C2	P2C1	P2C0

Bit 7 : Pin $P2_7$ input/output selection bit
Bit 6 : Pin $P2_6$ input/output selection bit
Bit 5 : Pin $P2_5$ input/output selection bit
Bit 4 : Pin $P2_4$ input/output selection bit
Bit 3 : Pin $P2_3$ input/output selection bit
Bit 2 : Pin $P2_2$ input/output selection bit
Bit 1 : Pin $P2_1$ input/output selection bit
Bit 0 : Pin $P2_0$ input/output selection bit

BIT	CONTENT
0	Input pin
1	Output pin

P3 (Data register)

Related block : Port 3
Overview : Access port 3

Bit 7 0

–	–	–	–	P33	P32	P31	P30

Bits P33 to P30 correspond to ports $P3_3$ to $P3_0$ which output Low level when the bit is "0" and High level when "1". However, the register always retains "0s" regardless of the state of the P3 pin when it is set to A/D pin.

P3C (Control register)

Related block : Port 3, A/D converter
Overview : Set pins of port 3 individually either to analog input for A/D* or normal (digital) input pin.

Bit 7 0

–	–	–	–	P3C3	P3C2	P3C1	P3C0

Bit 7 to 4 : Unused
Bit 3 : Pin $P3_3$ input selection bit
Bit 2 : Pin $P3_2$ input selection bit
Bit 1 : Pin $P3_1$ input selection bit
Bit 0 : Pin $P3_0$ input selection bit

BIT	CONTENT
0	A/D input pin
1	Digital input pin

* The pins set to analog input is called A/D pins one of which is further selected by the control register ADCC as the analog input for A/D converter.

NOTE :
The content of this register is unknown once reset by hardware. The initialization segment of the program should write appropriate value into this register.

P4 (Data register)

Related block : Port 4
Overview : Access port 4

Bit 7 0

P47	P46	P45	P44	P43	P42	P41	P40

Bits P47 to P40 correspond to ports $P4_7$ to $P4_0$. When pins are set to input, these bits are set to "0" when the corresponding pin is at Low level, and "1" when High level. When these pins are set to output, they output Low level when the corresponding bit is set to "0", and High level when the bit is "1".
Since P4 pin assumes additional function, its state changes depending on selected function.

P4C (Control register)

Related block : Port 4

Overview : Set pins of port 3 individually either to input or output pin.

Bit 7 0

P4C7	P4C6	P4C5	P4C4	P4C3	P4C2	P4C1	P4C0

Bit 7 : Pin $P4_7$ input/output selection bit
Bit 6 : Pin $P4_6$ input/output selection bit
Bit 5 : Pin $P4_5$ input/output selection bit
Bit 4 : Pin $P4_4$ input/output selection bit
Bit 3 : Pin $P4_3$ input/output selection bit
Bit 2 : Pin $P4_2$ input/output selection bit
Bit 1 : Pin $P4_1$ input/output selection bit
Bit 0 : Pin $P4_0$ input/output selection bit

BIT	CONTENT
0	Input pin
1	Output pin

P5 (Data register)

Related block : Port 5

Overview : Access port 5

Bit 7 0

P57	P56	P55	P54	P53	P52	P51	P50

Bits P57 to P50 correspond to ports $P5_7$ to $P5_0$ which output Low level when the bit is "0" and High level when 1.

P5C (Control register)

Related block : Port 5

Overview : Set pins of port 5 individually either to analog input for A/D or normal (digital) input pin

Bit 7 0

P5C7	P5C6	P5C5	P5C4	P5C3	P5C2	P5C1	P5C0

Bit 7 : Pin $P5_7$ input mode selection bit
Bit 6 : Pin $P5_6$ input mode selection bit
Bit 5 : Pin $P5_5$ input mode selection bit
Bit 4 : Pin $P5_4$ input mode selection bit
Bit 3 : Pin $P5_3$ input mode selection bit
Bit 2 : Pin $P5_2$ input mode selection bit
Bit 1 : Pin $P5_1$ input mode selection bit
Bit 0 : Pin $P5_0$ input mode selection bit

BIT	CONTENT
0	A/D input pin
1	Digital input pin

* The pins set to analog input is called A/D pins.

P6 (Data register)

Related block : Port 6

Overview : Access port 6

Bit 7 0

P67	P66	P65	P64	P63	P62	P61	P60

Bits P67 to P60 correspond to ports $P6_7$ to $P6_0$. When pins are set to input, these bits are set to "0" when the corresponding pin is at Low level, and "1" when High level. When these pins are set to output, they output Low level when the corresponding bit is set to "0", and High level when the bit is "1".

Even if $P6_7$ is used as an external interrupt input, it can be used in the same way as remaining P6 pins.

P6C (Control register)

Related block : Port 6

Overview : Set pins of port 6 individually either to input or output pin.

Bit 7							0
P6C7	P6C6	P6C5	P6C4	P6C3	P6C2	P6C1	P6C0

Bit 7 : Pin $P6_7$ input/output selection bit
Bit 6 : Pin $P6_6$ input/output selection bit
Bit 5 : Pin $P6_5$ input/output selection bit
Bit 4 : Pin $P6_4$ input/output selection bit
Bit 3 : Pin $P6_3$ input/output selection bit
Bit 2 : Pin $P6_2$ input/output selection bit
Bit 1 : Pin $P6_1$ input/output selection bit
Bit 0 : Pin $P6_0$ input/output selection bit

BIT	CONTENT
0	Input pin
1	Output pin

PLSC (Control register)

Related block : Pin $P4_6$, Timer 3

Overview : Set pin $P4_6$ to pulse input pin and control pulse width measurement function.

Bit 7							0
TM3OV	CO	–	–	–	S/R	SEL1	MD0

Bit 7 : Timer 3 overflow store bit*
Bit 6 : End of measurement flag store bit*
Bit 5 to 3 : Unused
Bit 2 : Start/reset bit

BIT	CONTENT
0	Stop
1	Starts measurement. Setting this bit to "0" during measurement pauses the measurement. Otherwise, the bit is automatcially to "0" at the end of measurement.

Bit 1 : Pulse measurement type selection bit

BIT	CONTENT
0	Measure High level duration
1	Measure Low level duration

Bit 0 : Pin $P4_6$ mode selection bit

BIT	CONTENT
0	(Digital) I/O pin
1	Pulse input pin

* These two bits will not be reset to "0" automatically. The program should set the bits to "0" as necessary.

SRC (Control register)

Related block : Serial interface

Overview : Control the serial interface. Set pin $P4_3$ to PWM waveform output pin.

Bit 7							0
S/R	–	–	PWM	MD3	MD2	MD1	MD0

Bit 7 : Start/reset bit

BIT	CONTENT
0	Stop transfer
1	Start transfer. Setting this bit to "0" pauses transfer. Reset to "0" at the end of transfer automatically.

Bit 6, 5 : Unused
Bit 4 : PWM waveform output ($P4_3$) select bit

BIT	CONTENT
0	Normal I/O
1	PWM waveform output from $P4_3$ pin

Bit 3 : Pins P4 ($P4_2$, $P4_1$, $P4_0$) mode select bit

BIT	CONTENT
0	Normal I/O pin
1	$P4_2$: serial shift clock I/O $P4_1$: serial output $P4_0$: serial I/O

Bit 2 : Pin S_{OUT} ($P4_1$) state set bit

BIT	CONTENT
0	Disable serial out (receive only)
1	Enable serial out (TX / RX)

Bit 1, 0 : Transfer clock selection bit

BIT 10	CONTENT	Transfer timing (level on $\overline{S_{CK}}$ pin)	
		Data output timing	Data latch timing
00	f_{SYS2}		
01	Timer 2 overflow (TM2OV)		
1*	Input clock from pin $\overline{S_{CK}}$		

* Don't care

Data is output at the time when the bit of the data register SRD is output to S_{OUT}. Data is latched at the time when S_{IN} level is latched and stored into the data register SRD.

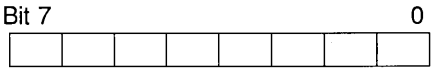
NOTE :

When writing a value into the control register SRC, use LD instruction. Do not use RES or SET instruction. If one of these instructions is given, the control register SRC may trigger the serial interface. The bit 7 of the SRC is write only. If read, this bit always returns "1".

SRD (Data register)

Related block : Serial interface

Overview : Store serial interface shift data



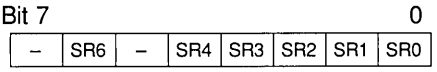
NOTE :

Reading or writing the data register SRD causes the octal counter in the serial interface block to be cleared. If the serial interface is forced to pause, it makes the contents of the octal counter unstable. To keep the contents of the octal counter consistent, clear the counter before starting the serial interface.

STPR (Stop release register)

Related block : Standby function stop mode

Overview : Set stop mode release event



Bit 7 : Unused

Bit 6 : Serial interface stop release enable bit

Bit 5 : Unused

Bit 4 : KH stop release enable bit*

Bit 3 : Timer 2 stop release enable bit

Bit 2 : Timer 1 stop release enable bit

Bit 1 : Timer 0 stop release enable bit

Bit 0 : KI stop release enable bit*

BIT	CONTENT
0	Disable
1	Enable

* To select KI and KH pins as stop mode cancel event input, the control register EXTC should be set to appropriate configuration. See control register EXTC for further information.

TM0 (Up counter)

Related block : Timer 0

Overview : Operate counting in synchronous with the selected count clock. Start timing not synced to count clock. Up to one count clock cycle of error may be encountered upon starting.

TM0M (Modulo register)

Related block : Timer 0

Overview : Set the initial value of the up counter TM0.

TM1 (Up counter)

Related block : Timer 1

Overview : Advance count in synchronous with the selected count clock. Start timing not synced to count clock. Up to one count clock cycle of error may be encountered upon starting.

TM1M (Modulo register)

Related block : Timer 1

Overview : Set the initial value of the up counter TM1M.

TM2 (Up counter)

Related block : Timer 2

Overview : Advance count in synchronous with the selected count clock. Start timing not synced to count clock. Up to one count clock cycle of error may be encountered upon starting.

TM2M (Modulo register)

Related block : Timer 2

Overview : Set the count initial value of the up counter TM2.

TM3H (Up counter)

Related block : Timer 3

Overview : Advance count in synchronous with the selected count clock. Start timing not synced to count clock. Up to one count clock cycle of error may be encountered upon starting. Provide upper 8-byte of the 16-bit up counter (Timer 3).

TM3HM (Modulo register)

Related block : Timer 3

Overview : Set the initial value of the Timer 3. Provide upper 8-byte of the 16-bit modulo register.

TM3L (Up counter)

Related block : Timer 3

Overview : Advance count in synchronous with the selected count clock. Start timing not synced to count clock. Up to one count clock cycle of error may be encountered upon starting. Provide lower 8-byte of the 16-bit up counter (Timer 3).

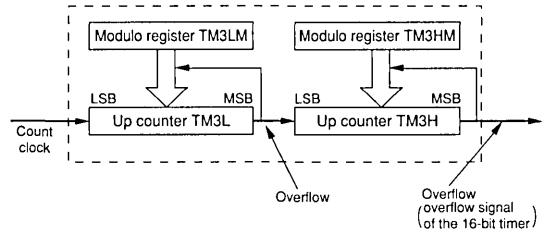
TM3LM (Modulo register)

Related block : Timer 3

Overview : Set the initial value of the Timer 3. Provide lower 8-byte of the 16-bit modulo register.

• Configuration of Timer 3

Two cascaded 8-bit timers constitute the 16-bit timer.



NOTE :

Up counter and modulo register are mapped to the idential address. Reading from this address location is to read the up counter. Writing into this address location is to write into modulo register.

TMC0 (Control register)

Related block : Timers 0, 1 and 2

Overview : Select the count clock to timers 0, 1 and 2 and stop them. Reset the contents of prescaler.

Bit 7							0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0

Bit 7 : Set to "0" only

Bit 6 : Prescaler reset bit

BIT	CONTENT
0	Normal count operation
1	Reset prescaler and then reset itself

Bit 5, 4 : Timer 2 count clock selection bit

BIT 54	CONTENT	COUNT EDGE
00	None (count stop)	
01	Timer 1 overflow (TM1OV)	↘
10	f_{SYS2} (system clock/2^2)	↗
11	f_{SYS8} (system clock/2^8)	

Bit 3 to 2 : Timer 1 count clock selection bit

BIT 32	CONTENT	COUNT EDGE
00	None (count stop)	
01	Timer 0 overflow (TM0OV)	↘
10	f_{SYS2} (system clock/2^2)	↗
11	f_{SYS8} (system clock/2^8)	

Bit 1 to 0 : Timer 0 count clock selection bit

BIT 10	CONTENT	COUNT EDGE
0*	None (count stop)	
10	f_{SYS2} (system clock/2^2)	↘
11	f_{OSC} (clock from OSC_{OUT})	↗

* Don't care

NOTE :

When writing a value into the control register TMC0, use LD instruction and do not use RES or SET instruction. Should these latter instructions are used for TMC0, contents of prescaler and watch dog timer WDT are cleared. Subsequent effects include silenced audio output.

TMC1 (Control register)

Related block : Timer 3, PWM, watch dog timer, port 4

Overview : Control Timer 3 (16-bit timer or pulse width measurement) and watch dog timer. Set a pin of $P4_7$ to F pin.

Bit 7							0
EN	SEL1	SEL0	S/R1	MD3	CO	MD1	S/R0

Bit 7 : PWM waveform output ($P4_3$) enable bit

BIT	CONTENT
0	Disable PWM waveform output
1	Enable PWM waveform output

Bit 6 to 5 : Pin F ($P4_7$) output select bit

BIT	CONTENT
0*	Stop output
10	Output f_{SYS9} (system clock/2^9)
11	Output PWM waveform

Bit 4 : Start/reset bit

BIT	CONTENT
0	Stop counting operation of watch dog timer
1	Start counting operation of watch dog timer

Bit 3, 1 : Timer 3 operation mode set bit

BIT	CONTENT
00	16-bit timer. Also in this setting for pulse width measurement.
10	Output PWM waveform
*1	Stop

Bit 2 : PWM waveform data storage bit

When read upon outputting PWM, bit 2 of the control register TMC1 represents the output level at that moment.

Bit 0 : Start/reset bit

BIT	CONTENT
0	Stop Timer 3 count operation
1	Start Timer 3 count operation

* Don't care

CAUTION :

Stop this counter before entering the standby mode. Initialize the counter as necessary.

NOTE :

When using the pulse width measurement function, set mode of the Timer 3 to 16-bit timer.

WDT (Up counter)

Related block : Watch dog timer

Overview : Counter section of watch dog timer. Generate non-maskable interrupt NMI upon overflowing to inform the CPU of a program error.

WDTM (Modulo register)

Related block : Watch dog timer

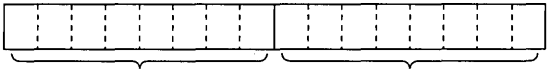
Overview : Set the initial value of the watch dog timer

NOTE :

Up counter WDT and modulo register WDTM are mapped to the idential address. Reading from this address location ($FFF5_H$) is to read the up counter WDT. Writing into this address location is to write into the modulo register WDTM.

INSTRUCTION SET

Definition of Symbols

SYMBOL	DESCRIPTION
(HL)	Contents of the memory designated by the content of register pair
←	Transfer direction
∪	Logical OR
∩	Logical AND
•	Exclusive OR
(HLI)	Increment the content of HL after executing instruction
(HLD)	Decrement the content of HL after executing instruction
nn	16-bit immediate data
n	8-bit immediate data
dd	Operand, BC, DE, HL, SP
qq	Operand, BC, DE, HL, AF
ss	Operand, BC, DE, HL, SP
s	Operand, r, (HL), n
m	Operand, r, (HL)
r	Operand, A, B, C, D, E, H, L
b	Operand 0-7 (define test bit)
t	Operand 0-7 (designate address of page zero)
cc	Operand 0-3 (designate conditional flag)
PC_H PC_L	 PC_H (Upper bytes) PC_L (Lower bytes)

Functions of symbols used in flags (Z, N, H, Cy) are as follows :

SYMBOL	DESCRIPTION
1	Set flag after execution of instruction.
0	Reset flag after execution of instruction.
•	Change no flag.
;	Set or reset the flag depending on execution.
*	Bring content of flag undefinable status after execution of instruction.
A0, A7	Load contents of bit 0 and 7 of register A.
m0, m7	Load contents of bit 0 and 7 of operand m.
IF0-IF3	Load contents of flags IF0 to IF3.
$\overline{(HL)\ b}$	Load the complement of the bit specified by b, at HL.
$\overline{rb}$	Load the complement of the bit specified by b, at register.
$\overline{cy}$	Load the complement of Cy flag.

The tables blow are code assignment of operands.

• Register r

r, r´	CODE
A	111
B	000
C	001
D	010
E	011
H	100
L	101

• Register pair dd

dd	CODE
BC	00
DE	01
HL	10
SP	11

• Register pair qq

qq	CODE
BC	00
DE	01
HL	10
AF	11

• Register pair ss

ss	CODE
BC	00
DE	01
HL	10
SP	11

• Bit specification

b	CODE
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

• Jump condition

cc	FLAG
00 (NZ, non-zero)	Z = 0
01 (Z, zero)	Z = 1
10 (NC, non-carry)	Cy = 0
11 (C, carry)	Cy = 1

• Code t and page zero memory

t (CODE)	p (PC_L)
0 (000)	00_H
1 (001)	08_H
2 (010)	10_H
3 (011)	18_H
4 (100)	20_H
5 (101)	28_H
6 (110)	30_H
7 (111)	38_H

Instruction Summary

8-Bit Transfer Instruction

MNEMONIC	OPERATION
LD A, (BC)	A ← (BC)
LD A, (C)	A ← (FF00H+C)
LD A, (DE)	A ← (DE)
LD A, (HLD)	A ← (HL) HL ← HL–1
LD A, (HLI)	A ← (HL) HL ← HL+1
LD A, (n)	A ← (FF00H+n)
LD (BC), A	(BC) ← A
LD (C), A	(FF00H+C) ← A
LD (DE), A	(DE) ← A
LD (HLD), A	(HL) ← A HL ← HL–1
LD (HLI), A	(HL) A HL ← HL+1
LD (HL), n	(HL) ← n
LD (HL), r	(HL) ← r
LD (n), A	(FF00H+n) ← A
LD r, (HL)	r ← (HL)
LD r, n	r ← n
LD r, r'	r ← r′
LDX A, (nn)	A ← (nn)
LDX (nn), A	(nn) ← A

16-Bit Transfer Instruction

MNEMONIC	OPERATION
LD dd, nn	dd ← nn
LD (nn), SP	(nn) ← SPL (nn+1) ← SPH
LD SP, HL	SP ← HL
LDHL SP, e	HL ← SP+e (e = –128 to +127)
POP qq	qqL (Lower bytes) ← (SP) qqH (Higher bytes) ← (SP+1) SP ← SP+2
PUSH qq	(SP–1) ← qqH (Higher bytes) (SP–2) ← qqL (Lower bytes) SP ← SP–2

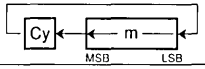
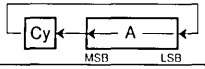
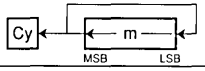
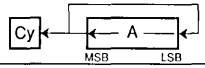
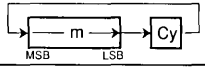
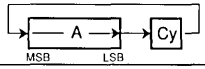
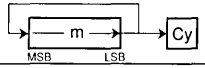
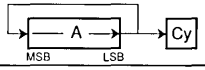
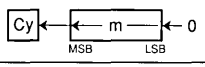
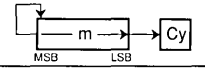
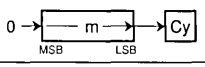
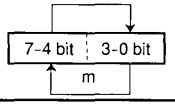
8-Bit Arithmetical and Logical Instructions

MNEMONIC	OPERATION
ADC A, s	A ← A+s+Cy
ADD A, s	A ← A+s
AND s	A ← A ∩ s
CP s	A–s (Register A remains unchanged)
CPL	A ← $\overline{A}$
DAA	Decimal adjust acc (Convert to binery coded decimal)
DEC m	m ← m–1
INC m	m ← m+1
OR s	A ← A ∪ s
SBC A, s	A ← A–s–Cy
SUB s (SUB A, s)	A ← A–s
XOR s	A ← A ⊕ s

16-Bit Arithmetical and Logical Instructions

MNEMONIC	OPERATION
ADD HL, ss	HL ← HL+ss
ADD SP, e	SP ← SP+e
DEC ss	ss ← ss–1
INC ss	ss ← ss+1

Rotate and Shift Instructions

MNEMONIC	OPERATION
RL m	
PLA	
RLC m	
RLCA	
RR m	
RRA	
RRC m	
RRCA	
SLA m	
SRA m	
SRL m	
SWAP m	

Bit Manipulation Instruction

MNEMONIC	OPERATION
BIT b, m	$Z \leftarrow \overline{mb}$
RES b, m	mb ← 0
SET b, m	mb ← 1

Jump Instruction

MNEMONIC	OPERATION
JP cc, nn	if cc true ↓ PC ← nn else next Inst.
JP (HL)	PC ← (HL)
JP nn	PC ← nn
JR cc, e	if cc true ↓ PC ← PC+e else next Inst.
JR e	PC ← PC+e

CPU Control Instructions

MNEMONIC	OPERATION
CCF	$Cy \leftarrow \overline{Cy}$
DI	IME ← 0
EI	IME ← 1
HALT	Halt
NOP	No operation
SCF	Cy ← 1
STOP	Stop

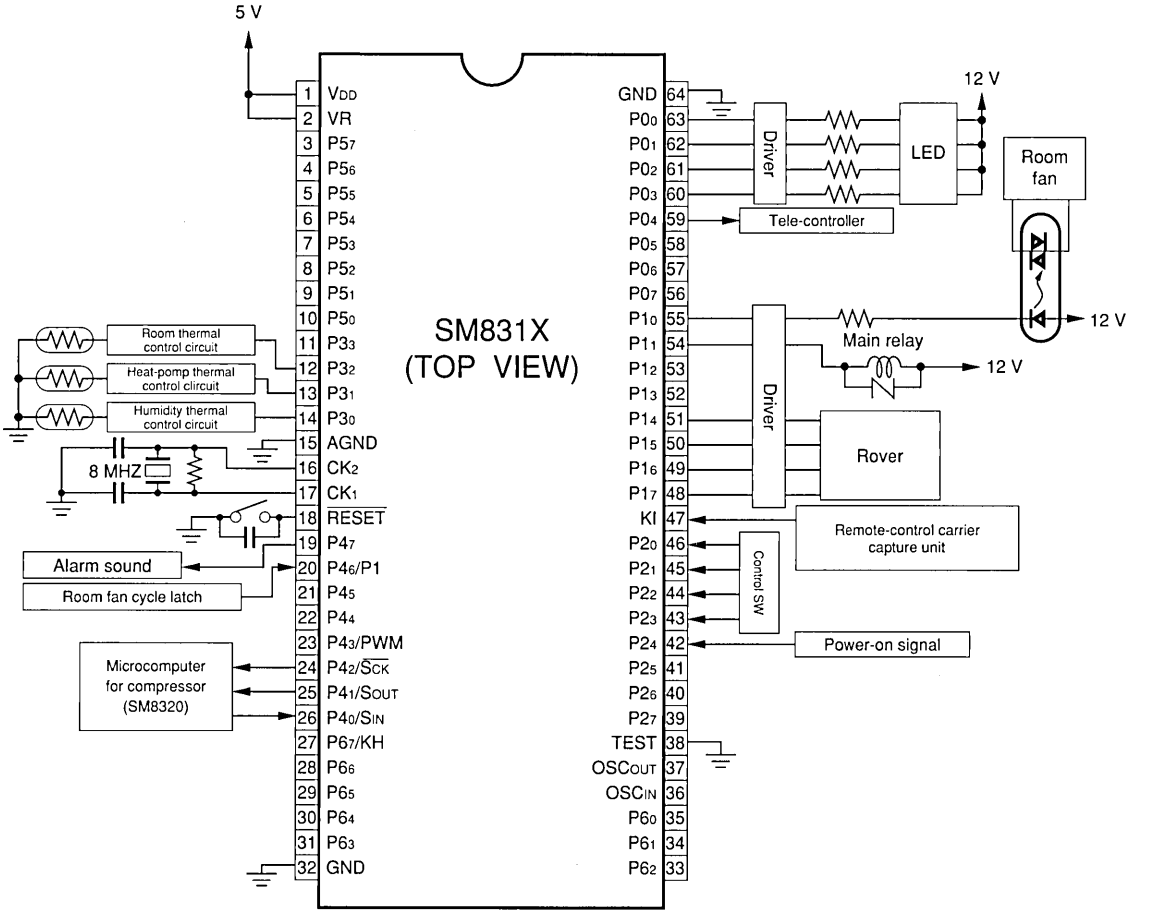
Call and Return Instructions

MNEMONIC	OPERATION
CALL cc, nn	if cc true ↓ (SP–1) ← PC_H (SP–2) ← PC_L PC ← nn SP ← SP–2 else next Inst.
CALL nn	(SP–1) ← PC_H (SP–2) ← PC_L PC ← nn SP ← SP–2
RET	PC ← (SP) PC_H ← (SP+1) SP ← SP+2
RET cc	if cc true ↓ PC ← (SP) PC_H ← (SP+1) SP ← SP+2 else next Inst.
RETI *	PC_L ← (SP) PC_H ← (SP+1) SP ← SP+2 IME ← 1
RST t	(SP–1) ← PC_H (SP–2) ← PC_L SP ← SP–2 PC_H ← 0 PC_L ← P

* At the maskable interrupt, the IME flag is forced to set and the program returns. At the non-maskable interrupt, the IME flag is recovered and the program returns. When DI instruction is executed within a non-maskable interrupt processing, IME flag is reset and the program returns. In contrast, if EI instruction is executed, IME flag is set and the program also returns.

SYSTEM CONFIGURATION EXAMPLE

• **Inverter air conditioner**



4-BIT SINGLE-CHIP MICROCOMPUTERS

SM5L1/5L2/5L3

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

The SM5L1/5L2/5L3 is CMOS 4-bit single-chip microcomputers operated in single 1.5 V power supply. This microcomputer integrates 4-bit parallel processing function, ROM, RAM, display RAM, 15-stage divider, 2-kind of interrupt and 4-level of subroutine stack. With a built-in LCD drive circuit for maximum of 84/136/168/ (SM5L1/5L2/5L3) elements, a 2-mode standby function, and a melody generator circuit in a single chip, the SM5L1/5L2/5L3 permits the design of system configuration with a minimum of peripheral components. It can be used in a variety of products from handheld equipment to electrical appliances, such as audio timers, and also achieves low power consumption.

FEATURES

- ROM capacity : 2 048 x 8 bits (SM5L1)
  3 072 x 8 bits (SM5L2)
  4 096 x 8 bits (SM5L3)
- RAM capacity :
  69 x 4 bits (including 21 x 4 bits display RAM) (SM5L1)
  130 x 4 bits (including 34 x 4 bits display RAM) (SM5L2)
  170 x 4 bits (including 42 x 4 bits display RAM) (SM5L3)
- Instruction sets : 51
- Subroutine nesting : 4 levels
- I/O port :

Input	1
Output	5
Input/output	8

- Interrupts :

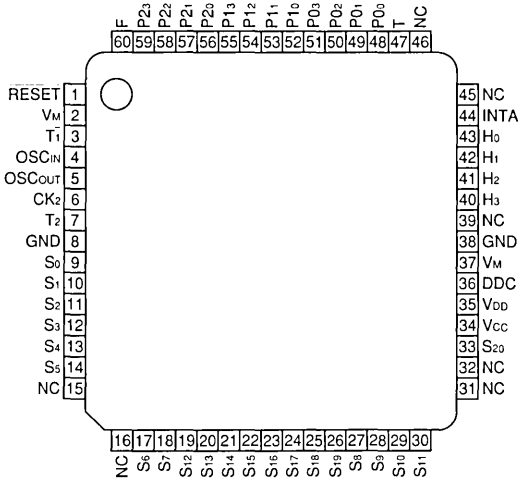
Internal interrupt	x 1 (INTA)
External interrupt	x 1 (divider overflow)

- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver :
  84 segments (SM5L1) / 136 segments (SM5L2) / 168 segments (SM5L3), 1/2 bias, 1/4 duty cycle
- Built-in melody generator circuit :
  Melody ROM
  160 steps (SM5L1), 256 steps (SM5L2/5L3)
  Generating time (at 32.768 kHz)
  20 s (MAX.) (SM5L1)
  32 s (MAX.) (SM5L2/5L3)
- Instruction cycle time : 61 µs (TYP., at 32.768 kHz)
- Standby function
- Supply voltage :
  1.5 V ± 10% (SM5L1)
  1.5 V ± 20% (SM5L2/5L3)
- Packages :
  60-pin QFP (QFP060-P-1414) (SM5L1)
  72-pin QFP (QFP072-P-1010) (SM5L2)
  80-pin QFP (QFP080-P-1420) (SM5L2/5L3)

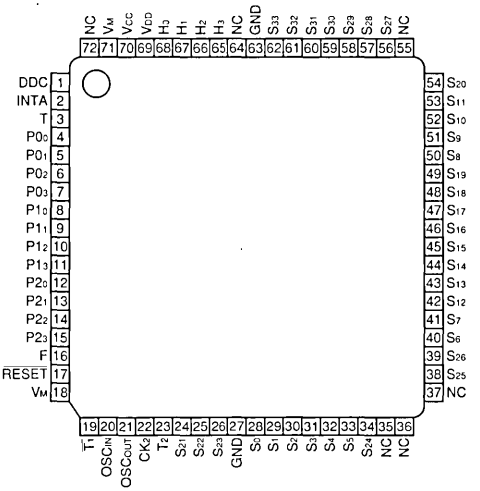
PIN CONNECTIONS

TOP VIEW

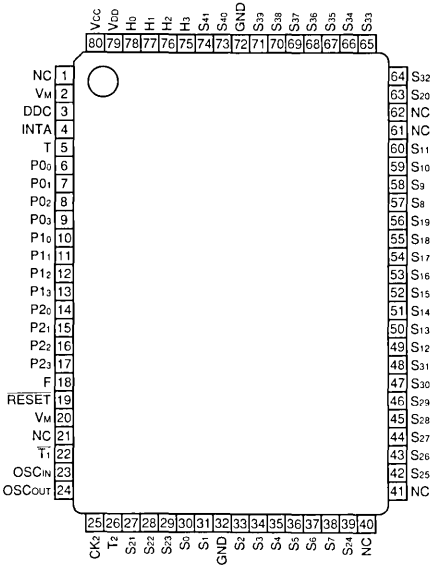
60-PIN QFP (SM5L1)



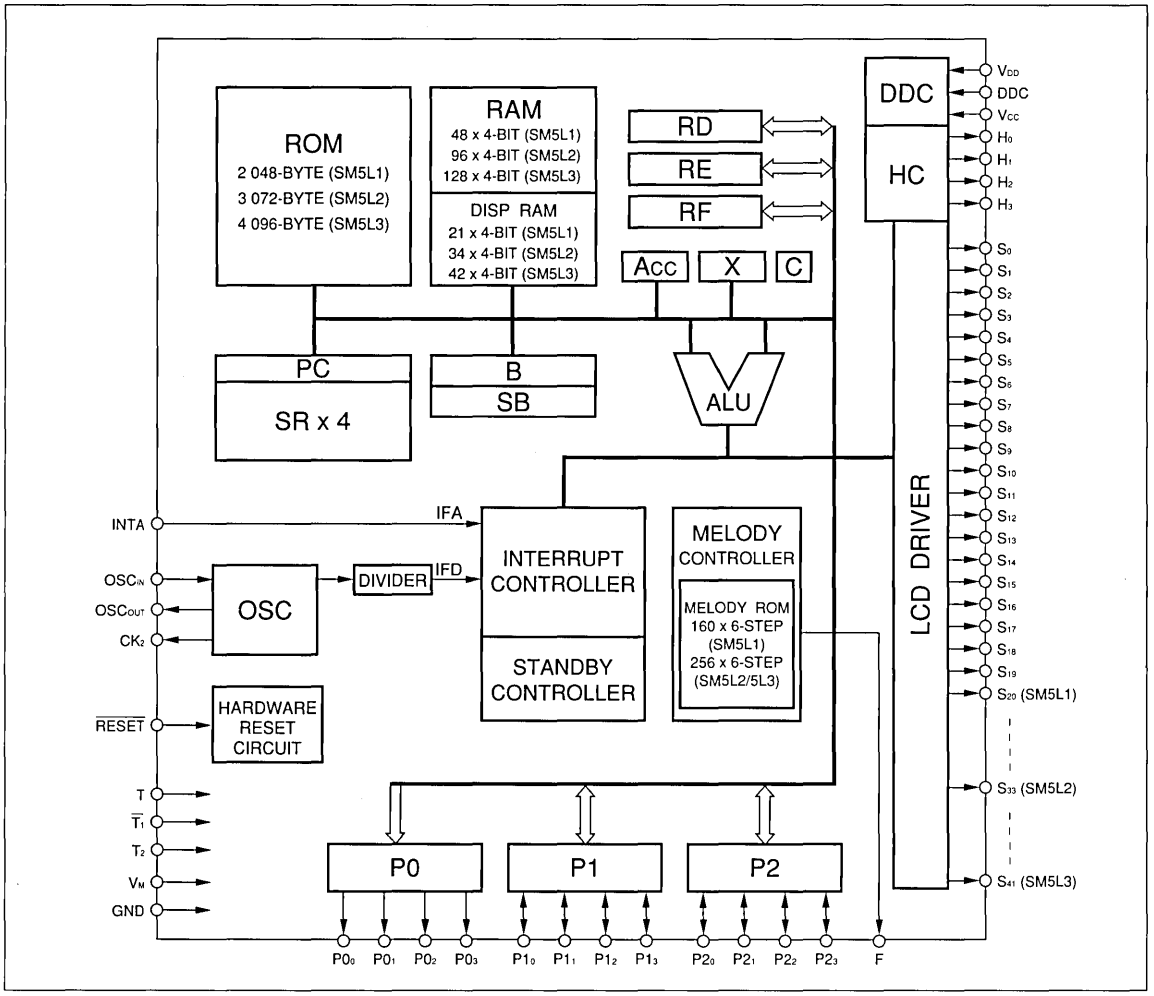
72-PIN QFP (SM5L2)



80-PIN QFP (SM5L2/SM5L3)



BLOCK DIAGRAM



Nomenclature

ACC	: Accumulator	P0-P2	: Port registers
ALU	: Arithmetic logic unit	PC	: Program counter
B	: RAM address register	RAM	: Data memory
C	: Carry flag	RD, RE, RF	: Mode registers
DDC	: Display boost circuit	ROM	: Program memory
HC	: Backplate signal generator circuit	SB	: Stack B register
IFA	: External interrupt flag	SR	: PC stack register
IFD	: Divider overflow flag	X	: X register
OSC	: System clock oscillator		

PIN DESCRIPTIONS

PIN NAME	I/O	FUNCTION
GND, V_M	I	Power supply pins. The V_M pin applies a positive supply with respect to the GND.
T, $\overline{T_1}$, T_2	I	LSI chip test pins. Cannot be used by the user. Connect T and T_2 pin to GND. Connect $\overline{T_1}$ pin to V_M.
$\overline{RESET}$	I	Input pin with built-in pull-up register. Hardware-reset the LSI chip when a Low level signal is input. Normally, a capacitor is connected between it and GND to form a power-on reset circuit.
OSC_{IN}, OSC_{OUT}, CK_2	I/O	CR or crystal oscillator pins. Connect a CR or crystal oscillating element across [OSC_{IN} - OSC_{OUT} (crystal)] or [OSC_{IN} - CK_2 (CR)] to form a clock generator circuit. (Use of a CR or crystal oscillating element is determined by the mask option)
F	O	Melody output pin. Outputs the contents of a melody ROM with 12-musical scale (555 to 2114 Hz) in two octaves.
H_0-H_3	O	Backplate output pins. Pins for the LCD's backplate signals.
S_0-S_{20} (SM5L1) S_0-S_{33} (SM5L2) S_0-S_{41} (SM5L3)	O	Pins for the LCD's segment signals.
INTA	I	Input pin for external interrupt. The IFA flag is set at the leading edge of INTA.
$P0_0$-$P0_3$	O	Output pins. The accumulator Acc can be transferred to this port by instruction.
$P1_0$-$P1_3$, $P2_0$-$P2_3$	I/O	I/O pins which can switch to input or output pins in 4-bit units by instruction. They can be used as output pins when configured for a key matrix. The SM5Lx is forced to hardware-reset when all of $P1_0$ to $P1_3$ pins are High level. (By mask option)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_M	−0.3 to 2.0	V	
	V_{DD}	−0.3 to 4.0		
Input voltage	V_I	−0.3 to V_M + 0.3	V	
Output voltage	V_O	−0.3 to V_M + 0.3	V	
Source output current for each pin	I_{O1}	2	mA	1
	I_{O2}	2	mA	2
	I_{O3}	2	mA	3
	I_{O4}	2	mA	4
Sink output current for each pin	I_{O5}	2	mA	1
	I_{O6}	100	μA	2
	I_{O7}	2	mA	3
	I_{O8}	2	mA	4
Total source output current	I_{OH}	10	mA	
Total sink output current	I_{OL}	10	mA	
Operating temperature	T_{OPR}	0 to 50	°C	
Storage temperature	T_{STG}	−55 to 150	°C	

NOTES :

1. Applicable pins : $P0_0$-$P0_3$
2. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
3. Applicable pins : F
4. Applicable pins : H_0-H_3, S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)

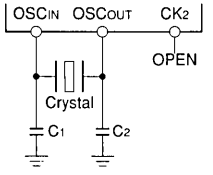
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_M	1.35 to 1.65 (SM5L1) 1.2 to 1.8 (SM5L2/5L3)	V	
	V_{DD}	2.4 to 3.6		
Instruction cycle	T_{SYS}	122 to 50	μs	
Oscillation starting voltage	V_{OSC}	1.4	V	1

NOTE :

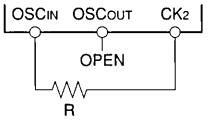
1. Use the crystal oscillation circuit

Oscillation Circuit



Crystal : 32.768 kHz
C_1 = 8 pF
C_2 = 8 pF

Crystal oscillation (frequency = 32.768 kHz)



Degree of fluctuation frequency : ± 30%
(V_M = 1.5 V, T_{OPR} = 25°C)

CR oscillation (frequency = 40 kHz)

NOTE :

Mount the R, C and crystal as close to the LSI chip as possible to minimize the effects of stray capacitance.

DC CHARACTERISTICS

(V_M = 1.5 ± 0.1 V, Ta = 0 to +50°C)

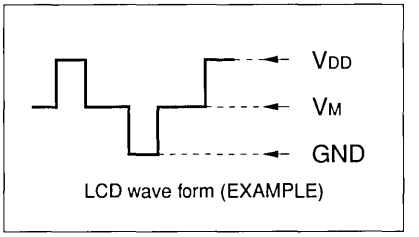
PARAMETER	SYMBOL	CONDITIONS	MIN.*1	TYP.*2	MAX.*1	UNIT	NOTE
Input voltage	V_{IH1}		0.8 x V_M		V_M	V	1
	V_{IL1}		0		0.2 x V_M		
	V_{IH2}		V_M–0.25		V_M	V	2
	V_{IL2}		0		0.25		
Input current	I_{IH1}	V_{IH} = V_M			1.0	μA	3
	I_{IH2}	V_{IH} = V_M		1.5/3/3			4
	I_{IL1}	V_{IL} = 0 V		1.5/3/3			5
Boost output voltage	V_{DD1}	V_M = 1.4 V RL = 5 MΩ	2.5			V	6
	V_{DD2}	V_M = 1.6 V RL = 5 MΩ	2.9				
Output current	$-I_{OH1}$	V_{OH} = V_M–0.5 V	100			μA	7
	I_{OL1}	V_{OL} = 0.5 V	100				
	$-I_{OH2}$	V_{OH} = V_M–0.5 V	100				8
	I_{OL2}	V_{OL} = 0.5 V	3.0				
Output impedance	D_{COM}	V_M = 1.5 V		15		kΩ	9
	D_S	V_M = 1.5 V		30			10
Supply current	I_{DA}	V_M = 1.5 V T_{SYS} = 122 μs		8/10/12	15	μA	11
	I_{DH1} (Halt mode)			5/7/8	8		12
	I_{DH2} (Halt mode)			3/4/5	5		13
	I_{DS} (Stop mode)			1/1.5/2	3		14

*1 : SM5L1's spec.

*2 : */*/* → SM5L1/5L2/5L3

NOTES :

1. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, T, INTA
3. Applicable pins : $P2_0$-$P2_3$
4. Applicable pins : T, INTA, $P1_0$-$P1_3$
5. Applicable pins : $\overline{RESET}$
6. Applicable pins : V_{DD}
7. Applicable pins : $P0_0$-$P0_3$, F
8. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
9. Applicable pins : H_0-H_3
10. Applicable pins : S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)
11. No-load condition. Supply current under the operation when driving a CR oscillator.
12. No-load condition. Supply current when driving a CR oscillator and turning LCD ON placed the device in halt mode.
13. No-load condition. Supply current when driving a CR oscillator and turning LCD OFF placed the device in halt mode.
14. No-load condition. Supply current when the entire system is inactivated.



LCD wave form (EXAMPLE)

SYSTEM CONFIGURATION

A Resister and X Register

The A register (or accumulator : Acc) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM, to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data.

A pair of A and X registers can accommodate 8-bit data.

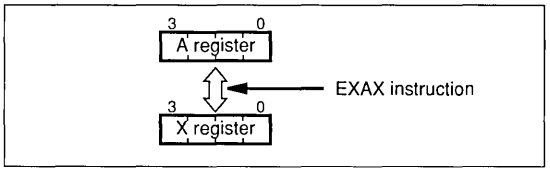


Fig. 1 Data Transfer Example Between A Register, and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation.

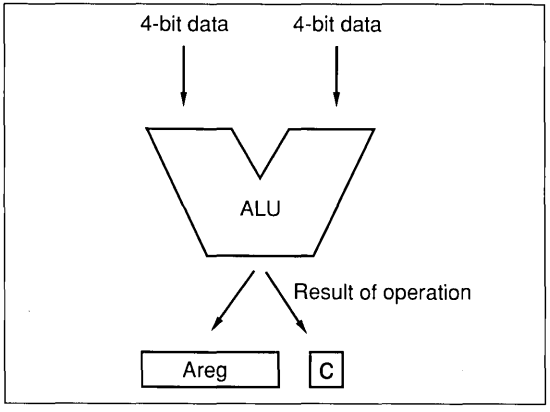


Fig. 2 ALU

The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy : ADC instruction sets/clear the content of the C flag; ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

B Register and SB Register

• B register (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address.

The upper 4-bit section is called B_M register and lower 4-bit B_L.

• SB register

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

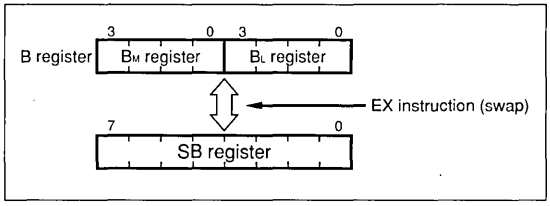


Fig. 3 B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used for data storage. The RAM capacity consists of

- SM5L1 : 69 x 4-bit (include 21 x 4-bit display RAM)
- SM5L2 : 130 x 4-bit (include 34 x 4-bit display RAM)
- SM5L3 : 170 x 4-bit (include 42 x 4-bit display RAM)

Display RAM which outputs data to an external pin for driving the segments of the LCD. Therefore, by writing data to the display RAM, the LCD can be driven at 1/4 duty (1/2 bias) to enable automatic display of the LCD.

As shown in Fig. 7 the display RAM is connected to segment outputs

- SM5L1 : Port S_0 to S_{20}
- SM5L2 : Port S_0 to S_{33}
- SM5L3 : Port S_0 to S_{41}

which correspond to the LCD backplate outputs H_0 to H_3. Data M_0 to M_3 for one column of the display RAM is output pins as a LCD drive waveform which corresponds to outputs H_0 to H_3. As a RAM, the display RAM operates exactly the same as other RAMs.

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}					
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}						

* The area surrounded by the thick line represents the display RAM where S_0 to S_{20} corresponds to the segment output.

Fig. 4 RAM Organization (SM5L1)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}															
B	S_{33}															

* The area surrounded by the thick line represents the display RAM where S_0 to S_{33} corresponds to the segment output.

Fig. 5 RAM Organization (SM5L2)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}	S_{34}	S_{36}	S_{38}	S_{40}											
B	S_{33}	S_{35}	S_{37}	S_{39}	S_{41}											

* The area surrounded by the thick line represents the display RAM where S_0 to S_{41} corresponds to the segment output.

Fig. 6 RAM Organization (SM5L3)

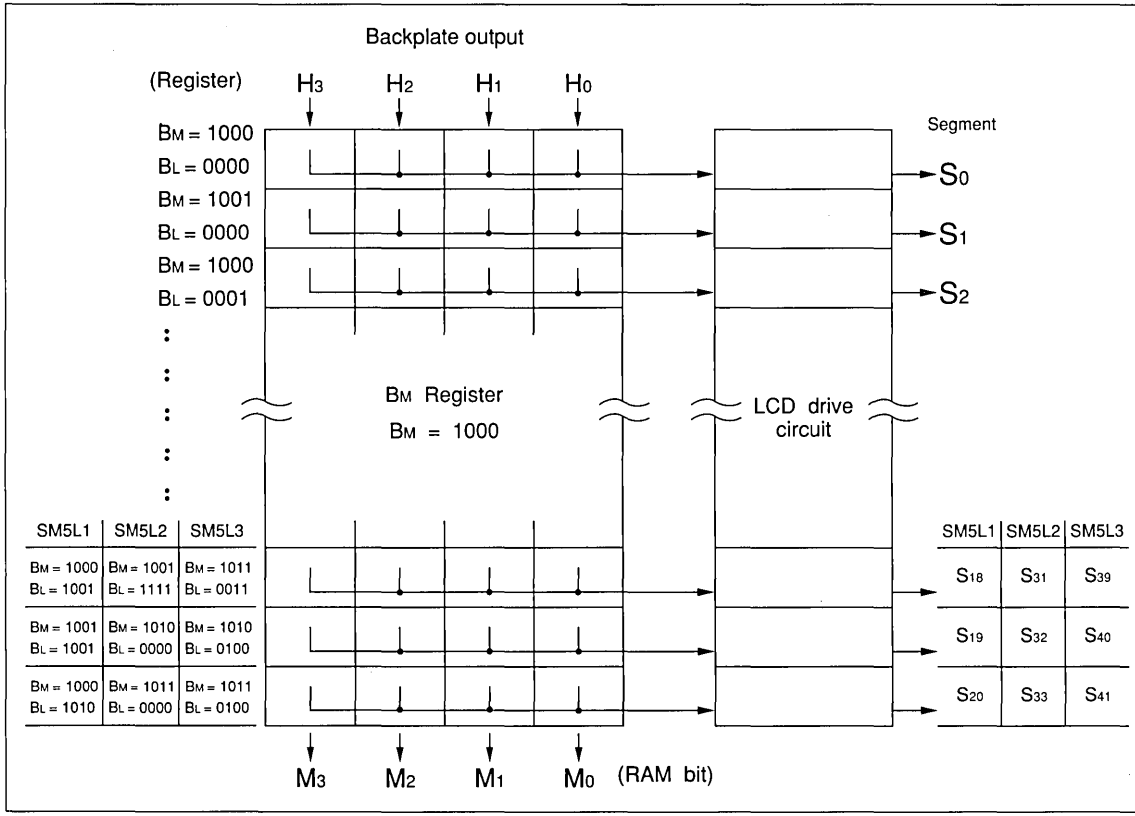


Fig. 7 Relationship between the Display RAM and LCD Segment Outputs / Backplate Outputs

Program Counter PC and Stack Register SR

A ROM address is specified by the program counter (PC). The PC comprises 12-bit where 6-bit (P_U) are used to specify the page (see Fig. 8) and 6-bit (P_L) are used to specify the step. P_U is a register and P_L is a binary counter.

The table reference instruction PAT executes a similar operation to that of the subroutine jump and uses one level of the stack register.

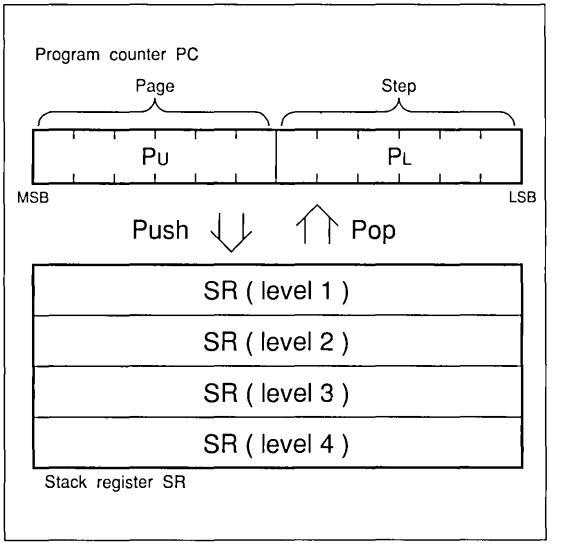


Fig. 8 Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used for program storage. The ROM capacity of the SM5Lx is 2 048/3 072/4 096-step (SM5L1/5L2/5L3). The ROM is organized into 32/48/64 (SM5L1/5L2/5L3)-page where one page is organized into 64-step.

Page	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH
PU	000000	000001	000010	000011	000100	000101	000110	000111	001000	001001	001010	001011	001100	001101	001110	001111
	Program start	First page of subroutine TRS	Interrupt	Standby release	Table reference page PAT											

Page	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
PU	010000	010001	010010	010011	010100	010101	010110	010111	011000	011001	011010	011011	011100	011101	011110	011111
																Last page (SM5L1)

Page	20H	21H	22H	23H	24H	25H	26H	27H	28H	29H	2AH	2BH	2CH	2DH	2EH	2FH
PU	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111
																Last page (SM5L2)

Page	30H	31H	32H	33H	34H	35H	36H	37H	38H	39H	3AH	3BH	3CH	3DH	3EH	3FH
PU	110000	110001	110010	110011	110100	110101	110110	110111	111000	111001	111010	111011	111100	111101	111110	111111
																Last Page (SM5L3)

Fig. 9 ROM Organization

Flags

The SM5Lx provides 3-flag (C flag and interrupt request flag <IFA, IF0>) which can be used to set or determine conditions.

Output Latch Registers and Mode Registers

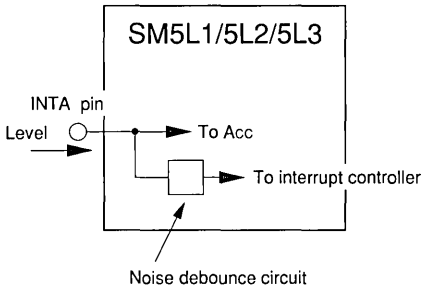
The output latch registers are connected to the P0, P1 and P2 pins. By instruction, the contents of the Acc can be transferred to the output latch registers. The SM5Lx also contains mode registers RD, RE, and RF. Setting the value of each register enables the LCD or interrupt to be controlled. Setting a register is performed in the same way as the other output pins. The functions of the mode registers are shown in Table 1.

• INTA pin

INTA level can be loaded to Acc (bit 0), as follows.

```
LBLX  4
IN
```

In case, INTA level does not through the noise debounce circuit.



CAUTION :

Connecting considerations of I/O port

When using an I/O port as bidirectional bus such as data bus, avoid setting the I/O port to output when the target pin is also set to output.

Whenever the both output data conflict each other, system failure will be causes due to damage to circuits or instantaneous supply voltage drop.

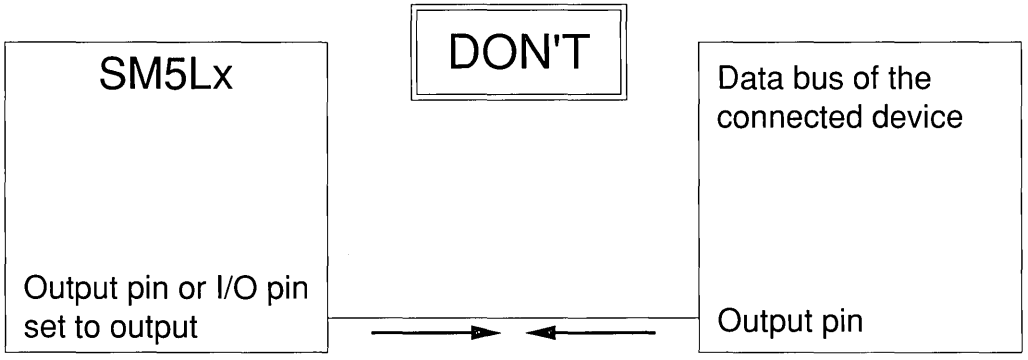


Table 1 Mode Register Setting

REGISTER TYPE	REGISTER BIT	SET VALUE	MODE DESCRIPTION
RD	RD0	0	Clear the ME F/F to stop a melody.
		1	Set the ME F/F to start a melody from a ROM pointer address.
	RD1		Set by stop instruction (of melody code) and reset by TPB instruction.
	RD2	–	Set to "0" only.
	RD3		
RE	RE0	0	Mask the interrupt based on the IFA flag.
		1	Accept the interrupt based on the IFA flag.
	RE1	–	Set to "0" only.
	RE2	0	Mask the interrupt based on the IFD flag.
		1	Accept the interrupt based on the IFD flag.
	RE3	–	No setting.
RF	RF0	0	Turn off the LCD.
		1	Turn on the LCD.
	RF1	0	Stop the function of a booster circuit.
		1	Operate the function of a booster circuit.
	RF2	0	Create the system clock frequency by dividing two the main oscillation frequency.
		1	Create the system clock frequency by dividing four the main oscillation frequency.
	RF3	–	Set to "0" only.

System Clock Generator and Dividers

The main oscillation frequency which is input through "OSC_{IN} - OSC_{OUT}" or "OSC_{IN} - CK_2" is divided into 2 or 4 to generate the system clock f_{SYS} (Fig. 10).

System clock f_{SYS} determines the execution instruction cycle so that the system clock period is the same as the instruction cycle.

However, the instruction execution cycle of two-word instruction is twice that of one-word instructions.

Use of a CR oscillating element or a crystal oscillating element for the oscillator circuit is determined by the mask option. On the final stage of the divider, fc can be set to 1 Hz or 2 Hz (in case of 32 kHz crystal oscillation) depending on the mask option.

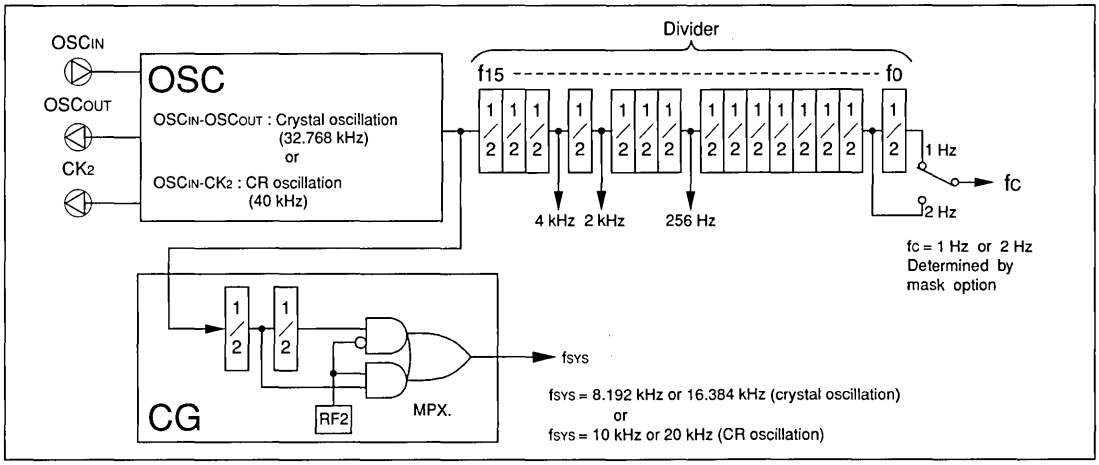


Fig. 10 System Clock Generator and Divider

Either of the system clock frequencies 16.384 kHz or 8.192 kHz (in case of 32.768 kHz oscillation) can be selected by the RF2 flag (See Table 2). The 8.192 kHz clock has slower command execution speed, but uses less power for the same function.

The system clock is initialized to 16.384 kHz after Hardware reset operation.

The Table 2 shows the relationship between the contents of RF2 flag for OSC resonator and the generated frequency, f_{SYS}.

Table 2 OSC Resonator and Frequency f_{SYS}

FOR OSC RESONATOR	CONTENTS OF RF2 FLAG	GENERATED FREQUENCY f_{SYS}
32.768 kHz crystal oscillation	0	16.384 kHz
	1	8.192 kHz
40 kHz CR oscillation	0	20 kHz
	1	10 kHz

FUNCTIONAL DESCRIPTION

Melody Output Function

The built-in chip melody generation circuit provides a variety of sound signals. Fig. 11 shows the block diagram of the melody generating circuit.

The melody ROM can store notes, rest and stop commands in 160/256/256 (SM5L1/5L2/5L3)-step (1 step consists of 6-bit), allowing the generation of 12-scale over two octaves (555 to 2 097 Hz) and the section of the time base for notes (125/62.5 ms).

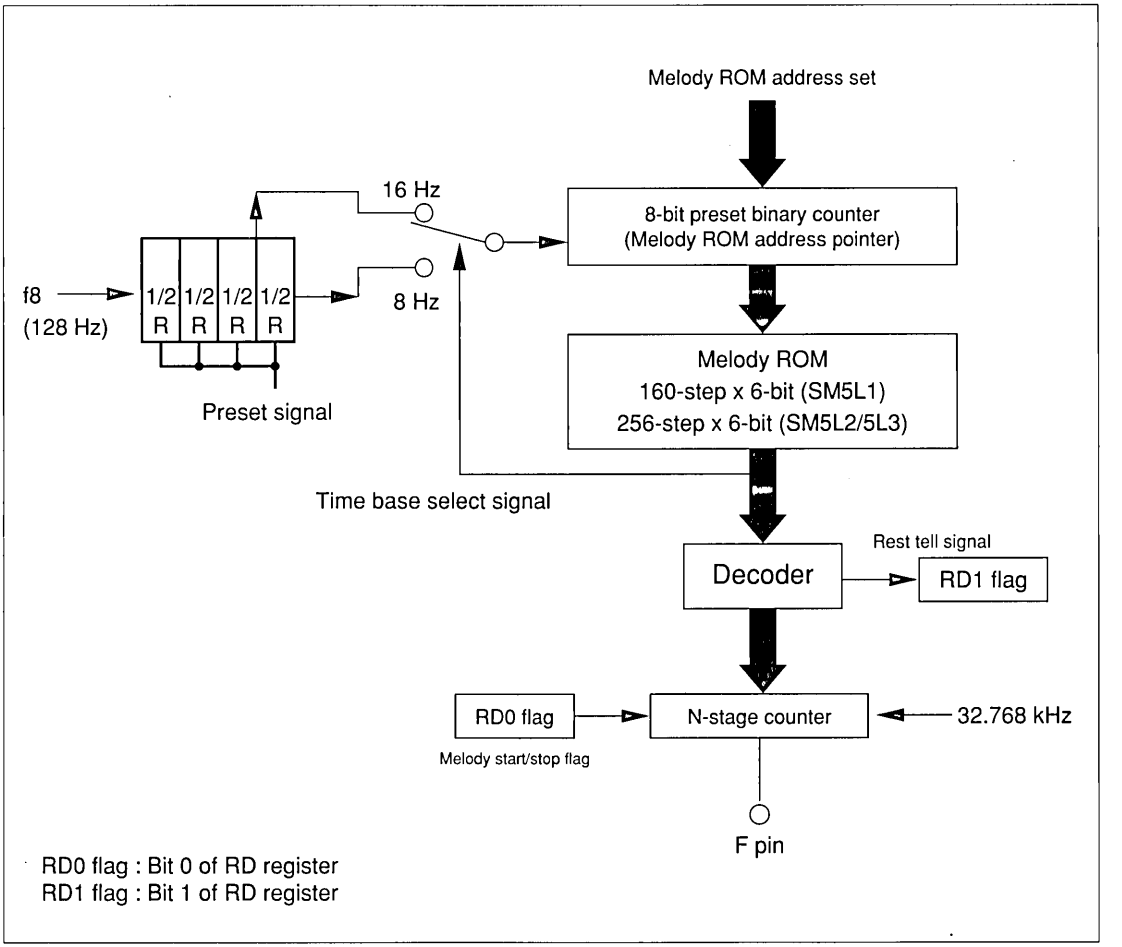


Fig. 11 Melody Generating Circuit

CONTROL PROCEDURE

The binary counter for designating the address of the melody ROM can be arbitrarily set using the PRE instruction. A performance is started and stopped by the RD0-flag to "1" and "0".

The stop code generates a "rest tell signal", and at the same time, sets the RD1 flag. The end of the melody can be found by testing the RD1 flag.

Accordingly, to stop a performance at the end of melody, the RD0 flag must be clear upon detection of RD1 flag = 1.

Next step of PRE instruction, put the NOP instruction.

The following is an example of a melody generating program.

```
MELO    LAX     2
        ATX
        LAX     1
        PRE             ; Set the starting address of
                          the melody at the 21st.
                          Hexadecimal step.
        NOP             ; Dummy command
        :
        :
        LBLX    0DH
        LAX     1
        OUT             ; Start the melody
        TPB     1       ; Executed for clear the
                          RD1 flag
        NOP             ; Dummy command
        :
        :
        LBLX    0DH
L1      TPB     1       ; Test the RD1 flag
        TR      L1      ; Loop for detect the stop
                          code
        LAX     0
        OUT             ; Stop the melody
```

Using these functions, the user can generate music, sound effects, alarm signals, etc. as desired, and any portion of the music can be repeated. Table 3 lists the melody output frequencies. The output frequency can be halved by making bit 5 (OCT) of the melody ROM 0 (Low). In Table 3, m0 to m3 show data in bits 1 to 4 of the melody ROM.

Table 3 Melody Output Frequency

	m_3 m_2 m_1 m_0	OUTPUT FREQUENCY (Hz)	CLOCK NUMBER *1	*2
do	0 0 1 0	2114.1	15.5	7 8 8 8
si	0 0 1 1	1985.9	16.5	8 8 8 9
la#	0 1 0 0	1872.4	17.5	8 9 9 9
la	0 1 0 1	1771.2	18.5	9 9 9 10
sol#	0 1 1 0	1680.4	19.5	9 10 10 10
sol	0 1 1 1	1560.4	21.0	10 11 10 11
fa#	1 0 0 0	1489.5	22.0	11 11 11 11
fa	1 0 0 1	1394.4	23.5	11 12 12 12
mi	1 0 1 0	1310.7	25.0	12 13 12 13
re#	1 0 1 1	1236.5	26.5	13 13 13 14
re	1 1 0 0	1170.3	28.0	14 14 14 14
do#	1 1 0 1	1110.8	29.5	14 15 15 15

*1 Number of clocks for one cycle

*2 The number (n) in the waveforms represents the number of periods of the oscillation frequency (32.768 kHz) from the crystal oscillator for the duration in that particular part of the waveform.

MELODY ROM INSTRUCTION

The melody ROM instruction is composed of 6-bit. This 6-bit instruction (1 set), corresponding to a musical note, generates a sound signal.

I	OCT	m_3	m_2	m_1	m_0

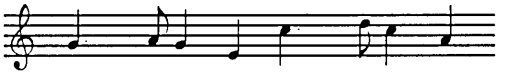
I : Control the tone length. When "1", 125 ms; when "0", 62.5 ms.

OCT : When the octave is "1", the frequency is determined by m_3 - m_0. When the octave is "0", 1/2 the frequency determined by m_3 - m_0.

m_3 - m_0 : Frequency as shown in Table 3. Pause when $m_3 = m_2 = m_1 = m_0 = 0$, stop instruction when $m_3 = m_2 = m_1 = 0$, $m_0 = 1$.

EXAMPLE OF WRITING ON THE MELODY ROM

An example of writing a tune such as the following, on the melody ROM will be shown.



MUSICAL SCALE	TONE LENGTH (ms)	OCT	m_3	m_2	m_1	m_0
sol	375	0	0	1	1	1
la	125	0	0	1	0	1
sol	250	0	0	1	1	1
mi	250	0	1	0	1	0
do	375	1	0	0	1	0
re	125	1	1	1	0	0
do	250	1	0	0	1	0
la	250	0	0	1	0	1

ADDRESS	DATA	MUSICAL NOTE INSTRUCITON
00	00	pause
01	27	sol
02	27	sol
03	27	sol
04	25	la
05	27	sol
06	27	sol
07	2A	mi
08	2A	mi
09	22	do
0A	22	do
0B	22	do
0C	3C	re
0D	22	do
0E	22	do
0F	25	la
10	25	la
11	01	stop

The tone length of an initial musical note which is generated from ROM addressed data assigned by a PRE instruction has an error of maximum ±4 ms. Therefore, by applying a pause as an initial note, a melody performs with a precisely regulated tone length.

Standby Function

A standby function is available which temporary stops program execution to conserve power consumption. The state during which a program is in execution is called the operation mode and the state during which the execution is temporary stopped is called the standby mode.

The standby mode further contains two modes, the stop mode and the halt mode. The stop mode stops the system section. In the stop mode, the display (LCD) is blanked. And the response speed of LCD returning to the display state (the operation) drops slightly.

The halt mode stops only system clock generator circuit (the state of the LCD is retained). This mode is used to activate the system immediately after a condition cause a release to the operation mode.

To enter the standby mode, select either stop mode or halt mode whichever appropriate. (Fig. 12)

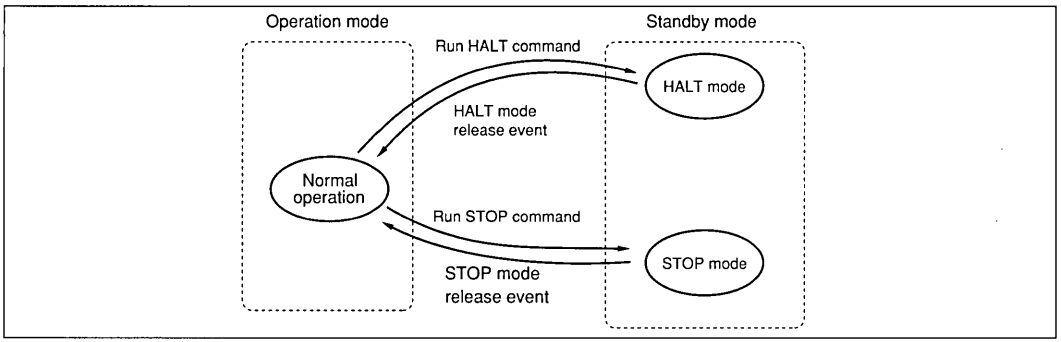


Fig. 12 Operation Shift of Program

During the standby mode, the contents of the RAM and C flag are retained. The contents of the flags, registers and output latches shown below are also retained.

FLAG
IFA flag
IFD flag
IME flag

REGISTER
Acc
X register
BM, BL register
SP
SR

OUTPUT LATCH REGISTER
P0 register
P1 register
P2 register

A release from the standby mode to the operation mode is performed by a reset port input, an interrupt from the nonmaskable INTA, and divider. A maskable interrupt request cannot become a factor in releasing back to the operation mode. The mask setting is performed with RE register. (see Table 2)

CAUTION :

When all of P10 to P13 level are High, the SM5Lx is performed to release the standby mode and enter normally hardware reset operation. (Mask option)

Next, the transition of the standby mode and the release method from the standby mode are described.

TRANSITION FORM THE OPERATION MODE TO THE STANDBY MODE

The HALT instruction is executed to set the halt mode and the STOP instruction is executed to set the stop mode.

Since the interrupt is used to release from the standby mode, the mode does not transfer to the standby mode if any of the following conditions are satisfied during execution of the STOP or HALT instruction.

a) RE0 is set and the INTA level is High.

b) RE2 is set and the IFD flag is set.

If any of the conditions above is satisfied, the mode does not transfer to the standby mode even if the STOP or HALT instruction is executed and the instruction at the address following that of the STOP or HALT instruction is executed. Therefore, place the JUMP instruction which specifies step 0 on page 3 to the location at the address following that of the STOP or HALT instruction.

RELEASE FROM THE STANDBY MODE TO THE OPERATION MODE

Release based on an interrupt request from the INTA pin, or divider overflow. However, the reset is limited to a nonmaskable interrupt request.

The program restarts from step 0 on page 3. However, if the IME flag is set, the instruction at step 0 on page 3 is executed and a subroutine jump is performed to the interrupt processing routine specified on page 2 according to the type of interrupt.

Even if Low level input on INTA pin is removed before 900 command cycles, the stop mode is released.

However, the program will not jump to 20_H page (interrupt process routine).

Interrupt request flag IFA is not set : the program continues at step 0 of 03_H page.

Interrupts

Interrupts originate from an INTA input or divider overflow. The IFA, and IFD flags become interrupt request flags.

The interrupt block is composed of mask flags (RE0, RE2), the IME flag and interrupt processing circuit.

As shown in Fig. 13, resetting a mask flag enables the interrupt request flag to be independently masked. Thus, the mask flags can be used in a program to establish the interrupt priority. The priority for interrupts generated simultaneously is shown in Table 4.

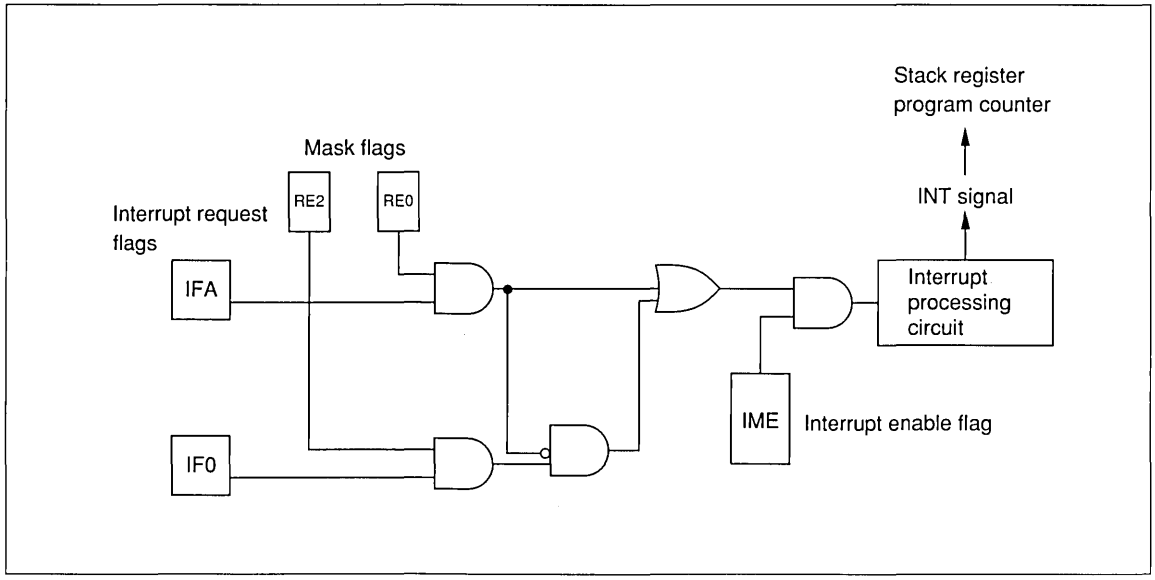


Fig. 13 Interrupt Block

Table 4 Interrupt Event Summary

INTERRUPT REQUEST (REQUEST FLAG)	JUMP DESTINATION		PRIORITY ORDER	INTERRUPT ENABLE FLAG
	PAGE	STEP		
INTA input (IFA)	2	0	1	RE0
Divider overflow (IFD)	2	4	2	RE2

When the IME flag is set, the interrupt circuit activates according to the interrupt request and a subroutine jump is performed to the specified address. The jump destinations according to interrupt origin are shown in Table 4. When the IME flag is cleared, an interrupt is not accepted even if an interrupt request is generated. The interrupt timing are shown in Fig. 14 and Fig. 15. The timing chart shown in Fig. 14 shows the interrupt enable state when an interrupt request has been generated. In this case, the interrupt processing signal INT goes High, one instruction cycle after the interrupt request flag is set. When INT goes High, the contents of the program counter are pushed into the stack register and execution jumps to the specified address. At this time, the INT signal and the IME flag are cleared to establish the interrupt disable mode. The IME flag is set again when the RTNI instruction is executed to establish the interrupt enable mode.

The timing chart shown in Fig. 15 shows the state when interrupts are enabled while multiple interrupts are generated. In this case, a subroutine jump is performed according to the interrupt having the highest priority. When returning from the subroutine by executing the RTNI instruction, the instruction (two words are executed for a two-word instruction) at the location of return is executed and the interrupt for the next highest priority is accepted.

If an interrupt request is generated during execution of a two-cycle instruction, the instruction is executed after which interrupt processing is performed. If consecutive LAX instructions are skipped or if the SKIP conditions are satisfied, the skip operation is terminated after which interrupt processing is performed.

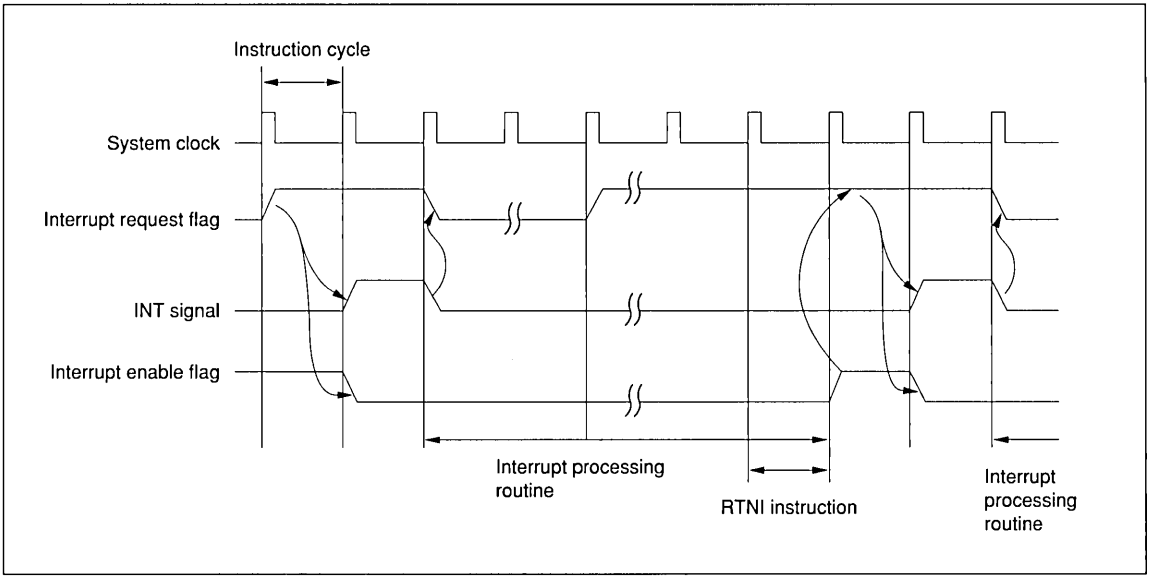


Fig. 14 Interrupt Timing Chart

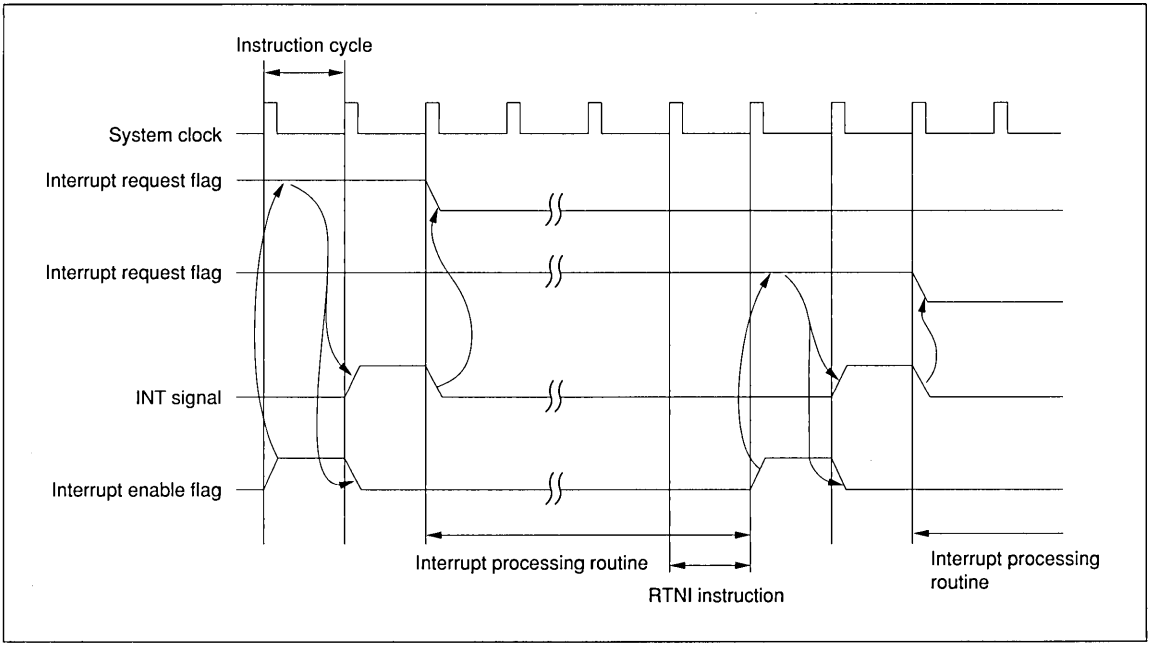


Fig. 15 Interrupt Timing Chart

NOTE :

Fig. 14 and Fig. 15 show the case where the interrupt request flags are not masked.

Hardware Reset Function

The hardware reset function mode activated two instruction cycles after the trailing edge from the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is changed from High to Low, the pulse which is input by the OSC_{IN} pin is counted 2^{15} times after which the reset mode clears and the program counter starts from address 0 on page 0.

The initialized status of the system after reset is shown in Table 5.

The following reset functions are available.

- The I/O port is set as an input port and the mode register RD, RE and RF are cleared. The output only port (P0) is cleared and output Low.
- The interrupt request flags (IFA, IFD) and the interrupt enable flag (IME) are clear and all interrupts become disabled.
- The program counter start from step 0 on page 0.

For activate reset function, when power is turned on, you must be connect a capacitor (0.1 µF, TYP.) across the $\overline{\text{RESET}}$ pin and GND.

Table 5 Reset Status

FLAG OR REGISTER, X-REGISTER	STATUS (in reset mode and at program start)
PC	0
SP	Level 1
RAM	Undefined
Acc	Undefined
X-register	Undefined
P0-P2 output latch registers	0
Divider	0
IFA flag	0
IFD flag	0
IME flag	0
C flag	Undefined
B_M, B_L registers	Undefined
Register RD (bit 0)	0
Register RD (bit 1)	Undefined
Register RE (bit 2, 1, 0)	0
Register RF (bit 3, 2, 1, 0)	0

NOTE :

When all of P1 pins ($P1_0$ to $P1_3$) level goes to High, the SM5Lx is performed to reset operation. (Mask option)

LCD Function

• Display segment

The SM5Lx contains a built-in circuit which directly drive a 1/4 duty, 1/2 bias LCD.

A sample LCD pattern is shown in Fig. 16.

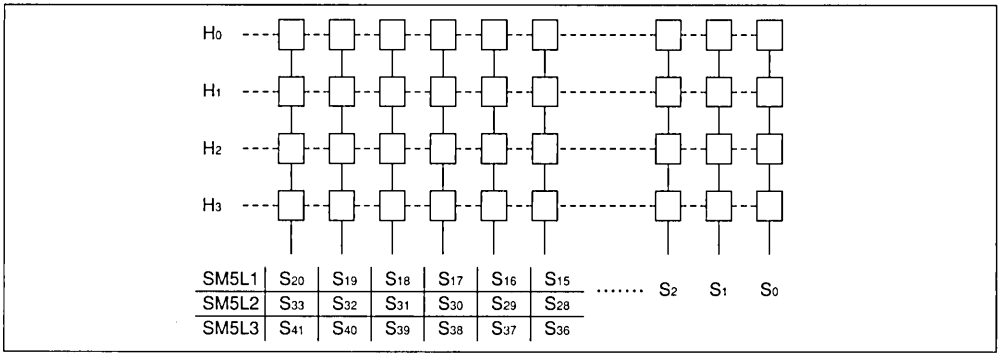


Fig. 16 LCD Pattern

A segment of the LCD can be turned on or off by setting the corresponding bit in the display RAM (see Fig. 7) to "1" or "0". The displayed segments can assume any configuration containing up to a maximum of 84/136/168 (SM5L1/5L2/5L3) segments. An example of a 7-segment numeric display is shown in Fig. 17.

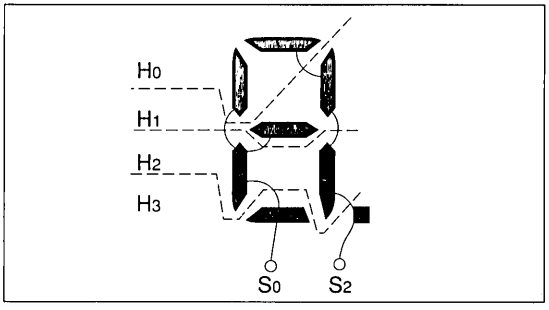


Fig. 17 Sample LCD Pattern for 7-Segment Numeric Display

• LCD drive waveforms

The LCD drive waveforms for the LCD pattern of Fig. 17 displaying a "5" are shown in Fig. 18 (the segment output uses S_0 and S_1). For Fig. 18, 3 V is applied to the V_{DD} pin, and 1.5 V is applied to the V_M pin.

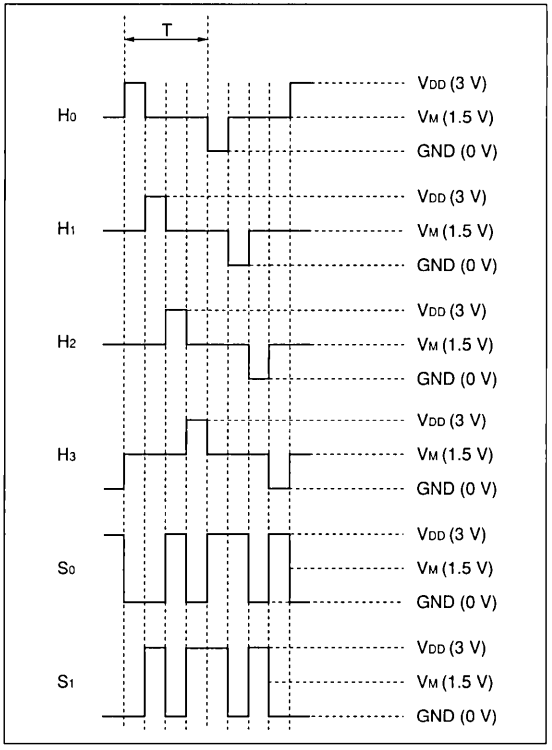


Fig. 18 LCD Drive Waveforms
(frame frequency = 1/T = 64 Hz or 128 Hz)

* Frame frequency is selectable by mask option.

• Booster circuit

The device contains a booster circuit which generates a voltage two times higher than the 1.5 V power supply.

Then, it is necessary to apply external capacitors between DDC pin and V_{CC} pin as well as V_{DD} pin and GND (see Fig. 19).

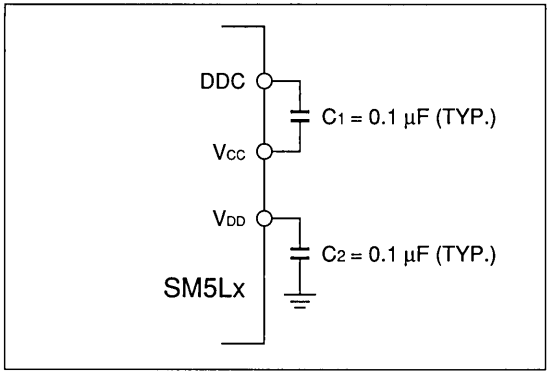


Fig. 19 Booster Circuit

• Blank display

There are two way to blank the entire display to match the purpose.

(a) Blanking the display for a short time.

Set bit 0 of the RF register to "1" : Display

Set bit 0 of the RF register to "0" : Blank state

(b) Blanking the display for a long period mainy to reduce supply current.

Set bit 0 and 1 of the RF register to "1" : Display

Set bit 0 and 1 of the RF register to "0" : Blank state

When bit 1 of the RF register is set to "0", the booster circuit does not operate and the backplate outputs and segment outputs are dropped to V_M level, and the display blanks. By stepping the function of the booster circuit, the supply current can be greatly reduced. However, when the display is blanked using method (b), the response speed of the LCD returning to the display state drops slightly. The RF register is on the blank state after initialization from hardware reset.

INSTRUCTION SET
Definition of Symbols

The following symbols are used in descriptions for the instructions.

M : Contents of RAM at the address specified by the B register
← : Transfer direction
∪ : Logical OR
∩ : Logical AND
⊕ : Logical XOR
Ai : ith bit of the Acc
Push : Content of the PC are decremented to the stack register.
Pop : The decremented contents are transferred back to the PC.
Pj : Pj register (j = 0, 1, 2, 3)
Rj : Rj register (j = D, E, F)
ROM ( ) : ROM contents for address within ( )
Cy : Carry of ALU (different from the C flag)

- Each bit of a register can be represented. For example, the ith bit of X register and R(0) register are represented as Xi and R(0) i. (i = 0, 1, 2, 3, ...)
- Increment and decrement denote the binary addition of 1_H and F_H, respectively.
- To skip a certain instruction means that the instruction is ignored and that no operation is performed until the execution transfers to the next instruction. In other words, the instruction is regarded as a NOP instruction. Therefore, one cycle is required to skip a one-word instruction and two cycles are required to skip a two-word instruction.

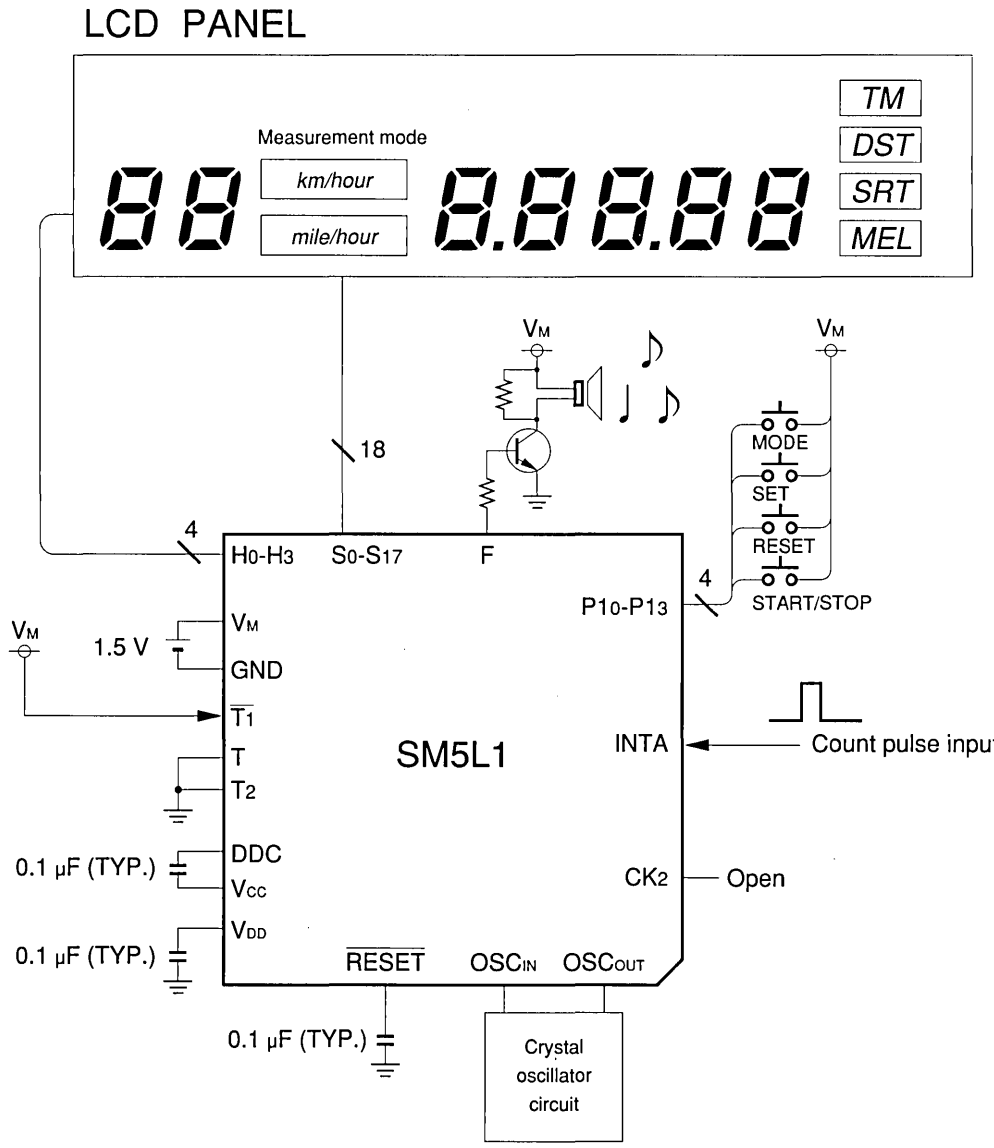
Instruction Summary

MNEMONIC	MACHINE CODE	OPERATION
ROM Address Control Instructions		
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy	E0 to EF 00 to FF	$P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
TRS x	C0 to DF	Push, $P_U \leftarrow 01_H$ $P_L \leftarrow x$ (I_4, I_3, I_2, I_1, I_0, 0)
CALL xy	F0 to FF 00 to FF	Push, $P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
RTN	7D	Pop
RTNS	7E	Pop, Skip the next step
RTNL	7F	Pop, IME $\leftarrow$ 1
Data Transfer Instructions		
LAX x	10 to 1F	$A_{CC} \leftarrow x$ (I_3-I_0)
LBMX x	30 to 2F	$B_M \leftarrow x$ (I_3-I_0)
LBLX x	20 to 2F	$B_L \leftarrow x$ (I_3-I_0)
LDA x	50 to 53	$A_{CC} \leftarrow M$ $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0) (i = 1, 0)
EXC x	54 to 57	$M \leftrightarrow A_{CC}$ $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0) (i = 1, 0)
EXCI x	58 to 5B	$M \leftrightarrow A_{CC}$, $B_L \leftarrow B_L$+1 $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0) (i = 1, 0) Skip if Cy = 1 ($B_L = F_H \rightarrow 0$)
EXCD x	5C to 5F	$M \leftrightarrow A_{CC}$, $B_L \leftarrow B_L$+F_H $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0) (i = 1, 0) Skip if Cy = 1 ($B_L = 0 \rightarrow F_H$)
EXAX	64	$A_{CC} \leftrightarrow X$
ATX	65	$x \leftarrow A_{CC}$
EXBM	66	$B_M \leftrightarrow A_{CC}$
EXBL	67	$B_L \leftrightarrow A_{CC}$
EX	68	B $\leftrightarrow$ SB
Arithmetic Instructions		
ADX x	00 to 0F	$A_{CC} \leftarrow A_{CC}$+x (I_3-I_0), Skip if Cy = 1
ADD	7A	$A_{CC} \leftarrow A_{CC}$+M
ADC	7B	$A_{CC} \leftarrow A_{CC}$ + M+C, C $\leftrightarrow$ Cy Skip if Cy = 1
COMA	79	$A_{CC} \leftarrow \overline{A_{CC}}$
INCB	78	$B_L \leftarrow B_L$+1, Skip if $B_L = F_H$
DECB	7C	$B_L \leftarrow B_L$–1, Skip if B_L = 0

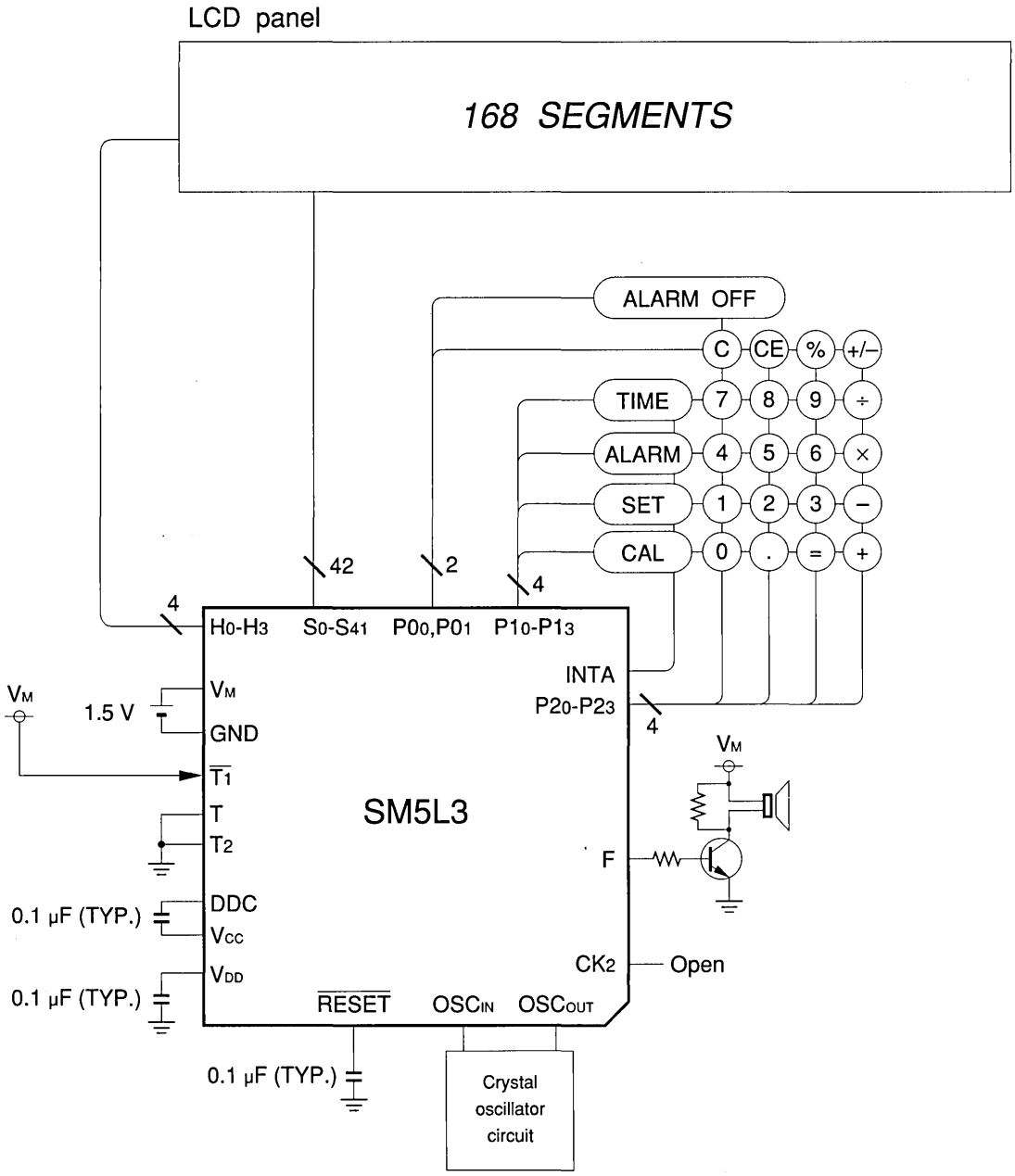
MNEMONIC	MACHINE CODE	OPERATION
Test Instructions		
TAM	6F	Skip if A_{CC} = M
TC x	6E	Skip if C = 1
TM	48 to 4B	Skip if Mi = 1 (i = 3 to 0)
TABL	6B	Skip if A = B_L
TPB x	4C to 4F	Skip if P (R) i = 1 (i = I_1, I_0)
TA	6C	Skip if IFA = 1, and (IFA $\leftarrow$ 0)
TD	69 02	Skip if IFD = 1, and (IFD $\leftarrow$ 0)
Bit Manipulation Instructions		
SM x	44 to 47	Mi $\leftarrow$ 1 (i = 3 to 0)
RM x	40 to 43	Mi $\leftarrow$ 0 (i = 3 to 0)
SC	61	c $\leftarrow$ 1
RC	60	c $\leftarrow$ 0
IE	63	IME $\leftarrow$ 1
ID	62	IME $\leftarrow$ 0
I/O Control Instructions		
INL	70	$A_{CC} \leftarrow$ P1i (i = 3 to 0)
OUTL	71	P0i $\leftarrow A_{CC}$ (i = 3 to 0)
ANP	72	Pj $\leftarrow$ Pj $\cap A_{CC}$ (j = 3 to 0)
ORP	73	Pj $\leftarrow$ Pj $\cup A_{CC}$ (j = 3 to 0)
IN	74	$A_{CC} \leftarrow$ Pj (j = 3, 2, 1)
OUT	75	Pj $\leftarrow A_{CC}$ (j = 3 to 0) Rj $\leftarrow A_{CC}$ (j = F to D)
Table Reference Instructions		
PAT	6A 00 to FF	Push $P_U \leftarrow$ (0, 4), P_L (X_1, X_0, A_{CC}) (X, A_{CC}) $\leftarrow$ I_7-I_0 Pop
Divider Instructions		
DR	69 03	DIV (f_7-f_0) Reset
DTA	69 04	$A_{CC} \leftarrow$ Divider (f_3 to f_0)
Melody Control Instructions		
PRE	6B	Melody ROM pointer preset Melody ROM pointer $\leftarrow$ X, A
Special Instructions		
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

• Sports watch



• **Watch and calculator**



SM5K4

4-Bit Single-Chip Microcomputer (Controller with 10-Bit A/D Converter)

DESCRIPTION

The SM5K4 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, ROM, RAM, 10-bit A/D converter and timer/counters.

It provides three kinds of interrupts and 4 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package : best suitable for Low power controlling, compact equipment like a precision charger.

FEATURES

- ROM capacity : 2 048 x 4 bits
- RAM capacity : 128 x 4 bits
- Instruction sets : 50
- Subroutine nesting : 4 levels
- I/O port :

Input	8 (30SDIP/32SOP/36QFP)
	5 (24SSOP)
Output	4
Input/output	12 (36QFP/32SOP)
	11 (30SDIP)
	8 (24SSOP)

- Interrupts :

Internal interrupt	x 1 (timer)
External interrupt	x 2 (2 external interrupt inputs)

- A/D converter :

Resolution	10 bits
Channels	4
Conversion cycle	122 µs (fosc = 500kHz)
Comparator mode cycle	50 µs (fosc = 500kHz)

- Timer/counter : 8 bits x 1
- Built-in main clock oscillator (CR oscillator : Capacitor is built-in) for system clock
- Oscillator frequency : 2.0 MHz (MAX.)
- Built-in 15 stages divider
- Instruction cycle time :
  1.2 µs (TYP.) (V_{DD} = 5 V, Rf = 33 kΩ)
- Large current output pins (LED direct drive) : 4
- Supply voltage : 2.7 to 5.5 V
- Packages :
  - 30-pin SDIP (SDIP030-P-0400)
  - 32-pin SOP (SOP032-P-0525)
  - 24-pin SSOP (SSOP024-P-0275)
  - 36-pin QFP (QFP036-P-1010)

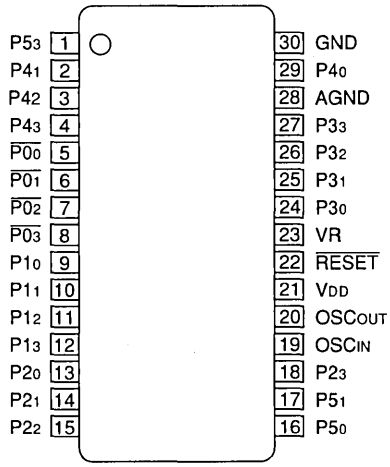
NOTE :

Refer to the SM5K5 concerning about system/functional information of SM5K4.

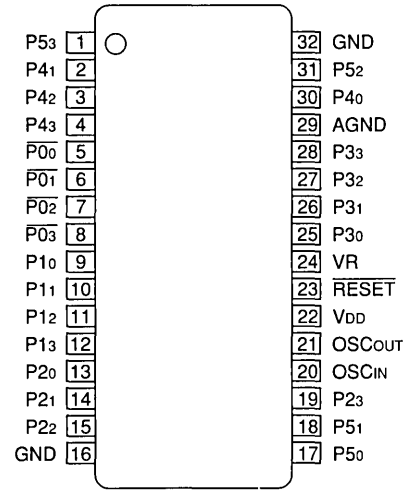
PIN CONNECTIONS

TOP VIEW

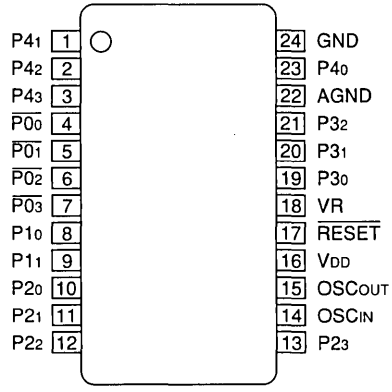
30-PIN SDIP



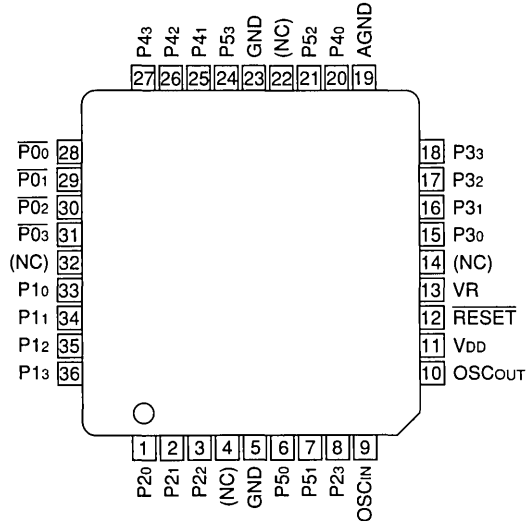
32-PIN SOP



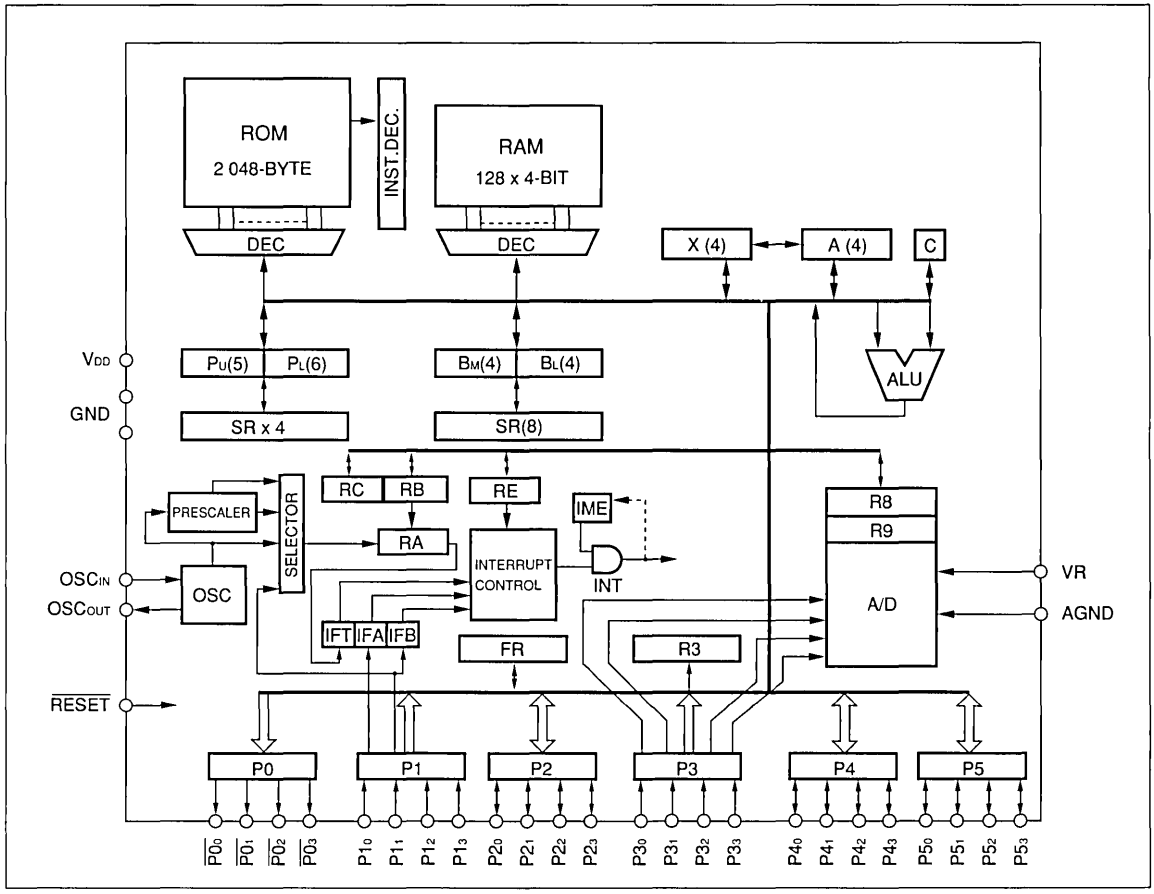
24-PIN SSOP



36-PIN QFP



BLOCK DIAGRAM



Nomenclature

A	: A register	INT	: Interrupt control unit
A/D	: A/D converter unit	P0-P5	: Port register
ALU	: Arithmetic logic unit	P_U, P_L	: Program counter
B_M, B_L	: RAM address register	R8, R9, RC, RE, RF	: Mode register
C	: Carry flag	RA	: Count register
IFA, IFB, IFT	: Interrupt request flag	RB	: Modulo register
IME	: Interrupt Master enable flag	SB	: SB register
INST. DEC.	: Instruction decoder	SR	: Stack register

PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
$\overline{P0_0}$-$\overline{P0_3}$	O	High current output (sink current 15 mA)
$P1_0$-$P1_1$	I	Input (standby release) (counter input : $P1_1$) with pull-up resistor
$P1_2$-$P1_3$	I	Input (standby release) with pull-up resistor
$P2_0$-$P2_3$	I/O	Input or output (independent) with pull-up resistor
$P3_0$-$P3_3$	I	Input (also used as analog input) with pull-up resistor
$P4_0$-$P4_3$, $P5_0$-$P5_3$	I/O	Input and output with pull-up resistor
OSC_{IN}, OSC_{OUT}	I/O	Crystal pins
$\overline{RESET}$	I	Reset signal input with pull-up resistor
VR, AGND	I	A/D converter reference supply input port
V_{DD}, GND	I	Power supply, Ground

NOTE :

Pin numbers apply to the 36-pin QFP and 32-pin SOP. (In case of 30-pin SDIP, $P5_2$ pin does not exist. In case of 24-pin SSOP, $P1_2$, $P1_3$ $P3_3$, $P5_0$-$P5_3$ pins do not exist.)

ABSOLUTE MAXIMUM RATINGS

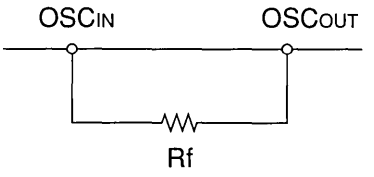
PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Maximum output current	I_{OH}	High-level output current (all outputs)	4	mA
	I_{OL0}	Low-level output current ($\overline{P0_0}$-$\overline{P0_3}$)	30	mA
	I_{OL1}	Low-level output current (all but $\overline{P0_0}$-$\overline{P0_3}$)	4	mA
Total output current	ΣI_{OH}	High-level output current (all outputs)	20	mA
	ΣI_{OL}	Low-level output current (all outputs)	80	mA
Operating temperature	T_{OPR}		−20 to +85	°C
Storage temperature	T_{STG}		−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.7 to 5.5	V
Instruction cycle	T_{SYS}	V_{DD} = 2.7 to 5.5 V	2 to 5	µs
		V_{DD} = 5.0 V ± 10%	1 to 5	
Main clock frequency * (OSC_{IN} - OSC_{OUT})	fosc	V_{DD} = 2.7 to 5.5 V	1 M to 400 k	Hz
		V_{DD} = 5.0 V ± 10%	2 M to 400 k	

* Degree of fluctuation frequency : ± 20%

OSCILLATION CIRCUIT



Rf = 33kΩ
(fosc = 1.67 MHz, TYP.)

NOTES :

- The typical oscillation frequency shall be determined in consideration of operating condition and fluctuation frequency.
- Mount Rf as close as possible to the oscillator pins of the LSI, in order to reduce an influence from floating capacitance.
- Since the value of resistor Rf varies depending on circuit pattern and others, the final Rf value shall be determined on the actual unit.
- Don't connect any line to OSC_{IN} and OSC_{OUT} except oscillator circuit.
- Don't put any signal line across the oscillator circuit line.
- On the multilayer circuit, do not let the oscillator circuit wiring cross other circuit.
- Minimize the wiring capacitance of GND and V_{DD} wiring.

DC CHARACTERISTICS

(V_{DD} = 2.7 to 5.5 V, Ta = –20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.7 to 3.3 V	1.0	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	15	70	250		
	I_{IH1}	V_{IN} = V_{DD}				3.0		
	I_{IL2}	V_{IN} = 0 V			1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1.0	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.7 to 3.3 V	3	15		mA	5
			V_{DD} = 4.5 to 5.5 V	12	25			
	I_{OH1}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.7 to 3.3 V	0.2	1.5			
			V_{DD} = 4.5 to 5.5 V	0.8	2.2			
	I_{OL2}	V_O = 1.5 V	V_{DD} = 4.5 to 5.5 V	4.0	9.0		mA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.7 to 3.3 V	0.2	2.0			
			V_{DD} = 4.5 to 5.5 V	0.8	2.4			
	I_{OH3}	V_{OH} = V_{DD} – 1.0 V	V_{DD} = 4.5 to 5.5 V	0.5			mA	7
Supply current	I_{DD}	f_{OSC} = 2.0 MHz	V_{DD} = 4.5 to 5.5 V		1 200	2 800	µA	8
		f_{OSC} = 1.0 MHz	V_{DD} = 2.7 to 3.3 V		300	900		
			V_{DD} = 4.5 to 5.5 V		600	1 400		
	I_{HLT}	f_{OSC} = 2.0 MHz	V_{DD} = 4.5 to 5.5 V		760	1 700		
		f_{OSC} = 1.0 MHz	V_{DD} = 4.5 to 5.5 V		400	1 000		
	I_{STOP}	V_{DD} = 2.7 to 5.5 V				5		
	I_{VR}	A/D conversion in operation	V_{DD} = 2.7 to 3.3 V		130	350	µA	9
			V_{DD} = 4.5 to 5.5 V		220	500		
		A/D conversion in stop	V_{DD} = 2.7 to 5.5 V			3	µA	10
A/D conversion	Resolution				10		bit	
	Differential error	f_{OSC} = 1.0 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Sequential error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		
Reference clock oscillator frequency	f_{OSC}	V_{DD} = 4.5 to 5.5 V, Rf = 33 kΩ		1.34	1.67	2.0	MHz	

NOTES :

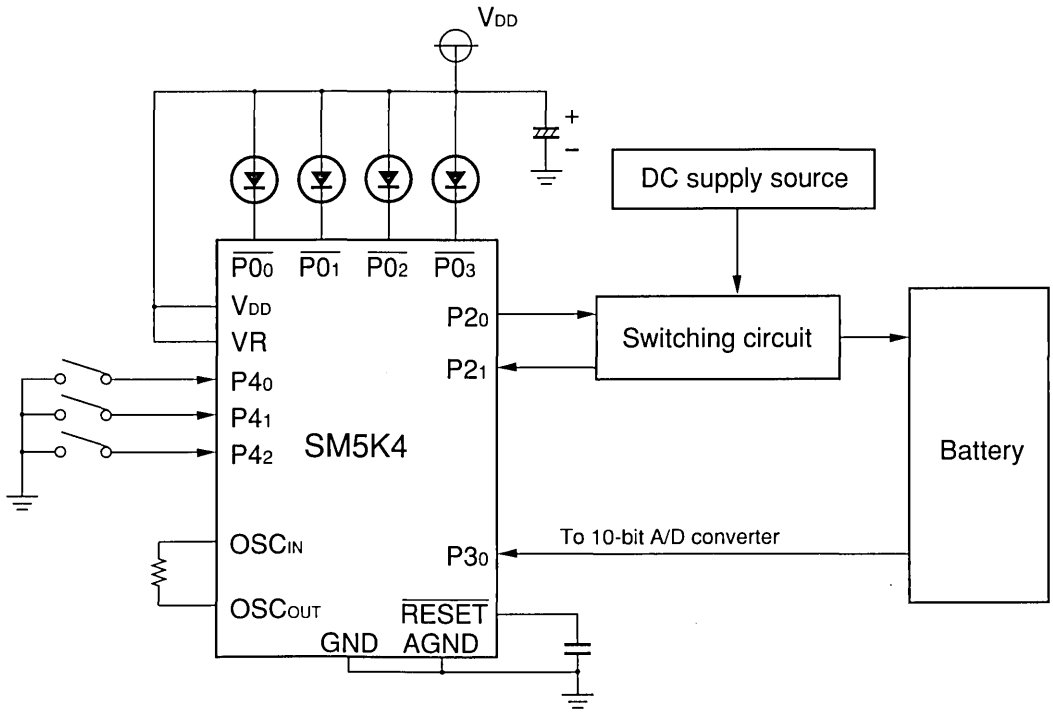
1. Applicable pins : $P1_2$, $P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_0$-$P4_3$, $P5_0$-$P5_3$*1
2. Applicable pins : $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$
3. Applicable pins : $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P3_0$-$P3_3$ (digital input mode)*1
4. Applicable pins : $P3_0$-$P3_3$ (analog input mode)
5. Applicable pins : $\overline{P0_0}$-$\overline{P0_3}$ (large current output)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode)*1
7. Applicable pins : $P3_0$-$P3_3$*2
8. No-load condition (A/D conversion in stop)
9. A/D conversion in operation (A/D conversion enable)
10. A/D conversion in stop (A/D conversion disable)

*1 In case of 36-pin QFP and 32-pin SOP.
(In case of 30-pin SDIP, $P5_2$ pin dose not exist. In case of 24-pin SSOP, $P1_2$, $P1_3$, $P3_3$, $P5_0$-$P5_3$ pins do not exist.)

*2 P3 ports are normally used for input port with pull-up resistor. These ports can be also used as a suspected case of output port.

SYSTEM CONFIGURATION EXAMPLE

• Charger controller



SM5K5

4-Bit Single-Chip Microcomputer (Controller With 10-Bit A/D Converter)

DESCRIPTION

The SM5K5 is a CMOS 4-bit single-chip micro computer incorporating 4-bit parallel processing function, ROM, RAM, 10-bit A/D converter and timer/counters.

It provides three kinds of interrupts and 4 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package : best suitable for Low power controlling, compact equipment like a precision charger.

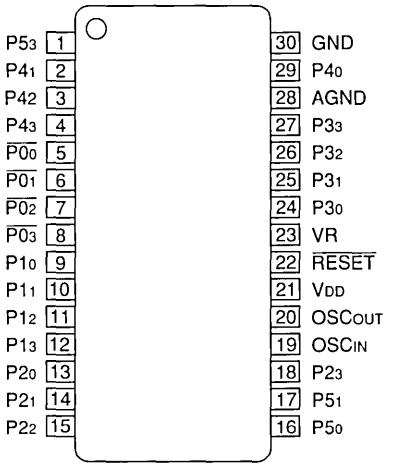
FEATURES

- ROM capacity : 2 048 x 4 bits
- RAM capacity : 128 x 4 bits
- Instruction sets : 50
- Subroutine nesting : 4 levels
- I/O port :
  - Input 8
  - Output 4
  - Input/output 12 (36QFP/32SOP)
    11 (30SDIP)
    8 (28SOP)
- Interrupts :
  - Internal interrupt x 1 (timer)
  - External interrupt x 2 (2 external interrupt inputs)
- A/D converter :
  - Resolution 10 bits
  - Channels 4
- Timer/counter : 8 bits x 1
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Instruction cycle time :
  - 1 µs (MIN.) (2 MHz, at 5 V ± 10%)
  - 2 µs (MIN.) (1 MHz, at 2.2 to 5.5 V)
- Large current output pins (LED direct drive) : 4
- Supply voltage : 2.2 to 5.5 V
- Packages :
  - 30-pin SDIP (SDIP030-P-0400)
  - 28-pin SOP (SOP028-P-0450)
  - 32-pin SOP (SOP032-P-0525)
  - 36-pin QFP (QFP036-P-1010)

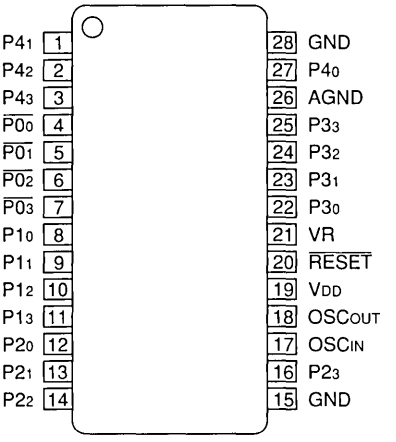
PIN CONNECTIONS

TOP VIEW

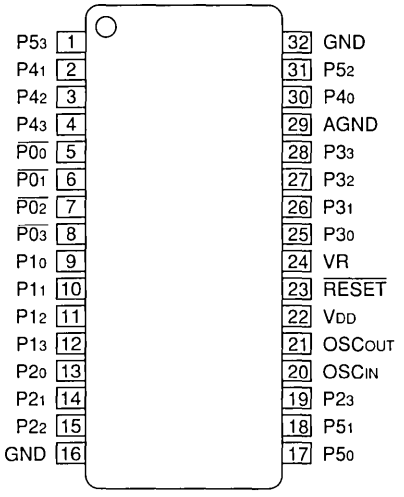
30-PIN SDIP



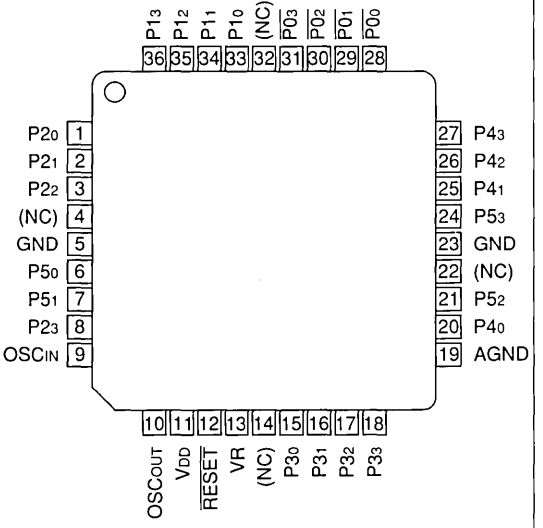
28-PIN SOP



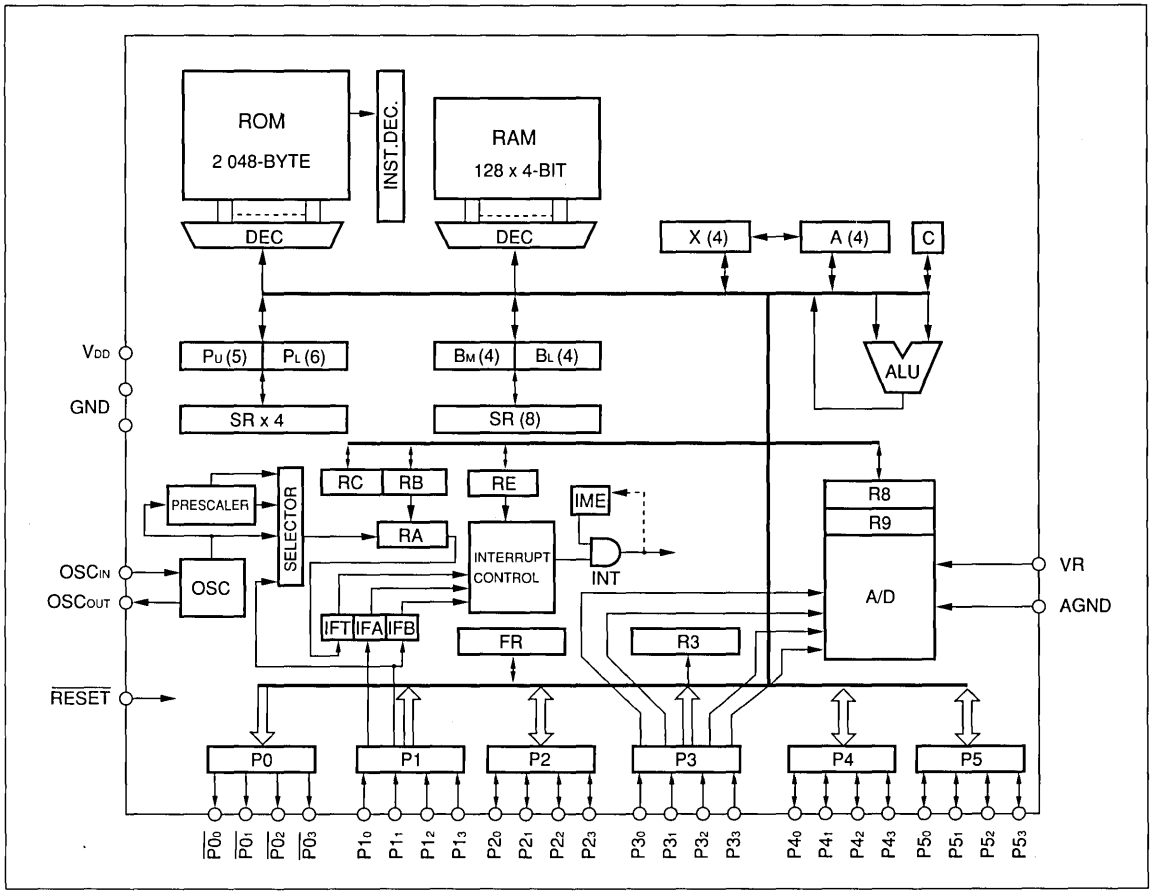
32-PIN SOP



36-PIN QFP



BLOCK DIAGRAM



Nomenclature

A	: A register
A/D	: A/D converter unit
ALU	: Arithmetic logic unit
B_M, B_L	: RAM address register
C	: Carry flag
IFA, IFB, IFT	: Interrupt request flag
IME	: Interrupt master enable flag
INST. DEC.	: Instruction decoder
INT	: Interrupt control unit
P0-P5	: Port register
P_U, P_L	: Program counter
R8, R9, RC, RE, RF	: Mode register
RA	: Count register
RB	: Modulo register
SB	: SB register
SR	: Stack register

PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
$\overline{P0_0}$-$\overline{P0_3}$	O	High current output (sink current 15 mA)
$P1_0$-$P1_1$	I	Input (standby release) (counter input : $P1_1$)
$P1_2$-$P1_3$	I	Input (standby release)
$P2_0$-$P2_3$	I/O	Input or output (independent)
$P3_0$-$P3_3$	I	Input (also used as analog input)
$P4_0$-$P4_3$, $P5_0$-$P5_3$	I/O	Input and output
OSC_{IN}, OSC_{OUT}	I/O	Crystal pins
$\overline{RESET}$	I	Reset signal input
VR, AGND	I	A/D converter reference supply input port
V_{DD}, GND	I	Power supply, Ground

NOTE :

Symbols apply to 32-pin SOP and 36-pin QFP. (In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$-$P5_3$ do not exist.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Maximum output current	I_{OH}	High-level output current (all outputs)	4	mA
	I_{OL0}	Low-level output current ($\overline{P0_0}$-$\overline{P0_3}$)	30	mA
	I_{OL1}	Low-level output current (all but $\overline{P0_0}$-$\overline{P0_3}$)	4	mA
Total output current	ΣI_{OH}	High-level output current (all outputs)	20	mA
	ΣI_{OL}	Low-level output current (all outputs)	80	mA
Operating temperature	T_{OPR}		−20 to +70	°C
Storage temperature	T_{STG}		−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.2 to 5.5	V
Instruction cycle	T_{SYS}	V_{DD} = 2.2 to 5.5 V	2 to 61	μs
		V_{DD} = 5.0 V ± 10%	1 to 61	
Main clock frequency (OSC_{IN}-OSC_{OUT})	f_{OSC}	V_{DD} = 2.2 to 5.5 V	1 M to 32.768 k	Hz
		V_{DD} = 5.0 V ± 10%	2 M to 32.768 k	

DC CHARACTERISTICS

(Ta = –20 to +70°C, Typ. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.2 to 3.3 V	2	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	25	70	250		
	I_{IH1}	V_{IN} = V_{DD}				2		
	I_{IL2}	V_{IN} = 0 V			1	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.2 to 3.3 V	5	15		mA	5
			V_{DD} = 4.5 to 5.5 V	15	25			
	I_{OH1}	V_O = V_{DD}–0.5 V	V_{DD} = 2.2 to 3.3 V	0.3	1.5			
			V_{DD} = 4.5 to 5.5 V	1.0	2.2			
	I_{OL2}	V_O = 0.5 V	V_{DD} = 2.2 to 3.3 V	7	35		µA	6
			V_{DD} = 4.5 to 5.5 V	20	60			
	I_{OH2}	V_O = V_{DD}–0.5 V	V_{DD} = 2.2 to 3.3 V	300	2 000			
			V_{DD} = 4.5 to 5.5 V	1 000	2 400			
Supply current	I_{DD}	f_{OSC} = 2 MHz	V_{DD} = 4.5 to 5.5 V		1 200	2 500	µA	7
		f_{OSC} = 1 MHz	V_{DD} = 2.2 to 3.3 V		300	800		
			V_{DD} = 4.5 to 5.5 V		600	1 200		
		f_{OSC} = 32.768 kHz	V_{DD} = 2.2 to 3.3 V		20	120		
			V_{DD} = 4.5 to 5.5 V		40	160		
	I_{HLT}	f_{OSC} = 2 MHz	V_{DD} = 4.5 to 5.5 V		760	1 500	µA	7
		f_{OSC} = 1 MHz	V_{DD} = 4.5 to 5.5 V		400	900		
		f_{OSC} = 32.768 kHz	V_{DD} = 2.2 to 3.3 V		15	60		
			V_{DD} = 4.5 to 5.5 V		20	90		
	I_{STOP}	Ceramic osc.	V_{DD} = 2.2 to 3.3 V			2		
		Crystal osc. (at 32.768 kHz)	V_{DD} = 2.2 to 3.3 V		2	10		
			V_{DD} = 4.5 to 5.5 V		10	25		
	I_{VR}	A/D in operation	V_{DD} = 2.2 to 3.3 V		130	300	µA	8
			V_{DD} = 4.5 to 5.5 V		220	450		
		A/D in stop	V_{DD} = 2.2 to 5.5 V			2	µA	9
A/D conversion	Resolution				10		bit	
	Differential linearity error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Linearity error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		

NOTES :

1. Applicable pins : $P1_2$, $P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_0$-$P4_3$, $P5_0$-$P5_3$*1
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, $P1_0$, $P1_1$
3. Applicable pins : $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (digital input mode)*1
4. Applicable pins : $P3_0$-$P3_3$ (analog input mode)
5. Applicable pins : $\overline{P0_0}$-$\overline{P0_3}$, (High current port)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (during output mode)*1
7. No load (A/D conversion in stop) MAX. value V_{DD} = 5.5 V (or 3.3 V), T_{OPR} = –20°C
8. A/D conversion in operation (operation enable)
9. A/D conversion in stop (operation disable)

*1 In case of 32-pin SOP and 36-pin QFP.
(In case of 30-pin SDIP, $P5_2$ dose not exist. In case of 28-pin SOP, $P5_0$-$P5_3$ do not exist.)

SYSTEM CONFIGURATION

A Register and X Register

The A register (or accumulator (ACC)) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM, to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register. When the table reference instruction PAT is used, the X and A registers load ROM data. A pair of A and X registers can accommodate 8-bit data.

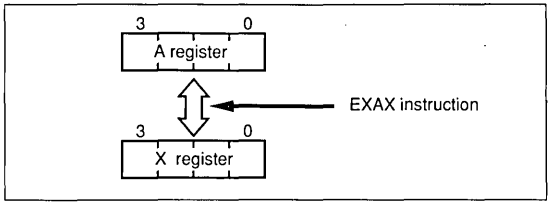


Fig. 1 Data Transfer Example between A Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation

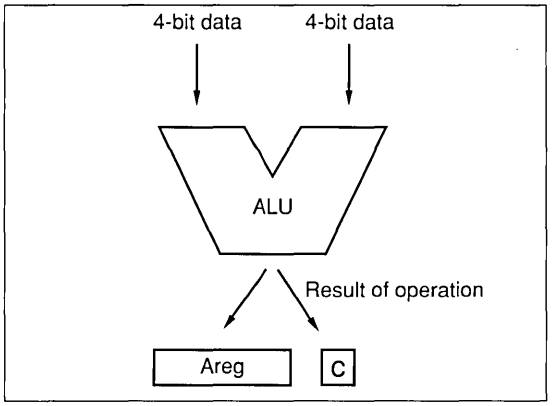


Fig. 2 ALU

The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy : ADC instruction sets/clears the content of the C flag; ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

B Register and SB Register

• B register (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address. The upper 4-bit section is called B_M register and lower 4-bit B_L.

• SB register

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

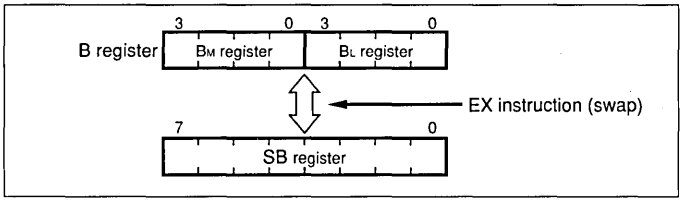


Fig. 3 B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used to store data up to 4 x 16 x 8 = 512 bits.

Word (0-FH)

BM \ BL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																※

File (0-7)

※ 1 word = 4-bit

Fig. 4 RAM File and Word

Program Counter PC and Stack Register SR

The program counter PC specifies the ROM address. The PC consists of 12-bit as shown in Fig. 5 : The upper 6-bit (P_U) represents a page while the lower 6-bit (P_L) denotes a step. The P_U section is a register and the P_L section, a binary counter.

Execution of interrupt handling and the table reference instruction PAT also automatically uses 1 stage of the stack register SR.

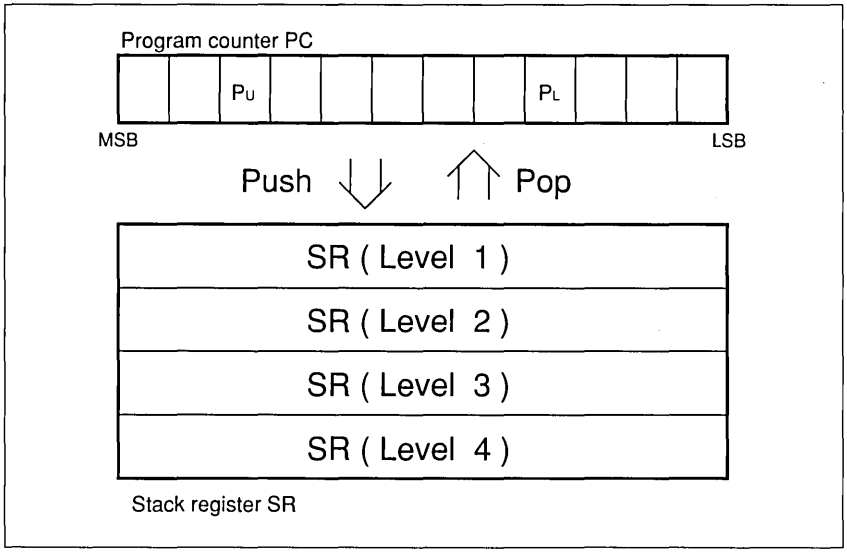


Fig. 5 Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used to store the program. The capacity of the ROM is 2 048-step (32-page by 64-step. See Fig. 6). The configuration of the ROM and program jumps are illustrated in Fig. 7.

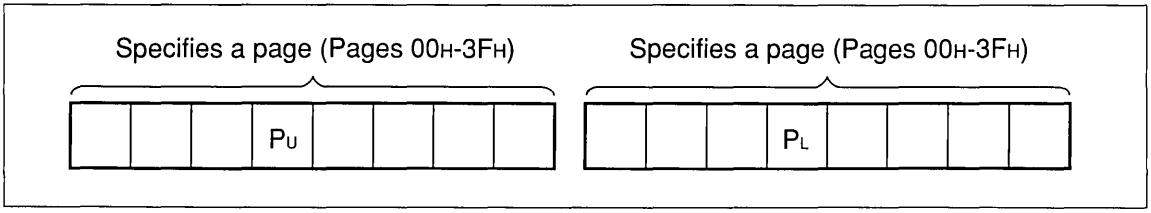
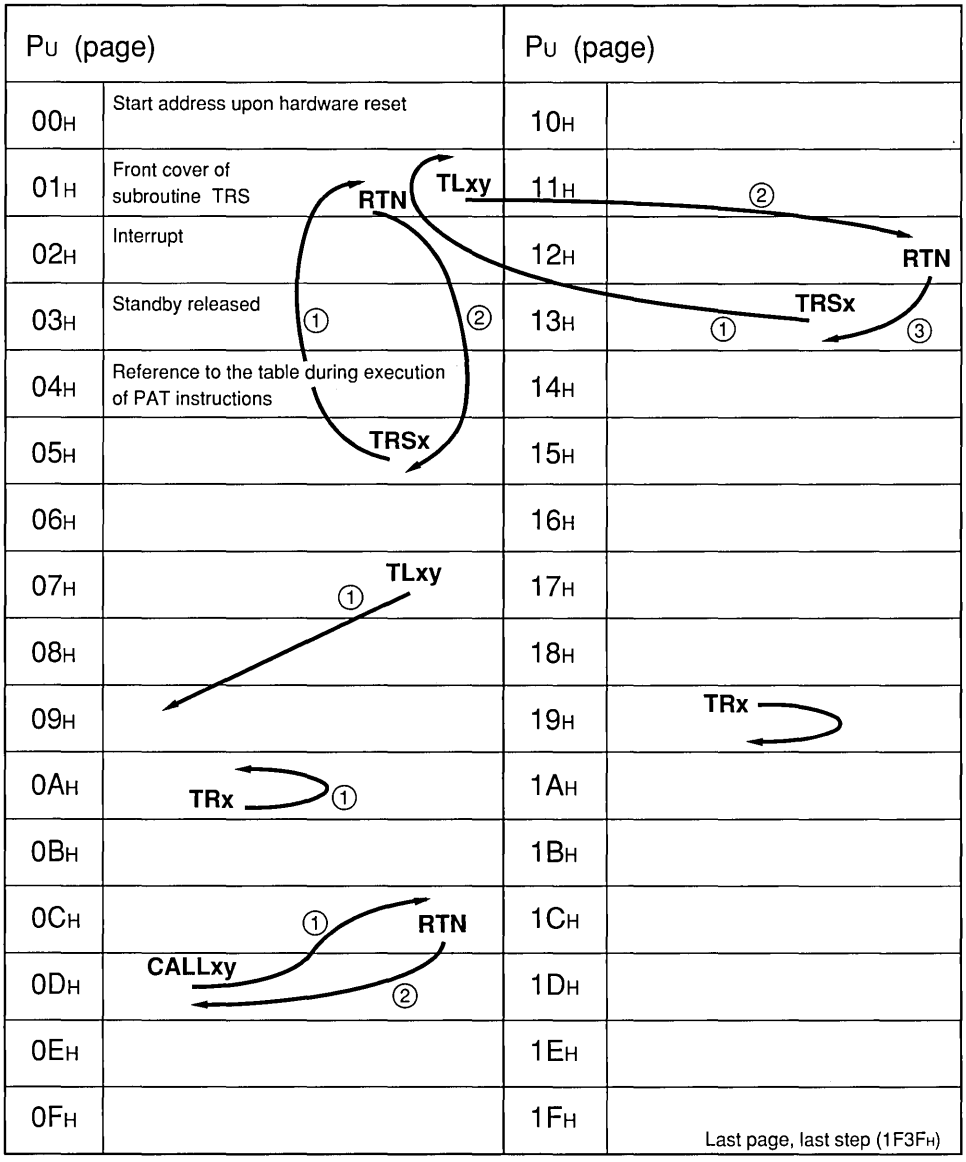


Fig. 6 Page and Step for ROM



Number in a circle is a step number in the program jump.

Fig. 7 ROM Configuration and Program Jump Example

Output Latch Register and Mode Register

The SM5K5 contains 6 output latch registers and 8 mode registers which either latch contents of output ports or control some functions of the SM5K5.

Theses registers, their functions and available transfer instructions are shown in Table 1 below.

Table 1 Output Latch Registers and Mode Registers

SYMBOL	FUNCTION	OUT	INL	OUT	IN/TPB	ANP/ORP	CONTENT OF B_L
P0	Output register	O	–	O	–	O	0
P1	Input register	–	O	–	O	–	1
P2	I/O register (independent)	–	–	O	O	O	2
P3	Input register (and analog input)	–	–	–	O	–	3
R3	Control register	–	–	O	–	–	3
P4	I/O register	–	–	O	O	O	4
P5	I/O register	–	–	O	O	O	5
R8*	A/D data/control register	–	–	O	O	–	8
R9*	A/D data register	–	–	O	O	–	9
RA*	Timer/counter register	–	–	O	O	–	A
RB*	Timer/modulo register	–	–	O	O	–	B
RC	Timer control register	–	–	O	O	–	C
RE	Interrupt mask register	–	–	O	O	–	E
RF	P2 directional register	–	–	O	O	–	F

* 8-bit register

NOTE :

Bit 4 (R84) in the R8 register is read only.
(Read or write operation of this bit does not affect any other operation.)

OUTPUT LATCH REGISTER

An output latch register sets the output level of the pin to which it is connected.

FUNCTIONAL DESCRIPTION

Hardware Reset Function

Reset function initializes the SM5K5 system.

When the input on the $\overline{\text{RESET}}$ pin goes Low, the system enters reset condition after 2 command cycles. After the $\overline{\text{RESET}}$ pin goes High level, the reset condition is removed as the input pulse from OSC_{IN} pin repeats 2^{15} times, forcing the program counter to start at 0 page and 0 address.

Initialized status of the system immediately after resetting is shown below.

Table 2 Status of Flags and Registers Immediately after Reset

FLAG REGISTER	STATUS	FLAG REGISTER	STATUS
PC	0	IFA flag	0
SP	Level 1	IFB flag	0
RAM	Undefined	IFT flag	0
Register A	Undefined	IME flag	0
Register X	Undefined	C flag	Undefined
P0, P2, P4, P5 output latch register	0	B_M, B_L registers	Undefined
Timers (RA, RB), divider	0	R3, R8*, R9, RC, RE, RF	0

* The content of the bit R84 is undefined because it is read only.

Reset causes the following changes.

1) I/O pins are set to input pins.
2) All mode registers are reset.
3) Output latch register P0 is reset, causing $\overline{P0_0}$ to $\overline{P0_3}$ pins go High level.
4) Interrupt request flags (IFA, IFB, and IFT), interrupt master enable flag (IME) are reset, disabling all interrupts.

Standby Feature

The standby function saves power by stopping the program whenever it is not necessary to run. The mode in which the microcomputer is executing the program is called the run mode and the mode in which it stops the program is called the standby mode. Standby mode is further divided into two modes : stop mode and halt mode, one of which is selected by halt instruction or stop instruction. Upon removal of standby condition, the SM5K5 returns from the standby mode to the normal run mode. To enter the standby mode, select either stop mode or halt mode whichever appropriate (Fig. 8).

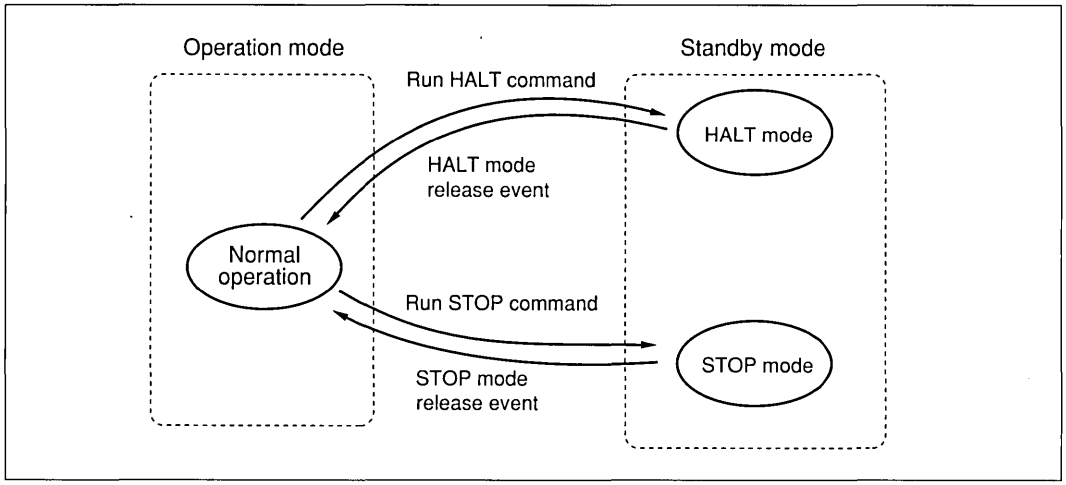


Fig. 8 Operation Shift of Program

• Blocks stopped during standby mode

In the halt mode

The system clock generating circuit stops during the halt mode, deactivating all the blocks driven by the system clock. The main clock and dividers remain active. This means that timers can be used while in the halt mode. Both internal and external clocks can be used as the count clock.

In the stop mode

The main clock and system clock stop upon entering the stop mode. Therefore, only timers using the external clock remain active.

• Counters that the system retains during standby mode

The contents that will be retained in the halt mode will also be retained in the stop mode. These items are shown in Table 3.

Table 3 System Contents Secured During Standby Mode

FLAG	REGISTER	OUTPUT LATCH REGISTER/MODE REGISTER	OTHER
IFA flag	A register	P0, P2, R3, P5	RAM
IFB flag	X register	R8, R9, RA, RB	
IFT flag	B_M, B_L register	RC, RE, RF	
IME flag	SP		
C flag	SR		

• Releasing events of standby mode (6-type)

RELEASING EVENT	FLAG	INT/EXT	MASKABLE / NONMASKABLE	PRIORITY
Reset input	–	External	Nonmaskable	–
Low level input on $P1_0$ pin	IFA	External	Maskable	1
Low level input on $P1_1$ pin	IFB	External	Maskable	2
Low level input on $P1_2$ pin	–	External	Nonmaskable	–
Low level input on $P1_3$ pin	–	External	Nonmaskable	–
Timer overflow	IFT	Internal	Maskable	3

• Usage of halt mode and stop mode

The system returns back to the normal operation mode upon occurring of a standby mode releasing condition. The halt mode should be used when the system must enter and exit normal operation frequently as in the case of key operation.

The halt mode should also be used to keep timers that are operating from the internal clock, while in the standby mode.

The stop mode further saves power than the halt mode but requires slightly longer time to return to the normal mode. Therefore, the stop mode should be used when the system will not be required to return to the normal mode in a short time.

Interrupt Feature

The interrupt block consists of mask flags (bits RE0, RE1, and RE2), IME flag and interrupt request handling circuit. Fig. 9 shows the configuration of the interrupt block.

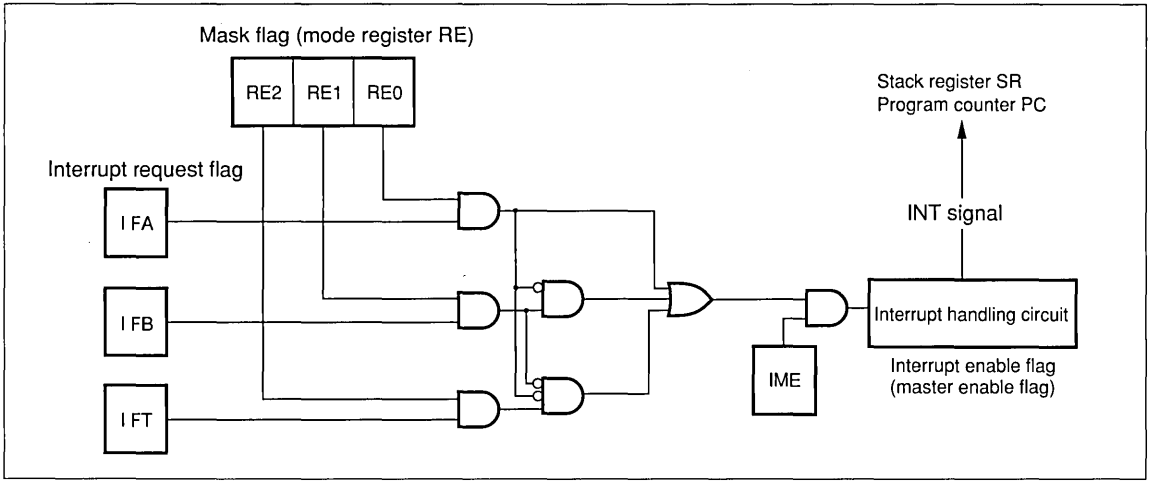


Fig. 9 Interrupt Block Diagram

• Interrupt used with SM5K5

Interrupt event occurs on the falling edge of $P1_0$ or $P1_1$ pin input, or the overflow at the timer. Theses events set flags IFA, IFB, and IFT, respectively, that then serve as interrupt request flag.

Table 4 shows interrupt handling priority level and jump address.

Table 4 Interrupt Event Summary

INTERRUPT EVENT (REQUEST FLAG)	JUMP ADDRESS		PRIORITY ORDER	INTERRUPT MASK FLAG
	PAGE	STEP		
Falling edge of input on $P1_0$ (IFA)	2	0	1	RE_0
Falling edge of input on $P1_1$ (IFB)	2	2	2	RE_1
Timer overflow (IFT)	2	4	3	RE_2

• IME flag (master enable flag)

The IME enables or disables all interrupts at the same time. The IE command, when executed, sets the IME flag and enables the interrupt specified by the mask flag setting. The ID command resets the IME flag, disabling process of any interrupt request. Setting the IME flag to reset after releasing hardware reset, all interrupts are inhibited.

• Mode register RE (interrupt mask flag)

The mode register RE (RE_0, RE_1, RE_2, interrupt mask flag) individually enables or disables three type of interrupts.

Timer/Counter

The SM5K5 has a pair of built-in timer/counter. The timer/counter are used to handle periodic interrupts and to count. The overflowing timer can be used to disable the halt mode. The timer/counter serve as interval timer.

The timer/counter consists of an 8-bit count register RA, modulo register RB (for counter initial value setting), 15-bit divider and 4-bit mode register RC (for count clock selection). The configuration of the timer/counter is shown in Fig. 10.

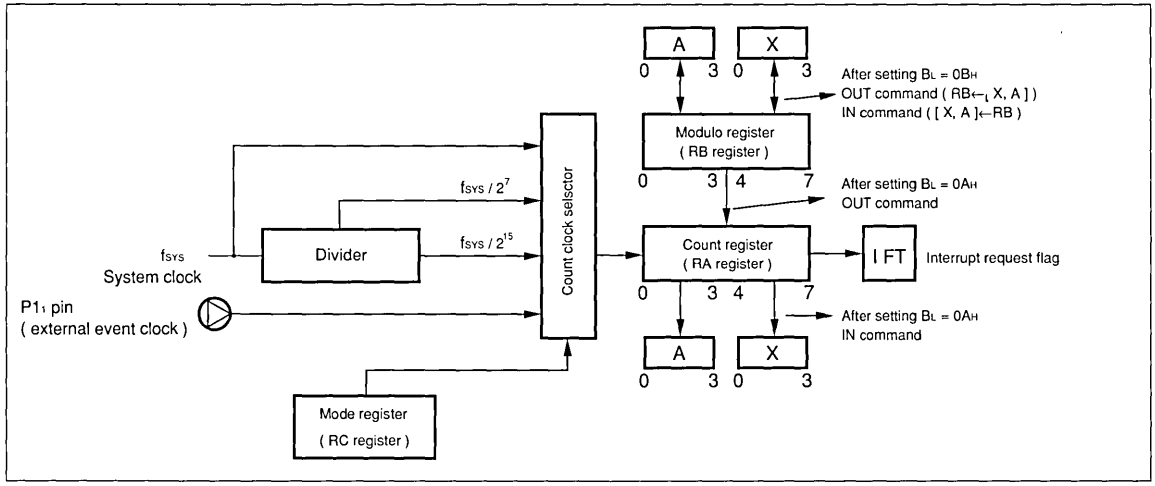


Fig. 10 Configuration of Timer/Counter

• Selecting count clock

A count clock is selected by the bit settings in the mode register RC.

Table 5 Count Clock Selection

LOWER 2-BIT OF RC BITS		SELECTED COUNT CLOCK
1	0	
0	0	f_{SYS} (system clock)
0	1	$f_{SYS}/2^7$
1	0	$f_{SYS}/2^{15}$
1	1	External event clock ($P1_1$)

A/D Conversion

The SM5K5 is provided with a built-in 10-bit A/D converter having 4-channel multiplexer analog inputs. The A/D converter operates in A/D conversion mode and comparison mode. In the A/D conversion mode, the converter converts the analog input from the P3 pin to the digital value; and in the comparison mode, it compares the input analog amplitude with that of a reference voltage set inside the SM5K5. The $P3_0$ to $P3_3$ pins can be used as analog voltage inputs. One or more of these 4 inputs can be set to assume A/D pin by the bit operation of the mode register R3. One of these A/D pins is further set as analog input by the bit operation of the mode register R8. The A/D converter is controlled by the bits set in the mode register R8. For details of the mode register R8, refer to MODE REGISTER R8. Configuration of the A/D converter is illustrated in Fig. 11.

CAUTIONS

- Keep the A/D converter reference voltage on the VR pin equal to or below V_{DD}.
- Do not apply the voltage to the VR pin before V_{DD} is applied.
- Connect AGND to GND.

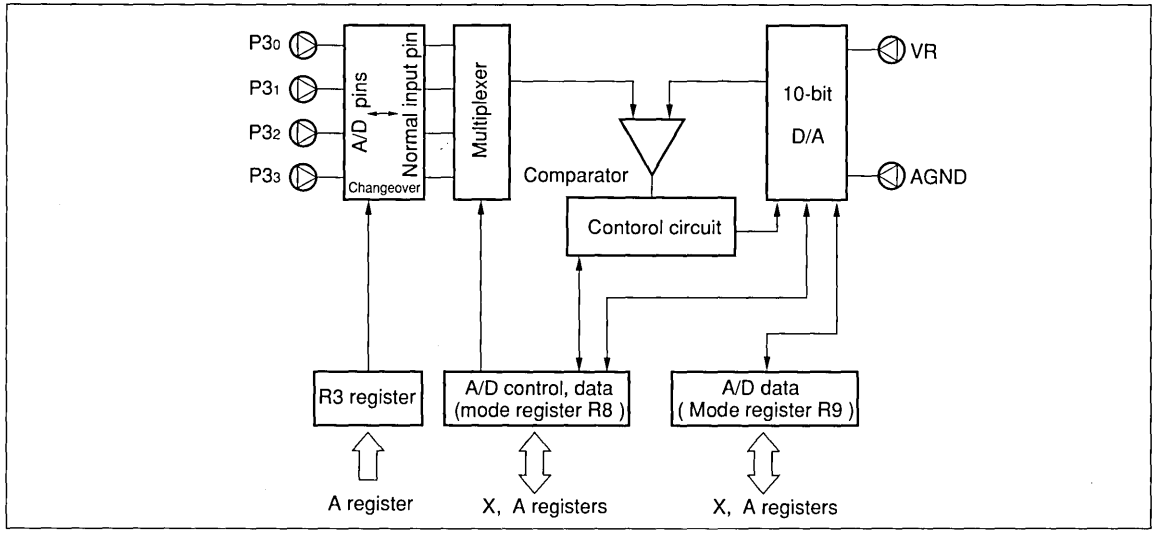


Fig. 11 A/D Converter Block Diagram

A/D CONVERSION MODE

In the A/D conversion mode, the converter converts the analog input voltage to the digital value. The analog input voltage is successively compared with the internal voltage charged on the weighted capacitor array until its digital equivalent is determined. The resultant digital data is stored into the mode registers R8 and R9.

The conversion requires 152.5 µs (main clock at 400 kHz/system clock at 5 µs) or 1.86 ms (main clock at 32.768 kHz/system clock at 61 µs).

COMPARISON MODE

In the comparison mode, the analog voltage from one of $P3_0$ to $P3_3$ pins is compared, in amplitude, with internally generated voltage whose value is set by the mode registers R8 and R9. The result data of the comparison is saved into the bit 4 (bit R84) position of the mode register R8. The comparison cycle lasts 62.5 µs (main clock at 400 kHz, system clock at 5 µs) or 763 µs (main clock at 32.768 kHz/system clock at 61 µs).

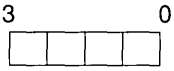
MODE REGISTERS

The registers which control functions of the SM5K5 and which serve as counter/timer are commonly referred to as "mode registers". In the SM5K5, R8 to RB are 8-bit mode registers; and R3, RC, RE and RF are 4-bit mode registers.

To set data into the mode registers, the OUT command is used; and to check the contents of the mode registers IN command is used.

R3 (A/D pin selection register)

Any pin on 4-pin port P3 can be set to accommodate analog voltage (hereafter called A/D pin).



Bit i (i = 3 to 0)

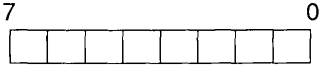
Set P3i pin to either general purpose input or A/D pin

0	(general purpose) input
1	A/D input

* Select one pin which is to be selected by mode register R8.

R8 (A/D conversion control & A/D data register)

An 8-bit register used to control A/D conversion and storing part of A/D conversion result. It also stores the results of comparison.



Bit 7, 6

Storage of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode)

- Use as part of a 10-bit data ragister in combination with mode register R9.
- Bit R86 is the LSB.
- Store lower 2-bit of converted data in A/D conversion mode.
- Use as lower 2-bit of internal voltage setting data in comparison mode.

Bit 5

* A/D operation enable/disable flag

0	Disable (A/D power source off)
1	Enable (A/D power source on)

Bit 4

Storage of comparison result (read only)

0	P3i pin voltage < internal setting voltage
1	P3i pin voltage > internal setting voltage

(i = 3 to 0)

Bit 3

* S/R flag (start/clear)

0	End of operation (or stop)
1	Start of operation (or in operation)

Bit 2

Operation mode selection

0	A/D conversion
1	Comparison

Bit 1, 0

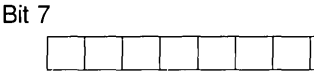
Select one of A/D pins as A/D conversion.

00	$P3_0$
01	$P3_1$
10	$P3_2$
11	$P3_3$

* When operation is end, these bits are cleared.

R9 (A/D data register)

The register to store the upper 8-bit of 10-bit data resulting from A/D conversion.



Bit i (i = 7 to 0)

Storage of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode)

- Use as part of a 10-bit data register in combination with mode register R8.
- Bit R97 is the MSB.
- Store upper 8-bit of A/D conversion result.
- Use as upper 8-bit of internal voltage setting data in comparison mode.

RA (Count register)

Bit 7 0

Bit i (i = 7 to 0)

Count clock input register

- Use as counter part of timer/counter (count clock input).
- Load the content of RB to RA when the RA overflows or when OUT command (B_L = $0A_H$) is executed.

  RA←RB
- Load the content of RA to X and A registers upon execution of IN command (B_L = $0A_H$).

  (X, A)←RA
- Bit 7 = MSB, bit 0 = LSB

RB (Modulo register)

Bit 7 0

Bit i (i = 7 to 0)

Count initial value storage register

- Use as modulo register of timer/counter
- Load the content of RB to X and A registers upon execution of

  IN command (B_L = $0B_H$) : X = upper bits, A = lower bits.

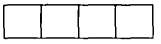
  (X, A)←RB
- Load the contents of X and A registers to RB upon execution of

  OUT command (B_L = $0B_H$) : X = upper bits, A = lower bits.

  RB←(X, A)
- Bit 7 : MSB, Bit 0 : LSB

RC (Timer control)

Bit 3 0



Bit 3

Start up count of the timer.

0	stop
1	start

Bit 2 (Unused)

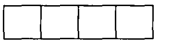
Bit 1, 0

Select the source clock to the timer.

00	f_{SYS} (system clock)
01	$f_{SYS}/2^7$
10	$f_{SYS}/2^{15}$
11	falling edge input on $P1_1$ pin

RE (Interrupt mask flag)

Bit 3 0



Bit 3 (Unused)

Bit 2

Remove overflow interrupt from timer or standby condition.

0	disable
1	enable

Bit 1

Interrupt on the falling edge of input from $P1_1$ pin, or release of standby mode by the Low input from $P1_1$ pin.

0	disable
1	enable

Bit 0

Interrupt on the falling edge of input on $P1_0$ pin, or release of standby mode by the Low input from $P1_0$ pin.

0	disable
1	enable

RF (P2 port direction register)

Bit 3 0

Bit i (i = 3 to 0)

Selection of input pin/output pin

0	Set P2i pin to input.
1	Set P2i pin to output.

I/O Ports

The SM5K5 has 24 ports : 8-input, 4-output and 12-I/O port. To verify the input, use suitable instruction to transfer the input on the pin directly to the A register. To select the output latch register to which the content of the A register is to be transferred, and to select the input port from which the signal or data is to be transferred to the A register, use the B_L register. For details of B_L settings and associated ports, refer to Table 1.

• Port $P0_0$ to $P0_3$ (CMOS inverting output port)
The data transfers in 4-bit string (use OUT or OUTL instruction) or in unit of 1-bit (use ANP or ORP instruction).

• Port $P1_0$ to $P1_3$ (input port with pull-up resistor)
The data transfers in unit of 4-bit. This port can be used as standby/external interrupt input or count pulse input. The P1 port can also be used as a standby release port without requiring specific setting on $P1_2$ and $P1_3$ pins. Pins $P1_0$ and $P1_1$ require settings through the mode resister RE. When using the P1 port as an external interrupt input, use pins $P1_0$ and $P1_1$ with suitable settings in the mode register RE. When using the P1 port as the count pulse input, use $P1_1$ pin.

• Port $P2_0$ to $P2_3$ (I/O port with pull-up resistor)
Each bit can be independently be set its direction and can be transferred independently or in combination of other 3-bit. The direction of the bits is determined by the RF register. After reset, the P2 port is set to input.

• Port $P3_0$ to $P3_3$ (input port with pull-up resistor)
The data transfers in unit of 4-bit. The port can also be used as A/D analog voltage input. To use the P3 port as the A/D port, set the mode register R3.

• Port $P4_0$ to $P4_3$ (I/O port with pull-up resistor)
The data transfers in unit of 4-bit.
When set to output, content of each bit can be set. Executing the input instruction (IN) sets the P4 ports ($P4_0$ to $P4_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P4 port is set to input.

• Port $P5_0$ to $P5_3$ (I/O port with pull-up resistor)
The data transfers in unit of 4-bit.
When set to output, content of each bit can be set. Executing the input instruction (IN) sets the P5 ports ($P5_0$ to $P5_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P5 port is set to input.

Flags

The SM5K5 has 4 flags (C flag and interrupt request flags [IFA, IFB, IFT]), which are used to perform setting and judgments.

System Clock Generator and Dividers

• System clock generator

The system clock is the divided-by-two main clock applied through OSC_{IN} and OSC_{OUT} (See Fig. 12). The system clock generator is shown in Fig. 13. One system clock cycle period is equal to one instruction execution time when the instruction consists of 1 word. When the ceramic oscillator runs at 400 kHz, the system clock fsys is 200 kHz. This means that the instruction execution time is 5 µs/word. Using a 32.768 kHz crystal oscillator generates 16.38 kHz fsys and the instruction execution time is 61 µs/word. The system clock can be used as count input pulse to the timer.

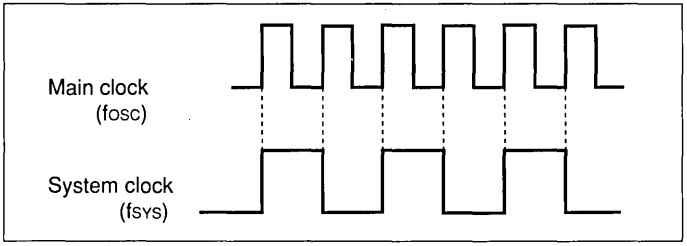


Fig. 12 Main Clock and System Clock

• Divider

The divider consists of 15 divided-by-two dividers, providing 2 ($f_{SYS}/2^7$, $f_{SYS}/2^{15}$) of 4 count clocks that are fed to the counter RA from the system clock. Its configuration is shown below. The divider can be clear by using the DR instruction.

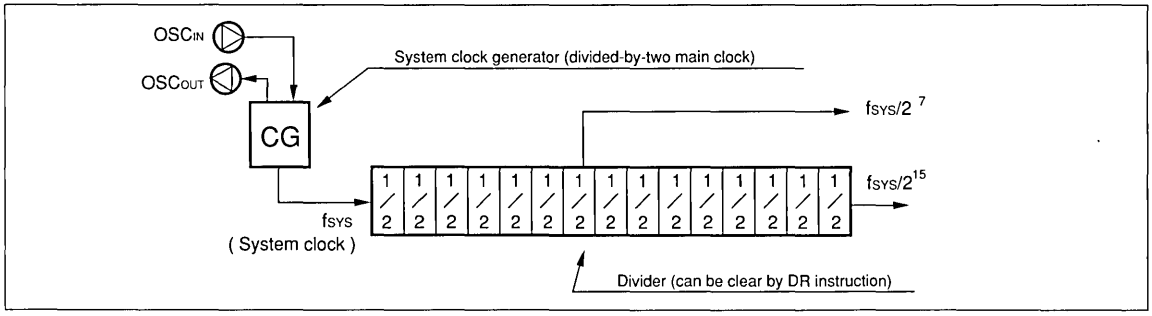


Fig. 13 System Clock Generator and Divider

• Oscillator mask option

Selection of type of oscillator, ceramic or crystal, is made by mask option.

INSTRUCTION SET

Definition of Symbols

M : Content of RAM at the address defined by the B register.

← : Transfer direction

∪ : Logical OR

∩ : Logical AND

⊕ : Exclusive OR

Ai : An i bit of A register (i = 3 to 0)

Push : Save the contents of PC to stack register SR.

Pop : Return the contents saved in the stack register back to PC.

Pj : Indicates output latch register or input register. Pj (j = 0, 1, 2, 3, 4, 5)

Rj : Mode register. Rj register (j = 3, A, B, C, E, F)

ROM ( ) : Content stored in ROM location defined by the value in ( ).

CY : Carry in ALU (independent of C flag) The CY(carry) is a signal which is generated when the ALU has been carried by the execution of a command. It is different from the C flag.

X : Used to represent a group of bits in the content of a register or memory. For example, the X in the LDAX instruction denotes the lower 2 digits (I_1 and I_0) of A register. For further information, see description of each instruction.

- A bit in a register is affixed to the register symbol, e.g. a bit (i = 0, 1, 2, 3....) of X register is expressed as Xi and P (R) register as P (R) i.
- Increment means binary addition of 1_H and decrement addition of F_H.
- Skipping (SKIP) of an instruction is ignorance of the instruction and no operation until the next instruction, regarding the instruction as NOP instruction. Skipping 1-word instruction requires 1-cycle, and 2-cycle for 2-word.

Instruction Summary (by function)

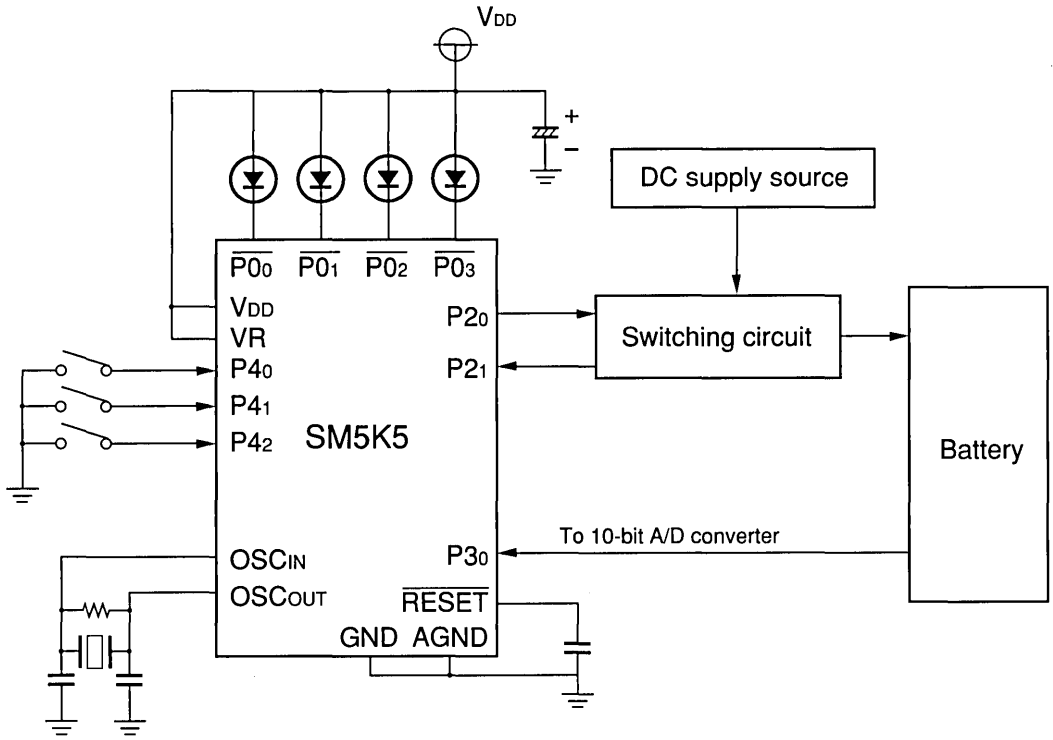
MNEMONIC	MACHINE CODE	OPERATION
ROM Addressing Instructions		
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy	E0 to E7, 00 to FF	$P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
TRS x	C0 to DF	Push, $P_U \leftarrow 01_H$, $P_L \leftarrow x$ (I_4, I_3, I_2, I_1, I_0)
CALL xy	F0 to F7 00 to FF	Push, $P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
RTN	7D	Pop
RTNS	7E	Pop, Skip the next step
RTNI	7F	Pop, IME←1
Data Load Instruction		
LAX x	10 to 1F	A←x (I_3-I_0)
LBMX x	30 to 3F	$B_M \leftarrow x$ (I_3-I_0)
LBLX x	20 to 2F	$B_L \leftarrow x$ (I_3-I_0)
LDA x	50 to 53	A←M, $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0)
EXC x	54 to 57	M↔A, $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0)
EXCI x	58 to 5B	M↔A, $B_L \leftarrow B_L+1$ $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0) Skip the next step, if result of B_L = 0
EXCD x	5C to 5F	M↔A, $B_L \leftarrow B_L-1$ $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0) Skip the next step, if result of B_L is = F_H
EXAX	64	A↔X-reg
ATX	65	X-reg←A
EXBM	66	B_M↔A
EXBL	67	B_L↔A
EX	68	B↔SB

MNEMONIC	MACHINE CODE	OPERATION
Arithmetic Instructions		
ADX x	00 to 0F	A←A+x (I_3-I_0) Skip the next step, if CY = 1
ADD	7A	A←A+M
ADC	7B	A←A+M+C, C←CY Skip the next step, if CY = 1
COMA	79	$A \leftarrow \overline{A}$
INCB	78	$B_L \leftarrow B_L+1$, Skip the next step, if result of B_L = 0
DECB	7C	$B_L \leftarrow B_L-1$, Skip the next step, if result of B_L = F_H
Test Instructions		
TAM	6F	Skip the next step, if A = M
TC x	6E	Skip the next step, if C = 1
TM	48 to 4B	Skip the next step, if Mi = 1, (i = 3 to 0)
TABL	6B	Skip the next step, if A = B_L
TPB x	4C to 4F	Skip the next step, if P (R) i = 1, (i = I_1, I_0)
TA	6C	Skip the next step, if IFA = 1 IFA←0
TB	6D	Skip the next step, if IFB = 1 IFB←0
TT	69 02	Skip the next step, if IFT = 1 IFT←0
Bit Operation Instructions		
SM x	44 to 47	Mi←1 (i = 3 to 0)
RM x	40 to 43	Mi←0 (i = 3 to 0)
SC	61	C←1
RC	60	C←0
IE	63	IME←1 (Interrupt enable)
ID	62	IME←0 (Interrupt disable)

MNEMONIC	MACHINE CODE	OPERATION
I/O Instructions		
INL	70	A←P1
OUTL	71	P0←A
ANP	72	Pj←Pj ∩ A (j = 0, 2, 4, 5)
ORP	73	Pj←Pj ∪ A (j = 0, 2, 4, 5)
IN	74	A←Pj (j = 1, 2, 3, 4, 5) X-reg, A←Rj (j = 8, 9, A, B) A←Rj (j = C, E, F)
OUT	75	Pj←A (j = 0, 2, 4, 5) Rj←X-reg, A (j = 8, 9, B) RA←RB Rj←A (j = 3, C, E, F)
Table Search Instructions		
PAT	6A	Push P_U←04_H, P_L←(X_1, X_0, A) X-reg←ROM_H, A←ROM_L Pop
Divider Operation Instructions		
DR	69 03	Divider (f_0-f_{15}) clear
Special Instructions		
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

• **Charger controller**



SM5K6

4-Bit Single-Chip Microcomputer (Controller With 10-Bit A/D Converter)

DESCRIPTION

The SM5K6 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, serial interface function, ROM, RAM, 10-bit A/D converter and timer/counters. It provides five kinds of interrupts and 8 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package : best suitable for low power controlling, compact equipment like a precision charger.

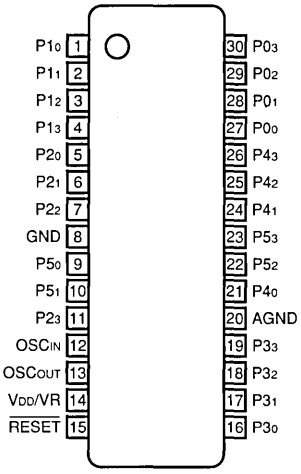
FEATURES

- ROM capacity : 4 096 x 8 bits
- RAM capacity : 256 x 4 bits
- Instruction sets : 52
- Subroutine nesting : 8 levels
- I/O port :
  - input 4
  - input/output 20
- Interrupts :
  - Internal interrupt x 3 (2 timers, 1 serial interface)
  - External interrupt x 2 (2 external interrupt inputs)
- A/D converter :
  - Resolution 10 bits
  - Inputs channels 8
- Timer/counter : 8 bits x 2
- Serial interface : 8 bits synchrounous x 1
- Watch dog timer : 8 bits x 1 (also used as timer 2)
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Instruction cycle time :
  - 1 µs (4 MHz, at 5 V ± 10%)
  - 4 µs (4 MHz, at 2.0 to 5.5 V)
- Large current output pins (LED direct drive) : 8
- Buzzer output
- Supply voltage : 2.0 to 5.5 V
- Packages :
  - 30-pin SDIP (SDIP030-P-0400)
  - 32-pin SOP (SOP032-P-0525)
  - 36-pin QFP (QFP036-P-1010)

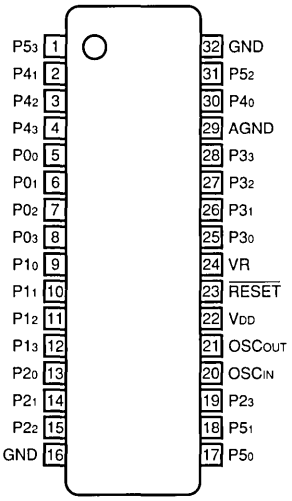
PIN CONNECTIONS

TOP VIEW

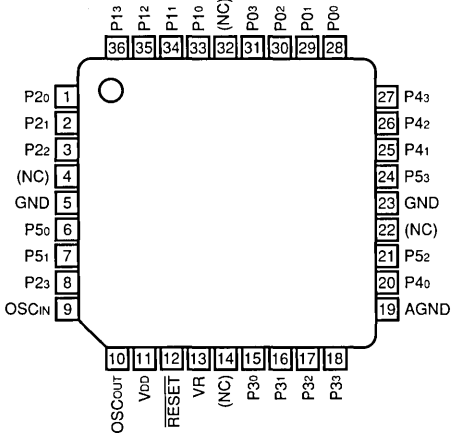
30-PIN SDIP



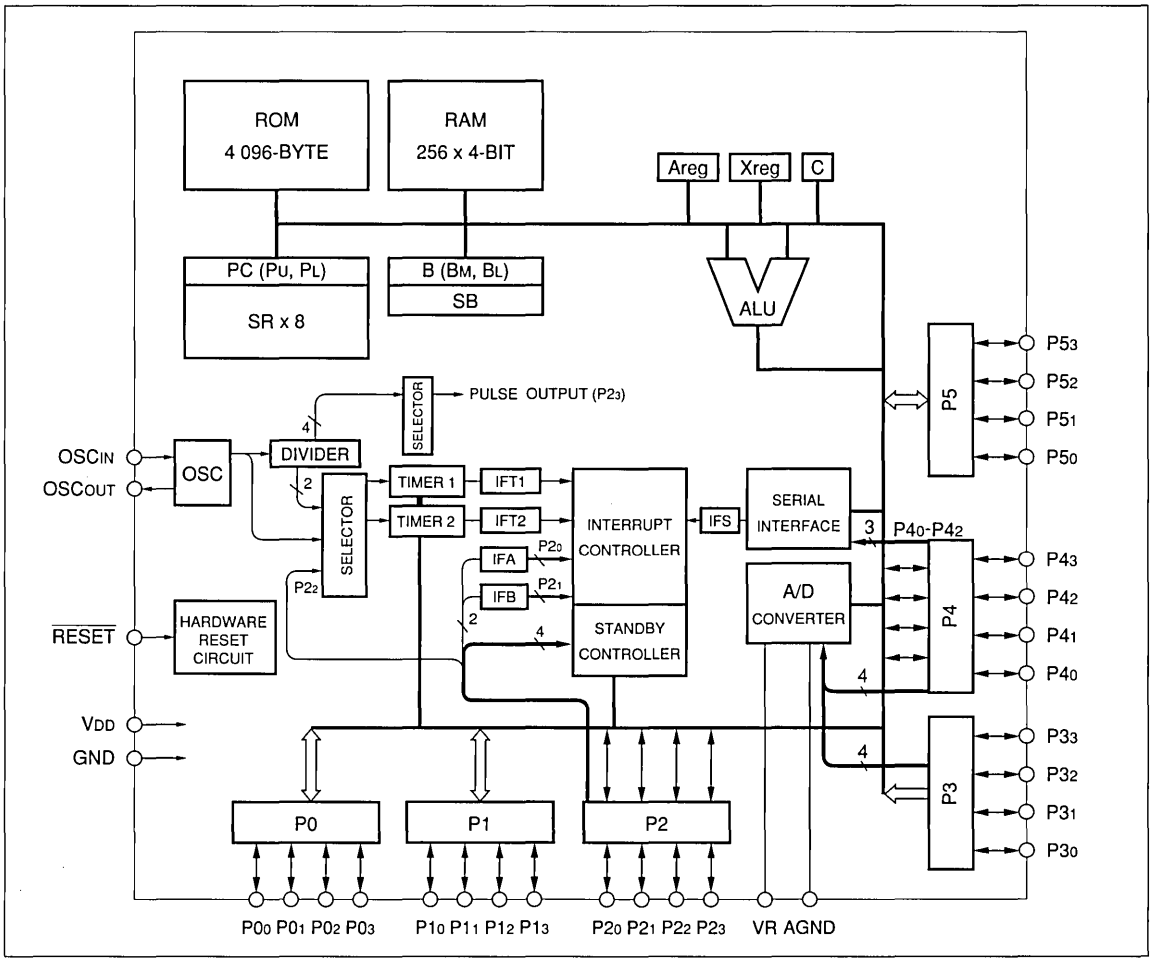
32-PIN SOP



36-PIN QFP



BLOCK DIAGRAM



Nomenclature

Areg	: A register (Accumulator)
ALU	: Arithmetic logic unit
B	: RAM address register
C	: Carry latch flag
IFA, IFB, IFS	: Interrupt request flag
IFT1, IFT2	
OSC	: System clock oscillator
P0, P1, P2	: I/O access
P3, P4, P5	
PC	: Program counter
RAM	: Data memory
ROM	: Program memory
SB	: SB register (Stack B-reg)
SR	: Stack register (Stack PC)
Xreg	: X register (Sub accumulator)

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$-$P0_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits. When set at output, each pin serves as a drive with a 15 mA (Typ.) current sinking capability.
$P1_0$-$P1_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits. When set at output, each pin serves as a drive with a 15mA (Typ.) current sinking capability
$P2_0$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes external interrupt input or standby release.
$P2_1$	I/O	Input or output (independent) : Direction of this pin can set independently. Assumes count clock input or standby release.
$P2_2$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes external interrupt input or standby release.
$P2_3$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes standby release or buzzer output (divider clock).
$P3_0$-$P3_3$	I	Parallel input : Accepts input in units of 4 bits. Also assumes A/D pins.
$P4_0$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO data input.
$P4_1$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO data output.
$P4_2$	I/O	Input or output (independent) : Direction of this pin can be set independently. Assumes A/D pin or SIO clock I/O.
$P4_3$	I/O	Input or output (independent) : Direction of this pin can be set independently. Also assumes A/D pin.
$P5_0$-$P5_3$	I/O	Parallel input/output : Direction of pins can be set in units of 4 bits.
$\overline{\text{RESET}}$	I	Hardware reset input : Input to this pin resets the microcomputer. For normal run, connect 0.1 µF (Typ.) across $\overline{\text{RESET}}$ and GND pins.
OSC_{IN}, OSC_{OUT}	I, O	Main clock circuit pins. Connecting a crystal across these pins completes main clock oscillator. The divided-by-4 main clock is used as the system clock.
V_{DD}, GND	-	Power supply input to the microcomputer
VR, AGND	-	A/D converter reference voltage : Connect to VR to V_{DD} pin and AGND to GND pin.

NOTES :

1. Hardware reset sets all I/O pins to input.
2. Input ports and I/O ports programmed as input port are provided with pull-up resistors.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}		−0.3 to V_{DD}+0.3	V
Max. Output current	I_{OH}	High-level output current (at each output)	4	mA
	I_{OL0}	Low-level output current ($P0_0$-$P0_3$, $P1_0$-$P1_3$)	30	mA
	I_{OL1}	Low-level output current (all but $P0_0$-$P0_3$, $P1_0$-$P1_3$)	4	mA
Total output current	ΣI_{OH}	High-level output current (all outputs)	20	mA
	ΣI_{OL}	Low-level output current (all outputs)	120	mA
Operating temperature	T_{OPR}		−20 to +70	°C
Storage temperature	T_{STG}		−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.0 to 5.5	V
Instruction cycle	t_{CYC}	V_{DD} = 2.0 to 5.5 V	4 to 122	µs
		V_{DD} = 5.0 V ± 10%	1 to 122	
System clock frequency	f_{SYS}	V_{DD} = 2.0 to 5.5 V	250 k to 8.192 k	Hz
		V_{DD} = 5 V ± 10%	1 M to 8.192 k	
Main clock frequency (OSC_{IN}-OSC_{OUT})	f_{OSC}	V_{DD} = 2.0 to 5.5 V	1 M to 32.768 k	Hz
		V_{DD} = 5.0 V ± 10%	4 M to 32.768 k	

DC CHARACTERISTICS

(Ta = –20 to 70°C, Typ. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.0 to 3.3 V	2	25	90	μA	3
			V_{DD} = 4.5 to 5.5 V	25	70	250		
	I_{IH1}	V_{IN} = V_{DD}				2		
	I_{IL2}	V_{IN} = 0 V			1	10	μA	4
	I_{IH2}	V_{IN} = V_{DD}			1	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.0 to 3.3 V	3	15		mA	5
			V_{DD} = 4.5 to 5.5 V	15	25			
	I_{OH1}	V_O = V_{DD} - 0.5 V	V_{DD} = 2.0 to 3.3 V	0.2	1.5			
			V_{DD} = 4.5 to 5.5 V	1.0	2.2			
	I_{OL2}	V_O = 0.5 V	V_{DD} = 2.0 to 3.3 V	70	600		μA	6
			V_{DD} = 4.5 to 5.5 V	400	1 000			
	I_{OH2}	V_O = V_{DD} - 0.5 V	V_{DD} = 2.0 to 3.3 V	200	2 000			
			V_{DD} = 4.5 to 5.5 V	1 000	2 400			
Supply current	I_{DD}	fosc = 2 MHz	V_{DD} = 4.5 to 5.5 V		1 600	3 500	μA	7
		fosc = 1 MHz	V_{DD} = 2.0 to 3.3 V		400	1 100		
			V_{DD} = 4.5 to 5.5 V		850	1 700		
		fosc = 32.768 kHz	V_{DD} = 2.0 to 3.3 V		28	170		
			V_{DD} = 4.5 to 5.5 V		55	220		
	I_{HALT}	fosc = 2 MHz	V_{DD} = 4.5 to 5.5 V		900	1 800		
		fosc = 1 MHz	V_{DD} = 4.5 to 5.5 V		500	1 100		
		fosc = 32.768 kHz	V_{DD} = 2.0 to 3.3 V		20	75		
			V_{DD} = 4.5 to 5.5 V		25	120		
	I_{STOP}	Ceramic OSC mode	V_{DD} = 2.0 to 3.3 V			3		
		Crystal OSC mode (32.786kHz)	V_{DD} = 2.0 to 5.5 V		20	45		
			V_{DD} = 4.5 to 5.5 V		25	65		
	I_{VR}	A/D active	V_{DD} = 2.0 to 3.3 V		180	420	μA	8
			V_{DD} = 4.5 to 5.5 V		300	650		
		A/D inactive	V_{DD} = 2.0 to 5.5 V			3	μA	9
A/D conversion	n	Resolution			10		bit	
	Differential linearity	fosc = 2 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Linearity	fosc = 2 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	fosc = 2 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		

NOTES :

1. Applicable pins : $P0_0$-$P0_3$, $P1_0$-$P1_3$, $P2_2$, $P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_1$, $P4_3$ (digital input mode), $P5_0$-$P5_3$
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, $P2_0$, $P2_1$, $P4_0$, $P4_2$ (digital input mode)
3. Applicable pins : $P4_0$-$P4_3$, $P3_0$-$P3_3$ (digital input mode), $\overline{RESET}$, $P2_0$-$P2_3$, $P5_0$-$P5_3$, $P0_0$-$P0_3$, $P1_0$-$P1_3$
4. Applicable pins : $P3_0$-$P3_3$, $P4_0$-$P4_3$ (A/D mode)
5. Applicable pins : $P0_0$-$P0_3$, $P1_0$-$P1_3$ (High current port)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode)
7. Non-load condition (A/D conversion disabled) MAX. V_{DD} = 5.5 V (or 3.3 V), T_{OPR} = –20°C
8. Current into VR at A/D conversion mode (run enable status)
9. Current into VR at Non-A/D conversion mode (run disable status)

SYSTEM CONFIGURATION

A Register and X Register

The A register (accumulator : Acc) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM, to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data.

A pair of A and X registers can accommodate 8 bit data.

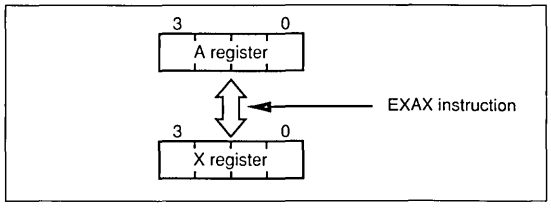


Fig. 1 Data Transfer Example between Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation.

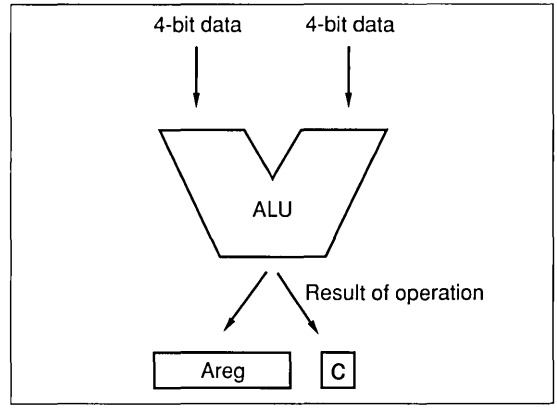


Fig. 2 ALU

The ALU operates binary addition in conjunction with RAM, C flag and A register. Cy is the symbol for carry signal and not for C flag.

The C flag latches the carry-over as the result of arithmetic instruction. The flag can be set/clear using SC and RC instructions.

The content of C flag can be tested using the TC instruction.

B Register and SB Register

• B register (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address.

The upper 4-bit section is called B_M register and lower 4-bit B_L.

• SB Register

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

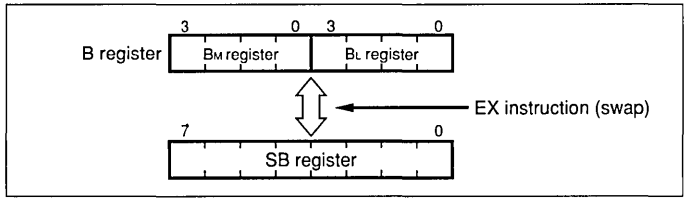


Fig. 3 B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used to store data up to 256 x 4 bits (256 nibbles).

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																※

※ 1 nibble = 4-bit

Fig. 4 RAM Nibble Mapping

Program Counter PC and Stack Register SR

• Program counter PC and stack

The program counter consists of a 7-bit page address register (P_U) and 6-bit binary counter (P_L) used to specify the steps within a page.

The stack pointer (SP) is a register which holds the starting address of the stack area of RAM space.

• Precaution on using PAT instruction

Execution of interrupt handling or the table reference instruction PAT automatically uses 1 level of the stack register SR, just like as in the case of subroutine handling process.

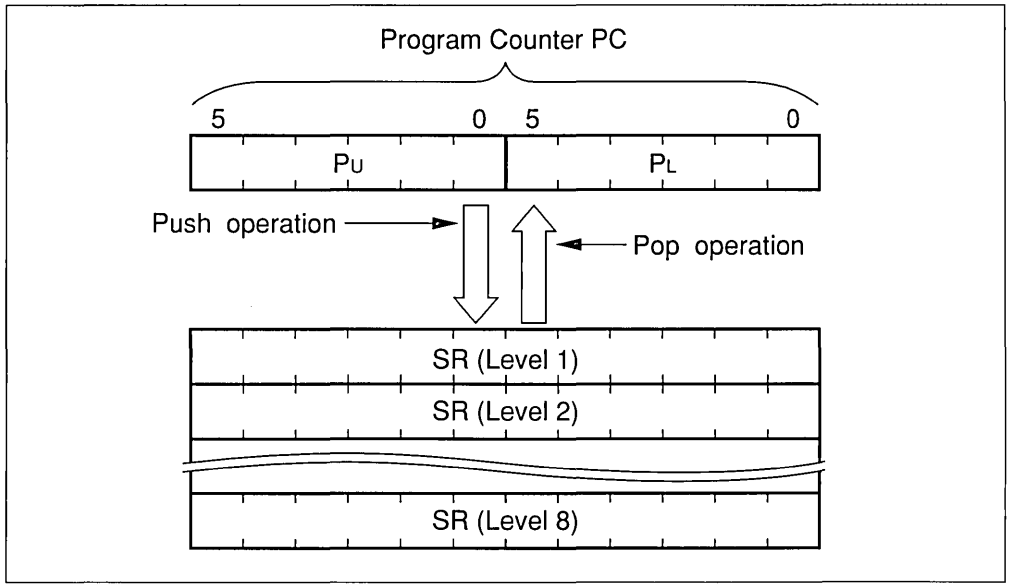


Fig. 5 Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used to store the user program. The capacity of the ROM is 4 096 bytes (64-page by 64-byte).

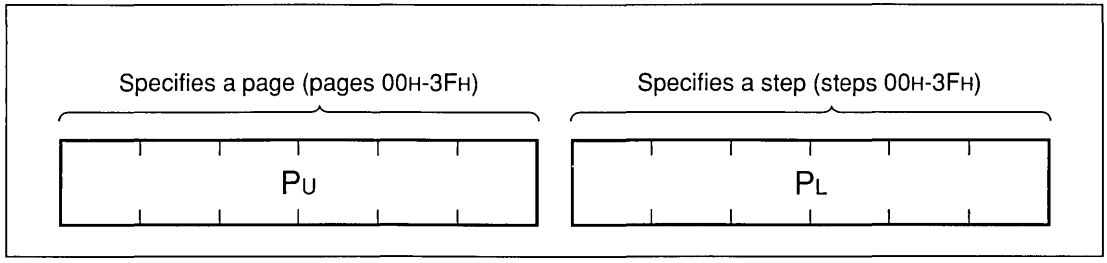
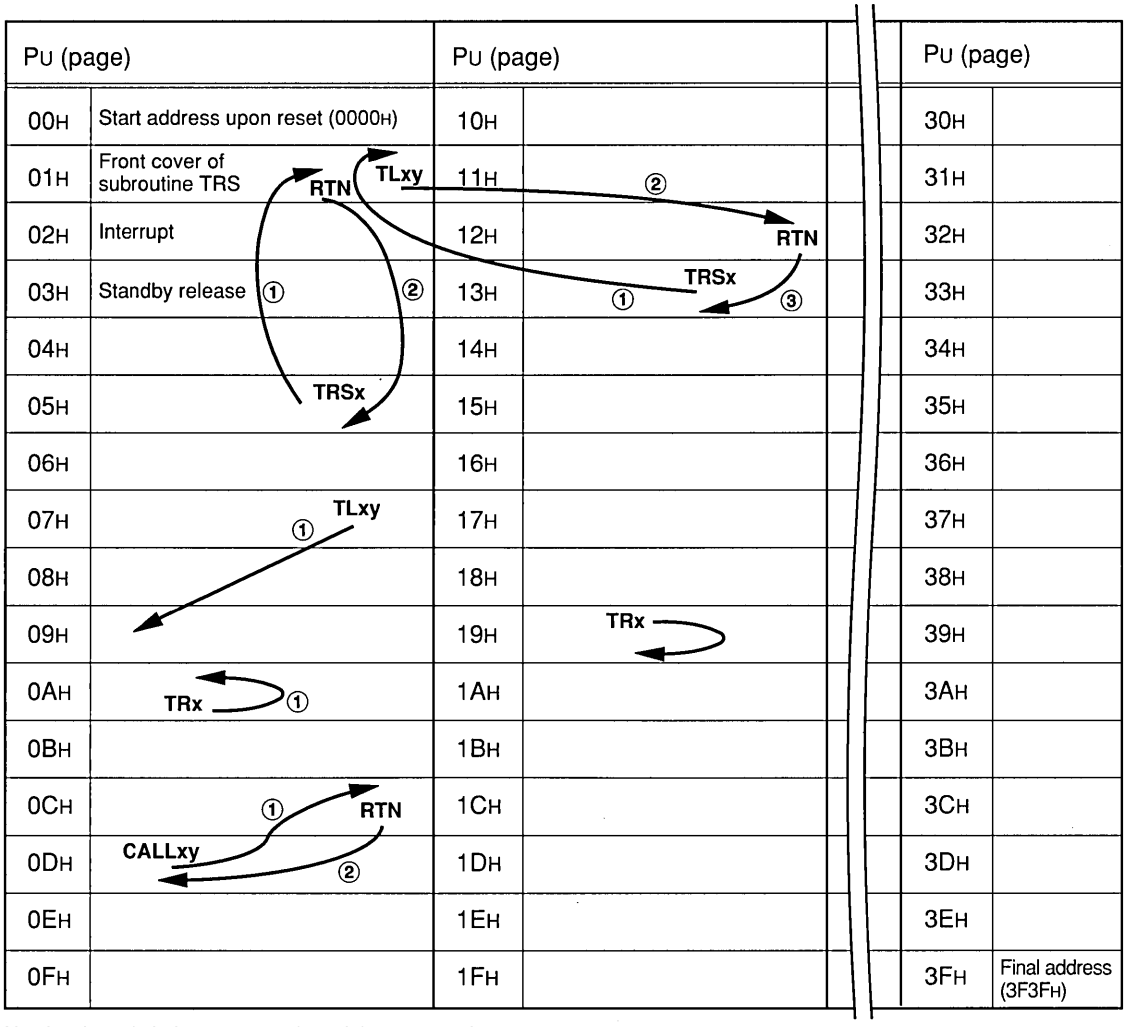


Fig. 6 Page and Step for ROM



Number in a circle is a step number of the program jump.

Fig. 7 ROM Configuration and Program Jump Example

Control Registers

Most of SM5K6 functions are controlled by reading and writing 22 control registers.

Table 1 Control Registers

ADDRESS		SYMBOL	NAME	UNIT	AVAILABLE INSTRUCTIONS				
B_M	B_L				INL	OUTL	IN/TPB	OUT	ANP/ORP
*	0	P0	P0 port	4	–	–	O	–	–
			P0 register	4	–	O	–	O	O
*	1	P1	P1 port	4	–	–	O	–	–
			P1 register	4	–	O	–	O	O
*	2	P2	P2 port	4	–	–	O	–	–
			P2 register	4	–	–	–	O	O
*	3	P3	P3 port	4	O	–	O	–	–
		R3	P3 mode register	4	–	–	–	O	O
*	4	P4	P4 port	4	–	–	O	–	–
			P4 register	4	–	–	–	O	O
*	5	P5	P5 port	4	–	–	O	–	–
			P5 register	4	–	–	–	O	O
*	6	R6	P4 direction register	4	–	–	O	O	O
*	7	R7	A/D select register	4	–	–	O	O	O
0	8	R08	A/D control register	8	–	–	Δ	O	–
0	9	R09	A/D data register	8	–	–	Δ	O	–
0	A	R0A	Timer 1 counter	8	–	–	Δ	Δ	–
0	B	R0B	Timer 1 modulo register	8	–	–	Δ	O	–
0	C	R0C	Timer 1 control register	4	–	–	O	O	O
*	D	RD	P4 mode register	4	–	–	O	O	O
*	E	RE	Interrupt enable register	4	–	–	O	O	O
0	F	R0F	P2 direction register	4	–	–	O	O	O
1	8	R18	SIO shift register	8	–	–	Δ	O	–
1	9	R19	SIO control register	8	–	–	Δ	O	–
1	A	R1A	Timer 2 counter	8	–	–	Δ	Δ	–
1	B	R1B	Timer 2 modulo register	8	–	–	Δ	O	–
1	C	R1C	Timer 2 control register	4	–	–	O	O	O
1	F	R1F	Buzzer control register	4	–	–	O	O	O

* : Don't care

O : Executable Δ : Executable but with some restriction – : Not executable

I/O Ports

The SM5K6 has 24 ports : 4 input and 20 I/O ports.

Some ports assume additional port functions :

- External interrupt input
- Standby release
- Count clock input
- Analog voltage input (A/D)
- SIO (serial interface)

• Port P0

This is a 4-bit I/O port, all 4 bits can be set to the same direction. When set as output, the port can accommodate up to 15 mA (Typ.) sink current. When used in conjunction with P1 port, the P0 delivers one half an 8-bit data.

• Port P1

This is a 4-bit I/O port, all 4 bits can be set to the same direction. When set at output, the port can accommodate up to 15 mA (Typ.) sink current. When used in conjunction with P0 port, the P1 delivers one half an 8-bit data.

• Port P2

This is a 4-bit I/O port. Each bit can be independently set its direction. Each pin of the port can also assume the following function pin.

- $P2_0$ and $P2_1$ pins : External interrupt input, standby release
- $P2_2$: Count clock input, standby release
- $P2_3$: Buzzer output, standby release

• Port P3

This is a 4-bit input port. It can serve as A/D pin in addition to a general purpose input pin.

• Port P4

This is a 4-bit I/O port. Direction of each bit can be independently set. Each pin of the port can also assume the following function pin.

- $P4_0$: A/D pin, serial data input
- $P4_1$: A/D pin, serial data output
- $P4_2$: A/D pin, serial clock I/O
- $P4_3$: A/D pin

• Port P5

This is a 4-bit I/O port, all 4 pins can be set to the same direction.

• $\overline{\text{RESET}}$ pin

Input to this pin initializes the microcomputer (hardware reset). Normal configuration is to connect a capacitor across $\overline{\text{RESET}}$ and GND pins so that the hardware reset automatically starts upon power-up. Do not leave $\overline{\text{RESET}}$ pin open.

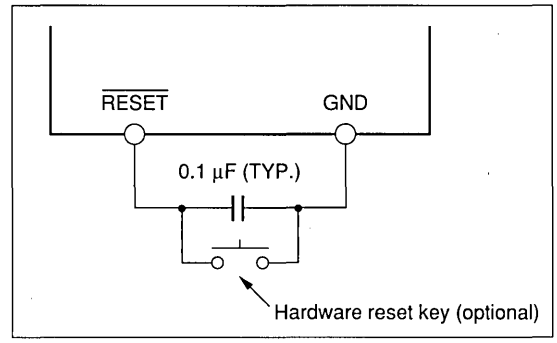


Fig. 8 Power-On Reset Circuit

Placing a low level on the $\overline{\text{RESET}}$ pin starts hardware reset of the SM5K6. For further information, see "Hardware Reset" in FUNCTIONAL DESCRIPTION.

• **OSC_{IN}, OSC_{OUT} pins**

Connecting required external components (crystal, etc.) to these pins configures the main clock oscillator.

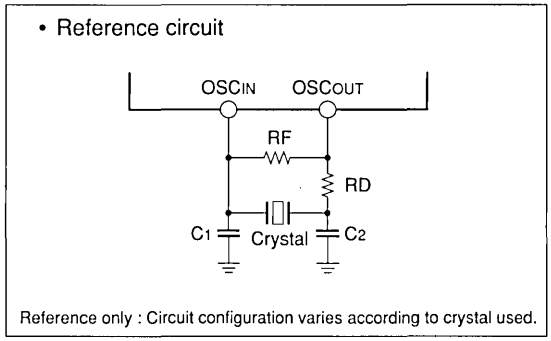


Fig. 9 Main Clock Oscillator Circuit (under evaluation)

Refer to "PRECAUTIONS FOR MICROCOMPUTERS".

• **V_{DD}, GND, VR and AGND pins**

These pins supply power supply to the SM5K6 : V_{DD} and GND supply the system power; VR and AGND supply the reference voltage to the internal A/D converter.

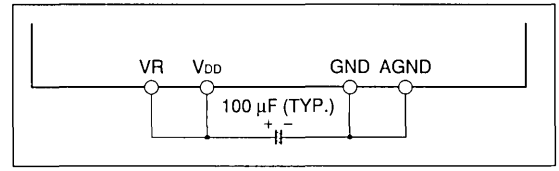


Fig. 10 Recommended Power Supply Connection

GND pin should be connected to AGND. Across V_{DD} and GND, connect an electro. capacitor to absorb external noise. Although VR can be separately supplied (2.0 to V_{DD}), it should be derived from V_{DD} for the best precise A/D conversion.

Flags

The SM5K6 has 6 flags (C flag and interrupt demand flag of IFA, IFB, IFT1, IFT2, and IFS) which are used to setting condition and judgment.

System Clock Generators and Dividers

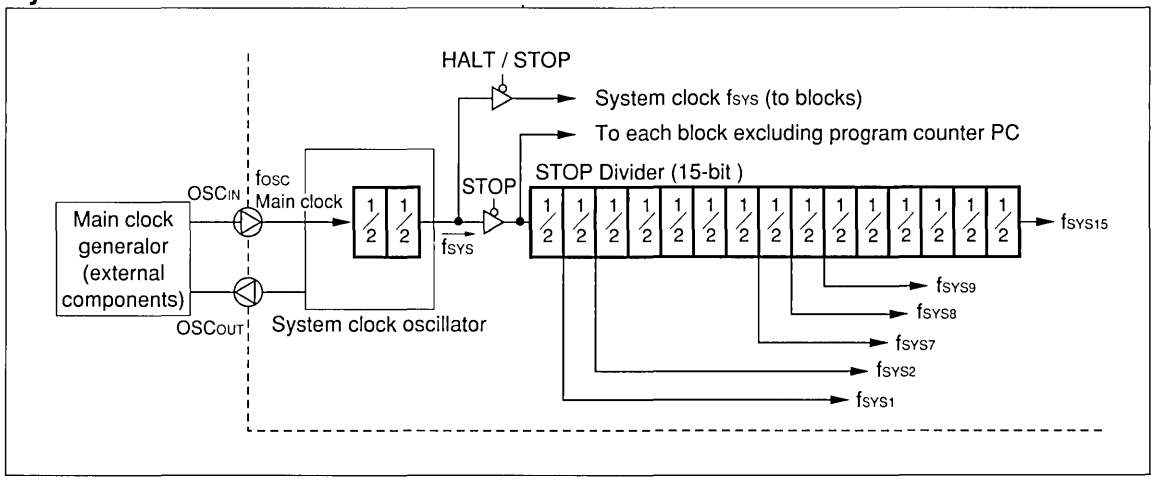


Fig. 11 System Clock Generator and Divider

• **System clock generator**

The system clock generating system is shown in Fig. 11. The system clock f_{SYS} is the divided-by-4 main clock applied through OSC_{IN} and OSC_{OUT}. See Fig. 12 for frequency relationship between these two clocks. To complete the main clock oscillator, external components must be connected between OSC_{IN} and OSC_{OUT} pins.

Execution time of 1 byte 1 cycle instruction is equal to 1 system clock period. The system clock (f_{SYS}) frequency is 1 MHz and the instruction execution time is 1 µs per cycle when the clock is derived from the 4 MHz ceramic.

The system clock frequency is 8 192 Hz and the instruction execution time is 122 µs per cycle when the clock is derived from the 32.768 kHz crystal.

The system clock f_{SYS} is also used as the count pulse input to the timer.

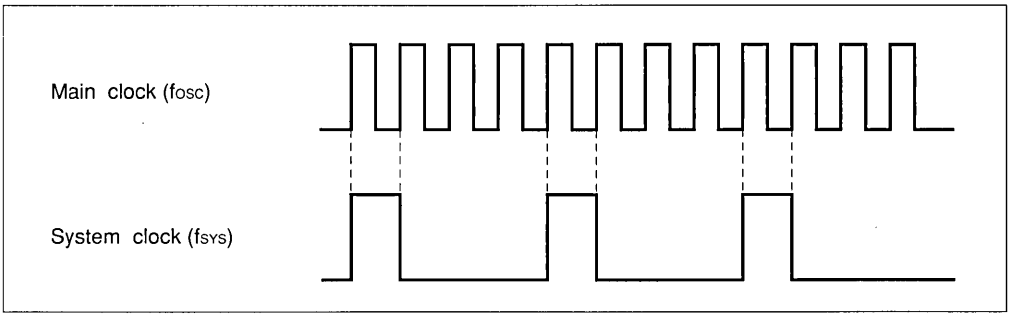


Fig. 12 Main Clock and System Clock

• **Divider (DIV)**

The divider consists of 15-step divider circuits and produces the following 6-clock from the system clock. These divided clocks are provided for timer/counters, serial interface and buzzer output. All steps of the divider can be cleared by DR instructions.

Table 2 Divider Output Clock vs f_{SYS}

SYMBOL	CLOCK
f_{SYS}*	System clock
f_{SYS1}	Divided by-2 system clock (output of 1st step)
f_{SYS2}	Divided by-4 system clock (output of 2nd step)
f_{SYS7}	Divided by-128 system clock (output of 7th step)
f_{SYS8}	Divided by-256 system clock (output of 8th step)
f_{SYS9}	Divided by-512 system clock (output of 9th step)
f_{SYS15}	Divided by-32 768 system clock (output of 15th step)

* Clock source to the 1st step of divider.

• **Resonator mask option**

Selection of type of resonator, i.e. ceramic or crystal, is made by masked option.

FUNCTIONAL DESCRIPTION

Hardware Reset

The hardware reset initializes the SM5K6 system. The hardware reset (power-on reset) starts upon power up. When the timer 2 is used as a watch dog timer, it also starts the hardware reset circuit as it overflows.

• Hardware reset and system status

The $\overline{\text{RESET}}$ pin is at high level while the SM5K6 is operating normally. When the level is forced to low externally, the hardware reset sequence starts after 2 instruction cycles. When the level on the $\overline{\text{RESET}}$ pin returns to high, the SM5K6 starts counting the main clock which is oscillating between OSC_{IN} and OSC_{OUT}. As a count about 2^{14} is reached, the system exits hardware reset status and the program starts at address 0 in page 0.

Table 3 Status of the System Immediately after Hardware Reset

PARAMETER		VALUE OR STATUS
All I/O ports (input and I/O ports)		Input mode with pull-up resistor connected
All control registers (except for SIO register R18)		0 (write only bits are also 0 when read into A register)
SIO shift register R18		Unconditional
Functions	AD converter Interrupt Standby Timer/counter Serial interface Buzzer out	All inactive or disabled
Flags	C flag	Unconditional
	Interrupt master enable flag IME	0 (all interrupts disabled)
	Interrupt request flag (IFA, IFB, IFT1, IFT2, IFS)	0
Others	A and X registers	Unconditional
	Program counter PC (P_U, P_L)	0000_H
	B register (B_M, B_L)	Unconditional
	SB register	Unconditional
	Stack register SR	Unconditional
	Level of stack register SR	Level 1
	Contents of RAM	Unconditional

Standby Feature

Standby feature saves power by stopping the program whenever it is not necessary to run. The mode in which the microcomputer is executing the program is called run mode and the mode in which it stops the program is called standby mode.
Standby mode is further divided into two modes : stop mode and halt mode, one of which is selected by Halt instruction or Stop instruction. Upon removal of standby condition, the SM5K6 returns from the standby mode to the normal run mode.
To enter the standby mode, select either stop mode or halt mode whichever appropriate.

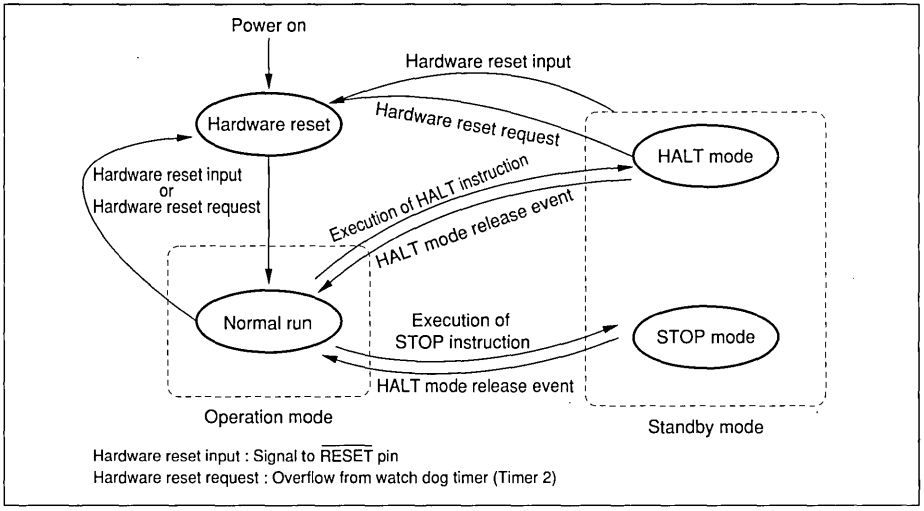


Fig. 13 Operation of Program

SYSTEM OPERATION AND STATUS DURING STANDBY MODE

• Operations in halt mode

In the halt mode, the program counter PC stops to pause the program. The system clock f_{SYS} is still supplied to other functional blocks keeping the blocks driven by the clocks from the divider and external clock activated.

• Operations in stop mode

In the stop mode, the main clock is stopped. This means that most of functional blocks are stopped.
Exceptions : P2 port can recognize external input, and the serial interface can work if operated by external clock.

Table 4 Operation / Status in Halt / Stop Mode

FUNCTIONAL BLOCK	OPERATION / STATUS	
	Halt mode	Stop mode
Hardware reset	Recognized	Recognized
Timer 1	O	×
Timer 2	O	×
A/D converter	×	×
Serial interface	O	Operates only on external clock
Buzzer out	Same as before entering halt mode	Stop (level unconditional)
I/O port	Same as before entering halt mode	Same as before entering stop mode

USE OF HALT MODE AND STOP MODE

The operation immediately returns from the halt mode to the normal mode as a halt mode release event occurs. Generally, the halt mode is used when the system repeatedly moves between the standby mode and run mode.

The stop mode further saves power than the halt mode but has some detrimental effects : time required for the system to return to the normal run mode is longer (approx. 450 instruction cycles) than that of halt mode; stop mode can be canceled only by applying low level on P2 port, SIO operating on an external clock or hardware reset. The stop mode is best suitable when the system stays for a longer period in the standby mode and does not require fast returning to the normal run mode. The standby mode retains I/O port settings and levels on the output ports as they are. Program should be prepared so that currents flowing to/from pins are reduced before the SM5K6 is put into the standby mode.

SETTING AND OPERATION OF STANDBY

• Standby release events (8-type)

RELEASING EVENT	MASKABLE	PRIORITY LEVEL	FLAG	APPLICABLE IN STOP MODE
Hardware reset input	No	–	–	Yes
Low level on $P2_0$	Yes	1	IFA	Yes
Low level on $P2_1$	Yes	3	IFB	Yes
Low level on $P2_2$	Yes	–	–	Yes
Low level on $P2_3$	Yes	–	–	Yes
End of SIO transfer	Yes	3	IFS	No
Interrupt request flag IFT1 is 1 (timer 1 overflow)	Yes	2	IFT1	No
Interrupt request flag IFT2 is 1 (timer 2 overflow)	Yes	4	IFT2	No

Interrupt Feature

The interrupt block consists of interrupt enable flags (bits of control register RE and interrupt master enable flag IME), interrupt request flags (IFA, IFB, IFT1, IFT2 and IFS) and interrupt handling circuit.

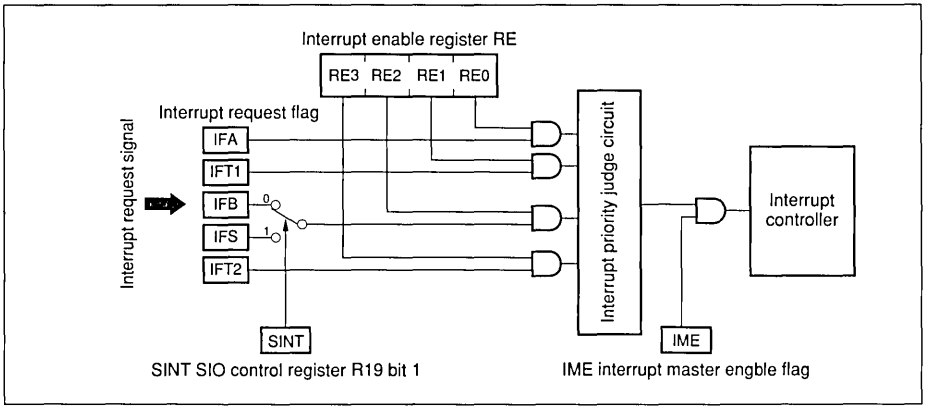


Fig. 14 Interrupt Block Diagram

• Interrupts used with SM5K6

Although the SM5K6 is provided with five interrupts, four interrupts are set at the same time because $P2_1$ selectively uses one of two.

When an interrupt occurs, the corresponding interrupt request flag (IFA, IFB, IFT1, IFT2, IFS) is set to "1" level.

• Disabling all interrupt requests (IME flag)

The interrupt master enable IME is the flag which inhibits all interrupt.

The execution of IE instruction sets the IME flag to "1", enabling the interrupt set by the interrupt enable register RE. In contrast, the ID instruction sets the IME flag to "0" and disables all interrupt requests.

Table 5 Interrupt Event Summary

INTERRUPT EVENT	FLAG	Corresponding bit of interrupt enable register RE	JUMP ADDRESS		PRIORITY LEVEL
			Page	Step	
$P2_0$ interrupt (falling edge on $P2_0$)	IFA	RE0	02H	00H	1
Timer 1 interrupt (timer 1 overflow)	IFT1	RE1	02H	02H	2
$P2_1$ interrupt (falling edge on $P2_1$)	IFB	RE2*	02H	04H	3
SIO interrupt (end of serial interface operation)	IFS				
Timer 2 interrupt (timer 2 overflow)	IFT2	RE3	02H	06H	4

* Either of $P2_1$ or SIO interrupts is selected by bit 1 of SIO control register R19.
R19 bit 1 = 0 : $P2_1$ interrupt
R19 bit 1 = 1 : SIO interrupt

• Enabling and disabling individual interrupt requests (interrupt enable register RE)

The interrupt enable register RE (RE0, RE1, RE2, RE3 : interrupt mask flag) enables and disables each of 5-interrupt. Each bit of RE is called mask flag.

Timer / Counter

The SM5K6 has two pairs of built-in timer/counter. These counters are used to handle periodic interrupts and to count external events. The overflowing timer can be used to disable the halt mode. The timer/counters serve as interval counter. In addition, the timer 2 can be used as watch dog timer (overrun detect timer). Each timer/counter consists of an 8-bit count register, modulo register and 4-bit timer control register.

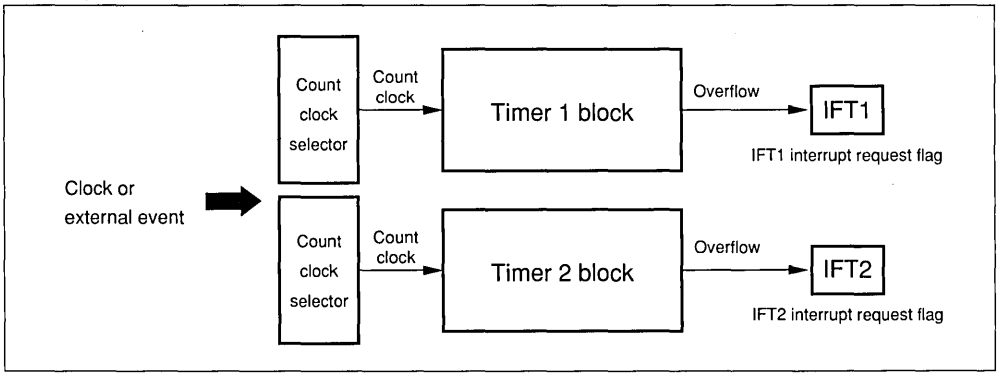


Fig. 15 Configuration of Timer / Counter

TIMER 1

The timer 1 is an 8-bit timer/counter. It counts a divided-by-n system clocks and external events. Figure 16 shows a block diagram of the timer 1. Timer 1 has no watch dog timer capability which the timer 2 has although both timers have the same configuration. Selectable clocks are also different between both timers.

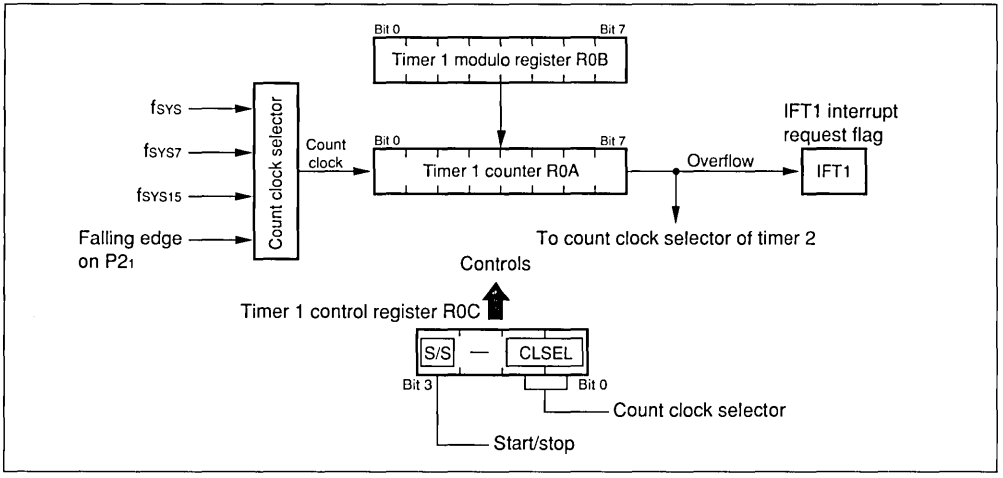


Fig. 16 Timer 1 Block

• Selecting count clock

Select the count clock by setting bits of the control register R0C.

Table 6 Selection of Count Clock

REGISTER R0C BITS		SELECTED COUNT CLOCK
$R0C_1$	$R0C_0$	
0	0	f_{SYS} (system clock)
0	1	f_{SYS7} (divided-by-7 system clock)
1	0	f_{SYS15} (divided-by-15 system clock)
1	1	External clock (falling edge on $P2_2$) When set external clock pin, $P2_2$ does not act as the standby release pin. This means that SM5K6 can count the external clock while in the halt mode. For further information, refer to "Standby Feature".

TIMER 2

The timer 2 is an 8-bit timer/counter. It counts a divided-by-n system clocks. Figure 17 shows a block diagram of the timer 2.

Timer 2 has watch dog timer capability which the timer 1 does not although both timers have the same configuration. Selectable clocks are also different between both timers.

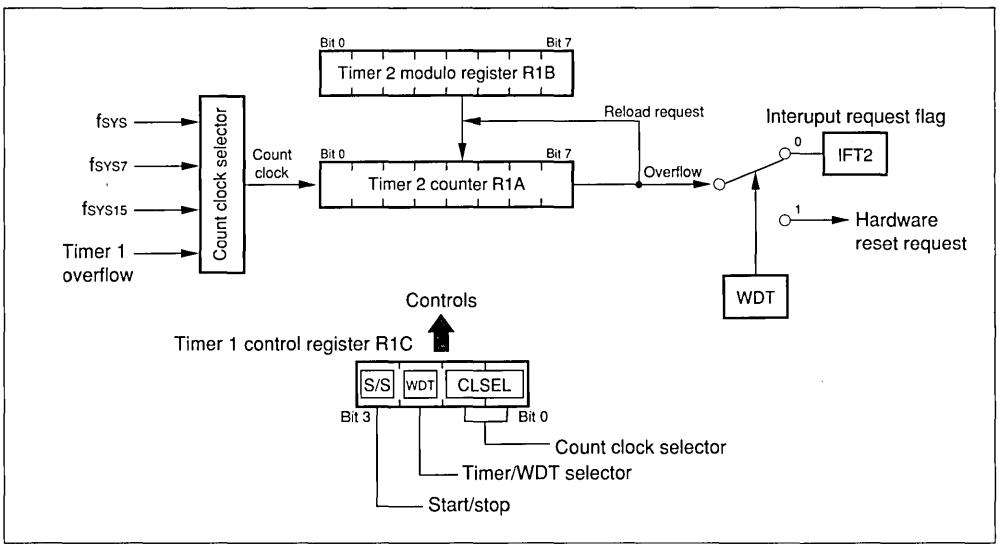


Fig. 17 Timer 2 Block

• Selecting count clock

Select the count clock by bit setting of the control register R1C. Selecting the overflow from the timer 1 as the count clock source connects the timer 2 to timer 1 in the cascade fashion, a single 16-bit timer.

• Selecting operation mode

The timer 2 can be used as a watch dog timer by the following mode setting.

Use as a normal timer :

Control register R1C, bit 2←store "0"

Use as a watch dog timer :

Control register R1C, bit 2←store "1"

This setting is made valid when done at the beginning of timer start.

Table 7 Selection of Count Clock

REGISTER R1C BITS		SELECTED COUNT CLOCK
$R1C_1$	$R1C_0$	
0	0	f_{SYS} (system clock)
0	1	f_{SYS7} (divided-by-7 system clock)
1	0	f_{SYS15} (divided-by-15 system clock)
1	1	Timer 1 overflow

• To use the timer 2 as the watch dog timer

Watch dog timer is also called overrun detect timer because it in informs the CPU that the CPU is in a closed loop and overrunning due to some trouble, for example, program error. The overflowing watch dog timer starts the hardware-reset sequence.

The program must write the initial value to the watch dog timer at an interval before the watch dog overflows. Therefore, an overflow from the watch dog timer means that the program is not running normal, for example, it is in an endless loop.

A/D converter

The SM5K6 internal 10-bit A/D converter is provided with 8 input channels and operates either in the A/D conversion mode or comparison mode.

The A/D converter mode converts the analog voltage coming through P3 and P4 ports to the equivalent digital value. The comparison mode compares the level of the input analog voltage with the voltage level set within the SM5K6 and stores the result in the microcomputer.

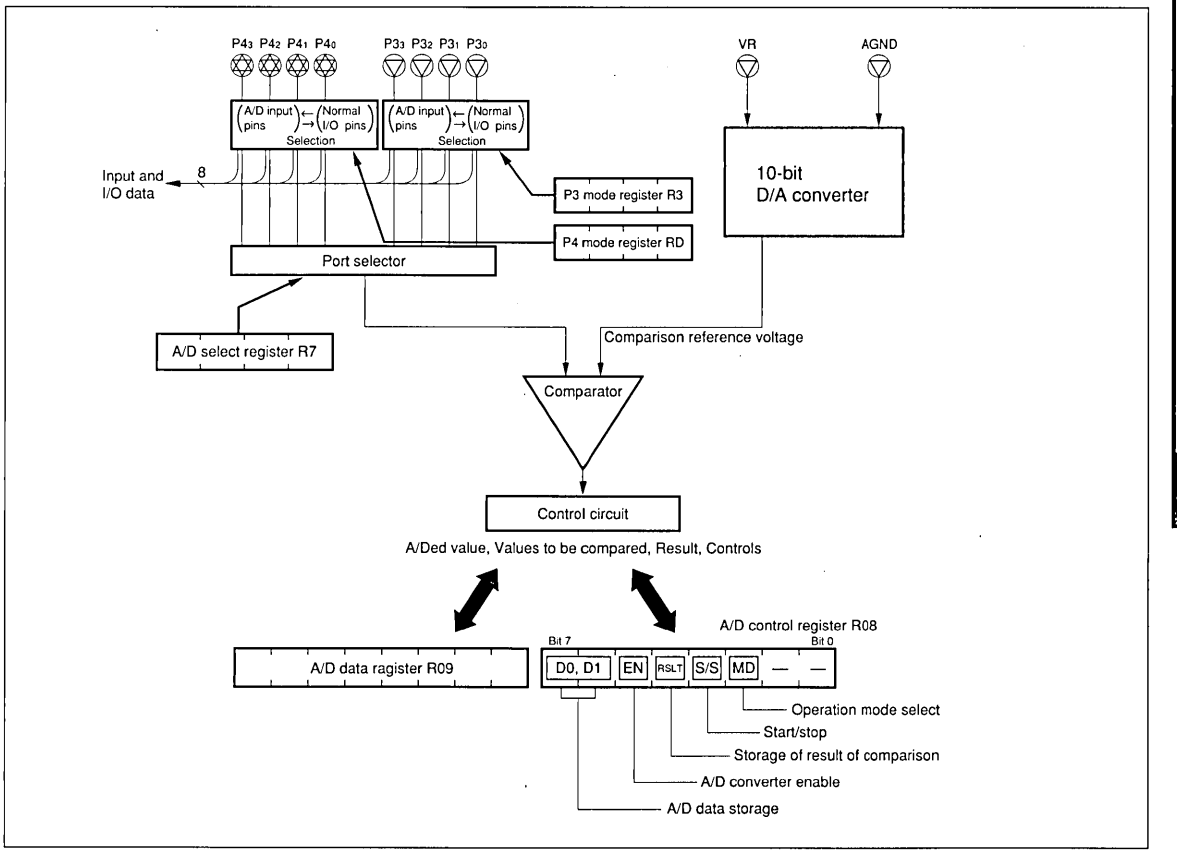


Fig. 18 Block of A/D Converter

NOTES :

1. Apply voltage within the range between 2.0 V and V_{DD} V to the VR pin, the A/D converter reference voltage pin. Do not apply a voltage outside this range.
2. Don't Apply the voltage to VR pin before feeding V_{DD} pin.
3. AGND pin must be connected to GND pin.

A/D CONVERSION MODE

The A/D conversion mode converts the analog voltage on A/D pin into the digital value. The input analog voltage is successively compared with weighted voltages from the capacitor array. Digitalized conversion data (10-bit) are stored into upper 2 bit places of the control register R08 and the remaining bits into the data register R09.
The time required for the converter to complete conversion is as follows :

Conversion duration = system clock period x 30.5
Example
- 30.5 µs (main clock at 4 MHz/1 µs system clock)
- 305 µs (main clock at 400 kHz/10 µs system clock)

Caution :
While in the A/D conversion mode, do not use registers (upper 2 bits of R08 register and the R09 register) reserved for storage of A/D data to store other data.

Serial Interface

The SM5K6 has an 8-bit synchronous serial interface which transfers 8-bit datastream in synchronous with the external or internal clock.

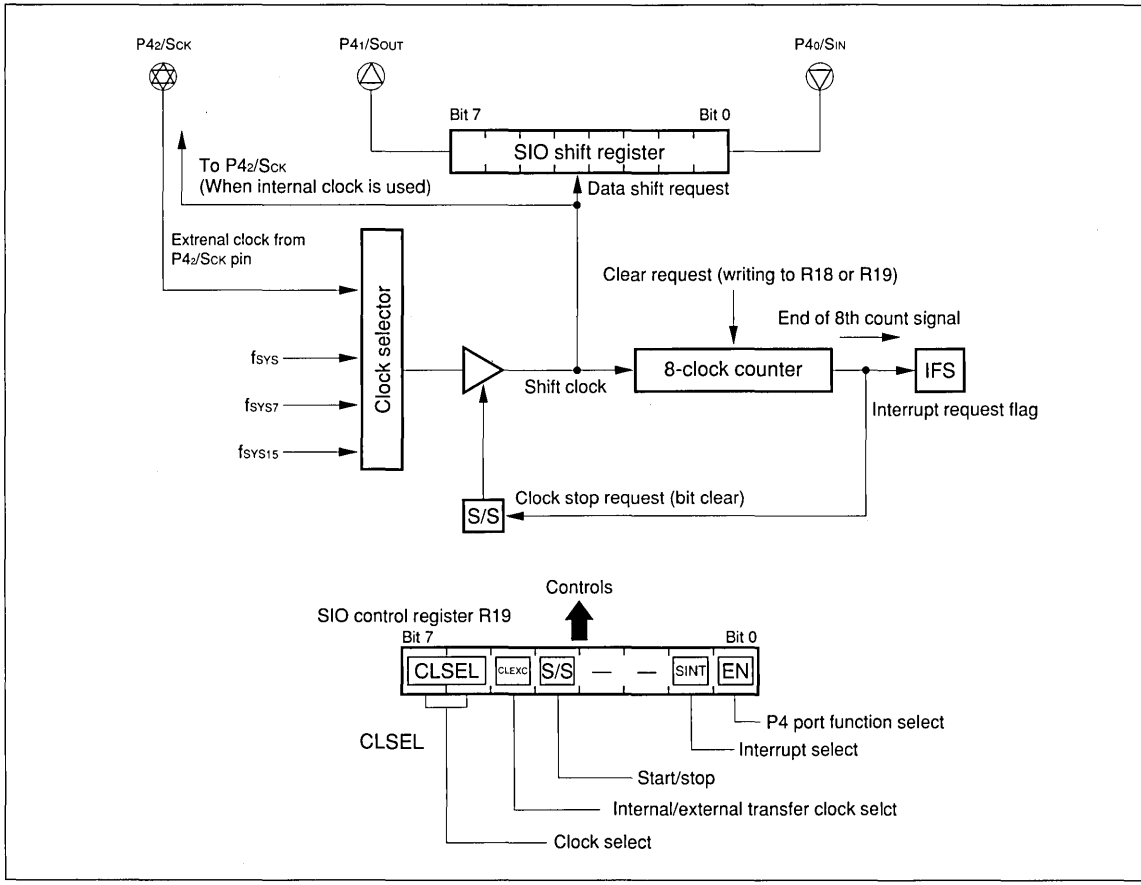


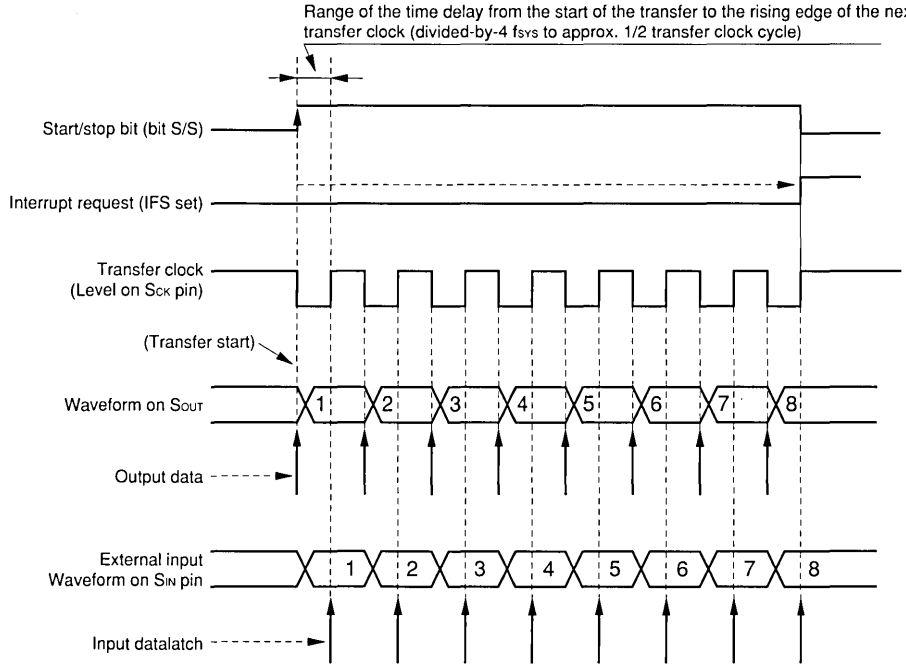
Fig. 19 Serial Interface Block

OPERATION AND CONTROL OF SIO

• Transfer timing

Transfers the contents of the shift register R18 to S_{OUT} pin on the falling edge of the transfer clock and then transfers the level on S_{IN} pin to the shift register R18 on the rising edge of the next transfer clock. Transmitted data is output MSB first and received data is input LSB first.

At the end of transfer, the oldest bit data is shifted to the MSB position of the shift register R18 and the latest data in the LSB position.



■ Transfer start timing

The SM5K6 starts transfer on the first rising edge of the transfer clock after bit S/S is set.

■ Range of the time delay from the start of the transfer to the rising edge of the next transfer clock

When the internal clock is selected as the transfer clock, the time from the falling edge of the transfer clock immediately after the start of the transfer to the rising of the next transfer clock depends on the start timing of the transfer. The minimum delay is equivalent of 1/4 f_{SYS} cycle (3/4 f_{SYS} cycle if f_{SYS} is used as the transfer clock) and maximum is approx. 1/2 clock cycle. This delay variations should be taken into consideration in applying SIO data to S_{IN} pin. To minimize delay variations, clear the divider immediately before the start of SIO.

■ Data output timing

The data output timing refers to the moment at which bits of the shift register are clocked out on S_{OUT} pin. Upwarding arrows in the diagram show output data shifting timing. Numbers (1 to 8) above indicate data output order (shift register bit 7 first, 0 last). The timing of latching the level on S_{OUT} pin to the external circuit should be determined by the external system connected to the SM5K6 based on the clock of S_{CK} pin.

■ Input data latch timing

This is the duration in which SM5K6 latches S_{IN} level to store the data into the shift register. This timing should also be determined by the external transferring device, based on the transfer clock.

Fig. 20 SIO Transfer Timing Chart

Buzzer Output

The SM5K6 generates 4 buzzer drive clocks one of which is selected and placed on $P2_3$ pin.

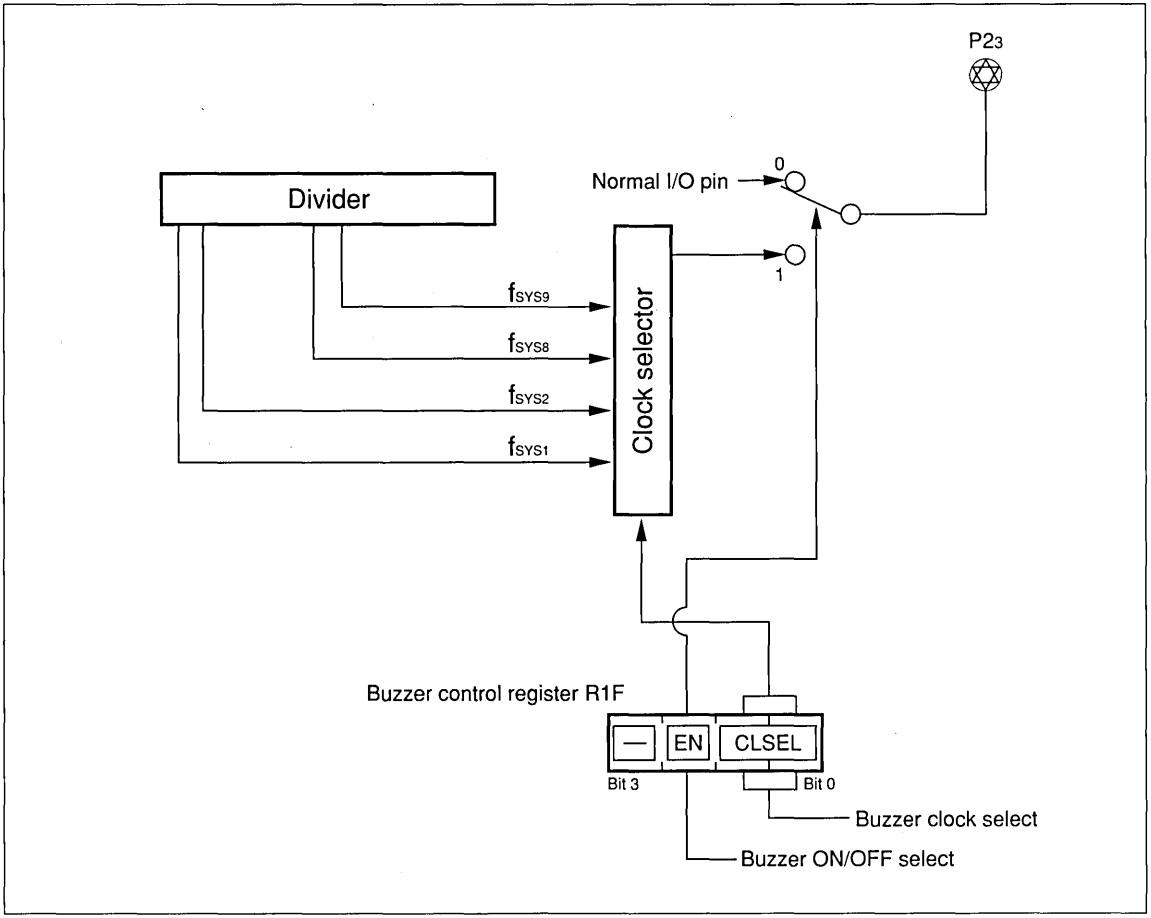


Fig. 21 Buzzer Output Block

CONTROL REGISTER SET

CONTROL REGISTER SUMMARY

Table 8 shows the configuration of control registers and settings of the B register which allows access to control register.

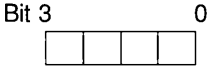
Table 8 Control Registers

B REISTER SETTING		CONTROL REGISTER NO.	NAME	CONFIGURATION
BM	BL			
*	0	P0	P0 port	———
			P0 register	P03 P02 P01 P00
*	1	P1	P1 port	———
			P1 register	P13 P12 P11 P10
*	2	P2	P2 port	———
			P2 register	P23 P22 P21 P20
*	3	P3	P3 port	———
		R3	P3 mode register	MD33 MD32 MD31 MD30
*	4	P4	P4 port	———
			P4 register	P43 P42 P41 P40
*	5	P5	P5 port	———
			P5 register	P53 P52 P51 P50
*	6	R6	P4 direction register	DR43 DR42 DR41 DR40
*	7	R7	A/D select register	– ADSEL
0	8	R08	A/D control register	D1. D0 EN RSLT S/S MD –
0	9	P09	A/D data register	D9 D8 D7 D6 D5 D4 D3 D2
0	A	R0A	Timer 1 counter	D7 D6 D5 D4 D3 D2 D1 D0
0	B	R0B	Timer 1 modulo register	D7 D6 D5 D4 D3 D2 D1 D0
0	C	R0C	Timer 1 control register	S/S – CLSEL
*	D	RD	P4 mode register	MD43 MD42 MD41 MD40
*	E	RE	Interrupt enable register	IE3 IE2 IE1 IE0
0	F	R0F	P2 direction register	DR23 DR22 DR21 DR20
1	8	R18	SIO shift register	D7 D6 D5 D4 D3 D2 D1 D0
1	9	R19	SIO control register	CLSEL CLEXC S/S – SINT EN
1	A	R1A	Timer 2 counter	D7 D6 D5 D4 D3 D2 D1 D0
1	B	R1B	Timer 2 modulo register	D7 D6 D5 D4 D3 D2 D1 D0
1	C	R1C	Timer 2 control register	S/S WDT CLSEL
1	F	R1F	Buzzer control register	– EN CLSEL

* Don't care

R3 (P3 mode register)

P3 mode register R3 sets the operation mode of P3 port (general purpose input or A/D port). The pull-up resistor is disconnected from the A/D pin which then, cannot be used as a general purpose input pin. When connecting A/D pins to the A/D converter, one of A/D pins must be set (by the corresponding bit of the A/D select register R7) to the analog voltage input pin.



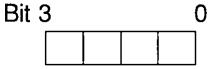
Bit i (i = 3 to 0) (Mode select bits)

Thers bits set P3i pin to either general purpose input or A/D pin.

0	(general purpose) Input
1	A/D input

R6 (P4 direction register)

P4 direction register R6 sets P4 port to input or output. P4 port also assumes A/D port and SIO I/O port. While P4 port is used as A/D or SIO port, it cannot be changed to input or output port even though direction of P4 is set by setting R6 (setting is established but ignored.)



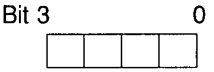
Bit i (i = 3 to 0) (Directon switch bit)

These bits switch the direction of P4i.

0	Input
1	Output

R7 (A/D select register)

The A/D select register R7 selects the A/D converter input pin among the A/D pins. Eight pins among P3 and P4 port should be set as A/D pins before setting R7. A pin other than A/D pins should not be selected as A/D converter input pin. To select A/D pins, use the P3 mode register R3 and P4 mode register RD.



Bit 3 (unused)

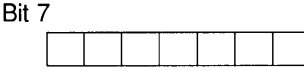
Bit 2, 1, 0 (A/D pin select bits)

These bits select one of 8 pins shown below.

000	$P3_0$	100	$P4_0$
001	$P3_1$	101	$P4_1$
010	$P3_2$	110	$P4_2$
011	$P3_3$	111	$P4_3$

R08 (A/D control register)

The A/D control register R08 stores controls of A/D converter and part of A/D data.



Bits 7, 6 (A/D data storage bits)

These bits store the A/D data (2 low bits out of 10 bits) after conversion while in the A/D conversion mode or the internal voltage set value while in the comparison mode.

Bit 5 (A/D converter enable bit)

To enable A/D converter set this bit to "1" level upon power-up. The bit is automatically reset to "0" at the end of conversion.

0	Disable
1	Enable

Bit 4 (Comparison result storage bit)

This bit stores the result of comparison when the A/D converter is operating in the comparison mode. When the pin voltage becomes equal to the internal set voltage, level of this bit is unconditional.

0 | Pin voltage < internal set voltage

1 | Pin voltage > internal set voltage

Bit 3 (Start/stop bit)

When at 1 level, the bit starts A/D converter and remains "1" level and becomes "0" at the end of conversion and remains "0" until next conversion starts. Monitoring this bit status is to monitor A/D operation.

0 | Not in operation

1 | In operation

Bit 2 (Operation mode select bit)

Change the operation mode of A/D converter.

0 | A/D conversion

1 | Comparison

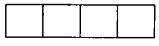
Bits 1, 0 (Unused)

R0C (Timer 1 control register)

Timer 1 control register selects the count clock for the timer 1 and starts and stops the timer.

Difference between timer 1 and timer 2 : types of count clocks selectable. Timer 2 has watch dog timer capability.

Bit 3 0



Bit 3 (Timer 1 start / stop bit)

Start and stops the timer 1 up count.

0 | Stop, in stop

1 | Count start, in operation

Bit 2 (Unused)

Bits 1, 0 (Timer 1 count clock select bits)

00 | f_{SYS} (system clock)

01 | f_{SYS7} (divided-by-7 system clock)

10 | f_{SYS15} (divided-by-15 system clock)

11 | $P2_2$ falling edge

RD (P4 mode register)

P4 mode register RD sets P4 mode to either general purpose I/O pin or A/D pin. The pin set to A/D is disconnected from the pull-up resistor. Once set to A/D port by RD, P4 cannot act as general purpose I/O or SIO port. To use P4 as I/O or SIO port, set again the mode register RD for desired P4 mode. To use A/D pins for A/D converter, set one of A/D pins to the analog voltage input pin by setting the bit of the A/D select register R7.

Bit 3 0

Bit i (i = 3 to 0) (Mode select bit)

These bits set P4i pin to general purpose I/O pin or A/D pin

0 | General purpose I/O pin

1 | A/D pin

RE (Interrupt enable register)

Interrupt enable register RE enables/disables individual interrupts. This register should be set in conjunction with the interrupt master enable flag IME (ID/IE instruction). When an interrupt is initiated, the corresponding interrupt request flag is set to "1". This and other interrupt request flags are not assigned to any control registers but separately provided. The status of each interrupt request flag can be identified by executing a specific instruction as shown below.

INTERRUPT	FLAG SYMBOL	INSTRUCTION	INTERRUPT ENABLE REGISTER BIT
$P2_0$ interrupt	IFA	TA	IE0
$P2_1$ interrupt	IFB	TB	IE2
Timer 1 interrupt	IFT1	TT1	IE1
Timer 2 interrupt	IFT2	TT2	IE3
SIO interrupt	IFS	TSF	IE2

Bit 3 0

Bit 3 (Timer 2 interrupt enable bit)
Enable the interrupt initiated by timer 2 overflow.

0	Disable
1	Enable

Bit 2 ($P2_1$/SIO interrupt enable bit)
Enable the interrupt initiated by the falling edge input on $P2_1$ or the interrupt initiated at the end of SIO (serial interface). One of these interrupt events must be selected by the setting of SIO control register R19 because only one of the events is used at a time.

0	Disable
1	Enable

Bit 1 (Timer 1 interrupt enable bit)
This bit enables initiated upon timer 1 overflow.

0	Disable
1	Enable

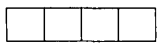
Bit 0 ($P2_0$ interrupt enable bit)
Enable interrupt from $P2_0$ initiated on falling edge on this pin.

0	Disable
1	Enable

R0F (P2 direction register)

P2 direction register R0F sets the direction of P2 port. P2 port can also assume input or output as set even if it is set as a functional port. For example, the level on this port can be read by using an input instruction, while it is set as count clock input. When $P2_3$ is set to the buzzer out, it outputs the buzzer clock as instructed to do so by the buzzer control register R1F.

Bit 3 0



Bit 3 ($P2_3$ direction switch bit)
This bit switches the direction of $P2_3$.

0	Input (standby release)
1	Output (buzzer out)

Bit 2 ($P2_2$ direction switch bit)
This bit switches the direction $P2_2$.

0	Input (standby release, count clock input)
1	Output

Bit 1 ($P2_1$ direction switch bit)
This bit switches the direction of $P2_1$.

0	Input (standby release, external interrupt)
1	Output

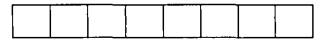
Bit 0 ($P2_0$ direction switch bit)
This bit switches the direction of $P2_0$.

0	Input (standby disable, external interrupt)
1	Output

R19 (SIO control register)

Executing OUT instruction on SIO control register clears 8 clock counter (reading serial clock 8 times). The same operation occurs if the OUT instruction is given to SIO shift register. These operations assure 8-bit data transfer upon continuing of SIO after interruption of SIO. $P2_1$ interrupt and SIO interrupt cannot be enabled at a time. End of SIO operation can be verified by "1" IFS flag through TSF instruction, if SIO interrupt cannot be used.

Bit 7 0



Bits 7, 6 (SIO transfer clock select bits)

00	f_{SYS} (system clock)
01	f_{SYS7} (divided-by-7 system clock)
10	f_{SYS15} (divided-by-15 system clock)
11	Timer 1 overflow

Bit 5 (SIO transfer clock external / internal select bit)
Select external source or internal source for transfer clock. Selection of external clock source disables setting of bits 7, 6 (SIO transfer clock select). Selection of the internal clock enables transfer of the internal clock to $P4_2$/S_{CK} pin while SIO is running.

0	External clock
1	Internal clock

Bit 4 (SIO start / stop bit)

When the internal transfer clock is selected, SIO starts upon setting of this bit to "1". When the external transfer clock, the first external clock after setting this bit to "1" starts the SIO. Upon counting 8 serial clocks, SIO stops and the external transfer clock is no longer catered for.

0 | Stop (no transfer clock catered for)

1 | Start (operation)

Bits 3, 2 (Unused)

Bit 1 (SIO interrupt select bit)

Either $P2_1$ interrupt (falling edge) or SIO interrupt is used at a time. This bit selects either interrupt.

0 | $P2_1$

1 | SIO

Bit 0 (P4 port function select bit)

This bit sets $P4_0$, $P4_1$ and $P4_2$ to general purpose I/O pin or SIO pin.

0 | $P4_0$, $P4_1$, $P4_2$: general purpose I/O

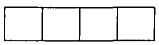
1 | $P4_0$, $P4_1$, $P4_2$: S_{IN}, S_{OUT}, S_{CK}

PIN	P4 DIRECTION SETTING BY REGISTER R6	SIO PIN CIRCUIT CONFIGURATION FOR SIO PIN (SIO STOP STATUS)
$P4_0/S_{IN}$	In (bit-R60←0)	Input with pull-up resistor
$P4_1/S_{OUT}$	Out (bit-R61←1)	CMOS output pin Previous bit is output Data unconditional after hardware reset
$P4_2/S_{CK}$	Internal clock selected : out (bit-R62←1)	CMOS output pin (high level)
	External clock selected : input (bit-R62←0)	Input pin with pull-up resistor

R1C (Timer 2 control register)

Timer 2 control register selects the count clock for the timer 2 and starts and stops the timer.
Difference between timer 1 and timer 2 : types of count clocks selectable. Timer 1 lacks watch dog timer capability.

Bit 3 0



Bit 3 (Timer 2 start / stop bit)

Start and stop the timer 2 up count.

0 | Stop, in stop

1 | Count start, in operation

Bit 2 (Timer function change bit)

Select the application of timer 2 : timer or watch dog timer (WDT, overrun detect timer)

0 | Standard timer

1 | WDT (starts hardware reset sequence upon counter overflow)

Bits 1, 0 (Timer 2 count clock select bits)

00 | f_{SYS} (system clock)

01 | f_{SYS7} (divided-by-7 system clock)

10 | f_{SYS15} (divided-by-15 system clock)

11 | Timer 1 overflow

R1F (Buzzer control register)

The buzzer control register R1F controls the clock placed on $P2_3$. This clock may also be used as an audio alarm. To use $P2_3$ as the buzzer output pin, set P2 direction register R0F for setting $P2_3$ as output pin. Once set to buzzer, $P2_3$ output must be turned off and on by the bit 2 of the buzzer control register. Once the buzzer stops, P2 output latch register is output to $P2_3$ whose level should be adjusted.

Summary of procedure :

- Set bit 3 of P2 output latch register P2 to the desired level (determine the $P2_3$ output level during buzzer stop).
- Set $P2_3$ to output pin by setting P2 direction register R0F.
- Set bit of the buzzer control register to select the output clock.
- Turn on and off the buzzer output by the bit 2 setting of buzzer control register.

Bit 3 0

Bit 3 (Unused)

Bit 2 (General purpose output / buzzer output select bit)

Select the function of $P2_3$.

0	Standard output (buzzer output stop)
1	Buzzer output

Bits 1, 0 (Output clock select bits)

Select clock to be output to $P2_3$.

00	f_{SYS9} (divided-by-9 system clock)
01	f_{SYS8} (divided-by-8 system clock)
10	f_{SYS2} (divided-by-2 system clock)
11	f_{SYS1} (divided-by-1 system clock)

INSTRUCTION SET
Definition of Symbols

M : Contents of the RAM memory location addressed by the contents of B register.

←, ↔ : Direction of transfer and exchange of contents

∪ : Logical OR

∩ : Logical AND

⊕ : Exclusive OR

Aregi : The ith (i = 0 to 3) bit of A register or control register and the like

Push : Save the contents of PC onto stack register SR

Pop : Return the contents saved in stack register SR back to PC

Pj : Port register Pj (j = 0, 1, 2, 4, 5)

Rj : Control register other than port register. j is one or two digits hexadecimal number

PORTj : Level on port (in or out)

ROM : Indicates contents at a ROM memory location :

ROM_H : Upper 4 bits of ROM content; ROML : lower 4 bits of ROM contents

CY : Carry signal. In this manual, the symbol CY is used to indicate that a carry occurs at ALU. This is also expressed as CY = 1 (note that this does not mean C flag nor bit state.

x (lower case) : Represents a set of bits in the operand. For example, an x in LDA x instruction denotes the 2 bits (I_1, I_0) in the operand. x may be substituted by "y".

reg : An abbreviation reg may follow a symbol to assure that the symbol is identified as a register. For example, Areg (or A-reg) for A register and Xreg (or X-reg) for X register to distinguish them from similar symbols or figures.

- A bit of a register is specified in the position immediately following the register symbol. For example, the bit i (0, 1, 2, 3 ...) of X register is expressed as Xi; that of P register is Pi, and so on.
- Increment means binary addition of 1_H and decrement means binary addition of F_H.
- Skipping an instruction means to ignore that instruction and to do nothing until starting the next instruction. In this sense, an instruction to be skipped is treated as an NOP instruction. Skipping 1-byte instruction requires 1-cycle, and 2-byte instruction 2-cycle. Skipping 1-byte 2-cycle instruction requires 1-cycle.

Instruction Summary (by function)

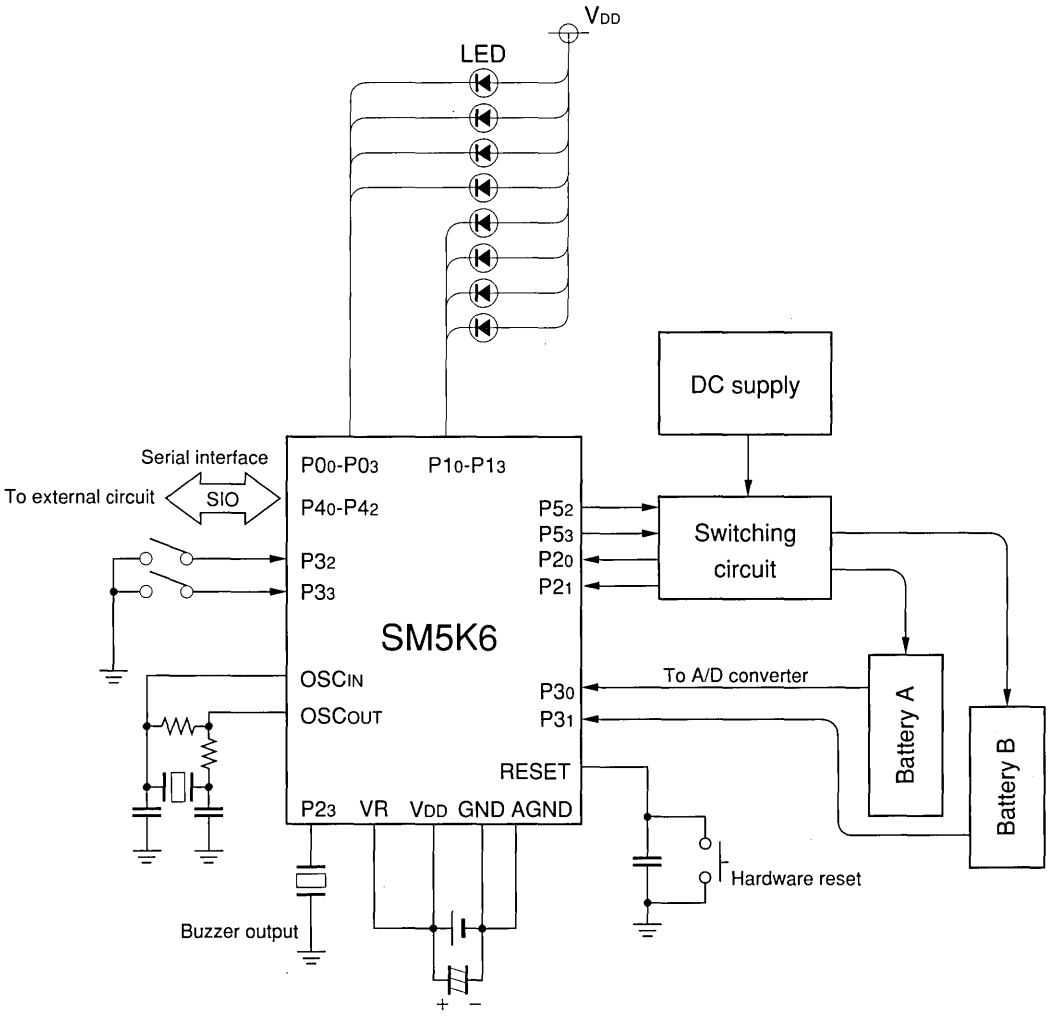
MNEMONIC	MACHINE CODE	OPERATION
ROM Addressing Instructions		
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy	E0 to E7	$P_U \leftarrow x$ (I_{11}-I_6)
	00 to FF	$P_L \leftarrow y$ (I_5-I_0)
TRS x	C0 to DF	Push, $P_U \leftarrow 01_H$ $P_L \leftarrow x$ (I_4-I_0, 0)
CALL xy	F0 to F7	Push, $P_U \leftarrow x$ (I_{11}-I_6)
	00 to FF	$P_L \leftarrow y$ (I_5-I_0)
RTN	7D	Pop (PC←SR)
RTNS	7E	Pop (PC←SR), Skip the return address
RTNI	7F	Pop (PC←SR), IME←1
Data Load Instruction		
LAX x	10 to 1F	Areg←x (I_3-I_0)
LBMX x	30 to 3F	$B_M \leftarrow x$ (I_3-I_0)
LBLX x	20 to 2F	$B_L \leftarrow x$ (I_3-I_0)
LDA x	50 to 53	Areg←M B_{M1}, $B_{M0} \leftarrow B_{M1}$, $B_{M0} \oplus x$ (I_1, I_0)
EXC x	54 to 57	M↔Areg B_{M1}, $B_{M0} \leftarrow B_{M1}$, $B_{M0} \oplus x$ (I_1, I_0)
EXCI x	58 to 5B	M↔Areg B_{M1}, $B_{M0} \leftarrow B_{M1}$, $B_{M0} \oplus x$ (I_1, I_0) $B_L \leftarrow B_L+1$ Skip the next step, if result of $B_L = 0_H$
EXCD x	5C to 5F	M↔Areg B_{M1}, $B_{M0} \leftarrow B_{M1}$, $B_{M0} \oplus x$ (I_1, I_0) $B_L \leftarrow B_L-1$ Skip the next step, if result of $B_L = 0_H$
EXAX	64	Areg↔Xreg
ATX	65	Xreg←Areg
EXBM	66	$B_M \leftrightarrow$Areg
EXBL	67	$B_L \leftrightarrow$Areg
EX	68	B-reg↔SB-reg

MNEMONIC	MACHINE CODE	OPERATION
Arithmetic Instructions		
ADX x	00 to 0F	Areg←x (I_3-I_0)+Areg Skip the next step,if CY = 1
ADD	7A	Areg←Areg + M
ADC	7B	Areg←Areg + M + C, C←CY Skip the next step, if CY = 1
COMA	79	Areg←$\overline{\text{Areg}}$
INCB	78	$B_L \leftarrow B_L+1$, Skip the next step,if result of $B_L = 0_H$
DECB	7C	$B_L \leftarrow B_L-1$, Skip the next step,if result of $B_L = 0F_H$
Test Instructions		
TAM	6F	Skip the next step, if Areg = M
TC x	6E	Skip the next step if C = 1
TM	48 to 4B	Skip the next step if Mi = 1, (i=I_1, I_0)
TABL	6B	Skip the next step if Areg = B_L
TPB x	4C to 4F	* (i = I_1, I_0) Skip the next step if PORTji* = 1 (j = 0, 1, 2, 3, 4, 5) Skip the next step Rji* = 1 (j = 08, 09, 0A, 0B, 18, 19, 1A, 1B) Skip the next step if Rji* = 1 (j = 6, 7, D, E, 0C, 0F, 1C, 1F)
TA	6C	Skip the next step if IFA = 1 IFA←0
TB	6D	Skip the next step if IFB = 1 IFB←0
TT1	69	Skip the next step if IFT1 = 1
	02	IFT1←0
TT2	69	Skip the next step if IFT2 = 1
	01	IFT2←0
TSF	69	Skip the next step if IFS = 1
	04	IFS←0
Bit Operation Instructions		
SM x	44 to 47	Mi←1, (i = I_1-I_0)
RM x	40 to 43	Mi←0, (i = I_1-I_0)
SC	61	C←1
RC	60	C←0
IE	63	IME←1
ID	62	IME←0

MNEMONIC	MACHINE CODE	OPERATION
I/O Instructions		
INL	70	Areg←PORT3
OUTL	71	P0←Areg P1←Xreg
ANP	72	Pj←Pj∩Areg (j = 0, 1, 2, 4, 5) Rj←Rj∩Areg (j = 0, 3, 6, 7, D, E, 0C, 0F, 1C, 1F)
ORP	73	Pj←Pj∪Areg (j = 0, 1, 2, 4, 5) Rj←Rj∪Areg (j = 0, 3, 6, 7, D, E, 0C, 0F, 1C, 1F)
IN	74	Acc←PORTj (j = 0, 1, 2, 3, 4, 5) Xreg, Areg←Rj (j = 08, 09, 0A, 0B, 18, 19, 1A, 1B) Areg←Rj (j = 6, 7, D, E, 0C, 0F, 1C, 1F)
OUT	75	Pj←Areg (j = 0, 1, 2, 4, 5) Rj←Xreg, Acc (j = 08, 09, 0B, 18, 19, 1B) Rj←Areg (j = 3, 6, 7, D, E, 0C, 0F, 1C, 1F) R0A←R0B, R1A←R1B
Table Reference Instruction		
PAT	6A	Push P_L← (Xreg1, Xreg0, Areg) Xreg←ROM_H, Areg←ROM_L Pop
Divider Operation Instruction		
DR	69 03	DIV (f_0-f_{15})←0 (Divider clear)
Special Instructions		
STOP	76	Change operation mode to STOP
HALT	77	Change operation mode to HALT
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

• **Versatile charger**



SM563

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

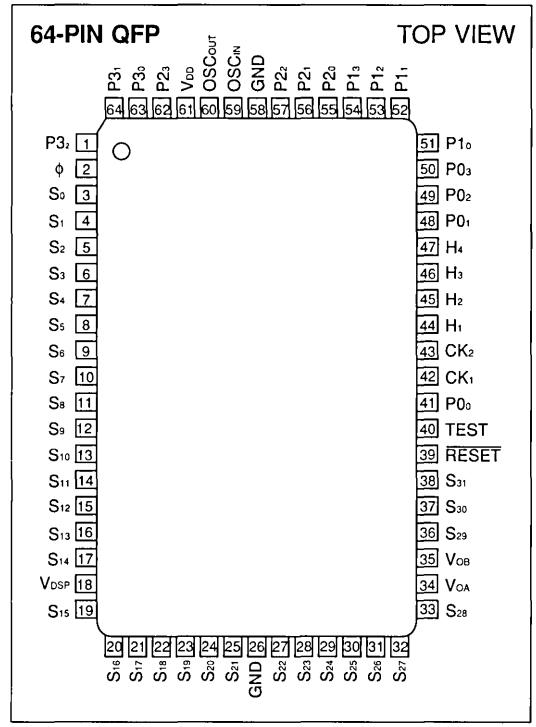
The SM563 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, ROM, RAM, I/O ports, serial interface, timer/counter in a single chip.

It provides 5 kinds of interrupt and subroutine stack function using the RAM area. Provided with a 128 segments LCD drive circuit, this microcomputer is applicable to Low power system with multiple LCD segments.

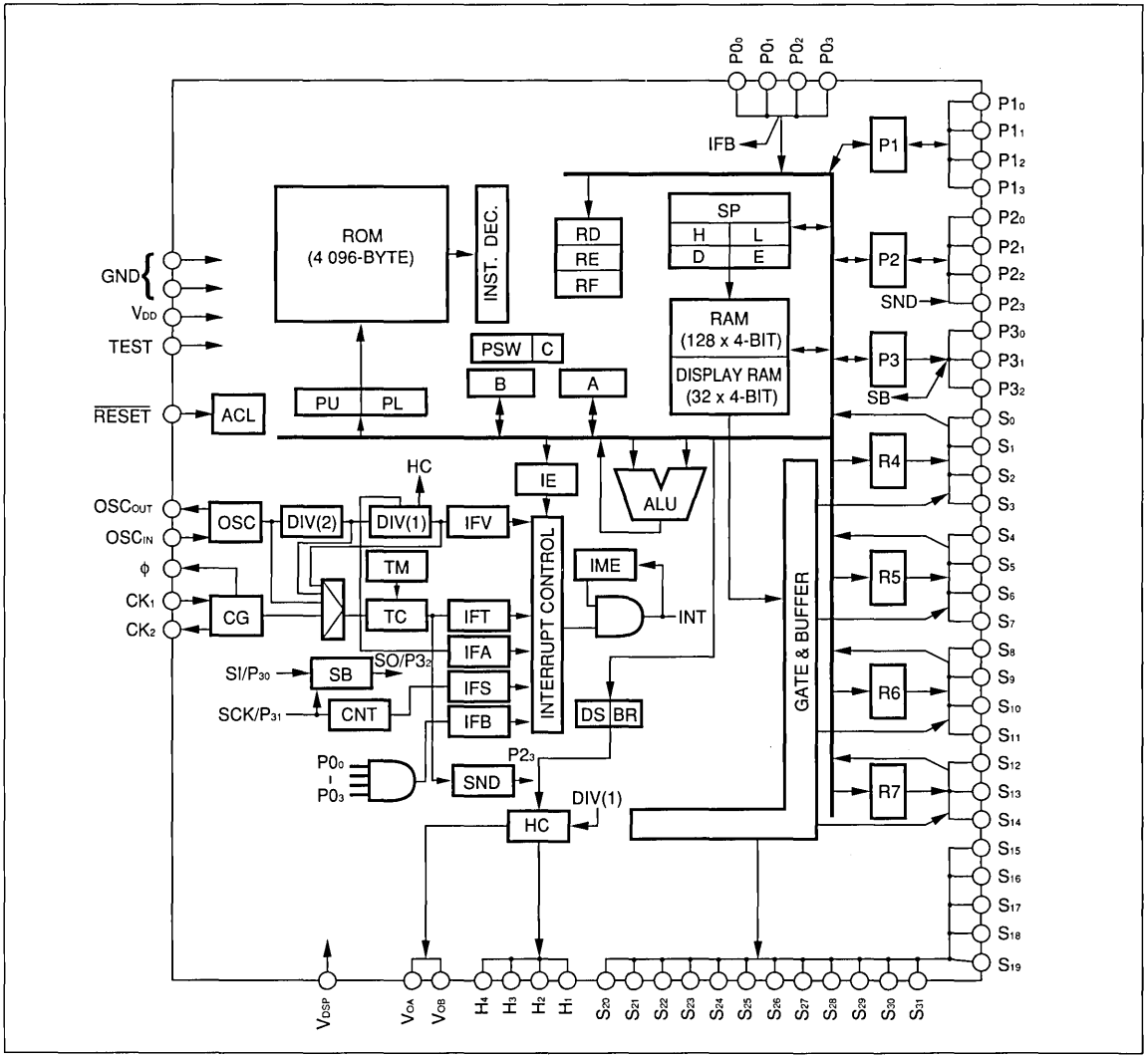
FEATURES

- ROM capacity : 4 096 x 8 bits
- RAM capacity : 160 x 4 bits (including 32 x 4 bits display RAM)
- Instruction sets : 98
- A RAM area is used as stack area
- I/O port :
  - Input 4
  - Input/output 11
  - +15 (also used as LCD segment port)
- Interrupts :
  - Internal interrupt x 4 (timer/counter, f4 signal, serial I/O, divider overflow)
  - External interrupt x 1 (P0 signal)
- Timer/counter : 8 bits x 1
- Serial interface : 8 bits x 1
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver : 128 segments, 1/3 bias, 1/4 duty cycle (If LCD drive circuit is used, a crystal oscillator circuit needs to be constituted between OSC_{IN} and OSC_{OUT})
- Instruction cycle time : 6.67 µs (at 3V), 2 µs (at 5V)
- Buzzer output
- Standby function
- Supply voltage : 2.7 to 5.5 V
- Package : 64-pin QFP (QFP064-P-1420)

PIN CONNECTIONS



BLOCK DIAGRAM



Nomenclature

A, B	: Accumulators	IME	: Interrupt master enable F/F
ACL	: Auto clear	P1-P3	: Registers
ALU	: Arithmetic logic unit	PL, PU	: Program counters
BR, DS	: Common signal control F/F	PSW	: Program status word register
CG	: Clock generator	R4-R7	: General-purpose registers
DIV	: Divider	RD, RE, RF	: Mode registers
D, E, H, L	: General-purpose registers	SB	: Shift register
HC	: Common signal circuit	SP	: Stack pointer
IE	: Interrupt enable F/F	TC	: Count register
IFA, IFB	: Interrupt requests	TM	: Modulo register
IFS, IFT, IFV			

PIN DESCRIPTION

SYMBOL	I/O	CIRCUIT TYPE	FUNCTION
$P0_0$-$P0_3$	I	Pull up	Acc←$P0_0$-$P0_3$
$P1_0$-$P1_3$	I/O	Pull up	I/O selectable by instructions
$P2_0$-$P2_3$	I/O	Pull up	I/O selectable independently Sound output only when $P2_3$ pin is used as an output
$P3_0$-$P3_3$	I/O	Pull up	Serial interface I/O by setting the mode register RE
S_0-S_{14}	O or I/O		Selectable between segment ports and I/O ports through an RC register
S_{15}-S_{31}	O		Display RAM contents output as LCD segment signals
H_1-H_4	O		4-value output capability; used for LCD common output
TEST	I	Pull down	For test (connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
ϕ	O		System clock output
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DSP}, V_{OA}, V_{OB}			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	−0.3 to +7	V	1
	V_{DSP}	−0.3 to +7	V	
Input voltage	V_{IN}	−0.3 to V_{DD} +0.3	V	1
Output voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V	1
Output current	I_{OUT}	20	mA	2
Operating temperature	T_{OPR}	−20 to +70	°C	
Storage temperature	T_{STG}	−55 to +150	°C	

NOTES :

1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

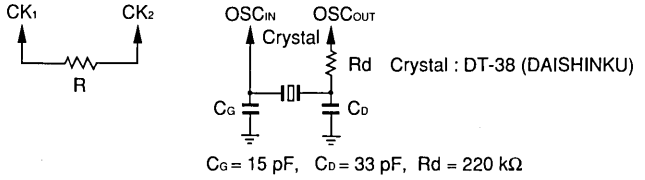
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}		2.7		5.5	V	
	V_{DSP}		2.7		V_{DD}	V	
Basic oscillation frequency	f	V_{DD} = 2.7 to 5.5 V	250		600	kHz	1
		V_{DD} = 4.5 to 5.5 V	250		2 000		
Instruction cycle	t	V_{DD} = 2.7 to 5.5 V	6.7		16	µs	
		V_{DD} = 4.5 to 5.5 V	2		16		
Crystal oscillation frequency	fosc			32.768		kHz	

NOTE :

1. Frequency fluctuation : ± 30%

Oscillation Circuit



C_G = 15 pF, C_D = 33 pF, Rd = 220 kΩ

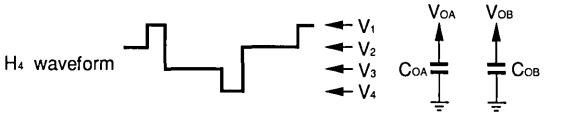
DC CHARACTERISTICS

(V_{DD} = 2.7 to 5.5 V, Ta = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}		0.7 x V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.3 x V_{DD}	V	
	V_{IH2}		V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}		0		0.5	V	
Input current	I_{IH}	V_{IN} = 0 V	2		200	µA	1
		V_{DD} = 4.5 to 5.5 V	20		200		
Output current	I_{OH1}	V_{OH} = V_{DD}−0.5 V	50			µA	3
	I_{OL1}	V_{OL} = 0.5 V	250			µA	
	I_{OH2}	V_{OH} = V_{DD}−0.5 V	5		250	µA	4
	I_{OL2}	V_{OL} = 0.5 V	500			µA	
	I_{OH3}	V_{OH} = V_{DD} − 0.5 V	100			µA	5
		V_{DD} = 4.5 to 5.5 V	400				
	I_{OL3}	V_{OL} = 0.5 V	0.5			mA	
		V_{DD} = 4.5 to 5.5 V	1.6				
Output impedance	R_C			5	20	kΩ	6
	R_S			10	40	kΩ	7
Output voltage	V_1	V_{DSP} = 3.0 V No load	2.7		3	V	8
	V_2		1.7	2	2.3	V	
	V_3		0.7	1	1.3	V	
	V_4		0		0.3	V	
Supply current	I_{OP}	f = 600 kHz, V_{DD} = 3.0 V		0.4	1.5	mA	9
	I_{SB}	Standby current V_{DSP} = 3.0 V		15	40	µA	10
		V_{DD} = 3.0 V		8	20		11

NOTES :

1. Applied to pins $P0_0$-$P0_3$, $\overline{\text{RESET}}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_2$ (during input mode).
2. Applied to pins CK_1, TEST, OSC_{IN}.
3. Applied to pin CK_2.
4. Applied to pins $P1_0$-$P1_3$ (during output mode).
5. Applied to pins $P2_0$-$P2_3$, $P3_0$-$P3_2$ (during output mode), ϕ.
6. Applied to pins H_1-H_4.
7. Applied to pins S_0-S_{31}.
8. Applied to pins H_1-H_4, S_0-S_{31}.
9. No load condition.
10. No load condition when bleeder resistance is ON.
11. No load condition when bleeder resistance is OFF.



C_{OA} = 1 µF, C_{OB} = 1 µF

PIN FUNCTIONS

• GND, V_{DD}, V_{DSP} (Power supply inputs)

Both GND pins 26 and 58 should be grounded.

The V_{DD} pin is the positive power supply with respect to GND.

The V_{DSP} pin is the positive power supply for an LCD driver with respect to GND.

• TEST (Test input)

The TEST pin should be left open or connected to GND with a pull-down resistor.

• $\overline{\text{RESET}}$ (Input)

The $\overline{\text{RESET}}$ accepts an active Low system reset which initializes the internal logic of the device.

Normally a capacitor of about 0.1 µF is connected between this pin and GND to provide a power on reset function.

• OSC_{IN}, OSC_{OUT} (Crystal oscillator pins)

The OSC_{IN} and OSC_{OUT} pins connect with an external crystal oscillator and these pins and the GND connect with a capacitor, which constitute an oscillator circuit.

The output of the oscillator is coupled to a clock divider for real-time clock operation.

• CK_1, CK_2 (System clock CR oscillator pins)

The CK_1 and CK_2 pins, in conjunction with a resistor between them, provide a system clock oscillator.

• H_1 to H_4 (Common signal outputs)

The H_1 to H_4 pins are used to drive the common of an LCD.

• S_0 to S_{31} (Segment outputs)

The S_0 to S_{31} pins drive LCD segments. Pins S_0 through S_{14} may also be used as I/O ports when specified with the mode register RC.

• $P0_0$ to $P0_3$ (Inputs)

The P0 pins are normally used to accept key input data. A falling edge at these pins resets the IFB flag.

• $P1_0$ to $P1_3$ (Input/output)

The P1 are I/O pins connected to the positive supply with pull-up resistors.

They may be switched between input and output modes through an instruction.

• $P2_0$ to $P2_3$ (Input/output)

The $P2_0$ to $P2_3$ pins are bit-independent I/O ports which can be independently set to input or output mode with the mode register RF.

When the $P2_3$ is used for an output pin, it serves exclusively as a sound output pin, which can output a sound signal with any frequency set up by the timer counter.

Pins $P2_0$ and $P2_1$ output the OD and R/W signals with the mode register RC.

• $P3_0$ to $P3_2$ (Input/output)

The $P3_0$ to $P3_2$ pins are I/O pins which are connected to the positive supply with pull-up resistors.

These pins can be set to I/O mode for use in a serial interface with the mode register RE.

SYSTEM CONFIGURATION

ROM and Program Counter

The on-chip ROM has a configuration of 64-page x 64-step x 8-bit, and stores programs and table data.

The program counter consists of a 6-bit page address counter P_U and a 6-bit binary counter P_L used to specify the steps within a page.

The locations shown in Fig. 1 are allocated in the on-chip ROM.

Stack Pointer (SP)

The stack pointer (SP) is an 8-bit shift register which holds the starting address of the stack area of RAM space. Immediately after the reset, the contents of the stack pointer are uninitialized and must be set to an appropriate value. If, for instance, the initial value of the stack pointer is set to 80_H, the data memory are beginning with the highest address (excluding the display RAM area) $7F_H$, is usable as a stack area.

RAM

Data memory has a 160-word x 4-bit configuration, and is used to store processing data and other information. Data memory is also used as a stack area to save register values, the program counter value, and program status word (PSW) at the time a subroutine jump or an interrupt occurs. Fig. 2 shows the RAM configuration. 2 x 16 x 4-bit of entire RAM space is used as a display RAM area from which data is output to LCD segment driving pins. An LCD with a 1/4 duty and 1/3 bias format can be directly driven by writing display data into the display RAM area. The display RAM outputs are, as shown in Fig.3, connected to segment output pins S_0 to S_{31} for individual set of common outputs H_1 to H_4. The segment output pins provide a single digit of display RAM data M_0 to M_3, as an LCD driving waveform signal according to H_1 to H_4 outputs. The operations of the display RAM are identical to those of other RAM areas.

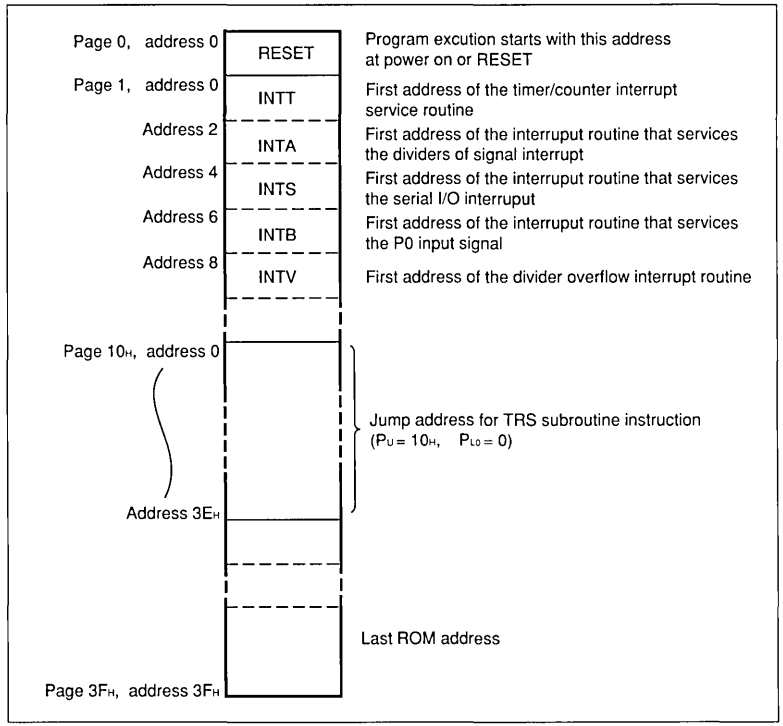


Fig. 1 Program ROM Map

L \ H	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
0000									S_0	S_{16}
0001									S_1	S_{17}
0010									S_2	S_{18}
0011									S_3	S_{19}
0100									S_4	S_{20}
0101									S_5	S_{21}
0110									S_6	S_{22}
0111									S_7	S_{23}
1000									S_8	S_{24}
1001									S_9	S_{25}
1010									S_{10}	S_{26}
1011									S_{11}	S_{27}
1100									S_{12}	S_{28}
1101									S_{13}	S_{29}
1110									S_{14}	S_{30}
1111									S_{15}	S_{31}

NOTE :

The area with the thick line is allocated for a display RAM and the Sn (n = 0 to 31) shows the related segment outputs.

Fig. 2 RAM Configuration

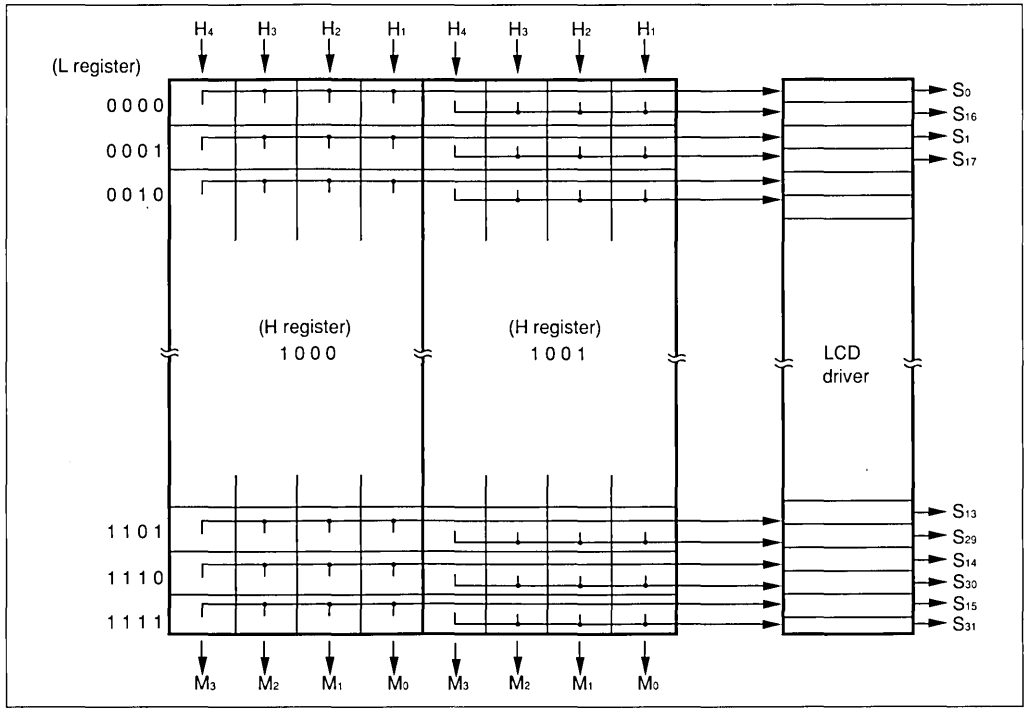


Fig. 3 Display RAM and its LCD Segment Outputs

Accumulator (A), Subaccumulator (B) and Arithmetic and Logic Unit (ALU)

The accumulator (A) is a 4-bit working register which is the nucleus of the single chip system. It holds the results of operations and transfers data to memory, I/O ports, and registers.

A subaccumulator (B) is another 4-bit register. It is used as one of general-purpose registers, and when combined with the A to form a B-A register pair, allows data transfer on an 8-bit basis.

The arithmetic and logic unit (ALU) performs, in conjunction with a carry flag (C), binary addition, shift operations, and logical operations such as AND, OR, EX-OR, and complement.

General-Purpose Registers (H, L, D, E)

Registers H and L are 4-bit general-purpose registers. They can transfer and compare data with the Acc on 4-bit basis. Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis. The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations. The L register can be incremented or decremented and is used to access I/O ports and mode registers.

Clock Divider, IFV Flag, IFA Flag

The device contains a crystal oscillator and a 15-stage divider, as shown in Fig. 4. A real-time clock

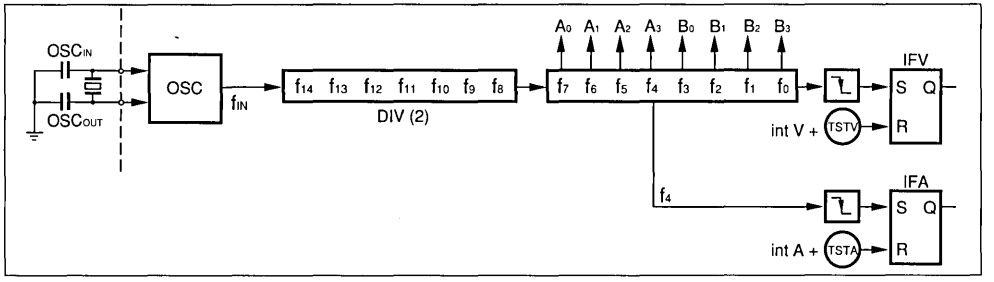


Fig. 4 Real-Time Clock and Divider

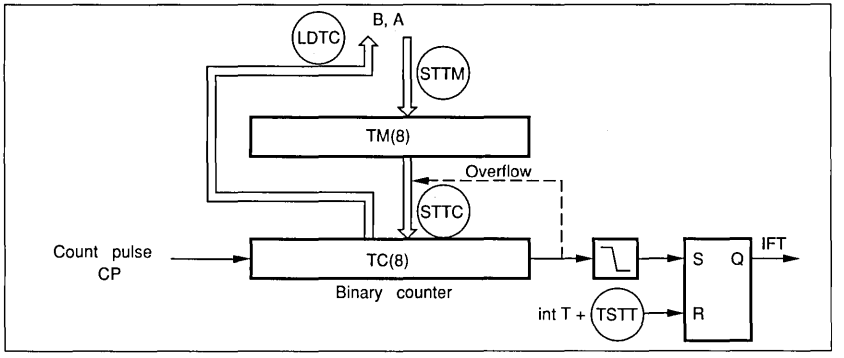


Fig. 5 Timer/Counter

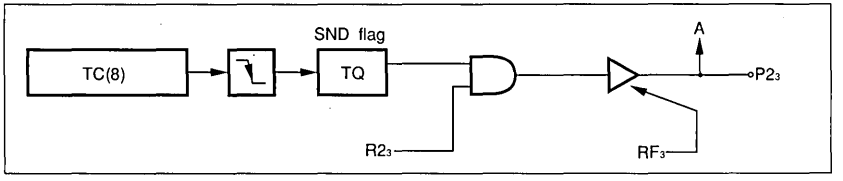


Fig. 6 SND Signal

can be provided by connecting an external crystal oscillator between the oscillator pins. When an external 32.768 kHz crystal oscillator is used, the f_0 signal is a frequency of 1 Hz.

Timer/Counter and the SND Signal

The timer/counter consists of an 8-bit count register (TC) and an 8-bit mudulo register (TM).

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register (See Fig. 5).

The count pulse CP can be selected from divider signals f_{IN}, f_8 and f_0, and the system clock, by using the mode register RD. If the count register (TC) overflows, the SND flag reverses its status at the falling edge of the TC. A sound signal can be obtained at the TC output by putting P2 in output mode and sending a "1" to pin $P2_3$ (See Fig. 6).

Serial Interface and IFS

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data. The serial clock can be selected with either an internal clock (system clock) or an external clock.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin, and the data input from the SI pin at the rising edge of a serial clock is loaded into the lowest bit of the shift register. When the internal clock is used, immediately after the SIO instruction is executed, the serial operation begins and stops with 8 clocks which are output from the SCK pin.

Upon completion completion of an 8-bit shift operation, the serial I/O ending flag IFS is set each time a 3-bit counter overflows, and an interrupt request occurs.

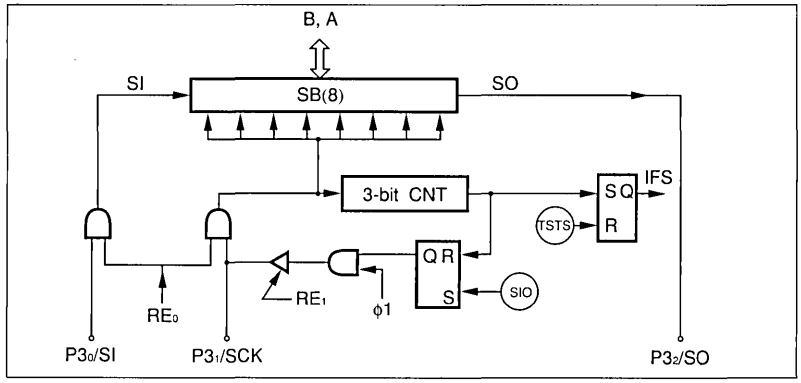


Fig. 7 Serial Interface

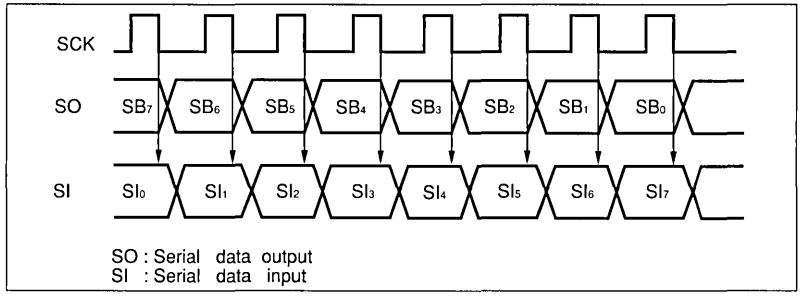


Fig. 8 Serial Interface Timing

Input Port P0 and IFB Flag

The IFB flag is set at the falling edge of the signal applied to the input port P0 by which the interrupt is enabled.

When port P0 is used as a key input, it can cause an interrupt each time a key is operated.

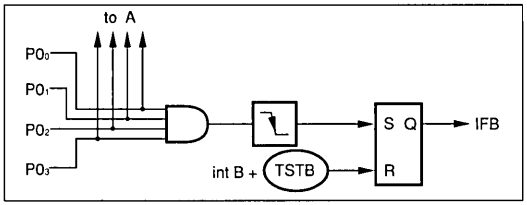


Fig. 9 P0 port

Interrupts

When an interrupt occurs, the corresponding interrupt request flag is set. The CPU acknowledges the interrupt if it is enabled (Master interrupt enable flag and the corresponding interrupt enable flag are set). If more than one interrupt occurs simultaneously, all of the corresponding interrupt request flags will be set, but the CPU will only acknowledge that interrupt with the highest priority and other interrupts will be queued.

I/O Ports

Port P0 is a 4-bit parallel input port. The IFB flag is set at the falling edge of this port.

Port P1 can be switched between input and output modes, 4-bit at a time.

Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.

Ports $P2_0$ and $P2_1$ can output the OD and R/W signals, respectively. In those cases, these pins should be kept High in an output mode. Port $P2_3$ outputs the SND signal in the output mode.

Port P3 is a 4-bit I/O port which can be placed in input or output mode, 3-bit at a time. Each bit of port P3 can be set to the I/O modes (SI, SO, SCK) of a serial interface.

Ports P1 and P3 are placed in an output mode when a port output instruction is executed, and in an input mode when a port input instruction is executed. After an ACL operation, ports P1, P2 and P3 are all placed in an input mode.

Every input port has pull-up resistors. (Pull-up resistors for I/O ports are effective only when the ports are placed in an input mode.)

Ports P1 through P3 in an output mode can be independently set or reset by instructions.

When a key-matrix is configured by using I/O ports, if the short on output pins may occur caused by a multiple key depression, port P1 should be used as an output.

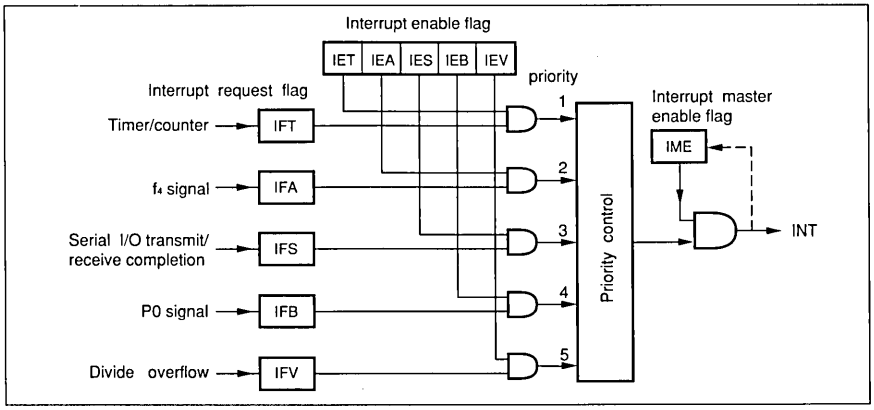


Fig. 10 Interrupt Handling

Table 1 Characteristics of I/O Ports

PORT	FUNCTION	Direct 4-bit parallel I/O		IN, OUT instruction		Bit independent output SPn
		Input (INA)	Output (OUTA)	Input (IN)	Output (OUT)	Direct pin-independent output RPn
P0	Input-only port	O	X	O	X	X
P1	I/O port	O	O	X	O	O
P2	I/O port, P_{23} -sound output	O	O	X	X	O
P3	$P3_0$-SI, $P3_1$-SCK, $P3_2$-SO, multi-control port	O	O	X	X	O

O : Yes, X : No

Standby Mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated. Standby mode may be cleared with the interrupt request or the RESET signal.

Reset Function (ACL)

Applying a Low level signal to the $\overline{\text{RESET}}$ pin resets the internal logic of the device and applying a High level signal starts execution of the program at address 0, page 0. Once the device is reset, all I/O ports are placed in input mode, all interrupts are disabled, and the LCD display turns off. The device is also reset when it is powered up.

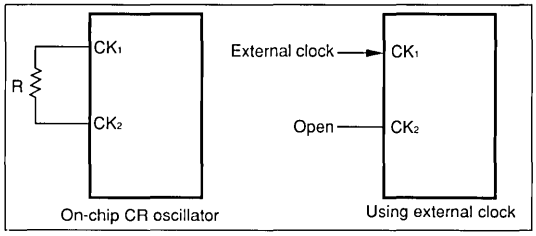


Fig. 11 Main Clock Sources

Main Clock Oscillator Circuit

The main clock oscillator requires an external resistor across pins CK_1 and CK_2. Instead of using on-chip oscillator, an external clock may be applied to pin CK_1. In this case, pin CK_2 should be left open. The system clock ϕ is a divided clock equivalent to 1/4 of the clock applied to pin CK_1.

LCD Driver

• Display segment

The SM563 contains an on-chip LCD driver which can directly drive an LCD with a 1/4 duty and 1/3 bias. Fig.12 shows an example of LCD segment configuration for 1/4 duty.

Each segment of the LCD can be turned on or off by software control of the setting of the corresponding bit "1" or "0" in the display RAM area (see Fig. 3).

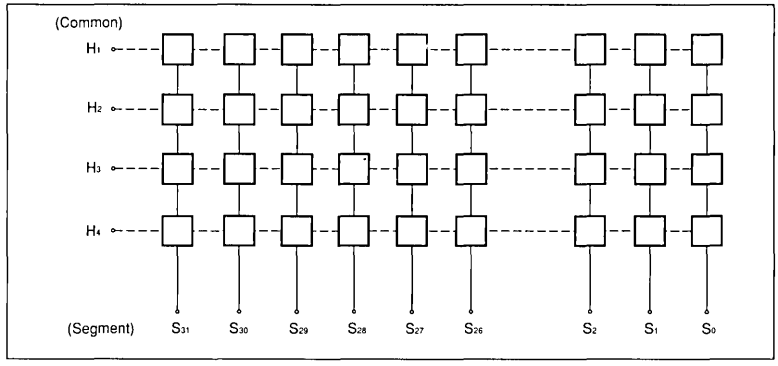


Fig. 12 LCD Segment Configuration for 1/4 Duty

The LCD digit may have any shape, provided that the maximum number of segments does not exceed 128 (see Fig. 12). Fig. 13 shows an example of a 7-Segment Numeric LCD Digit.

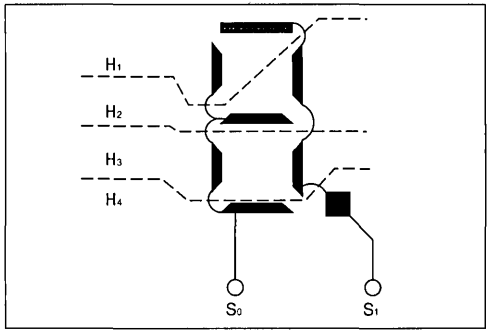


Fig. 13 7-Segment Numeric LCD Digit

• LCD driving signal waveform

Fig. 14 shows the LCD signal driving waveforms required to display the number "5" on the 7-segment display shown in Fig. 13 (segment outputs S_0 and S_1 are used). A voltage of 3 V is applied to pin V_{DSP} in the Fig. 14. The frame frequency (I/T) can be selected from 64 Hz or 128 Hz by mask options.

• V_{OA} and V_{OB} pins

The device contains bleeder resistors to allow 1/3 bias driving. When V_{DSP} is 3 V, voltages of 2 V and 1 V are output from pins V_{OA} and V_{OB} respectively. Normally pins V_{OA} and V_{OB} are left open. When an LCD with a large display area is driven, connect capacitors across pins V_{OA} and V_{DSP} and across V_{OB} and V_{DSP} to improve the rise time of the LCD driving signal.

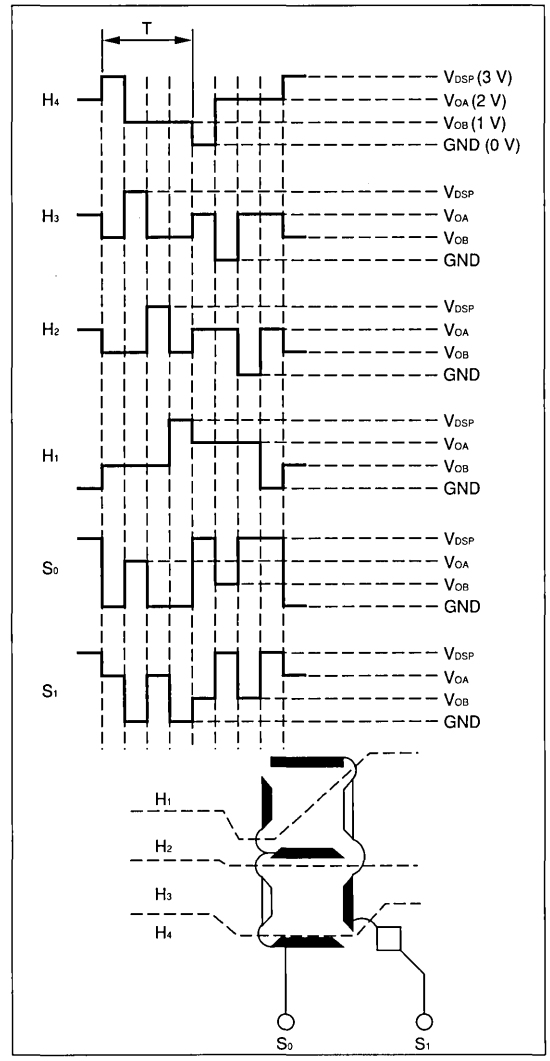


Fig. 14 LCD Driving Signal Waveform (required to display the number 5)

INSTRUCTION SET

ROM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy (2-byte)	E0 to EF 00 to FF	$P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
TRS x	C0 to DF	(SP–2), (SP–3), (SP–4)←PC SP←SP–4 $P_U \leftarrow 10_H$ $P_L \leftarrow x$ (I_4,I_3,I_2,I_1,I_0,O)
CALL xy (2-byte)	F0 to FF 00 to FF	(SP–2), (SP–3), (SP–4)←PC SP←SP–4, $P_U \leftarrow x$ (I_{11}-I_6), $P_L \leftarrow y$ (I_5-I_0)
JBA x (2-byte)	7F 30 to 3F	P_{U5}-$P_{U2} \leftarrow x$ (I_3-I_0), P_{U1}, P_{U0}, P_{L5}, P_{L4}←B, P_{L3}-P_{L0}←A
RTN	61	P_U, P_L←(SP), (SP+1), (SP+2)
RTNS	62	P_U, P_L←(SP), (SP+1), (SP+2), SP←SP+4
RTNI	63	P_U, P_L←(SP), (SP+1), (SP+2), PSW←(SP+3), SP←SP+4, IME←1

RAM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
STL	69	L←A
STH	68	H←A
EXHD	3F	H↔D L↔E
LIHL xy (2-byte)	3D 00 to FF	H←x (I_7-I_4), L←y (I_3-I_0)

Data Transfer Instructions

MNEMONIC	MACHINE CODE	OPERATION
EX pr	5C to 5F	A↔(pr)
LDX adr (2-byte)	7D 00 to FF	A←(adr)
STX adr (2-byte)	7E 00 to FF	(adr)←A
EXX adr (2-byte)	7C 00 to FF	A↔(adr)
LAX x	10 to 1F	A←x (I_3-I_0)
LIBA xy (2-byte)	3C 00 to FF	B←x (I_7-I_4) A←y (I_3-I_0)
LBAT	60	B←ROM (P_{U5}-P_{U2}, B, A)$_H$ A←ROM (P_{U5}-P_{U2}, B, A)$_L$
LDL	65	A←L
LD pr	54 to 57	A←(pr)
ST pr	58 to 5B	(pr)←A
EXH	6C	A↔H
EXL	6D	A↔L
EXB	6E	A↔B
STB	6A	B←A
LDB	66	A←B
LDH	64	A←H
PSHBA	28	(SP–1)←B, (SP–2)←A, SP←SP–2
PSHHL	29	(SP–1)←H, (SP–2)←L, SP←S–2
POPBA	38	B←(SP+1), A←(SP), SP←SP+2
POPHL	39	H←(SP+1), L←(SP), SP←SP+2
STSB	70	SB_H←B, SB_L←A
STSP	71	SP_H←B, SP_L←A
STTC	72	TC←TM
STTM	73	TM_H←B, TM_L←A
LDSB	74	B←SB_H, A←SB_L
LDSP	75	B←SP_H, A←SP_L
LDTC	76	B←TC_H, A←TC_L
LDDIV	77	B←DIV_H, A←DIV_L

Arithmetic Instructions

MNEMONIC	MACHINE CODE	OPERATION
ADX x	00 to 0F	A←A+x (I_3-I_0), Skip if C_Y = 1
ADD	36	A←A+(HL)
ADDC	37	A←A+(HL)+C, C←C_Y, Skip if Cy = 1
OR	31	A←A ∨ (HL)
AND	32	A←A ∧ (HL)
EOR	33	A←A ⊕ (HL)
ANDB	22	A←A ∧ B
ORB	21	A←A ∨ B
EORB	23	A←A ⊕ B
COMA	6F	A←$\overline{A}$
ROTR	25	C→A_3→A_2→A_1→A_0→C
ROTL	35	C←A_3←A_2←A_1←A_0←C
INCB	52	B←B+1, Skip if B = F_H
DECB	53	B←B–1, Skip if B = 0
INCL	50	L←L+1, Skip if L = F_H
DECL	51	L←L–1, Skip if L = 0
DECM adr	79 00 to FF	(adr)←(adr) –1, Skip if (adr) = 0
INCM adr	78 00 to FF	(adr)←(adr) +1, Skip if (adr) = F_H

Test Instructions

MNEMONIC	MACHINE CODE	OPERATION
TAM	30	Skip if A = (HL)
TAH	24	Skip if A = H
TAL	34	Skip if A = L
TAB	20	Skip if A = B
TC	2A	Skip if C = 0
TM x	48 to 4B	Skip if (HL), x = 1
TA x	4C to 4F	Skip if Ax = 1
TSTT	2B	Skip if IFT = 1, IFT←0
TSTA	2C	Skip if IFA = 1, IFA←0
TSTS	2D	Skip if IFS = 1, IFS←0
TSTB	2E	Skip if IFB = 1, IFB←0
TSTV	2F	Skip if IFV = 1, IFV←0

Bit Manipulation Instructions

MNEMONIC	MACHINE CODE	OPERATION
SM x	40 to 43	(HL) x←1
RM x	44 to 47	(HL) x←0
RC	26	C←0
SC	27	C←1
RIME	3A	IME←0
SIME	3B	IME←1
DI x (2-byte)	7F C0 to DF	IEF←IEF ∧ x
EI x (2-byte)	7F E0 to FF	IEF ∨ x

I/O Instructions

MNEMONIC	MACHINE CODE	OPERATION
IN	67	A←P0
OUT	6B	P1←A
INA x (2-byte)	7F A0 to A9	A←P (x), R (x)
OUTA x (2-byte)	7F B0 to BF	P (x), R (x)←A
INBA x	7F 80 to 81	B←R (x +1) A←R (x)
OUTBA x (2-byte)	7F 90 to 91	R (x +1)←B R (x)←A
SP xy (2-byte)	7A 00 to F3	P (y)←P (y) x
BP xy (2-byte)	7B 00 to F3	P (y)←P (y) x
RDS (2-byte)	7F 60	DS←0
RBR (2-byte)	7F 70	BR←0
SDS (2-byte)	7F 61	DS←1
SBR (2-byte)	7F 71	BR←0
READ (2-byte)	7F 62	A←P4 with OD
WRIT (2-byte)	7F 72	P4←A with R/W
READB (2-byte)	7F 63	A←P4, with OD B←P5
WRITB (2-byte)	7F 73	P4←A, with R/W P5←B

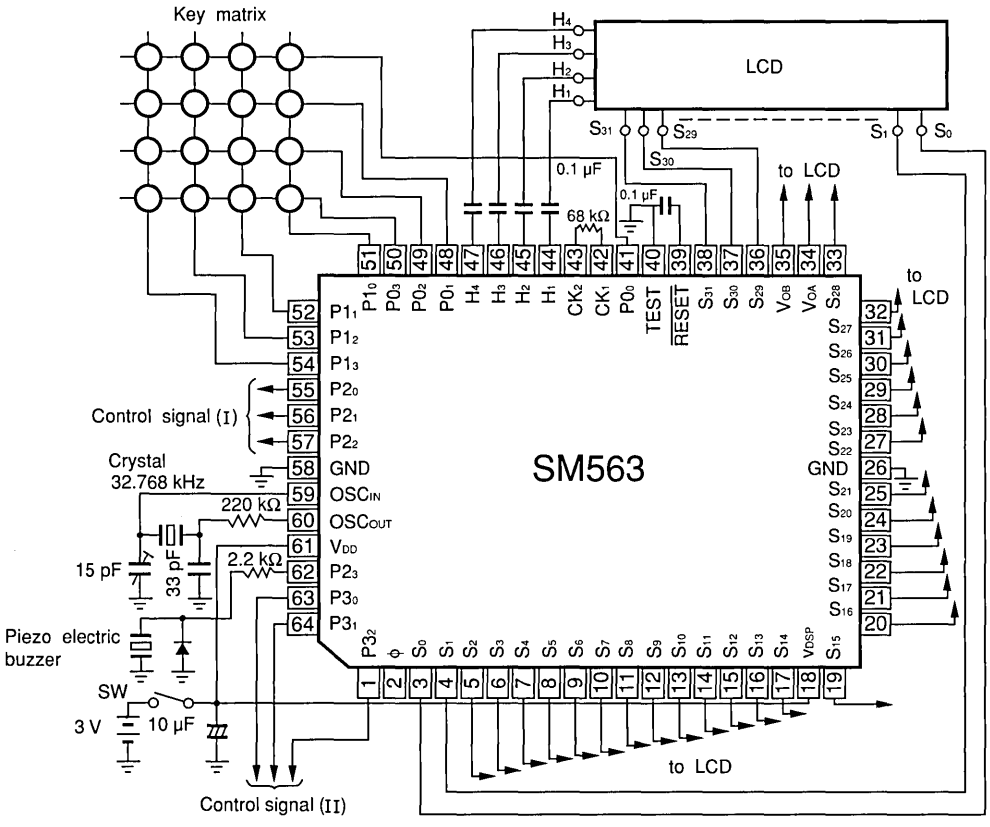
Special Instructions

MNEMONIC	MACHINE CODE	OPERATION
SIO	3E	Serial I/O start
IDIV (2-byte)	7F 10	DIV←0
SKIP	00	No operation
CEND (2-byte)	7F 00	System clock stop

NOTE :

The machine code consists of 8-bit of I_7, I_6, I_5, I_4, I_3, I_2, I_1 and I_0.

SYSTEM CONFIGURATION EXAMPLE



SM565

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

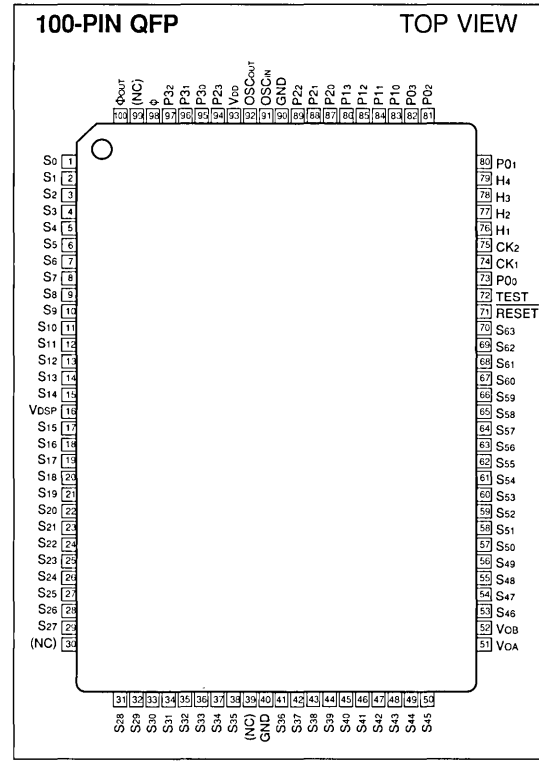
The SM565 is a CMOS 4-bit single-chip microcomputer incorporating carrier output circuit for remote control, ROM, RAM, I/O ports, serial interface, and timer/counter. It provides 5 kinds of interrupts and subroutine stack function using the RAM area. Provided with a 256 segments LCD drive circuit, this microcomputer is applicable to a multi-functional AV remote control system, high performance hand-held LCD games or any other similar system with Low power consumption.

FEATURES

- ROM capacity : 8 192 x 8 bits
- RAM capacity : 256 x 4 bits (including 64 x 4 bits display RAM)
- Instruction sets : 98
- A RAM area is used as stack area
- I/O port :
  - Input 4
  - Input/output 11
  - +16 (Also used as LCD segment port)
- Interrupts :
  - Internal interrupt x 4 (timer/counter, f4 signal, serial I/O, divider overflow)
  - External interrupt x 1 (P0 signal)
- Timer/counter : 8 bits x 1
- Serial interface : 8 bits x 1
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver : 256 segments, 1/3 bias, 1/4 duty cycle (If LCD drive circuit is used, a crystal oscillator circuit needs to be constituted between OSC_{IN} and OSC_{OUT}.)

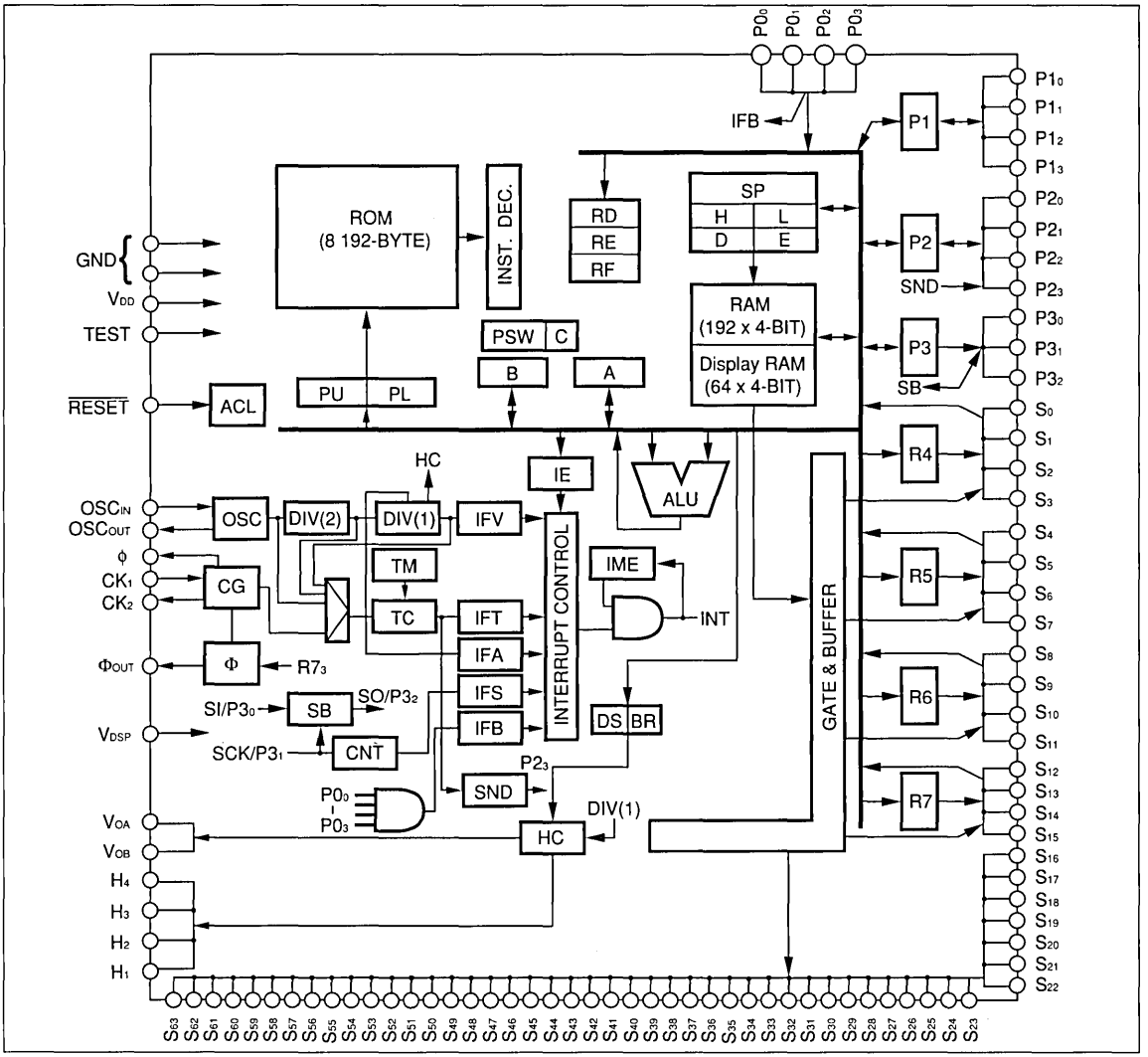
PIN CONNECTIONS

100-PIN QFP TOP VIEW



- Built-in carrier output circuit for remote control
  - Carrier frequency 37.9 kHz
  - Basic oscillation frequency (main clock) 455kHz
  - Duty cycle 1/3 or 1/2 (mask option)
  - Reversal polarity (mask option)
- Instruction cycle time :
  - 8.79 µs (TYP., 455 kHz, at 3 or 5 V)
- Buzzer output
- Standby function
- Supply voltage : 2.4 to 5.5 V
- Package : 100-pin QFP (QFP100-P-1420)

BLOCK DIAGRAM



Nomenclature

A, B	: Accumulators
ACL	: Auto clear
ALU	: Arithmetic logic unit
BR, DS	: Common signal control F/F
CG	: Clock generator
DIV	: Divider
D, E, H, L	: General-purpose registers
HC	: Common signal circuit
IE	: Interrupt enable F/F
IFA, IFB	: Interrupt requests
IFS, IFT, IFV	
IME	: Interrupt master enable F/F
P1-P3	: Registers
PL, PU	: Program counters
PSW	: Program status word register
R4-R7	: General-purpose registers
RD, RE, RF	: Mode registers
SB	: Shift register
SP	: Stack pointer
TC	: Count register
TM	: Modulo register
Φ	: Carrier contlol circuit

PIN DESCRIPTION

SYMBOL	I/O	CIRCUIT TYPE	FUNCTION
$P0_0$-$P0_3$	I	Pull up	Acc ← $P0_0$-$P0_3$
$P1_0$-$P1_3$	I/O	Pull up	I/O selectable by instructions
$P2_0$-$P2_3$	I/O	Pull up	I/O selectable independently Sound output only when $P2_3$ pin is used as an output
$P3_0$-$P3_3$	I/O	Pull up	Serial interface I/O by setting the mode register RE
S_0-S_{15}	O or I/O		Selectable between segment ports and I/O ports through an RC register
S_{16}-S_{63}	O		Display RAM contents output as LCD segment signals
H_1-H_4	O		4-value output capability; used for LCD common output
TEST	I	Pull down	For test (connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
ϕ	O		System clock output
Φ_{OUT}	O		Carrier output pin for remote control
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DSP}, V_{OA}, V_{OB}			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	−0.3 to +7	V	1
	V_{DSP}	−0.3 to +7	V	
Input voltage	V_{IN}	−0.3 to V_{DD} +0.3	V	1
Output voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V	1
Output current	I_{OUT}	20	mA	2
Operating temperature	T_{OPR}	−20 to +70	°C	
Storage temperature	T_{STG}	−55 to +150	°C	

NOTES :

1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

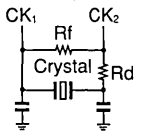
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}		2.4		5.5	V	
	V_{DSP}		2.4		V_{DD}	V	
Basic oscillation frequency	f			455		kHz	
Instruction cycle	t			8.79		µs	
Crystal oscillation frequency	f_{OSC}			32.768		kHz	1

NOTE :

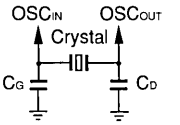
1. Starting condition : within 10 seconds after power on.

Oscillation Circuit



Oscillator circuit 1
C1 = 470 pF, C2 = 470 pF
Rf = 1 MΩ
Rd = 1 kΩ
Oscillator : KBR-455B (Kyocera)

Oscillator circuit 2
C1 = 330 pF, C2 = 330 pF
Rf = 1 MΩ
Rd = 1.5 kΩ
Oscillator : CSB455E (Murata)



CG = 33 pF, CD = 22 pF

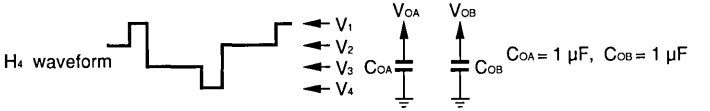
DC CHARACTERISTICS

(VDD = 2.4 to 5.5 V, Ta = –20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}		0.7 x V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.3 x V_{DD}	V	
	V_{IH2}		V_{DD}–0.5		V_{DD}	V	2
	V_{IL2}		0		0.5	V	
Input current	I_{IH}	V_{IN} = 0 V	2		200	µA	1
Output current	I_{OH1}	V_{OH} = V_{DD}–0.5 V	50			µA	3
	I_{OL1}	V_{OL} = 0.5 V	250			µA	
	I_{OH2}	V_{OH} = V_{DD}–0.5 V	50			µA	4
	I_{OH2D}	V_{OH} = V_{DD}–0.5 V	160			µA	5
	I_{OL2}	V_{OL} = 0.5 V	500			µA	6
	I_{OH3}	V_{OH} =V_{DD}–0.5 V	20			µA	7
	I_{OH3D}	V_{OH} =V_{DD}–0.5 V	90			µA	8
	I_{OL3}	V_{OL} = 0.5 V	0.2			mA	7
Output impedance	R_C			5	20	kΩ	9
	R_S			10	40	kΩ	10
Output voltage	V_1	V_{DSP} = 3.0 V No load	2.7		3	V	11
	V_2		1.7	2	2.3	V	
	V_3		0.7	1	1.3	V	
	V_4		0		0.3	V	
Supply current	I_{OP}	f = 455 kHz, V_{DD} = 3.0 V		160	320	µA	12
	I_{SB}	Standby current V_{DSP} = 3.0 V		15	40		13
		Standby current V_{DD} = 3.0 V		8	20		14

NOTES :

1. Applied to pins $P0_0$-$P0_3$, $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_2$ (during input mode).
2. Applied to pins CK_1, TEST, OSC_{IN}.
3. Applied to pin CK_2.
4. Applied to pins $P1_0$-$P1_3$, $P2_0$-$P2_2$, $P3_0$-$P3_2$ (during output mode).
5. Applied to pins $P2_3$, Φ_{OUT} (during output mode).
6. Applied to pins $P1_0$-$P1_3$, $P2_0$-$P2_2$, $P3_0$-$P3_2$, Φ_{OUT} (during output mode).
7. Applied to pins S_0-S_{15} (during data output mode).
8. Pins cited in NOTE 7 are applicable with mask option used.
9. Applied to pins H_1-H_4.
10. Applied to pins S_0-S_{63} (during LCD output mode).
11. Applied to pins H_1-H_4, S_0-S_{63} (during LCD output mode).
12. No load condition.
13. No load condition when bleeder resistance is ON, V_{DSP} = 3.0 V, during 32.768 kHz crystal oscillation.
14. No load condition when bleeder resistance is OFF, during 32.768 kHz crystal oscillation.



COA = 1 µF, COB = 1 µF

PIN FUNCTIONS

• GND, V_{DD}, V_{DSP} (Power supply inputs)

Both GND pins 40 and 90 should be grounded.

The V_{DD} pin is the positive power supply with respect to GND.

The V_{DSP} pin is the positive power supply for an LCD driver with respect to GND.

• TEST (Test input)

The TEST pin should be left open or connected to GND with a pull-down resistor.

• $\overline{\text{RESET}}$ (Input)

The $\overline{\text{RESET}}$ accepts an active Low system reset which initializes the internal logic of the device.

Normally a capacitor of about 0.1 µF is connected between this pin and GND to provide a power on reset function.

• OSC_{IN}, OSC_{OUT} (Crystal oscillator pins)

The OSC_{IN} and OSC_{OUT} pins connect with an external crystal oscillator and these pins and the GND connect with a capacitor, which constitute an oscillator circuit.

The output of the oscillator is coupled to a clock divider for real-time clock operation.

• CK_1, CK_2 (System clock oscillator pins)

The CK_1 and CK_2 pins provide a system clock oscillator.

• H_1 to H_4 (Common signal outputs)

The H_1 to H_4 pins are used to drive the common of an LCD.

• S_0 to S_{63} (Segment outputs)

The S_0 to S_{63} pins drive LCD segments. Pins S_0 through S_{15} may also be used as I/O ports when specified with the mode register RC.

• $P0_0$ to $P0_3$ (Inputs)

The P0 pins are normally used to accept key input data. A falling edge at these pins resets the IFB flag.

• $P1_0$ to $P1_3$ (Input/output)

The P1 are I/O pins connected to the positive supply with pull-up resistors.

They may be switched between input and output modes through an instruction.

• $P2_0$ to $P2_3$ (Input/output)

The $P2_0$ to $P2_3$ pins are bit-independent I/O ports which can be independently set to input or output mode with the mode register RF.

When the $P2_3$ is used for an output pin, it serves exclusively as a sound output pin, which can output a sound signal with any frequency set up by the timer counter.

Pins $P2_0$ and $P2_1$ output the OD and R/W signals with the mode register RC.

• $P3_0$ to $P3_2$ (Input/output)

The $P3_0$ to $P3_2$ pins are I/O pins which are connected to the positive supply with pull-up resistors.

These pins can be set to I/O mode for use in a serial interface with the mode register RE.

• Φ_{OUT} (Carrier output pin for remote control)

A carrier signal output pin for remote control. It is used to control carrier signal output by setting the bits in the bit 3 of R7 register.

SYSTEM CONFIGURATION

ROM and Program Counter

The on-chip ROM has a configuration of 128-page x 64-step x 8-bit, and stores programs and table data.

The program counter consists of a 7-bit page address counter P_U and a 6-bit binary counter P_L used to specify the steps within a page.

The locations shown in Fig. 1 are allocated in the on-chip ROM.

Stack Pointer (SP)

The stack pointer (SP) is an 8-bit shift register which holds the starting address of the stack area of RAM space. Immediately after the reset, the contents of the stack pointer are uninitialized and must be set to an appropriate value. If, for instance, the initial value of the stack pointer is set to 80_H, the data memory are beginning with the highest address (excluding the display RAM area) $7F_H$, is usable as a stack area.

RAM

Data memory has a 256-word x 4-bit configuration, and is used to store processing data and other information. Data memory is also used as a stack area to save register values, the program counter value, and program status word (PSW) at the time a subroutine jump or an interrupt occurs. Fig. 2 shows the RAM configuration. 64 x 4-bit of entire RAM space is used as a display RAM area from which data is output to LCD segment driving pins. An LCD with a 1/4 duty and 1/3 bias format can be directly driven by writing display data into the display RAM area. The display RAM outputs are, as shown in Fig.3, connected to segment output pins S_0 to S_{63} for individual set of common outputs H_1 to H_4. The segment output pins provide a single digit of display RAM data M_0 to M_3, as an LCD driving waveform signal according to H_1 to H_4 outputs. The operations of the display RAM are identical to those of other RAM areas.

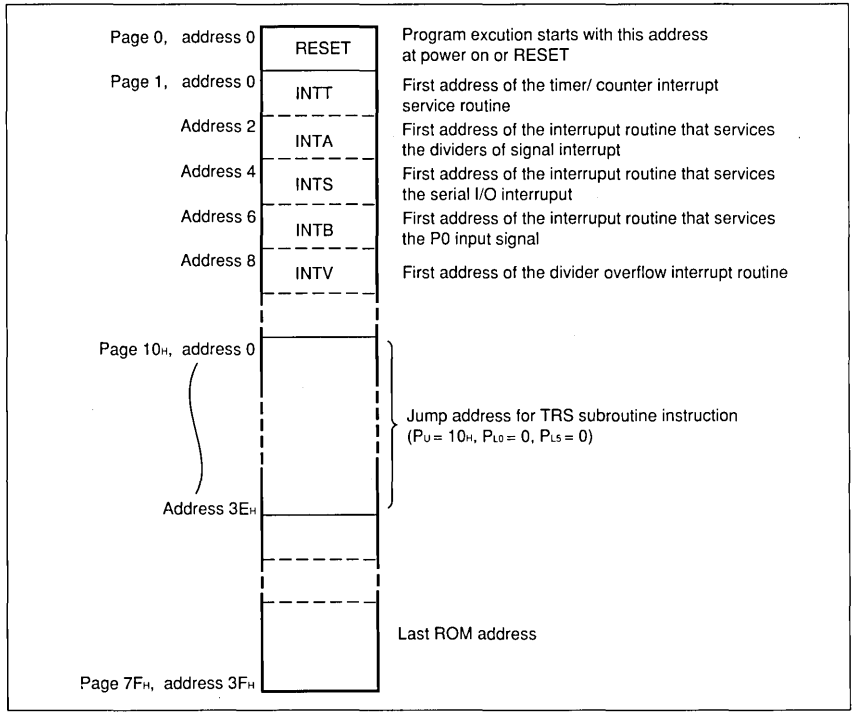


Fig. 1 Program ROM Map

Higher address H / Lower address L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0													S_0	S_{16}	S_{32}	S_{48}
1													S_1	S_{17}	S_{33}	S_{49}
2													S_2	S_{18}	S_{34}	S_{50}
3													S_3	S_{19}	S_{35}	S_{51}
4													S_4	S_{20}	S_{36}	S_{52}
5													S_5	S_{21}	S_{37}	S_{53}
6													S_6	S_{22}	S_{38}	S_{54}
7													S_7	S_{23}	S_{39}	S_{55}
8													S_8	S_{24}	S_{40}	S_{56}
9													S_9	S_{25}	S_{41}	S_{57}
A													S_{10}	S_{26}	S_{42}	S_{58}
B													S_{11}	S_{27}	S_{43}	S_{59}
C													S_{12}	S_{28}	S_{44}	S_{60}
D													S_{13}	S_{29}	S_{45}	S_{61}
E													S_{14}	S_{30}	S_{46}	S_{62}
F													S_{15}	S_{31}	S_{47}	S_{63}

NOTE :

The area with the thick line is allocated for a display RAM and the Sn (n = 0 to 63) shows the related segment outputs.

Fig. 2 RAM Configuration

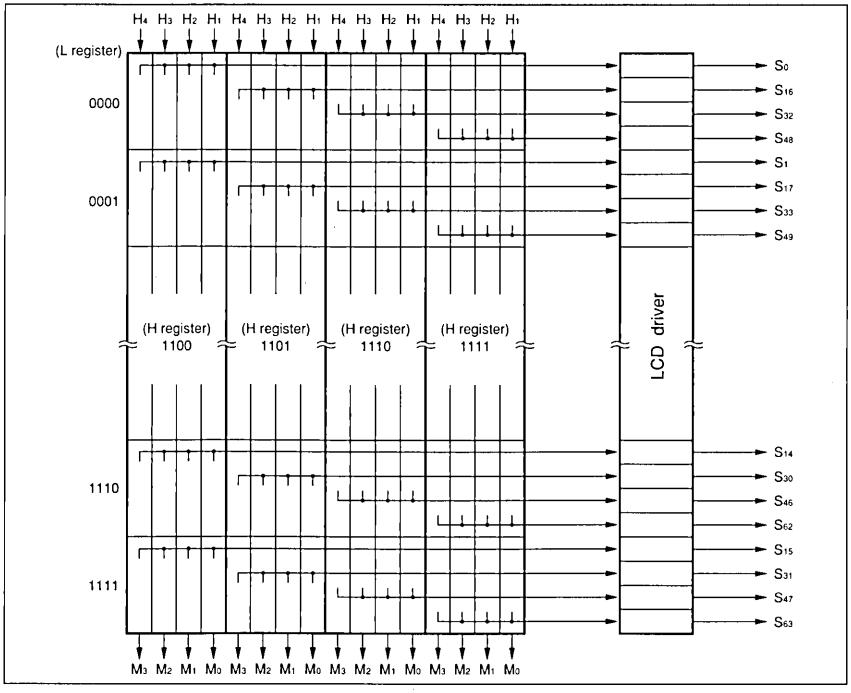


Fig. 3 Display RAM and its LCD Segment Outputs

Accumulator (A), Subaccumulator (B) and Arithmetic and Logic Unit (ALU)

The accumulator (A) is a 4-bit working register which is the nucleus of the single chip system. It holds the results of operations and transfers data to memory, I/O ports, and registers.

A subaccumulator (B) is another 4-bit register. It is used as one of general-purpose registers, and when combined with the A to form a B-A register pair, allows data transfer on an 8-bit basis.

The arithmetic and logic unit (ALU) performs, in conjunction with a carry flag (C), binary addition, shift operations, and logical operations such as AND, OR, EX-OR, and complement.

General-Purpose Registers (H, L, D, E)

Registers H and L are 4-bit general-purpose registers. They can transfer and compare data with the Acc on 4-bit basis. Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis.

The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations.

The L register can be incremented or decremented and is used to access I/O ports and mode registers.

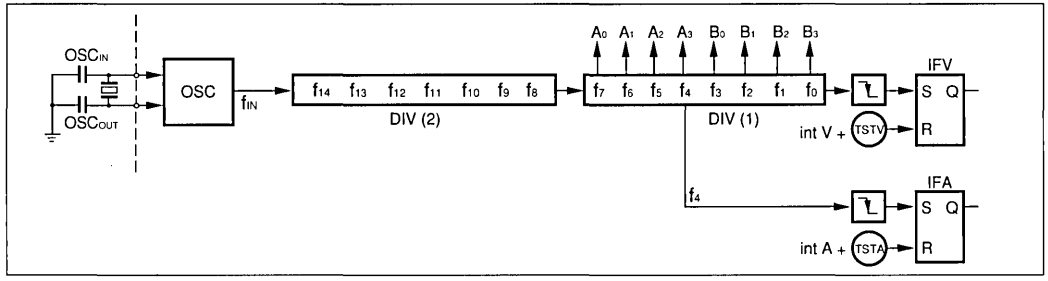


Fig. 4 Real-Time Clock and Divider

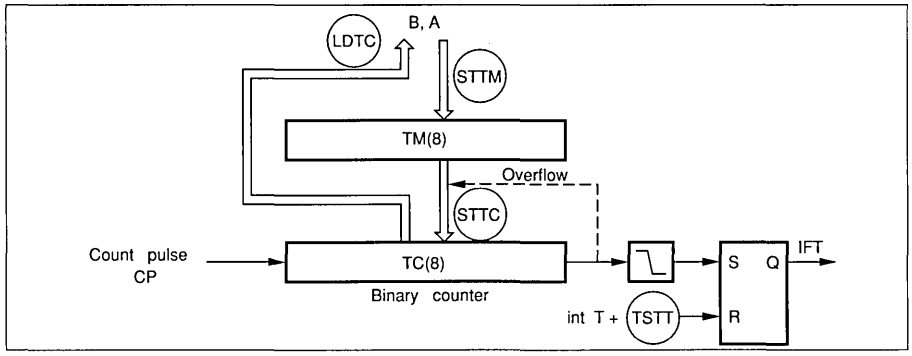


Fig. 5 Timer/Counter

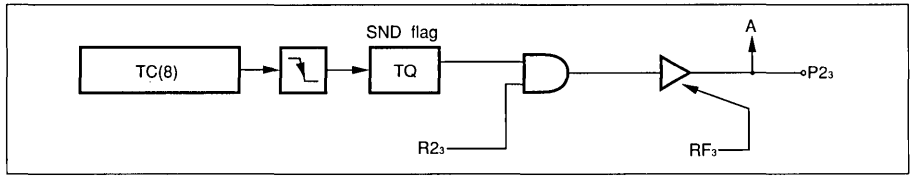


Fig. 6 SND Signal

Clock Divider, IFV Flag, IFA Flag

The device contains a crystal oscillator and a 15-stage divider, as shown in Fig. 4. A real-time clock can be provided by connecting an external crystal oscillator between the oscillator pins. When an external 32.768 kHz crystal oscillator is used, the f_0 signal is set at a frequency of 1 Hz.

Timer/Counter and the SND Signal

The timer/counter consists of an 8-bit count register (TC) and an 8-bit mudulo register (TM).

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register (See Fig. 5).

The count pulse CP can be selected from divider signals f_{IN}, f_0 and the system clock, by using the mode register RD. If the count register (TC) overflows, the SND flag reverses its status at the falling edge of the TC. A sound signal can be obtained at the TC output by putting P2 in output mode and sending a "1" to pin $P2_3$ (See Fig. 6).

Serial Interface and IFS

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data.The serial clock can be selected with either an internal clock (system clock) or an external clock.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin, and the data input from the SI pin at the rising edge of a serial clock is loaded into the lowest bit of the shift register. When the internal clock is used, immediately after the SIO instruction is executed, the serial operation begins and stops with 8- clock which are output from the SCK pin. Upon completion of an 8-bit shift operation, the serial I/O ending flag IFS is set each time a 3-bit counter overflows, and an interrupt request occurs.

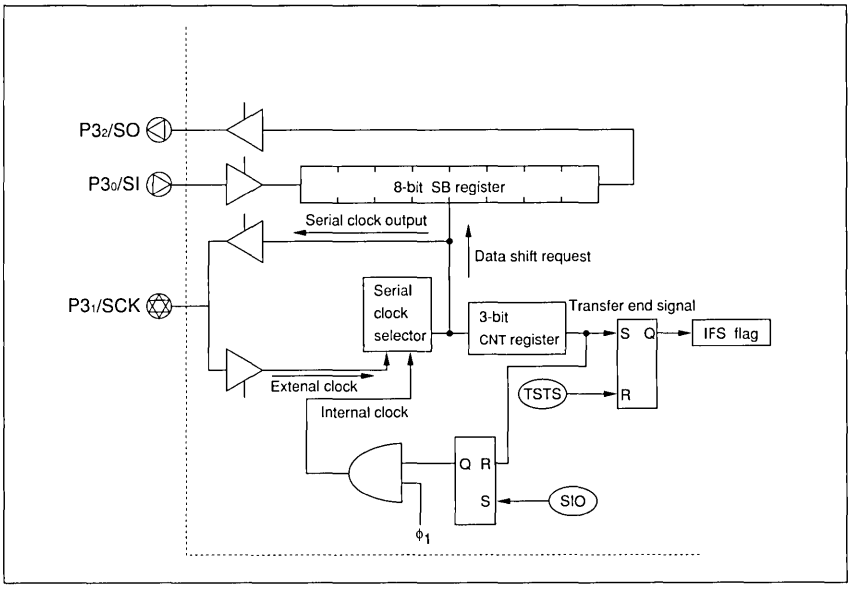
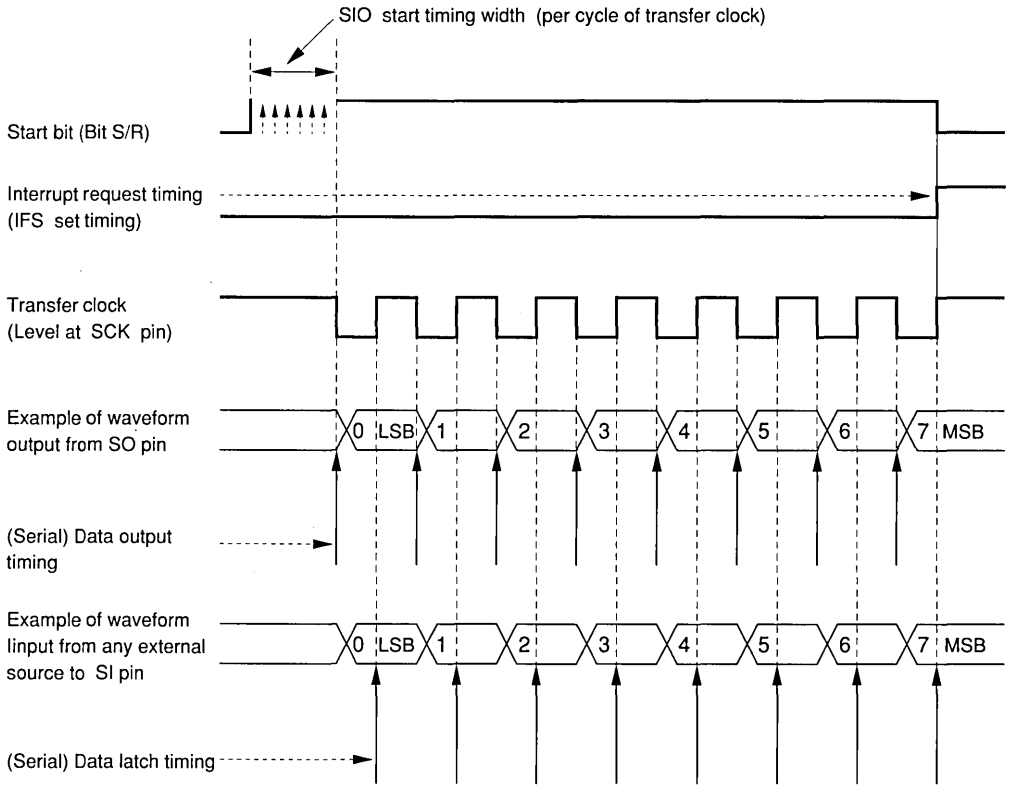


Fig. 7 Serial Interface



Data output timing

Data output timing is timing to output the contents of SB register bit to SO pin any user needs to decide timing latch the SO pin level at the outside of SM565 according to the SCK pin clock.

Data latch timing

Data latch timing is timing that SM565 latches the SI pin level and stores it to SB register.
Any user needs to decide timing to SI pin according to the SCK pin clock.

Fig. 8 Serial Interface Timing

Input Port P0 and IFB Flag

The IFB flag is set at the falling edge of the signal applied to the input port P0 by which the interrupt is enabled.

When port P0 is used as a key input, it can cause an interrupt each time a key is operated.

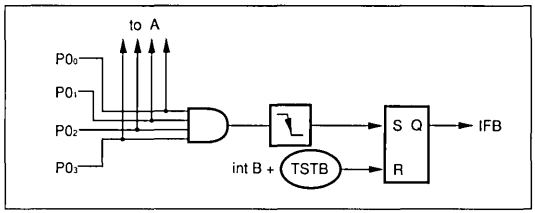


Fig. 9 P0 Port

Interrupts

When an interrupt occurs, the corresponding interrupt request flag is set. The CPU acknowledges the interrupt if it is enabled (master interrupt enable flag and the corresponding interrupt enable flag are set). If more than one interrupt occurs simultaneously, all of the corresponding interrupt request flags will be set, but the CPU will only acknowledge that interrupt with the highest priority and other interrupts will be queued.

I/O Ports

Port P0 is a 4-bit parallel input port. The IFB flag is set at the falling edge of this port.

Port P1 can be switched between input and output modes, 4-bit at a time.

Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.

Ports $P2_0$ and $P2_1$ can output the OD and R/W signals, respectively. In those cases, these pins should be kept High in an output mode. Port $P2_3$ outputs the SND signal in the output mode.

Port P3 is a 4-bit I/O port which can be placed in input or output mode, 3-bit at a time. Each bit of port P3 can be set to the I/O modes (SI, SO, SCK) of a serial interface.

Ports P1 and P3 are placed in an output mode when a port output instruction is executed, and in an input mode when a port input instruction is executed. After an ACL operation, ports P1, P2 and P3 are all placed in an input mode.

Every input port has pull-up resistors. (Pull-up resistors for I/O ports are effective only when the ports are placed in an input mode.)

Ports P1 through P3 in an output mode can be independently set or reset by instructions.

When a key-matrix is configured by using I/O ports, if the short on output pins may occur caused by a multiple key depression, port P1 should be used as an output.

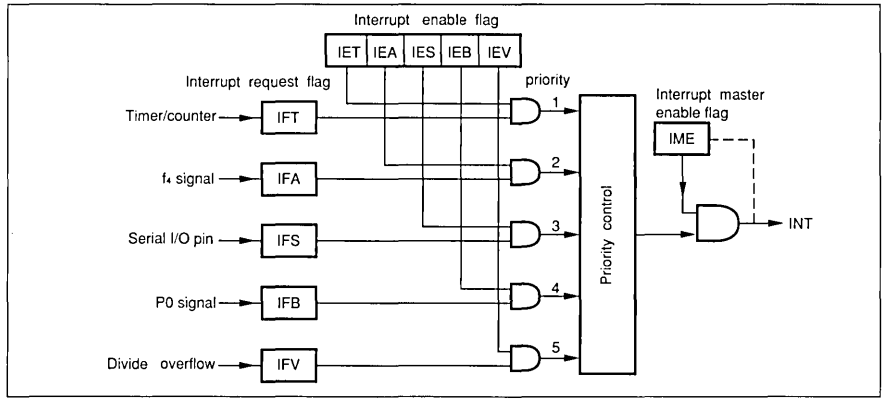


Fig. 10 Interrupt Handling

Table 1 Characteristics of I/O Ports and Registers

PORT	FUNCTION	Direct 4-bit parallel I/O		IN, OUT instruction		Bit independent SPn output
		Input (INA)	Output (OUTA)	Input (IN)	Output (OUT)	Direct pin-indepedent output RPn
P0	Input-only port	O	X	O	X	X
P1	I/O port	O	O	X	O	O
P2	I/O port, P_{23}-sound output	O	O	X	X	O
P3	$P3_0$-SI, $P3_1$-SCK, $P3_2$-SO, multi-control port	O	O	X	X	O

O : Yes, X : No

Standby Mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated. Standby mode may be cleared with the interrupt request or the RESET signal.

Reset Function (ACL)

Applying a Low level signal to the $\overline{\text{RESET}}$ pin resets the internal logic of the device and applying a High level signal starts execution of the program at address 0, page 0. Once the device is reset, all I/O ports are placed in input mode, all interrupts are disabled, and the LCD display turns off. The device is also reset when it is powered up.

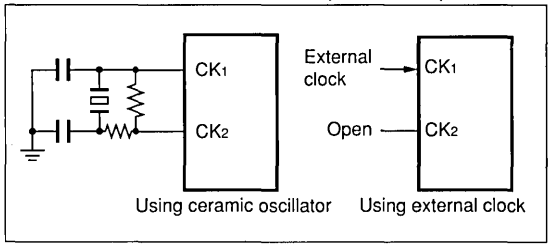


Fig. 11 CK_2 Main Clock Sources

Main Clock Oscillator Circuit

The main clock oscillator requires an external resistor across pins CK_1 and CK_2. Instead of using on-chip oscillator, an external clock may be applied to pin CK_1. In this case, pin CK_2 should be left open. The system clock ϕ is a divided clock equivalent to 1/4 of the clock applied to pin CK_1.

LCD Driver

• Display segment

The SM565 contains an on-chip LCD driver which can directly drive an LCD with a 1/4 duty and 1/3 bias. Fig.12 shows an example of LCD segment configuration for 1/4 duty.

Each segment of the LCD can be turned on or off by software control of the setting of the corresponding bit "1" or "0" in the display RAM area (see Fig. 3).

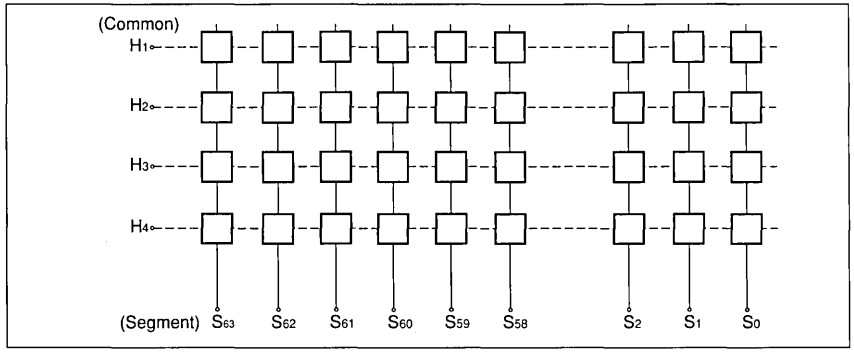


Fig. 12 LCD Segment Configuration for 1/4 Duty

The LCD digit may have any shape, provided that the maximum number of segments does not exceed 256 (see Fig. 12). Fig. 13 shows an example of a 7-segment numeric LCD digit.

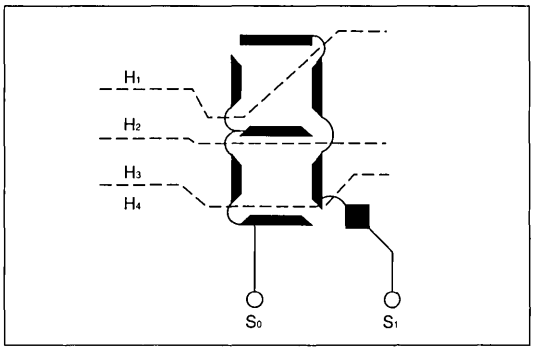


Fig. 13 7-Segment Numeric LCD Digit

• LCD driving signal waveform

Fig. 14 shows the LCD signal driving waveforms required to display the number "5" on the 7-segment display shown in Fig. 13 (segment outputs S_0 and S_1 are used). A voltage of 3 V is applied to pin V_{DSP} in the Fig. 14. The frame frequency (I/T) can be selected from 64 Hz or 128 Hz by mask options.

• V_{OA} and V_{OB} pins

The device contains bleeder resistors to allow 1/3 bias driving. When V_{DSP} is 3 V, voltages of 2 V and 1 V are output from pins V_{OA} and V_{OB} respectively. Normally pins V_{OA} and V_{OB} are left open. When an LCD with a large display area is driven, connect capacitors across pins V_{OA} and V_{DSP} and across V_{OB} and V_{DSP} to improve the rise time of the LCD driving signal.

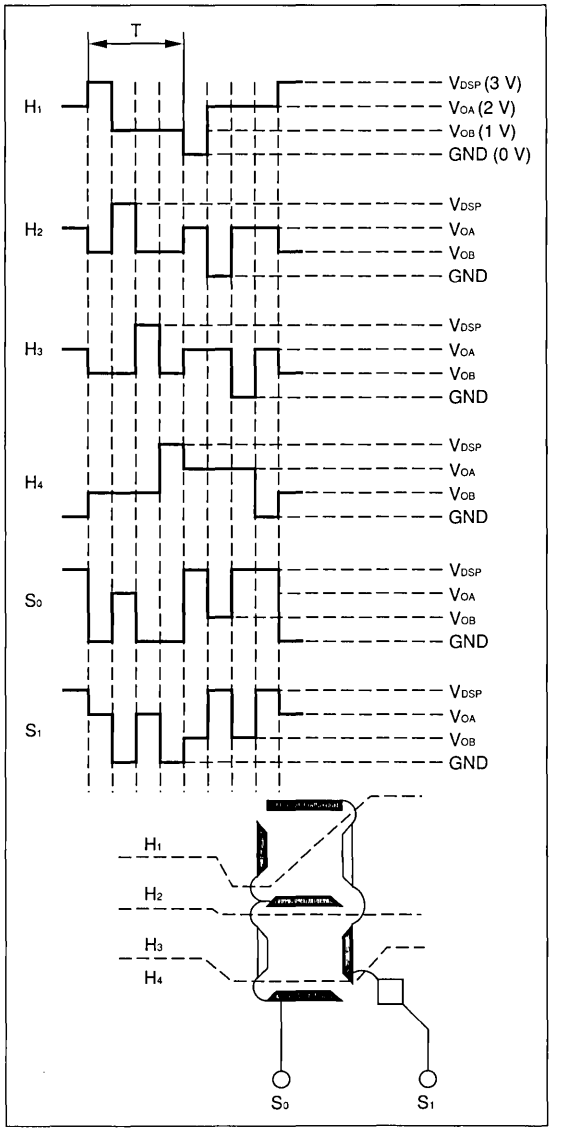


Fig. 14 LCD Driving Signal Waveform (required to display the number 5)

Remote Control Carrier Output Function

SM565 has a carrier output function for remote control output.

A carrier is output from Φ_{OUT}, and controlled using the register R73. Setting "0" in the bit of R73 causes the output from Φ_{OUT} to be set to constant and High output. If "1" is set, a carrier, which is a remote control signal, is output. If "0" is set in the bit of R73,the output level is set to constant and High as stated above. However, it can be set to the constant Low level using the mask option.

Either 1/2 or 1/3 can be selected as the duty of the carrier. (See Table 2 and Fig. 15.)

The frequency of the carrier is approximately 37.9 kHz (1/2 duty or 1/3duty) when the basic oscillation frequency (main clock) is 455 kHz.

Table 2 Mask Option for Φ_{OUT} pin Output

SELECTION OF PLA		Φ_{OUT} OUTPUT	
PLA1	PLA2	Output waveform	When remote control signal is not output :
1	1	A	Constant Low output
2	1	B	Constant Low output
1	2	$\bar{A}$	Constant High output
2	2	$\bar{B}$	Constant High output

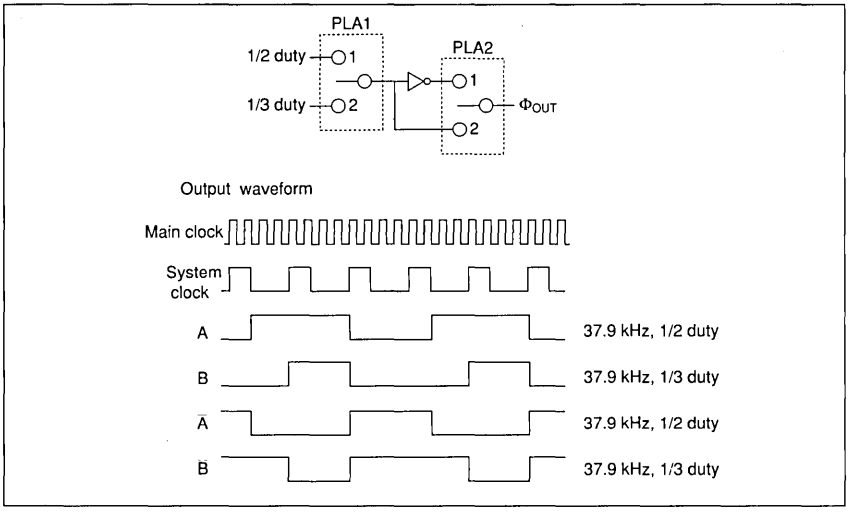


Fig. 15 Mask Option for Φ_{OUT} Output

Fig. 16 shows an example of a circuit that converts remote control carrier signal from the Φ_{OUT} pin into infrared signal.

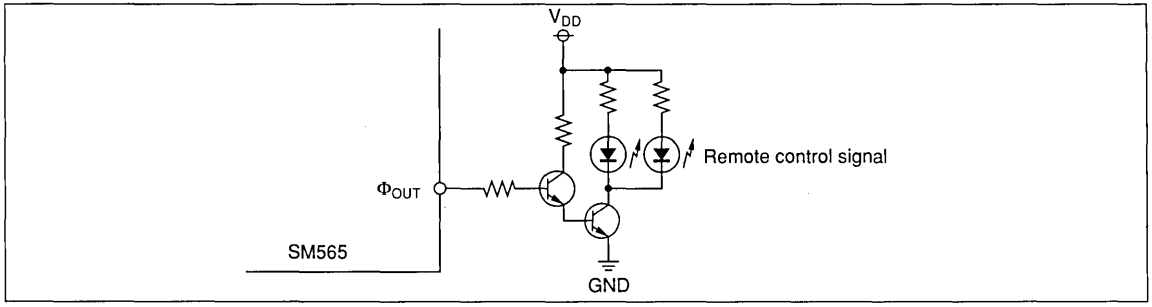


Fig. 16 Remote Control Signal Output Circuit

INSTRUCTION SET

ROM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy (2-byte)	C0 to DF 00 to FF	$P_U \leftarrow x$ (I_{12}-I_6) $P_L \leftarrow y$ (I_5-I_0)
TRS x	E0 to EF	(SP–1)–(SP–4)←PC SP←SP–4 $P_U \leftarrow 10_H$ $P_L \leftarrow x$ (0,I_3,I_2,I_1,I_0,O)
CALL xy (2-byte)	F0 to FF 00 to FF	(SP–1)–(SP–4)←PC SP←SP–4, $P_U \leftarrow x$ (I_{11}-I_6), $P_L \leftarrow y$ (I_5-I_0)
JBA x (2-byte)	7F 20 to 3F	P_{U5}-$P_{U2} \leftarrow x$ (I_3-I_0), P_{U1}, P_{U0}, P_{L5}, $P_{L4} \leftarrow$ B, P_{L3}-$P_{L0} \leftarrow$ A
RTN	61	P_U, $P_L \leftarrow$ (SP), (SP+1),(SP+2)
RTNS	62	P_U, $P_L \leftarrow$ (SP), (SP+1),(SP+2) SP←SP+4
RTNI	63	P_U, $P_L \leftarrow$ (SP), (SP+1),(SP+2) PSW←(SP+3), SP←SP+4, IME←1

RAM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
STL	69	L←A
STH	68	H←A
EXHD	3F	H↔D L↔E
LIHL xy (2-byte)	3D 00 to FF	H←x (I_7-I_4), L←y (I_3-I_0)

Data Transfer Instructions

MNEMONIC	MACHINE CODE	OPERATION
EX pr	5C to 5F	A↔(pr)
LDX adr (2-byte)	7D 00 to FF	A←(adr)
STX adr (2-byte)	7E 00 to FF	(adr)←A
EXX adr (2-byte)	7C 00 to FF	A↔(adr)
LAX x	10 to 1F	A←x (I_3-I_0)
LIBA xy (2-byte)	3C 00 to FF	B←x (I_7-I_4) A←y (I_3-I_0)
LBAT	60	B←ROM (P_{U5}-P_{U2}, B, A)$_H$ A←ROM (P_{U5}-P_{U2}, B, A)$_L$
LDL	65	A←L
LD pr	54 to 57	A←(pr)
ST pr	58 to 5B	(pr)←A
EXH	6C	A↔H
EXL	6D	A↔L
EXB	6E	A↔B
STB	6A	B←A
LDB	66	A←B
LDH	64	A←H
PSHBA	28	(SP–1)←B, (SP–2)←A, SP←SP–2
PSHHL	29	(SP–1)←H, (SP–2)←L, SP←SP–2
POPBA	38	B←(SP+1), A←(SP), SP←SP+2
POPHL	39	H←(SP+1), L←(SP), SP←SP+2
STSB	70	$SB_H \leftarrow$B, $SB_L \leftarrow$A
STSP	71	$SP_H \leftarrow$B, $SP_L \leftarrow$A
STTC	72	TC←TM
STTM	73	$TM_H \leftarrow$B, $TM_L \leftarrow$A
LDSB	74	B←SB_H, A←SB_L
LDSP	75	B←SP_H, A←SP_L
LDTC	76	B←TC_H, A←TC_L
LDDIV	77	B←DIV_H, A←DIV_L

Arithmetic Instructions

MNEMONIC	MACHINE CODE	OPERATION
ADX x	00 to 0F	A←A+x (I_3-I_0), Skip if C_Y = 1
ADD	36	A←A+(HL)
ADDC	37	A←A+(HL)+C, C←C_Y Skip if CY = 1
OR	31	A←A ∪ (HL)
AND	32	A←A ∩ (HL)
EOR	33	A←A ⊕ (HL)
ANDB	22	A←A ∩ B
ORB	21	A←A ∪ B
EORB	23	A←A ⊕ B
COMA	6F	A←$\bar{A}$
ROTR	25	C→A_3→A_2→A_1→A_0→C
ROTL	35	C←A_3←A_2←A_1←A_0←C
INCB	52	B←B+1, Skip if B = F_H
DECB	53	B←B–1, Skip if B = 0
INCL	50	L←L+1, Skip if L = F_H
DECL	51	L←L–1, Skip if L = 0
DECM adr	79 00 to FF	(adr)←(adr)–1, Skip if (adr) = 0
INCM adr	78 00 to FF	(adr)←(adr)+1, Skip if (adr) = F_H

Test Instructions

MNEMONIC	MACHINE CODE	OPERATION
TAM	30	Skip if A = (HL)
TAH	24	Skip if A = H
TAL	34	Skip if A = L
TAB	20	Skip if A = B
TC	2A	Skip if C = 0
TM x	48 to 4B	Skip if (HL), x = 1
TA x	4C to 4F	Skip if Ax = 1
TSTT	2B	Skip if IFT = 1, IFT←0
TSTA	2C	Skip if IFA = 1, IFA←0
TSTS	2D	Skip if IFS = 1, IFS←0
TSTB	2E	Skip if IFB = 1, IFB←0
TSTV	2F	Skip if IFV = 1, IFV←0

Bit Manipulation Instructions

MNEMONIC	MACHINE CODE	OPERATION
SM x	40 to 43	(HL) x←1
RM x	44 to 47	(HL) x←0
RC	26	C←0
SC	27	C←1
RIME	3A	IME←0
SIME	3B	IME←1
DI x (2-byte)	7F C0 to DF	IEF←IEF ∩ x
EI x (2-byte)	7F E0 to FF	IEF ∪ x

I/O Instructions

MNEMONIC	MACHINE CODE	OPERATION
IN	67	A←P0
OUT	6B	P1←A
INA x (2-byte)	7F A0 to A9	A←P (x), R (x)
OUTA x (2-byte)	7F B0 to BF	P (x), R (x)←A
INBA x	7F 80 to 81	B←R (x+1) A←R (x)
OUTBA x (2-byte)	7F 90 to 91	R (x+1)←B R (x)←A
SP xy (2-byte)	7A 00 to F3	P (y)←P (y) x
BP xy (2-byte)	7B 00 to F3	P (y)←P (y) x
RDS (2-byte)	7F 60	DS←0
RBR (2-byte)	7F 70	BR←0
SDS (2-byte)	7F 61	DS←1
SBR (2-byte)	7F 71	BR←0
READ (2-byte)	7F 62	A←P4 with OD
WRIT (2-byte)	7F 72	P4←A with R/W
READB (2-byte)	7F 63	A←P4, with OD B←P5
WRITB (2-byte)	7F 73	P4←A, with R/W P5←B

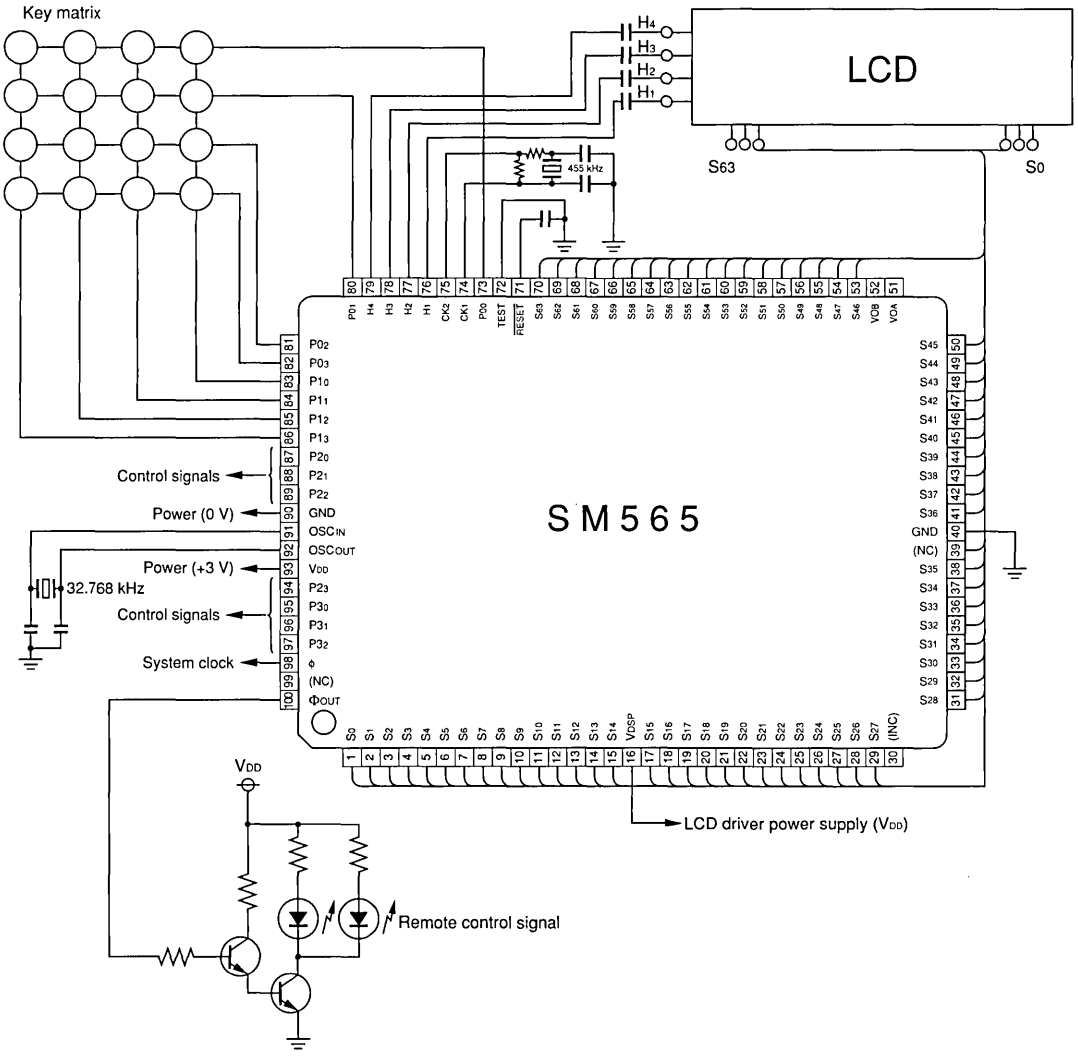
Special Instructions

MNEMONIC	MACHINE CODE	OPERATION
SIO	3E	Serial I/O start
IDIV (2-byte)	7F 10	DIV←0
SKIP	00	No operation
CEND (2-byte)	7F 00	System clock stop

NOTE :

The machine code consists of 8-bit of I_7, I_6, I_5, I_4, I_3, I_2, I_1 and I_0.

SYSTEM CONFIGURATION EXAMPLE



SM3903

4-Bit Single-Chip Microcomputer (For Remote Control)

DESCRIPTION

The SM3903 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, carrier output circuit for remote control, ROM, RAM, 15-stage divider. Provided with 132 segments LCD drive circuit, this microcomputer is applicable to remote control system with a Low power consumption.

FEATURES

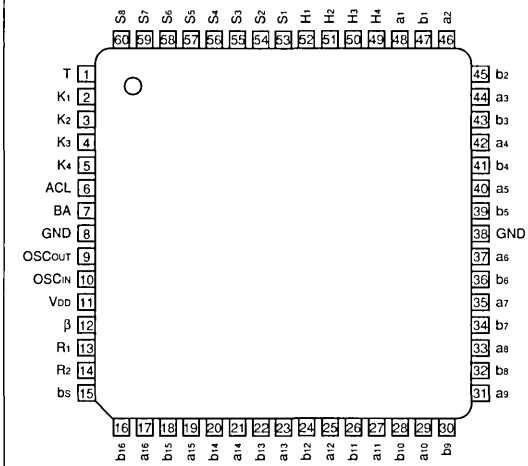
- ROM capacity : 2 772 x 8 bits
- RAM capacity : 128 x 4 bits (including 32 x 4 bits display RAM)
- Instruction sets : 49
- Subroutine nesting : 2 levels
- I/O Port :
  - Input 6
  - Output 10
  - 33 (Used as LCD segment output port)
  - 4 (Used as LCD common output port)
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider circuit for real time clock
- Built-in carrier output circuit for remote control
- Built-in LCD driver : 132 segments (1/3 bias, 1/4 duty cycle)
- Built-in carrier output circuit for remote control

Carrier frequency	32.768 kHz
Bacic oscillation frequency (main clock)	32.768 kHz
Duty cycle	1/2

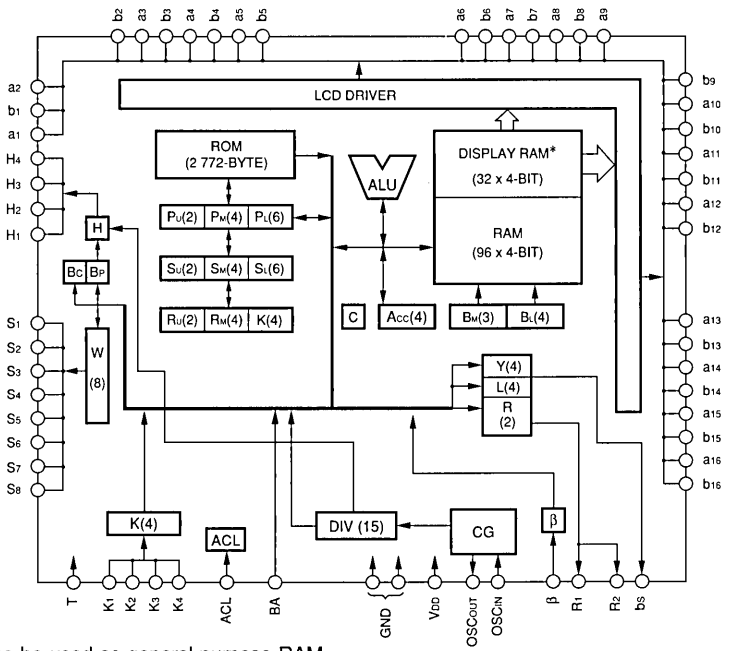
- Instruction cycle time : 61 µs (TYP., 32.768 kHz, at –3 V)
- Standby function
- Supply voltage : –2.6 to –3.2 V
- Package : 60-pin QFP(QFP060-P-1414)

PIN CONNECTIONS

60-PIN QFP TOP VIEW



BLOCK DIAGRAM



* Display RAM can also be used as general purpose RAM.

Nomenclature

ALU	: Arithmetic logic unit	W	: 8-bit shift register
Acc	: Accumulator	β	: Independent input register
ACL	: Auto clear circuit	B_M, B_L	: RAM address register
C	: Carry F/F	B_P, B_C	: Backplate signal generator circuit
P_U, P_M, P_L	: Program counter	H, L, Y	: 4-bit F/F
S_U, S_M, S_L	: Stack register of program counter	R	: Control register for remote control output
R_U, R_M, R_L	: Stack register of program counter	K	: Key input F/F
DIV	: Divider	CG	: Clock Generator

PIN DESCRIPTION

SYMBOL	I/O	CIRCUIT TYPE	FUNCTION
ai, bi	O		Segment output ports (i = 1 to 16)
b_S			
H_1-H_4	O		Common output ports
S_1-S_8	O		Strobe output ports
T	I		Test input port (normally connected to GND)
K_1-K_4	I	pull-down	Key input ports
OSC_{IN}			Crystal oscillator
OSC_{OUT}			
BA, β	I	pull-up	Independent input ports
GND, V_{DD}			Power supply
R_1, R_2	O		Remote control carrier output
ACL	I	pull-down	Auto clear input port

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	–3.5 to +0.3	V	1
	V_{IN}	V_{DD} to +0.3	V	
Operating temperature	T_{OPR}	0 to +50	°C	
Storage temperature	T_{STG}	–20 to +125	°C	

NOTE :

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	–3.2 to –2.6	V
Crystal oscillation frequency	fosc	32.768 (TYP.)	kHz

DC CHARACTERISTICS

(V_{DD} = –3.2 to –2.9 V, Ta = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}		– 0.6			V	1
	V_{IL1}				V_{DD}+0.6	V	
	V_{IH2}		– 0.3			V	2
	V_{IL2}				V_{DD}+0.3	V	
Input current	I_{IH}	V_{IN} = 0 V			15	µA	3
	I_{IL}	V_{IN} = V_{DD}			15	µA	4
Output voltage	V_{OH}	I_{OUT} = 50 µA to V_{DD}	– 0.5			V	5
	V_{OL}	I_{OUT} = 5 µA to GND			V_{DD}+0.5	V	
	V_{OA}	V_{DD} = –3.0 V No load	– 0.3	0	0	V	6
	V_{OB}		–1.3	–1.0	– 0.7	V	
	V_{OC}		–2.3	–2.0	–1.7	V	
	V_{OD}		–3.0	–3.0	–2.7	V	
Output current	I_{SO}	V_{OUT} = –0.2 V	100			µA	7
	I_{SIN}	V_{OUT} = V_{DD}+0.2 V	100			µA	
Supply current	I_{DA}	During full-range operation		40		µA	8
	I_{DS}	When system clock is stationary		12		µA	

NOTES :

1. Applied to pins K_1-K_4, β.
2. Applied to pins ACL, BA.
3. Applied to pins K_1-K_4.
4. Applied to pin β.
5. Applied to pins S_1-S_8.
6. Applied to pins a_1-a_{16}, b_1-b_{16}, b_5, H_1-H_4.
7. Applied to pins R_1, R_2.
8. No load condition when bleeder resistance is ON.

PIN FUNCTIONS

• K_1 to K_4 (Inputs)

The K_1 to K_4 ports normally pulled down are connected to, and loaded into the accumulator (Acc) by instructions. A matrix composed of K input ports and strobe output ports (S_1 to S_8) enables up to 32-kind of keys to be connected. In this case, be sure to take the interval at least 1 instructon cycle between strobe outputs and K inputs.

• BA, ß (Individual inputs)

The individual input ports BA and β normally pulled up can be tested by using the TAL and TB instructions. Applying a High level to these ports skips the next instruction.

• S_1 to S_8 (Strobe outputs)

The strobe outputs (S_1 to S_8) are used to output an 8-bit W register, and constitute a key input matrix in combination with the input ports K_1 to K_4.

The W register is an 8-bit register transferred by the PTW instruction in parallel. The W register is an 8-bit shift register of which the least significant bit W_1 is set and reset by WS and WR instructions, and the entire contents of W register are shifted by one bit.

• a_1 to a_{16}, b_1 to b_{16}, bs

The segment outputs a_1 to a_{16}, b_1 to b_{16} are connected to the display RAM. By transferring appropriate data to the display RAM, alphanumeric characters are automatically displayed.

The bs is used to output the contents of the L or Y register. Segment output ports are designed to drive an LCD with 1/4 duty cycle. The bs is used to flash the display such as a colon under the control of Y register.

• H_1 to H_4 (Common outputs)

The H_1 to H_4 are used to drive an LCD with 1/4 duty cycle and 1/3 bias, and have the 4-level of output.

The common outputs control the BP F/F, BC F/F to select the display mode or blanking mode.

Below shows the conditions of a display mode to be selected.

BP = 1 and BC = 0

• R (Remote control carrier output)

The R_1 and R_2 output ports are used to carrier output for remote control. The R port can generate the contents of the R register with a mask change, and used as a control signal.

SYSTEM CONFIGURATION

Program Counter and Stack

Program counter consists of a 2-bit register P_U, a 4-bit register R_M and a 6-bit polynomial counter P_L. The P_U and P_M specify the pages and the P_L specifies the steps within a page.

The stack consists of registers S_U, S_M, S_L and R_U, R_M, R_L, and has 2-level of nesting.

Program Memory (ROM)

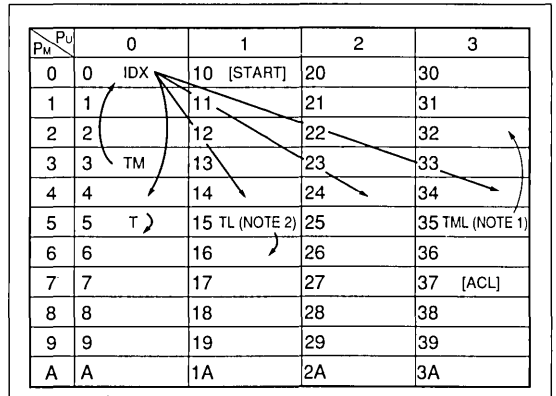
An on-chip 2 772-bit ROM is organized as 44- page x 63-step. Fig. 1 shows the ROM configuration.

- When power on, the program starts execution from the address P_U = 3, P_M = 7, P_L = 0 specified by an ACL circuit.
- When the program starts execution from the system clock halt state by a 1 s signal or a key input signal, the address starts at P_U = 1, P_M = 0, P_L = 0.
- For the instructions except for a jump instruction, the polynomial counter P_L is shifted by 1 step according to a polynomial code.
- The combination of jump instructions including T, TL, TM, TML, RTN0, RTN1 and ATPL enables to jump to any page or any subroutine. Fig. 2 shows the relationship between jump instructions and jump addresses on a ROM map.

P_M \ P_U	0	1	2	3
0	0 Subroutine cover page	10 Start form CEND	20	30
1	1	11	21	31
2	2	12	22	32
3	3	13	23	33
4	4	14	24	34
5	5	15	25	35
6	6	16	26	36
7	7	17	27	37 Power on
8	8	18	28	38
9	9	19	29	39
A	A	1A	2A	3A

* page consists of 63-step.

Fig. 1 ROM Configuraton



NOTES :

1. Jump address of TML, P_M = 0 to 3
2. Jump address of TL, all addresses

Fig. 2 Jump Instruction and Jump Addresser

Data Memory RAM

A 512-bit data RAM consists of 8 x 16 x 4-bit. The RAM is specified by a 3-bit B_M and a 4-bit B_L. The B_M is used to specify the files and the B_L specifies the words. Note that 1 word consists of 4-bit. The SM3903 has 2 x 16 x 4-bit of display RAM area out of the entire RAM, and the display RAM is connected to external pins for segment outputs. Writing data to the display RAM directly drives an LCD with 1/4 duty and 1/3 bias scheme.

B_L \ B_M	X 000	Y 001	Z 010	M 011	P 100	Q 101	R 110	S 111
0000								
0001								
0010								
0011								
0100								
0101								
0110								
0111								
1000								
1001								
1010								
1011								
1100								
1101								
1110								
1111								

The area (R, S) with the thick line is allocated for a display RAM.

Fig. 3 RAM Configuration

Divider Circuit for Clock Function

An internal 15-stage divider circuit is used to make a clock system. The divider outputs the signal at 1 s unit (1 s), and the γ F/F is set at the rising edge of 1 s signal. The γ F/F can be tested by an instruction, and reset by the test. A 1 s count is notified upon execution of this instruction.

Standby Function

The SM3903 is a Low power consumption design due to CMOS process. Further Low power feature can also be obtained by halting almost all the system clocks through the CEND instruction for Low power requirements. The γ F/F must be reset or one or more inputs of K1 to K4 must go High in order to restart the system clock from the halt state. Then the program starts at the ROM address 1000 (P_U = 1, P_M = 0, P_L = 0).

Clock Generator (CG)

The device contains an on-chip crystal oscillator circuit which consists of the external circuit shown in Fig. 4. The system clock has a frequency of one second that of the oscillator frequency.

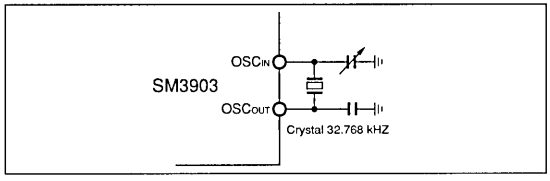


Fig. 4 Oscillation Circuit

ACL Circuit

Resistors and capacitors are mounted in an ACL circuit which does not normally require any external circuits. The ACL will be cleared in about 0.5 s from a crystal oscillator circuit starts oscillation after power on, and the program starts at P_U = 3, P_M = 7, P_L = 0. The ACL operations can be obtained by transferring signals into the ACL pin after power on. Note that it takes about 0.5 s to start execution of the program after the ACL signal is released. In case noise may harm the ACL operation, apply a 0.01 to 0.1 μF of capacitor between ACL pin and GND pin. Fig. 5 shows the sample circuit.

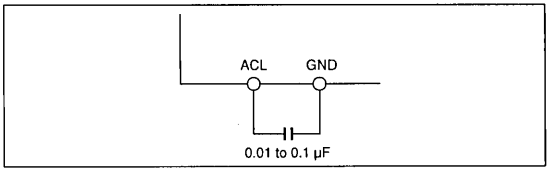


Fig. 5 Compensator for ACL

Remote Control Signal Output (R)

The SM3903 outputs carrier wave for remote control signal. The carrier signal is output from R1 and R2 pins. Those pins are at Low level when not outputting the carrier. Fig. 6 shows external circuit that accepts the remote control signal and the carrier waveform.

The carrier output is controlled by program. Lower 2-bit (bits 0 and 1) of accumulator correspond to bit 1 (pin R1) and bit 2 (pin R2) of the R register. Executing the ATR instruction with a bit of one accumulator set at 1 causes the output of carrier signal through the corresponding R pin.

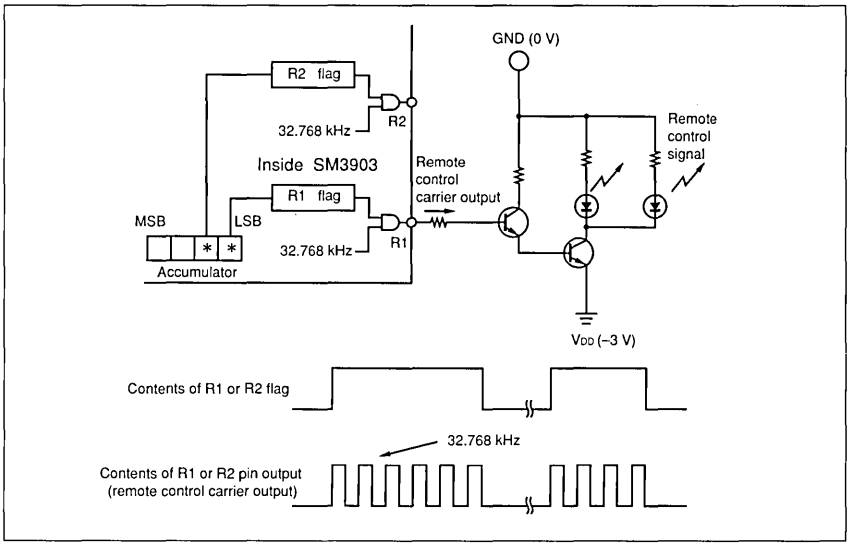


Fig. 6 Remote Control LED Output Circuit

LCD Driver

• LCD segment

The SM3903 has an on-chip LCD driver circuit which can directly drive an LCD with a 3 V, 1/4 duty and 1/3 bias scheme. The display RAM is connected to segment outputs of ai, bi (i = 1 to 16) according to LCD common outputs of H_1 to H_4 as shown in fig 7. The segment outputs provide 1-digit data (M_1 to M_4) of the display RAM in synchronizing with H_1 to H_4 outputs.

Each segment of the LCD can be turned on or off by controlling the corresponding bit data "1" or "0" in the display RAM area.

The LCD driving waveform relative to the display mode is automatically generated. The device provides the maximum of 132-segment. Fig. 7 shows the segment display example.

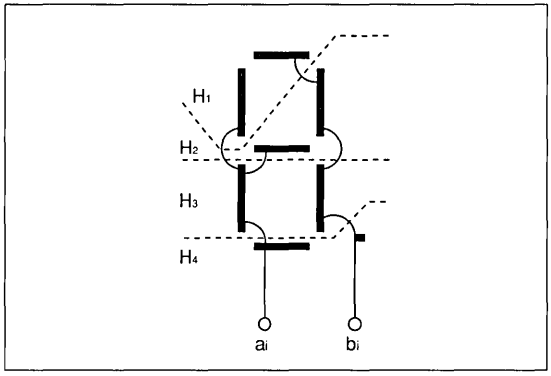


Fig. 7 7-Segment Numeric LCD Digit

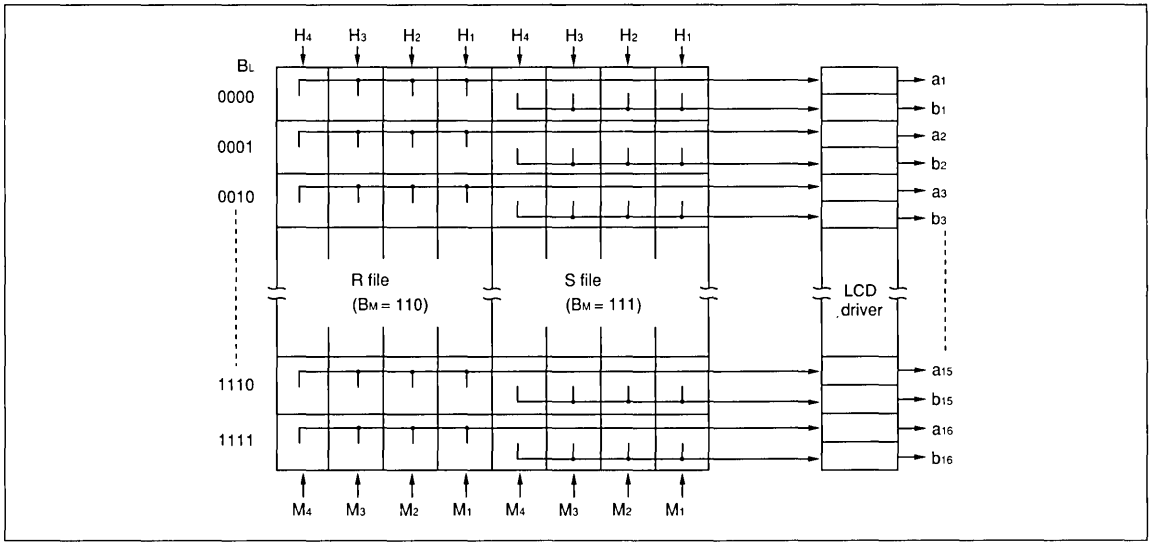


Fig. 8 Display RAM and LCD Segment Output

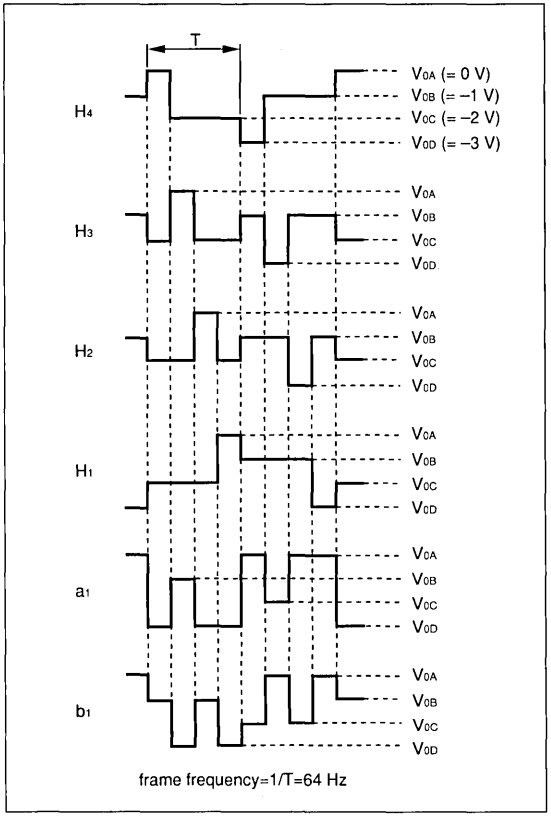


Fig. 9 LCD Driving Signal Waveform

• Display waveform

Fig. 9 shows the display waveforms required to display the number "5" on the LCD pattern shown in Fig. 8 (segment outputs a_1, b_1 are used).

In the combination that the potential difference between the common output and segment output is 3 V (in the combination of H_4 and a_1), shown in Fig. 9, the segment is turned on, and in the case of 2 V or less (in the combination of H_4 and a_1), the segment is turned off.

• LCD flashing output (bs)

The bs output is used to flash symbols displayed on the LCD screen. Otherwise, the bs is used as a segment output in the same way as ai, bi (i = 1 to 16).

• Blanking the display

There are two ways for blanking the entire display depending on applications.

1. For blanking the display in a short period of time. Control the common signal generator circuit by the ATBP instruction.
2. For blanking the display in a long period of time to decrease power consumption. Use the BDC instruction to turn on and off the liquid crystal bleeder current. In this case, cutting off the bleeder current decreases great amount of power consumption.

INSTRUCTION SET

RAM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
LB x	40 to 4F	B_{L3}, B_{L2}←x (I_3) ⊕ x (I_2) B_{L1}, B_{L0}←x (I_3, I_2) B_{M1}, B_{M0}←x (I_1, I_0)
LBL xy (2-byte)	5F 00 to FF	B_M←x (I_6-I_4), B_L←y (I_3-I_0)
SBM	02	B_{M2}←1 (only next step)
EXBLA	0B	Acc↔B_L
INCB	64	Skip if B_L = F_H, B_L←B_L+1
DECB	6C	Skip if B_L = 0, B_L←B_L−1

ROM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
ATPL	03	P_{L3}-P_{L0}←Acc
RTN0	6E	P_U←S_U←R_U, P_M←S_M←R_M P_L←S_L←R_L
RTN1	6F	P_U←S_U←R_U, P_M←S_M←R_M P_L←S_L←R_L, Skip next step
TL xyz (2-byte)	70 to 7A 00 to FE	P_M←x (I_3-I_0), P_U←y (I_7, I_6) P_L←z (I_5-I_0)
TML xyz (2-byte)	7C to 7F 00 to FE	R←S←PC+1,P_{M3},P_{M2}←(0, 0) P_{M1}, P_{M0}←x (I_1, I_0),P_U←y (I_7, I_6) P_L←z (I_5-I_0)
TM x IDX yz (2-byte)	C0 to FE 00 to FE	R←S←PC+1, P_U←0, P_M←0 P_L←x (I_5-I_0), P_U←y (I_7, I_6) P_L←z (I_5-I_0), P_M←4
T xy	80 to BE	P_L←x (I_5-I_0)

Data Transfer Instructions

MNEMONIC	MACHINE CODE	OPERATION
EXC x	10 to 13	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x (I_1, I_0)
BDC	6D	BC←C Display on if C = 0 Display off if C = 1
EXCI x	14 to 17	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x (I_1, I_0) Skip if B_L = F_H, B_L←B_L+1
EXCD x	1C to 1F	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x (I_1, I_0) Skip if B_L = 0, B_L←B_L−1
LDA x	18 to 1B	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x (I_1, I_0)
LAX x	20 to 2F	Acc↔x (I_4-I_1) Skip when in succession
WR	62	W_7←W_6←···←W_0←0
WS	63	W_7←W_6←···←W_0←1

I/O Instructions

MNEMONIC	MACHINE CODE	OPERATION
KTA	6A	Acc←K
ATBP	01	BP←Acc
ATL	59	L←Acc
ATFC	60	Y←Acc
ATR	61	Ri←Acc (i = 1, 2)

Arithmetic Instructions

MNEMONIC	MACHINE CODE	OPERATION
ADD	08	Acc←Acc+M
ADD11	09	Acc←Acc+M+C, C←CY Skip if CY = 1
ADX x	30 to 3F	Acc←Acc+x (I_3-I_0) Skip if CY = 1
COMA	0A	Acc←$\overline{\text{Acc}}$
DC	3A	Acc←Acc+A_H
ROT	6B	Acc_0←Acc_1←···Acc_3←C
RC	66	C←0
SC	67	C←1

Test Instructions

MNEMONIC	MACHINE CODE	OPERATION
TB	51	Skip if β = 1
TC	52	Skip if C = 0
TAM	53	Skip if Acc = M
TMI x	54 to 57	Skip if Mi = 1, (i = x (I_1, I_0))
TA0	5A	Skip if Acc = 0
TABL	5B	Skip if Acc = B_L
TIS	58	Skip if 1 s = 0, γ←0
TAL	5E	Skip if BA = 1
TF1	68	Skip if f_1 = 1
TF4	69	Skip if f_4 = 1

Bit Manipulation Instructions

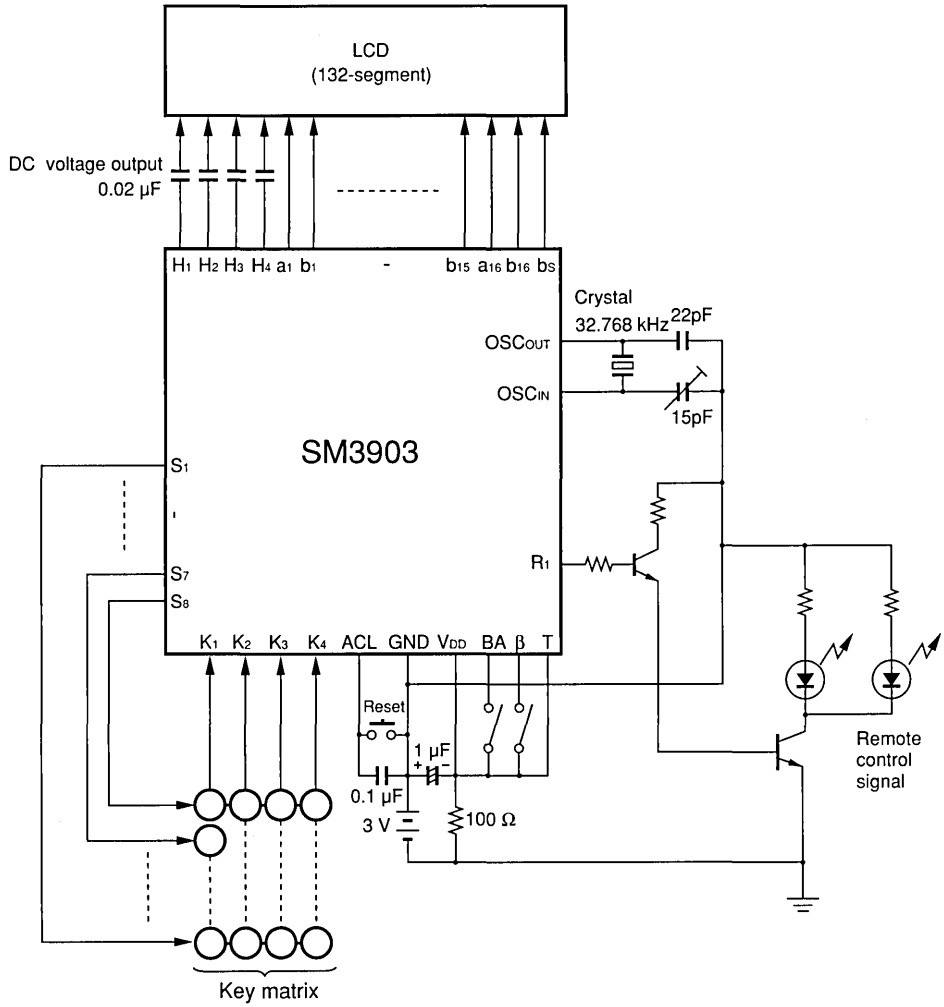
MNEMONIC	MACHINE CODE	OPERATION
RM x	04 to 07	Mi←0, i = (I_1, I_0)
SM x	0C to 0F	Mi←1, i = (I_1, I_0)

Special Instructions

MNEMONIC	MACHINE CODE	OPERATION
SKIP	00	No operation
CEND	5D	Clock stop
IDIV	65	DIV←0

SYSTEM CONFIGURATION EXAMPLE

• **Remote control with LCD display**



SM3905

4-Bit Single-Chip Microcomputer (LCD Driver)

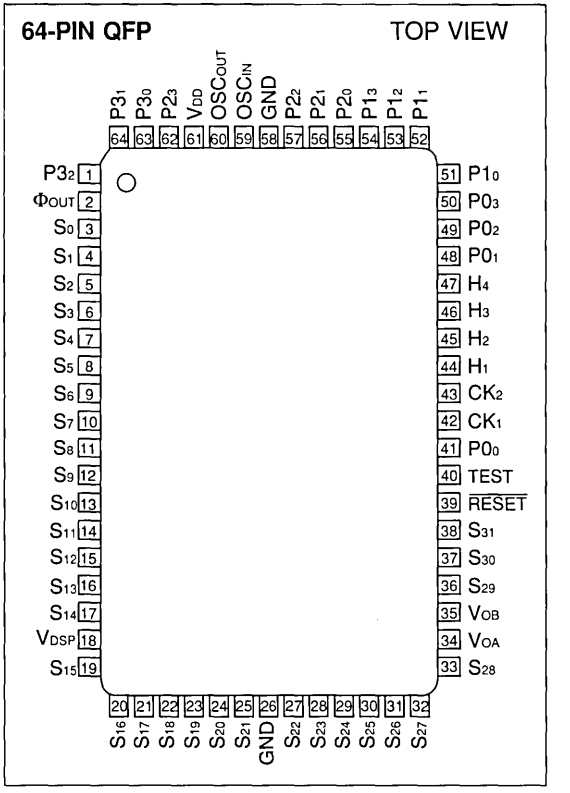
DESCRIPTION

The SM3905 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, carrier output circuit for remote control, ROM, RAM, I/O ports, serial interface, and timer/counter. It provides 5 kinds of interrupts and subroutine stack using a RAM area. Provided with 128 segments LCD drive circuit, this microcomputer is applicable to multi-functional AV remote control system, or any other similar system with a Low power consumption.

FEATURES

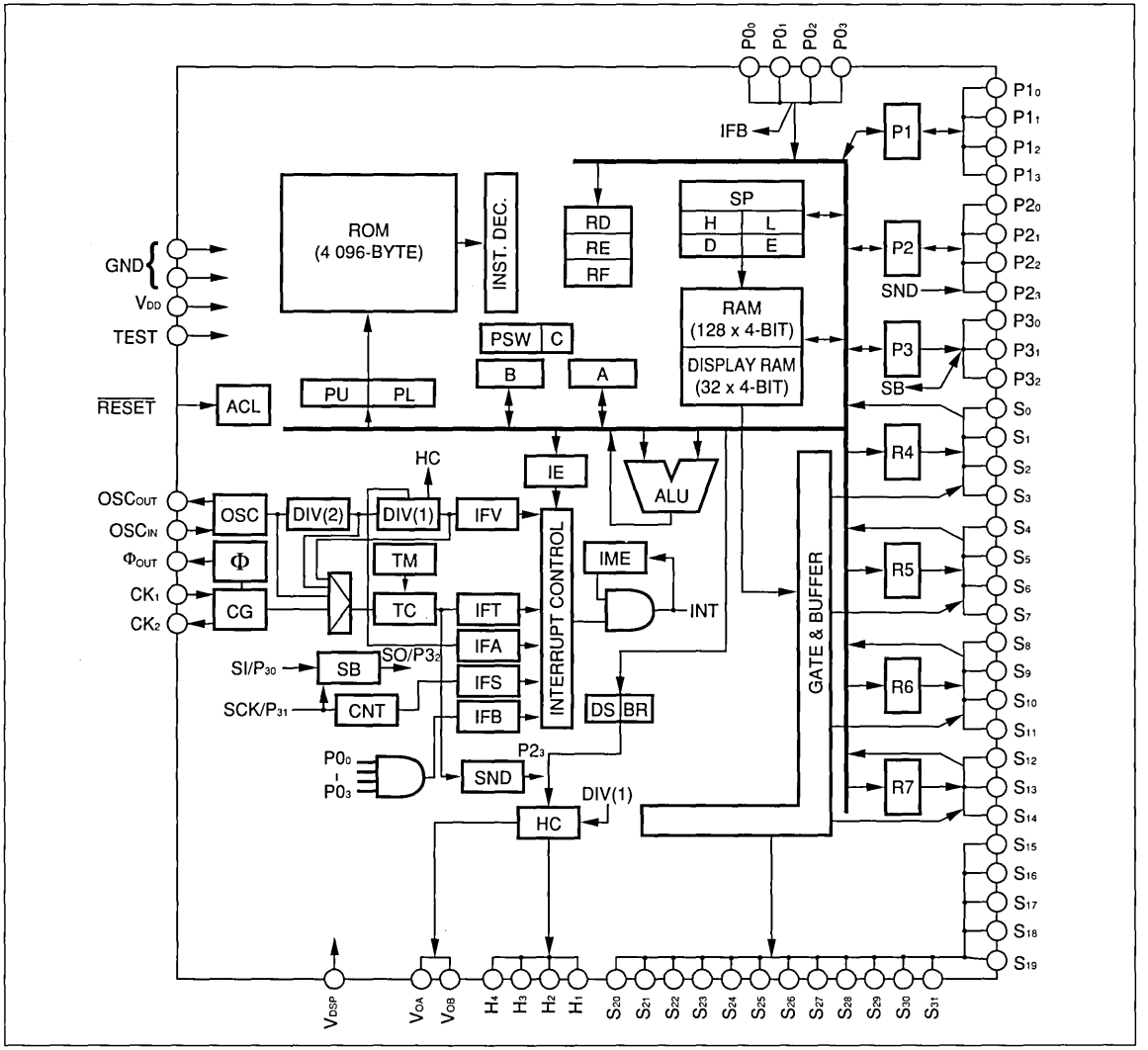
- ROM capacity : 4 096 x 8 bits
- RAM capacity : 160 x 4 bits (including 32 x 4 bits display RAM)
- Instruction sets : 98
- A RAM area is used as stack area
- I/O port :
  - Input 4
  - Output 11
  - +15 (also used as LCD segment port)
- Interrupts :
  - Internal interrupts x 4 (timer/counter, f4 signal, serial I/O, divider overflow)
  - External interrupts x 1 (P0 signal)
- Timer/counter : 8 bits x 1
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver : 128 segments, 1/3 bias, 1/4 duty cycle (if LCD drive circuit is used, a crystal oscillator circuit needs to be constituted between OSC_{IN} and OSC_{OUT}.)

PIN CONNECTIONS



- Built-in carrier output circuit for remote control
  - Carrier frequency 37.9 kHz
  - Basic oscillaton frequency (main clock) 455 kHz
  - Duty cycle 1/3 or 1/2 (mask option)
  - Reversal polarity (mask option)
- Instruction cycle time :
  - 8.79 µs (TYP., 455 kHz, at 3 V)
- Buzzer output
- Standby function
- Supply voltage : 2.7 to 3.6 V
- Package : 64-pin QFP (QFP064-P-1420)

BLOCK DIAGRAM



Nomenclature

A, B	: Accumulators
ACL	: Auto clear
ALU	: Arithmetic logic unit
BR, DS	: Common signal control F/F
CG	: Clock generator
DIV	: Divider
D, E, H, L	: General-purpose registers
HC	: Common signal circuit
IE	: Interrupt enable F/F
IFA, IFB	: Interrupt requests
IFS, IFT, IFV	
IME	: Interrupt master enable F/F
P1-P3	: Hegisters
PL, PU	: Program counters
PSW	: Program status word register
R4-R7	: General-purpose registers
RD, RE, RF	: Mode registers
SB	: Shift register
SP	: Stack pointer
TC	: Count register
TM	: Modulo register
ΦOUT	: Carrier control circuit

PIN DESCRIPTION

SYMBOL	I/O	CIRCUIT TYPE	FUNCTION
$P0_0$-$P0_3$	I	Pull up	Acc←$P0_0$-$P0_3$
$P1_0$-$P1_3$	I/O	Pull up	I/O selectable by instructions
$P2_0$-$P2_3$	I/O	Pull up	I/O selectable independently Sound output only when $P2_3$ pin is used as an output
$P3_0$-$P3_3$	I/O	Pull up	Serial interface I/O by setting the mode register RE
S_0-S_{14}	O or I/O		Selectable between segment ports and I/O ports through an RC register
S_{15}-S_{31}	O		Display RAM contents output as LCD segment signals
H_1-H_4	O		4-value output capability; used for LCD common output
TEST	I	Pull down	For test (connected to GND normally)
$\overline{\text{RESET}}$	I	Pull up	Auto clear
Φ_{OUT}	O		Carrier output remote control
CK_1, CK_2			For system clock oscillation
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_{DSP}, V_{OA}, V_{OB}			Power supply for LCD driver
V_{DD}, GND			Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	−0.3 to +7	V	1
	V_{DSP}	−0.3 to +7	V	
Input voltage	V_{IN}	−0.3 to V_{DD} +0.3	V	1
Output voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V	1
Output current	I_{OUT}	20	mA	2
Operating temperature	T_{OPR}	−20 to +70	°C	
Storage temperature	T_{STG}	−55 to +150	°C	

NOTES :

1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

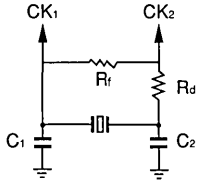
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}		2.7		3.6	V	
	V_{DSP}		2.7		V_{DD}	V	
Basic oscillation frequency	f	V_{DD} = 2.7 to 3.6 V		455		kHz	1
Instruction cycle	t	V_{DD} = 2.7 to 3.6 V		8.79		µs	
Crystal oscillation frequency	fosc			32.768		kHz	

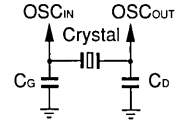
NOTE :

1. Starting condition : within 10 seconds after power on.

Oscillation Circuit



Oscillator : KBR-455B (Kyocera)
R_f = 1 MΩ
R_d = 5.6 kΩ
C_1 = 220 pF
C_2 = 100 pF



C_G=10 pF, C_D=8 pF

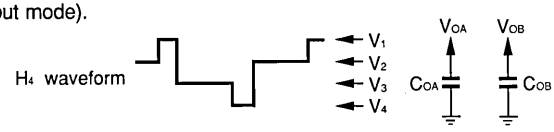
DC CHARACTERISTICS

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}		0.7 x V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.3 x V_{DD}	V	
	V_{IH2}		V_{DD}–0.5		V_{DD}	V	2
	V_{IL2}		0		0.5	V	
Input current	I_{IH}	V_{IN} = 0 V	2		200	µA	1
Output current	I_{OH1}	V_{OH} = V_{DD}–0.5 V	50			µA	3
	I_{OL1}	V_{OL} = 0.5 V	250			µA	
	I_{OH2}	V_{OH} = V_{DD}–0.5 V	50			µA	4
	I_{OH2D}	V_{OH} = V_{DD}–0.5 V	160			µA	5
	I_{OL2}	V_{OL} = 0.5 V	0.5			mA	6
	I_{OH3}	V_{OH} = V_{DD}–0.5 V	20			µA	7
	I_{OH3D}	V_{OH} = V_{DD}–0.5 V	90			µA	8
	I_{OL3}	V_{OL} = 0.5 V	0.2			mA	7
Output impedance	R_C			5	20	kΩ	9
	R_S			10	40	kΩ	10
Output voltage	V_1	V_{DSP} = 3.0 V No load	2.7		3	V	11
	V_2		1.7	2	2.3	V	
	V_3		0.7	1	1.3	V	
	V_4		0		0.3	V	
Supply current	I_{OP}	f = 455 kHz, V_{DD} = 3.0 V		160	320	µA	12
	I_{SB}	Standby current V_{DSP} = 3.0 V		15	40		13
		Standby current V_{DD} = 3.0 V		8	20		14

NOTES :

1. Applied to pins $P0_0$-$P0_3$, $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_2$ (during input mode).
2. Applied to pins CK_1, TEST, OSC_{IN}.
3. Applied to pin CK_2.
4. Applied to pins $P1_0$-$P1_3$, $P2_0$-$P2_2$, $P3_0$-$P3_2$ (during output mode).
5. Applied to pins $P2_3$, Φ_{OUT} (during output mode).
6. Applied to pins $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_2$, Φ_{OUT} (during output mode).
7. Applied to pins S_0-S_{14} (during data output mode).
8. Pins cited in NOTE 7 are applicable with mask option used.
9. Applied to pins H_1-H_4.
10. Applied to pins S_0-S_{31} (in LCD output mode).
11. Applied to pins H_1-H_4, S_0-S_{31} (in LCD output mode).
12. No load condition.
13. No load condition when bleeder resistance is ON, V_{DSP} = 3.0 V, during 32.768 kHz crystal oscillation.
14. No load condition when bleeder resistance is OFF, during 32.768 kHz crystal oscillation.



C_{OA} = 1 µF, C_{OB} = 1 µF

PIN FUNCTIONS

• GND, V_{DD}, V_{DSP} (Power supply inputs)

Both GND pins 26 and 58 should be grounded.

The V_{DD} pin is the positive power supply with respect to GND.

The V_{DSP} pin is the positive power supply for an LCD driver with respect to GND.

• TEST (Test input)

The TEST pin should be left open or connected to GND with a pull-down resistor.

• $\overline{\text{RESET}}$ (Input)

The $\overline{\text{RESET}}$ accepts an active Low system reset which initializes the internal logic of the device.

Normally a capacitor of about 0.1 µF is connected between this pin and GND to provide a power on reset function.

• OSC_{IN}, OSC_{OUT} (Crystal oscillator pins)

The OSC_{IN} and OSC_{OUT} pins connect with an external crystal oscillator and these pins and the GND connect with a capacitor, which constitute an oscillator circuit.

The output of the oscillator is coupled to a clock divider for real-time clock operation.

• CK_1, CK_2 (System clock oscillator pins)

The CK_1 and CK_2 pins provide a system clock oscillator.

• H_1 to H_4 (Common signal outputs)

The H_1 to H_4 pins are used to drive the common of an LCD.

• S_0 to S_{31} (Segment outputs)

The S_0 to S_{31} pins drive LCD segments. Pins S_0 through S_{14} may also be used as I/O ports when specified with the mode register RC.

• $P0_0$ to $P0_3$ (Inputs)

The P0 pins are normally used to accept key input data. A falling edge at these pins resets the IFB flag.

• $P1_0$ to $P1_3$ (Input/output)

The P1 are I/O pins connected to the positive supply with pull-up resistors.

They may be switched between input and output modes through an instruction.

• $P2_0$ to $P2_3$ (Input/output)

The $P2_0$ to $P2_3$ pins are bit-independent I/O ports which can be independently set to input or output mode with the mode register RF.

When the $P2_3$ is used for an output pin, it serves exclusively as a sound output pin, which can output a sound signal with any frequency set up by the timer counter.

Pins $P2_0$ and $P2_1$ output the OD and R/W signals with the mode register RC.

• $P3_0$ to $P3_2$ (Input/output)

The $P3_0$ to $P3_2$ pins are I/O pins which are connected to the positive supply with pull-up resistors.

These pins can be set to I/O mode for use in a serial interface with the mode register RE.

• Φ_{OUT} (Carrier output pin for remote control)

A carrier signal output pin for remote control. It is used to control carrier signal output by setting the bits in the bit of R7 register.

SYSTEM CONFIGURATION

ROM and Program Counter

The on-chip ROM has a configuration of 64-page x 64-step x 8-bit, and stores programs and table data. The program counter consists of a 6-bit page address counter P_U and a 6-bit binary counter P_L used to specify the steps within a page.

The locations shown in Fig. 1 are allocated in the on-chip ROM.

Stack Pointer (SP)

The stack pointer (SP) is an 8-bit shift register which holds the starting address of the stack area of RAM space. Immediately after the reset, the contents of the stack pointer are uninitialized and must be set to an appropriate value. If, for instance, the initial value of the stack pointer is set to 80_H, the data memory are beginning with the highest address (excluding the display RAM area) $7F_H$, is usable as a stack area.

RAM

Data memory has a 160-word x 4-bit configuration, and is used to store processing data and other information. Data memory is also used as a stack area to save register values, the program counter value, and program status word (PSW) at the time a subroutine jump or an interrupt occurs. Fig. 2 shows the RAM configuration. 2 x 16 x 4-bit of entire RAM space is used as a display RAM area from which data is output to LCD segment driving pins. An LCD with a 1/4 duty and 1/3 bias format can be directly driven by writing display data into the display RAM area. The display RAM outputs are, as shown in Fig.3, connected to segment output pins S_0 to S_{31} for individual set of common outputs H_1 to H_4. The segment output pins provide a single digit of display RAM data M_0 to M_3, as an LCD driving waveform signal according to H_1 to H_4 outputs. The operations of the display RAM are identical to those of other RAM areas.

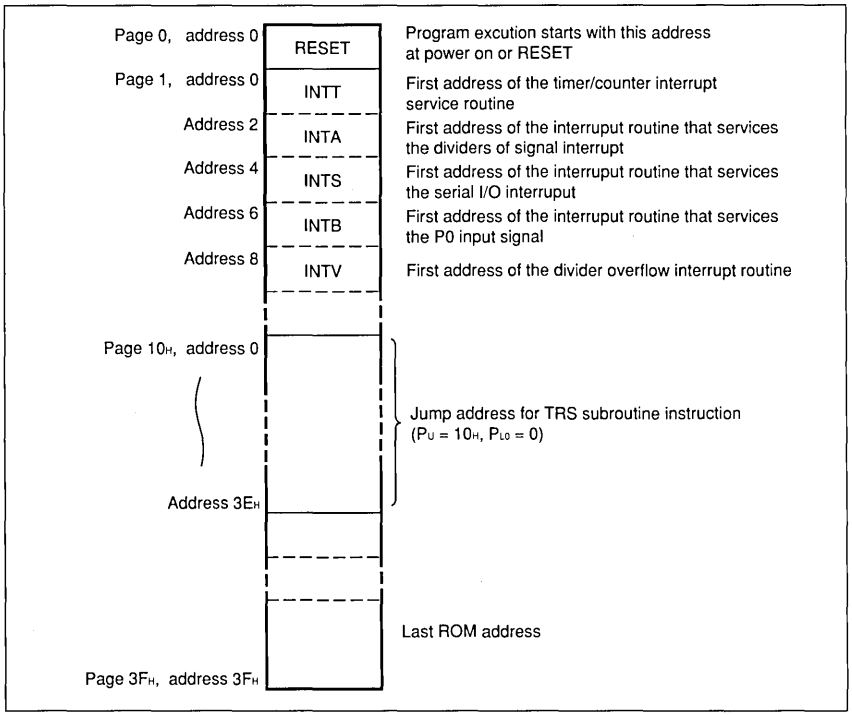


Fig. 1 Program ROM Map

L \ H	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
0000									S_0	S_{16}
0001									S_1	S_{17}
0010									S_2	S_{18}
0011									S_3	S_{19}
0100									S_4	S_{20}
0101									S_5	S_{21}
0110									S_6	S_{22}
0111									S_7	S_{23}
1000									S_8	S_{24}
1001									S_9	S_{25}
1010									S_{10}	S_{26}
1011									S_{11}	S_{27}
1100									S_{12}	S_{28}
1101									S_{13}	S_{29}
1110									S_{14}	S_{30}
1111									S_{15}	S_{31}

NOTE :

The area with the thick line is allocated for a display RAM and the Sn (n = 0 to 31) shows the related segment outputs.

Fig. 2 RAM Configuration

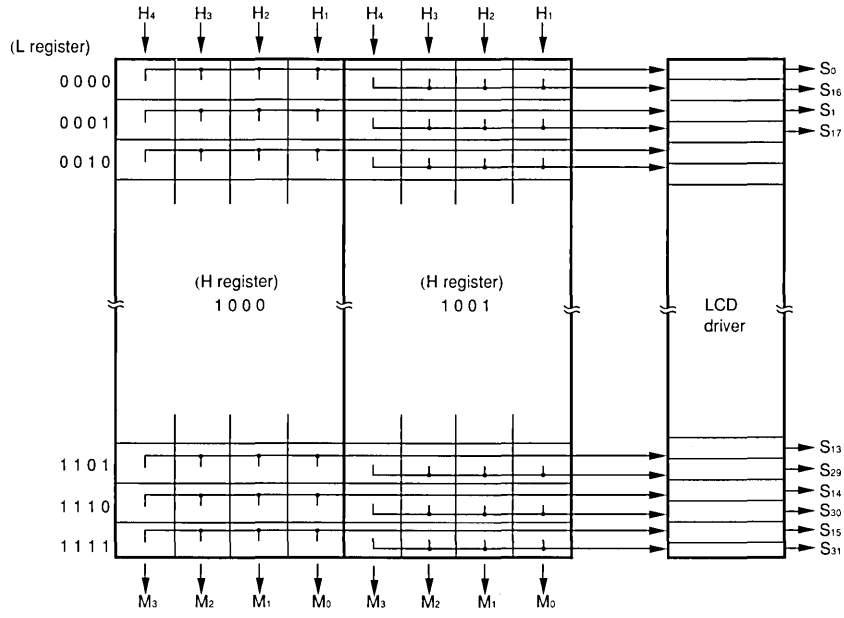


Fig. 3 Display RAM and its LCD Segment Outputs

Accumulator (A), Subaccumulator (B) and Arithmetic and Logic Unit (ALU)

The accumulator (A) is a 4-bit working register which is the nucleus of the single chip system. It holds the results of operations and transfers data to memory, I/O ports, and registers.

A subaccumulator (B) is another 4-bit register. It is used as one of general-purpose registers, and when combined with the A to form a B-A register pair, allows data transfer on an 8-bit basis.

The arithmetic and logic unit (ALU) performs, in conjunction with a carry flag (C), binary addition, shift operations, and logical operations such as AND, OR, EX-OR, and complement.

General-Purpose Registers (H, L, D, E)

Registers H and L are 4-bit general-purpose registers. They can transfer and compare data with the Acc on 4-bit basis. Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis. The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations. The L register can be incremented or decremented and is used to access I/O ports and mode registers.

Clock Divider, IFV Flag, IFA Flag

The device contains a crystal oscillator and a 15-stage divider, as shown in Fig. 4. A real-time clock

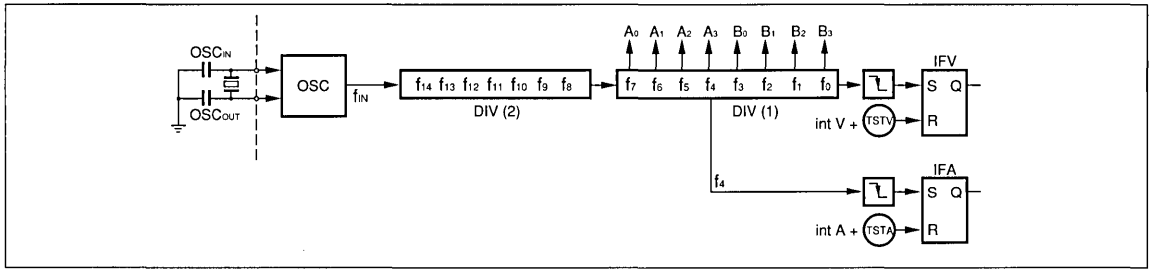


Fig. 4 Real-Time Clock and Divider

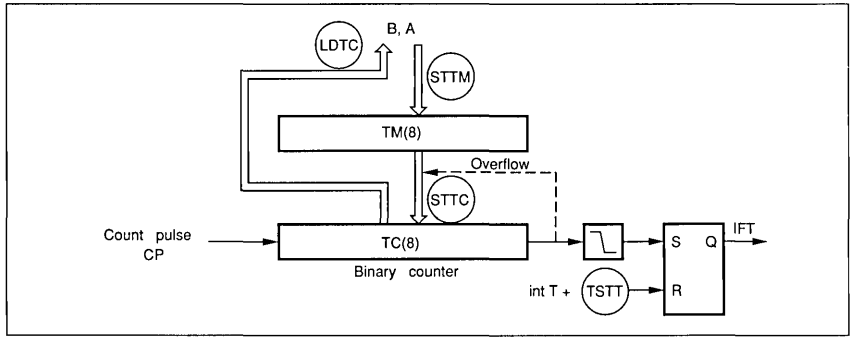


Fig. 5 Timer Counter

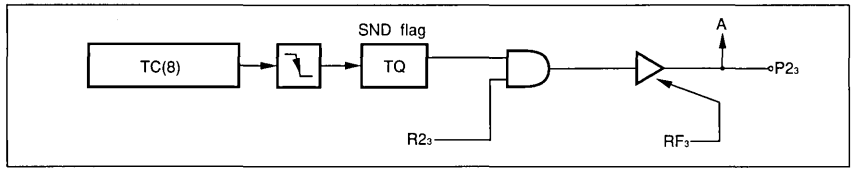


Fig. 6 SND Signal

can be provided by connecting an external crystal oscillator between the oscillator pins. When an external 32.768 kHz crystal oscillator is used, the f_0 signal is a frequency of 1 Hz.

Timer/Counter and the SND Signal

The timer/counter consists of an 8-bit count register (TC) and an 8-bit mudulo register (TM).

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register (See Fig. 5). The count pulse CP can be selected from divider signals f_{IN}, f_0 and the system clock, by using the mode register RD. If the count register (TC) overflows, the SND flag reverses its status at the falling edge of the TC. A sound signal can be obtained at the TC output by putting P2 in output mode and sending a "1" to pin $P2_3$ (See Fig. 6).

Serial Interface and IFS

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data. The serial clock can be selected with either an internal clock (system clock) or an external clock.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin, and the data input from the SI pin at the rising edge of a serial clock is loaded into the lowest bit of the shift register. When the internal clock is used, immediately after the SIO instruction is executed, the serial operation begins and stops with 8-clock which are output from the SCK pin.

Upon completion of an 8-bit shift operation, the serial I/O ending flag IFS is set each time a 3-bit counter overflows, and an interrupt request occurs.

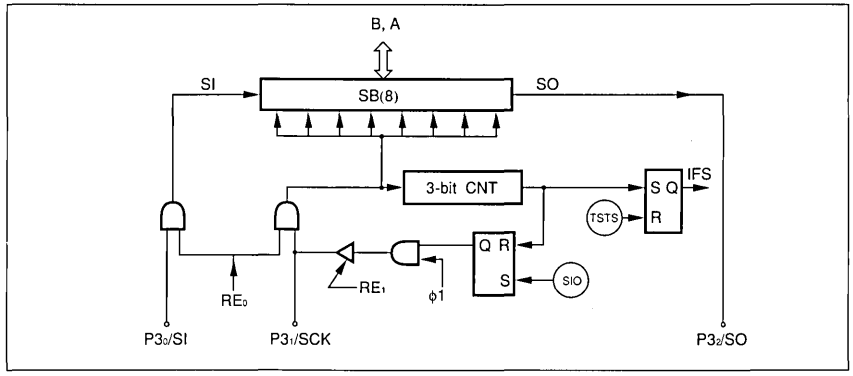


Fig. 7 Serial Interface

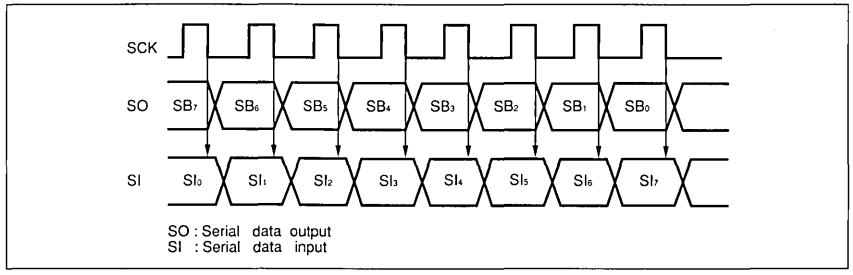


Fig. 8 Serial Interface Timing

Input Port P0 and IFB Flag

The IFB flag is set at the falling edge of the signal applied to the input port P0 by which the interrupt is enabled.

When port P0 is used as a key input, it can cause an interrupt each time a key is operated.

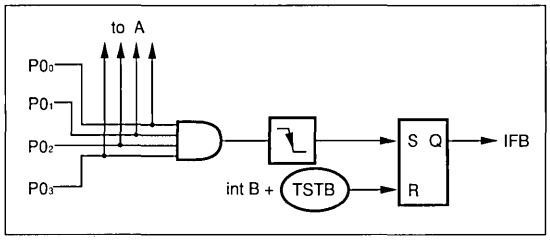


Fig. 9 P0 Port

Interrupts

When an interrupt occurs, the corresponding interrupt request flag is set. The CPU acknowledges the interrupt if it is enabled (Master interrupt enable flag and the corresponding interrupt enable flag are set). If more than one interrupt occurs simultaneously, all of the corresponding interrupt request flags will be set, but the CPU will only acknowledge that interrupt with the highest priority and other interrupts will be queued.

I/O Ports

Port P0 is a 4-bit parallel input port. The IFB flag is set at the falling edge of this port.

Port P1 can be switched between input and output modes, 4-bit at a time.

Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.

Ports $P2_0$ and $P2_1$ can output the OD and R/W signals, respectively. In those cases, these pins should be kept High in an output mode. Port $P2_3$ outputs the SND signal in the output mode.

Port P3 is a 3-bit I/O port which can be placed in input or output mode, 3-bit at a time. Each bit of port P3 can be set to the I/O modes (SI, SO, SCK) of a serial interface.

Ports P1 and P3 are placed in an output mode when a port output instruction is executed, and in an input mode when a port input instruction is executed. After an ACL operation, ports P1, P2 and P3 are all placed in an input mode.

Every input port has pull-up resistors. (Pull-up resistors for I/O ports are effective only when the ports are placed in an input mode.)

Ports P1 through P3 in an output mode can be independently set or reset by instructions.

When a key-matrix is configured by using I/O ports, if the short on output pins may occur caused by a multiple key depression, port P1 should be used as an output.

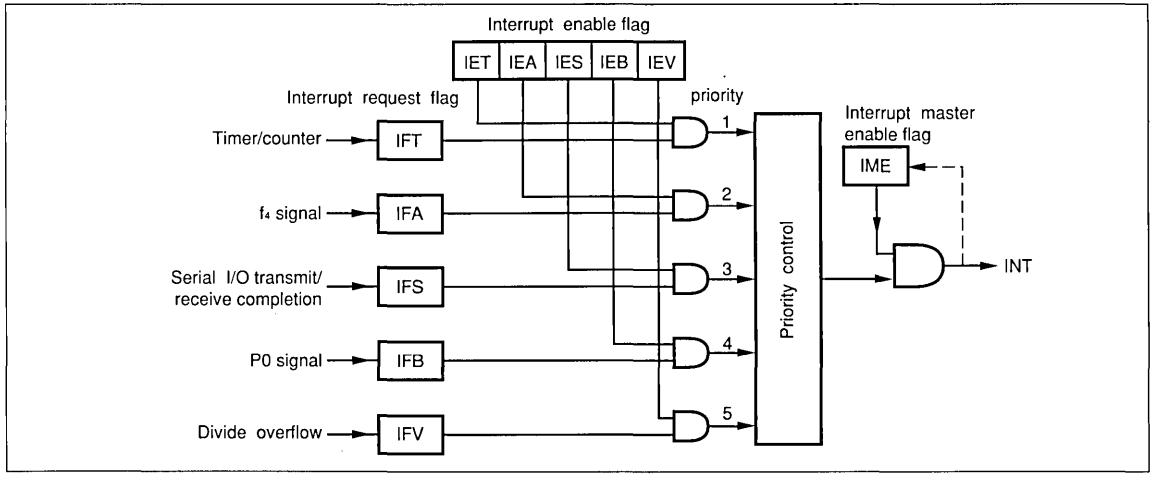


Fig. 10 Interrupt Handling

Table 1 Characteristics of I/O Ports

PORT	FUNCTION	Direct 4-bit parallel I/O		IN, OUT instruction		Bit independent output SPn
		Input (INA)	Output (OUTA)	Input (IN)	Output (OUT)	Direct pin-independent output RPn
P0	Input-only port	O	X	O	X	X
P1	I/O port	O	O	X	O	O
P2	I/O port, P_{23}-sound output	O	O	X	X	O
P3	$P3_0$-SI, $P3_1$-SCK, $P3_2$-SO, multi-control port	O	O	X	X	O

O : Yes, X : No

Standby Mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated. Standby mode may be cleared with the interrupt request or the $\overline{\text{RESET}}$ signal.

Reset Function (ACL)

Applying a Low level signal to the $\overline{\text{RESET}}$ pin resets the internal logic of the device and applying a High level signal starts execution of the program at address 0, page 0. Once the device is reset, all I/O ports are placed in input mode, all interrupts are disabled, and the LCD display turns off. The device is also reset when it is powered up.

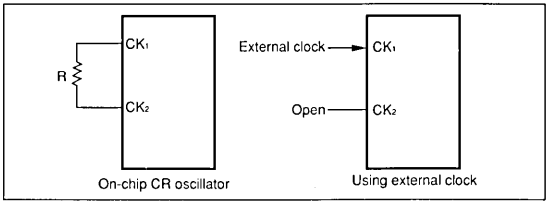


Fig. 11 Main Clock Sources

Main Clock Oscillator Circuit

The main clock oscillator requires an external resistor across pins CK_1 and CK_2. Instead of using on-chip oscillator, an external clock may be applied to pin CK_1. In this case, pin CK_2 should be left open. The system clock ϕ is a divided clock equivalent to 1/4 of the clock applied to pin CK_1.

LCD Driver

• Display segment

The SM3905 contains an on-chip LCD driver which can directly drive an LCD with a 1/4 duty and 1/3 bias. Fig.12 shows an example of LCD segment configuration for 1/4 duty.

Each segment of the LCD can be turned on or off by software control of the setting of the corresponding bit "1" or "0" in the display RAM area (see Fig. 3).

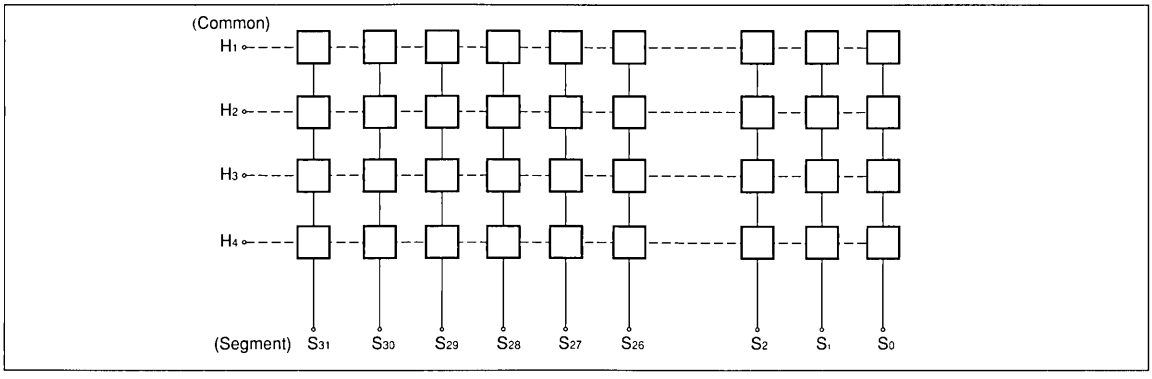


Fig. 12 LCD Segment Configuration for 1/4 Duty

The LCD digit may have any shape, provided that the maximum number of segments does not exceed 128 (see Fig. 12). Fig. 13 shows an example of a 7-Segment Numeric LCD Digit.

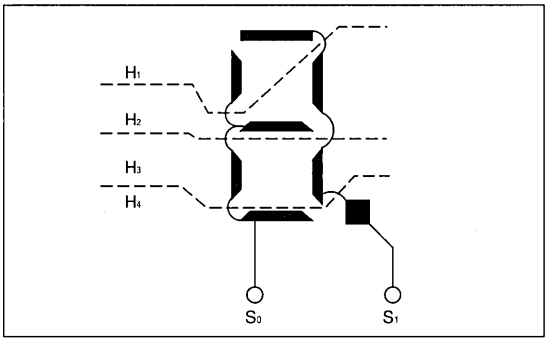


Fig. 13 7-Segment Numeric LCD Digit

• LCD driving signal waveform

Fig. 14 shows the LCD signal driving waveforms required to display the number "5" on the 7-segment display shown in Fig. 13 (segment outputs S_0 and S_1 are used). A voltage of 3 V is applied to pin V_{DSP} in the Fig. 14. The frame frequency (I/T) can be selected from 64 Hz or 128 Hz by mask options.

• V_{OA} and V_{OB} pins

The device contains bleeder resistors to allow 1/3 bias driving. When V_{DSP} is 3 V, voltages of 2 V and 1 V are output from pins V_{OA} and V_{OB} respectively. Normally pins V_{OA} and V_{OB} are left open. When an LCD with a large display area is driven, connect capacitors across pins V_{OA} and V_{DSP} and across V_{OB} and V_{DSP} to improve the rise time of the LCD driving signal.

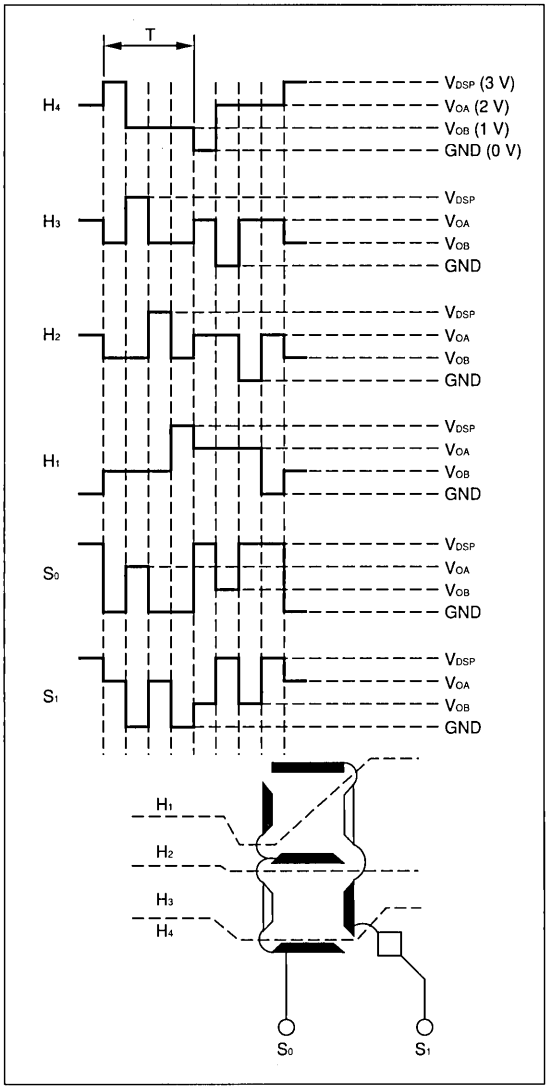


Fig. 14 LCD Driving Signal Waveform (required to display the number 5)

Remote Control Carrier Output Function

SM3905 has a carrier output function for remote control output. A carrier is output from Φ_{OUT}, and controlled using the register R73. Setting "0" in the bit of R73 causes the output from Φ_{OUT} to be set to constant and High output. If "1" is set, a carrier, which is a remote control signal, is output. If "0" is set in the bit of R73, the output level is set to constant and High as stated above. However, it can be set to the constant Low level using the mask option. Either 1/2 or 1/3 can be selected as the duty of the carrier. (See Table 2 and Fig. 15)

The frequency of the carrier is approximately 37.9 kHz (1/2 duty or 1/3 duty) when the basic oscillation frequency (main clock) is 455 kHz.

Table 2 Mask Option for Φ_{OUT} Pin Output

SELECTION OF PLA		Φ_{OUT} OUTPUT	
PLA1	PLA2	Output waveform	When remote control signal is not output :
1	1	A	Constant Low output
2	1	B	Constant Low output
1	2	$\overline{A}$	Constant High output
2	2	$\overline{B}$	Constant High output

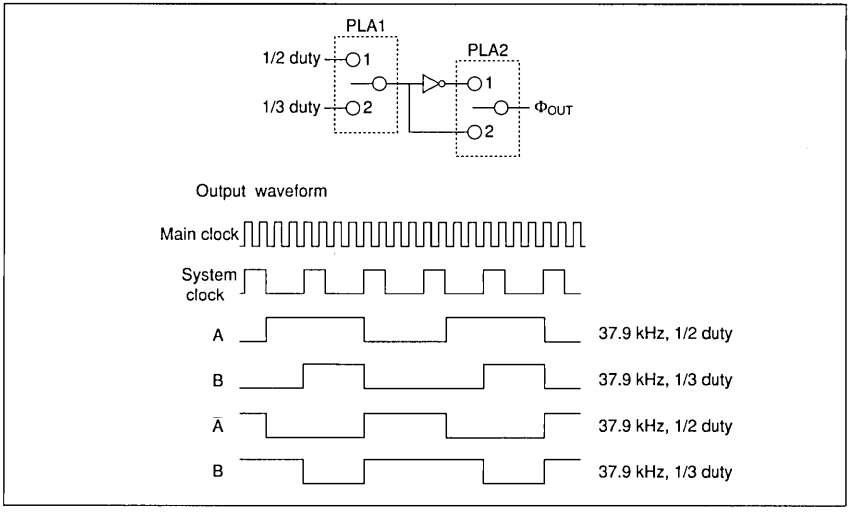


Fig. 15 Mask Option for Φ_{OUT} Output

Fig. 16 shows an example of a circuit that converts remote control carrier signal from the Φ_{OUT} pin into infrared signal.

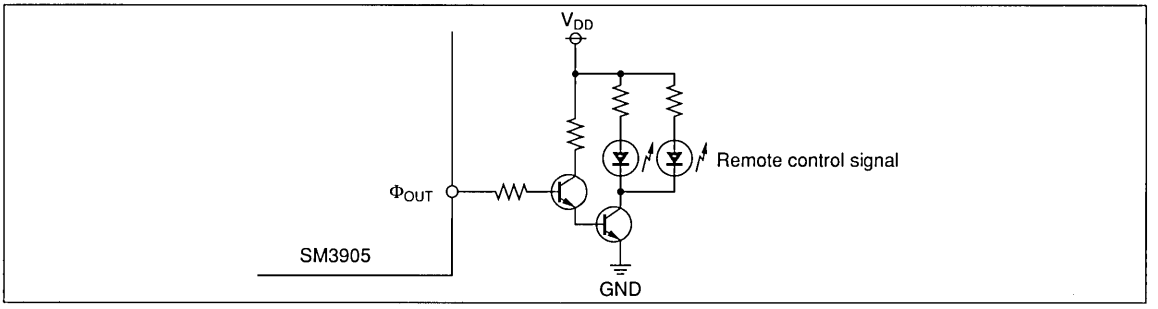


Fig. 16 Remote Control Signal Output Circuit

INSTRUCTION SET

ROM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
TR x	80 to BF	$P_L \leftarrow x\ (I_5\text{-}I_0)$
TL xy (2-byte)	E0 to EF 00 to FF	$P_U \leftarrow x\ (I_{11}\text{-}I_6)$ $P_L \leftarrow y\ (I_5\text{-}I_0)$
TRS x	C0 to DF	(SP–2), (SP–3), (SP–4)←PC SP←SP–4 $P_U \leftarrow 10_H$ $P_L \leftarrow x\ (I_4, I_3, I_2, I_1, I_0, O)$
CALL xy (2-byte)	F0 to FF 00 to FF	(SP–2), (SP–3), (SP–4)←PC SP←SP–4, $P_U \leftarrow x\ (I_{11}\text{-}I_6)$, $P_L \leftarrow y\ (I_5\text{-}I_0)$
JBA x (2-byte)	7F 30 to 3F	$P_{U5}\text{-}P_{U2} \leftarrow x\ (I_3\text{-}I_0)$, $P_{U1}, P_{U0}, P_{L5}, P_{L4} \leftarrow B$, $P_{L3}\text{-}P_{L0} \leftarrow A$
RTN	61	$P_U, P_L \leftarrow (SP), (SP+1), (SP+2)$
RTNS	62	$P_U, P_L \leftarrow (SP), (SP+1), (SP+2)$, SP←SP+4
RTNI	63	$P_U, P_L \leftarrow (SP), (SP+1), (SP+2)$, PSW←(SP+3), SP←SP+4, IME←1

RAM Address Instructions

MNEMONIC	MACHINE CODE	OPERATION
STL	69	L←A
STH	68	H←A
EXHD	3F	H↔D L↔E
LIHL xy (2-byte)	3D 00 to FF	$H \leftarrow x\ (I_7\text{-}I_4)$, $L \leftarrow y\ (I_3\text{-}I_0)$

Data Transfer Instructions

MNEMONIC	MACHINE CODE	OPERATION
EX pr	5C to 5F	A↔(pr)
LDX adr (2-byte)	7D 00 to FF	A←(adr)
STX adr (2-byte)	7E 00 to FF	(adr)←A
EXX adr (2-byte)	7C 00 to FF	A↔(adr)
LAX x	10 to 1F	$A \leftarrow x\ (I_3\text{-}I_0)$
LIBA xy (2-byte)	3C 00 to FF	$B \leftarrow x\ (I_7\text{-}I_4)$ $A \leftarrow y\ (I_3\text{-}I_0)$
LBAT	60	$B \leftarrow ROM\ (P_{U5}\text{-}P_{U2}, B, A)_H$ $A \leftarrow ROM\ (P_{U5}\text{-}P_{U2}, B, A)_L$
LDL	65	A←L
LD pr	54 to 57	A←(pr)
ST pr	58 to 5B	(pr)←A
EXH	6C	A↔H
EXL	6D	A↔L
EXB	6E	A↔B
STB	6A	B←A
LDB	66	A←B
LDH	64	A←H
PSHBA	28	(SP–1)←B, (SP–2)←A, SP←SP–2
PSHHL	29	(SP–1)←H, (SP–2)←L, SP←SP–2
POPBA	38	B←(SP+1), A←(SP), SP←SP+2
POPHL	39	H←(SP+1), L←(SP), SP←SP+2
STSB	70	$SB_H \leftarrow B, SB_L \leftarrow A$
STSP	71	$SP_H \leftarrow B, SP_L \leftarrow A$
STTC	72	TC←TM
STTM	73	$TM_H \leftarrow B, TM_L \leftarrow A$
LDSB	74	$B \leftarrow SB_H, A \leftarrow SB_L$
LDSP	75	$B \leftarrow SP_H, A \leftarrow SP_L$
LDTC	76	$B \leftarrow TC_H, A \leftarrow TC_L$
LDDIV	77	$B \leftarrow DIV_H, A \leftarrow DIV_L$

Arithmetic Instructions

MNEMONIC	MACHINE CODE	OPERATION
ADX x	00 to 0F	A←A+x (I_3-I_0), Skip if C_Y = 1
ADD	36	A←A+(HL)
ADDC	37	A←A+(HL)+C, C←C_Y Skip if Cy = 1
OR	31	A←A ∪ (HL)
AND	32	A←A ∩ (HL)
EOR	33	A←A ⊕ (HL)
ANDB	22	A←A ∩ B
ORB	21	A←A ∪ B
EORB	23	A←A ⊕ B
COMA	6F	A←$\bar{A}$
ROTR	25	C→A_3→A_2→A_1→A_0→C
ROTL	35	C←A_3←A_2←A_1←A_0←C
INCB	52	B←B+1, Skip if B = F_H
DECB	53	B←B–1, Skip if B = 0
INCL	50	L←L+1, Skip if L = F_H
DECL	51	L←L–1, Skip if L = 0
DECM adr	79 00 to FF	(adr)←(adr)–1, Skip if (adr) = 0
INCM adr	78 00 to FF	(adr)←(adr)+1, Skip if (adr) = F_H

Test Instructions

MNEMONIC	MACHINE CODE	OPERATION
TAM	30	Skip if A = (HL)
TAH	24	Skip if A = H
TAL	34	Skip if A = L
TAB	20	Skip if A = B
TC	2A	Skip if C = 0
TM x	48 to 4B	Skip if (HL), x = 1
TA x	4C to 4F	Skip if Ax = 1
TSTT	2B	Skip if IFT = 1, IFT←0
TSTA	2C	Skip if IFA = 1, IFA←0
TSTS	2D	Skip if IFS = 1, IFS←0
TSTB	2E	Skip if IFB = 1, IFB←0
TSTV	2F	Skip if IFV = 1, IFV←0

Bit Manipulation Instructions

MNEMONIC	MACHINE CODE	OPERATION
SM x	40 to 43	(HL) x←1
RM x	44 to 47	(HL) x←0
RC	26	C←0
SC	27	C←1
RIME	3A	IME←0
SIME	3B	IME←1
DI x (2-byte)	7F C0 to DF	IEF←IEF ∩ x
EI x (2-byte)	7F E0 to FF	IEF ∪ x

I/O Instructions

MNEMONIC	MACHINE CODE	OPERATION
IN	67	A←P0
OUT	6B	P1←A
INA x (2-byte)	7F A0 to A9	A←P (x), R (x)
OUTA x (2-byte)	7F B0 to BF	P (x), R (x)←A
INBA x	7F 80 to 81	B←R (x +1) A←R (x)
OUTBA x (2-byte)	7F 90 to 91	R (x +1)←B R (x)←A
SP xy (2-byte)	7A 00 to F3	P (y)←P (y) x
BP xy (2-byte)	7B 00 to F3	P (y)←P (y) x
RDS (2-byte)	7F 60	DS←0
RBR (2-byte)	7F 70	BR←0
SDS (2-byte)	7F 61	DS←1
SBR (2-byte)	7F 71	BR←0
READ (2-byte)	7F 62	A←P4 with OD
WRIT (2-byte)	7F 72	P4←A with R/W
READB (2-byte)	7F 63	A←P4, with OD B←P5
WRITB (2-byte)	7F 73	P4←A, with R/W P5←B

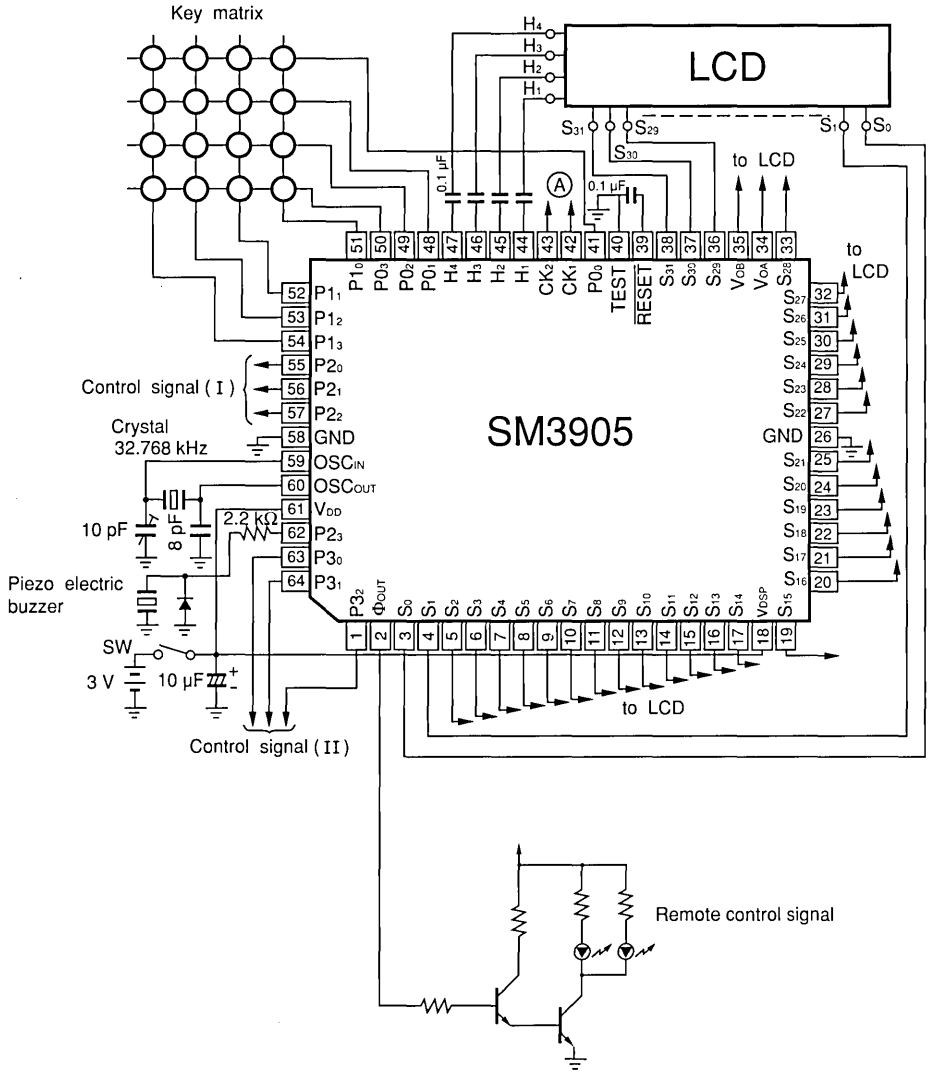
Special Instructions

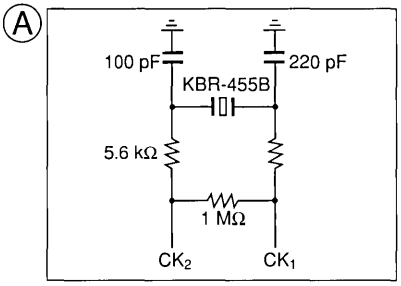
MNEMONIC	MACHINE CODE	OPERATION
SIO	3E	Serial I/O start
IDIV (2-byte)	7F 10	DIV←0
SKIP	00	No operation
CEND (2-byte)	7F 00	System clock stop

NOTE :

The machine code consists of 8-bit of I_7, I_6, I_5, I_4, I_3, I_2, I_1 and I_0.

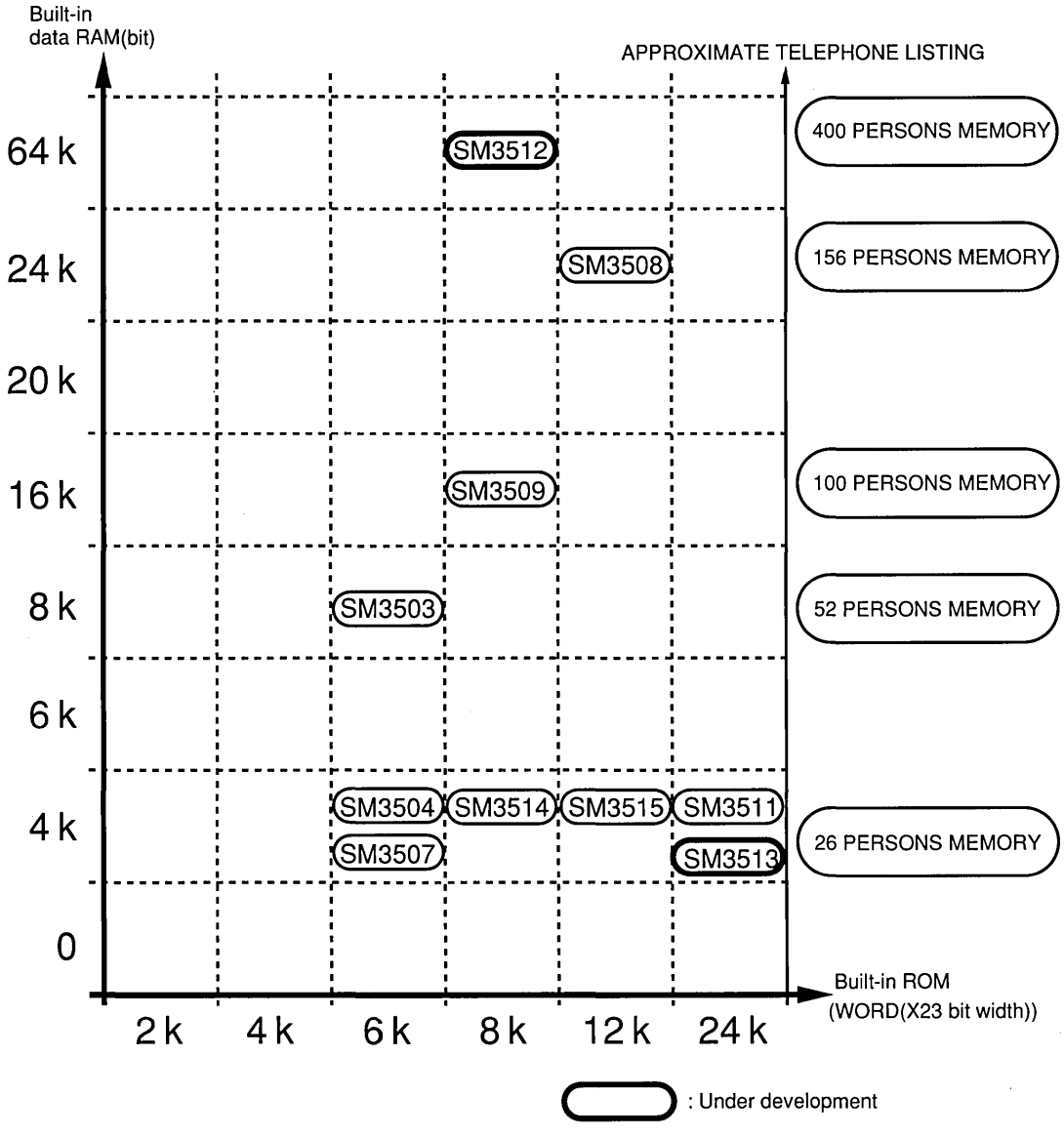
SYSTEM CONFIGURATION EXAMPLE



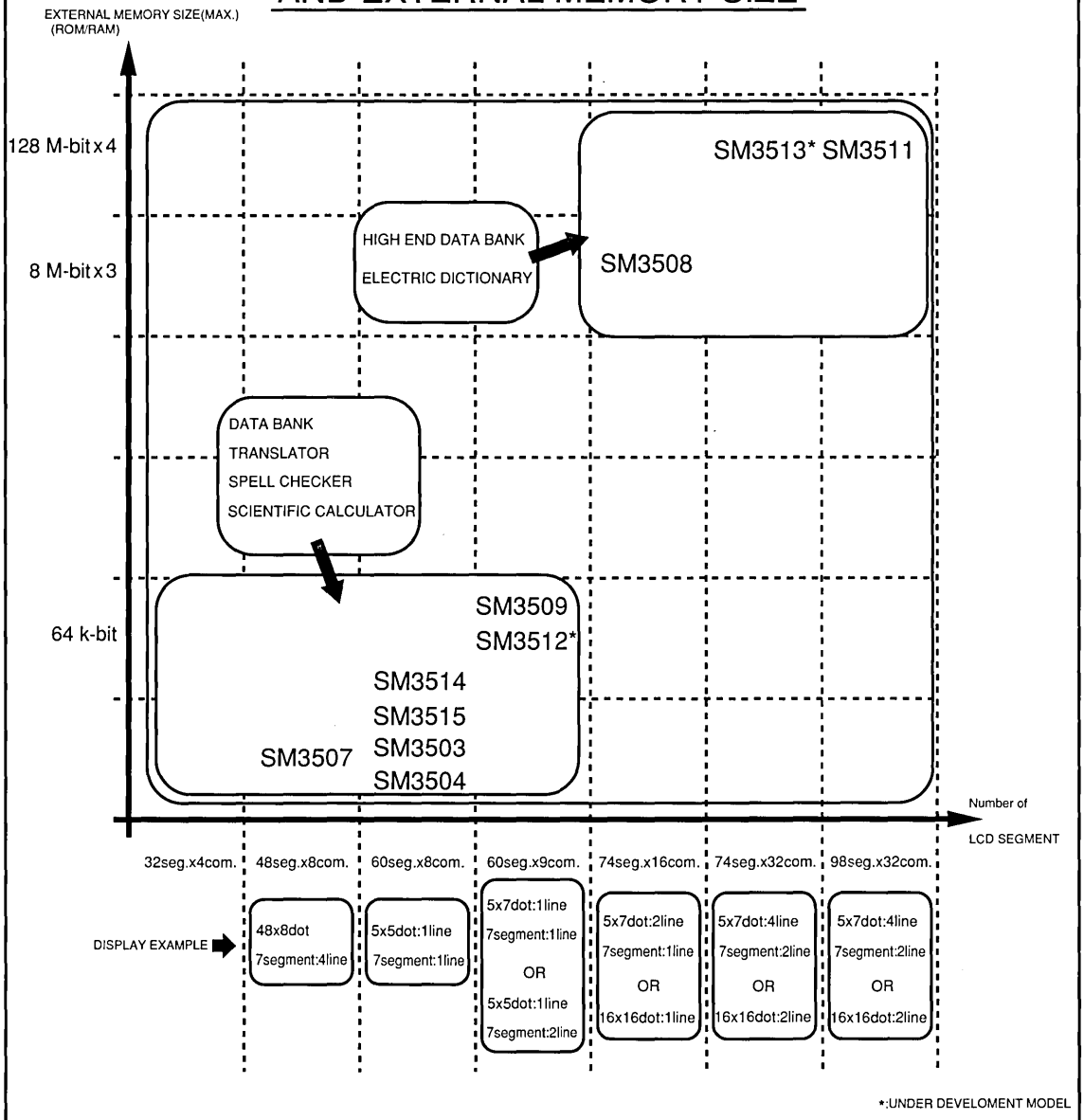


4-BIT SINGLE-CHIP MICROCOMPUTERS (FOR DATA BANK USE)

PRODUCT SELECTION BY BUILT-IN MEMORY SIZE



PRODUCT SELECTION BY LCD SEGMENT NUMBER AND EXTERNAL MEMORY SIZE



*:UNDER DEVELOMENT MODEL

COMPARISON TABLE

		SM3507	SM3503	SM3504	SM3514	SM3515
Application		Game	52 Persons Data Bank	26 Persons Data Bank	26 Persons Data Bank	26 Persons Data Bank
Built-in Program ROM Size (word (23-bit width))		6 k	6 k	6 k	8 k	12 k
Built-in Data RAM Size (byte)		0.5 k	1 k	0.5 k	0.5 k	0.5 k
Enternal Memory (byte)		-	-	-	-	-
LCD Display (seg. x com.)		48 x 8 (384 dots)	60 x 8 (480 dots)	60 x 8 (480 dots)	60 x 8 (480 dots)	60 x 8 (480 dots)
LCD Contrast Adjustable Level		-	-	-	-	-
IR Communication (External Ceramic Resonator)		-	-	-	-	-
I/O	Parallel I/O	8	-	-	-	-
	Output	2	-	-	-	-
	Buzzer Output	1	1	1	1	1
	Input	2	-	-	-	-
Key Matrix		14 x 4	14 x 6	14 x 6	14 x 6	14 x 6
ON Key		1	1	1	1	1
Low Battery Detector (Extenal Reference Voltage)		-	-	-	-	-
Supply Voltage (V)		2.5 to 3.4	2.5 to 3.4	2.5 to 3.4	2.5 to 3.4	2.5 to 3.4
Power Consumption (μA) (Display Mode)		TYP.20 (at 3V)	TYP.20 (at 3V)	TYP.20 (at 3V)	TYP.20 (at 3V)	TYP.20 (at 3V)
Package		Chip/80QFP	Chip/100QFP	Chip/80QFP	Chip/100QFP	Chip/100QFP
Tooling (EV-Board)		Now	Now	Now	Now	Now

		SM3509	SM3512*1	SM3508	SM3511	SM3513*1
Application		100 Persons Data Bank	100 Persons Data Bank	156 Persons Data Bank	High End Data Bank	High End Data Bank
Built-in Program ROM Size (word (23-bit width))		8 k	8 k	12 k	24 k	24 k
Built-in Data RAM Size (byte)		2 k	8 k	3 k	0.5 k	0.5 k
Enternal Memory (byte)		8 k	8 k	3 M	64 M	64 M
LCD Display (seg. x com.)		60 x 9 (540 dots)	60 x 9 (540 dots)	74 x 16 (1 184 dots)	98 x 32 (3 136 dots)	74 x 32 (2 368 dots)
LCD Contrast Adjustable Level		-	-	16	16	16
IR Communication (External Ceramic Resonator)		-	-	O	O	O
I/O	Parallel I/O	8	8	8	8	8
	Output	2	2	2	3	3
	Buzzer Output	1	1	1	1	1
	Input	-	-	2	2	2
Key Matrix		14 x 6	14 x 6	16 x 5	16 x 5	16 x 5
ON Key		1	1	1*	1*	1*
Low Battery Detector (Extenal Reference Voltage)		-	-	-	O	O
Supply Voltage (V)		2.5 to 3.4	2.5 to 3.4	2.5 to 5.5	3.8 to 6.0	3.8 to 6.0
Power Consumption (μA) (Display Mode)		TYP.20 (at 3V)	TYP.20*2 (at 3V)	TYP.40 (at 3V)	TYP.50 (at 5V)	TYP.50*2 (at 5V)
Package		Chip/100QFP	Chip/100QFP	Chip/128QFP	Chip	Chip
Tooling (EV-Board)		Now	Now	Now	Now	Now

* Can be used as key matrix.
★1 : Under Development
★2 : Preliminary

SM3507

4-Bit Single-Chip Microcomputer (For Data Bank Use)

DESCRIPTION

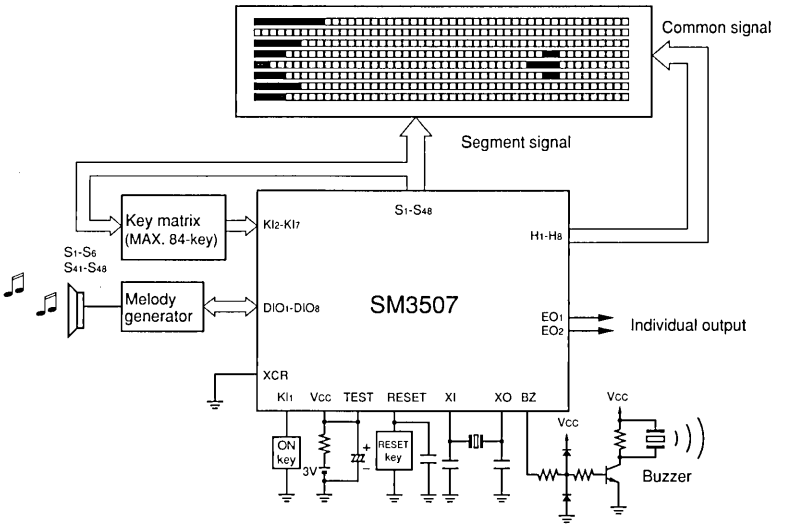
The SM3507 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key input circuit and buzzer output circuit. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

FEATURES

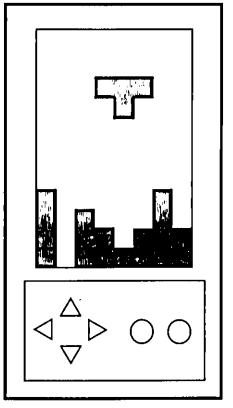
- ROM capacity :
  - Program ROM 6 k x 23 bits
  - Character ROM 4 x 8 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 48 x 8 bits
  - Data RAM 512 x 8 bits
- LCD display : 48 segment x 8 common
- I/O ports :
  - Parallel I/O 8 bits
  - Output 2 bits
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 250 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 12 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 80-pin QFP (QFP080-P-1420)
  - Chip (83-pad)

SYSTEM COMFIGURATION EXAMPLE

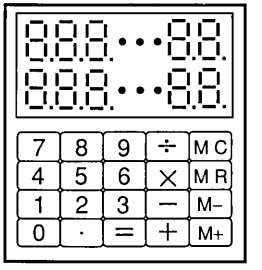
(FOR GAME APPLICATION)



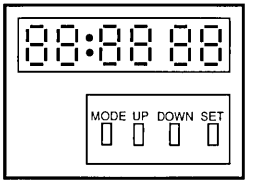
APPLICATION EXAMPLE



LCD GAME



DUAL LINE CAL.



WORLD TIME CLOCK

SM3503

4-Bit Single-Chip Microcomputer (For Data Bank Use)

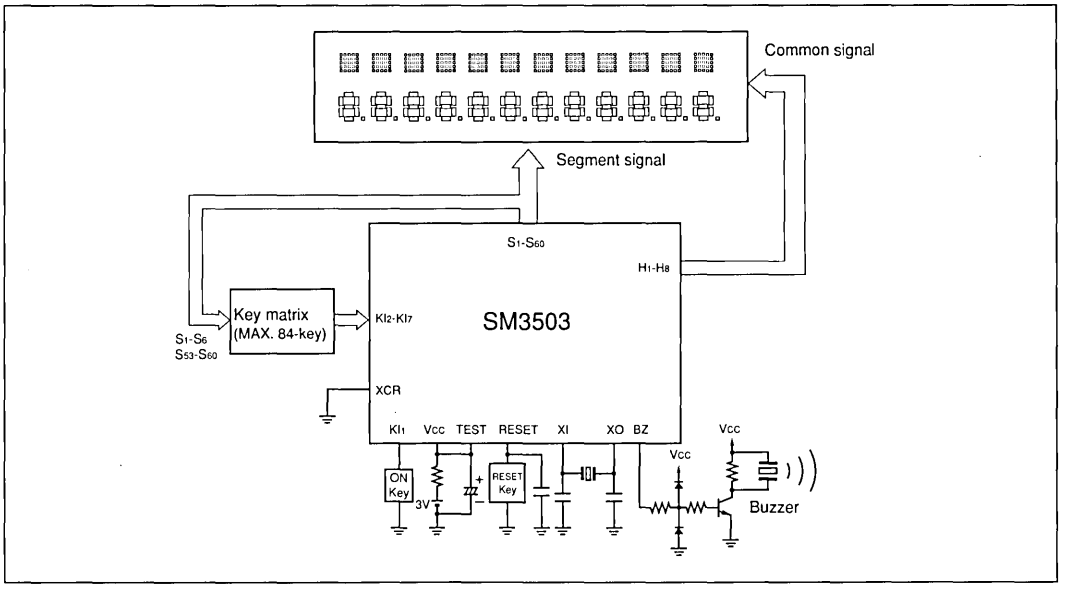
DESCRIPTION

The SM3503 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key input circuit and buzzer output circuit. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

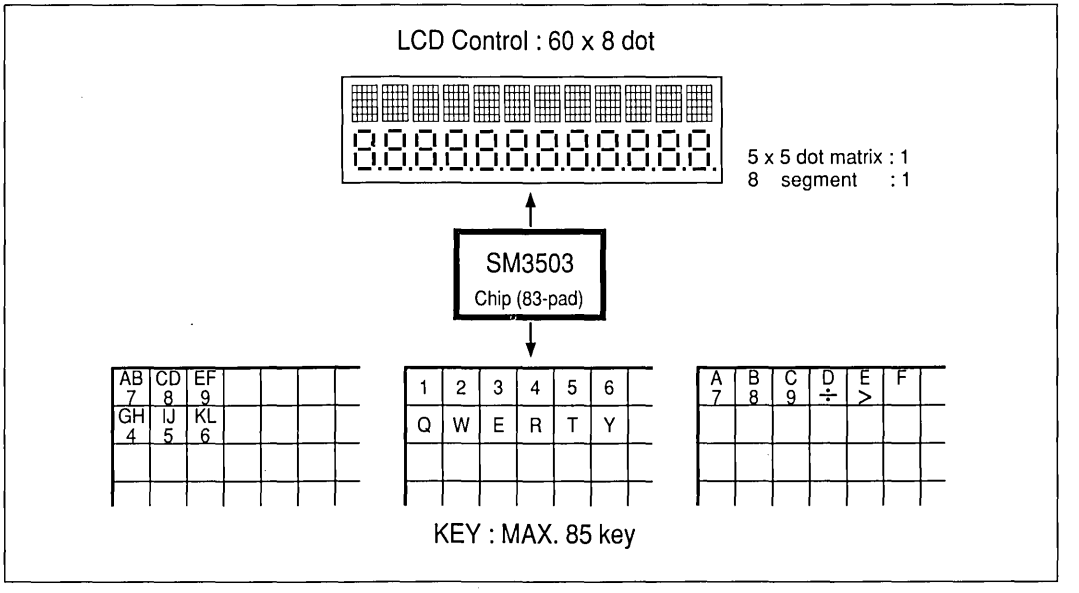
FEATURES

- ROM capacity :
  - Program ROM 6 k x 23 bits
  - Character ROM 5 x 8 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 8 bits
  - Data RAM 1 k x 8 bits
- LCD display : 60 segment x 8 common
- I/O ports :
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 250 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 12 µs
- Operating temperature : –10 to +60°C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 100-pin QFP (QFP100-P-1420)
  - Chip (84-pad)

SYSTEM COMFIGURATION EXAMPLE



APPLICATION EXAMPLE



SM3504

4-Bit Single-Chip Microcomputer (For Data Bank Use)

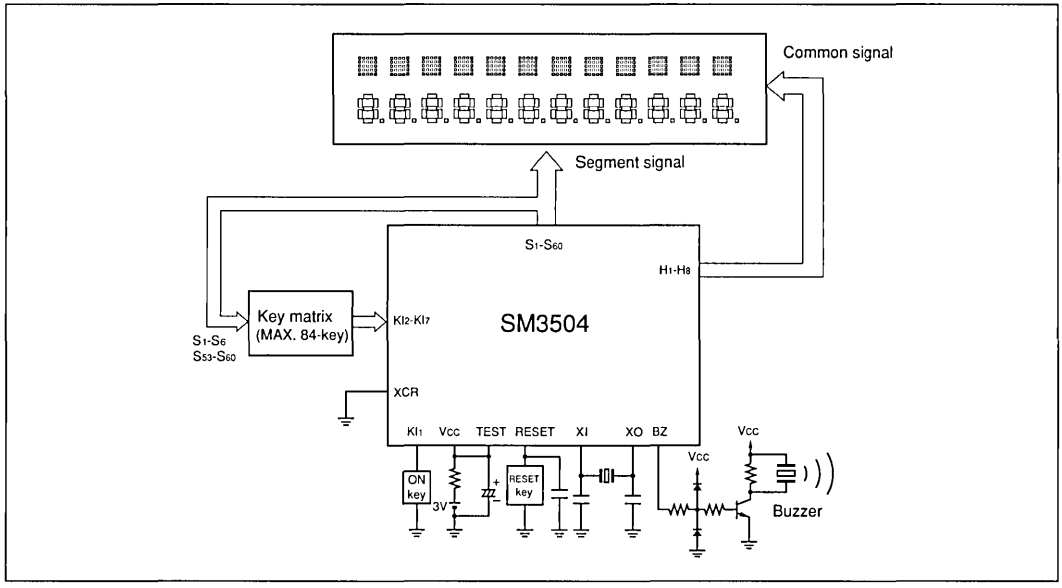
DESCRIPTION

The SM3504 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key input circuit and buzzer output circuit. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

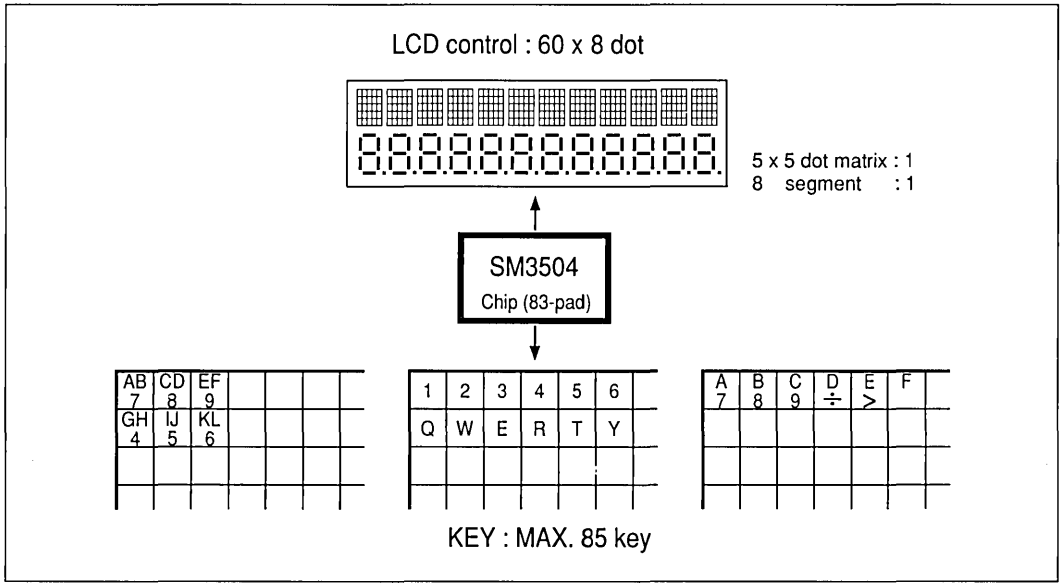
FEATURES

- ROM capacity :
  - Program ROM 6 k x 23 bits
  - Character ROM 5 x 8 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 8 bits
  - Data RAM 512 x 8 bits
- LCD display : 60 segment x 8 common
- I/O ports :
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 250 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 12 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 v
- Packages :
  - 80-pin QFP (QFP80-P-1420)
  - Chip (83-pad)

SYSTEM COMFIGURATION EXAMPLE



APPLICATION EXAMPLE



SM3514

4-Bit Single-Chip Microcomputer (For Data Bank Use)

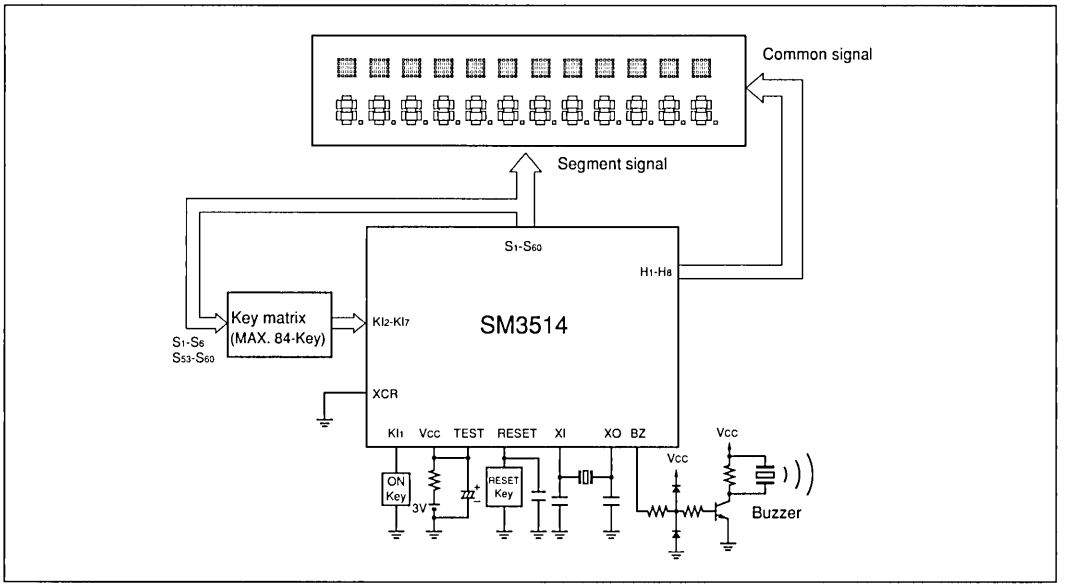
DESCRIPTION

The SM3514 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key input circuits and buzzer output circuit. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

FEATURES

- ROM capacity :
  - Program ROM 8 k x 23 bits
  - Character ROM 5 x 8 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 10 bits
  - Data RAM 512 x 8 bits
- LCD display : 60 segment x 8 common
- I/O ports :
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 300 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 10 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 100-pin QFP (QFP100-P-1420)
  - Chip (83-pad)

SYSTEM COMFIGURATION EXAMPLE



SM3515

4-Bit Single-Chip Microcomputer (For Data Bank Use)

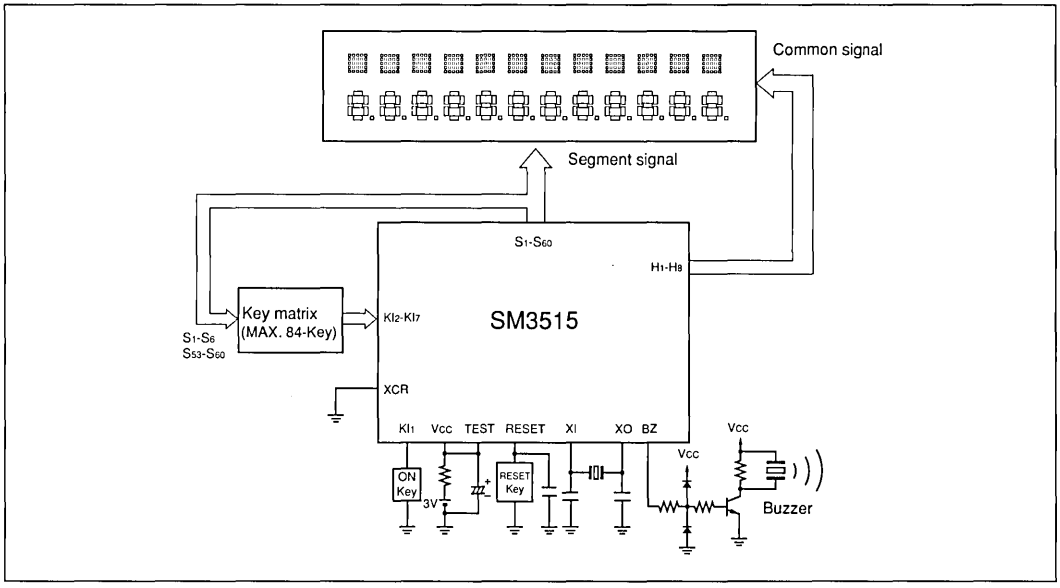
DESCRIPTION

The SM3515 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key input circuits and buzzer output circuit. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

FEATURES

- ROM capacity :
  - Program ROM 12 k x 23 bits
  - Character ROM 5 x 8 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 10 bits
  - Data RAM 512 x 8 bits
- LCD display : 60 segment x 8 common
- I/O ports :
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 300 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 10 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 100-pin QFP (QFP100-P-1420)
  - Chip (83-pad)

SYSTEM COMFIGURATION EXAMPLE



SM3509

4-Bit Single-Chip Microcomputer (For Data Bank Use)

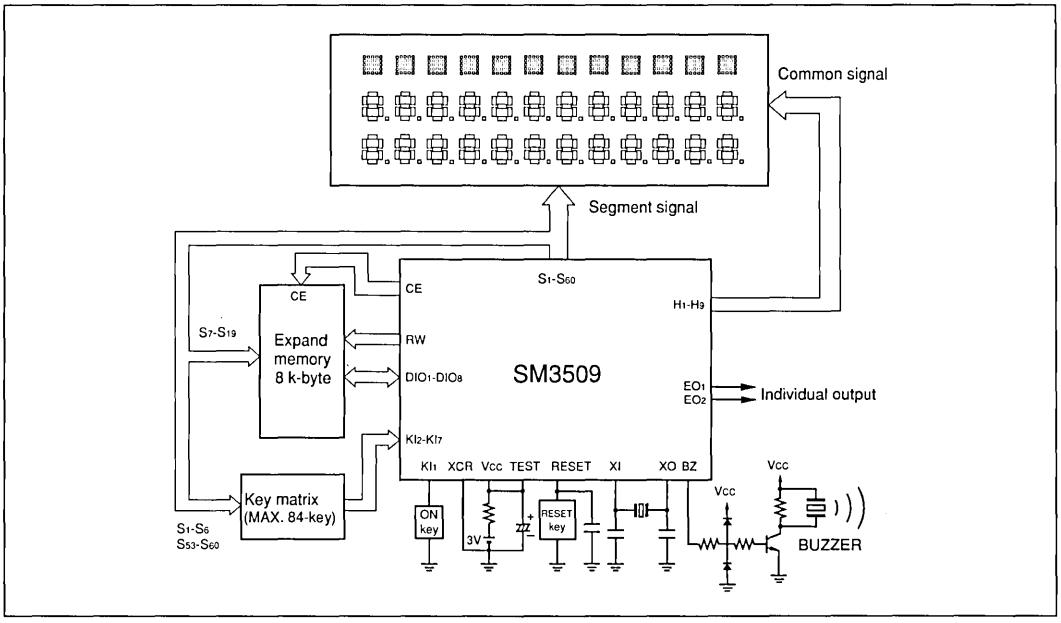
DESCRIPTION

The SM3509 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key/switch input circuit, 8-bit parallel I/O port, 2 output ports, external memory control circuit, and buzzer output circuit.

FEATURES

- ROM capacity :
  - Program ROM 8 k x 23 bits
  - Character ROM 5 x 9 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 9 bits
  - Data RAM 2 k x 8 bits
- Memory expansion (external) : 8 k x 8 bits
- LCD display : 60 segment x 9 common
- I/O ports :
  - Parallel I/O 8 bits
  - Output 2 bits
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 250 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 12 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 100-pin QFP (QFP100-P-1420)
  - Chip (98-pad)

SYSTEM COMFIGURATION EXAMPLE



SM3512

4-Bit Single-Chip Microcomputer (For Data Bank Use)

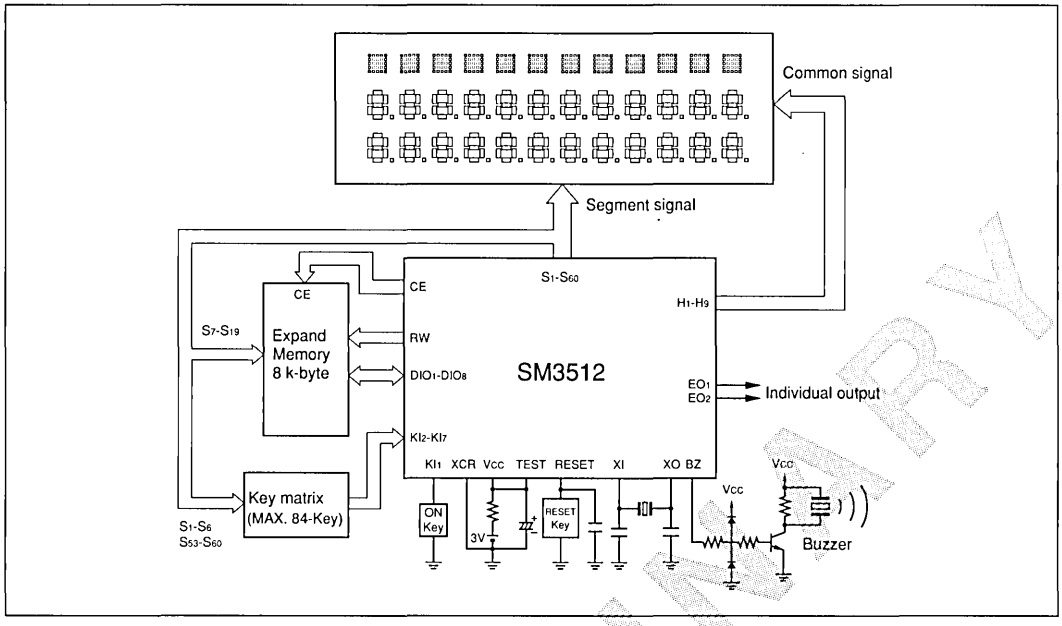
DESCRIPTION

SM3512 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver, key/switch input circuit, 8-bit parallel I/O port, 2 output ports, external memory control circuit, and buzzer output circuit.

FEATURES

- ROM capacity :
  - Program ROM 8 k x 23 bits
  - Character ROM 5 x 9 x 128 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 60 x 9 bits
  - Data RAM 8 k x 8 bits
- Memory expansion (external) : 8 k x 8 bits
- LCD display : 60 segment x 9 common
- I/O ports :
  - Parallel I/O 8 bits
  - Output 2 bits
  - Buzzer output 1 bit (4 kHz)
  - Key input 7 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 250 kHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 12 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 3.4 V
- Packages :
  - 100-pin QFP (QFP100-P-1420)
  - Chip (102-pad)

SYSTEM COMFIGURATION EXAMPLE



SM3508

4-Bit Single-Chip Microcomputer (For Data Bank Use)

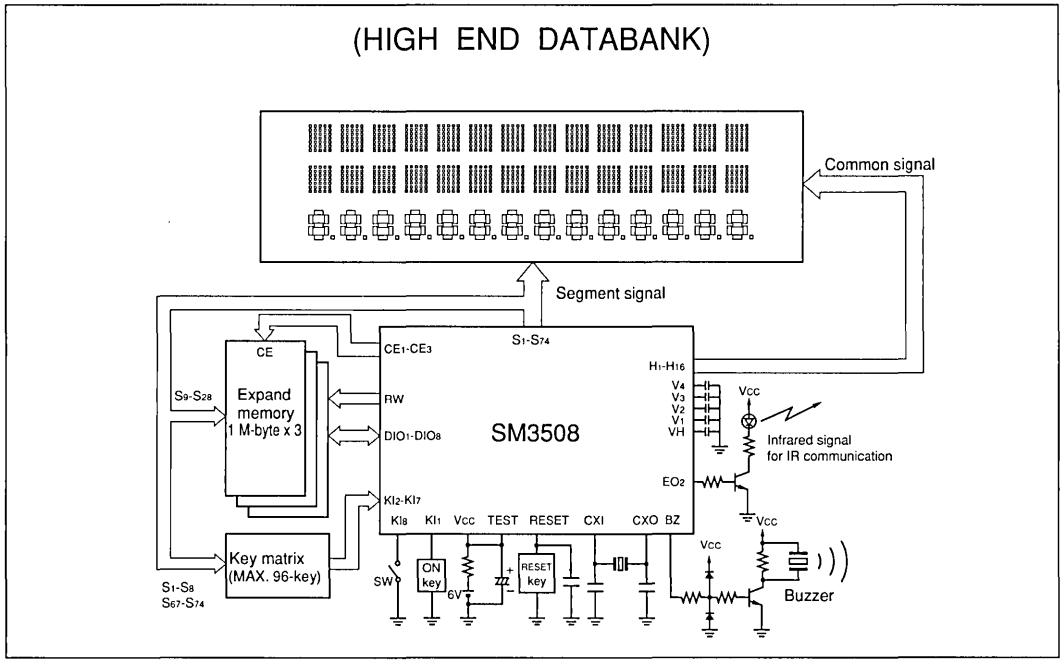
DESCRIPTION

The SM3508 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver (the output is adjustable in 16 steps for various contrast), key/switch input circuit, 8-bit parallel I/O port, 2 output ports and buzzer output circuit. The chip also has memory expansion controlling feature. One of two ports contains special output circuit for infrared(IR) communication. By connecting an external crystal, a 1Hz timer interrupt is made possible for easier clock function.

FEATURES

- ROM capacity :
  - Program ROM 12 k x 23 bits
  - Character ROM 6 x 8 x 256 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 74 x 16 bits
  - Data RAM 3 k x 8 bits
- Memory expansion (external) : 1M x 8 bits x 3
- LCD display : 74 segment x 16 common
- I/O ports :
  - Parallel I/O 8 bits
  - Input 2 bits
  - Output 2 bits
  - Buzzer outpu 1 bit (4 kHz)
  - Key input 6 bits
- Standby release : 2 events (2 Hz signal, key input)
- Built-in oscillator :
  - System clock (built-in CR oscillator) 1 MHz
  - (external ceramic resonator) 1 MHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 3 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 2.5 to 5.5 V
- Packages :
  - 128-pin QFP (QFP128-p-2828)
  - Chip (128-pad)

SYSTEM COMFIGURATION EXAMPLE



SM3511

4-Bit Single-Chip Microcomputer (For Data Bank Use)

DESCRIPTION

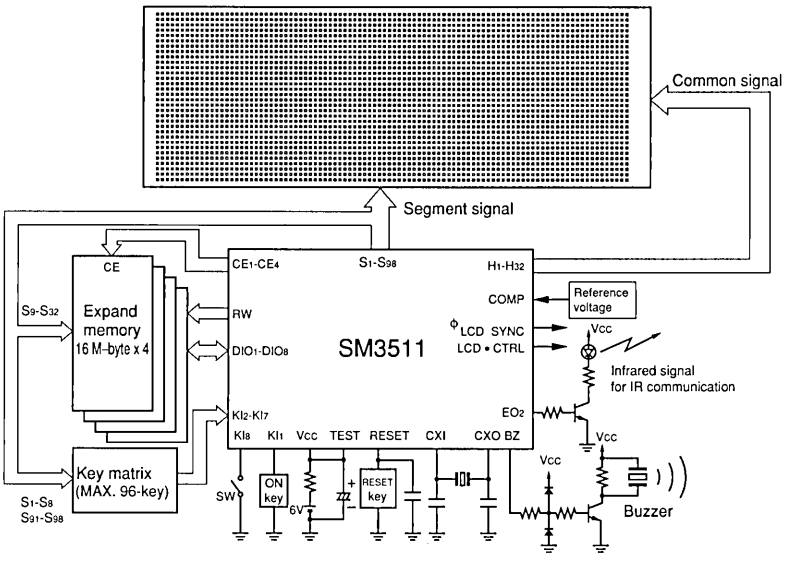
The SM3511 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver (the output is adjustable in 16 steps for various contrast), key/switch input circuit, 8-bit parallel I/O port, 3 output ports, external memory control circuit, buzzer output circuit and voltage detector circuit. One of three ports contains special output circuit for infrared(IR) communication. It is easy to realize timer function by timer signal interrupt since the oscillator circuit is built-in.

FEATURES

- ROM capacity :
  - Program ROM 24 k x 23 bits
  - Character ROM 6 x 8 x 256 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 98 x 32 bits
  - Data RAM 512 x 8 bits
- Memory expansion (external) : 16 M x 8 bits x 4
- Built-in battery detector
- LCD display : 98 segment x 32 common
- I/O ports :
  - Parallel I/O 8 bits
  - Input 2 bits
  - Output 3 bits
  - Buzzer output 1 bit (4 kHz)
  - Key input 6 bits
- Standby release : 2 events (Timer signal, key input)
- LCD contrast adjustable : 16 levels
- Built-in oscillator :
  - System clock (built-in CR oscillator) 1 MHz
  - (external ceramic resonator) 1 MHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 3 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 3.8 to 6.0 V
- Package : Chip (180-pad)

SYSTEM COMFIGURATION EXAMPLE

(HIGH END DATABANK)



SM3513

4-Bit Single-Chip Microcomputer (For Data Bank Use)

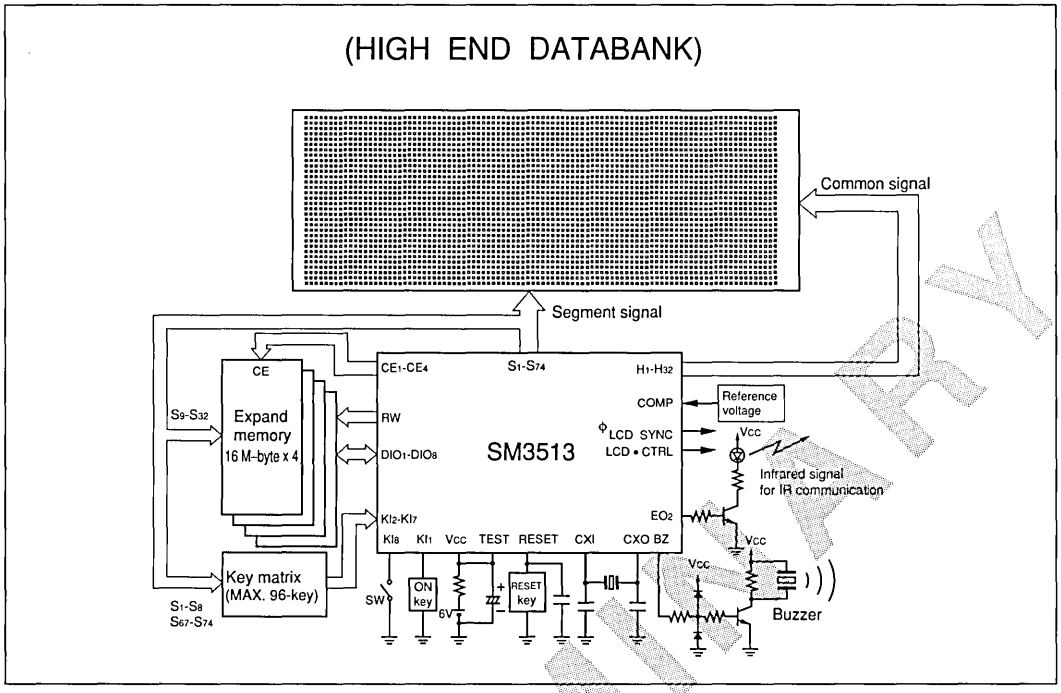
DESCRIPTION

The SM3513 is a CMOS 4-bit single-chip microcomputer for databank incorporating data memory RAM, LCD driver (the output is adjustable in 16 steps for various contrast), key/switch input circuit, 8-bit parallel I/O port, 3 output ports, external memory control circuit, buzzer circuit and voltage detector circuit. One of three ports contains special output circuit for infrared (IR) communication. It is easy to realize timer function by timer signal interrupt since the oscillator circuit is built-in.

FEATURES

- ROM capacity :
  - Program ROM 24 k x 23 bits
  - Character ROM 6 x 8 x 256 bits
- RAM capacity :
  - Working RAM 256 x 4 bits
  - Display RAM 74 x 32 bits
  - Data RAM 512 x 8 bits
- Memory expansion (external) : 16M x 8 bits x 4
- Buil-in battery detector
- LCD display : 74 segment x 32 common
- I/O ports :
  - Parallel I/O 8 bits
  - Input 2 bits
  - Output 3 bits
  - Buzzer output 1 bit (4 kHz)
  - Key input 6 bits
- Standby release : 2 events (Timer signal, key input)
- LCD contrast adjustable : 16 levels
- Built-in oscillator :
  - System clock (built-in CR oscillator) 1 MHz
  - (external ceramic resonator) 1 MHz
  - Timer (built-in CR oscillator) 32.8 kHz
  - (external crystal) 32.768 kHz
- Instruction cycle time : 3 µs
- Operating temperature : –10 to +60 °C
- Supply voltage : 3.8 to 6.0 V
- Package : Chip (156-pad)

SYSTEM COMFIGURATION EXAMPLE



PRECAUTIONS FOR SINGLE-CHIP MICROCOMPUTERS

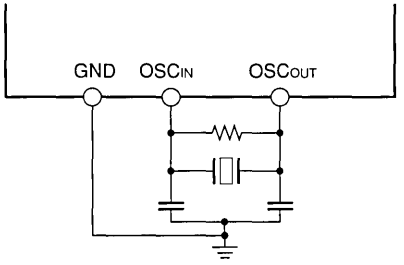
PRECAUTIONS FOR SINGLE-CHIP MICROCOMPUTERS

Installation Considerations-Mounting OSC on PCB

When mounting LSI and oscillation circuit on PCB, observe the following precautions to minimize stray capacitance of wiring and noise interference.

1) All wirings to/from oscillator must be as short as possible. Capacitor and crystal must be placed close to the LSI.
2) Do not connect GND of oscillator to return line of high current circuit.
3) Do not derive clock directly from oscillator wirings, leads.
4) On a multi-layered PCB, do not intercross oscillator pattern and other circuit pattern.
5) Do not run patterns carrying high current near the oscillator.
6) Connect ground lead of capacitor directly to GND of LSI to eliminate potential difference. This also minimizes stray capacitance of wiring and leads.
7) Stray capacitance of wiring to GND and V_{DD} of LSI must be minimum.

Recommended OSC circuit connection

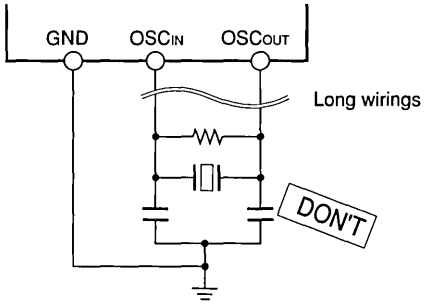


Preferable connection practice

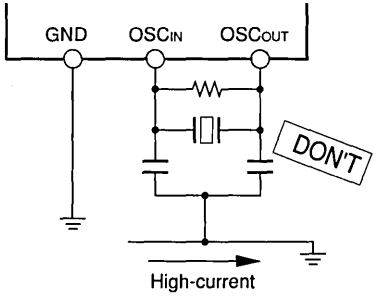
- Short wiring. Short distance between LSI and oscillator.
- No direct clock output.
- No high-current return is connected.
- No intercross with wiring from/to other circuit(s).
- All returns of oscillation circuit are at the same potential.
- No high-current pattern running nearby.

Undesirable Oscillator Circuit Connections

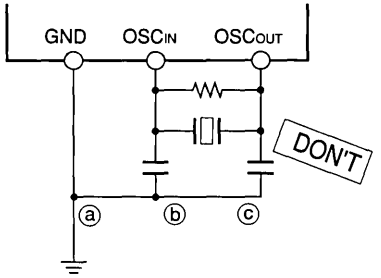
• Long wiring. Crystal is not close to LSI.



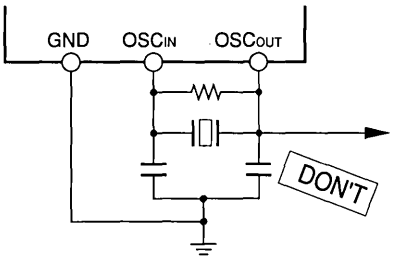
• GND of oscillator is connected to return path of High-current.



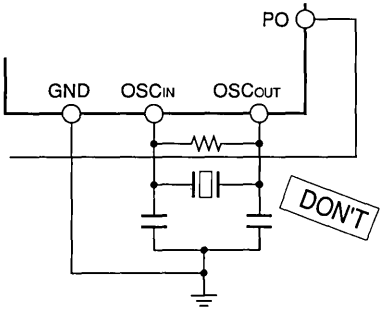
• Current flows on line connecting ground points of oscillator. Voltage drops occurs across points a, b and c.



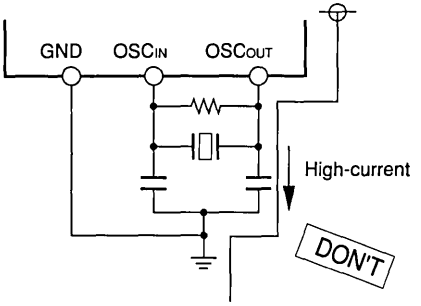
• Clock is directly output.



• (Multi-layered PCB) Oscillator wiring and another wiring intercross.



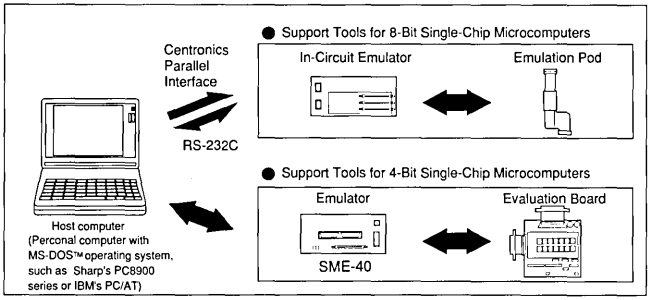
• Pattern carrying High-current runs along oscillator.



DEVELOPMENT SUPPORT SYSTEMS

DEVELOPMENT SUPPORT SYSTEMS

The development support systems for 8-bit single-chip microcomputers are configured with a host computer and an appropriate in-circuit emulator.
The development support systems for 4-bit single-chip microcomputers are configured with a host computer and dedicated debugging tools (an emulator and an evaluation board). The SME-40 is a currently available high-performance SM emulator.



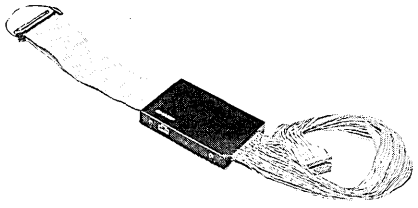
8-Bit Single-Chip Microcomputer Development Support Systems

In-circuit Emulator

This emulator helps develop 8-bit single-chip microcomputer programs efficiently.
It implements the functions of a single-chip microcomputer, allowing PC-based program entry and debugging.

Emulation Pod

This emulation pod connects an emulator to a user system.
It has a probe cable for external signals.



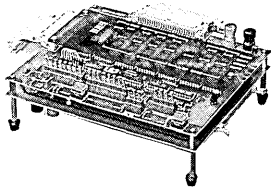
4-Bit Single-Chip Microcomputer Development Support Systems

Emulator

This emulator expedites the development of 4-bit single-chip microcomputer programs.
An evaluation board connected to an SME-40 emulator allows program development plus PC-based program entry and debugging.

Evaluation Board

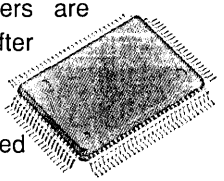
Evaluation boards provide the functions of a single-chip microcomputer running in a user system. An evaluation chip and an EPROM socket are mounted on the board.
An evaluation board connected to an SME-40 emulator permits programs to be run in the emulator.



One-Time Programmable Microcomputer

8-bit single-chip microcomputers with one-time-programmable (OTP) memory are pin compatible with SM8300 series microcomputers. Data can be witten to their program ROM once only in the same way as a EPROM is written to.

When OTP microcomputers are installed in user systems after memory writing, they function in the same way as masked ROM devices used for evaluation or production.



Microcomputer with Built-In Flash Memory

Microcomputers with built-in flash memory are pin compatible with SM8500, SM6000 series microcomputers.

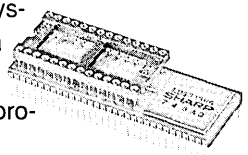
Data can be rewritten repeatedly to their program ROM in three write modes of PROM mode, copy mode and serial transmit mode(on-board mode). When the microcomputers with built-in flash memory are installed in user systems after memory writing, they function in the same way as masked ROM devices used for evaluation or production.

Evaluation Chip

An evaluation chip is a program debugging LSI device to which an external memory module can be connected in place of the internal ROM of a single-chip microcomputer.

Piggyback

Piggyback chips have a double stacking structure in which an EPROM socket is mounted on an evaluation chip housed in a regular IC pakage. They can be installed in user systems to allow evaluation in a physical package similar to that used in mass production.



★ Under development

8-Bit Single-Chip Microcomputer Development Support Tools

Model No.	In-Circuit Emulator		Evaluation Chip	Piggyback	OTP Microcomputer
	Unit	Emulation Pod			
SM8311/3/4/5	LU8300H7	LU8313H4	LU8313H5	LU8313H6	LU8311P0/P1
SM8502*/3*/4/5*/6	Refer to page 379				★LU8500F0/F1*

* Microcomputers with built-in flash memory.

Support Tool	Features	
In-circuit emulators (LU8300H7)	• 64k-byte emulation memory	• Line assembler and reverse assembler
	• RS232C interface to host	• Centronics interface
	• Instruction cycle time count	• Coverage function
	• Real-time trace function	• Structured assemler for SM8300

★ Under development

4-Bit Single-Chip Microcomputer Development Support Tools

SME-40 System
• Target microcomputers : 4-bit single-chip microcomputers • Emulator : SME-40 (LU4DH400) • Evaluation board • Host computer Personal computer with MS-DOS™ operating system • Optional software : Cross-assembler/Mapper Emulator software

Supported MPU	Evaluaton Board	Piggyback / OTP
SM3503/04/14	LI3504H2	–
SM3507	LI3504H2*1	–
SM3508	LI3508H2	–
SM3509	LI3502H2	–
SM3511/13*	LI3511H2	–
★SM3512	LI3512H2	–
SM3515	LI3515H2	–
SM3903	–	–
SM3905	–	–
SM563	LU563H2	LU563H6
SM565	LU565H2	LU565H6
SM5K4/5K5	LU5K5H2	LU5K5P0/P1/P2/P5/P6/P7*2
SM5K6	★LU5K6H2	★LU5K6P00/P10/P20/P50/P60/P70*2
SM5L1/5L2/5L3	LU5L1H2	–

*1 Evaluation chip : LI3507H5
*2 OTP microcomputer

★ Under development

16-Bit/8-Bit Single-Chip Microcomputers, 32-Bit RISC Microcomputer Development Support Tools

The development support tools for 16-bit/8-bit microcomputers and 32-bit RISC microcomputer are supplied by the YOKOGAWA Digital Computer Components.

Supported MPU	Support tool		Package
SM8311/13/14/15	Emulator advice	AD200-S56/PP001	64SDIP
SM8502*/03*/04/05*/06		AD200-S56/PP150	100QFP 100QFP*
★SM6003/04/05		★	100QFP 100QFP*
ARM7D Core		★	QFP, PGA, etc.

* 0.5mm pin-pitch advice is the registered trademark of YOKOGAWA Digital Computer Corporation.

Debbuger	Supported MPU	Language
microVIEW	SM8311/13/14/15	Assembler
	SM8502*/03*/04/05*/06	Assembler, Structured assembler/C compiler by ADaC
	★SM6003/04/05	Structured assembler/C compiler by ADaC
	ARM7D Core	C compiler confirming to ANSI by ARM

ADaC : Advanced Data Controls Corp. ARM : Advanced RISC Machines, Ltd.

FEATURES

	SM8300 Series (SM8311/13/14/15)	SM8500 Series (SM8502*/03*/04/05*/06)	★SM6000 Series	ARM7D Core
CPU core	8-bit CPU	8-bit CPU	16-bit CPU	32-bit RISC CPU
ROM (byte)	8k to 32k	24k to 60k	16k to 96k	Selectable at user's option
RAM (byte)	512 to 1k	1k to 2k	512 to 3.5k	
I/O	52	84	88	
Operating voltage	2.7 to 5.5 V	1.8 to 5.5 V	2.5 to 5.5 V	2.7 to 5.5 V
Instruction cycle	500ns (at 5V)	330ns (at 5V)	67 ns (at 5 V)/100 ns (at 3 V)	30 ns (at 5 V)/50 ns (at 3 V)
Remarks	• A/D converter • Zero cross detector circuit • Pulse width measuring function • SIO	• Timer 16-bit x 1 • Timer 8-bit x 7 • A/D converter • D/A converter • UART/SIO	• Timer/counter 16-bit x 6 • A/D converter • D/A converter • PWM • UART/SIO	• DMAC • INTC • IOC/BUSC • RTC • 82CXX series etc.
Application	Office Automation equipment, Home appliances	Communication equipment, Home appliances	Audio visual equipment, Bussiness equipment	PDA etc.

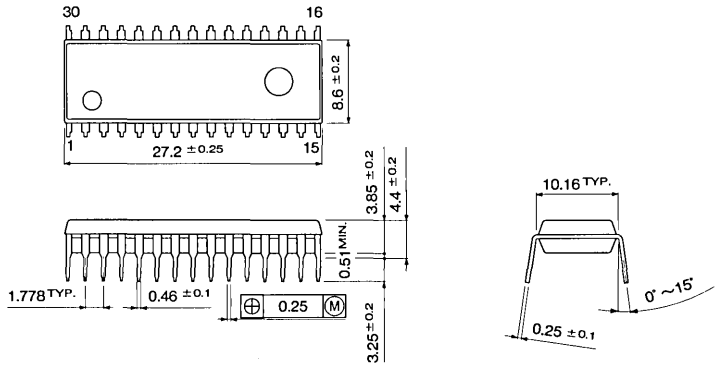
ARM is the trademark of Advanced RISC Machines, Ltd.

PACKAGING

Package Outline

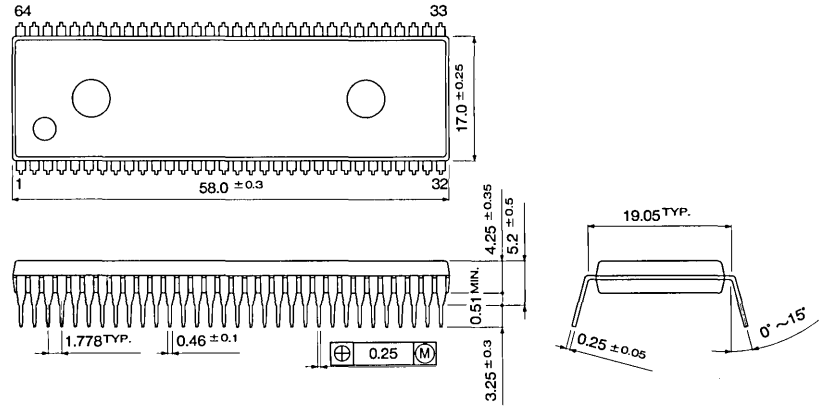
(Unit : mm)

30 SDIP (SDIP030-P-0400)

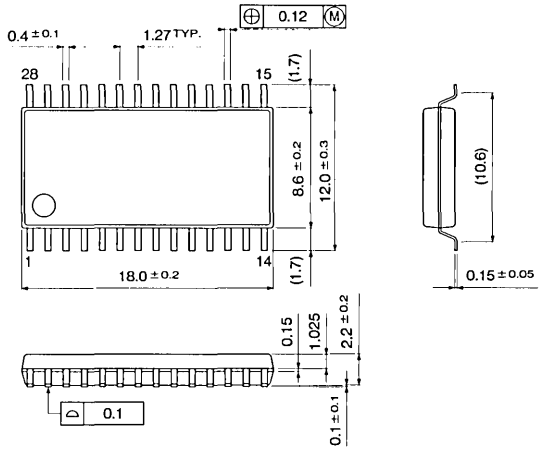


SDIP : Shrink DIP*
SOP : Small Outline Package
QFP : Quad Flat Package
LQFP : Low Profile QFP
*DIP : Dual In-line Package

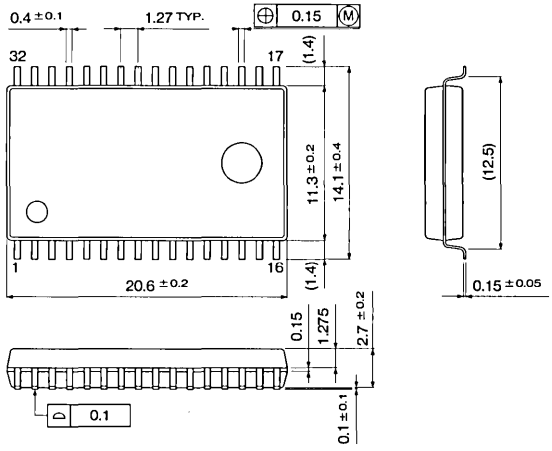
64 SDIP (SDIP064-P-0750)



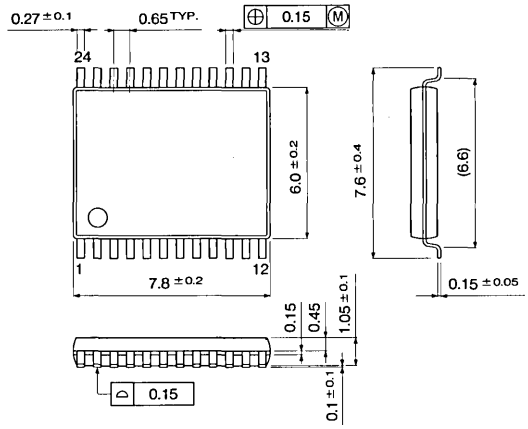
28 SOP (SOP028-P-0450)



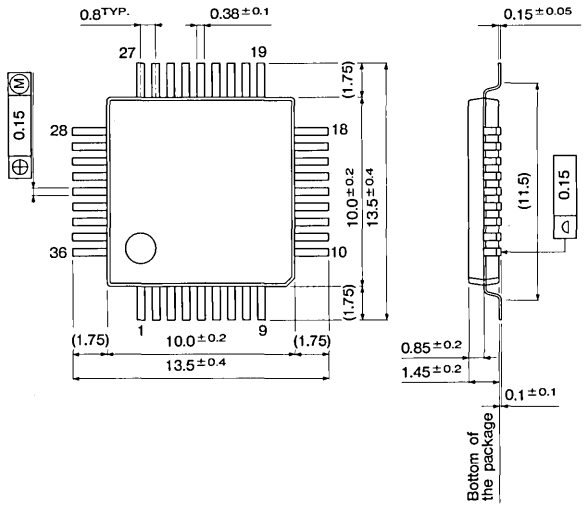
32 SOP (SOP032-P-0525)



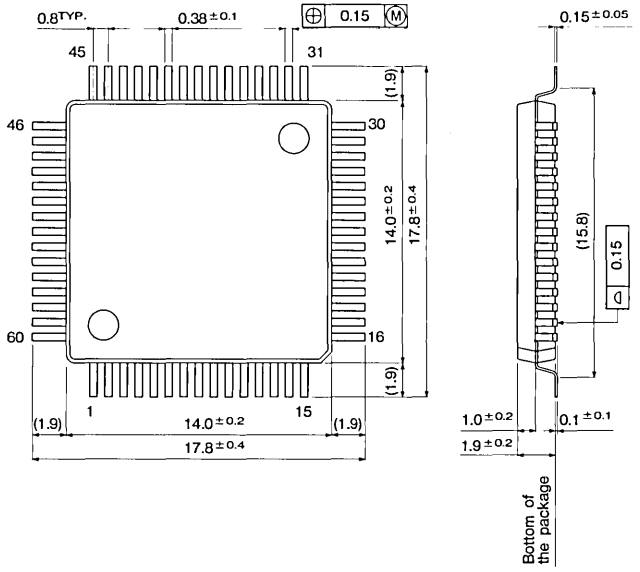
24 SSOP (SSOP024-P-0275)



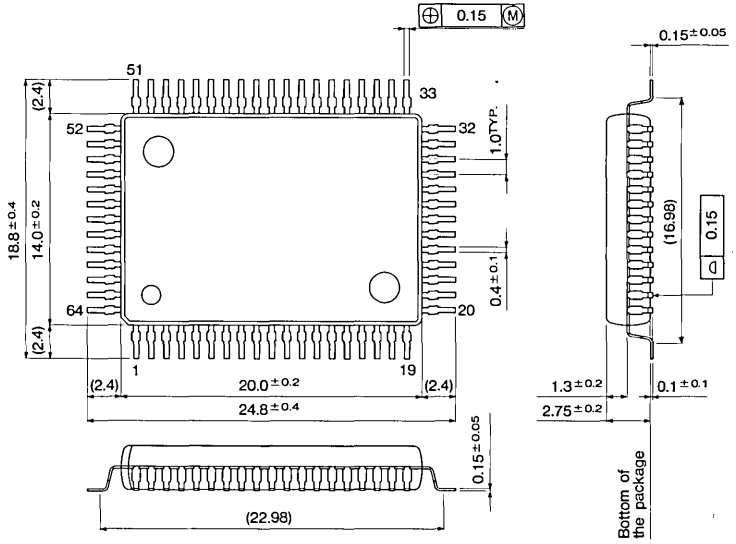
36 QFP (QFP036-P-1010)



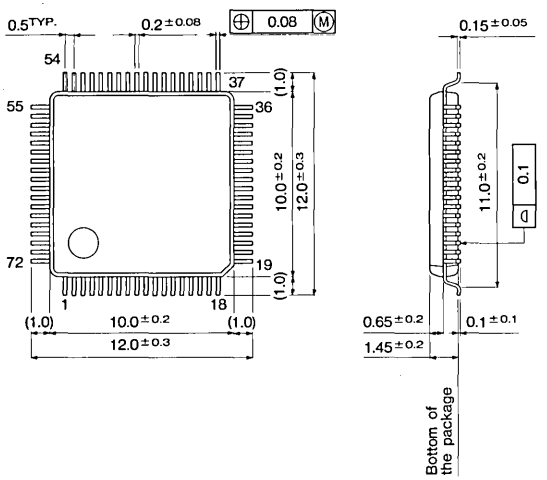
60 QFP (QFP060-P-1414)



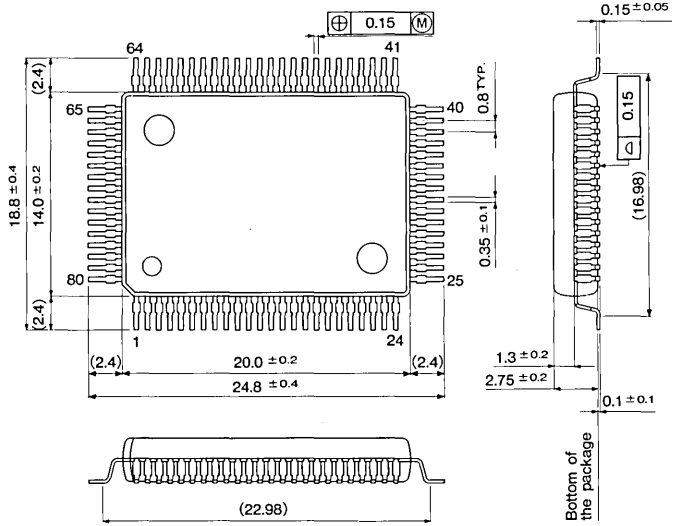
64 QFP (QFP064-P-1420)



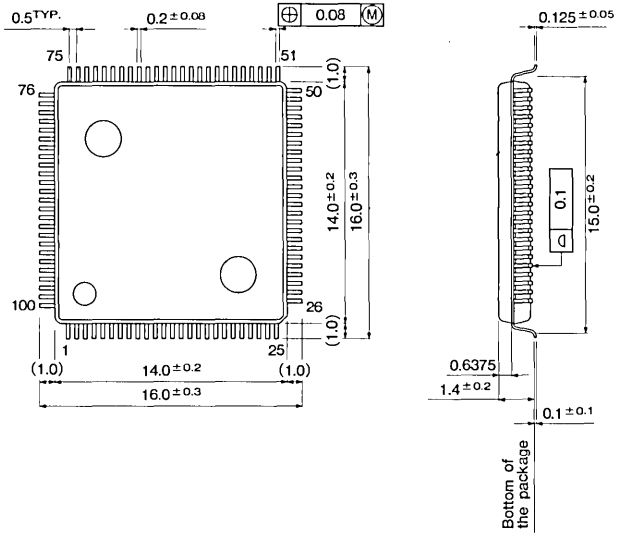
72 QFP (QFP072-P-1010)



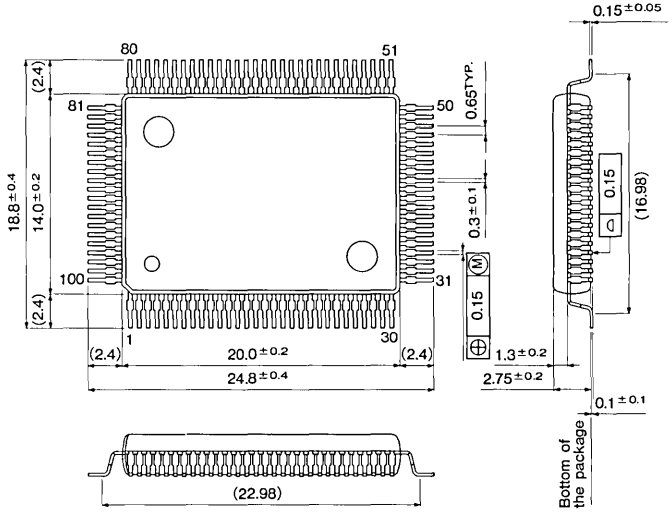
80 QFP (QFP080-P-1420)



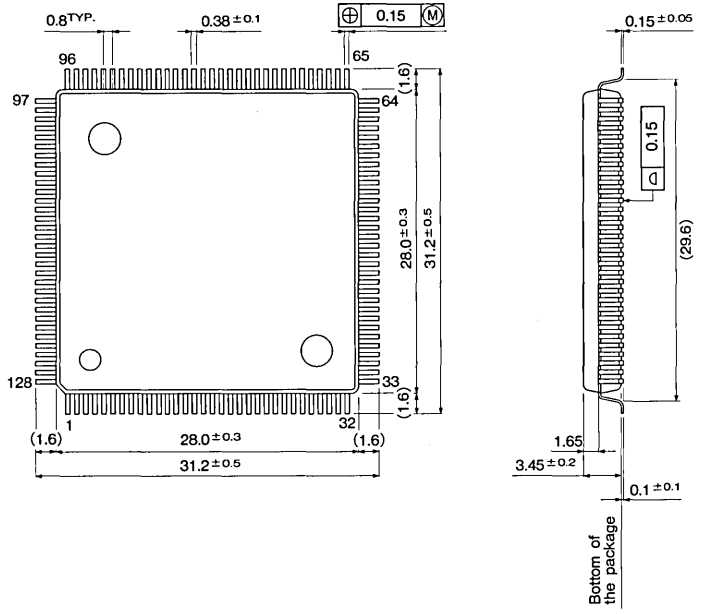
100 LQFP (LQFP100-P-1414)



100 QFP (QFP100-P-1420)



128 QFP (QFP128-P-2828)



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