DISTRIBUTED LOGIC CORP.

DILOG

INSTRUCTION MANUAL

FOR

MODEL DQ120

TAPE CONTROLLER

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FORWARD

This INSTRUCTION MANUAL is intended to assist engineering personnel in maintaining an LSI-11 based computer system that contains a DISTRIBUTED LOGIC CORPORATION DQ120 controller. The material assumes a knowledge of the operation of the LSI-11 based computer, experience in troubleshooting digital logic circuits, and a basic understanding of digital computer theory. For ease of reference, the material in a companion document entitled "USER'S GUIDE FOR MODEL DQ120 TAPE CONTROLLER" is duplicated as the first four sections of this manual.

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SECTION I

GENERAL DESCRIPTION

1.0 INTRODUCTION

This material defines the functional characteristics of a magnetic tape controller that interfaces LSI-11 based computer systems to industry-standard 7- and 9-track magnetic tape transports. Magnetic tape transports from manufacturers other than DEC* can be used while still retaining software and format compatibility with TM11 tape systems. The controller is completely contained on one quad module that occupies two device locations in the backplane. Data transfers are via the DMA facility of the LSI-11. Transfer rates vary, depending on the density and speed of the transports included in the system, between 2,500 and 90,000 characters per second.

From one to four tape transports may be connected to the controller. The transports can be either seven or nine track units reading or writing on one-half inch magnetic tape in NRZI format with densities of 200, 556, or 800 characters per inch (CPI). Recording formats conform with ANSI standards X3.14-1972 and X3.22-1973 Recorded Magnetic Tape For Information Interchange (200 and 800 CPI, NRZI).

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read only memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self test is done automatically each time power is applied. A DIAGNOSTIC indicator on the board lights if self-test passes. If self-test fails, the controller has an AUTOMATIC DATA PROTECT feature that stops the CPU from interacting with the tape and thus prevents writing erroneous information into critical data base areas.

Two additional indicators on the controller board display dynamic operating conditions to an operator. The conditions displayed are controller BUSY and controller transferring data (DMA busy).

A 50-pin connector, located near the top center of the controller, terminates a shielded ribbon cable through which signals are transferred between the controller and tape drives.

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1.1 GENERAL DESCRIPTION

The DQ120 Magnetic Tape Controller links an LSI-11 based computer to one or more tape drives. The controller permits information to be read and written on tape in industry-compatible format; therefore data can be transferred between the LSI-11 system and other computers, either small or large scale, and of various manufacturers (DEC, IBM, Data General, Honeywell, etc.). The controller performs the following major functions:

a. Buffers and interlocks data and status transfers across the computer I/O bus.

b. Controls the timing and the format of data transfers between the computer and the tape units.

c. Monitors the status of the tape units and the quality of the data transferred onto the tape and presents this information to the computer.

d. Generates all the control signals to the tape units, i.e., start, stop, rewind, generate IRG gap, generate EOF gap and tape mark, etc.

The controller can link up to four tape units to the computer in various configurations. Table 1-1 lists various configurations. Figure 1-1 illustrates a simplified system.

A high-speed microprocessor is the control and timing center of the controller. PROMs on the controller board provide control instructions for the microprocessor, contain configuration-control information, and serve as general purpose logic elements. The microprocessor also optionally permits automatic self tests of the controller board.

1.1.1 LSI-11 Q Bus Interface

Commands, data, and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O interrupt control. Data transfer rates are from 1,250 to 45,000 16-bit words per second, depending upon tape packing density and tape drive speed. Controller/Q bus interface lines are listed in Table 1-2.

TABLE 1-1: Magnetic Tape Configurations

TAPE REEL SIZE	10-1/2 INCH	8-1/2 INCH	7 INCH
CHARACTERISTICS			
Tape Type	Computer Grade 0.5 inch wide		
Tracks	7 or 9		
Format	NRZI IBM and ANSI compatible.		
Data Density	7 track - 200/556/ 800 cpi 9 track - 800 cpi		
Tape Speed Range	12.5 to 112.5 ips	12.5 to 37.5	12.5 to 37.5 ips
Tape Reel Capacity	2,400 feet	1,200 feet	600 feet
Tape Handling	Tension arm to 45 ips Vacuum column at 75 and 112.5	Tension arm	Tension arm
Rewind Speed	150 to 200 ips	120 ips	120 ips
Physical Dimensions	24"Hx19"Wx10" to 18"D	12.5"Hx19"W x13"D	8.75"Hx19"Wx13"D
Mounting	Standard EIA rack mount		
Weight	90 pounds max	50 pounds	40 pounds
Power	115VAC ±10%, 47-400Hz		
Operating Temperature	35°F to 122°F		
Humidity	15% to 95% non-condensing		
Altitude	0 - 30,000 feet		

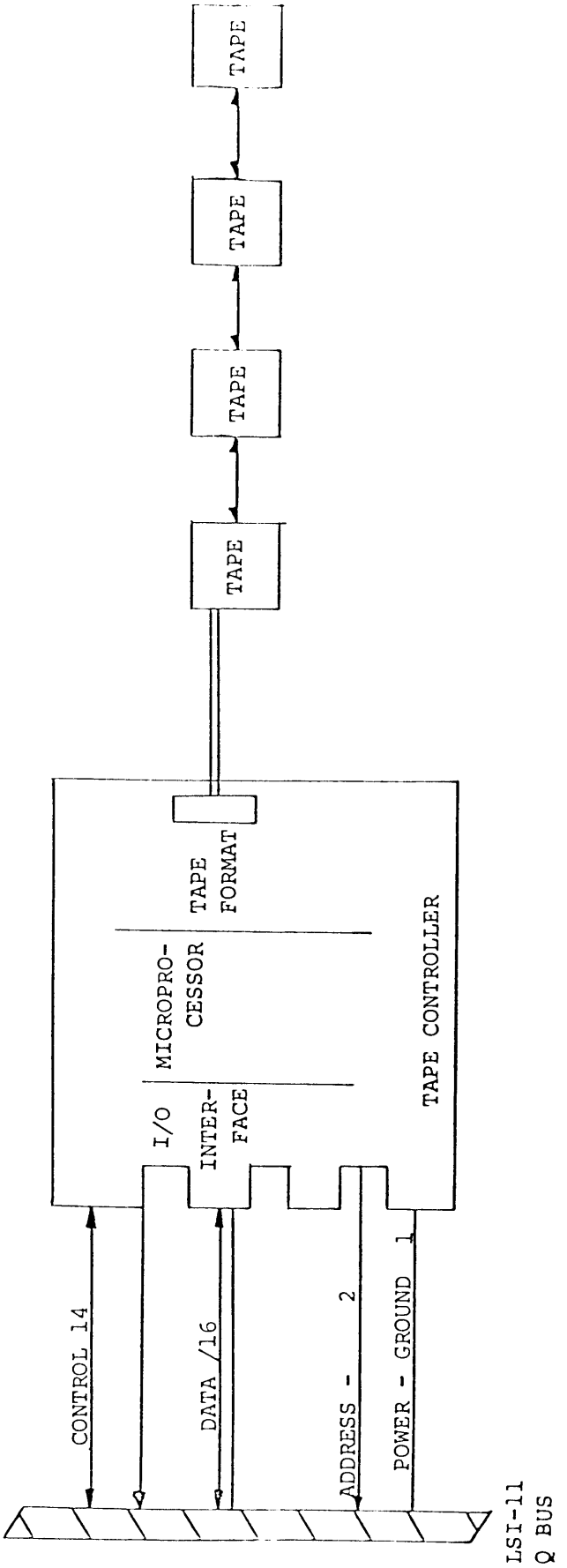


FIGURE 1-1: TAPE CONTROLLER SIMPLIFIED DIAGRAM

TABLE 1-2: Controller/Qbus Interface Lines

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AJ1,AM1, RT1	GND		Signal Ground and DC Return
AN1	BDMR L	To	Direct Memory Access (DMA) request from controller: Active low
AP1	BHALT L	To	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	From	Memory Refresh. Not used.
BA1	BDCOK H	From	DC Power OK. All DC voltages are normal.
BB1	BPOK H	From	Primary power OK. When low activates power fail trap sequence.
J1,BM1,BT1,BC2	GND		Signal Ground and DC return.
BN1	BSACK L	To	Select acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	To	External Event Interrupt Request. Not used.
BV1,AA2,BA2	+5	From	+5 volt system power.
AD2,BD2	+12	From	+12 volt system power.
E2	BDOUT L	From/To	Data out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	From/To	Reply from slave to BDOUT BDIN and during IAK.
AH2	BDIN L	From/To	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNCL	From/To	Synchronize: becomes active when master places address on bus; stays active during transfer.
K2	BWTBT L	From/To	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	B1RQ L	To	Interrupt Request
AM2 AN2	B1AK1 L B1AK0 L	From/To	Serial interrupt acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain.
AP2	BBS7 L	From/To	Bank 7 select. Asserted by bus master when addresses in upper 4K bank (28-32K words) are placed on the bus.
AR2 AS2	BDMG1 L BDMGO L	From/To	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.

(more)

'LE 1-2: Controller/QBus Interface Lines, continued

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AT2	BINIT L	From	Initialize. Clears devices on I/O bus
AU2,AV2	BDAL0/DAL1	From/To	Data/address lines 0 & 1, (2 of 16)
BE2,BF2,BH2	BDAL2	From/To	Data/address lines, 2-15, (14 of 16)
BJ2,BK2,BL2	through		
BM2,BN2,BP2	BDAL 15		
BR2,BS2,BT2			
)U2,BV2			

1.1.2 Interrupt

The interrupt vector address is factory set to address 224, which is compatible with TM11 software. Interrupts are generated when processor attention is required or when an error occurs.

1.1.3 Tape Interface

The controller interfaces with the tape drive, or first of a series of tape drives, through the 50 pin 3M connector at the top, center of the controller board. A series of tapes are connected to the controller in a daisy chain manner. The maximum cable length from the controller to the last tape drive in a series string is 20 feet. A ribbon cable connects the controller to the tape drives. Table 1-3 lists the controller to tape drive interface lines.

1.2 SPECIFICATIONS

. Data Format:	Industry standard non-return-to-zero (NRZ) recording.
	7 or 9 tracks
	7 track recording density: 200, 556, or 800 characters per inch; program selectable.
	9 track recording density: 800 characters per inch.
	Interrecord gap, 7 track: 0.75 inch min , 9 track: 0.60 inch min
	Tape parity marks: 7 track - LPC, LRC 9 track - LPC, CRC, LRC

TABLE 1-3: Controller To Tape Interface Lines

PIN	MNEMONIC	TO/FROM TAPE	DESCRIPTION
6	$\overline{RD0}$	From	Read line bit 0 (eighth bit)
20	$\overline{RD1}$	From	Read line bit 1
14	$\overline{RD2}$	From	Read line bit 2
15	$\overline{RD3}$	From	Read line bit 3
5	$\overline{RD4}$	From	Read line bit 4
11	$\overline{RD5}$	From	Read line bit 5
8	$\overline{RD6}$	From	Read line bit 6
16	$\overline{RD7}$	From	Read line bit 7 (first bit)
25	$\overline{EOT}$	From	End of tape mark
24	$\overline{RDS}$	From	Read data strobe
17	$\overline{ONL}$	From	On Line
9	$\overline{BOT}$	From	Beginning of tape mark
10	$\overline{7TRK}$	From	7 Track: Asserted is 7 track, $\overline{Asserted}$ is 9 track
18	$\overline{RDP}$	From	Read parity line
13	$\overline{FLPT}$	From	File Protect
12	$\overline{RWS}$	From	Rewind Status
9	$\overline{TRDY}$	From	Tape Ready Status
33	WD 0	To	Write data line bit 0 (eighth bit)
41	WD 1	To	Write data line bit 1
36	WD 3	To	Write data line bit 3
40	WD 5	To	Write data line bit 5
39	WD 7	To	Write data line bit 7 (first bit)
34	SRC	To	Space Reverse Command
35	DSL	To	Density Select
45	WD 4	To	Write data line bit 4
48	WD 2	To	Write data line bit 2
49	WD 6	To	Write data line bit 6
46	SWS	To	Set Write Select
50	WDS	To	Write Data Strobe
47	OFC	To	Off Line Command
29	WDP	To	Write data parity line
30	RWC	To	Rewind command
23	SFC	To	Space forward command
27	WARS	To	Write amplifier reset
3,4,22,2	SEL1-SEL4	To	Drive Select, four lines
1,21,32	GND		Ground

	Industry standard 7 track tape records contain from 24 to 4,008 characters; 9 track records contain from 18 to 2,048 characters. Byte order recorded or read is switch selectable: DEC = LSB first; IBM = MSB first.

- Media Characteristics:

Type -	1/2" wide mylar base, oxide coated, magnetic tape.
Reel Size -	7", 8-1/2", or 10-1/2" diameter tape reels containing 600, 1,200 and 2,400 feet of tape respectively.
Data Capacity -	Assumes 800 CPI and approximate 70% recording efficiency: 600 feet, 5.75 million characters 1,200 feet, 11.5 million characters 2,400 feet, 22 million characters
Data Transfer Rate -	Assumes 800 CPI: 12.5 ips= 10,000 characters per second 25 ips= 20,000 characters per second 37.5 ips= 30,000 characters per second 45 ips= 36,000 characters per second 75 ips= 60,000 characters per second 112.5 ips= 90,000 characters per second
Register Address -	Status (MTS) 772 520 Command (MTC) 772 522 Byte Record Counter (MTBRC) 772 524 Current Memory Address (MTCMA) 772 526 Data Buffer (MTD) 772 530 Tape Read Lines (MTRD) 772 532
Computer I/O Interface -	Interrupt Vector Address 224. DMA data transfer. 1 bus load.

Tape Interface -	Compatible with tapes manufactured by Perlec, Kennedy, Tandberg, Cipher, CDC. Connector on controller end is a 3M, 50 pin, ribbon cable connecter.
Packaging -	The controller is completely contained on one quad module 10.44 inches wide by 8.88 inches deep. Optionally supplied with the controller is one cable to the first tape unit.
Documentation -	One User's Guide is supplied with the first controller.
Software -	One diagnostic routine with object listing is optionally supplied with a controller (or the first of a series of OEM controllers). Driver routine is optic
Power -	+5, ±0.25 VDC at 3.6 amps, from computer backplane.
Environment -	Operating temperature $50^{o}F$ to $104^{o}F$* Operating humidity 0 to 90% non-condensing.* *Note that the quality of recording and reading information on magnetic tape is affected by temperature and humidity. Typically the area within which the tape is used should be maintained within the following limits: Temperature: $15^{o}C.$ to $32^{o}C.$ Humidity: 20% to 80%
Shipping Weight -	5 pounds including documentation.
Options -	Tape cable(s), on-site installation, factory integration, complete tape systems, driver routine, auto self test, diagnostic routine.

SECTION 2

INSTALLATION

2.0 INTRODUCTION

The padded shipping carton that contains the controller board also contains an instruction manual and a cable to the first tape drive (if this option is exercised). The controller is completely contained on the quad-size printed circuit board. The tape (or tapes), if supplied, are each contained in a separate shipping carton.

CAUTION

IF DAMAGE TO ANY OF THE COMPONENTS IS NOTED, DO NOT INSTALL. IMMEDIATELY INFORM THE CARRIER AND DILOG.

Installation instruction for the tape are contained in the tape manual. Before installing any components of the tape system, read Sections 1, 2 and 3 of the instruction manual for the controller.

2.1 PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a DMA device available for the PDP1103 systems. Certain configurations require minor modifications before operating the DQ120 tape system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the DQ120 controller if the DMA refresh logic on the REV11-C is enabled.

B. If the REV11-C module is installed, cut etch to pin 12 on circuit D30 (top of board) and add jumper between pin 12 and pin 13 of D30.

C. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

D. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

E. If system requires more than a 4 x 4 backplane, place the REV-11 terminator in the last available location in the last backplane.

2.2 CONFIGURATION-TAPE SPEED AND DEC/IBM FORMAT SELECT

Verify that switch J5 is properly positioned to provide required system configuration. Various option configurations are provided on the DILOG controller. The options are configured by switch J5. Figure 2-1 shows the switch positions and crystal frequencies. The switch positions are typically factory configured since the controllers are tested to individual customer requirements. Switch position 5 of J5 selects eigher DEC or IBM format. DEC format requires the least significant byte be written first; in IBM format, the most significant byte is written first. SW5 ON selects DEC format, SW5 OFF selects IBM format.

2.3 INSTALLING

To install the controller module, proceed as follows:

CAUTION

A. REMOVE DC POWER FROM MOUNTING ASSEMBLY BEFORE INSERTING OR REMOVING CONTROLLER MODULE.

B. DAMAGE TO THE BACKPLANE ASSEMBLY MAY OCCUR IF THE CONTROLLER MODULE IS PLUGGED IN BACKWARDS.

1. Select the backplane location into which the controller is to be inserted. Be sure that the tape drive controller is the highest priority DMA device in the computer next to the disc controller, except if the DMA refresh/bootstrap ROM option module is installed in the system. The highest priority device is the device closest to the processor module.

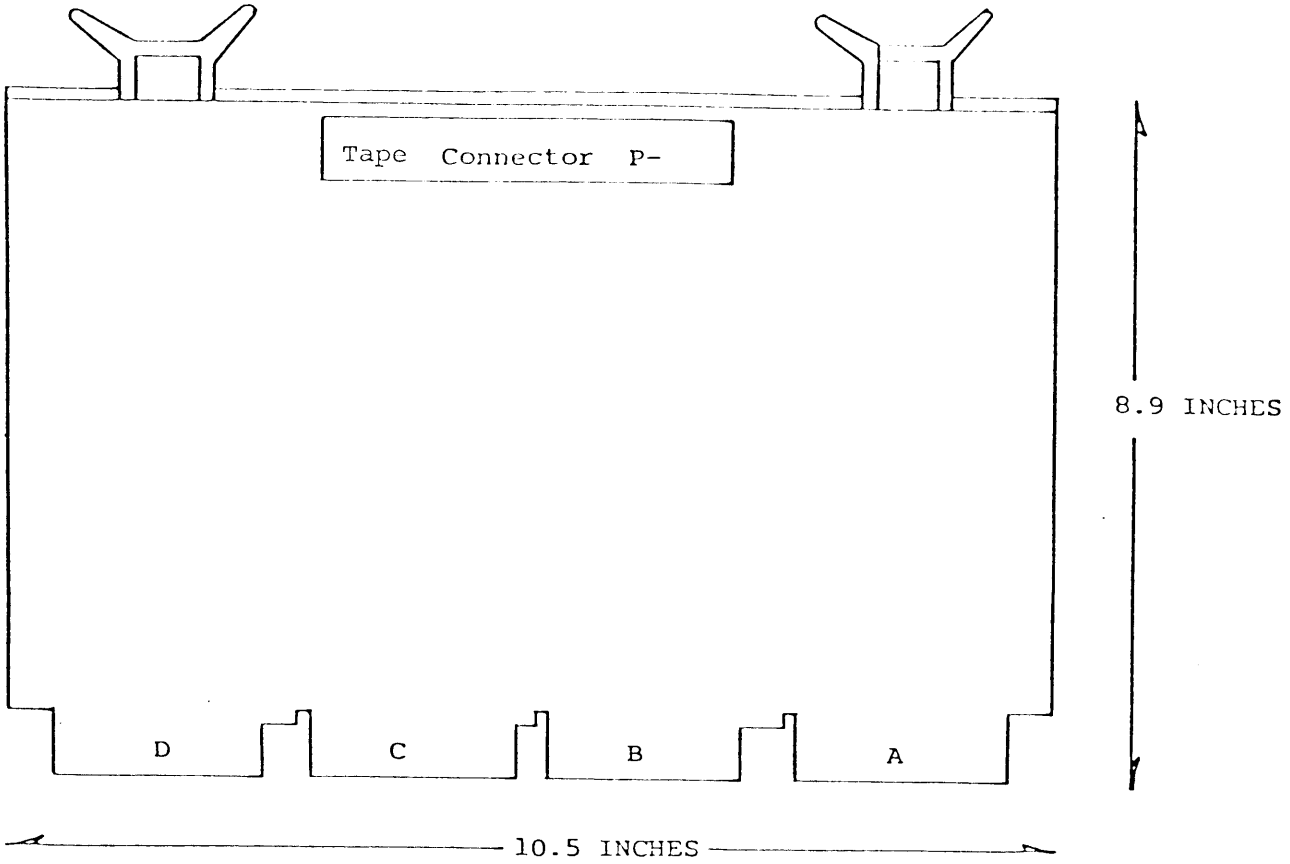
   There are several backplane assemblies depending on the type system: H9270 backplane, DDV11-B backplane, BA11 expansion box. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or the first location in the first backplane of multiple backplane systems.

   Further note that memory need not be installed next to the processor module; it is not DMA or interrupt priority dependent.

   It is important that all option slots between the processor and the tape controller be filled if the controller cannot be next to the processor. This is necessary to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If empty slots are between the controller and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
COXN2	COXM2	BIAK1/L0
COXS2	COXR2	BDMG1/L0

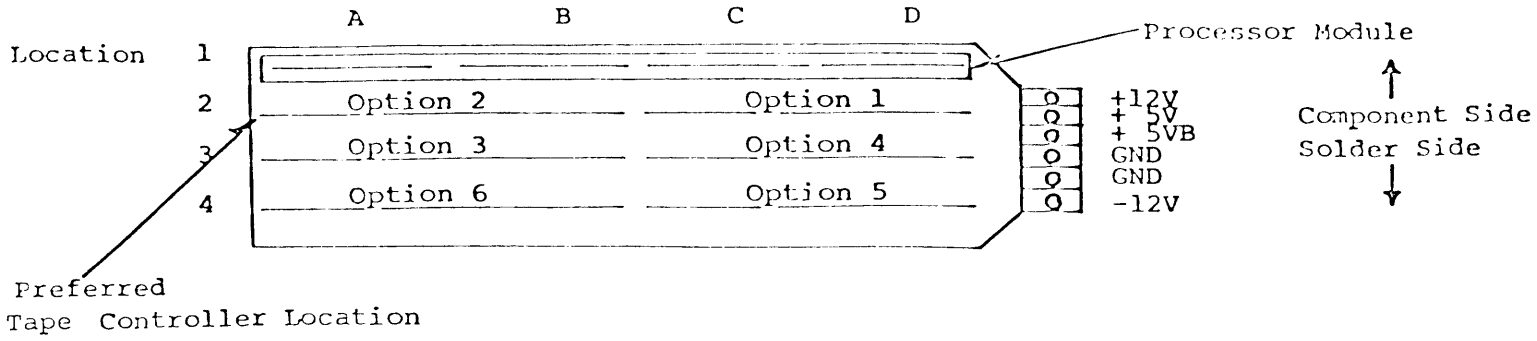
Last full option slot — Controller slot



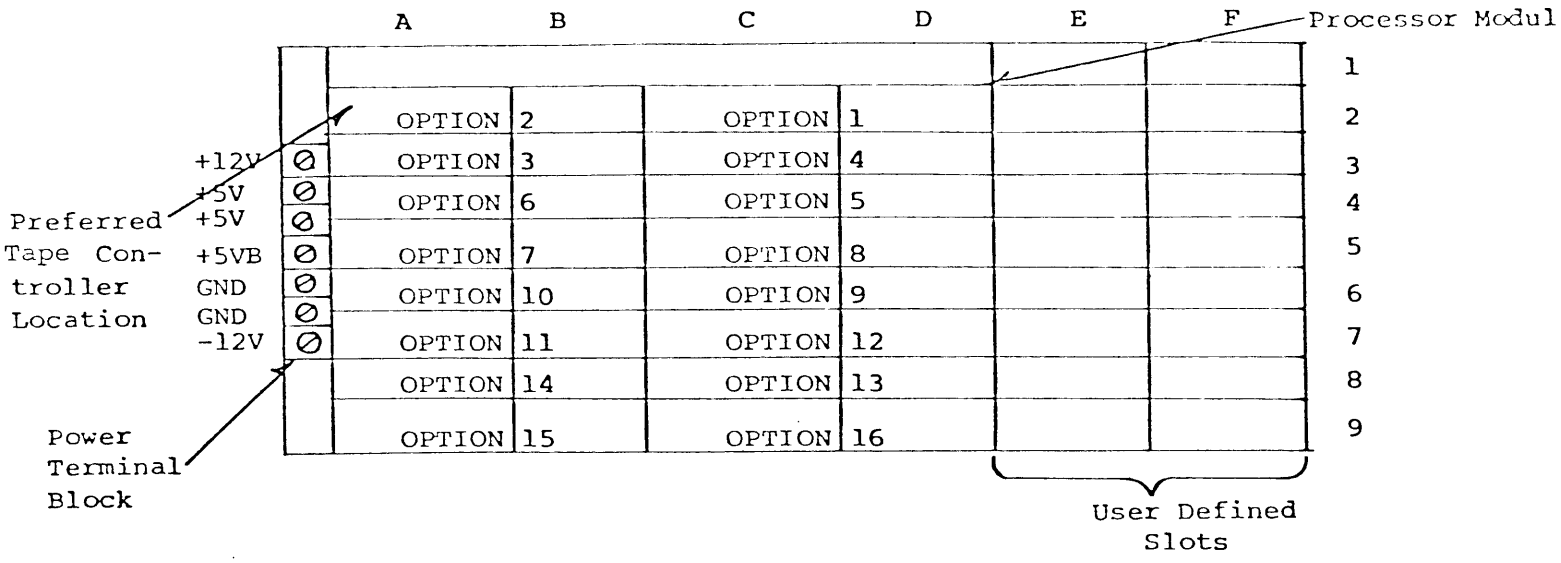
TAPE SPEED (IPS)	SWITCH SETTING				FORMAT SWITCH 5	
	4	3	2	1	DEC	IBM
112.5	0	0	0	0	1	0
75	0	0	0	1		
45	0	1	0	1		
37.5	0	0	1	0		
25	0	1	1	1		
12.5	1	1	1	1		

NOTE: 0 = Switch Off
1 = Switch On

FIGURE 2-1: Controller Tape Speed/Format Configuration



H9270 MODULE INSERTION SIDE



DDV11-B Backplane Module Insertion Side

NOTE: Memory can be installed in any slot; it is not priority dependent and does not need to be adjacent to the processor.

FIGURE 2-2: Typical Backplane Configurations

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing Row One (1).

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

3. Feed the module connector end of the tape I/O ribbon cable into the computer module area. Install the cable connector into module connector J. Verify that the connector is firmly seated.

4. Connect the tape drive end of the I/O ribbon cable to the tape drive "Y" cable I/O connector.

5. Refer to the tape drive manual for operating instructions and apply power to the drive and computer.

6. Observe that the DIAGNOSTIC LED on the controller board is lit.

7. The system is now ready to operate. Load diagnostic program _____, refer to listing _____ for operating instructions. Run diagnostic to verify correct operation of tape system.

NOTE

LED indicator BUSY and DMA will both be lit to indicate proper operation.

SECTION III

OPERATION

3.0 INTRODUCTION

Prior to system operation, the operation section of the manual for the tape drive, should be studied. The functions of the controls and indicators on the tape drive and procedures for mounting and removing tape reels should be understood. Special attention should be given to handling the magnetic tape to prevent loss of data or damage to the tape handling equipment. The following precautions should be observed:

a. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape transport operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the transport or tape storage area. Tobacco smoke and ash are especially damaging to tape.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer. When system operation is desired, be sure the tape drive on-line indicator is lit. On-line operation is a function of program commands described in Section 4 of this manual. To understand the programmed operation of a magnetic tape system, the user should study the following portions of "RT-11 VOLUME 3":

1. Chapter 2, Programmed Requests.
2. Paragraph 1.4.7, Programming For Specific Devices.

3.1 TAPE FORMAT

The storage ability of magnetic tape is provided by a thin magnetic coating put down upon a stable, inert, non-magnetic material. Mylar is currently used as the base material. The magnetic coating is typically a complex mixture of magnetic particles, polymeric binder for adherance to the mylar base, carbon particles to provide conductivity to prevent static charge build up, and lubricants to reduce abrasion and extend media surface and head life.

Information is stored on digital magnetic tape as a pattern of ones and zero achieved by saturating the matnetic media in a positive or negative direction. Saturating the tape is defined as recording or writing on tape. During reading the tape, the positive and negative saturations or flux changes are detected and converted to binary ones and zeros.

There are currently three principle recording techniques: NRZI (Non-Return to Zero - change on a 1), PE (Phase Encoding), and GCR (Group Code Recording).

The DQ120 system uses NRZI recording. This recording technique requires a change of state (flux change) to write a 1, and no change of state (no flux change) to write a 0. The DQ120 system accommodates two format types: 7 track and 9 track. A seven track tape comprises six data channels and a lateral parity channel. A nine track tape comprises eight tracks of data plus a lateral parity channel. To permit the controller to recognize and respond to data areas on tape, data is recorded in a specific manner. Figure 3-1a illustrates 7 track format; Figure 3-1b illustrates 9 track format. To aid in understanding the Figure, the following are definitions commonly used when discussing magnetic tape:

1. Reference Edge - The edge of the tape toward the operator when the tape reel is mounted on the tape drive.

2. BOT (Beginning of Tape) - A reflective strip place on the reference edge, 15 feet (± 1 foot) from the beginning of tape.

3. EOT (End of Tape) - A reflective strip placed on the non-oxide side of the tape, against the non-reference edge, 25 to 30 feet from the end of the tape.

4. Tape Character - Up to 7 or 9 bits recorded laterally across the tape.

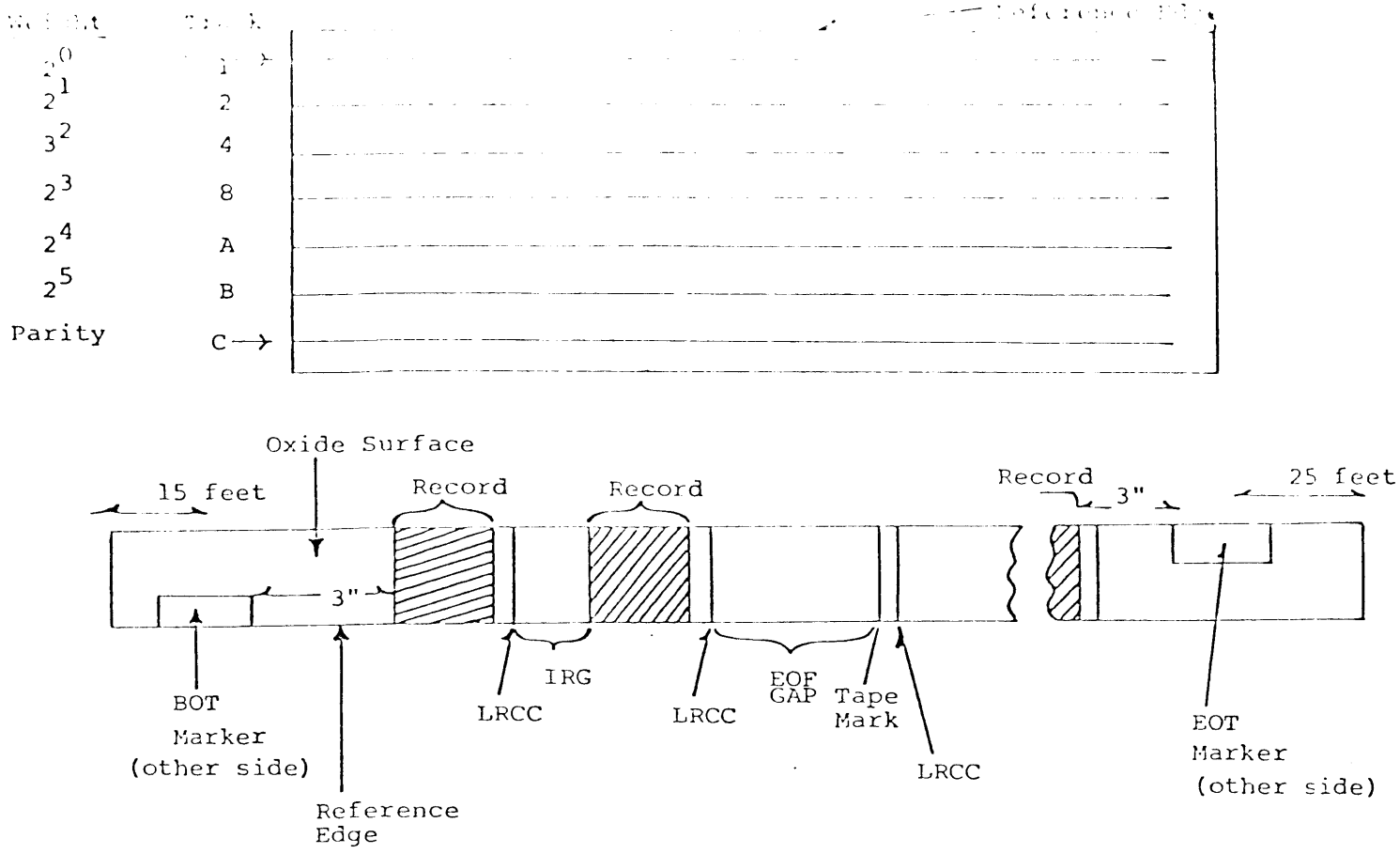


FIGURE 3-1a 7-Track Tape Format

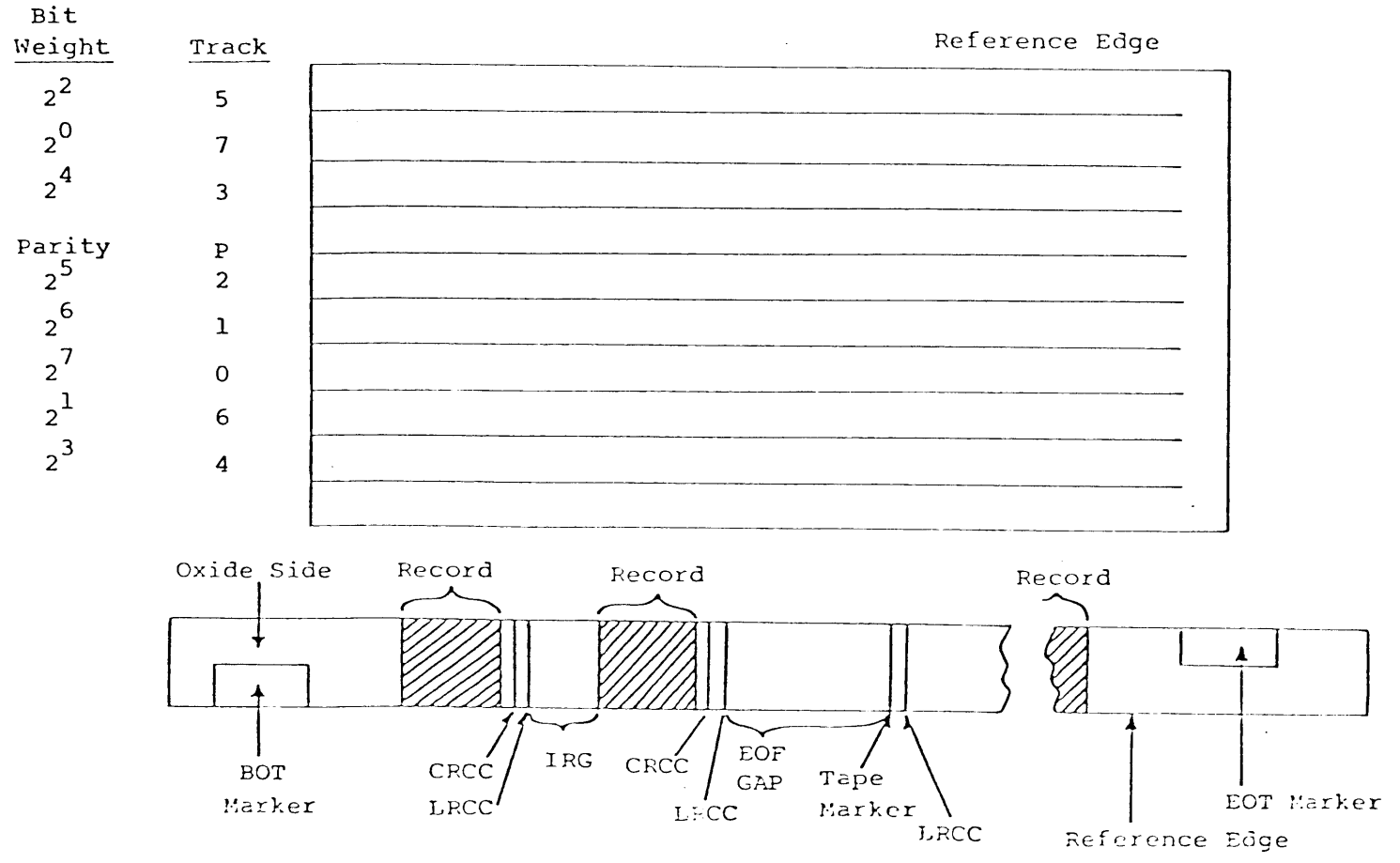


FIGURE 3-1b 9-Track Tape Format

5. Record - A group of consecutive tape characters.

6. File - A series of record, one minimum, no maximum.

7. IRG (Inter-record Gap) - a length of erased tape used to separate records; gap length is 0.75 inches for 7 track tape, and 0.6 inches for 9 track tape (lengths are minimums). Maximum gap length is 25 feet.

8. EOF Gap (End of File) - A 3 inch minimum gap used to separate files on tape and as a minimum erased area preceding the first record on tape.

9. EOF Tape Mark - A special one-character tape record followed by an LRCC character that defines the end of a tape file. The tape mark is always preceded by an EOF gap.

10. Tape Speed - The speed at which tape moves past the read/write heads; normally stated in inches per second (IPS).

11. Tape Density - The density of sequential characters on the tape. It is specified by ANSI in characters per inch (CPI), but is also referred to as bytes per inch (BPI). The following densities have been adopted as standards: NRZI 7 track, 200, 556, and 800 CPI; NRZI 9 track, 800 CPI; PE 9 track, 1,600 CPI; GCR, 6,250 CPI.

12. Write Enable Ring - A rubber ring which must be inserted on the supply tape reel to allow the transport to write on the particular tape. This is a safety feature to help prevent accidental destruction of previously recorded data.

13. CRCC (Cyclic Redundance Check Character) - A check character that is written four character spaces after the last character of an NRZ, 9 track only, record. The CRCC is derived by a complex mathematical formula applied to the characters written in the record. The CRCC can be used to recover a lost bit in a record read from the tape.

14. LRCC (Longitudinal Parity Check Character) - A check character written four character spaces after the last character of a record in 7 track tape or after the CRCC character in 9 track tape. LRCC consists of one bit of even parity for each track of data. For example, if track one had an odd number of 1's written in a record, then a 1 must be written in the LRCC bit associated with track one.

15. Lateral Parity - The parity bit in each character. Odd parity convention is normally used. This permits a read after write data-quality check to be made by monitoring each character after it is written on tape for an odd number of bits.

Reading and writing occurs when the tape if moving forward, but the controller can move the tape to new positions in forward or reverse. For writing on tape, 16-bit data words are transferred from memory to a data buffer in the controller. From the data buffer, information is supplied to the tape a character at a time. During reading, the sequence is reversed; information is read from tape as 6-bit characters for 7 track tape or 8-bit characters for 9 track tape and transferred to the data buffer. When a computer word has been assembled in the data buffer, a DMA transfer is initiated to transfer the data buffer word into memory.

A seven track tape includes six data channels and a lateral parity channel. Density modes of 200, 556, and 800 bytes per inch are selectable. Nine-track tape is similar to the 7-track tape except densities of only 800 bytes per inch are possible in the NRZI mode, and an industry standard cyclic redundancy character is written at the end of each record. The front and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 feet of blank tape is wound on a reel and precedes the BOT and EOT strips. A 3-inch gap is left from the load point before writing can begin.

Each computer word contains two 8-bit tape characters. Record blocks are separated by 3/4 inch gaps on 7-track tape and 1/2 inch gaps on 9-track tape. Industry standard 7-track tape records contain from 24 to 4,008 characters and 9-track tape records contain from 18 to 2,048 characters.

3.1.1 7-Track Tape Packing

Each character frame in a 7-channel tape (see Figure 3-1a) consists of six character bits (B,A,8,4,2,1) in descending order of significance. The parity bit, or check bit (C), is the seventh bit and is set or cleared by the transport write head. One byte of a LSI-11 word corresponds to one tape character. However, because one byte contains eight bits and a tape character contains only six data bits, two bits within each byte are not used. During a read operation, the extra bits are forced to 0; during a write operation, the bits remain unchanged. During the core dump mode of operation, one LSI-11 byte corresponds to two tape characters. Thus, all bits within the byte are used; however, the two most significant bits on the tape are not used.

3.1.2 DEC/IBM Byte Order

The order in which data bytes are written on tape differs between DEC and IBM formats. In standard DEC format the least significant byte (LSB) is written first; in IBM format the most significant byte (MSB) is written first. Position 5 of switch J5 permits the operator to change the byte order written/read. SW5 ON equals DEC; SW5 OFF equals IBM.

SECTION IV

PROGRAMMING

4.1 PROGRAMMING DEFINITIONS

Function - The expected activity of the tape system (read, write, rewind).

Command - To initiate a function (GO, Select).

Instruction - One or more orders executed in a prescribed sequence that cause a function to be performed.

Address - The binary code placed on the BDAL0-15 lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip-flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register - An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often registers are the contents of addressed locations in solid-state or core memory.

4.2 TAPE CONTROLLER FUNCTIONS AND REGISTERS

The tape controller performs eight functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command, and perform a function, the controller must be properly addressed and the tape drives must be powered up, at operational speed, and be ready.

All software interaction between the tape controller, the processor, and processor memory is accomplished by six registers in the tape controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The six controller registers, their addresses, mnemonics, and their bit assignments are shown in Figure 4-1.

The eight functions performed by the controller are established by bits 01, 02, and 03 of the command register (MTC).

REGISTER	ADDRESS	BIT POSITION	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Status (MTS)	772 520		ILL COM	EOF		PRE	BGL	EOT	RLE	BTE	NX M	SE LR	BOT	7 CH	SD WN	WRL	RWS	TUR
Command (MTC)	772 522		ERR	DEN 8	DEN 5	PC LR	PE VN	US 2	US 1	US 0	CU R	INT ENB	XBA 17	XBM 16	FU 2	FU 1	FU 0	GO
By Record Counter (MTBRC)	772 524		15															00
Current Memory Address (MTCMA)	772 526		CM 15	CM 14	CM 13	CM 12	CM 11	CM 10	CM 09	CM 08	CM 07	CM 06	CM 05	CM 04	CM 03	CM 02	CM 01	CM 00
Data Buffer (MTD)	772 530									DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00
Ta Read Lines (MTRD)	772 532		TIMER	CRC/ LPC		GS				P	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7

FIGURE 4-1 Controller Register Configuration

The address of the MTS register is 772 520. MTS is a read only register. The functions of the bits of this register are as follows:

Bit 15: Illegal Command - Set by any of the following illegal commands:

1. Any DATO or DATOB to the command register during the tape operation period.

2. A write, write EOF, or write with extended IRG operation when the File Protect bit is a 1.

3. A command to a tape unit whose Select Remote bit is a 0.

4. The Select Remote (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition, the CU ready bit remains set.

Bit 14: End of File (EOF) - Set when an EOF character is detected during a read, space forward, or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the File Mark signal upon EOF detection.

Bit 13: Not Used

Bit 12: Parity Error (PAE) - The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected.

A parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred to tape and in a read operation, the entire record is written into core memory.

For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF and write with extended IRG operations. The entire record is checked including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of 1's is detected on any track in the record. A lateral parity error occurs when an even number of 1's is detected on any character when PEVN is a 0, or an odd number of 1's is detected on any character when PEVN is a 1.

Bit 11: Bus Grant Late (BGL) - Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

Bit 10: End of Tape (EOT) - Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

Bit 9: Record Length Error (RLE) - Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.

Bit 8: Bad Tape Error (BTE) - Sets when a character is detected (RDS pulse) during the gap shut-down or settling down period for all operations (except rewind). When BTE is detected the ERR bit is set immediately, and if INT ENB is set, an interrupt sequence is started.

Bit 7: Non-Existent Memory (NXM) - Set during NPR operations when the control unit is bus master, and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

Bit 6: Select Remote (SELR) - Cleared when the tape unit addressed does not exist, is off line, or has its power turned off.

Bit 5: Beginning Of Tape (BOT) - Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

Bit 4: Seven Channel (7 CH) - Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.

Bit 3: Tape Settle Down (SDWN) - Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

Bit 2: Write Lock (WRL) - Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.

Bit 1: Rewind Status (RWS) - Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.)

Bit 0: Tape Unit Ready (TUR) - Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

4.2.2 Command Register (MTC)

The address of MTC is 772 522. The functions of the bits of this register are as follows:

Bit 15: Error (ERR) - Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.

Bits 14-13: Density (DEN 8, DEN 5) - Cleared on INIT.

BIT 14	BIT 13		
0	0	200 bpi	7 channel
0	1	556 bpi	7 channel
1	0	800 bpi	7 channel
1	1	800 bpi	9 channel

Bit 12: Power Clear (PCLR) - Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.

Bit 11: Lateral Parity (PEVN) - Set for even parity. Cleared for odd parity. A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.

Bits 10-8: Unit Select - Specifies one of the four possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

Bit 7: CU Ready (CUR) - Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.

Bit 6: Interrupt Enable (INT ENB) - When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit (i.e. CU READY or ERROR = 1).

Bits 5-4: Address Bits - Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

Bits 3-1: Function Bits - Selects 1 of 8 functions (programmable commands).

BIT 3	BIT 2	BIT 1	
0	0	0	Off line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write with Extended Interrecord Gap
1	1	1	Rewind

Bit 0: Go - When set, begins the operation defined by the function bits.

4.2.3 Byte Record Counter (MTBRC)

The address of MTBRC is 772 524.

The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

4.2.4 Current Memory Address Register (MTCMA)

The address of MTCMA is 772 526.

The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 2 immediately

after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 2 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

4.2.5 Data Buffer (MTD)

The address of MTD is 772 530.

The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In a DMA operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape.. The polarity of the parity bit is determined by the PEVN bit in the MTC.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

4.2.6 Tape Read Lines (MTRD)

The address of MTRD is 772 532.

The memory locations allocated for the tape read lines are:

Bits 0-7 for the channels 7-0 respectively.

Bit 8 for the parity bit.

Bit 12 for the gap shutdown bit.

Bit 13 Not used.

Bit 14 for the CRC, LPC character selector.

Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit.
Bit 14 is set and cleared by the processor and cleared by INIT.
Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

4.2.7 Timer

TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SECTION 5

TECHNICAL DESCRIPTION

5.0 INTRODUCTION

This section contains the theory of operation of the DQ120 tape controller. The text references block and timing diagrams interspersed with text, a Glossary of Terms at the end of the section, and detailed logic diagrams in Section 6. The material is organized as a General Description followed by a Functional Description.

The General Description primarily describes the interconnection of the major logic elements that make up the controller. The principle reference is the controller simplified block diagram. The Functional Description describes the individual logic elements within the controller. The text is referenced to the detailed block diagram. The description assumes an understanding of the LSI-11 I/O bus and a basic understanding of digital computer theory.

5.1 GENERAL DESCRIPTION

Figure 5-1 is a simplified block diagram of the controller. The controller comprises three logical sections:

A. Computer Interface

B. Microprocessor

C. Peripheral Interface

The three sections function together to transfer data between the I/O bus of the computer and up to four tape drives. The two interface sections primarily match the voltage levels and load/drive characteristics of the computer I/O bus and tape I/O lines to the logic levels of the controller. The microprocessor is the control, timing, and data conversion section of the controller.

The microprocessor functions under control of firmware instructions stored in solid state, programmable, Read Only Memory (PROM). The microprocessor is implemented with AM2900-series bit-slice microprocessor chips. Refer to "MICROPROGRAMMING HANDBOOK" from Advanced Micro Devices, Inc., 1901 Thompson Place, Sunnyvale, California 94086 for introductory material on microprogramming a bipolar microprocessor.

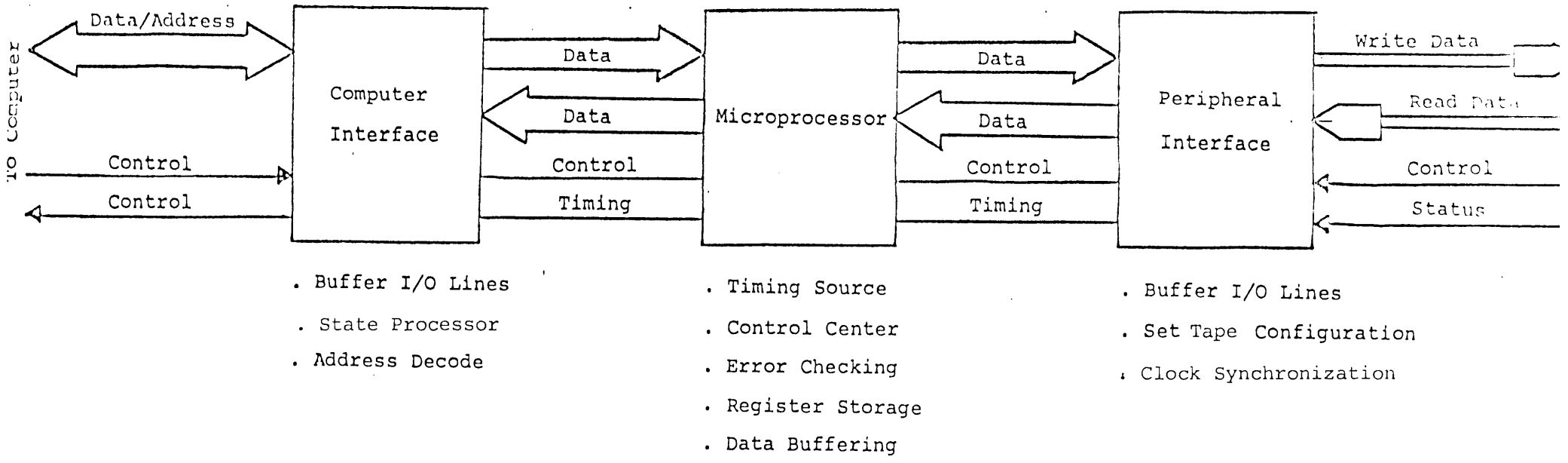


FIGURE 5-1: Simplified Block Diagram
Peripheral Controller

5.1.1 Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q bus of the computer and the controller and (2) synchronize information transfers. There are two major classes of lines connected to the computer interface:

A. Data/address lines

B. Control lines

There are 16 bidirectional data/address lines. Both device addresses and data are transferred over these lines. Address information is first placed on the lines by a bus master. The bus master then either receives input data from, or outputs data to, the addressed slave device, or memory, over the same lines. During initialization and status-transfer sequences, the controller is a slave and is selected by address 224_8. During data transfers, the controller is bus master and either receives data from, or outputs data to, the processor memory via the DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and originate either at the processor or at the controller.

The computer interface controls the synchronization, or "bus arbitration" sequence. Bus synchronization is done by a separate hardware state processor rather than by the microprocessor, to minimize bus use by the controller. This permits other devices to use the DMA channel on a time multiplexed basis with the disc controller.

5.1.2 Microprocessor

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read only memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the computer. The instruction operands are stored in registers within the microprocessor.

When a GO command is issued by the computer, the firmware microinstructions cause the registers to be examined and either a data transfer sequence or a rewind sequence to be performed. Note that rewind functions can be performed on any tape drive not involved in a data transfer operation simultaneous with data transfers.

The microprocessor contains an eight word RAM memory dedicated to buffering data between the Q bus and the microprocessor. This allows several DMA cycle requests to be missed without missing data words being transferred between the tape and computer memory.

The rate and order (format) at which data is transferred to the tape is controlled by the microprocessor. Within the microprocessor, data is handled in 8-bit parallel bytes. Error check bits are calculated (LRCC, CRCC) and supplied to the tape during a write function. During a read function, the microprocessor monitors the error check bits and the data being read. Discrepancies are flagged as errors to the computer. The microprocessor detects other types of errors during the transfer functions (data late, programming error, etc.) and monitors status lines from the tape for malfunctions within this assembly. All errors are assembled into a status word for access by the processor.

5.1.3 Peripheral Interface

The purpose of the peripheral interface is to match the characteristics of the tape drive to the characteristics of the microprocessor. The peripheral interface:

A. Contains line drivers and receivers that buffer the information lines between the controller and the tape drives over cable lengths up to 20 feet.

B. Contains the PROM and switches that permit configuring the controller to match the different tape subsystem configurations.

5.2 FUNCTIONAL DESCRIPTION

The detailed block diagram (Figure 5-2) shows the functional elements of the tape controller. A circled number, or numbers, within the blocks of the diagram references the sheet(s) of the detailed logic drawing represented by the block. The detailed logic drawings are in Section 6. A Glossary of Terms, located at the end of this section, defines the mnemonics used in this text and on the logic drawings.

5.2.1 Computer Interface

The computer interface comprises the following elements:

A. Data/Address Receivers

B. Control Receiver/Drivers

C. Data/Address Drivers

D. Bus and Arbitration Sequence (Hard-wired state processor)

The computer interface is a hard-wired logic section that buffers and synchronizes information transfers between the I/O bus and the controller.

5.2.1.1 Data/Address Receivers

Both data and device addresses are time multiplexed on 16 I/O bus lines ($BDAL00_L$ - $BDAL15_L$). The tri-state receiver/driver circuits E11, E13, E14, and E16 shown on sheet 3, buffer these lines into the controller. Once buffered, the received lines are identified as DB00 - DB15 and routed to the bus arbitration sequence logic and the μ data file multiplexer in the microprocessor.

5.2.1.2 Control Receiver/Drivers

The control lines between the I/O bus and the controller are buffered by circuits E5, E6, E7, and E8 shown on sheet 4. The receivers are always connected to the bus. Setting circuit pins 7 and 9 low enables the tri-state drivers to the bus. Two of the circuits are permanently enabled; circuit E9 is enabled by Transmit Select Acknowledge ($\overline{TSACK}$), and circuit E7 is enabled by Device Enable ($\overline{DEN}$) and $\overline{TSACK}$.

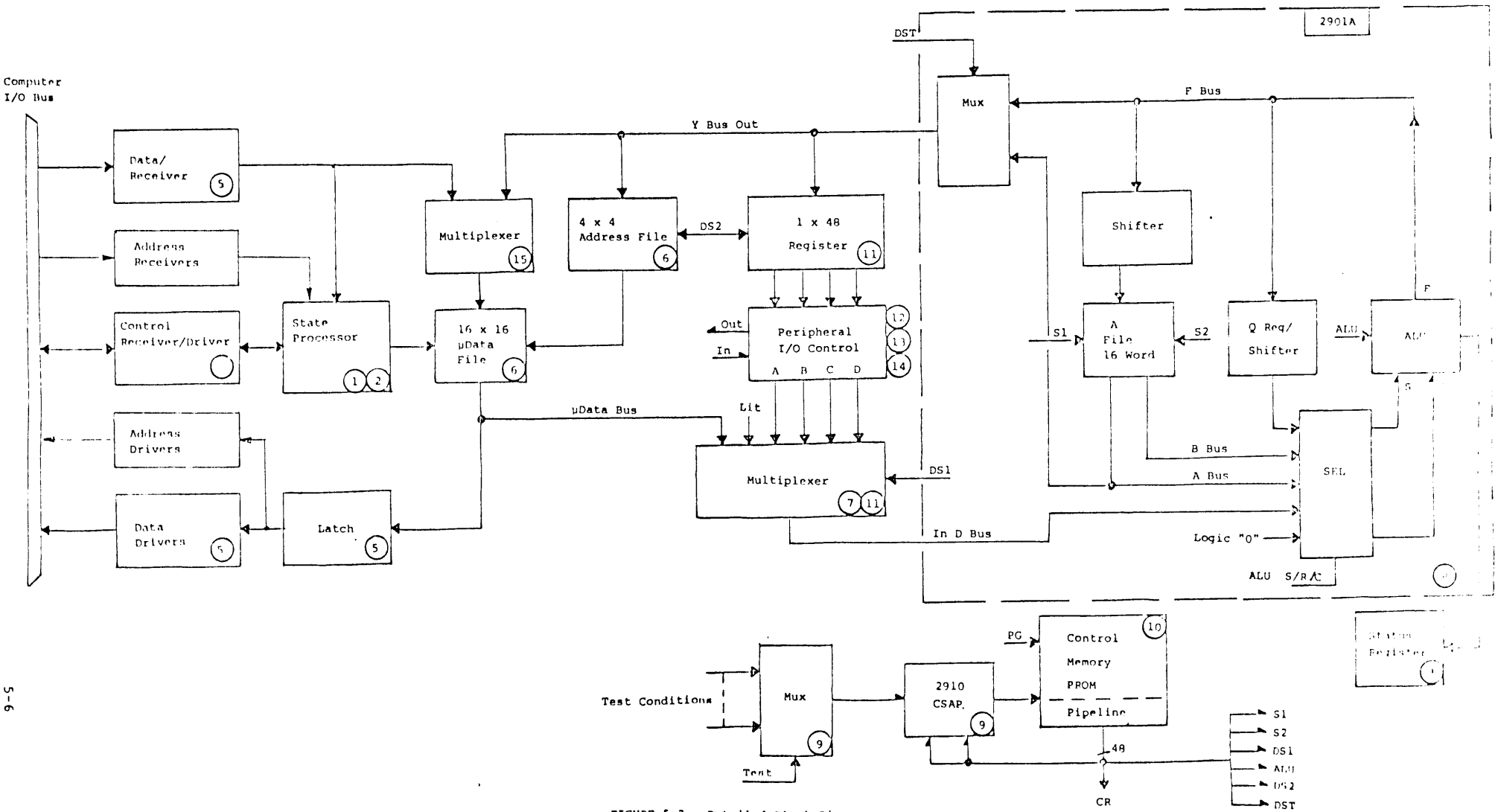


FIGURE 5-2: Detailed Block Diagram
Peripheral Controller

5.2.1.3 Data/Address Drivers

The tri-state drivers in circuits E11, E13, E14, and E16 are enabled by Device Enable ($\overline{DEN}$) to gate addresses and data to the I/O bus. Addresses and data to the I/O bus are temporarily stored by register circuits E12 and E15. Information from the FQ bus is clocked into the registers either by signal Data (DA) or by signal Load Address (LDADD). The least significant bit (DOO) is gated with control term TDOOG to the line drivers.

5.2.1.4 Bus And Arbitration Sequence (State Processor)

To ensure fastest response time, the synchronization of I/O bus transfers is done by hard-wired state logic illustrated on sheets 1 and 2. Information transfers are of two kinds: programmed I/O and direct memory access (DMA). During programmed I/O transfers, the processor is bus master. During DMA transfers, the controller is bus master. Distinguishing between the two transfer types is the function of the arbitration logic.

The bus sequence logic synchronizes master/slave transfers over the I/O bus.

Transfers between the I/O bus and the controller are of two types:

a) Register transfers via programmed I/O.

b) Data transfers via DMA.

During programmed I/O transfers, the seven controller registers are accessed: initialization information is transferred to the registers; status information is accessed from the registers. The registers are located in the μdata file. Address information from the processor is decoded by circuits E10 and F10. Circuit E10 decodes the 7774 portion of the address word; circuit condition of the four least significant bits which are buffered to become A00 - A03. Figure 5-2 shows the registers selected by specific configurations of these bits. Note that bits A00 - A03 are used throughout the bus and arbitration sequence logic.

The bus and sequence arbitration logic primarily comprises PROM's, used as decoders, and flip-flops that temporarily store control information. For example, the storage elements for the DMA light, the Busy light, and the Diagnostic light are contained in this logic. Monostable multivibrators J2-13 and J2-5 monitor bus activity to insure responses to the bus master occur within 10 microseconds. Circuits H3 and K4-16 establish the crystal-controlled time base for the controller. The 10 megabyte output of A3 is divided by two to generate 200 nanosecond clock PCLK buffered to become PPCLK, $\overline{PPCLK}$, and $\overline{CLK}$*.

5.2.1.5 Bus Transfer Timing

The two major types of transfers are divided into the following I/O operations and an interrupt sequence:

- Data Input Transfer (DATI) slave
- Data Output Transfer (DATO) slave
- Data Input Transfer (DATI) DMA
- Data Output Transfer (DATO) DMA
- Interrupt Requests

Programmed I/O transfers are initiated with the controller when the computer places the device address of the controller on the BDAL04 through BDAL15 lines, sets the BBS7L signal at a low level, and switches signal BSYNCL low. Within the controller, BSYNCL converts to RSYNC.

Address decoder E10 monitors the address lines. When the controller address is decoded and RSYNC is asserted, the Bus Active (BACTFF) sets. This sets in motion the transfer sequence.

The sequence for a DATI operation is shown in Figure 5-3. For a DATI sequence, the state processor steps through states 1, 2, and 7. The controller responds to input requests by asserting TRPLY within 10 microseconds of a DATI request. DATI operations read status from the controller.

The sequence for a DATO operation is shown in Figure 5-4. DATO operations transfer commands to the controller registers. A DATO is similar to a DATI. The principal difference is that during a DATO, the Data Out FF rather than the Data In FF is set and the Data Available (DA) signal is not generated.

DMA transfers are between the controller and computer memory. The controller is always bus master. There are two transfer types: data in to memory (DATI) and data out of memory (DATO). Once the controller has been granted DMA bus control, the transfer sequence is similar to I/O bus transfers.

Figure 5-5 illustrates the DMA DATI timing; Figure 5-6 illustrates the DMA DATO timing.

Interrupt request timing is illustrated by Figure 5-7. Interrupt requests are originated by Memory Request A (MRQA), a function of Y00 bit and the FUNC signal. The interrupt vector address is 224_8.

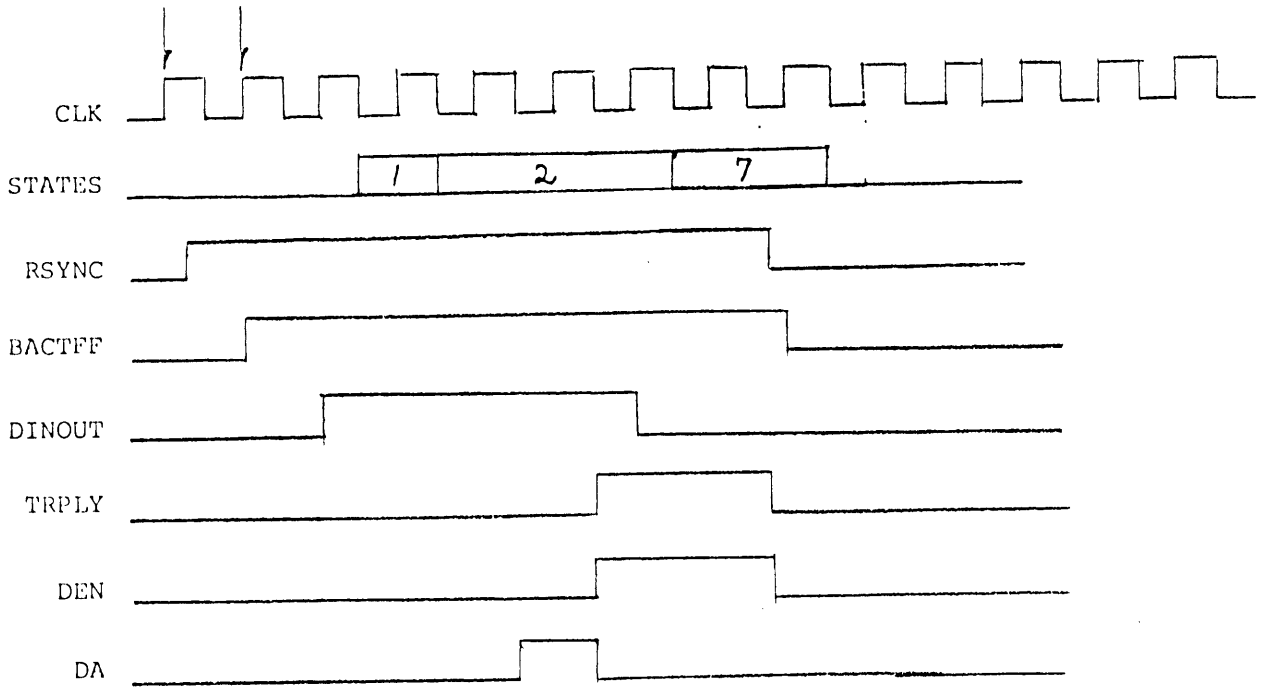


Figure 5-3: DATI - SLAVE, Q BUS

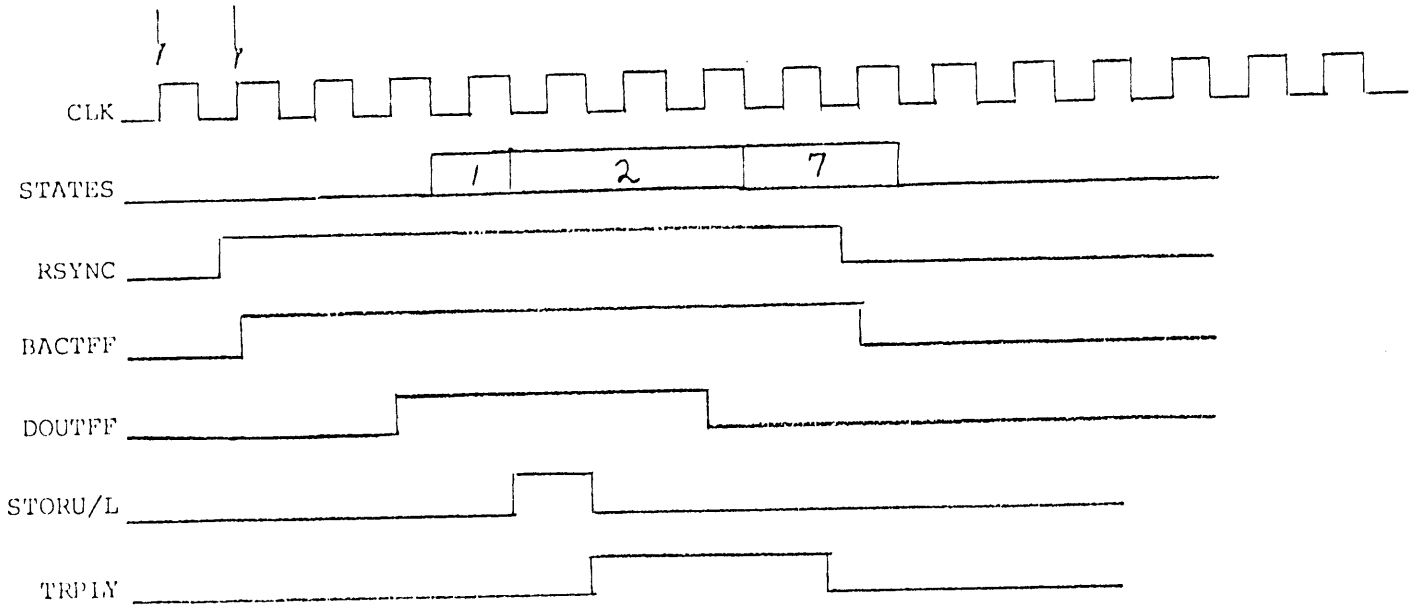


Figure 5-4: DATO - SLAVE, Q BUS TRANSFERS

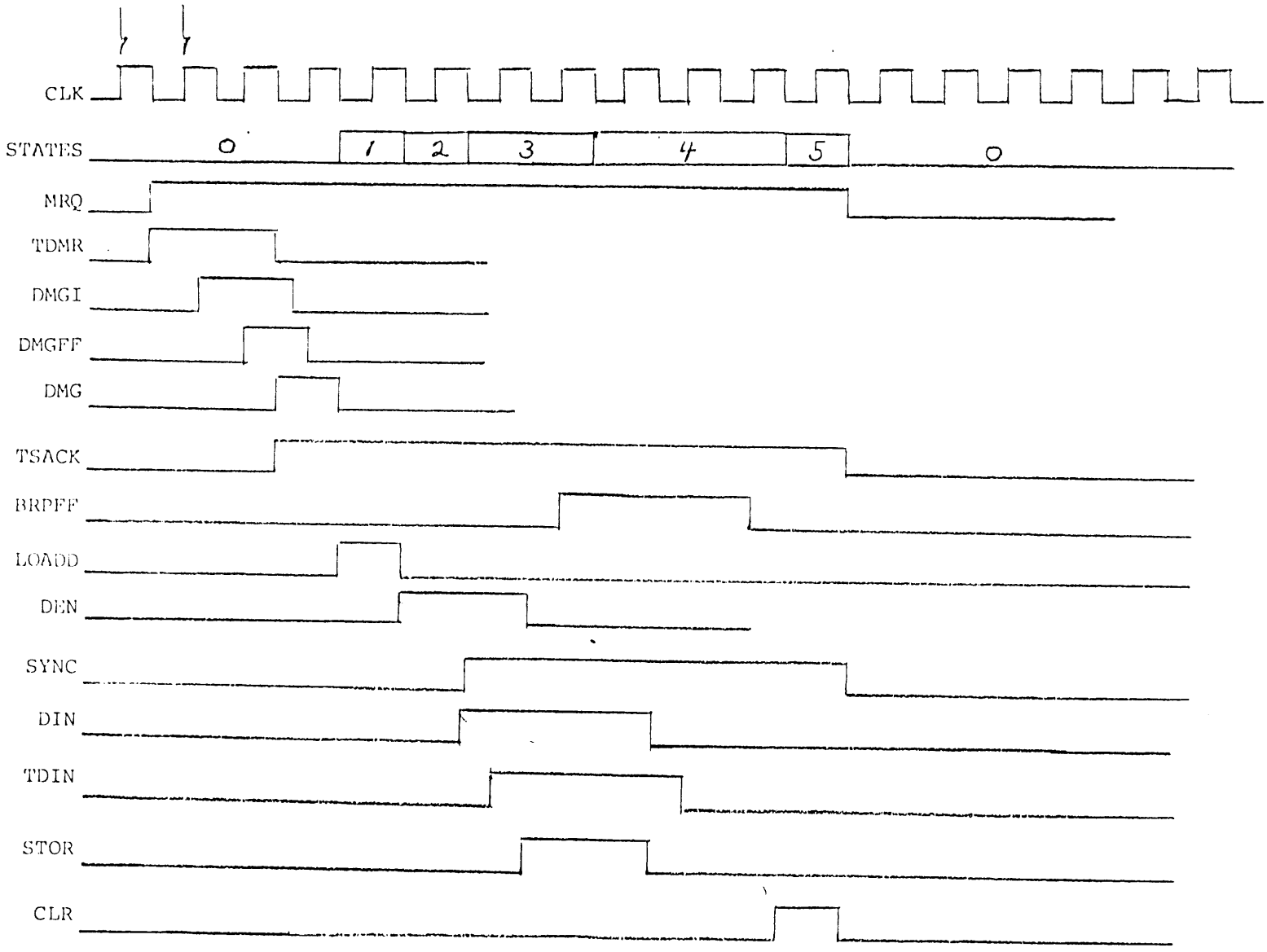


Figure 5-5: DATI - Q BUS DMA TRANSFERS

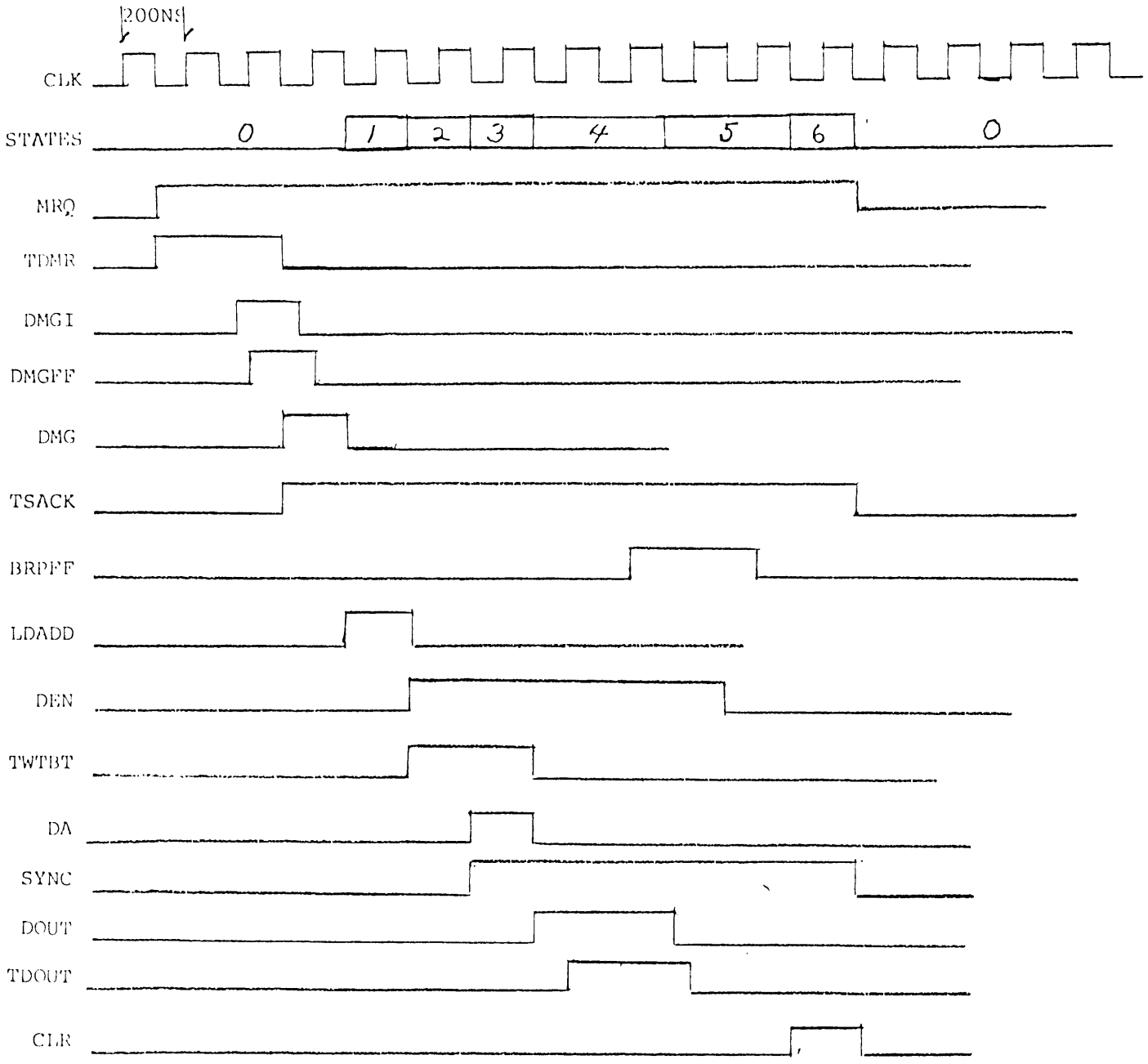


Figure 5-6: DATO - Q BUS DMA TIMING

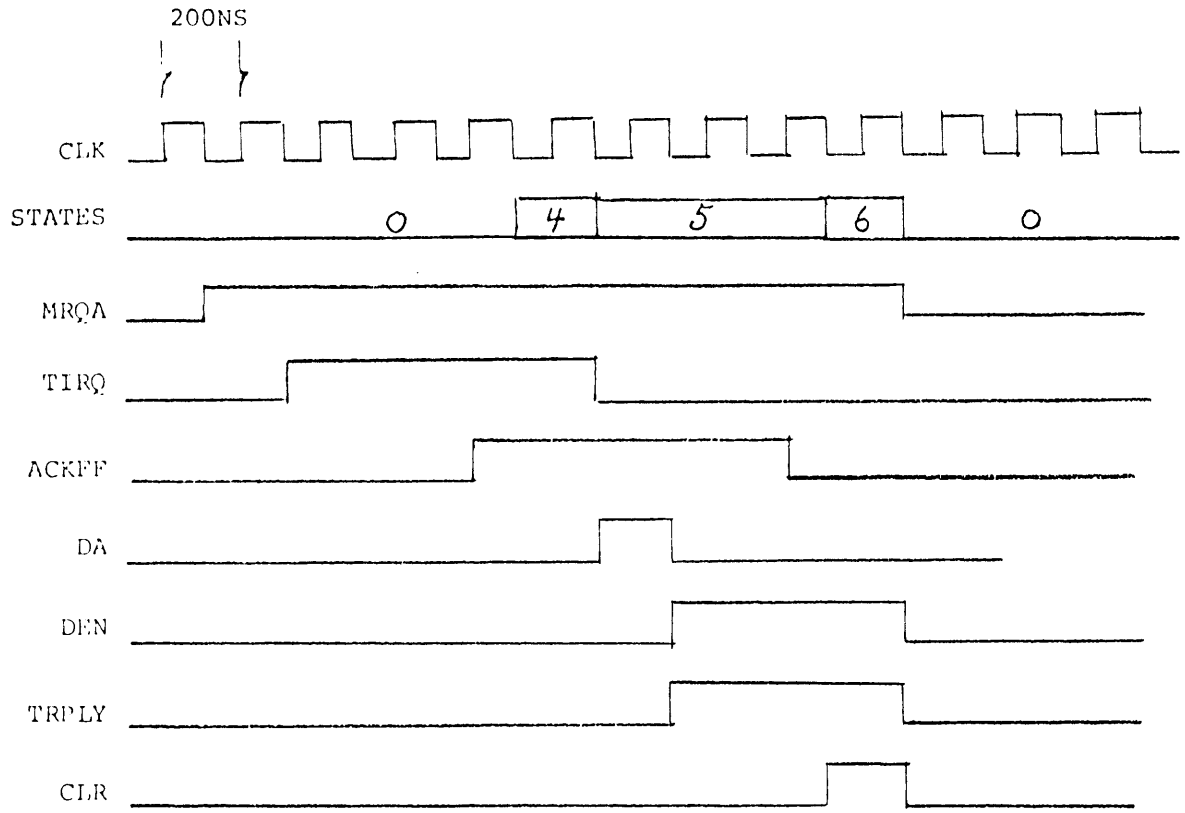


FIGURE 5-7: INTERRUPT SEQUENCE TIMING

5.2.2 Microprocessor

The microprocessor comprises the following major elements:

A. µData File

B. µData File Address Register

C. µData File multiplexer

D. 2901A Array and Status Register

E. Control Memory and Register

F. Control Store Address Programmer and Test Multiplexer

G. D Bus Multiplexer

The preceding elements are interconnected to perform the control, timing, error checking, and data manipulation functions of the controller. Information is transferred among the elements over internal buses defined by Table 5-1.

A microprocessor functions under control of instructions stored in read only memory (ROM or PROM). These instructions are called microinstructions because most often a series of them is required to perform a function. All of the microinstructions are called firmware since, once stored in PROM, they cannot be altered. To understand the function of a microprocessor, please refer to "The Microprogramming Handbook" from Advanced Micro Devices, Inc, 901 Thompson Place, Sunnyvale, California 94086. Detailed technical descriptions of the 2901A four-bit bipolar microprocessor slice and of the 2901 microprogram controller are given in the Advanced Micro Devices "AM2900 Family Data Book". These two elements are the major components of the controller.

5.2.2.1 Micro Data File

This 16 word, 16-bit each word, data file has two functions:

A. Storage for the seven controller registers in locations 9_{16} through F_{16} as follows:

TABLE 5-1: Controller Buses

DESIGNATION	FUNCTION
B	LSI-11 I/O bus: Data and Address lines are bidirectional, most control lines are unidirectional.
DB	Data bus FROM I/O bus receivers into controller.
D	Input Data bus to 2901A supplied with information from multiplexer F11, F14, H14, 8 bits wide.
P	Peripheral Bus: Data and Control signals.
T	Transmit data or control signals from controller to LSI-11 I/O bus.
Y	Output data bus from 2901A array.
FQ	Output of 16 x 16 μData file.

TABLE 5-2:Controller Register Storage

Register	File Location (Hex)
RKDB	9
RKDA	A
RKBA	B
RKWC	C
RKCS	D
RKER	E
RKDS	F

B. Buffer storage for data words being transferred via DMA between memory and disc (locations 0 through 7).

Sheet 6 shows the data file. Inputs to the data file are from the data file multiplexer on lines FI00 - FI15. Outputs from the data file are on lines F100 - F015 to the microdata bus. Data file locations are accessed by the address file and by the DS2 portion of the control register word. Note that the data file is separated into 8-bit bytes and that the upper byte (FX08 - FX15), the lower byte (FX00 - FX07), or both bytes can be written into or read from.

5.2.2.2 Micro Data File Addressing

The microdata file address logic is shown on sheet 6. Two sources address the data file:

A. The bus and arbitration sequence logic (circuit F8).

B. The 4 x 4 address file (circuit H8).

Address control from the bus and arbitration sequence logic is address lines A01 - A03, which select specific controller registers.

The 4 x 4 address file is capable of storing up to four addresses. The source of address information to the address file is bit 03 of field three of the control register word and bits 00, 01, and 02 of the Y bus. Information can be read from and written into different locations of the address file simultaneously. When addresses are being buffered through circuit F8, circuit H8 is disabled from supplying addresses. Write and read addresses to the address file are from field three of the control register word directly, and indirectly via PROM J9 (Sheet 2).

5.2.2.3 Micro Data File Multiplexer

The microdata file multiplexer, shown on sheet 5, switches the input to the microdata file between two sources: the contents of the Y bus, and the contents of the data bus (DB). The contents of field three of the control register word control the selection. Note that bits 13, 14, and 15 to the multiplexer from the data bus can be selected by circuit H11 to be either DB13, 14, or 15 or file output bits 13, 14, 15 restored in the file.

5.2.2.4 2901A Array And Status Register

The 2901A array is shown on sheet 8. The status register is shown on sheet 9 (circuit J14). The 2901A array comprises two AM2901A four-bit bipolar microprocessor slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. The major sections of the AM2901 are shown within dashed lines on the block diagram. A description of the operation of this device is given in the "AM2900 Family Data Book".

The D bus supplies external data to the 2901A. Data from the 2901A is on the Y bus. Control inputs to the 2901A are as follows:

TABLE 5-3: Control Inputs To 2901A

Mnemonic	Signal Source	Definition
A0-3	Control Register	Address inputs: selects the A file register contents to be connected to the 2901A, A bus. (S1)
B0-3	Control Register	Address inputs: selects the A file register contents to be connected to the 2901A, B bus. (S2)
I0-8	Control Register	Instruction control lines: lines 0-2 select the data sources to be applied to the ALU; lines 3-5 select the ALU function to be performed; lines 6-8 determine the routing of the output of the ALU within the ALU and the source of data supplied to the Y (output) bus. (ALU, ALU SRC, DST)
CN	Control Register	Carry input of ALU. Used during arithmetic operations.
CP	Crystal Oscillator	200 nanosecond clock to 2901A.

The status register is updated on a controller clock with the ALU status. The register stores the following conditions:

TABLE 5-4: Status Register Bits

Mnemonic	Definition
Z_s	Indicates result of ALU operation is Zero
C_s	Indicates a "carry out" of ALU
N_s	The most significant ALU bit (sign of result).
V_s	Overflow has occurred.

5.2.2.5 Control Memory And Register

The control memory stores the firmware that controls the operation of the controller. It comprises six 512 x 8 bit programmable read-only-memories (PROMs) identified as L10, L11, L12, L13, L14, and L15 on sheet 10. The PROMs have a pipeline register at the output identified as the Control Register (CR). The six PROMs produce a 48-bit instruction word divided into six 8-bit fields. Figure 5-8 depicts the instruction word.

The contents of the control memory are accessed by the Control Store Address Processor and strobed into the control register by the PPCLK clock. The contents of the control register (CR1-00-07 through CR5-00--07 and literal D00-D07) are routed throughout the logic of the controller.

5.2.2.6 Control Store Address Programmer

The control Store Address Programmer (CSAP) is an AM2910 microprogram control circuit and is described in "The AM2900 Family Data Book". It controls the sequence of execution of microinstructions stored in the control memory. The CSAP is shown on sheet 9.

Control Store output address lines CSA00 through CSA08 select one of 512 locations in control memory and are also routed to test connector J2. Inputs to the CSAP are primarily from fields four and five of the control register and the $\overline{\text{TEST}}$ output of test conditions multiplexer K14 (shown on sheet 9). Bits 00 through 07(LSB) of field five (CR5) supply branch addresses to the CSAP. Bits 00 through 03 of field four (CR4) supply instruction codes to the CSAP. Any one of 16 instructions can be selected. The instructions can be modified by the state of the $\overline{\text{TEST}}$ input. The instructions select the next source of addresses to the control memory. The primary sources of addresses are as follows:

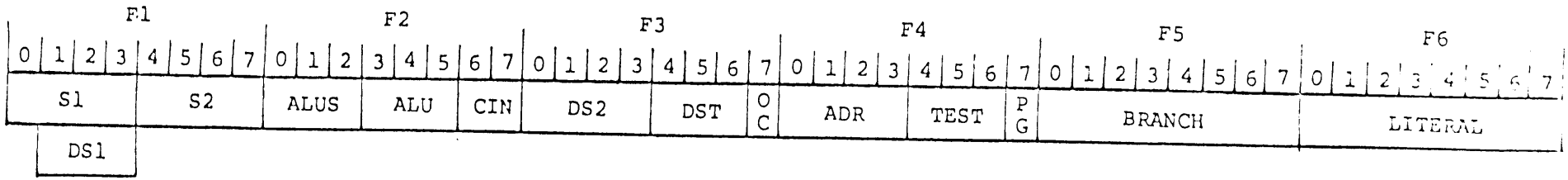


FIGURE 5-8 Microinstruction Word

1. A program counter/register within the CSAP.

2. A five word stack within the CSAP.

3. Branch addresses directly from bits 00-07 of field five (CD-5).

Note that bits 04 through 06 of field four (CR4) control test condition multiplexer K14. This multiplexer connects one of seven selected conditions to the $\overline{TEST}$ line when specified by the current microinstruction being executed. The conditions tested for are as follows:

TABLE 5-5: Address Modification Conditions

Mnemonic	Condition
$\overline{C}$	No carry from 2901A ALU
Z	ALU result is zero
C	Carry from ALU
N	ALU sign bit is logical true
V	ALU has overflowed
INIT	Initiate

Note that bus signal BDCOKH if ever low disables the output of the CSAP and generates a Reset (RST) signal.

5.2.2.7 D Bus Multiplexer

The D bus multiplexer, shown on sheets 7 and 11, is the information source to the 2901A array processor. The multiplexer comprises circuits F11, F14, and H14 on sheet 7 and circuits J5, J6, and K4 on sheet 11. Circuits J5, J6, and K4 also function as storage registers. One additional information source for the D bus is PROM L14, shown on sheet 10, which supplies the literal (LIT).

Field one, bits 00 through 03, and bit 02 of field two, via circuit L9 (sheet 2) gate the selected source to the D bus. Information sources to the D bus are as follows:

TABLE 5-6: Information Sources To D Bus

Circuit	Sheet	Source
L14	10	Literal from control memory
F11, F14	7	Microdata data bus upper and lower bytes
H14	7	Controller status
J6	11	Data from disc
J5, K4	11	Disc status

5.2.3.3 Tape Timing And Configuration Logic

The logic shown on sheet 12 generates the proper frequencies at which characters are written on tape depending on tape speed and packing density. To derive all the frequencies required, a second oscillator, K1, is required. This oscillator generates a frequency of 1.44MHZ.

CLKA is divided by circuit L1 to generate a frequency of 1MHZ. The output of K1 is divided by H1 to generate a frequency of 360KHZ. Frequencies 1.44MHZ, 1MHZ, and 360KHZ are connected to selector J1 the output of which is $\overline{\text{CLK1}}$. J1 is controlled by PIC05 and PIC06 (via the Y bus) to select the transfer density. Density is selected by bits of the MTC register.

Signal $\overline{\text{CLK1}}$ is divided by circuits H5 and J7 to generate CLK2, which is the Write Data Strobe (WDS) to the tape drive.

Circuits H5 and J7 are controlled by switch J5 to generate the proper clock frequency to the tape depending upon tape speed. The switch settings versus tape speed are given in Table 2-1.

Note that circuits F1 and H8 divide the 1MHZ clock. The circuits are connected as divide-by-10 counters, therefore, the output at TIMER is a frequency of 1KHZ.

The output of flip-flop F4-5 is the write clock; the output of flip-flop F4-9 is the read clock. These two clocks are ORed then synchronized by $\overline{\text{PPCLK}}$ in flip-flop to generate the Data Request Flag (DRQ FLG).

5.2.3.4 Cable Driver/Receivers and Control Buffers

Sheet 13 illustrates the interconnect circuits between the tape drives and the controller, tape drive address decoder, and control buffers.

Circuits L7, L8 and L9 buffer signals to the tape drives. Refer to the Glossary of Terms for signal definitions.

Circuit L4 decodes PIC00, PIC01, and PIC02 to select one of a possible four tape drives.

Circuit K9 temporarily stores:

1. Read Data Parity CRDP from tape
2. Write Amplifier Reset (WAR) to tape
3. Set Write Status to tape

TABLE 5-4: [illegible]

TERM	DESCRIPTION	ORIGIN SHEET
A00	Q bus Address bit o, LSB	1
A01	Q bus Address bit 1	1
A02	Q bus Address bit 2	1
A03	Q bus Address bit 3, MSB	1
ACK	Acknowledge	1
ACKFF	Acknowledge Flip-Flop	1
ADRA	Address A	2
ADRB	Address B	2
A00FF	Address bit 0 Flip-Flop	1
AS00	A State Sequencer bit 00	1
AS01	A State Sequencer bit 01	1
AS02	A State Sequencer bit 02	1
BACT FF	Bus Activity Flip-Flop	1
BBS7 L	Q bus Bank Seven Select	4
BDAL00 L-	Q bus Data Address Lines (16)	3
BDAL15 L		
BDCOKH	Q bus DC power OK	4
BDOUT L	Q bus Data Out from master	4
BDIN L	Q bus Data In from master	4
BDMGI L	Q bus DMA Grant In	4
BDMGO L	Q bus DMA Grant Out	4
BIAKI L	Q bus Interrupt Acknowledge Input	4
BIAKO L	Q bus Interrupt Acknowledge Output	4
BINIT L	Q bus Initialize	4
BIRQ L	Q bus Interrupt Request	4
BDMR L	Q bus Direct Memory Request	4
$\overline{\text{BOT}}$	Beginning of Tape Mark	13
BRPLY L	Q bus Reply from slave	4
BSACK L	Q bus Select Acknowledge	4
$\overline{\text{BSTCLK}}$	Q bus Clock	2
BSYNC L	Q bus Synchronize	4
BWTBT L	Q bus Write Byte	4
BR°FF	Bus Reply Flip-Flop	1
BSS7	Bank 7 Select	4
BSY	Busy	2

TERM	DESCRIPTION	ORIGIN SHEET
CLKA	Clock 10 megahertz	2
$\overline{\text{CLK 1}}$	Clock one to the tape drive	12
CN+2	Carry output of 2901	8
$\overline{\text{CLRB}}$	Clear Bus	2
$\overline{\text{CLR}}$	Clear	1
CR1-00-- CR1-07	Control Register one output bits 0-7	10
CR2-00-- CR2-07	Control Register two output bits 0-7	10
CR3-00-- CR3-07	Control Register three output buts 0-7	10
CR4-00-- CR4-07	Control Register four output bits 0-7	10
CR5-00-- CR5-07	Control Register fieve output bits 0-7	10
CS	Carry signal out of second 2901	8
CSA00-- CSA08	Control Store Address bits 0 through 08 (9)	9
D00-- D07	2901 Data bus bits 0-7	10/11
DA	Data Enable	1
DA16,DA17	Data Address bits 16 and 17	2
DB00- DB15	Data bus bits 00-15 from Q bus Bit 15 is MSB, bit 00 is LSB	3
DB16,DB17	Data bus bits 16 and 17 (Address extension)	4
$\overline{\text{DEN}}$	Device Enable	1
DIN	Data In	1
DINFF	Data In Flip-Flop	1
DMG	Direct Memory Grant Delayed	1
DMGFF	Direct Memory Grant Flip-Flop	1
DMGI	Direct Memory Grant In from Q bus	4
+DMR	Direct Memory Request	1
DOUT	Data Out	1
DOUTFF	Data Out Flip-Flop	1
DRQFLG	Data Request Flag	12
DSL	Density Select to Tape	13
$\overline{\text{EOT}}$	End of Tape from Tape	13
FLPT	File Protect from Tape	13

TERMS	DESCRIPTION	ORIGIN SHEET
RSYNC	Synchronize From Q bus	4
RWC	Rewind Command to Tape	13
$\overline{\text{7TRK}}$	7 or 9 Track Status from Tape	13
SEL1-SEL4	Select Tapes 1, 2, 3, or 4	13
SFC	Synchronous Forward Command to Tape	13
SWS	Set Write Status	13
SRC	Synchronous Reverse Command to Tape	13
$\overline{\text{STA}}$	Status	2
STORL,U	Store Lower, Upper Byte	1
TA	Tag clock for extended address bits	2
TDIN	Transmit D Bus In	1
TDOUT	Transmit D Bus Out	1
TD00G	Transmit D Bus bit 00 Gated	1
TDMR	Transmit Direct Memory Request	1
TDMG	Transmit Direct Memory Grant	1
TIAK	Transmit Interrupt Acknowledge	1
TIRQ	Transmit Interrupt Request	1
TRPLY	Transmit Reply	1
TSACK	Transmit Select Acknowledge	1
TO	Time Out	2
TOD	Time Out Delay	2
TSYNC	Transmit Sync	1
$\overline{\text{TRDY}}$	Tape Ready from Tape	13
TWTBT	Transmit Write Byte	1
VS	Overflow from 2901	8
WARS	Write Amplifier Reset to Tape	13
WDS	Write Data Strobe to Tape	13
WDP	Write Data Parity to Tape	13
WD0-WD7	Write Data Lines (8) to Tape	13
$\overline{\text{WRL}}$	Write Load	2
$\overline{\text{WRU}}$	Write Unload	2
WTBTFF	Write Byte Flip-Flop	1
Y00--	Y Bus bits 0 through 7	8
Y07		

SECTION 6

TROUBLESHOOTING GUIDE

6.0 INTRODUCTION

The purpose of this section is to assist the maintenance engineer in isolating malfunctions to specific assemblies of the tape based computer system. Normally, once a malfunctioning assembly (tape drive, memory, controller, CPU board, etc.) is located, a known good assembly should be substituted while the malfunctioning unit is returned to a repair depot. Be sure to read carefully paragraph 6.2, Operating Precautions, before troubleshooting the system.

6.1 GENERAL

System malfunctions come under two major classifications: intermittent and continuous. Intermittent failures are normally very difficult to isolate and usually require step-by-step substitution of equipment over a period of time until the intermittant assembly is isolated. This section will primarily discuss continuous failure isolation.

When troubleshooting electronic equipment, certain basic items should always be checked:

A. Is power properly applied to all system assemblies -- switches on, fuses good, AC power cords plugged in, area power circuit breakers on, etc.

B. Check DC power at backplane terminals of computer - +5V DC, +12V DC. If DC voltages are low, verify AC line voltage is within tolerance:

100 - 127 Vrms, 50±1 HZ or 60±1 HZ
200 - 254 Vrms, 50±1 HZ or 60±1 HZ

C. Verify system generates proper response when system is powered-up (refer to operation instructions for the processor).

D. Verify all modules are properly plugged in. No empty slots should exist between modules.

E. Verify all signal cables (tape, console terminal) are properly plugged in. Check each end of cables.

F. Can the console be operated in "Local" mode? If not, console is defective.

G. Is the tape drive READY light on?

H. Are the computer panel switches set correctly (ENA HALT LTC, etc.)?

I. Is green DIAG light on tape controller board on?

6.2 OPERATING PRECAUTIONS

While troubleshooting the system, the engineer should check the following items:

A. Is the tape clean? Dirty tape or tape read/write heads cause bit dropouts.

B. If tape produces a high-pitched whine or metal-to-metal sound, immediately power down the tape; a bad bearing is possible.

C. Was any module pulled out or plugged in while power was applied? Shorting connector pins together can cause integrated circuit to fail.

D. Has ribbon cable connector been plugged in upside down at controller? This connector is not keyed. Be sure the arrows on the female connector line up with arrows on male connector.

6.3 POSSIBLE TROUBLES

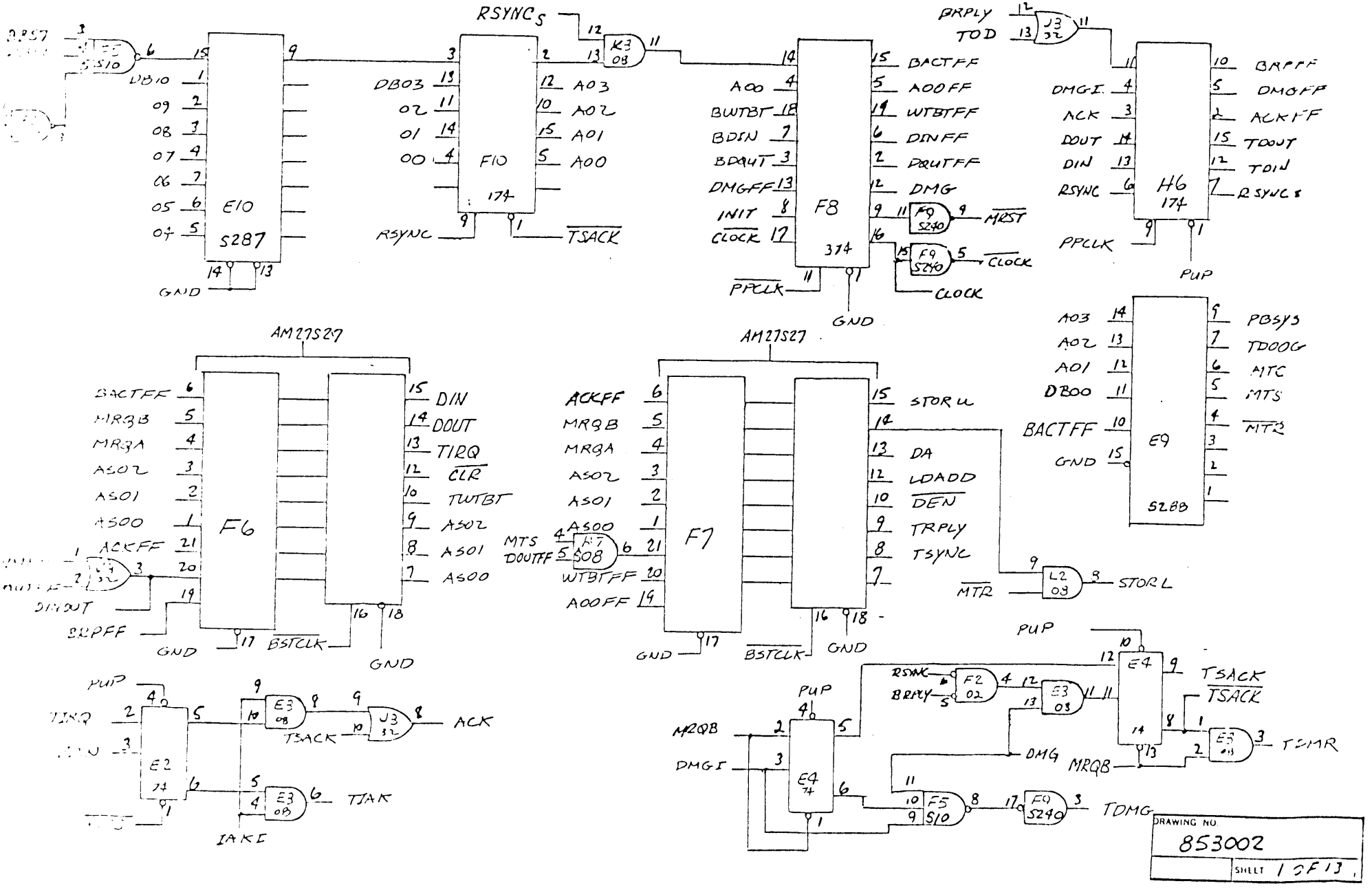
This paragraph provides possible malfunction locations based on either visual indications or tests and assumes the basic items in paragraph 6.1 have been checked and found normal.

NOTE

Before troubleshooting the system be sure proper operating procedures are being followed and the system is properly configured. Refer to Sections 2 and 3 of this manual or the USER'S GUIDE.

The following pages contain a trouble chart. Space is left on the chart for field failures not in the chart to be noted.

PROBLEM	POSSIBLE CAUSE	CHECK/REPLACE
1. GREEN DIAGnostic light on controller is OFF.	1. Microprocessor section of controller inoperative.	1. Controller.
	a. Crystal not seated in socket or in wrong.	Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or stuck low", or half-amplitude pulses. If no switching, either power or crystal bad.
	b. Short or open on board.	
	c. Bad integrated circuit.	
2. No communication between console and computer.	2. I/O section of controller "hanging up" QBus.	2. Computer interface logic of controller.
	a. $\overline{\text{DEN}}$ always low.	a. Check signal DEN for constant assertion.
	b. Shorted bus transceiver IC.	b. Check I/O IC's. Remove controller board to see if trouble goes away.
	c. Bad CPU board	c. Run CPU diagnostics.
3. No data transfers to/from tape. BSY light never lights.	3. Tape not ready or bad cable connection.	3. Check tape switches and cable connectors.
	a. Improper communication with tape registers on controller or bad IC in register section of controller.	a. Load and read tape registers from console with processor halted. i.e. RKDS, RKDA, RKER. Verify bits loaded can be read.
4. Data transferred to/from tape incorrect. DMA and BSY lights blink to indicate transfers.	4. Bad memory board in backplane.	4. Run memory diagnostis.
	a. Noise or intermittent source of DC power in computer.	a. Check AC and DC power.
	b. Bad IC in tape I/O section of controller.	b. While operating, check lines from controller to tape with a 'scope for short or open.
	c. Run tape diagnostic, set console to make system "Halt On Error."	c. Analyze error halt.
	d. Bad area on tape.	d. Errors should always occur in same sector of tape.
	e. Head worn.	e. Replace head.
	f. Crystal in controller wrong frequency.	f. Check characteristics of tape drive.
	g. Configuration switch J4 not set properly.	g. Check configuration paragraph of Installation Section.


RSYNCS
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BACTFF
AOOFF
WTBTFF
DINFF
DOUTFF
DMG
MRST
CLOCK
TSACK
DB10
DB03
DB02
DB01
DB00
A03
A02
A01
A00
RSYNC
GND
PPCLK
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DMGI
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PUP
TOOUT
TOIN
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TDOOG
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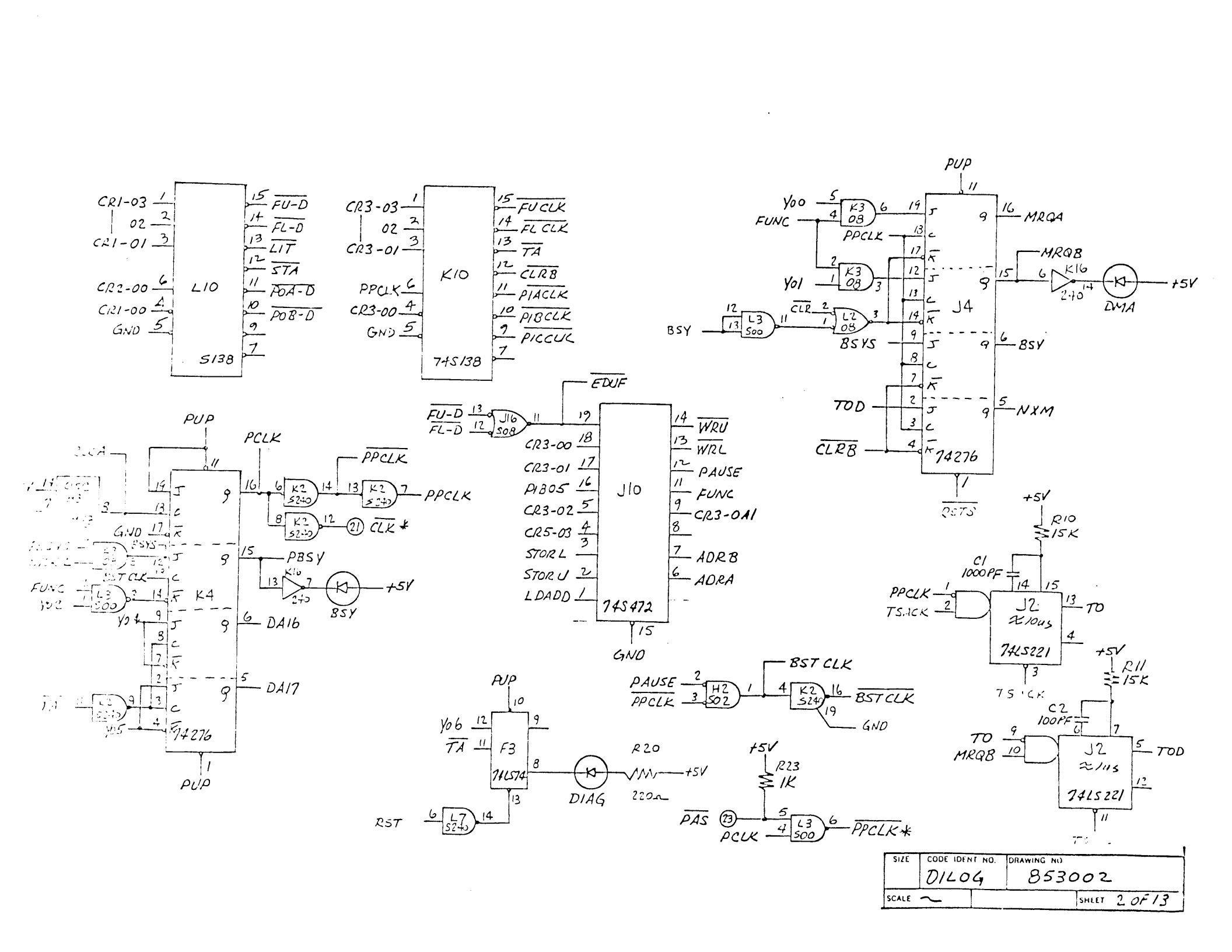

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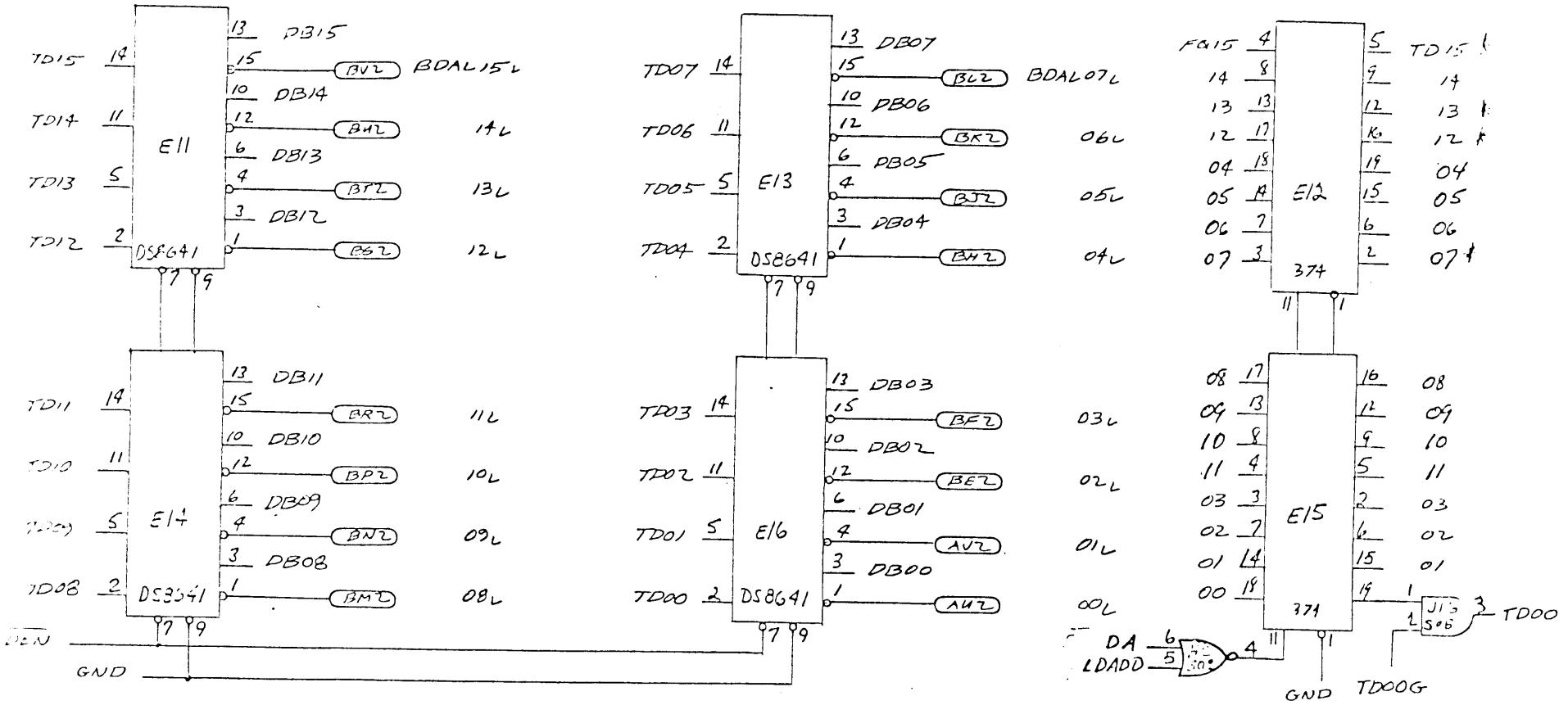

DATA BUS RCVR/DVR

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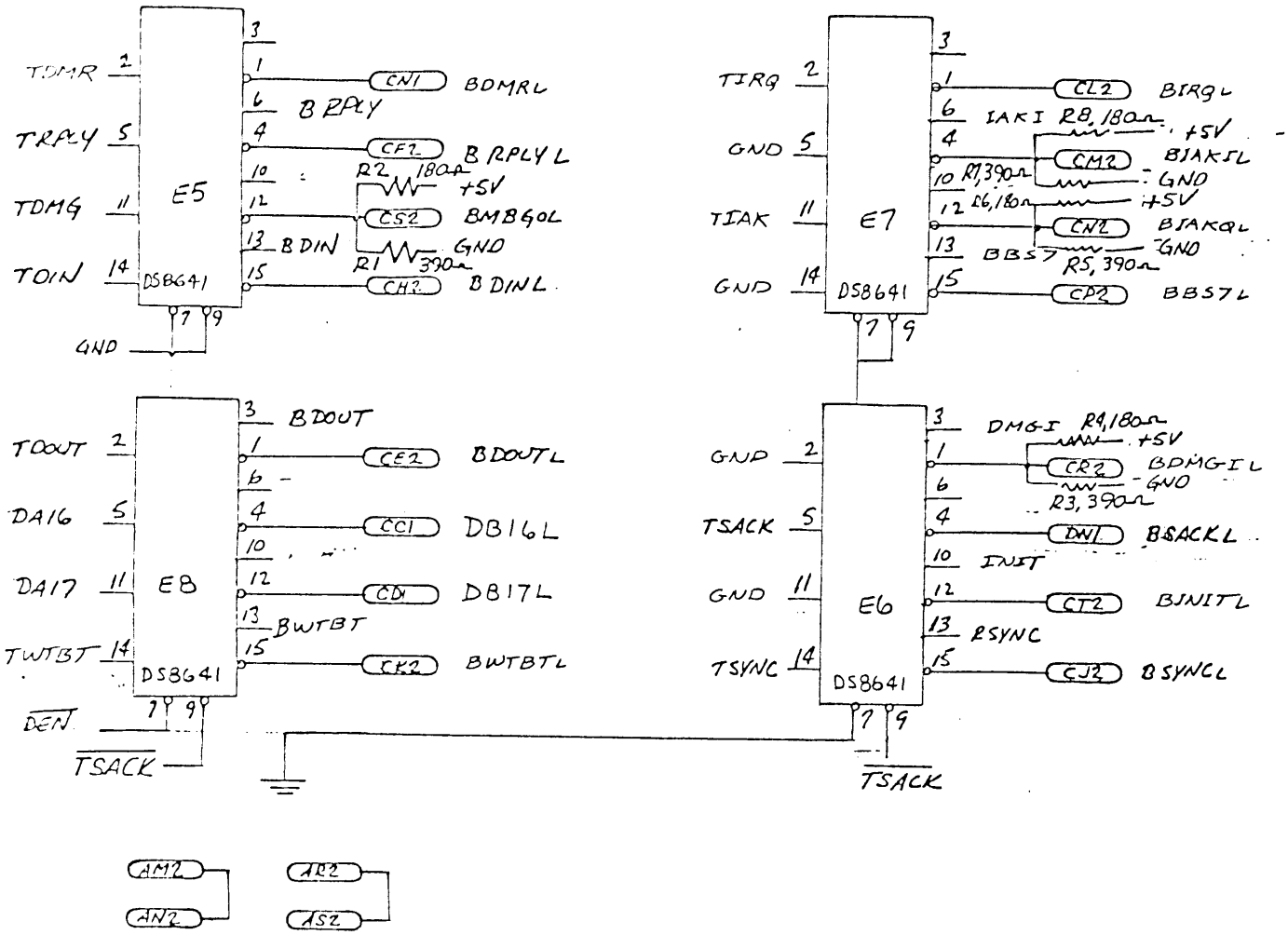

9 BUS CONTROL

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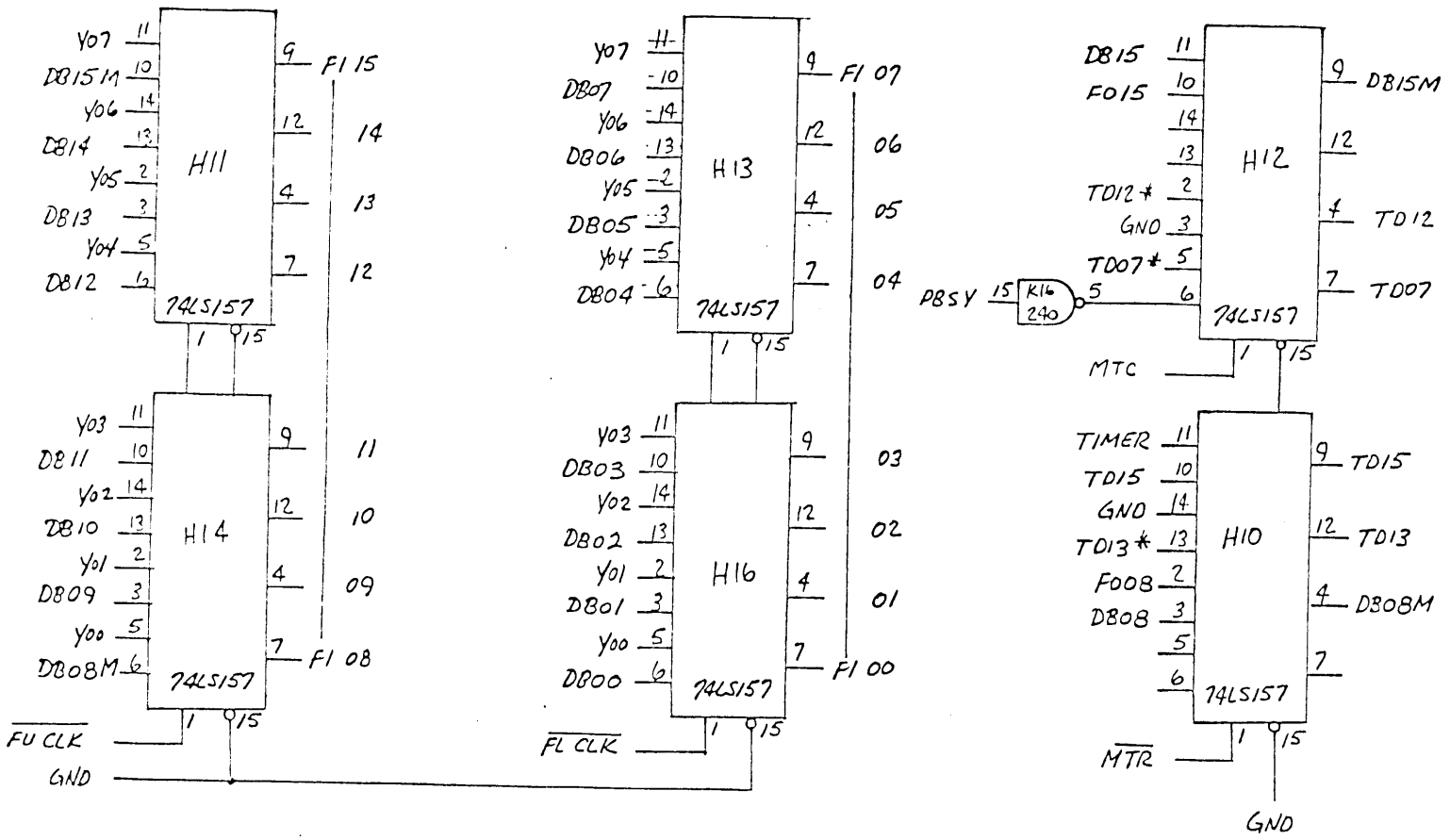

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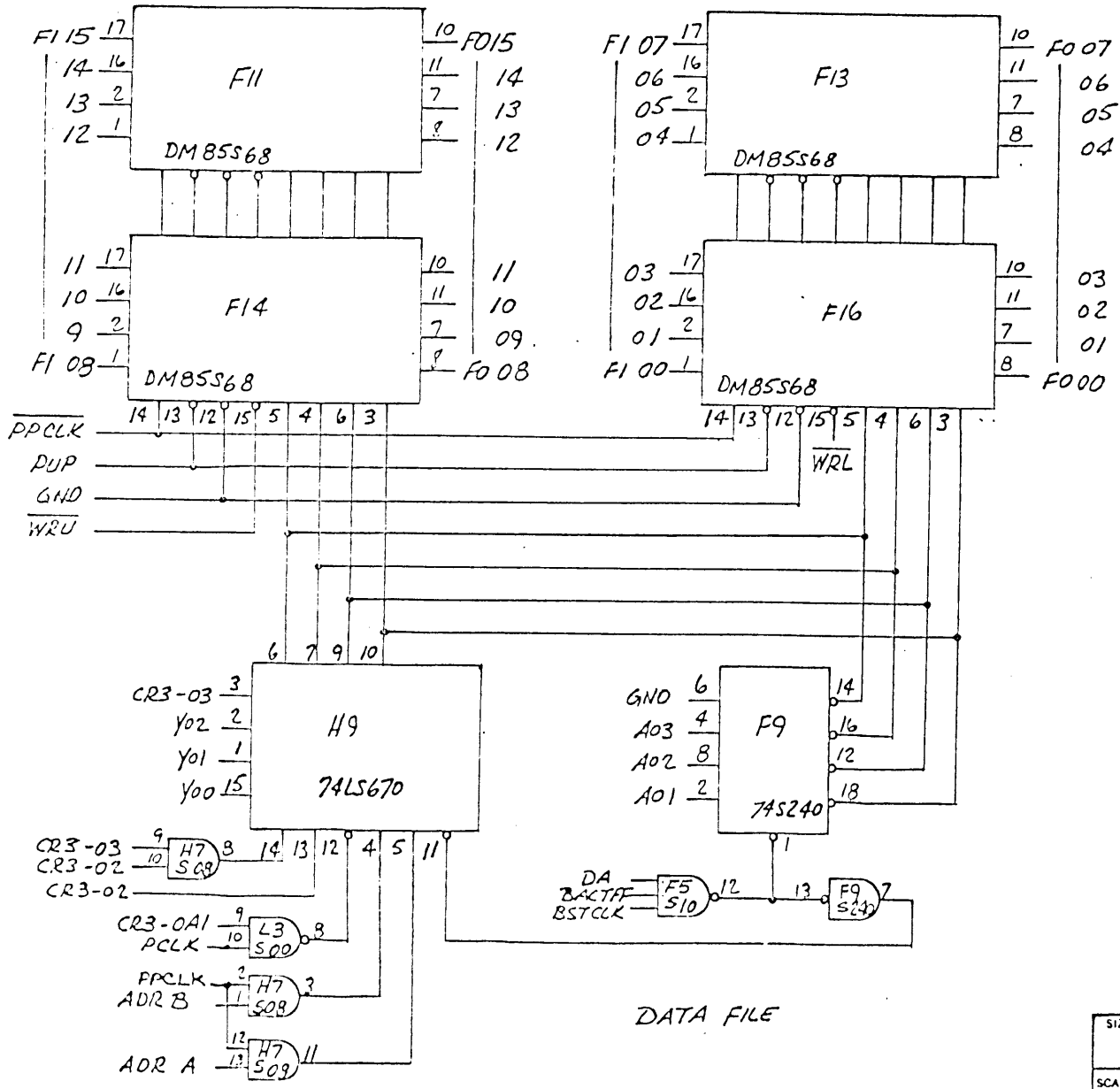

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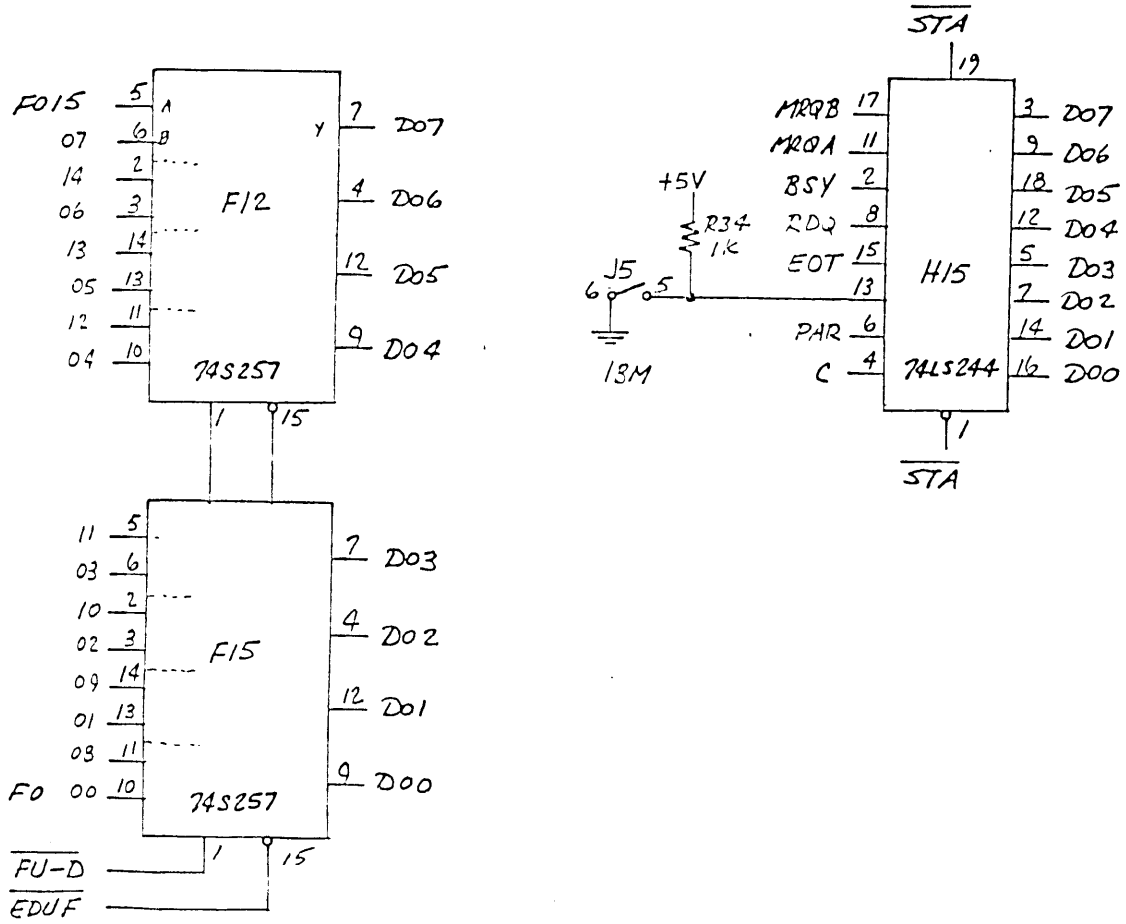

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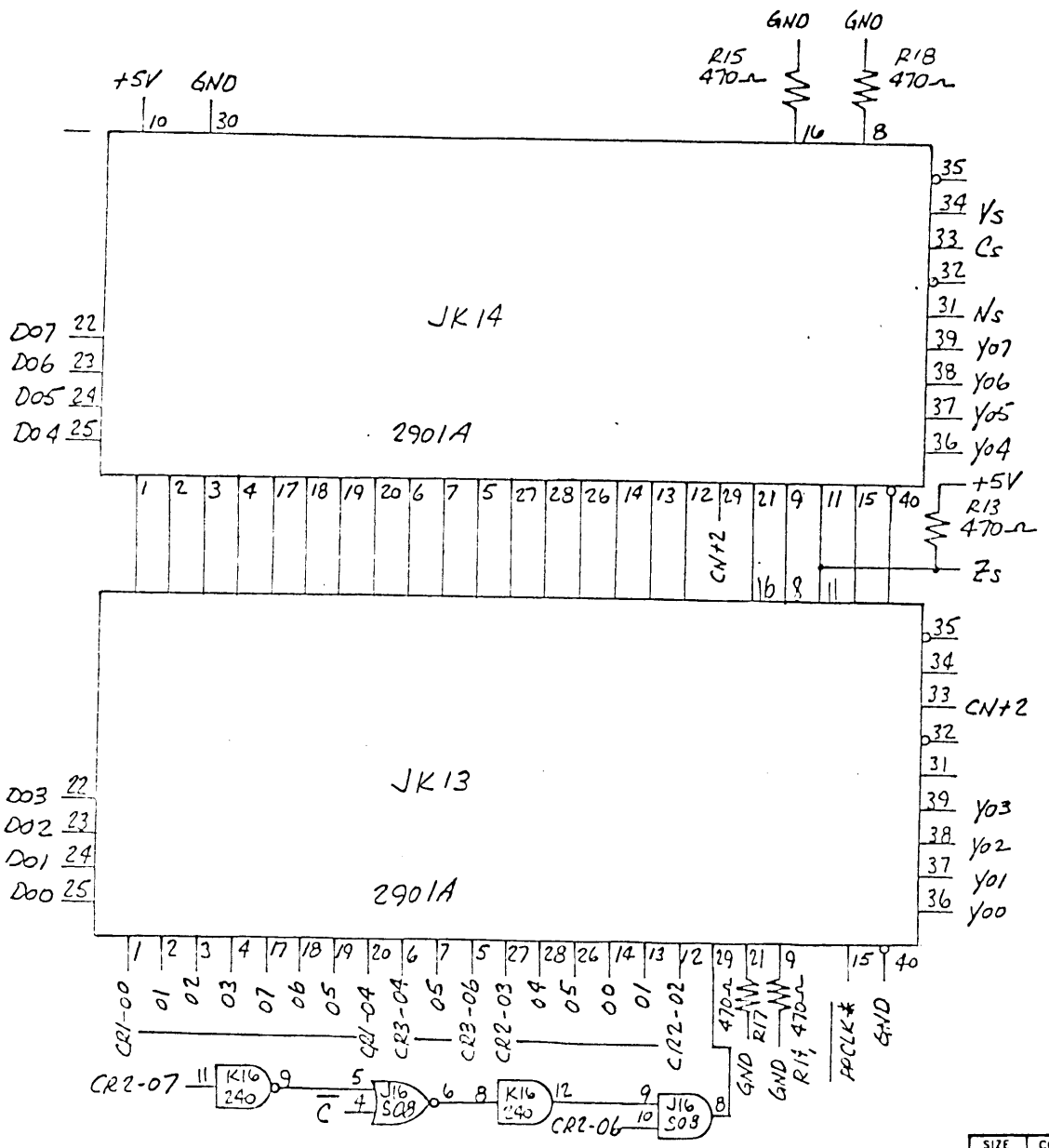

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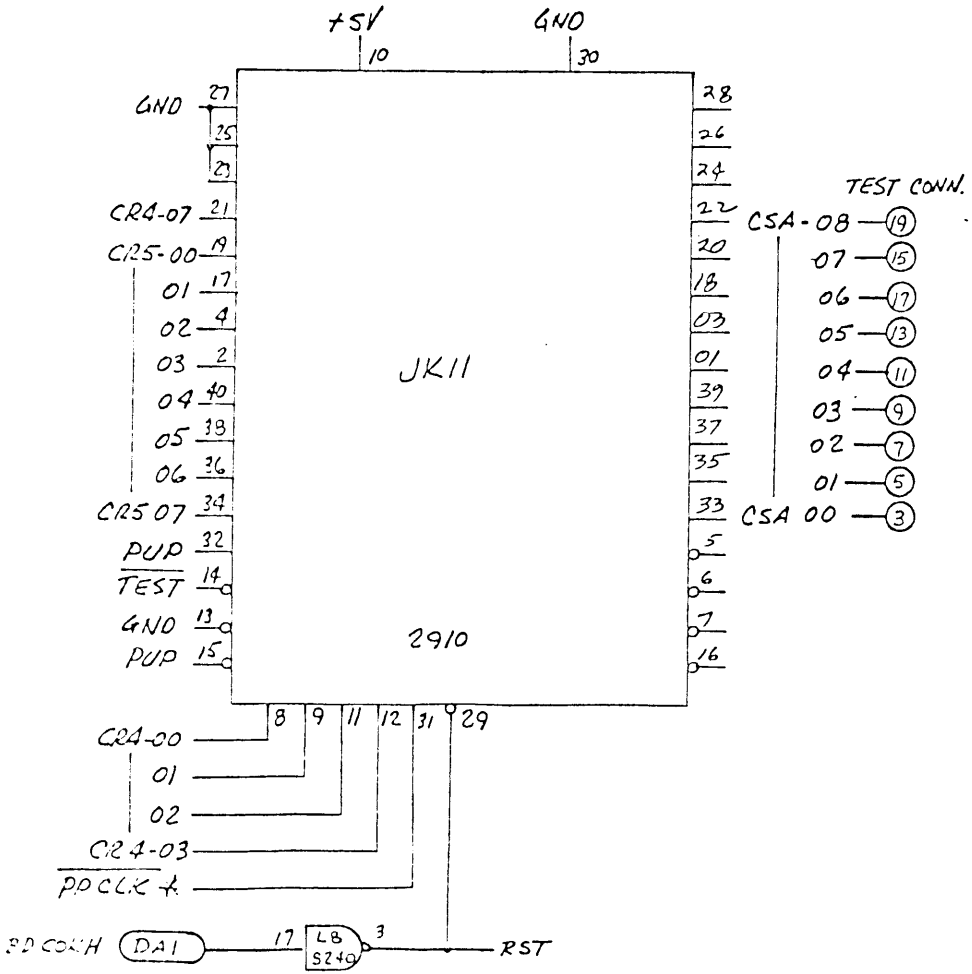

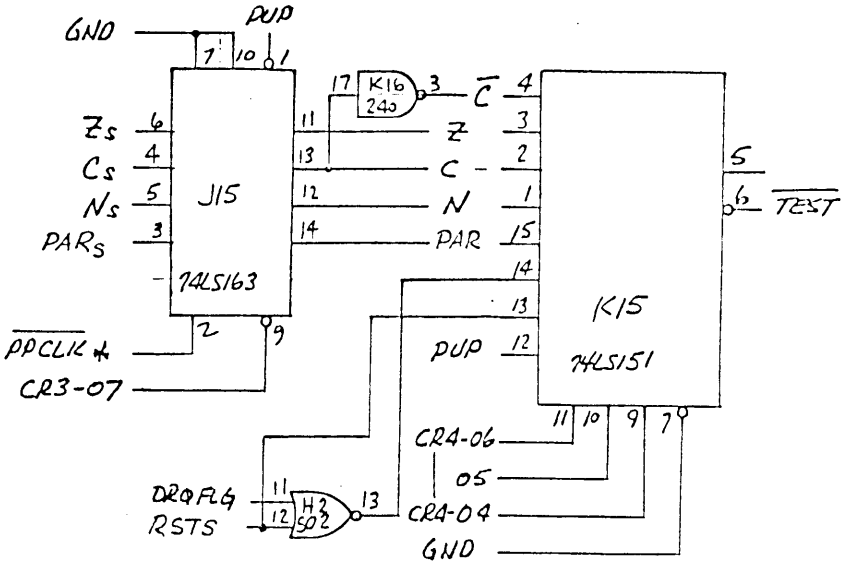

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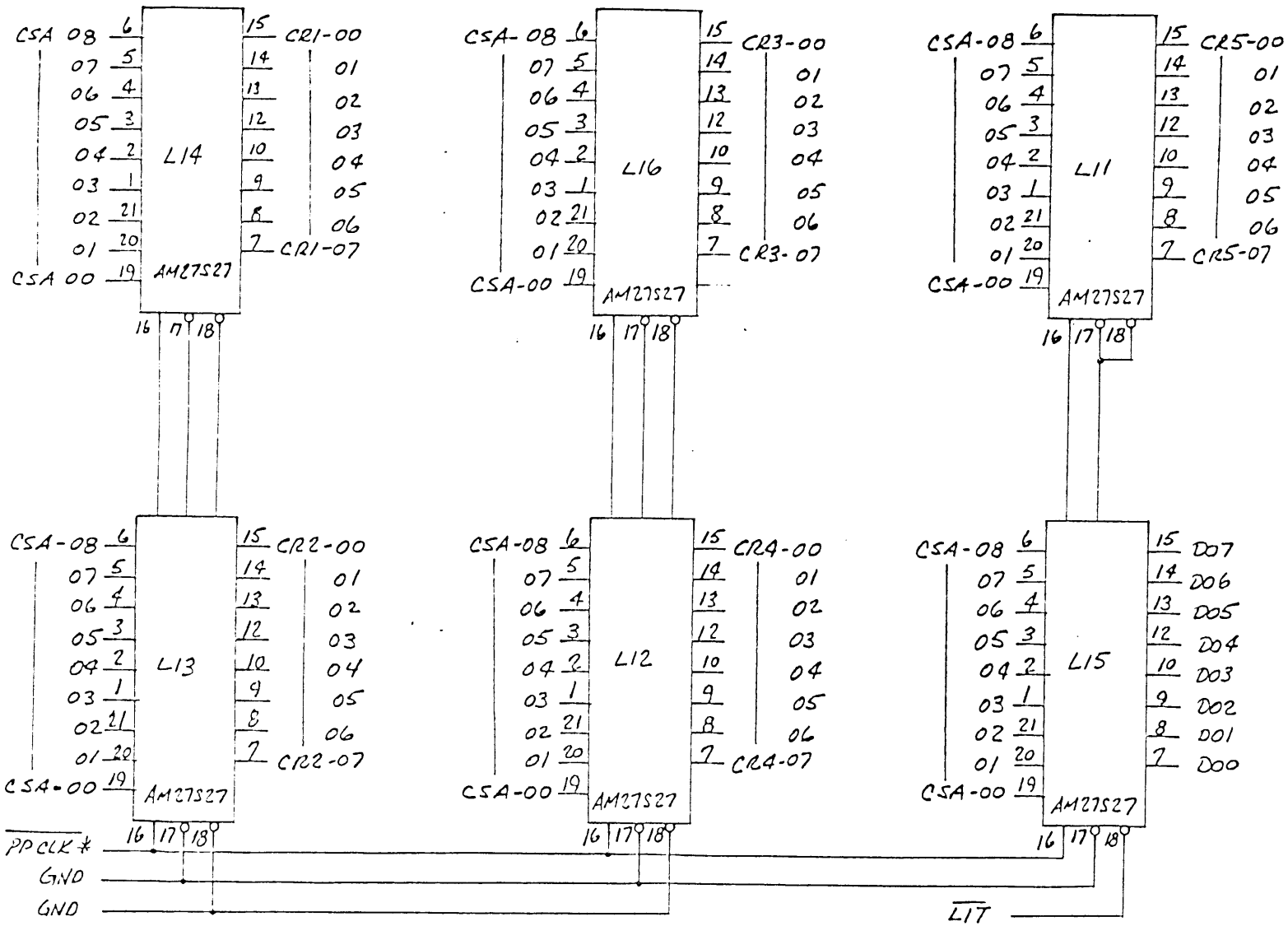

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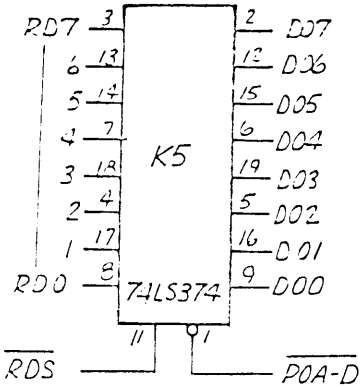
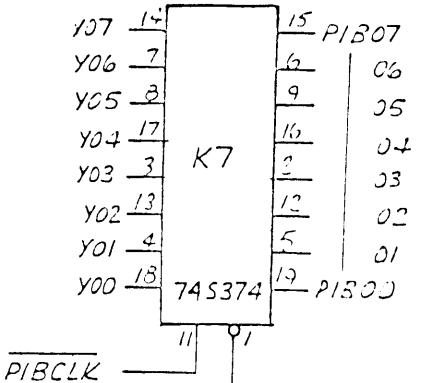
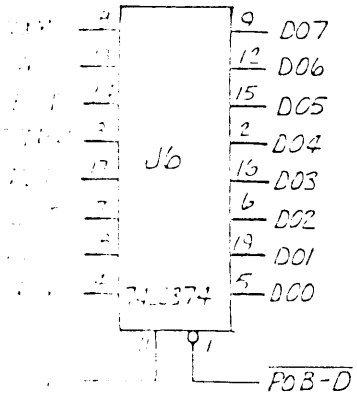
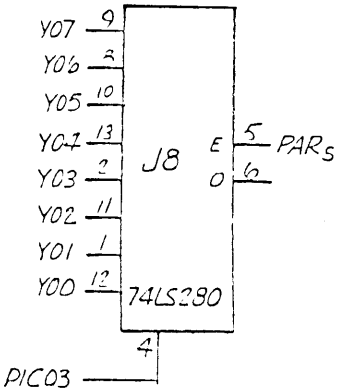
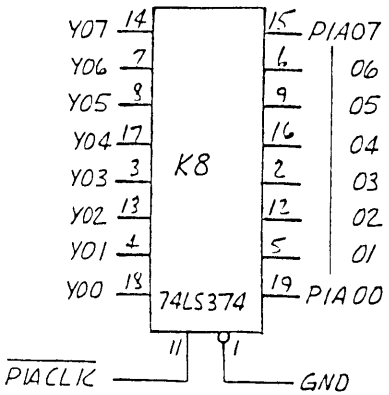
SCALE ~		SHEET 10 OF 13

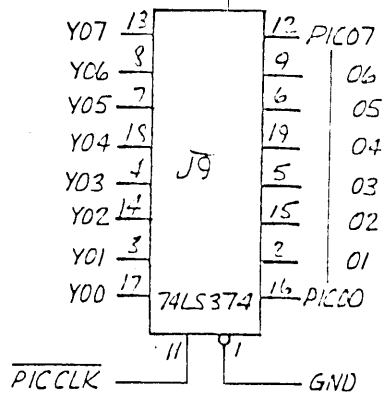




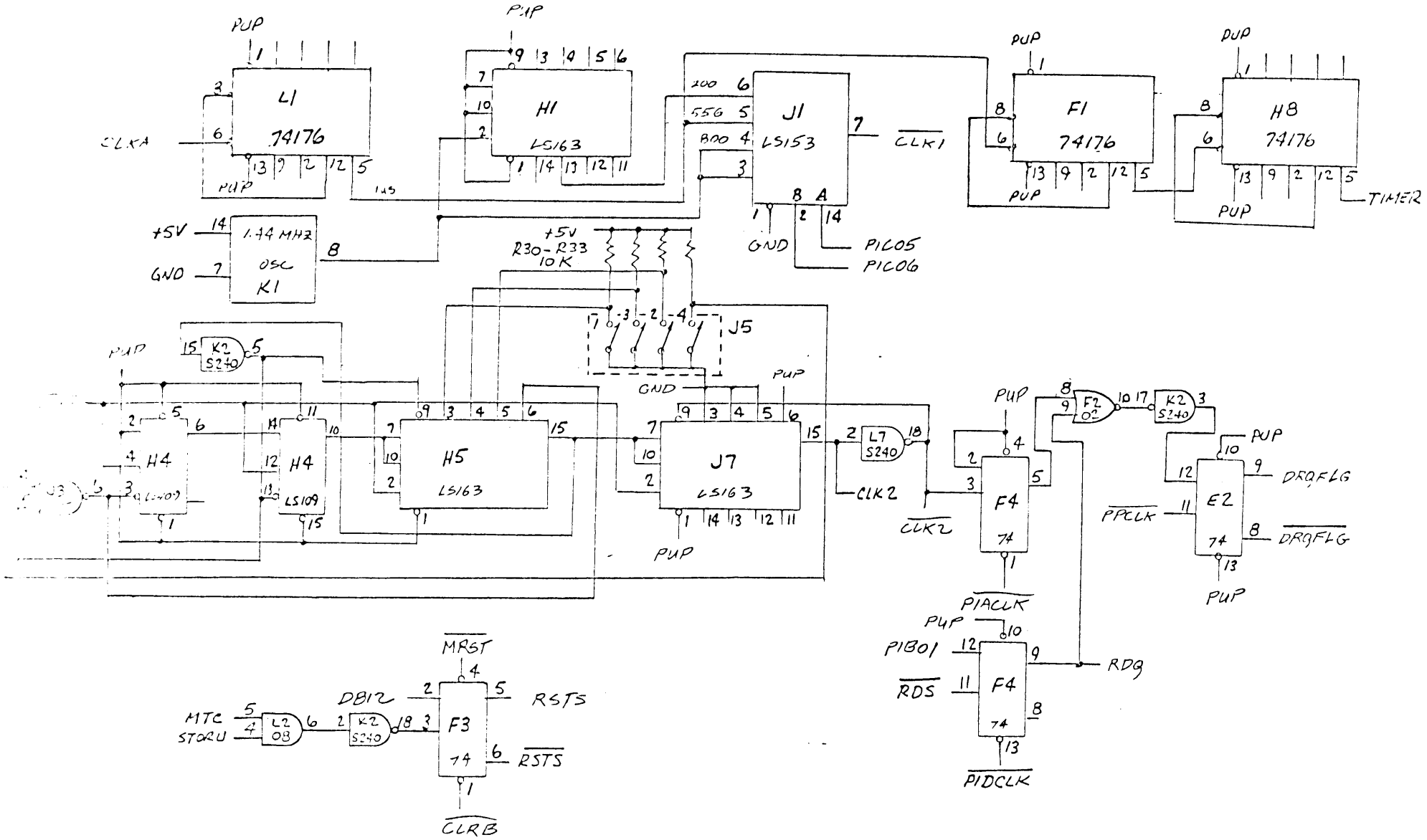




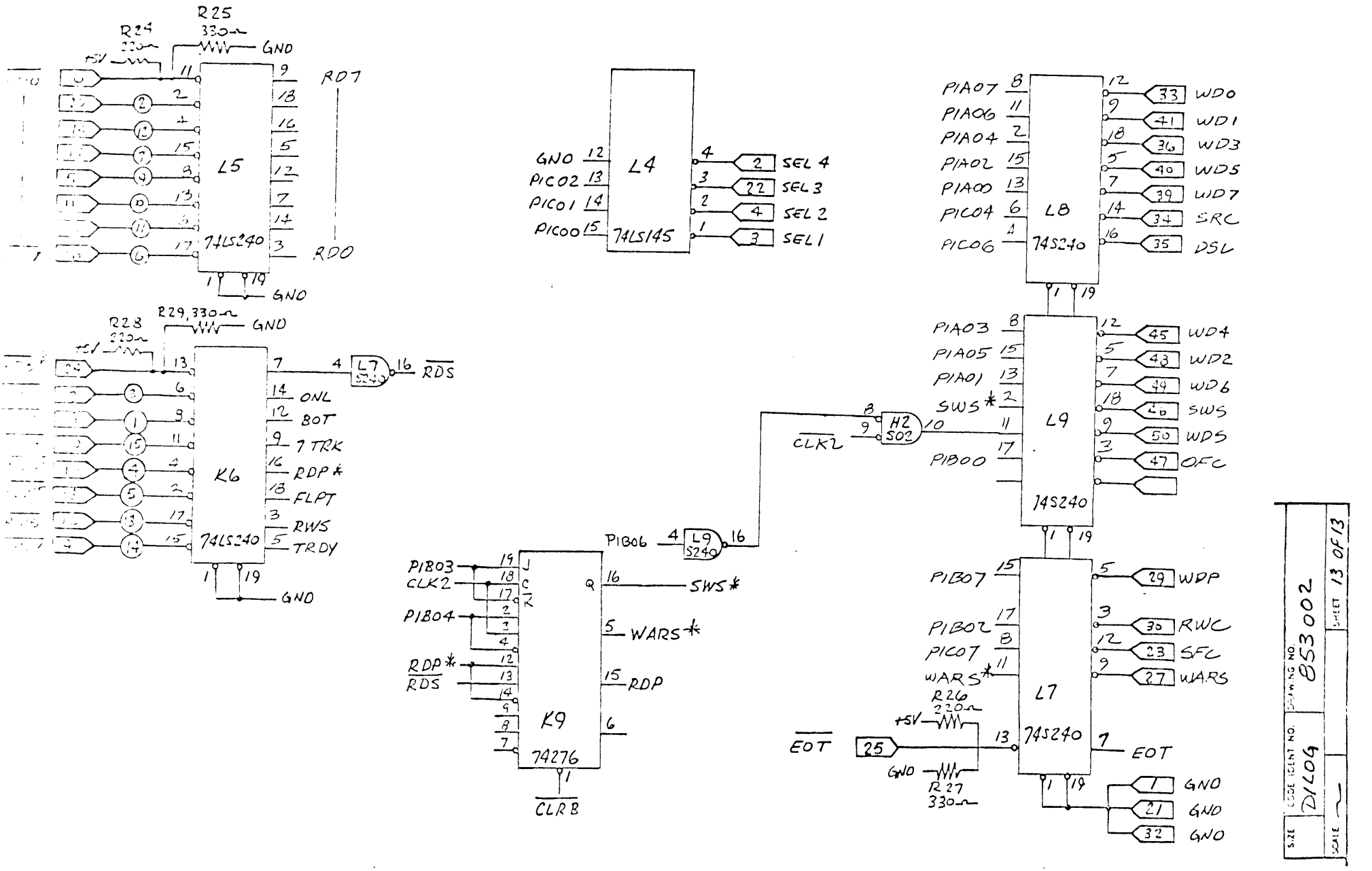




SIZE	CODE IDENT NO.	DRAWING NO.
	DICOG	853002
SCALE ~		SHEET 11 OF 13



SIZE	CODE IDENT NO.	DRAWING NO.
	DIL04	853002
SCALE ~		SHEET 12 OF 13



SIZE	CODE IDENT NO. D1L04	DRAWING NO. 853002	SHEET 13 OF 13
		SCALE	

APPENDIX "A"

CABLE LIST

[illegible] LIST

FROM	TO	FUNCTION
P1- 1	J101-2	GND
2	J101-V	SEL4
3	J101-J	SEL1
4	J101-A	SEL2
5	J103-14	RD4
6	J103-3	RD0
7	J103-V	GND
8	J103-17	RD6
9	J101-T	TRDY
10	J103-11	7TRK
11	J103-15	RD5
12	J101-N	RWS
13	J101-P	FLPT
14	J103-8	RD2
15	J103-9	RD3
16	J103-18	RD7
17	J101-M	ONL
18	J103-1	RDP
19	J101-R	BOT
20	J103-4	RD1
21	J103-B	GND
22	J101-18	SEL3
23	J101-C	SFC
24	J103-2	RDS
25	J101-U	EOT
26	J101-17	GND
27	J102-C	WARS
28	J102-18	GND
29	J102-L	WDP
30	J101-H	RWC
31	J101-7	GND
32	J102-1	GND
33	J102-M	WD0
34	J101-E	SRC

MAGNETIC TAPE CABLE LIST, continued

FROM	TO	FUNCTION
P1-35	J101-D	DSL
36	J102-R	WD3
37	J102-13	GND
38	J102-11	GND
39	J102-V	WD7
40	J102-T	WD5
41	J102-N	WD1
42	J102-17	GND
43		GND
44		GND
45	J102-S	WD4
46	J101-K	SWS
47	J101-L	OFC
48	J102-P	WD2
49	J102-U	WD6
50	J102-A	WDS

P1 = 3425-6050 (3M) 50 pin socket

J101, J102, J103 = 251-18-30-160 (TRW) 18 pin dual contact edge card