

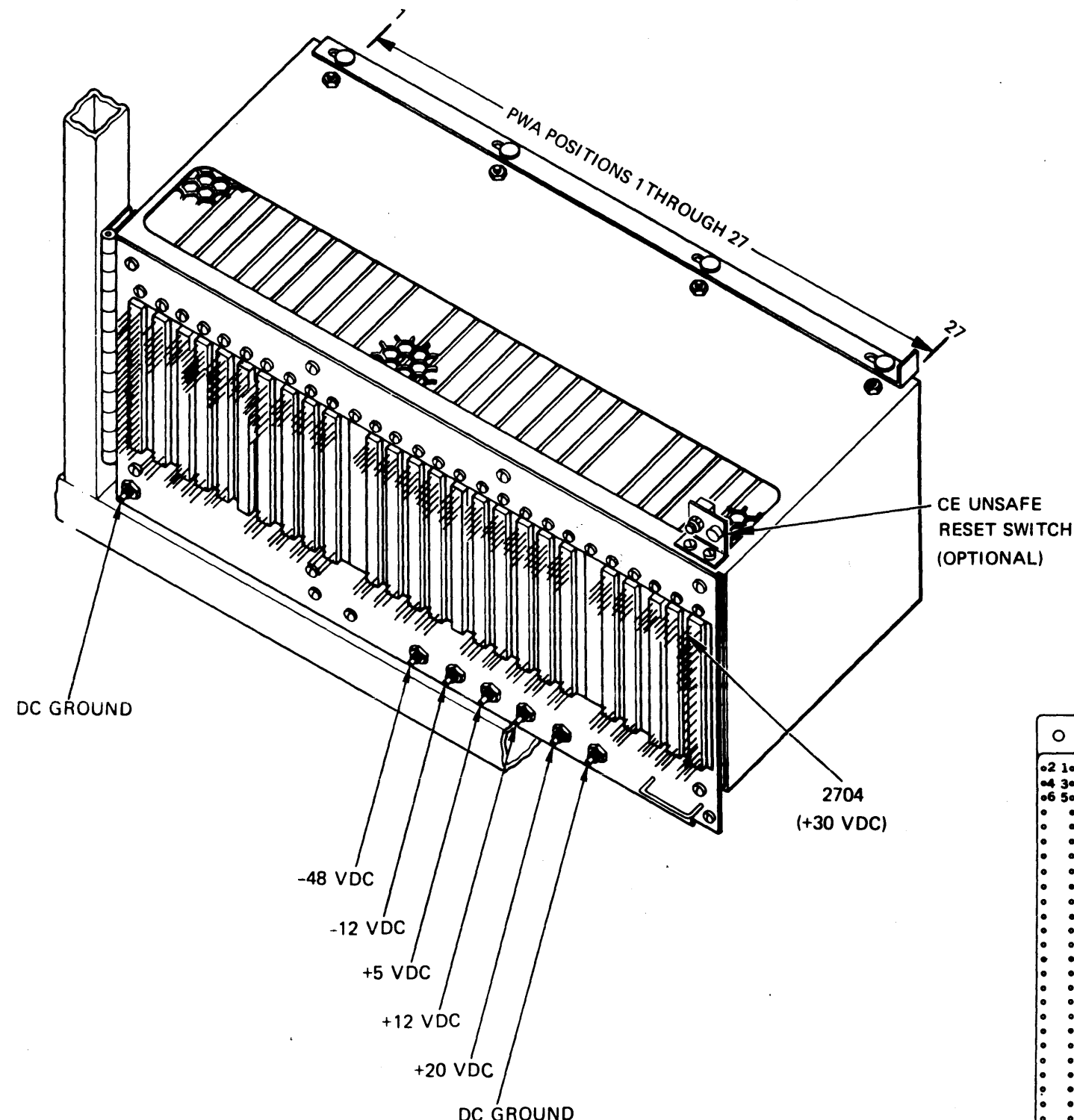
10.6 PWA ASSIGNMENTS

Table 10-3 lists the printed wiring assemblies located in the electronic gate. The revision level of each part number is given in Chapter 9, Parts Identification.

Table 10-3. PWA Assignments in Electronic Gate

GATE POS.	PART NUMBER	PWA TITLE
1	INTERFACE	READ/WRITE PADDLE
2	75000003-X	SELECT 0-9
3	75000068-X	SELECT 10-19
4	75004343 X	WRITE
5	75003548-X	READ
6	75003978-X	DEFECT DETECTOR
7	INTERFACE	SCU SIGNAL PADDLE
8	75004484-X	HEAD ADDRESS REGISTER (HAR)
9	75003727-X	CYLINDER ADDRESS REGISTER (CAR)
10	INTERFACE	DIAG UNIT DISPLAY PADDLE
11	NOT USED	
12	75003461-X	FILE STATUS
13	75003728-X	DIFFERENCE COUNTER
14	75003370-X	ACCESS CONTROL
15	75002523-X	CURVE GENERATOR
16	75004293-X	DIFFERENCE CALCULATOR
17	75003462-X	INDEX TRANSDUCER CUSTOMER OPTION
18	75004139-X	TEMPERATURE COMP & SAFETY
19	INTERFACE	TRANSDUCER PADDLE
20	75003713-X	CYLINDER DETECTOR
21	75002521-X	AUTOMATIC GAIN CONTROL (AGC)
22	NOT USED	
23	75003719-X	TACHOMETER
24	75003720-X	PULSER AND SUMMING AMP
25	75004138-X	CYLINDER SELECTOR
26	INTERFACE	PWR SEQ AND PULSER PADDLE
27	75003394-X	POWER CONTROL
*28	75000065-X	MATRIX A
*29	75000065-X	MATRIX B

*These PWA's located on CAM Tower



VOLTAGE LEVELS	
NOMINAL	RANGE
-48 VDC	-43.7 TO -51.3 VDC
-12 VDC	-11.5 TO -13.5 VDC
+12 VDC	+11.5 TO +13.5 VDC
+20 VDC	+19.5 TO +21.5 VDC
+5 VDC	+4.75 TO +5.25 VDC
+30 VDC SOCKET 27, PIN 4	+27.6 TO +32.4 VDC

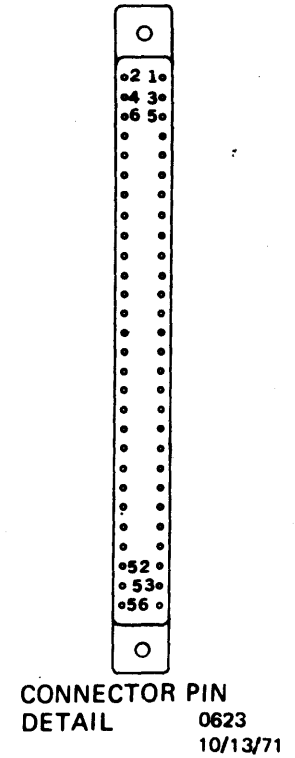


Figure 10-20. Electronic Gate

10.7 LOGIC AND SCHEMATIC

Logic diagrams and schematic diagrams for printed wiring assemblies (PWA's) are arranged in socket number order. Each diagram is a logical representation of a particular circuit configuration that is identified by a basic part number and a dash number.

In addition, schematic diagrams are presented for the following circuits located elsewhere in the disk drive:

DC Power Supply (50 Hz and 60 Hz)

Sequence Panel (50 Hz and 60 Hz)

Power Driver

The following PWA schematic diagrams are not included in this section due to their proprietary nature:

PWA 6, Defect Detector

PWA 18, Temp Comp and Safety

PWA 20, Cylinder Detector

PWA 21, AGC

PWA 23, Tachometer

10.7.1 Pin Connections

Only pins used for input and output signals are shown on the diagrams. These pins correspond with sockets in the electronic gate or terminal connection points located on other components. Test points and voltage values are provided where applicable. Voltages and ranges at pin locations where normally present are listed in Table 10-4.

Table 10-4. Pin Location Voltage Levels

PIN NO.	VOLTAGE LEVEL	RANGE
2	DC Ground	-----
10	+5V	+4.75 to +5.25 VDC
20	+12V	+11.5 to +13.5 VDC
30	+20V	+19.5 to +21.5 VDC
40	-12V	-11.5 to -13.5 VDC
56	-48V	-43.7 to -51.3 VDC

10.7.2 Logic Voltage Levels

A standard level interface voltage is employed for signal lines which interface with the control unit. The down (low) level is 0.0 to +0.5 volts (+0.0V nominal). The up (high) level is +2.5 to +5.0 volts (+3.0V nominal). Voltage levels between +0.5 and +2.5 volts are spurious signals and indicate the circuit is defective.

10.7.3 Line Names

Names assigned to signal lines on diagrams are listed at source output and destination input points. Additional information provided below the line name shows the socket and pin numbers for connection with other circuits.

For example, the output signal "+Velocity Too Great" from socket 18, pin 16 goes to 1406.

Where: 14 = Socket Number
06 = Pin Number on Socket

The sign (+) or (-) in front of the line name indicates the logic level of internal lines when active and inactive status by the designation 0X+3, -12X0, 0X-48, or 0X-12. The first value (0, -12) is the active state of the line and the second value (+3, 0, -48, -12) is the inactive state of the line. The "X" is used as a divider between the two line states.

10.7.4 Waveforms

Lines associated with a waveform are indicated by a triangle and number $\triangle 15$. The waveforms pertain to a 192-cylinder seek-seek and an 8-cylinder seek-seek, and they are presented in 10.4.

2

RELEASED FOR PUBLIC USE
 SKT 1

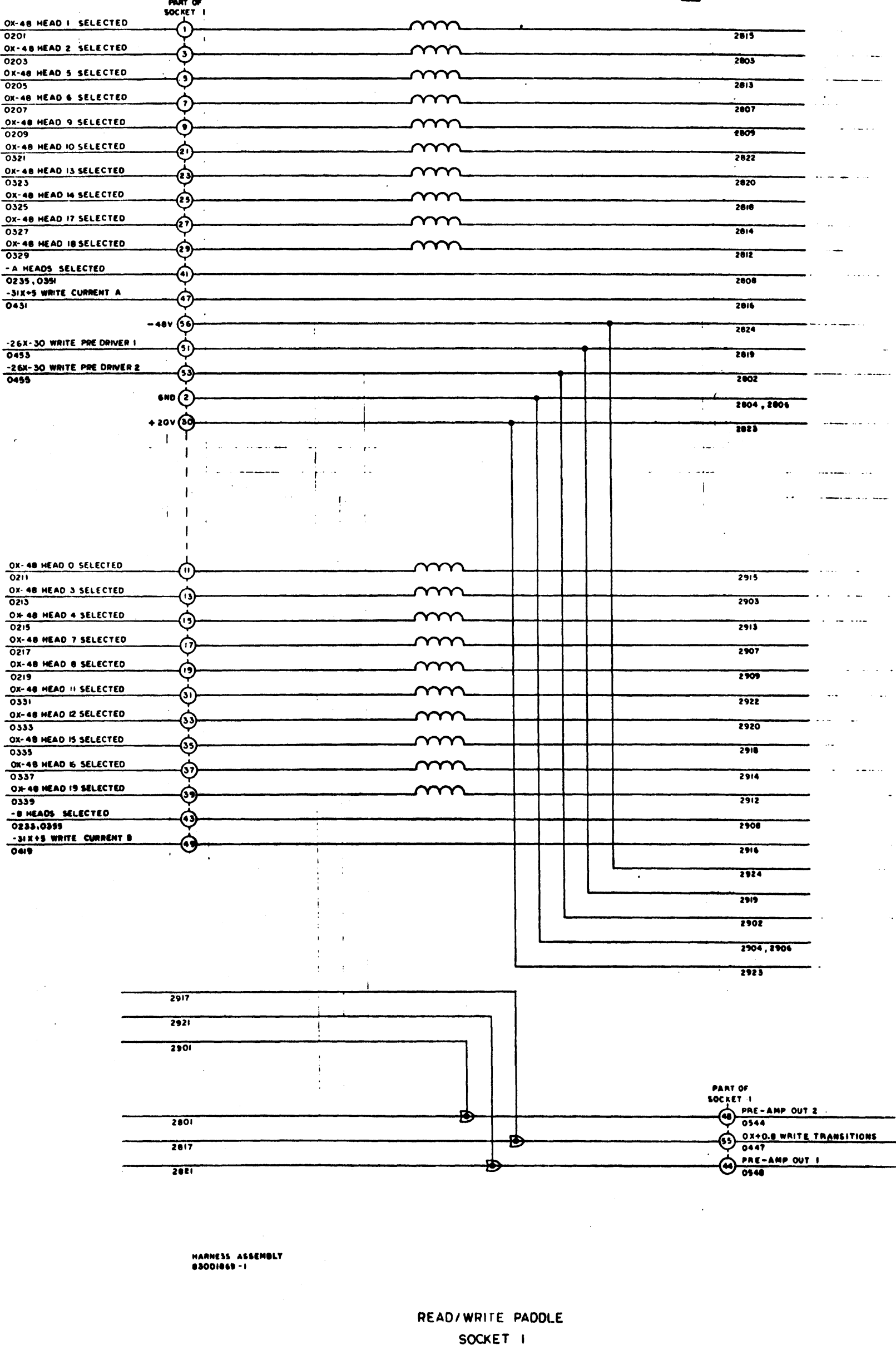
REDUCED SIZE
 PRINT

INTERCONNECTION
 DIAGRAM -
 READ/WRITE PADDLE

REV	A	DATE	
ENGR		DATE	
CHKD		DATE	
APPR		DATE	

TOLERANCES UNLESS OTHERWISE SPECIFIED
 .005" MIN. UNLESS OTHERWISE SPECIFIED
 .010" MIN. UNLESS OTHERWISE SPECIFIED
 .015" MIN. UNLESS OTHERWISE SPECIFIED
 .020" MIN. UNLESS OTHERWISE SPECIFIED
 .030" MIN. UNLESS OTHERWISE SPECIFIED
 .040" MIN. UNLESS OTHERWISE SPECIFIED
 .050" MIN. UNLESS OTHERWISE SPECIFIED
 .060" MIN. UNLESS OTHERWISE SPECIFIED
 .070" MIN. UNLESS OTHERWISE SPECIFIED
 .080" MIN. UNLESS OTHERWISE SPECIFIED
 .090" MIN. UNLESS OTHERWISE SPECIFIED
 .100" MIN. UNLESS OTHERWISE SPECIFIED

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HARNES ASSEMBLY
 83001869 -1

READ/WRITE PADDLE
 SOCKET 1

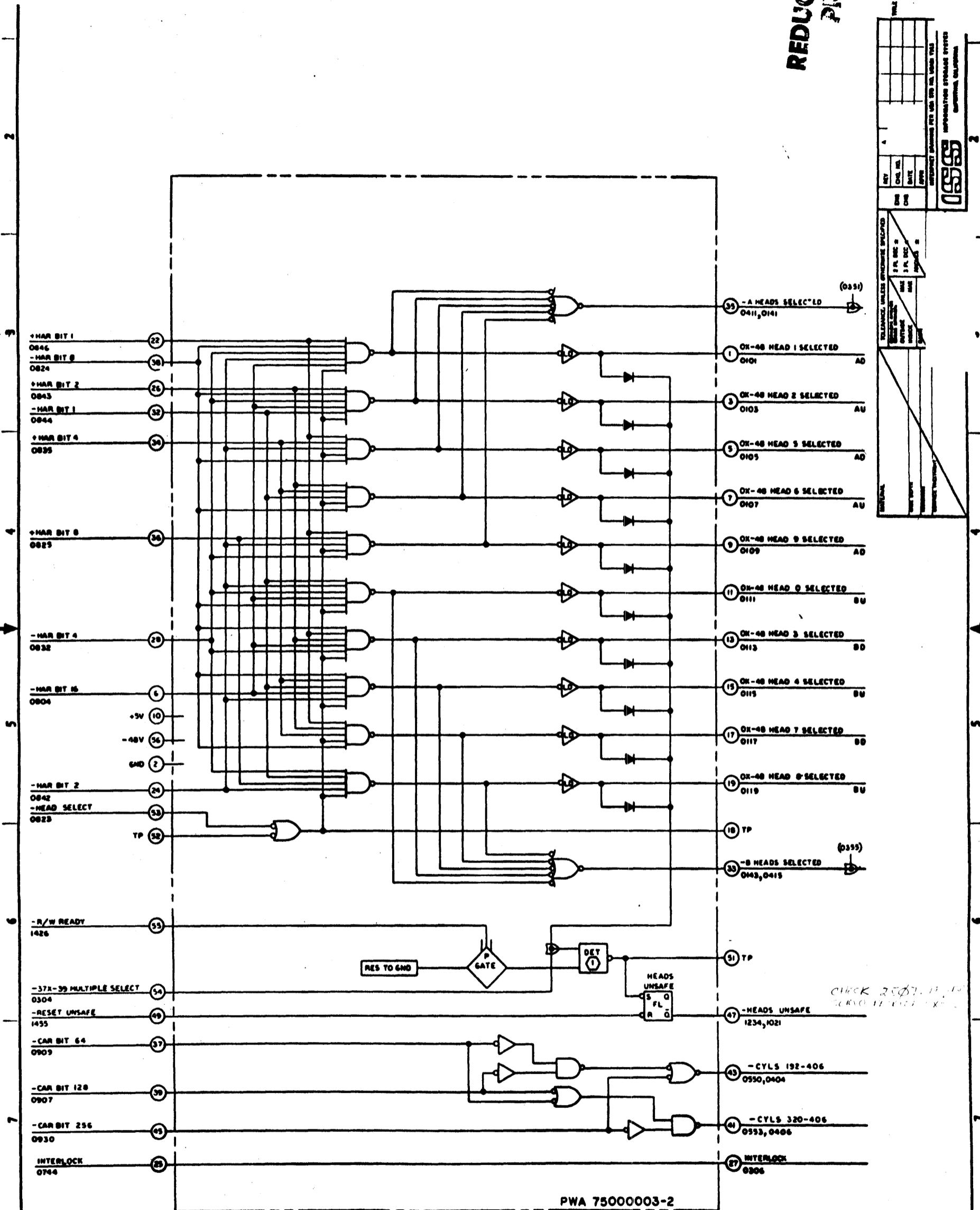
3

SKT 2
 RELAYED FOR INFO.
 DATE:

**REDUCED SIZE
PRINT**

LOGIC DIAGRAM -
 SELECT 0-9

TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT	TEST POINT
1	2	3	4	5	6	7	8	9	10
11	12	13	14	15	16	17	18	19	20
21	22	23	24	25	26	27	28	29	30
31	32	33	34	35	36	37	38	39	40



① OUTPUT IS LOW IF 2 OR MORE HEADS
 SELECTED OR ANY HEAD SELECTED
 AND NO R/W READY

SELECT 0-9
 SOCKET 2

CHECK 2507, 11/18
 CURVO 11/18/11

REDUCED SIZE
PRINT

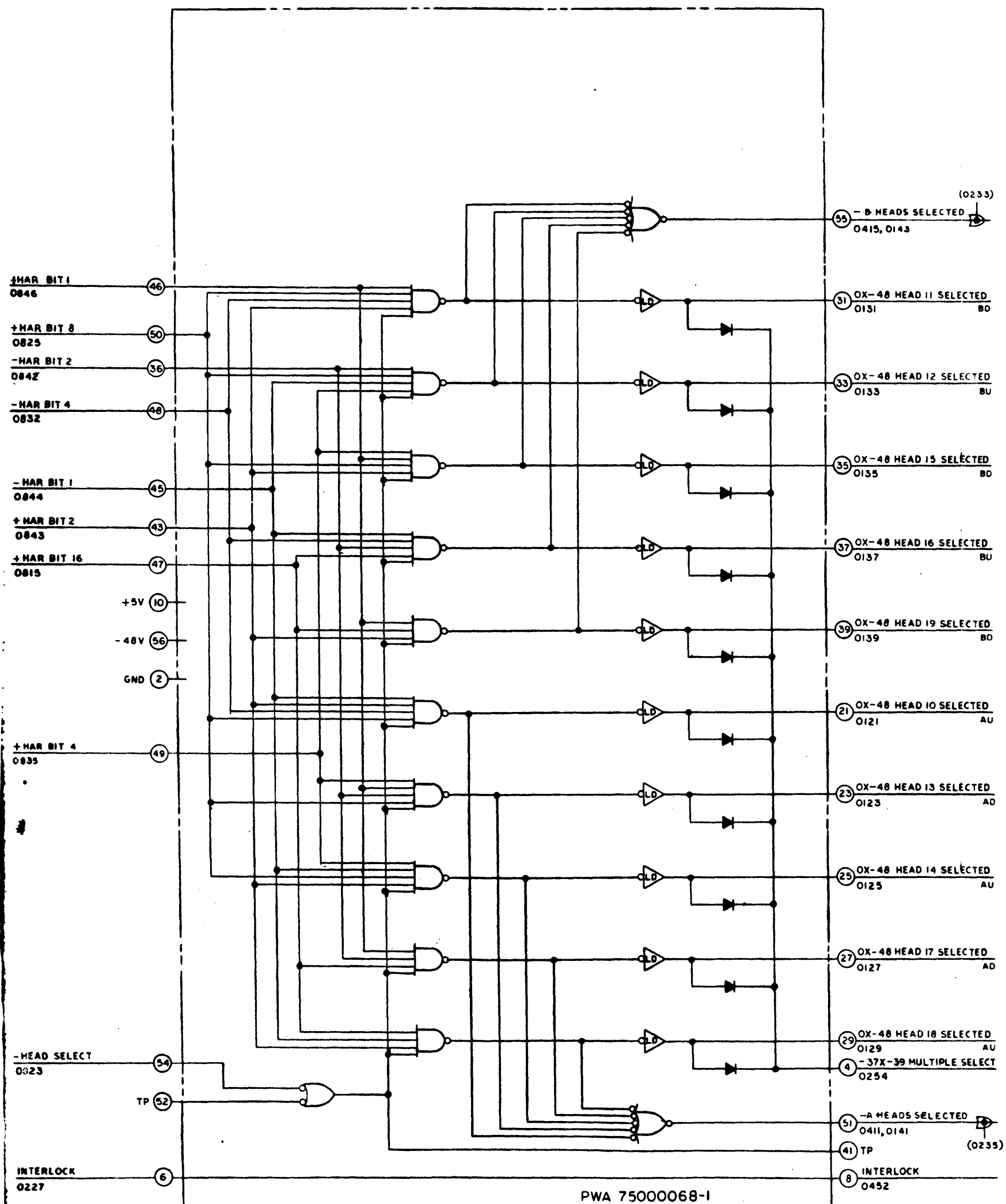
LOGIC DIAGRAM—
SELECT 10-19

5

REV	A
CHG	ONE
DATE	
BY	
TOLERANCE UNLESS OTHERWISE SPECIFIED	
1 PL. USE	2
3 PL. USE	3
4 PL. USE	4
5 PL. USE	5
6 PL. USE	6
7 PL. USE	7
8 PL. USE	8
9 PL. USE	9
10 PL. USE	10
11 PL. USE	11
12 PL. USE	12
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99 PL. USE	99
100 PL. USE	100

ISS

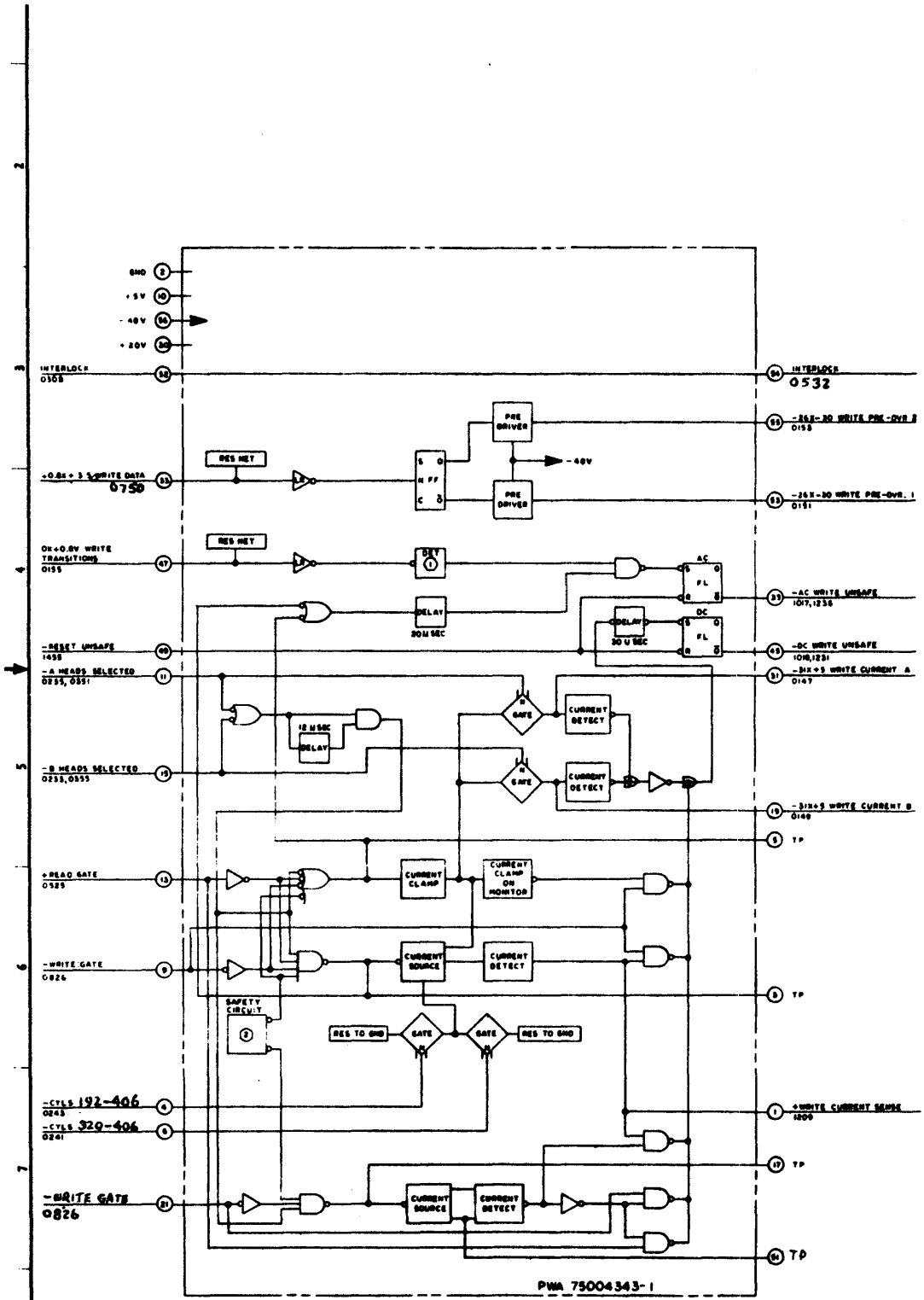
OPERATING STORAGE SYSTEMS
CORPORATION, CALIFORNIA



SELECT 10-19
SOCKET 3

3
4
5
6
7
8

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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SOCKET 4 WRITE

- ① SETS UNSAFE IF WRITE TRANSITION BIT-TO-BIT TIME IS > 0.84 SEC.
- ② DISABLES WRITE CIRCUIT DURING OUTPUT LOAD IF 0.8V IS LOST.

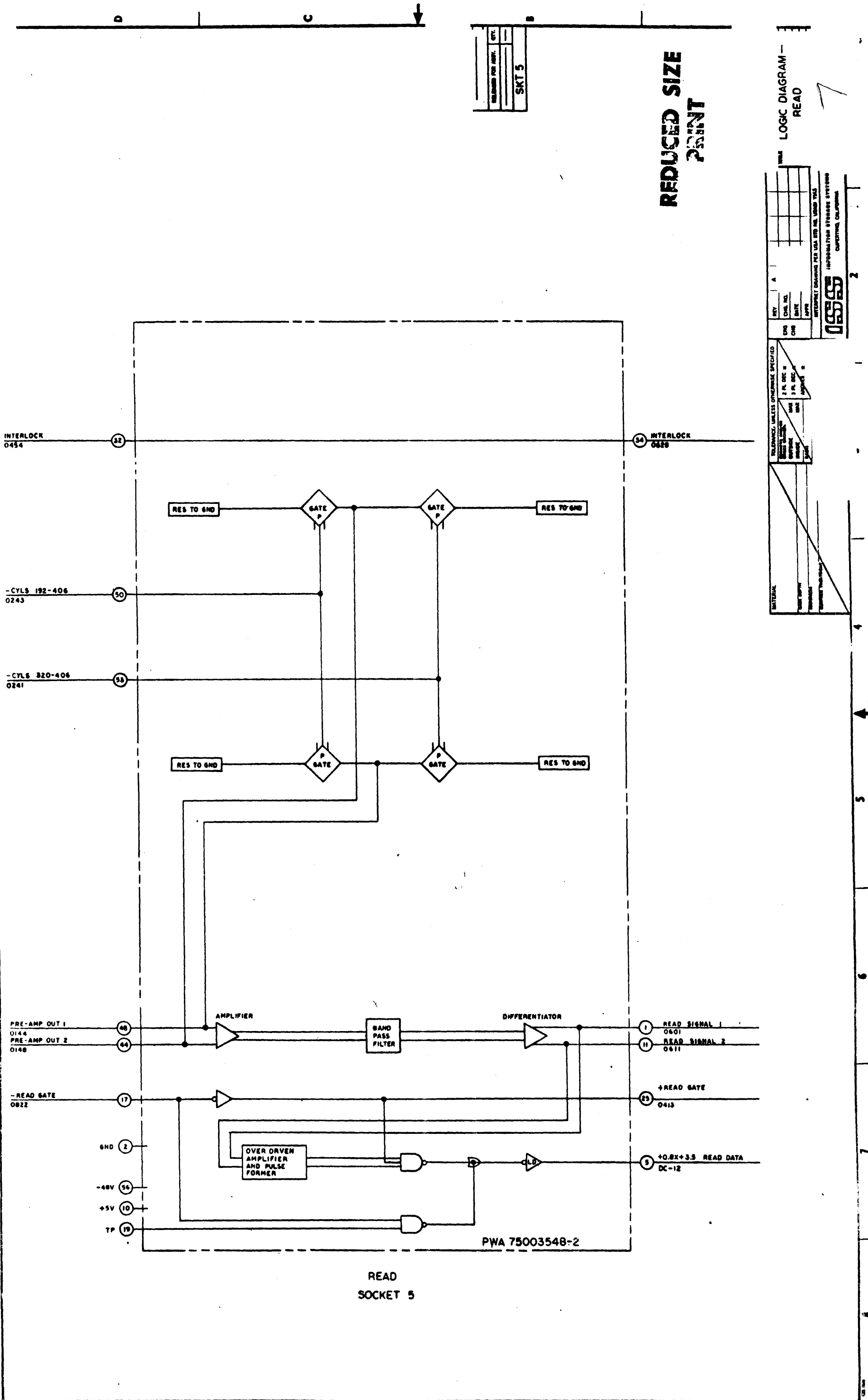
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REV.	
DATE	
BY	
CHKD BY	
APPROVED BY	
SKT 5	

**REDUCED SIZE
PRINT**

REV. A	
CON. NO.	
DATE	
CHKD	
BY	
TOLERANCES UNLESS OTHERWISE SPECIFIED	
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UNLESS OTHERWISE SPECIFIED	
1 P. DEC.	
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3 P. DEC.	
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UNLESS OTHERWISE SPECIFIED	
1 P. DEC.	
2 P. DEC.	
3 P. DEC.	
4 P. DEC.	
5 P. DEC.	
UNLESS OTHERWISE SPECIFIED	
1 P. DEC.	
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3 P. DEC.	
4 P. DEC.	
5 P. DEC.	

LOGIC DIAGRAM -
READ



READ
SOCKET 5

3

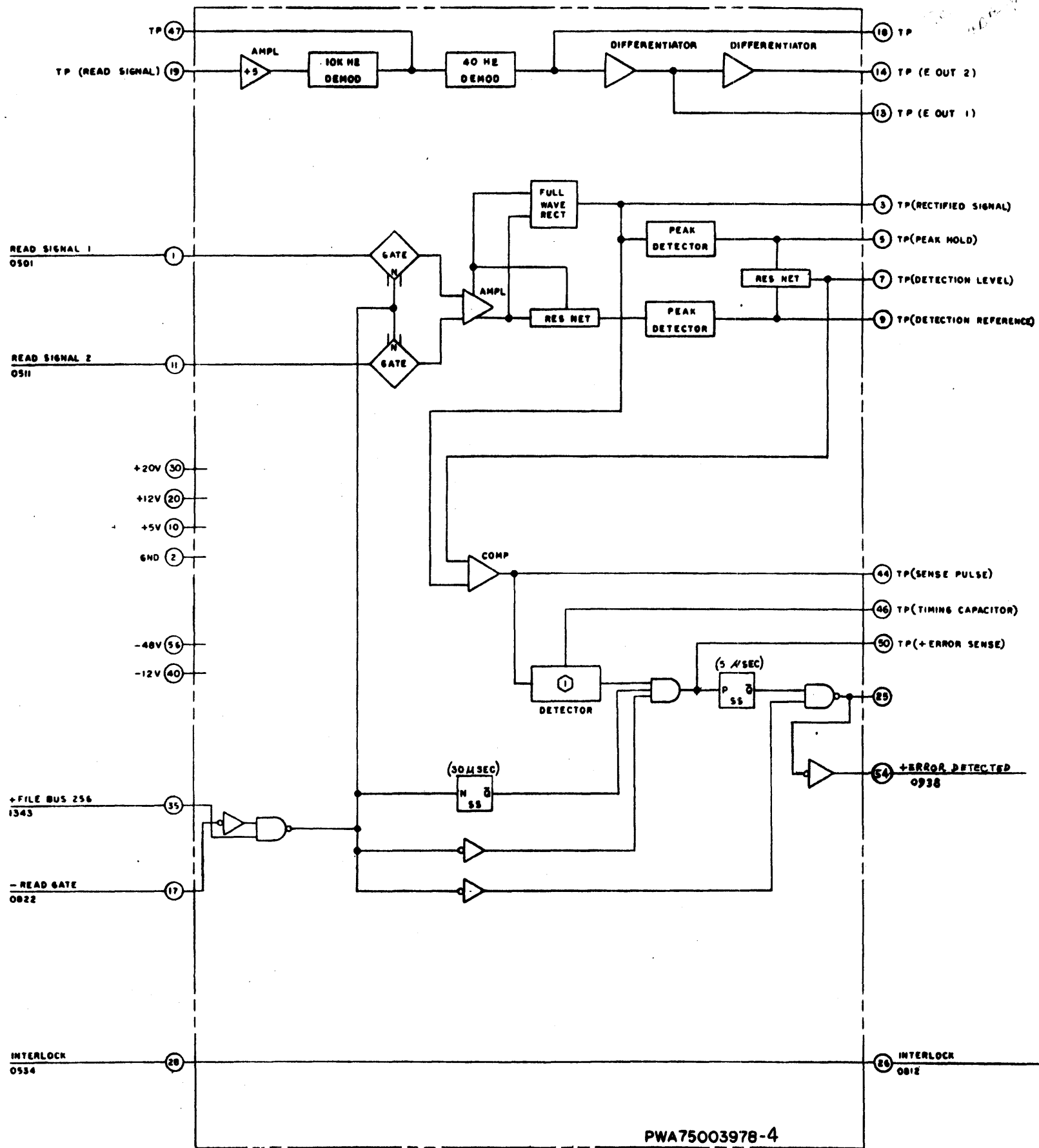
SKT 6

REDUCED SIZE
PRINT

LOGIC DIAGRAM -
DEFECT DETECTOR

DATE: _____
DRAWN BY: _____
CHECKED BY: _____

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① DETECTOR PRODUCES +ERROR SENSE IF SPACING BETWEEN ANY TWO SENSE PULSES EXCEEDS 500 N SEC

DEFECT DETECTOR
SOCKET 6

PWA75003978-4

8

2

5

6

7

8

DEVELOPMENT NO.
 RELEASED PER AUTH. BY

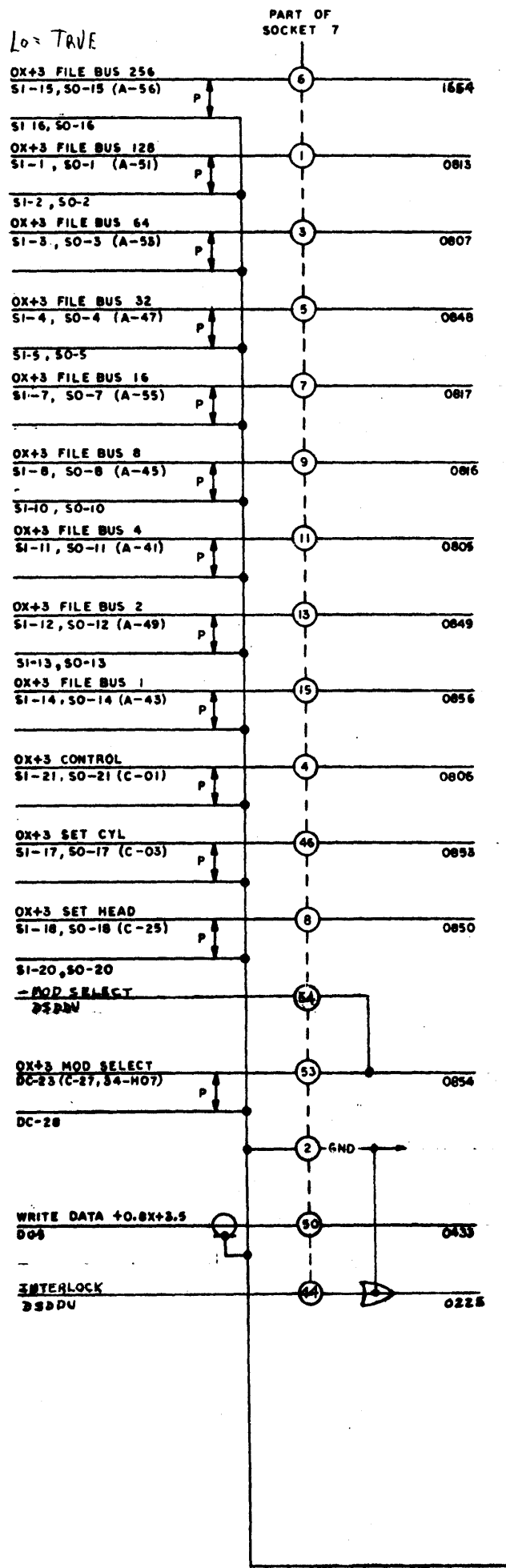
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INTERCONNECTION
 DIAGRAM - SIGNAL PADDLE

REV A

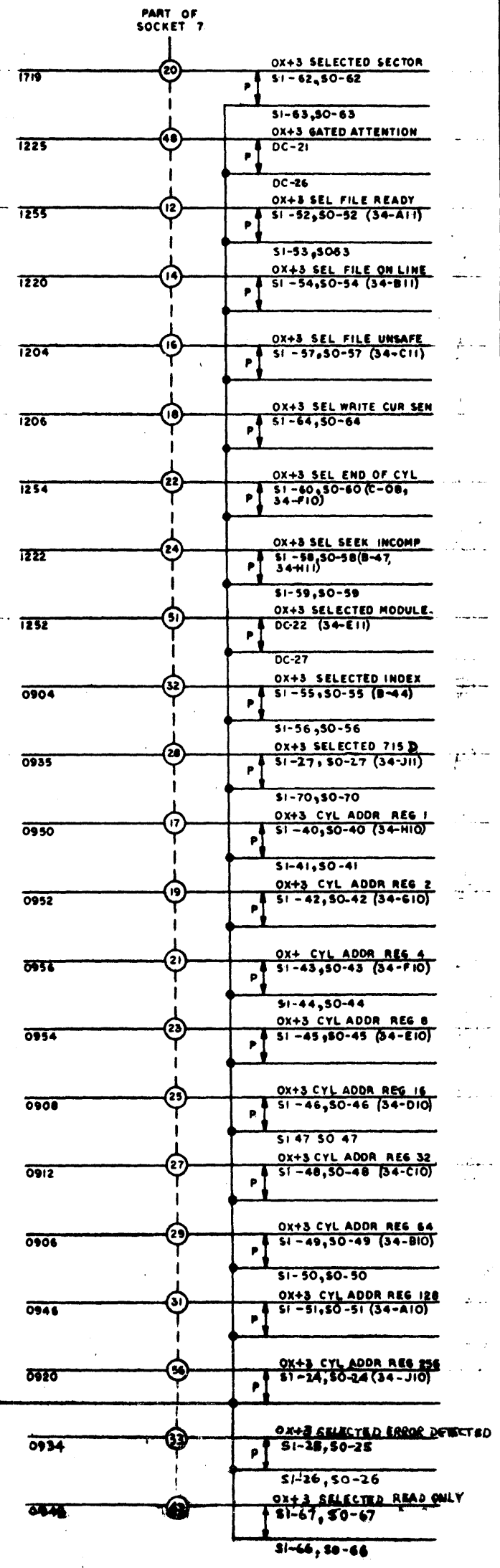
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ISS INFORMATION STORAGE SYSTEMS
 CUPERTINO, CALIFORNIA



PART OF HARNESS ASSEMBLY 83004888-1

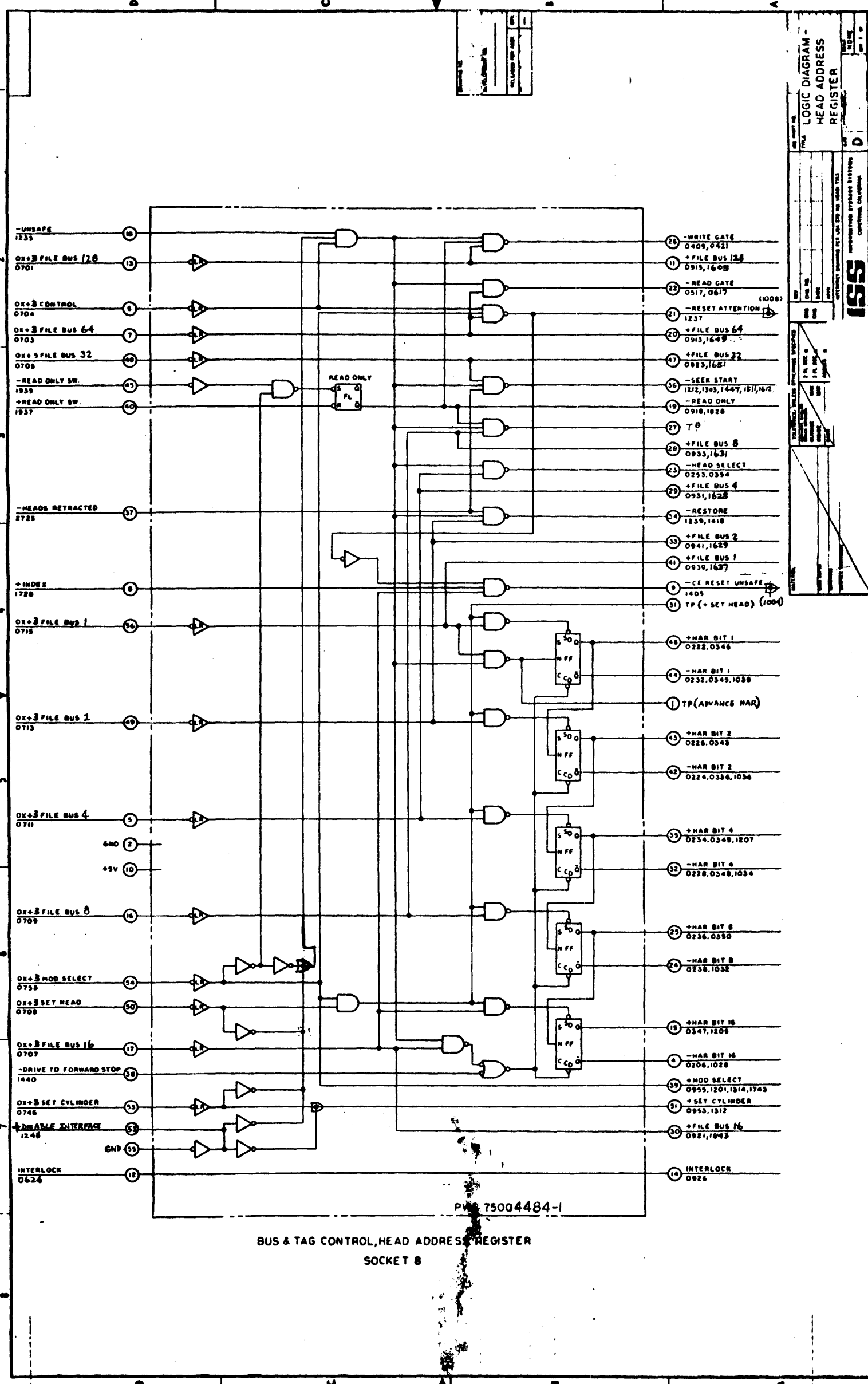
SIGNAL PADDLE
 SOCKET 7



TOLERANCES, UNLESS OTHERWISE SPECIFIED

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 1 P. DEC 54

AMPLIFIER 2



LOGIC DIAGRAM -
HEAD ADDRESS REGISTER

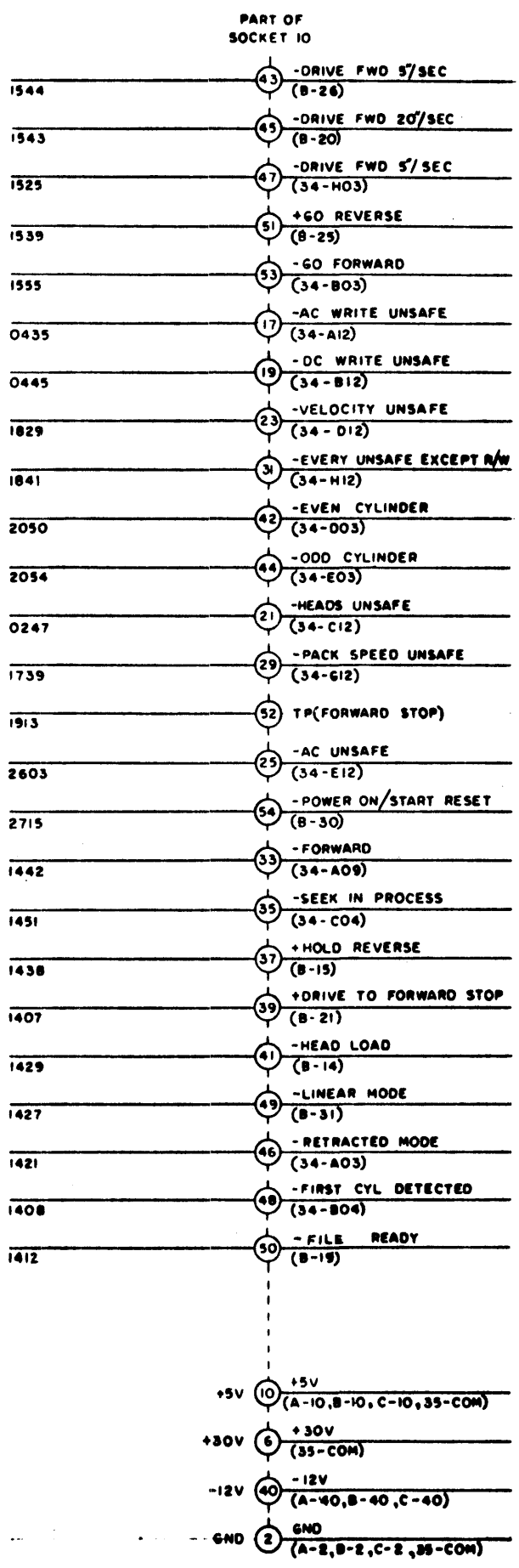
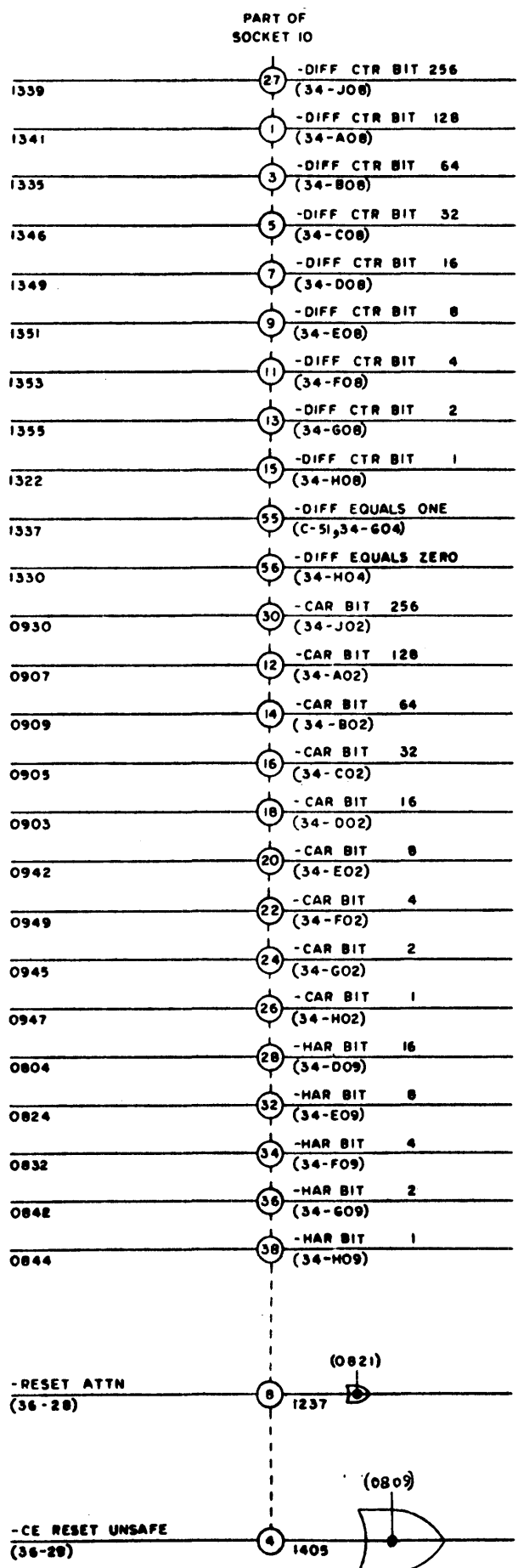
REV. 11-67

ISS INFORMATION SYSTEMS CORPORATION, CALIFORNIA

1

PWA 75004484-1
BUS & TAG CONTROL, HEAD ADDRESS REGISTER
SOCKET 8

12



DSDDU MONITOR
SOCKET 10

ISS PART

REV	
CHK NO.	
CHK DATE	
APPV	

INTERCONNECT DIAGRAM PER ISS STD NO. USA41 715 D

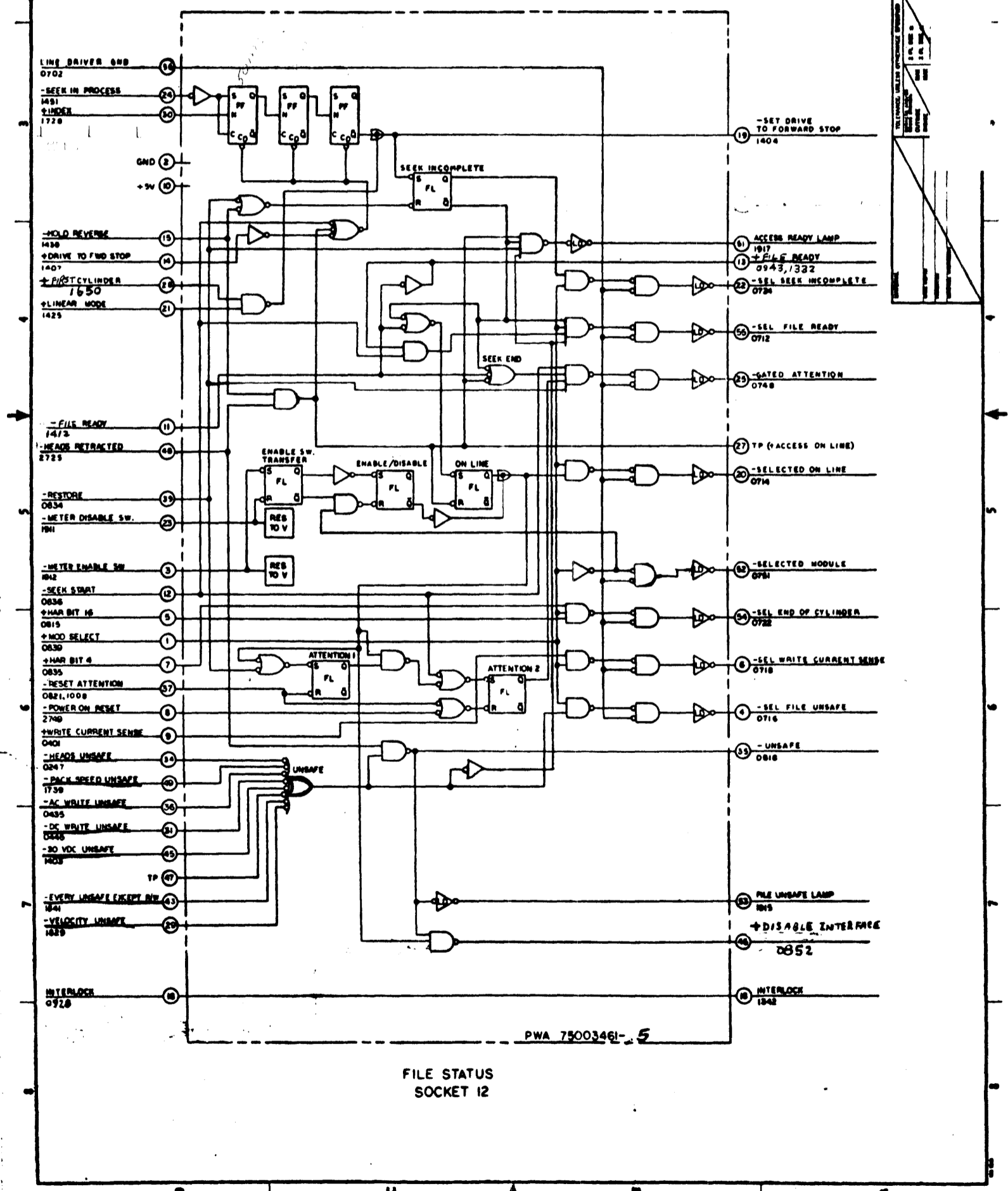
ISS INFORMATION STORAGE SYSTEMS
CORPORATION, CALIFORNIA

17

75003461

LOGIC DIAGRAM -
FILE STATUS

REV	DATE	BY	CHKD



PWA 75003461-5

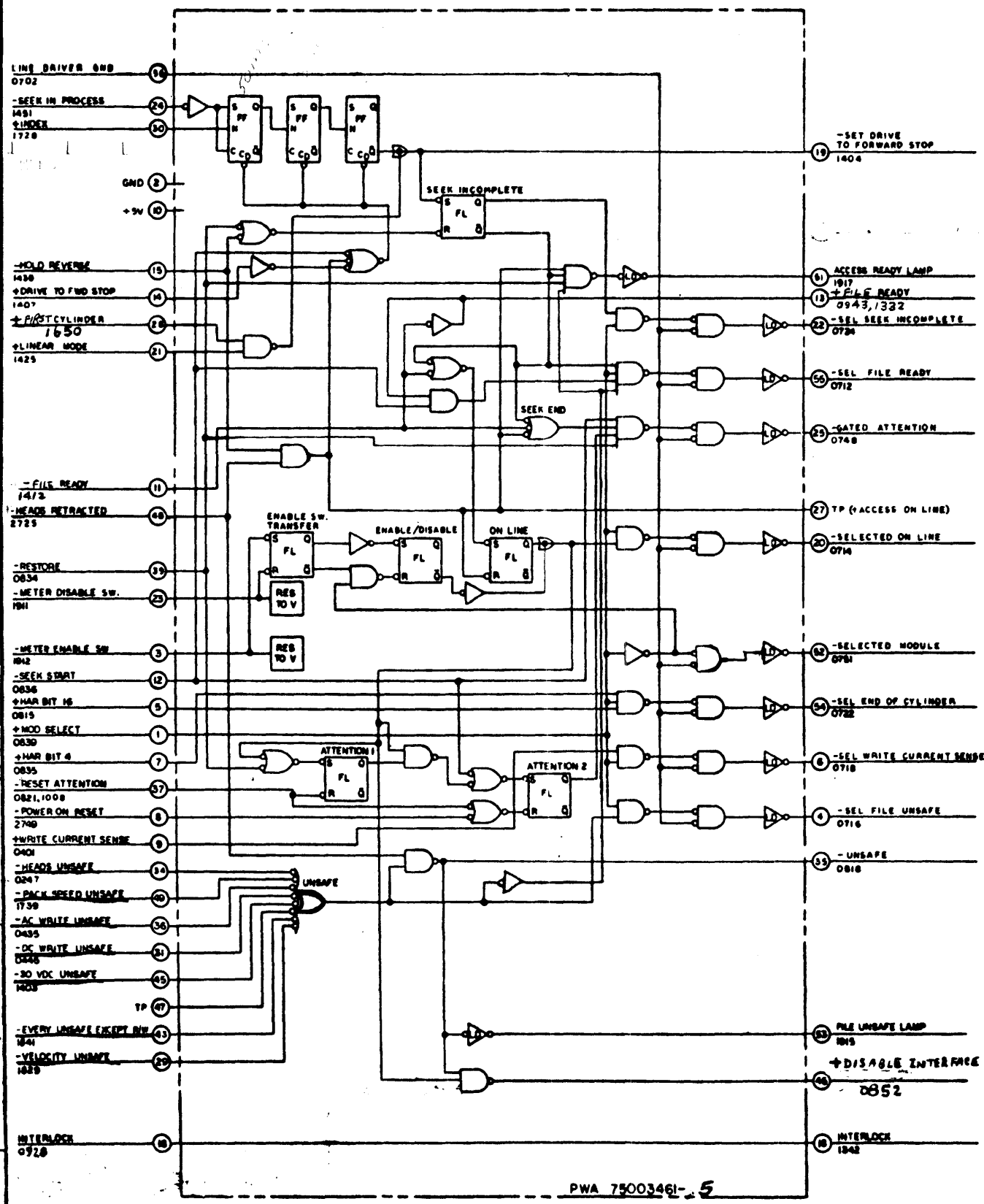
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SOCKET 12

75003461

LOGIC DIAGRAM -
FILE STATUS

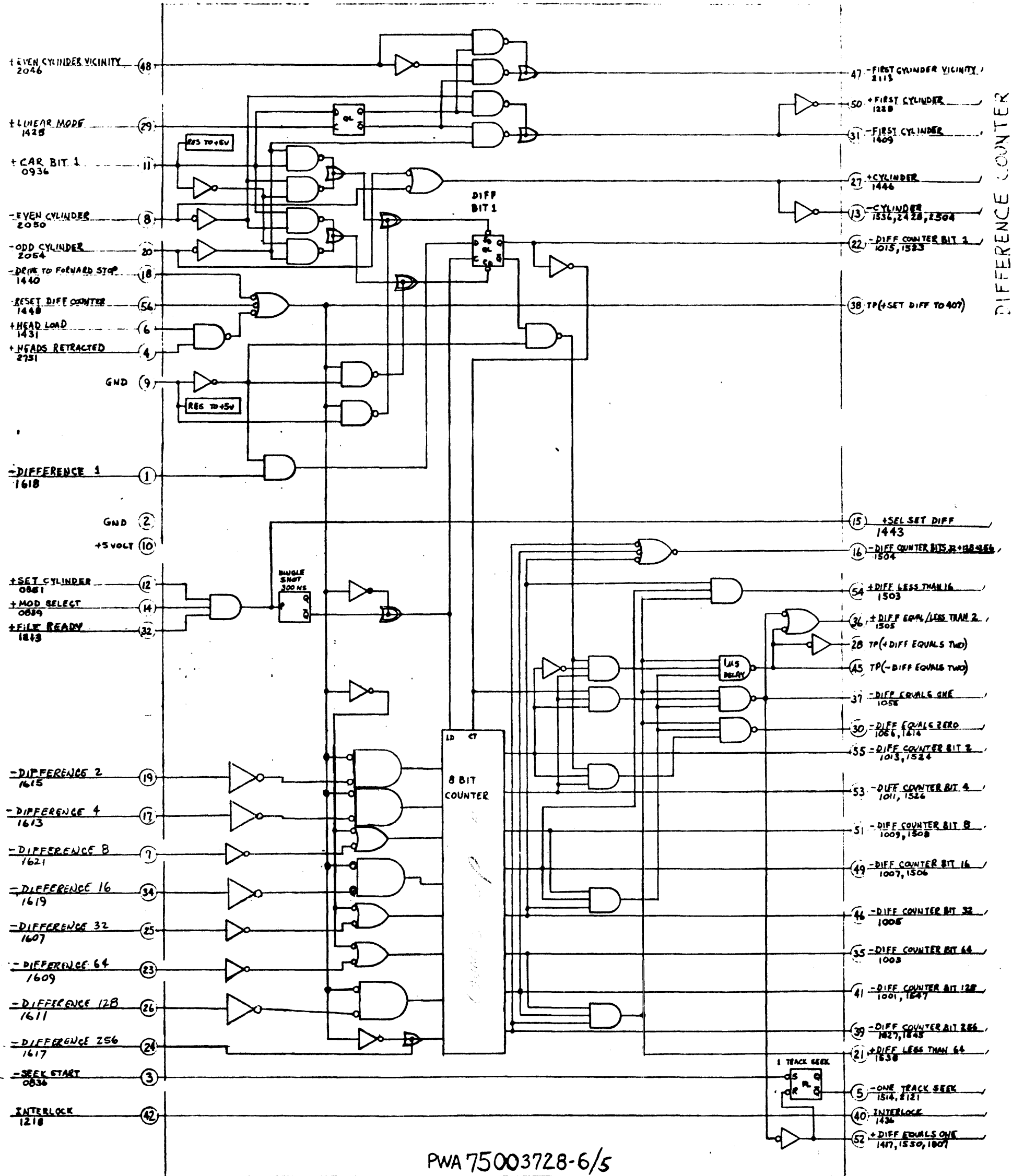
REV	DATE	BY

ISS



FILE STATUS
SOCKET 12

PWA 75003461-5

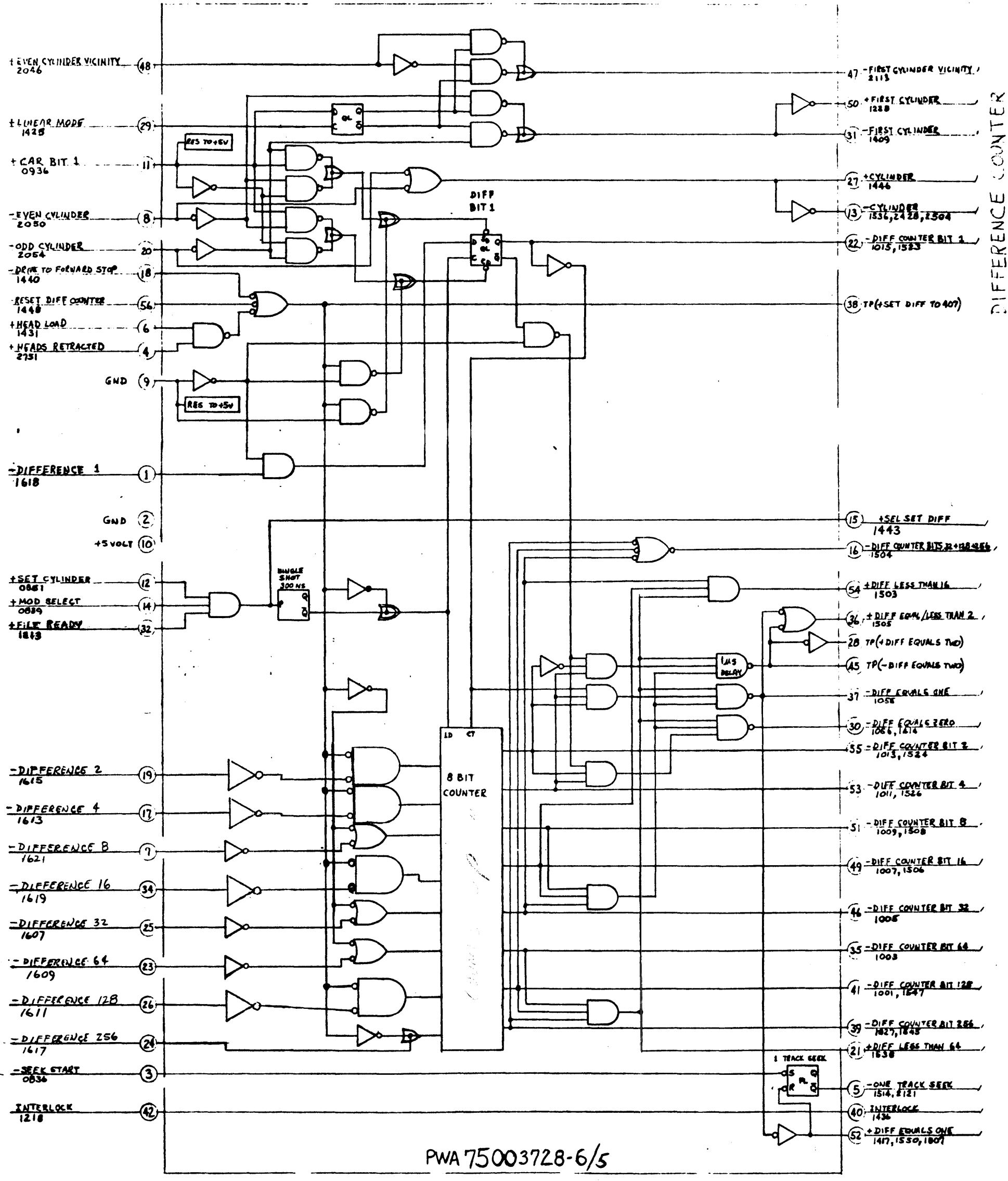


PWA 75003728-6/5

DIFFERENCE COUNTER
SOCKET T 13

DIFFERENCE COUNTER

14



PWA 75003728-6/5

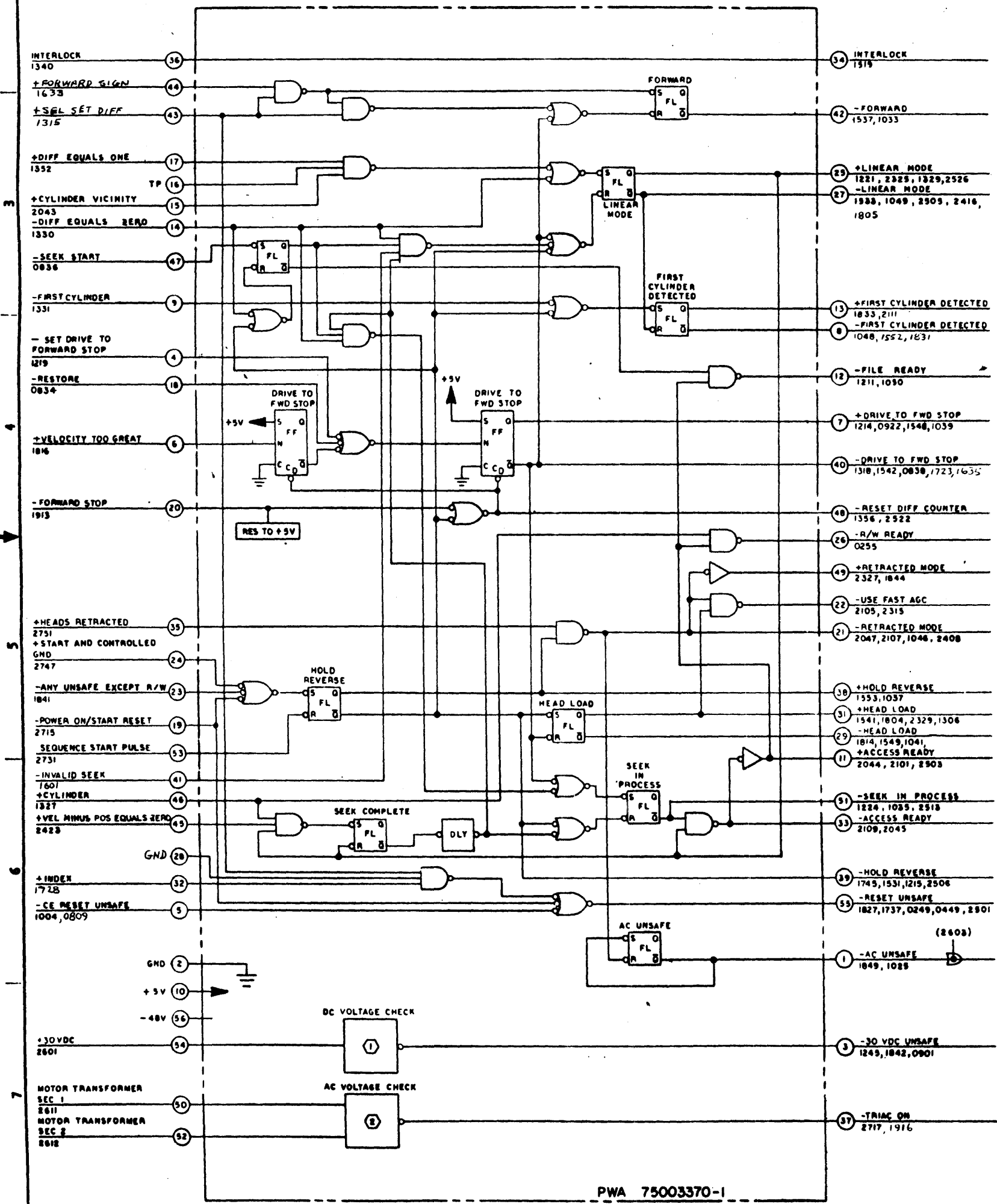
DIFFERENCE COUNTER
SOCKET 13

DIFFERENCE COUNTER

REVISION NO.	
RELEASED FOR USE	
DATE	
BY	
SKT14	

LOGIC DIAGRAM-
ACCESS CONTROL

REV					
CHK NO.					
CHK DATE					
DATE					
APP'D					
BY					
TOLERANCE UNLESS OTHERWISE SPECIFIED					
2 P. DEC.					
3 P. DEC.					
MAX.					
MIN.					
OUTSIDE					
INSIDE					
DATE					
BY					
ATTACHED DRAWING PER USA STD NO. USAB P43					
INFORMATION SYSTEMS DIVISION					
CUPERTINO, CALIFORNIA					



① OUTPUT LOW IF INPUT BELOW 5 VOLTS.
② OUTPUT LOW IF AC INPUT PRESENT.

ACCESS CONTROL
SOCKET I4

PWA 75003370-1

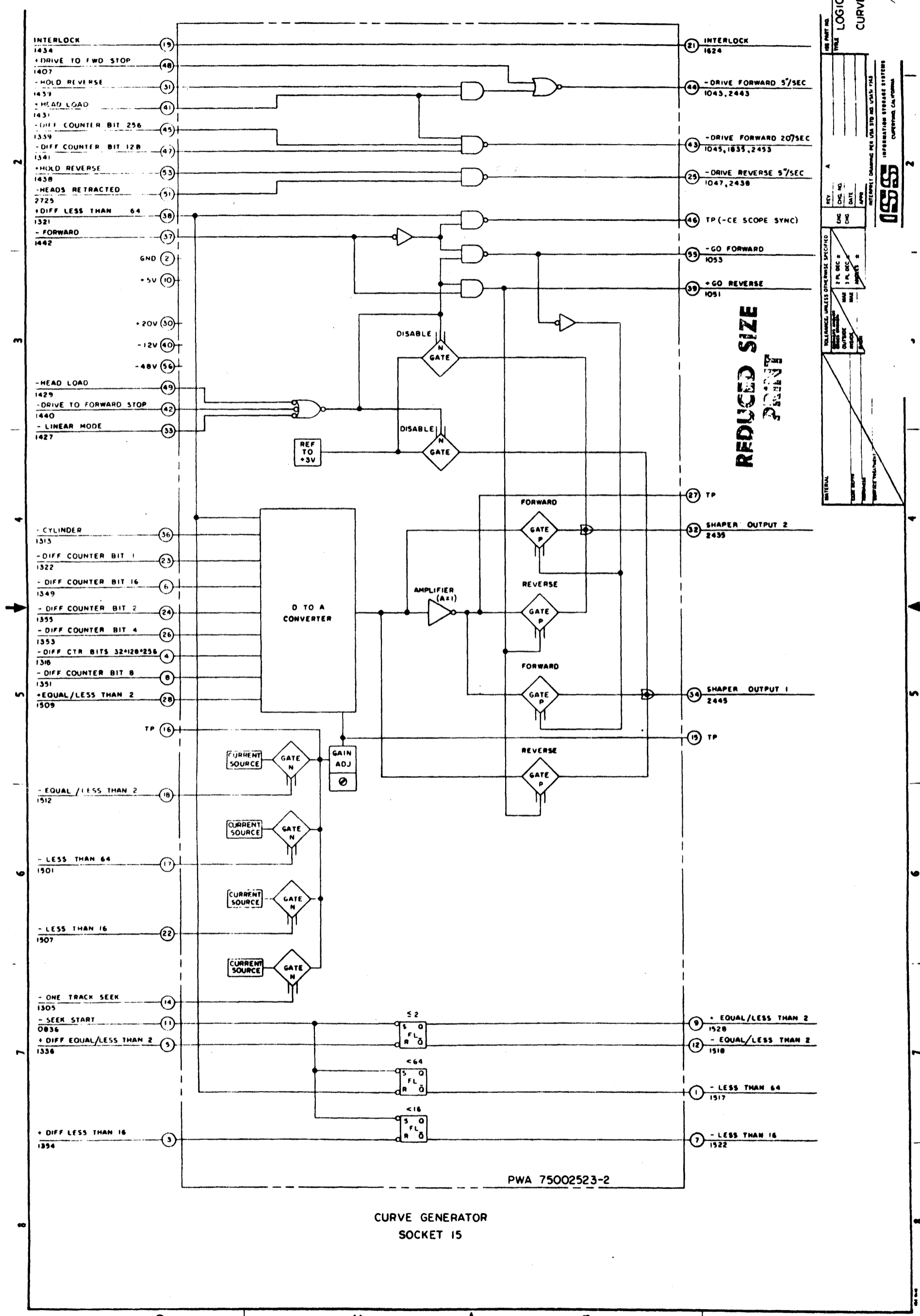
15

07
 RELEASED PER AUTHORITY
 SKT 15

LOGIC DIAGRAM -
 CURVE GENERATOR
 16

KEY	DATE	BY
1 P. DEC 2	1 P. DEC 2	1 P. DEC 2
2 P. DEC 2	2 P. DEC 2	2 P. DEC 2
3 P. DEC 2	3 P. DEC 2	3 P. DEC 2
4 P. DEC 2	4 P. DEC 2	4 P. DEC 2
5 P. DEC 2	5 P. DEC 2	5 P. DEC 2
6 P. DEC 2	6 P. DEC 2	6 P. DEC 2
7 P. DEC 2	7 P. DEC 2	7 P. DEC 2
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9 P. DEC 2	9 P. DEC 2	9 P. DEC 2
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14 P. DEC 2	14 P. DEC 2	14 P. DEC 2
15 P. DEC 2	15 P. DEC 2	15 P. DEC 2
16 P. DEC 2	16 P. DEC 2	16 P. DEC 2
17 P. DEC 2	17 P. DEC 2	17 P. DEC 2
18 P. DEC 2	18 P. DEC 2	18 P. DEC 2
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22 P. DEC 2	22 P. DEC 2	22 P. DEC 2
23 P. DEC 2	23 P. DEC 2	23 P. DEC 2
24 P. DEC 2	24 P. DEC 2	24 P. DEC 2
25 P. DEC 2	25 P. DEC 2	25 P. DEC 2
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27 P. DEC 2	27 P. DEC 2	27 P. DEC 2
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60 P. DEC 2	60 P. DEC 2	60 P. DEC 2
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75 P. DEC 2	75 P. DEC 2	75 P. DEC 2
76 P. DEC 2	76 P. DEC 2	76 P. DEC 2
77 P. DEC 2	77 P. DEC 2	77 P. DEC 2
78 P. DEC 2	78 P. DEC 2	78 P. DEC 2
79 P. DEC 2	79 P. DEC 2	79 P. DEC 2
80 P. DEC 2	80 P. DEC 2	80 P. DEC 2

REDUCED SIZE
 PRINT



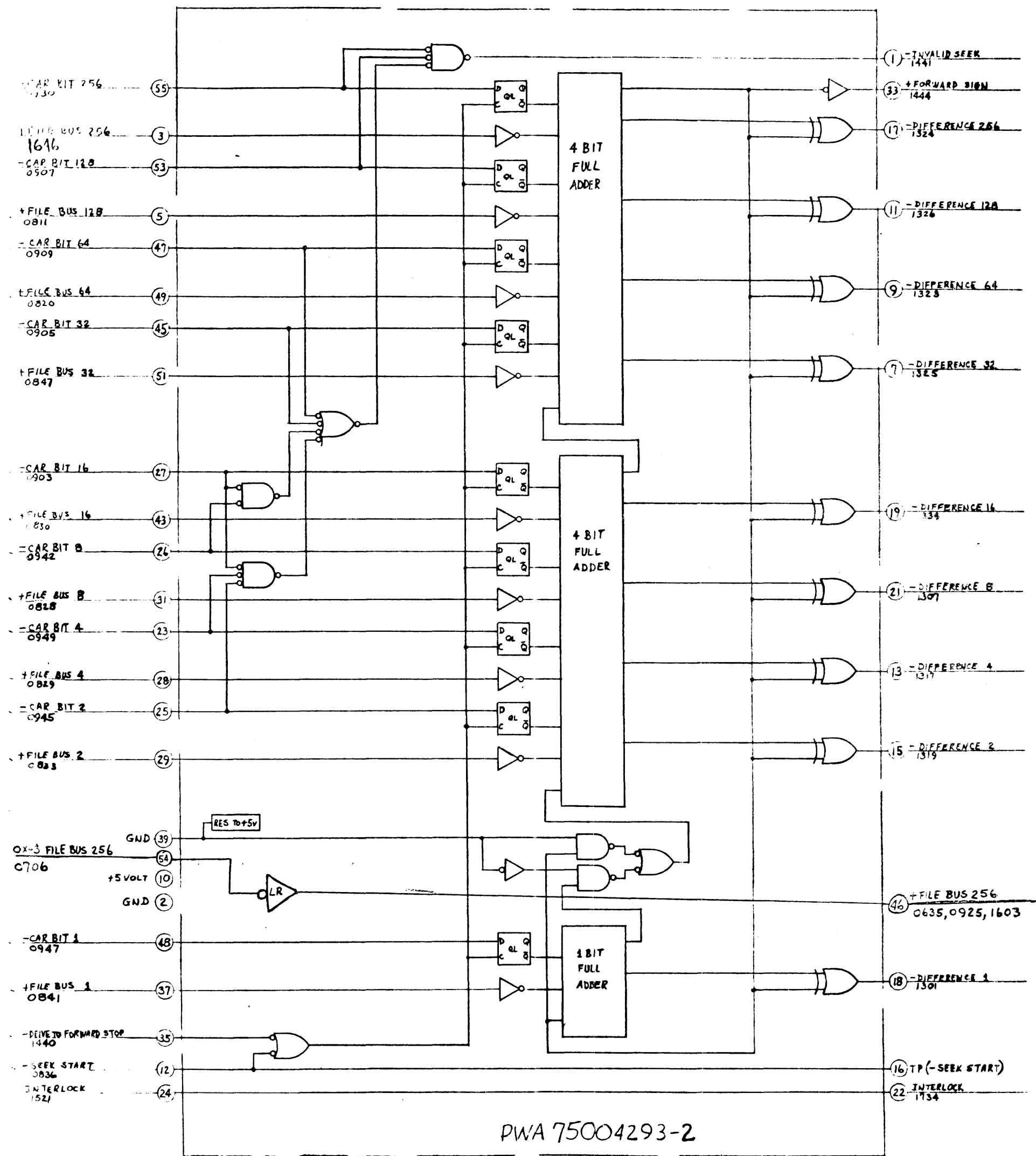
CURVE GENERATOR
 SOCKET 15

PWA 75002523-2

INFORMATION STORAGE SYSTEMS
 CUPERTINO, CALIFORNIA



IBM PART NO. 16
 TITLE LOGIC DIAGRAM - CURVE GENERATOR
 KEY: 1 P. DEC 2, 2 P. DEC 2, 3 P. DEC 2, 4 P. DEC 2, 5 P. DEC 2, 6 P. DEC 2, 7 P. DEC 2, 8 P. DEC 2, 9 P. DEC 2, 10 P. DEC 2, 11 P. DEC 2, 12 P. DEC 2, 13 P. DEC 2, 14 P. DEC 2, 15 P. DEC 2, 16 P. DEC 2, 17 P. DEC 2, 18 P. DEC 2, 19 P. DEC 2, 20 P. DEC 2, 21 P. DEC 2, 22 P. DEC 2, 23 P. DEC 2, 24 P. DEC 2, 25 P. DEC 2, 26 P. DEC 2, 27 P. DEC 2, 28 P. DEC 2, 29 P. DEC 2, 30 P. DEC 2, 31 P. DEC 2, 32 P. DEC 2, 33 P. DEC 2, 34 P. DEC 2, 35 P. DEC 2, 36 P. DEC 2, 37 P. DEC 2, 38 P. DEC 2, 39 P. DEC 2, 40 P. DEC 2, 41 P. DEC 2, 42 P. DEC 2, 43 P. DEC 2, 44 P. DEC 2, 45 P. DEC 2, 46 P. DEC 2, 47 P. DEC 2, 48 P. DEC 2, 49 P. DEC 2, 50 P. DEC 2, 51 P. DEC 2, 52 P. DEC 2, 53 P. DEC 2, 54 P. DEC 2, 55 P. DEC 2, 56 P. DEC 2, 57 P. DEC 2, 58 P. DEC 2, 59 P. DEC 2, 60 P. DEC 2, 61 P. DEC 2, 62 P. DEC 2, 63 P. DEC 2, 64 P. DEC 2, 65 P. DEC 2, 66 P. DEC 2, 67 P. DEC 2, 68 P. DEC 2, 69 P. DEC 2, 70 P. DEC 2, 71 P. DEC 2, 72 P. DEC 2, 73 P. DEC 2, 74 P. DEC 2, 75 P. DEC 2, 76 P. DEC 2, 77 P. DEC 2, 78 P. DEC 2, 79 P. DEC 2, 80 P. DEC 2



DIFFERENCE CALCULATOR
 SOCKET 16

REVISIONS	DATE	BY

REV. SHEET NO.	REV. SHEET	REV. SHEET	REV. SHEET
1	1	1	1
1	1	1	1
1	1	1	1

ISS

LOGIC DIAGRAM
INDEX TRANSDUCER

DATE: 10/1/73

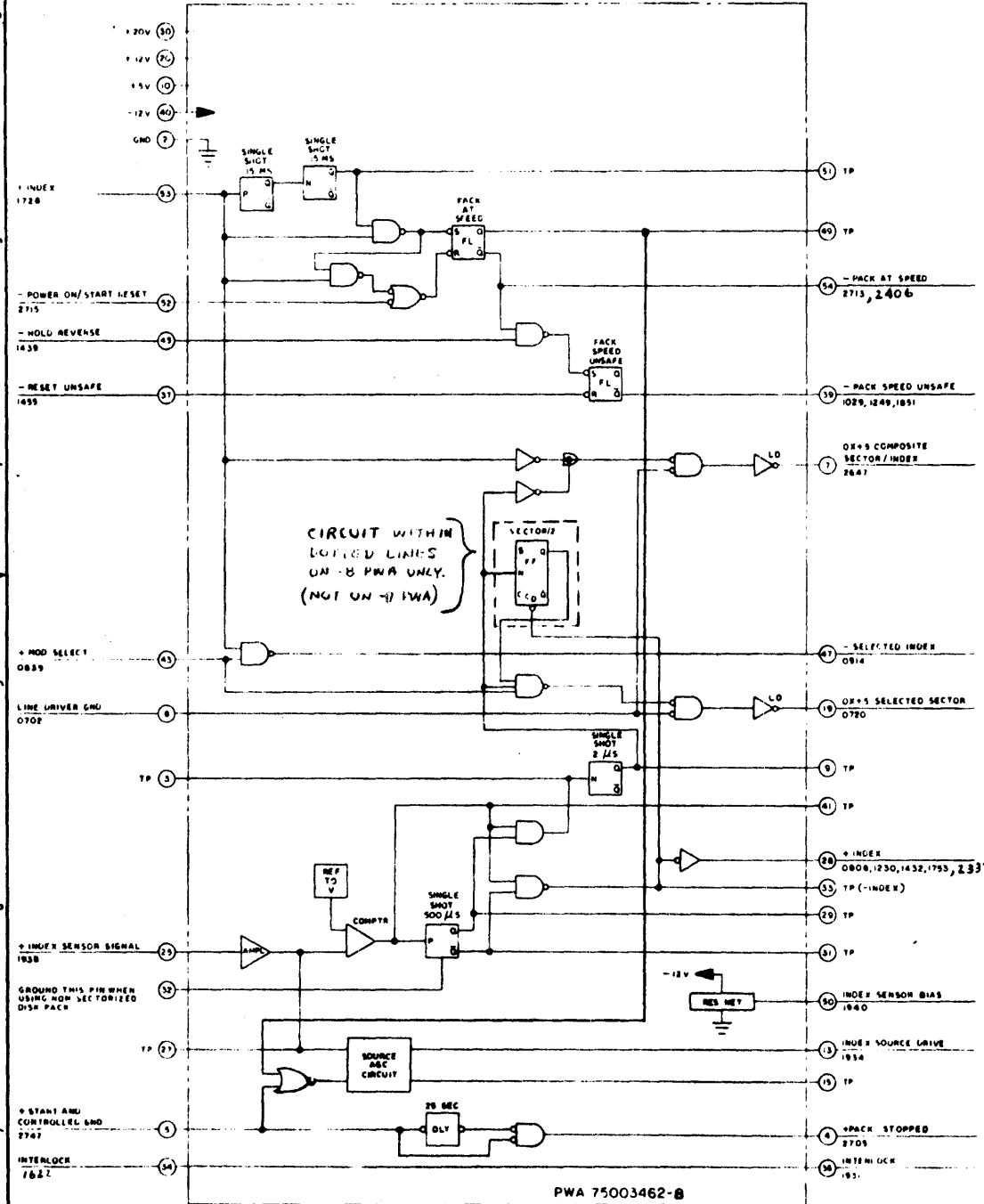
BY: [Signature]

FOR: [Signature]

APPROVED: [Signature]

REVISIONS:

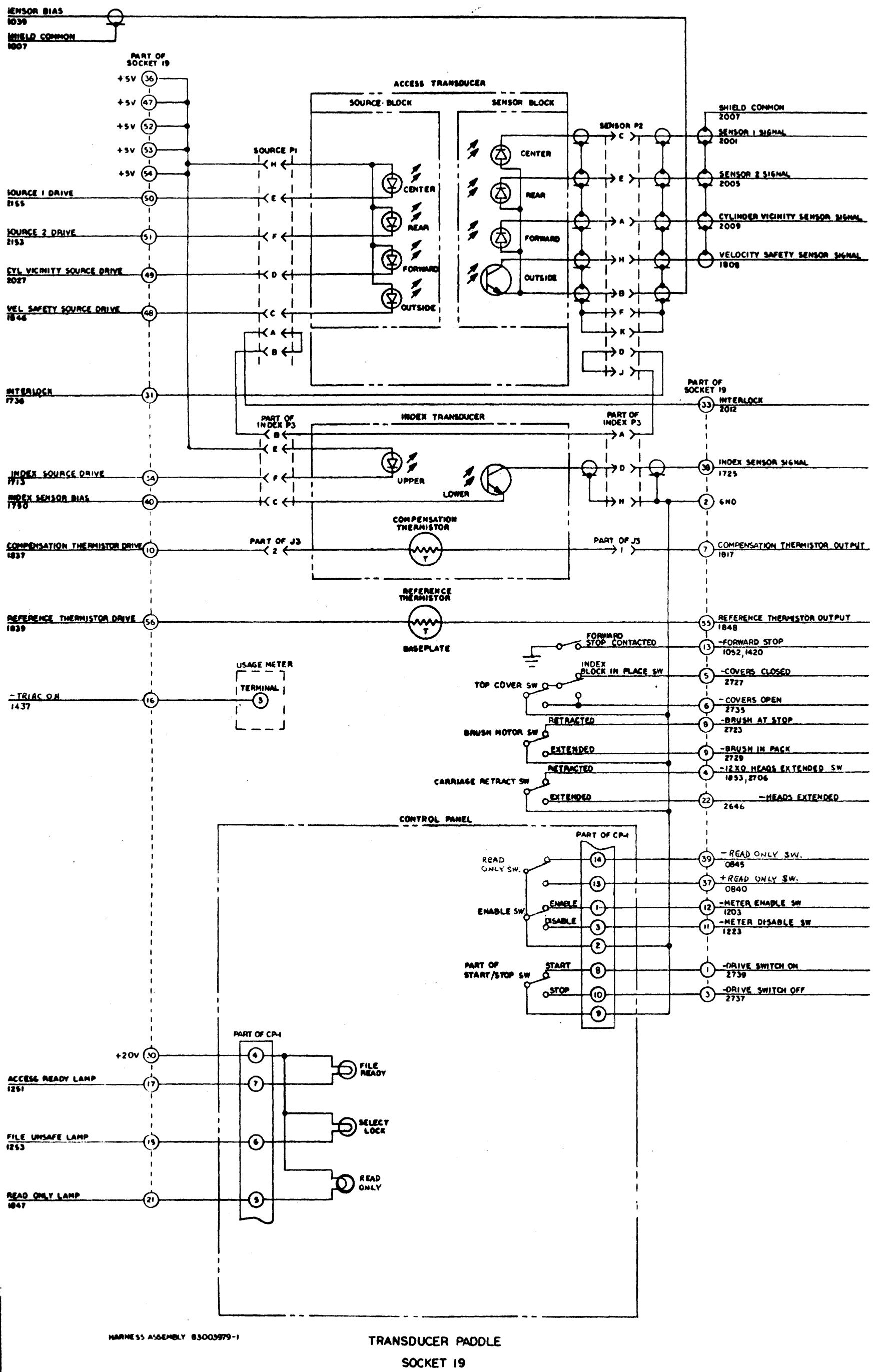
NO.	DESCRIPTION	DATE



SOCKET 17
INDEX TRANSDUCER

PWA 75003462-B

20



HARNESS ASSEMBLY 83003979-1

TRANSDUCER PADDLE
 SOCKET 19

TOLERANCE UNLESS OTHERWISE SPECIFIED

RESISTANCE	± 1%
CAPACITANCE	± 5%
INDUCTIVE	± 10%
WIRE GAUGE	± 0.001"
ANGLE	± 0.5°

2
 3
 4
 5
 6
 7
 8

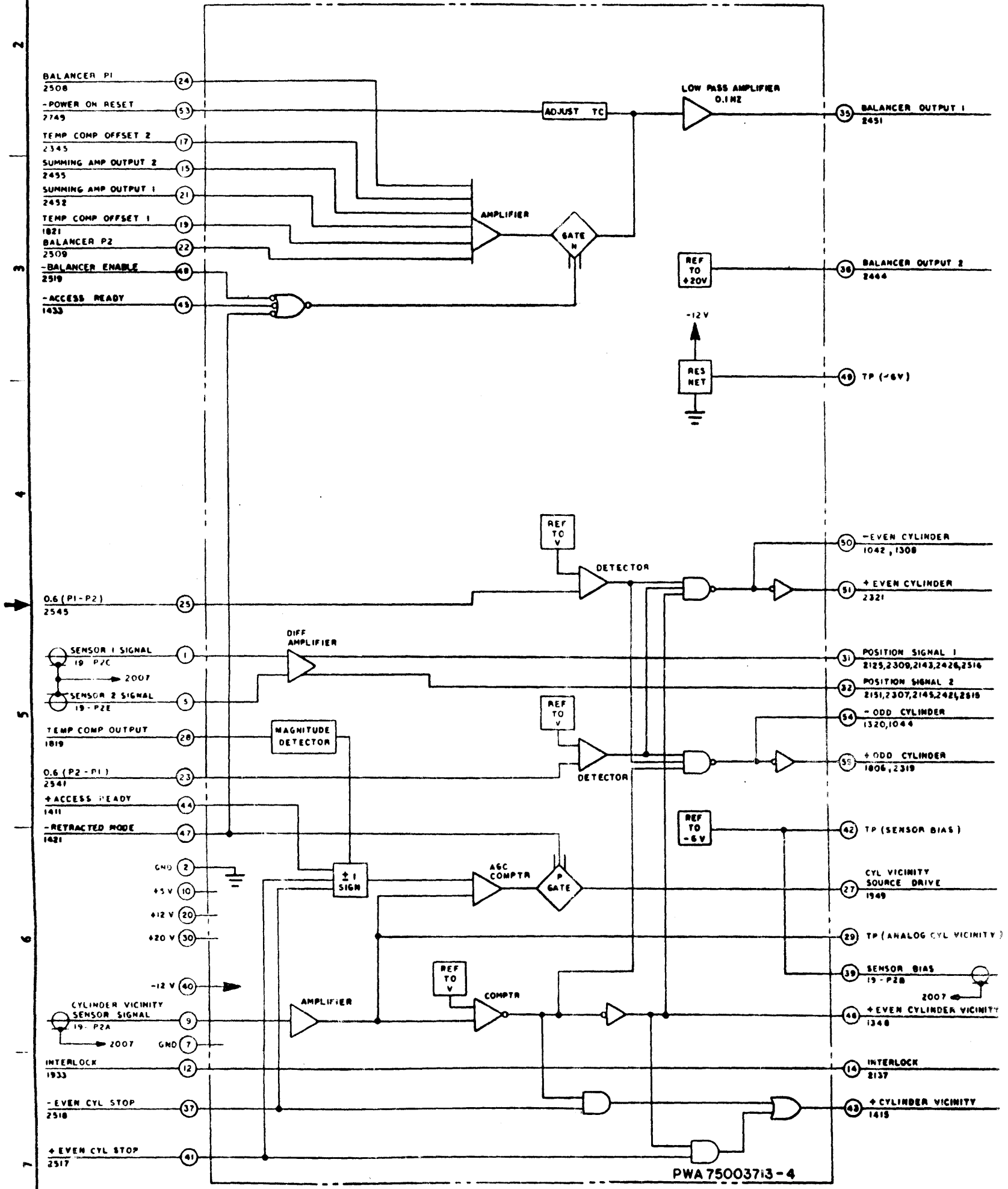
SKT 20

REDUCED SIZE
PRINT

LOGIC DIAGRAM -
CYLINDER
DETECTOR

INFORMATION STORAGE SYSTEMS
CORPORATION, CALIFORNIA

DATE: 1968
DRAWN BY: [Signature]
CHECKED BY: [Signature]



CYLINDER DETECTOR
SOCKET 20

21

2

1

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4

5

6

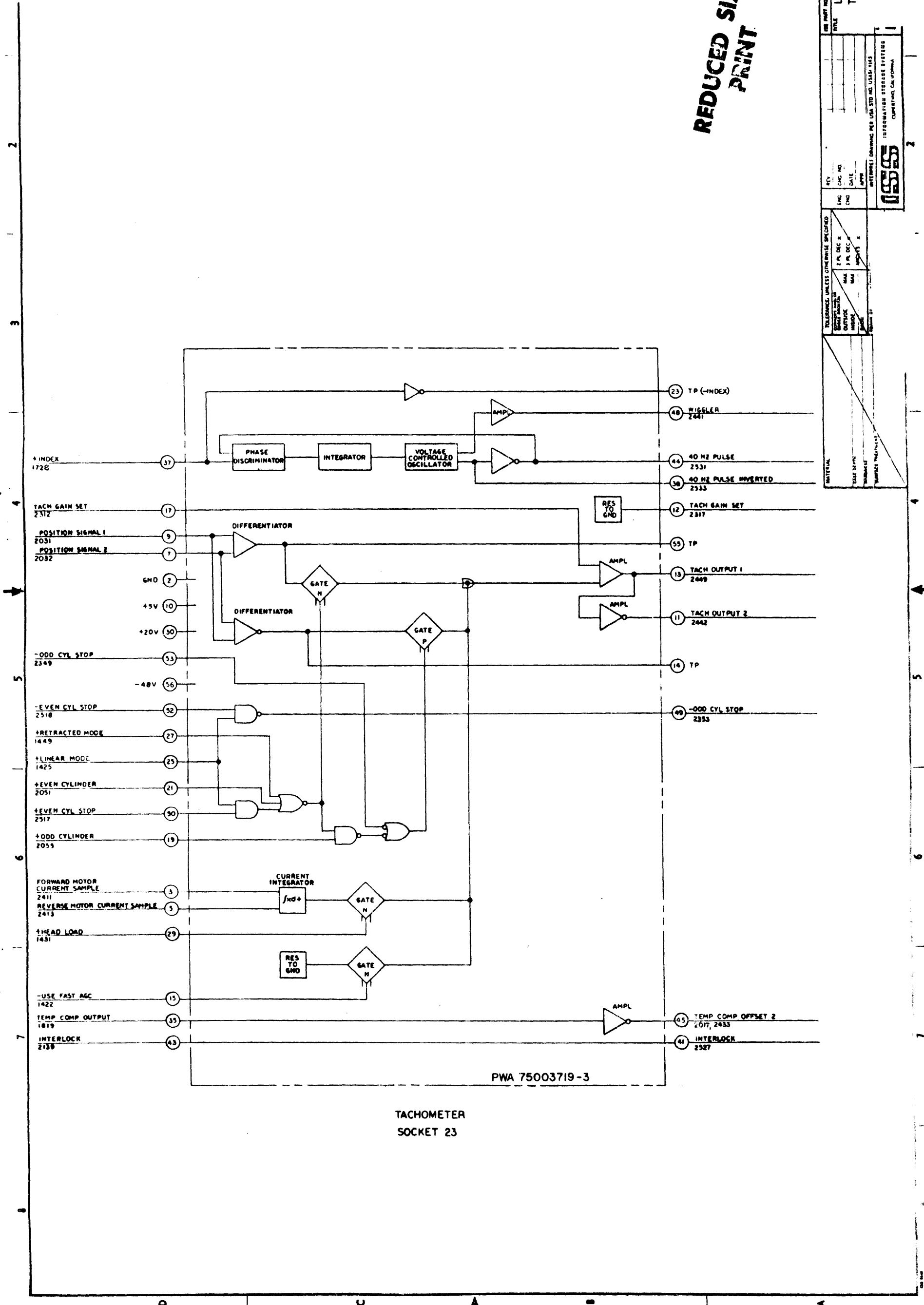
7

8

REVISION NO.	
RELEASED FOR AUTH.	
QTY.	
SKT 23	

**REDUCED SIZE
PRINT**

LOGIC DIAGRAM	
TACHOMETER	
PWA 75003719-3	
INTERPRET DRAWING PER USA STD NO. USA1-1965	
INFORMATION STORAGE SYSTEMS	
CAMP BELL, CALIFORNIA	
DATE: _____	
BY: _____	
CHK NO: _____	
CHK DATE: _____	
APP: _____	
TOLERANCES UNLESS OTHERWISE SPECIFIED	
FR. DEC. #	DATE
ASSEMBLY	PROJECT #
DATE SHIP	PROJECT
MARKET	PROJECT



RELEASED FOR	BY:
DATE:	
SKT 24	

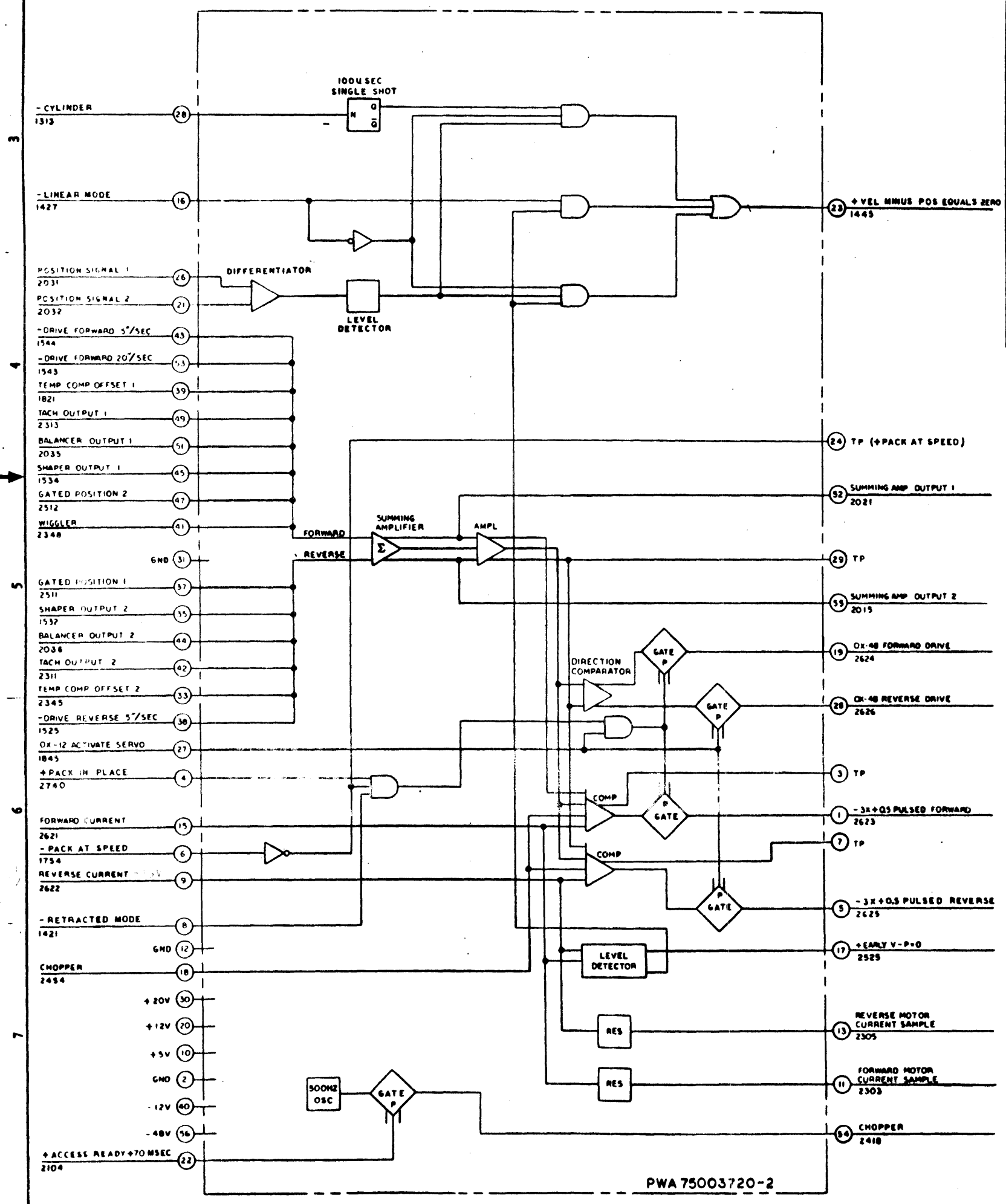
**REDUCED SIZE
PRINT**

REV.	CHG.	DATE	BY

TITLE: LOGIC DIAGRAM -
 SUMMING AND PULSER

24

INFORMATION STORAGE SYSTEMS
 COMPUTING CORPORATION



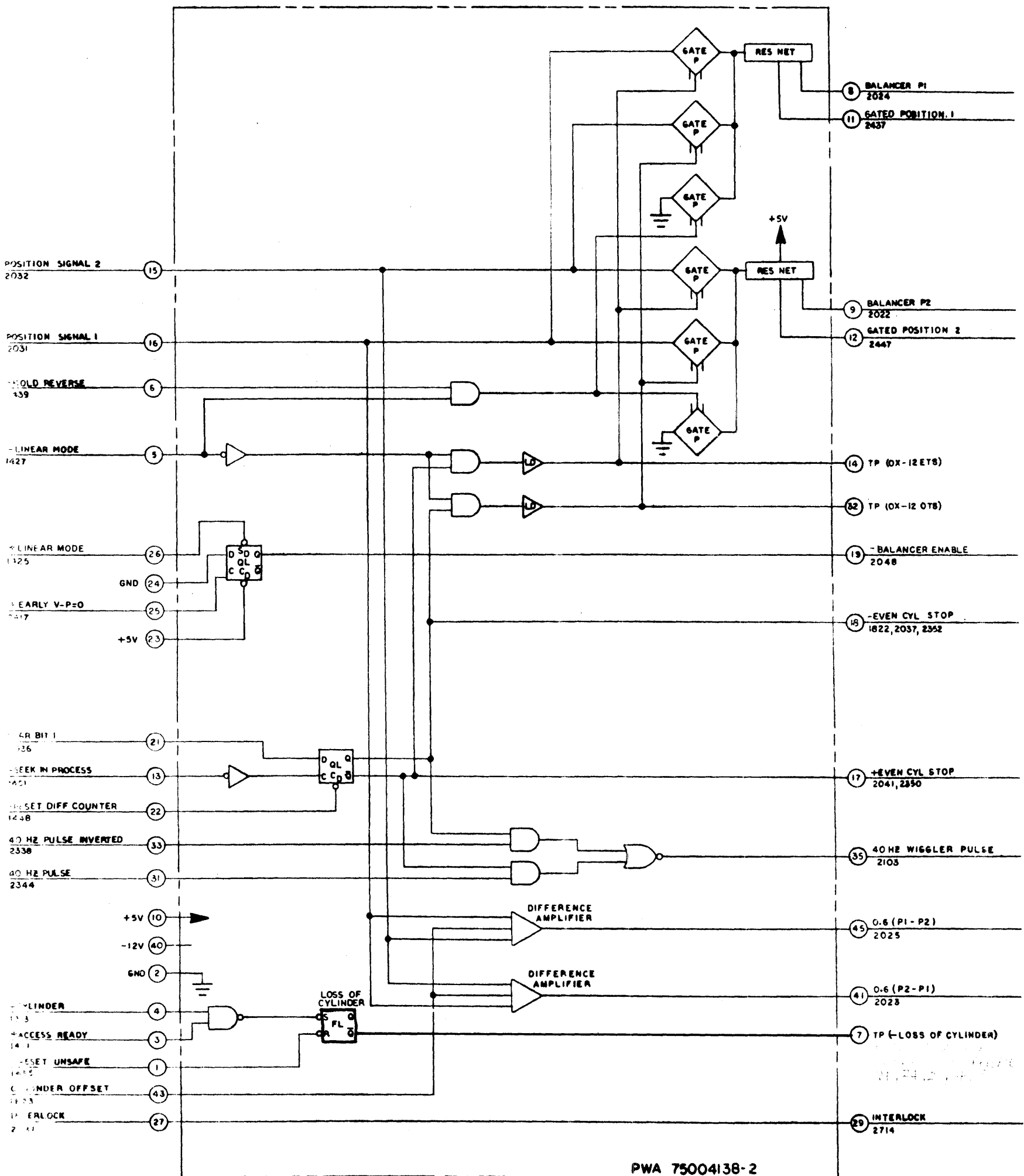
**SUMMING AND PULSER
SOCKET 24**

PWA 75003720-2

24

RELEASED FOR MNT. QTY:	1
REV	1
SKT 25	

LOGIC DIAGRAM CYLINDER SELECT	ISS INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
REV: _____ DESIGNED BY: _____ DATE: _____	QTY: _____ DATE: _____
TOLERANCE UNLESS OTHERWISE SPECIFIED: RESISTORS: 5% (1%, 2%, 5%, 10%, 20%, 50%, 100%) CAPACITORS: 5% (1%, 2%, 5%, 10%, 20%, 50%, 100%) DIMENSIONS: AS SHOWN	



CYLINDER SELECT
SOCKET 25

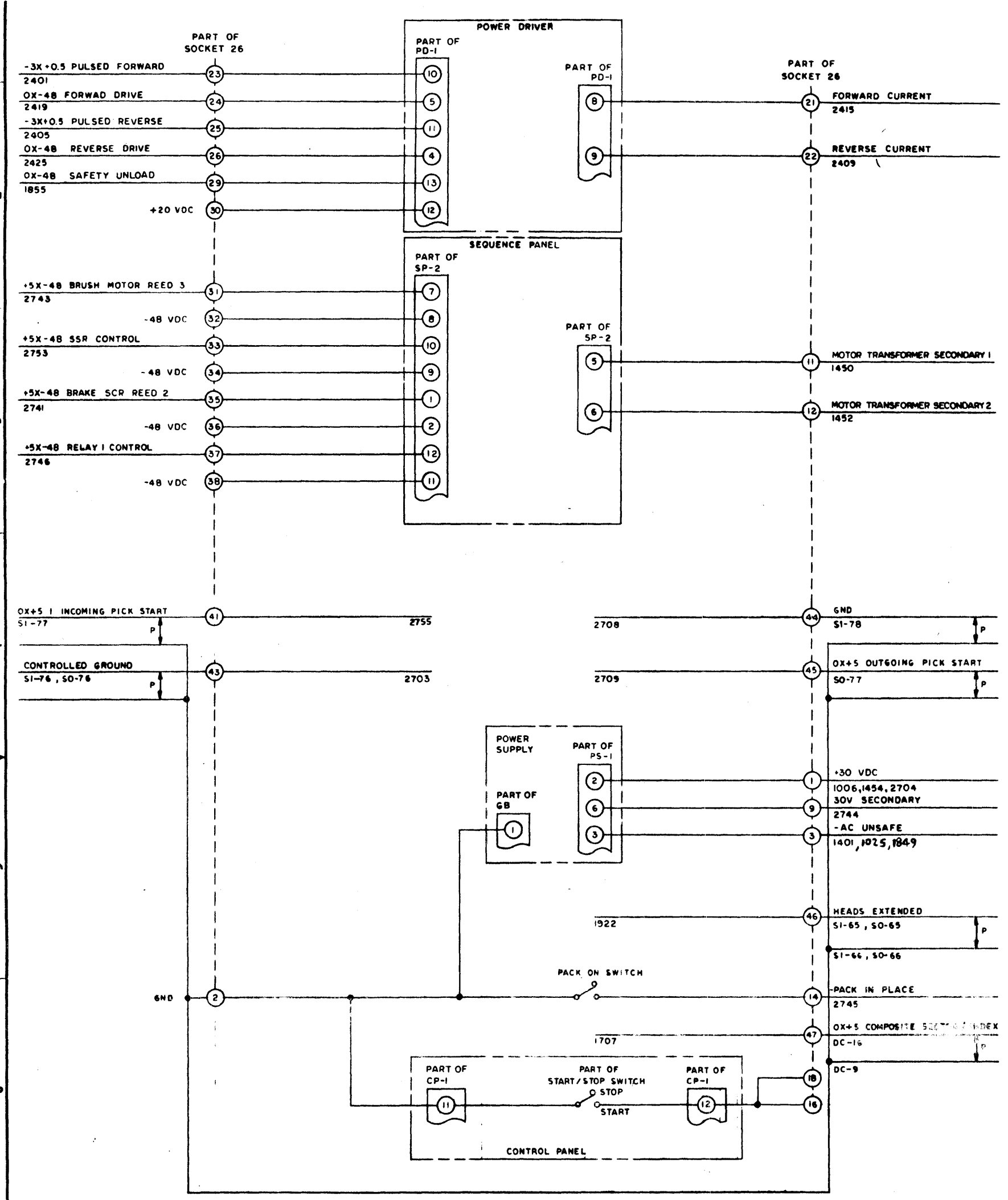
PWA 75004138-2

RELEASED FOR AMB. USE

26
26

ISS INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA

INTERCONNECTION DIAGRAM
POWER SEQUENCER AND
PULSER PADDLE



PART OF HARNESS ASSEMBLY
83004358-1

POWER SEQUENCER AND PULSER PADDLE
SOCKET 26

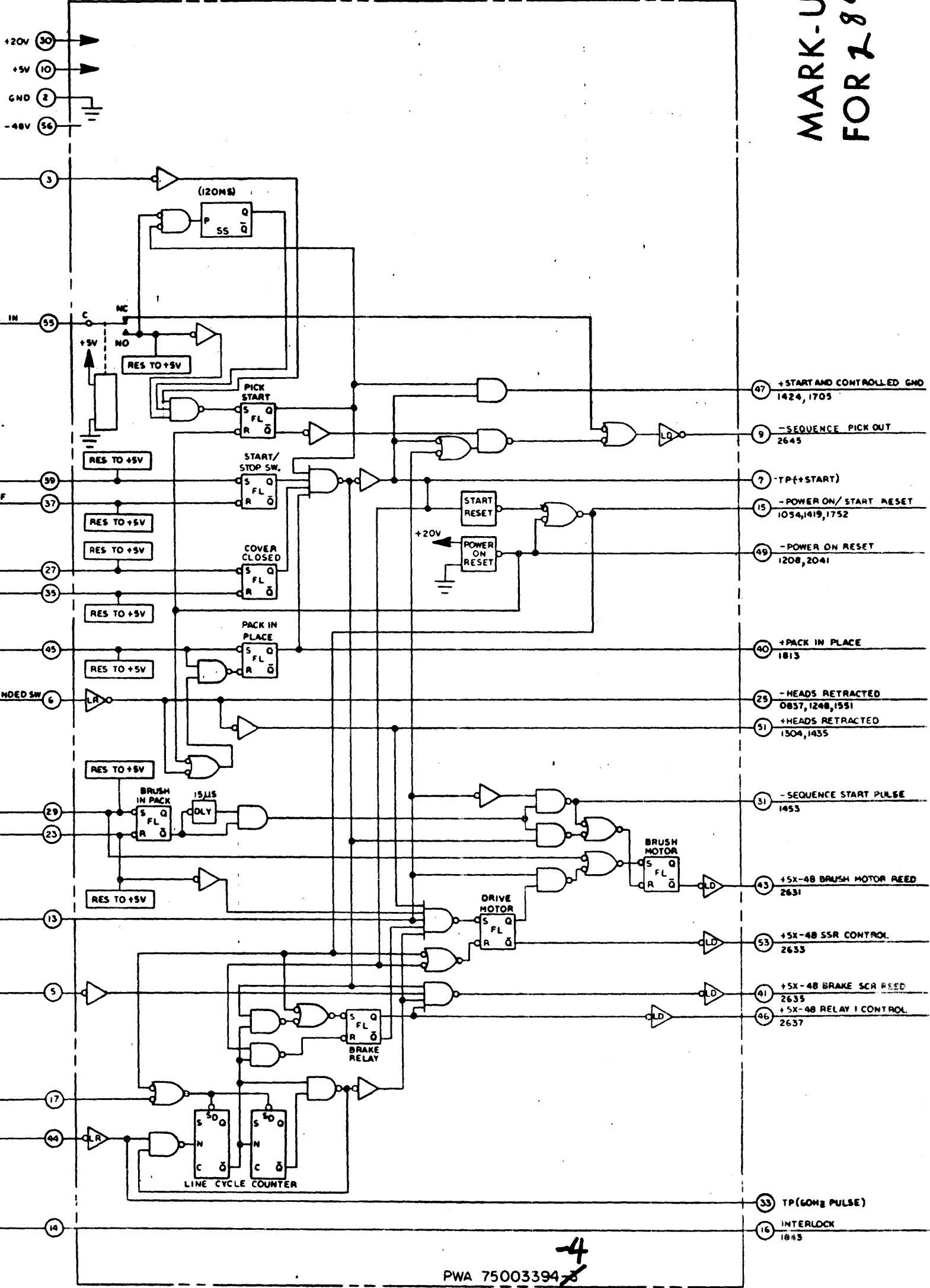
07003394-3A

REDUCED SIZE
PRINT

DRAWING NO.	07003394-3A
DEVELOPMENT NO.	
RELEASED FOR ASST.	QTY.

REV	A	07003394-3A
CHK NO.	E1232	LOGIC DIAGRAM
DATE	7/20/71	POWER CONTROL
APP	MJ	
INTERRUPT DRAWING PER USA 229 AND USAM 1744		
ISS		
REVISION NO.	D	07003394-3A
DESCRIPTION		OPERATION STORAGE SYSTEMS
CENTRAL COLLEGE		

MARK-UP
FOR 2844B



POWER CONTROL
SOCKET 27

REV	A	07003394-3A
CHK NO.	E1232	LOGIC DIAGRAM
DATE	7/20/71	POWER CONTROL
APP	MJ	
INTERRUPT DRAWING PER USA 229 AND USAM 1744		
ISS		
REVISION NO.	D	07003394-3A
DESCRIPTION		OPERATION STORAGE SYSTEMS
CENTRAL COLLEGE		

SKT28

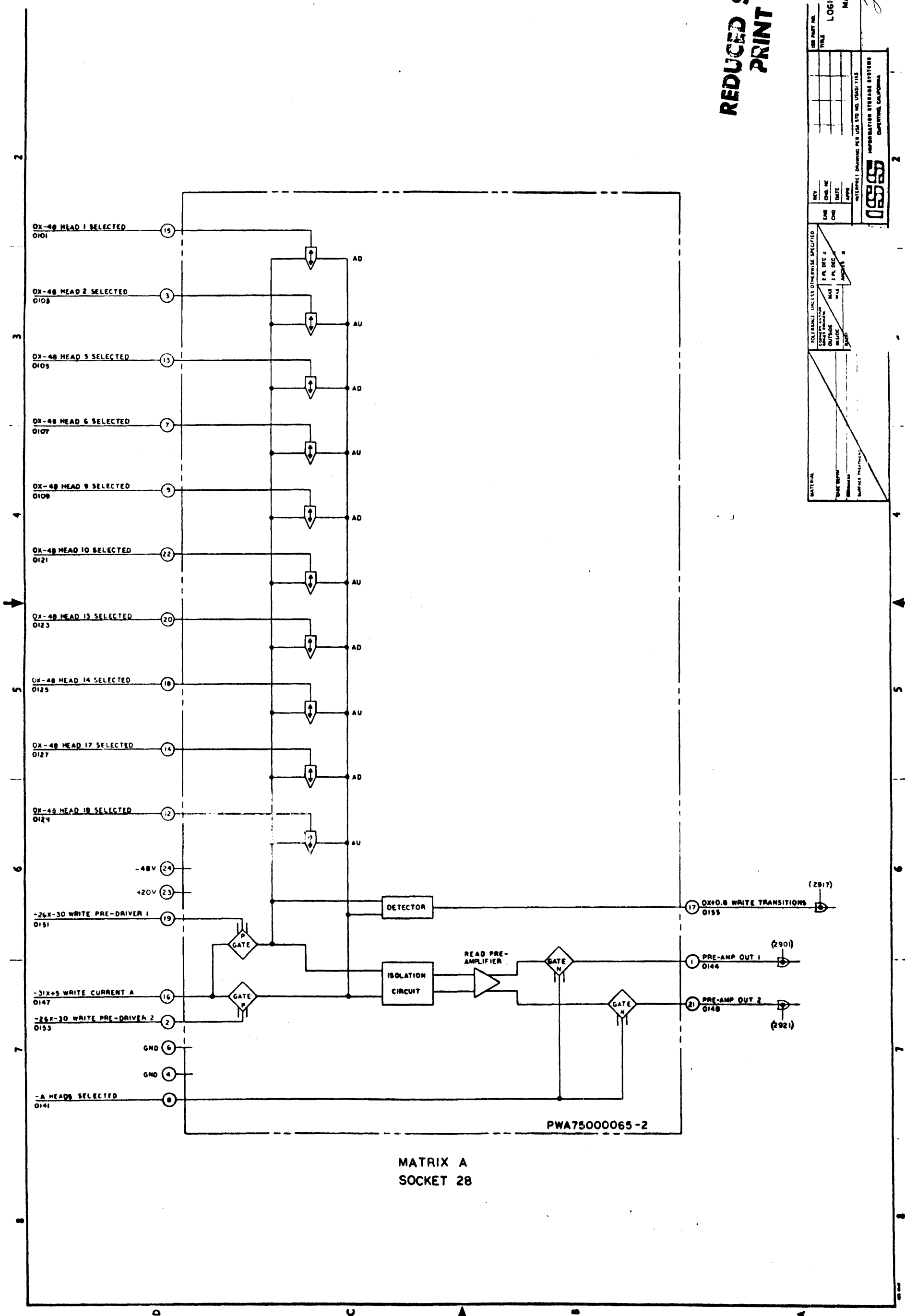
REDUCED SIZE
PRINT

LOGIC DIAGRAM -
MATRIX A

28

DATE: _____
DRAWN BY: _____
CHECKED BY: _____
DATE: _____

INFORMATION STORAGE SYSTEMS
CALIFORNIA

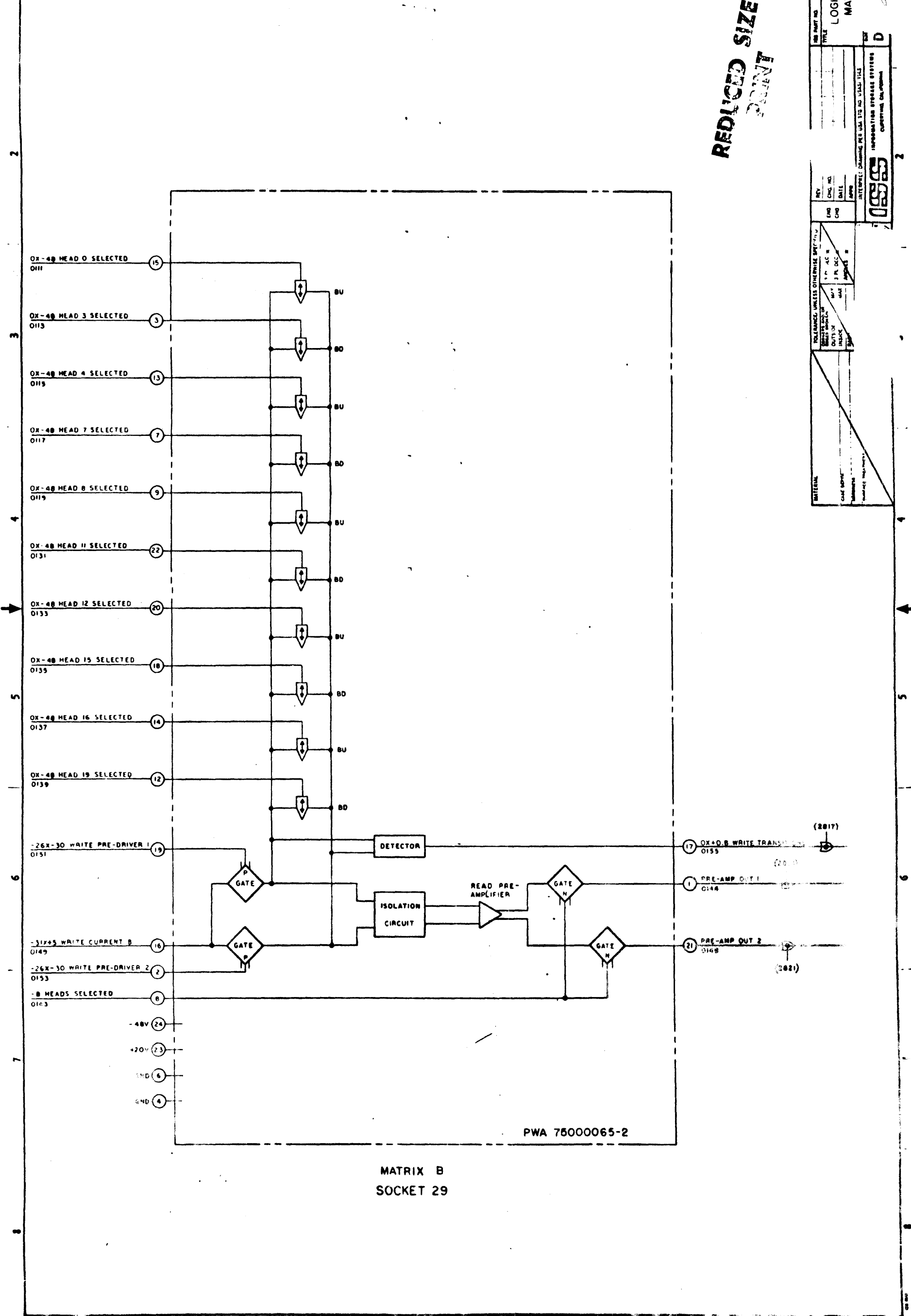


MATRIX A
SOCKET 28

RELEASED FOR AMT. CPT.
SKT 29

REDUCED SIZE
PRINT

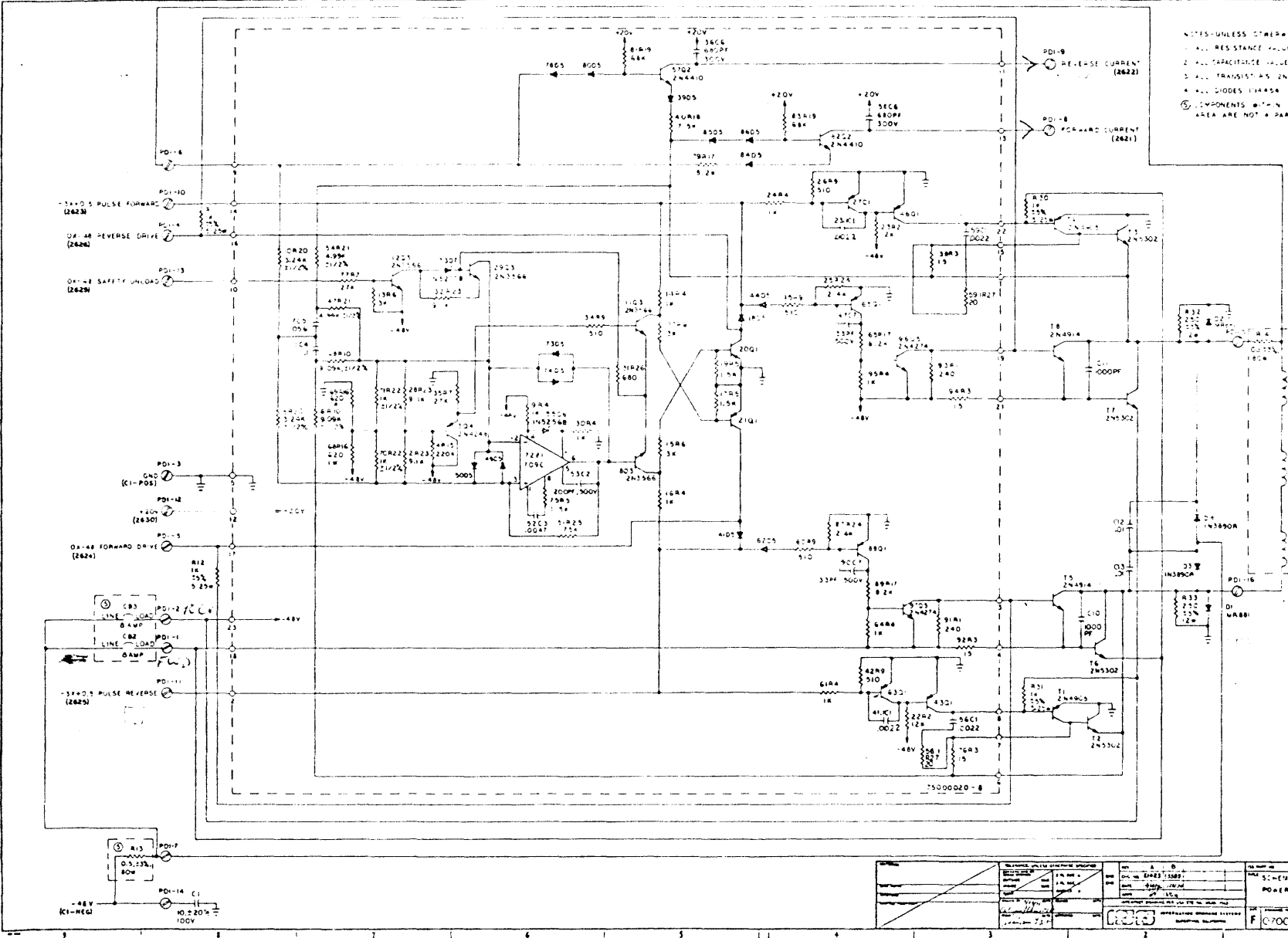
REV	REV	REV	REV	REV
DATE	DATE	DATE	DATE	DATE
BY	BY	BY	BY	BY
CHKD	CHKD	CHKD	CHKD	CHKD
APPV	APPV	APPV	APPV	APPV
LOGIC DIAGRAM - MATRIX - B 29				
INTEROFFICE DRAWING PER MIL-STD-883C INFORMATION STORAGE SYSTEMS COMPUTING DIVISION				



MATRIX B
SOCKET 29

29

- NOTES-UNLESS OTHERWISE SPECIFIED:
- 1. ALL RESISTANCE VALUES IN OHMS/22K/M
 - 2. ALL CAPACITANCE VALUES IN P.F./100/500V
 - 3. ALL TRANSISTORS 2N2645
 - 4. ALL DIODES 1N454
 - 5. COMPONENTS WITHIN THIS DOTTED AREA ARE NOT A PART OF THIS ASSY



REV	1	DATE	10/10/63
REV	2	DATE	11/10/63
REV	3	DATE	12/10/63

REV	4	DATE	1/10/64
REV	5	DATE	2/10/64
REV	6	DATE	3/10/64

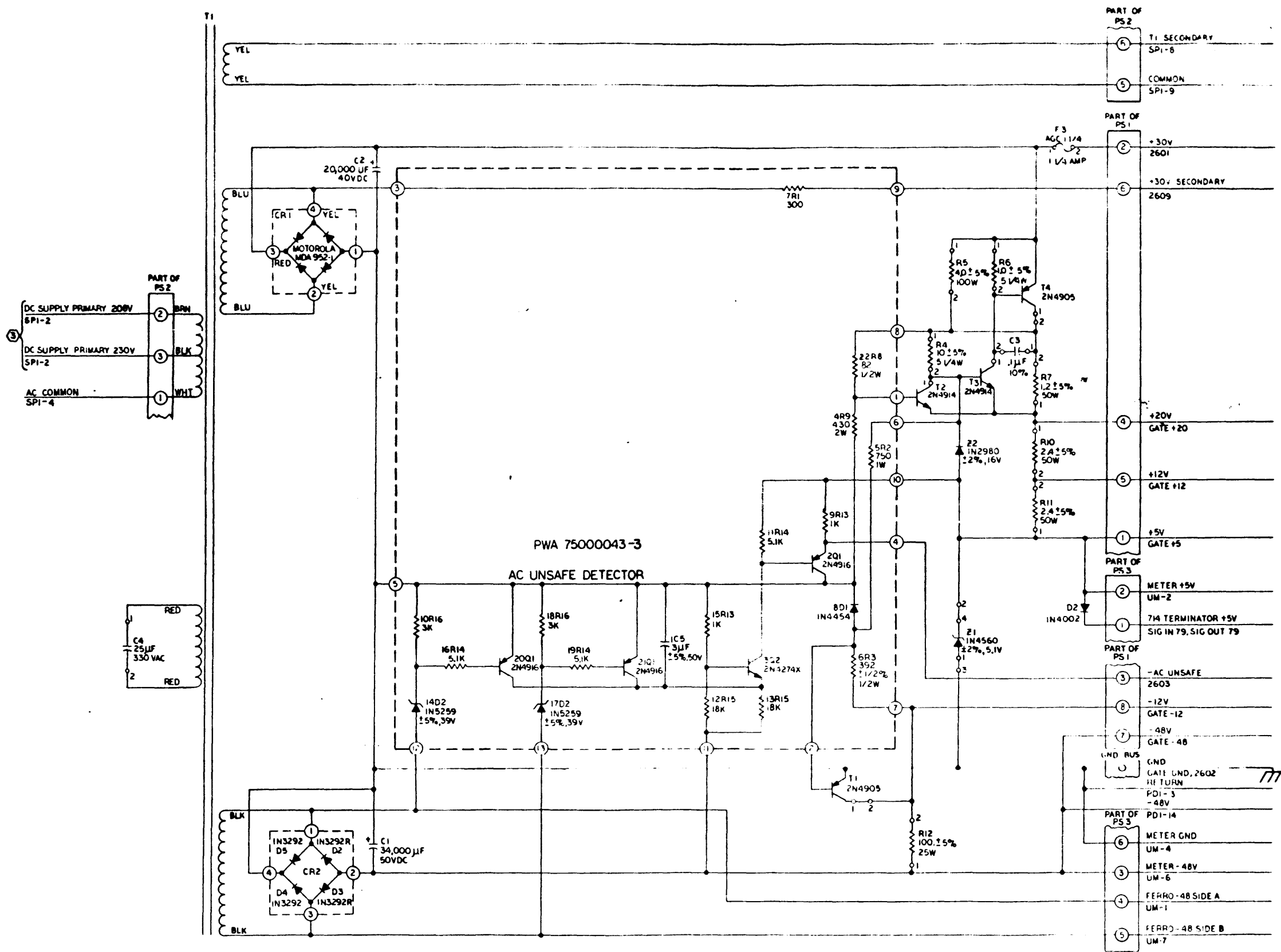
REV	7	DATE	4/10/64
REV	8	DATE	5/10/64
REV	9	DATE	6/10/64

REV	10	DATE	7/10/64
REV	11	DATE	8/10/64
REV	12	DATE	9/10/64

REV	13	DATE	10/10/64
REV	14	DATE	11/10/64
REV	15	DATE	12/10/64

REV	16	DATE	1/10/65
REV	17	DATE	2/10/65
REV	18	DATE	3/10/65

NOTES - UNLESS OTHERWISE SPECIFIED:
 1. ALL RESISTANCE VALUES IN OHMS, 2.2%, 1/4W
 2. § TERMINAL DESIGNATION
 3. ONLY ONE OF THE TWO INPUTS IS CONNECTED TO SPI-2 DEPENDING ON INPUT LEVEL
 4. TERMINATION ABBREVIATIONS:
 PD - POWER DRIVER SP - SEQUENCE PAPER
 PS - POWER SUPPLY UM - USAGE METER



REDUCED SIZE PRINT

07000605-2
DEVELOPMENT NO.
RELEASED FOR REPAIR
REVISION

TOLERANCE UNLESS OTHERWISE SPECIFIED:	REV. A	REV. PART NO.	07000605-2
RESISTOR	1 IN. DEC. 2	TITLE	SCHEMATIC DIAGRAM
CAPACITOR	1 IN. DEC. 2	DC POWER SUPPLY - 60HZ	
INDUCTOR	1 IN. DEC. 2		
DIODE	1 IN. DEC. 2		
TRANSISTOR	1 IN. DEC. 2		
TRIGGER	1 IN. DEC. 2		
RELAY	1 IN. DEC. 2		
VALVE	1 IN. DEC. 2		
OTHER	1 IN. DEC. 2		
DATE	3/15/74	DESIGNED BY	
APP'D		CHECKED BY	
REVISIONS		DATE	
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