DATAPOINT

Model 1241 VISTA-PC ARC NETWORK RIM

Product Specification

61823

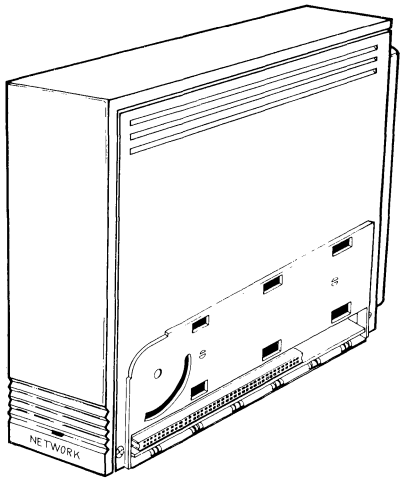
January 1985

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Document No. 61823.

DATAPOINT



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PREFACE

Systems designers and other individuals requiring detailed technical information about the 1241 NETWORK Resource Interface Module (RIM), including the ARCNET RIM components, should read this manual. Included in this product specification is a technical description of the module and programming information.

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Chapter 1.
PRODUCT SPECIFICATION

Overview

Introduction

The DATAPOINT Model 1241 ARC [R] NETWORK RIM is an ARCNET [R] interface product designed for use with the 1200 Professional Color Computer (VISTA-PC [TM]). This product specification provides the following information about the module:

- technical description,
- hardware requirements,
- interface description, and
- programming information.

For additional information about the module, refer to the *VISTA-PC ARC User's Guide* (Document No. 80951).

Purpose

The DATAPOINT NETWORK RIM Module enables the 1200 Professional Color Computer (VISTA-PC) to share computing resources and data bases over the Attached Resource Computer (ARC) local area network.

Description

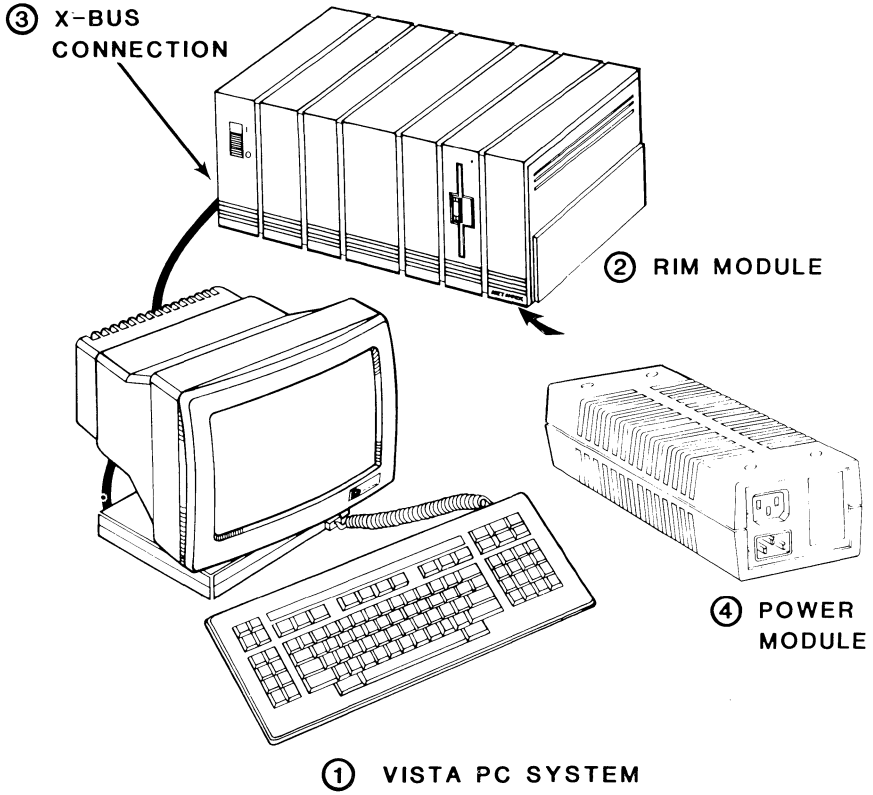
The ARC NETWORK RIM, housed in a vertical module, connects directly to the processor bus (X-BUS) as an expansion module. The module may be latched into place anywhere along the X-BUS, with two exceptions.

- The Processor module must be connected to the Graphics module; the NETWORK RIM module cannot be placed between them.

- Expansion disk drives without controllers must be connected to the disk module containing the controller; the NETWORK RIM module cannot be placed between them.

VISTA-PC/RIM module diagram

The following diagram illustrates the NETWORK RIM module connected to other VISTA-PC modules along the X-BUS.



Parts table

The following table describes the connection points between the NETWORK RIM module and the VISTA-PC.

DIAGRAM KEY	PART NAME
1	VISTA-PC
2	NETWORK RIM module
3	X-BUS connection point
4	Power supply converter

Connection specifications

Two factors can affect the connection of a NETWORK RIM module to the X-BUS:

- X-BUS signal load limit, and
- available DC power.

X-BUS signals

The X-BUS has a maximum signal range of 24 in. (measured from the right side of the processor module to the right side of the last X-BUS module). If adding another module to the X-BUS exceeds this limit, then performance degradation may occur.

Power Supply

Introduction

The NETWORK RIM module's power supply, as part of the VISTA-PC system, has two main subdivisions.

- Internal power--each module contains an internal DC/DC converter that converts 36 VDC to the necessary DC operating voltages.

- External power--the system power supply is an external AC/DC (Model No. 1223) converter. The converter connects directly to the processor and powers the processor through the internal DC/DC converter. Power is also sent along the X-BUS to power additional X-BUS modules.

  The following sections describe the requirements for connecting additional external power supplies and provide an example.

Power codes

The rear panel of a VISTA-PC module may display a POWER CODE label indicating the power consumption. Certain VISTA-PC modules do not have a POWER CODE label. For example, the NETWORK RIM module is not labeled. The following table describes when a module is or is not labeled.

IF A MODULE HAS A POWER CONSUMPTION OF...	THEN THE MODULE...
over one-half of one POWER CODE.	is labeled with a POWER CODE number.
less than one-half of one POWER CODE.	is not labeled with a POWER CODE number.

When to add power supplies

Each module on the X-BUS has provisions for accepting additional power from a 1223 AC/DC converter power supply. The following table describes how to determine when another AC/DC power supply is required.

IF...	THEN...
a module is added to the X-BUS system,	add the POWER CODES of all the modules together.
the sum of all the POWER CODES exceeds ten (the power supply capacity),	add another 1223 AC/DC power supply to the module that caused the sum of the codes to exceed ten.

Note:

Each module has a built-in power supply switch/converter which automatically disconnects the remaining X-BUS power system from the previous power supply.

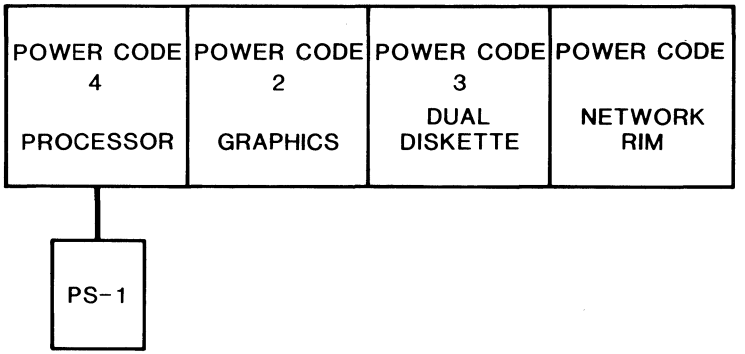
Example

The NETWORK RIM module has no POWER CODE marking, but its power consumption cannot be ignored.

IF THE SUM OF...	THEN...
all the modules already attached to the VISTA-PC is ten,	add another AC/DC converter before you add the NETWORK RIM module.
all other modules is only nine,	the NETWORK RIM module can be added without additional power supplies.

External power supply diagram

The following block diagram illustrates the use of 1223 AC/DC external power supplies.



PS-1 is always connected to the processor

Model 1241 NETWORK RIM Module

Introduction

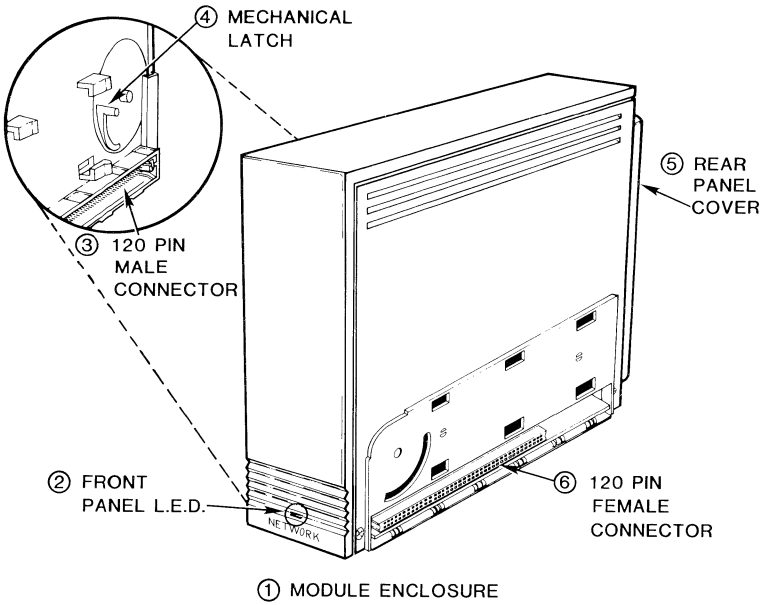
The ARC NETWORK RIM module has four basic parts:

- NETWORK RIM module enclosure,
- front panel indicator,
- edge connectors, and
- rear panel connectors, indicator, and switch.

The following sections describe each module component.

NETWORK RIM module diagram

The diagram below illustrates the main parts of the NETWORK RIM module. The following sections describe each major part in greater detail.



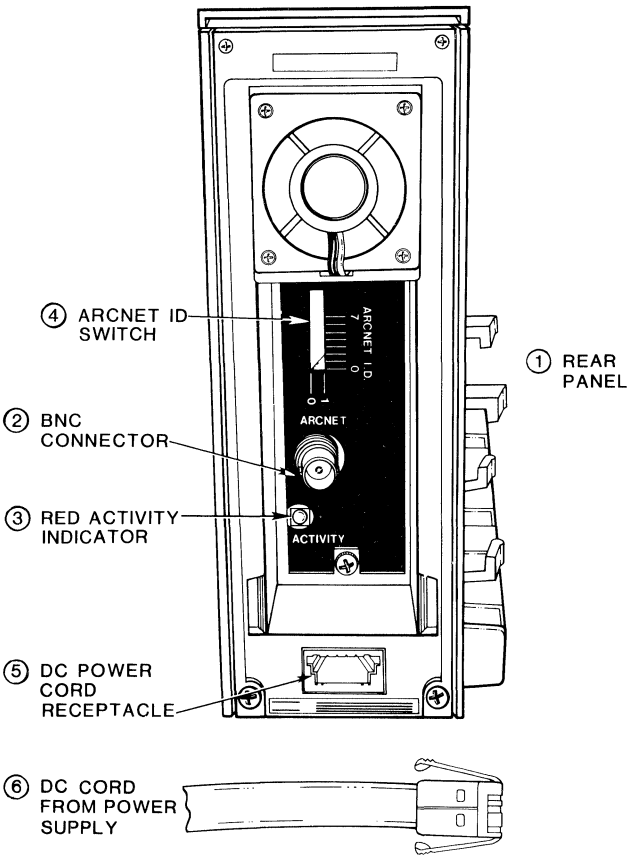
Parts/functions table

The module's major parts and their functions are listed below.

DIAGRAM KEY AND PART NAME		FUNCTION
1	Module enclosure	Contains RIM electronics
2	Front panel LED	Indicates module initialization is complete
3	120-pin male edge connector	Connects X-BUS signal lines of the RIM module to the previous module
4	Mechanical latch	Enables the module to be locked into place along the X-BUS
5	Rear panel cover	Provides protection for coaxial connection
6	120-pin female edge connector	Connects X-BUS signal lines of the RIM module to the subsequent module

Rear panel diagram

The following diagram illustrates the main parts of the NETWORK RIM module rear panel.



Rear panel parts/functions table

The following table describes the main parts of the NETWORK RIM module rear panel.

DIAGRAM KEY AND PART NAME		FUNCTION
1	Rear panel	Contains network activity indicator and network BNC connection
2	BNC connector	Connects the VISTA-PC to the local area network through coaxial cable
3	Rear panel LED	Indicates network activity
4	ARCNET ID switch	Enables the ARCNET network ID number to be manually set
5	DC power cord receptacle	Provides DC power connection

Hardware description

General performance characteristics of the NETWORK RIM module include:

SPECIFICATION	DESCRIPTION
Module type	Self-contained, add on, Resource Interface Module (RIM)
Interface type	1200 processor bus (X-BUS)
Coaxial port	1 standard with BNC connector
Network data rate	2.5 megabaud per second (Mbps) token passing
X-BUS data transfer (to and from 1200 processor)	8 bits per transfer

Environmental Specifications

Introduction

The NETWORK RIM module is designed to operate within the following environmental parameters.

Power specifications

SPECIFICATION	DESCRIPTION
Power consumption	7 watts (1/2 of one POWER CODE)
DC power	36 volts supplied through X-BUS or external power converter
Power cord	DC line cord if required

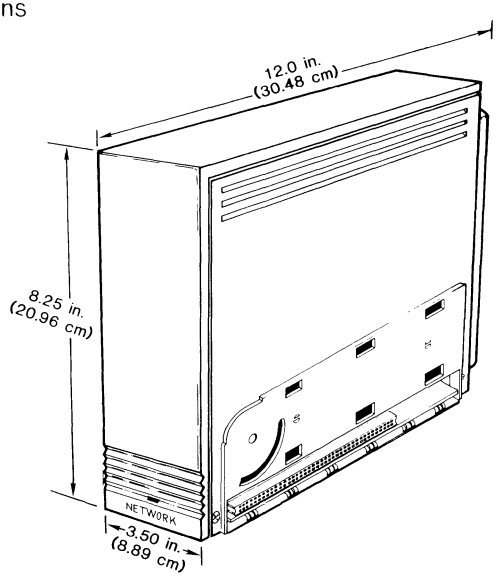
Temperature specifications

SPECIFICATION	DESCRIPTION
Operating	50 to 80 degrees Fahrenheit 10 to 27 degrees Celsius
Relative humidity	20 to 80% noncondensing

Environmental conformance

SPECIFICATION	DESCRIPTION
Radiated and conducted emissions	FCC part 15, subpart J, with proper installation, Class A
Regulatory compliance	UL 478, CSA C 22.2 No. 154-1983

Module dimensions



SPECIFICATION	DESCRIPTION
Height	8.25 inches (20.96 centimeters)
Width	3.50 inches maximum (8.89 centimeters)
Depth	12.00 inches maximum (30.48 centimeters)
Weight	4.50 pounds maximum (2.04 kilograms)

System Requirements

Introduction

In addition to standard compatibility requirements, the NETWORK RIM module has three basic system requirements:

- connection to the system's X-BUS,
- X-BUS power supply connector, and
- support for the coaxial cable.

The requirements are described in the following sections.

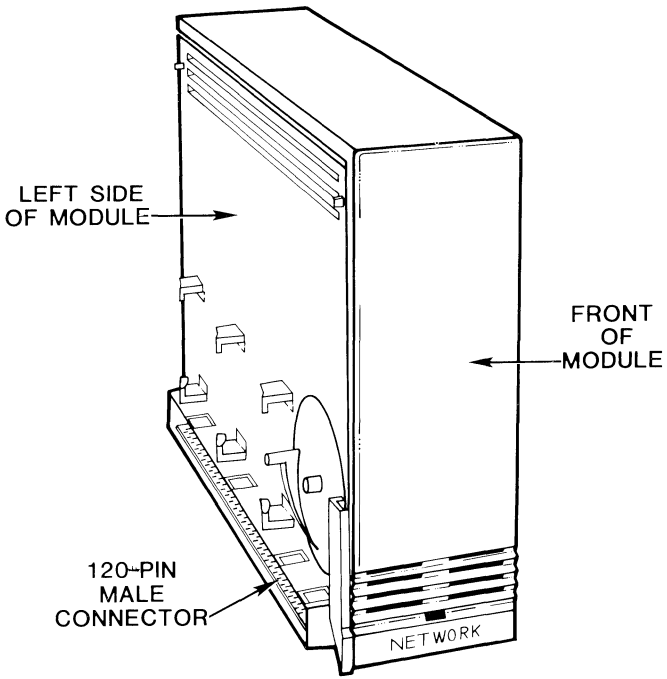
X-BUS connection

The NETWORK RIM module connects directly to the X-BUS by means of a 120-pin edge connector. As viewed from the front, the module has two types of edge connectors:

- a 120-pin male connector located on the left edge of the module, and
- a 120-pin female connector located on the right edge of the module.

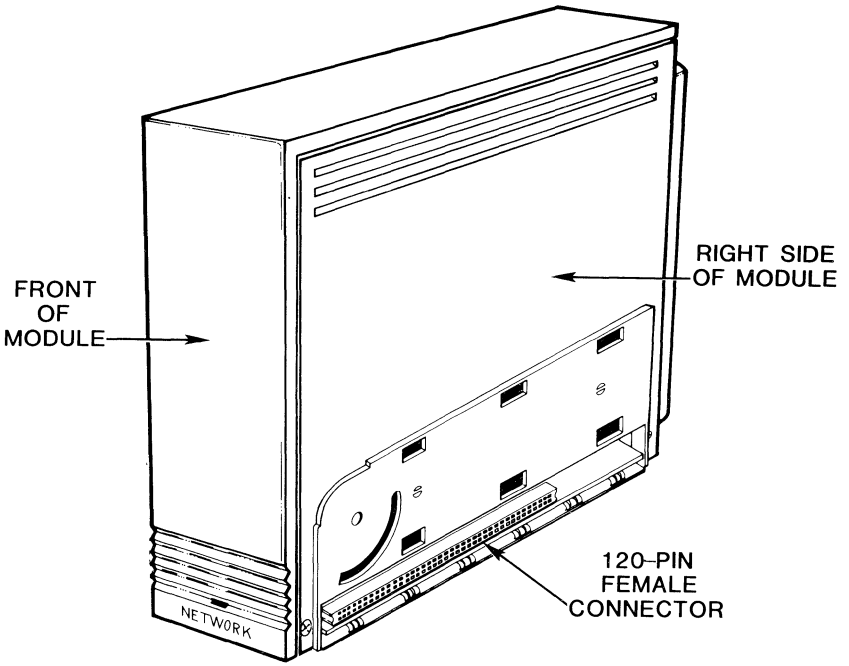
Left edge connector diagram

The following diagram illustrates the 120-pin male edge connector located on the lower left edge of the module.



Right edge connector diagram

The following diagram illustrates the 120-pin female edge connector located on the lower right edge of the module.



Connector requirements

X-BUS connection

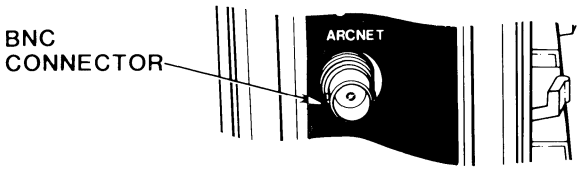
Integral to the NETWORK RIM module is a motherboard providing the interconnection between modules on the X-BUS.

Coaxial connection

To accommodate the network's coaxial cable, the module also contains a rear-panel-mounted BNC connector.

BNC connector

The following diagram illustrates the BNC connector located on the module's rear panel.



REAR PANEL

Software noncompatibility warning

The ARCNET Local Area Network Controller (LANC) chip can be configured for nonstandard operation to provide for messages longer than 253 bytes.

Caution:

Reconfiguring the LANC chip to permit messages longer than 253 bytes results in a system incompatible with standard ARCNET-based systems. Therefore, this feature should only be implemented after careful consideration.

Chapter 2.
INTERFACE CONSIDERATIONS

Overview

Introduction

Three types of interfaces enable the NETWORK RIM module to communicate with the processor and the network:

- a software interface,
- a local area network interface, and
- the processor interface bus (X-BUS).

Contents

This chapter describes the three types of NETWORK RIM interfaces. The first two are discussed in this section; the next section provides information about the X-BUS interface.

Software interface

The Local Area Network operating system controls the software interface. The software interface consists of the module's data buffer memory and the Local Area Network Controller's status and control registers which are discussed in *Chapter 3, PROGRAMMING CONSIDERATIONS.*

Local network interface

The module's inputs and outputs over the Local Area Network are by means of a bidirectional half duplex RG62 coaxial cable. A BNC connector located on the rear of the module serves as the interface to the Local Area Network.

Local Area Network characteristics

The Local Area Network is a high-speed, special-purpose, interprocessor communications link. The NETWORK RIM module supports standard ARCNET features.

- Data is transmitted over a coaxial cable at 2.5 megabits per second in a unique token-passing format.
- Each processor on the network has its own unique identification code established through the rear panel ARCNET ID switches.
- The network is self-polling, and packets of data are moved between processors using the ARCNET identification codes for the addresses.
- A single network can support up to 255 processors.

Note:

ID zero is reserved and cannot be used for a network ID.

X-BUS Interface

Introduction

The processor interface bus (X-BUS) provides the hardware interface between the processor and the NETWORK RIM module.

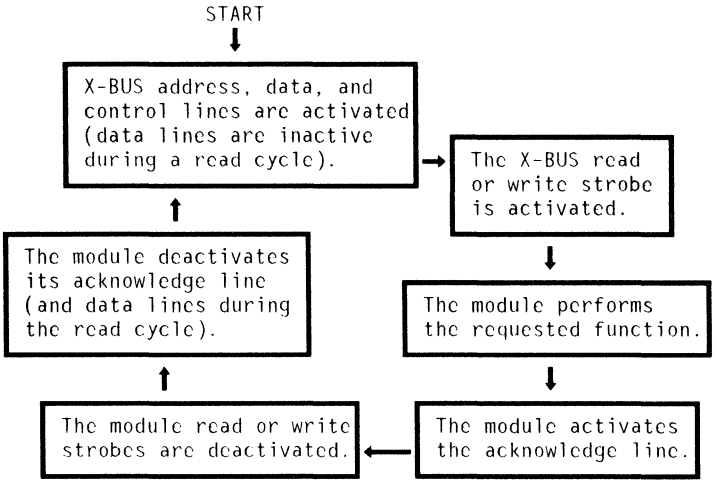
Description

The X-BUS is a system of interconnections permitting the processor to control data transfers to and from the NETWORK RIM module. The X-BUS has the following signal lines:

- address,
- data,
- control, and
- status.

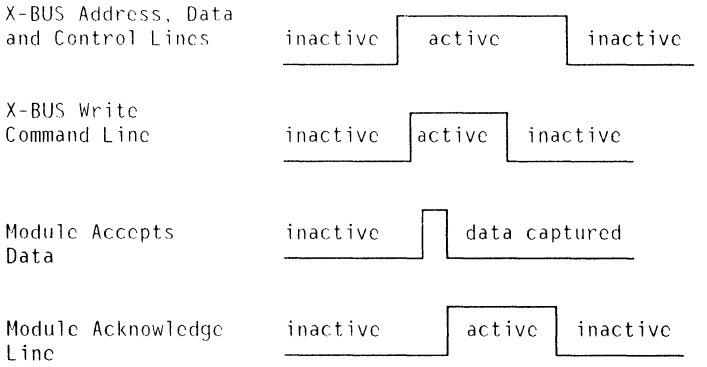
X-BUS cycles

The following sequence of events occurs on the X-BUS for every module read or write cycle, except during the module initialization cycle.



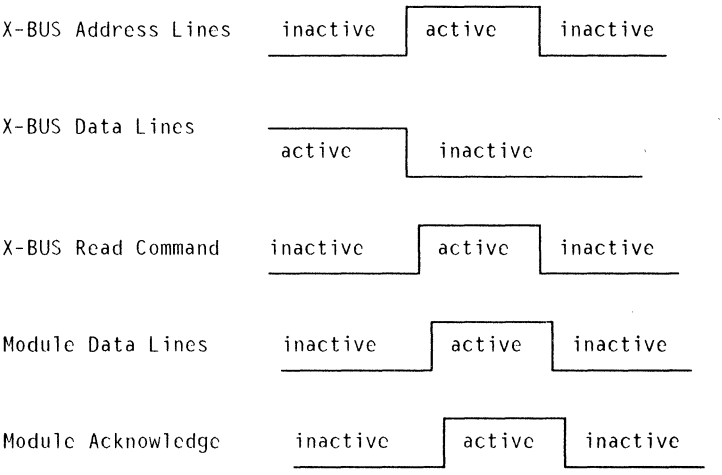
Write cycle timing diagram

The following diagram illustrates the write cycle timing sequence.



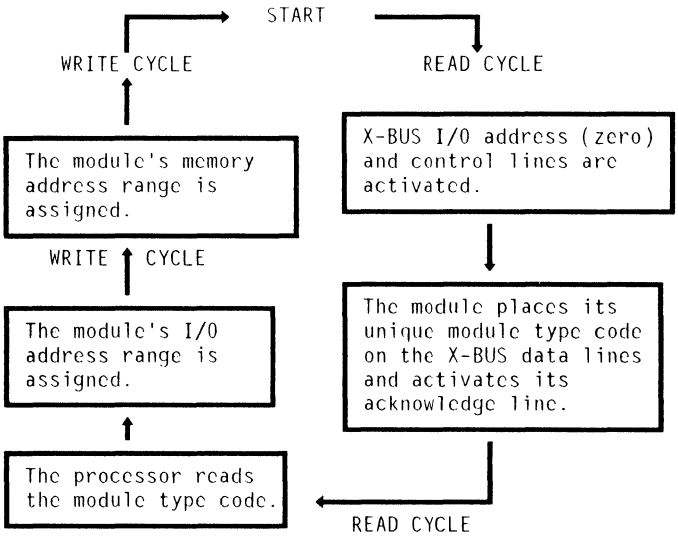
Read cycle timing diagram

The following diagram illustrates the read cycle timing sequence.



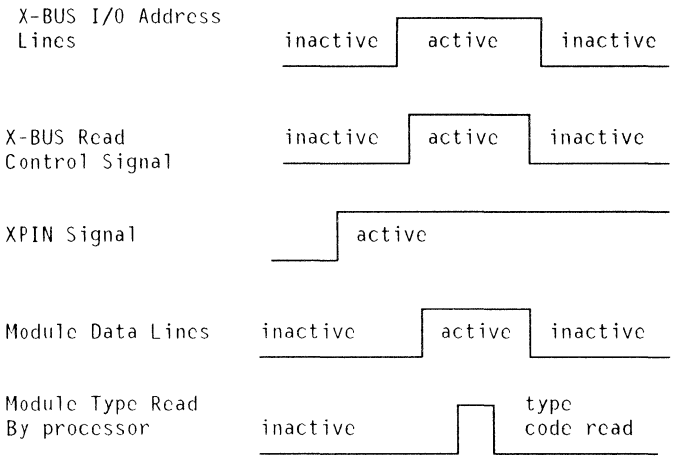
X-BUS initialization cycle

The following sequence of events occurs on the X-BUS to initialize each X-BUS module.



Module code read cycle timing

The following diagram illustrates the module type code read cycle timing sequence described in the previous section, *X-BUS initialization cycle*.



Chapter 3.
PROGRAMMING CONSIDERATIONS

Overview

Introduction

This chapter provides a functional description of the major circuits of the NETWORK RIM module. Programming information necessary to understand the module's functions and to aid in software development is also included.

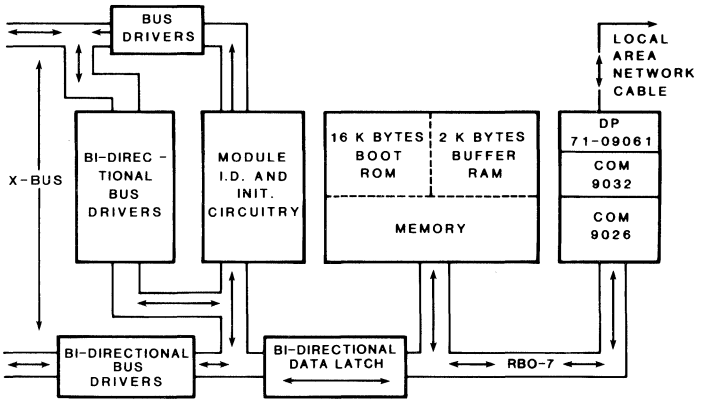
Module functions

The NETWORK RIM module has five major functions:

- Local Area Network control,
- Interrupt generation,
- Bootstrap ROM (not currently used),
- Status indications, and
- Module initialization.

Module data flow paths

The following diagram shows the NETWORK RIM module data flow paths. The module contains all of the necessary support circuitry to control these data flow paths.



Module I/O devices

With the exception of the 16-bit module type code (the module's device control register), all module components are 8-bit I/O devices. After the module's type code is read, the module supports 8-bit processor transfers only.

Network ID swtiches

An 8-bit switch bank, located on the back panel of the NETWORK RIM module, is used to set the ARCNET ID code. The ID code allows the network to identify each processor connected to the ARC local area network.

ID assignment

The ID code is assigned upon installation and may take any value from 1 to 255 (decimal). Zero (0) is reserved for broadcasts to the entire network of processors.

Note:

The list below provides the equivalent octal and hexadecimal (HEX) notation for the decimal values 1 to 255.

- 1 to 255 (decimal) = 1 to 377 in octal notation
- 1 to 255 (decimal) = 1 to FF in HEX notation

Local Area Network Controller (LANC)

Introduction

The heart of the entire module is the Local Area Network Controller (LANC). The LANC contains the majority of the intelligence required for local network interfacing and error detection.

Purpose

The Local Area Network Controller manages all network communications protocols and arbitrates all processor accesses to the module's memory devices.

Note:

All processor accesses to the LANC are by means of 8-bit (byte) transfers.

LANC chip support

Two associated circuits provide support and cable interfacing for the LANC chip.

- The COM 9032 transceiver gate array provides all timing and gating functions.
- The 71-0961 NETWORK RIM Interface hybrid controls the actual cable driving and receiver signal conditioning for the local network data.

LANC I/O addresses

The LANC requires two I/O address locations. The module's 256-I/O address range is assigned during module initialization.

LANC operations

The following table lists the LANC operations and their addresses.

OFFSET I/O ADDRESS	COMMAND	FUNCTION
40 (HEX)	Write	Write Interrupt Mask
40 (HEX)	Read	Read Status Register
41 (HEX)	Write	Write LANC Command
41 (HEX)	Read	Reserved

Read Status Register Commands

Introduction

The following sections describe the operations of the read status register, read status register LANC commands, and bit position definitions.

Read status register

Issuing a read status register command places the contents of the status register on the data bus (D0 to D7).

LANC status register contents

The LANC status register contents are defined as follows:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	ETS2	ETS1	POR	TEST	RECON TIMER	TMA	TRNSMTR. AVAILABLE

Register commands

The following table describes the contents of the LANC status register. Bit positions are listed in descending numerical order.

BIT	COMMAND	DESCRIPTION
7	Receiver Inhibited (RI)	If set to 1, bit 7 indicates a packet has been deposited into the RAM buffer inhibiting the receiver. Caution: The setting of this bit can cause an interrupt if enabled during a WRITE INTERRUPT MASK command.
6	ETS2	Bit 6 is preset to a logical 1.
5	ETS1	Bit 5 is preset to a logical 1.
4	Power-On Reset (POR)	If set to 1, bit 4 indicates the LANC has been reset. Setting bit 4 causes an interrupt which cannot be masked in this module.
3	Test (TEST)	Bit 3 is preset to a logical 0.
2	Reconfiguration (RECON)	When set to 1, bit 2 indicates the reconfiguration timer has timed out because the network receive input was idle for 78.2 microseconds. Bit 2 is reset to 0 during a Clear Flags command. Caution: The setting of the Clear Flags bit can cause an interrupt if enabled during the write interrupt mask command.

Read Status Register Commands

BIT	COMMAND	DESCRIPTION
1	Transmit Message Acknowledged (TMA)	If set to 1, bit 1 indicates the packet transmitted by an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged by the network receiving node (nn is the current transmit page). Bit 1 should be considered valid only after the TAt bit (bit 0) is set. Note: Broadcast messages are never acknowledged.
0	Transmitter Available (TA)	If set to 1, bit 0 indicates that the LANC is available for transmitting. Bit 0 is set at the conclusion of an ENABLE TRANSMIT FROM PAGE nn command or when DISABLE TRANSMITTER command is issued. Caution: Setting bit 0 can cause an interrupt if enabled during the WRITE INTERRUPT MASK command.

POR register states

During power-on reset (POR), the read status register assumes the following state:

BIT	7	6	5	4	3	2	1	0
STATE	1	1	1	1	0	0	0	1

WRITE LANC INTERRUPT MASK

Introduction

When certain bits in the status register are true (set to 1), the LANC generates an interrupt signal. Any ARC network event would cause an interrupt to the processor if a method were not in place to prevent it. The LANC INTERRUPT MASK is the register that prevents inapplicable network events from generating processor interrupts. The following sections describe the LANC INTERRUPT MASK register and its functions.

LANC MASK register

The following diagram illustrates the LANC MASK register contents in comparison with the status register:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	NOT USED	NOT USED	POR	NOT USED	RECON TIMER	NOT USED	TRNSMTR. AVAILABLE

WRITE LANC INTERRUPT MASK

Background

The following list provides background information about the LANC INTERRUPT MASK register and its use with the status register.

- Each bit position in the LANC INTERRUPT MASK is in the same position as its corresponding bit in the status register.
- A write to the LANC INTERRUPT MASK determines which of the bits in the status register can cause the interrupt.
- A logical 1 in a status register bit position enables the corresponding interrupt with one exception; the setting of the TMA status bit never causes an interrupt.
- The POR status bit causes an interrupt that cannot be masked inside the NETWORK RIM module regardless of the value of the corresponding LANC MASK register bit.

Interrupt signal

Interrupt signal generation

To produce a LANC interrupt signal, the three maskable status bits are AND'ed with their respective mask bits and the results are OR'ed with the POR status bit.

Deactivating the interrupt signal

The LANC interrupt signal returns to its inactive state when the interrupting status bit is reset to a logical 0 or when the corresponding bit in the LANC MASK register is reset to a logical 0.

Interrupt clear procedure

To clear an interrupt, use the method indicated in the following table:

TO CLEAR AN INTERRUPT GENERATED BY...	USE...
POR,	Clear Flags.
RECON,	
TA,	the corresponding mask bits reset to a logical 0.
RI,	

WRITE LANC (COM 9026) Commands

Introduction

Execution of a processor write to module I/O address XX41 (HEX) with the data shown results in execution of the commands described below. The WRITE LANC commands are listed in ascending order.

Reserved

00000000

Reserved.

Disable Transmitter

00000001

The Disable Transmitter command cancels any pending transmit command (transmission not yet started) when the LANC next receives the token. Upon receipt of the token, this command sets the Transmitter Available (TA) status bit.

Disable Receiver

The Disable Receiver command cancels any pending receive command. If the LANC has not yet received a packet, the next token received sets the Receiver Inhibited (RI) bit. If packet reception is already underway, reception runs to its normal conclusion.

Enable Transmit From Page nn

000nn011

The Enable Transmit command prepares the LANC to begin a transmit sequence from Random Access Memory (RAM) buffer page nn the next time it receives the token. As shown in the following table, the transmit process has five main stages.

STAGE	PROCESS
1	The command is issued and loaded.
2	The TA and TMA bits are reset to a logical 0.
3	The transmit sequence occurs.
4	The TA bit is set to a logical 1 upon completion of the transmit sequence.
5	The TMA bit is set if the LANC has received an acknowledgement from the destination network node.

Note:

The acknowledgement is managed strictly at the hardware level; the receiving node's LANC sends the acknowledgement even before its controlling processor detects a message.

Enable Reception to Page nn

b00nn100

The Enable Transmit command reception allows the LANC to receive data packets into RAM buffer page nn and resets the RI status bit to a logical 0. If b is a logical 0, then the LANC also receives broadcast transmissions. (A broadcast transmission is a transmission to network ID zero.) Successful reception of a message sets the RI status bit to a logical 0.

Define Configuration

0000c101

Setting c to a logical 1, enables the LANC to handle short as well as long packets (508 bytes or less). Setting c to a logical 0, causes the LANC to be configured for short packets (253 bytes or less) only.

Note:

The short packet configuration is the standard ARCNET component compatible configuration.

Clear Flags

000rp110

Setting p to a logical 1, clears the POR flag. Setting r to a logical 1, clears the RECON flag.

Buffer Memory

Introduction

A 2,048 byte RAM serves as the NETWORK RIM module buffer memory.

Description

The buffer memory is divided into four pages of 512 bytes each. Each of these pages may be used as either a transmit or a receive buffer area. The appropriate buffer size is specified in the Define Configuration command.

Buffer page initialization

The Processor I/O command enables either the LANC receiver or its transmitter and initializes the buffer page register.

Packet size

The LANC interprets the packet size based on the contents of buffer memory location 02.

IF BUFFER LOCATION 02 CONTAINS...	THE PACKET IS...
a zero byte,	long.
a nonzero byte,	short.

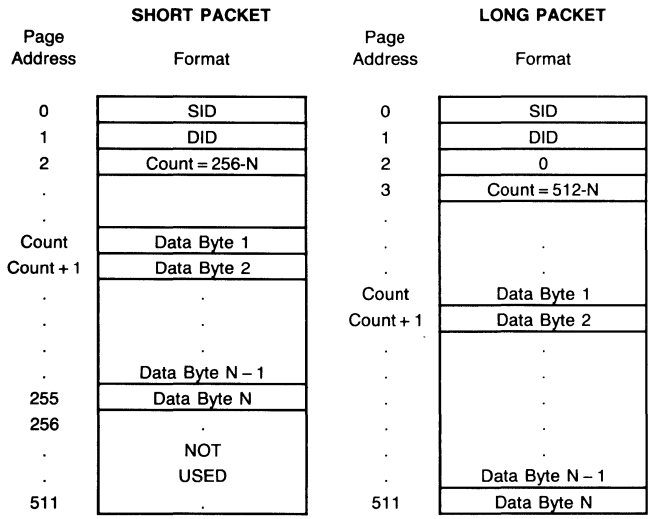
Buffer memory access

Both the processor and the LANC may gain access to the buffer memory; however, the LANC arbitrates processor access to this memory. The LANC circuit delays the X-BUS module acknowledge signal back to the processor to obtain the time necessary to gain access to the buffer.

Processor memory access requests are always serviced within 2.2 microseconds.

Buffer format

The diagram below illustrates the format of the buffers.



N = Data packet length (maximum: 253 of 508)
SID = Source ID
DID = Destination ID (0 for broadcast)

Buffer operation

During a transmit sequence, the LANC fetches data from the transmit buffer section of memory. During a receive sequence, the LANC stores data in the appropriate receive buffer.

Buffer memory address

Buffer memory occupies memory address range 04000 (HEX) to 047FF (HEX) of the 1 megabyte total module memory space allocated by the processor. The following table describes the buffer memory offset address space.

PAGE nn	OFFSET ADDRESS SPACE (HEX)
00	04000 to 041FF
01	04200 to 043FF
10	04400 to 045FF
11	04600 to 047FF

Bootstrap ROM

The NETWORK RIM module can provide up to 16 K bytes of Read Only Memory (ROM). The ROM is to be used as nonvolatile storage of bootstrapping firmware routines. All reads from this memory are by means of 8-bit (byte) transfers. ROM occupies the memory address range between X0000 and X03FFF (HEX).

Note:

This bootstrap ROM is not currently used.

Memory and I/O Address Use

Introduction

The following sections describe the module's:

- X-BUS address lines,
- memory and I/O addresses, and
- status indicators.

X-BUS address lines

The address functions for memory and I/O are described in the following table.

ADDRESS	FUNCTION
XADR17h to XADR14h	These bits are decoded so that any memory operation within the module's 1 MB memory address range is answered by the NETWORK RIM module memory.
XADR13h to XADR10h	Internally decoded, these bits are used for the most significant bits of the module's memory operations.
XADRFh to XADR8h	These bits are decoded so that any I/O operation within the module's 256-I/O address range is answered by the module's I/O logic. During a memory operation, the bits are midmost significant address bits.
XADR7h to XADR0h	Internally decoded, these bits are used for the least significant bits of the module's memory and/or I/O operations.

Submodule I/O addresses

The module's I/O functions occupy the following I/O address segments:

- one module memory register, and
- two LANC registers.

Assignment of the module's 256-I/O address range occurs during module initialization.

I/O functions

The module's I/O functions with their corresponding I/O addresses are shown in the table below.

FUNCTION	OFFSET HEX ADDRESS
Module Memory Register	20
LANC Mask Register (Write)	40
LANC Status Register (Read)	40
LANC Command Register (Write)	41
Reserved (Read)	41

Status indicators

The NETWORK RIM module has two types of status indicators:

- a module ready indicator, and
- an ARCNET local network activity indicator.

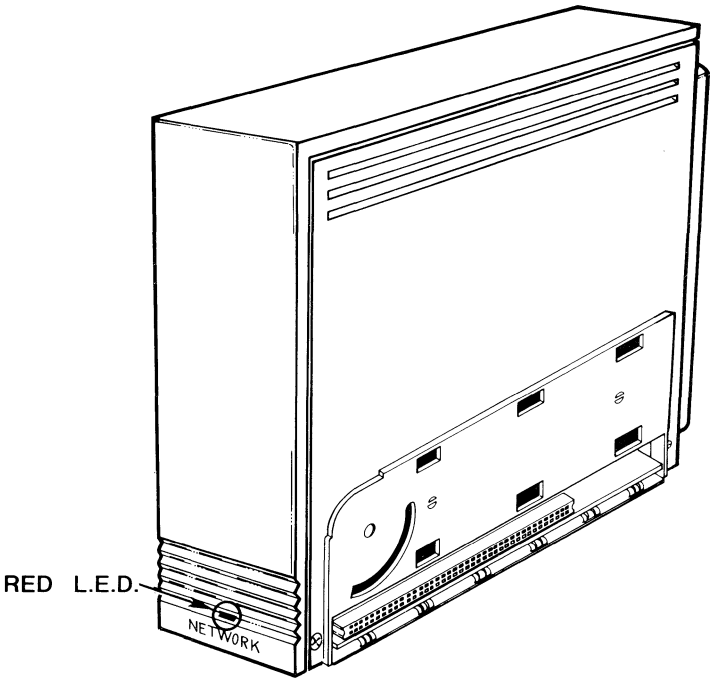
Module ready indicator

The module's front panel contains a ready indicator. The indicator lights after the processor readdresses the module. When illuminated, the light indicates:

- the processor has recognized the presence of the NETWORK RIM module, and
- the module is configured into the 1200 VISTA-PC system.

Ready indicator diagram

The following diagram illustrates the module ready indicator.

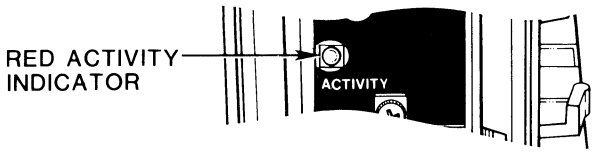


ARCNET activity indicator

The module's rear panel (coaxial connector side) contains the ARCNET local network activity indicator. The indicator lights whenever ARCNET local network activity is detected. The indicator can be used as a maintenance aid for servicing.

Activity indicator diagram

The following diagram illustrates the network activity indicator.



REAR PANEL

Module Initialization

Introduction

The following sections briefly describe module initialization and define each of the module device control register bits.

Stages of initialization

The following table describes the five stages of module initialization.

STAGE	DESCRIPTION
1	An X-BUS initialization command resets all X-BUS modules and breaks the X-BUS connection between adjacent modules; only the module being initialized can respond.
2	The processor writes an I/O address range to X-BUS I/O port 000h (a register in the module).
3	Once the I/O address range is written, the module re-enables the X-BUS connection to the next module and ignores accesses to I/O port 000h allowing the processor to repeat the action for each module.
4	The processor writes a memory address range into the module's memory address register.
5	Each module connected to the X-BUS returns a unique module code which identifies its type. Note: The code can be read only at this time.

Device control register

The definition of each of the module device control register bits is shown below.

ACTIVE HIGH CONTROL BIT	PRESET STATE	FUNCTION
15 14 13 12 11 10 9 8	1 0 0 0 0 0 0 0	Bits 15 to 8 represent the unique Module Type Code. The NETWORK RIM module is 80 HEX.
7	0	Bit 7 indicates that this module is not a video controller.
6	X	Bit 6 indicates whether the module is a bootable device with its own boot ROM; 0 = No ROM, 1 = ROM. Note: Bit 6 is currently set to zero.
5 4	0 0	Bits 5 and 4 specify which DMA channel to use when reading the contents of the module's ROM (Bit 6 = 1). This module does not support DMA transfers.
3 2	0 0	Bits 3 and 2 are reserved for future expansion.
1 0	X X	Bits 1 and 0 represent the Module Version number.

Address/Command Summary

Introduction

The following sections provide a summary of the following registers, commands, and addresses.

- LANC status register,
- LANC interrupt mask register,
- LANC write command summary,
- LANC buffer memory,
- Submodule memory addresses, and
- Submodule I/O addresses.

LANC registers

The following diagram illustrates the LANC status register bit definitions and the LANC interrupt mask register bit definitions.

LANC

LANC STATUS REGISTER BIT DEFINITIONS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RI	SET TO ONE	SET TO ONE	POR	SET TO ZERO	RECON TIMER	TMA	TA

LANC INTERRUPT MASK REGISTER BIT DEFINITIONS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RI	NOT USED	NOT USED	POR (NMI)	NOT USED	RECON	NOT USED	TA

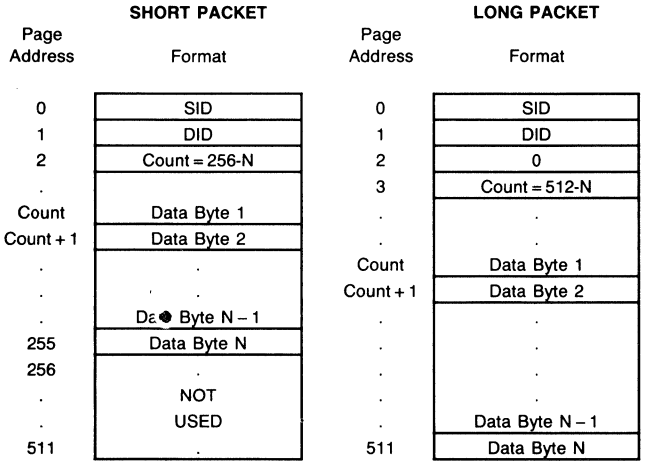
LANC write command summary

The following table summarizes the Local Area Network Controller write commands.

DATA	COMMAND
00000001	Disable Transmitter
00000010	Disable Receiver
000nn011	Enable Transmit From Page nn
b00nn100	Enable Reception to Page nn
0000c101	Define Configuration
000rp110	Clear Flags

Memory data organization

The following diagram illustrates the LANC buffer memory data organization.



N = Data packet length (maximum: 253 or 508)
SID = Source ID
DID = Destination ID (0 for broadcast)

Submodule memory address

The following table summarizes the submodule memory addresses.

FUNCTION	OFFSET HEX ADDRESS
ROM	00000 to 03FFF
Buffer	04000 to 047FF

Submodule I/O addresses

The five submodule I/O addresses are listed in the following table:

FUNCTION	OFFSET HEX ADDRESS
Module memory register	20
LANC mask register (Write)	40
LANC status register (Read)	40
LANC command register (Write)	41
Reserved (Read)	41

Appendix A.
X-BUS PIN DEFINITIONS

Pin Assignments

Pin definition table

PIN	SIGNAL
1	Reserved
2	Reserved
3	GND
4	GND
5	XPWREN-
6	XDACK3-
7	XDRQ3-
8	XDACK2-
9	XDRQ2-
10	XDACK1-
11	GND
12	XDRQ1
13	XDRQ4-
14	XADRF-
15	XADRE-
16	XADRD-
17	GND
18	XADRC-
19	XADRB-
20	XADRA-
21	XADR17-
22	XADR16-
23	GND
24	XADR15-
25	XADR14-
26	XADR13-
27	XADR12-
28	XADR11-
29	GND
30	XADR10-
31	XADR9-
32	XADR8-
33	XADR7-
34	XADR6-
35	GND

PIN	SIGNAL
36	XADR5-
37	XADR4-
38	XADR3-
39	XADR2-
40	XADR1-
41	GND
42	XADR0-
43	(Reserved)
44	XPIN + (XPOUT+)
45	(Reserved)
46	X33KHZSYNC+
47	GND
48	XINTR5-
49	XINTR3-
50	XINTR4-
51	XINTR2-
52	XINTR1-
53	GND
54	XINTR0-
55	XMODE3-
56	(Reserved)
57	XMEMRD-
58	XMEMWR-
59	GND
60	XDMAEN-
61	XMODE2-
62	XDATF-
63	XDATE-
64	XDATD-
65	GND
66	XDATC-
67	XDATB-
68	XDATA-
69	XDAT9-
70	XDAT8-
71	GND
72	XDAT7-
73	XDAT6-
74	XDAT5-
75	XDAT4-
76	XDAT3-
77	GND
78	XDAT2-
79	XDAT1-
80	XDAT0-

PIN	SIGNAL
81	XSPKR-
82	XACK-
83	GND
84	XLOCK-
85	XBHE+
86	XRESET-
87	(Reserved)
88	(Reserved)
89	GND
90	(Reserved)
91	XIOWR-
92	XIORD-
93	XPCLK+
94	GND
95	XDCLK-
96	GND
97	GND
98	GND
99	(Reserved)
100	(Reserved)
101	(Reserved)
102	(Reserved)
103	(Reserved)
104	(Reserved)
105	(Reserved)
106	(Reserved)
107	(Reserved)
108	(Reserved)
109	+36VRTN
110	+36VDC
111	+36VRTN
112	+36VDC
113	+36VRTN
114	+36VDC
115	+36VTRN
116	+36VDC
117	+36VRTN
118	+36VDC
119	+36VRTN
120	+36VDC

Appendix B. ASCII CONVERSIONS

Conversion table

ASCII conversions

DECIMAL	BINARY	OCTAL	HEXADECIMAL	ASCII CHARACTER
0	00000000	000	00	NUL
1	00000001	001	01	SOH
2	00000010	002	02	STX
3	00000011	003	03	ETX
4	00000100	004	04	EOT
5	00000101	005	05	ENQ
6	00000110	006	06	ACK
7	00000111	007	07	BEL
8	00001000	010	08	BS
9	00001001	011	09	HT
10	00001010	012	0A	LF
11	00001011	013	0B	VT
12	00001100	014	0C	FF
13	00001101	015	0D	CR
14	00001110	016	0E	SO
15	00001111	017	0F	SI
16	00010000	020	10	DLE
17	00010001	021	11	DC1
18	00010010	022	12	DC2
19	00010011	023	13	DC3
20	00010100	024	14	DC4
21	00010101	025	15	NAK
22	00010110	026	16	SYN
23	00010111	027	17	ETB
24	00011000	030	18	CAN
25	00011001	031	19	EM

DECIMAL	BINARY	OCTAL	HEXADECIMAL	ASCII CHARACTER
26	00011010	032	1A	SUB
27	00011011	033	1B	ESC
28	00011100	034	1C	FS
29	00011101	035	1D	GS
30	00011110	036	1E	RS
31	00011111	037	1F	US
32	00100000	040	20	SP
33	00100001	041	21	!
34	00100010	042	22	"
35	00100011	043	23	#
36	00100100	044	24	$
37	00100101	045	25	%
38	00100110	046	26	&
39	00100111	047	27	'
40	00101000	050	28	(
41	00101001	051	29	)
42	00101010	052	2A	*
43	00101011	053	2B	+
44	00101100	054	2C	,
45	00101101	055	2D	-
46	00101110	056	2E	.
47	00101111	057	2F	/
48	00110000	060	30	0
49	00110001	061	31	1
50	00110010	062	32	2
51	00110011	063	33	3
52	00110100	064	34	4
53	00110101	065	35	5
54	00110110	066	36	6
55	00110111	067	37	7
56	00111000	070	38	8
57	00111001	071	39	9
58	00111010	072	3A	:
59	00111011	073	3B	;
60	00111100	074	3C	<

Conversion table

DECIMAL	BINARY	OCTAL	HEXADECIMAL	ASCII CHARACTER
61	00111101	075	3D	=
62	00111110	076	3E	>
63	00111111	077	3F	?
64	01000000	100	40	@
65	01000001	101	41	A
66	01000010	102	42	B
67	01000011	103	43	C
68	01000100	104	44	D
69	01000101	105	45	E
70	01000110	106	46	F
71	01000111	107	47	G
72	01001000	110	48	H
73	01001001	111	49	I
74	01001010	112	4A	J
75	01001011	113	4B	K
76	01001100	114	4C	L
77	01001101	115	4D	M
78	01001110	116	4E	N
79	01001111	117	4F	O
80	01010000	120	50	P
81	01010001	121	51	Q
82	01010010	122	52	R
83	01010011	123	53	S
84	01010100	124	54	T
85	01010101	125	55	U
86	01010110	126	56	V
87	01010111	127	57	W
88	01011000	130	58	X
89	01011001	131	59	Y
90	01011010	132	5A	Z
91	01011011	133	5B	[
92	01011100	134	5C	
93	01011101	135	5D	]
94	01011110	136	5E	^
95	01011111	137	5F	-

Conversion table

DECIMAL	BINARY	OCTAL	HEXADECIMAL	ASCII CHARACTER
96	01100000	140	60	
97	01100001	141	61	a
98	01100010	142	62	b
99	01100011	143	63	c
100	01100100	144	64	d
101	01100101	145	65	e
102	01100110	146	66	f
103	01100111	147	67	g
104	01101000	150	68	h
105	01101001	151	69	i
106	01101010	152	6A	j
107	01101011	153	6B	k
108	01101100	154	6C	l
109	01101101	155	6D	m
110	01101110	156	6E	n
111	01101111	157	6F	o
112	01110000	160	70	p
113	01110001	161	71	q
114	01110010	162	72	r
115	01110011	163	73	s
116	01110100	164	74	t
117	01110101	165	75	u
118	01110110	166	76	v
119	01110111	167	77	w
120	01111000	170	78	x
121	01111001	171	79	y
122	01111010	172	7A	z
123	01111011	173	7B	{
124	01111100	174	7C	|
125	01111101	175	7D	}
126	01111110	176	7E	~
127	01111111	177	7F	DEL


DATAPOINT