DDP-516-21

DIRECT MEMORY ACCESS

Option Manual

August 1967

Honeywell

COMPUTER CONTROL
DIVISION

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ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

DDP-516-21
DIRECT MEMORY ACCESS OPTION

INTRODUCTION

This document contains a detailed description of the Direct Memory Access (DMA) option.

Reference Data

Instruction Manual for DDP-516 General Purpose Computer: Volume I, 3C Doc. No. 130071620; Volume II, 3C Doc. No. 130071621; Volume III, 3C Doc. No. 130071622.

Functional Description

The DMA provides a direct, high-speed path for an external device to computer memory for up to four channels. The DMA word-transfer-rate approaches $0.9 \mu s$ and is capable of addressing up to 32K of memory.

To effect a transfer, the DMA causes computer breaks between cycles without regard to end of instruction. The initiation and termination of the DMA cycle is controlled by the external device request lines.

INSTALLATION

The DMA is contained in two bays, one of which is the main frame (unit A). The DMA logic in the main-frame bay is located in fixed positions as shown on LBD No. 248. The DMA logic external to the main frame is a relocatable 2 x 3 BLOC, whose PAC allocations are shown on LBD No. 249. DMA cable No. 1 transfers the address counter lines (ACTXX) to the CPU Y-register.

INSTRUCTION COMPLEMENT

DMA instructions are for loading the address and range counters and for reading the contents of the range counters.

Load Address Counter Channel 1, SMK '0124

This instruction has the following function:

$$(0) \rightarrow (AC1)_{1-16} \quad \Big| \quad (A)_{1-16} \rightarrow (AC1)_{1-16} \quad \Big| \quad (0) \rightarrow (RC1)_{1-16}$$

The contents of A are the address of the memory location to be accessed by the first DMA cycle for channel 1. Note that the load-address instruction clears the range counter and should therefore precede the load-range instruction.

Load Address Counter Channel 2, SMK '0224

This instruction is the same as SMK '0124 except that it is for Channel 2.

Load Address Counter Channel 3, SMK '0324

This instruction is the same as SMK '0124 except that it is for Channel 3.

Load Address Counter Channel 4, SMK '0424

This instruction is the same as SMK '0124 except that it is for Channel 4.

Load Range Counter Channel 1, SMK '1124

This instruction has the following function:

$$(A)_{2-16} \rightarrow (RC1)_{2-16}$$

The contents of A are the two's complement of the number of transfers to be accomplished. Note that RC must be cleared previously by an SMK '0X24 (load address counter) instruction so that the transfer count is not altered when loaded into the range counter. (Essentially, the contents of A are inclusively-ORed with the contents of RC.)

Load Range Counter Channel 2, SMK '1224

This instruction is the same as SMK '1124 except that it is for Channel 2.

Load Range Counter Channel 3, SMK '1324

This instruction is the same as SMK '1124 except that it is for Channel 3.

Load Range Counter Channel 4, SMK '1424

This instruction is the same as SMK '1124 except that it is for Channel 4.

Read Range Counter Channel 1, INA '1124

This instruction functions as follows.

If (RC) = 0: NOP and execute next sequential instruction

If (RC) ≠ 0: $(0) \rightarrow (A)$ │ $(RC) \rightarrow (A)$ │ skip next sequential instruction

Read Range Counter Channel 2, INA '1224

Instruction INA '1224 is the same as INA '1124 except that INA '1224 is for Channel 2.

Read Range Counter Channel 3, INA '1324

Instruction INA '1324 is the same as INA '1124 except that INA '1324 is for Channel 3.

Read Range Counter Channel 4, INA '1424

Instruction INA '1424 is the same as INA '1124 except that INA '1424 is for Channel 4.

THEORY OF OPERATION

Functional Areas (See Figure 1)

Control Logic. -- The DMA control logic (LBD No. 241) contains the priority network (PN) for determining the priority of the active DMA requests (DILAX) and the logic for initiating and controlling the DMA cycle.

Timing Level Generator. -- The DMA Timing Level Generator (LBD No. 240) generates the various timing levels required for a DMA cycle. A DMA request (DMARQ) enables the CPU master clock oscillator outputs MCSET, MCRST, and MTLG, to trigger the DMA timing level flip-flops. There are five of these flip-flops: TLAFF, TLBFF, TLCFF, TLDFF, and TLEFF. See Figure 2 which shows the level sequence if only one DMA cycle is required. The transition from one level to the next is controlled by the TACFF, TBCFF, and SAMIN flip-flops. Note that the TL4FF flip-flop (LBD No. 118) is inhibited while the DMA timing level generator is enabled.

If two or more DMA cycles occur in succession, timing levels TLA and TLE occur simultaneously except at the beginning of the first cycle when only TLA is generated and the end of the last cycle when only TLE is generated. The levels for two or more successive DMA cycles are generated as shown below.

Start DMA														End DMA
TL3	TLA	TLB	TLC	TLD	TLE· TLA	TLB	TLC	TLD	TLE· TLA	TLB	TLC	TLD	TLE	TL4

Repeat N Times

3
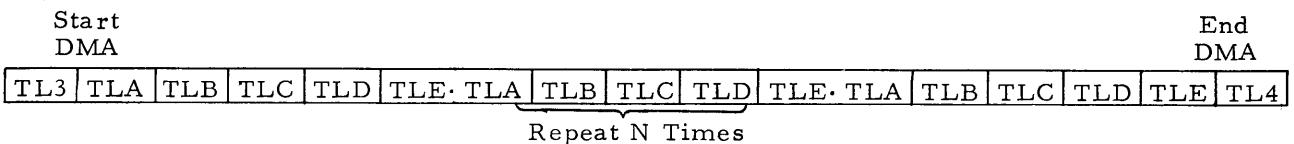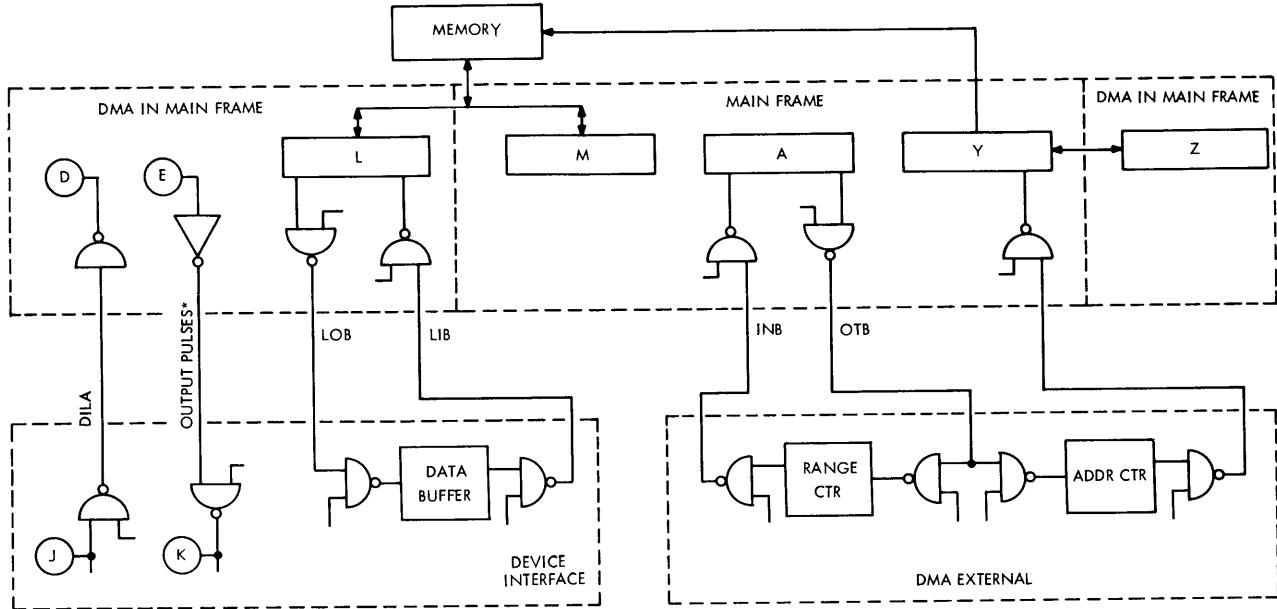
Figure 1. CPU/DMA/External Device Interface Block Diagram

L-Register. -- The L-register (LBDs No. 242 and 243) is the memory buffer register. All transfers to and from memory occur through the L-register.

Z-Register. -- The Z-register (LBD No. 244) provides storage for the contents of the Y-register during the DMA cycle while the DMA is using the Y-register.

Address Counter (AC). -- Each channel has a 16-bit address counter (LBDs No. 251, 253, 255) which stores DMA cycle starting address and the read/write control bit. The highest order bit (bit 1) position of AC stores the read/write control. A ONE specifies a write cycle (input mode) and a ZERO specifies a read cycle (output mode). The address contents of AC (bits 2 through 16) are incremented once each cycle to provide the address for the next cycle.

Range Counter (RC). -- Each channel has a 16-bit range counter (LBDs No. 252, 254, 256) which stores the two's complement of the number of transfers to take place. The contents of RC are incremented once each cycle. When RC equals all ONEs an end of range signal (ERCHX) is delivered to the external device signifying that the required number of transfers has been accomplished.
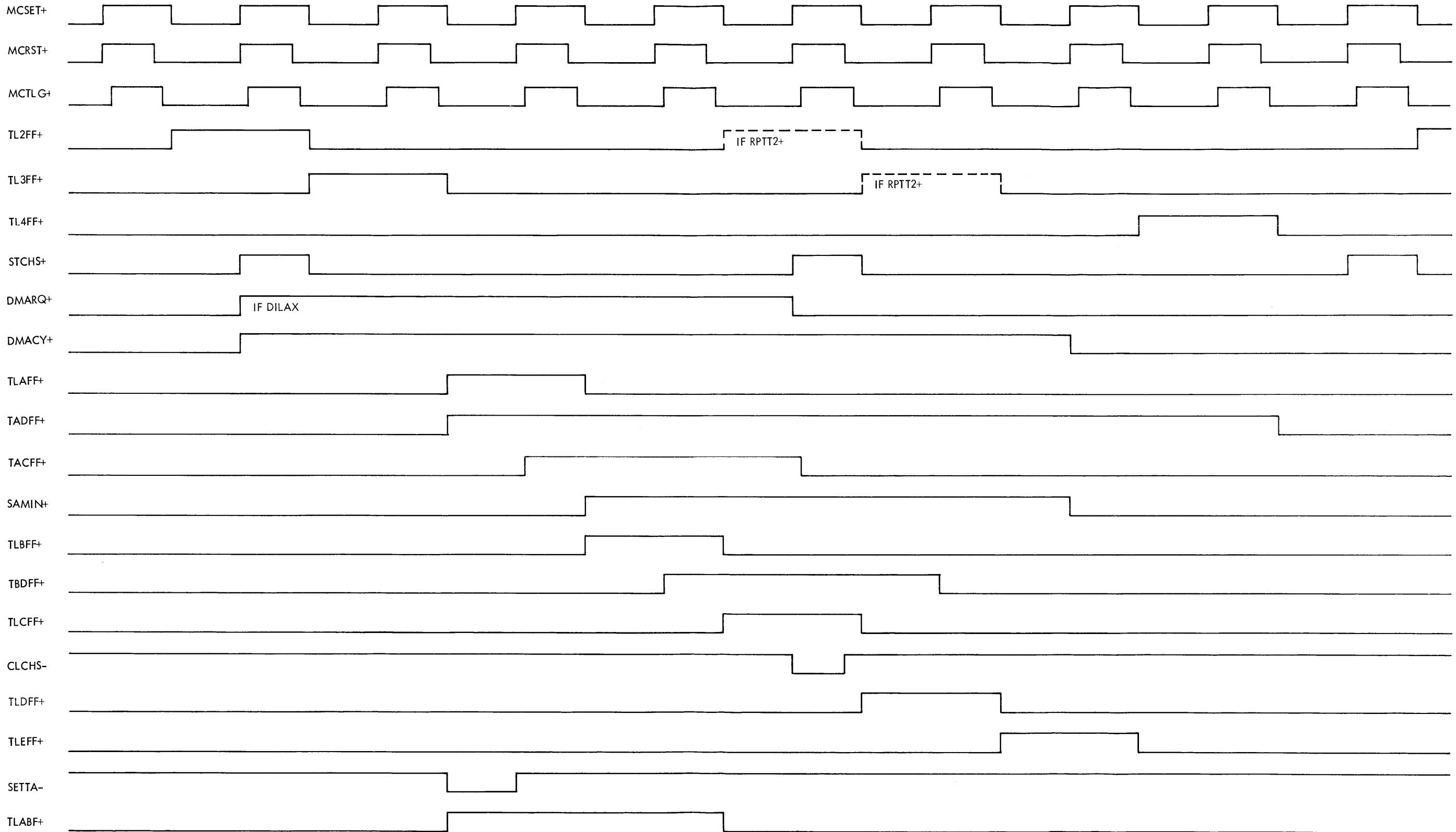
Figure 2. Timing Levels and Primary Control
Signals for One DMA Cycle

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SMK and INA Instruction Logic

For SMK load AC or RC instruction, the address bus lines (ADBXX) are sent to a decoder (LBD No. 250-B9). The decoder outputs (OTPAX or OTPRX) specify a particular address counter (AC) or range counter (RC). Note that a load AC SMK instruction should be executed before a load RC for the same channel because the load AC SMK clears both the AC and RC. The load RC SMK clears neither of these counters. For example, when a load AC SMK '0X24 is executed, the decoder output OTPAX is gated with CMKXX (LBD No. 134-K7) to generate CLARX (LBDs No. 251, 253, 255-D10). CLARX clears the AC and RC for that channel. On the trailing edge of CMKXX, the OTPAX flip-flop (LBDs No. 251, 253, 255-G11) is set to gate the output bus (OTBXX) onto the SAXXX lines. The SAXXX lines then set the AC stages. At the end of the instruction, when signal SMKXX goes false, the OTPAX flip-flop is DC reset, thereby preventing the OTBXX lines from affecting the counter. For a load RC instruction (for example SMK '1X24), an OTPRX decoder output enables the OTBXX lines to the proper range counter.

An INA instruction is decoded by a gate (LBDs No. 252, 254, 256-D11) whose output enables the contents of RC (RCXXX) to the input bus (INBXX). The INA also enables ERLAX (indicates RC contains all ZEROs) to generate DRLIN. The state of DRLIN determines whether the INA is to be treated as a NOP or the contents of RC are transferred to the A-register and the next sequential instruction is to be skipped.

DMA Cycle

For a detailed DMA cycle description, see DMA cycle flow chart (Figure 3) and flow chart analysis. The DMA logic is shown on LBDs No. 240 through 245 and 248 through 259. DMA-external-device timing is shown in Figure 4. The DMA mnemonics are defined in the function index list.

A DMA cycle is activated by an external device request. The priority network (PN) logic determines the request priority and enables the proper channel logic. The DMA cycle begins at the trailing edge of TL3. It inhibits TL4 and begins generation of its own timing signals. Every TL1 the contents of Y are transferred to Z for preservation in case of a DMA cycle. The DMA cycle starts a memory cycle which is a read or write cycle depending on the state of the DMAWR flip-flop. The Y-register is cleared and the contents of address counter (AC) representing the address to be accessed in the first DMA cycle are placed in Y. AC is then incremented to form the address for the next DMA cycle. For a read cycle, the contents of the addressed memory location are inhibited from the M-register and placed in the L-register. The L-register is then transferred to the LOBXX lines and from thence to the external device. For a write cycle, the external device data is transferred from the external device to the L-register via the LIBXX lines and from the L-register to the addressed memory location.

If end of range (RC equals all ONEs) is reached, the external device disables its request line and transfers for this channel are terminated. The contents of RC are then incremented. The DMA again searches its request lines. If any are active, it causes another DMA cycle. If no requests exist, the DMA returns control to the CPU and enables TL4.
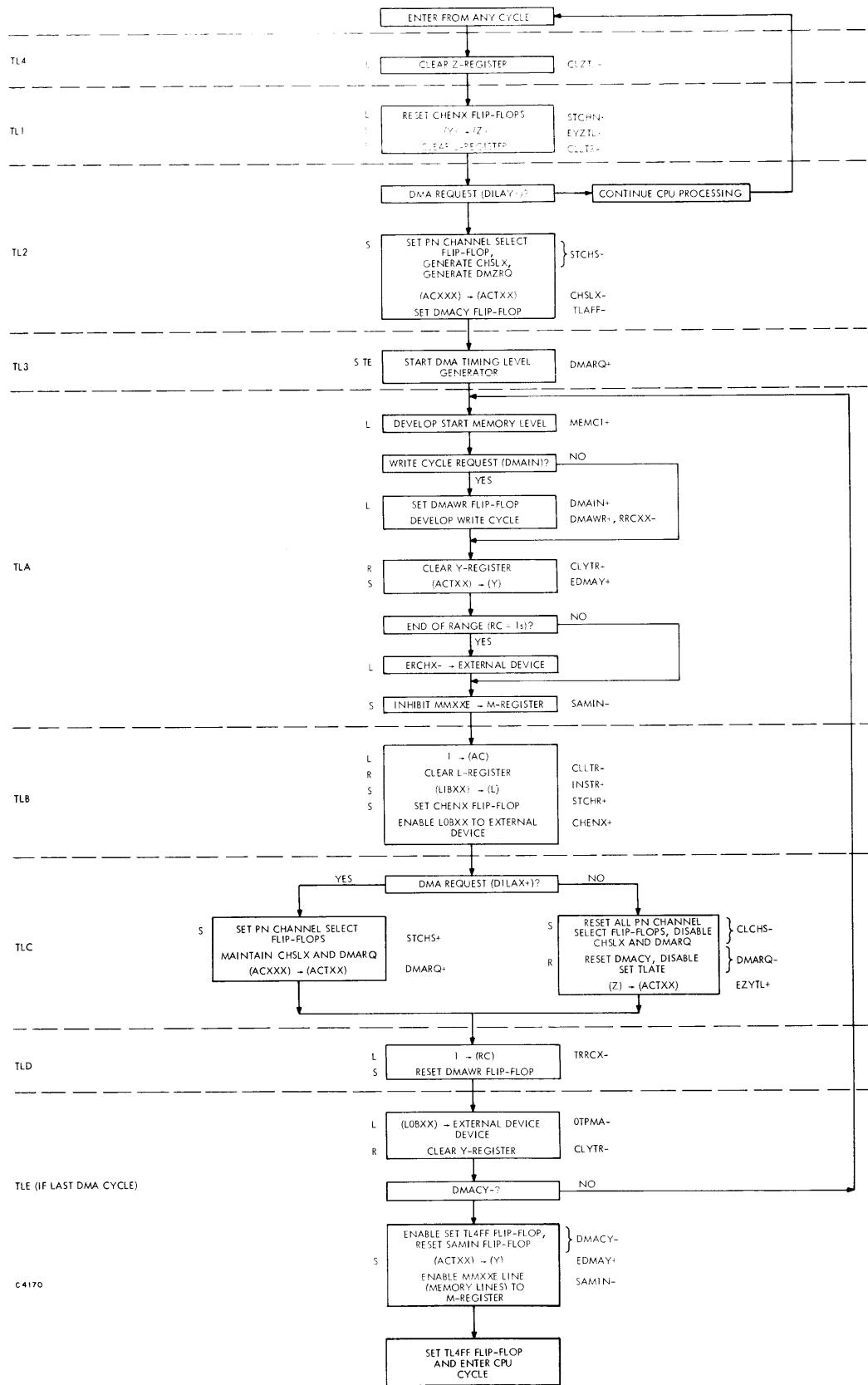
Figure 3. DMA Cycle Flow Chart
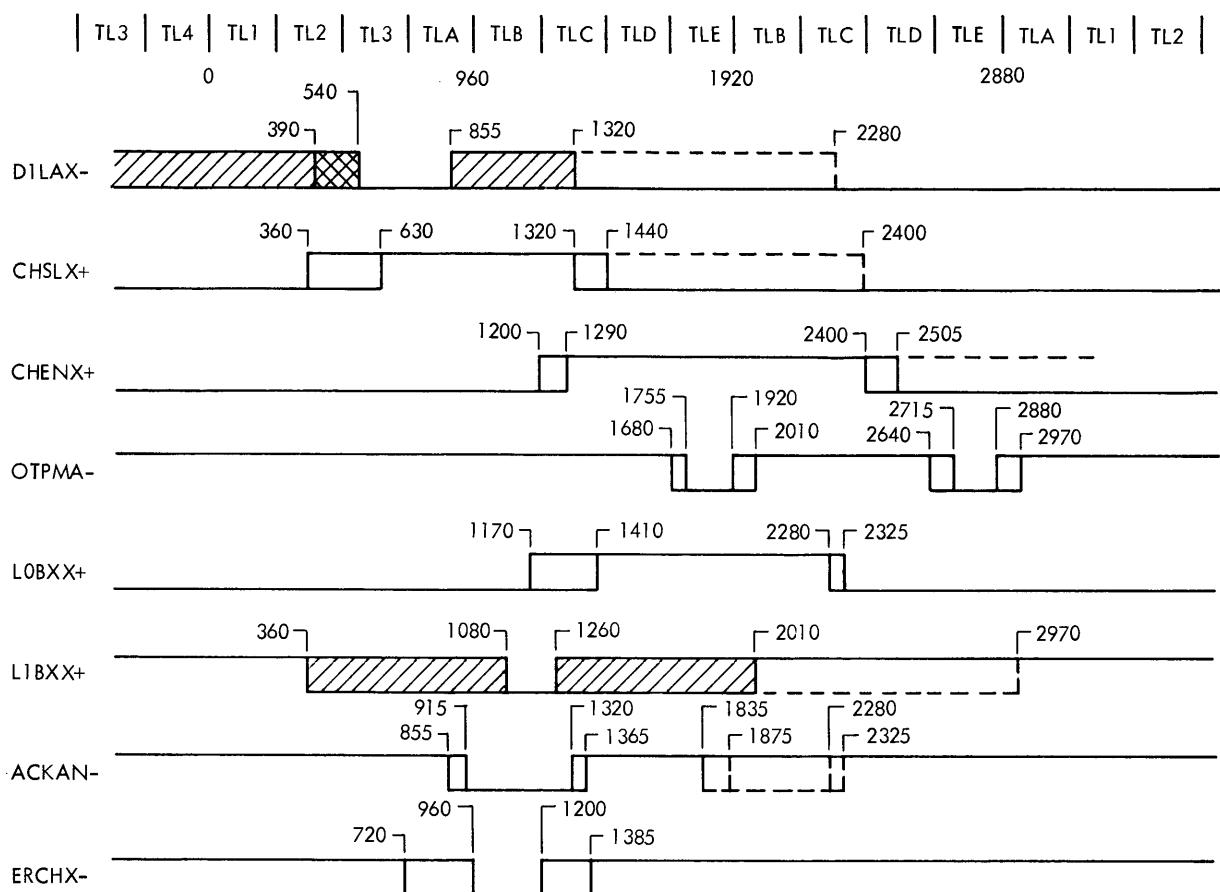
Figure 4. DMA/External Device Interface Timing

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
CLZTL-	241-L5	CPU	TL4	L	(TL4FF+)	241-L5	244-A3/D2/ F3/J2	Clears Z-register
STCHN+	241-L1	CPU	TL1	L	(TL1FF+)	241-L1	241-A7/A9/ C7/C9	Resets CHENX flip-flops
EYZTL+	241-L6	CPU	TL1	L	(TL1FF+)	241-L6	244-A3/C2/ F2/J1	Gate contents of Y-register to Z-register
CLLTR-	241-L10	CPU	TL1	R	(HOLDM-)(TL1FF+) (MCRST+)	241-G10	242-C11/K11 and 243-C11/K11	Clears L-register
D1LAX	External device						241-A1/A2/ A3/A4	DMA cycle request lines from external device to DMA PN
STCHS+	241-J6	CPU	TL2	S	(TL2FF+)(MCSET+)	241-G6	241-A3	Set PN channel select flip-flops associated with active D1LAX lines
CHSLX-	241-C2/ C3/C4				PN channel select flip-flop set	241-G6	241-B2/B3/ B4	Enables setting of associated channel enable flip-flop (CHENX)
							251-H1/K1 253-H1/K1 255-H1/K1	Gate ACXXX lines to ACTXX lines
							257-B3/ D3/F3	Enables associated end of range signal ERCH-
							External device	Enables external device to gate data onto L1BXX lines
DMARQ+	241-C4				PN channel select flip-flop set	241-B2/ B3/B4	240-D11	Enables setting of TLAFF flip-flop thus enabling the starting of DMA timing level generator
							241-J7	Disables EZYTL+
DMARQ-	241-C4				PN channel select flip-flop set	241-B2/ B3/B4	241-F2	Generates DMCYQ-
DMACY+	241-L7				(TLAFF+)	241-L7	118-E5 240-H3 241-F2	Holds TL4FF reset Enables SAM1N-A Generates DMCYQ-
SETTA-	240-G11	CPU	TL3	S	(DMARQ+)(TL23F-)(TL24F+) (TACFF-)(TBCFF-) (MCSET-)	240-D10	118-G6	Resets TL3FF flip-flop
MEMC1+	126-J11	DMA	TLA	L	(TLAFF-)	126-J11	150-C1	Start memory cycle
MEMC1+B	149-J10	DMA	TLA	L	(TLAFF-)	149-J10	142-G10	Start memory cycle
DMAWR+	241-G8	DMA	TLA	L	(DMA1N+)(TLAFF+)	241-E7	126-G10	Causes write cycle (disables RRCXX)
CLYTR-	129-J3	DMA	TLA	R	(TLAFF+)(MCRST+)	129-F3/ H3	101---116-L11	Clears Y-register
EDMAY+	241-L3/L4	DMA	TLA	S	(TLAFF+)(MCSET+)	241-G3/ J3	101---116-F10	Gates ACTXX lines to Y-register
ERCHX-	257-B3/ D3/F3	DMA	TLAB	L	(CHSLX+)(RCX01+ through RCX16+)(TLABF+)	257-A/ D/F	External device	End of range signal. Disables external device D1LAX+ signal
DMCYQ-	241-G2				(DMARQ+) (DMACY+)	241-F2	118-F5	Inhibits TL4FF

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
SAMIN+	240-H3	DMA	TAC	S	(TACFF+)(TBDFF-) (MCSET-)	240-D9	240-D2 242/243-B3/ G3	Enables setting of TLEFF flip-flop. Inhibits MMXXE lines (contents of accessed memory location) from M-register
TR1GX-	250-D1/ D2/D3	DMA	TLB	L	(CHSLX+)(TLBFF+)	250-D1/ D2/D3	251-F1, 253-F1, 255-F1	Increments contents of associated Address Counter by one
CLLTR-	241-L10	DMA	TLB	R	(TLBFF+)(MCRST+)	241-J10/ L10	242-C11/K11 and 243-C11/ K11	Clears L-register
1NSTR+	241-L2	DMA	TLB	S	(TLBFF+)(MCSET+)	241-J2	242-A1/G1 and 243-A1/ G1	Strobes contents of L1BXX lines into L-register
STCHN+	241-L1	DMA	TLB	S	(TLBFF+)(MCSET+)	241-J2	241-A7/A9/ C7/C9	Sets selected CHENX flip-flop and resets non-selected CHENX flip-flop
CHENX+	241-A7/ A9/C7/ C9				(CHSLX+)(STCHN+)	241-A7/ A9/C7/ C9	252,254,256- F10 External device	Enables TRRCX-. Enables external device to receive data from L0BXX lines
STCHS+	241-J6	DMA	TLC	S	(TLCFF+)(MCSET+)	241-G5	241-A3	Sets PN channel select flip-flops whose D1LAX lines are active. A set PN flip-flop generates CHSLX-, DMARQ+, and holds DMACY set to cause another DMA cycle immediately following the present DMA cycle
CLCHS-	241-J5	DMA	TLC	R	(TLCFF+)(MCRST+)	241-J5	241-A4	Resets PN channel select flip-flops whose D1LAX lines are not active. If all PN flip-flops are reset, CHSLX- and DMARQ are disabled and the resetting of DMACY is enabled
DMARQ-	241-C5				(D1LA1-)(D1LA2-)(D1LA3-) (D1LA4-)(CLCHS)	241-A2/ A3/A4	240-D1/ 241-J7	Disables TLAFF flip-flop. Generates EZYTL+
EZYTL+	241-J7				(DMARQ-)	241-J7	244-B2/ D1/H2/ J1	Gates contents of Z-register to ACTXX lines
TRRCX-	252, 254, 256- F10	DMA	TLD	L	(CHENX+)(TLDFF+)	252, 254, 256- F10	252,254, 256-F1	Increment range counter by one
DMAWR-	241-G9	DMA	TLD	S	(TLDFF+)(MCSET+)	241-E9	126-G10	Enables RRCXX

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
OTPMA-	240-H7	DMA	TLE	L	(TLEFF+)	240-H7	External device	Enables device to transfer contents of L0BXX lines into its buffer register
CLYTR-	129-J3	DMA	TLE	R	(TLEFF+)(MCRST+)	129-F3/ H3	101---116- L11	Clears Y-register
DMACY-	241-L8	DMA	TLE	R	(TLAFF-)(TLEFF+) (MCRST+)	241-J8	118-E5 240-H3	Enables TL4FF flip-flop. Resets SAM1N flip-flop
EDMAY+	241- L3/ L4	DMA	TLE	S	(TLEFF+)(MCSET+)	241-G3/ J3	101---116- F10	Gates ACTXX lines to Y-register
SAMIN-	240-H4				(DMACY-)	240-H3	242/243- B3/G3	Enables MMXXE lines to M-register

PARTS LIST

Table 1 contains the parts list for the items located in both the main frame and option drawer.

The A1 prefix reference designation is permanently assigned to the main frame and will not be reassigned. The XX prefix reference designation is for reference only and will be reassigned accordingly to each option drawer of a system's configuration.

Component parts for the μ-PAC Digital Modules, unless otherwise indicated, will be found on the data sheets included in 3C Doc. No. 130071620, Instruction Manual, DDP-516 General Purpose Computer, Vol. I, Theory of Operation and Maintenance.

LOGIC BLOCK DIAGRAMS

The logic block diagrams for the DDP-516-21 Direct Memory Access Option follow the parts list.

Refer to Table 2 for a list of signal mnemonics.

Table 1.
DDP-516-21 DMA Option Parts List

Reference Designation	Description	3C Part No.	Quantity Required
	The following items are located in the Main Frame logic drawer, A1-Unit, and are required for all DMA configurations.		
A1D11	μ-PAC DIGITAL MODULE--priority	Model CC-044	1
A1D12,13	μ-PAC DIGITAL MODULE--NAND power amplifier type II	Model CC-073	2
A1D14 A1F41,42,44, 45,46,47 A1F56 A1F63,64,65, 67,68	μ-PAC DIGITAL MODULE--NAND power amplifier type I	Model CC-045	13
A1E18, A1D18	μ-PAC DIGITAL MODULE--termination PAC	Model CC-154	2
A1D15 A1E11,12 A1F12,13,14, 15,16	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	8
A1D16,17 A1D33	μ-PAC DIGITAL MODULE--NAND gate type I	Model DI-335	3
A1D56	μ-PAC DIGITAL MODULE--parallel transfer gate	Model CM-022	1
A1E13,14,15, 17 A1F17	μ-PAC DIGITAL MODULE--power inverter	Model PA-336	5
A1E16	μ-PAC DIGITAL MODULE--gated flip-flop	Model CC-089	1

Table 1. (Cont)
DDP-516-21 DMA Option Parts List

Reference Designation	Description	3C Part No.	Total Qty Req. for Channels:		
			1	2	3

	The following items are located in an option drawer; reference designations applicable to each channel are indicated as follows:
	
	    1st Channel --- No marking
	    2nd Channel --- Marked*
	    3rd Channel --- Marked #				

XXA11#,12#, 13#,14# XXB12*,13* XXB26,27 XXC12*,13* XXC26,27	μ-PAC DIGITAL MODULE--fast carry counter	Model CC-091	4	8	12
XXA15# XXB15* XXB23 XXC14*,23	μ-PAC DIGITAL MODULE--transfer gate PAC	Model CC-152	3	4	5
XXA17	μ-PAC DIGITAL MODULE--parallel transfer gate	Model CM-022	-	-	1
XXA16# XXB14*,17#,18 XXB22,24,25 XXC16*,17*,18 XXC22,25	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	7	10	12
XXA18# XXA22,23*	μ-PAC DIGITAL MODULE--multi-input NAND gate	Model DC-335	1	2	3
XXB16# XXC15* XXC24	μ-PAC DIGITAL MODULE--power inverter	Model PA-336	1	2	3
XXB21	μ-PAC DIGITAL MODULE--octal/decimal decoder	Model OD-335	1	1	1
XXA25	μ-PAC DIGITAL MODULE--NAND gate Type II	Model DL-335	1	1	1
XXA24	μ-PAC DIGITAL MODULE--gated flip-flop	Model CC-089	1	1	1
XXA/B/C1 XXA/B/C2	CONNECTOR PLANE ASSY--c/o 2 x 3 module (6 blocks of 8 connectors each), framework and associated parts; factory repairable only		1	1	1
	CABLE ASSY--interconnecting cable assemblies will be specified by each system configuration		AR	AR	AR

Table 2.
Function Index

Mnemonic	LBD/Grid	Description
OTPAX	250-B8	Output address pulse. Gates starting address on OTBXX to address counter.
OTPMA	240-H7	Output pulse used to strobe LOB into external device buffer register.
OTPRX	250-B9	Output range pulse. Gates two's complement of number of transfers on OTBXX lines to range counter.
INSTR	241-L2	Input strobe. Gates LIBXX lines to L-register.
ACXXX	251-J/L 253-J/L 255-J/L	Address counter output lines.
ACKAX	241-C3	Acknowledge DILAX lines.
ACTXX	244, 251, 253, 255	Address count transfer lines 1 through 16 from Z register or address counter to Y-register.
ADQ24	250-G11	Address ;equals 24 control signals.
CHENX	241-A8/C8	Channel enable flip-flops. Enables output bus lines (LOBXX) to external device.
CHSLX	241-C3	Channel select signal used to set associated channel enable (CHENX) flip-flop. Also enables external device to gate data onto the input bus lines LIBXX.
CLCHS		Clear channel select flip-flops (in priority network).
CLLTR	241-L10	Clear L-register signal.
CLZTL	241-L5	Clear Z-register signal.
DILAX	241-A3	Data interrupt lines from external device to request DMA cycle.
DMACY	241-L7	DMA cycle control signal.
DMARQ	241-C5	DMA cycle request signal. Occurs when an active request (DILAX) has been sampled.
DMAWR	241-G8	DMA write/read control flip-flop.
DMCYQ	241-G2	DMA cycle request signal for main frame.
EDMAY	241-L3	Enable DMA address counter lines to Y-register.
ERCHX		End of range signal to external device.
ERLAX		End of range signal for "INA" instruction.
EYZTL	241-L6	Enable Y-register to Z-register transfer signal.

Table 2. (Cont)
Function Index

Mnemonic	LBD/Grid	Description
EZYTL	241-J7	Enable Z-register to Y-register transfer signal.
LIBXX	242-243	L-register input bus lines. Data from external device.
LXXFF	242-243	L-register flip-flops.
MMXXE	242-243	Memory output lines to M-register.
RCXXX	252-G 254-G 256-G	Range counter output lines.
SAXXX	251-C/D 253-C/D 255-C/D	Set address counter lines.
SAMIN	240-H3	Sense amplifier to M-register inhibit signal.
SETTA	240-G11	Set TLAFF flip-flop signal.
SRXXX	252-B/D 254-B/D 256-B/D	Set range counter lines.
STCHN	241-L1	Set channel enable flip-flop.
STCHS	241-J6	Set channel select flip-flop (priority network flip-flop).
TACFF	240-C6	Timing level A through timing level C flip-flop.
TADFF	240-A2	Timing level A through timing level D flip-flop.
TBDFF	240-C9	Timing level B through timing level D flip-flop.
TLAFF	240-G10	Timing level A flip-flop (first DMA timing level).
TLBFF	240-G9	Timing level B flip-flop (second DMA timing level).
TLCFF	240-G7	Timing level C flip-flop (third DMA timing level).
TLDFF	240-G4	Timing level D flip-flop (fourth DMA timing level).
TLEFF	240-G2	Timing level E flip-flop (fifth DMA timing level). When set, remains set until CPU timing level TL4 is generated.
TRIGX	250-D2	Increments address counter contents by one.
TRRCX	252, 254 256-F10	Increments range counter by one.
ZXXFF	244	Z-register flip-flops.

DMA TIMING LEVEL GEN.

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HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

	REV.	REVISIONS	CHK.
	C	ECO 4237	
		REDRAWN, NO CHG	
	D	ECO 4464	
		EXT CHANGES	
		SEE ECO	
		8/2/67	

TITLE
DDP-516-21
DMA CONTROL

DR. A. Kurtzer   DATE 1/18/67
ENG. J. Grindleman 1-20-67
APP. GCHendrie   1-20-67
PROJECT NO. 55215

SIZE C   DWG NO. 016358   REV. D

21

A   B   C   D   E   F   G   H   J   K   L

AIF16
[245] LIBO1 —
AIF16
[101] EDMO1 —
AIF42
LO1FF +
TG-335
AIF41
[142] MMO1A —
[142] MMO1B —
[142] MMO1C —
[142] MMO1D —
[241] INSTR +
CC-045
LO1FF —
AIF42
MMO1X +
CC-045
AIE14
[240] SAMIN—A
AIF41
MMO1E —
CC-045
AIF43
LOBO1+
CC-073
CC-153

AIF16
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AIF16
[102] EDMO2 —
AIF44
LO2FF +
TG-335
TG-335
AIF41
[142] MMO2A —
[142] MMO2B —
[142] MMO2C —
[142] MMO2D —
CC-045
LO2FF —
AIF44
MMO2X +
CC-045
AIE14
AIF41
MMO2E —
CC-045
AIF43
LOBO2+
CC-073
CC-153

AIF16
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AIF16
[103] EDMO3 —
AIF44
LO3FF +
TG-335
TG-335
AIF41
[142] MMO3A —
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[142] MMO3C —
[142] MMO3D —
CC-045
LO3FF —
AIF44
MMO3X +
CC-045
AIE15
AIF41
MMO3E —
CC-045
AIF43
LOBO3+
CC-073
CC-153

AIF16
[245] LIBO4 —
AIF16
[104] EDMO4 —
AIF44
LO4FF +
TG-335
TG-335
AIF45
[142] MMO4A —
[142] MMO4B —
[142] MMO4C —
[142] MMO4D —
CC-045
LO4FF —
AIF44
MMO4X +
CC-045
AIE15
AIF45
MMO4E —
CC-045
AIF43
LOBO4+
[142] CLMMP —
[241] CLLTR — B
CC-073
CC-153

AIF16
[245] LIBO5 —
AIF16
[105] EDMO5 —
AIF46
LO5FF +
TG-335
AIF45
[142] MMO5A —
[142] MMO5B —
[142] MMO5C —
[142] MMO5D —
[241] INSTR +
CC-045
LO5FF —
AIF46
MMO5X +
CC-045
AIE15
[240] SAMIN—A
AIF45
MMO5E —
CC-045
AIF43
LOBO5+
CC-073
CC-153

AIF16
[245] LIBO6 —
AIF16
[106] EDMO6 —
AIF46
LO6FF +
TG-335
TG-335
AIF45
[142] MMO6A —
[142] MMO6B —
[142] MMO6C —
[142] MMO6D —
CC-045
LO6FF —
AIF46
MMO6X +
CC-045
AIE15
AIF45
MMO6E —
CC-045
AIF43
LOBO6+
CC-073
CC-153

AIF15
[245] LIBO7 —
AIF16
[107] EDMO7 —
AIF46
LO7FF +
TG-335
TG-335
AIF47
[142] MMO7A —
[142] MMO7B —
[142] MMO7C —
[142] MMO7D —
CC-045
LO7FF —
AIF46
MMO7X +
CC-045
AIE15
AIF47
MMO7E —
CC-045
AIF62
LOBO7+
CC-073
CC-153

AIF15
[245] LIBO8 —
AIF16
[108] EDMO8 —
AIF63
LO8FF +
TG-335
TG-335
AIF47
[142] MMO8A —
[142] MMO8B —
[142] MMO8C —
[142] MMO8D —
CC-045
LO8FF —
AIF63
MMO8X +
CC-045
AIE15
AIF47
MMO8E —
CC-045
AIF62
LOBO8+
[142] CLMMP —
[241] CLLTR — B
CC-073
CC-153

1 2 3 4 5 6 7 8 9 10 11

A   B   C   D   E   F   G   H   J   K   L

[245] LIB09 −   AIFI5   AIFI5   AIF63   [109] EDM09 −   L09FF +   L09FF −
[241] INSTR +
[142] MM09A   AIF56   MM09X +   AIF63   AIF62   AIE13   LOB09+
[142] MM09B
[142] MM09C
[142] MM09D
[240] SAMIN −C   AIF56   MM09E −

[245] LIB10 −   AIFI5   AIFI5   [110] EDM10 −   AIF63   L10FF +   L10FF −
[142] MM10A   AIF56   MM10X +   AIF63   AIF62   AIE13   LOB10+
[142] MM10B
[142] MM10C
[142] MM10D   AIF56   MM10E −

[245] LIB11 −   AIFI5   AIFI5   [111] EDM11 −   AIF65   L11FF +   L11FF −
[142] MM11A   AIF64   MM11X +   AIF65   AIF66   AIE13   LOB11+
[142] MM11B
[142] MM11C
[142] MM11D   AIF64   MM11E −

[245] LIB12 −   AIFI5   AIFI5   [112] EDM12 −   AIF65   L12FF +   L12FF −
[142] MM12A   AIF64   MM12X +   AIF65   AIF66   AIE13   LOB12+
[142] MM12B
[142] MM12C
[142] MM12D   AIF64   MM12E −   [142] CLMMP −   [241] CLLTR − D

[245] LIB13 −   AIFI4   AIFI5   [113] EDM13 −   AIF65   L13FF +   L13FF −
[241] INSTR +
[142] MM13A   AIF64   MM13X +   AIF65   AIF66   AIE13   LOB13+
[142] MM13B
[142] MM13C
[142] MM13D
[240] SAMIN −C   AIF64   MM13E −

[245] LIB14 −   AIFI4   AIFI5   [114] EDM14 −   AIF67   L14FF +   L14FF −
[142] MM14A   AIF68   MM14X +   AIF67   AIF66   AIE13   LOB14+
[142] MM14B
[142] MM14C
[142] MM14D   AIF68   MM14E −

[245] LIB15 −   AIFI4   AIFI5   [115] EDM15 −   AIF67   L15FF +   L15FF −
[142] MM15A   AIF68   MM15X +   AIF67   AIF66   AIE14   LOB15+
[142] MM15B
[142] MM15C
[142] MM15D   AIF68   MM15E −

[245] LIB16 −   AIFI4   AIFI5   [116] EDM16 −   AIF67   L16FF +   L16FF −
[142] MM16A   AIF68   MM16X +   AIF67   AIF66   AIE14   LOB16+
[142] MM16B
[142] MM16C
[142] MM16D   AIF68   MM16E −   [142] CLMMP −   [241] CLLTR − D

1 2 3 4 5 6 7 8 9 10 11

25

HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

TITLE
DDP-516-21
DMA Z REGISTER

DR. A. Kurtzer   DATE 1/18/67
ENG.
APP.
PROJECT NO. 55215

SIZE DWG NO.
C   016361

REV.
B

NOTES:

REVISIONS
ECO 4237 2.28.67

A1E25
CC-043
BUS TERMINATIONS

L1B01- — 13	14 — L1B09-
L1B02- — 15	16 — L1B10-
L1B03- — 17	18 — L1B11-
L1B04- — 19	20 — L1B12-
L1B05- — 21	22 — L1B13-
L1B06- — 23	24 — L1B14-
L1B07- — 25	26 — L1B15-
L1B08- — 27	28 — L1B16-

A1D18

[242] LOBO1+	1	2	L1B01- [*]
[*] L1BO2-	3	4	ADBO7- [138]
[138] ADBO8-	5	6	LOBO2+ [242]
[242] LOBO3+	7	8	L1BO3- [*]
[*] L1BO4-	9	10	ADBO9- [138]
[138] ADB10-	11	12	LOBO4+ [242]
[242] LOBO5+	13	14	L1BO5- [*]
[*] L1BO6-	15	16	ADB11- [138]
[*] DRL1N-	17	18	LOBO6+ [242]
[242] LOBO7+	19	20	L1BO7- [*]
[*] L1BO8-	21	22	PARCK- [*]
	23	24	LOBO8+ [242]
[134] SMKXX-	25	26	A1D1833 [GND]
[134] OCPLS-	27	28	A1D1833 [GND]
[134] SMKOI-	29	30	A1D1833 [GND]
[259] ERLAX-	31	32	A1D1833 [GND]

A1E18

[242] LOB09+	1	2	L1B09- [*] [241]
[*] L1B10-	3	4	ADB12- [138] [241]
[138] ADB13-	5	6	LOB10+ [242]
[242] LOB11+	7	8	L1B11- [*] [241]
[*] L1B12-	9	10	ADB14- [138] [241]
[138] ADB15-	11	12	LOB12+ [242]
[242] LOB13+	13	14	L1B13- [*] [241]
[*] L1B14-	15	16	ADB16- [138] [241]
[*] P1L00-	17	18	LOB14+ [242]
[242] LOB15+	19	20	L1B15- [*] [241]
[*] L1B16-	21	22	[241]
[148] PWRFL-	23	24	LOB16+ [243]
[134] CMKXX-	25	26	A1E1833 [GND]
[240] OTPMA-	27	28	A1E1833 [GND]
[240] OTPMA-	29	30	VDC06- [148]
[131] MSTCL-	31	32	VDC06- [148]

A1F11

[241] ACKA1-	1	2	CHSL1+ [241]
[241] CHEN1+	3	4	D1LA1- [*]
ERLA1+	5	6	DMA1N- [*]
[241] ACKA2-	7	8	CHSL2+ [241]
[241] CHEN2+	9	10	D1LA2- [*]
ERLA2+	11	12	
[241] ACKA3-	13	14	CHSL3+ [241]
[241] CHEN3+	15	16	D1LA3- [*]
ERLA3+	17	18	
[241] ACKA4-	19	20	CHSL4+ [241]
[241] CHEN4+	21	22	D1LA4- [*]
ERLA4+	23	24	

A1F18

[259] ERLAX-	1	2	DMAIN- [259]
	3	4	ACTO2+ [259]
[259] ACTO3+	5	6	
	7	8	ACTO4+ [259]
[259] ACTO5+	9	10	
	11	12	ACTO6+ [259]
[259] ACTO7+	13	14	
	15	16	ACTO8+ [259]
[259] ACTO9+	17	18	
[240] TLBFF+A	19	20	ACTIO+ [259]
[259] ACT11+	21	22	TLDFF+A [240]
[240] TLABF+	23	24	ACTI2+ [259]
[259] ACTI3+	25	26	
	27	28	ACTI4+ [259]
[259] ACTI5+	29	30	
	31	32	ACTI6+ [259]

[*] THESE SIGNALS ARRIVE BY BUS FROM I/O OPTIONS, DEPENDING ON SYSTEM CONFIGURATION

DMA MF PAC ALLOCATION diagram

Top column labels: F E D C B A

Grid labels across top: A B C D E F G H J K L

HINGE

Card slots (partial contents):

Column F, top group: CC-045, CC-045, CC-045, CC-045, CC-045

Column F: CC-045

Column D (row 5): CM-022

Column F (middle group): CC-045, CC-045, CC-045, CC-045, CC-045, CC-045

Column D (row 7): DI-335

Bottom row group:

Column F:
8	CONN
7	PA-336
6	TG-335
5	TG-335
4	TG-335
3	TG-335
2	TG-335
1	CONN

Column E:
8	CC-154
7	PA-336
6	CC-089
5	CC-153
4	CC-163
3	CC-153
2	TG-335
1	TG-335

Column D:
8	CC-154
7	DI-335
6	DI-335
5	TG-335
4	CC-045
3	CC-073
2	CC-C73
1	CC-044

Notes:

⚠ THESE PACS ARE SHARED WITH THE EXTENDED ADDR OPTION

⚠ CC-154 IN LOCATIONS E18 AND D18 SHOULD BE REMOVED AND PLACED IN LAST OPTION AT END OF DMA BUS WHEN OPTIONS ARE USED

REVISIONS

TAKEN FROM SK-C413S4 DUCKWORTH 10-25-66 A
ECO 3707 B
EXT CHANGES 1/23/67 ECO 3995 C
EXT CHANGES 2/20/67 ECO 4226 D
EXT CHANGES SEE ECO 5/25/67

TITLE
DMA
MF PAC ALLOCATION
DDP-516-21

SIZE C   DWG NO. 016586   REV. D

A   B   C   D   E   F   G   H   J   K   L

Row 4

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

Row 3

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

Row 2

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	8	CONN														
	7															
	6															
001	5	DL-335														
001	4	CC-089														
002	3	DC-335														
001	2	DC-335														
	1	CONN														

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	8	CONN														
001	7	CC-091														
001	6	CC-091														
001	5	TG-335														
001	4	TG-335														
001	3	CC-152														
001	2	TG-335														
001	1	OD-335														

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	8	CONN														
001	7	CC-091														
001	6	CC-091														
001	5	TG-335														
001	4	PA-336														
001	3	CC-152														
001	2	TG-335														
	1	CONN														

Row 1

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
003	8	DC-335														
003	7	CM-022														
003	6	TG-335														
003	5	CC-152														
003	4	CC-091														
003	3	CC-091														
003	2	CC-091														
003	1	CC-091														

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
001	8	TG-335														
003	7	TG-335														
003	6	PA-336														
002	5	CC-152														
002	4	TG-335														
002	3	CC-091														
002	2	CC-091														
	1	CONN														

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
001	8	TG-335														
002	7	TG-335														
002	6	TG-335														
002	5	PA-336														
002	4	CC-152														
002	3	CC-091														
002	2	CC-091														
	1	CONN														

A   B   C

PAC SIDE

001   DMA WITH 1 CHANNEL
002   1st ADDITIONAL CHANNEL (CHANNEL 2)
003   2nd ADDITIONAL CHANNEL (CHANNEL 3)

33

A   B   C   D   E   F   G   H   J   K   L

Column 1 / 2 / 3 — CHSL gates

[259] CHSL1+A — B24 — 15 17 13 E G — TG-335 → C24 16 7 18 11 9 A — PA-336 → CHSL1+

[259] CHSL2+A — B24 — 14 12 13 E — TG-335 → C15 16 7 18 11 9 A — PA-336 → CHSL2+

[259] CHSL3+A — B24 — 16 18 13 F — TG-335 → B16 16 7 18 11 9 C — PA-336 → CHSL3+

TRIG gates (B18)

CHSL1+ — 4, [240] TLBFF+A — 6 2 G — B18 TG-335 → TRIG1−

CHSL2+ — 8, [240] TLBFF+A — 6 10 — B18 TG-335 → TRIG2−

CHSL3+ — 5, [240] TLBFF+A — 6 7 C — B18 TG-335 → TRIG3−

ADB buffers (B22)

[259] ADB07 ≫ 4 2 6 A — B22 TG-335 → ADB07+L
B22 8 10 6 G — TG-335 → ADB07−L

[259] ADB09 ≫ 5 7 6 C — B22 TG-335 → ADB09+L
B22 1 3 6 D — TG-335 → ADB09−L

[259] ADB10 ≫ 14 12 13 E — B22 TG-335 → ADB10+L
B22 16 18 13 F — TG-335 → ADB10−L

[259] ADB14 ≫ 15 17 6 G — B22 TG-335 → ADB14+L

OTB gates (columns F/G/H)

[259] OTB01+ — 14 12 13 E — B18 TG-335 → 16 18 F — B18 TG-335 → OTB01+L

[259] OTB02+ — 15 17 13 E — B18 TG-335 → 11 9 H — B18 TG-335 → OTB02+L

[259] OTB03+ — 14 12 13 E — C18 TG-335 → 16 18 F — C18 TG-335 → OTB03+L

[259] OTB04+ — 15 17 13 G — C18 TG-335 → 11 9 H — C18 TG-335 → OTB04+L

[259] OTB05+ — 4 2 6 A — C18 TG-335 → 8 10 B — C18 TG-335 → OTB05+L

[259] OTB06+ — 5 7 6 C — C18 TG-335 → 1 3 6 D — C18 TG-335 → OTB06+L

[259] OTB07+ — 4 2 6 A — C22 TG-335 → 8 10 B — C22 TG-335 → OTB07+L

[259] OTB08+ — 5 7 6 C — C22 TG-335 → 1 3 6 D — C22 TG-335 → OTB08+L

OTB gates (columns J/K/L)

[259] OTB09+ — 14 12 13 E — C22 TG-335 → 16 18 F — C22 TG-335 → OTB09+L

[259] OTB10+ — 15 17 13 E — C22 TG-335 → 11 9 H — C22 TG-335 → OTB10+L

[259] OTB11+ — 22 20 23 J — B18 TG-335 → 24 26 K — B18 TG-335 → OTB11+L

[259] OTB12+ — 27 31 29 M — B18 TG-335 → 25 28 N — B18 TG-335 → OTB12+L

[259] OTB13+ — 22 20 23 J — C18 TG-335 → 24 26 K — C18 TG-335 → OTB13+L

[259] OTB14+ — 27 31 29 M — C18 TG-335 → 25 28 N — C18 TG-335 → OTB14+L

[259] OTB15+ — 22 20 23 J — C22 TG-335 → 24 26 K — C22 TG-335 → OTB15+L

[259] OTB16+ — 21 19 23 L — C18 TG-335 → 21 19 23 L — C22 TG-335 → OTB16+L

B21 block

B21 OD-335
ADB10+L — 22
ADB10−L — 12   26 — OTPA4−
ADB09+L — 6   24 — OTPA1−
ADB09−L — 28   10 — OTPA2−
ADB07+L — 2   8 — OTPA3−
ADB07−L — 4   20 — OTPR4−
              18 — OTPR1−
SMKXX+L — 7   16 — OTPR2−
ADB14+L — 9   14 — OTPR3−
              11   A

Lower center

[259] ADB12− — 11 9 13 H — B22 TG-335
[259] ADB11− — 21 15, [259] ADP13− — 17, ADB14+L — 1, [259] ADB15− — 3, [259] ADB16− — 5 B — B21 OD-335 → 23 → 32 30 29 P — C18 TG-335 → ADQ24+

[259] SMKXX− — 21 19 23 — B18 TG-335 → SMKXX+L

[259] CMKXX− — 32 30 29 P — B18 TG-335 → CMKXX+L

Title block

DDP-516-21
DMA CHANNEL #1
ADDRESS COUNTER

HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer   DATE 1/18/67
ENG.   1-20-67
APP. G.C. Hendrie   1-20-67
PROJECT NO. 55215

SIZE C   DWG NO. 016364   REV. c

37

B24
[250] OTB09 +L — 25 28 SR109 —
29 N
TG-335

B24
[250] OTB02 +L — 27 31 SR102 —
29 M
TG-335

B24
[250] OTB10 +L — 32 30 SR110 —
29 P
TG-335

C25
[250] OTB03 +L — 22 20 SR103 —
23 J
TG-335

B25
[250] OTB11 +L — 22 20 SR111 —
23 J
TG-335

C25
[250] OTB04 +L — 24 26 SR104 —
23 K
TG-335

B25
[250] OTB12 +L — 24 26 SR112 —
23 K
TG-335

C25
[250] OTB05 +L — 21 19 SR105 —
23 L
TG-335

B25
[250] OTB13 +L — 21 19 SR113 —
23 L
TG-335

C25
[250] OTB06 +L — 27 31 SR106 —
29 M
TG-335

B25
[250] OTB14 +L — 27 31 SR114 —
29 M
TG-335

C25
[250] OTB07 +L — 25 28 SR107 —
29 N
TG-335

B25
[250] OTB15 +L — 25 28 SR115 —
29 N
TG-335

C25
[250] OTB08 +L — 32 30 SR108 —
29 P
TG-335

B25
[250] OTB16 +L — 32 30 SR116 —
29 P
TG-335

C24
[250] OTPR1 — 12 14 16 5 3 OTPR1 +
D
PA-335

B26 CC-091
TRRC1 — 30
SR116 — 29   26 RCA16 +
31 20 24
SR115 — 25   22 RCA15 +
22 18
SR114 — 21   23 RCA14 +
19
SR113 — 17   28 RCA13 +
6 15
SR112 — 13   8 RCA12 +
2 11
SR111 — 9   10 RCA11 +
4 3
SR110 — 1   12 RCA10 +
5 14
SR109 — 7   RCA09 +
32

B27 CC-091
30
SR108 — 29   26 RCA08 +
31 20 24
SR107 — 25   27 RCA07 +
22 18
SR106 — 21   23 RCA06 +
16 19
SR105 — 17   28 RCA05 +
6 15
SR104 — 13   8 RCA04 +
2 11
SR103 — 9   10 RCA03 +
4 3
SR102 — 1   12 RCA02 +
7 5 14
[251] CLARA — 32   ERLA1 —

A22
[259] TLDFF +A — 26
[259] CHEN1 + — 24
22 14 16 18
28 TRRC1 —
E
DC-335

B23
RCA02 + — 4 2 INB01 —
6 A
CC-152

B23
RCA02 + — 8 10 INB02 —
6 B
CC-152

B23
RCA03 + — 5 7 INB03 —
6 C
CC-152

B23
RCA04 + — 1 3 INB04 —
6 D
CC-152

C23
RCA05 + — 4 2 INB05 —
6 A
CC-152

C23
RCA06 + — 8 10 INB06 —
6 B
CC-152

C23
RCA07 + — 5 7 INB07 —
6 C
CC-152

C23
RCA08 + — 1 3 INB08 —
6 D
CC-152

C23
RCA09 + — 22 20 INB09 —
23 J
CC-152

C23
RCA10 + — 24 26 INB10 —
23 K
CC-152

C23
RCA11 + — 21 19 INB11 —
23 L
CC-152

C23
RCA12 + — 27 31 INB12 —
29 M
CC-152

C23
RCA13 + — 25 28 INB13 —
29 N
CC-152

C23
RCA14 + — 32 30 INB14 —
29 P
CC-152

B23
RCA15 + — 27 31 INB15 —
29 M
CC-152

B23
RCA16 + — 25 28 INB16 —
29 N
CC-152

B23
ERLA1 — 32 30 DRLIN —
29 P
CC-152

B21
[250] ADQ24 + — 27
29
[250] ADB09 — L — 19 25
30
[250] ADB10 + L — 32
C
OD-335

C24
28 25
30
29 27
F
PA-336

[250] OTB01 +L — C16 — 15 17 SA201 — TG-335
[250] OTB02 +L — C16 — 11 9 SA202 — TG-335
[250] OTB03 +L — C16 — 4 2 SA203 — TG-335
[250] OTB04 +L — C16 — 8 10 SA204 — TG-335
[250] OTB05 +L — C16 — 5 7 SA205 — TG-335
[250] OTB06 +L — C16 — 1 3 SA206 — TG-335
[250] OTB07 +L — C16 — 14 12 SA207 — TG-335
[250] OTB08 +L — C16 — 16 18 SA208 — TG-335

[250] OTB09 +L — B14 — 4 2 SA209 — TG-335
[250] OTB10 +L — B14 — 8 10 SA210 — TG-335
[250] OTB11 +L — C17 — 4 2 SA211 — TG-335
[250] OTB12 +L — C17 — 8 10 SA212 — TG-335
[250] OTB13 +L — C17 — 5 7 SA213 — TG-335
[250] OTB14 +L — C17 — 1 3 SA214 — TG-335
[250] OTB15 +L — B14 — 5 7 SA215 — TG-335
[250] OTB16 +L — B14 — 1 3 SA216 — TG-335

C13 CC-091
[250] TRIG2 — 30
SA216 — 29 26 31 ACB16 —
SA215 — 25 20 24 ACB15 —
SA214 — 21 27 22 23 ACB14 —
SA213 — 17 18 16 19 ACB13 —
SA212 — 13 28 6 15 ACB12 —
SA211 — 9 8 2 11 ACB11 —
SA210 — 1 10 4 3 ACB10 —
SA209 — 7 12 5 ACB09 —
32 14

C12 CC-091
30
SA208 — 29 26 31 ACB08 —
SA207 — 25 20 24 27 ACB07 —
SA206 — 21 22 23 16 ACB06 —
SA205 — 17 18 19 28 ACB05 —
SA204 — 13 6 15 8 ACB04 —
SA203 — 9 2 11 10 ACB03 — C1233 [GND]
SA202 — 1 4 3 ACB02 —
SA201 — 7 12 5 INPTB +
32 14

ACB02 — C17 — 14 12 ACTO2 + TG-335
[250] CHSL2 + — E
ACB03 — C17 — 16 18 ACTO3 + TG-335 F
ACB04 — C17 — 15 17 ACTO4 + TG-335 G
ACB05 — C17 — 11 9 ACTO5 + TG-335 H
ACB06 — C14 — 4 2 ACTO6 + CC-152 A
ACB07 — C14 — 8 10 ACTO7 + CC-152 B
ACB08 — C14 — 5 7 ACTO8 + CC-152
C14 — 1 3 DMAIN — CC-152 D

ACB09 — B15 — 4 2 ACTO9 + CC-152 A
[250] CHSL2 +
ACB10 — B15 — 8 10 ACT10 + CC-152 B
ACB11 — B15 — 5 7 ACT11 + CC-152 C
ACB12 — B15 — 1 3 ACT12 + CC-152 D
ACB13 — C14 — 14 12 ACT13 + CC-152 E
ACB14 — C14 — 16 18 ACT14 + CC-152 F
ACB15 + — C14 — 15 17 ACT15 + CC-152
ACB16 — C14 — 11 9 ACT16 + CC-152 H

C15 — 20 19 22 23 21 B PA-336 OTPA2 +
C15 — 8 2 10 6 4 C PA-336
[250] CMKXX + L
CLARB —

A25 — OTPA2 — 22 19 20 17 15 C DL-335 CMKXX+L
SMKXX+L

A24 CC-089 — 16 18 20 22 24 4 B 12 14

41

A   B   C   D   E   F   G   H   J   K   L

B14
[250] OTB09 + L   25 28 SR209 −
29
N
TG-335

B14
[250] OTB02 + L   27 31 SR202 −
29
M
TG-335

B14
[250] OTB10 + L   32 30 SR210 −
29
P
TG-335

C16
[250] OTB03 + L   22 20 SR203 −
23
J
TG-335

C17
[250] OTB11 + L   22 20 SR211 −
23
TG-335

C16
[250] OTB04 + L   24 26 SR204 −
23
K
TG-335

C17
[250] OTB12 + L   24 26 SR212 −
23
TG-335

C16
[250] OTB05 + L   21 19 SR205 −
23
L
TG-335

C17
[250] OTB13 + L   21 19 SR213 −
23
TG-335

C16
[250] OTB06 + L   27 31 SR206 −
29
M
TG-335

C17
[250] OTB14 + L   27 31 SR214 −
29
M
TG-335

C16
[250] OTB07 + L   25 28 SR207 −
29
N
TG-335

C17
[250] OTB15 + L   25 28 SR215 −
29
TG-335

C16
[250] OTB08 + L   32 30 SR208 −
29
P
TG-335

C17
[250] OTB16 + L   32 30 SR216 −
29
TG-335

C15
[250] OTPR2 −   12 1
14
5   3
D   OTPR2 +
PA-336

B13   CC-091
TRRC2 − 30
SR216 − 29   26 RCB16 +
31
20
SR215 − 25   24 RCB15 +
27
22
SR214 − 21   18 RCB14 +
23
SR213 − 17   16 RCB13 +
19
28
SR212 − 13   6 RCB12 +
15
8
SR211 − 9   2 RCB11 +
11
10
SR210 − 1   4 RCB10 +
3
SR209 − 7   12 RCB09 +
5
32   14

B12   CC-091
30
SR208 − 29   26 RCB08 +
31
20
SR207 − 25   24 RCB07 +
27
22
SR206 − 21   18 RCB06 +
23
SR205 − 17   16 RCB05 +
19
28
SR204 − 13   6 RCB04 +
15
8
SR203 − 9   2 RCB03 +
11
10
SR202 − 1   4 RCB02 +
3
12
[253] CLARB −   5 ERLA2 −
32   14

A23
[259] TLDFF + A   26 20
[259] CHEN2 +   24
22
14
16   28 TRRC2 −
18
E
DC-335

C15
[250] ADQ24 +   24 13
26
[250] ADB09 + L   17 15
[250] ADB10 − L   E
PA-336

C24
24
26
17 15
E
PA-336

B23
14 12 INB01 −
13
E
CC-152

B23
RCB02 +   16 18 INB02 −
13
F
CC-152

B23
RCB03 +   15 17 INB03 −
13
G
CC-152

B23
RCB04 +   11 9 INB04 −
13
M
CC-152

C23
RCB05 +   14 12 INB05 −
13
E
CC-152

C23
RCB06 +   16 18 INB06 −
13
F
CC-152

C23
RCB07 +   15 17 INB07 −
13
G
CC-152

C23
RCB08 +   11 9 INB08 −
13
H
CC-152

C14
RCB09 +   22 20 INB09 −
23
CC-152

C14
RCB10 +   24 26 INB10 −
23
K
CC-152

C14
RCB11 +   21 19 INB11 −
23
CC-152

C14
RCB12 +   27 31 INB12 −
29
M
CC-152

C14
RCB13 +   25 28 INB13 −
29
N
CC-152

C14
RCB14 +   32 30 INB14 −
29
P
CC-152

B15
RCB15 +   27 31 INB15 −
29
M
CC-152

B15
RCB16 +   25 28 INB16 −
29
N
CC-152

B15
ERLA2 −   32 30 DRLIN −
29
P
CC-152

REV.
D ECO 4237
C REDRAWN, NO CHG 2-28-67
C ECO 4042 EXT. CHANGES J.D. 8/4/67
CHK REVISIONS

NOTES;
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43

A   B   C   D   E   F   G   H   J   K   L

1   2   3   4   5   6   7   8   9   10   11

A16 [250] OTB01 + L — 15 17 SA301 — 13 G — TG-335

A16 [250] OTB02 + L — 11 9 SA302 — 13 H — TG-335

A16 [250] OTB03 + L — 4 2 SA303 — 6 A — TG-335

A16 [250] OTB04 + L — 8 10 SA304 — 6 B — TG-335

A16 [250] OTB05 + L — 5 7 SA305 — 6 C — TG-335

A16 [250] OTB06 + L — 1 3 SA306 — 6 D — TG-335

A16 [250] OTB07 + L — 14 12 SA307 — 13 E — TG-335

A16 [250] OTB08 + L — 16 18 SA308 — 13 F — TG-335

B14 [250] OTB09 + L — 15 17 SA309 — 13 G — TG-335

B14 [250] OTB10 + L — 11 9 SA310 — 13 H — TG-335

B17 [250] OTB11 + L — 4 2 SA311 — 6 A — TG-335

B17 [250] OTB12 + L — 8 10 SA312 — 6 B — TG-335

B17 [250] OTB13 + L — 5 7 SA313 — 6 C — TG-335

B17 [250] OTB14 + L — 1 3 SA314 — 6 D — TG-335

B14 [250] OTB15 + L — 14 12 SA315 — 13 E — TG-335

B14 [250] OTB16 + L — 16 18 SA316 — 13 F — TG-335

A14 CC-091
[250] TRIG3 — 30
SA316 — 29   26 / 31 / 20 / 24 ACC16 —
SA315 — 25   27 / 22 ACC15 —
SA314 — 21   18 / 23 / 16 ACC14 —
SA313 — 17   19 / 28 ACC13 —
SA312 — 13   6 / 15 / 8 ACC12 —
SA311 — 9   2 / 11 ACC11 —
SA310 — 1   4 / 3 / 12 ACC10 —
SA309 — 32   5 / 14 ACC09 —

A13 CC-091
30
SA308 — 29   26 / 31 / 20 / 24 AGC08 —
SA307 — 25   27 / 22 ACC07 —
SA306 — 21   18 / 23 / 16 ACC06 —
SA305 — 17   19 / 28 ACC05 —
SA304 — 13   6 / 15 / 8 ACC04 —
SA303 — 9   2 / 11 ACC03 —
                  10 A1333 [GND]
SA302 — 1   4 / 3 ACC02 —
SA301 — 7   12 / 5 INPTC +
              32 14

A15 ACCO2 — 11 9 ACTO2 + [250] CHSL3 + 13 H — CC-152

A17 ACCO3 — 4 2 ACTO3 + 13 A — CM-022

A17 ACCO4 — 8 10 ACTO4 + 13 B — CM-022

A17 ACCO5 — 5 7 ACTO5 + 13 C — CM-022

A17 ACCO6 — 1 3 ACTO6 + 6 — CM-022

A15 ACCO7 — 14 12 ACTO7 + 13 E — CC-152

A15 ACCO8 — 16 18 ACTO8 + 13 F — CC-152

A15 15 17 DMAIN — 13 G — CC-152

B17 [250] CHSL3 + 15 17 ACTO9 + 13 G — TG-335

B17 ACC10 — 11 9 ACT10 + 13 H — TG-335

A17 ACC11 — 14 12 ACT11 + 13 E — CM-022

A17 ACC12 — 16 18 ACT12 + 13 F — CM-022

A17 ACC13 — 15 17 ACT13 + 13 G — CM-022

A17 ACC14 — 11 9 ACT14 + 13 H — CM-022

B17 ACC15 — 14 12 ACT15 + 13 E — TG-335

B17 ACC16 — 16 18 ACT16 + 13 F — TG-335

B16 20 19 / 22 / 23 21 — OTPA3 + B — PA-336

B16 8 2 / 10 / 4 — CLARC — C — PA-336 [250] CMKXX + L

A25 DL-335 [250] OTPA3 — 16 / 11 18 / 13 D

A24 CC-089 CMKXX+L — 31 / 29 / 27 / 25 SMKXX+L — 23 / 4 C — 1 / 5 / 3

45

A | B | C | D | E | F | G | H | J | K | L

B14 TG-335
[250] OTB09 +L — 24 / 26 — SR309 −
23 / K

B14 TG-335
[250] OTB02 +L — 22 / 20 — SR302 −
23 / J

B14 TG-335
[250] OTB10 +L — 21 / 19 — SR310 −
23 / L

B17 TG-335
[250] OTB03 +L — 22 / 20 — SR303 −
23 / J

A16 TG-335
[250] OTB11 +L — 22 / 20 — SR311 −
23 / J

B17 TG-335
[250] OTB04 +L — 24 / 26 — SR304 −
23 / K

A16 TG-335
[250] OTB12 +L — 24 / 26 — SR312 −
23 / K

B17 TG-335
[250] OTB05 +L — 21 / 19 — SR305 −
23 / L

A16 TG-335
[250] OTB13 +L — 21 / 19 — SR313 −
23 / L

B17 TG-335
[250] OTB06 +L — 27 / 31 — SR306 −
29 / M

A16 TG-335
[250] OTB14 +L — 27 / 31 — SR314 −
29 / M

B17 TG-335
[250] OTB07 +L — 25 / 28 — SR307 −
29 / N

A16 TG-335
[250] OTB15 +L — 25 / 28 — SR315 −
29 / N

B17 TG-335
[250] OTB08 +L — 32 / 30 — SR308 −
29 / P

A16 TG-335
[250] OTB16 +L — 32 / 30 — SR316 −
29 / P

B16 PA-336
[250] OTPR3 − — 12 / 1, 14, 5 / 3 — OTPR3 +

B16 PA-336
[250] ADQ24 + — 24 / 13
[250] ADB09 +L — 26
[250] ADB10 +L — 17 / 15
E

C15 PA-336
28 / 25, 30, 29 / 27
F

A12 CC-091
TRRC3 − — 30
SR316 − — 29 — 26 — RCC16 +
— 31
— 20
SR315 − — 25 — 24 — RCC15 +
— 27
— 22
SR314 − — 21 — 18 — RCC14 +
— 23
SR313 − — 17 — 16 — RCC13 +
— 19
— 28
SR312 − — 13 — 6 — RCC12 +
— 15
— 8
SR311 − — 9 — RCC11 +
— 11
— 10
SR310 − — 1 — 4 — RCC10 +
— 3
SR309 − — 7 — 2 — RCC09 +
— 5
— 32 — 14

A11 CC-091
— 30
SR308 − — 29 — 26 — RCC08 +
— 31
— 20
SR307 − — 25 — 24 — RCC07 +
— 27
— 22
SR306 − — 21 — 18 — RCC06 +
— 23
SR305 − — 17 — 16 — RCC05 +
— 19
— 28
SR304 − — 13 — 6 — RCC04 +
— 15
— 8
SR303 − — 9 — 2 — RCC03 +
— 11
— 10
SR302 − — 1 — 4 — RCC02 +
— 3
[255] CLARC − — 7 — 5 — ERLA3 −
— 32 — 14

A18 DC-335
[259] TLDFF +A — 26 / 20
[259] CHEN3 + — 24
— 22
— 14 — 28 — TRRC3 −
— 16
— 18
E

A15 CC-152
RCC09 + — 4 / 6 — 2 — INB01 −

A15 CC-152
RCC02 + — 8 / 10 — INB02 −
B

A15 CC-152
RCC03 + — 5 / 7 — INB03 −
6 / C

A15 CC-152
RCC04 + — 1 / 3 — INB04 −
6 / D

B15 CC-152
RCC05 + — 14 / 12 — INB05 −
13 / E

B15 CC-152
RCC06 + — 16 / 18 — INB06 −
13 / F

B15 CC-152
RCC07 + — 15 / 17 — INB07 −
13 / G

B15 CC-152
RCC08 + — 11 / 9 — INB08 −
13 / H

A15 CC-152
RCC09 + — 22 / 20 — INB09 −
23

A15 CC-152
RCC10 + — 24 / 26 — INB10 −
K

A15 CC-152
RCC11 + — 21 / 19 — INB11 −
23

A15 CC-152
RCC12 + — 27 / 31 — INB12 −
29 / M

A15 CC-152
RCC13 + — 25 / 28 — INB13 −
N

A15 CC-152
RCC14 + — 32 / 30 — INB14 −
29 / P

B15 CC-152
RCC15 + — 22 / 20 — INB15 −
23 / J

B15 CC-152
RCC16 + — 24 / 26 — INB16 −
23 / K

B15 CC-152
ERLA3 − — 21 / 19 — DRLIN −
23

1 · 2 · 3 · 4 · 5 · 6 · 7 · 8 · 9 · 10 · 11

A B C D E F G H J K L

A22
12
CHSL1 + 32
RCA16 + 31
RCA15 + 29   30 ⊙─ ERCH1−
RCA14 + 6
RCA13 + 8
RCA12 + 10
F
DC−335

A23
12
CHSL2 + 32
RCB16 + 31
RCB15 + 29   30 ⊙─ ERCH2−
RCB14 + 6
RCB13 + 8
RCB12 + 10
F
DC−335

A18
12
CHSL3 + 32
RCC16 + 31
RCC15 + 29   30 ⊙─ ERCH3−
RCC14 + 6
RCC13 + 8
RCC12 + 10
F
DC−335

A22
1
RCA11 + 2
RCA10 + 3
RCA09 + 4
A
DC−335

A23
1
RCB11 + 2
RCB10 + 3
RCB09 + 4
A
DC−335

A18
1
RCC11 + 2
RCC10 + 3
RCC09 + 4
A
DC−335

A22
5
RCA08 + 7
RCA07 + 9
RCA06 + 11
B
DC−335

A23
5
RCB08 + 7
RCB07 + 9
RCB06 + 11
B
DC−335

A18
5
RCC08 + 7
RCC07 + 9
RCC06 + 11
B
DC−335

A22
13
RCA05 + 15
RCA04 + 17
RCA03 + 19
C
DC−335

A23
13
RCB05 + 15
RCB04 + 17
RCB03 + 19
C
DC−335

A18
13
RCC05 + 15
RCC04 + 17
RCC03 + 19
C
DC−335

A22
21
RCA02 + 23
[259] TLABF + 25
27
D
DC−335

A23
21
RCB02 + 23
[259] TLABF + 25
27
D
DC−335

A18
21
RCC02 + 23
[259] TLABF + 25
27
D
DC−335

NOTES;
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△
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CHK
REV B
REVISIONS ECO 4237
RF REDRAWN, NO CHG
7 June 2 28 67

TITLE
DDP − 516 − 21
DMA END − OF − RANGE CONTROL

SIZE DWG NO. REV.
C 016370 B

49

A-28

[245] ACKA1-	1	2	CHSL1+A [245]
[245] CHEN1+	3	4	DILA1- *
[257] ERCH1-	5	6	DMAIN- [251]
[245] ACKA2-	7	8	CHSL2+A [245]
[245] CHEN2+	9	10	DILA2- *
[257] ERCH2-	11	12	DUMMY+C
[245] ACKA3-	13	14	CHSL3+A [245]
[245] CHEN3+	15	16	DILA3- *
[257] ERCH3-	17	18	DUMMY+E
[245] ACKA4-	19	20	CHSL4+A [245]
[245] CHEN4+	21	22	DILA4- *
ERCH4-	23	24	DUMMY+G
DUMMY+H	25	26	DUMMY+J
DUMMY+K	27	28	DUMMY+L
DUMMY+M	29	30	DUMMY+N
DUMMY+P	31	32	DUMMY+R

B28

[143] OTB09+	1	2	INB09- [252]
[252] INB10-	3	4	ADB12- [143]
[143] ADB13-	5	6	OTB10+ [143]
[143] OTB11+	7	8	INB11- [252]
[252] INB12-	9	10	ADB14- [143]
[143] ADB15-	11	12	OTB12+ [143]
[143] OTB13+	13	14	INB13- [252]
[252] INB14-	15	16	ADB16- [143]
* PIL00-	17	18	OTB14+ [143]
[143] OTB15+	19	20	INB15- [252]
[252] INB16-	21	22	SPARE+B
[148] PWPFL-	23	24	OTB16+ [143]
[143] CMKXX-	25	26	VDC00-E
[143] SPARE+D	27	28	VDC00-F
[143] RRLIN-	29	30	VDC06-A
[143] MSTCL-	31	32	VDC06-B

C28

[143] OTB01+	1	2	INBC1- [252]
[252] INB02-	3	4	ADB07- [143]
[143] ADB08-	5	6	OTB02+ [143]
[143] OTB03+	7	8	INB03- [252]
[252] INB04-	9	10	ADB09- [143]
[143] ADB10-	11	12	CTB04+ [143]
[143] OTB05+	13	14	INB05- [252]
[252] INB06-	15	16	ADB11- [143]
[252] DRLIN-	17	18	OTB06+ [143]
[143] OTB07+	19	20	INB07- [252]
[252] INB08-	21	22	PARCK- *
SPARE+A	23	24	OTB08+ [143]
[143] SMKXX-	25	26	VDC00-A
[143] OCPLS-	27	28	VDC00-B
[143] SMK01-	29	30	VDC00-C
[143] ERLXX-	31	32	VDC00-D

A-21

[245] ACKA1-	1	2	CHSL1+A [245]
[245] CHEN1+	3	4	DILA1- *
[257] ERCH1-	5	6	DMAIN- [251]
[245] ACKA2-	7	8	CHSL2+A [245]
[245] CHEN2+	9	10	DILA2- *
[257] ERCH2-	11	12	DUMMY+C
[245] ACKA3-	13	14	CHSL3+A [245]
[245] CHEN3+	15	16	DILA3- *
[257] ERCH3-	17	18	DUMMY+E
[245] ACKA4-	19	20	CHSL4+A [245]
[245] CHEN4+	21	22	DILA4- *
ERCH4-	23	24	DUMMY+G
DUMMY+H	25	26	DUMMY+J
DUMMY+K	27	28	DUMMY+L
DUMMY+M	29	30	DUMMY+N
DUMMY+P	31	32	DUMMY+R

B11

[143] OTB09+	1	2	INB09- [252]
[252] INB10-	3	4	ADB12- [143]
[143] ADB13-	5	6	OTB10+ [143]
[143] OTB11+	7	8	INB11- [252]
[252] INB12-	9	10	ADB14- [143]
[143] ADB15-	11	12	OTB12+ [143]
[143] OTB13+	13	14	INB13- [252]
[252] INB14-	15	16	ADB16- [143]
* PIL00-	17	18	OTB14+ [143]
[143] OTB15+	19	20	INB15- [252]
[252] INB16-	21	22	SPARE+B
[148] PWRFL-	23	24	OTB16+ [143]
[143] CMKXX-	25	26	VDC00-E
[143] SPARE+D	27	28	VDC00-F
[143] RRL'N-	29	30	VDC06-A
[143] MSTCL-	31	32	VDC06-B

C11

[143] OTB01+	1	2	INB01- [252]
[252] INB02-	3	4	ADB07- [143]
[143] ADB08-	5	6	OTB02+ [143]
[143] OTB03+	7	8	INB03- [252]
[252] INB04-	9	10	ADB09- [143]
[143] ADB10-	11	12	OTB04+ [143]
[143] OTB05+	13	14	INB05- [252]
[252] INB06-	15	16	ADB11- [143]
[252] DRLIN-	17	18	OTB06+ [143]
[143] OTB07+	19	20	INB07- [252]
[252] INB08-	21	22	PARCK- *
SPARE+A	23	24	OTB08+ [143]
[143] SMKXX-	25	26	VDC00-A
[143] OCPLS-	27	28	VDC00-B
[143] SMK01-	29	30	VDC00-C
[143] ERLXX-	31	32	VDC00-D

C21

	1	2	
[251] ACT03+	3	4	ACT02+ [251]
	5	6	ACT04+ [251]
[251] ACT05+	7	8	
	9	10	ACT06+ [251]
[251] ACT07+	11	12	
	13	14	ACT08+ [251]
	15	16	
[251] ACT09+	17	18	
[245] TLBFF+A	19	20	ACT10+ [251]
[251] ACT11+	21	22	TLDFF+A [245]
[245] TLABF+	23	24	ACT12+ [251]
[251] ACT13+	25	26	
	27	28	ACT14+ [251]
[251] ACT15+	29	30	
	31	32	ACT16+ [251]

[*] THESE SIGNALS ARRIVE BY BUS FROM I/O OPTIONS, DEPENDING ON SYSTEM CONFIGURATIONS

REVISIONS

TITLE: DMA CABLES

SIZE C · DWG NO. 016371 · REV. A

APPENDIX
PAC DESCRIPTIONS

Descriptions of PACs CC-152 and CC-154 follow.

TRANSFER GATE PAC, MODEL CC-152

GENERAL

The Transfer Gate PAC, Model CC-152 (Figure 1), contains 14 2-input NAND gates without collector resistors arranged in four independent groups. Two of the groups contain four NAND gates each with one input being common to the four gates. The other two groups contain three NAND gates each with one input being common to the three gates. All fourteen circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The Model CC-152 PAC can be used for the common transfer control of up to 14 data signals with the common input used as a control or strobe input. Turn-on rise time is controlled so as to have a guaranteed minimum of 50 nsec with no load.

SPECIFICATIONS

Frequency of Operation

DC to 5 mc (max)

Input Loading

Individual inputs: 1 unit load each
Common inputs: 1 unit load per gate

Output Drive Capability

8 unit loads

Circuit Delay

120 nsec (max) turn on
40 nsec (max) turn off

Current Requirements

+6v: 95 ma

Power Dissipation

560 mw (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C2-C15	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 10 pf ±10%, 100 vdc	930 173 204
M1-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001

M1 F-01

M5 F-01

M2 F-01

M6 F-01

M3 F-01

M7 F-01

M4 F-01

C1 0.033 μf
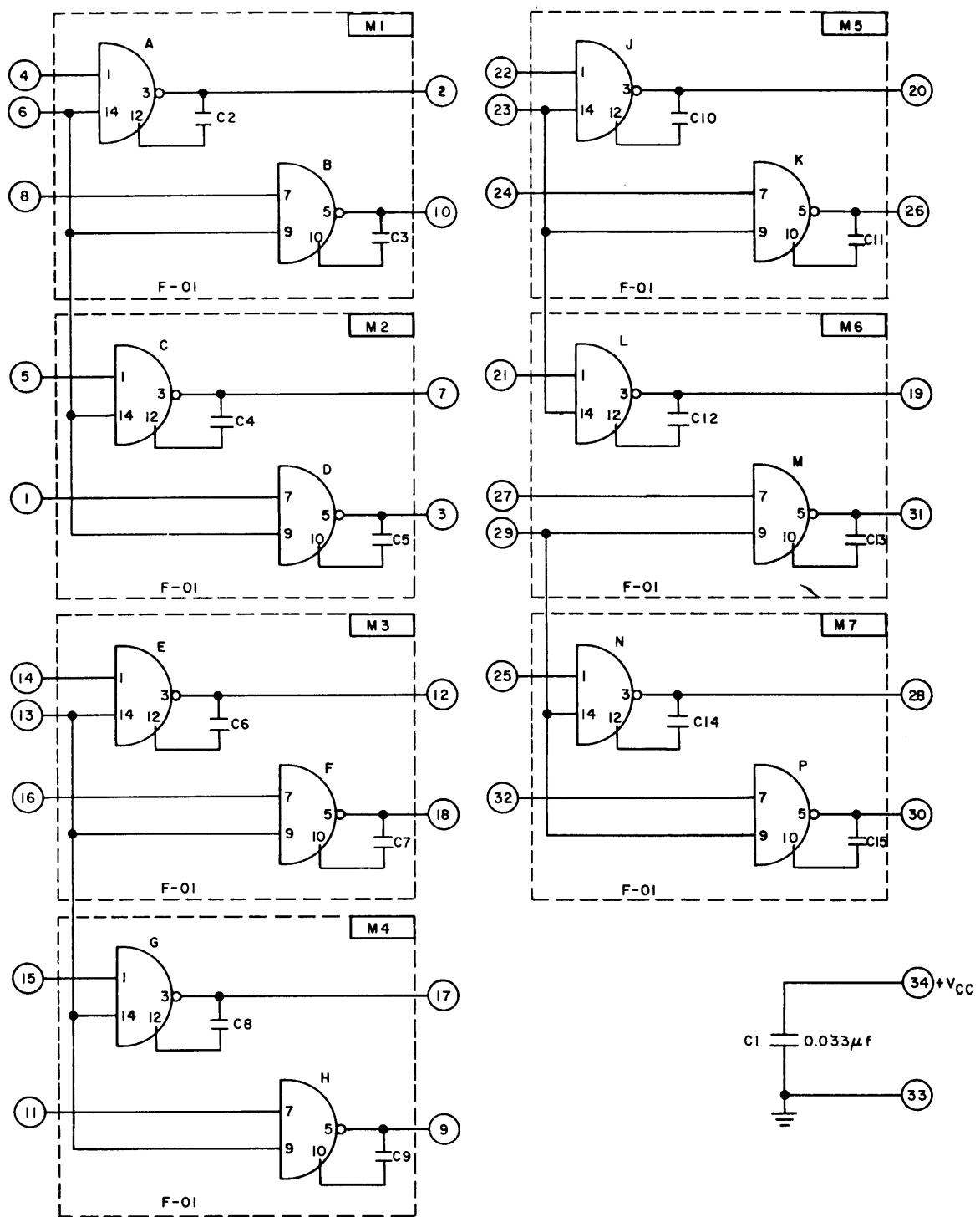
(1)- PIN NUMBER OF PAC

⊣2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

3997

Figure 1. Transfer Gate PAC, Model CC-152,
Schematic Diagram

TERMINATION PAC, MODEL CC-154

The Termination PAC, Model CC-154 (Figure 1), contains 27 diode clamp circuits to prevent input signals from overshooting below ground. In addition, the PAC has eight inputs which have 1K resistors connected from input pins to +6 volts.

SPECIFICATIONS:

Frequency of Operation	Current Requirements
5 mc	+6v: 50 ma

Input Loading	Power Dissipation
Inputs with resistors: 3 unit loads Inputs without resistors: 0 unit loads	300 mw (max.)

Electrical Parts List

| Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR27	DIODE	943 024 002
R1-R8	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049
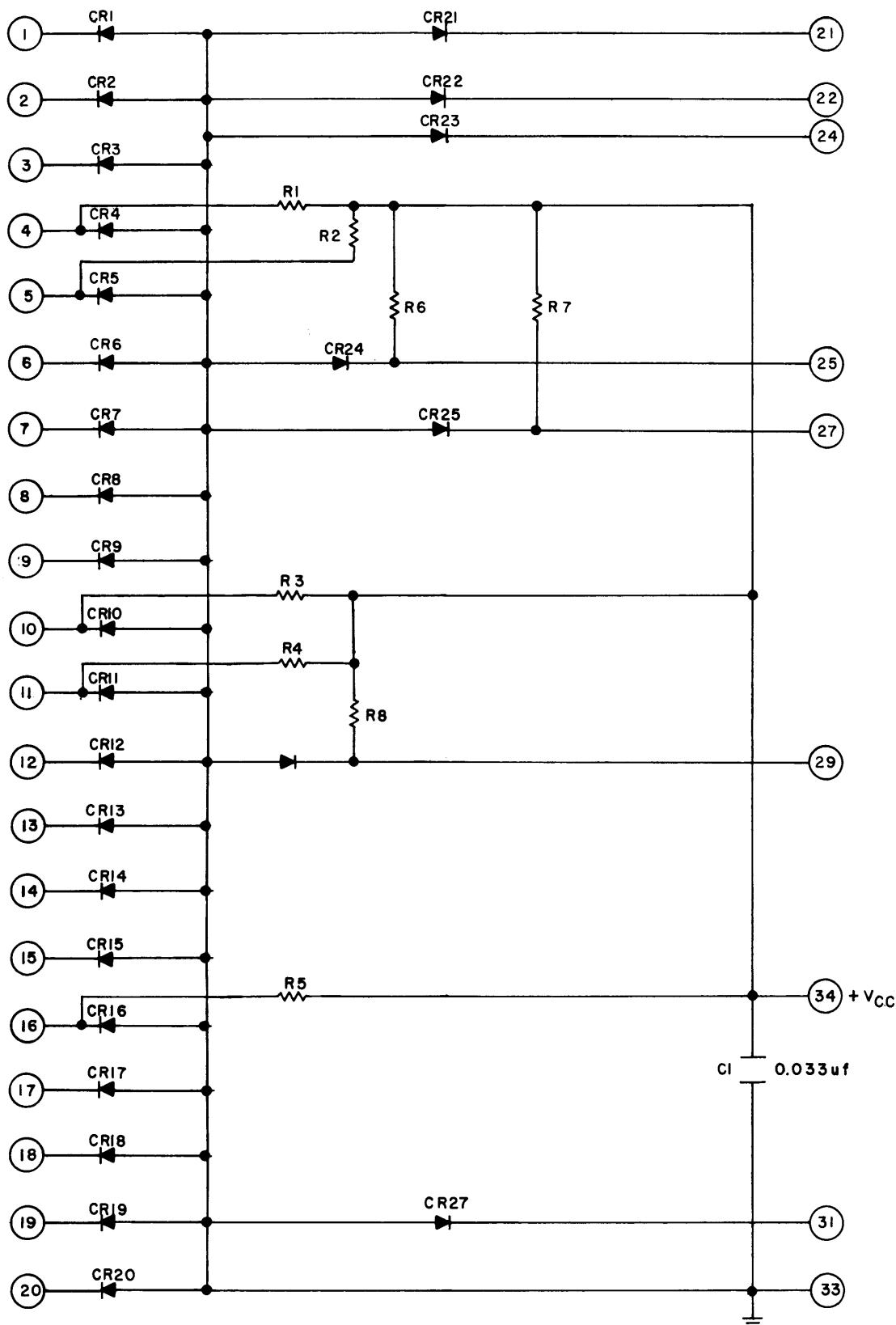
Figure 1. Termination PAC, Model CC-154,
Schematic Diagram

4017