B 0244

LINE PRINTER (B9247) I/O CONTROL

(FOR B700 SYSTEMS)

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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Introduction and Operation

INTRODUCTION

The B0244 line printer I/O control (IOC or DDP), hereinafter called the IOC, provides the interface between the B9247 Line Printer and the central processing unit to control the transfer of information to be printed. The printer operates at nominal rates of 400 lines per minute or 750 lines per minute with a 48-character set and single line spacing of six lines per inch. The interface capability is 750 LPM, however the enhanced print quality version is 400 LPM.

The IOC acts upon control words from the processor, performs the operation specified, and upon completion of the operation, generates a status word containing operation status and error status information. Processor internal codes (ASCII), representing the characters to be printed, are converted by the IOC into data representing chain position codes for the printer. (Refer to Table I-1.)

PROCESSOR INTERFACE

As shown in Figure I-1, interface communications between the IOC and the processor consist of input data lines (LUMIR08/ through LUMIR16/), output data lines (EXT01/, EXT12/, EXT15/, and EXT16/), and various control signals as follows:

PROCESSOR TO IOC

a. Enable Status Line (PSENSTn/). When false, PSENST/ initiates transfer of the status word from the IOC to the processor.
b. Read Line (PSREADn/). When false, PSREAD/ initiates a one-character data transfer from the IOC to the processor.
c. Write Line (PSWRITn/). When false, PSWRITn/ initiates a one-character data transfer from the processor to the IOC.
d. Instruction Line (PSINSTn). When true, PSINSTn indicates that the data on the MIR lines is a control word.
e. Clock Line (CDSCLKPn). Provides system clock pulses from the processor.
f. Clear Line (CGCLR). When true, CGCLR clears all control flip-flops in the IOC.

IOC TO PROCESSOR

a. Status Interrupt (SINT/). When false, SINT/ indicates that the IOC has a status word for the processor.
b. Data Interrupt (DINT/). When false, DINT/ indicates to the processor that the IOC is ready for another data transfer operation.

WORD FORMATS

The initiation of an information transfer between the processor and an IOC is the same for all devices, the distinction being in the device address contained in the base register (BR1 or BR2) of the processor output select gates. The port select unit decodes three bit groups from the processor to completely define the operation that is to take place. Nanobits 51 through 54 establish whether an operation is to be a device read or a device write. The four least significant bits of BR1 or BR2 contain the specific device address; the most significant bit of BR1/BR2, in conjunction with the type of operation, distinguishes between control, data, and status words. The word formats are illustrated in Figure I-2.

TABLE I-1. TYPICAL CHAIN PRINTER CODE SET, ASCII

Print Char.*	Printer Code	Print Char.*	Printer Code
0	0011 0000	P	0101 0000
1	0011 0001	Q	0101 0001
2	0011 0010	R	0101 0010
3	0011 0011	S	0101 0011
4	0011 0100	T	0101 0100
5	0011 0101	U	0101 0101
6	0011 0110	V	0101 0110
7	0011 0111	W	0101 0111
8	0011 1000	X	0101 1000
9	0011 1001	Y	0101 1001
.	0010 1110	Z	0101 1010
$	0010 0100	&	0010 0110
*	0010 1010	/	0010 1111
-	0010 1101	%	0010 0101
,	0010 1100	#	0010 0011
?	0011 1111	'	0010 0111
@	0100 0000	+	0010 1011
A	0100 0001	(	0010 1000
B	0100 0010	)	0010 1001
C	0100 0011	:	0011 1010
D	0100 0100	"	0010 0010
E	0100 0101	[	0101 1011
F	0100 0110	<	0011 1100
G	0100 0111	]	0101 1101
H	0100 1000	;	0011 1011
I	0100 1001	>	0011 1110
J	0100 1010	=	0011 1101
K	0100 1011	\	0101 1100
L	0100 1100	-	0101 1111
M	0100 1101	!	0010 0001
N	0100 1110	^	0101 1110
O	0100 1111		

* Listed in the sequence appearing on the print chain.

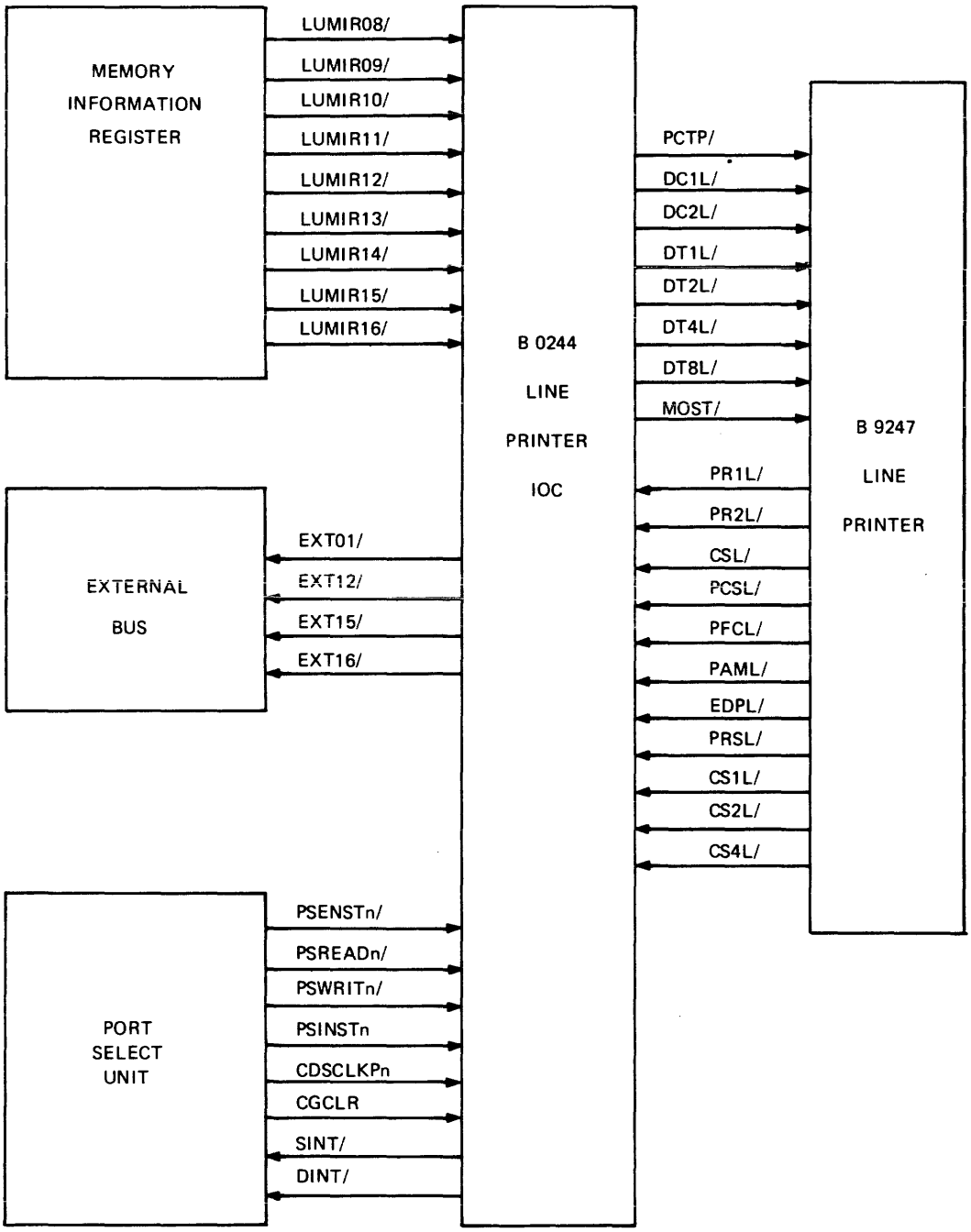


Fig. I-1 INTERFACE BLOCK DIAGRAM

Control Word

Operation of the line printer is initiated by transfer of a control word from the processor to the IOC. The control defines the function to be performed by the printer as follows:

MIR Bits	Function
1 through 7	Not used
8	Load Print Data: accept n characters (up to 132) and store them into the printer print buffer.
9 through 16	Format Control

The printer uses a 12-channel tape device for format control. The following codes define printer format control:

Bit Position								Operation
9	10	11	12	13	14	15	16	
0	0	0	0	0	0	F	0	No space
0	0	0	0	0	0	F	1	No space
0	0	0	0	0	1	F	0	Single Space
1	1	1	0	0	0	F	1	Single Space
0	0	0	0	1	0	F	0	Double Space
1	1	1	1	0	0	F	1	Double Space
0	0	0	1	0	0	F	0	Top of form – channel 1 skip
0	0	0	1	0	0	F	1	Top of form – channel 1 skip
0	0	1	0	0	0	F	0	Channel 2 skip
0	0	1	0	0	0	F	1	Channel 2 skip
0	0	1	1	0	0	F	1	Channel 3 skip
0	1	0	0	0	0	F	1	Channel 4 skip
0	1	0	1	0	0	F	1	Channel 5 skip
0	1	1	0	0	0	F	1	Channel 6 skip
0	1	1	1	0	0	F	1	Channel 7 skip
1	0	0	0	0	0	F	0	Channel 8 skip
1	0	0	0	0	0	F	1	Channel 8 skip
1	0	0	1	0	0	F	1	Channel 9 skip
1	0	1	0	0	0	F	1	Channel 10 skip
1	0	1	1	0	0	F	1	Channel 11 skip
1	1	0	0	0	0	F	0	Channel 12 skip
1	1	0	0	0	0	F	1	Channel 12 skip
1	1	0	1	0	0	F	1	Channel 13 skip - invalid on Channel 12 control

NOTES:

1. **F=0, execute print followed by specified format control.**
2. **F=1, execute specified format control only.**

	MSB 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	LSB 16
CONTROL WORD	---	---	---	---	---	---	---	LOAD PRINT DATA	FORM CONT. 7	FORM CONT. 6	FORM CONT. 5	FORM CONT. 4	FORM CONT. 3	FORM CONT. 2	FORM CONT. 1	FORM CONT. 0
DATA WORD	---	---	---	---	---	---	---	---	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
STATUS WORD	DATA REQUEST	---	---	DEV. ADDR 4	DEV. ADDR 3	DEV. ADDR 2	DEV. ADDR 1	DEV. ADDR 0	---	---	---	PRINT COMPL.	---	---	END OF PAGE	NOT READY

NOTE: DEVICE ADDRESS BITS OF STATUS WORD ARE INSERTED AT PSU.

Fig. I-2 LINE PRINTER IOC WORD FORMATS

Data Word

Data transfer between the processor and the IOC is in 8-bit parallel, where bit 16 of the data word is considered the least significant bit. The functions are as follows:

MIR Bits	Function
1 through 8	Not used
9 through 16	Data: eight bits transferred in parallel from processor to IOC and define the character to be printed.

Status Word

The status word is transferred from the IOC to the processor to notify the processor of a failure or functional condition. It consists of a device address which is inserted at the port select unit and a device status. The functions are as follows:

EXT Bits	Function
1	Data Request: IOC is ready to receive next character. This status condition follows the data interrupt signal to the processor.
2 through 3	Not used
4 through 8	Device Address: device address bits are inserted at the port select unit.
9 through 11	Not used
12	Print Complete: print buffer in printer is ready to be filled.
13 through 14	Not used
15	End of Page: an end-of-page marker has been sensed by the printer.
16	Not Ready: printer is not ready for operation because power is not on, gate is not closed, brush reader is not closed, hammer solenoid fuse is blown, paper runaway condition exists, or tractor switches did not detect paper.

PRINTER INTERFACE

The printer interface is illustrated in Figure I-1. The signals are as follows:

IOC TO PRINTER

a. Printer Column Timing Pulse (PCTP/). Provides the printer with a clock pulse at a rate of 250KHz. This signal is used by the printer to gate bit information into column storage and to advance the column counter.

b. Data Control Levels (DC1L/, DC2L/). Used for transfer of information or format control data to the printer. This function consists of two lines coded as follows:

DC2L/	DC1L/	
1	1	No action
1	0	Column storage load
0	1	Format transfer
0	0	Dummy format

c. Form Align Levels (DT1L/, DT2L/, DT4L/, DT8L/). Used in conjunction with DC1L and DC2L to transfer information or format control data to the printer. If DCnL = 10, a serial stream of data on DT1L transfers chain position codes to the printer for the line of characters to be printed. If DCnL = 01, all four lines are used to transfer format control information to the printer.

d. Motor Start Level (MOST/). Notifies the printer to start the motor. It is sent after a print command has been initiated if the printer is ready but the chain motor drive is off.

PRINTER TO IOC

a. Printer Ready Level (PR1L/, PR2L/). When false, PR1L/ designates the following printer status: power on, paper loaded, no slew alarm, train installed and locked in print position, and start button pressed. When PR2L/ is also false, the train drive motor is on. The first DC1L/ or DC2L/ received from the control initiates a print or paper motion operation. If the stop button is pressed, the execution of the stop command is inhibited until the indicated paper advance is completed, after which the printer goes to not ready. Ready levels change state only on the trailing edge of PCTP, and when PCSL is false, as follows:

PR2L	PR1L	State
0	0	Not ready
0	1	Ready, train motor off
1	0	Invalid code
1	1	Ready and train motor on

b. Chain Sync Level (CSL/). Occurs once per character set and specifies the beginning of a character set.

c. Printer Column Strobe Level (PCSL/). Printer is prepared to accept bit information into column storage.

d. Printer Final Column Level (PFCL/). Printer column counter is at 39, 59, or 65 for 80, 120, or 132 column printers, respectively. The printer will accept one additional information bit for the odd or even transfer.

e. Paper Motion Level (PAML/). Indicates format register load complete. Remains high until paper motion is complete. This signal is received from the printer in response to a format transfer command or dummy paper motion format.

f. End of Paper Level (EDPL/). End-of-page was sensed. This signal is received from the printer only in response to a single or double space command and is not transmitted otherwise.

g. Printer Speed Level (PRSL/). When true, this level indicates that printer interface capability is 750 LPM, and when false, indicates that the 400 LPM enhanced print quality version is used.

h. Code Set Level (CS1L/, CS2L/, CS4L/). Codes indicate the number of characters in the print character set of the printer as follows:

CS4L/	CS2L/	CS1L/	POSITION
1	1	1	Off or 1 for 64-character set
1	1	0	2 for a 48-character set
1	0	1	3 for a 16-character set
1	0	0	4 for a 96-character set
0	1	1	5 for a 48-character set
0	1	0	6 for a 48-character set
0	0	1	Not used
0	0	0	Not used

GLOSSARY OF TERMS AND SIGNALS

The following is a list of the mnemonics and names of signals used in the printer IOC:

Signal	Name/Function
CDSCLKPn	System clock
CGCLEAR	Clear
COMP	Print complete
CSL/	Chain sync level
CSnL/	Code set level
DCnLF	Device control level flip-flop
DCnL/	Device control level n
DINT/	Data interrupt
DTnL/	Data level
DTOL	Data out line
EDPL/	End of paper level
EXTn/	External bus bit n
ICPC	Increment chain position counter
ISPC	Increment scan position counter
LDBUF/	Load buffer
LUMIRn	Output from memory information register n
MOST/	Motor start level
PAML/	Paper motion level
PCSL/	Printer column strobe level
PCTP/	Printer column timing pulse
PFCL/	Printer final column level
PINC/	Increment buffer
PRnL/	Printer ready level
PRSL/	Printer speed level
PSENTn/	Enable status from port selector
PSINSTn	Port select instruction
PSREADn/	Port select read
PSWRITn/	Port select write
PTBCLA/	Buffer clear
PTBCSL/	Buffered chain sync level
PTBUSY/	Busy
PTCLR/	Clear
PTCND	Print cycle end
PTCTRY	Counter ready
PTDFI/	No space decode
PTDTOL	Data out line
PTIA	Data or forms level
PTICPC	Increment chain position counter
PTIOn	Inputs to ROM
PTIn	Chain position number
PTINC	Increment buffer
PTISPC	Increment scan position counter
PTJB	J input of busy flip-flop
PTMIR08/	MIR bus bit 8
PTPE	Parallel entry
PTPM	Paper motion
PTPMOL	Paper motion only flip-flop
PTn/	Chain position code to comparator
PTWSB/	Write strobe for print buffer
PT1ST	First cycle (400 LPM)
RDST	Read status
SCNRDY	Scan ready
SET/	Set
SINT/	Status interrupt
16	16-character code set level
48	48-character code set level
64	64-character code set level
96	96-character code set level

GENERAL OPERATION

A block diagram of the IOC operation is presented in Figure II-1. At the bottom of each block is the Printer IOC card designation (PTn) followed by the page numbers on which the logic circuits are contained.

All print data and paper motion commands are transferred to the IOC in 8-bit parallel form. Paper motion instructions are sent directly to the printer as DTnL under control of DCnL signals.

Print data signals are routed to a read-only memory (ROM) where a conversion is made from ASCII to a chain position corresponding to the location of the character on the chain. The chain position numbers are then loaded into the print buffer (RAM) in addresses 0 through 131. (These addresses correspond to the 132 print positions.) A control word is received by the IOC to print and space.

Whenever the printer is running, the IOC must continually monitor the chain position. A 250-KHz clock pulse is sent to the printer, which then responds with two timing signals: (1) CSL/, which is sent once at the beginning of each character set to reset the chain position counter in the IOC, and (2) PCSL/, which is sent once for each piece of type on the chain to increment the chain position counter. In this manner, the IOC continuously senses which chain position number is located at column 1 on the printer.

When a print operation is called for, a scan-ready signal is developed to initiate a scan and print cycle. The contents of the chain position counter are transferred in parallel into the scan position counter. The scan position counter is then incremented at the clock rate.

The address counter is also incremented and, at each column of the address, a comparison is made between the RAM contents and the scan position counter contents. For each column that compares, the DTOL signal is produced to set a flip-flop in the printer and fire the hammer in a particular column.

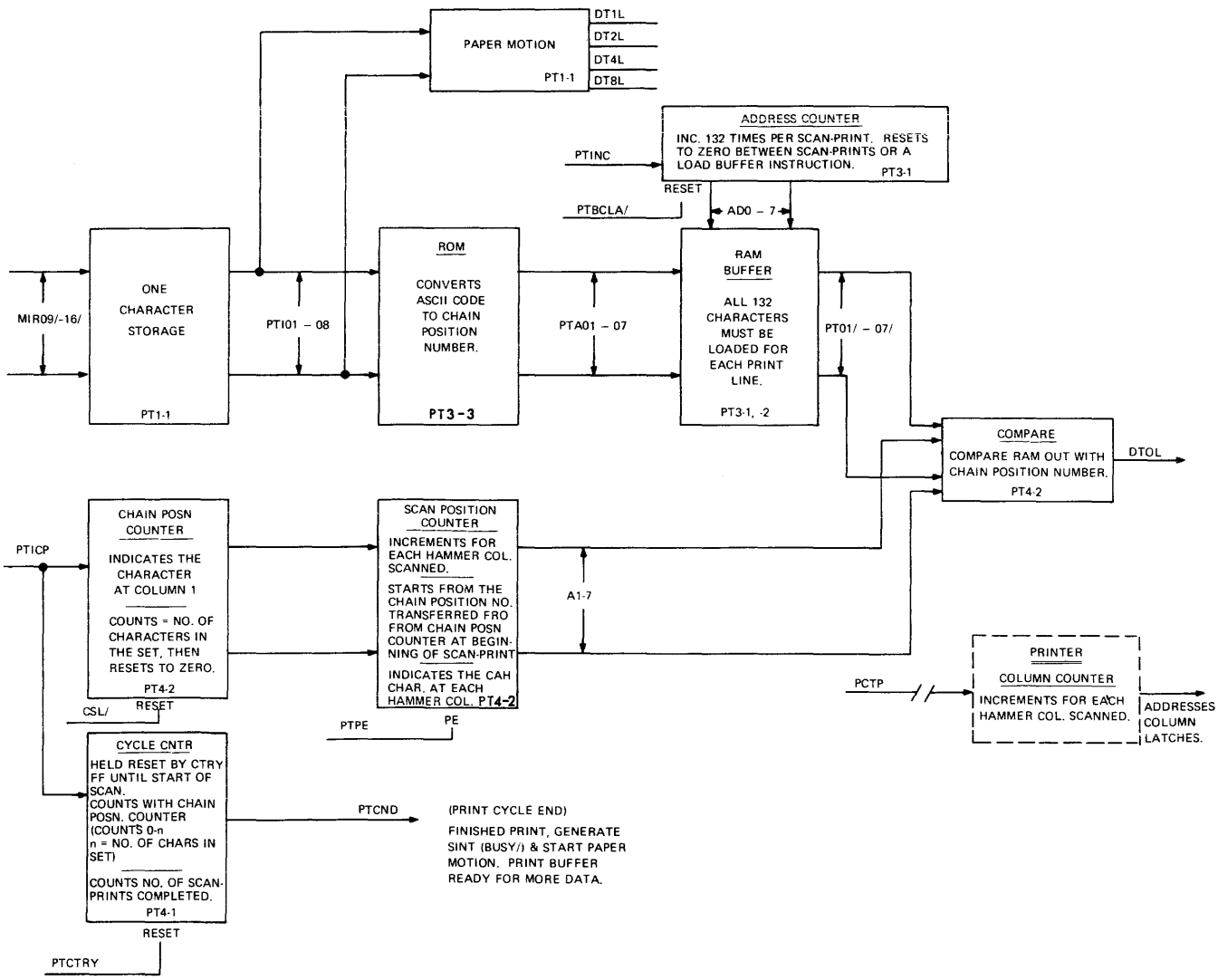


Fig. II-1 B0244 IOC BLOCK DIAGRAM

Functional Detail

Each even column is looked at before the chain is moved one type position. (See Figure II-2.) When the chain is moved one type position, the chain position counter and the cycle counter are incremented; then the entire even scan is repeated. This process continues until one complete set of print characters has rotated by column 1. At this time all even columns have been printed, PTCND is produced, and a dummy paper motion format is sent to the printer. The entire process is then repeated with a comparison of the odd columns on the chain, and a second PTCND is produced. When the entire line has been printed, a valid paper motion command is sent to the printer. While the paper motion is in progress, the processor can proceed to load the buffer with the next line of print. A flow diagram of the buffer load and print operation is presented in Figure II-3.

The 750-LPM printer has a hammer for each column. The odd column printing immediately follows even column printing requiring only one-half the time necessary to print a line of a 400-LPM printer.

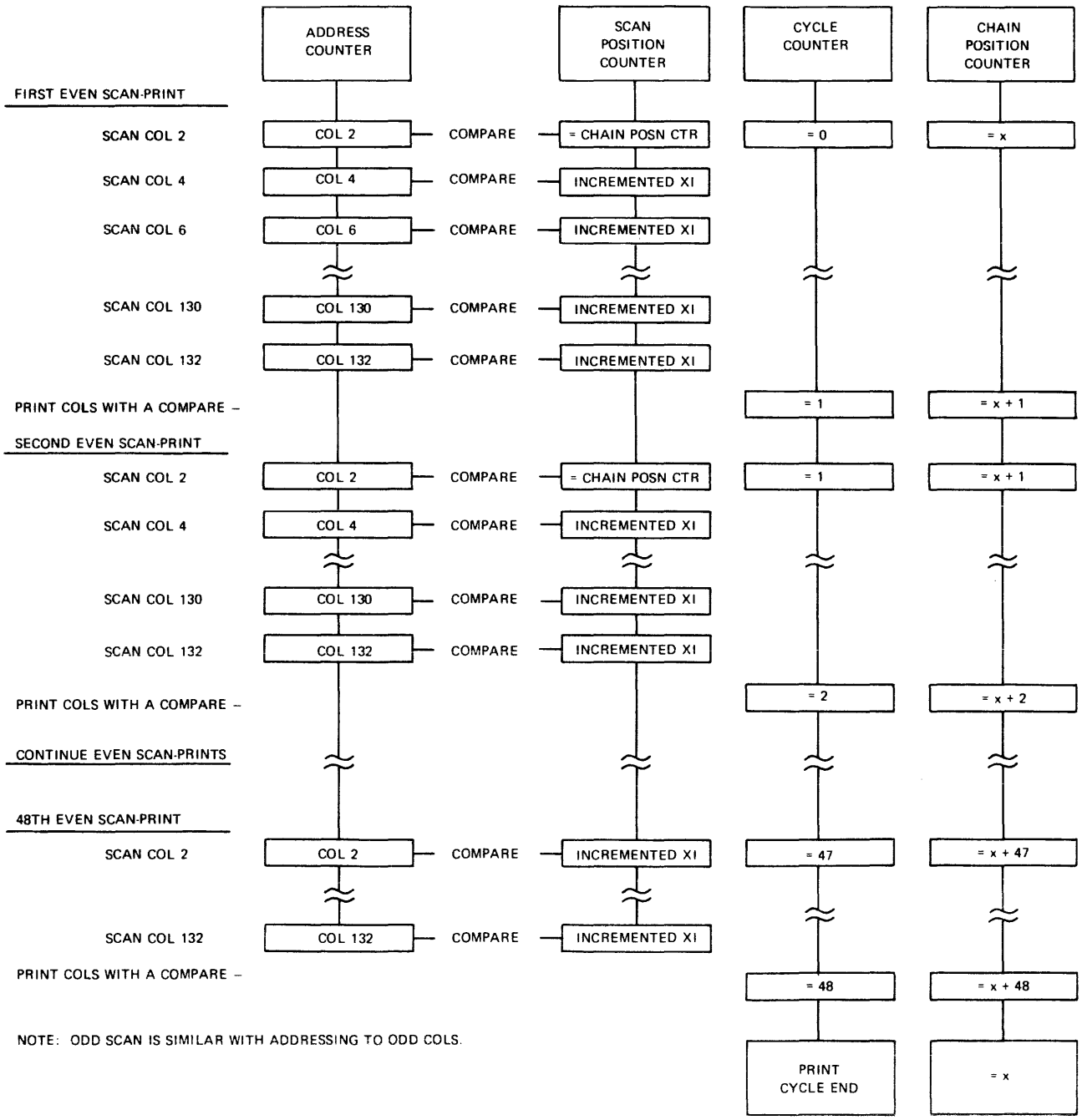


Fig. II-2 400 – LPM EVEN SCAN OPERATION

Functional Detail

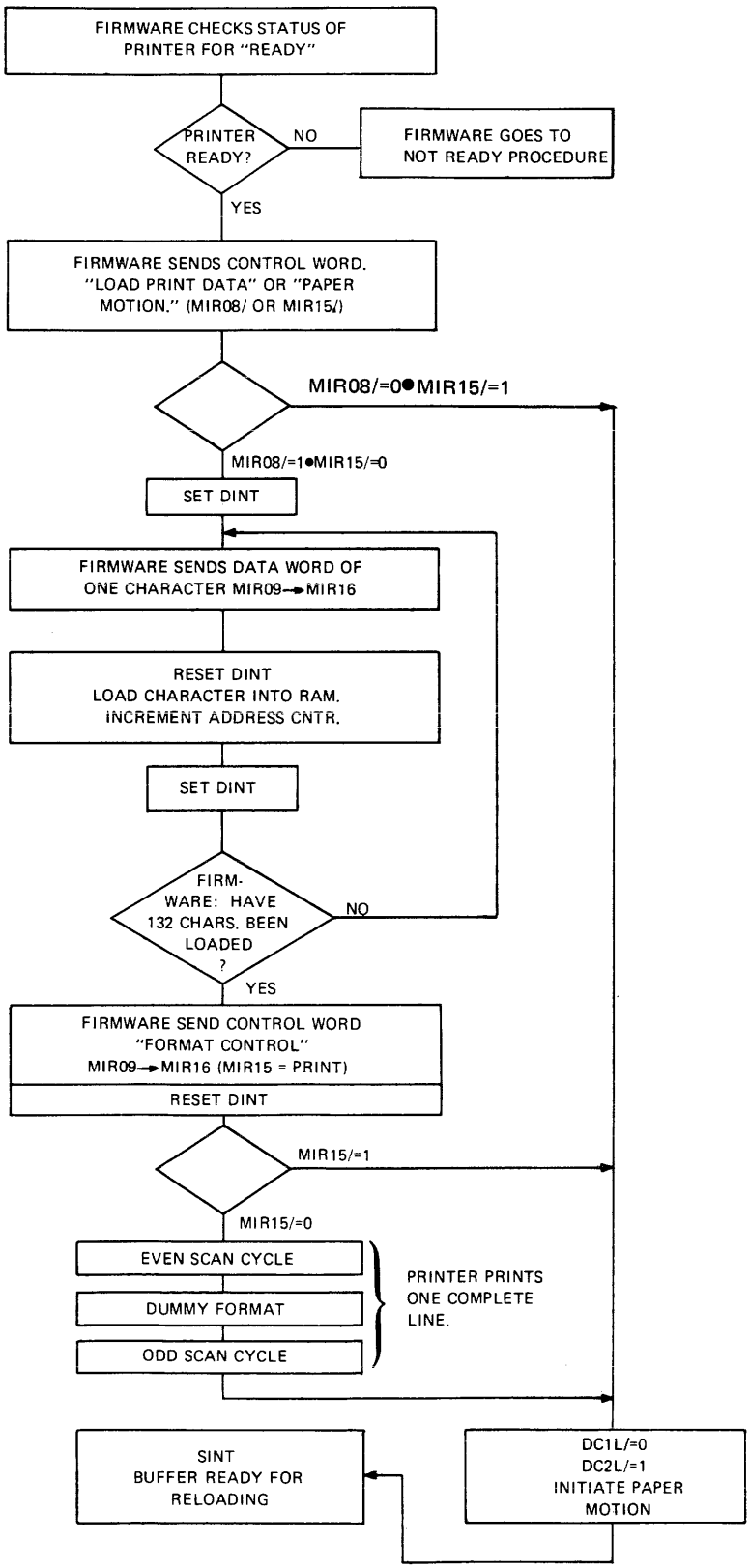


Fig. II-3 BUFFER LOAD AND PRINT OPERATION

LOGIC DESCRIPTION

CLOCK CIRCUIT

The IOC clock circuit logic is illustrated in Figure II-4. A basic operational timing diagram is shown in Figure II-5. The processor provides the IOC with clock pulses (CDSCLKPn) at a rate of 1 MHz. This clock is applied to a flip-flop which produces a square-wave output (2CTP) at the Q-side of 500-KHz (Figure II-4). 2CTP and PCLK produce a 500-KHz pulse which is applied to a second flip-flop resulting in clock outputs at 250-KHz. The outputs are the increment scan position counter (ISPC) signal and the printer column timing pulse (PCTP/).

The generation of the increment chain position counter (ICPC) signal is dependent on the level of PCSL from the printer. PCSL is true during the time that the IOC is scanning data to set up column strobe latches. During this time, the increment chain position counter (ICPC) remains false. When PCSL goes false, ARST goes true and results in the generation of ICPC when EVEN is true.

MOTOR START OPERATION

Signal MOST/, when false, notifies the printer to start the chain drive motor. MOST/ is false when PR1L/ is false, PTBUSY/ is false or PTPMOL is true, and PR2L/ is true.

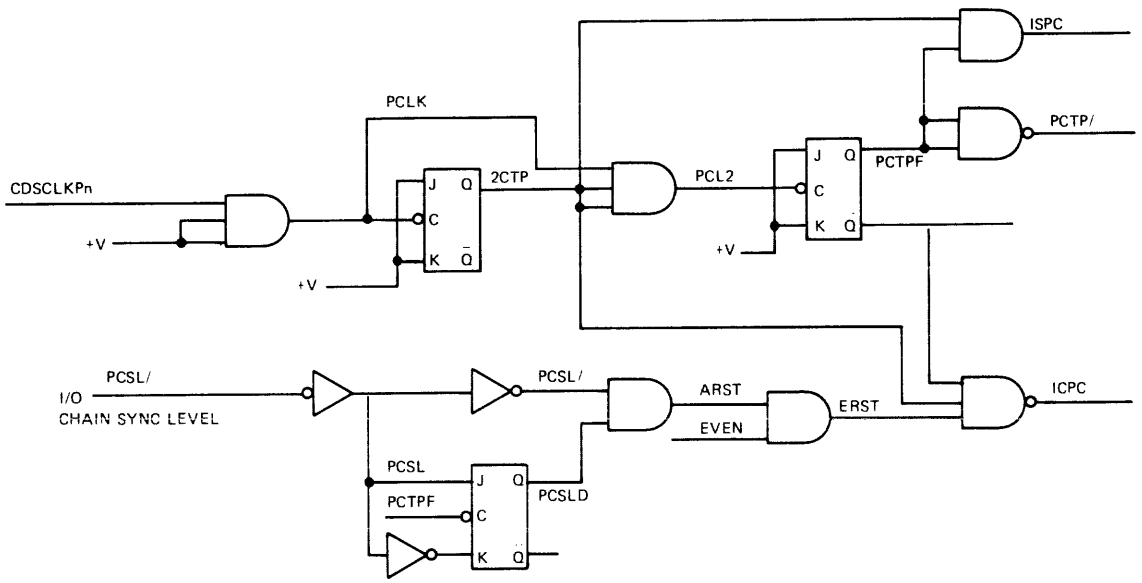


Fig. II-4 CLOCK CIRCUIT

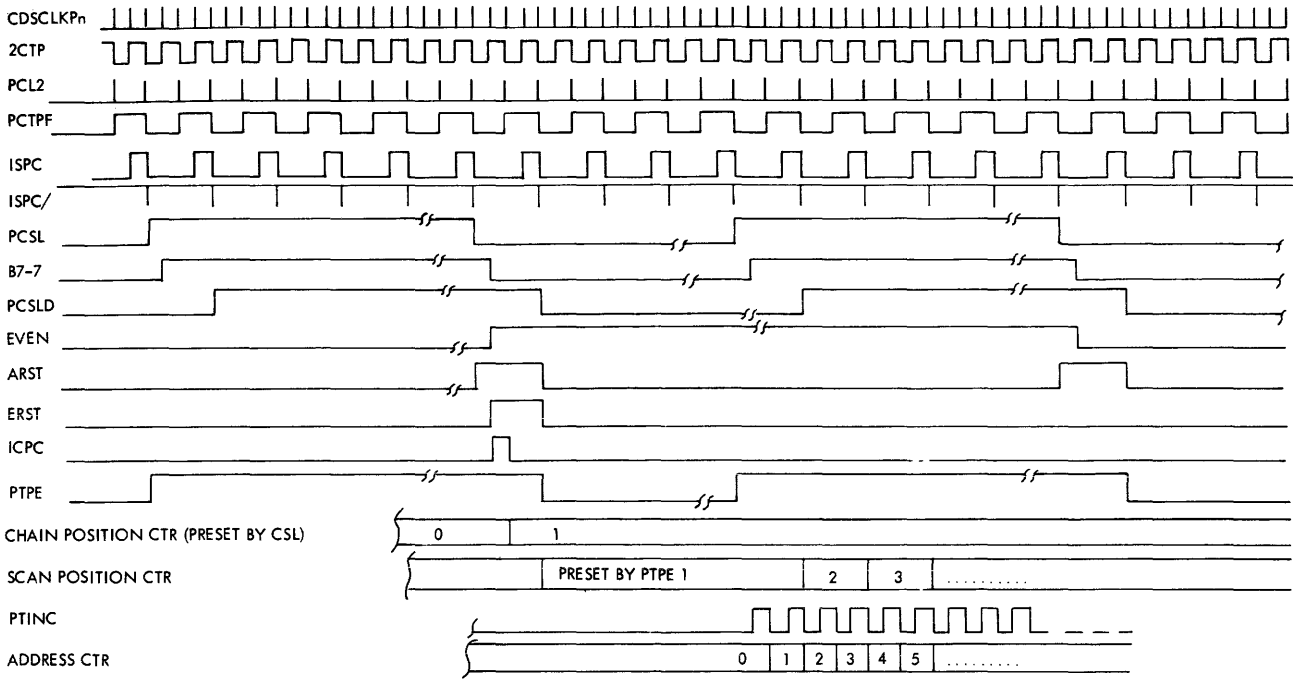


Fig. II-5 OPERATIONAL TIMING DIAGRAM

PRINT DATA OPERATION

Data Interrupt

The receipt of an instruction signal (PSINSTn is true) and a write signal (PSWRITn/ is false) from the processor specifies to the IOC that the information on the data lines is a control word. A false PTMIR08 indicates a load print buffer operation. (See Figure II-6.) The resulting false DINT/ signals the processor to start to send data to the IOC.

The IOC transfers a character from the data lines into two 4-bit registers. (See Figure II-7.) The character is shifted out of the register by a system clock pulse, converted to chain position data, and stored in the print line buffer. After storing the first character, PSINSTn goes false and the IOC generates a data interrupt (DINT/ is false) to request the next character. (See Figure II-8.) The data request is generated by the presence of an instruction signal (PSINSTn is true) and a read signal (PSREADn/ is false) resulting in the transfer of a true EXT01 signal to the processor.

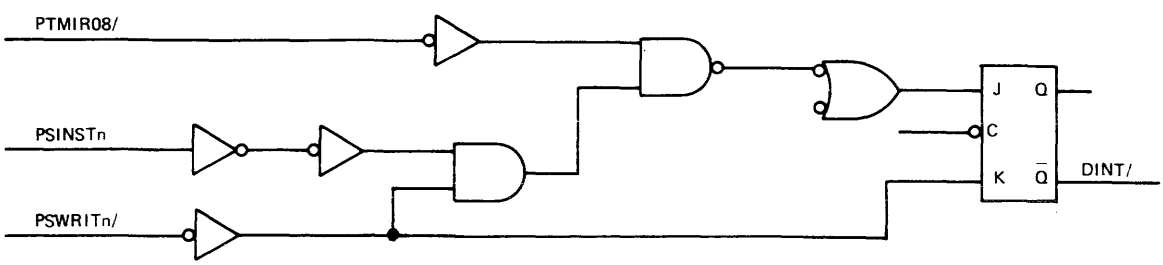


Fig. II-6 DINT FROM LOAD BUFFER CONTROL WORD

Functional Detail

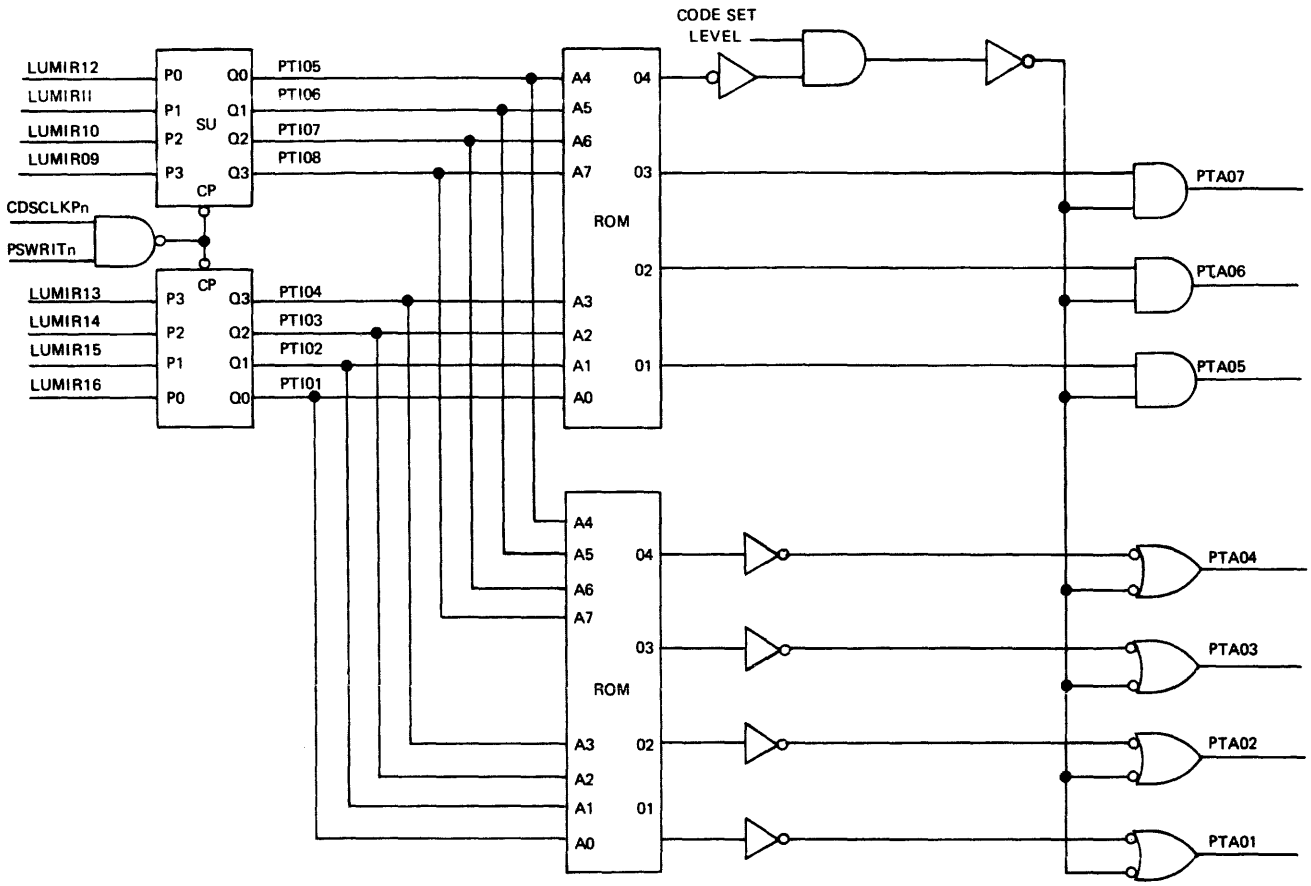


Fig. II-7 ASCII TO PRINTER LANGUAGE CONVERSION

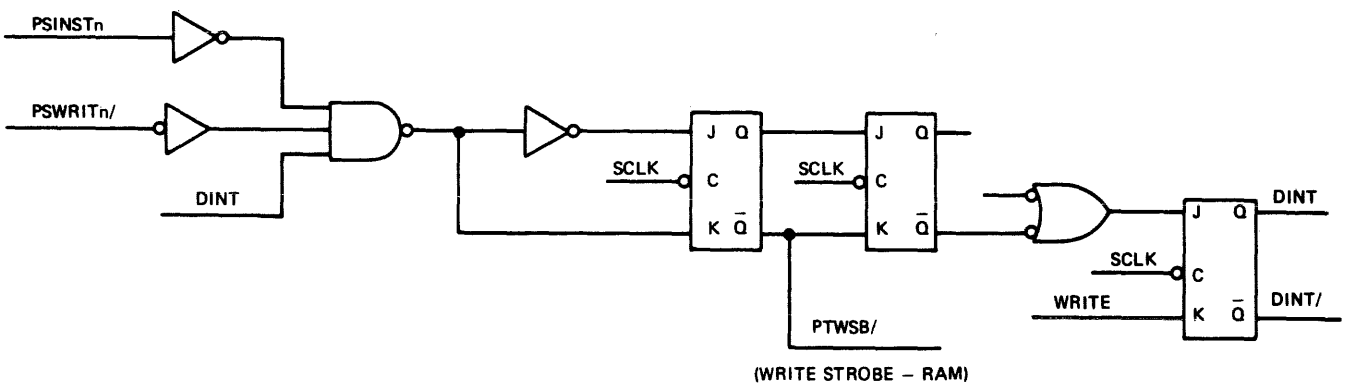


Fig. II-8 DINT AFTER LOAD OF EACH CHARACTER

Data Conversion

The outputs of the ROM are the chain-position equivalent of the ASCII character sent from the processor. The information is transferred to the print buffer when the proper character code set levels are present. The print buffer is a random-access memory (RAM).

Data Comparison

The address counter (Figure II-9) is incremented 132 times for each scan cycle by the increment buffer clock (PTINC). The address counter reset signal (PTBCLA/) is generated when the printer column strobe level (PCSL) goes false or the scan ready flip-flop (SCNRDY) is not set. The address counts are applied to each RAM chip on parallel lines. With PSWRITn and DINT/ false, the write strobe for the print buffer is generated (PTSWB/ is false) when PSINSTn goes low after each character store.

The data control levels (DCnL) indicate to the printer that either print or format control information is present on the data transfer lines. When DC2L/ is true and DC1L/ is false, the printer is notified that bit information is available to be transferred into the printer column storage. (See Figure II-10 for timing.)

Data for all even columns is transferred during the first PCSL of each PCSL pair, and the data for all odd columns is transferred during the second PCSL of each PCSL pair.

For the 400-LPM printer, the printing of even columns is completed and is followed by a dummy format transfer (DC1L/ and DC2L/ are false), causing PAML/ to go false for approximately 16 milliseconds. When PAML/ goes true, the printing of odd columns is followed by the normal format transfer. During the printing of the odd columns, the first of each pair of PCSL's is ignored. During the printing of even columns, the second of each pair of PCSL's is ignored.

Print Complete

After printing is complete, the IOC returns a print complete status word (RDST and COMP are true). A cycle end (PTCND is true) and a first cycle not (PT1ST/ is true) produce a status interrupt (SINT/ false) to indicate to the processor that the buffer is ready for more data. (See Figure II-11.) SINT is reset at the system clock during status interrogation.

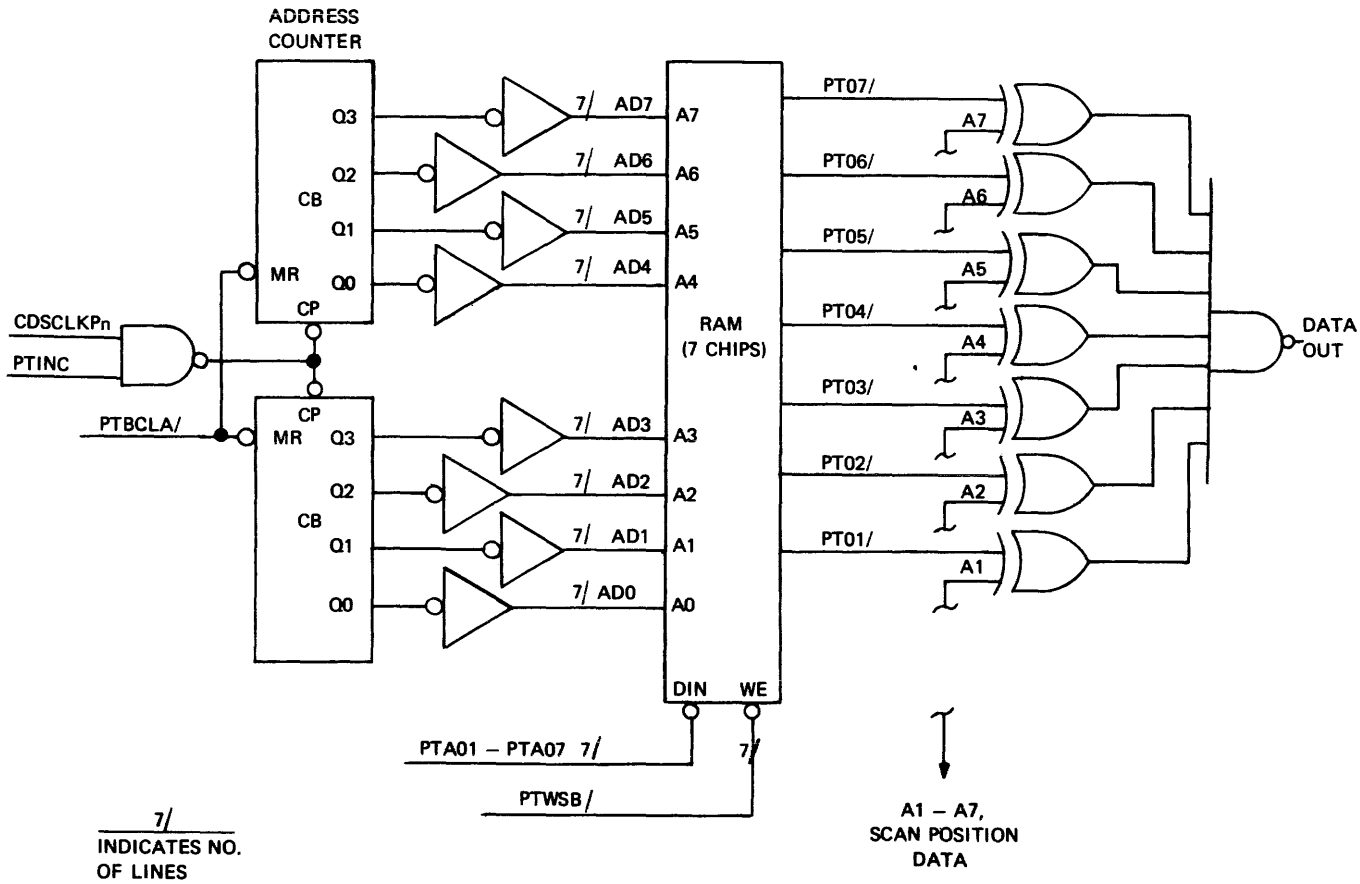


Fig. II-9 DATA COMPARISON

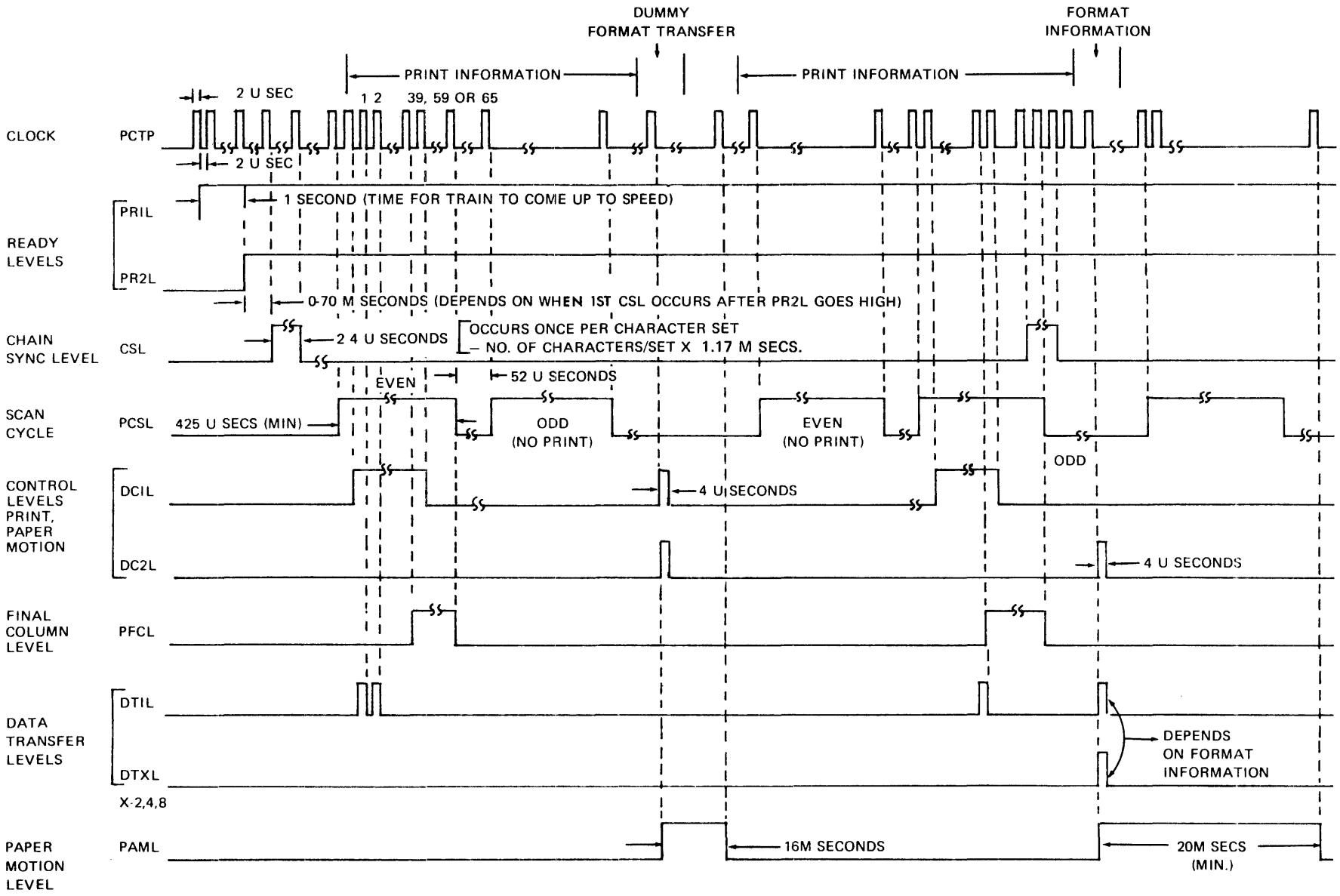


Fig. II-10 TIMING DIAGRAM FOR 400 LPM PRINTER

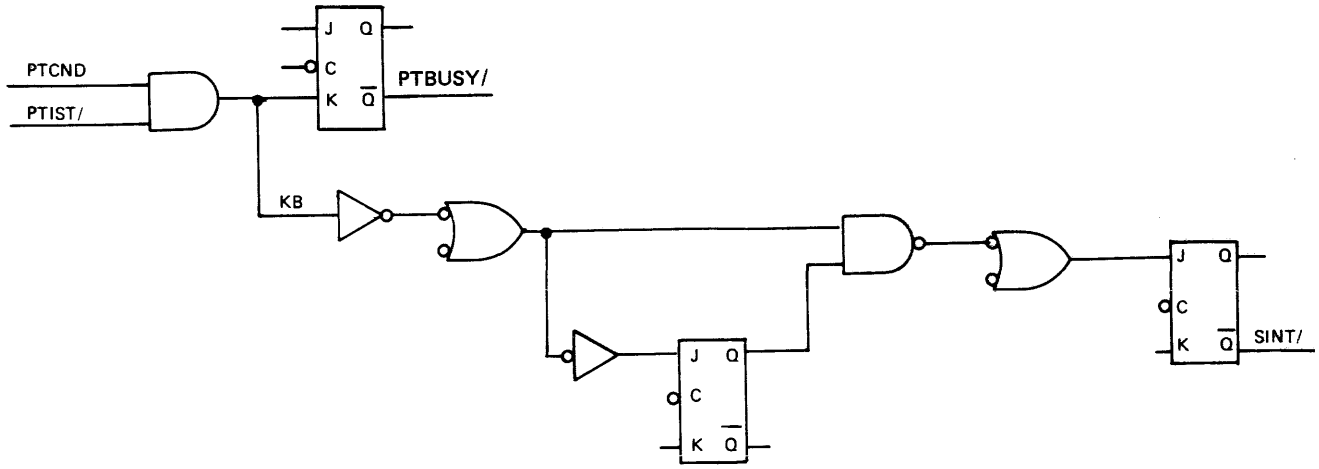


Fig. II-11 SINT, BUFFER READY FOR MORE DATA

FORMAT CONTROL OPERATION

When bit 15 of a control word is false (LUMIR15/ is true), the IOC initiates printing of a line and follows with the specified format control. When bit 15 of a control word is true (LUMIR15/ is false), the IOC initiates only the specified format control.

Paper Motion Selection

When a write signal (PSWRITn/ is false) and an instruction signal (PSINSTn is true) are received from the processor, signal WRC is generated. The presence of WRC, printer ready level (PRIL), printer not busy (PTBUSY), and MIR15 causes the paper motion only (PTPMOL) flip-flop to be set. (See Figure II-12.)

No Space Decode

A no space decode signal (PTDFI/ is false) is present whenever there are no data on the MIR09 through MIR14 lines (LUMIR09/ through LUMIR14/ are true). A false PTDFI/ generates a true DC2L/ signal which inhibits format transfer to the printer.

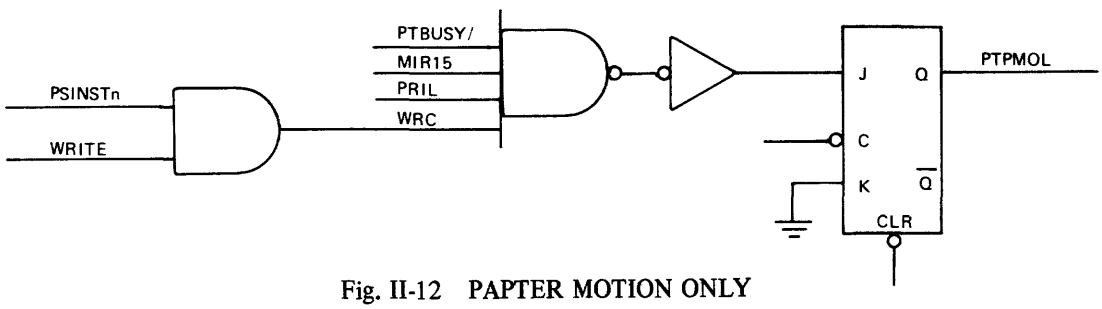


Fig. II-12 PAPTER MOTION ONLY

Form Alignment Levels

Format control data is transmitted over the LUMIR data lines, LUMIR09 through LUMIR16. The data are applied through a register to the 1 inputs (Figure II-13) of a multiplexer. The 0 inputs to the multiplexer are always true. When LUMIR13 and LUMIR14 are both true, the select (SEL) line to the multiplexer is false and the 0 inputs are applied to the four outputs lines of the multiplexer. When LUMIR13 or LUMIR14 are false, a true is applied to SEL and the 1 inputs are selected as the outputs of the multiplexer. The outputs, form alignment levels DT1L/, DT4L/, and DT8L/, are applied to the printer. The DT1L/ form alignment is present when PTIA is true, the DC2L flip-flop is set (DC2LF is true), and the DC1L flip-flop is reset (DC1LF/ is true). Thus, with DC2L true and DC1L false, data lines DT1L, DT2L, DT4L, and DT8L are used to transfer format information to the printer. The states of the data transfer lines (DTXL) result in the following:

DTXL = 0	No advance
DTXL = 1	Advance to heading position
DXTL = 2-11	Skip to designated channel position
DTXL = 12	Skip to channel-12 position
DTXL = 13	Skip to next designated channel position or end of page position. DXTL = 13 invalid for 12-channel format tape option.
DTXL = 14	Single space
DTXL = 15	Double space

When the format register in the printer is loaded, a paper motion level (PAML/ is true) signal is sent to the IOC. This signal remains true until paper motion is complete. When PAML/ goes false, the DC2L flip-flop is reset and DC2L/ goes true to inhibit format transfers.

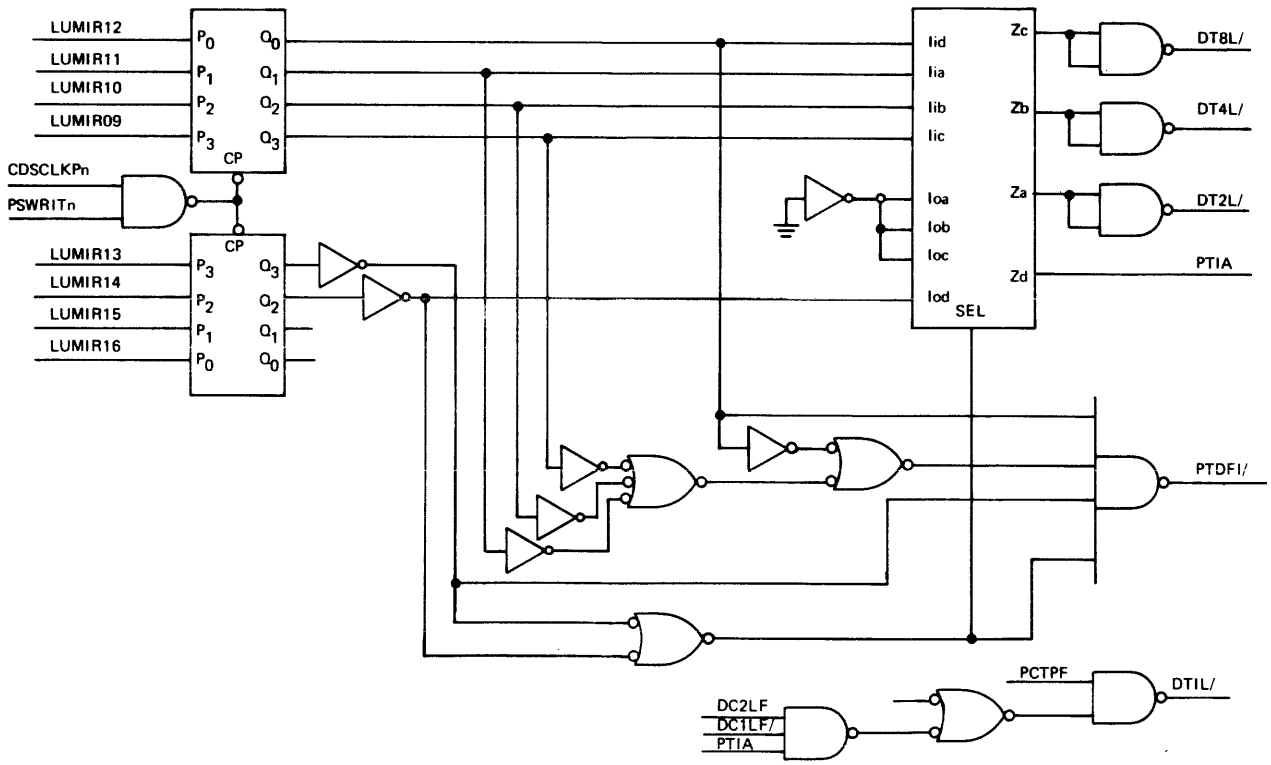


Fig. II-13 FORMAT CONTROL DATA

Circuit Detail

INTRODUCTION

Most of the IC chips (modules) used in the B0244 Printer IOC are also used in the Processor. The IC's used in both units are described in the Central Processing Unit FETM; the IC's unique to the Printer IOC are described in this section.

TWO-INPUT POSITIVE NAND GATE (1447 0240) AND TWO-INPUT POSITIVE NAND BUFFER (1447 9596)

The NAND gate module and the NAND buffer module are shown in Figure III-1. The functional operation of the NAND buffer is identical to the functional operation of the NAND gate; however, because of its higher driving capability, it is referred to as a buffer rather than a gate. The NAND circuits operate such that a low-level output is produced only when both inputs are high. When either or both inputs are low, a high level output is produced.

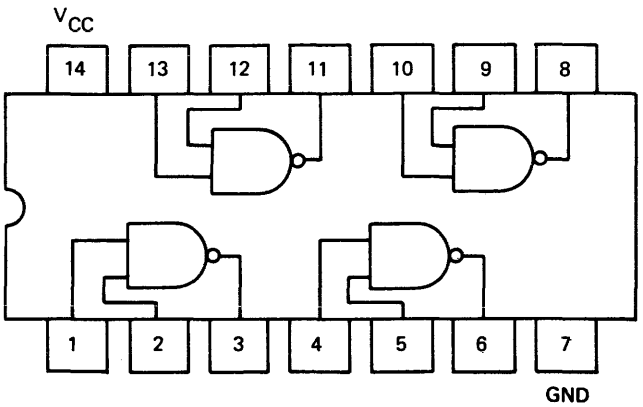
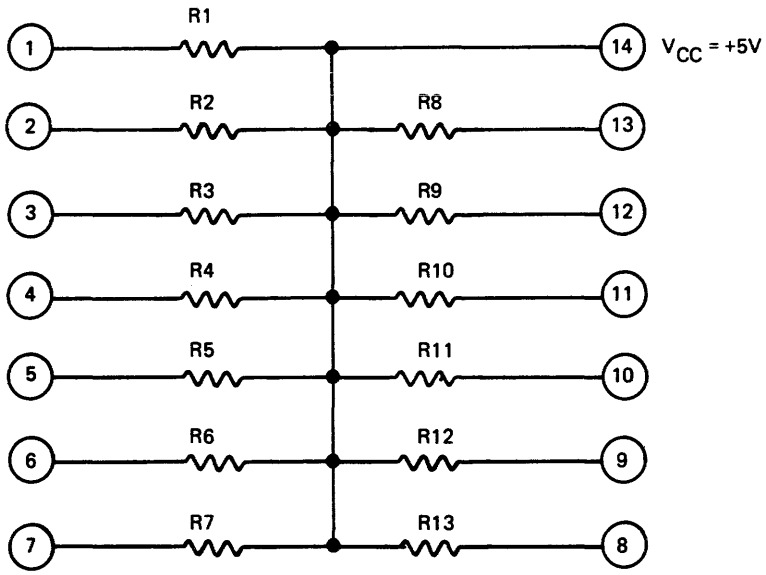


Fig. III-1 TWO-INPUT POSITIVE NAND BUFFER (1447 9596) AND TWO-INPUT POSITIVE NAND GATE (1447 0240)

RESISTOR MODULE (1448 2319)

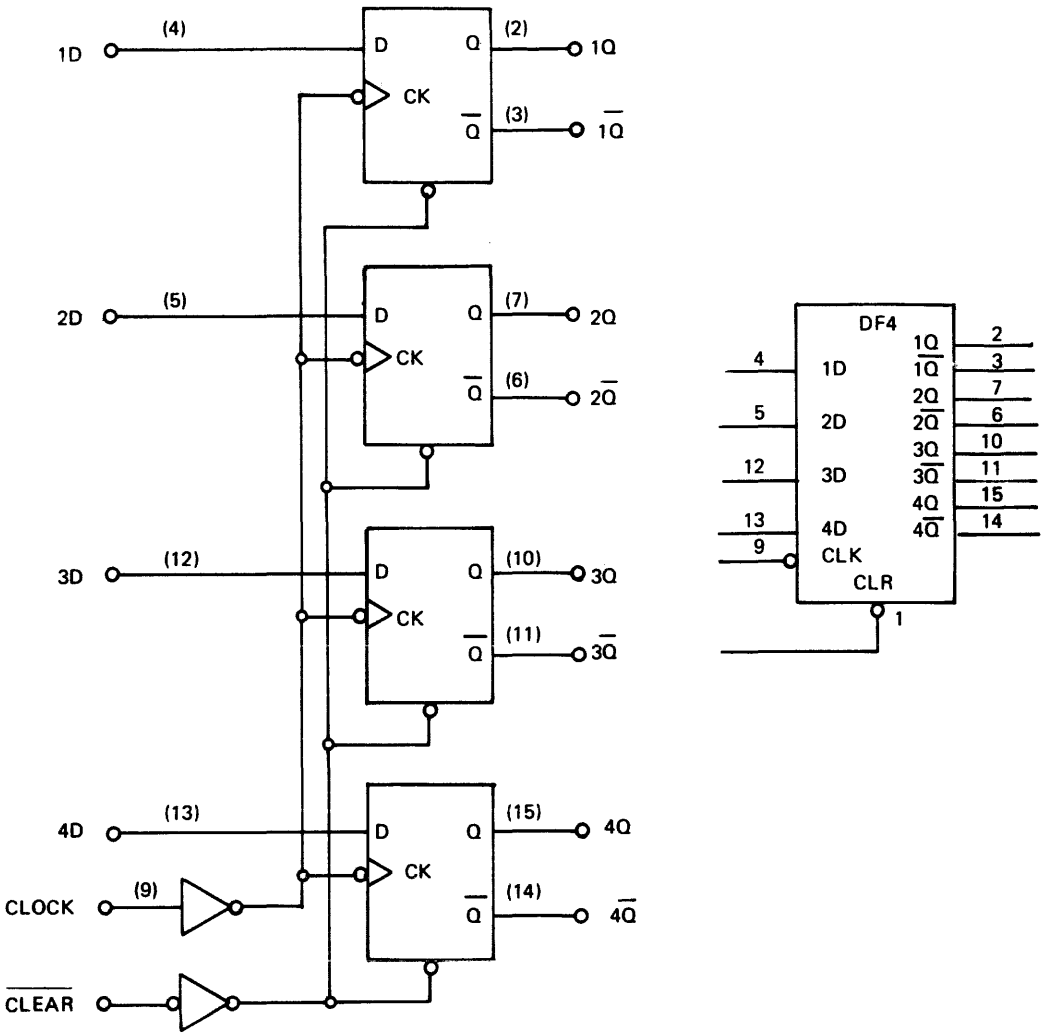
The resistor module, illustrated in Figure III-2, is comprised of 13 1.5K resistors used as pullup resistors.



RESISTOR NO.	RESISTANCE (25°C)	MAX. OPERATING POWER DISSIPATION (70°C)
R1 THRU R13	1.5K ±5%	50MW

Fig. III-2 RESISTOR MODULE (1448 2319)

Circuit Detail



NUMBERS IN PARENTHESIS INDICATE PIN NUMBERS

V_{CC} PIN 16

GROUND PIN 8

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

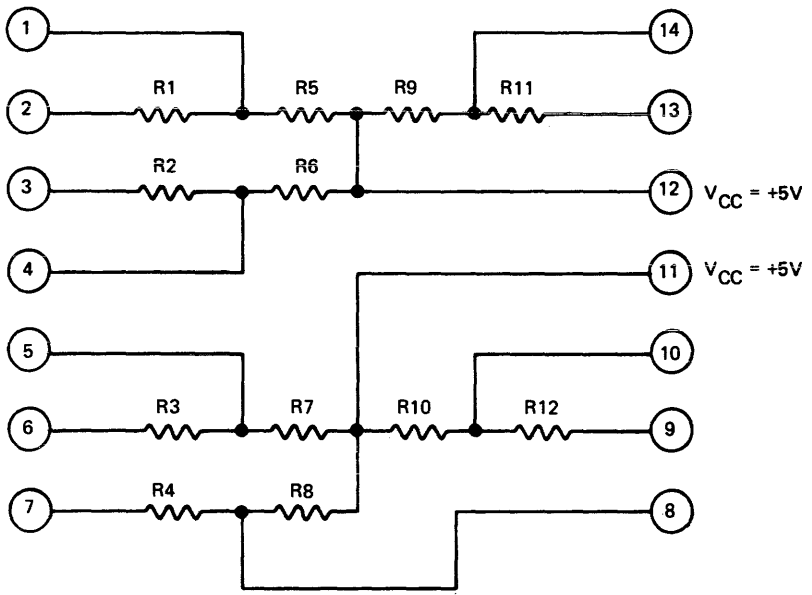
Fig. III-3 QUAD D-TYPE FLIP-FLOP (1449 1278)

QUAD D-TYPE FLIP-FLOP (1449 1278)

The D-type flip-flop module is illustrated in Figure III-3. The flip-flops have a direct clear and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. A low-level signal to the clear input sets Q to a logical 0 level. The clear inputs to each flip-flop are independent of the clock.

RESISTOR MODULE (1449 5396)

The resistor module illustrated in Figure III-4 is comprised of six 402-ohm resistors and six 237-ohm resistors which are arranged such that a variety of resistive values can be tapped at the pins. These resistance values are used for pullup functions.



RESISTOR NO.	RESISTANCE (25°C)	MAX. OPERATING POWER DISSIPATION (70°C)
R1, R2, R3, R4, R11, R12	402Ω ±2%	125 MW
R5, R6, R7 R8, R9, R10	237Ω ±2%	250 MW

Fig. III-4 RESISTOR MODULE (1449 5396)

Maintenance Procedures

MAINTENANCE PHILOSOPHY

The approach used in detecting, diagnosing, and repairing failures in the printer IOC is to run the appropriate Maintenance Test Routines (MTR'S) and then replace or repair defective circuit chips or discrete components in accordance with the diagnostic information obtained from the MTR'S. Additional manual diagnostic operations, using this technical manual, FT&R documentation, and test equipment may be required by the Field Engineer to further diagnose and repair failures if the MTR'S do not locate the defective component/circuit.

MAINTENANCE AIDS AND EQUIPMENT

The following maintenance aids are required to implement the MTR'S and perform maintenance on the IOC:

a. Field Engineering (F.E.) cards FE-1 through FE-4.
b. MTR meter.
c. Tektronix Model 453 oscilloscope.
d. Processor card extender kit (1447 7102).
e. Applicable MTR'S.
f. Special maintenance tools (insertion/extraction, wire wrap/unwrap, pin extractor, and card puller tools).

The B700 Processor Technical manual, form 1064482 Section V, contains descriptions and identification/application data for the F.E. cards, MTR meter, and card extender kit.

MAINTENANCE TEST ROUTINES (MTR'S)

Each B700 system installation is provided a set of MTR'S, on system-compatible media, tailored to the installation configuration and revision level. The MTR Configuration Document (2601 8200), issued by the respective branch office to each installation, provides a complete list of MTR reference data, including the revision status and applicability.

The MTR provided for the B0244 printer IOC is the PMTR (2602 9678). A program listing, complete operating instructions, a failure dictionary, and waveforms are provided in the PMTR Operator Instructions Document (Listing), 2602 9660.

When implemented, the PMTR detects and diagnoses failures within the IOC, or validates the operation of the IOC and interfacing printer. The PMTR cannot diagnose a failure in the printer, but can be interpreted to indicate or point to a failure in the printer.

Note that, for complete diagnosis or validation of the IOC and the printer operations, the FEMT, MEMLDR, PROC, BSW, MCU, CONS or CONS96 (or SPO in B771), and DPM MTR's must be run in the sequence indicated before the PMTR is run. Refer to Section V of the B700 Processor Technical Manual, form 1064482 for a description of the MTR implementation and diagnostic process.

Installation Procedures

INSTALLATION PACKAGE

The B0244 IOC installation package is comprised of the following items:

a. Four printed circuit cards, PT1 through PT4.
b. Two frontplane connectors (1534 3940).
c. One adapter cable.
d. Two backplane templates.
e. One identification decal.

Table VI-1 (B711 Processor) and Table VI-2 (B771 Processor) identify the four IOC circuit cards and their functions, along with corresponding IOC/DDP backplane location and cable connections for installation in the interchangeable IOC/DDP location areas.

INSTALLATION PROCEDURE

Ensure that all items in the IOC installation package are available, then proceed as follows:

1. After the I/O service priority has been established for the IOC (Section VIII of form 1064482), install cards PT1 through PT4 in the corresponding card slots of the selected IOC/DDP location. (Refer to Table VI-1 or Table VI-2.)
2. Connect one frontplane connector to card pair PT1 and PT2; connect another frontplane connector to card pair PT3 and PT4.
3. On wiring side of backplane, slide the large template over the backplane pins for selected IOC location.
4. On the wiring side of backplane, slide the small template over backplane pins for the appropriate I/O connector listed in Table VI-1 or Table VI-2.
5. Attach 50-pin connector of the adapter cable which has the strain relief bracket, to appropriate I/O connector on insertion side of the backplane.
6. Secure circuit card connector on the other end of adapter cable to location J24 on adapter panel using number 6-32X5/16" pan head screws, number 6 lockwashers and number 6 knurled nuts which are provided.
7. Affix the decal, which identifies the control and contains the serial number, to IOC decal corresponding to the IOC location.
8. Check +5 volt power as described in +5-volt Tap Adjustment Procedure in Volume 1 of the Processor FT&R document.
9. Connect I/O cable to printer.
10. Run appropriate MTR'S to ensure proper system operation.

Card			DDP Location, Card Slots, and Cable Connector						
Type	Part No.	Function	1(J97)	2(J96)	3(J95)	4(J94)	5(J93)	6(J92)	7(J91)
PT1	1448 0016	Control	FW6	DW6	FV4	DV4	FU2	DU2	DT0
PT2	1448 0032	Data 9-16	FW3	DW3	FV1	DV1	FT9	DT9	DS7
PT3	1448 0057	Data 1-8	FW0	DW0	FU8	DU8	FT6	DT6	DS4
PT4	1448 0073	Special	FV7	DV7	FU5	DU5	FT3	DT3	DS1

TABLE VI-1. B711 PRINTER IOC CARDS, LOCATIONS, AND CONNECTORS

Card			DDP Location, Card Slots, and Cable Connector					
Type	Part No.	Function	2(J96)	3(J95)	4(J94)	5(J93)	6(J92)	7(J91)
PT1	1448 0016	Control	DW6	FV4	DV4	FU2	DU2	DP1
PT2	1448 0032	Data 9-16	DW3	FV1	DV1	FT9	DT9	DN8
PT3	1448 0057	Data 1-8	DW0	FU8	DU8	FT6	DT6	DN5
PT4	1448 0073	Special	DV7	FU5	DU5	FT3	DT3	DN2

TABLE VI-2. B771 PRINTER IOC CARDS, LOCATIONS, AND CONNECTORS