B 0311/B 0418

CARD PERIPHERAL I/O CONTROLS

(For B700 Systems)

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

INTRODUCTION AND OPERATION

FUNCTIONAL DETAIL

CIRCUIT DETAIL

MAINTENANCE PROCEDURES

INSTALLATION PROCEDURES

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INTRODUCTION

This manual covers the B0311 and B0418 reader-punch I/O controls (IOC'S). The B0311 reader-punch I/O control is used to interface a B700-series processor with the 96-column A9119 and A9419 series card readers-punches. The B0418 reader punch I/O control is used to interface a B700 series processor with the 80-column A9418 card reader-punch. The B0311 and B0418 are identical in terms of hardware; they differ only in the software applications. In this manual, the B0311 and B0418 are referred to as the reader-punch IOC. The reader-punch IOC provides the necessary control functions for directing card read and card punch operations and also provides the buffering required for transferring information to and from the card reader-punch.

The reader-punch IOC consists of four plug-in chip boards (RC1, RC2, RC3, and RC4) which can be located in any of the interchangeable Device-Dependent Ports (DDP's) in the processor logic rack. (Refer to Section VI.) All operating voltages are derived from the internal power supplies of the processor cabinet.

CARD READER-PUNCH INTERFACE

The standard interface for the card reader-punch peripherals consists of two 25-pin connectors, serviced by two I/O signal cables. One connector and one cable are used for reader units; the other cable and connector are used for punch-print units. Any unit capable of reading, punching, and printing (such as the A9419-2) uses two cables and connectors.

The pin assignments and signal names for the I/O connectors are shown in Figure I-1. It should be noted that the interface is capable of handling either 96- or 80-column card codes. Some of the signals are time-shared; that is, the line may transmit data or control signals at different points of time in the peripheral operation. Also note that, because either or both of the I/O connectors may be used with different styles of peripherals, some controls are transmitted through both I/O cables.

As shown in Figure I-1, control signals and data are interchanged between the reader-punch IOC and the card reader-punch peripheral. These signals are transferred as false levels and are defined in the signal glossary provided at the end of this section.

IOC/READER-PUNCH OPERATIONS

When the processor sends a control word, with the punch and/or print instruction bits set to the reader punch IOC, the IOC effects the feeding of the card in the visible station through the punch and print stations and to a selected stacker. When the card is approximately half-way through the punch station, the next card (if required) may be released from the selected hopper, read, and then left in the visible station.

The data required to be printed and/or punched is sent to the peripheral and loaded into a memory, called the punch buffer, prior to the card moving out of the visible station. If a separate print operation is required, the card pauses in the punch station while the processor transmits the required print data.

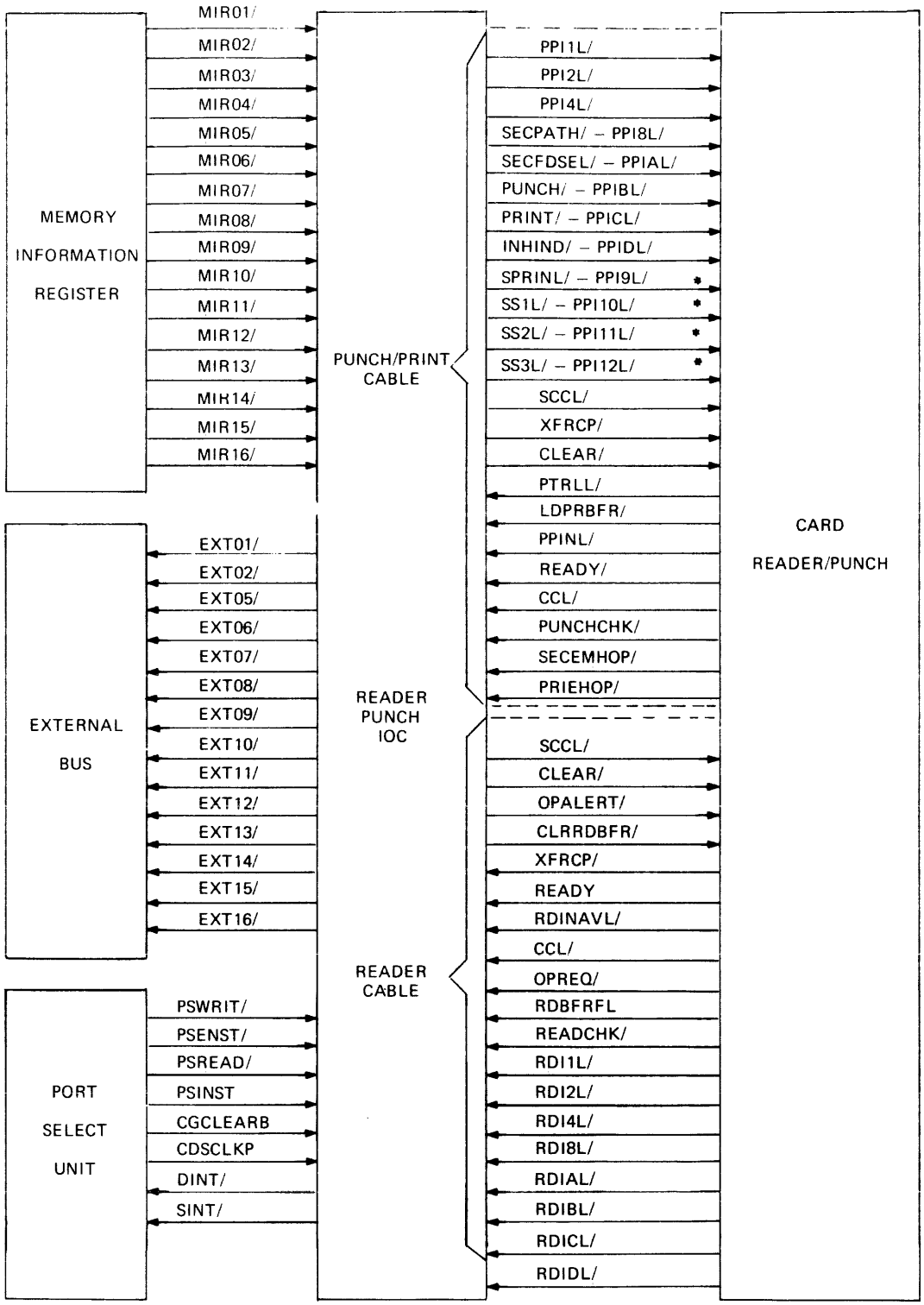
B700 PROCESSOR INTERFACE

As shown in Figure I-1, interface communications between the reader-punch IOC and the processor consists of input data lines MIR01/ through MIR16/, output data lines EXT01/, EXT02/, and EXT05/ through EXT16/, and various control signal lines. The reader-punch IOC/ processor interface control signals are as follows:

a. Write Line (PSWRIT). When false, PSWRIT/ initiates a one-character data transfer from the processor to the reader-punch IOC.
b. Read Line (PSREAD). When false, PSREAD/ initiates a one-character data transfer from the reader-punch IOC to the processor.
c. Enable Status Line (PSENST). When false, PSENST/ initiates transfer of the status word from the reader-punch IOC to the processor.
d. Instruction Line (PSINST). When false, PSINST/ indicates that the data on the MIR input data lines is a control word.
e. Clear Line (CGCLEARB). When true, CGCLEARB clears all control flip-flops in reader-punch IOC.
f. Data Interrupt (DINT). When false, DINT/ indicates to the processor that the reader-punch IOC is ready for another data-transfer operation.
g. Status Interrupt (SINT). When false, SINT/ indicates that the reader-punch IOC has a status word for the processor.
h. System Clock Pulse (CDSCLKP). When true, CDSCLKP indicates a 1-MHz clock pulse.

IOC/PROCESSOR OPERATIONS

The initiation of an information transfer between the processor and the IOC is controlled by the firmware and is the same for all devices. The distinction is made by the device address contained in the Base Register (BR1 or BR2) of the processor output select gates. The Port Select Unit decodes three-bit groups from the processor to completely define the operation that is to take place. The command field (nanobits 51 through 54) establishes whether the operation is to be a device read (DR) or a device write (DW). The four least-significant bits of BR1 or BR2 contain the specific device address. The most-significant bit of BR1



* – SIGNALS PPI9L/ THROUGH PPI12L/ APPLY TO 80-COLUMN CARD PUNCH

Fig. I-1 INTERFACE BLOCK DIAGRAM

	MSB 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	LSB 16
CONTROL WORD	OPER ALERT	DISABLE STATUS	CLEAR	TERM	STKR SEL 4	STKR SEL 2	STKR SEL 1	SEP PRINT	INH INPUT FEED	PRINT	PUNCH	SECOND FEED SELECT	SELECT SECOND PATH	LOAD OUTPUT BUFFER	UNLOAD INPUT BUFFER	START CARD CYCLE
96 COL., 6 BITS	--	--	--	--	--	--	--	--	--	--	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
96 COL., 8 BITS	--	--	--	--	--	--	--	--	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
80 COL., 12 BITS	--	--	--	--	DATA 11	DATA 10	DATA 9	DATA 8	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
STATUS WORD	DATA REQ	OPER REQ	--	DEV ADDR 4	DEV ADDR 3	DEV ADDR 2	DEV ADDR 1	DEV ADDR 0	--	PRINT LINE LGTH.	--	SELECT HOPPER EMPTY	PUNCH CHECK	READ CHECK	CARD CYCLE COMPL	NOT READY

NOTE: DEVICE ADDRESS BITS OF STATUS WORD ARE INSERTED AT PSU.

FIGURE I-2. IOC INTERFACE WORD FORMATS

or BR2, in conjunction with the command type, determines whether the data transfer is a control word, data word, or status word.

The control and data words are sent over the same interface lines (MIR01 through MIR16). The instruction signal (PSINST) determines whether the word present on the MIR lines is a control word or data word. The presence of the instruction signal in conjunction with the write signal (PSWRIT) indicates the presence of a control word. The absence of the instruction signal in conjunction with signal PSWRIT indicates the presence of a data word. Likewise, the instruction signal determines whether a data word or status word is sent to the processor by the IOC. The presence of the instruction signal in conjunction with the read signal (PSREAD) enables a readout of the status word over the EXT data lines, whereas the receipt of signal PSREAD without the instruction signal enables the transfer of a data word to the processor over the EXT data lines.

When the IOC requires data from the processor, or when the IOC has data for the processor, it generates a data-interrupt (DINT) to indicate to the processor that I/O service is required. When some unexpected action occurs within the peripheral (for example: feed hopper empty or peripheral is not ready) the IOC generates a status-interrupt (SINT) to alert the processor. These two interrupts are under the control of the processor and may be enabled or disabled, as required.

The data exchanged between the processor and IOC is present on the EXT and MIR lines for one clock cycle. Because the card peripheral requires the data at different times in its operation, the IOC contains various buffers to hold the data until it is required by the peripheral.

The formats of the control, data, and status words for the reader-punch IOC are shown in Figure I-2.

Control Word

A control word is a 16-bit word which is sent to the reader-punch IOC by the processor to initiate a card operation. The control word contains various control bits which define the operation to be performed. The following is a description of the control bits:

Bit	Function
1	Operator Alert. Unlocks the keyboard to allow keying into the input buffer and activates the READY indicator to alert the operator that the processor is ready to accept a keyboard input.
2	Disable Status. Disables status interrupts to the processor.
3	Clear. Activates the clear logic in the IOC.
4	Terminate. Terminates the buffer unload sequence.
5-7	Stacker Select. Used to specify the output stacker for the card sitting in the wait station as follows:

Stacker	STKR SEL4	STK SEL2	STK SEL1
Error stacker	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
Overflow	1	1	1

8	Separate Print. Indicates separate loading of the print buffer and the output buffer when both the print and punch control bits are present.
9	Inhibit Input Feed. Inhibits the input feed portion of the feed cycle. Permits the last card

of the job to be fed through the punch and print station.

10 Print. Enables printing of a card as it is advanced through the punch station.

11 Punch. Enables punching of a card as it is advanced through the punch station.

12 Secondary Feed Select. Enables feeding of cards from the secondary input hopper.

13 Select Secondary Path. When set in conjunction with the secondary feed select bit, causes the card fed from the secondary hopper to be stopped at the secondary wait stacker; otherwise, the card will go directly to the primary wait station without stopping at the secondary wait station.

14 Load Output Buffer. Enables IOC to load output buffer.

15 Unload Input Buffer. Enables IOC to unload input buffer.

16 Start Cycle Card. Initiates advancement of a card from the wait station through the primary or secondary path to the selected stacker.

Data Word

As shown in Figure I-2, the data words vary in length, depending on the particular model of card reader-punch being used. The data words are transferred on parallel lines; bit 16 is the least-significant bit.

Status Word

The status word is sent to the processor by the reader-punch IOC to notify the processor that a failure or specific functional condition has occurred. The status word consists of a device status field (bits 10 through 16), an operator request bit (bit 2), and a data request bit (bit 1). Before the status word is sent to the processor, the Port Select Unit (PSU) inserts a device address field (bits 4 through 8). The following is a description of the status bits:

Bit	Function
1	Data Request. Indicates that the IOC is ready to receive or transmit the next character. This status condition follows the data interrupt signal to the processor.
2	Operator Request. Indicates that the operator has pressed a program select key and is ready to enter input data.
3	Not used.
4-8	Device Address. IOC address inserted by the PSU.
9	Not used.
10	Print Line Length. Card reader punch has 128-character printer capability.
11	Not used.
12	Selected Hopper Empty. Indicates no card is present in the selected hopper.
13	Punch Check. Punch error detected.
14	Read Check. Read error detected.
15	Card Cycle Complete. Card reader-punch has processed card and is ready to start another card cycle.
16	Not Ready. Card reader-punch is not in the ready state and is incapable of accepting and executing commands.

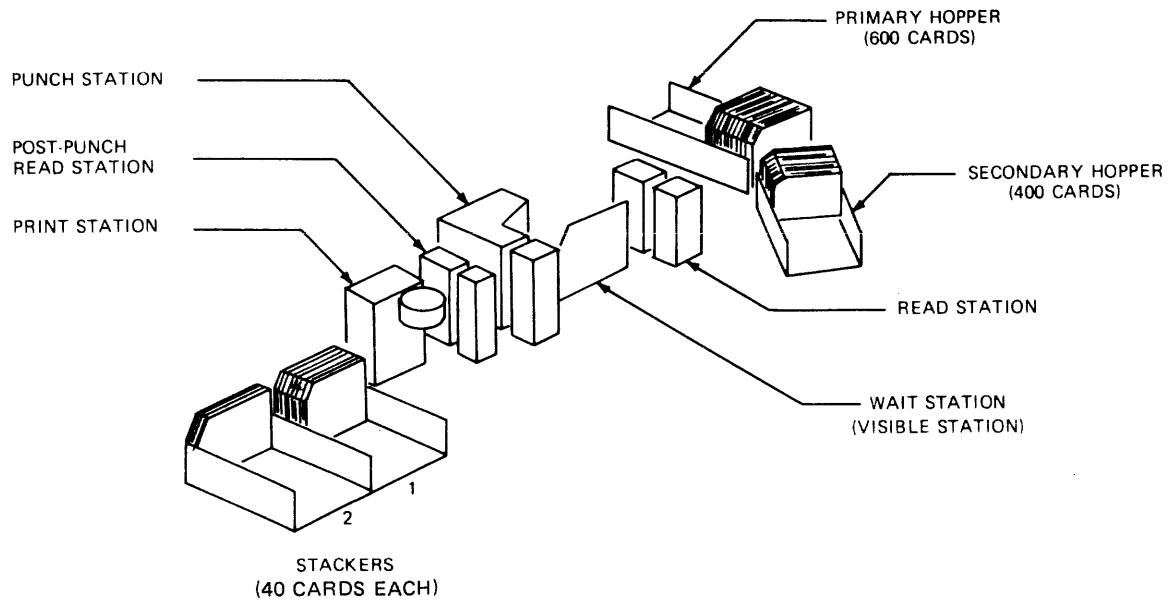


Fig. I-3 A9419-2 MECHANICAL LAYOUT

Char.	Card Code (B A 8 4 2 1)	Char.	Card Code (B A 8 4 2 1)
Space	00 0000	-	10 0000
1	00 0001	J	10 0001
2	00 0010	K	10 0010
3	00 0011	L	10 0011
4	00 0100	M	10 0100
5	00 0101	N	10 0101
6	00 0110	O	10 0110
7	00 0111	P	10 0111
8	00 1000	Q	10 1000
9	00 1001	R	10 1001
:	00 1010	!	10 1010
#	00 1011	$	10 1011
@	00 1100	*	10 1100
'	00 1101	)	10 1101
=	00 1110	;	10 1110
"	00 1111	¬	10 1111
0	01 0000	}	11 0000
/	01 0001	A	11 0001
S	01 0010	B	11 0010
T	01 0011	C	11 0011
U	01 0100	D	11 0100
V	01 0101	E	11 0101
W	01 0110	F	11 0110
X	01 0111	G	11 0111
Y	01 1000	H	11 1000
Z	01 1001	I	11 1001
&	01 1010	¢	11 1010
,	01 1011	.	11 1011
%	01 1100	<	11 1100
_	01 1101	(	11 1101
>	01 1110	+	11 1110
?	01 1111	|	11 1111

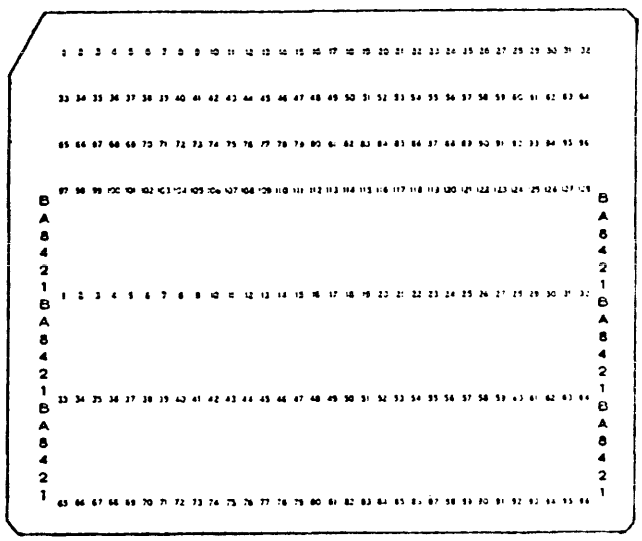


Fig. I-4 96 COLUMN CARD CODES

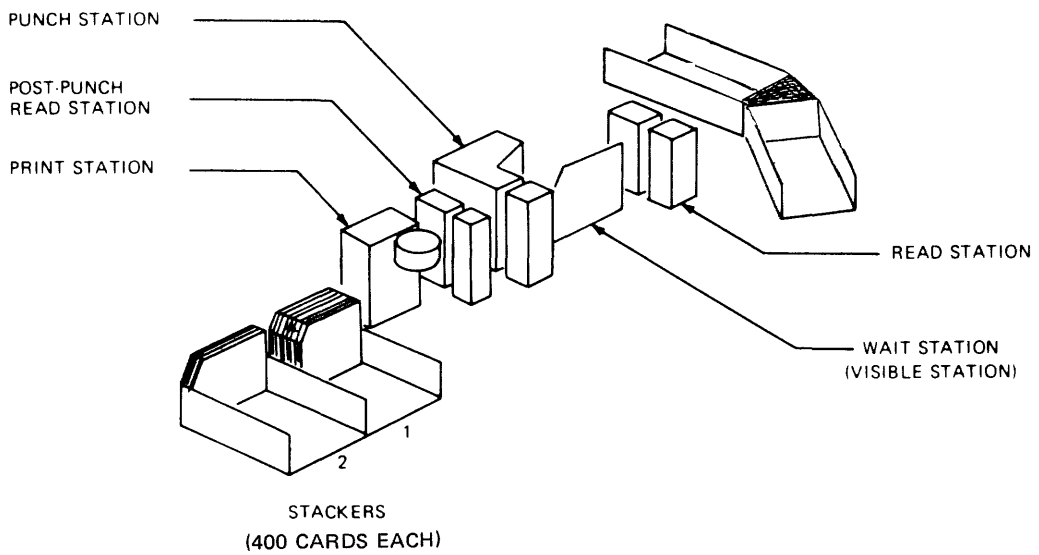


Fig. I-5 A9418-2 MECHANICAL LAYOUT

A9419 GENERAL DESCRIPTION

As stated previously, the B0311 IOC services the A9419 (96-olumn) card peripheral unit. In the on-line mode, the A9419 performs either independently, or in combination, any of the following functions:

a. Read.
b. Punch.
c. Print (same data as punched).
d. Separate print.

In addition to controlling the above functions, the processor can select the required hoppers and stackers for the card in process and may also permit data entry through the peripheral keyboard by the system operator. Figure I-3 shows the layout of the physical components of the A9419. Figure I-4 illustrates the 96-column card format. The physical components are as follows:

a. Primary Hopper. The primary hopper has a capacity of 600 cards. The cards are placed in the hopper face forward, with column 1 to the left and the printing area across the top. The front card feeds into the machine first. The card follower holds the cards firmly against the feed rollers.
b. Secondary Hopper. The secondary hopper has a capacity of 400 cards. The cards are also placed in the hopper face forward, with column 1 to the left and the printing area along the top of the first card visible. This visible card is the last card to feed into the machine.
c. Read Station. The read station reads the data prepunched on input cards when in certain operating modes.
d. Visible Station. Prior to entry into the punch station, the card is stopped in the visible station, where the print and punch areas of the card can be seen. This is helpful when in the verify mode of operation because the card does not have to be removed to be read by the operator.
e. Punch Station. Data is punched in the card three tiers at a time. The card is then moved to the next column pair that is to be punched.
f. Post-Punch Read Station. This read station functions to detect punching errors that occur during an on-line operation. The data transferred to the punch memory is compared with the data read from the punched card. A non-comparison condition lights the PUNCH CHECK indicator.
g. Print Station. The print station consists of a four-column drum printer. A replaceable ink cartridge rides in contact with the drum to maintain a constant supply of ink on the drum characters.
h. Stackers. Two stackers with a capacity of 400 cards each receive cards in the order they are fed. Stacker selection is determined by the various operating modes described later.

A9418 GENERAL DESCRIPTION

The A9418 (80-column) card peripheral unit is controlled by the B0418 IOC. In the on-line mode, the A9418 may be used to perform card punch and/or read operations. The processor can select the required hoppers and stackers for the card in process. Figure I-5 shows the layout of the physical components of the A9418-2. The function of these components is the same as described for the A9419-2. Figure I-6 illustrates the 80-column card format.

NUMERIC Graphic	Card Code	ALPHABETIC Graphic	Card Code	SPECIAL Graphic	Card Code
0	0	A	12-1	:	8-2
1	1	B	12-2	#	8-3
2	2	C	12-3	@	8-4
3	3	D	12-4	'	8-5
4	4	E	12-5	=	8-6
5	5	F	12-6	"	8-7
6	6	G	12-7	&	12
7	7	H	12-8	¢	12-8-2
8	8	I	12-9	.	12-8-3
9	9	J	11-1	<	12-8-4
		K	11-2	(	12-8-5
		L	11-3	+	12-8-6
		M	11-4	|	12-8-7
		N	11-5	-	11
		O	11-6	!	11-8-2
		P	11-7	$	11-8-3
		Q	11-8	*	11-8-4
		R	11-9	)	11-8-5
		S	0-2	;	11-8-6
		T	0-3	¬	11-8-7
		U	0-4	/	0-1
		V	0-5	Blank	0-8-2
		W	0-6	,	0-8-3
		X	0-7	%	0-8-4
		Y	0-8	_	0-8-5
		Z	0-9	>	0-8-6
				?	0-8-7
				Blank	NONE

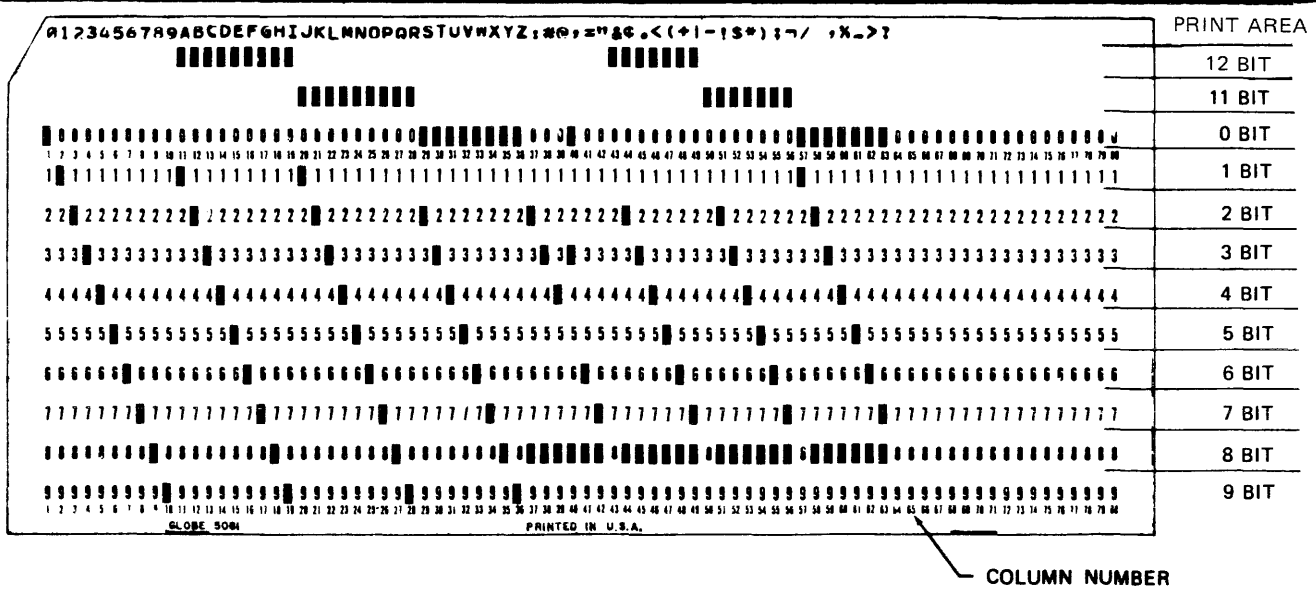


Fig. I-6 80-COLUMN CARD BIT CODES

GLOSSARY OF TERMS AND SYMBOLS

NOTE

In the schematics and backplane circuit list, many of the following signals are prefixed with RC. This indicates that they originate within the B0311 or B0418 logic.

Signal or Term	Description
ASR	Address and Status Request. Nanoinstruction which causes the PSU to enable the status bits of the highest priority IOC generating an IRQ to the ERT lines, together with the address of that IOC, from the PSU.
ACPONCL	Power-on Clear. Signal from the AC control section of processor. Used to initially reset all logic at power-on time.
BRn	Base Register n (n = 1 or 2). One of two registers in processor (MCU) which controls the address lines to select an IOC.
Bit14	Decoded from MIR14 line.
Bit15	Decoded from MIR15 line.
CCC/	Card Cycle Complete Not. Indicates that a peripheral operation is in progress. Goes low when processor sends a control word to IOC, and remains low until end of peripheral operation.
CCL/	Card Cycle Level Not. Interface signal from peripheral. Low while peripheral operation is in progress.
CLEAR/	Interface signal to peripheral (30 microseconds). Used to reset peripheral logic.
CLR/	Clear Not. Used to reset most of the B0311 logic; developed from Processor CLEAR line.
CLRRDBFR/	Clear Read Buffer Not. Interface signal to peripheral. When low, indicates that processor does not desire to read any more data from peripheral input memory.
CSF	Cycle Start Flip-flop. Used to control CCC/.
DATRD/	Data Read/. Developed from READ*INST/.
DINT	Data Interrupt.
DISTAT	Disable Status.
ENABLE	Output of Interrupt enable flip-flop.
ENST	Enable Status. (Refer to PSENSTn.)
EXTn	Processor External (input) data bus line.
INHCLK/	Inhibit Clock Not. Single, low-going clock pulse used to initiate SCCL when processor sends a control word to IOC.
INHINFD/	Inhibit Input Feed Not. Interface signal to peripheral. When low, prevents peripheral from feeding a card from its input hoppers.
INST	Instruction bit. (Refer to PSINST.)
INST*WRITE	Indicates that processor is sending a control word to IOC.
IOC	I/O Control.
IWNB4	Instruction Write Not Bit 4. Indicates that processor is sending a control word that does not specify terminate operation.
LDPRBFR/	Load Print Buffer Not. Interface signal from peripheral. When low, indicates that the processor may send separate print data.
LOB	Load Output Buffer. Developed from MIR14; indicates that processor wishes to transmit either punch or print data (or both) to peripheral.
MIR	Memory Input Register. Data output bus from processor (to memory or peripheral devices).
OPALERT/	Operator Alert Not. Interface signal to peripheral to enable entry of data at peripheral keyboard.
OPALF	Operator Alert Flip-flop.
OPREQ/	Operator Request Not. Interface signal from peripheral. When low, indicates that operator wishes to input data.
PONCL	Power on Clear. (Refer to ACPONCL.)
PPInL/	Punch or Print Information n Level. (where n = 1 through D Hex, or 1 through 12 Dec.) Interface data lines to peripheral.
PPINL/	Punch or Print Information Needed Level. Interface signal from peripheral. When low, indicates that peripheral is ready to load a character for punching or printing.

GLOSSARY OF TERMS AND SYMBOLS (CONTINUED)

Signal or Term	Description
PRIEHOP/	Primary Empty Hopper Not. Interface signal from peripheral; low when primary hopper is empty.
PRINT/	Interface signal to peripheral. When low, indicates that processor wishes to print data during the subsequent card cycle.
PSENT	Port Select Enable Status. Control line from PSU to IOC. Used to put status data on the EXT lines when processor executes an ASR.
PSINSTn/	Instruction bit from PSU, true when MSB of selected Br equals 1. When true during a device write, indicates that data on the MIR lines is a control word. When true during a device-read, calls for status, rather than data from the IOC.
PSREADn/	Port Select Read n (n = IOC address). Read line from PSU to IOC.
PSWRITEn/	Port Select Write n (n = IOC address). Write line from PSU to IOC.
PSU	Port Select Unit.
PTRLL/	Print Line Length Not. Interface signal from peripheral. When low, indicates device has 128 print positions, as opposed to 96.
PUNCH/	Interface signal to peripheral. When low, indicates that processor wishes to punch data during the subsequent card cycle.
RC1 through RC4	B0311 IOC printed circuit board types 1 through 4.
RDBFRFL/	Read Buffer Full Not. Interface signal from peripheral. When low, indicates presence of data in the input memory.
RDn/L	Read Data n Level. (Where n = 1 through D Hex, or 1 through 12 Dec.) Interface data from peripheral.
RDINAVL/	Read In Available Not. Interface signal from peripheral. When low, indicates that a character is present on the data lines. (RDnL)
READ	Refer to PSREADn.
READCHK/	Read Check Not. Interface signal from peripheral. When low, indicates that an error was detected during a card-read operation.
READY/	Interface signal from peripheral. When low, indicates that device is in the on-line mode.
RESET/	Low-going signal used to reset the motion control data in the B0311 after the peripheral has received it.
SCC1-2-3F	Timing control flip-flops for generation of SCCL.
SCCL/	Start card cycle level not. Interface signal to peripheral to strobe motion data to device and commence a card cycle.
SCCLF	Control flip-flop for SCCL.
SCLK	System clock.
SECEHOP/	Secondary Empty Hopper Not. Interface signal from peripheral; low when hopper is empty.
SECPATH/	Second Path Not. Interface signal to peripheral. When low, instructs peripheral to feed the next card over the secondary path (only devices with two feed paths).
SELHOP	Selected Hopper (empty). When true, indicates that hopper selected by the processor is empty.
SINT	Status Interrupt.
SINTF	Control flip-flop for SINT.
SPRINL/	Separate Print Level Not. Interface signals to peripheral. When low, indicates that processor requires data, other than that which is punched, to be printed on the card.
SS1-2-4L/	Stacker Select n Level Not. Interface signals to peripheral. Used to select one of six receiving stackers.
ST+INRD	Status or Instruction Read. Used to gate status data to EXT lines.
SECFDSEL/	Secondary Feed Select No. Interface signal to peripheral. When low, instructs device to feed the next card from the secondary hopper.
SU	Storage Unit. IC chip type.
UIB	Unload Input Buffer Developed from MIR15. Indicates that processor wishes to read data from the next card fed to the visible station.
WRITE	Refer to PSWRITEn/.
XFRC1-2F	Timing control flip-flops for generation of XFRCP/.
XFRCP/	Transfer Clock Pulse Not. Interface signal to peripheral. Used to strobe individual characters to the device.
XFRCPF	Control flip-flop for XFRCP/.

A/B9419 ON LINE INTERFACE

In order to understand the functions of the B311 IOC it is necessary to understand the basic operation of the A/B9419 on-line interface.

The interface logic within the A/B9419 contains a six-state Control Counter as represented in Fig. II-1, these states, for reference, are numbered 0 through 5.

State 0 represents the idle state of logic. While it is in state 0 the IOC may condition the control lines to the peripheral and then make the signal SCCL/ false. When the peripheral receives SCCL from the IOC, it accepts the data on the control lines, which correspond to Control word bits 1 and 5 through 12, into some buffer flip-flops, and advances to state 1. As it goes to state 1 the signal CCL/ is made false to indicate to the IOC that a Card cycle is in process.

Note that CCL/ remains false until the Control Counter returns to state 0. CCL is returned to the IOC approximately 12 microseconds after SCCL/ goes false.

In State 1 the peripheral is ready to receive data which is to be loaded into its input memory. It then makes the signal PPINL/ false to indicate that it is ready to receive one character.

Upon receipt of PPINL the IOC sends a data interrupt (DINT) to the processor which will respond by sending one character to the IOC. The IOC then buffers the data, conditions the data lines to the A/B9419, resets the DINT and sends XFRCP to the peripheral.

When the peripheral receives XFRCP it resets PPINL and loads the character into its input memory. After loading is completed the peripheral will again make PPINL/ false to indicate that it is ready to receive the next character.

The above procedure is then repeated, for a total of 96 operations, so as to load a complete card image into the input memory of the A/B9419. When 96 data transfers are completed the logic advances to state 2.

In State 2 the logic initiates the release of a Card, from the Visible Station, to the Punch registration stop and advances to State 3. At about this time the data in the input memory is transferred to the Punch memory.

In State 3, if Separate Print was called for in the original Control word (MIR08), the peripheral is ready to receive data to be loaded into its Print Buffer. It then makes the signal PPINL/ false to indicate to the IOC that it is ready to receive a character. However at this time it also makes LDPRBFR/ false to indicate that the data is required for printing.

When the IOC receives PPINL it then, as in the State 1 operation, sends DINT to the processor. The operation is then exactly the same as the State 1 operation where the input memory was loaded. Again 96 data transfers are required to fill the Print buffer. When the data transfer is completed the logic advances to state 4.

As the logic advances to state 4 the card, which was last left at the Punch registration stop, continues its movement through the Punch and Print Stations, where it is processed, and on to the stacker selected in the original control word (MIR 05, 06, 07). When this card is approximately halfway through the Punch station the A/B9419 initiates an Input feed cycle which feeds the next card in the input hopper (selected in the original control word, MIR 12) through the Read station and into the Visible station. Any data pre-punched in the Card is now in the input memory and available for the Processor. At the completion of the read operation the logic advances to state 5.

In State 5 the peripheral is ready, if required, to unload its input memory to the processor. It then places the first character onto the data lines and makes RDINAVL/ and RDBFRFL/ false to alert the IOC. If "Unload Input Buffer" was requested in the original Control word the IOC will send DINT to the Processor. The Processor will respond by executing a device read to call the data from the IOC.

The IOC will then reset the DINT put the character onto the EXT lines and send and XFRCP to the peripheral to call for the next character.

When the peripheral receives XFRCP it resets RDINAVL and shifts the next character to the data lines. When shifting is completed the peripheral again makes RDINAVL/ false and the above process is repeated. The data transfer operation will then consist of 96 operations as described above to unload a complete card image to the Processor.

If the Processor does not require a complete card image it may terminate this operation, after receiving the required number of characters, by sending a Control word to the IOC with MIR 04 set. The IOC will then make CLRRDBFR/ false which causes the peripheral to cease transmitting data. The A/B9419 interface control counter returns to state 0 and the signal CCL/ goes true to indicate that the Card cycle is completed.

OPREQ & OPALERT

Built into the logic of the A/B9419 and the B311 IOC is the ability to permit the system operator to key-in additional data at the peripheral keyboard while the peripheral is in the On-line mode.

If the operator depresses program key 1 the A/B9419 will make OPREQ/ false. The IOC will then generate a status interrupt (SINT) to alert the Processor.

When the Processor interpreter is ready it may send a Control word with MIR01 true. This causes the IOC to make OPALERT/ false to the peripheral.

When the peripheral receives OPALERT the Control counter states advance through to State 4. (See Fig. II-1.) At this time the peripheral KB is enabled and the Ready indicator lamp, on the peripheral, flashes to indicate to the operator, that the KB is available.

After 96 characters have been indexed, or when the operator depresses the Release key, the Control counter advances to state 6 where the data may be unloaded to the Processor, as in a normal read operation.

NOTE: This function is not presently used by the B705/711 system software.

MOTION BITS/DATA BUFFER

MIR05 through 16 (ref. Fig. I-2) can either contain information related to a card process (motion bits) or data to be sent to the peripheral for either Punching or Printing.

Whenever the Processor executes a device write to the IOC MIR05 through MIR16 are loaded into a buffer consisting of three S.U. IC chips located on RC2 and RC3.

As soon as the data is loaded into the buffer it is made available to the peripheral. Fig. II-2 shows the buffers. When the WRITE signal goes true, from the PSU, it permits one clock pulse to strobe the MIR data into the buffers. In the case of a Control word the data remains in the buffers until the CCL signal is received from the peripheral to indicate that it has received the motion bits, at this time the signal RESET/ will go false to clear the SU chips through the master reset. In the case of Data characters the data remains in the buffer until the Processor executes a device write to send the next character to the IOC.

NOTE: The signal RESET/ will also go false to clear the buffer whenever the Processor is cleared. XFRCP is the signal which alerts the peripheral to accept data on the interface lines (see Fig. II-8).

SCCL GENERATION

The interface logic in the A/B9419 requires that the motion control data be stable on the interface for 1 micro-second prior to SCCL/ going false. This is to ensure that the

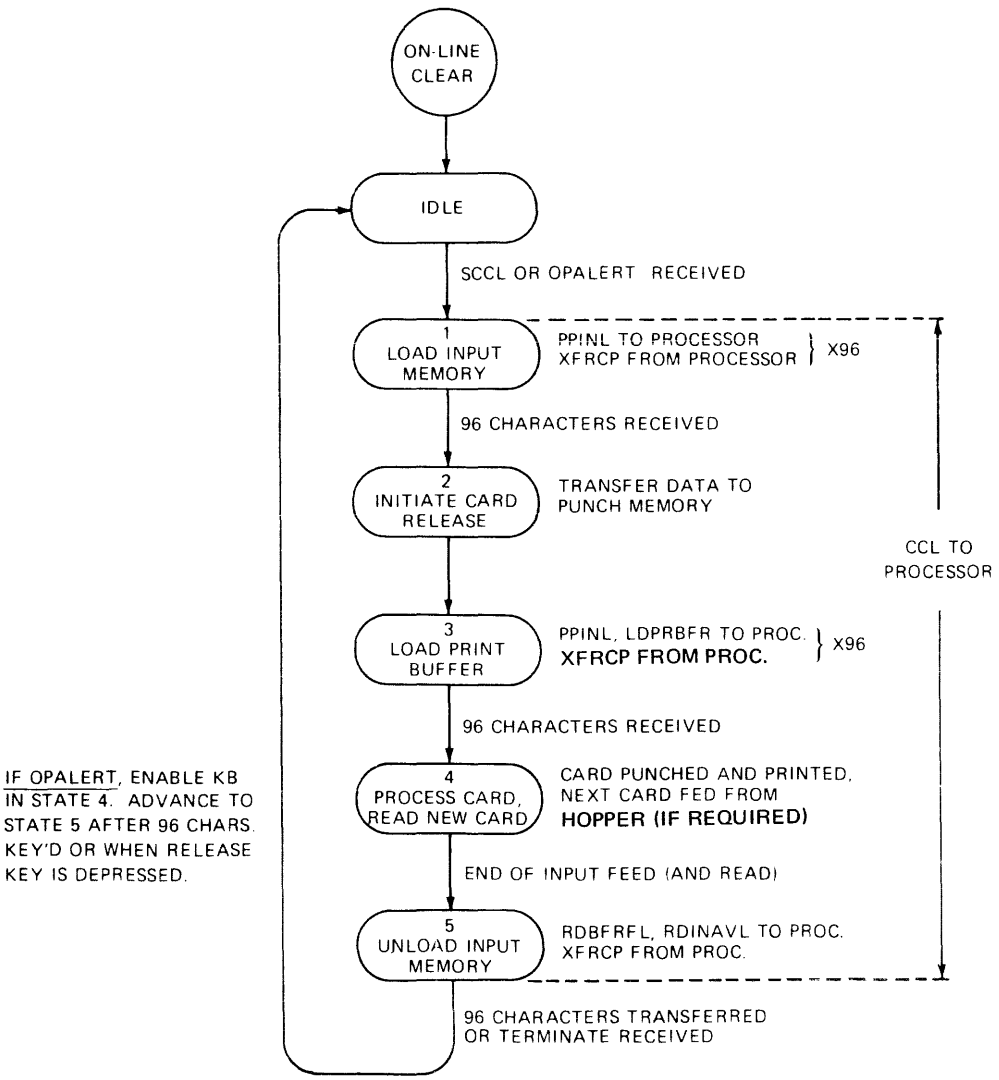


Fig. II-1 A9419 ON-LINE CONTROL COUNTER STATES

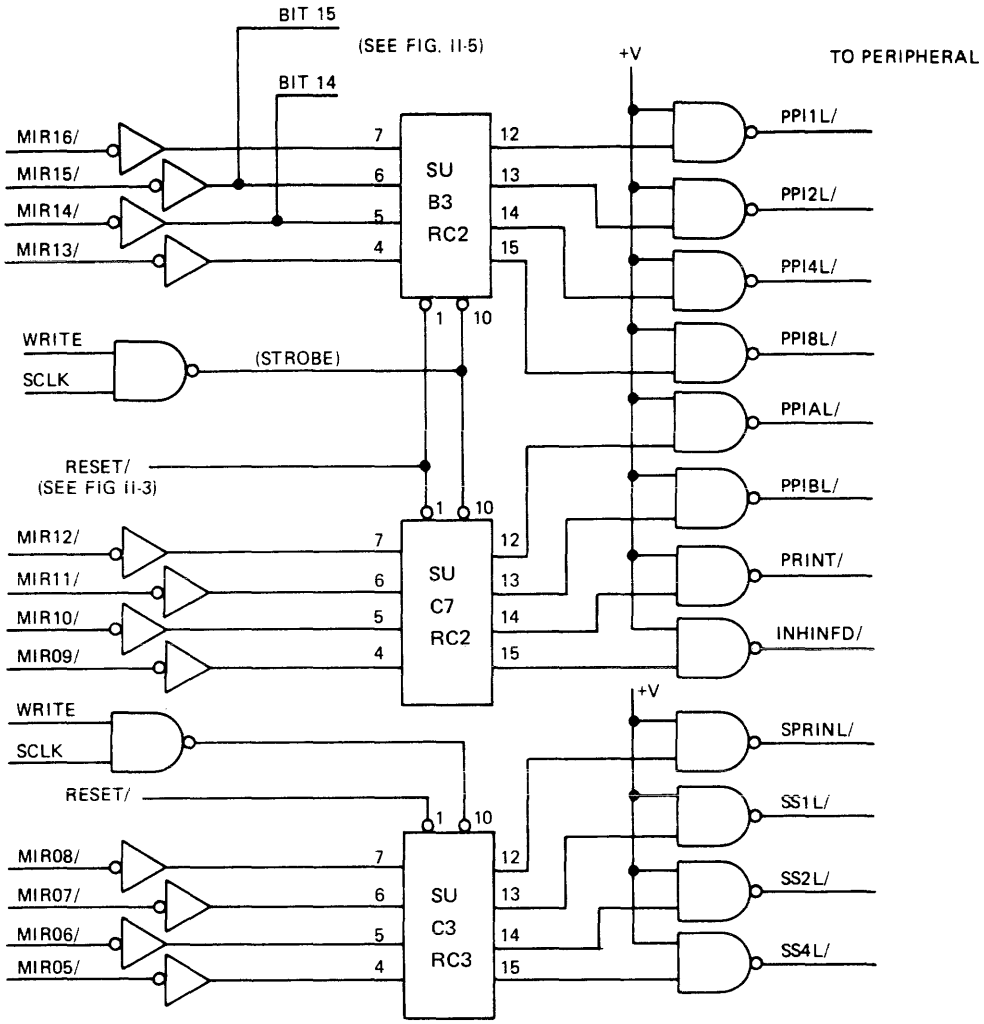


Fig. II-2 MOTION BITS/DATA BUFFER

data is accurately read into the peripheral.

When the Processor executes a device write, to the B311, with MIR16 true and MIR04 false, a single low going INHCLK/ is enabled (see Fig. II-3) which sets the first flip-flop (SCC1F) in the SCCL delay circuit. Three clock periods later the signal SCCL goes true to make SCCL/ false to the peripheral. Within approximately 13 microseconds (10-16) the peripheral will make CCL/ false to indicate that it has received the data. RCCCL/ going false directly resets the SCC1F in the SCCL delay circuit. Thus three clock periods later SCCL goes false.

SCCL is gated with SCC3F so that the clock pulse which resets SCCL also makes RESET/ false to clear the data-buffer. Thus, at 1 MHz clock rate, the motion control data is present on the interface lines for 3 usec before SCCL.

The signal PONCL/ is false when the Processor is first powered up. It is used to inhibit SCCL until the Processor power supply and logic is stabilized, this is to prevent any spurious peripheral operation being initiated.

The signal CCC/ (card cycle complete not) is generated to make the status word bit 1 true, (ref. Fig. I-2) until the peripheral has completed any operation.

Referring to Fig. II-4 it is seen that the INHCLK/ signal, which generates SCCL/, is also used to reset CSF (cycle start flip-flop). CSF is set by CCL * SCCL * SCLK, or by OPALF * CCL * SCLK once the peripheral has started the required operation.

CSF is then gated with CCL/ to produce the signal CCC/, which will be true from the time that the Processor sends a control word to the IOC, until the device completes that required operation.

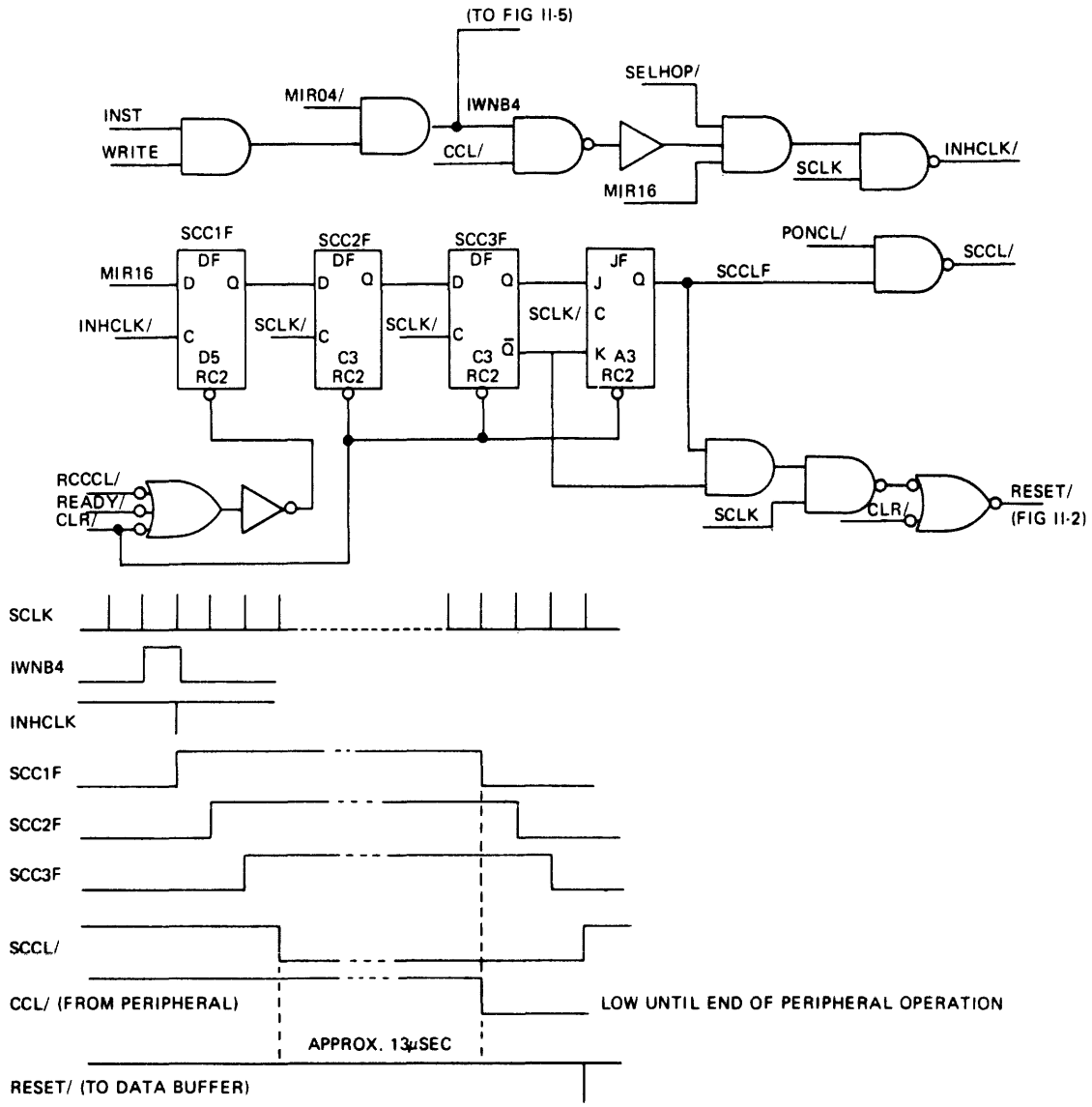


Fig. II-3 INHCLK, SCCL GENERATION AND TIMING

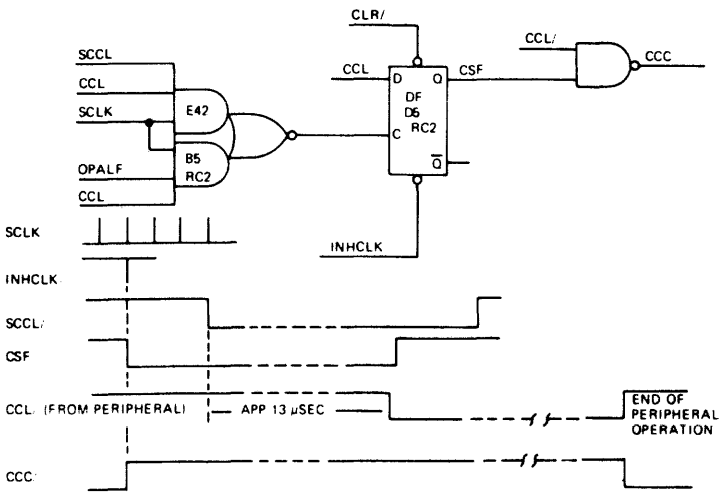


Fig. II-4 CSF, CCC/ AND TIMING

CONTROL BUFFER

MIR Bits 1 through 4 contain only control data for the IOC, never data. These bits, together with MIR14 and MIR15 are stored in a separate Control Buffer whenever they are present in a Control word. They are stored in the buffer for use later in the peripheral operation.

Fig. II-5 shows the Control Buffer which consists of an SU chip and two D-type flip-flops. When the Processor executes a Device write to the IOC with the Instruction bit set, (MSB of Base Register) and MIR04 = 0, the signal IWNB4 is developed (see Fig. 11-3). This is gated with SCLK to strobe bit 14, Bit 15, MIR03, and MIR02 in the SU chip, Fig. II-5 and conditions one D type flip-flop according to the state of MIR01. The other flip-flop, for MIR04 is set or reset by INST*WRITE gated with SCLK. Thus it can be seen that when MIR04 is true in a Control word it will cause BIT4F to be set but will inhibit the loading of the SU and OPALERT flip-flop by making IWNB4 false.

Of these signals only one, OPALERT, is sent directly to the peripheral. The output of MIR03, CLEAR, triggers a 30 microsecond single shot which makes CLEAR/ false to the peripheral, and the remaining signals are used within the DDP.

Note that under normal operations MIR bits 1, 2, 3, 4, and 16 would not be present together in one control word since each is a separate control function.

ENABLE FLIP-FLOP

The purpose of the Enable flip-flop is to prevent the IOC generating either Data or Status interrupts (DINT, SINT)

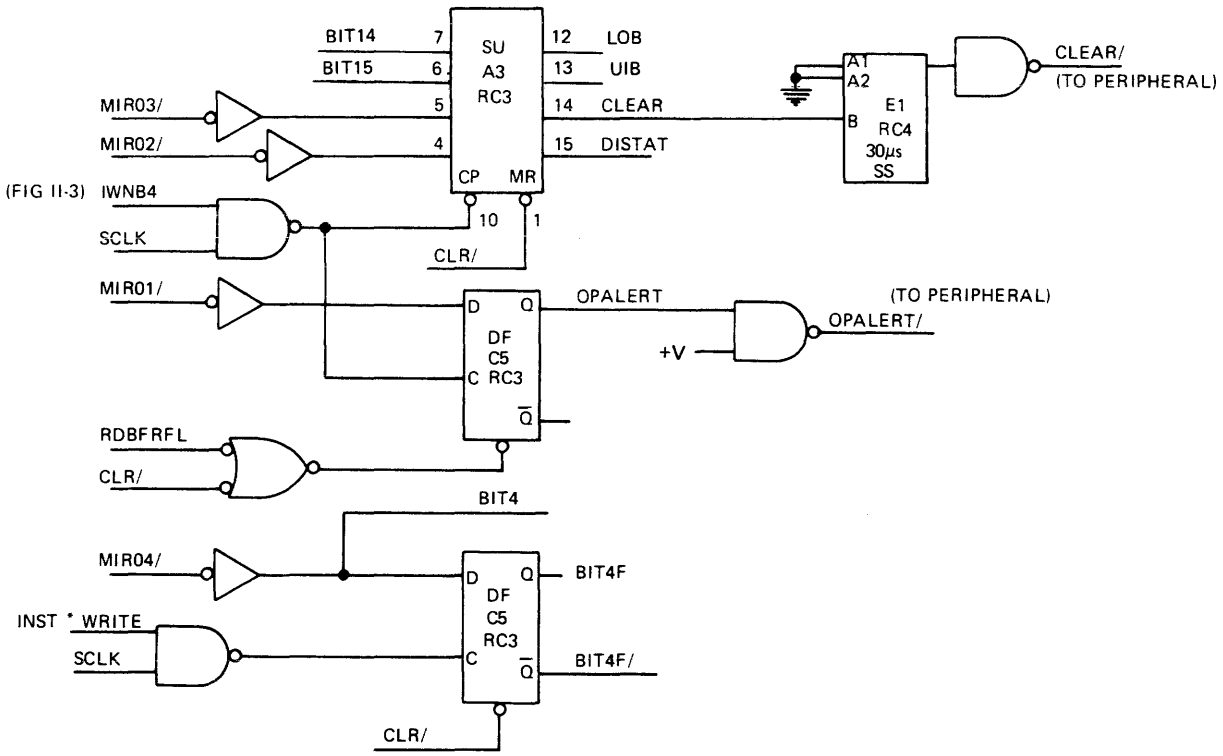


Fig. II-5 CONTROL BUFFER

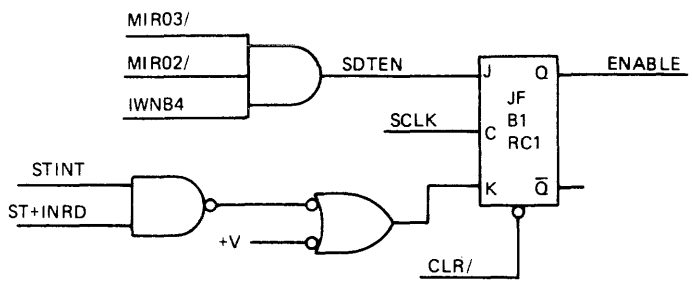


Fig. II-6 INTERRUPT ENABLE FF

when it is not in use. For example turning the peripheral on or off while the Processor is working with other devices should not cause any interrupts to the Interpreter.

Referring to Fig. II-6 it is seen that when the Processor executes a device-write to the peripheral with the instruction bit set, and MIR2, 3, and 4 false (ref. Fig. I-2) the Enable flip-flop is set. This will permit the generation of DINT and SINT (reference Figs. II-7 and II-10).

In normal operation the first SINT generated will be when CCC/ goes false at the completion of the peripheral operation. When the Processor executes an ASR (or device-read with the instruction bit set) to interrogate the SINT, the signals STINT * ST+INRD will reset the Enable flip-flop thus preventing further DINT's or SINT's until another operation is required.

DATA INTERRUPT (DINT)

Referring to Fig. II-1, it can be seen that there are three states, of the peripheral card cycle operation, during which data is transferred between the Peripheral and the Processor. These occur when the Peripheral is ready to load its Input buffer (state 1), when the Peripheral is ready to load its Print buffer (state 3), and when the Peripheral is ready to unload its Input memory, following a card read operation (state 5).

In state 1, the signal received from the Peripheral is PPINL. Referring to Fig. II-7, it can be seen that PPINL is gated with LOB to set a D flip-flop, provided that Enable flip-flop is set. (LOB will be true if MIR14 = 1 in the Control word which initiates the card cycle.) The set output of the D flip-flop allows the next SCLK to set the DINT flip-flop thus making DINT/ false to the Processor. The reset output of the DINT flip-flop then resets the D flip-flop.

The DINT flip-flop is reset, when the Processor executes a device write to transmit a data character to the IOC, by the signals INST/ and WRITE.

In state 3 the Peripheral sends PPINL and LDPRBFR when it is ready to receive a print character. These two signals are gated to set the DINT flip-flop and, as above, DINT flip-flop will reset when the Processor responds by executing a device write.

Note that LDPRBFR is true throughout the load Print buffer operation, while PPINL is the signal which goes true for each of the 96 characters.

In state 5, the Peripheral sends RDBFRFL for the duration of state 5, and RDINAVL as each character is made available to the IOC. In Fig. II-7 it may be seen that RDINAVL and RDBFRFL are gated with UIB (from MIR15 in the initiating control word) to set the D type flip-flop and generate DINT.

The DINT will be reset when the Processor executes a Device read, to take the character from the IOC, by the signals READ and INST/.

XFRCP CONTROL

When the IOC outputs data, the signal XFRCP (Transfer clock pulse) is sent to the peripheral to generate a data transfer within the peripheral interface. This will load the output character into the Input Memory of the peripheral. The "load cycle" takes approximately 12 us.

Referring to Fig. II-8, it is seen that when the Processor sends a character to the IOC and resets DINT, (Ref. Figs. II-2, II-7) DINTF/ going true sets XFRC1F. Two clock times later XFRCPF is set and XFRCP/ goes false to the peripheral to initiate a load to the Input Memory.

When XFRCPF sets it initiates the reset of XFRC1F and XFRC2F, however XFRCPF remains set until PPINL/ or RDINAVL/ goes true indicating that the data has been accepted by the peripheral. PPINL is used during interface states 2 and 3 (ref. Fig. II-1) and RDINAVL is used during interface state 5.

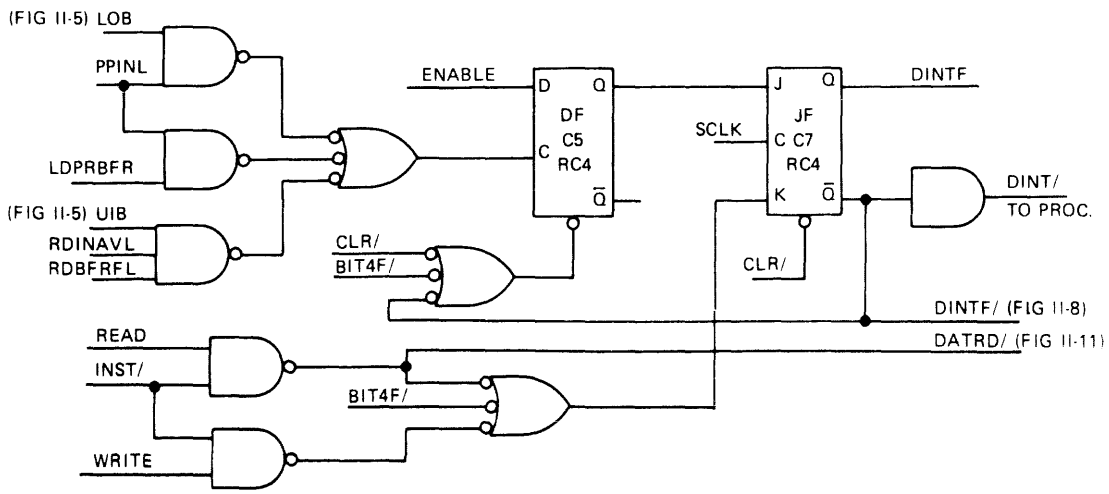


Fig. II-7 DATA INTERRUPT CONTROL

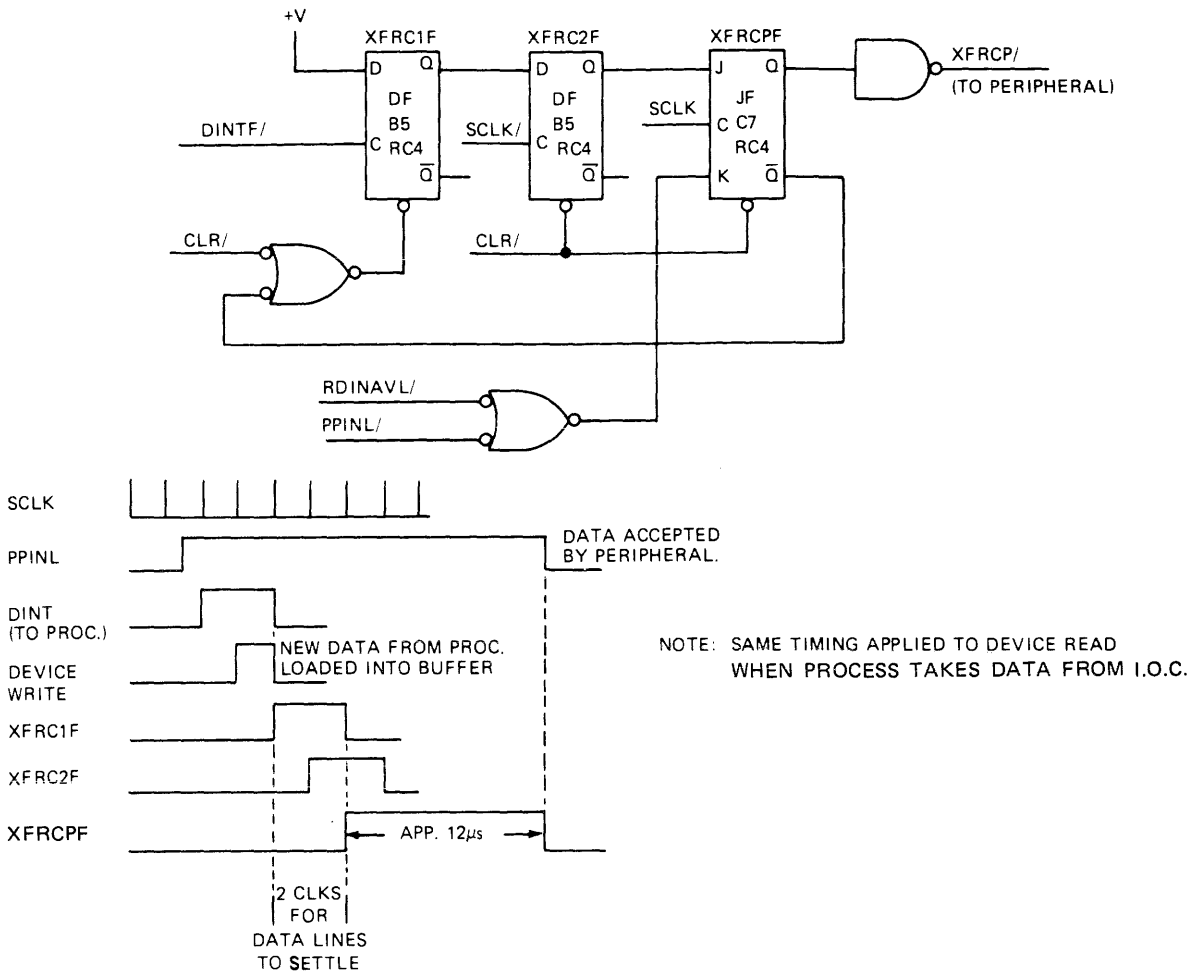


Fig. II-8 XFRCP CONTROL AND TIMING

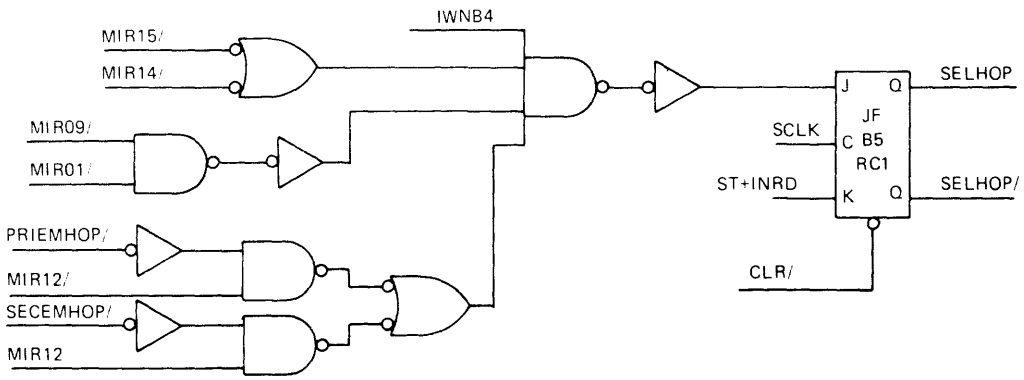


Fig. II-9 SELECTED HOPPER EMPTY FF

SELECTED HOPPER EMPTY FLIP-FLOP

Whenever the card hopper, selected in the control word, is empty the SELHOPF is set and a status interrupt is sent to the processor.

The peripheral has two interface signals which can indicate an empty hopper, these are PRIEMHOP/, primary hopper empty not, and SECEMHOP/, secondary hopper empty not.

In a control word (ref. Fig. I-2) MIR12 is used to select the secondary hopper, if MIR12 is false then the primary hopper is selected.

Referring to Fig. II-9 it is seen that the signals IWNB4 *

(MIR15 + MIR14) * MIR09/ * MIR01/ are used to enable the set input of SELHOPF. This gating is active when a control word is sent to the IOC which requires a card to be fed from either the primary or secondary hopper.

To complete the gating PRIEMHOP is gated with MIR12/, and SECEMHOP is gated with MIR12. Thus, if the selected hopper is empty, SELHOPF is set.

SELHOPF will generate a SINT to the processor (see Fig. II-10) and when the processor interrogates the SINT, by executing an ASR or a Device read with the instruction bit set, the signal ST + INRD will reset SELHOPF.

STATUS INTERRUPT CONTROL

A status interrupt (SINT) is sent to the processor whenever certain conditions occur within the peripheral and alerts the processor that some action may be required. It is then a function of the interpreter (firmware) to interrogate the status condition, determine what it is, and take the necessary action.

A SINT is generated by the following conditions:

1. Operator request (from Prog. 1 key on the peripheral).
2. Empty selected card hopper.
3. End of peripheral card cycle (when the peripheral interface states go from 5 to 0 and CCC/ goes false).
4. Peripheral going to the not-ready condition between card cycles (from Punch data check, Read check – optional, both hoppers empty, Full stacker or Card-jam).

Referring to Figure II-10 it is seen that when the operator depresses Prog. 1 key on the peripheral keyboard the signal RCOPREQ/ going false will set a D flip-flop (A). This in turn will set the SINT FF at the next SCLK.

If a selected hopper is empty the signal SELHOP/ (ref. Fig. II-9) going low sets SINTF.

At the end of a peripheral operation the signal CCC/ going low will set a D flip-flop (B) which will set SINTF.

The signal READY/ from the peripheral, if it goes true, can also set the D flip-flop (B) but only while CCC/ is false (i.e., between peripheral operations).

Note that when SINTF sets its reset output going low will directly reset the D flip-flops.

Under certain conditions the processor firmware may choose to ignore a SINT from the IOC. If a control word is sent to the IOC with MIR02 true the signal DISTAT (ref. Fig. II-5) will reset both the D flip-flops (A & B) and SINTF. The only exception being if SINTF has been set from OPREQ/. In this case the processor must execute an ASR or Instruction-read to take the status condition and clear the SINT.

When the processor executes an ASR, or Device-read with the instruction bit set, the signals ENST/, or INST * READ, will rest SINTF through its K input.

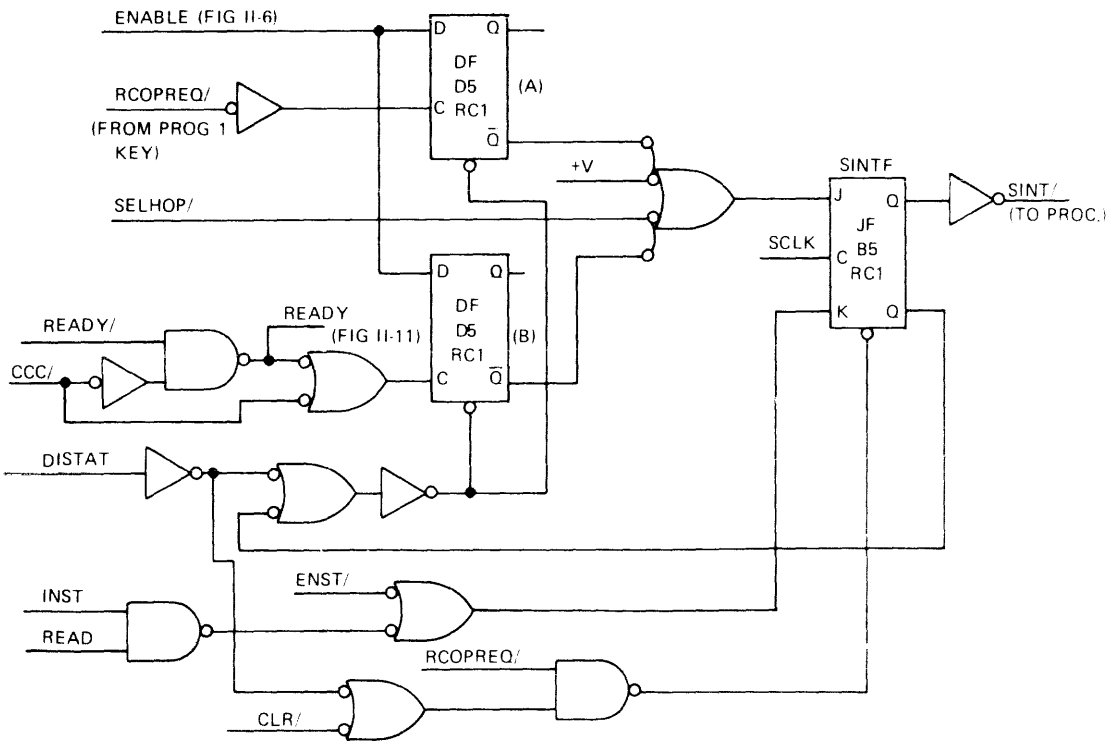


Fig. II-10 STATUS INTERRUPT CONTROL

DATA OR STATUS TO EXT LINES

When the processor executes a device-read to the IOC it is the instruction bit (MSB of BRn) which indicates whether data from the peripheral or status information from the IOC is required. The selection of data or status is accomplished through the use of two quad-one-of-two data selector IC's on the RC2 board.

Referring to Fig. II-11 it can be seen that when the processor executes an ASR or an Instruction-read to the IOC the signals ENST or INST * READ will generate the signal ST+INRD. This signal controls the data-selectors (S2) so that the inputs I1A, B, C, & D are gated to the A B C & D outputs. At the same time ENEXT enables the output of the selectors to the EXT lines. Thus the processor receives the status information.

When the processor executes a device-read with the instruction bit reset the signal ST+INRD is false so the inputs IOA, B, C, & D are gated to the A B C & D outputs of the selectors. In this case the signal DATRD/ (ref. Fig. II-7) generates ENEXT and gates the data out to the EXT lines.

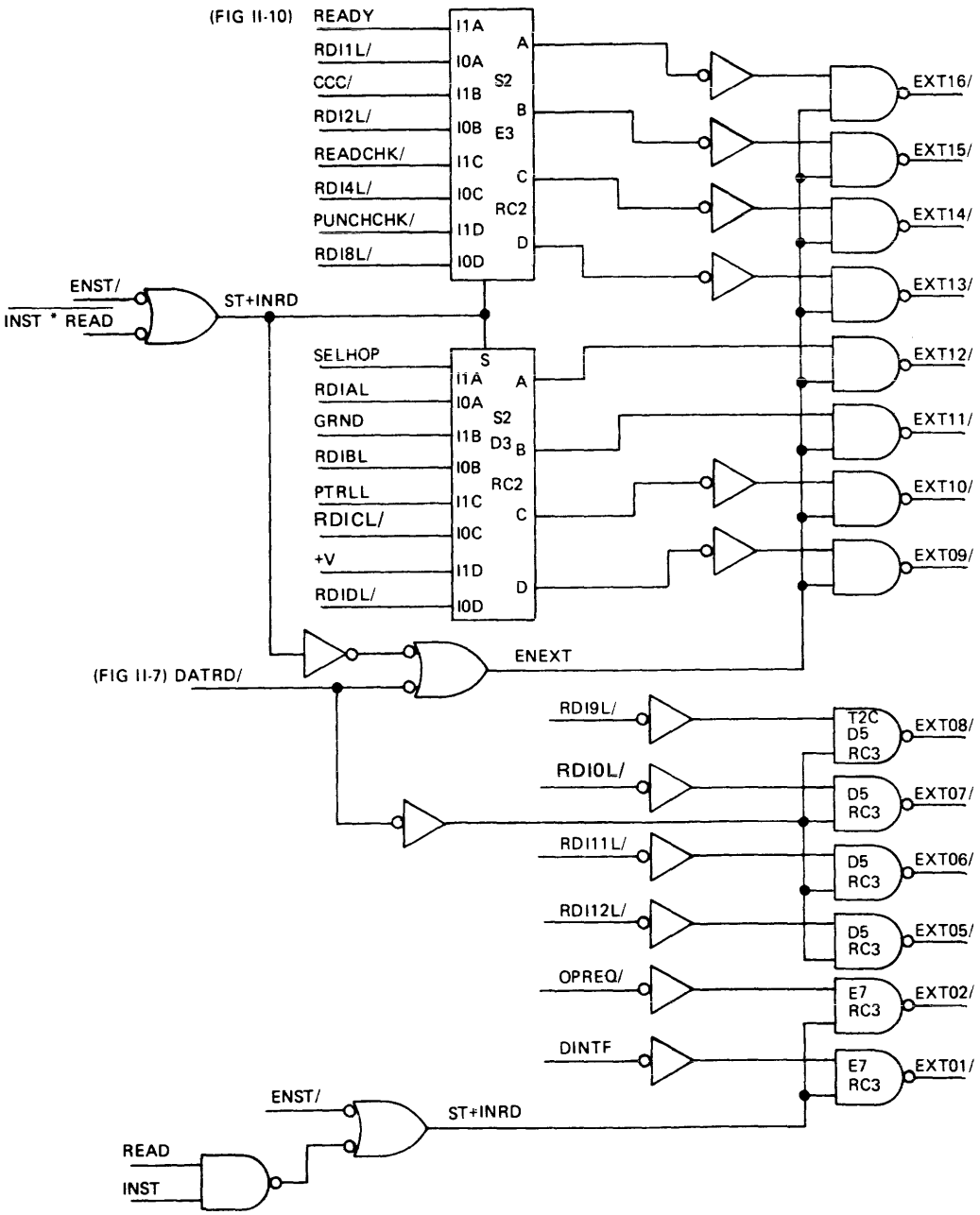


Fig. II-11 DATA OR STATUS TO EXT

Note that because of logic partitioning and circuit board layout the signal ST+INRD is generated twice, once on RC2 and again on RC3.

CLEAR READ BUFFER

During interface state 5 (ref. Fig. II-1) the processor may terminate the unload input memory operation after it has received sufficient data. (i.e., it is not obliged to read all ninety-six columns.)

Referring to Fig. II-12 it can be seen that if the processor sends a control word with MIR04 (terminate) true, to the IOC, the signals BIT4 and INST * WRITE make CLRRDBF/ false to the peripheral. This will cause the peripheral to cease its operation and the interface states return to 0.

If the processor sends a control word to the IOC with MIR14 and MIR15/, indicating a card operation with no data to be read, the signals UIB/ and LOB will make CLRRDBF/ false. In this case the interface states will effectively skip state 5 and return to state 0 from state 4.

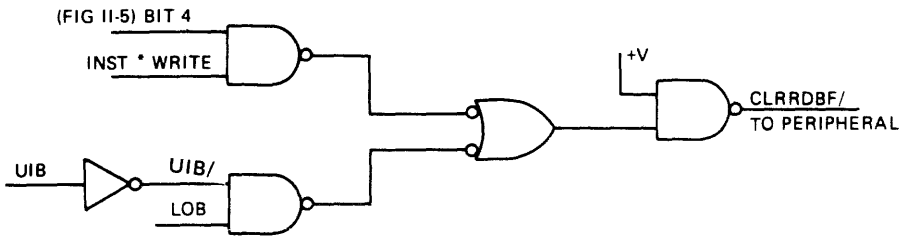


Fig. II-12 CLEAR READ BUFFER

INTRODUCTION

Section III contains the detailed description of the circuits used in the B311 IOC. The following subsections explains the electronic functions of all the Transistor-Transistor Logic (TTL) circuits used in the B311 IOC.

TRANSISTOR-TRANSISTOR LOGIC (TTL)

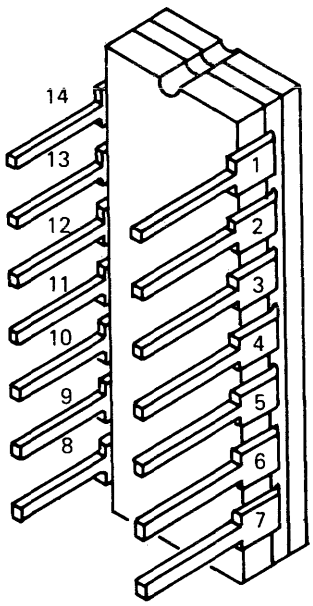
The Monolithic Elements, known as chips, are Dual-In-Line packages with either 14 or 16 pins. See Fig. III-1. The supply voltage for the TTL chips is +5.0 volts. A logical true level (HIGH LEVEL) is between +2.4 volts and +5.25 volts, and a logical false level (LOW LEVEL) is between 0 volts and 0.4 volts.

NAND GATES

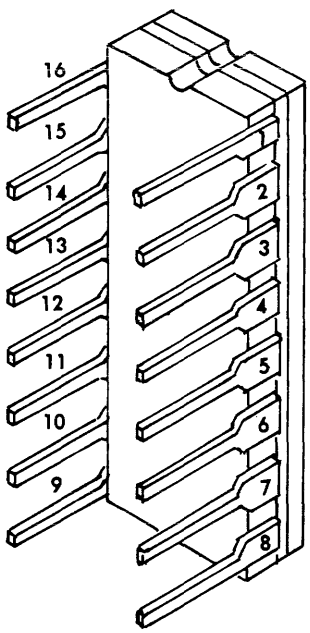
The various Nand Gates used in the B311 IOC are shown in Fig. III-2. The Nand Gates are 2, 3, 4 or 8 input gates. The 2, 3 and 4 input Nand Gates have a high speed gate series. The Nand Gates are identified by: T2 for the 2 input Nand Gate, T3 for the 3 input Nand Gate, T4 for the 4 input Nand Gate and T8 for the 8 input Gate.

The High Speed Gates are identified by T2H for the 2 input gate, T3H for the 3 input gate and T4H for the 4 input gate. The T2C series Nand Gate chips are open-collector output gates and are used for wire or functions. Whenever a Nand Gate is used from this chip, the output of the gate will be connected for a wire or function.

Operation for all Nand Gates used in the B311 IOC is as follows: a high level output is produced by any low level input and a low level output is provided when all inputs are high.



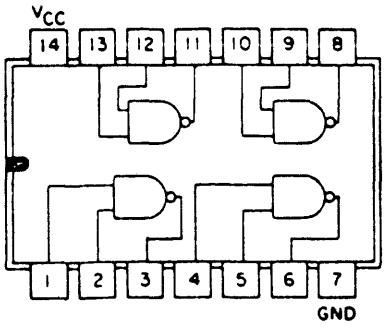
14-PIN PACKAGE



16-PIN PACKAGE

Fig. III-1 14 AND 16 PIN CHIPS

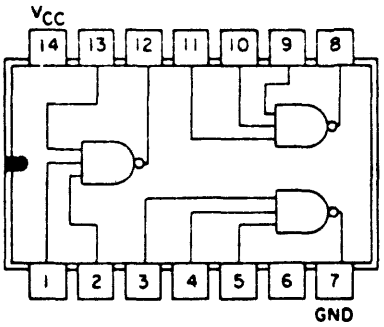
Circuit Detail



1447 3516 T2 2-INPUT NAND GATE (7400)

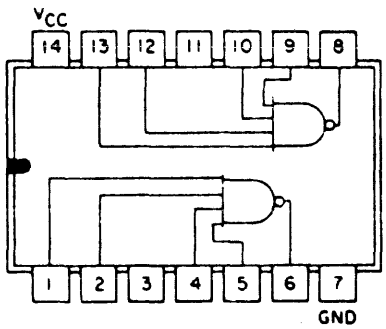
1479 0240 T2H 2-INPUT HIGH SPEED NAND GATE (74H00)

1447 3581 T2C 2-INPUT NAND GATE OPEN COLLECTOR (7438)



1447 3540 T3 3-INPUT NAND GATE (7410)

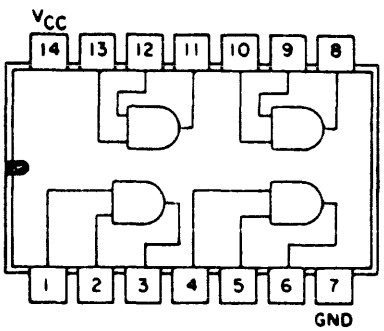
1486 8780 T3H 3-INPUT HIGH SPEED NAND GATE (74H10)



1447 3565 T4 4-INPUT NAND GATE (7420)

1479 0265 T4H 4-INPUT HIGH SPEED NAND GATE (74H20)

1447 3599 B4 4-INPUT NAND BUFFER (7440)

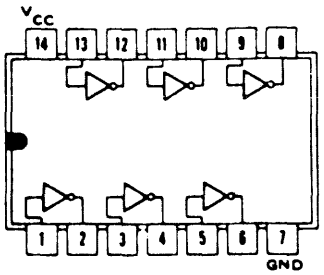


1447 3524 T2A 2-INPUT AND GATE (7408)

Fig. III-2 NAND & AND GATES

T1 HEX INVERTER

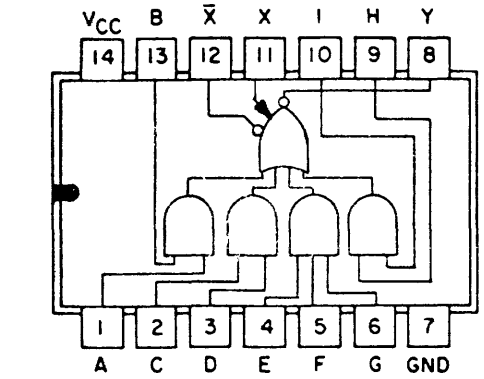
The Hex Inverter contains 6 inverter gates as shown in Fig. III-3. T1 is a standard inverter whereby a high level output is produced by a low level input and a low level output is produced by a high level input.



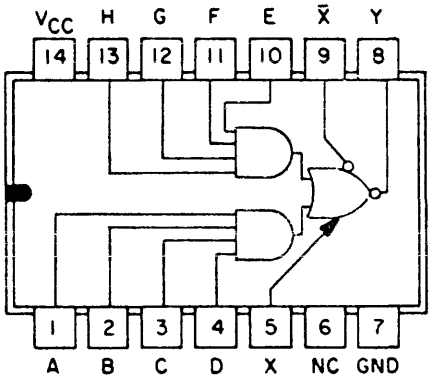
1447 3532

1447 3532 T1 HEX INVERTER (7404)

Fig. III-3



1447 3649 E24 2-2-2-3 INPUT AND–OR INVERTER GATE (74H53)



1447 3656 E42 4-4 INPUT AND–OR INVERTER GATE (74H55)

Fig. III-4 AND/OR INVERTER GATES

E24 2-2-2-3 INPUT AND/OR INVERTER GATE

The 2-2-2-3 Input And/Or Inverter Gate chip is shown in Fig. III-4. The function performed by this chip is specified by the following logical equation: Y/ = (AB)+(CD)+(EFG)+(HI). Refer to Fig. III-4.

A high level is required at all inputs of a AND gate to produce a low level output from this circuit. A low level at any one input of each of the AND gates produces a high level output.

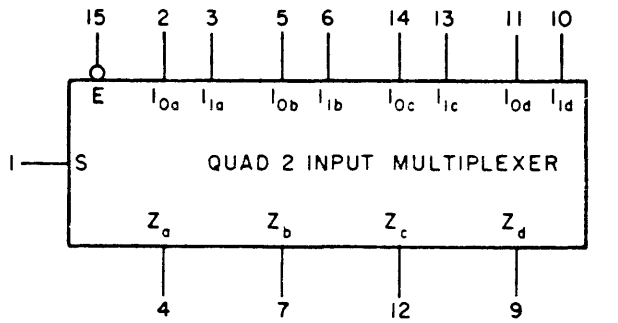
E42 4-4 INPUT AND/OR INVERTER GATE

The 4-4 Input AND/OR Inverter Gate chip is shown in Fig. III-4. The function performed by this chip is specified by the following logical equation: Y/= (ABCD)+(EFGH). Refer to Fig. III-4.

A high level is required at all inputs of a AND gate to produce a low level output from this circuit. A low level at any one input of both AND gates produces a high level output.

S2 QUAD 2-INPUT DATA SELECTOR

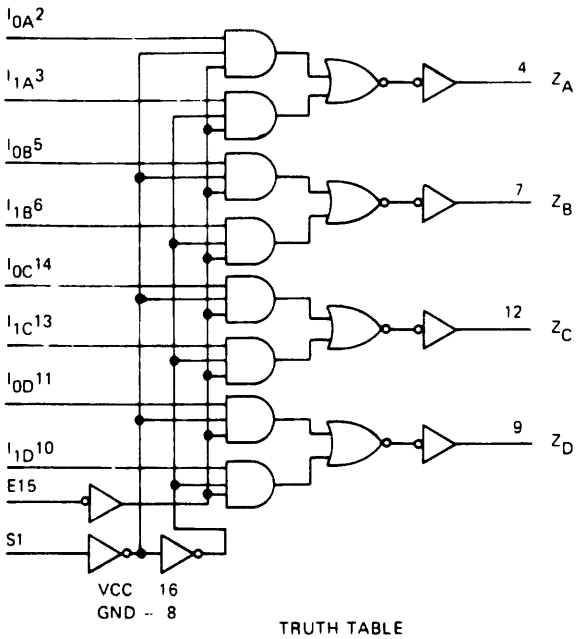
The Quad 2-Input Multiplexor chips as shown in Fig. III-5, consists of four 2-Input Multiplexors with common input select logic, common active low enable, and active high output. It allows four bits of data to be switched in parallel to the appropriate output from the four 2-bit data sources. When the enable is not active, all the outputs are held at a low level. The functional logic and the truth table for this chip is shown in Fig. III-6.



1447 3797 S2 (9322)

Fig. III-5 QUAD 2-INPUT DATA SELECTOR

Circuit Detail



PIN NAMES

S	COMMON SELECT INPUT
E	ENABLE (ACTIVE LOW) INPUT
MULTIPLEXERS A,B,C,D	
I_0, I_1	MULTIPLEXER INPUTS
Z	MULTIPLEXER OUTPUT

TRUTH TABLE

E	S	I_{0a}, I_{0b}, I_{0c}, I_{0d}	I_{1a}, I_{1b}, I_{1c}, I_{1d}	Z_a, Z_b, Z_c, Z_d
H	X	X	X	L
L	L	H	X	H
L	L	L	X	L
L	H	X	H	H
L	H	X	L	L

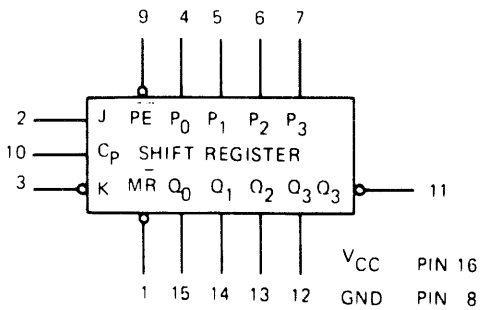
H HIGH VOLTAGE LEVEL
L LOW VOLTAGE LEVEL
X DON'T CARE CONDITION

Fig. III-6 S2 QUAD 2-INPUT MULTIPLEXOR, FUNCTIONAL LOGIC AND TRUTH TABLE

SU FOUR-BIT SHIFT REGISTER

The Four-Bit Shift Register chip is shown in Fig. III-7. This chip is a synchronous four-bit shift register and performs such functions as storage and shifting. This register has non-inverting outputs on each stage, plus an inverting output on the last stage, an overriding asynchronous master reset, JK input configuration, and a synchronous parallel load facility. Data entry is synchronous with the registers changing state after each low level to high level.

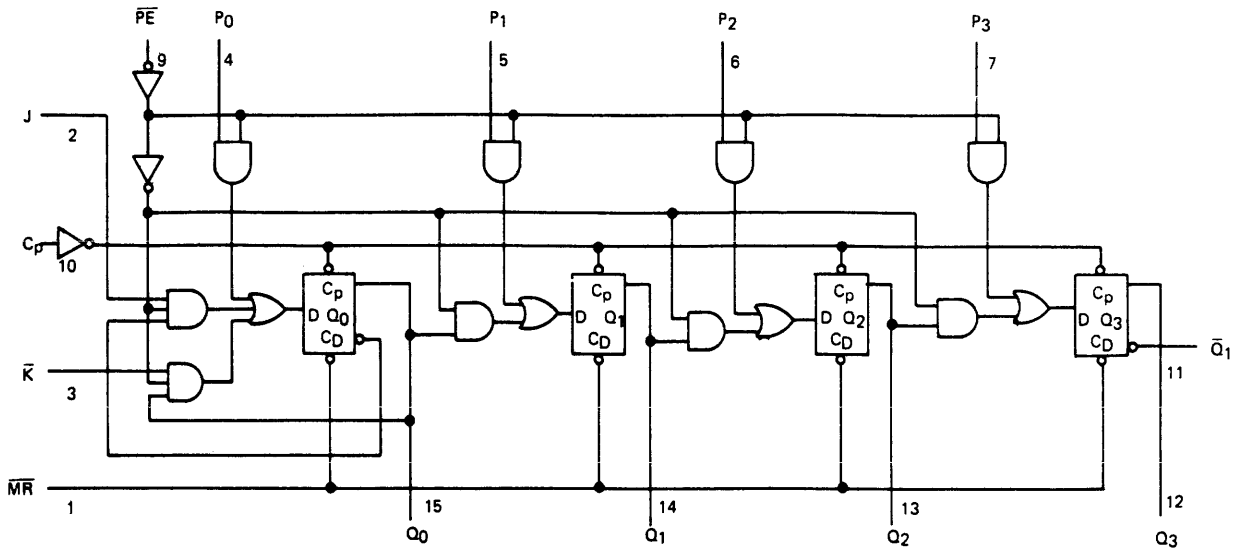
At transition of the clock pulse with the Parallel Enable input (PE) at a low level, the parallel inputs (P0,P1,P2,P3) determine the next condition of the shift register. When the Parallel Enable (PE) input is at a high level, the shift register performs a one bit shift to the right, with data entering the First Stage flip-flop through the JK inputs. When the two inputs (JK) are connected to each other, D type entry is obtained. When the asynchronous active low master reset is activated, all other input conditions are overridden and the register is cleared. The functional logic of this chip is shown in Fig. III-8.



1447 3755 SU 4-BIT SHIFT REGISTER (9300)

Fig. III-7 SU 4-BIT SHIFT REGISTER

Circuit Detail



J	K	Q_0 AT n + 1
L	L	L
L	H	Q_0 AT n (NO CHANGE)
H	L	Q_0AT n (TOGGLES)
H	H	H

PE = HIGH, MR = HIGH,
(n + 1) INDICATES STATE
AFTER NEXT CLOCK

PE	PARALLEL ENABLE (ACTIVE LOW) INPUT
P_0,P_1,P_2,P_3	PARALLEL INPUTS
J	FIRST STAGE J (ACTIVE HIGH) INPUT
K	FIRST STAGE K (ACTIVE LOW) INPUT
C_p	CLOCK ACTIVE HIGH GOING EDGE INPUT
MR	MASTER RESET (ACTIVE LOW) INPUT
Q_0,Q_1,Q_2,Q_3	PARALLEL OUTPUTS
$\bar{Q}_3$	COMPLEMENTARY LAST STAGE OUTPUT

SU TRUTH TABLE

Fig. III-8 SU – 4-BIT SHIFT REGISTER – FUNCTIONAL LOGIC AND TRUTH TABLE

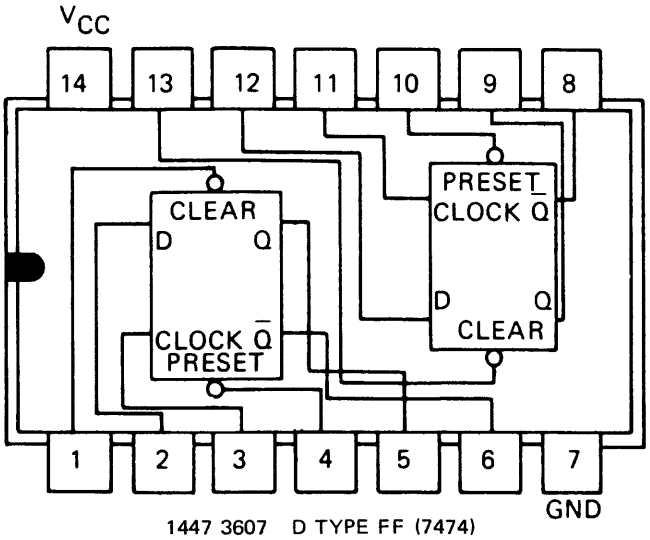


Fig. III-9 DF

TRUTH TABLE
(EACH FLIP-FLOP)

INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

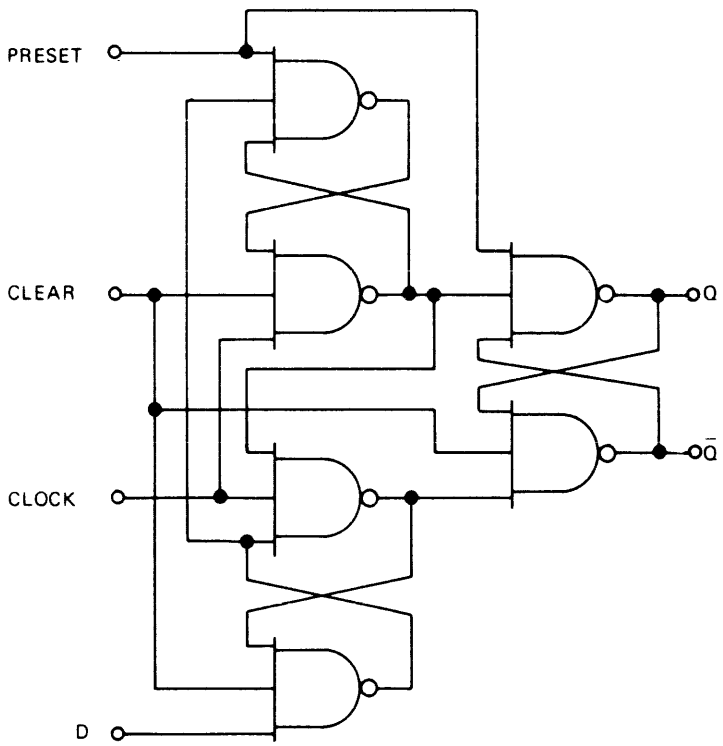
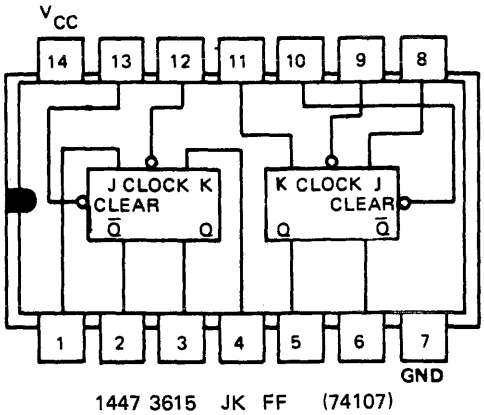


Fig. III-10 DF FUNCTIONAL LOGIC

DF DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

The DF Dual D Type Edge Triggered flip-flop chip, Fig. III-9 contains 2 flip-flops. The functional block diagram for each flip-flop is shown in Fig. III-10. These flip-flops have a direct clear and a preset inputs and complementary Q and Q/outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. A low level signal to the preset input sets Q to a logical 1 level. A low level signal to the clear input sets Q to a logical 0 level. The preset and clear inputs to each flip-flop are independent of the clock.

Circuit Detail



1447 3615 JK FF (74107)

Fig. III-11 JF

TRUTH TABLE (EACH FLIP-FLOP)		
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

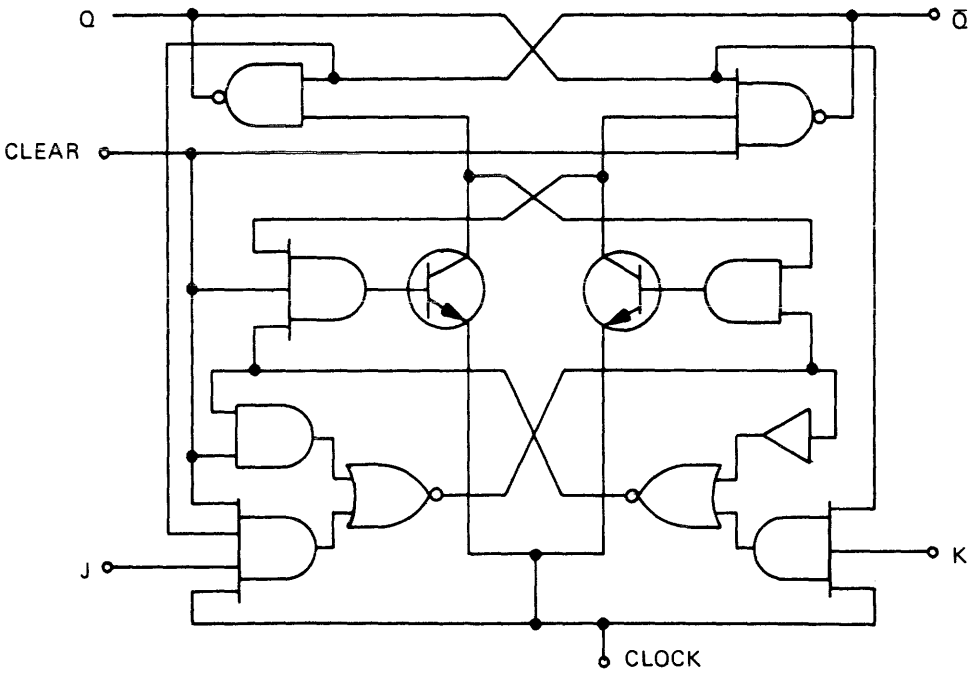


Fig. III-12 JF FUNCTIONAL LOGIC

JF DUAL J-K MASTER SLAVE FLIP-FLOP

The JF Dual J-K Master Slave flip-flop chip is shown in Fig. III-11. These J-K flip-flops are based on the master slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regualtes the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows.

1. Isolate slave from master.
2. Enter information from the J-K inputs to the master.
3. Disable J&K inputs.
4. Transfer information from master to slave.

A low level signal applied to the clear input sets Q output to a logical 0. The clear signal is independent of the clock. Refer to Fig. III-12 for the functional logic of this chip.

SS MONOSTABLE MULTIVIBRATOR CHIP

The SS Monostable Multivibrator chip and Truth Table are shown in Fig. III-13. The SS features D-C triggering from positive or gated negative going inputs with an inhibit facility provided. Both positive and negative going output pulses are provided with a full fan-out of up to 10 normalized loads.

Negative edge-triggered inputs at A1 and A2 allow the One-Shot Multivibrator to be triggered when either or both inputs are at a logical 0 level and the B input is at a logical 1 level. The B input is a Positive Schmitt-Trigger input, which allows jitter free triggering from inputs with slow transition times.

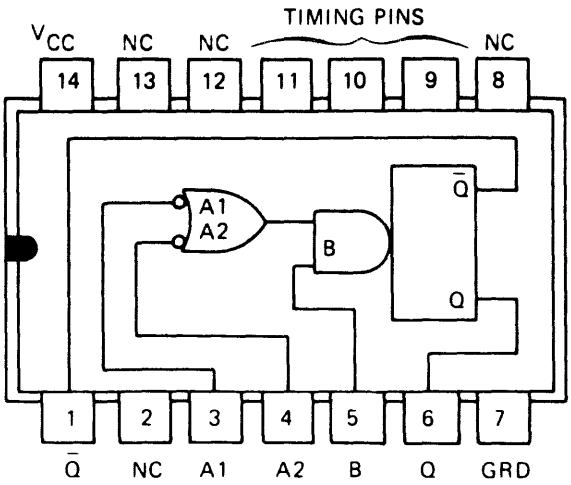
Whenever the B input is at a logical 1 level and both the A1 and A2 inputs are at a logical 1 level, the output is

Circuit Detail

TRUTH TABLE

INPUT			OUTPUT
A1	A2	B	
1	1	1	INHIBIT
0	X	0	INHIBIT
X	0	0	INHIBIT
0	X	1	ONE SHOT
X	0	1	ONE SHOT
X	0	1	ONE SHOT
0	X	1	ONE SHOT
X	1	0	INHIBIT
1	X	0	INHIBIT
1	1	1	INHIBIT
1	1	1	INHIBIT
X	0	0	INHIBIT
0	X	0	INHIBIT

NOTE: X INDICATES THAT EITHER A LOGICAL 0 OR 1 MAY BE PRESENT.



1447 3706 SINGLE SHOT (74121)

Fig. III-13 SS

inhibited. The output is also inhibited whenever the B input is at a logical 0 level. Refer to Fig. III-13. Once the One-Shot Multivibrator is triggered, the output is independent of further transistions of the input pulse and relies only on the external timing component (RC network) added to the circuit. The output pulse length may be varied from 40 nanoseconds to 40 seconds by selection of the appropriate timing components. With no external timing components added to the circuit, an output pulse of 30 nanoseconds can be obtained.

PERIPHERAL	MTR NAME	PART NUMBER	10 DIGIT ID #	OPERATING INSTRUCTIONS
A/B 9419-2 A/B 9419-6	RP96MTR	1448 7003 (punched tape)	4-3005-008-XX	1448 6880

The maintenance of the B311 is accomplished in a B700 system by use of the appropriate MTR procedure which is designed to suit a specific peripheral.

The above program uses a test deck:
RP96TD 1448 7961 TEST DECK.*

For operational details reference should be made to the B700 MTR Manual, form 1066115.

*The RP96TD test deck may be generated locally by punching the following set of cards:

1 Card (First)	Blank
2 Cards	1 Punched in All Columns (Refer to
2 Cards	2 Punched in All Columns Fig. VI-1 for
2 Cards	3 Punched in All Columns code set.)
2 Cards	4 Punched in All Columns
2 Cards	5 Punched in All Columns
2 Cards	6 Punched in All Columns
2 Cards	7 Punched in All Columns
2 Cards	8 Punched in All Columns
2 Cards	9 Punched in All Columns
2 Cards	: Punched in All Columns
2 Cards	# Punched in All Columns
2 Cards	@ Punched in All Columns
2 Cards	' Punched in all Columns
2 Cards	= Punched in All Columns
2 Cards	" Punched in All Columns
2 Cards	0 (numeric) Punched in All Columns
2 Cards	/ Punched in All Columns
2 Cards	S Punched in All Columns
2 Cards	T Punched in All Columns
2 Cards	U Punched in All Columns
2 Cards	V Punched in All Columns
2 Cards	W Punched in All Columns
2 Cards	X Punched in All Columns
2 Cards	Z Punched in All Columns
2 Cards	& Punched in All Columns
2 Cards	, Punched in All Columns
2 Cards	% Punched in All Columns
2 Cards	_ (underscore) Punched in All Columns
2 Cards	> Punched in All Columns
2 Cards	? Punched in All Columns
2 Cards	- (dash) Punched in All Columns
2 Cards	J Punched in All Columns
2 Cards	K Punched in All Columns
2 Cards	L Punched in All Columns
2 Cards	M Punched in All Columns
2 Cards	N Punched in All Columns
2 Cards	O Punched in All Columns
2 Cards	P Punched in All Columns
2 Cards	Q Punched in All Columns
2 Cards	R Punched in All Columns
2 Cards	! Punched in All Columns
2 Cards	$ Punched in All Columns
2 Cards	* Punched in All Columns
2 Cards	) Punched in All Columns
2 Cards	; Punched in All Columns
2 Cards	¬ Punched in All Columns
2 Cards	} Punched in All Columns
2 Cards	A Punched in All Columns
2 Cards	B Punched in All Columns
2 Cards	C Punched in All Columns
2 Cards	D Punched in All Columns
2 Cards	E Punched in All Columns
2 Cards	F Punched in All Columns
2 Cards	G Punched in All Columns
2 Cards	H Punched in All Columns
2 Cards	I Punched in All Columns
2 Cards	¢ Punched in All Columns
2 Cards	. Punched in All Columns
2 Cards	< Punched in All Columns
2 Cards	(Punched in All Columns
2 Cards	+ Punched in All Columns
2 Cards	| (all bits) Punched in odd numbered cols. only
1 Card	| (all bits) Punched in even numbered cols. only
1 Card	| (all bits) Punched in odd numbered cols. only
1 Card	| (all bits) Punched in even numbered cols. only
1 Card (Last)	| (all bits) Punched in odd numbered cols. only

133 Cards Total

Numeric Characters

Punch Positions		0	1	2	3	4	5	6	7	8	9
	Zone	B									
		A	A								
	Digit	8								8	8
		4				4	4	4	4		
		2		2	2			2	2		
		1	1		1		1		1		1

Alphabetic Characters

Punch Positions		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
	Zone	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B								
		A	A	A	A	A	A	A	A	A										A	A	A	A	A	A	A	A
	Digit	8							8	8								8	8							8	8
		4			4	4	4	4						4	4	4	4				4	4	4	4			
		2		2	2			2	2			2	2			2	2			2	2			2	2		
		1	1		1		1		1		1		1		1		1		1		1		1		1		1

Special Characters

Punch Positions		{	¢		<	(	+	|	!	$	*	)	;	¬	–	/	&	,	.	%	_	>	?	:	#	@	'	=	"	ъ
	Zone	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B															
		A	A	A	A	A	A	A	A								A	A	A	A	A	A	A	A							
	Digit	8		8	8	8	8	8	8	8	8	8	8	8			8	8	8	8	8	8	8	8	8	8	8	8			
		4				4	4	4	4			4	4	4	4					4	4	4	4			4	4	4	4		
		2		2	2			2	2	2	2			2	2			2	2			2	2	2	2			2	2		
		1			1		1		1		1		1		1		1		1		1		1		1		1		1	

CHARACTER SET AND PUNCH COMBINATIONS

Fig. V-1 TYPICAL 96 COLUMN CODE SET

INSTALLATION

The B0311 or B0418 card peripheral IOC may be installed in any one of the seven interchangeable control locations in the B700 Processor logic frame. The locations are numbered IOC (or DDP) 1 through IOC 7. Refer to tables VI-1 and VI-2 for installing the printed circuit boards in B705/711 and B771/772 Processors, respectively.

After installing the boards, connect the two front-plane connectors between the following boards:

a. RC1 (1448 8241) and RC2 (1447 5214).

b. RC3 (1448 8290) and RC4 (1448 8324).

ADAPTER CABLE

The IOC adapter cable (1449 1252) provides the means of connecting either (or both) of the I/O cables (supplied with the peripheral) to the IOC connector on the logic frame.

The single-ended 50-pin connector is connected to the appropriate IOC connector, while the two connectors on the other end are mounted on the adapter panel (part of A.C. control assembly) with the supplied mounting hardware.

NOTE: It is recommended that the connectors marked J14 and J15 be mounted in locations J20 and J21, respectively. (Refer to B700 Processor Technical Manual, Form 1064482, Sec. VI.)

When installing the peripheral cables, care must be taken to ensure that J14 (J20) connects to PCB 14 in the A9419, and that J15 (J21) connects to PCB 15.

After the IOC and cables have been installed, the processor +5V supply must be checked as outlined in document 1448 4588 (FT&R document 1448 7185, Volume 1, supplied with Processor).

After the peripheral has been installed, the appropriate MTR should be run to verify that the system is operational.

Table VI-1

Reader Punch IOC Cards, Locations, and Connectors
(B705/711 Processor)

Card Type	Part No.	DDP Number and Card Location						
		1(J97)	2(J96)	3(J95)	4(J94)	5(J93)	6(J92)	7(J91)
RC1	1448 8241	FW6	DW6	FV4	DV4	FV2	DU2	DT0
RC2	1447 5214	FW3	DW3	FV1	DV1	FT9	DT9	DS7
RC3	1448 8290	FW0	DW0	FU8	DU8	FT6	DT6	DS4
RC4	1448 8324	FV7	DV7	FU5	DU5	FT3	DT3	DS1

Table VI-2

Reader Punch IOC Cards, Locations, and Connectors
(B771/772 Processor)

Card Type	Part No.	DDP Numbered Card Location					
		2(J96)	3(J95)	4(J94)	5(J93)	6(J92)	7(J91)
RC1	1448 8241	DW6	FV4	DU4	FU2	DU2	DP1
RC2	1447 5214	DW3	FV1	DV1	FT9	DT9	DN8
RC3	1448 8290	DW0	FU8	DU8	FT6	DT6	DN5
RC4	1448 8324	DV7	FU5	DU5	FT3	DT3	DN2

cut along dotted line

cut along dotted line

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