

Burroughs
SERIES E 2100
DIRECT ACCOUNTING
COMPUTER

INSTRUCTION BOOK

Section VIII



ELECTRICAL

REFERENCE INFORMATION

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Electrical Reference Information

SIGNALS AND TERMS

| | |
|------------|---|
| A | Memory location 01. |
| Add A | Add selected memory location or Keyboard to A. |
| Add B | Add selected memory location or Keyboard to B. |
| Add C | Add A, B or Keyboard to a C location. |
| Adder | System of AND gates, OR gates and inverters which combines data from the MR, WR & CiFF to provide an instantaneous sum. |
| AEC | Automatic Electronic Cycles, Cycles of the Electronic Processor only. |
| AEC TC1 | A timing cam operated from the AEC tappet reset shaft. |
| AT | All totals. |
| <u>ATR</u> | Not all totals reset. |
| AP | Amount Protection (Causes a dollar sign to be printed to the left of MSD). Associated Control Unit abbreviation is AP. |
| A Status | Signal which permits altering routine according to whether memory location 01 is clear or non-clear, minus or plus. |
| B | Memory location 10. |
| BB | Suffix used with other signals to mean Before Buffer. |
| B Status | Signal which permits altering the routine according to whether memory location 10 is clear or non-clear, minus or plus. |
| C | Character signal such as "AL", "TX", etc. |
| "C" Char | Keyboard activated Character. Prints and causes the amount in B & D to be shifted 2 places to the right. |
| Ci | Carry-in signal to the adder. Produced by the carry out-signal resulting from a sum greater than 9. |
| CFM | Change factor and multiply. Associated Control Unit abbreviation is CFM. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|----------------------------|--|
| CLRA, B, D, C | Clear data from respective memory locations during T6 time. Associated Control Unit abbreviation is C. |
| CLR MEM. | Clear entire memory from depression of CL MEM key and pin in Lane 65. |
| C- | C minus. Amount indexed on keyboard with the subtract key. |
| CMAU & CMAT 1-8 | Count memory address tens and units. |
| CMS | "C" or "M" shift. Causes 2 or 3 place shift to right. |
| CN | Consecutive numbering signal. Associated Control Unit abbreviation is CN. |
| CNT | Net Count. Adds or subtracts one to or from col. 10 of P during transfer time. |
| CO | Carry out. Signal developed by adder to indicate a sum greater than 9. |
| C+10 | Perform arithmetic in selected C address and in memory location 10 higher than selected address. (Programed location must have an even tens digit.) Associated Control Unit abbreviation is ETD. |
| Con 10 | Consecutive tens. Perform C arithmetic for selected C address and for additional location of C in increments of 10. Associated Control Unit abbreviation is CT. |
| CS | Change Sign. |
| C1-C7 | Signals from character keys which control setting of the character rack stop flip-flop. |
| CTR GND & CTR LN COMMON | Controlled ground or controlled common indicates grounds or commons that can be switched by the manual relay. |
| CY | Carry signal developed in each 1 bit binary adder. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|------------------------------|--|
| CY4-CY8 | Signals indicating carry conditions between adder and decimal corrector |
| D | Memory location 11. |
| DCA if MN | Do programed C arithmetic if the status of A (or B if pinned) is minus and not clear--minus net. Associated Control Unit abbreviation is AMC or BMC. |
| DCA if PN | Do programed C arithmetic if the status of A (or B if pinned) is plus & not clear--plus net. Associated Control Unit abbreviation is APC or BPC. |
| DD | Digit Distributor flip-flop. Selects keyboard column or digit position of active memory location. |
| DDO | Sign digit position of any memory location. |
| DDMSD | Digit Distributor for the most significant digit of a word. |
| DDT | Digit Distributor for tens of memory address. |
| DDU | Digit Distributor for Units of memory address. |
| DECIMAL CORRECTOR | Circuitry which corrects adder outputs between 10 and 19 to a carryout and a significant digit. |
| DELTA MACH. RESET (Δ MR) | 11 to 20 μ s pulse which is delayed 67 to 97 μ s from machine reset. |
| DELTA READ (Δ R) | A signal developed by the memory timing circuit to control reading from memory. |
| DELTA WRITE (Δ W) | A signal developed by the memory timing circuit to control writing into the memory. |
| DIVIDEND | The factor that is stored in B at the start of a divide operation. |
| DIVISOR | The factor that is stored in P during a divide operation. |
| DMV | Delay multivibrator - a mono-stable multivibrator that produces a pulse of fixed amplitude and duration with varying input signals. |
| DSC | Disconnect-circuitry which contains the +35V used in conjunction with the special wetters for the keyboard data key switches. |
| DV | Layout designation for divide. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|-------------------------------|--|
| ENABLE RSC WRITE | Signal which enables the writing of columns 1-6 with Read Specified Columns programed. |
| EOC | End of Cycle. A signal that occurs at the end of each (A, B & C) arithmetic cycle. |
| EOCA | End of C arithmetic. Indicates all arithmetic for the indexed machine Cycle has been completed. |
| EOT | Signal produced at the end of each T time. |
| END OP | End Operation signal which indicates that the electronic cycle has been completed. |
| ESK | Enable shift from C or M Key. |
| EUK | Enforced Use of Keys. Pertains to the forced indexing of memory address on manual cycles or when programed with lane 53 (Read Keyboard Address). |
| FF | Flip-Flop, or bi-stable multivibrator. |
| FFC | FFC is the output of an AND gate whose inputs are the not sides of FFA, FFB, FFD and FFP. |
| GT CLK DR | Gated Clock Driver. The signal which permits the clock circuit to produce a special clock pulse along with the regular clock pulse. |
| GT CLK | Gated Clock pulse. A regular clock pulse only occurring when setting or resetting the WR flip-flops with any gate to WR signal high. |
| GT INHIBIT | Gated Inhibit signal. Causes the inhibit current to flow in all memory planes on write operations when no cores are to be switched. |
| GTCMS → WR | Gate "C" or "M" Shift to the Working Register. Allows the "C" or "M" keyboard information to be transferred to the WR. |
| GTKB → WR | Gate Keyboard to the Working Register. Allows the keyboard data to be transferred to the WR |
| GTMAR TENS and GTMAR UNITS | Gate Memory Address Register Tens and Units from keyboard or lane control. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|--------------------|--|
| HB | Heavy Buffer. |
| I | Inverter-circuitry that delivers an output 180° out of phase from input. |
| I1, 2, 4, & 8 | Inhibit Signal from memory driver which causes current to flow in the respective inhibit lines. |
| IND | Indicator Card used as a service aid. Provides a light as an indication of the set or reset condition of FF's such as T times DD's, etc. |
| INHIBIT LINE | A wire which passes through every core of a given memory plane to control the writing of data. These lines run parallel to the Y lines. |
| INITIAL CONDITIONS | Term used for the logic signals that are initially set at the beginning of each T time. |
| KBMA COMMON | The ground for the Keyboard Memory Address keys. This ground is under control of the manual relay and the Read Keyboard address lanes 53 and 65. |
| KBMAU 1, 2, 4 & 8 | Keyboard Memory Address Units signals from the KBMAU decoder. |
| KBD 1-9 | Keyboard digits 1 thru 9 which are encoded to binary KB1, KB2, KB4, KB8 bits. |
| LC A, B, C, D & E | Standard logic cards A, B, C, D & E. |
| LN | Lane Control |
| LN3 if NC | Lane 3 index if Non-Clear (Controlled by status of A or B.) Associated Control Unit abbreviation is AN3 or BN3. |
| LN3 if MNC | Lane 3 index if Non-Clear minus (controlled by status of A or B.) Associated Control Unit abbreviation is AM3 or BM3. |
| LNMAT 1, 2, 4 & 8 | Lane Memory Address Tens 1, 2, 4 and 8 bits. |
| LNMAU 1, 2, 4 & 8 | Lane Memory Address Units 1, 2, 4 & 8 bits. |
| LN3 SOL | Solenoid that indexes Lane 3 tab. Controlled by status of A or B. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|----------------------|--|
| LS 1, 2, 3, 4 or 8 | Lane Shift. Indicates number of places B and D are to be shifted during TO time. |
| LSD | Least significant Digit. |
| MAN RELAY | Manual Relay. |
| MAT | Memory Address Tens from KB or lane. |
| MAU | Memory Address Units from KB or lane. |
| M CHAR | Character printed when M key is indexed. M key also causes a shift of 3 places to the right in B and D during TO time. |
| MAG PICKUP | Magnetic Pickup which generates pulses to indicate the position of the add racks. |
| MAN COMMON | Ground for memory address and control keys during a manual operation. |
| MEM CLR SYM | Signal for Clear Memory symbol (Δ). |
| MART 1 & 2 | Memory Address Tens Register flip-flops used to control the memory address tens during C arithmetic. |
| MEM ADD | The active memory address selected by the keyboard or lane programing. |
| MR | Memory Register. Consists of 4 special flip-flops which receive data read from memory. |
| MR = O | Signal which indicates that the MRFF's are reset and contain "O". |
| MR \rightarrow MEM | Signal indicating that the data in the MRFF's is to be written into the memory. |
| MR \rightarrow WR | Signal which indicates that the data in the MRFF's is to be transferred to the WRFF's. |
| MSD | Most Significant Digit. |
| MTA & MTB | Memory timing A & B special circuits which develop signals from the clock pulse to be used during reading and writing in memory. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|------------------|--|
| MUL | Multiply. Associated Control Unit abbreviation is M. |
| MD | Memory Driver. |
| 15 V(M) | The -15V for the memory circuits. |
| NC | Non-Clear. |
| NS COMMON | Ground for non-sensing lanes 51 thru 66. |
| 9 → WR | A logic signal when high causes the WR1 and WR8 FF's to be set. |
| P | Memory location 00. |
| PG | Pulse generator. |
| PG GRN | Pulse generator ground. |
| PN | Plus net. |
| PRT or PK | Print or Print keyboard analogous to Read or Read keyboard (see R). |
| PRINT A, B, OR C | Print data from the selected memory location. Associated Control Unit abbreviation is R (Read or Subtotal). |
| POR | Power on Reset. |
| PC | Print Control. |
| PS | Pulse Standardizer. |
| QUOTIENT | Result of division stored in B after the divide operation. |
| R | Read. (In effect a subtotal operation) |
| RE | Reverse Entry. |
| REMAINDER | Data in D after division is finished. |
| RKA | Read keyboard address. Associated Control Unit abbreviation is also RKA. |
| RND | Round. Indicates a round operation. Associated Control Unit abbreviation used with shift is S5R or S4R, etc. |
| RS | Reset Standardizer. |
| RS | Ribbon shift. |
| RS1 - RS12 | Rack stop FF signals. |

(Continued)

SIGNALS AND TERMS (Continued)

| | |
|----------------------|---|
| RSD | Rack stop driver. |
| RR SOL | Red Ribbon solenoid. |
| RW | Relay Wetter circuit. |
| SCALING | Entering factors into the keyboard in the proper place to obtain the correct decimal location in the result of multiplication or division. |
| SO - S9 | Sequences of logic flow in the arithmetic & memory unit within each T time. |
| SUBTOTAL | Subtotal memory location A, B or C. Associated Control Unit abbreviation is R (Read). |
| SM | Shift Memory. Indicates that the selected ETD memory location is to be altered to the next increment of ten (ETD must also be programed). Associated Control Unit abbreviation is ASM or BSM. |
| SPL COMMON | A ground used with the CLR MEM, AT, RKA and EKA. |
| SR RE | Start Relay Reset. A reset pulse triggered by the dropping of the start relay. |
| SSC | Single Shot Clock. A circuit enabling one clock pulse to be triggered at a time for trouble shooting purposes. |
| SP | Sense Pulse which results from switching of cores during read. |
| STEP DD | Reset a given DDFF and set the next higher DD. |
| STI | Substitute Tens Increment of C address. Programable lane for changing C address by 10. |
| STROBE (Δ 5) | A pulse from memory timing card B which gates the sense pulse during a read memory operation. |
| SUM 1, 2, 4 & 8 | Binary output lines from the adder. |
| SUM = 0 | A signal that is high when the sum of the adder inputs is equal to zero or ten. |
| SUM \neq 0 | A signal that is high when the sum of the adder inputs not equal to zero or ten. |

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SIGNALS AND TERMS (Continued)

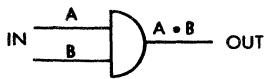
| | |
|-------------------------------|--|
| SUM = 9 | A signal that is high when the sum of the adder inputs is equal to nine. |
| SUM → MEM. | Signal to indicate that the adder output is to be written in memory. |
| SYM | Symbol column signal. |
| SD | Solenoid Driver. |
| SW or RW | Special Wetter or Relay Wetter. |
| TO - T7 | Time 0 through 7, time periods into which electronic operations are divided. |
| TC | Transfer clear, programable circuit which allows transferring data into a memory location with prior clearing. |
| TC 661-669 | Timing signals from timing switches in the printer. |
| T/C 1, 2, 4 & 8 | True/complement input to the adder. |
| TPM | Transfer to P minus. Transfer data to P and change the sign of the number. |
| TM and $\overline{\text{TM}}$ | Transfer minus and not transfer minus. |
| TOTAL | Total. Read A, B or C and clear during T6. |
| RSC | Read Specified Columns. |
| TX | Indicates A, B or C arithmetic time (T3, T4 or T5). |
| US2 and 4 | Uncorrected Sum 2 and 4 signals which appear between the adder and decimal corrector. |
| WR | Working Register. Four FF's used throughout the arithmetic operations as a temporary storage for data. |
| WR → MEM | Indicates that the data in the WR is to be written in the memory. |
| WRITE or W | Logic signal which indicates that data is to be written in the memory. |
| WR = 0 | Indicates that all WRFF's are reset. |
| WE | Wetter Encoder. Converts keyboard MAT and MAU decimal signal to binary form. |

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SIGNALS AND TERMS (Continued)

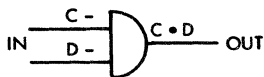
| | |
|-----------|--|
| X | Driver lines in the core memory planes. |
| X-DRIVERS | Circuits which cause read or write current to flow in the X-wires. |
| Y | Driver lines in the core memory planes. |
| Y-DRIVERS | Circuits which cause read or write current to flow in the Y-wires. |

LOGIC SYMBOLS

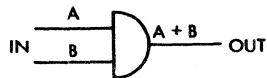


AND GATE - A circuit that permits a high signal to appear at its output only when a high signal is applied simultaneously to each of its inputs. This is more specifically a **POSITIVE AND GATE** but is usually referred to simply as an **AND GATE**. See **NEGATIVE OR GATE**.

POSITIVE AND GATE - See **AND GATE**

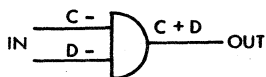


NEGATIVE AND GATE - A circuit that permits a low signal to appear at its output only when a negative signal is applied simultaneously to each of its inputs. This circuit is identical to a **POSITIVE OR GATE**.



OR GATE - A circuit that permits a high signal to appear at its output whenever a high signal is applied to at least one of its inputs. This is more specifically a **POSITIVE OR GATE** but is usually referred to simply as an **OR GATE**. See **NEGATIVE AND GATE**.

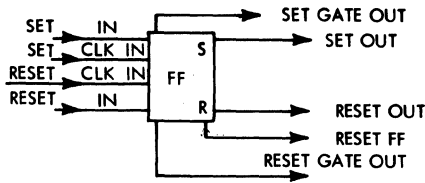
POSITIVE OR GATE - See **OR GATE**



NEGATIVE OR GATE - A circuit that permits a low signal to appear at its output whenever a low signal is applied to at least one of its inputs. This circuit is identical to a **POSITIVE AND GATE**.

FLIP-FLOP - A bistable multivibrator with typical inputs and outputs as shown. With trigger signals previously applied on the Set and Set

LOGIC SYMBOLS (Continued)



Clk legs simultaneously, the FF will be triggered to a set condition as the input gate goes negative. A high level signal then appears on the Set output. The gated Set input pulse appears on the Set Gate output leg. With trigger signals applied to the Reset Clk and Reset input legs simultaneously, the FF is reset and a high level output appears on the reset outputs. Also, the gated reset pulse appears on the reset gate output leg. With a reset signal applied to the Reset FF leg, the FF will be triggered to a reset condition.



INVERTER - Circuitry which inverts the input signal and produces an output signal 180° out of phase.



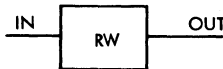
RACK STOP DRIVER - Amplifier which produces an output to momentarily interrupt the current to the Rack Stop Solenoids.



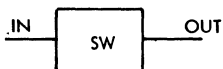
SOLENOID DRIVER - Amplifier to produce high current output for driving solenoids.



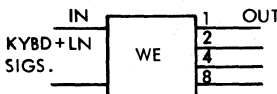
MEMORY DRIVER - Current amplifier that produces the drive current for switching the cores in the memory.



RELAY WETTER - Circuit which contains wetting voltages to ensure switch continuity. Used on all relays and switches except the data Key switches and some of the control key switches.



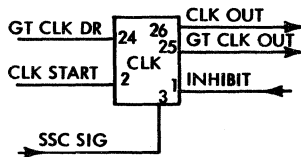
SPECIAL WETTER - Circuits which contain part of the wetting voltage to ensure switch continuity from the keyboard data key switches and some of the control key switches. The remainder of the wetting voltages required is supplied by the Disconnect Circuitry.



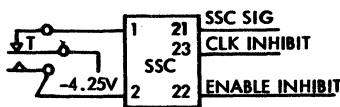
WETTER-ENCODER - Circuitry for wetting the MAT and MAU electrical lanes and wetting and encoding the MAT and MAU keyboard switch decimal signals to binary form.

CLOCK - Free running multivibrator which produces the timing clock pulses to control the system logic. The clock pulses are emitted from the clock out leg. When the Gated Clk.

LOGIC SYMBOLS (Continued)



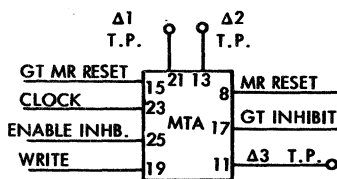
driver signal is applied, it is gated with a clock pulse and produces a gated clk pulse signal along with the regular clock pulse. The start leg has a signal applied whenever the system is turned on, this is to ensure clock multivibrator starts. The inhibit leg stops the clock when the Single Shot clock card is inserted. This inhibit signal prevents the regular clock pulses from being emitted when the SSC is being used. The SSC signal produced by the SSC multivibrator is fed into the clock card and out the normal clock out circuit.



SINGLE SHOT CLOCK - The SSC is used to manually produce one clock pulse approximately the same width and amplitude as the regular clock pulse for trouble-shooting purposes. When the push button is depressed, one clock pulse is emitted from SSC signal output leg. The clock inhibit signal inhibits the clock multivibrator when the SSC card is inserted. The enable inhibit signal is used to control the inhibit drivers connected with the core memory. This signal will remain high only as long as the SSC switch is held depressed.

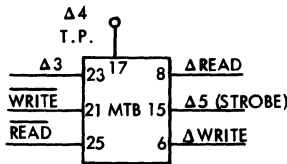


HEAVY BUFFER - An emitter follower circuit to provide increased power for a signal to drive a number of other logic stages with no inversion of the input signal.



MEMORY TIMING A - Circuitry used to provide some of the delayed signals and gating required by the core memory. The MTA circuit is triggered by the clock pulse. Following the clock pulse the MTA circuit produces three delayed pulses ($\Delta 1$, $\Delta 2$, and $\Delta 3$) each following the other. The incoming write signal or Enable Inhibit (active when the SSC is used) is gated with $\Delta 1$ to produce the output signal Gated Inhibit. The incoming GT MR Reset signal is gated with the $\Delta 2$ signal to produce the MR Reset output. Test points are provided for checking the $\Delta 1$, $\Delta 2$ and $\Delta 3$ timing signals. The $\Delta 3$ signal is used to trigger the MTB circuitry.

LOGIC SYMBOLS (Continued)



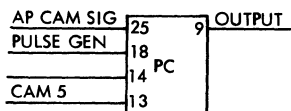
MEMORY TIMING B - The Memory Timing B circuit provides signals for reading and writing into memory not provided by the Memory Timing A circuit. The $\Delta 3$ signal from MTA is gated with either the $\overline{\text{read}}$ or $\overline{\text{write}}$ signals from the logic to produce delayed read (Δ Read) or delayed write (Δ Write) signals. Whenever a Δ Read signal is produced ($\Delta 3$ and $\overline{\text{Read}}$) a $\Delta 4$ signal is also produced and causes the $\Delta 5$ or Strobe signal to be emitted.



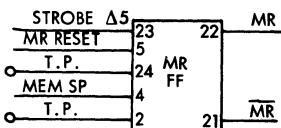
INDICATOR CARD - Contains 8 neon light which are wired to various flip-flops to provide a visual indication of the condition of the FF (set or reset) which aids in trouble shooting.



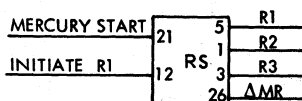
PULSE GENERATOR - The pulse generator is a combination of a magnetic pickup that senses the position of the printer racks and a circuit that amplifies these signals to be fed into the Print Control Card.



PRINT CONTROL - The print control circuitry produces pulses of the correct amplitude and duration after receiving the initial pulses from either the amount protection (\$) timing signal or the pulse generator. The Cam 5 signal is gated together with the modified AP (\$) and pulse generator signals to produce the output signals.



MEMORY REGISTER - The MR's are used to temporarily store the information when the core memory is sensed. When the Strobe and memory sense pulses occur simultaneously the MR FF is set producing an output on the MR leg. The MR reset leg has a pulse applied just prior to the sense pulse and strobe signals in order to reset the FF and make it ready for new information. The test points (T.P.) are provided to enable observation of the memory sense pulses with an oscilloscope.



RESET STANDARDIZER - This circuitry produces signals of a definite amplitude and duration for resetting FF's and produces Δ Machine Reset signal when the mercury start signal is applied. The initiate R1 signal triggers only the Reset 1 output. The initiate R1 signal is produced

LOGIC SYMBOLS (Continued)

when the machine is turned on and R1 resets the DDFFS.

FLIP-FLOPS

There are approximately 84 flip-flops in the arithmetic and memory unit. They are identical with the exception of the MR flip-flops. The flip-flops are designed to trigger on a negative-going pulse or voltage swing. Since the clock or control pulse of the machine is a positive pulse (-4V to ground), the flip-flops trigger on the trailing edge of the pulse. Since a flip-flop is bistable, a signal is required for resetting as well as setting. The set or reset signal is almost always gated with a clock pulse to time the operation throughout the cycle.

The flip-flops may also be reset by a reset pulse without a coincident clock pulse. This signal of approximately -15V is used to reset the flip-flops prior to the start of a cycle.

The following is a list of flip-flops with their basic functions:

| <u>DESIGNATION</u> | <u>NAME</u> | <u>FUNCTION</u> |
|----------------------|-------------------------------|---|
| AMFF | Automatic Mode | Provides control signal during the AEC operations. |
| APFF (\$) | Amount Protection | The APFF controls the search for the dollar signs. |
| CiFF | Carry-In | Provides a means of carrying from one digit to another on an arithmetic operation and as a control or storage flip-flop on other operations. |
| CFMFF | Change Factor Mode | Permits selection of memory location 02 instead of 00 during multiply or divide when lane 46D is programed. |
| COMPFF | Complement | Controls the addition of complements on arithmetic operations and is used as a control flip-flop on other operations. |
| CHARFF | Character | The character flip-flop controls the release of the rack stop clapper for the character column. |
| CMAUFF 1, 2, 4, 8 | Count Memory Address Units | CMAU and CMAT flip-flops select the memory address on an all total operation. The flip-flops are counted consecutively from 00 to 29 (39) (79) (99) by the END OP signal. |
| CMATFF 1, 2, 4, 8 | Count Memory Address Tens | |
| DDREVVFF | Digit Distributor Reverse | The Digit Distributer Reverse flip-flop is used during the shift and multiply operation to reverse the order of selection of data digits by the DDFV's from the memory. |

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FLIP-FLOPS (Continued)

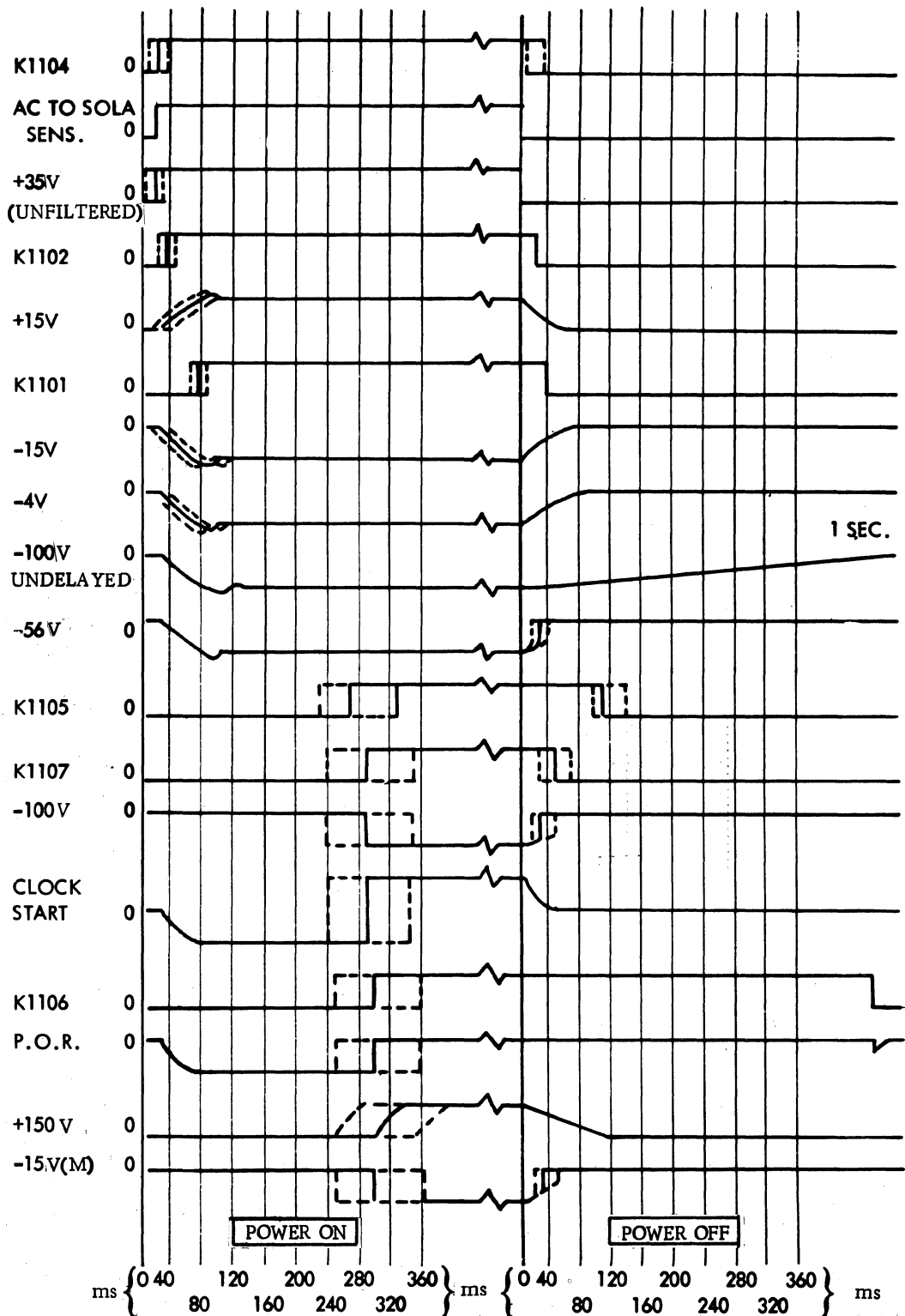
| | | |
|---|---|--|
| DDOFF thru DDMSD, DDUFF and DDTFF | Digit Distributer 0 thru MDS, units and tens of memory address | The Digit Distributer flip-flops select the active digit from memory, or the keyboard column on a keyboard entry. |
| DDMSD | Most significant digit. | The most significant data digit (Col. 12). |
| DVFF | Divide | Provides signals for the divide operation. |
| ECNCFE | Electronic Cycle not Complete Flip-Flop | Locks machine if the electronic unit does not complete the required T times. |
| FFA | A | Selects the A memory location (01) as the active location. |
| FFB | B | Selects the B memory location (10) as the active location. |
| FFC | C | See "SIGNALS AND TERMS". |
| FFD | D | Selects memory location 11 as the active location. |
| FFP | P | Selects memory location 00. |
| LN3FF | Lane Three | The lane three flip-flop controls indexing lane 3 carriage control from status of A or B. |
| MAFF | Memory Address | Signifies an invalid memory address when set. |
| MART 1 and MART 2 | Memory Address Register Tens 1 & 2 | The MART 1 & 2 flip-flops alter the programmed memory address in conjunction with consecutive tens, modified consecutive tens, etc. |
| MR1FF MR2FF MR4FF MR8FF | Memory Register 1, 2, 4 & 8 bits. | These are special flip-flops which receive data read from the memory. |
| MR → MEMFF | Memory Register to Memory | The MR → MEMFF when set allows the data in the MRFF's to be written into memory. |
| NZFF | Non-zero | Non-zero flip-flop indicates clear or non-clear condition of A or B during C arithmetic time. Non-zero is used as a control flip-flop on other operations. |
| PAFF | Print Alarm | Indicates that the proper number of pulses were not received during print (T2) and that the print should be verified. |

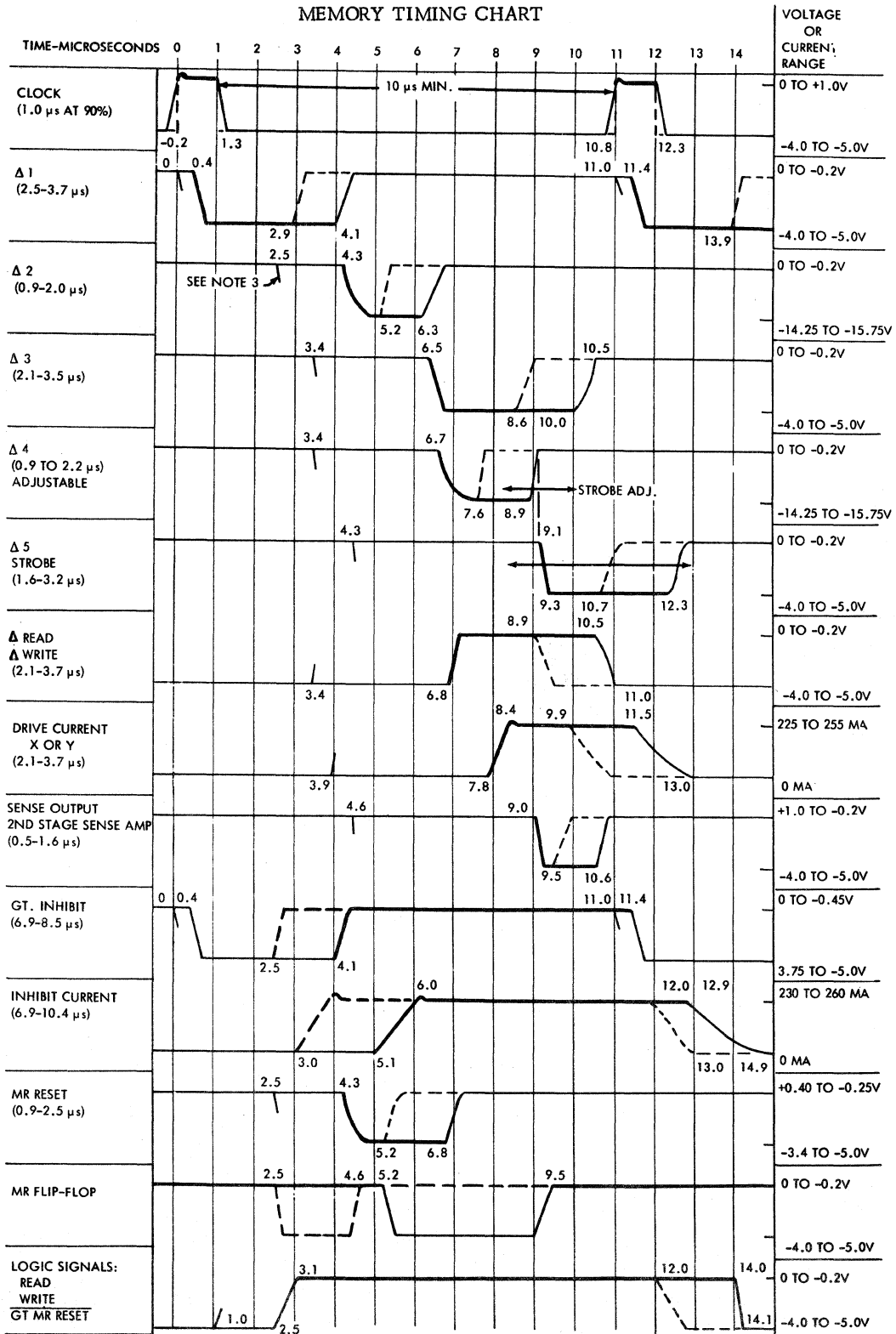
(Continued)

FLIP-FLOPS (Continued)

| | | |
|----------------------------------|--|---|
| RSFF | Rack-Stop | The Rack-Stop flip-flops control the release of the rack-stop clappers for columns one thru 12, DDU, DDT, CHAR and SYM. |
| SCFF | Special Control | The Special Control flip-flop is used for various control purposes. |
| SFF | SIGN | Sign flip-flop indicates the sign of A or B, plus or minus, during C arithmetic. SFF is also used as a control flip-flop on other operations. |
| SOFF thru S9FF | Sequence zero thru sequence 9 | The Sequence flip-flops control the logic progression during each T time. |
| SUM → MEMFF | SUM to MEM | The Sum to Memory flip-flop indicates that the adder output is to be written into the Memory. |
| SYMFF | SYMBOL | The Symbol flip-flop controls the release of the Rack Stop clapper for the symbol column. |
| TOFF thru T7FF | TIME | The Time flip-flop control the various operations of the Arithmetic and Memory Unit. TO - Shift or shift and Round. T1 - Transfer T2 - Print T3 - A arithmetic T4 - B arithmetic T5 - C arithmetic T6 - Clear T7 - Multiply or Divide |
| WR1FF WR2FF WR4FF WR8FF | WORKING REGISTER 1, 2, 4 & 8 bit. | The Working Register flip-flops provide a temporary storage location for data as an operation progresses. WR is always an input to the adder. |

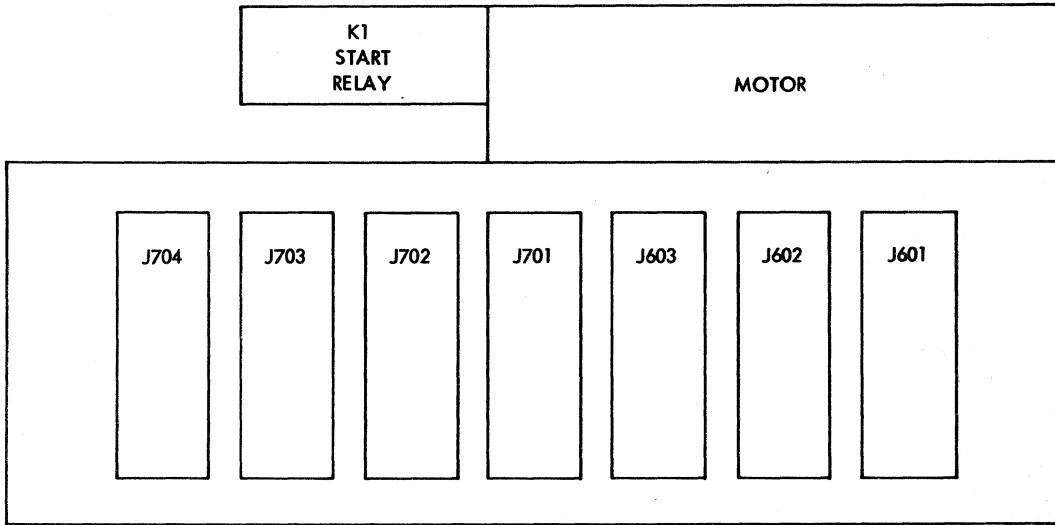
POWER ON - POWER OFF SEQUENCE



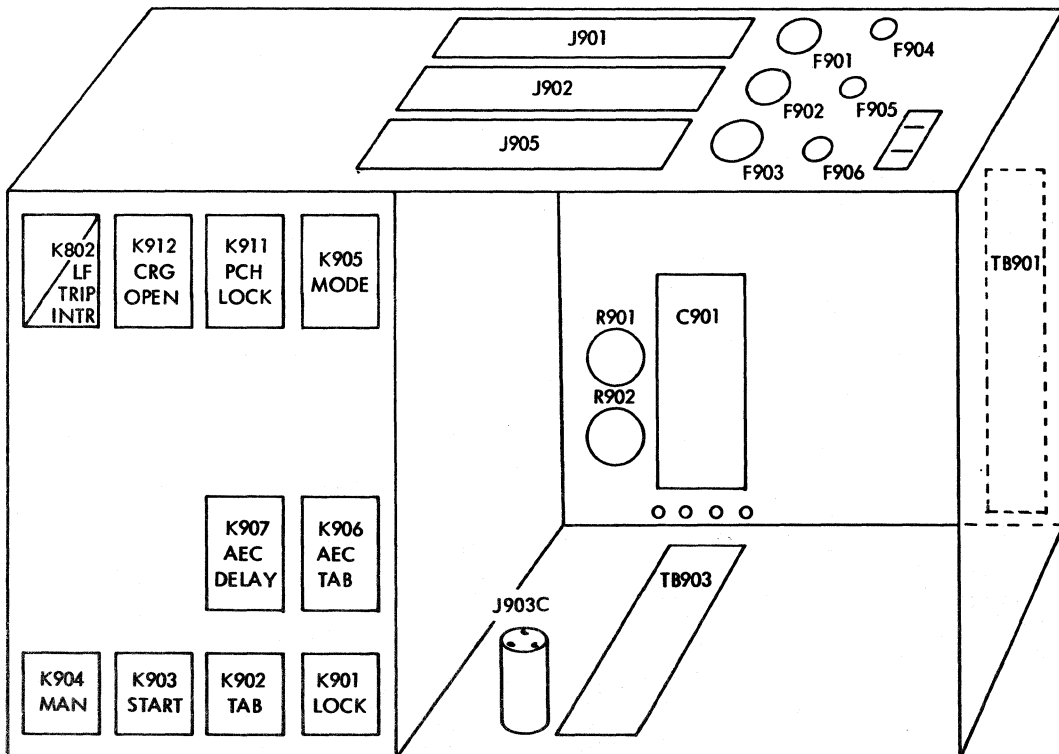


- NOTES:
1. TIME MEASUREMENTS REFER TO 10% AND 90% POINTS OF WAVEFORMS.
 2. PULSE DURATION AND DELAY ARE DRAWN AT MAXIMUM. RISE AND FALL TIMES ARE NOMINAL.
 3. NOTCH INDICATES EARLIEST TIME OF PULSE OCCURRENCE.

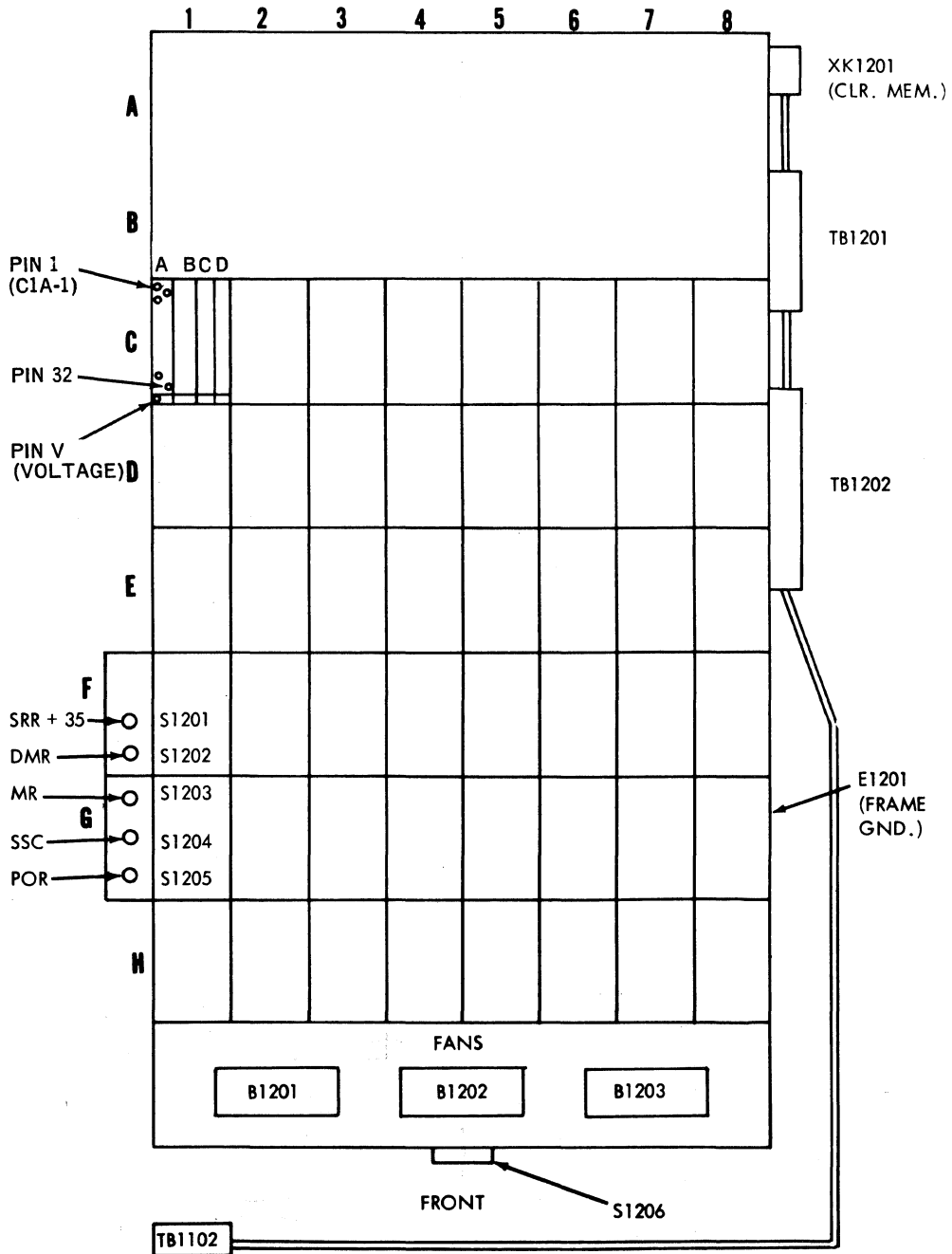
REAR VIEW - PRINTER CONNECTORS



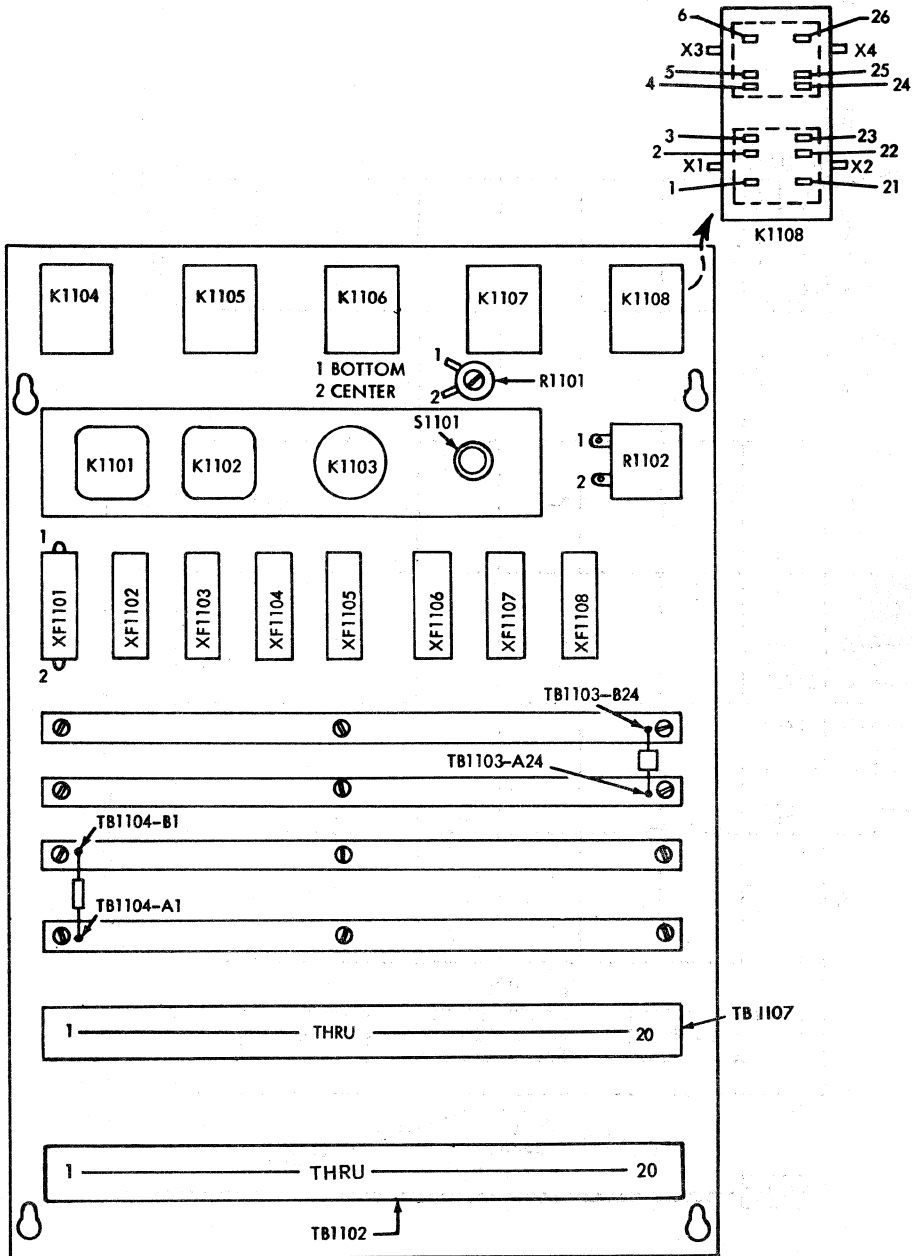
PRINTER - POWER SUPPLY



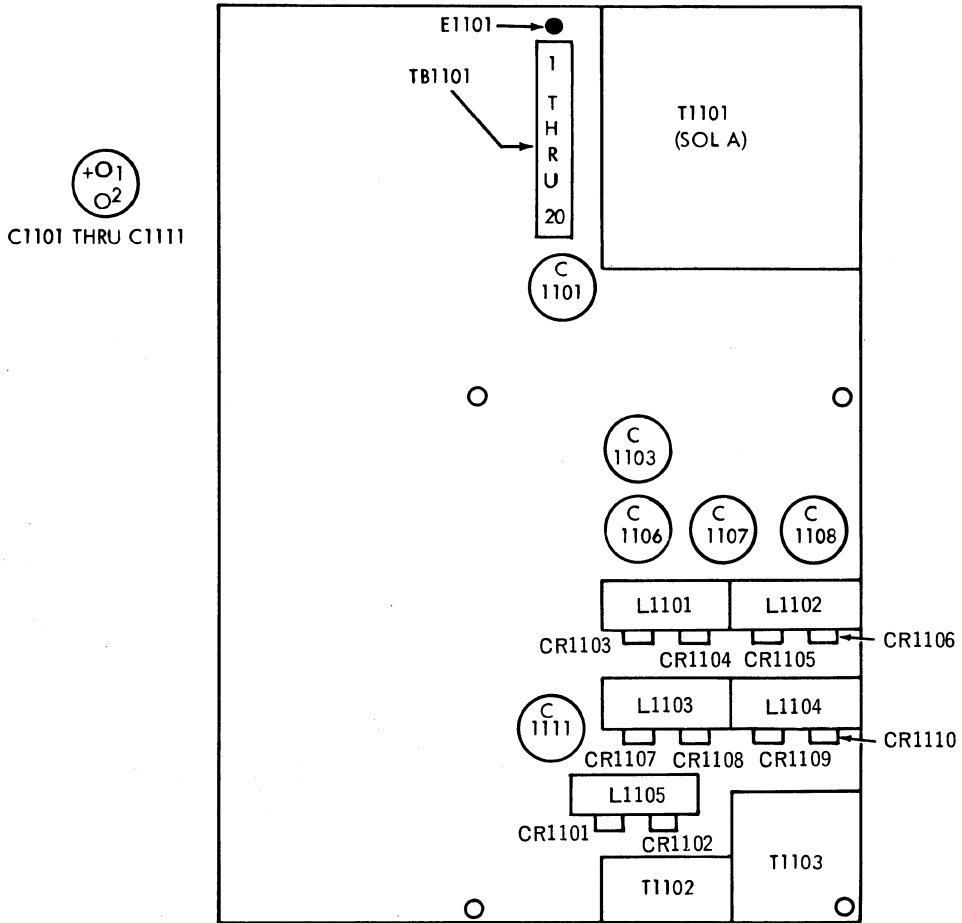
BOTTOM VIEW OF ARITHMETIC AND MEMORY UNIT GATE WHEN TILTED



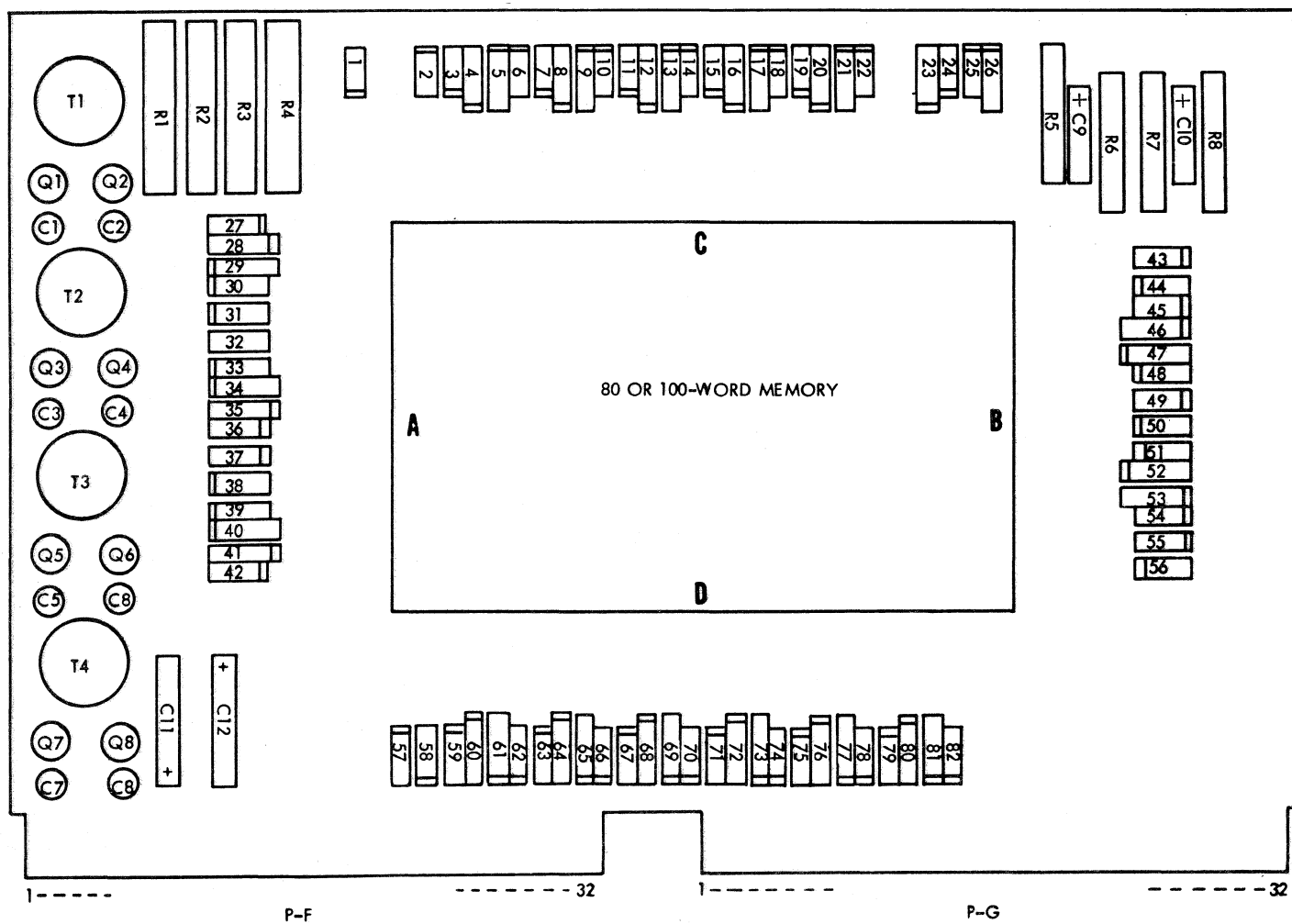
ARITHMETIC & MEMORY UNIT POWER SUPPLY COMPONENTS AND RELAYS



ARITHMETIC & MEMORY UNIT POWER SUPPLY
TRANSFORMERS, CHOKES & CAPACITORS

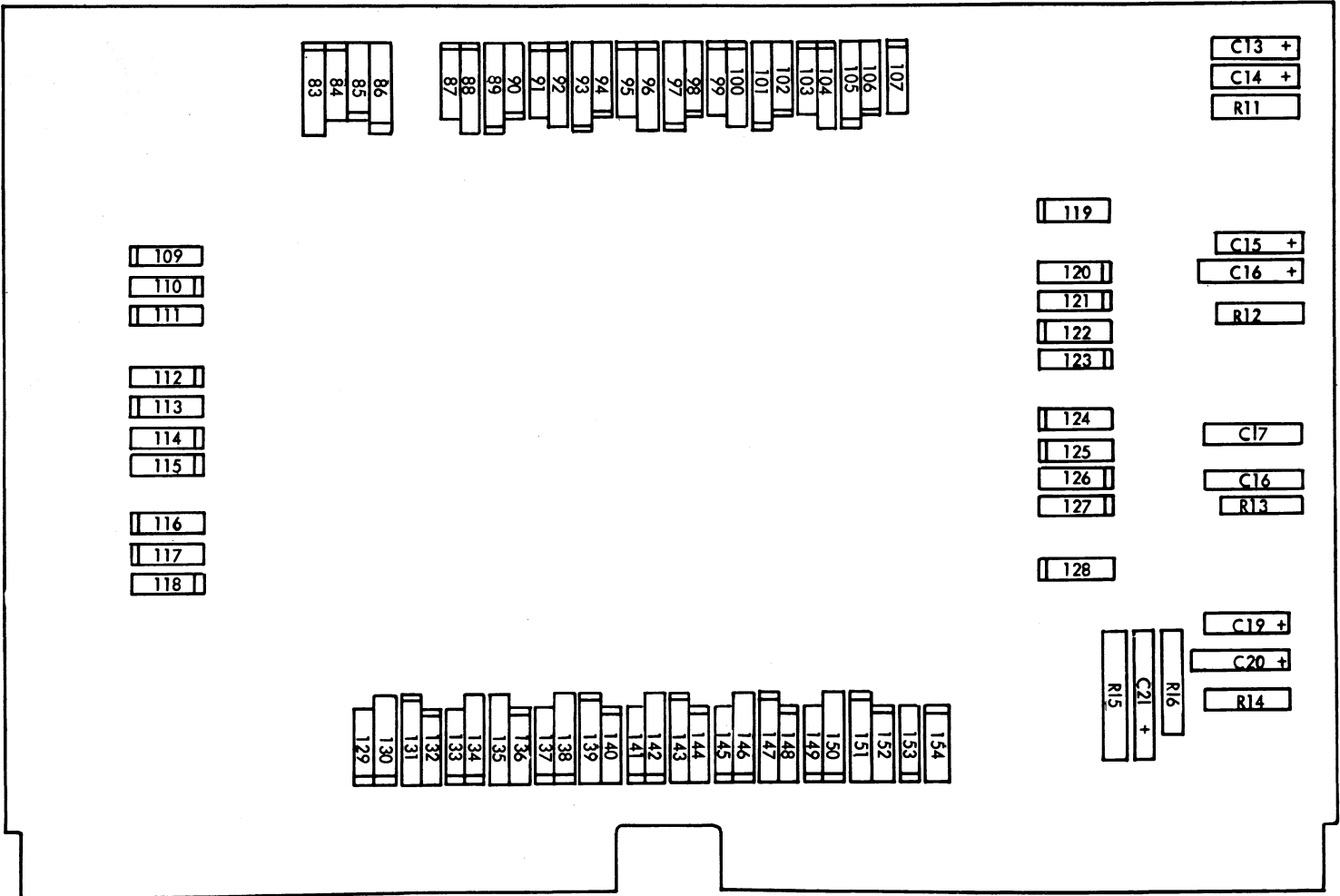


80 & 100 - WORD MEMORY (TOP VIEW)

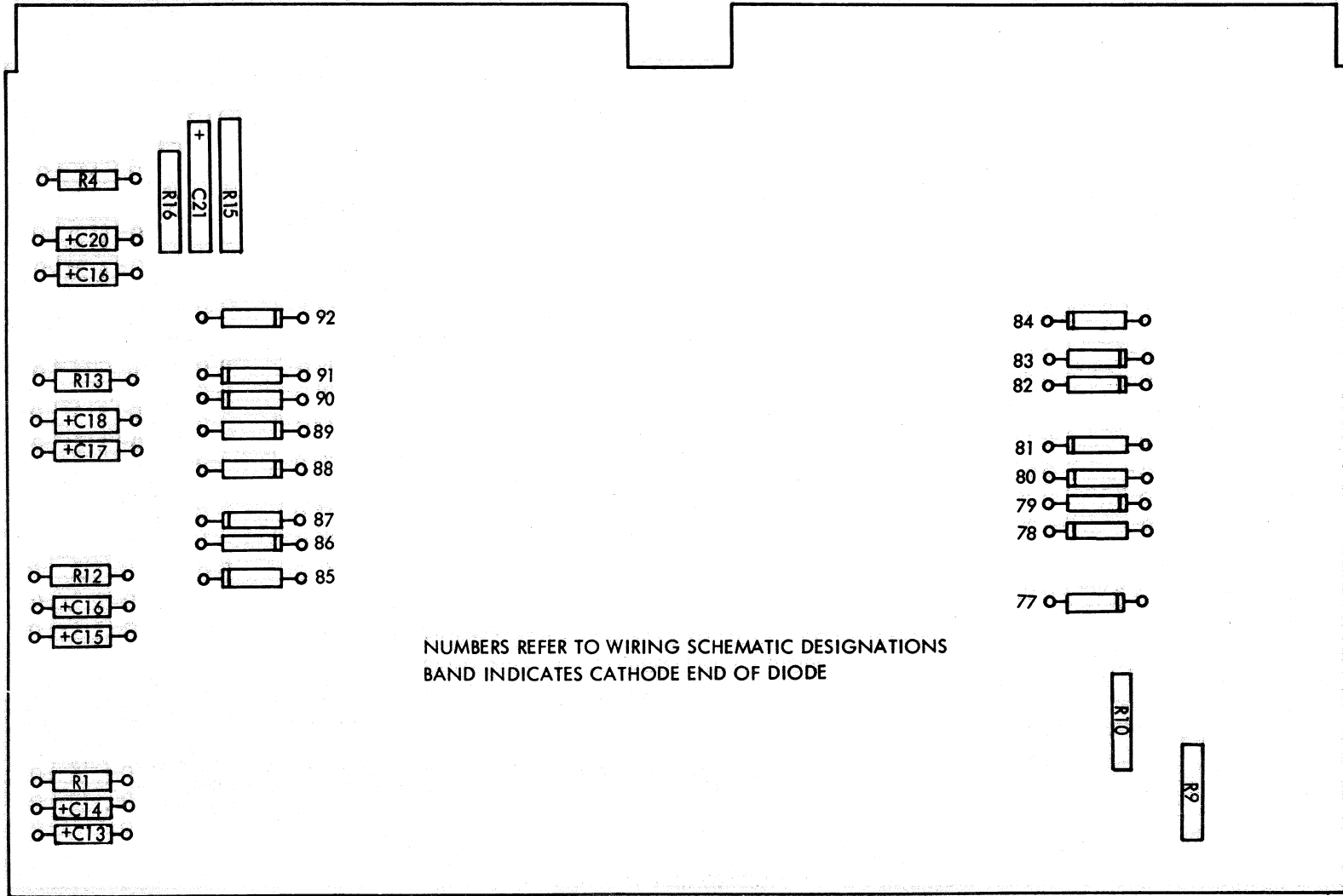


NUMBERS REFER TO WIRING SCHEMATIC DESIGNATIONS - BAND INDICATES CATHODE END OF DIODE

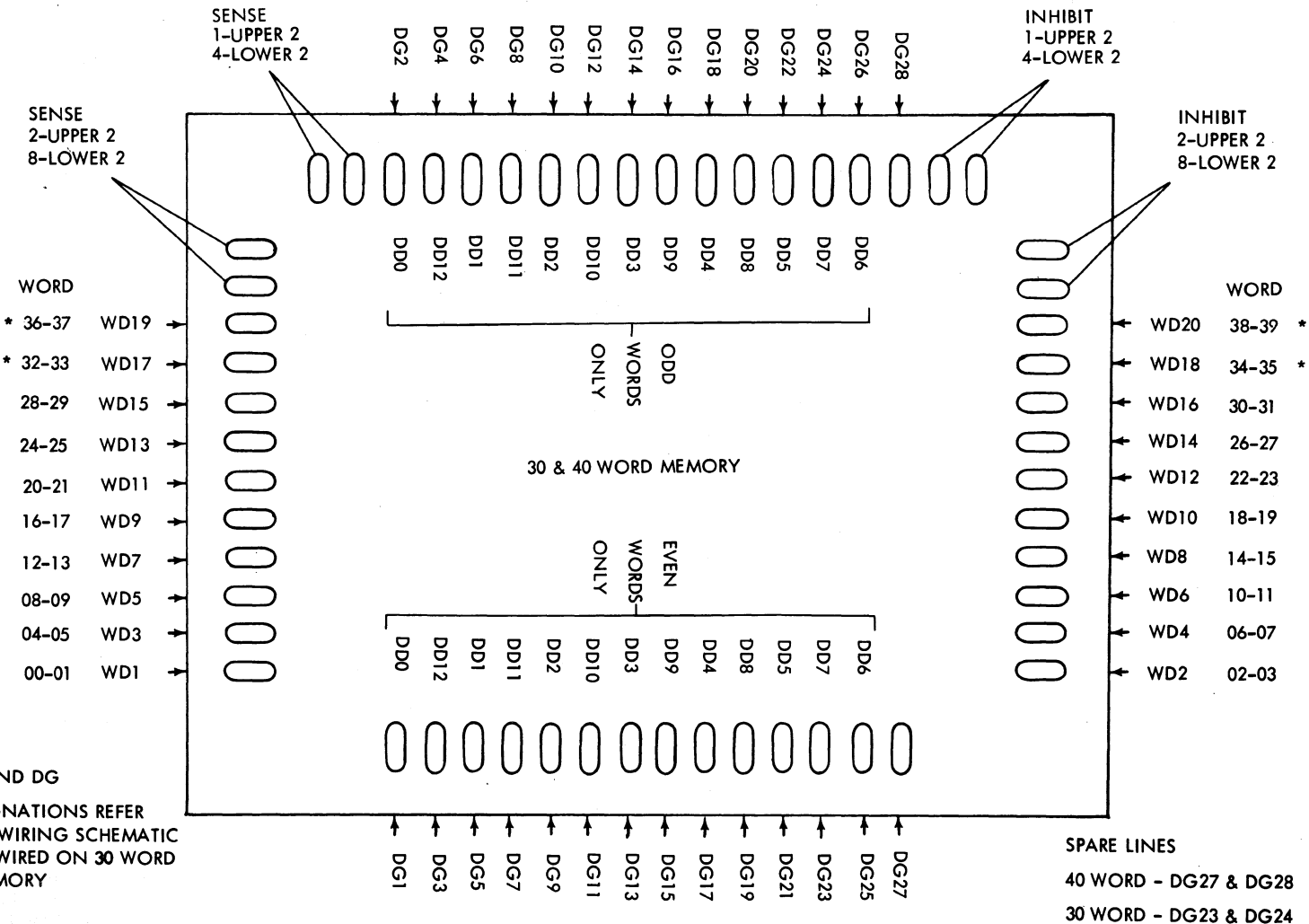
80 & 100 - WORD MEMORY (BOTTOM VIEW)



30 & 40 - WORD MEMORY (BOTTOM VIEW)



30 & 40 WORD MEMORY CORE ASSEMBLY



NOTES:

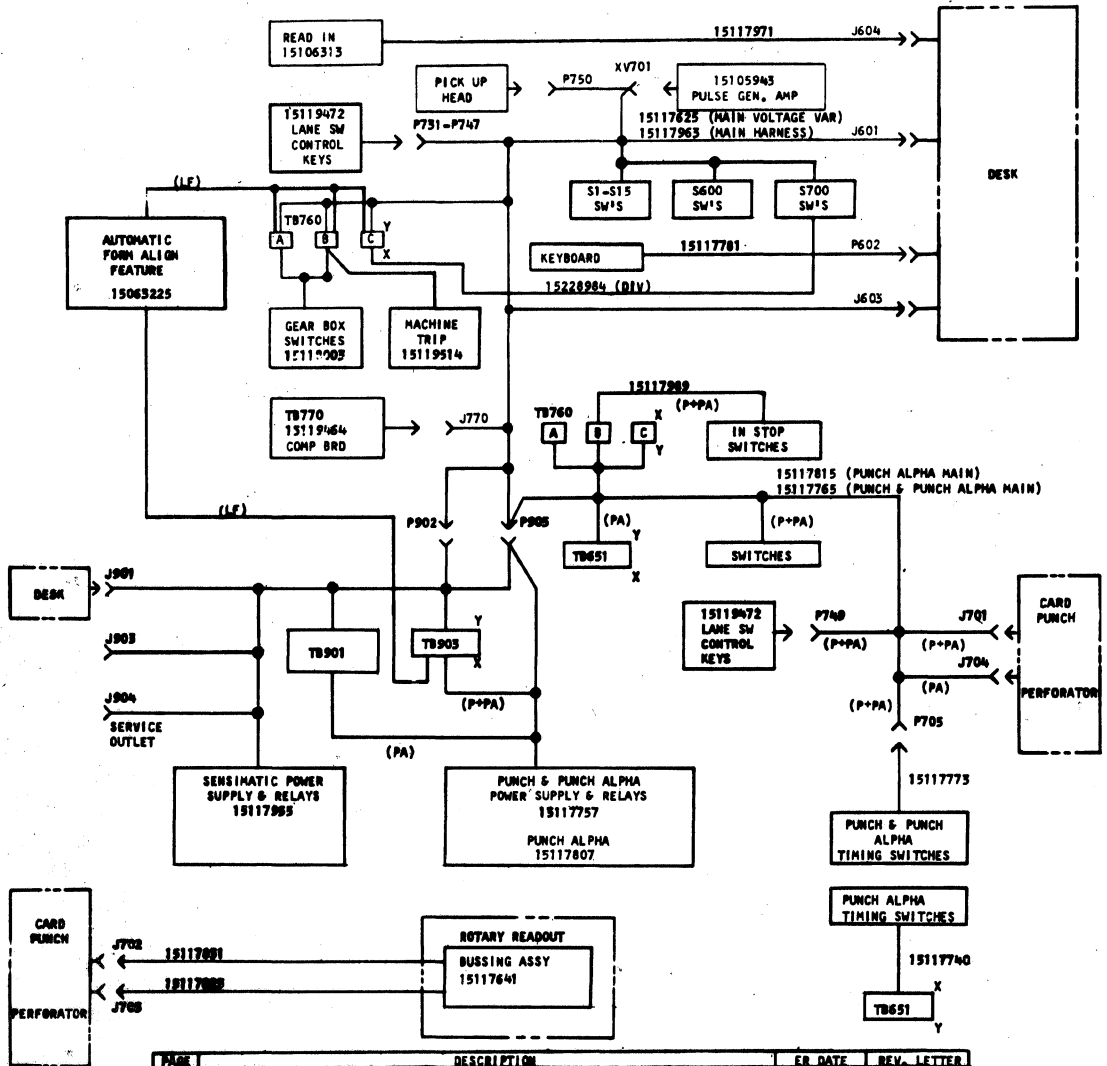
WD AND DG DESIGNATIONS REFER TO WIRING SCHEMATIC
 * NOT WIRED ON 30 WORD MEMORY

**SCHEMATIC DRAWINGS FOR CONTROL CONSOLE
AND PROCESSING ELECTRONICS**

The following Instruction Book pages include a set of typical schematic drawings covering the electronics pertaining to the E 2100 product.

These prints should be used only for logic and reference study of the electronic system.

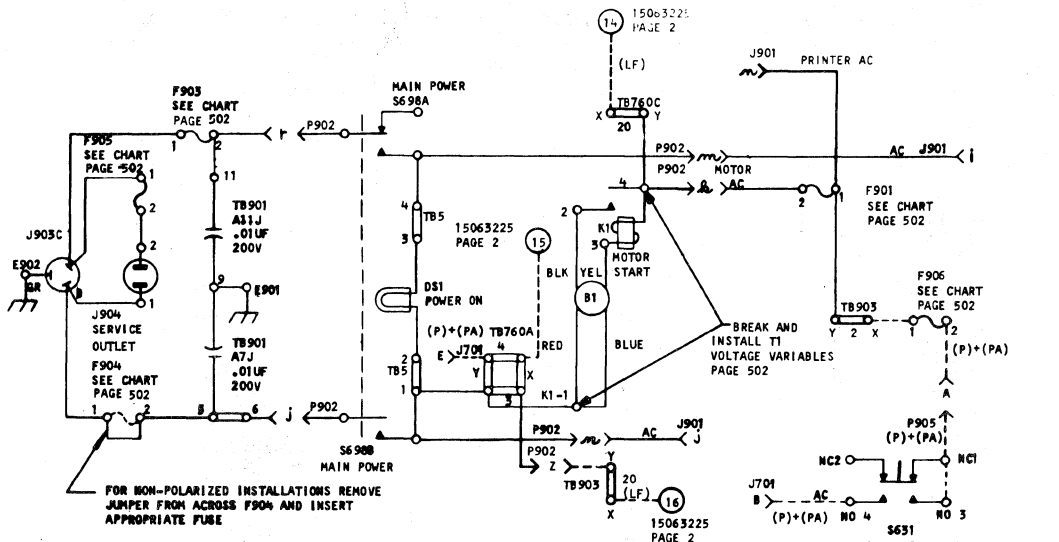
When servicing E 2100 systems, use the blue line schematic prints furnished with the particular system being serviced.



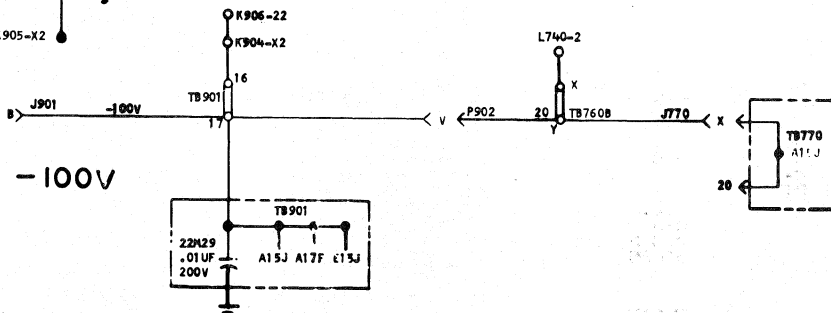
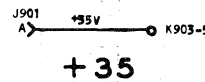
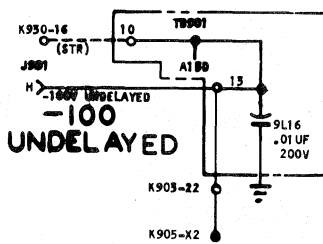
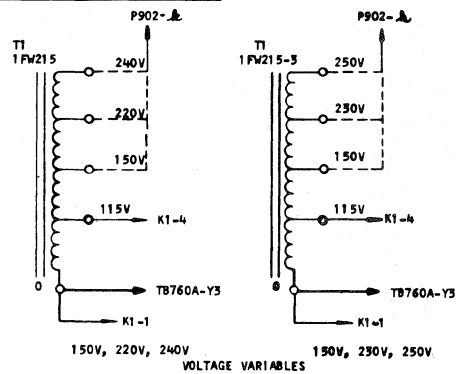
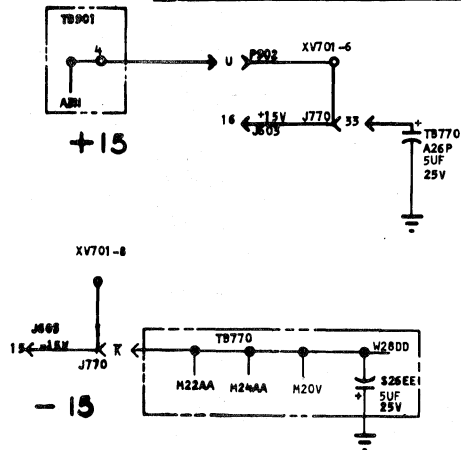
| PAGE | DESCRIPTION | ER DATE | REV. LETTER |
|------|---|---------|-------------|
| 901 | KEYBOARD PRINTER INDEX | 4-3-64 | C |
| 902 | AC INPUT & DC VOLTAGE ROUTING | 4-1-64 | B |
| 903 | +150 SUPPLY, GRD ROUTING & LANES 31-33 | 4-1-64 | B |
| 904 | LANE COMB, MANUAL KEYS, MANUAL RELAY, & LANES 34-36 | 4-1-64 | B |
| 909 | LANES 37-44 | 4-1-64 | B |
| 906 | LANES 45-48, RE KEY, LANE 3, RED RIBBON, & RACK STOP COILS | 4-1-64 | B |
| 907 | LANES 51-55, 57, 59, 61, 63, 66 & DECIMAL LIGHTS | 4-3-64 | C |
| 908 | TC4, TCS, SRR, ALL TOTAL, PG AMP, LANE 65, CLR MEM KEY, TC9 | 4-1-64 | B |
| 909 | SENSINATIC AND TYPEWRITER CONTROLS | 4-1-64 | B |
| 910 | AEC AND TYPEWRITER CONTROLS, STR INTLK, MAGNETIC CLUTCH | 4-1-64 | B |
| 911 | MEMORY ADDRESS, CHAR, & KEYBOARD SWITCHES, MODE RELAY, AEC TAB M5 & PRINT | 4-1-64 | B |
| 912 | PUNCH ALPHA FEATURE WIRING | 4-1-64 | B |
| 913 | PUNCH AND PUNCH ALPHA FEATURE WIRING | 4-1-64 | B |
| 914 | COMPONENT LISTING | 4-3-64 | C |
| 915 | RELAY CONFIGURATION & SIGNAL ROUTING | 4-1-64 | B |
| 916 | KEYBOARD CONSTRUCTION FOR STANDARD & STERLING | 4-1-64 | B |

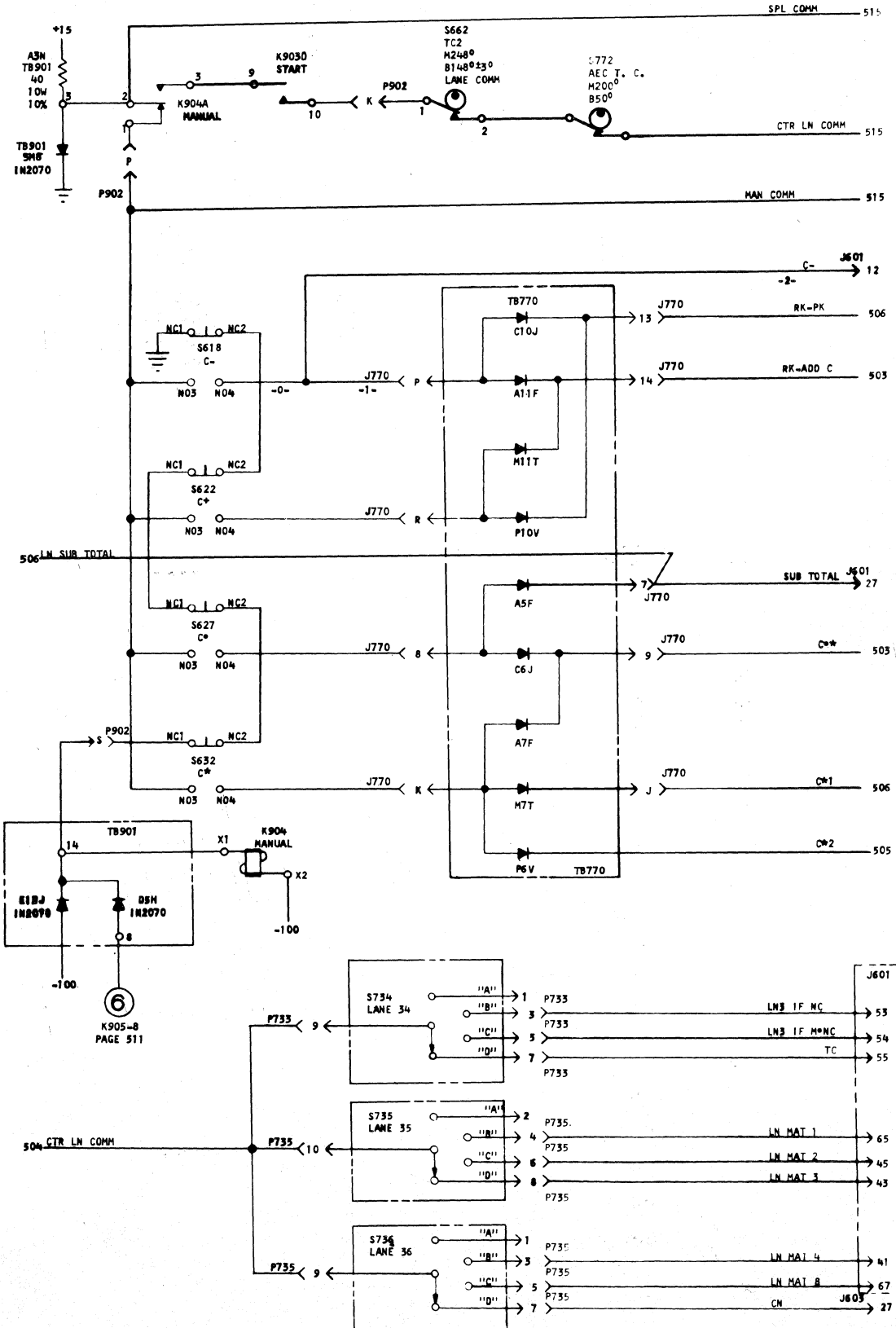
- NOTES:
1. WIRING SHOWN IN DASHED LINES INDICATES FEATURES (-----)
 - A. PUNCH ALPHA FTE. WIRING INDICATED BY (PA)
 - B. PUNCH & PUNCH ALPHA FTE. WIRING INDICATED BY (P+PA)
 - C. STERLING FTE WIRING INDICATED BY (STR)
 - D. AUTOMATIC FORM ALIGN FTE WIRING INDICATED BY (LF)
 - E. DIVIDE FTE WIRING INDICATED BY (DIV)
 2. DESK WIRING SHOWN IN PHANTOM LINES FOR REF PURPOSE ONLY (-----)
 3. * INDICATES SOURCE OF SIGNAL.
 4. PAGE NUMBERS ON INPUT SIGNALS INDICATE PAGE OF ORIGIN
 5. WHEN PAGE NUMBER DOES NOT APPEAR ON INPUT OR OUTPUT REFER TO CONNECTOR INDEX CHART ON APPLICABLE SCHEMATIC TO DETERMINE WHERE SIGNALS ENTER OR LEAVE.

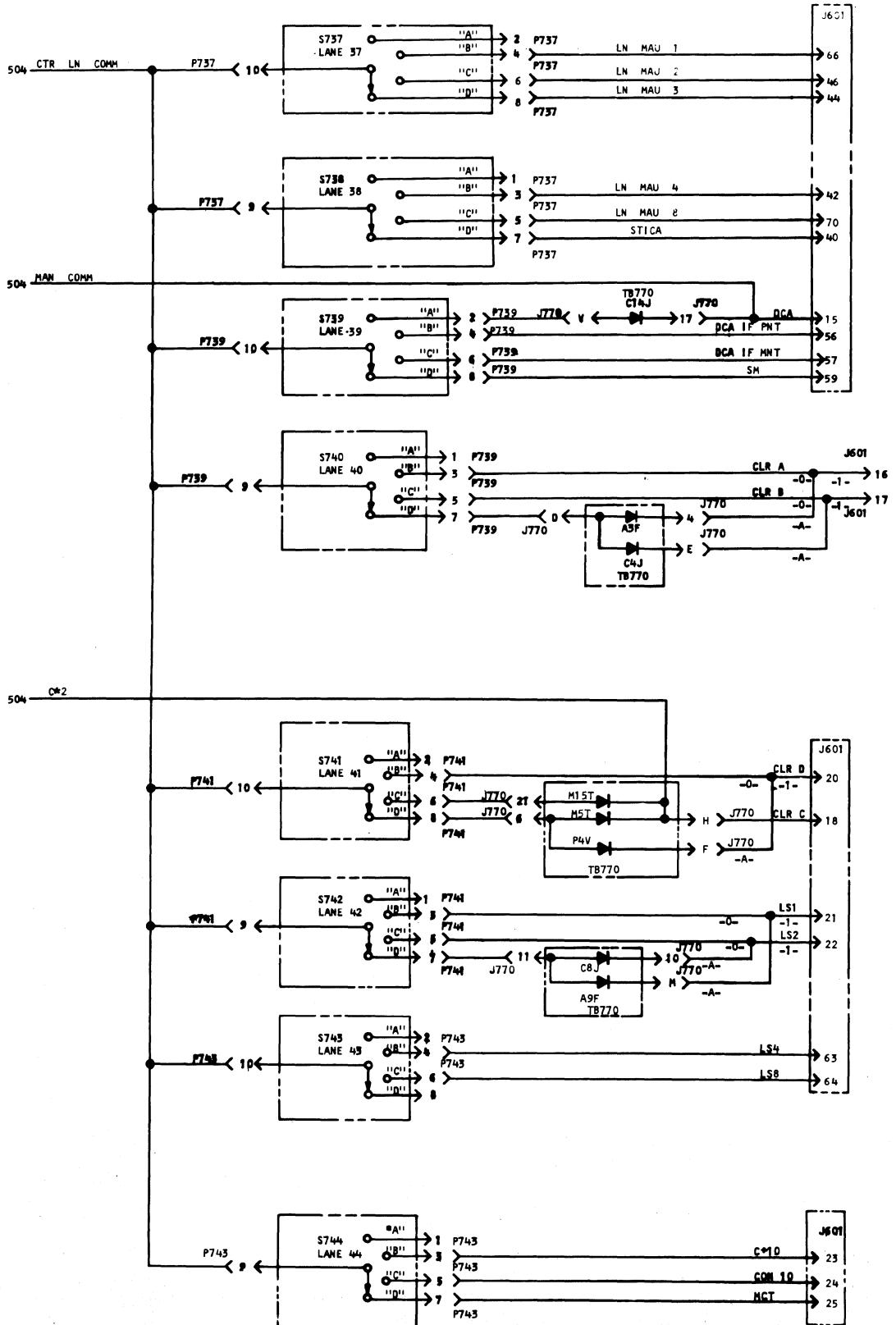
UNLESS OTHERWISE SPECIFIED:
 ALL DIODES ARE IN270
 ALL RESISTANCES ARE 1/4 WATT



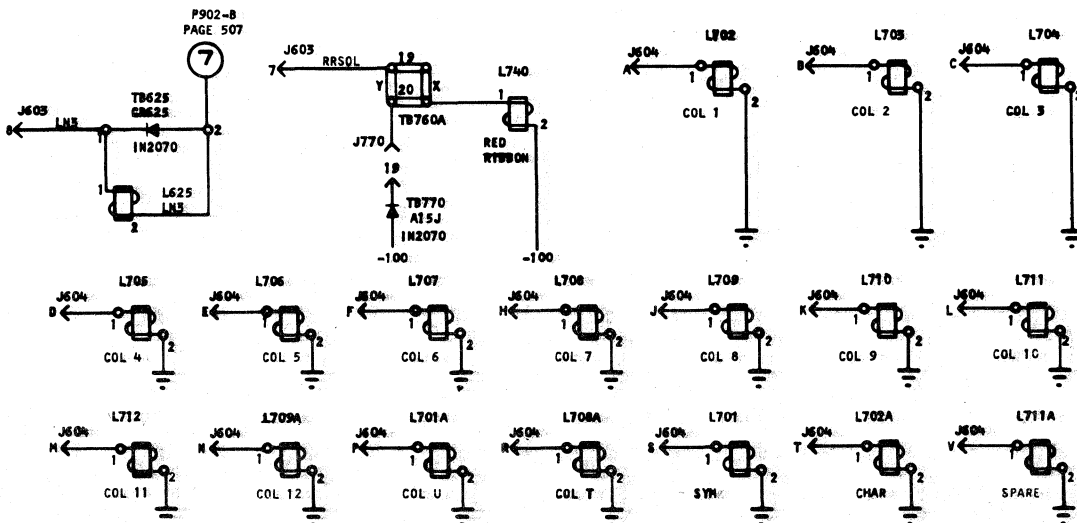
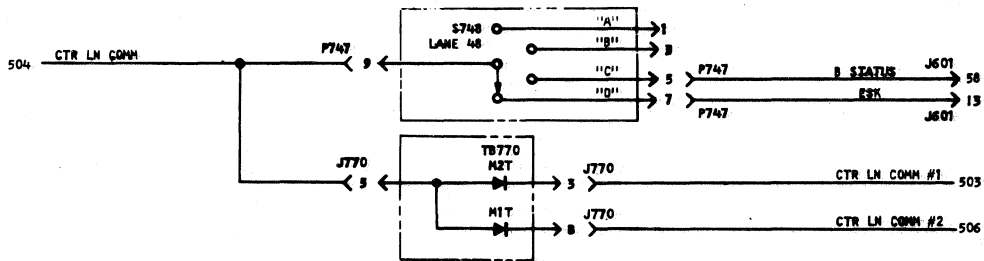
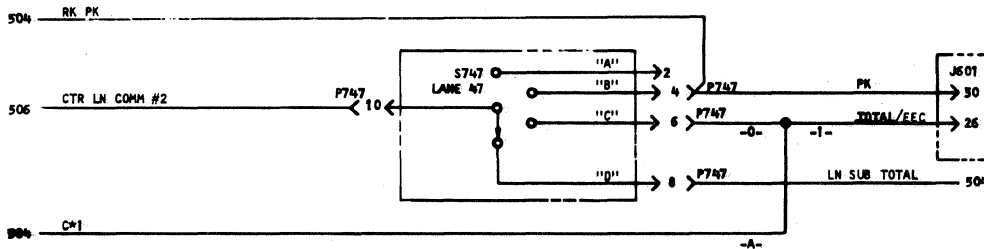
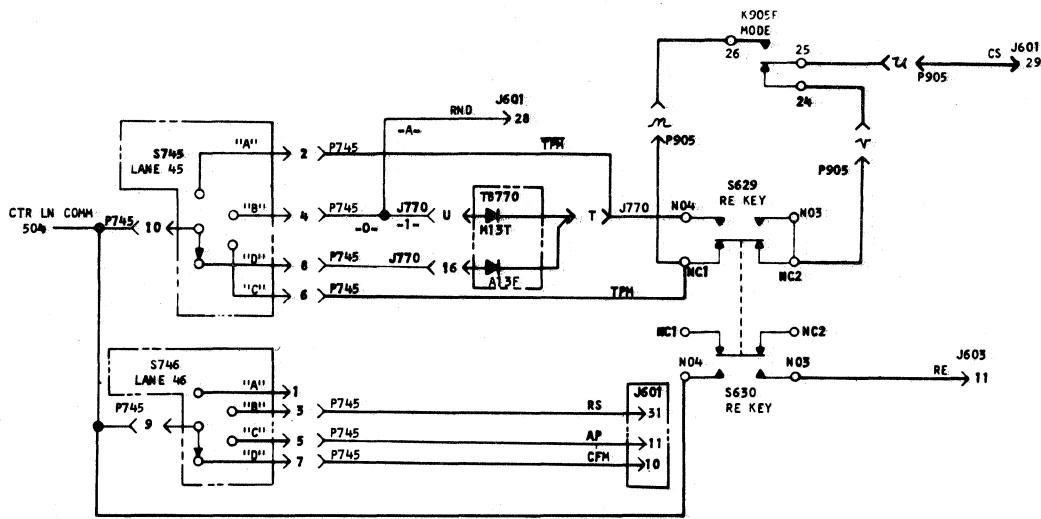
| LINE VOLTAGE | F901 | F903 | F904 | F905 | F906 | DS1 |
|--------------|------------|----------------|----------------|------------|---------------|---------|
| 120 | 3, 2A 125V | 6, 25A SB 250V | 6, 25A SB 250V | 7A SB 125V | 1, 5A SB 125V | 1FX417 |
| 150 | 2A 250V | 4A SB 250V | 4A SB 250V | 2A 250V | 2, 5A SB 250V | 1FX48-4 |
| 220 - 250 | 2A 250V | 3, 2A SB 250V | 3, 2A SB 250V | 2A 250V | 2, 5A SB 250V | 1FX48-4 |

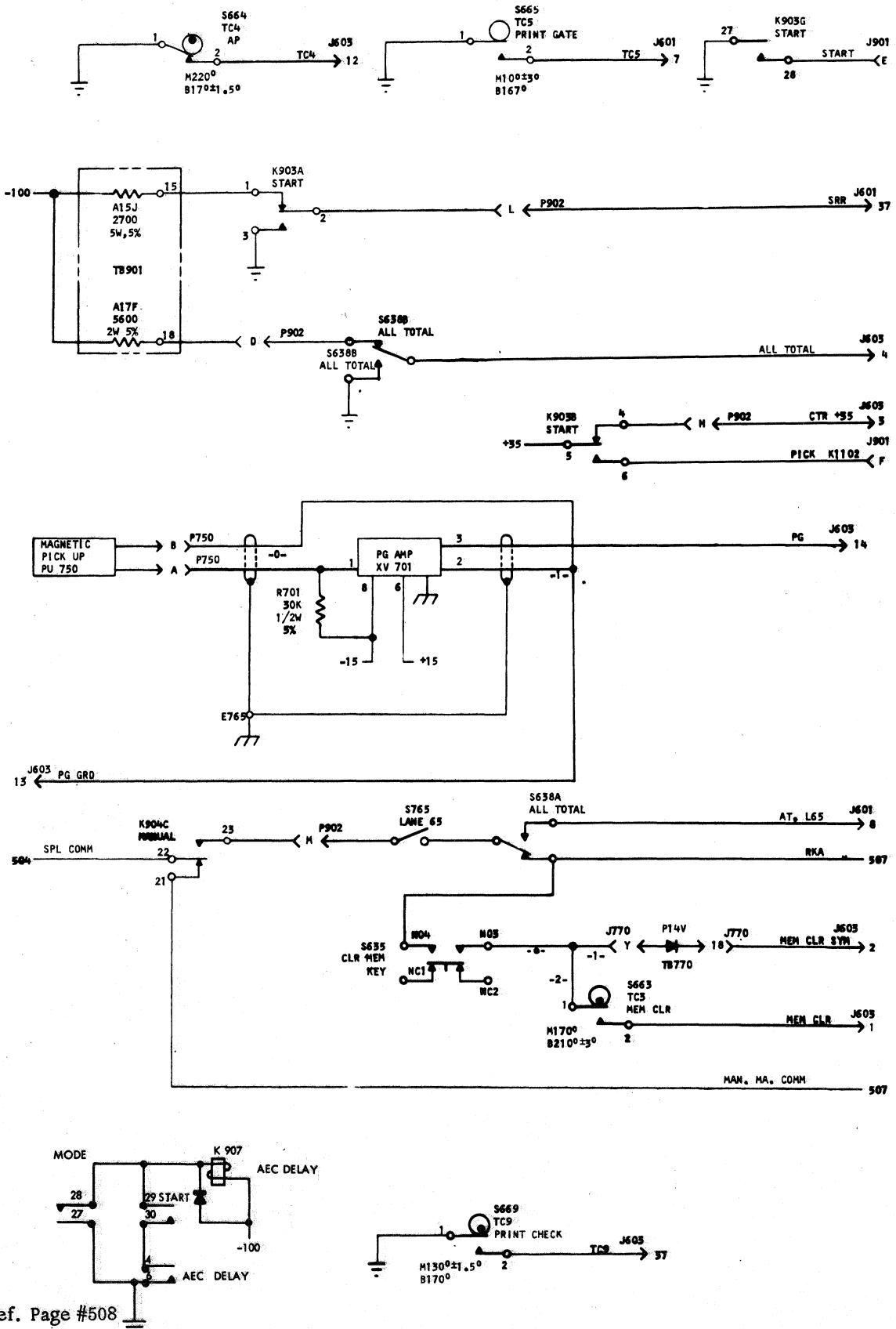


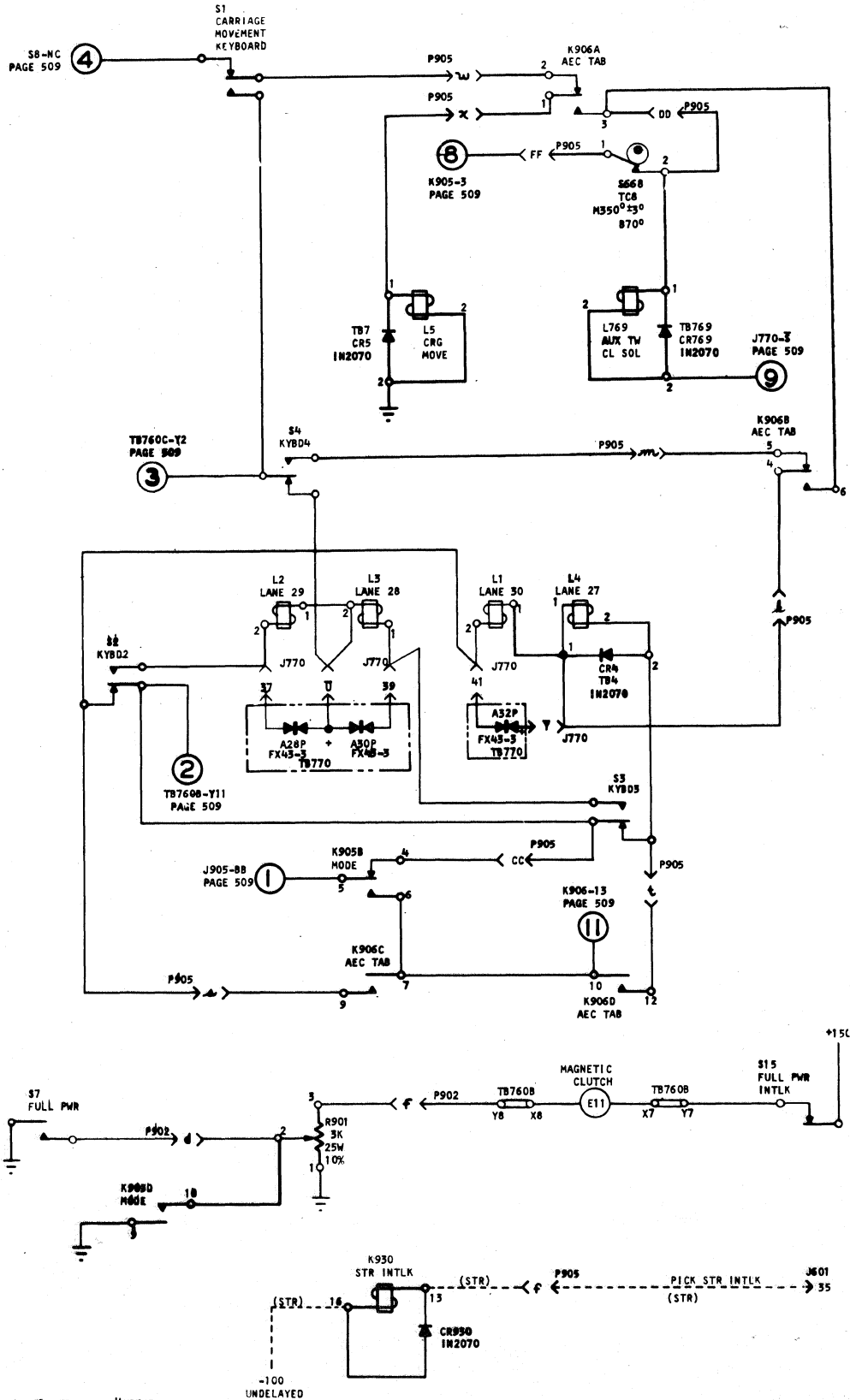


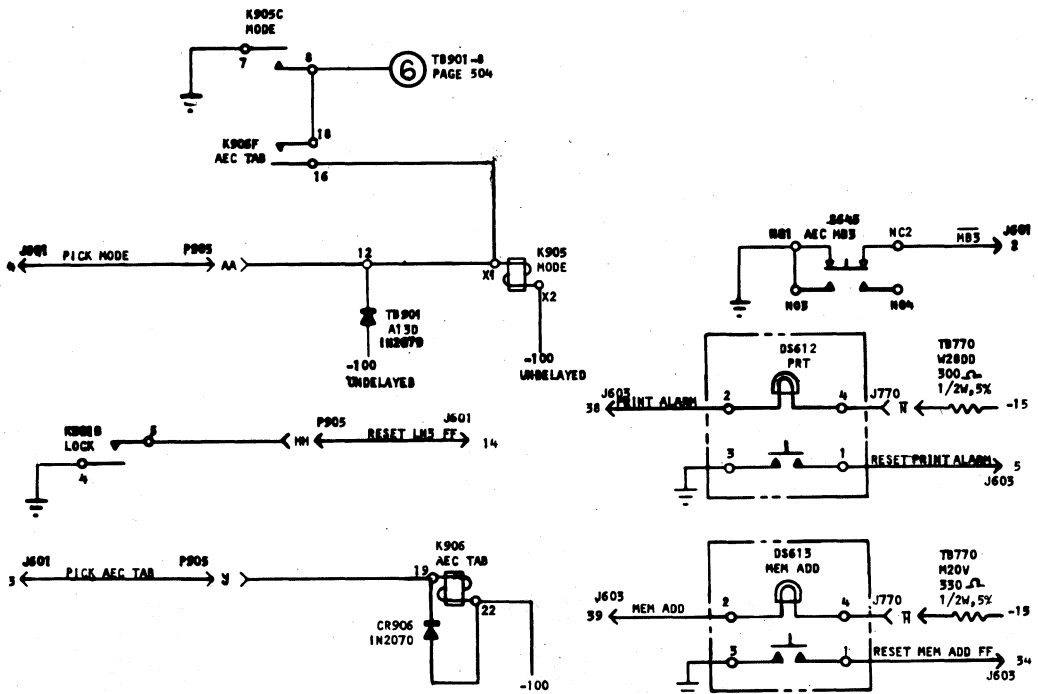
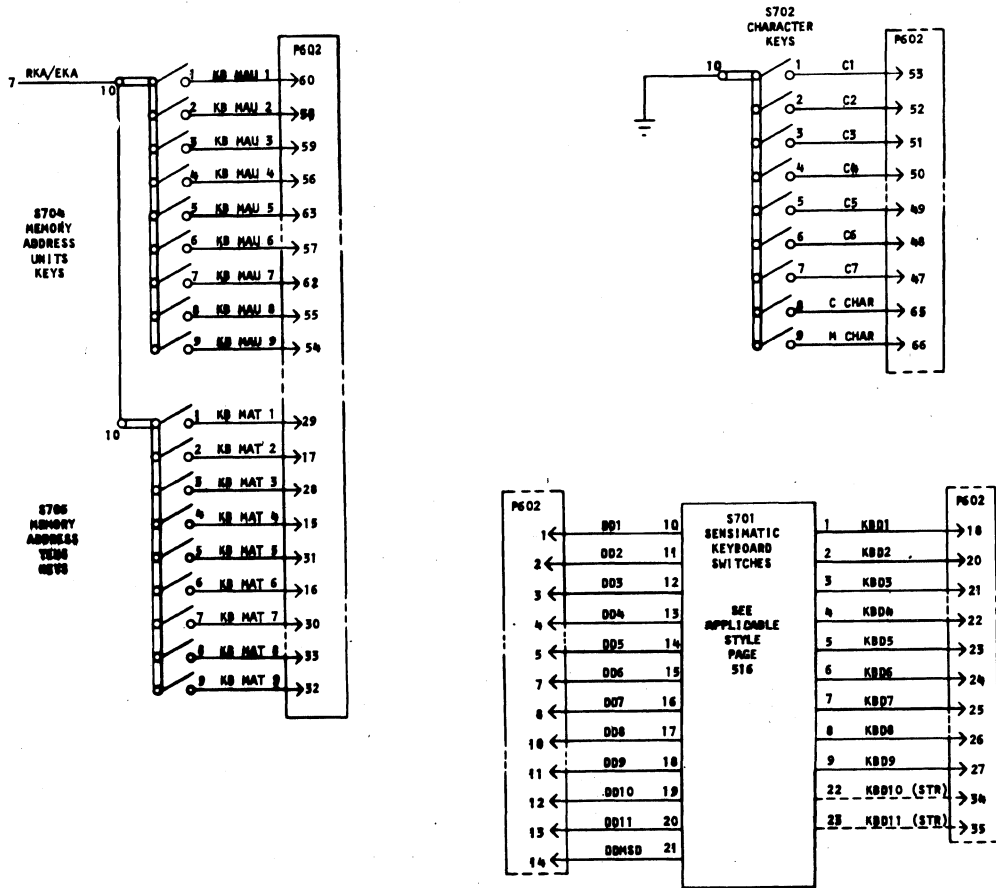


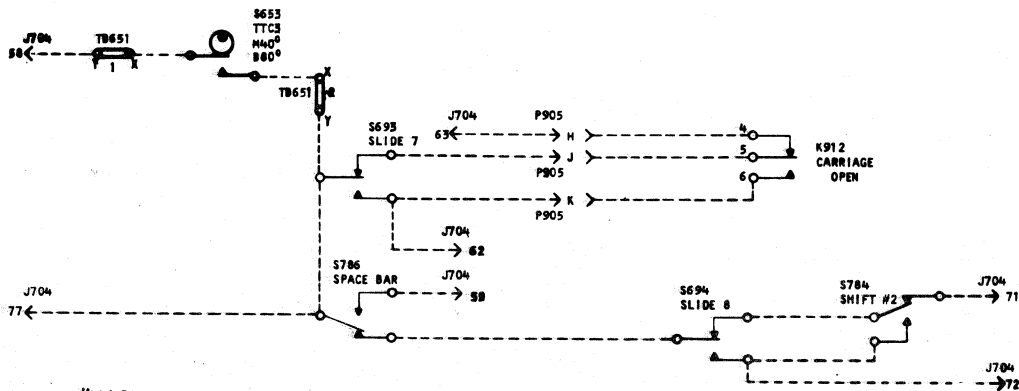
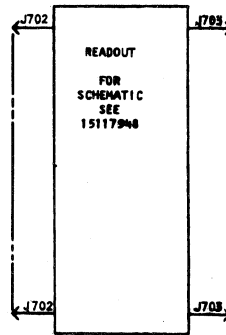
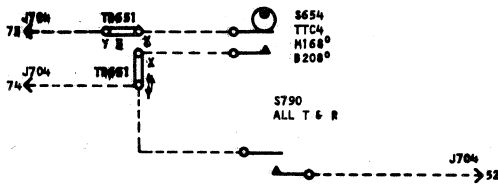
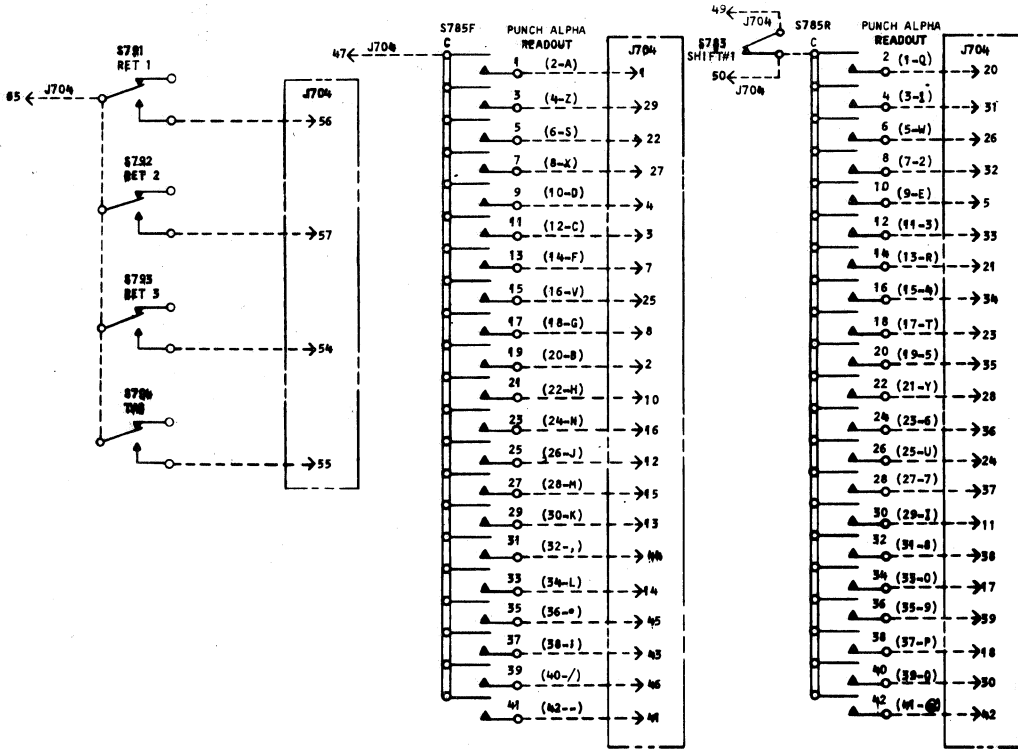
Ref. Page #505

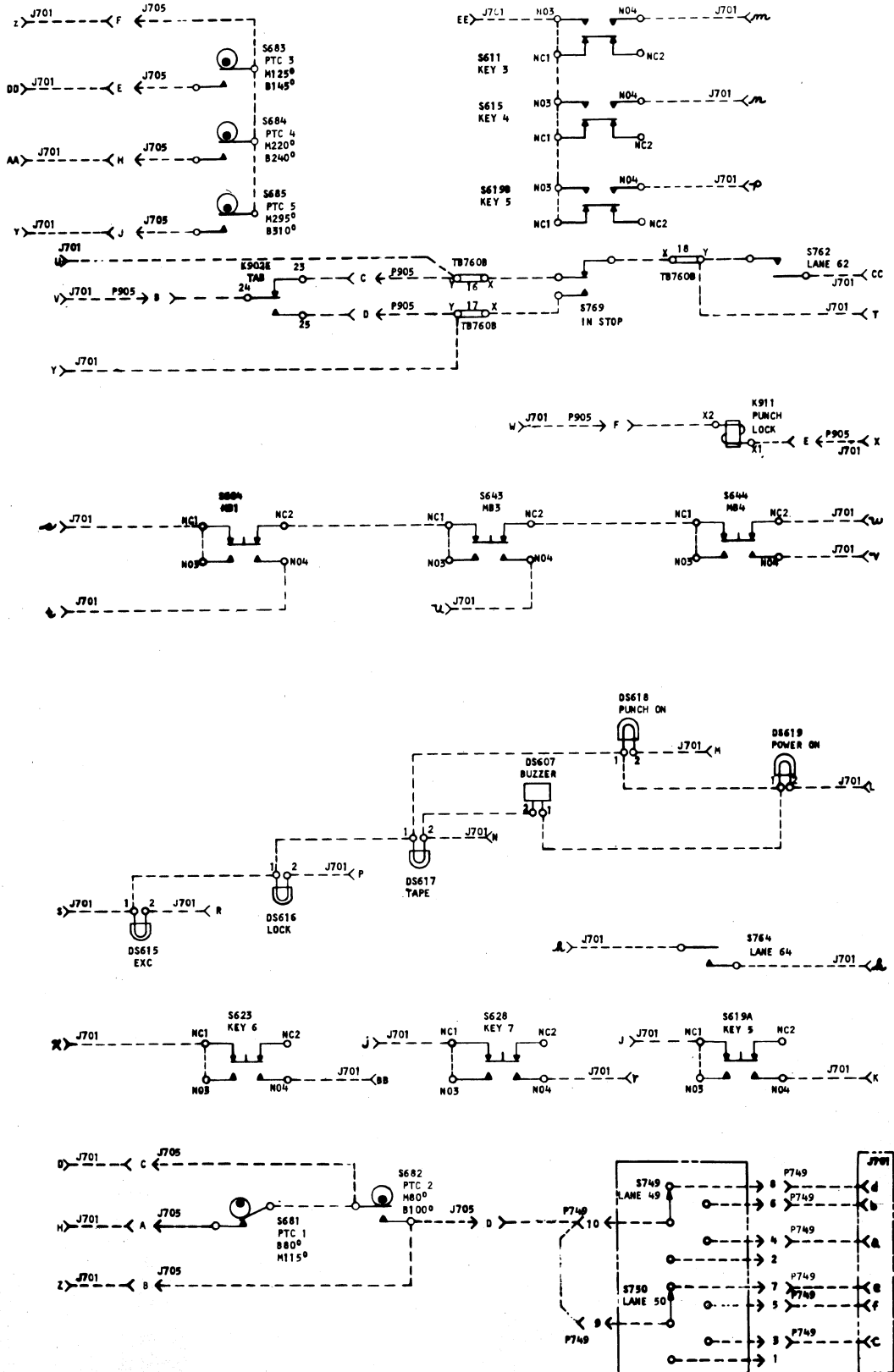




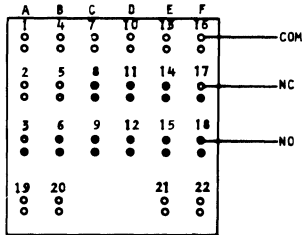
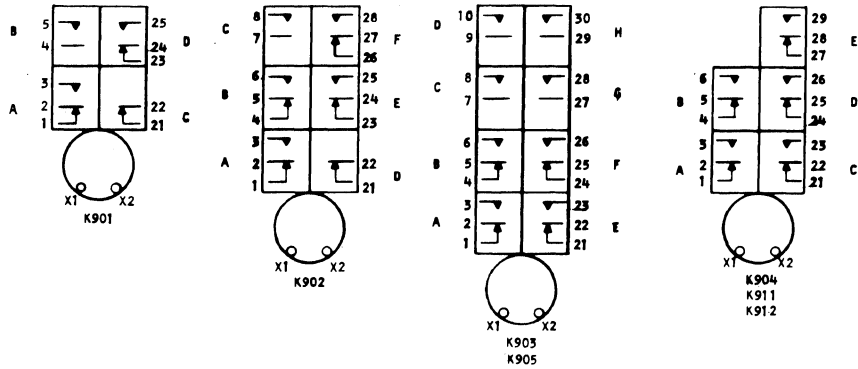




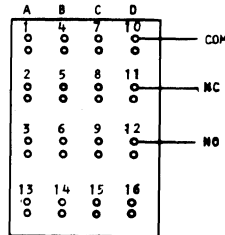




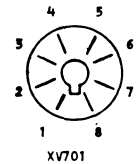
Ref. Page #513



K906



K990
K907



XV701

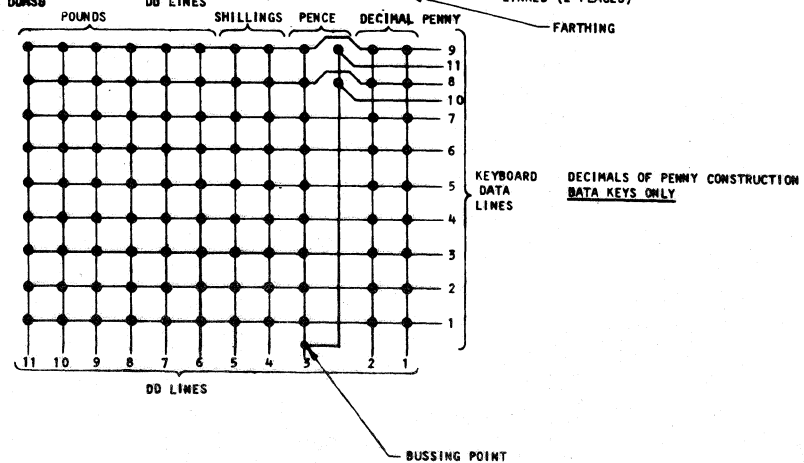
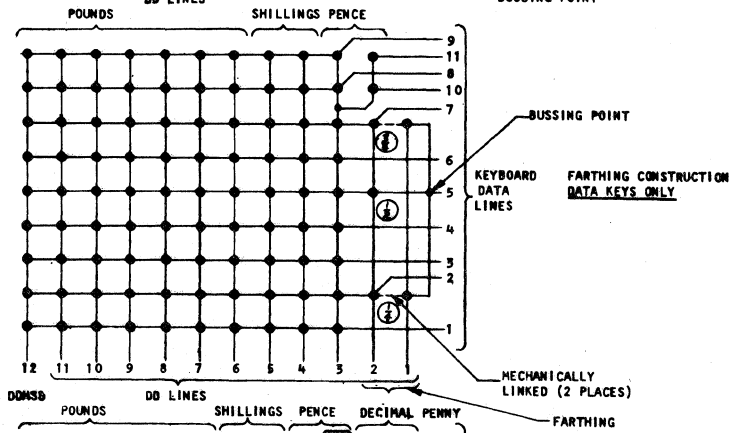
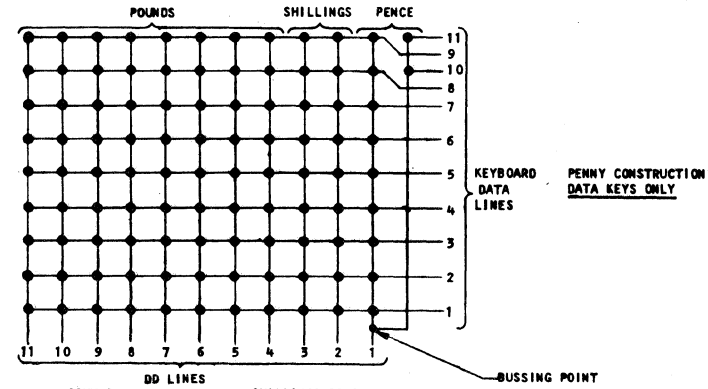
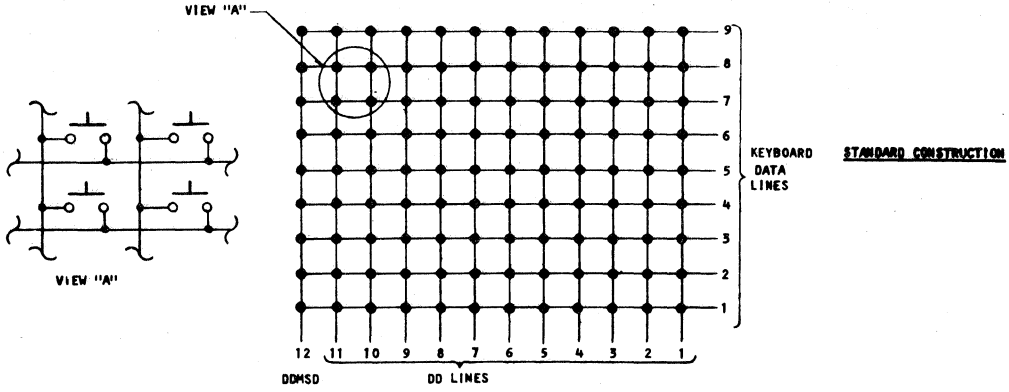
| RELAYS | NAME | PAGE | | | | | | | | | | | |
|---------------|----------------|------|-----|-----|-----|-----|-----|-----|---|---|-----|-----|--|
| | | COIL | A | B | C | D | E | F | G | H | | | |
| K901 | MOTOR START | 502 | | | | | | | | | | | |
| K901 | LOCK | 507 | 509 | 511 | 509 | | | | | | | | |
| K902 | TAB | 509 | 509 | 507 | 509 | 507 | 513 | | | | | | |
| K903 | START | 509 | 508 | 508 | 509 | 504 | 507 | | | | 508 | 508 | |
| K904 | MANUAL | 504 | 504 | 507 | 508 | 507 | | | | | 508 | | |
| K905 (AEC) | MODE | 511 | 509 | 510 | 511 | 510 | 509 | 506 | | | | | |
| K907 (AEC) | AEC DELAY | 508 | 509 | 508 | | | | | | | | | |
| K906 (AEC) | AEC TAB | 511 | 510 | 510 | 510 | 510 | 509 | 511 | | | | | |
| K911 (P)+(PA) | PUNCH LOCK | 513 | 507 | 509 | | | | | | | | | |
| K912 (PA) | CARRIAGE OPEN | 509 | 509 | 512 | | | | | | | | | |
| K950 (STR) | STERLING INTLK | 510 | 509 | | | | | | | | | | |

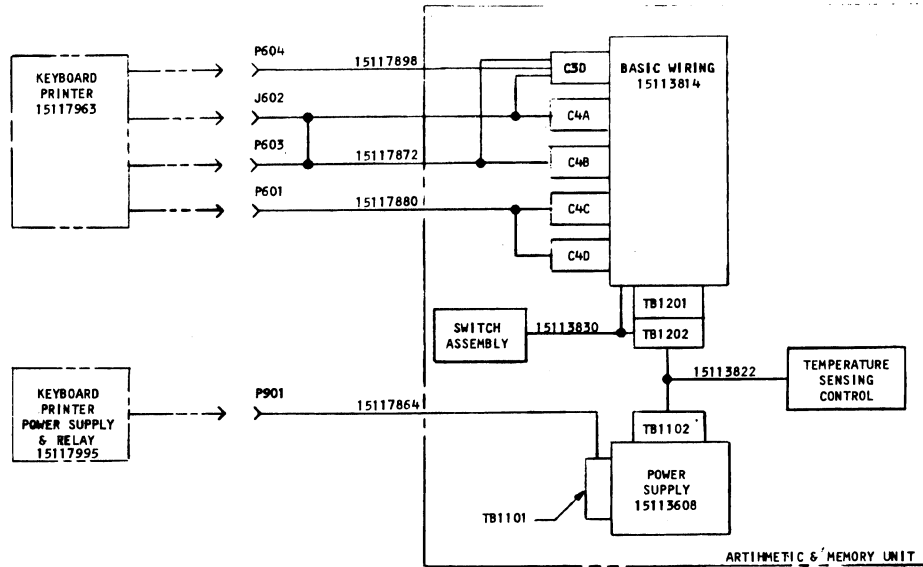
| CTR LN COMM | PAGE |
|-------------|------|
| *S772-N0 | 504 |
| P731-10 | 503 |
| P731-9 | 503 |
| P733-9 | 504 |
| P735-10 | 504 |
| P735-9 | 504 |
| P737-10 | 505 |
| P737-9 | 505 |
| P739-10 | 505 |
| P739-9 | 505 |
| P741-10 | 505 |
| P741-9 | 505 |
| P743-10 | 505 |
| P743-9 | 505 |
| P745-10 | 506 |
| P745-9 | 506 |
| P747-9 | 506 |
| J770-5 | 506 |
| S630-N04 | 506 |

| SPL COMM | PAGE |
|----------|------|
| *T901-3 | 504 |
| K904-2 | 504 |
| K904-5 | 507 |
| K904-22 | 508 |

| COMPONENT | NAME | PAGE |
|-----------|-----------------------|------|
| DS1 | POWER ON | 502 |
| DS601 | DEC. LIGHT COL. 2 & 3 | 507 |
| DS602 | DEC. LIGHT COL. 5 & 6 | 507 |
| DS603 | DEC. LIGHT COL. 8 & 9 | 507 |
| DS607 | BUZZER (TAPE) | 513 |
| DS615 | EXC | 513 |
| DS616 | LOCK (TAPE) | 513 |
| DS617 | TAPE | 513 |
| DS618 | PUNCH ON | 513 |
| DS619 | POWER ON (TAPE) | 513 |
| DS612 | PRT | 511 |
| DS613 | MEM ADD | 511 |
| XV701 | PG AMP SOCKET | 508 |

| MAN COMM | PAGE |
|----------|------|
| *P902-P | 504 |
| S618-N03 | 504 |
| S622-N03 | 504 |
| S627-N03 | 504 |
| S632-N03 | 504 |
| J770-17 | 505 |
| J601-15 | 505 |





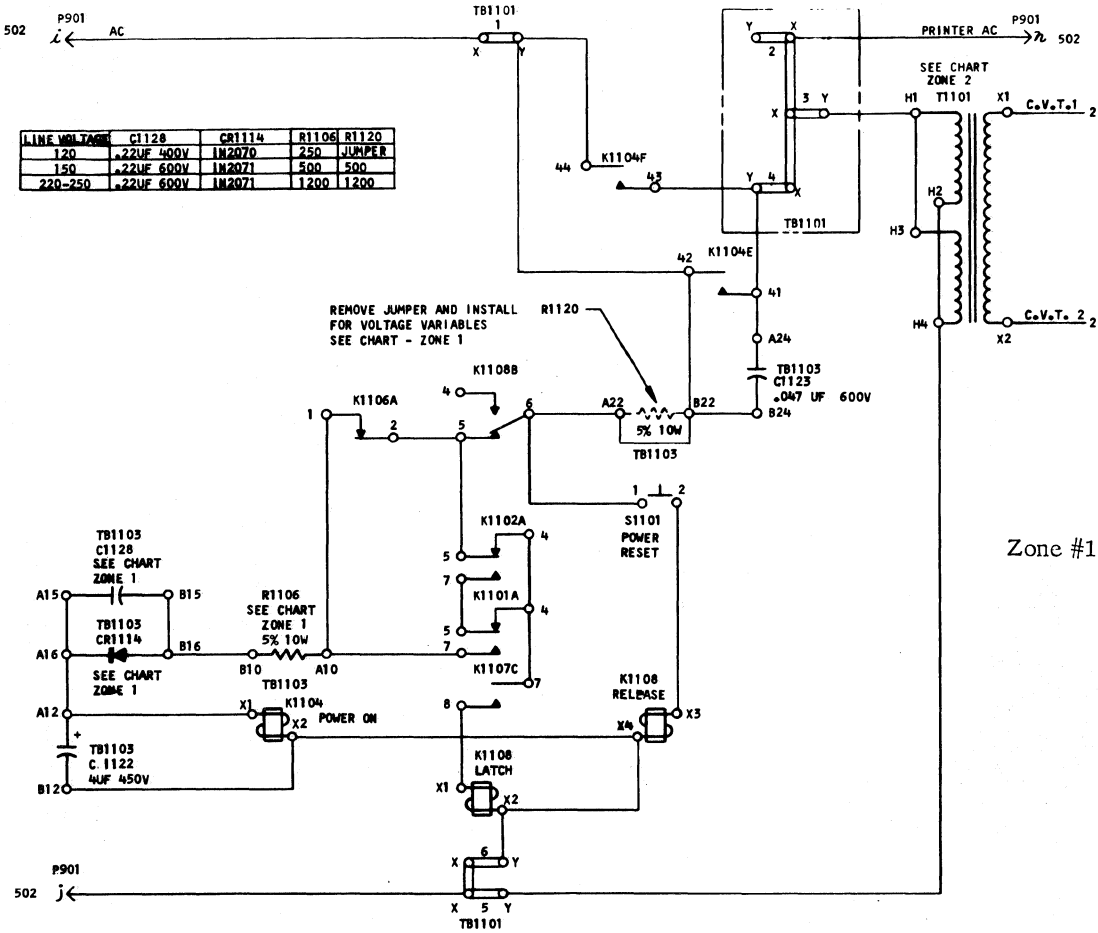
| PAGE | DESCRIPTION | ER DATE | REV | PAGE | DESCRIPTION | ER DATE | REV |
|------|---|---------|-----|------|--|---------|-----|
| 100 | ARITHMETIC & MEMORY UNIT INDEX | 3-18-64 | B | 140 | KB OUTPUT, C1 - C7, C & M CHAR, ESK | 3-13-64 | A |
| 101 | POWER SUPPLY | 3-13-64 | A | 141 | MEMORY ADDRESS ENCODING | 3-13-64 | A |
| 102 | POWER SUPPLY | 3-18-64 | B | 142 | EMCNFF, MAFF, LOCK RY SD, PRINT ALARM FF | 3-13-64 | A |
| 103 | NOT USED | 3-13-64 | A | 143 | RESET STANDARDIZER, CLK, SSC, POR, MERCURY START | 3-13-64 | A |
| 104 | *15V, BACKPLANE GROUND DISTRIBUTION | 3-13-64 | A | 144 | START RELAY RESET (SR RE), *35V SENSING RELAY | 3-13-64 | A |
| 105 | -4, 25V, GROUND DISTRIBUTION | 3-13-64 | A | 145 | AEC, LANE 63, AMFF, AEC LOCK | 3-13-64 | A |
| 106 | -15V, -15M, -100 V DISTRIBUTION | 3-13-64 | A | 146 | T0 - SHIFT RIGHT OR SHIFT RIGHT & ROUND LOGIC | 3-13-64 | A |
| 107 | DIGIT DISTRIBUTOR - DDO THRU DD7 | 3-13-64 | A | 147 | T1 - TRANSFER LOGIC | 3-13-64 | A |
| 108 | DIGIT DISTRIBUTOR - DDB THRU DDT | 3-13-64 | A | 148 | T2 - PRINT LOGIC | 3-13-64 | A |
| 109 | MART FF'S | 3-13-64 | A | 149 | T3, 4 & 5 - ADD OR SUB, A, B OR C LOGIC | 3-13-64 | A |
| 110 | MEMORY DECODING - X DRIVERS, ENABLE TSC WRITE | 3-13-64 | A | 150 | T6 - CLEAR LOGIC | 3-13-64 | A |
| 111 | MEMORY DECODING - X DRIVERS (7, 8, 9, 10) | 3-13-64 | A | 151 | T7 - MULTIPLY LOGIC | 3-13-64 | A |
| 112 | MEMORY DECODING - X DRIVERS (11, 12, 13) | 3-13-64 | A | 152 | T7 - DIVIDE LOGIC | 3-13-64 | A |
| 113 | MEMORY DECODING - Y DRIVERS (1-8) | 3-13-64 | A | 153 | NOT USED | 3-13-64 | A |
| 114 | Y9 & Y10 MEMORY DRIVERS, MEMORY CARD AND MRFF'S | 3-13-64 | A | 154 | CARD LOCATION CHART | 3-13-64 | A |
| 115 | MEMORY CARD, ADDRESS SELECTION CHART | 3-13-64 | A | 155 | CARD LOCATION CHART | 3-13-64 | A |
| 116 | FFA, FFB, PRINT C | 3-13-64 | A | 156 | CARD LOCATION CHART | 3-13-64 | A |
| 117 | FFD, FFP, "FFC" | 3-13-64 | A | 157 | CARD LOCATION CHART | 3-13-64 | A |
| 118 | NOT USED | 3-13-64 | A | 158 | CARD ELEMENTS | 3-13-64 | A |
| 119 | TIME FF'S - T0 - T7, DVFF, TC | 3-13-64 | A | 159 | CARD ELEMENTS | 3-13-64 | A |
| 120 | EOT, MTA, MTB, READ, WRITE | 3-13-64 | A | 160 | CARD ELEMENTS, RELAY PILE UP | 3-13-64 | A |
| 121 | READ B1 | 3-13-64 | A | 161 | COMPONENT LOCATION | 3-13-64 | A |
| 122 | KB DATA ENCODER, PK, 9 → WR, MR → WR, KB → WR | 3-13-64 | A | 162 | CONNECTOR INDEX | 3-13-64 | A |
| 123 | MRFF'S | 3-13-64 | A | | | | |
| 124 | T/C1, T/C2, T/C4, T/C8 | 3-13-64 | A | | | | |
| 125 | SUM → MEMFF, MR → MEMFF, INHIBIT DRIVERS | 3-13-64 | A | | | | |
| 126 | MEMORY CLEAR, EOCA, END OP, MUL + DIV | 3-13-64 | A | | | | |
| 127 | ADD + SUB, DCA, SM | 3-13-64 | A | | | | |
| 128 | SUM 1, ADDER DECIMAL CORRECTOR | 3-13-64 | A | | | | |
| 129 | ADDER, SUM 2, SUM 4, SUM 8, SUM 9, SUM 0, SUM 0 | 3-13-64 | A | | | | |
| 130 | SET SUM → MEM | 3-13-64 | A | | | | |
| 131 | CIFF, DOREVFF | 3-13-64 | A | | | | |
| 132 | COMFF, LN3FF, NZFF, SFF | 3-13-64 | A | | | | |
| 133 | SCFF, RRSOL | 3-13-64 | A | | | | |
| 134 | RACK STOP FF'S COL. 1-7 | 3-13-64 | A | | | | |
| 135 | RACK STOP FF'S COL. 8-12, U, T, CHAR | 3-13-64 | A | | | | |
| 136 | RACK STOP FF SYM | 3-13-64 | A | | | | |
| 137 | FF'S - S0 - S4, PC | 3-13-64 | A | | | | |
| 138 | FF'S S5-S9 | 3-13-64 | A | | | | |
| 139 | ALL TOTALS | 3-13-64 | A | | | | |

NOTES:

1. WIRING SHOWN IN DASHED LINES INDICATE OPTIONAL FEATURES
2. CHARACTERS IN PARENTHESIS ON WIRING INDICATES NAME OF OPTIONAL FEATURE REQUIRING THE WIRING
3. CHARACTERS IN PARENTHESIS LOCATED NEAR CARD ELEMENT INDICATES OPTIONAL FEATURE REQUIRING THAT CARD.
4. ZONES ON INPUT SIGNALS INDICATE ZONE OF ORIGIN.
5. PAGE NUMBERS 500-550 REFER TO KEYBOARD PRINTER SCHEMATIC 15118011.
6. PRINTER SHOWN IN PHANTOM LINES(---) FOR REFERENCE PURPOSES ONLY.
7. "ME" INDICATES A SIGNAL WHICH REQUIRED CONSIDERATION OF MUTUAL EXCLUSIVENESS IN THE DETERMINATION OF ITS LOAD.
8. ALL ELEMENT PINS (OTHER THEN VOLTAGES) ARE SHOWN EXCEPT ON FF ELEMENTS. PINS 10 & 15, 19 & 21 IF SHOWN ON FF ELEMENTS ARE "CLOCK" INPUTS. ALL OTHER ELEMENT PINS SHOWN WITHOUT SIGNAL ARE NOT WIRED.

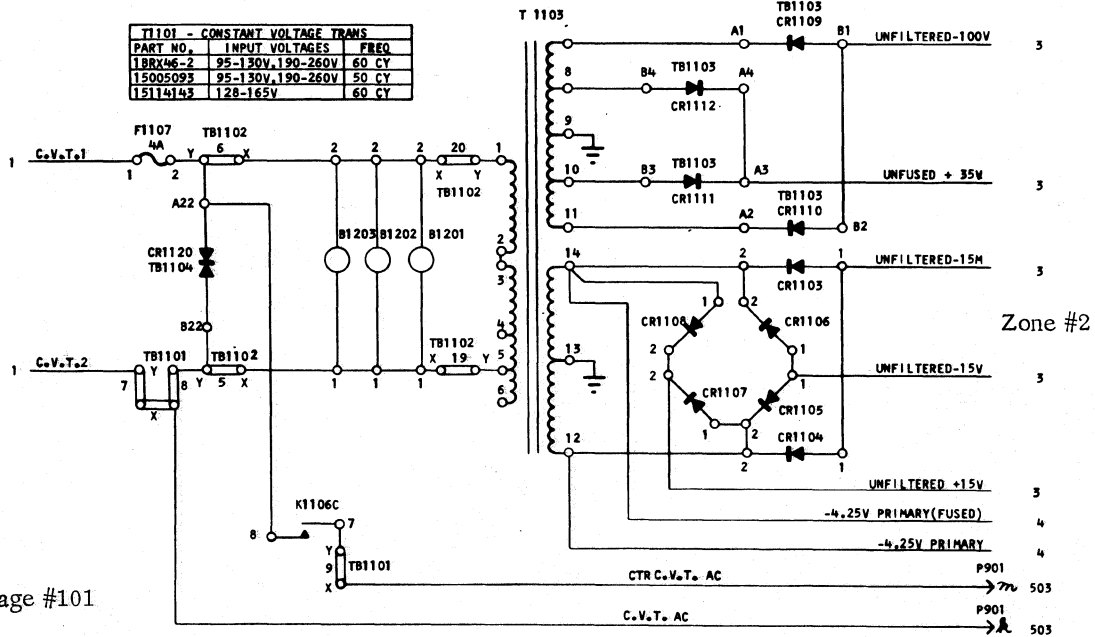
ABBREVIATIONS:

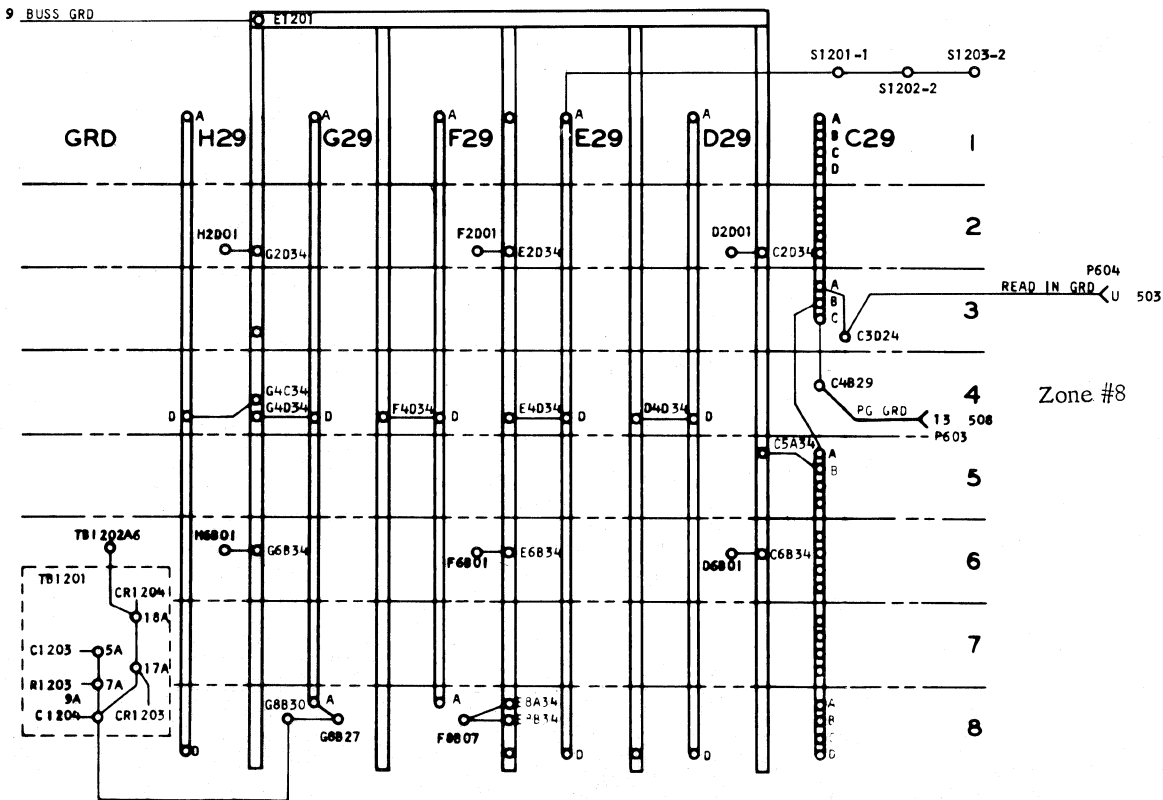
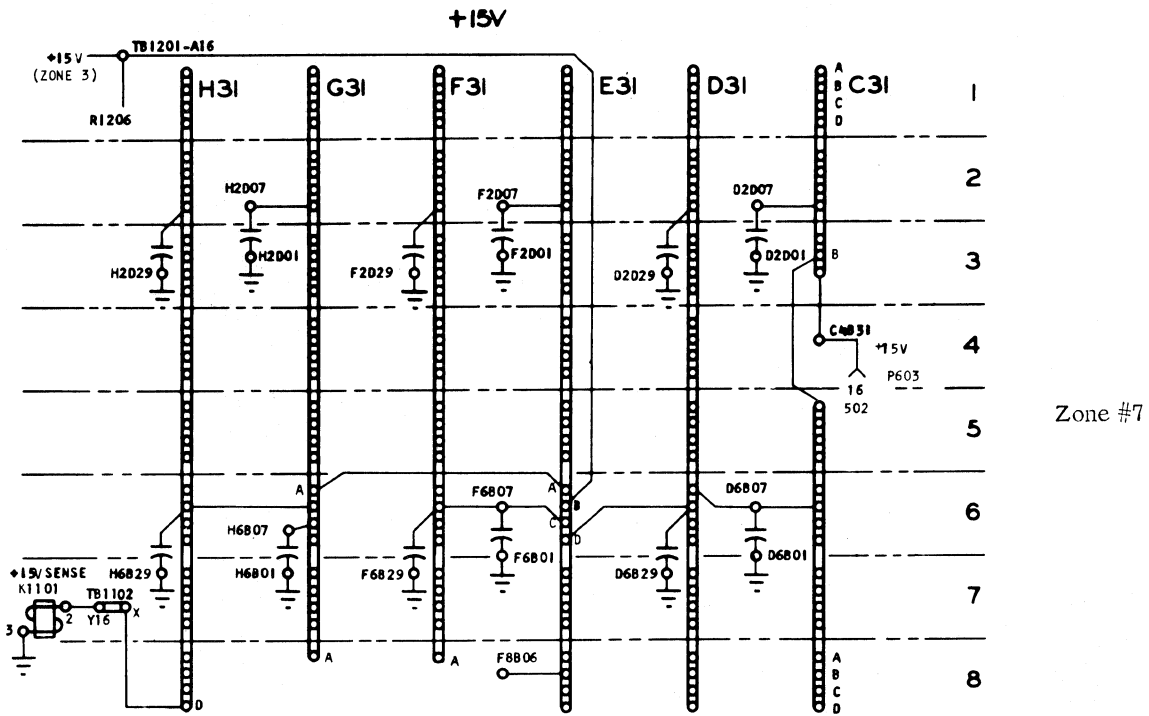
| | |
|----------------------|----------|
| OPTIONAL FEATURES: | WIRING: |
| (3M) 30 WORD MEMORY | 15113897 |
| (4M) 40 WORD MEMORY | 15113905 |
| (8M) 80 WORD MEMORY | 15113913 |
| (1M) 100 WORD MEMORY | 15113921 |
| (DV) DIVIDE | 15225899 |
| (DV) DIVIDE INACTIVE | 15225881 |

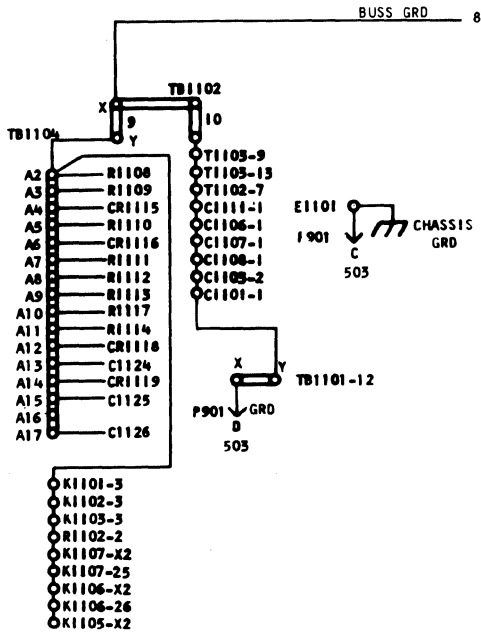


T1101 - CONSTANT VOLTAGE TRANS

| PART NO. | INPUT VOLTAGES | FREQ |
|----------|-------------------|-------|
| 1BRX46-2 | 95-130V, 190-260V | 60 CY |
| 15005023 | 95-130V, 190-260V | 50 CY |
| 15114143 | 128-165V | 60 CY |



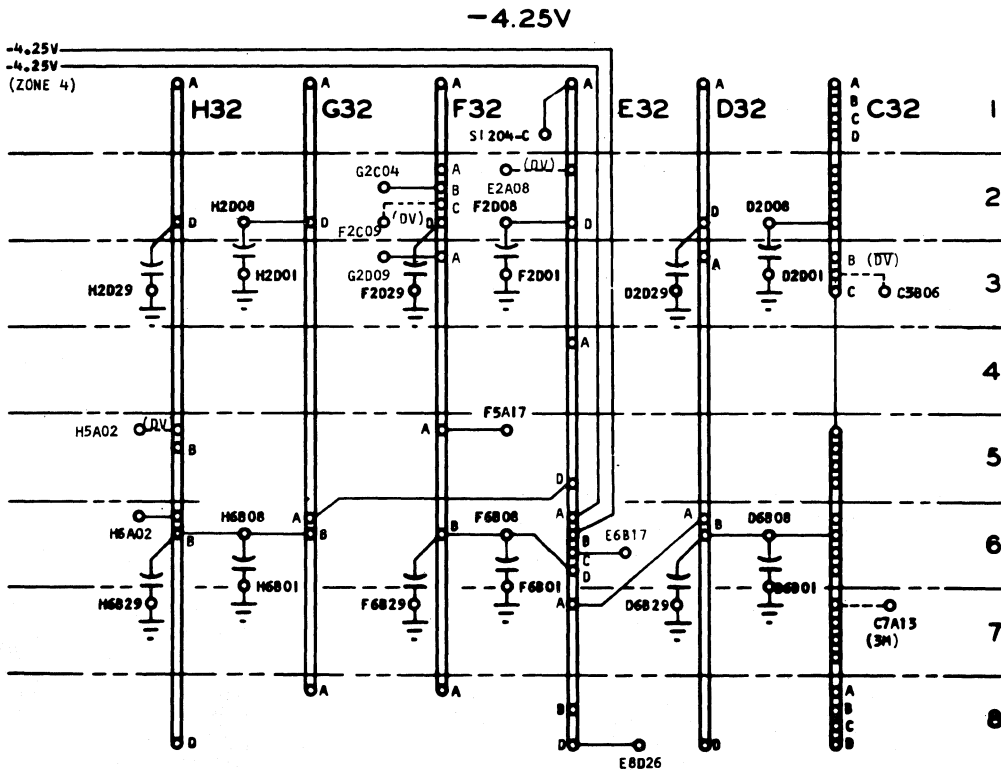




| REFERENCE INFORMATION | | |
|-----------------------|-----------|--------------------------|
| SUPPLY VOLTS | TOLERANCE | * MAXIMUM CURRENT (AMPS) |
| +1E | ±5% | 3.0 |
| -1E | ±5% | 3.0 |
| +15EH | ±5% | 2.2 |
| -4.25 | ±5% | 2.5 |
| -100 | ±5% | 1.5 |
| -5E | ±10% | 0.25 |
| +35UF | ±5% | 0.05 |
| +150 | ±10% | 0.5 |

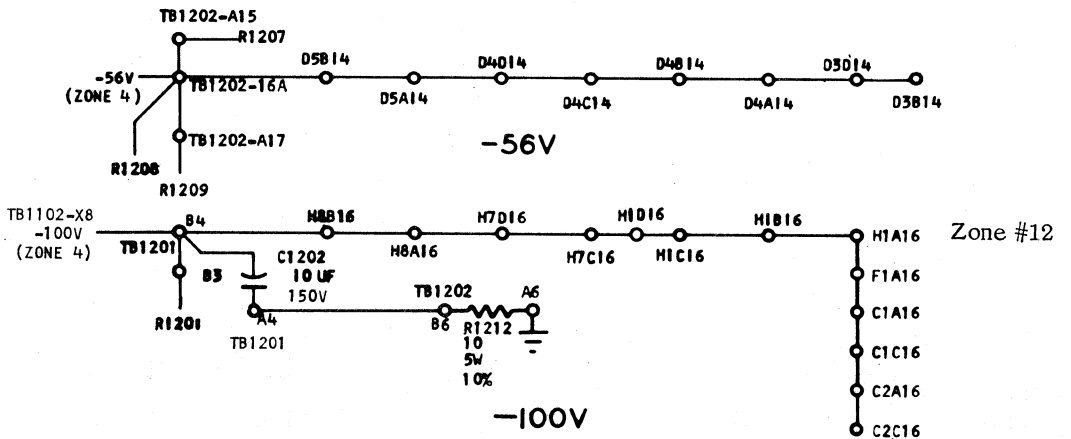
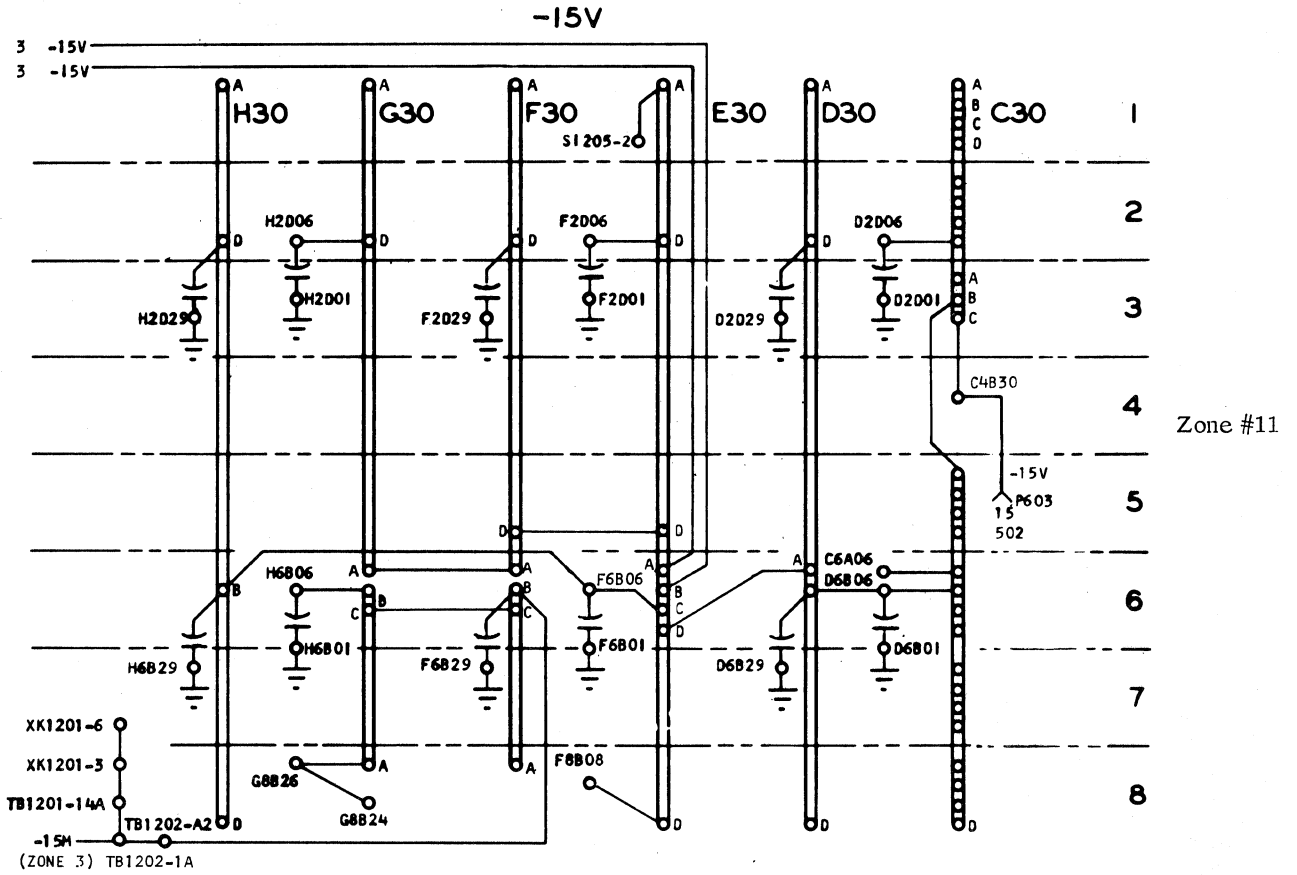
* INCLUDES RIPPLE TOLERANCE AND INPUT VOLTAGE VARIATION OF 95-130 VOLTS.

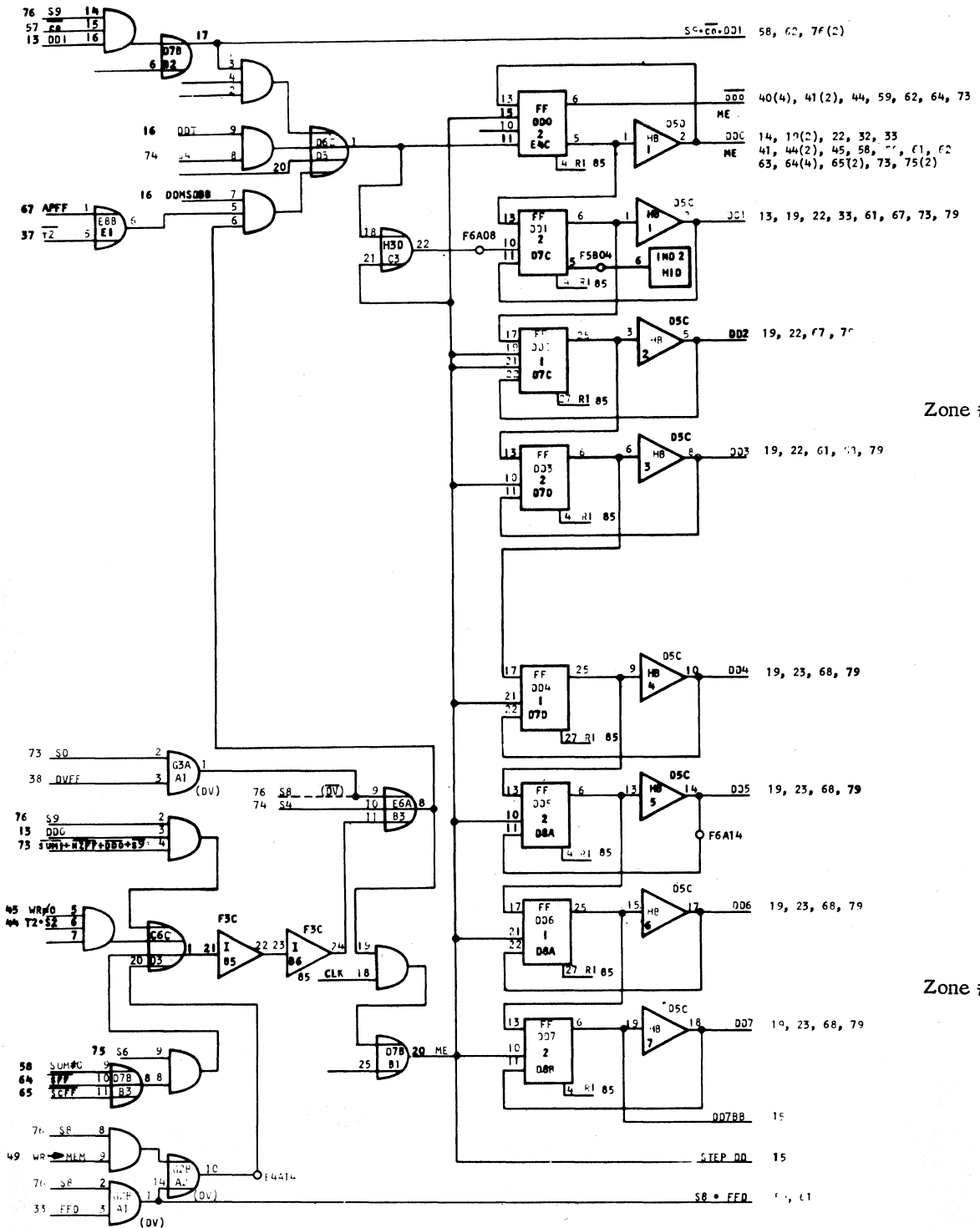
Zone #9



Zone #10

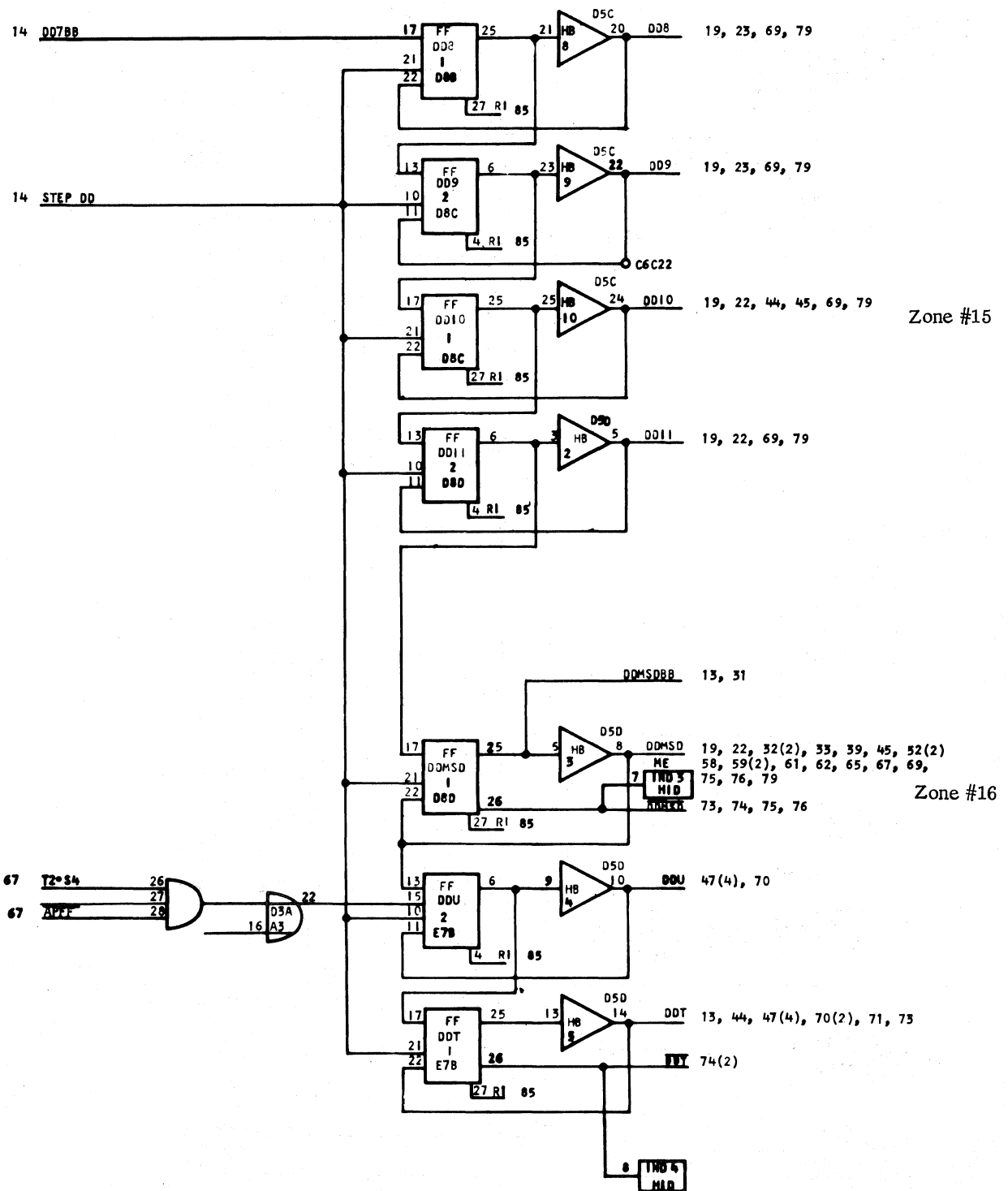
Ref. Page #105

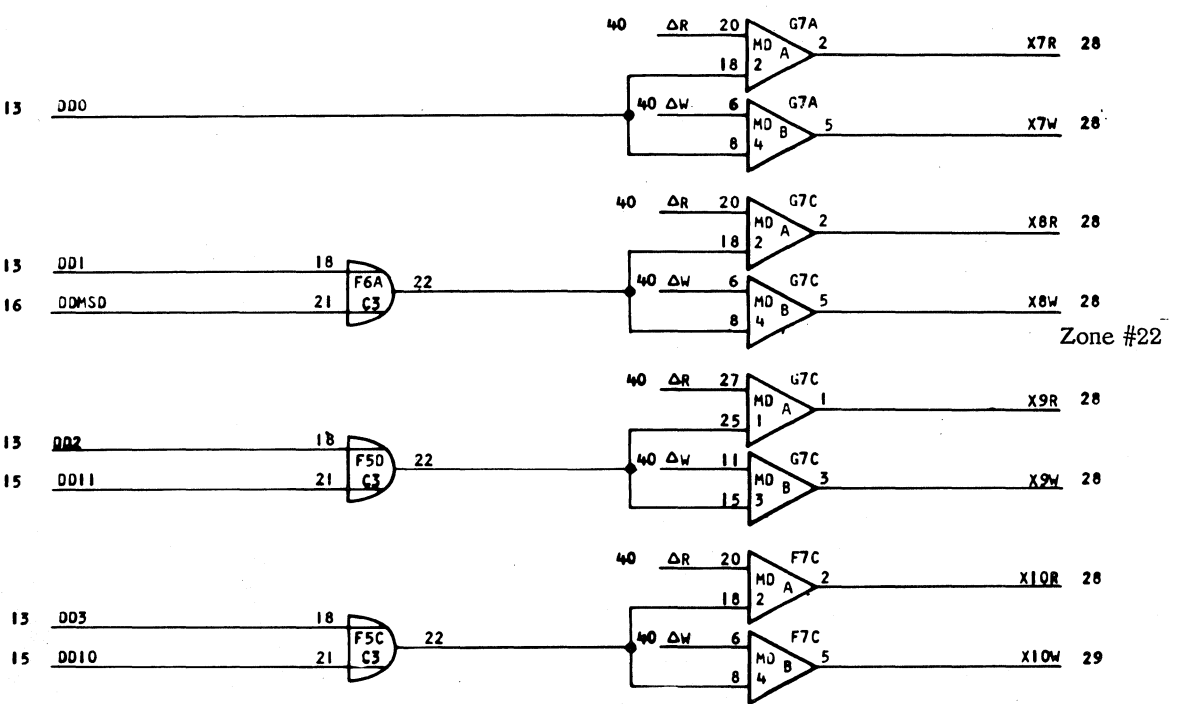
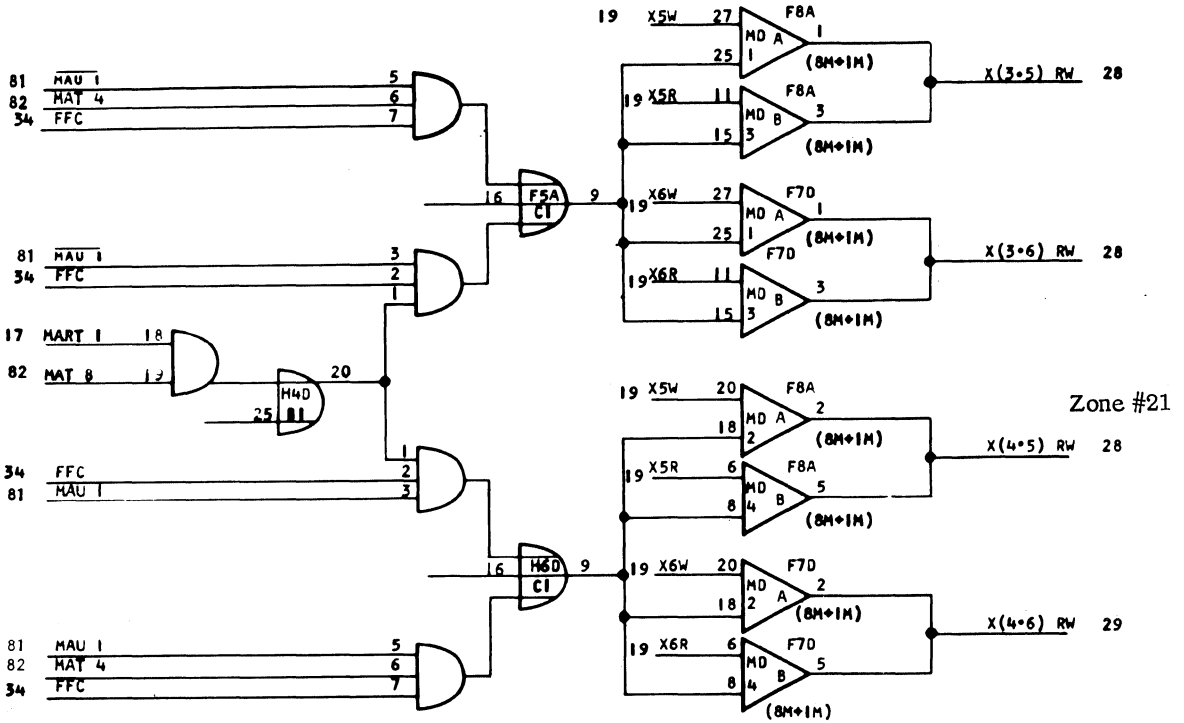


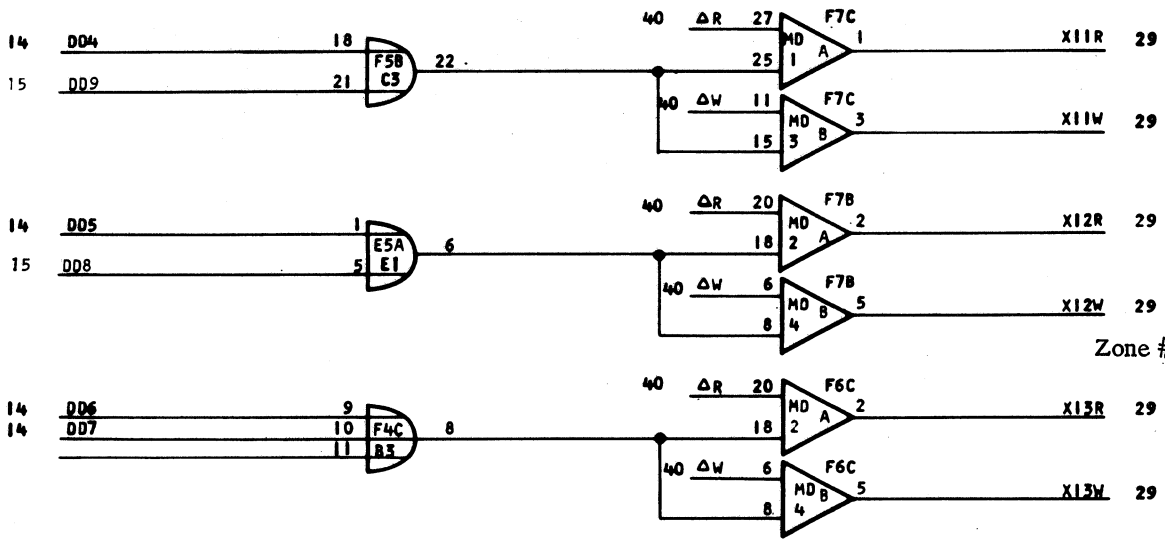


Zone #13

Zone #14

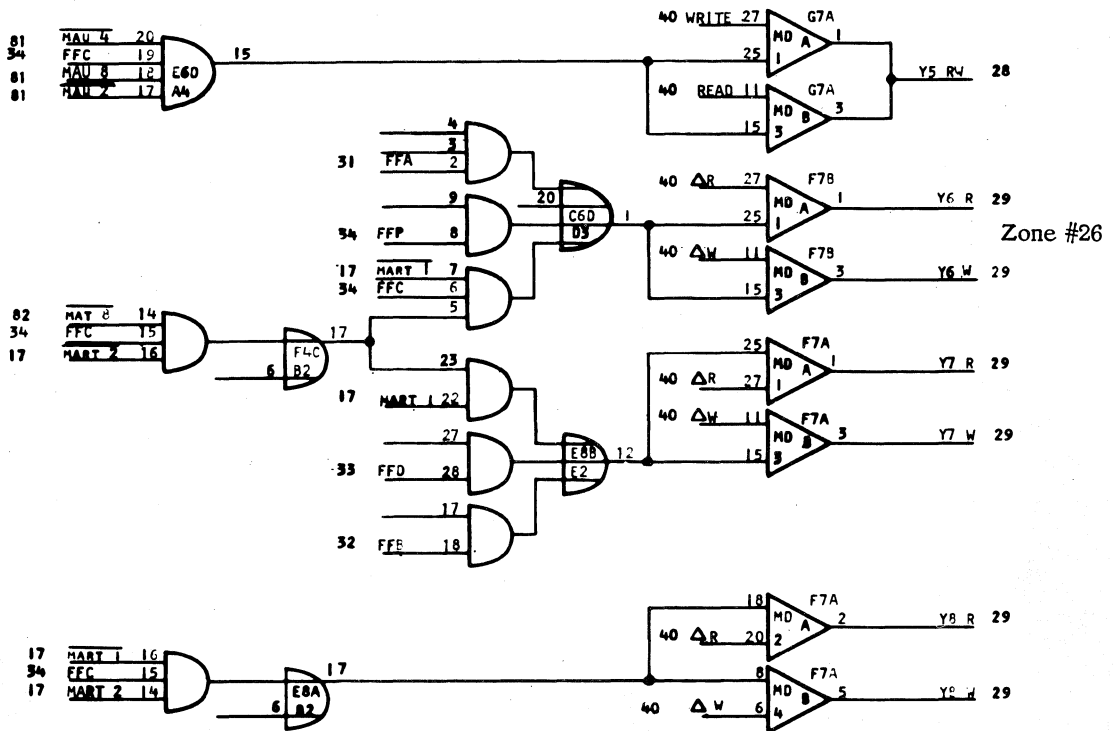
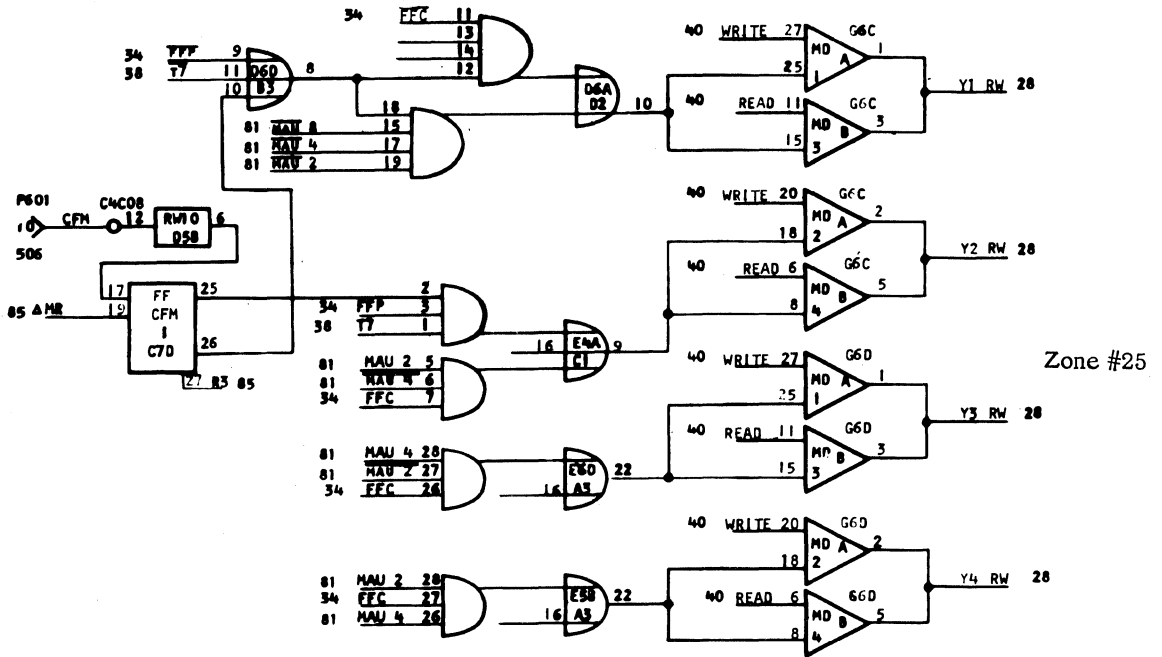


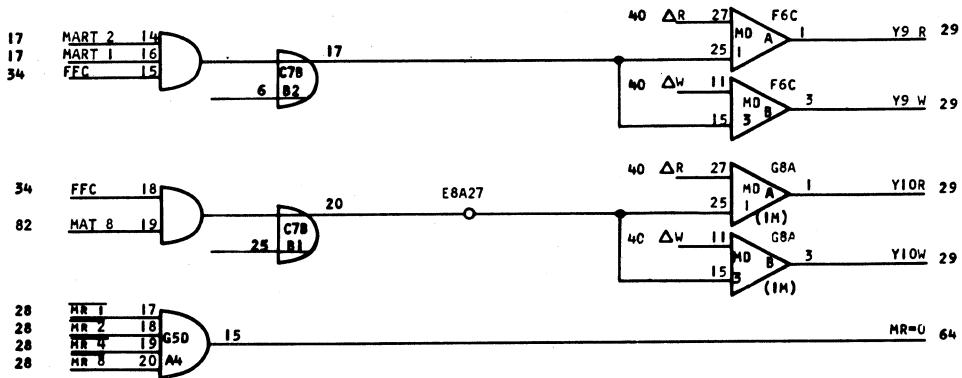




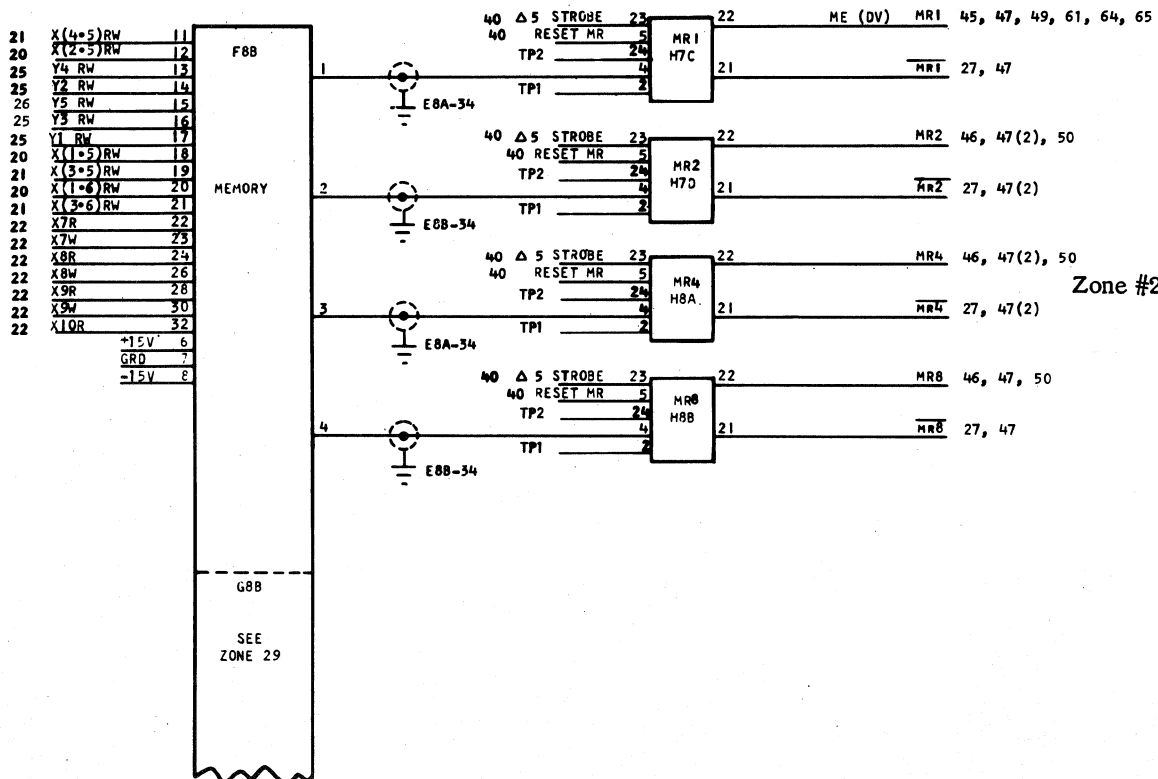
Zone #23

Zone #24





Zone #27



Zone #28

| | | |
|----|----------------|-------------|
| | | SEE ZONE 28 |
| | | GRB |
| 22 | X10W | 1 |
| 23 | X11R | 3 |
| 23 | X11W | 5 |
| 23 | X12R | 7 |
| 20 | X(2*6)RW | 8 |
| 23 | X12W | 9 |
| 21 | X(4*6)RW | 10 |
| 23 | X13R | 11 |
| 23 | X13W | 12 |
| 26 | Y6R | 13 |
| 26 | Y7W | 14 |
| 26 | Y6W | 15 |
| 26 | Y7R | 16 |
| 26 | Y8R | 17 |
| 26 | Y8W | 18 |
| 27 | Y9R | 19 |
| 27 | Y9W | 20 |
| 27 | Y10R | 21 |
| 27 | Y10W | 22 |
| 50 | I2 | 23 |
| 51 | CLR 2 | |
| 50 | I8 | 25 |
| 51 | CLR 8 | |
| 49 | I1 | 28 |
| 51 | CLR 1 | |
| 50 | I4 | 29 |
| 51 | CLR 4 | |
| 51 | -15M MEM CLR 2 | 31 |
| 51 | -15M MEM CLR 1 | 32 |
| | -15M | 24 |
| | -15M | 26 |
| | GRD | 27 |
| | GRD | 30 |

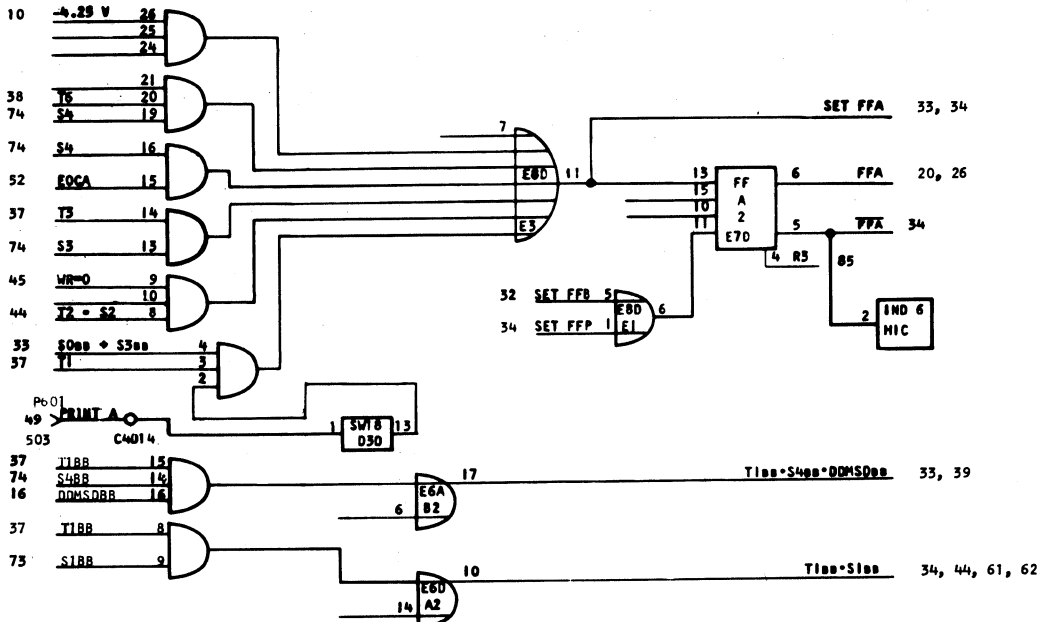
Zone #29

| E2100 MEMORY ADDRESS SELECTION | | | | | | | | | |
|--------------------------------|-----------------|---|-----|-----------------|---|-----|-----------------|---|------|
| FLIP FLOP | MEMORY LOCATION | X | Y | MEMORY LOCATION | X | Y | MEMORY LOCATION | X | Y |
| P | 00 | 1 | 1.6 | 34 | 1 | 3.9 | 68 | 3 | 5.8 |
| A | 01 | 2 | 1.6 | 35 | 2 | 3.9 | 69 | 4 | 5.8 |
| | 02 | 1 | 2.6 | 36 | 1 | 4.9 | 70 | 3 | 1.9 |
| | 03 | 2 | 2.6 | 37 | 2 | 4.9 | 71 | 4 | 1.9 |
| | 04 | 1 | 3.6 | 38 | 1 | 5.9 | 72 | 3 | 2.9 |
| | 05 | 2 | 3.6 | 39 | 2 | 5.9 | 73 | 4 | 2.9 |
| | 06 | 1 | 4.6 | 40 | 3 | 1.6 | 74 | 3 | 3.9 |
| | 07 | 2 | 4.6 | 41 | 4 | 1.6 | 75 | 4 | 3.9 |
| | 08 | 1 | 5.6 | 42 | 3 | 2.6 | 76 | 3 | 4.9 |
| | 09 | 2 | 5.6 | 43 | 4 | 2.6 | 77 | 4 | 4.9 |
| B | 10 | 1 | 1.7 | 44 | 3 | 3.6 | 78 | 3 | 5.9 |
| D | 11 | 2 | 1.7 | 45 | 4 | 3.6 | 79 | 4 | 5.9 |
| | 12 | 1 | 2.7 | 46 | 3 | 4.6 | 80 | 1 | 1.10 |
| | 13 | 2 | 2.7 | 47 | 4 | 4.6 | 81 | 2 | 1.10 |
| | 14 | 1 | 3.7 | 48 | 3 | 5.6 | 82 | 1 | 2.10 |
| | 15 | 2 | 3.7 | 49 | 4 | 5.6 | 83 | 2 | 2.10 |
| | 16 | 1 | 4.7 | 50 | 3 | 1.7 | 84 | 1 | 3.10 |
| | 17 | 2 | 4.7 | 51 | 4 | 1.7 | 85 | 2 | 3.10 |
| | 18 | 1 | 5.7 | 52 | 3 | 2.7 | 86 | 1 | 4.10 |
| | 19 | 2 | 5.7 | 53 | 4 | 2.7 | 87 | 2 | 4.10 |
| | 20 | 1 | 1.8 | 54 | 3 | 3.7 | 88 | 1 | 5.10 |
| | 21 | 2 | 1.8 | 55 | 4 | 3.7 | 89 | 2 | 5.10 |
| | 22 | 1 | 2.8 | 56 | 3 | 4.7 | 90 | 3 | 1.10 |
| | 23 | 2 | 2.8 | 57 | 4 | 4.7 | 91 | 4 | 1.10 |
| | 24 | 1 | 3.8 | 58 | 3 | 5.7 | 92 | 3 | 2.10 |
| | 25 | 2 | 3.8 | 59 | 4 | 5.7 | 93 | 4 | 2.10 |
| | 26 | 1 | 4.8 | 60 | 3 | 1.8 | 94 | 3 | 3.10 |
| | 27 | 2 | 4.8 | 61 | 4 | 1.8 | 95 | 4 | 3.10 |
| | 28 | 1 | 5.8 | 62 | 3 | 2.8 | 96 | 3 | 4.10 |
| | 29 | 2 | 5.8 | 63 | 4 | 2.8 | 97 | 4 | 4.10 |
| | 30 | 1 | 1.9 | 64 | 3 | 3.8 | 98 | 3 | 5.10 |
| | 31 | 2 | 1.9 | 65 | 4 | 3.8 | 99 | 4 | 5.10 |
| | 32 | 1 | 2.9 | 66 | 3 | 4.8 | | | |
| | 33 | 2 | 2.9 | 67 | 4 | 4.8 | | | |

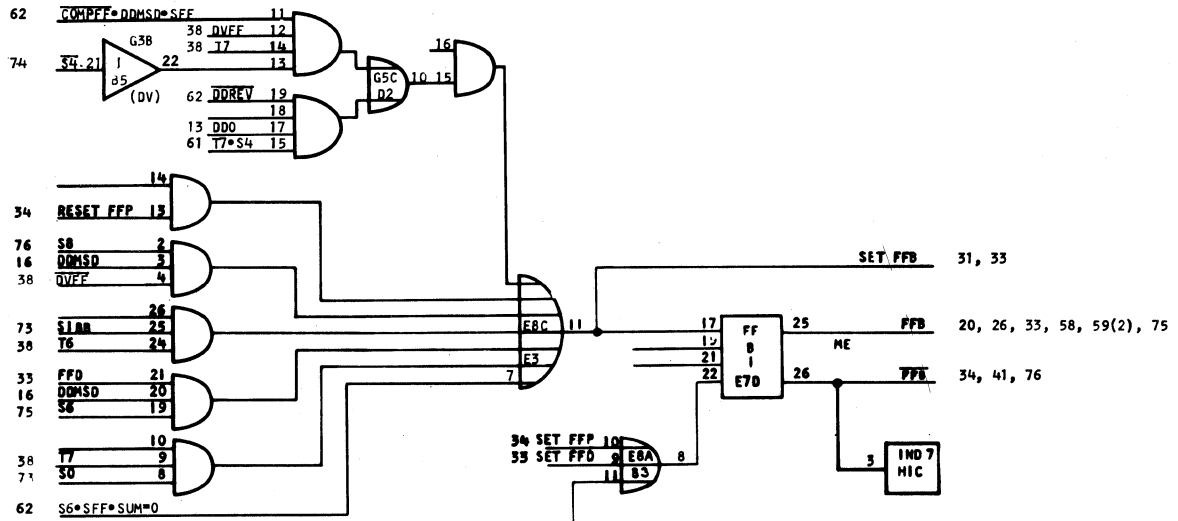
| DIGIT POSITION | X |
|----------------|------|
| 0 | 7.5 |
| 1 | 8.5 |
| 2 | 9.5 |
| 3 | 10.5 |
| 4 | 11.5 |
| 5 | 12.5 |
| 6 | 13.5 |
| 7 | 13.6 |
| 8 | 12.6 |
| 9 | 11.6 |
| 10 | 10.6 |
| 11 | 9.6 |
| 12 | 8.6 |

Zone #30

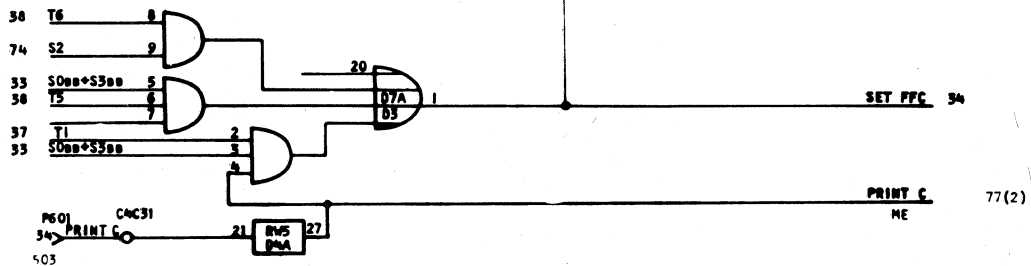
| MEMORY SIZE | MEMORY LOCATIONS |
|-------------|------------------|
| 30 WORD | 00-29 |
| 40 WORD | 00-39 |
| 80 WORD | 00-79 |
| 100 WORD | 00-99 |

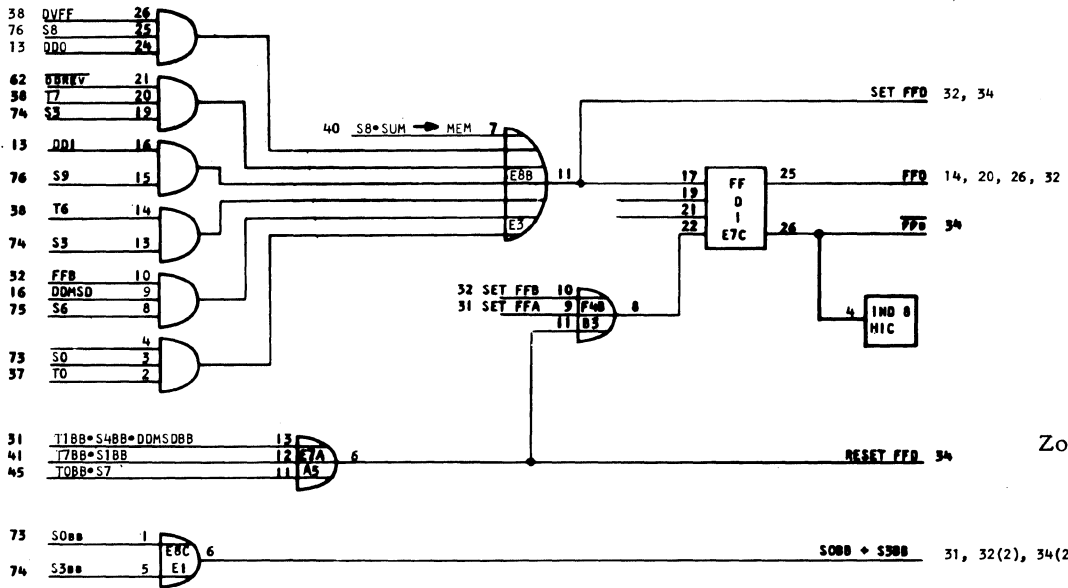


Zone #31

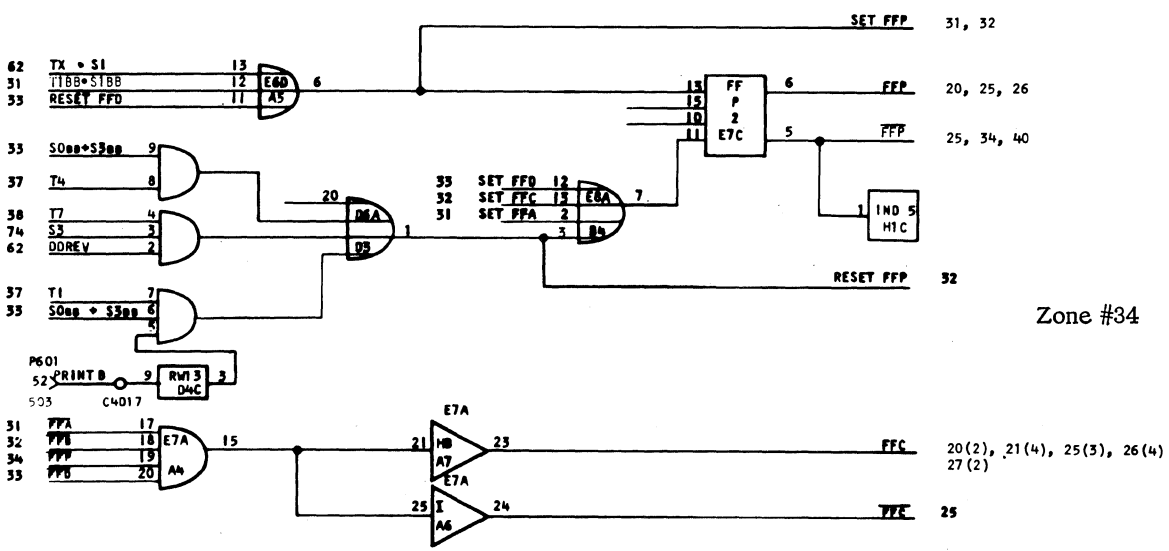


Zone #32

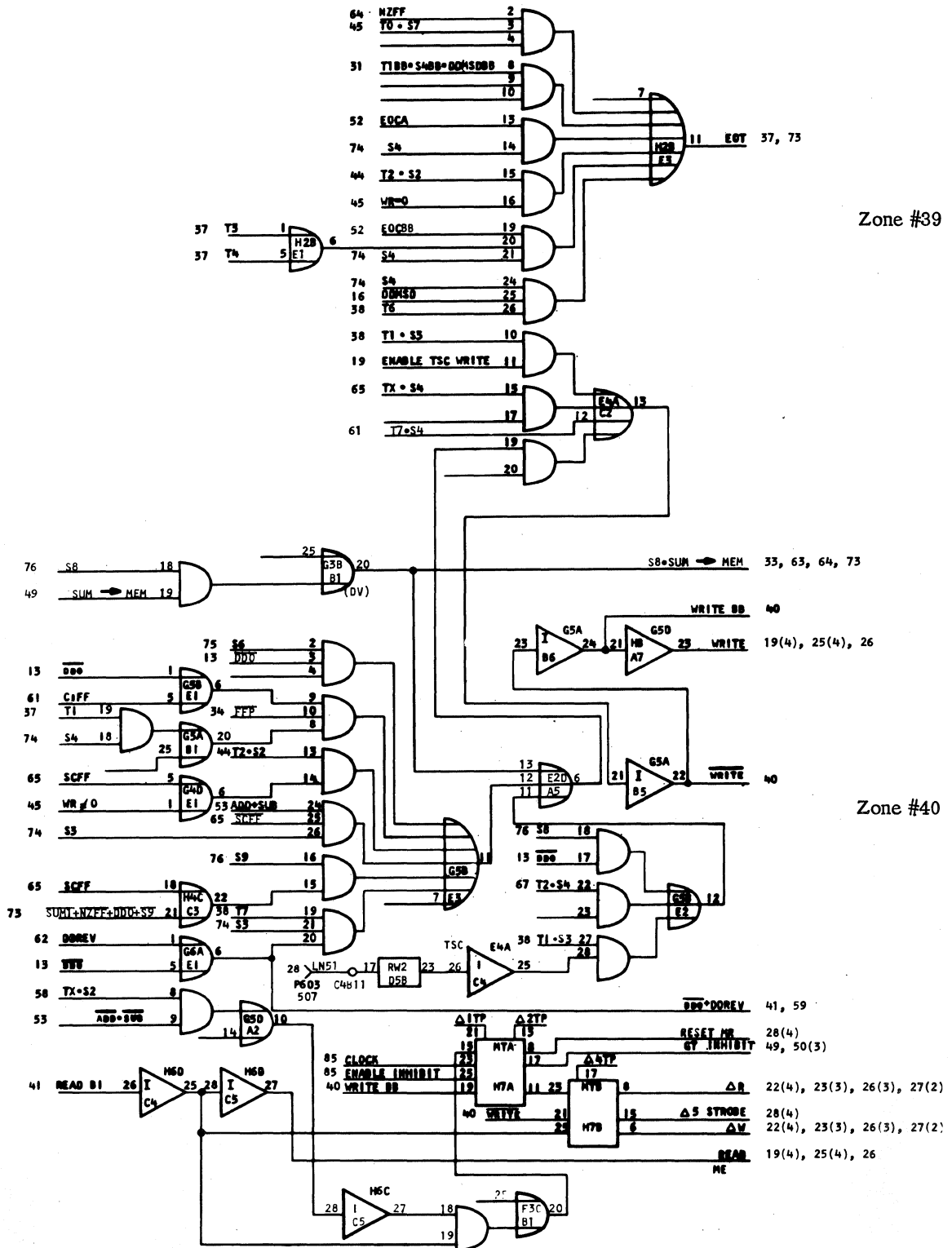


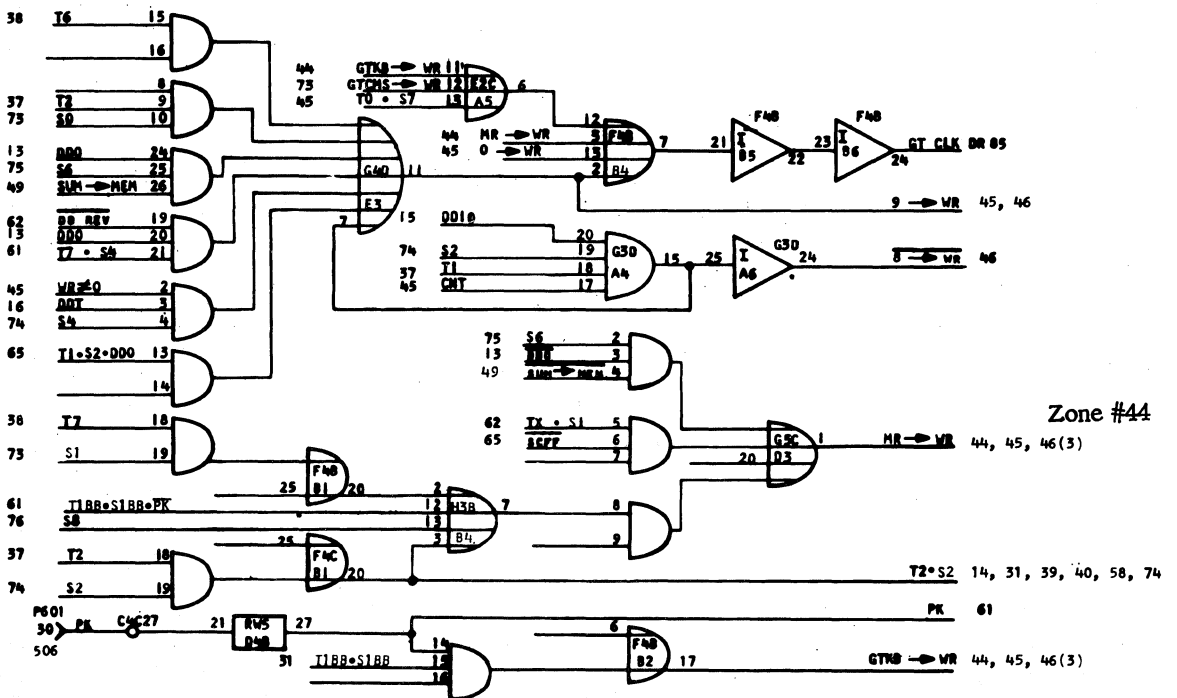
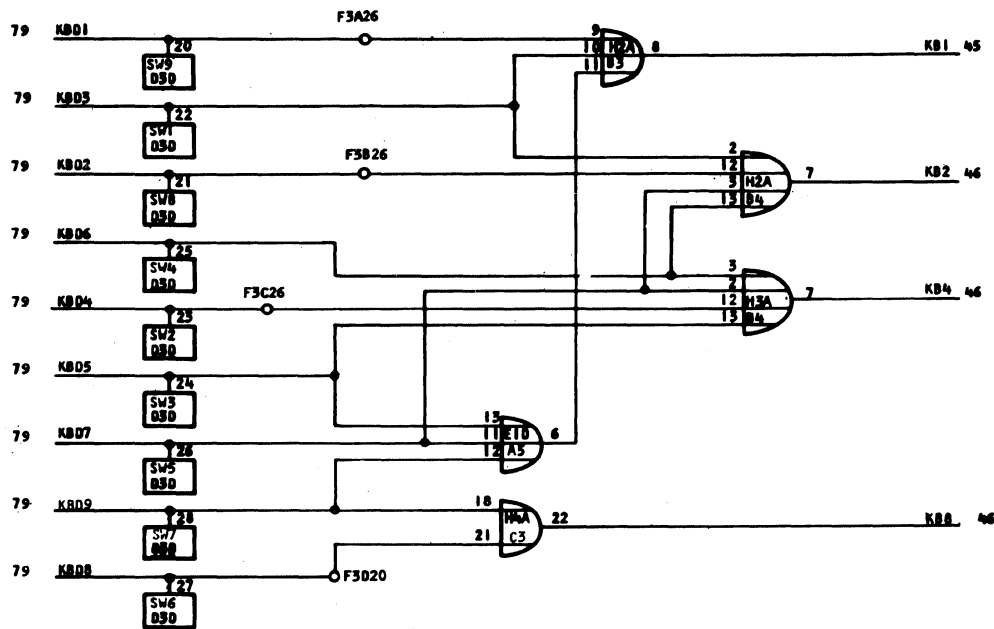


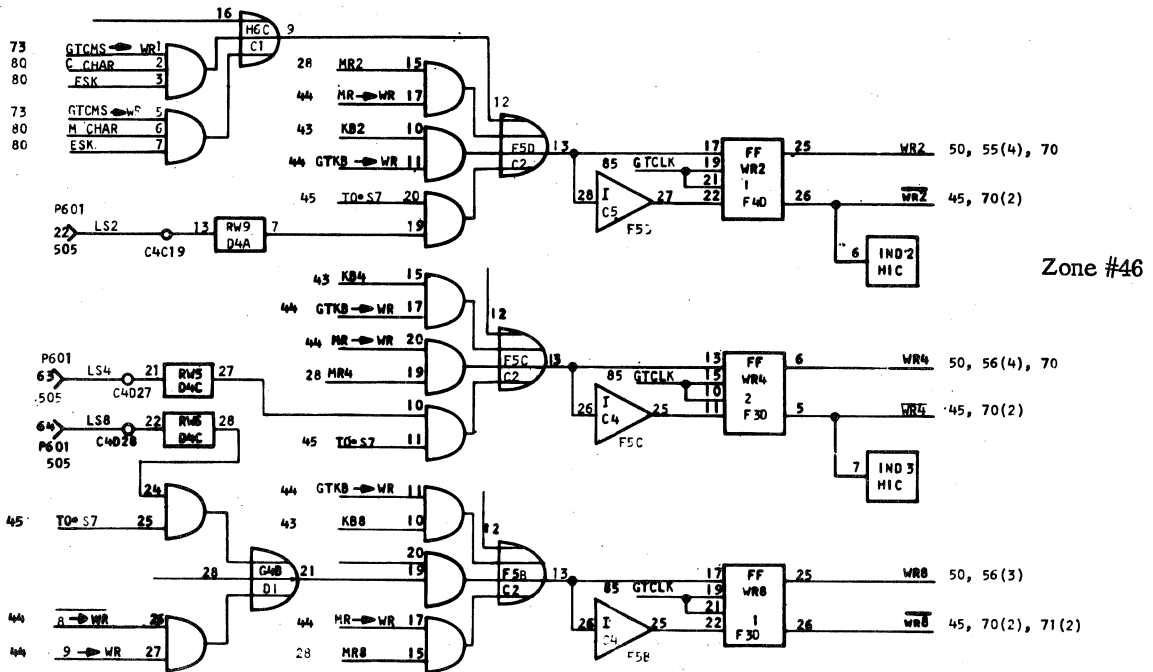
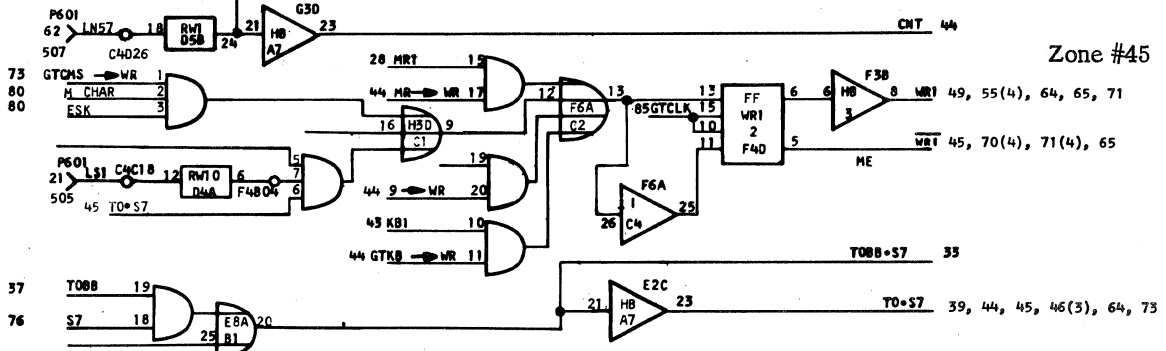
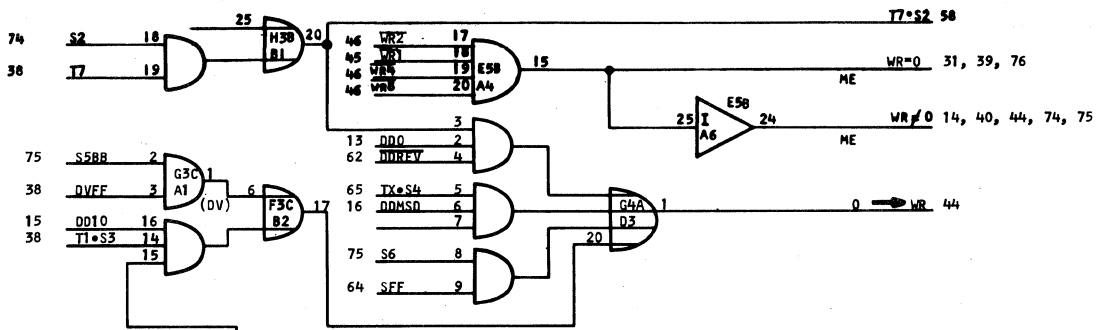
Zone #33

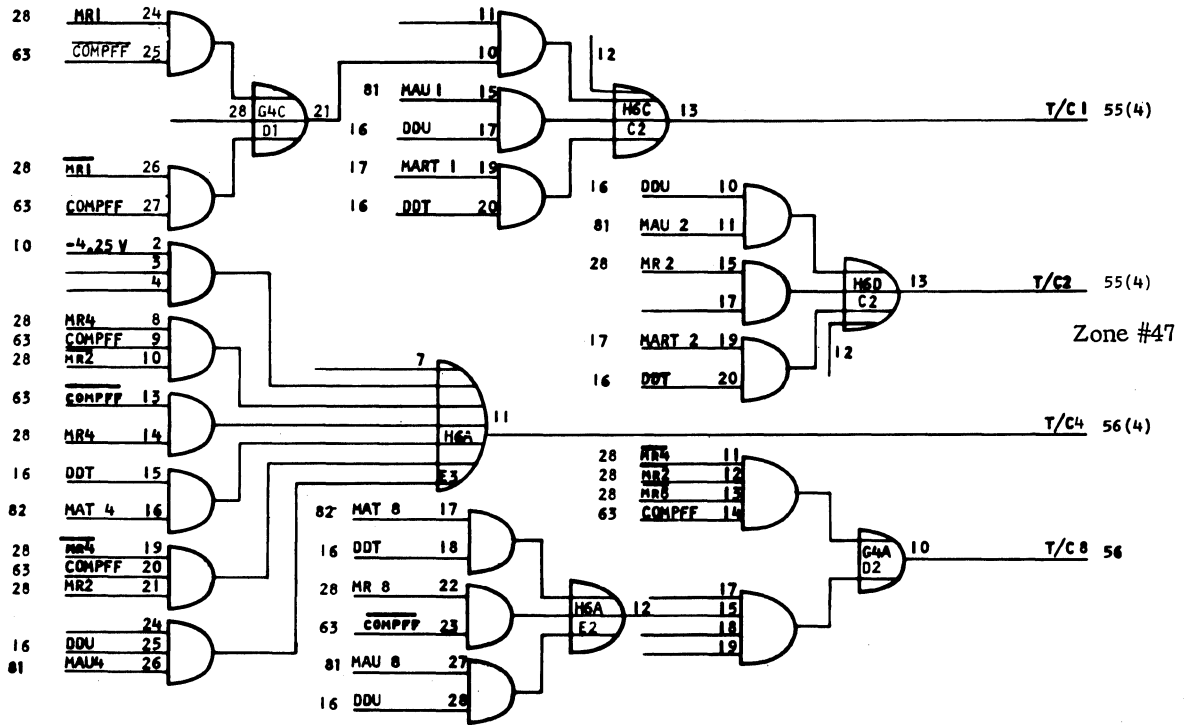


Zone #34

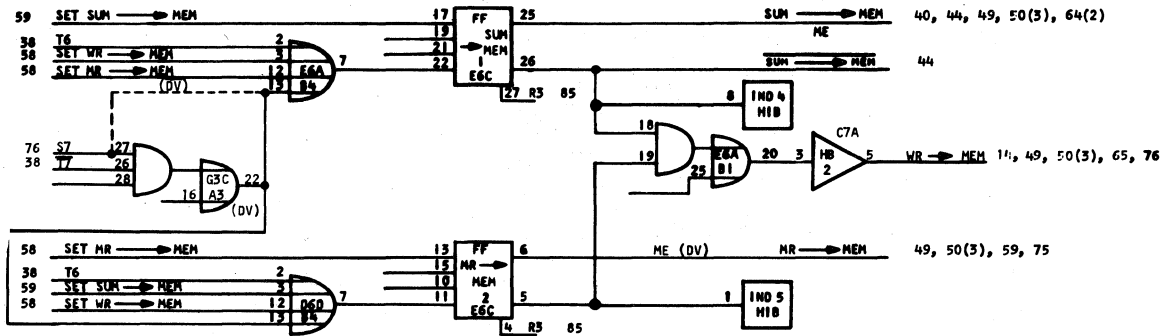




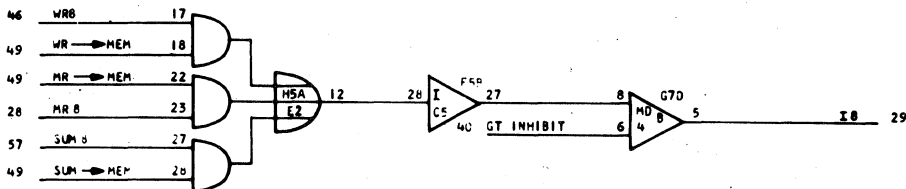
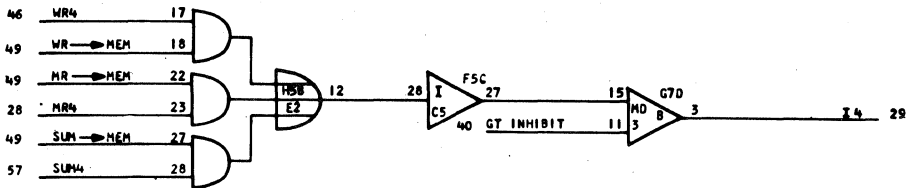
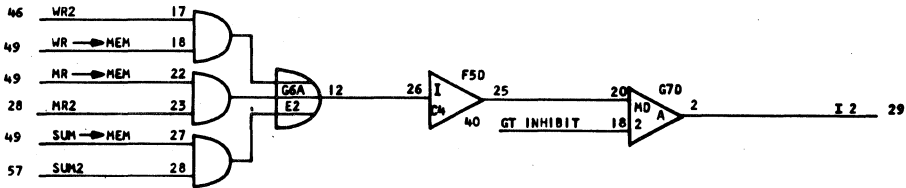
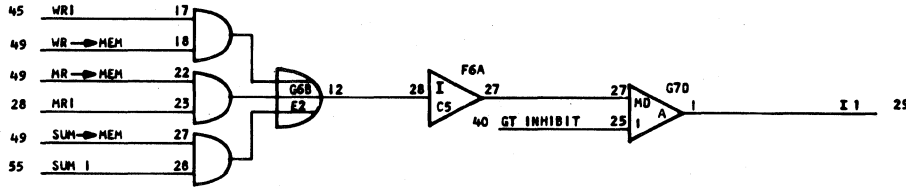




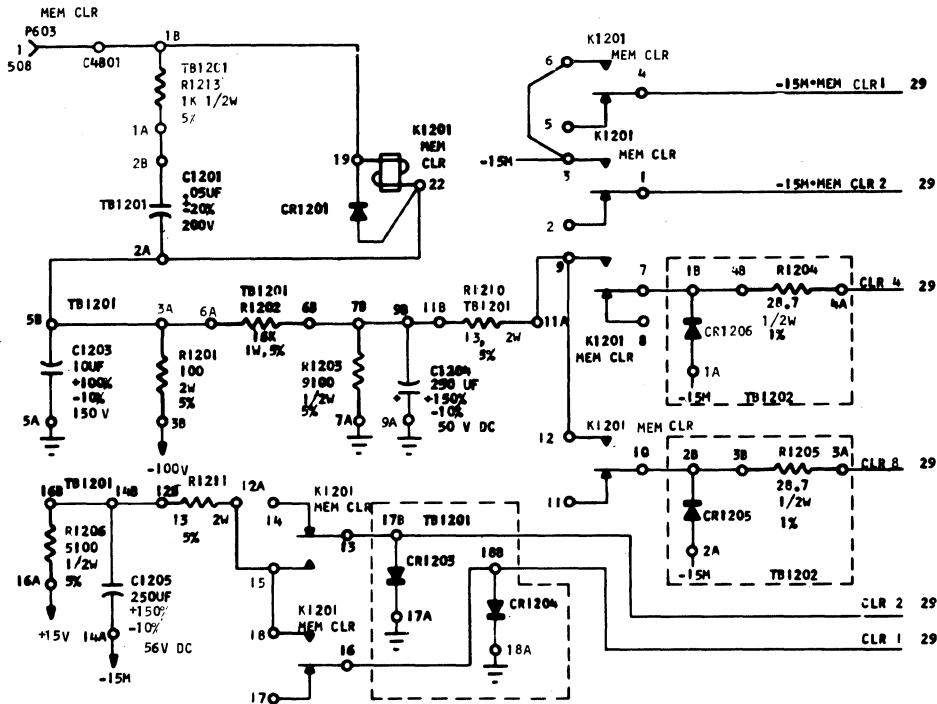
Zone #48



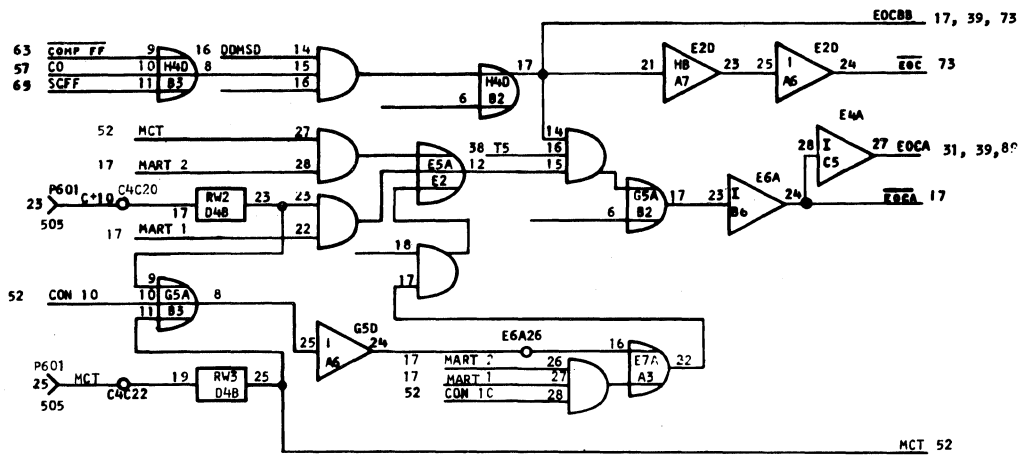
Zone #49



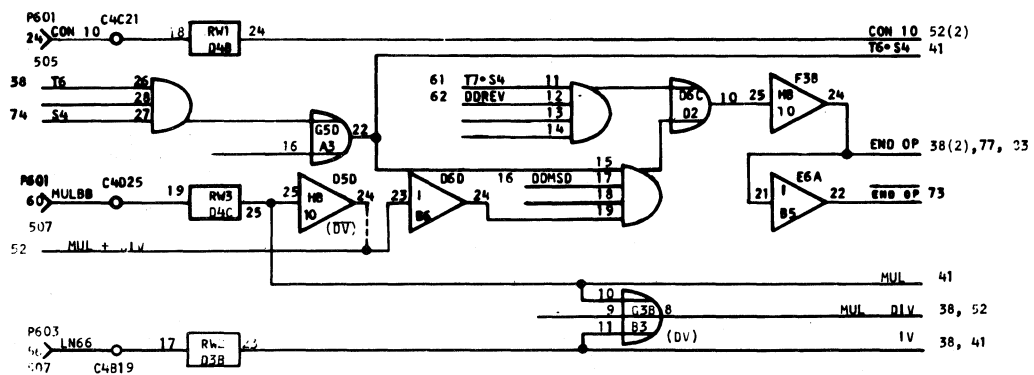
Zone #50

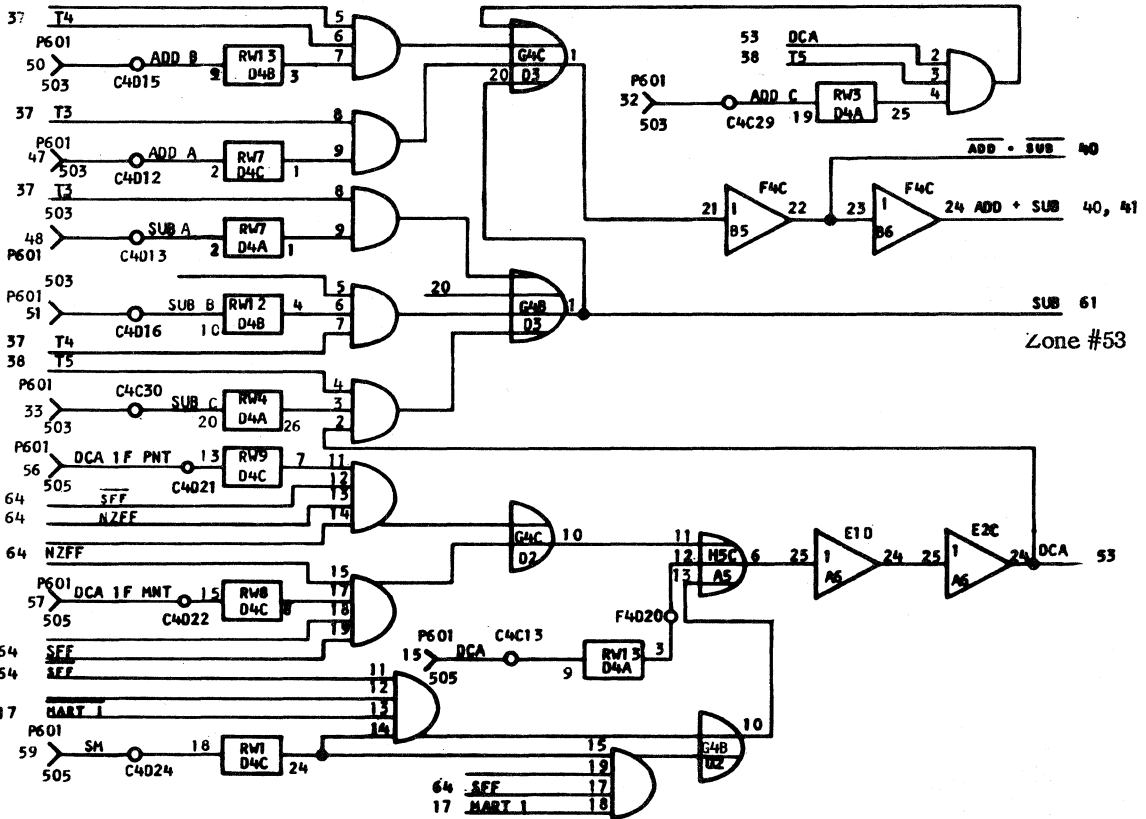


Zone #51

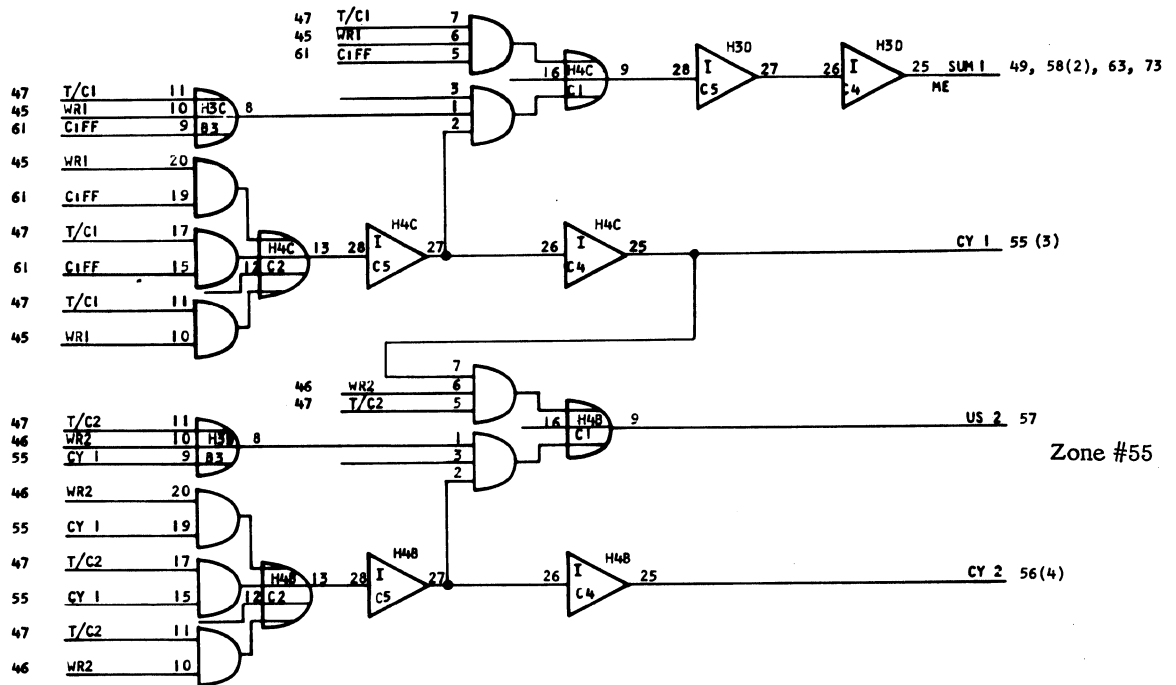


Zone #52

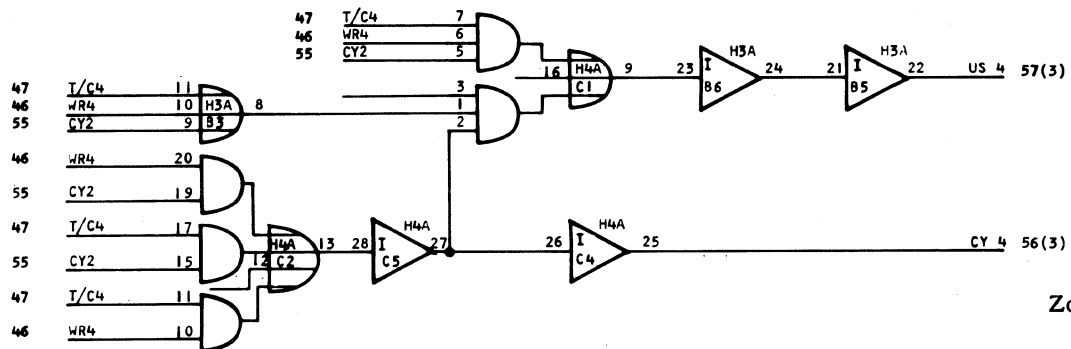




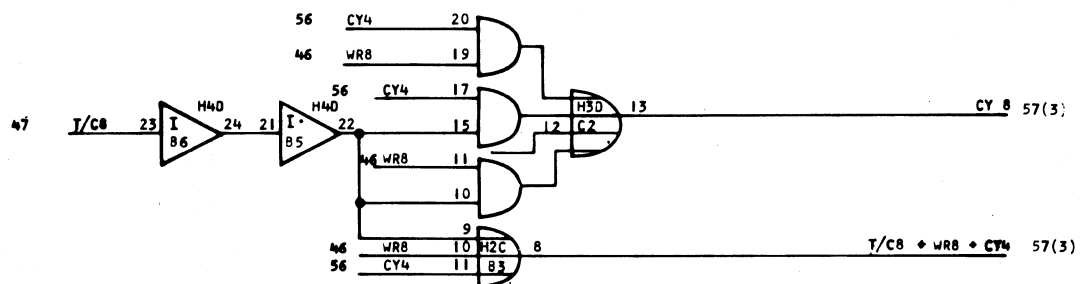
Zone #54

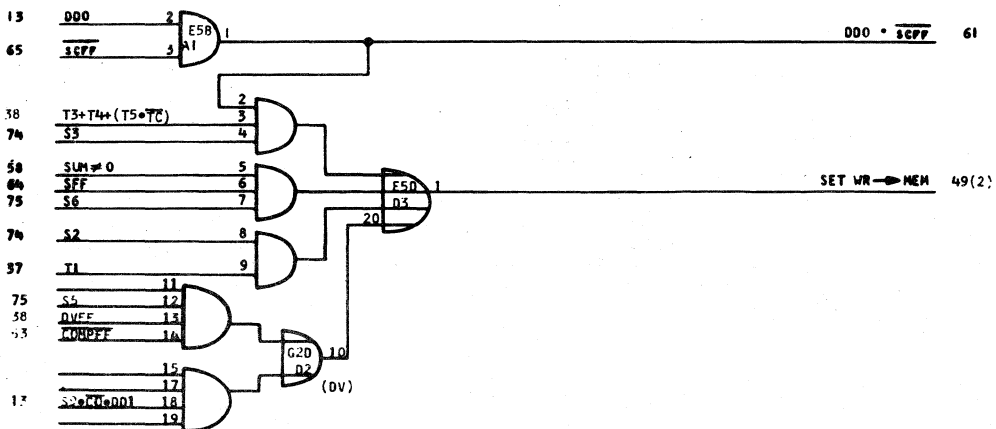
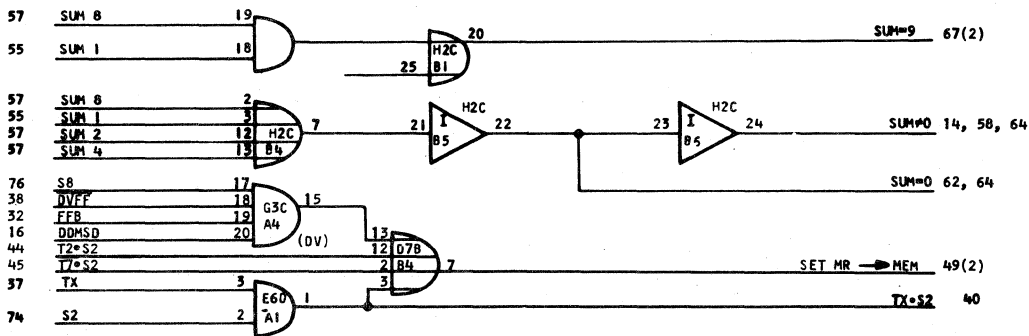
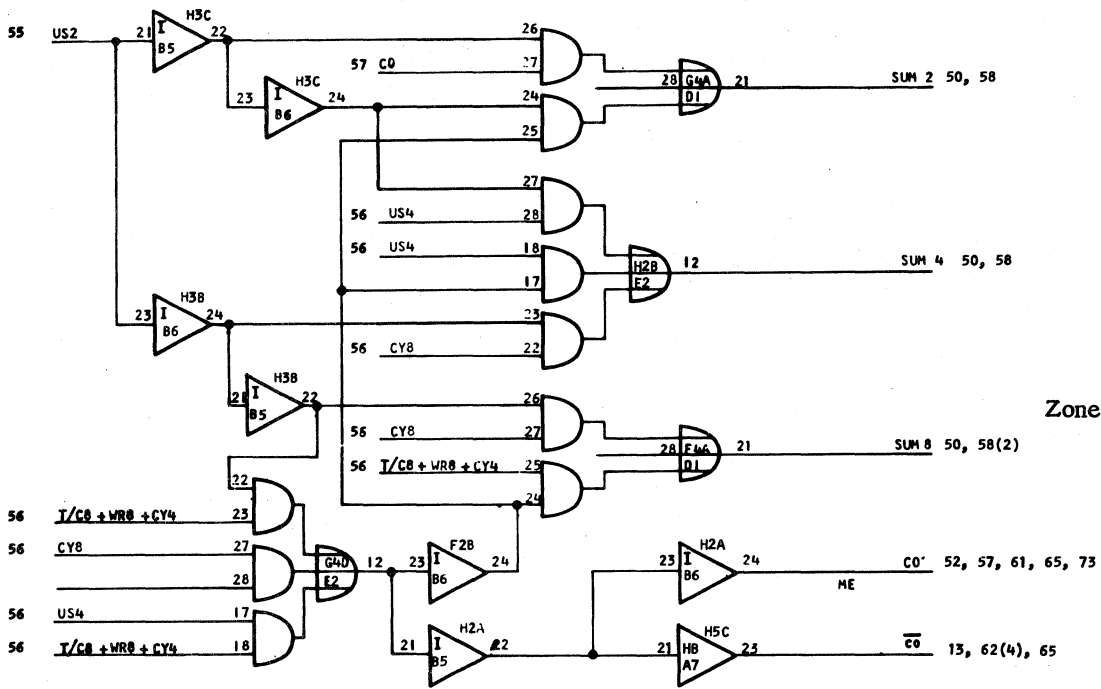


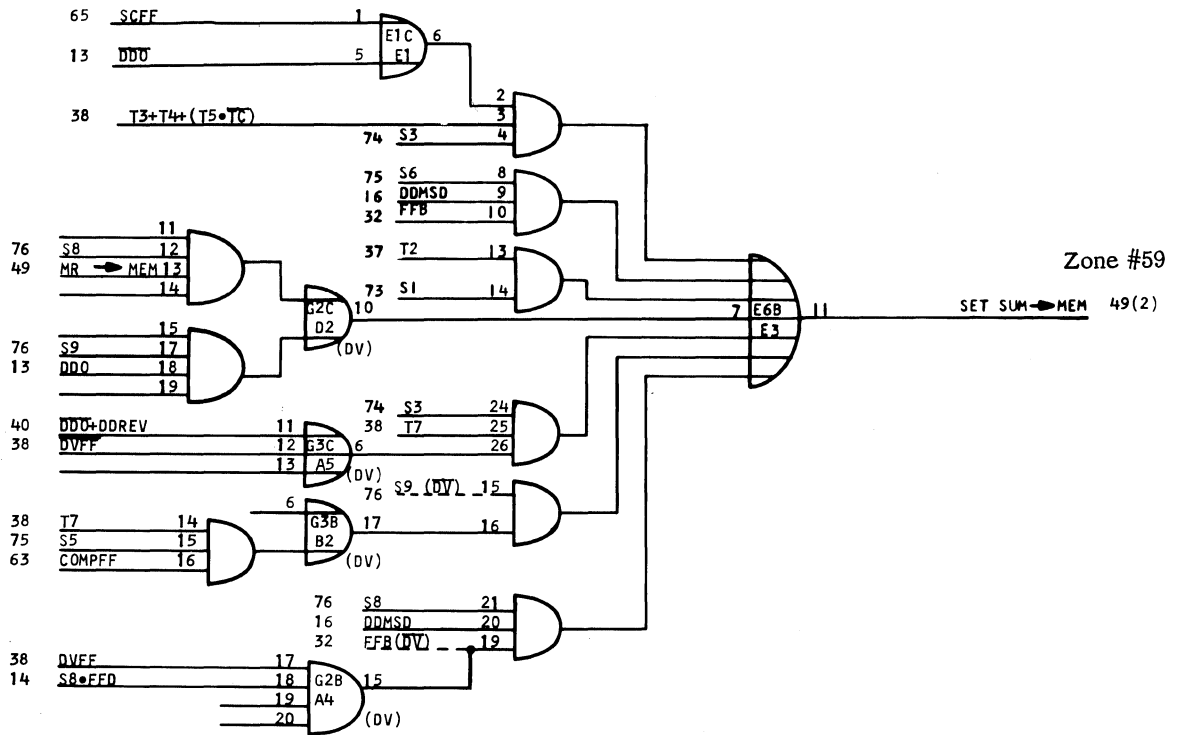
Zone #55



Zone #56

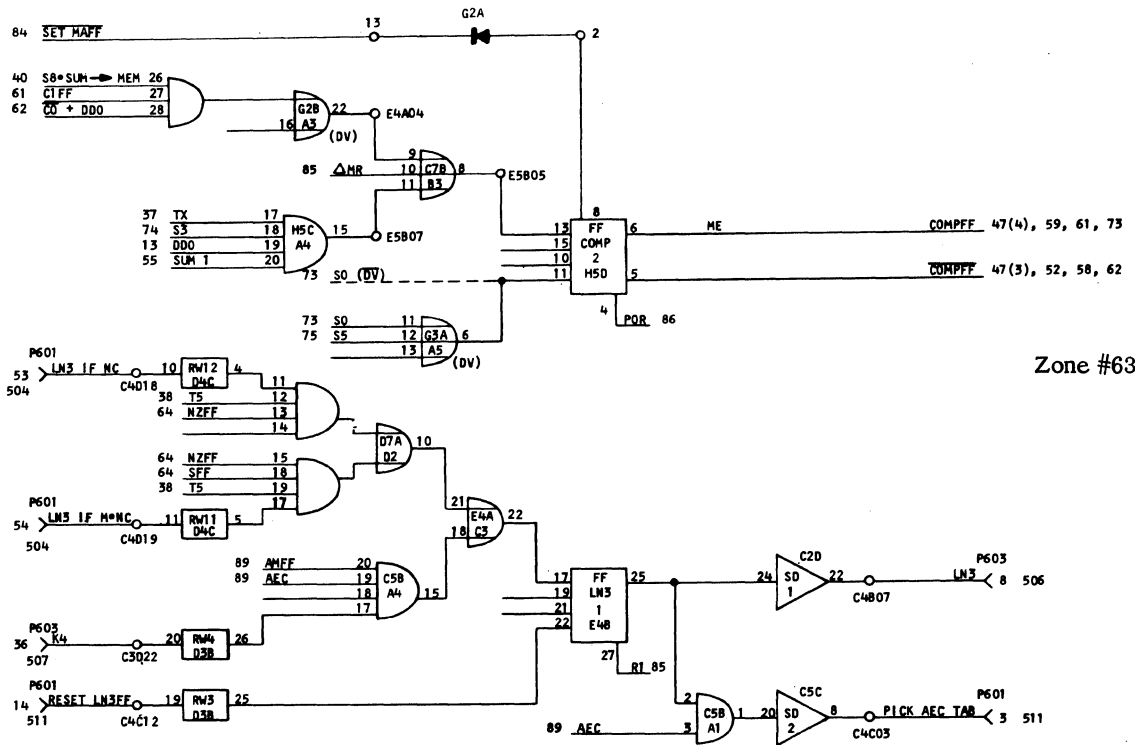




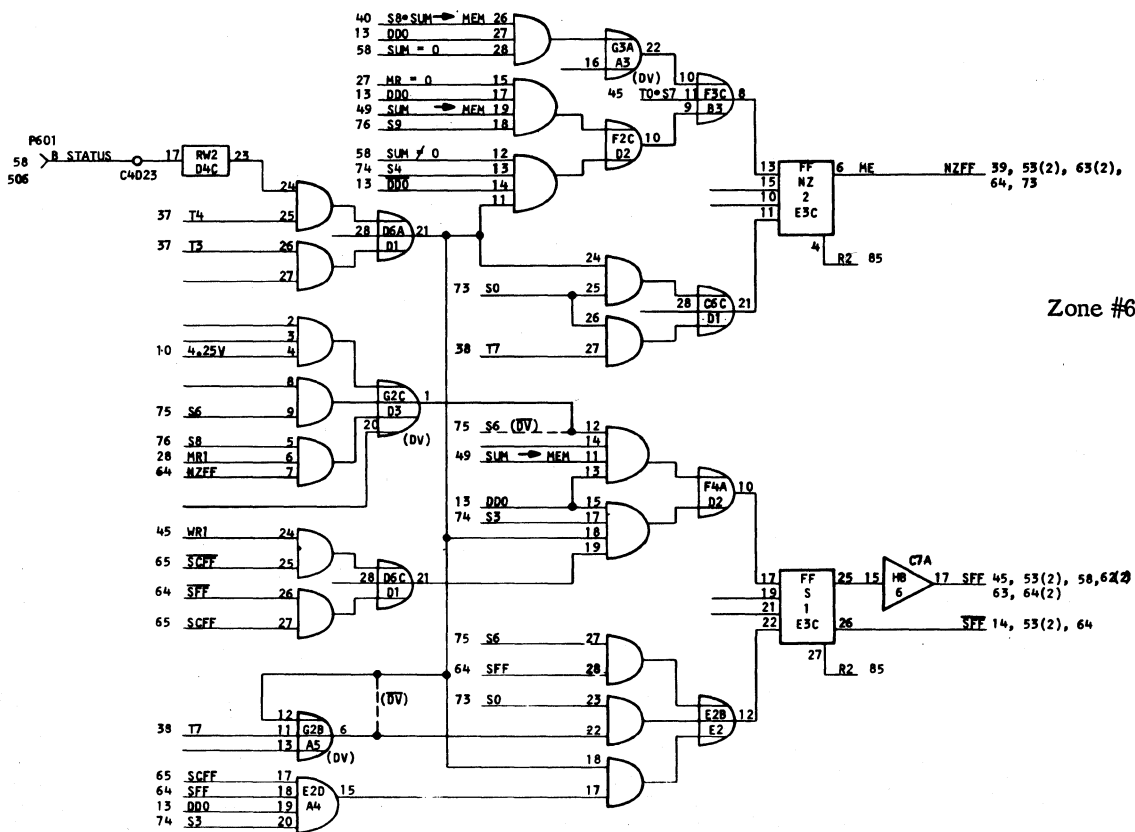


Zone #59

Zone #60

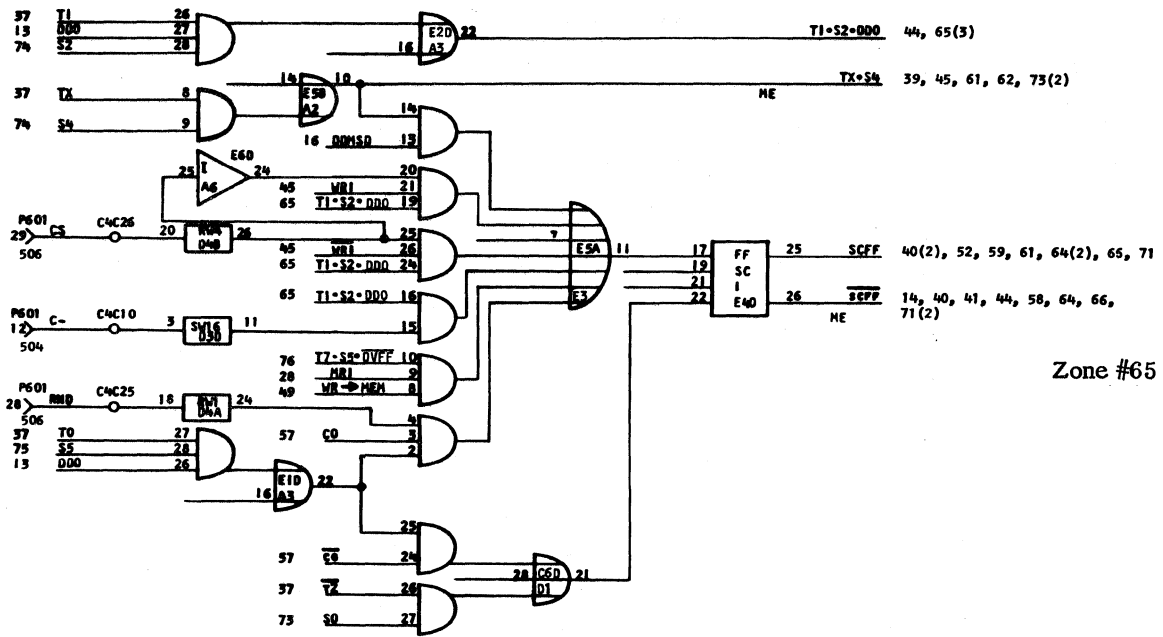


Zone #63

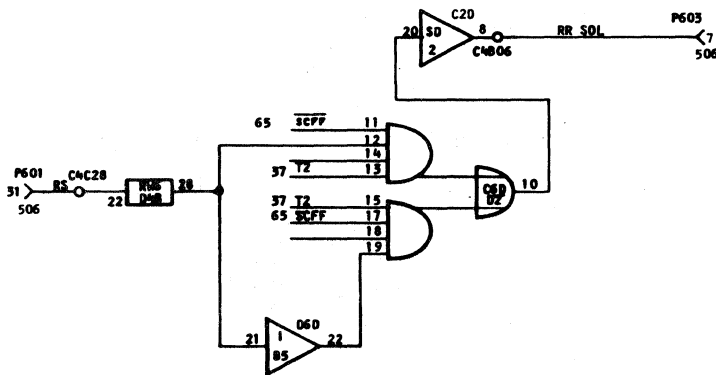


Zone #64

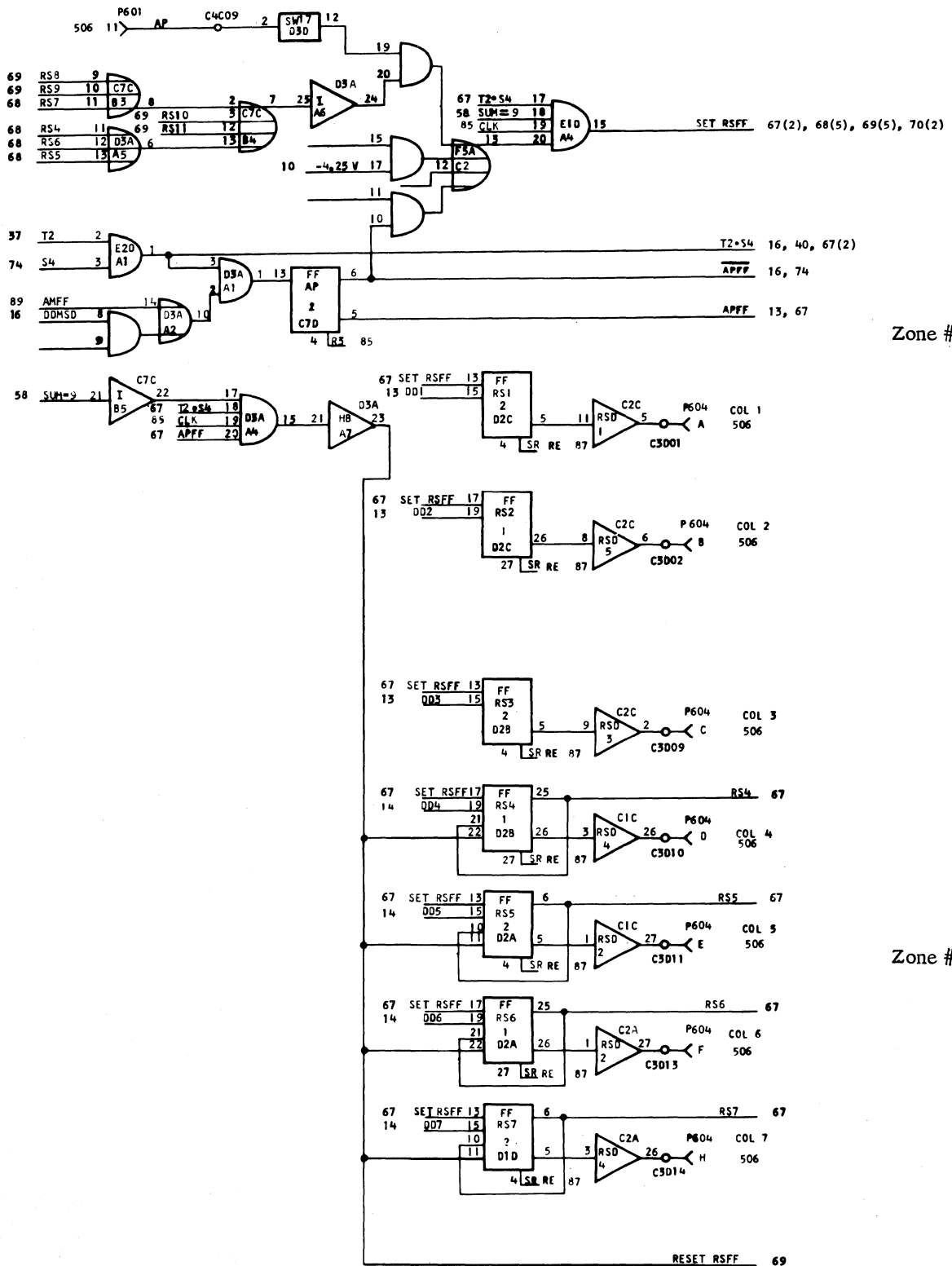
Ref. Page #132



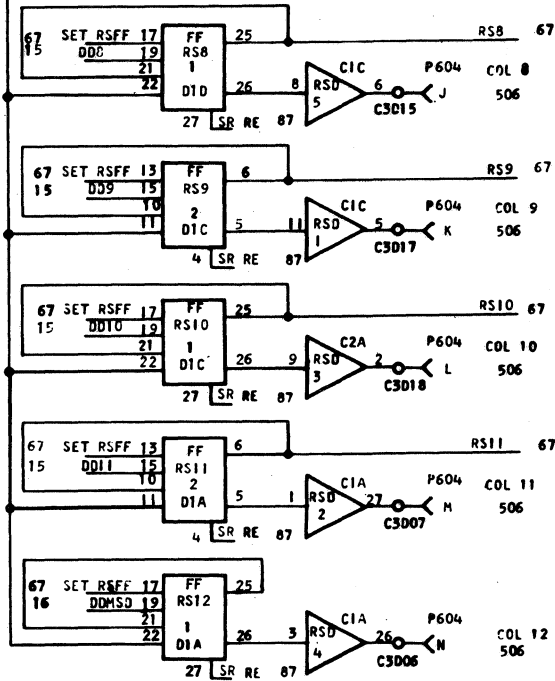
Zone #65



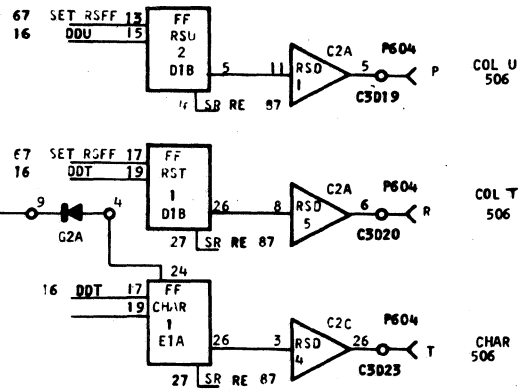
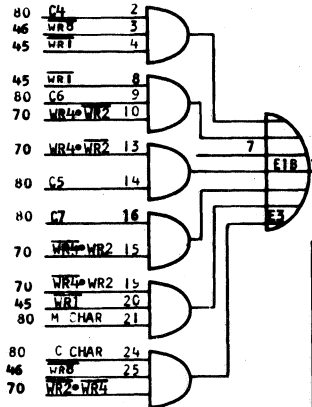
Zone #66



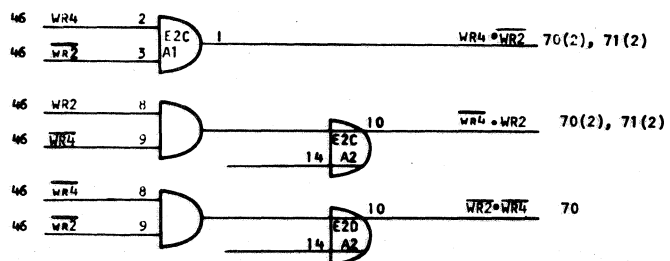
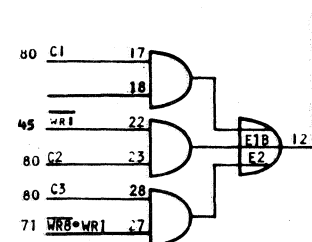
68 RESET RSFF

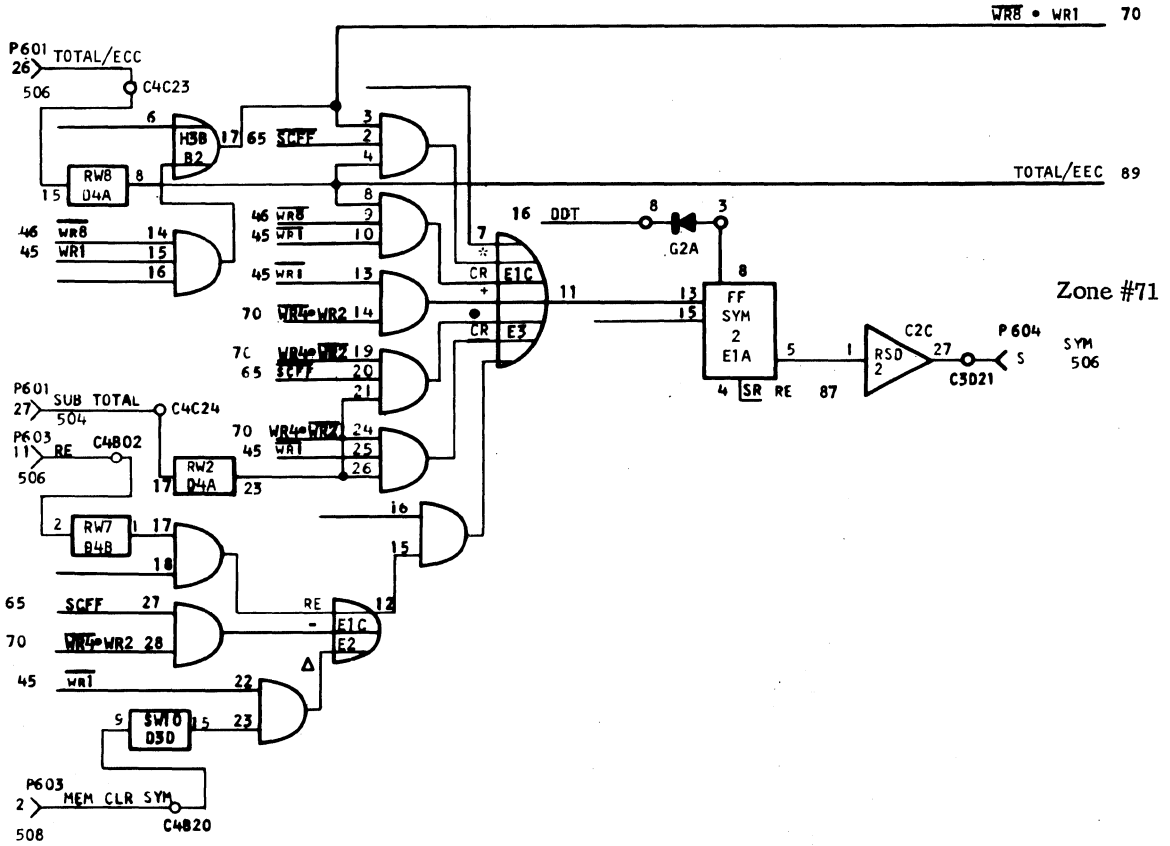


Zone #69



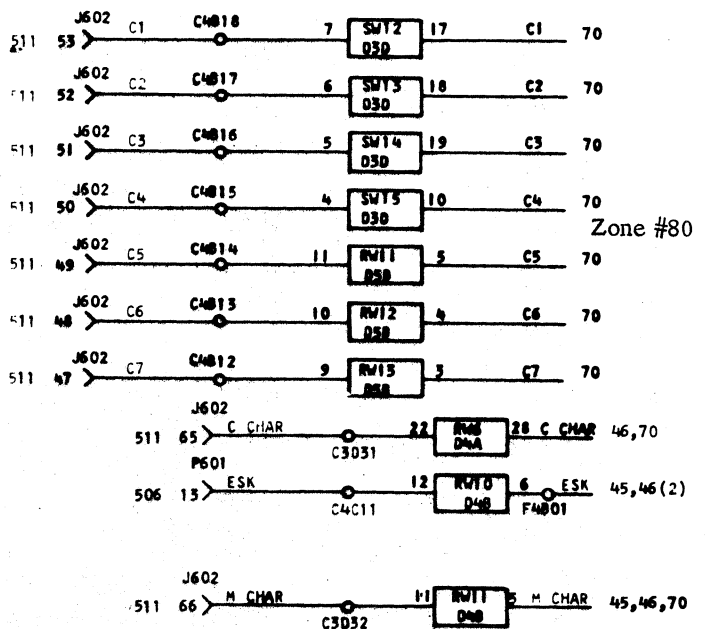
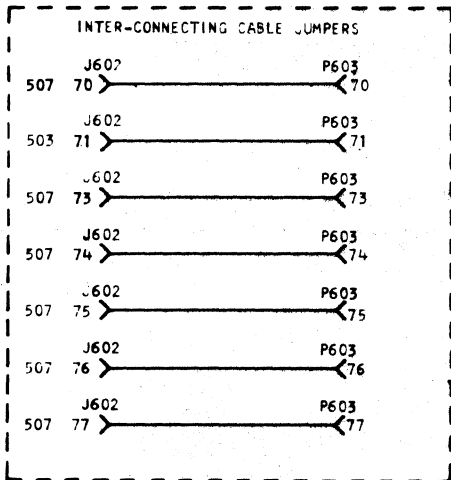
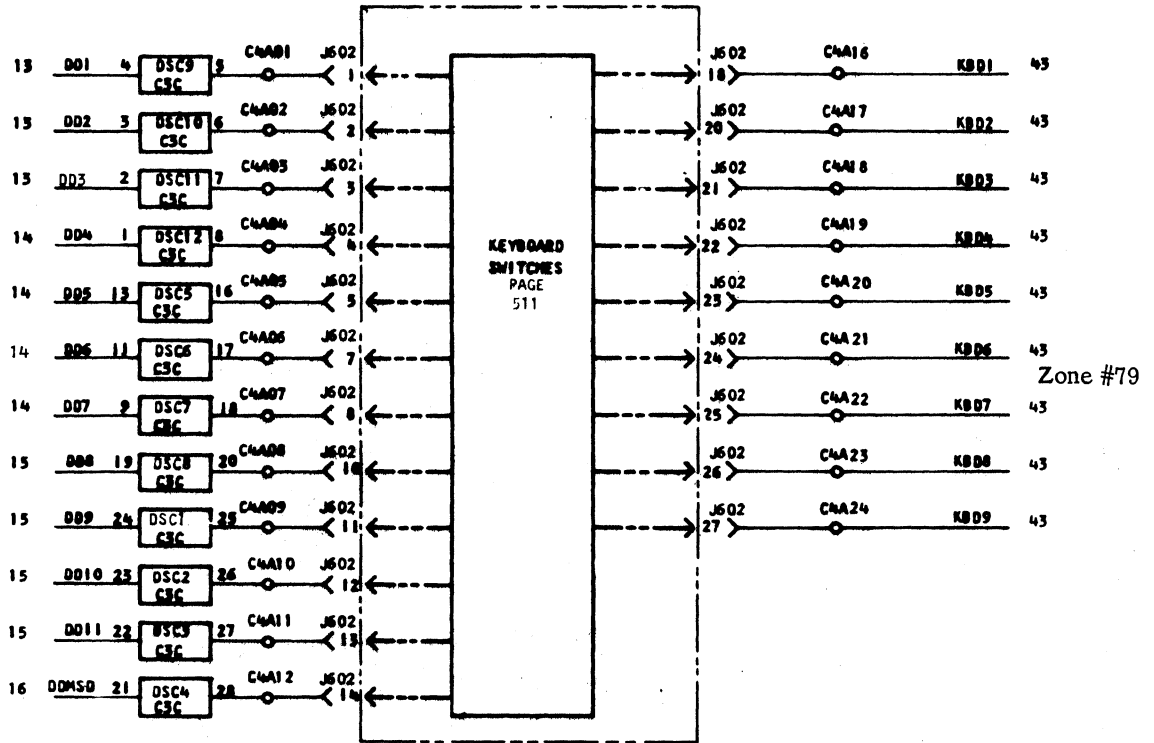
Zone #70



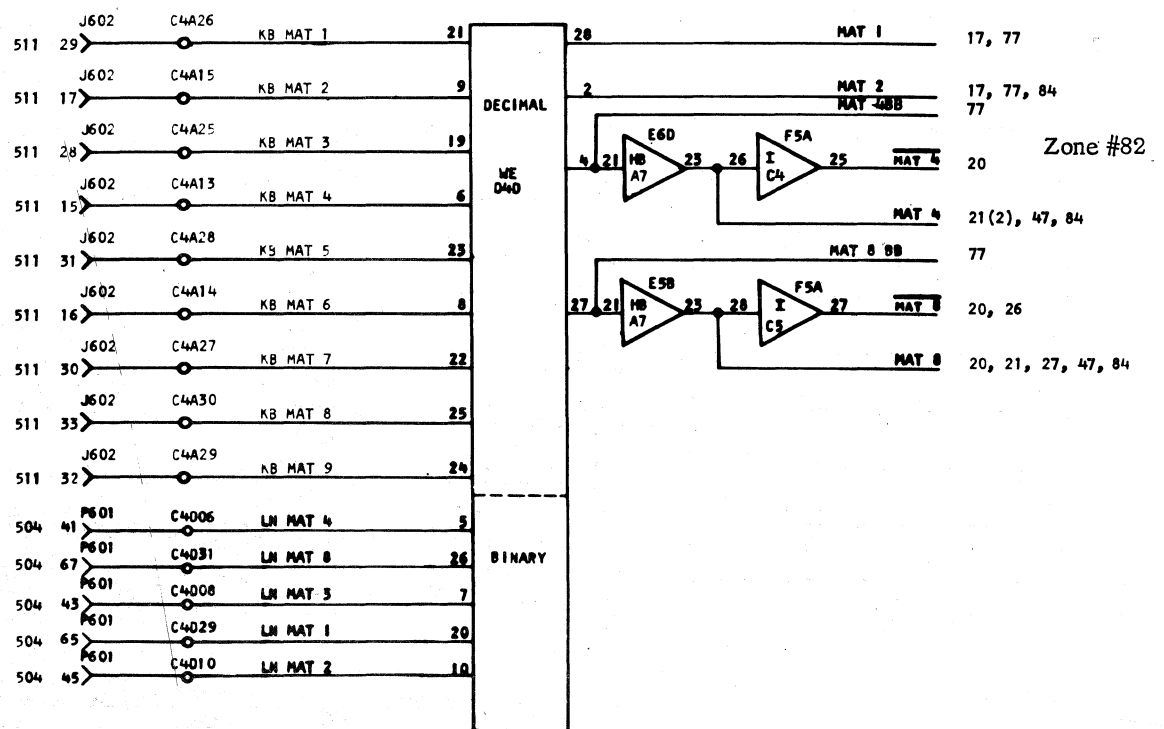
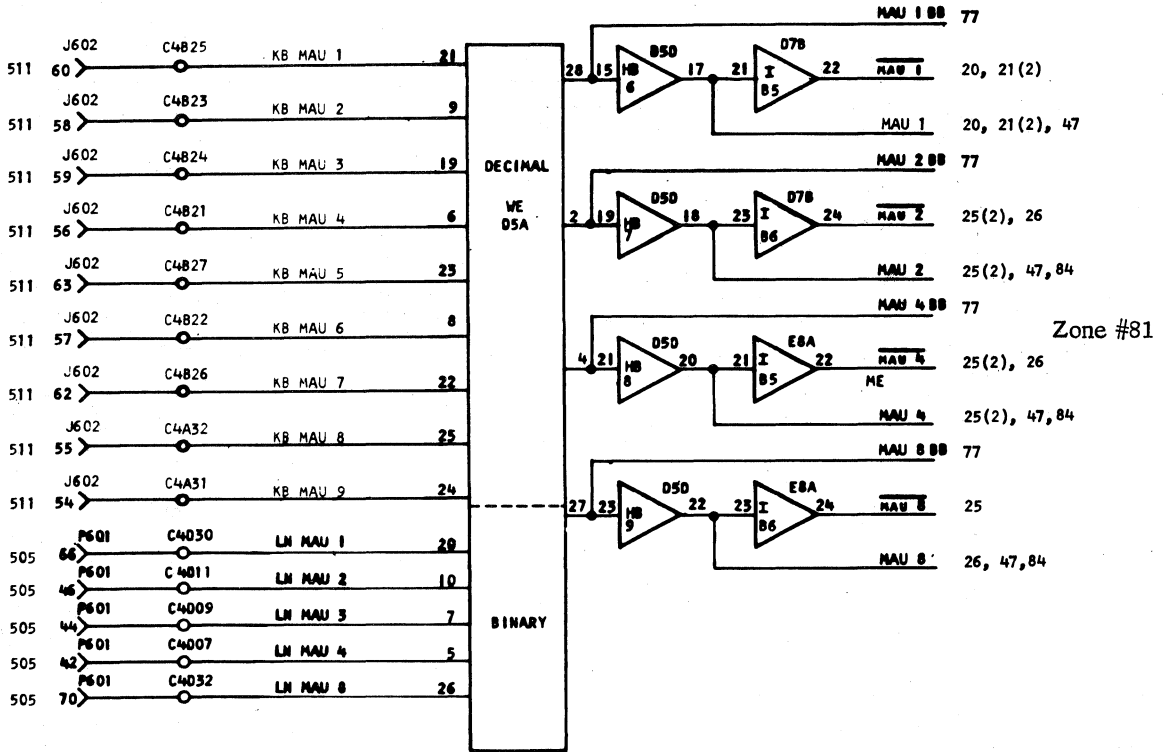


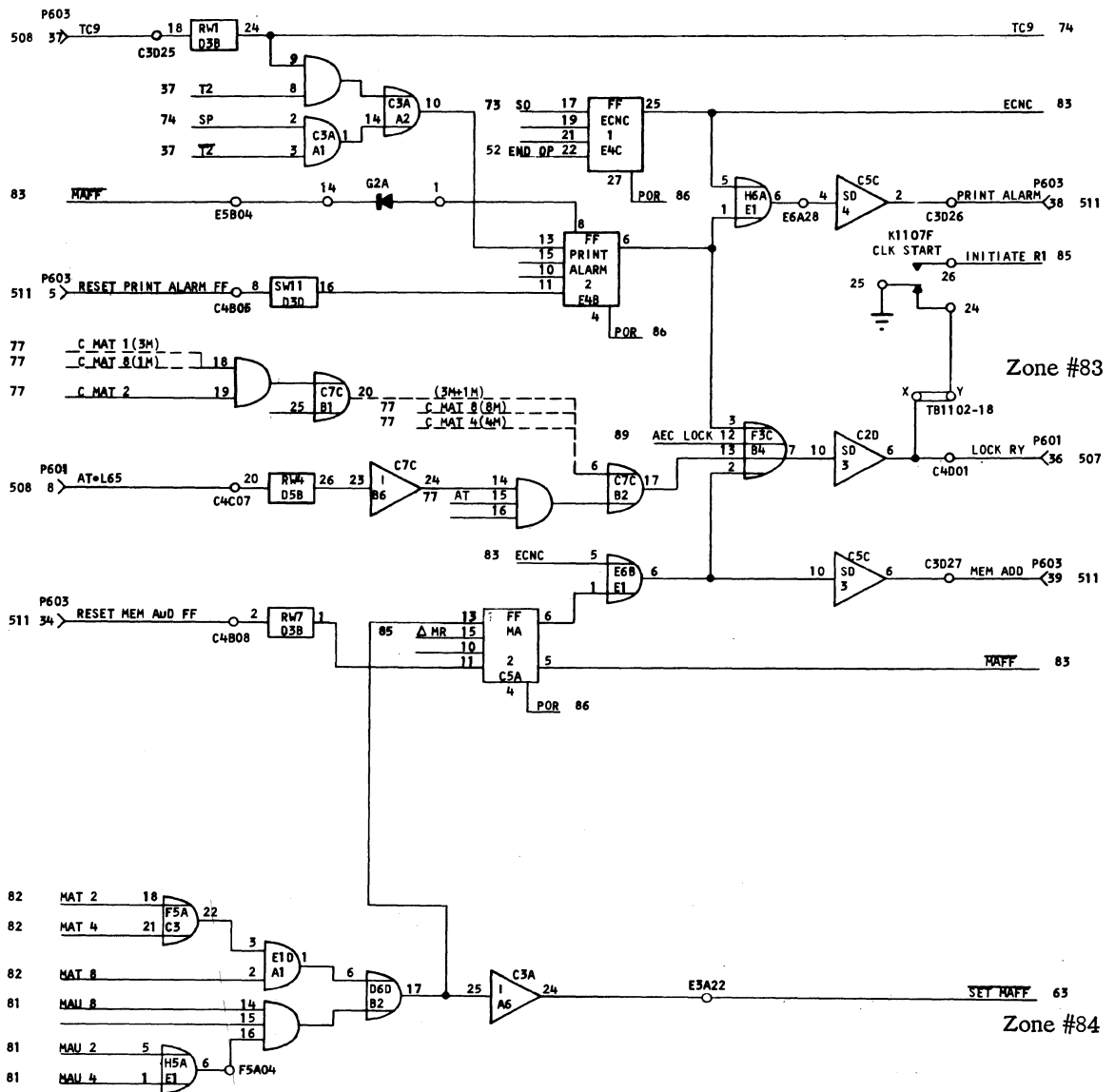
Zone #71

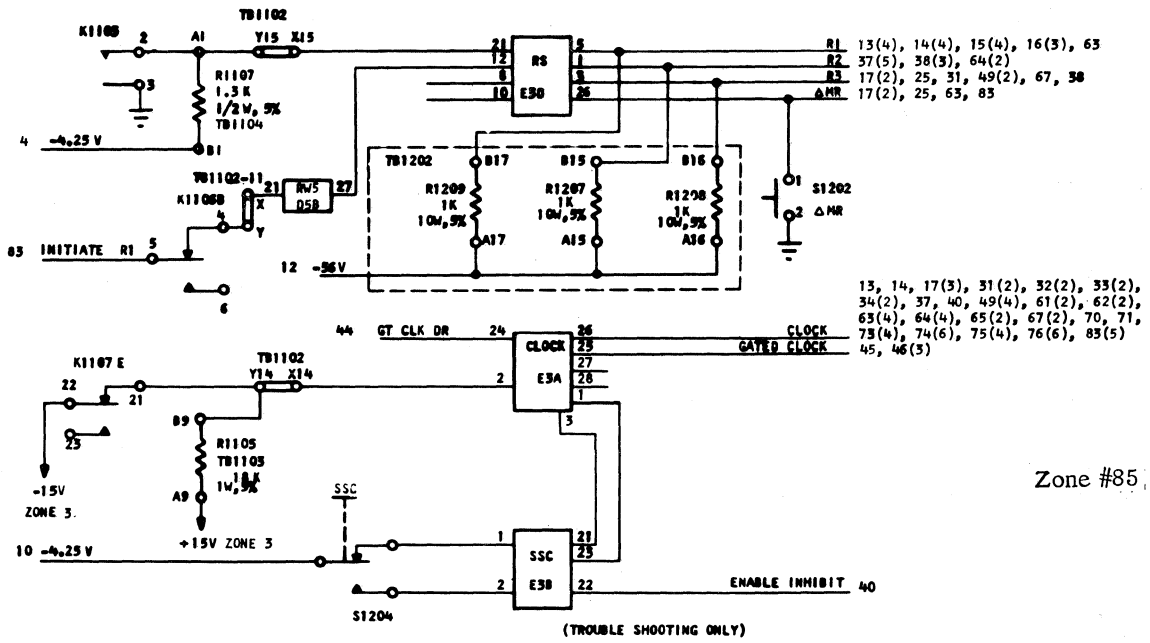
Zone #72



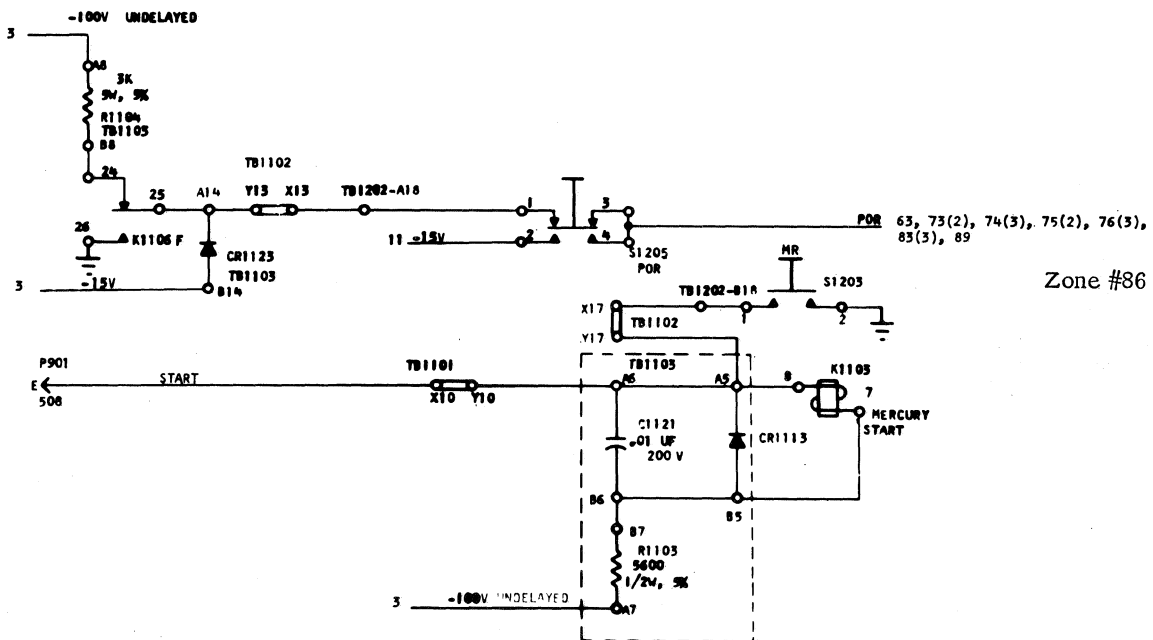
Ref. Page #140



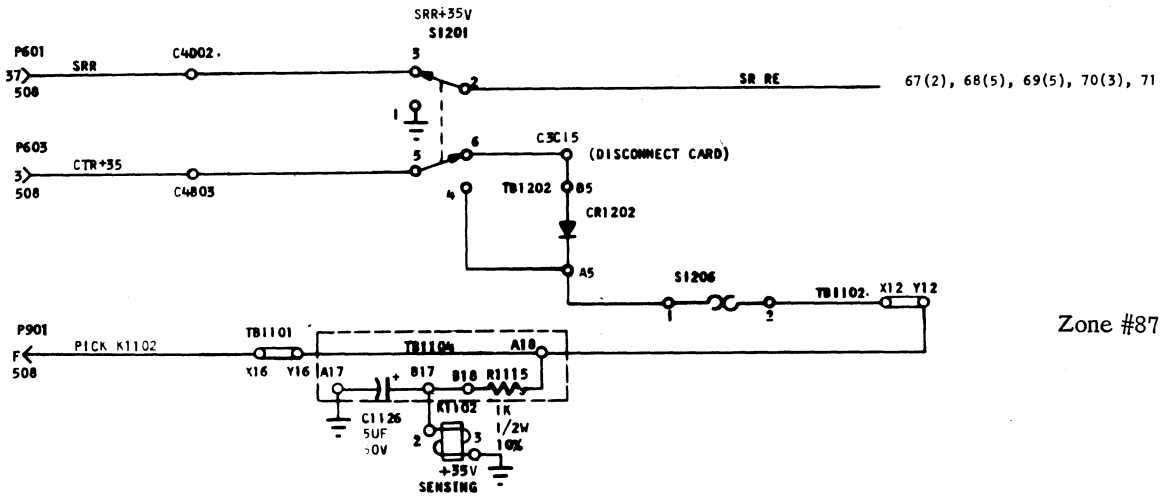




Zone #85

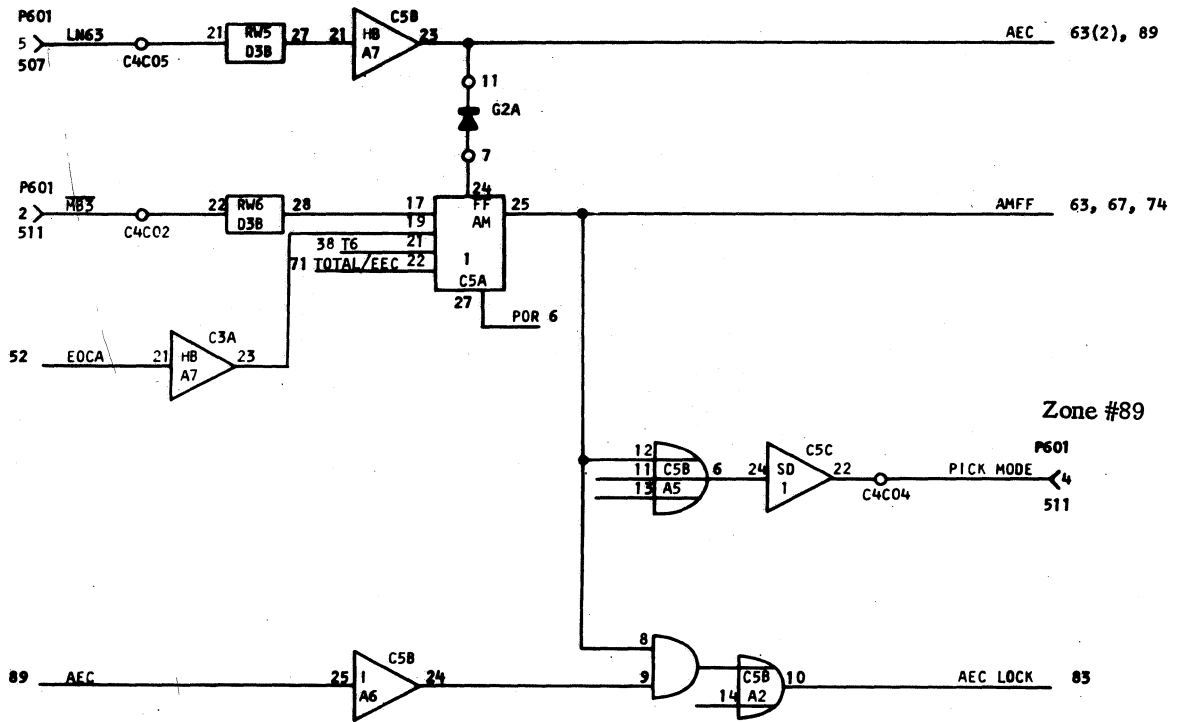


Zone #86



Zone #87

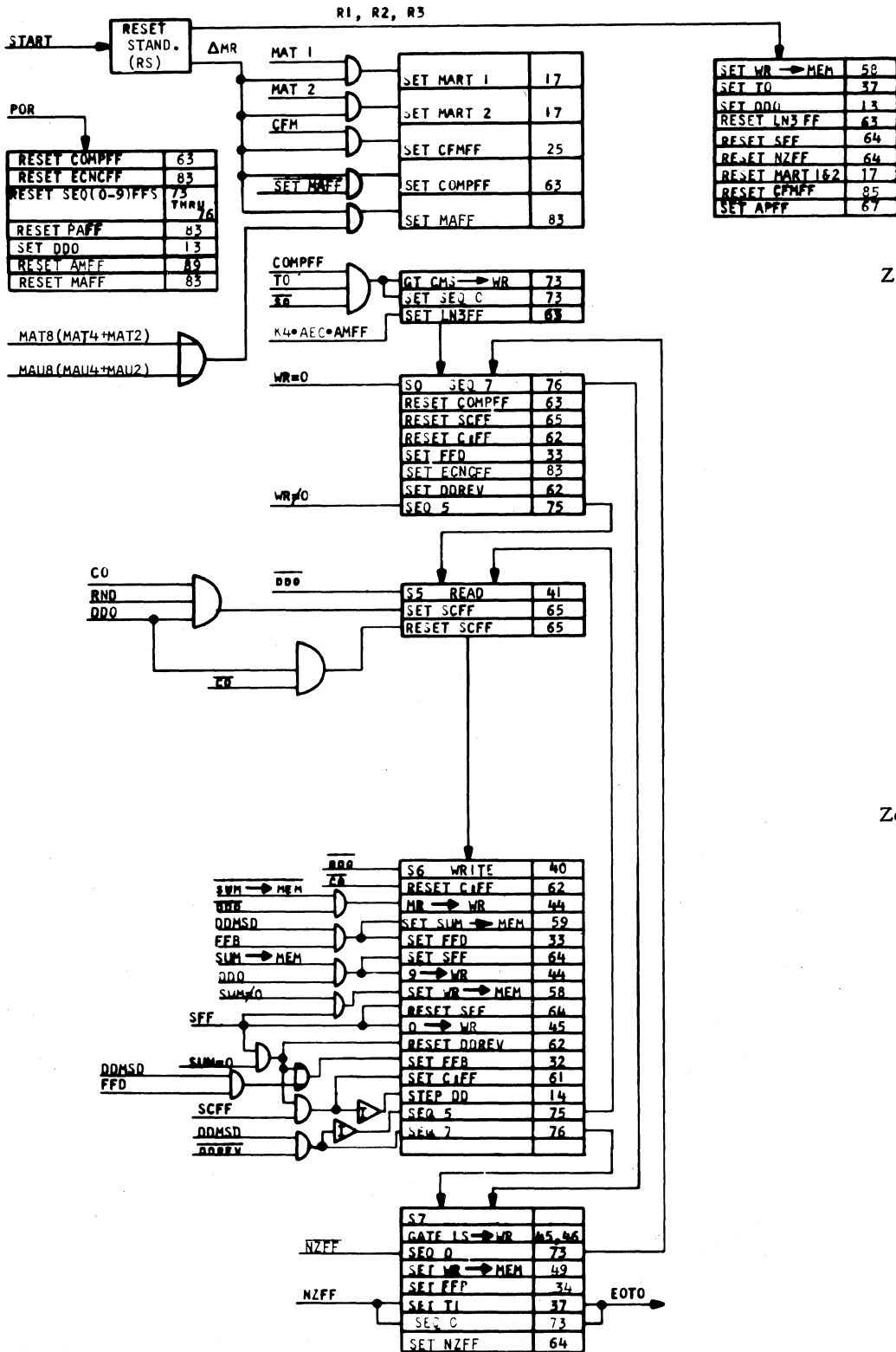
Zone #88



Zone #89

Zone #90

TIME T-0 SHIFT RIGHT OR SHIFT RIGHT & ROUND



Zone #91

Zone #92

TIME T-1 TRANSFER LOGIC

| INITIAL CONDITIONS | |
|--------------------|----|
| FFP | 34 |
| DDO | 13 |
| T1 | 37 |
| | |
| | |
| | |

EOTO

| | | |
|---------|--------------|----|
| PRINT A | S0 SET FFA | 31 |
| PRINT B | SET FFB | 32 |
| PRINT C | SET FFC | 32 |
| STIGA | COUNT MANT | 17 |
| | RESET SCFF | 65 |
| | RESET C IFF | 62 |
| | RESET COMPFF | 63 |
| | | |
| | | |

Zone #93

| | | |
|-------------|---------|----|
| PK | S1 READ | 40 |
| MR → WR | 44 | 44 |
| GTKB → WR | 44 | 44 |
| SET FFP | 34 | 34 |
| SET C IFF | 61 | 61 |
| RESET DOREV | 62 | 62 |
| | | |
| | | |

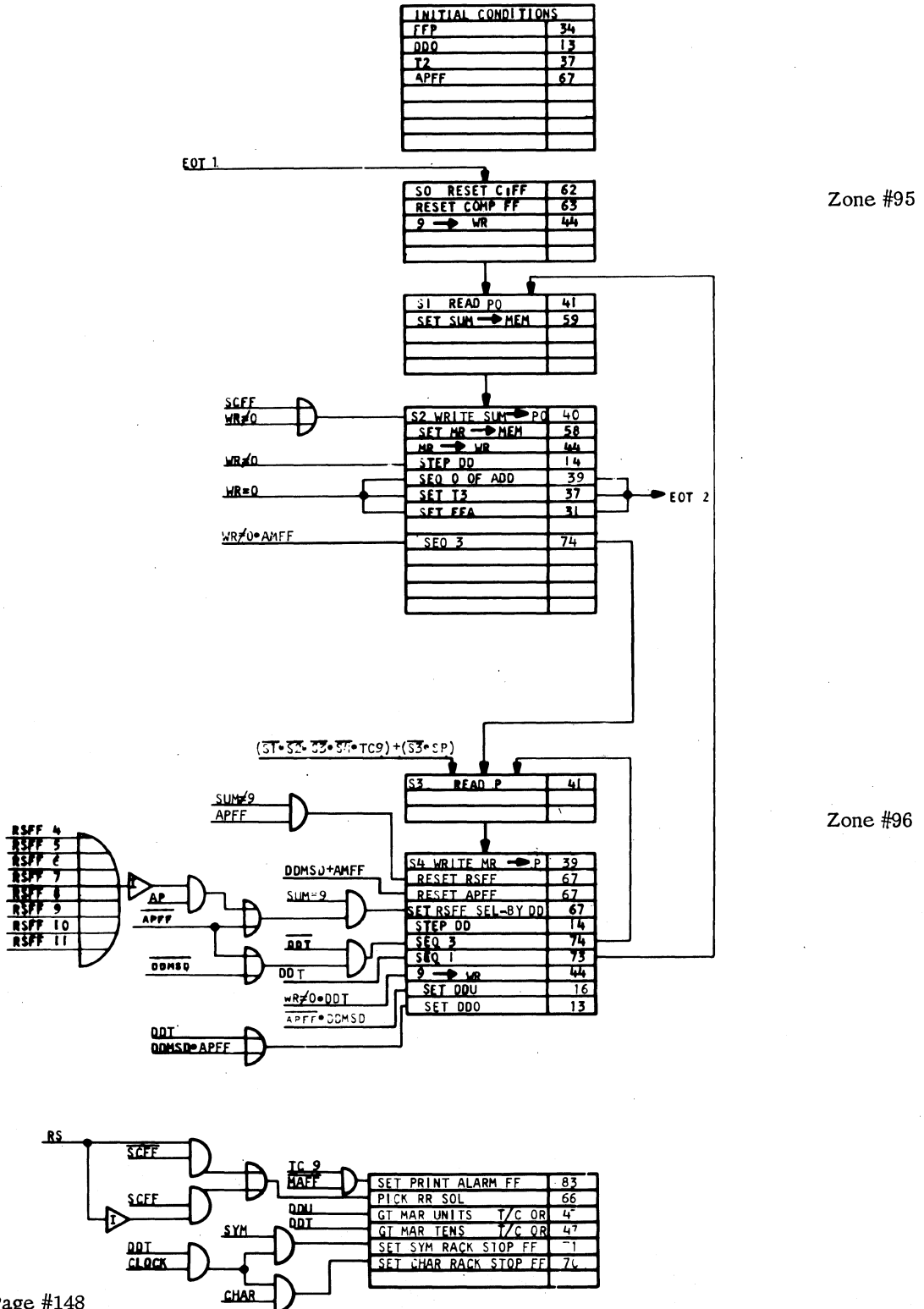
| | | |
|------|--------------|----|
| CS | S2 READ P | 40 |
| WR1 | SET SCFF | 65 |
| DDO | SET WR → MEM | 58 |
| WR1 | 9 → WR | 44 |
| C- | 1 → WR | 45 |
| DD10 | | |
| CNT | | |
| | | |
| | | |

Zone #94

| | | |
|---------|-----------------|----|
| QDC-6 | S3 WRITE WR → P | 40 |
| PRINT A | SET FFA | 31 |
| PRINT B | SET FFB | 32 |
| PRINT C | SET FFC | 32 |
| | 0 → WR | 45 |
| | | |
| | | |
| | | |

| | | |
|-------|---------------|----|
| DDO | S4 WRITE WR | 40 |
| C IFF | STEP DD | 14 |
| | SET I | 73 |
| | RESET C IFF | 62 |
| | | |
| DDMSD | SET FFP | 34 |
| | SET 0 OF PRIM | 39 |
| | SET T2 | 37 |
| | | |
| | | |

TIME T-2 PRINT LOGIC

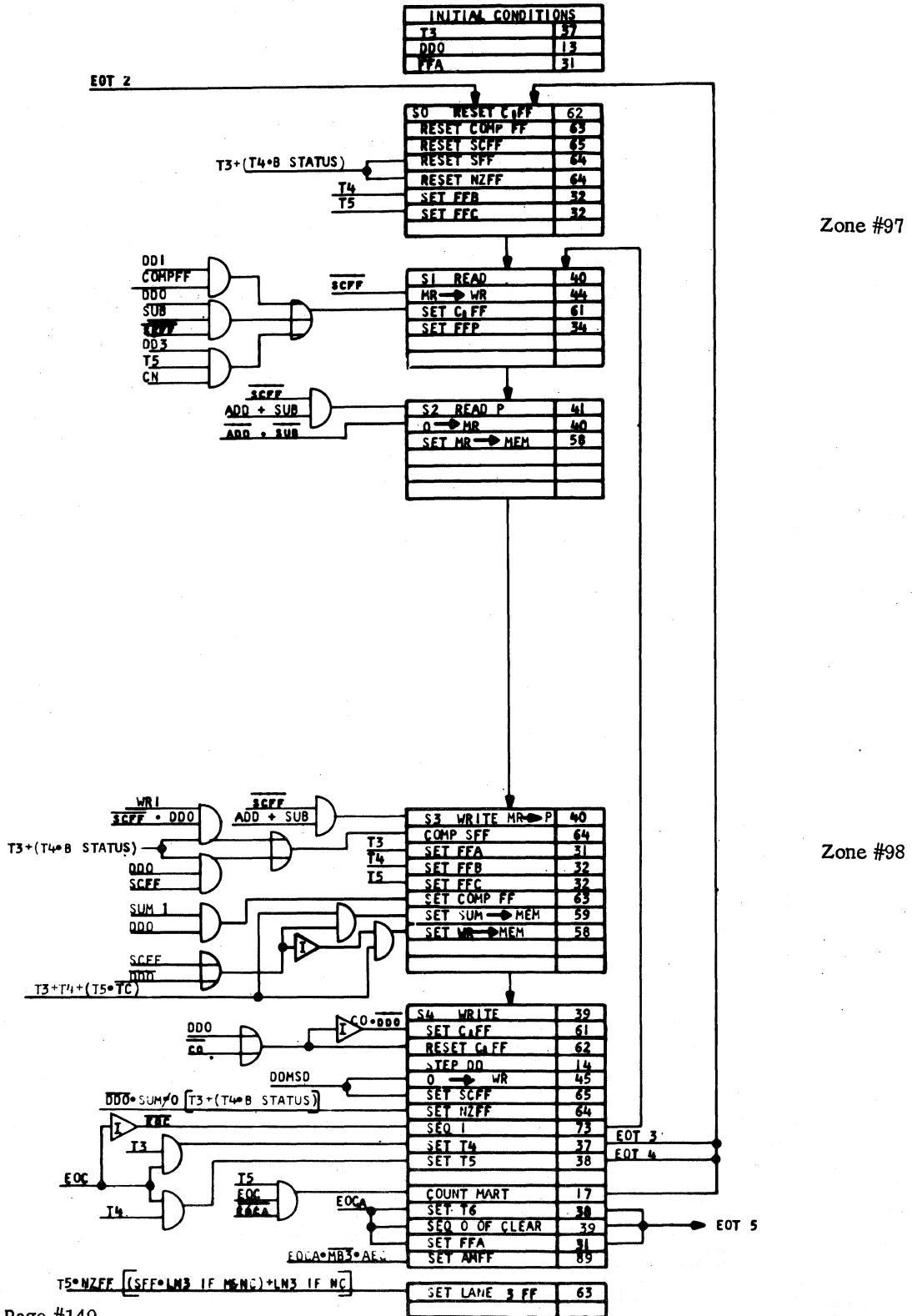


Zone #95

Zone #96

Ref. Page #148

TIME T-3, 4 & 5 ADD OR SUB. A, B OR C LOGIC



TIME T-6 CLEAR LOGIC

| INITIAL CONDITIONS | |
|--------------------|----|
| FFA | 31 |
| DDO | 13 |
| T 6 | 38 |
| | |
| | |

EOT5

| | | |
|----|---------------|----|
| S0 | RESET C IFF | 62 |
| | RESET SCFF | 65 |
| | RESET COMP FF | 63 |
| | | |
| | | |

Zone #99

CLR A

| | | |
|----|---------|----|
| S1 | READ A | 41 |
| | SET FEB | 32 |
| | | |
| | | |

CLR B

| | | |
|----|---------|----|
| S2 | READ B | 41 |
| | SET FFC | 32 |
| | | |
| | | |

CLR C

| | | |
|----|---------|----|
| S3 | READ C | 41 |
| | SET FFD | 33 |
| | | |
| | | |

CLR D + (DDO * MUL) + DIV

DDMSD

DDMSD * (DIV + MUL)

DDMSD * DIV * MUL

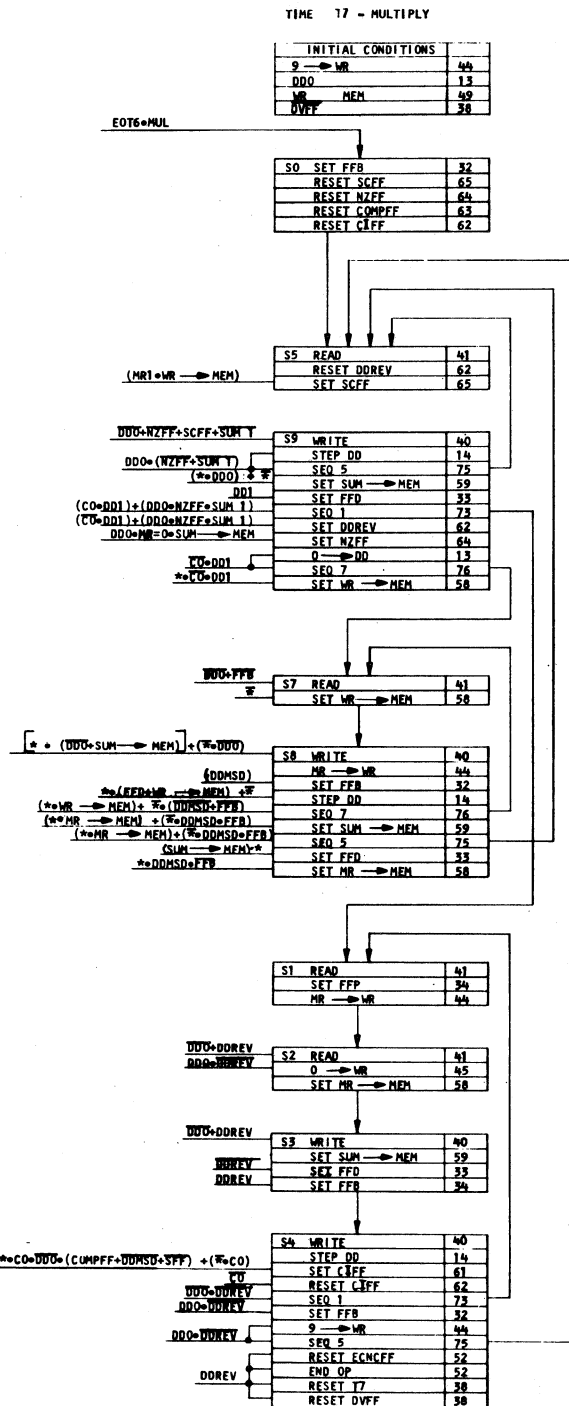
DDMSD * TOTAL / ECC

| | | |
|----|---------------------|----|
| S4 | READ D | 41 |
| | SET FFA | 31 |
| | SEQ 1 | 73 |
| | SET T7 | 38 |
| | SEQ 0 OF MULT + DIV | 39 |
| | STEP DD | 14 |
| | END OP | 52 |
| | RESET ECNCF | 52 |
| | RESET AMFF | 89 |

EOT6 * (MUL + DIV)

Zone #100

| | | |
|--------|-----|----|
| SET WR | MEM | 58 |
| 9 | WR | 44 |
| | | |

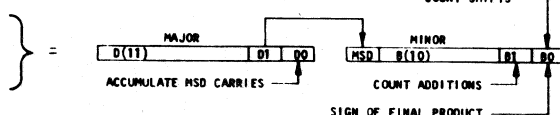


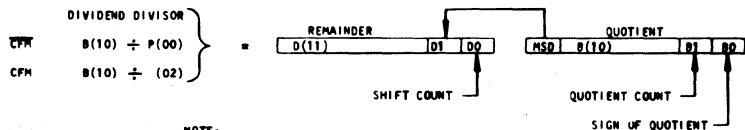
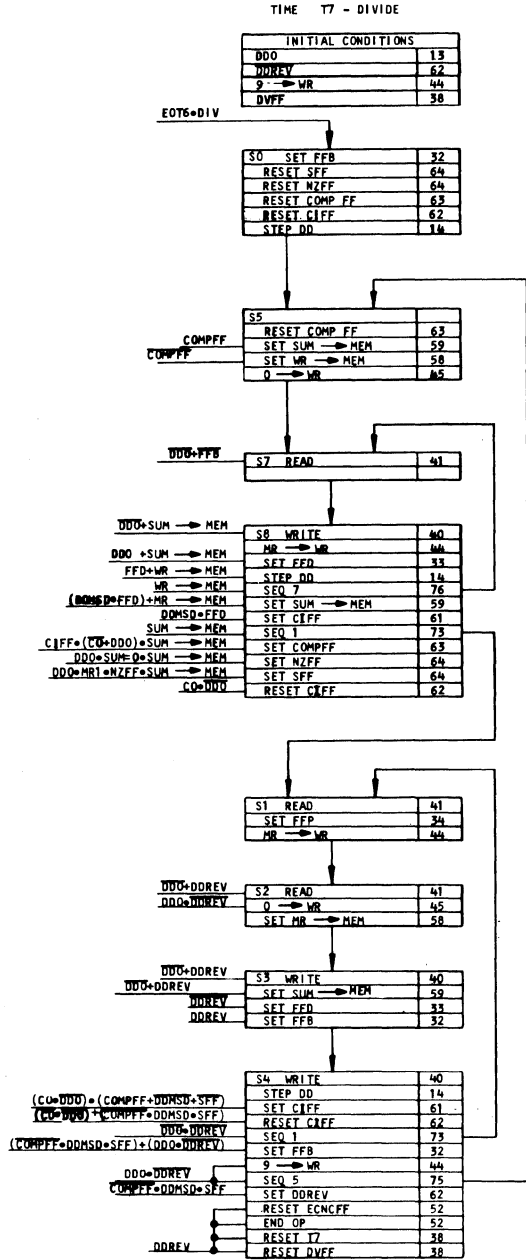
Zone #101

Zone #102

* MACHINE WITH DIVIDE OPTION
 * MACHINE WITHOUT DIVIDE OPTION

| | | | | |
|-----|-------------|---|------------|--|
| | MULTPLICAND | | MULTIPLIER | |
| CFR | P(00) | x | B(10) | |
| CFM | (02) | x | B(10) | |





NOTE:
 DIVISION BY ZERO:
 1. QUOTIENT (Q) IS ZERO. SIGN IS RESULT OF COMPARISON.
 2. REMAINDER (D) EQUALS ORIGINAL DIVIDEND(B). SIGN IS PLUS.

| CARD LOC | TYPE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | FEATURE | TIE POINTS PIN/ZONE | |
|----------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------------------|-------------|
| E8A | B | 45 | 26 | 32 | 34 | 81 | 81 | | | | | | | | | | | | | | 27/27 | |
| E8B | E | 13 | 26 | 33 | | | | | | | | | | | | | | | | | | |
| E8C | E | 33 | 20 | 32 | | | | | | | | | | | | | | | | | | |
| E8D | E | 31 | 20 | 31 | | | | | | | | | | | | | | | | | | |
| F1A | FF | 76 | 76 | | | | | | | | | | | | | | | | | | | |
| F1B | FF | 76 | 75 | | | | | | | | | | | | | | | | | | | |
| F1C | FF | 75 | 74 | | | | | | | | | | | | | | | | | | | |
| F1D | FF | 74 | 74 | | | | | | | | | | | | | | | | | | | |
| F2A | FF | 73 | 73 | | | | | | | | | | | | | | | | | | | |
| F2B | B | 73 | 73 | 37 | 73 | 73 | 57 | | | | | | | | | | | | | | | |
| F2C | D | 73 | 64 | 76 | | | | | | | | | | | | | | | | | | |
| F2D | DC | 11 | 11 | 7 | 7 | 10 | 10 | | | | | | | | | | | | | | | |
| F3A | HB | 73 | 74 | 74 | 74 | 75 | 75 | 76 | 76 | 73 | | | | | | | | | | | | 26/43 |
| F3B | HB | 37 | 37 | 45 | 37 | 37 | 38 | 38 | 38 | 37 | 52 | | | | | | | | | | | 26/43 |
| F3C | B | 40 | 45 | 64 | 83 | 14 | 14 | | | | | | | | | | | | | | | 26/43 |
| F3D | FF | 46 | 46 | | | | | | | | | | | | | | | | | | | 20/43 |
| F4A | D | 57 | 64 | 74 | | | | | | | | | | | | | | | | | | |
| F4B | B | 44 | 44 | 33 | 44 | 44 | 44 | | | | | | | | | | | | | | | 04/45 01/80 |
| F4C | B | 44 | 26 | 22 | 19 | 53 | 53 | | | | | | | | | | | | | | | |
| F4D | FF | 46 | 45 | | | | | | | | | | | | | | | | | | | 20/53 |
| F5A | C | 21 | 67 | 84 | 82 | 82 | | | | | | | | | | | | | | | | 04/81 |
| F5B | C | 19 | 46 | 23 | 46 | 50 | | | | | | | | | | | | | | | | 04/13 |
| F5C | C | 19 | 46 | 22 | 46 | 50 | | | | | | | | | | | | | | | | |
| F5D | C | 19 | 46 | 22 | 50 | 46 | | | | | | | | | | | | | | | | |
| F6A | C | 19 | 45 | 22 | 45 | 49 | | | | | | | | | | | | | | | | 08/13 14/14 |
| F6B | DC | 11 | 11 | 7 | 7 | 10 | 10 | | | | | | | | | | | | | | | |
| F6C | MD | 27 | 23 | 27 | 23 | | | | | | | | | | | | | | | | | |
| F6D | MD | 20 | 20 | 20 | 20 | | | | | | | | | | | | | | | | | |
| F7A | MD | 26 | 26 | 26 | 26 | | | | | | | | | | | | | | | | | |
| F7B | MD | 26 | 23 | 26 | 23 | | | | | | | | | | | | | | | | | |
| F7C | MD | 23 | 22 | 23 | 22 | | | | | | | | | | | | | | | | | |
| F7D | MD | 21 | 21 | 21 | 21 | | | | | | | | | | | | | | | | | |
| F8A | MD | 21 | 21 | 21 | 21 | | | | | | | | | | | | | | | | | (M+1M) |
| F8B | MEMORY | 28 | | | | | | | | | | | | | | | | | | | | (M+1M) |
| F8C | | | | | | | | | | | | | | | | | | | | | | |
| F8D | | | | | | | | | | | | | | | | | | | | | | |
| G1A | FF | 38 | 38 | | | | | | | | | | | | | | | | | | | |
| G1B | FF | 38 | 37 | | | | | | | | | | | | | | | | | | | |
| G1C | FF | 37 | 37 | | | | | | | | | | | | | | | | | | | |
| G1D | FF | 37 | 37 | | | | | | | | | | | | | | | | | | | |
| G2A | COMP | | 89 | 75 | 70 | 71 | 63 | 83 | | | | | | | | | | | | | | |
| G2B | A | 14 | 14 | 63 | 59 | 64 | 61 | | | | | | | | | | | | | | | (DV) |
| G2C | D | 76 | 59 | 64 | | | | | | | | | | | | | | | | | | (DV) |
| G2D | D | 62 | 58 | 61 | | | | | | | | | | | | | | | | | | (DV) |
| G3A | A | 14 | 62 | 64 | 62 | 63 | 62 | | | | | | | | | | | | | | | (DV) |
| G3B | B | 40 | 59 | 52 | | 32 | 62 | | | | | | | | | | | | | | | (DV) |
| G3C | A | 45 | 75 | 69 | 58 | 59 | 61 | | | | | | | | | | | | | | | (DV) |
| G3D | A | | 61 | 61 | 64 | 64 | 65 | | | | | | | | | | | | | | | |
| G4A | D | 57 | 47 | 45 | | | | | | | | | | | | | | | | | | |
| G4B | D | 46 | 53 | 53 | | | | | | | | | | | | | | | | | | |
| G4C | D | 47 | 53 | 53 | | | | | | | | | | | | | | | | | | |
| G4D | E | 40 | 57 | 44 | | | | | | | | | | | | | | | | | | |
| G5A | B | 40 | 52 | 52 | 19 | 40 | 40 | | | | | | | | | | | | | | | |
| G5B | E | 40 | 40 | 40 | | | | | | | | | | | | | | | | | | |
| G5C | D | 41 | 32 | 44 | | | | | | | | | | | | | | | | | | |
| G5D | A | 41 | 40 | 52 | 27 | 19 | 52 | 40 | | | | | | | | | | | | | | |
| G6A | E | 40 | 50 | 41 | | | | | | | | | | | | | | | | | | |
| G6B | E | 41 | 49 | 41 | | | | | | | | | | | | | | | | | | |
| G6C | MD | 25 | 25 | 25 | 25 | | | | | | | | | | | | | | | | | |
| G6D | MD | 25 | 25 | 25 | 25 | | | | | | | | | | | | | | | | | |
| G7A | MD | 26 | 22 | 26 | 22 | | | | | | | | | | | | | | | | | |
| G7B | MD | 20 | 20 | 20 | 20 | | | | | | | | | | | | | | | | | |
| G7C | MD | 22 | 22 | 22 | 22 | | | | | | | | | | | | | | | | | |
| G7D | MD | 49 | 50 | 50 | 50 | | | | | | | | | | | | | | | | | |
| G8A | MD | 27 | | 27 | | | | | | | | | | | | | | | | | | (1M) |
| G8B | MEMORY | 29 | | | | | | | | | | | | | | | | | | | | |
| G8C | | | | | | | | | | | | | | | | | | | | | | |
| G8D | | | | | | | | | | | | | | | | | | | | | | |
| H1A | IND | 73 | 73 | 74 | 74 | 74 | 75 | 75 | 76 | | | | | | | | | | | | | |
| H1B | IND | 37 | 38 | 38 | 49 | 49 | 61 | 76 | 76 | | | | | | | | | | | | | |
| H1C | IND | | 46 | 46 | | 34 | 21 | 32 | 33 | | | | | | | | | | | | | |
| H1D | IND | 13 | 16 | 16 | | | | | | | | | | | | | | | | | | |
| H2A | B | 76 | | 43 | 43 | 57 | 57 | | | | | | | | | | | | | | | |
| H2B | E | 39 | 57 | 39 | | | | | | | | | | | | | | | | | | |
| H2C | B | 58 | 76 | 56 | 58 | 58 | 58 | | | | | | | | | | | | | | | |
| H2D | D | 11 | | 11 | 7 | 7 | 10 | 10 | | | | | | | | | | | | | | |
| H3A | B | 37 | 73 | 56 | 45 | 56 | 56 | | | | | | | | | | | | | | | |
| H3B | B | 45 | 71 | 55 | 44 | 27 | 27 | | | | | | | | | | | | | | | |
| H3C | B | 62 | 62 | 52 | 62 | 27 | 27 | | | | | | | | | | | | | | | |
| H3D | B | 42 | 26 | 12 | 22 | 22 | | | | | | | | | | | | | | | | |
| LCC | TYPE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | FEATURE | TIE POINT | |
| CARD | | | | | | | | | | | | | | | | | | | | | | |

Zone #111

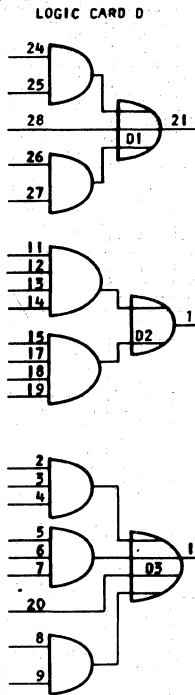
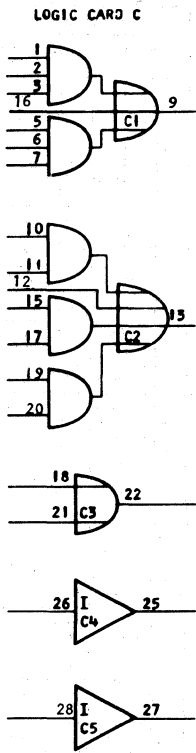
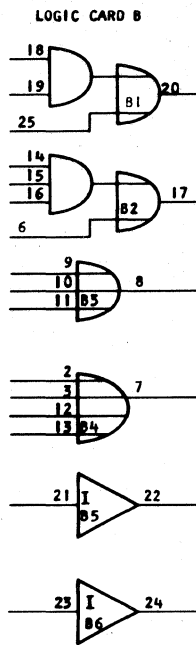
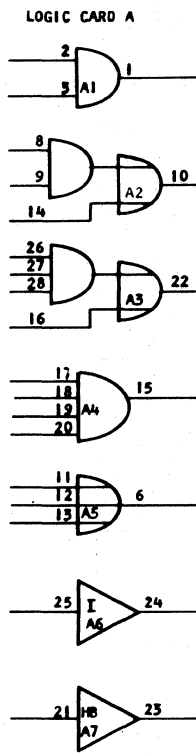
Zone #112

| CARD | | | | | | | | | | | | | | | | | TIE POINTS | | | | | |
|------|------|----|----|----|----|----|----|----|---|---|----|----|----|----|----|----|------------|----|----|---------|-----|------|
| LOC | TYPE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | FEATURE | PIN | LINE |
| H4A | C | 56 | 56 | 43 | 56 | 54 | | | | | | | | | | | | | | | | |
| H4B | C | 55 | 55 | | 55 | 55 | | | | | | | | | | | | | | | | |
| H4C | C | 55 | 55 | 40 | 55 | 55 | | | | | | | | | | | | | | | | |
| H4D | B | 21 | 52 | 52 | 41 | 56 | 56 | | | | | | | | | | | | | | | |
| H5A | F | 84 | 50 | 61 | | | | | | | | | | | | | | | | | | |
| H5B | F | 61 | 50 | 62 | | | | | | | | | | | | | | | | | | |
| H5C | A | 61 | 62 | 61 | 63 | 53 | 61 | 57 | | | | | | | | | | | | | | |
| H5D | FF | 61 | 63 | | | | | | | | | | | | | | | | | | | |
| H6A | F | 83 | 47 | 47 | | | | | | | | | | | | | | | | | | |
| H6B | DC | 11 | | 11 | 7 | 7 | 10 | 10 | | | | | | | | | | | | | | |
| H6C | C | 46 | 47 | 19 | 61 | 40 | | | | | | | | | | | | | | | | |
| H6D | C | 21 | 47 | 41 | 40 | 40 | | | | | | | | | | | | | | | | |
| H7A | NTA | 40 | | | | | | | | | | | | | | | | | | | | |
| H7B | MTR | 40 | | | | | | | | | | | | | | | | | | | | |
| H7C | MR | 28 | | | | | | | | | | | | | | | | | | | | |
| H7D | MR | 28 | | | | | | | | | | | | | | | | | | | | |
| H8A | MR | 28 | | | | | | | | | | | | | | | | | | | | |
| H8B | MR | 28 | | | | | | | | | | | | | | | | | | | | |
| H8C | | | | | | | | | | | | | | | | | | | | | | |
| H8D | | | | | | | | | | | | | | | | | | | | | | |

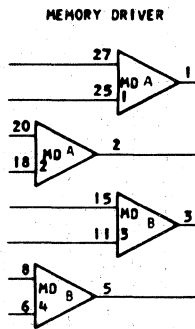
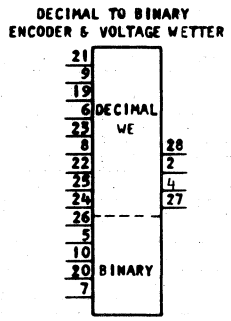
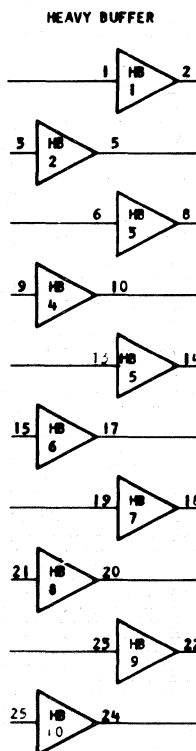
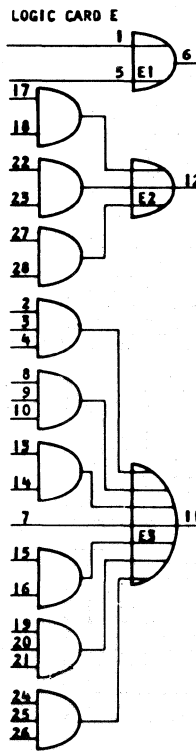
Zone #113

Zone #114

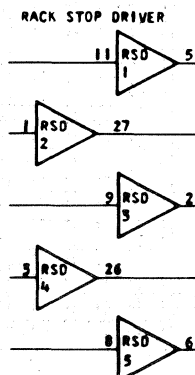
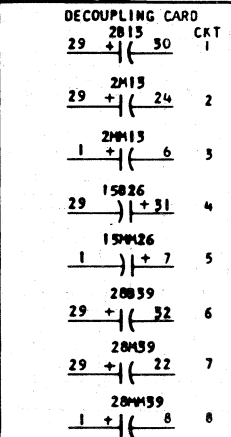
Ref. Page #157

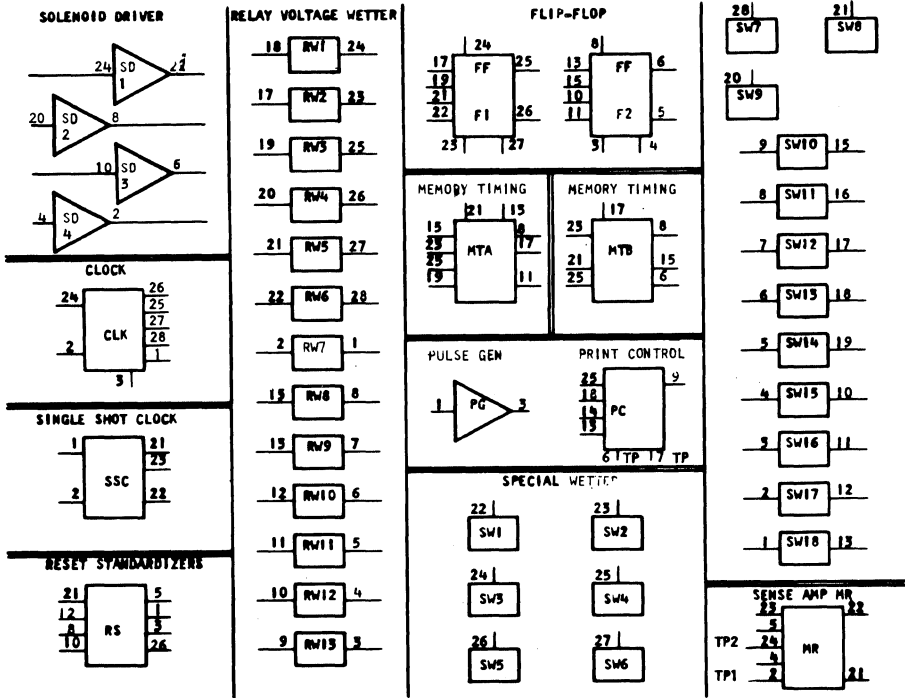


Zone #115

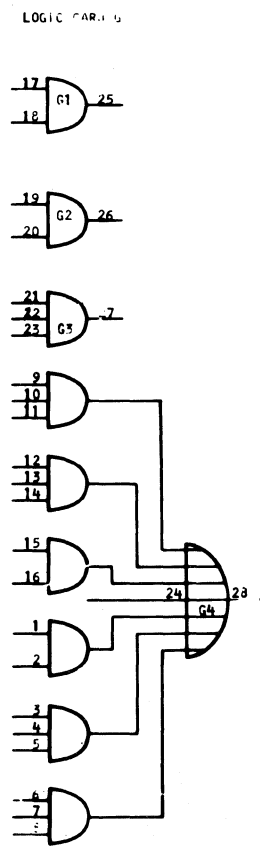
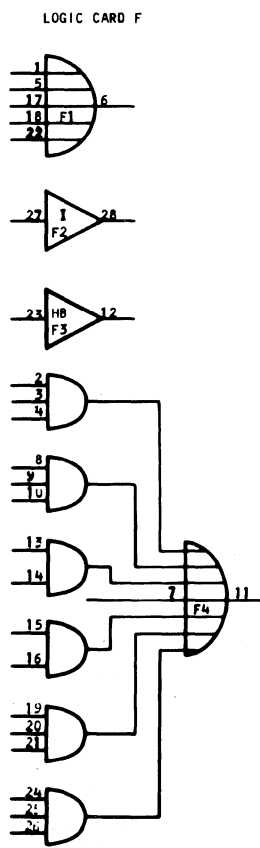


Zone #116

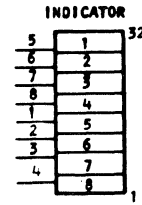
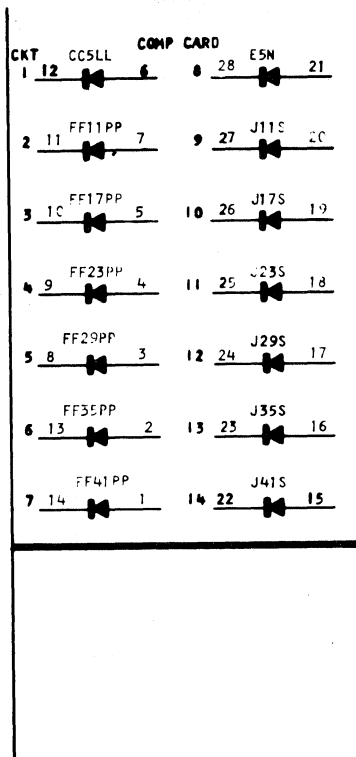
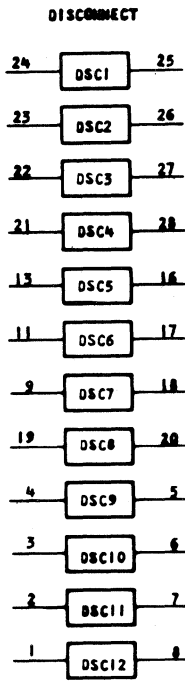




Zone #117

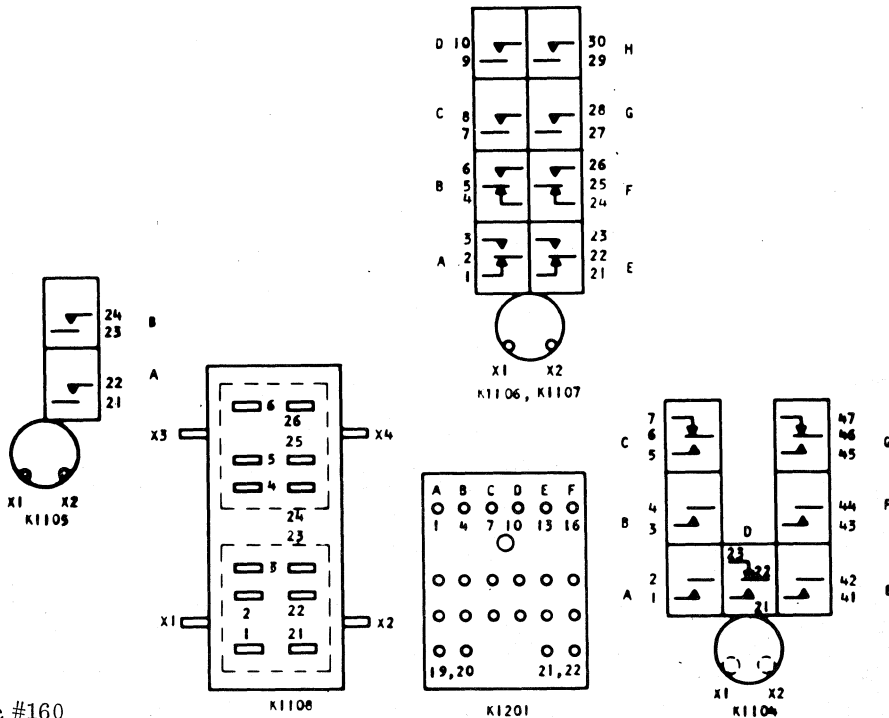


Zone #118

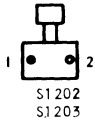
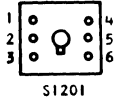


FOR SERVICE ONLY

Zone #119



Zone #120



| RELAYS | NAME | ZONE | | | | | | | | | |
|--------|---------------|-------|----|----|----|----|----|----|---|---|--|
| | | COIL | A | B | C | D | E | F | G | H | |
| K1101 | +15VSENSE | 7 | 1 | | | | | | | | |
| K1102 | +35VSENSE | 87 | 1 | | | | | | | | |
| K1103 | MERCURY START | 86 | 85 | | | | | | | | |
| K1104 | POWER ON | 1 | | | 3 | 3 | 1 | 1 | 4 | | |
| K1105 | DELAY | 4 | 4 | | | | | | | | |
| K1106 | POR | 5 | 1 | 85 | 2 | | | 86 | | | |
| K1107 | CLOCK START | 4 | 3 | | 1 | 4 | 85 | 83 | | | |
| K1108 | LATCH | 1 & 1 | | 1 | | | | | | | |
| K1201 | MEMORY CLEAR | 51 | 51 | 51 | 51 | 51 | 51 | 51 | | | |

Zone #121

| SWITCHES | NAME | ZONE |
|----------|-------------|------|
| S1101 | POWER RESET | 1 |
| S1201 | SRM+35 | 87 |
| S1202 | △ MR | 85 |
| S1203 | MR | 86 |
| S1204 | SSC | 85 |
| S1205 | POR | 86 |
| S1206 | THERMOSTAT | 87 |

| RESISTORS | ZONE |
|-----------|------|
| R1101 | 4 |
| R1102 | 4 |
| R1103 | 86 |
| R1104 | 86 |
| R1105 | 85 |
| R1106 | 1 |
| R1107 | 85 |
| R1108 | 4 |
| R1109 | 3 |
| R1110 | 3 |
| R1111 | 3 |
| R1112 | 3 |
| R1113 | 3 |
| R1114 | 4 |
| R1115 | 87 |
| R1116 | 4 |
| R1117 | 3 |
| R1201 | 51 |
| R1202 | 51 |
| R1203 | 51 |
| R1204 | 51 |
| R1205 | 51 |
| R1206 | 51 |
| R1207 | 85 |
| R1208 | 85 |
| R1209 | 85 |
| R1210 | 51 |
| R1211 | 51 |
| R1212 | 12 |
| R1213 | 51 |
| R1120 | 1 |

| CAPACITORS | ZONE |
|------------|------|
| C1101 | 3 |
| C1103 | 3 |
| C1106 | 3 |
| C1107 | 3 |
| C1108 | 3 |
| C1111 | 4 |
| C1121 | 86 |
| C1122 | 1 |
| C1123 | 1 |
| C1124 | 4 |
| C1125 | 4 |
| C1126 | 87 |
| C1201 | 51 |
| C1202 | 12 |
| C1203 | 51 |
| C1204 | 51 |
| C1205 | 51 |

| DIODES | ZONE |
|--------|------|
| CR1101 | 4 |
| CR1102 | 4 |
| CR1103 | 2 |
| CR1104 | 2 |
| CR1105 | 2 |
| CR1106 | 2 |
| CR1107 | 2 |
| CR1108 | 2 |
| CR1109 | 2 |
| CR1110 | 2 |
| CR1111 | 2 |
| CR1112 | 2 |
| CR1113 | 86 |
| CR1114 | 1 |
| CR1115 | 3 |
| CR1116 | 3 |
| CR1118 | 3 |
| CR1119 | 4 |
| CR1120 | 2 |
| CR1121 | 4 |
| CR1122 | 4 |
| CR1123 | 86 |
| CR1201 | 51 |
| CR1202 | 87 |
| CR1203 | 4 |
| CR1204 | 51 |
| CR1205 | 51 |
| CR1206 | 51 |

| CHOKES | NAME | ZONE |
|--------|--------|------|
| L1101 | FILTER | 3 |
| L1102 | FILTER | 3 |
| L1103 | FILTER | 3 |
| L1104 | FILTER | 3 |
| L1105 | FILTER | 4 |

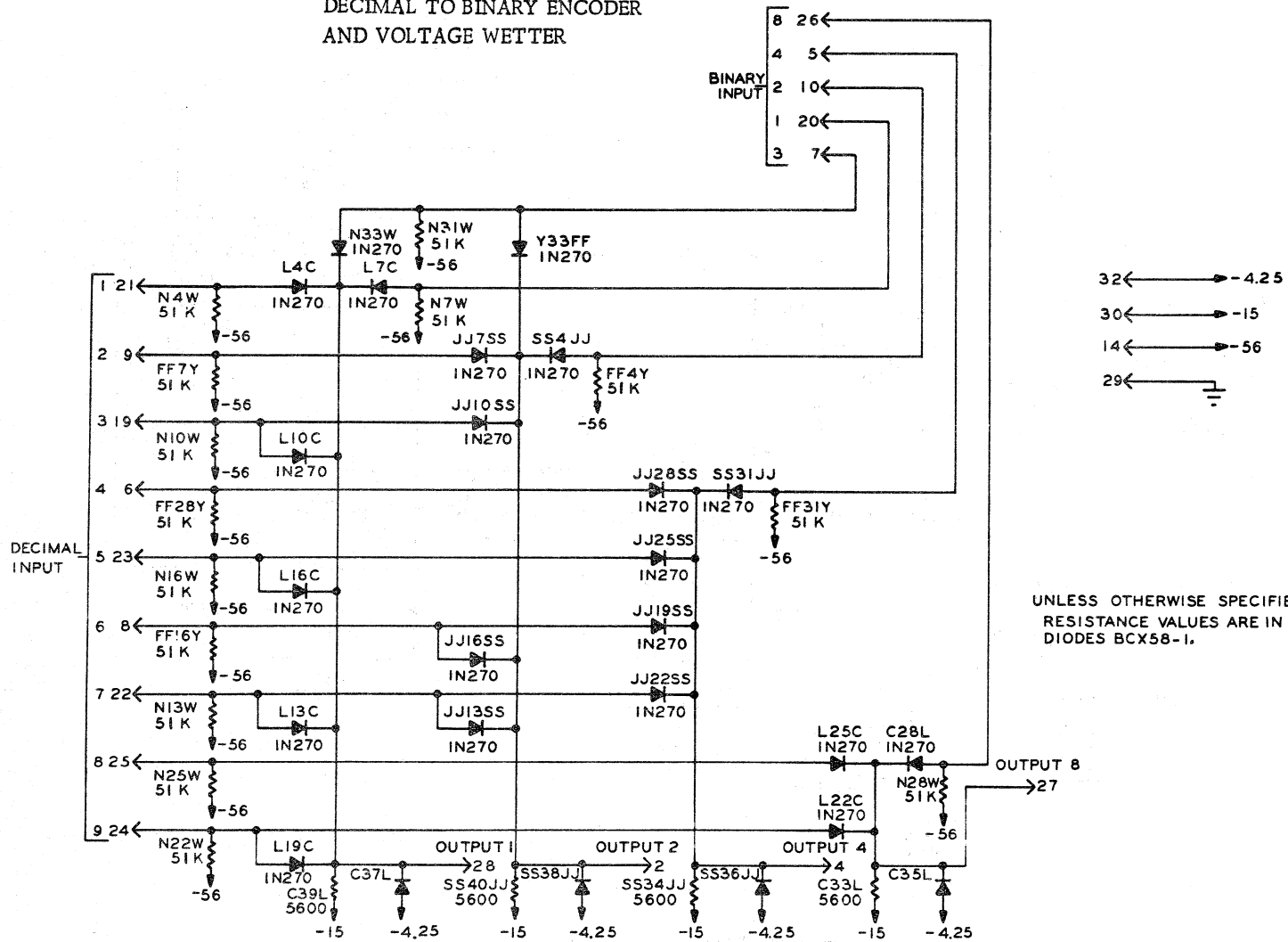
Zone #122

| CONNECTOR INDEX | | | | | | | | | | | | | | | |
|-----------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| P601 | | P601 | | J602 | | J602 | | P603 | | P603 | | P604 | | P901 | |
| PIN | ZONE | PIN | ZONE | PIN | ZONE | PIN | ZONE | PIN | ZONE | PIN | ZONE | PIN | ZONE | PIN | ZONE |
| 1 | | 43 | 82 | 1 | 79 | 43 | | 1 | 51 | 43 | | A | 67 | A | 3 |
| 2 | 89 | 44 | 81 | 2 | 79 | 44 | | 2 | 71 | 44 | | B | 67 | B | 4 |
| 3 | 63 | 45 | 82 | 3 | 79 | 45 | | 3 | 87 | 45 | | C | 68 | C | 9 |
| 4 | 89 | 46 | 81 | 4 | 79 | 46 | | 4 | 77 | 46 | | D | 68 | D | 9 |
| 5 | 89 | 47 | 53 | 5 | 79 | 47 | 80 | 5 | 83 | 47 | | E | 68 | E | 86 |
| 7 | 74 | 48 | 53 | 7 | 79 | 48 | 80 | 7 | 66 | 48 | | F | 68 | F | 87 |
| 8 | 83 | 49 | 31 | 8 | 79 | 49 | 80 | 8 | 63 | 49 | | H | 68 | H | 3 |
| 10 | 25 | 50 | 53 | 10 | 79 | 50 | 80 | 10 | | 50 | | J | 69 | J | |
| 11 | 67 | 51 | 53 | 11 | 79 | 51 | 80 | 11 | 71 | 51 | | K | 69 | K | |
| 12 | 65 | 52 | 34 | 12 | 79 | 52 | 80 | 12 | 74 | 52 | | L | 69 | L | |
| 13 | 80 | 53 | 63 | 13 | 79 | 53 | 80 | 13 | 8 | 53 | | M | 69 | M | |
| 14 | 63 | 54 | 63 | 14 | 79 | 54 | 81 | 14 | 74 | 54 | | N | 69 | N | |
| 15 | 53 | 55 | 38 | 15 | 82 | 55 | 81 | 15 | 11 | 55 | | P | 70 | P | |
| 16 | 41 | 56 | 53 | 16 | 82 | 56 | 81 | 16 | 7 | 56 | 52 | R | 70 | R | |
| 17 | 41 | 57 | 53 | 17 | 82 | 57 | 81 | 17 | | 57 | | S | 71 | S | |
| 18 | 41 | 58 | 64 | 18 | 79 | 58 | 81 | 18 | | 58 | | T | 70 | T | |
| 20 | 41 | 59 | 53 | 20 | 79 | 59 | 81 | 20 | | 59 | | U | 8 | U | |
| 21 | 45 | 60 | 52 | 21 | 79 | 60 | 81 | 21 | | 60 | | V | | V | |
| 22 | 46 | 62 | 45 | 22 | 79 | 62 | 81 | 22 | | 62 | | W | | W | |
| 23 | 52 | 63 | 46 | 23 | 79 | 63 | 81 | 23 | | 63 | | X | | X | |
| 24 | 52 | 64 | 46 | 24 | 79 | 64 | | 24 | | 64 | | Y | | Y | |
| 25 | 52 | 65 | 82 | 25 | 79 | 65 | 80 | 25 | | 65 | | Z | | Z | |
| 26 | 71 | 66 | 81 | 26 | 79 | 66 | 80 | 26 | | 66 | | A | | A | |
| 27 | 71 | 67 | 82 | 27 | 79 | 67 | | 27 | 61 | 67 | | B | | B | |
| 28 | 65 | 70 | 81 | 28 | 82 | 70 | 80 | 28 | 40 | 70 | 80 | C | | C | |
| 29 | 65 | 71 | | 29 | 82 | 71 | 80 | 29 | | 71 | 80 | D | | D | |
| 30 | 44 | 72 | | 30 | 82 | 72 | | 30 | | 72 | | | | | |
| 31 | 66 | 73 | | 31 | 82 | 73 | 80 | 31 | | 73 | 80 | F | | F | |
| 32 | 53 | 74 | | 32 | 82 | 74 | 80 | 32 | | 74 | 80 | G | | G | |
| 33 | 53 | 75 | | 33 | 82 | 75 | 80 | 33 | | 75 | 80 | H | | H | |
| 34 | 32 | 76 | | 34 | | 76 | 80 | 34 | 83 | 76 | 80 | I | | I | 1 |
| 35 | | 77 | | 35 | | 77 | 80 | 35 | | 77 | 80 | J | | J | 1 |
| 36 | 83 | 78 | | 36 | | 78 | | 36 | 63 | 78 | | K | | K | 2 |
| 37 | 87 | 79 | | 37 | | 79 | | 37 | 83 | 79 | | H | | H | 2 |
| 38 | | 80 | | 38 | | 80 | | 38 | 83 | 80 | | N | | N | 1 |
| 39 | | 82 | | 39 | | 82 | | 39 | 83 | 82 | | | | | |
| 40 | 17 | | | 40 | | | | 40 | | | | | | | |
| 41 | 82 | | | 41 | | | | 41 | | | | | | | |
| 42 | 81 | | | 42 | | | | 42 | | | | | | | |

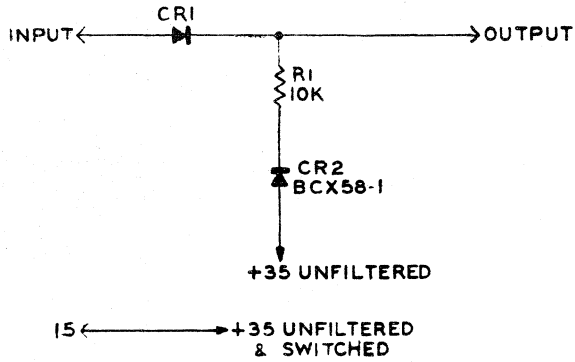
Zone #123

Zone #124

DECIMAL TO BINARY ENCODER AND VOLTAGE WETTER



UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS $\pm 5\%$ 1/2W.
DIODES BCX58-1.

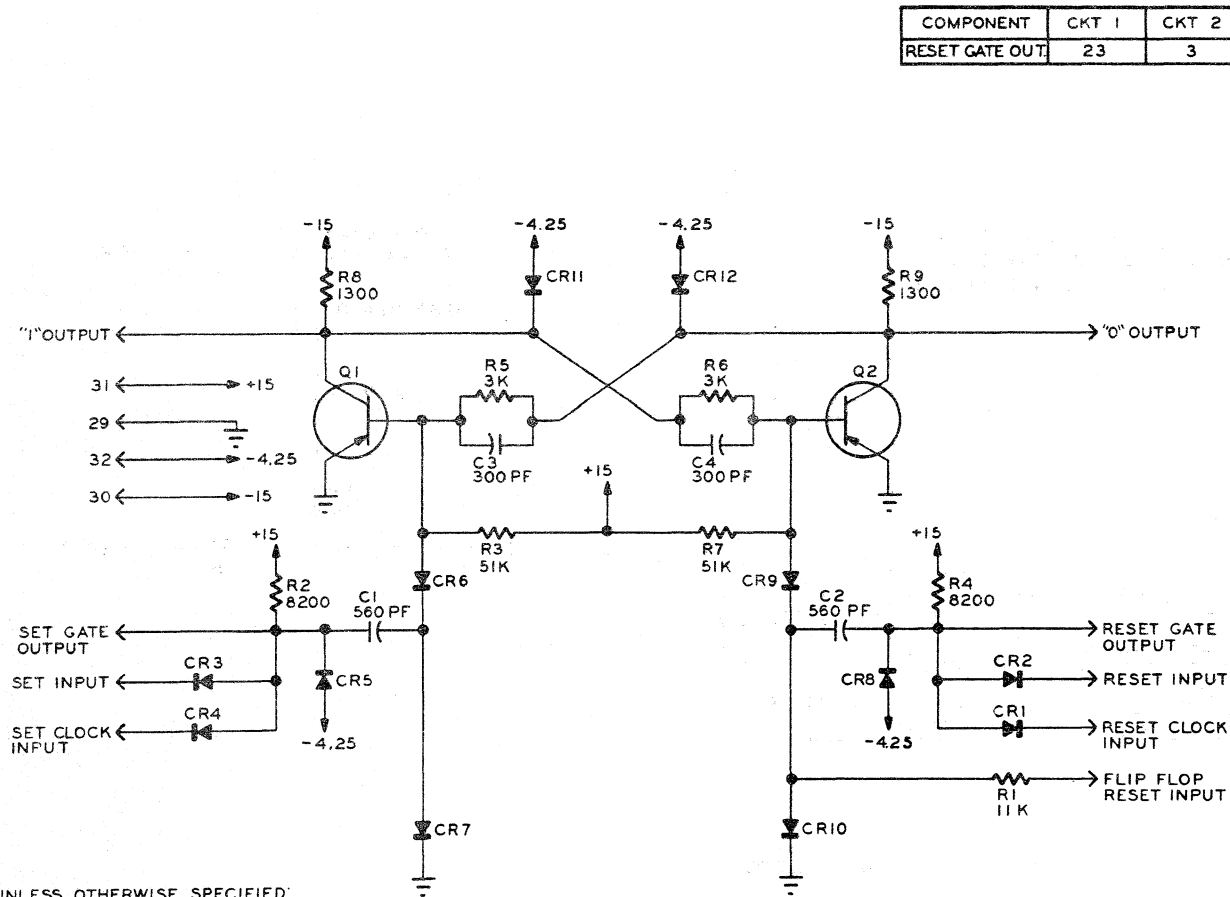


DISCONNECT

| | | | | | | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|
| | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 | CKT 6 | CKT 7 | CKT 8 | CKT 9 | CKT 10 | CKT 11 | CKT 12 |
| CR1 | L5C | L14C | L23C | L32C | BB5U | BB14U | BB23U | BB32U | SS5JJ | SS14JJ | SS23JJ | SS32JJ |
| CR2 | L11C | L20C | L29C | L38C | BB11U | BB20U | BB29U | BB38U | SS11JJ | SS20JJ | SS29JJ | SS38JJ |
| R1 | L8C | L17C | L26C | L35C | BB8U | BB17U | BB26U | BB35U | SS8JJ | SS17JJ | SS26JJ | SS35JJ |
| INPUT | 24 | 23 | 22 | 21 | 13 | 11 | 9 | 19 | 4 | 3 | 2 | 1 |
| OUTPUT | 25 | 26 | 27 | 28 | 16 | 17 | 18 | 20 | 5 | 6 | 7 | 8 |

UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES ARE IN OHMS, ±5%, 1/2W.
 DIODES ARE IN270.

FLIP FLOP (2 ELEMENTS)

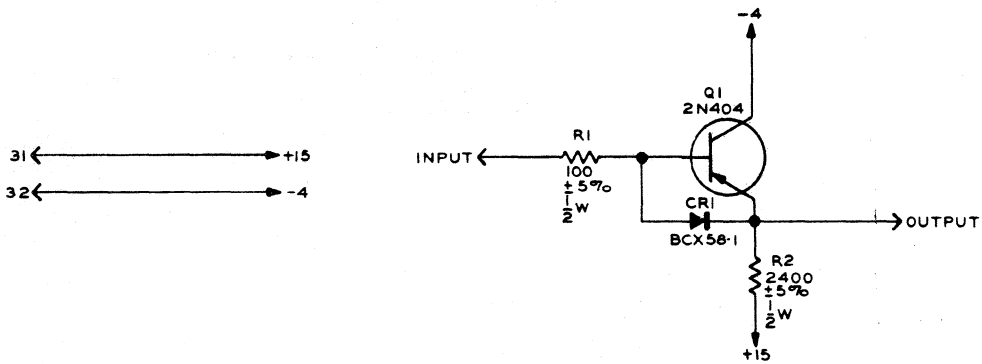


UNLESS OTHERWISE SPECIFIED:
 RESISTANCES ARE IN OHMS, 5%, 1/2W.
 TRANSISTORS 2N404.
 DIODES BCX 58-1
 CAPACITANCES ARE ± 10% 500WVDC

| COMPONENT | CKT 1 | CKT 2 | COMPONENT | CKT 1 | CKT 2 |
|-----------------|-------|-------|-----------|-------|--------|
| RESET GATE OUT. | 23 | 3 | C1 | K5B | KK5TT |
| | | | C2 | B35K | TT35KK |
| | | | C3 | I5P22 | I5EE22 |
| | | | C4 | I5H22 | I5MM22 |
| | | | CR1 | M35V | HH37Z |
| | | | CR2 | M37V | HH35Z |
| | | | CR3 | V3M | Z3HH |
| | | | CR4 | VIM | Z1HH |
| | | | CR5 | K3B | KK3TT |
| | | | CR6 | K11B | KK11TT |
| | | | CR7 | B7K | TT9KK |
| | | | CR8 | B37K | KK37TT |
| | | | CR9 | K28B | KK28TT |
| | | | CR10 | B30K | TT31KK |
| | | | CR11 | B9K | TT7KK |
| | | | CR12 | B26K | TT26KK |
| | | | Q1 | N10R | EE10HH |
| | | | Q2 | N31R | EE31HH |
| | | | R1 | B32K | TT33KK |
| | | | R2 | B1K | TT1KK |
| | | | R3 | K13B | KK13TT |
| | | | R4 | B39K | TT39KK |
| | | | R5 | I5M22 | I5HH22 |
| | | | R6 | I5K22 | I5KK22 |
| | | | R7 | B24K | TT24KK |
| | | | R8 | V6M | Z6HH |
| | | | R9 | V26M | Z26HH |
| SET INPUT | 17 | 13 | | | |
| RESET INPUT | 22 | 11 | | | |
| FLIP FLOP RESET | 27 | 4 | | | |
| SET CLOCK IN. | 19 | 15 | | | |
| RESET CLOCK IN. | 21 | 10 | | | |
| '1' OUTPUT | 25 | 6 | | | |
| '0' OUTPUT | 26 | 5 | | | |
| SET GATE OUT. | 24 | 8 | | | |

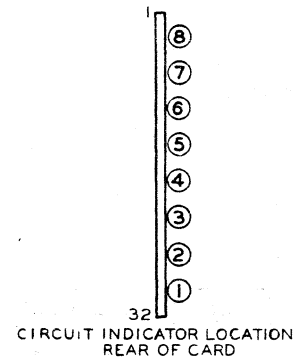
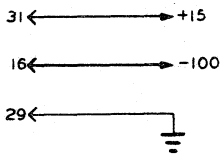
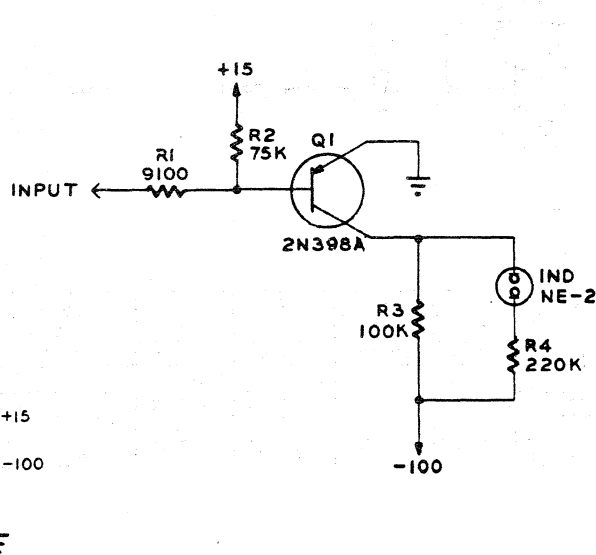
HEAVY BUFFER

| COMPONENT | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 | CKT 6 | CKT 7 | CKT 8 | CKT 9 | CKT 10 |
|-----------|--------|--------|--------|--------|-------|-------|-------|-------|-------|--------|
| R1 | KK4TT | LL15UU | KK25TT | KK35TT | CC1IV | CC25V | M35D | M25D | M15D | B5K |
| R2 | CC13LL | DD23MM | FF33PP | U41BB | V21CC | U34BB | U36BB | B31K | B21K | B11K |
| CR1 | KK11TT | KK21TT | KK31TT | CC39LL | V15CC | U31BB | J39S | D33M | D23M | C13L |
| Q1 | NN8RR | NN18RR | NN28RR | NN38RR | W18Y | W28Y | D38F | D28F | D18F | D8F |
| INPUT | 1 | 3 | 6 | 9 | 13 | 15 | 19 | 21 | 23 | 25 |
| OUTPUT | 2 | 5 | 8 | 10 | 14 | 17 | 18 | 20 | 22 | 24 |



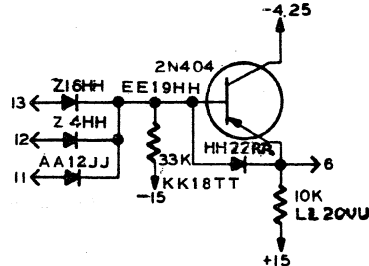
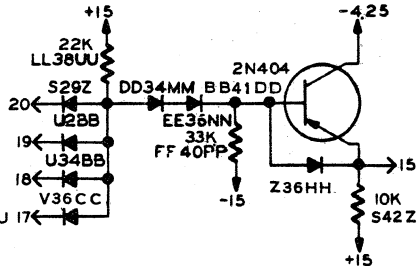
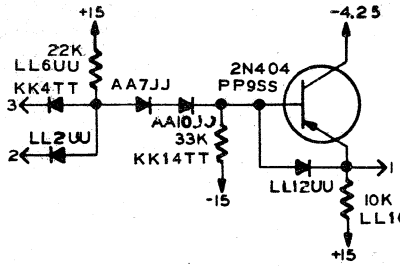
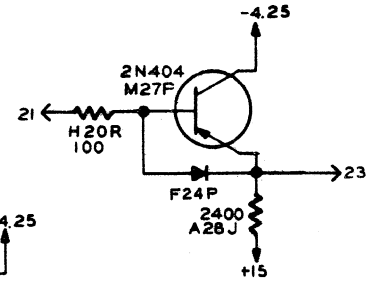
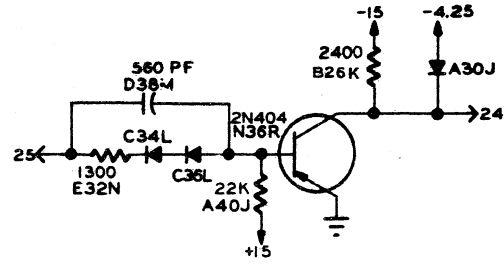
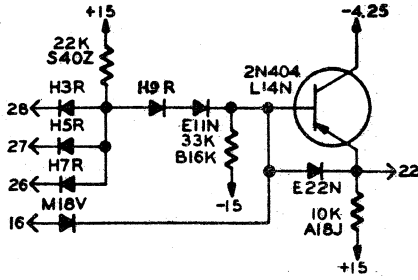
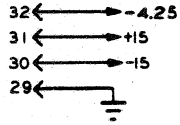
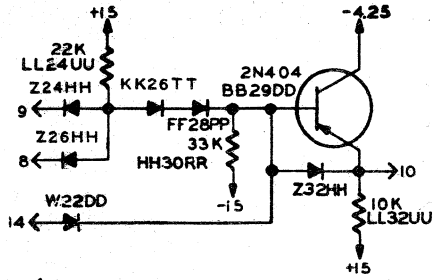
INDICATOR CARD

| | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 | CKT 6 | CKT 7 | CKT 8 |
|-------|-------|-------|-------|-------|-------|--------|--------|--------|
| R1 | A31J | A23J | A15J | A7J | LL4UU | LL9UU | LL17UU | LL25UU |
| R2 | A25J | A17J | A9J | A1J | LL6UU | LL15UU | LL23UU | LL31UU |
| R3 | N25W | N19W | N13W | N7W | Y7FF | Y13FF | Y19FF | Y25FF |
| R4 | N28W | N22W | N16W | N10W | Y10FF | Y16FF | Y22FF | Y28FF |
| Q1 | J28L | J20L | J12L | J4L | FF4JJ | JJ12LL | JJ20LL | JJ28LL |
| IND | E34H | K34M | P34S | U34W | Y34AA | CC34EE | HH34KK | MM34PP |
| INPUT | 5 | 6 | 7 | 8 | 1 | 2 | 3 | 4 |



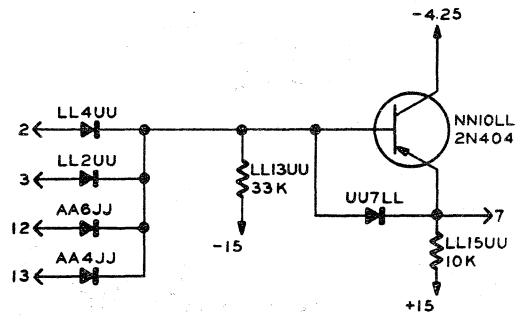
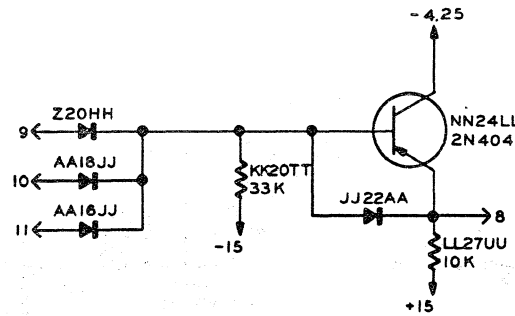
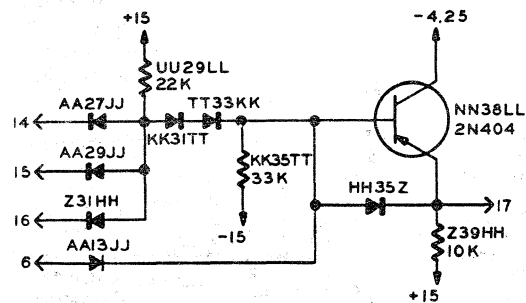
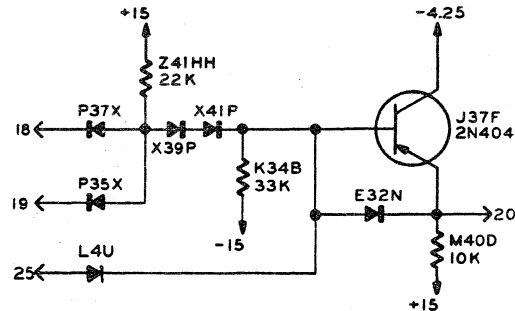
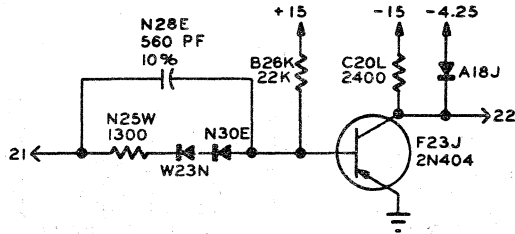
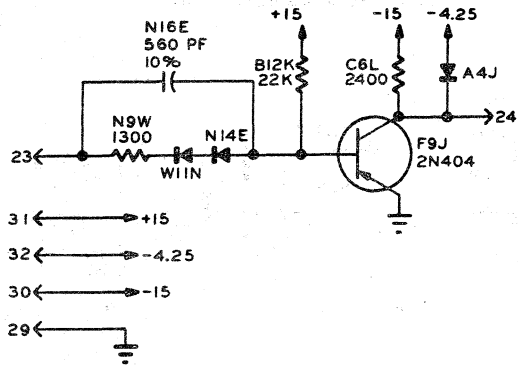
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
±5%, 1/2W.

LOGIC CARD "A"



UNLESS OTHERWISE SPECIFIED
 RESISTANCE VALUES ARE IN OHMS $\pm 5\%$ 1/2W
 DIODES ARE BCX58-1
 CAPACITANCE VALUES ARE $\pm 10\%$, 500V

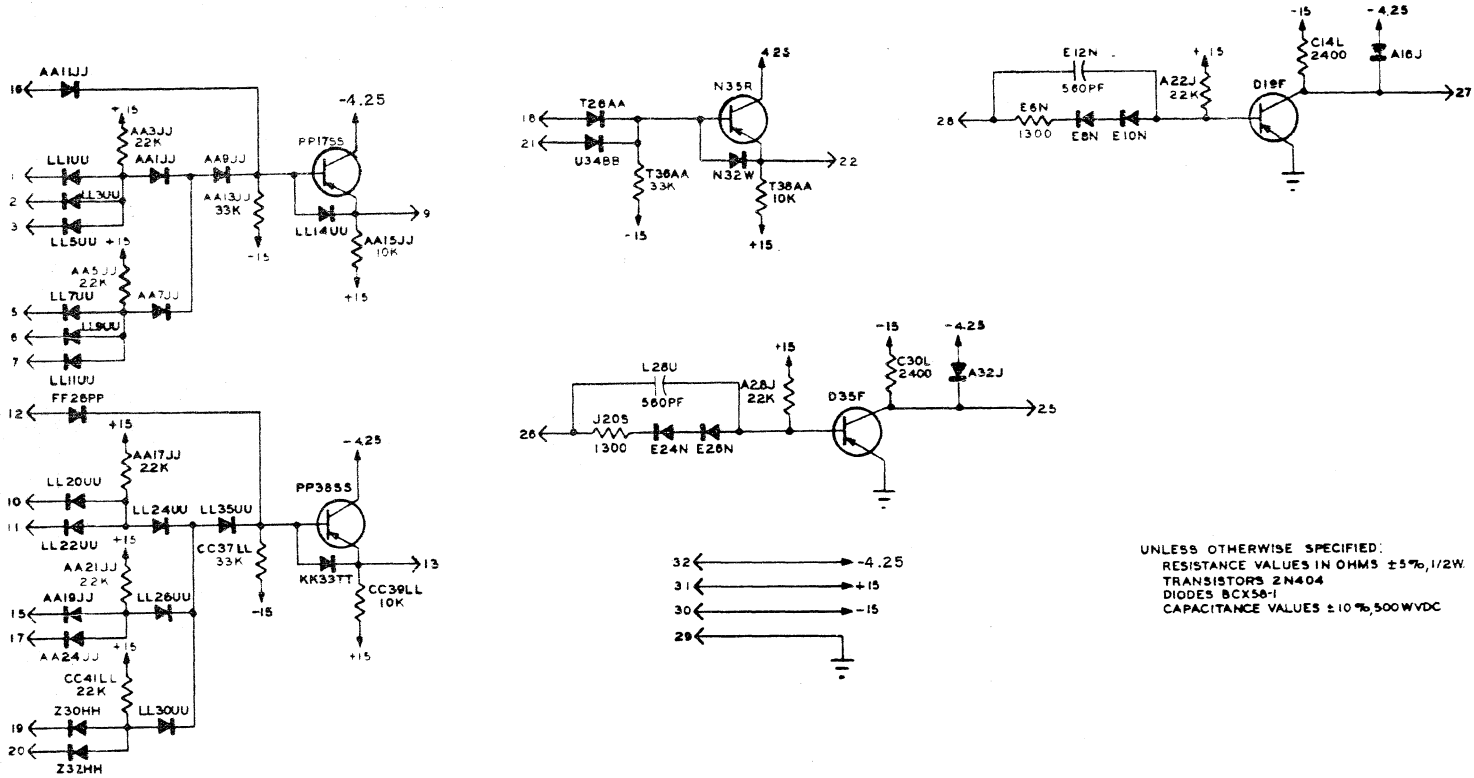
LOGIC CARD "B"



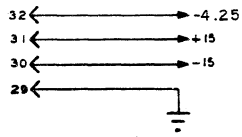
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS±5%,
1/2 W.
DIODES ARE BCX58-1

7000-100-1-1

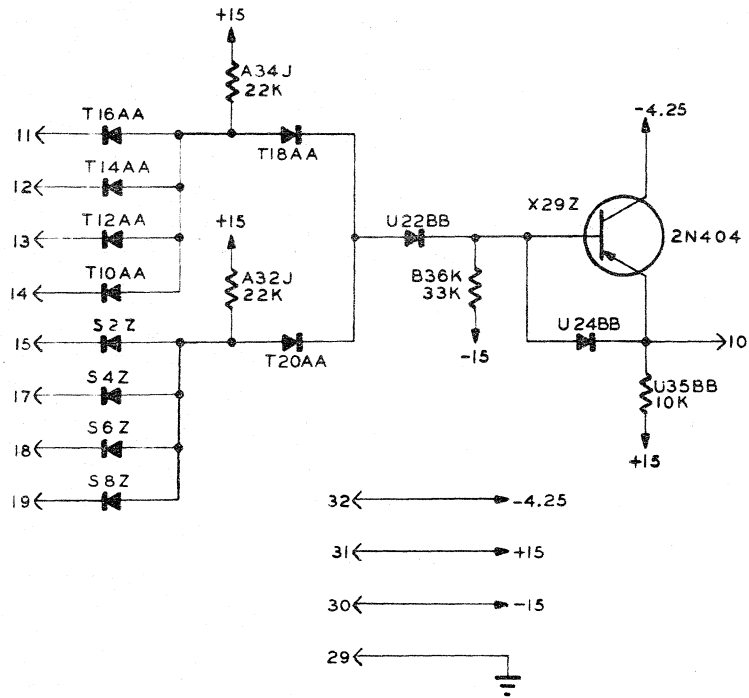
LOGIC CARD "C"



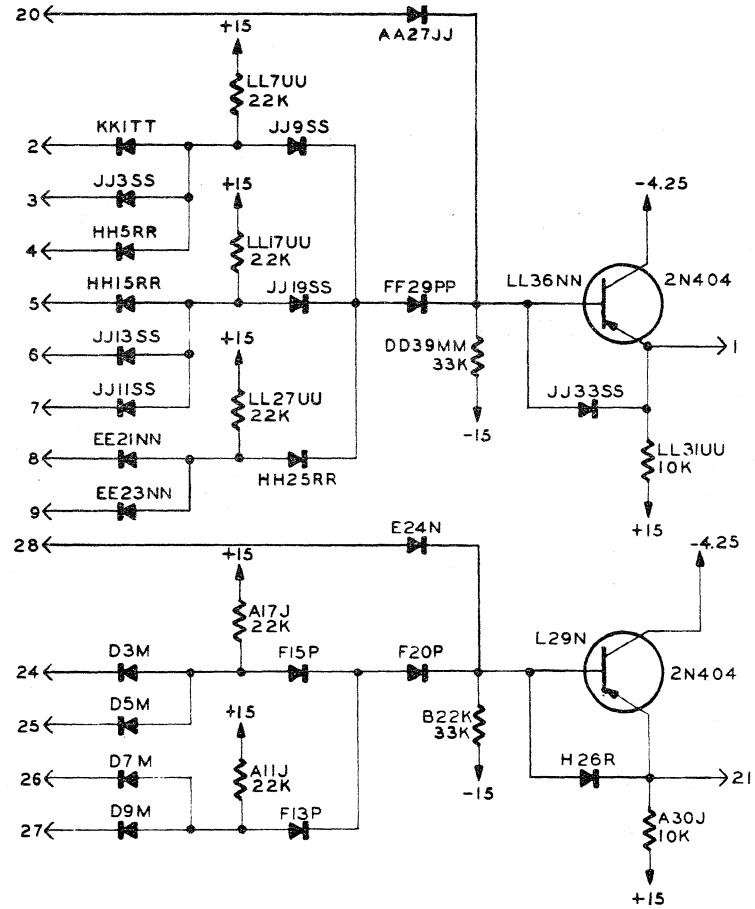
UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES IN OHMS $\pm 5\%$, 1/2W.
 TRANSISTORS 2N404
 DIODES BCX58-1
 CAPACITANCE VALUES $\pm 10\%$, 500WVDC



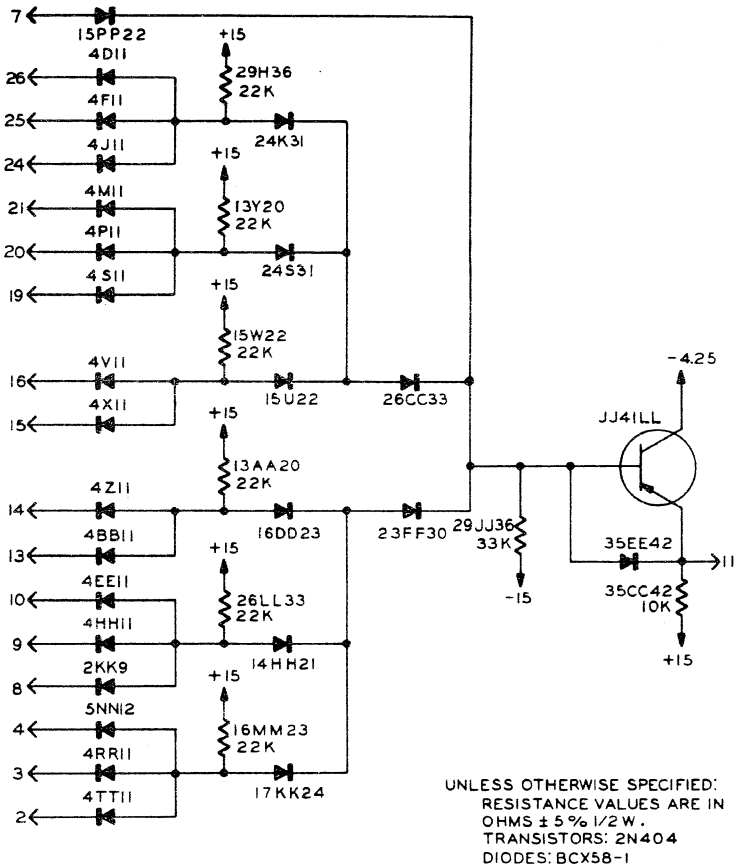
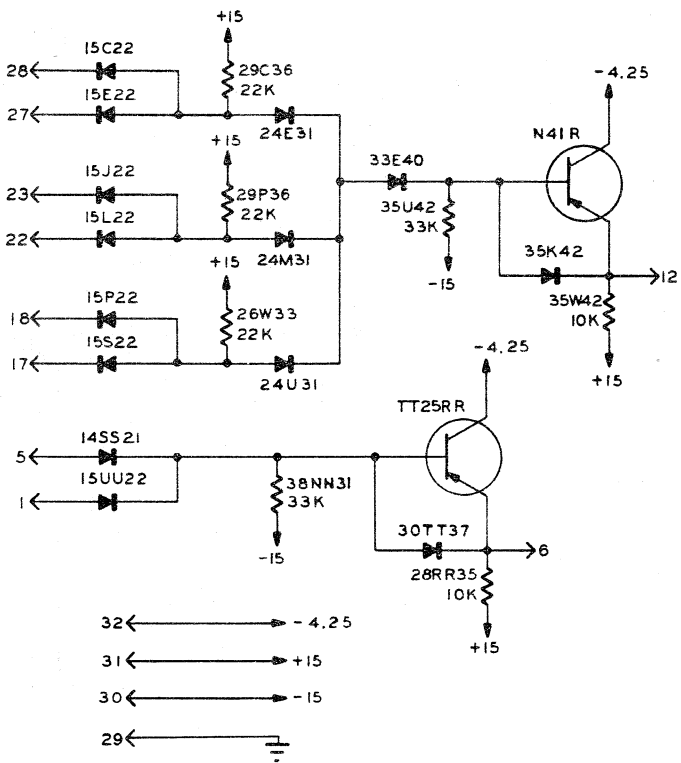
LOGIC CARD "D"



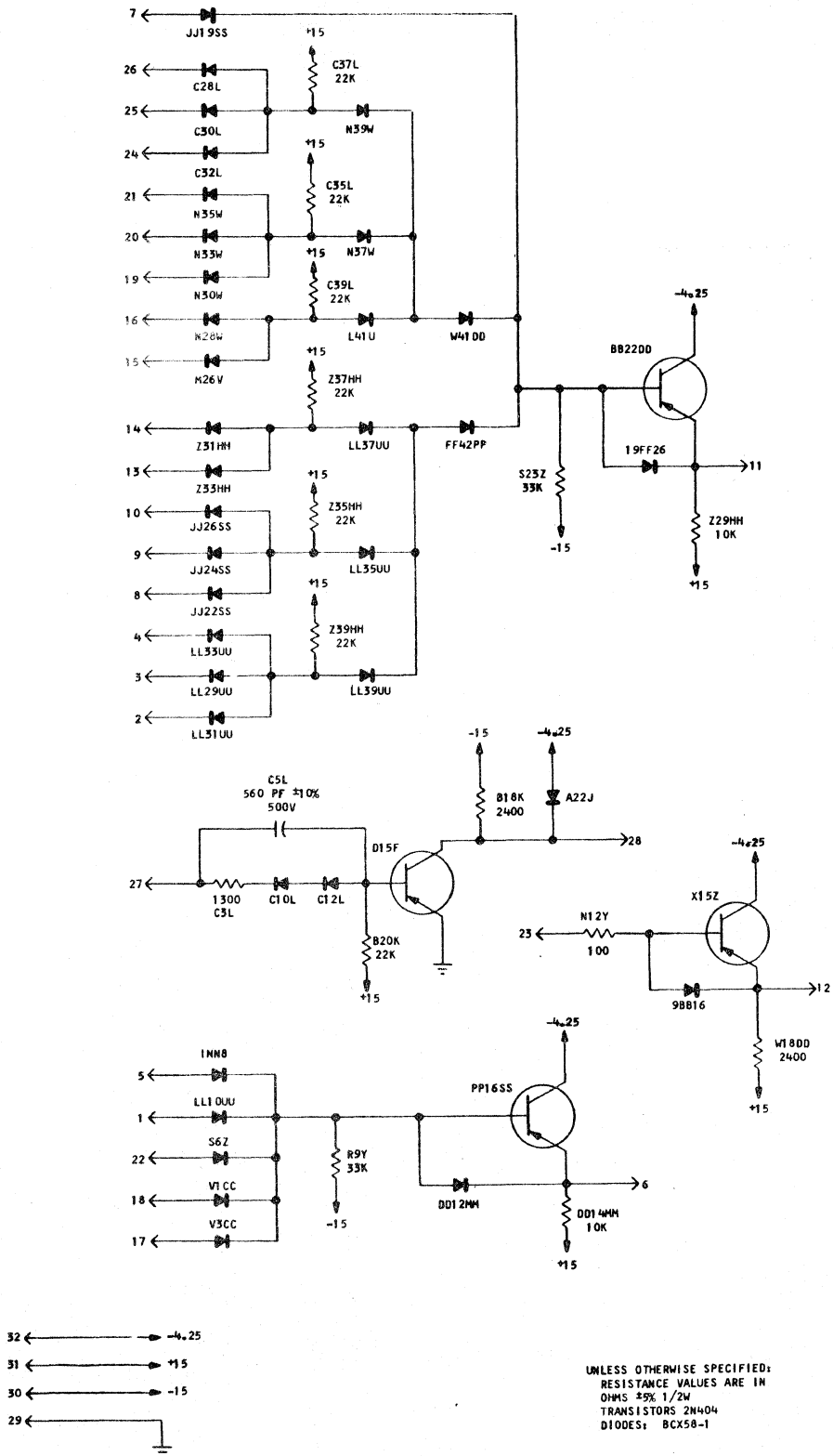
UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES IN OHMS, 5%,
 1/2 W.
 DIODES ARE BCX58-I.



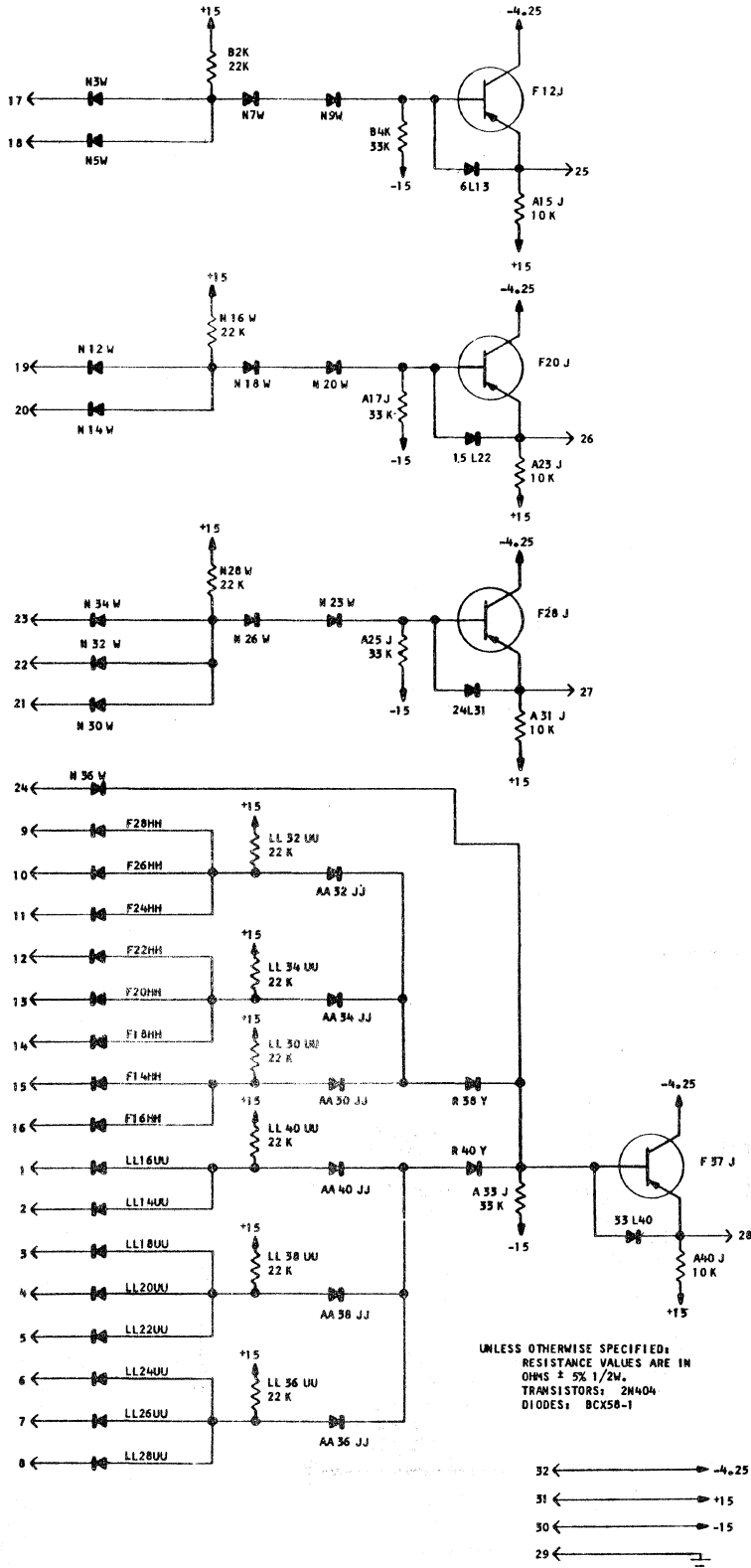
LOGIC CARD "E"



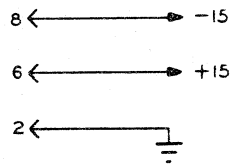
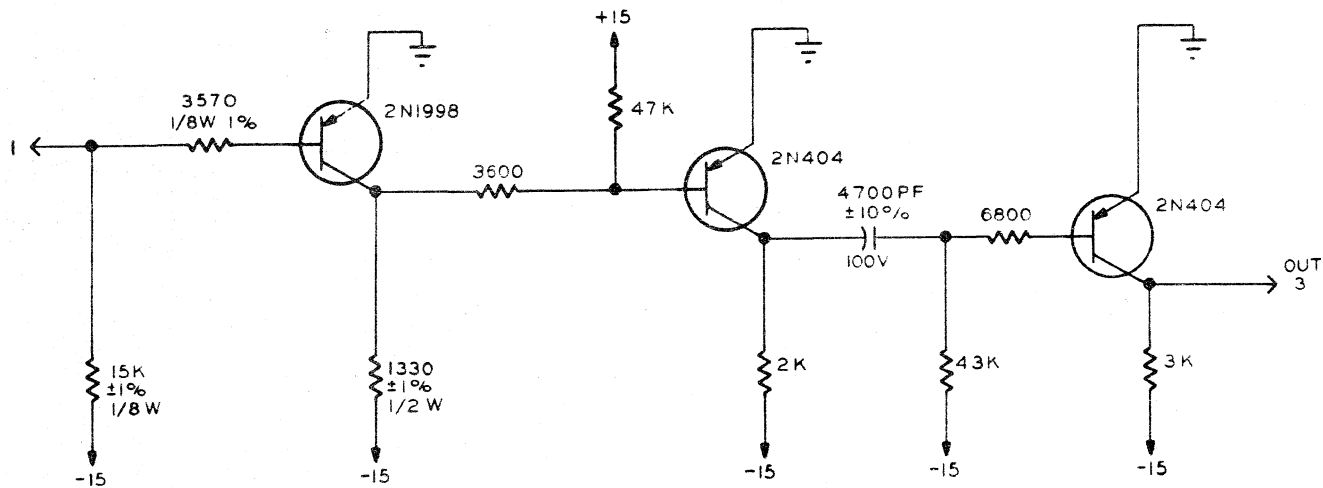
LOGIC CARD "F"



LOGIC CARD "G"



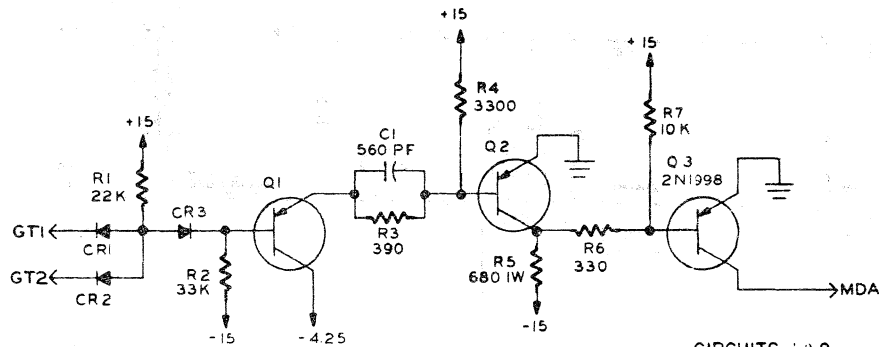
MAG. PICK UP PULSE GEN.



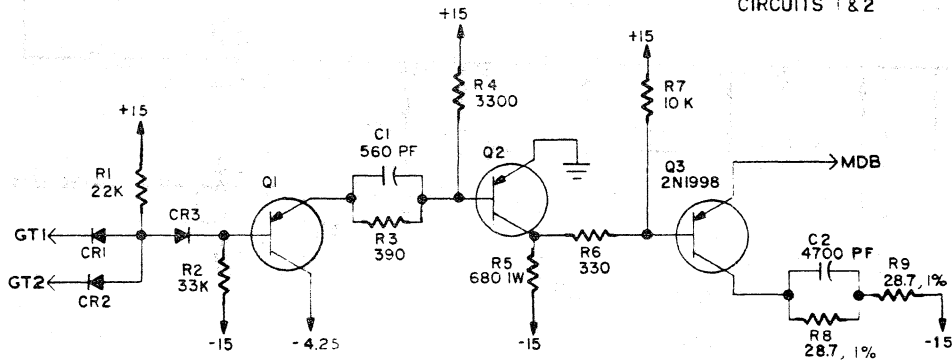
UNLESS OTHERWISE SPECIFIED
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2 W

MEMORY DRIVER (4 ELEMENTS)

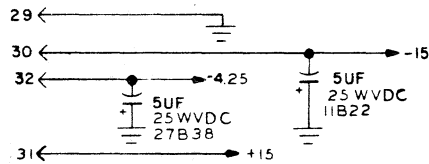
| COMPONENT | CKT 1 | CKT 2 | CKT 3 | CKT 4 |
|-----------|-----------|-----------|-------------|-------------|
| C1 | I2 J 19 | I2 T 19 | I2 BB19 | I2 LL19 |
| C2 | — | — | 34 U42 | 34 EE42 |
| CR 1 | I J 6 | I T 6 | I BB 6 | I LL 6 |
| CR 2 | I L 6 | I V 6 | I DD 6 | I NN 6 |
| CR 3 | 3 F 8 | 3 R 8 | 3 Z 8 | 3 J J 8 |
| Q1 | J 9 L | T 9 V | B B 9 D D | L L 9 N N |
| Q2 | F 2 2 J | N 2 2 R | Y 2 2 A A | J J 2 2 L L |
| Q3 | F 4 0 J | N 4 0 R | Z 4 0 B B | L L 4 0 N N |
| R1 | 6 D 1 3 | I N 8 | I X 8 | I F F 8 |
| R2 | 1 0 F 1 7 | 1 0 R 1 7 | 1 0 Z 1 7 | 1 0 J J 1 7 |
| R3 | 1 3 L 2 0 | 1 3 V 2 0 | 1 3 D D 2 0 | 1 3 N N 2 0 |
| R4 | 1 5 D 2 2 | 1 0 N 1 7 | 1 0 X 1 7 | 1 0 F F 1 7 |
| R5 | 2 6 E 3 5 | 2 6 M 3 5 | 2 5 Y 3 4 | 2 5 K K 3 4 |
| R6 | 2 8 H 3 7 | 2 8 P 3 7 | 2 7 A A 3 6 | 2 7 M M 3 6 |
| R7 | 3 0 K 3 7 | 3 0 S 3 7 | 3 0 C C 3 7 | 3 0 P P 3 7 |
| R8 | — | — | 3 1 W 4 2 | 3 1 H H 4 2 |
| R9 | — | — | 2 2 U 3 3 | 2 2 E E 3 3 |
| GT1 | 2 7 | 2 0 | 1 5 | 8 |
| GT2 | 2 5 | 1 8 | 1 1 | 6 |
| MDA | 1 | 2 | — | — |
| MDB | — | — | 3 | 5 |



CIRCUITS 1 & 2

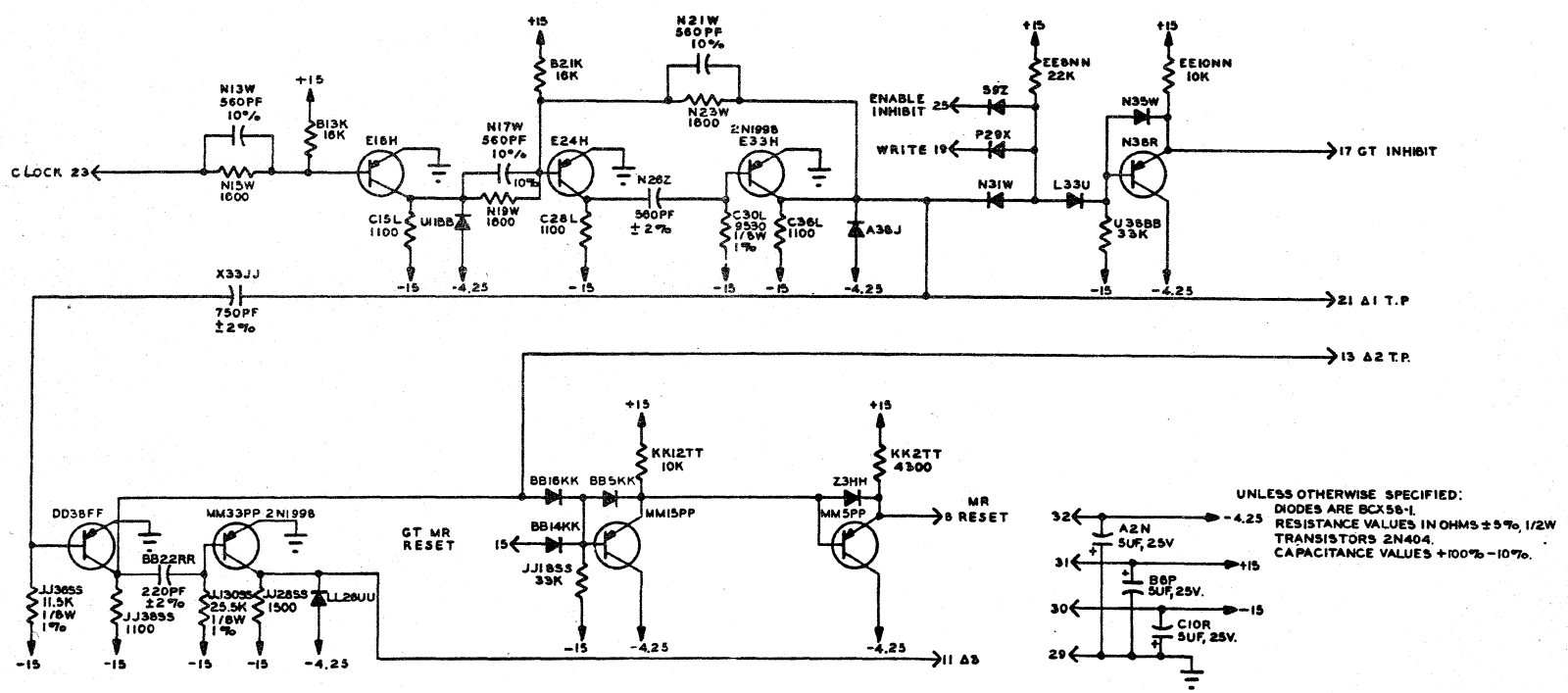


CIRCUITS 3 & 4



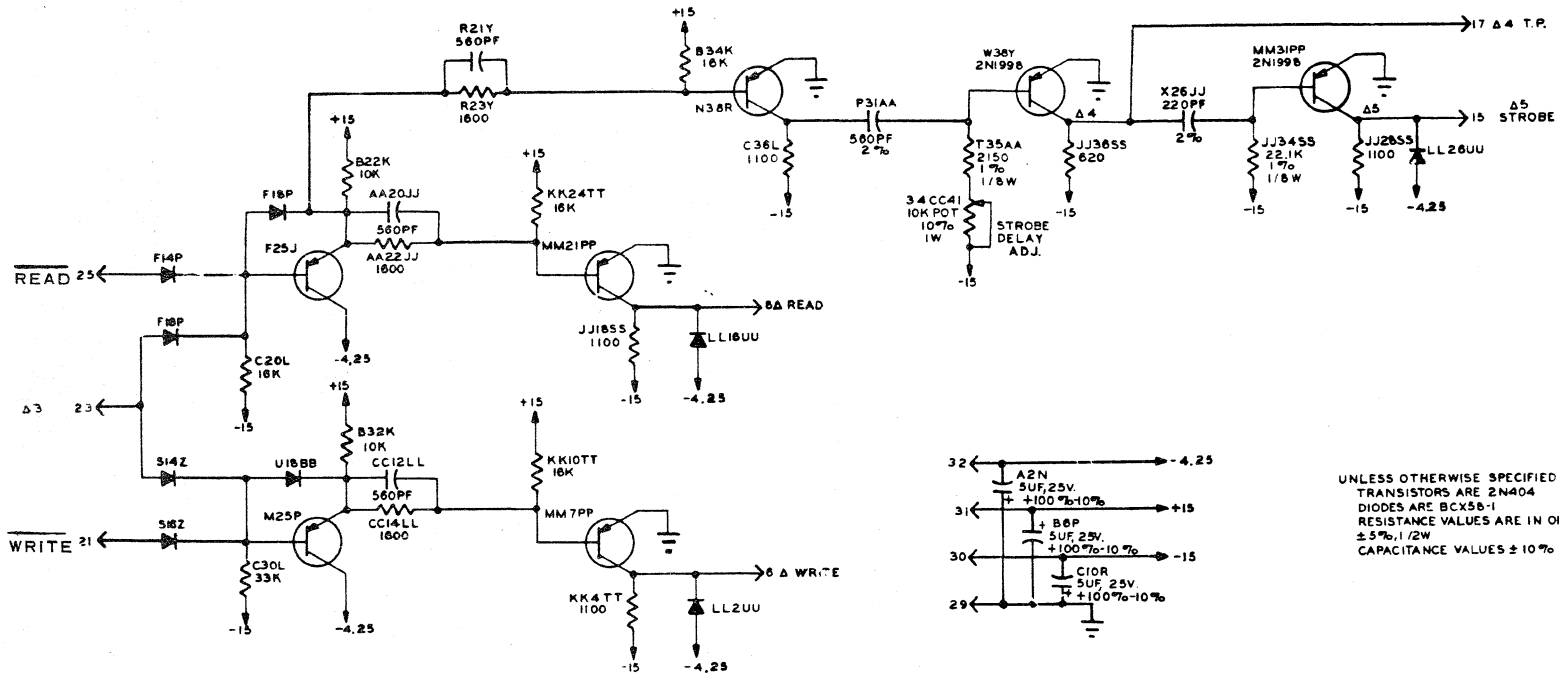
UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES ARE IN OHMS 5%, 1/2 W
 TRANSISTORS 2N404
 DIODES BCX58-1
 CAPACITANCE VALUES ARE ±10%

MEMORY TIMING "A"



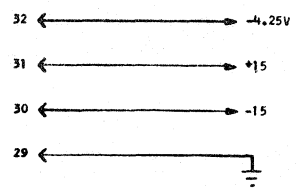
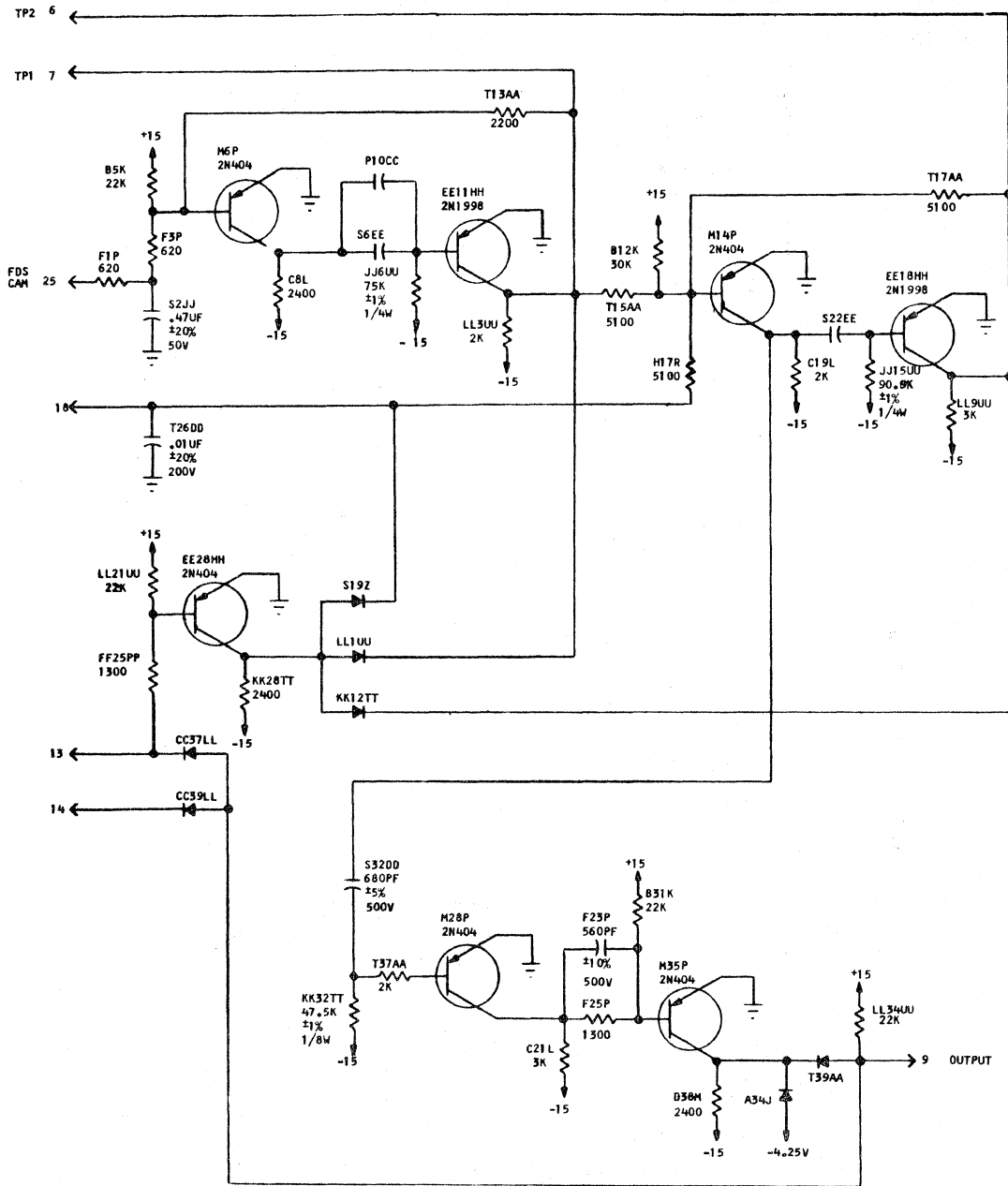
UNLESS OTHERWISE SPECIFIED:
DIODES ARE BCX58-1
RESISTANCE VALUES IN OHMS ± 5%, 1/2W
TRANSISTORS 2N404
CAPACITANCE VALUES +100% -10%

MEMORY TIMING "B"



UNLESS OTHERWISE SPECIFIED
 TRANSISTORS ARE 2N404
 DIODES ARE BCX55-1
 RESISTANCE VALUES ARE IN OHMS,
 ±5%, 1/2W
 CAPACITANCE VALUES ±10%

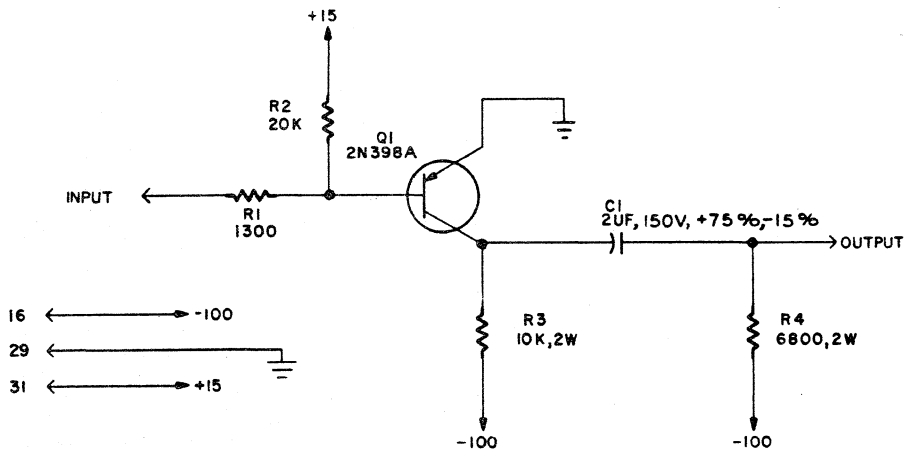
PRINT CONTROL



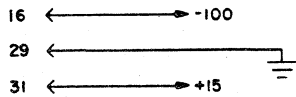
UNLESS OTHERWISE SPECIFIED
 RESISTANCE VALUES ARE IN OHMS ±5% 1/2W
 CAPACITANCE VALUES .1 UF ±5%, 100WVDC
 DIODES ARE BCX58-1

RACK STOP DRIVER (5 ELEMENTS)

| COMPONENT | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 |
|-----------|-------|--------|--------|--------|--------|
| C 1 | W8SS | B10X | X25TT | B27X | T4INN |
| Q 1 | M4P | EE16HH | M19P | EE32HH | M36P |
| R 1 | U1BB | LL15UU | U18BB | LL31UU | T34AA |
| R 2 | A3J | LL17UU | A18J | LL33UU | A35J |
| R 3 | T4DD | R14BB | T21DD | R31BB | T37DD |
| R 4 | EE2SS | B14N | TT20FF | B31N | TT37FF |
| INPUT | 11 | 1 | 9 | 3 | 8 |
| OUTPUT | 5 | 27 | 2 | 26 | 6 |

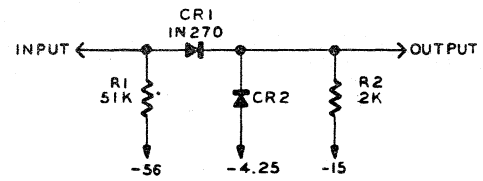


UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
± 5 %, 1/2 W.

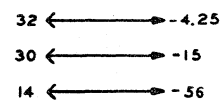


RELAY VOLTAGE WETTER (13 ELEMENTS)

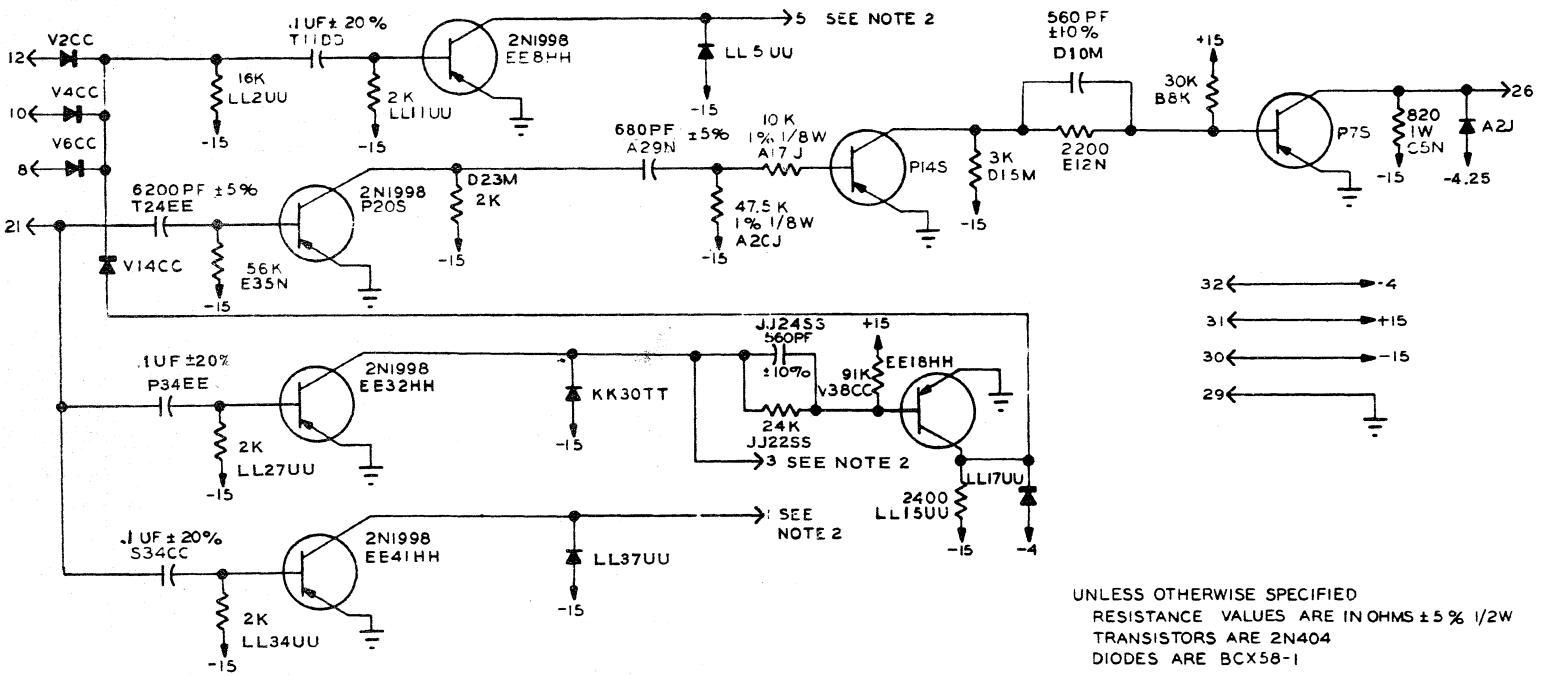
| COMP. | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 | CKT 6 | CKT 7 | CKT 8 | CKT 9 | CKT 10 | CKT 11 | CKT 12 | CKT 13 |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|
| CR1 | L2U | L8U | L14U | L20U | L26U | L32U | L39U | Z4HH | Z10HH | Z16HH | Z22HH | Z28HH | Z34HH |
| CR2 | A2J | A8J | A14J | A20J | A26J | A32J | A39J | LL2UU | LL10UU | LL16UU | LL22UU | LL28UU | LL34UU |
| R1 | N4W | N10W | N16W | N22W | N28W | N34W | N37W | Y2FF | Y8FF | Y14FF | Y20FF | Y26FF | Y32FF |
| R2 | B4K | B10K | B16K | B22K | B28K | B34K | B37K | LL4UU | KK8TT | KK14TT | KK20TT | KK26TT | KK32TT |
| INPUT | 18 | 17 | 19 | 20 | 21 | 22 | 2 | 15 | 13 | 12 | 11 | 10 | 9 |
| OUTPUT | 24 | 23 | 25 | 26 | 27 | 28 | 1 | 8 | 7 | 6 | 5 | 4 | 3 |



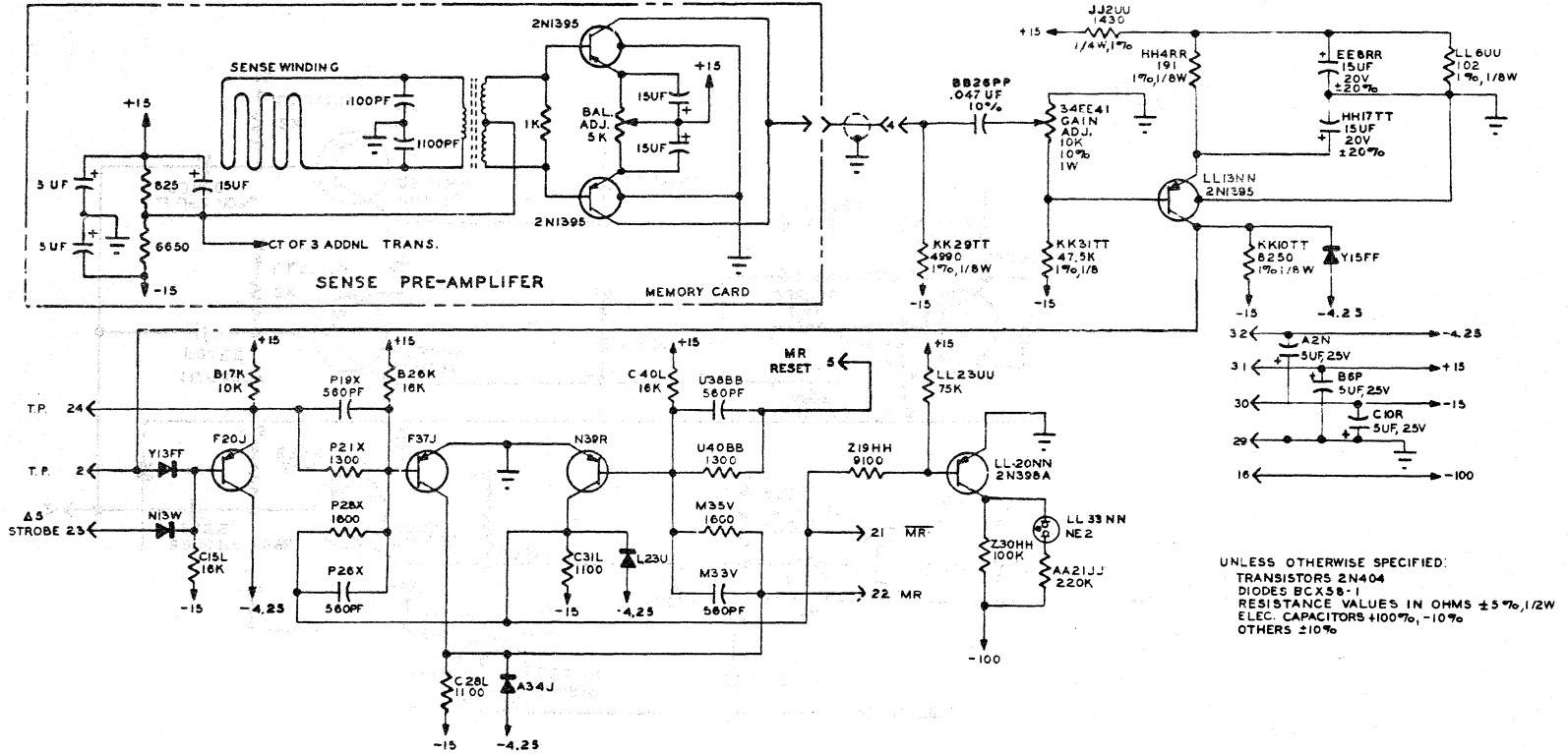
UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES ARE IN OHMS ± 5%, 1/2W
 DIODES ARE BCX58-1



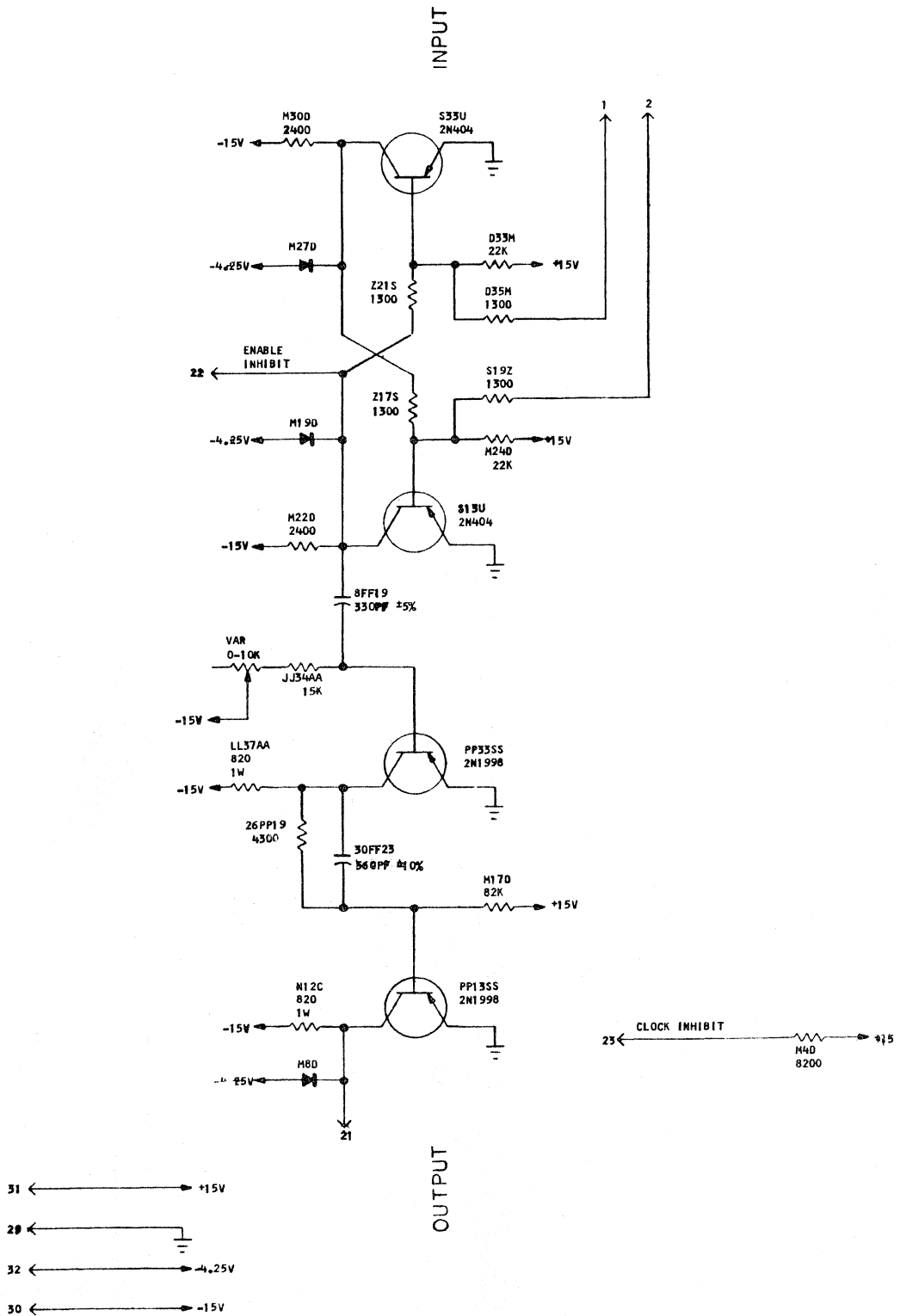
RESET STANDARDIZERS



SENSE AMPLIFIER - MR

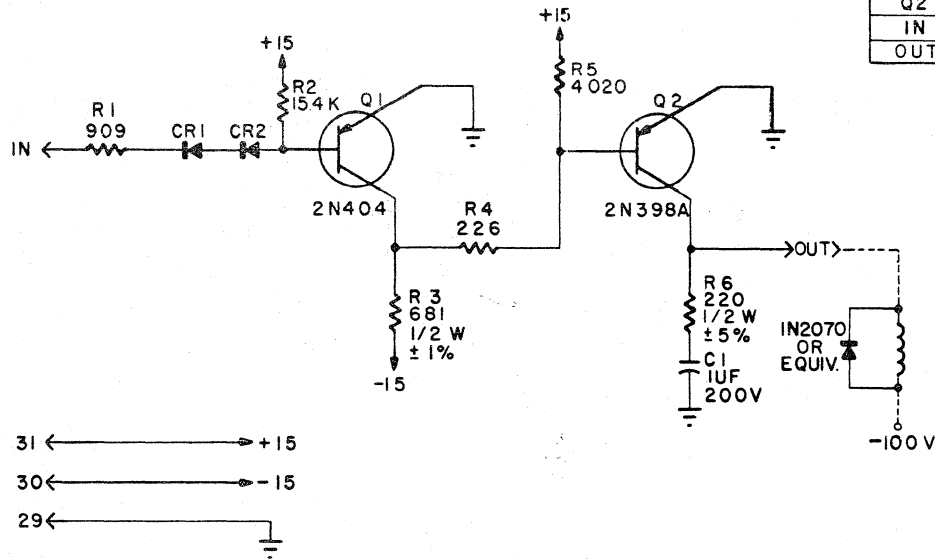


SINGLE SHOT CLOCK



SINGLE SHOT CLOCK

SOLENOID DRIVER



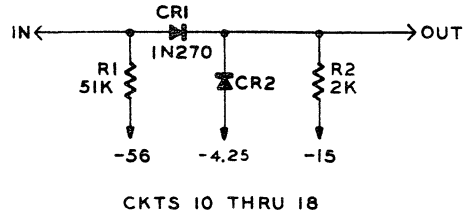
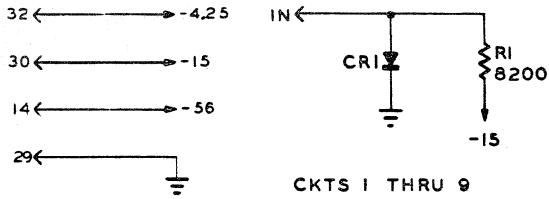
| COMP. | CKT. 1 | CKT. 2 | CKT. 3 | CKT. 4 |
|-------|--------|--------|---------|----------|
| R1 | F2P | F22P | CC 2 LL | CC 22 LL |
| R2 | C4L | C24L | JJ 4 SS | JJ 24 SS |
| R3 | C10R | C30R | DD10 SS | DD30 SS |
| R4 | M12V | M32V | AA12 JJ | Z32 HH |
| R5 | B12K | B32K | LL12 UU | KK32 TT |
| R6 | C16L | C36L | JJ16 SS | JJ36 SS |
| C1 | C19U | C39U | AA19 SS | AA39 SS |
| CR1 | C8L | C28L | JJ8 SS | JJ28 SS |
| CR2 | C6L | C26L | JJ6 SS | JJ26 SS |
| Q1 | N6R | N26R | DD6 FF | DD26 FF |
| Q2 | N15R | N35R | DD15 FF | DD35 FF |
| IN | 24 | 20 | 10 | 4 |
| OUT | 22 | 8 | 6 | 2 |

WHEN AN INDUCTIVE LOAD IS CONNECTED TO THE OUTPUT, A DAMPING DIODE MUST BE CONNECTED ACROSS THE LOAD AS SHOWN.

UNLESS OTHERWISE SPECIFIED:
 RESISTANCE VALUES ARE IN OHMS, ±1%, 1/8 W.
 CAPACITANCE VALUES ±20%
 DIODES ARE BCX58-I

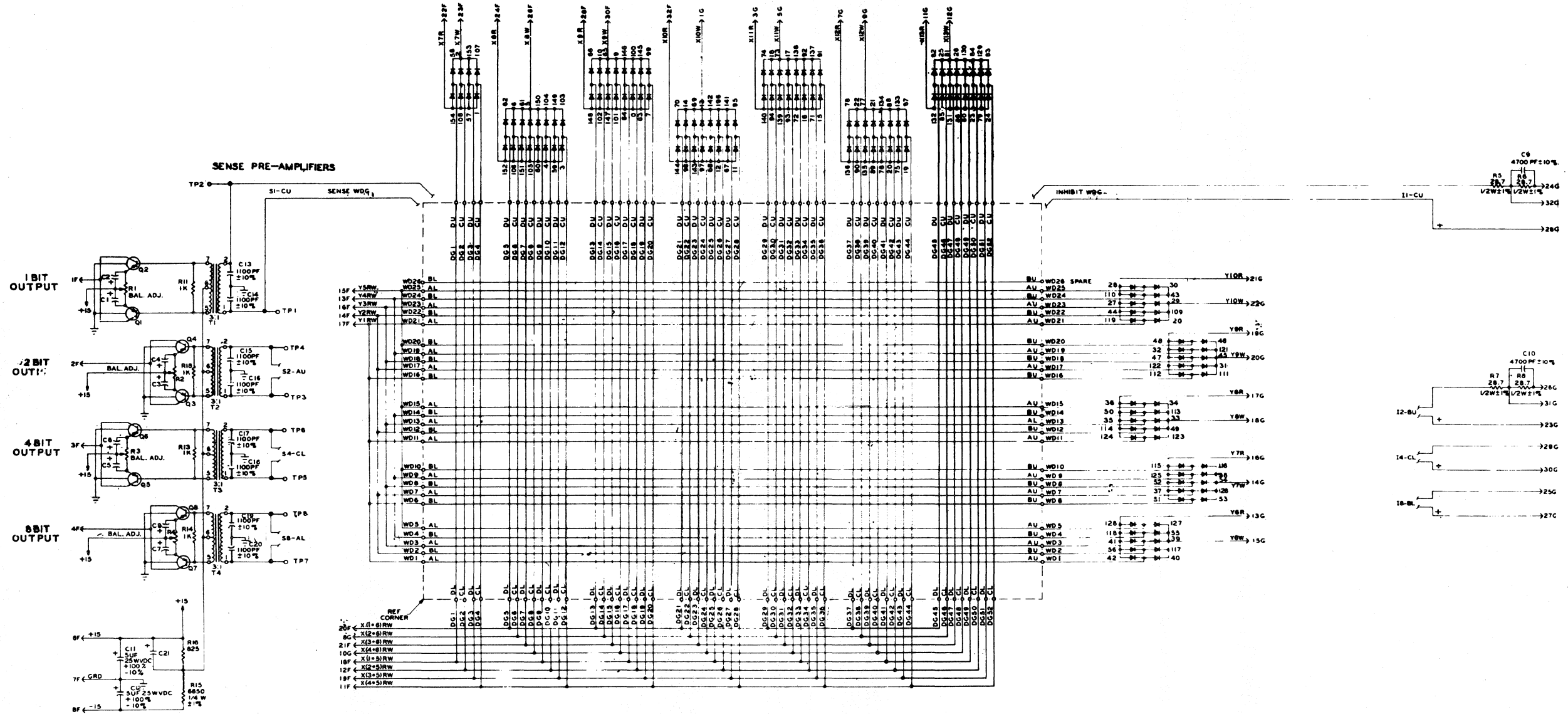
SPECIAL WETTER

| | CKT 1 | CKT 2 | CKT 3 | CKT 4 | CKT 5 | CKT 6 | CKT 7 | CKT 8 | CKT 9 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| CRI | F5P | F9P | F13P | F17P | F21P | F25P | F29P | F33P | F37P |
| RI | F7P | F11P | F15P | F19P | F23P | F27P | F31P | F35P | F39P |
| INPUT | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 21 | 20 |
| | | | | | | | | | |
| | CKT 10 | CKT 11 | CKT 12 | CKT 13 | CKT 14 | CKT 15 | CKT 16 | CKT 17 | CKT 18 |
| CRI | DD5MM | DD9MM | DD13MM | DD17MM | DD21MM | DD25MM | DD29MM | DD33MM | DD37MM |
| CR2 | U5BB | U9BB | U13BB | U17BB | U21BB | U25BB | U29BB | U33BB | U37BB |
| RI | DD7MM | DD11MM | DD15MM | DD19MM | DD23MM | DD27MM | DD31MM | DD35MM | DD39MM |
| R2 | U7BB | U11BB | U15BB | U19BB | U23BB | U27BB | U31BB | U35BB | U39BB |
| INPUT | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| OUTPUT | 15 | 16 | 17 | 18 | 19 | 10 | 11 | 12 | 13 |



UNLESS OTHERWISE SPECIFIED;
 RESISTANCE VALUES ARE IN
 OHMS, ± 5%, 1/2 W
 DIODES ARE BCX58-1

MEMORY CARD
100 WORD 12 DIGIT



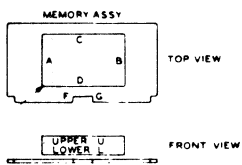
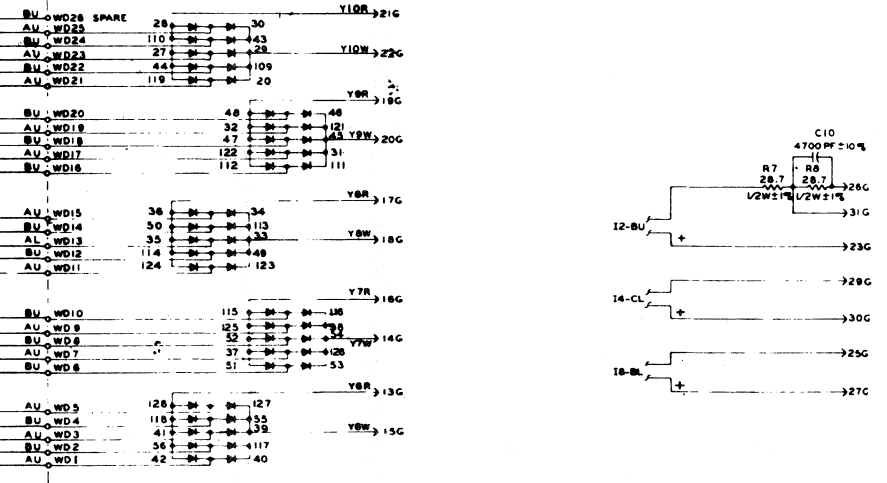
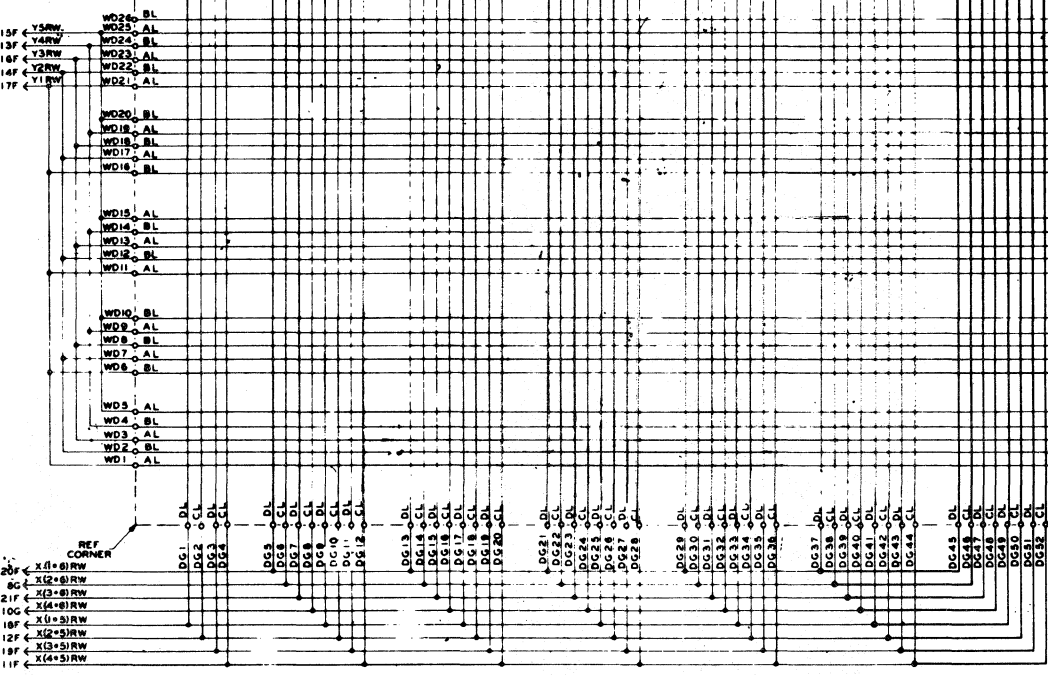
1 BIT OUTPUT

2 BIT OUTPUT

4 BIT OUTPUT

8 BIT OUTPUT

SENSE PRE-AMPLIFIERS



UNLESS OTHERWISE SPECIFIED
CAPACITORS ARE 15UF 20WVDC ± 20%
RESISTANCE VALUES ARE IN OHMS 1.0W ± 5%
DIODES ARE 1N270.
TRANSISTORS ARE 2N1395.
VAR RESISTORS ARE 5K W210%
PREFIX COMPONENT NUMBERS WITH CR.