FIELD ENGINEERING TECHNICAL MANUAL

Burroughs

B 461

HI-SPEED CORE MEMORY

Printed in U.S. America 1-15-65 B461.51

INDEX - SECTION I

1 INTRODUCTION

Printed in U.S.A.

1.1 GENERAL DESCRIPTION

The B461 Memory Unit is a high speed, random-access Memory using ferromagnetic cores as a storage media. The Memory is a self-contained Unit including Power Regulators, Current Drivers, Sense Amplifiers, Timing Circuits, and Information and Address Registers.

All circuitry in the B461 is of the solid state type with gating characteristics conforming to the B5500.

Figure 1.1-1 is a Front View and Figure 1.1-2 is a Rear View of a B461 Memory Module.

See Pages 1.1-2 & 1.1-3.

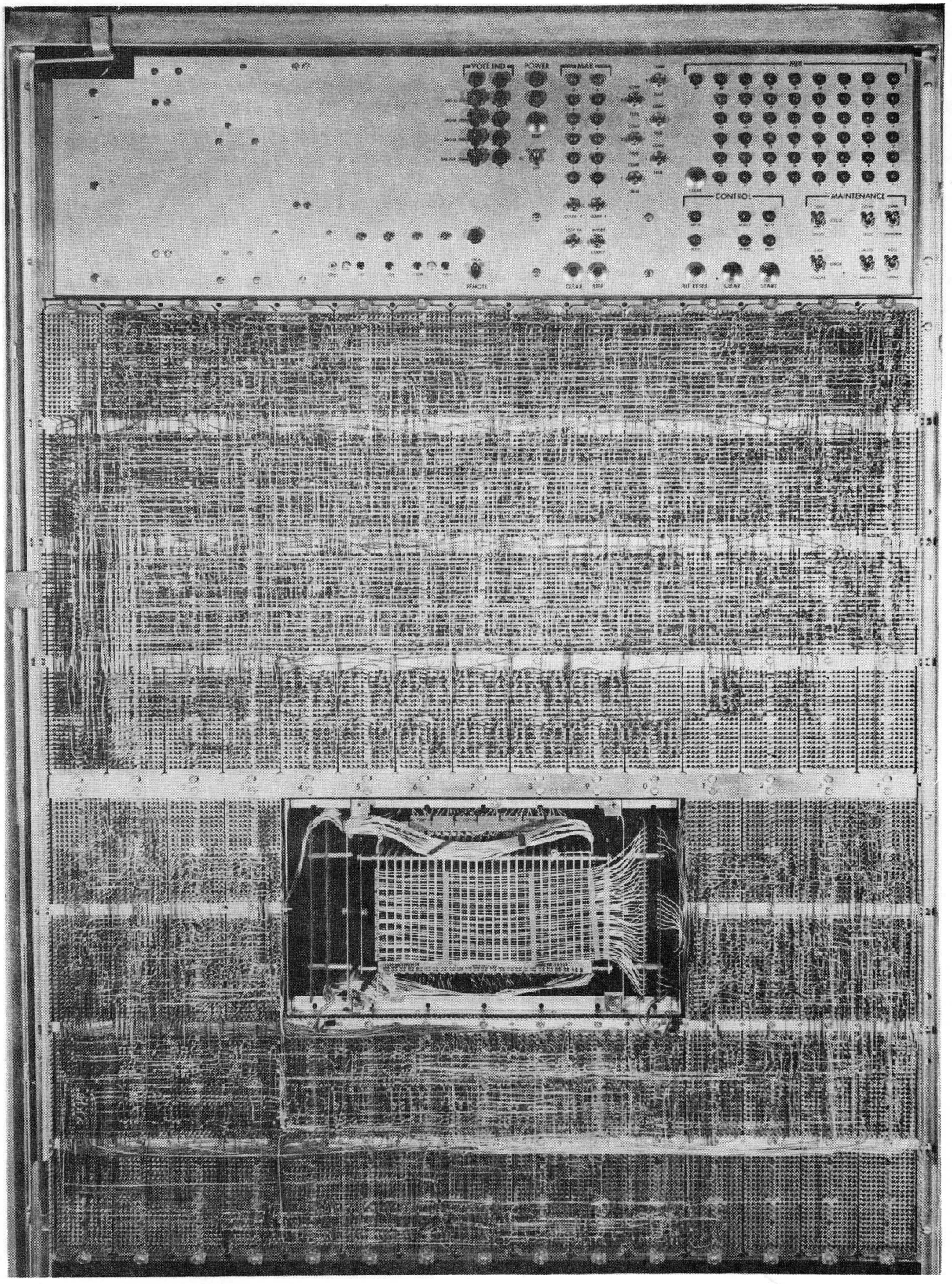


FIGURE 1.1-1
MEMORY MODULE - FRONT VIEW (WIRING SIDE)

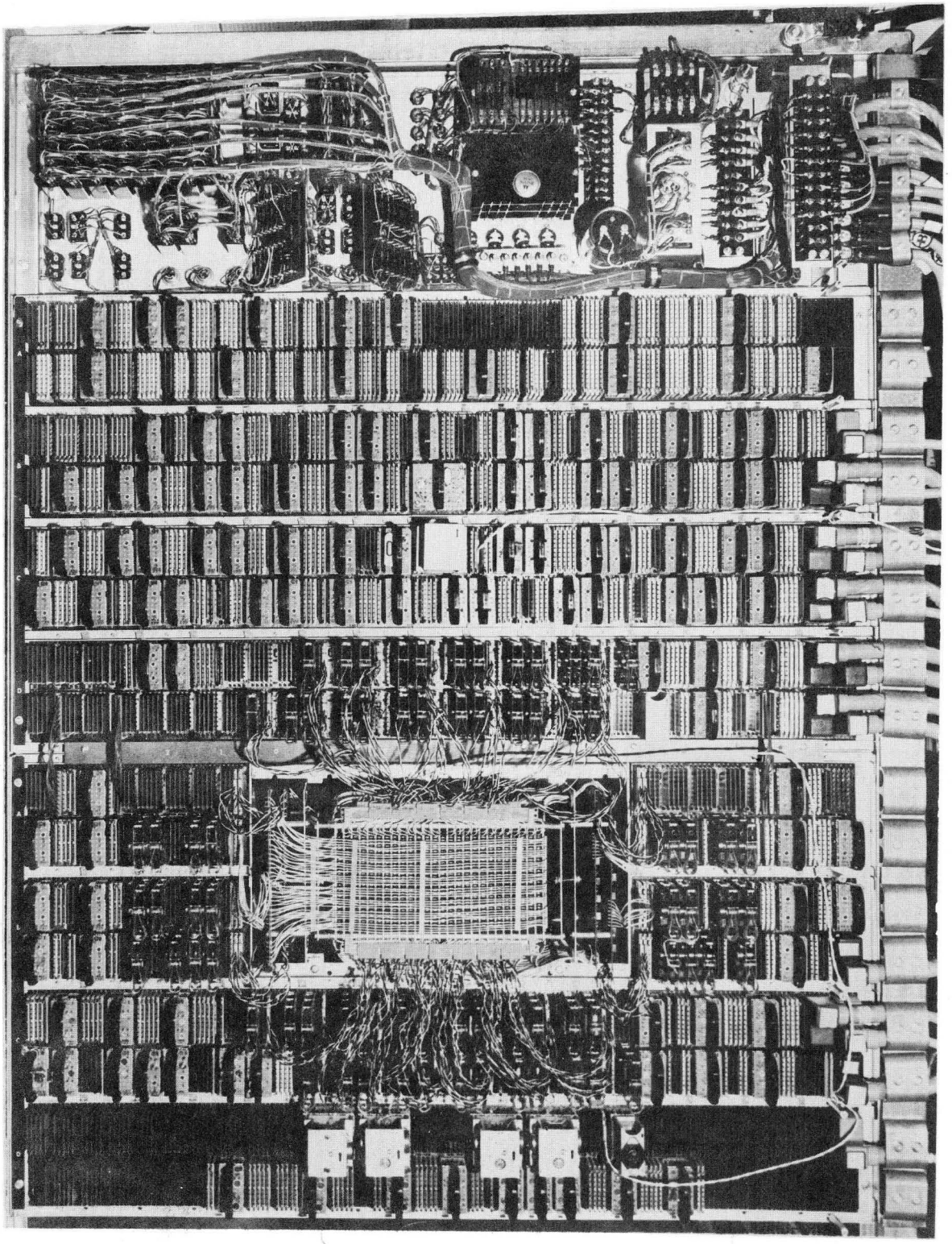
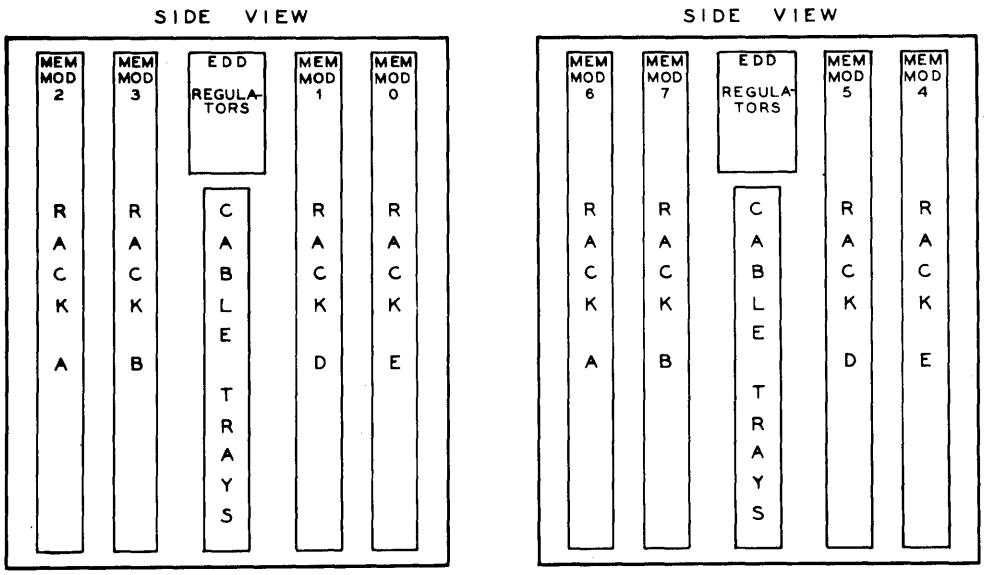


FIGURE 1.1-2
MEMORY MODULE - REAR VIEW (PACKAGE SIDE)

1.2 EQUIPMENT SPECIFICATIONS

The B461 Memory is mounted in the B5260 Cabinet of the B5500. The B5260 can contain four B461 Memory Modules. If more than four B461 Memory Modules are needed on a B5500, then a second B5260 Memory Sub-System is installed which can also contain four B461 Modules.

Figure 1.2-1 is an illustration of the B461 Modules in a B5260 Memory Sub-System with the locations of each of the Modules.



First B5260 Second B5260

FIGURE 1.2-1
B5260 MEMORY SUB-SYSTEM

The only difference between the two Sub-Systems is the numbering of the B461 Modules; 0 thru 3 in the first B5260, and 4 thru 7 in the second B5260.

Information Capacity

Each B461 Memory Module has a capacity of 4096 words. Each B5260 Sub-System can then contain 16,384 words and a maximum size Memory System with two B5260 units can consist of 32,768 words of core storage. Each word consists of 49 bits; 48 Information bits and 1 Parity bit.

Speed

The B461 has a Memory cycle time, READ or WRITE of four microseconds. The READ access time is two microseconds and the WRITE access time is one microsecond.

1.3 COMMUNICATION

Communication with a B461 by a Requesting Unit, Processor or I/O, is via the Memory Exchange portion of Central Control. Each B461 on a System is individually cabled from Central Control for all Information and Control Lines to and from the Module. The following is a list of the Communication Lines for any particular Memory Module.

Control Lines To Memory

1. 1 line Clock
2. 1 line Write Level (W00D-C)
3. 1 line Start Memory (A00S-C)
4. 12 lines Address (A01S-C thru A12S-C)
5. 48 lines Write Information (W01S-C thru W48S-C)
6. 1 line Single Pulse Status (SPUL/)
7. 1 line Master Clear

Control Lines From Memory

1. 1 line Cable Interlock (CINL/)
2. 1 line Memory Parity Error (MERF)
3. 4 lines Memory Timing
   a. 1 line Read Obtained Line (MWCF)
   b. 1 line Memory Cycle Finished Not (MCFS/)
   c. 2 lines Read Access Obtained Lines (RAØD & RAØS/)
4. 49 lines Read Information (I01F/ thru I48F/ and I48F)
5. 1 line Memory Not Available (MNAL)

1.4 POWER & POWER CONTROL

All power required by a B461 Memory Module is obtained from the B5500 Power Supply. This power is delivered to the B5260 Memory Sub-System, then distributed to the Memory Modules. Power sequencing is controlled by the B5500 and each Memory Module. Over and Under Voltage Sensing circuitry is provided in each Memory Module and Thermal protection in each Memory Sub-System.

The following is a list of the Power and Power Control lines to a Memory Sub-System.

11 lines	DC Power Input
1 line	Logic Ground
1 line	-24 Volt Ground
1 line	Excess Current Sensing
3 lines	Voltage Sensing
1 line	DC Lockout Sensing
1 line	Temperature Sensing

1.5 OFF-LINE FUNCTIONS

Off-line functions are accomplished within each individual Module and are used for maintenance and testing of the Memory. The testing of a Memory is divided into three categories:

1. Manual
2. Automatic
3. Checkerboard

These three modes of testing will be explained in Section 6 of this manual.

An additional Off-line maintenance feature is that DC Power can be turned ON and OFF in a particular Module without affecting the remainder of the System.

1.6 GLOSSARY OF TERMS

AØØS ..... Memory Start from Central Control
A01S thru A12S ..... Address Lines from Central Control
A+1D ..... Address Register Plus One Driver
A+1L ..... Address Register Plus One Level
A+1S/..... Address Register Plus One Not Switch
A+1S ..... Address Register Plus One Switch
ACDF ..... Address Counter Delay Flip-Flop
A01F thru A12F ..... Address Register Flip-Flops
AX1S thru AX6S ..... Address X Switches
AX1S/ thru AX6S/ ..... Address X Not Switches
AY1S thru AY6S ..... Address Y Switches
AY1S/ thru AY6S/ ..... Address Y Not Switches

CAG001 ..... AX1S · AX2S · CØXL · (A+1D)
CAG002 ..... AX1S · AX2S · AX3S · AX4S · CØXL · (A+1D)
CAG003 ..... CØYD · AY1S · AY2S
CAG004 ..... CØYD · AY1S · AY2S · AY3S · AY4S
CAG005 ..... AX1S · AX2S · AX3S · AX4S · AX5S · AX6S · AY1S · AY2S · AY3S · AY4S · AY5S · AY6S
CAG006 ..... PC3S · TRMS/ · MANS/
CAG007 ..... MSTL · MP1F/ · MP2F/ · MSTF · MANS/
CAG008 ..... MP1F · MP2F · MSTF · MANS/
CCP-1 thru CCP-6 ..... Local Clock Driver Output
1CLP-1 ..... Local Clock Oscillator Output 1
1CLP-2 ..... Local Clock Oscillator Output 2
1MCP ..... Local 1 Megacycle Pulse
CØYD ..... Count Y Driver
CTUS ..... Continue Switch
ØAAS ..... Parity Odd I01F thru I04F Switch
EAAS ..... Parity Even I01F thru I04F Switch
ØBAS ..... Parity Odd I05F thru I08F Switch
EBAS ..... Parity Even I05F thru I08F Switch
ØCAS ..... Parity Odd I09F thru I12F Switch
ECAS ..... Parity Even I09F thru I12F Switch
ØDAS ..... Parity Odd I13F thru I16F Switch
EDAS ..... Parity Even I13F thru I16 F Switch

ØEAS ..... Parity Odd I17F thru I20F Switch
EEAS ..... Parity Even I17F thru I20F Switch
ØFAS ..... Parity Odd I21F thru I24F Switch
EFAS ..... Parity Even I21F thru I24F Switch
ØGAS ..... Parity Odd I25F thru I28F Switch
EGAS ..... Parity Even I25F thru I28F Switch
ØHAS ..... Parity Odd I29F thru I32F Switch
EHAS ..... Parity Even I29F thru I32F Switch
ØIAS ..... Parity Odd I33F thru I36F Switch
EIAS ..... Parity Even I33F thru I36F Switch
ØJAS ..... Parity Odd I37F thru I40F Switch
EJAS ..... Parity Even I37F thru I40F Switch
ØKAS ..... Parity Odd I41F thru I44F Switch
EKAS ..... Parity Even I41F thru I44F Switch
ØLAS ..... Parity Odd I45F thru I48F Switch
ELAS ..... Parity Even I45F thru I48F Switch
ØABS ..... Parity Odd AA thru DA Switch
EABS ..... Parity Even AA thru DA Switch
ØBBS ..... Parity Odd EA thru HA Switch
EBBS ..... Parity Even EA thru HA Switch
ØCBS ..... Parity Odd IA thru LA Switch
ECBS ..... Parity Even IA thru LA Switch
I01D thru I49D ..... Inhibit Drivers
I01F thru I49F ..... Information Register Flip-Flops
MACD ..... Memory Address Register Clear Driver
MANS/ ..... Manual Not Switch
MC1D ..... Maintenance Control 1 Bit Driver
MC2D ..... Maintenance Control 2 Bit Driver
MC4D ..... Maintenance Control 4 Bit Driver
MC8D ..... Maintenance Control 8 Bit Driver
MCAD ..... Maintenance Control A Bit Driver
MCBD ..... Maintenance Control B Bit Driver
MC1S/ ..... Maintenance Control 1 Bit Not Switch
MC2S/ ..... Maintenance Control 2 Bit Not Switch
MC4S/ ..... Maintenance Control 4 Bit Not Switch
MC8S/ ..... Maintenance Control 8 Bit Not Switch
MCAS/ ..... Maintenance Control A Bit Not Switch

MCBS/ ..... Maintenance Control B Bit Not Switch
MCFS/ ..... Memory Cycle Finished Not Switch
MERF ..... Memory Error Flip-Flop
MICD-1 ..... Memory Information Register Clear Driver 1
MICD-2 ..... Memory Information Register Clear Driver 2
MICM ..... Memory Information Clear Multi
MIHD ..... Memory Inhibit Driver
MIHM ..... Memory Inhibit Multi
MIHS/ ..... Memory Inhibit Not Switch
MISD ..... Memory Input Strobe Driver (Remote Write)
MP1F ..... Memory Pulse Counter 1 Flip-Flop
MP2F ..... Memory Pulse Counter 2 Flip-Flop
MR2M ..... Memory Read 2 Multi
MRWP ..... Memory Read to Write Delay Pulse
MS1M ..... Memory Switch 1 Multi
MSTD ..... Memory Start Driver
MSTF ..... Memory Start Flip-Flop
MSTL ..... Memory Start Level
MSTS ..... Memory Start Switch
MSTS/ ..... Memory Start Not Switch
MW2M ..... Memory Write 2 Multi
MW2S ..... Memory Write 2 Multi Switch
MWCF ..... Maintenance Worst Case Flip-Flop
MWRF ..... Memory Write Flip-Flop
P03S ..... Pulse Counter Equals 0 or 3 Switch
PC2D ..... Pulse Counter Equals 2 Driver
PC1S ..... Checkerboard Control Logic 1 Switch
PC2S ..... Checkerboard Control Logic 2 Switch
PC3S ..... Checkerboard Control Logic 3 Switch
PC4S ..... Checkerboard Control Logic 4 Switch
PERL ..... Parity Error Level
RAØD ..... Read Access Obtained Driver
RAØS/ ..... Read Access Obtained Not Switch
RISD-1 ..... Read Information Strobe Driver 1
RISD-2 ..... Read Information Strobe Driver 2
RISD-3 ..... Read Information Strobe Driver 3

RISD-4 ..... Read Information Strobe Driver 4
RSPD-1 ..... Reset Single Pulse Driver 1
RSPD-2 ..... Reset Single Pulse Driver 2
S1BS ..... Sense 1 Bits Switch
S1BS/ ..... Sense 1 Bits Not Switch
S2BS ..... Sense 2 Bit Switch
S2BS/ ..... Sense 2 Bits Not Switch
S4BS ..... Sense 4 Bits Switch
S4BS/ ..... Sense 4 Bits Not Switch
S8BS ..... Sense 8 Bits Switch
S8BS/ ..... Sense 8 Bits Not Switch
SABS ..... Sense A Bits Switch
SABS/ ..... Sense A Bits Not Switch
SBBS ..... Sense B Bits Switch
SBBS/ ..... Sense B Bits Not Switch
S01P thru S49P ..... Sense Amplifiers
SPUS ..... Single Pulse Switch
STTP ..... Strobe Timing Pulse
TRMS/ ..... Remote Not Switch
WISD-1 ..... Write Information Strobe Driver 1
WISD-2 ..... Write Information Strobe Driver 2
XR0D thru XR7D ..... X Axis Read Driver
XW0D thru XW7D ..... X Axis Write Driver
X00S thru X70S ..... X Axis Switch Output
X00G thru X70G ..... X Axis Switch Return
YR0D thru YR7D ..... Y Axis Read Driver
YW0D thru YW7D ..... Y Axis Write Driver
Y00S thru Y70S ..... Y Axis Switch Output
Y00G thru Y70G ..... Y Axis Switch Return

INDEX - SECTION 2

2. PRINCIPLES OF OPERATION

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2.1 ON-LINE OPERATION

The B461 Core Memory is designed to operate with the B5500. All interconnecting lines conform to the requirements of the B5220 Central Control for Timing and Information flow. The following is a list of the inter-connecting lines between Central Control and the Core Memory.

Central Control to Core Memory

1. AnnS - 12 lines labeled A01S thru A12S, Address lines to the Address Register in Memory.
2. A00S - 1 line, Memory Start Pulse to initiate a Memory cycle.
3. W00D - 1 line, occurs at the same time as A00S, used to indicate a Memory Write Operation.
4. SPUL/ - 1 line, indicates that the System Clock Control switch in D & D is in the NORMAL position.
5. WnnS - 48 lines labeled W01S thru W48S, Write Information to the Memory Information Register.

CORE MEMORY to Central Control

1. InnF - 49 lines labeled I01F/ thru I48F/ and I48F, Memory Read Information from the Memory Information Register to Central Control.
2. MCFS/ - 1 line labeled MT4F/ in Central Control, used to clear the Cross-point Flip-flop and Memory cycle Flip-flop at the end of a Memory access.
3. MWCF - 1 line labeled MRØF in Central Control, gates the Read Information lines from Central Control to Processor.
4. RAØD - 1 line labeled MT2F in Central Control, develops MT2F to the Processor to indicate Read Information is in the Memory Information Register.
5. RAØS/ - 1 line labeled MT2F/ in Central Control, develops MT2S to the I/O Channels to indicate that the Read Information is in the Memory Information Register.
6. MERF - 1 line labeled MPEF in Central Control, indicates a Parity Error in Memory during a Memory Read access.

The various Logical Units of the Memory Module, as indicated in Figure 2.1-1, are the Logical Units of the Memory Module used during an On-Line operation. These Units serve the following functions:

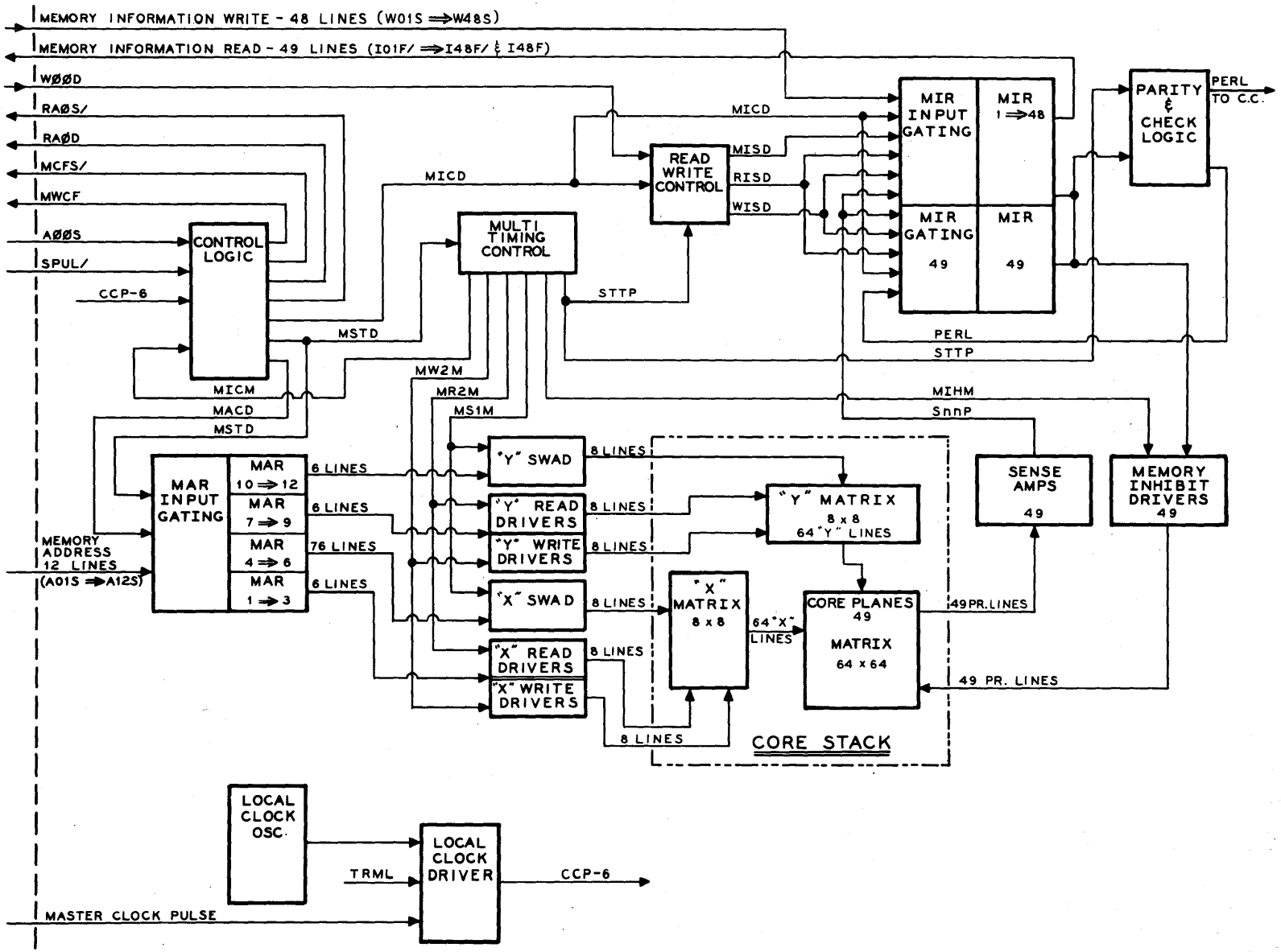


FIGURE 2.1-1
BLOCK DIAGRAM CORE MEMORY LOGIC

1. Control Logic - Controls all Memory functions which depend upon the System Clock. It also develops the Control levels that go to Central Control.

2. Multi Timing Control - Initiated by MSTD from the Control Logic; but once initiated, continues on its own, completely independent of the System Clock. This circuit is used to control all Addressing and Information lines to and from the Core Stack.

3. Read/Write Control - Retains the fact that a Memory Access is a Read or Write. Controls the flow of Information for either a Read or a Write operation.

4. MIR & Parity - MIR is a temporary storage for Information going to or from the Core Stack. The Parity circuitry uses the Information in the Information Register (MIR) to generate the correct Parity during a Write Access and to check for correct Parity during a Memory Read Access.

5. Address - The Addressing portion of Figure 2.1-1 consists of the Address Register, the Address switches, and the Read/Write Drivers. The Address Register contains the Core Address being accessed and in turn will determine the Address switch and Read/Write Driver to be used. The Address switch and Read/Write Driver outputs go to the "X" and "Y" Transformer Matrices to select one of the Transformers which will in turn select one of the 64 "X" lines and "Y" lines to the Core Stack.

Information Flow

The flow of Information during a Memory Write Access is from Central Control via the Memory Information Write lines to MIR 1 thru 48. While this Information is in MIR, the correct Parity is generated by the Parity generation circuitry and set into MIR 49. During the Write phase of the Memory Access, the information is transferred into the Core Stack via the 49 Inhibit Drivers.

The flow of Information during a Memory Read Access is from the Core Stack to MIR via the 49 Sense Amps. The outputs of the Sense Amps are strobed into MIR with the Strobe Timing Pulse (STTP). While the Information is in MIR, the Parity circuitry checks the 49 bits for correct Parity. If the Parity is in error, then the Error Flip-Flop (MERF) is set to indicate this condition to Central Control.

After Parity is checked, the Information in MIR is transferred to Central Control via the Memory Information Read lines. Only bits 1 thru 48 are transferred to and from the Memory Module. Bit 49 is the Parity bit and its status (ON or OFF) is determined in the Memory and remains in the Memory Module.

Central Control Operation

The function of Memory Exchange in Central Control is to logically con-

nect a Memory Module with an Accessing Unit (Processor or I/O). The Control and Information lines will be gated through Memory Exchange between the Accessing Unit and the Memory Module.

When the Processor or I/O requests a Memory Access and that access can be accomplished, the Cross-point Flip-Flop in Central Control is set (Unclocked). See Figure 2.1-2.

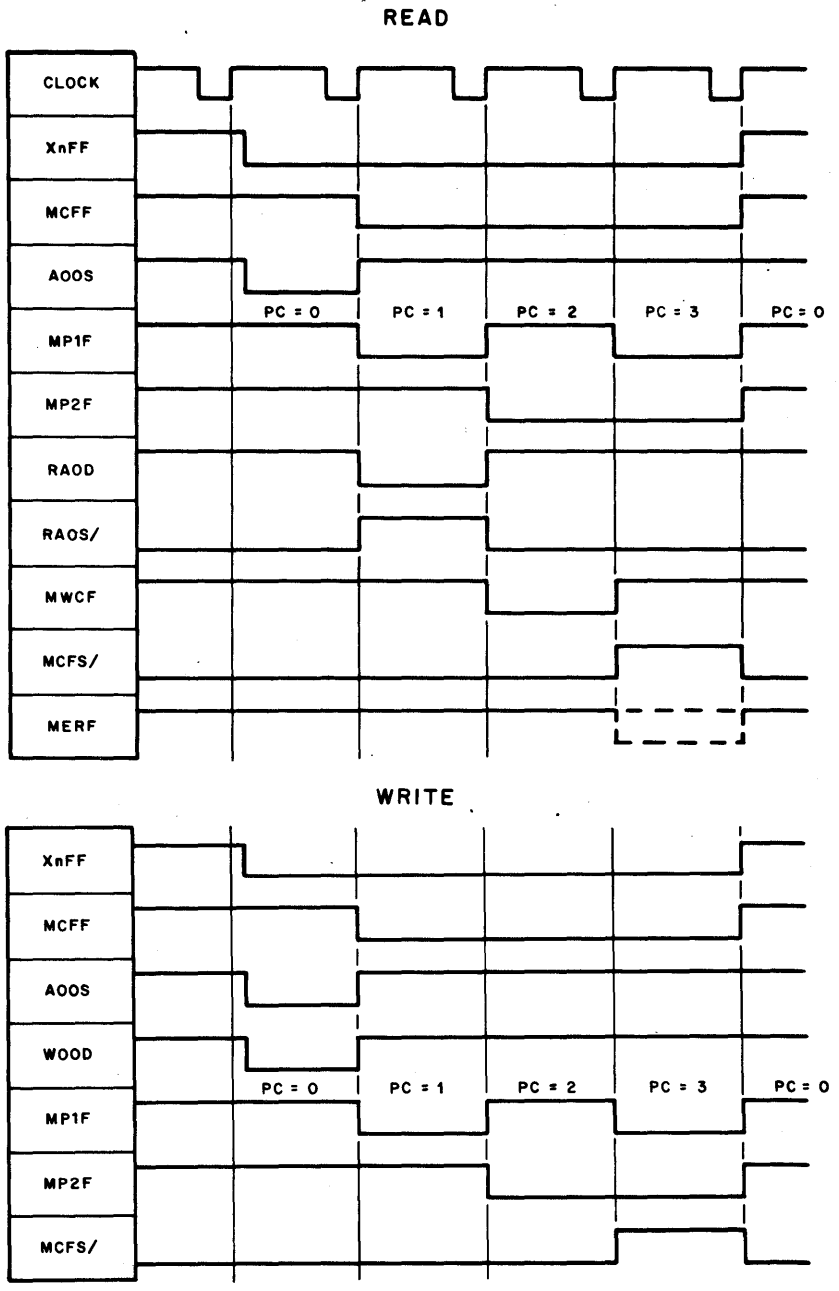


FIGURE 2.1-2
MEMORY TO CENTRAL CONTROL TIMING

With the Cross-point set, level A00S (Memory Start) is developed in Central Control and sent to the Memory Module. If the operation is a

Memory Write, then the Memory Write Level(W00D) is also sent to the Memory Module. A00S will initiate the Memory operation in the Memory Module, and W00D will allow the Information to be written to be set into the Information Register and set the Memory Write Flip-Flop (MWRF).

In the Memory Module, the Pulse Counter is counted with each Clock Pulse from 0 to 3 and back to 0. Its purpose is to determine when the Logical levels will be TRUE to keep the Logical operation of the Memory and Central Control in sync with the Multi Timing to the Core Stack.

The Logical levels RA0D, RA0S/ and MCFS/ are developed from the Pulse Counter to gate the Processor or I/O and the Central Control during a Memory Access. The terms RA0D, RA0S/, MWCF and MERF are used only during a Memory Read operation. The only term used during a Write operation is MCFS/. Its use is to indicate to Central Control that a Memory operation is completed, clearing the Memory Cross-point and Memory cycle flip-flop.

Memory Operation

The functions which occur in the Memory Module during a Memory operation are controlled by the Memory Pulse Counter and the Multi Timing circuitry. The Pulse Counter controls those functions which use the 1 meg. Clock instead of the Multis for their timing. The Multi timing, initiated by the 1 meg. Clock, is completely asynchronous in its operation.

Referencing Figure 2.1-3, the Memory operation is started when MSTD (Memory Start Driver) is TRUE. MSTD with the T_0 Clock Pulse will set the Address Register(AnnF) and initiate the Multi Timing by triggering MS1M (Memory Switch 1 Multi). This Multi will be TRUE for the entire Memory cycle, approximately 3 microseconds. Occurring with MSTD is the level MISD (Memory Input Strobe Driver) for a Write operation only. MISD will set the Information Register (InnF) to the information to be written and set the Memory Write Flip-Flop (MWRF).

The next occurrence is in the Multi Timing. MS1M sets MR2M (Memory Read 2 Multi). With MS1M and MR2M both TRUE, a destructive Read of the Stack is done. At Strobe Time (STTP), bit 49 in the Information Register will be set (or not set) to generate the correct Parity in the Information Register. The Clock Pulse T_1 occurs during the Read portion of the Memory cycle and its only function for a Write operation is to count the Pulse Counter to two. While the Pulse Counter is at a value of two, the Read out is terminated with the time out of MR2M which in turn sets MRWP (Memory Read to Write Delay Pulse). MRWP in turn, triggers MIHM (Memory Inhibit Multi). MIHM turns on the Inhibit Drivers that are associated with those bits in the Information Register that are in the "zero" state. MIHM also turns on the Memory Write 2 Multi (MW2M) to drive Write current in the "X" and "Y" lines in the Core Stack.

During the Write portion of the Memory cycle, the T_2 Clock Pulse will count the Pulse Counter to Three. With the Pulse Counter equal to three, the level MCFS/ (Memory Cycle Finished Not Switch) goes FALSE.

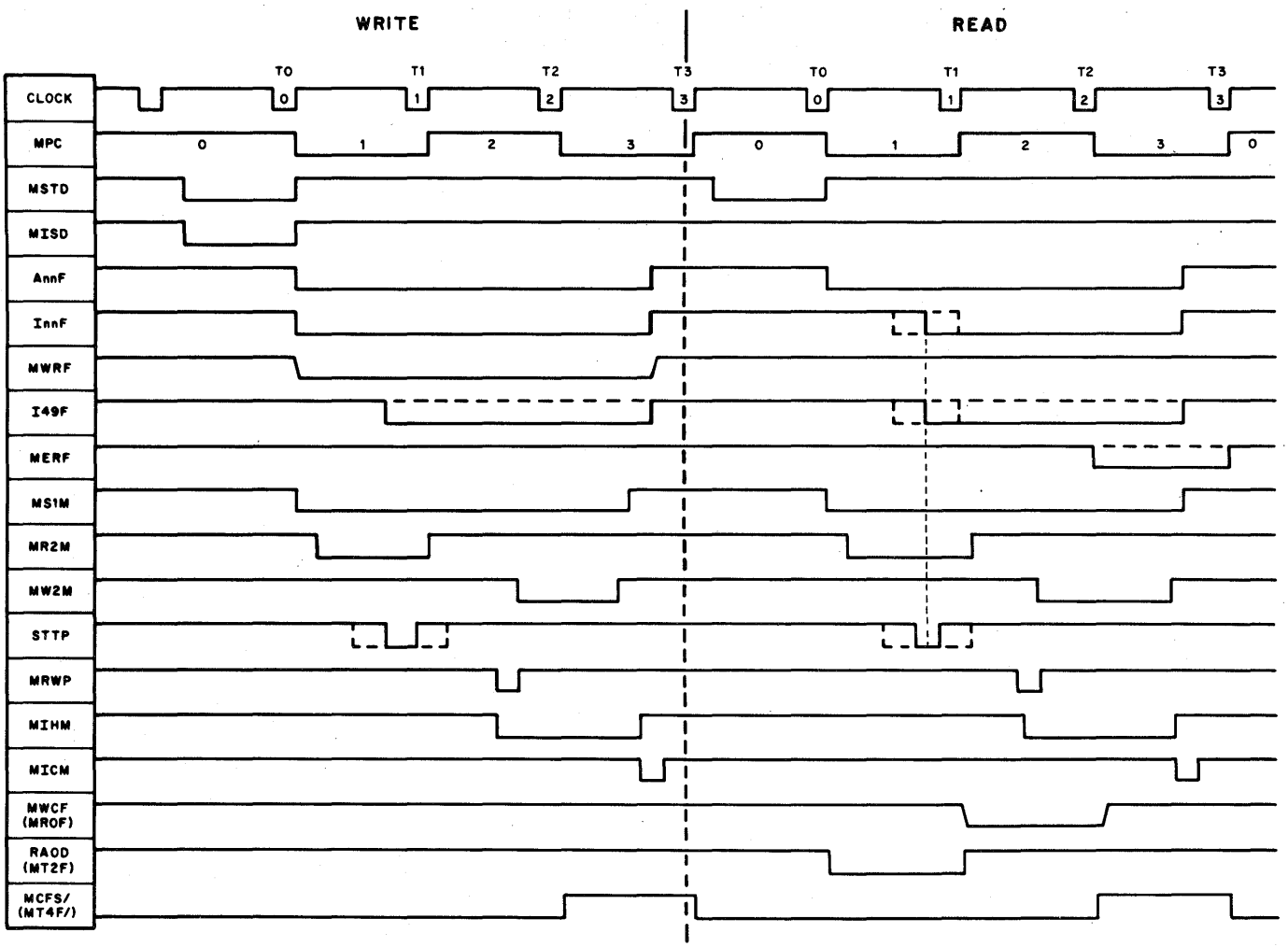


FIGURE 2.1-3
REMOTE MEMORY TIMING

This FALSE level, with the T_3 Clock Pulse, indicates to Central Control that the Memory operation is complete. The T3 Clock Pulse will count the Pulse Counter back to zero, and with MCFS/ FALSE, the same Clock Pulse will clear the Cross-point and Memory cycle Flip-Flops in Central Control. In the Multi Timing, at approximately the same time as T_3, MS1M and MW2M and MIHM will time out. MIHM timing out will set MICM (Memory Information Register Clear Multi) which will result in clearing the Memory Module.

In a Memory Read operation, the actions of the Pulse Counter and Multi Timing are identical to the Memory Write operation. During a Read operation, the level MISD remains FALSE. This results in the Information Register and MWRF remaining in the "Zero" state. When STTP occurs during the Read phase of the operation, the information being read from the Stack is set into the Information Register, including the Parity bit I49F. The Parity circuit will check the information in the Information Register and if a Parity Error exists (even number of bits ON in the Information Register), MERF (Memory Error Flip-Flop) will be set with T_2 Clock Pulse.

Other differences between a Read and a Write operation are in the Logical levels sent to the Central Control. During a Memory Read operation (indicated by MWRF in the "zero" state), the RAOD level will be TRUE when the Pulse Counter is equal to one. This allows the accessing Unit (Processor or I/O) to prepare to accept the Read information from Memory at Clock Pulse T_2. MWCF is TRUE when the Pulse Counter equals two. This indicates to Central Control that the Read information can now be transferred to the Processor. MCFS/ serves the same purpose in a Memory Read Operation as it did in a Memory Write operation, clearing the flip-flops in Central Control at T_3.

Clocked Flow

The Core Memory flow charts are separated into two groups, Clocked and Unclocked. The description of these flows will cover the two groups separately. The described actions will be identified as to their respective MPC values (Memory Pulse Counter).

MPC = 0

All actions occurring at this MPC count require the Memory Module to be in Remote (TRML). Reference Figure 2.1-4.

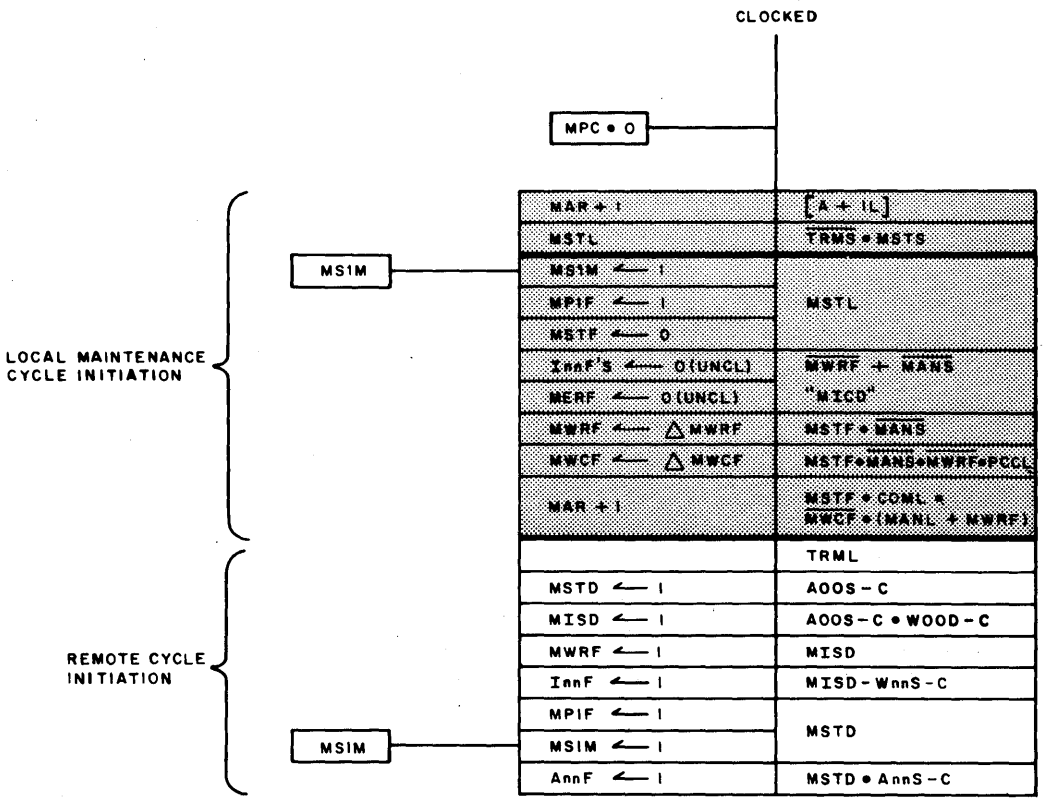


FIGURE 2.1-4
MPC = 0 FLOW

MSTD ← 1 (Unclocked)

With the Start Pulse from Central Control (A00S-C), the Memory Start Driver will go TRUE to start the Memory operation.

MISD ← 1 (Unclocked)

If the Memory operation is a Memory Write, then the Memory Input Strobe Driver will go TRUE at the start of the Memory cycle (A00S-C • W00D-C).

MWRF ← 1

Set the Memory Write flip-flop if this is a Memory Write operation as indicated by MISD being TRUE.

InnF ← 1

Set the information to be written into the Information Register as specified by the Write Information lines (MISD • WnnS-C). The nn in this case are the values of 01 thru 48.

MP1F ← 1, MS1M ← 1

Set MP1F to give the Pulse Counter a value of "one" in preparation for the next sequence operation. With MSTD, set the MS1M multi to initiate the Multi Timing to the Core Stack.

AnnF ← 1

Set the Address of the Core Stack into the Memory Address Register at the start of the operation (MSTD • AnnS-C). AnnS-C are the 12 Address lines from Central Control.

MPC = 1

For the flow chart of this MPC value, refer to Figure 2.1-5.

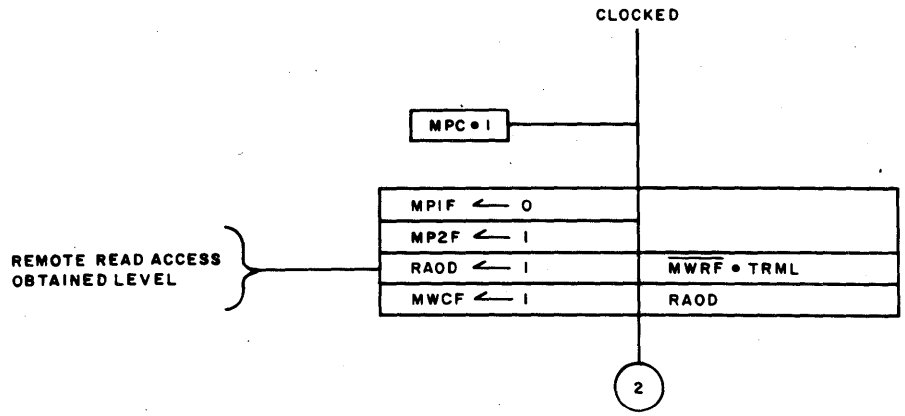


FIGURE 2.1-5
MPC = 1 FLOW

Unconditionally increase the value of the Pulse Counter by "one" (MP1F to 0 and MP2F to 1).

RAOD ← 1

While the Pulse Counter is at a value of "one", allow the Remote Read Access Obtained Level to be TRUE to Central Control if the Memory operation is a Read and the Memory Module is in REMOTE (MWRF/ · TRML).

MWCF ← 1

With RAOD, the operation is a Read. Set MWCF.

MPC = 2

For the actions listed for this MPC value, refer to Figure 2.1-6.

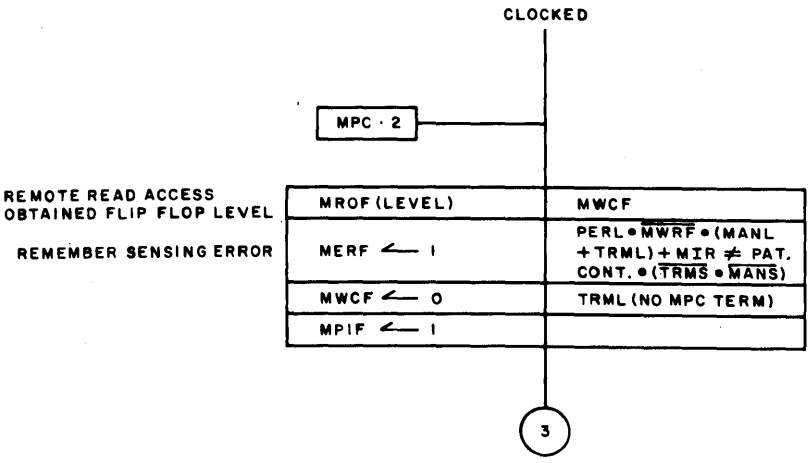


FIGURE 2.1-6
MPC = 2 FLOW

MROF (Level)

With MWCF set, the MROF level is developed in Central Control to gate the Information lines from Central Control to the Processor. If the Accessing Unit is an I/O channel, then this level will not effect Central Control.

MERF ← 1

There are two conditions by which MERF can be set. The one that is used when in a REMOTE operation is the term PERL · MWRF/ · (MANL + TRML). PERL will be TRUE if an even number of bits are ON in the Information Register indicating a Parity Error during a Read operation (MWRF/).

If the Memory is being operated in REMOTE or MANUAL (TRML + MANL), then set the Memory Error Flip-Flop (MERF to 1).

MWCF ← 0

Set MWCF to zero when in REMOTE (TRML).

MP1F ← 1

Unconditionally set MP1F to one at MPC = 2 to increase the Pulse Counter to a value of three.

MPC = 3

For all actions occurring at this MPC count, refer to Figure 2.1-7.

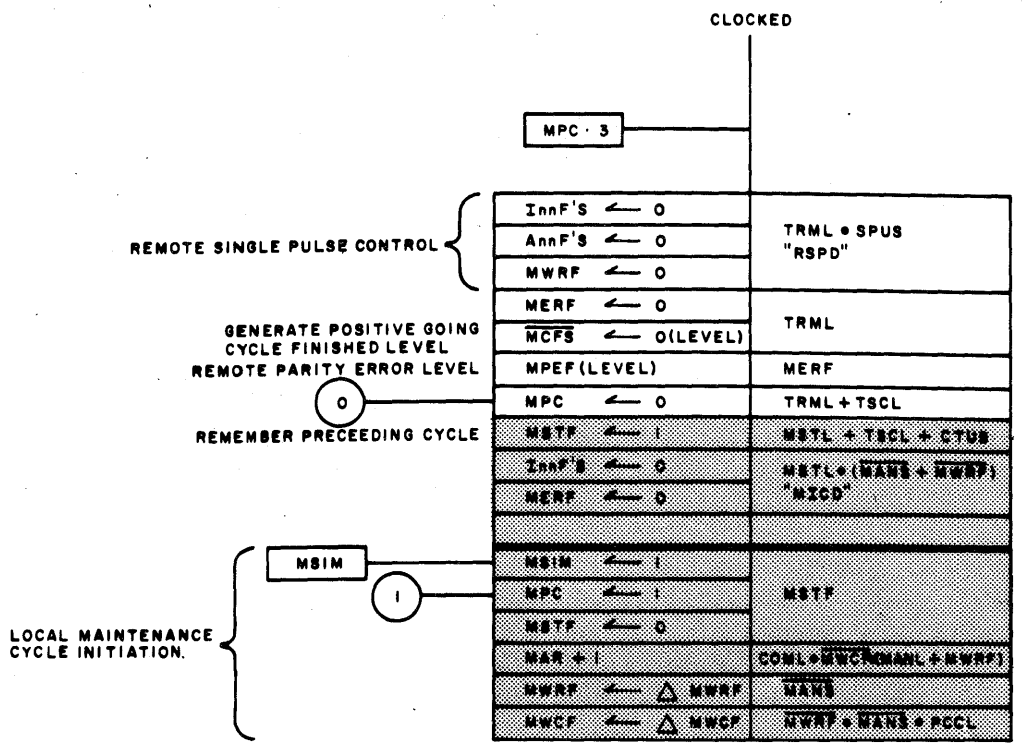


FIGURE 2.1-7
MPC = 3 FLOW

InnFs ← 0, AnnFs ← 0, MWRF ← 0

When terminating a Memory operation, it is necessary to clear the Memory Module in order to have all flip-flops in the "zero" state at the start of some future Memory operation. If the System Clock is in single or double pulse, then the clearing of some of the Module will be done with a Clock pulse via the Remote Single Pulse Driver (RSPD). RSPD = TRML · SPUS, the Memory Module in Remote and the System Clock not in the Normal Mode. If this condition exists, then clear the Information Register (InnFs), the Address Register (AnnFs), and the Memory Write Flip-flop (MWRF).

MERF ← 0, MCFS/ ← 0

When operating in REMOTE, unconditionally set the Error Flip-flop to zero; and with MPC = 3, the MCFS/ level goes FALSE to Central Control. This level will result in the controlling flip-flops in Central Control being cleared.

MPEF (Level)

If a Memory Parity Error existed in the Read operation, then MERF will be ON. With MERF in the "one" state, develop the Memory Parity Error Level (MPEF) in Central Control.

MPC ← 0

When in REMOTE, and at MPC = 3, unconditionally set the Memory Pulse Counter to zero. This results in the termination of the Memory operation. At MPC = 0, a Memory Start is needed from Central Control for any more actions to take place. Refer to Figure 2.1-4.

Unclocked Flow

The Unclocked flow is primarily concerned with the Multi Timing and those functions which are a result of the multis. The Multi Timing circuitry is initiated by MSTD and a Clock pulse at MPC = 0, (see Figure 2.1-4) by setting the MS1M multi. Once MS1M is set, the multi train will continue to completion, completely independent of the System Clock as described below.

NOTE

All timings given in this section of the Manual are approximations only. For exact timings of the Multis, refer to Section 5 of this Manual.

MS1M

MS1M is turned ON at the start of a Memory operation and remains ON for the entire Memory operation, approximately 3 microseconds. MS1M enables the Address switches selected by the Address in the Address Register. Refer to Figure 2.1-8.

MR2M ← 1

MR2M is turned ON by MS1M if the Inhibit multi is OFF (MIHM/). MR2M is on for approximately 1.0 microsecond and enables the "X" and "Y" Read drivers to drive Read current in the Core Stack.

MR2M

While MR2M is TRUE, the Strobe Pulse will occur approximately 630 nanoseconds after the Leading Edge of MR2M. The Strobe Pulse (STTP) will gate several functions during the Read phase of the Memory operation.

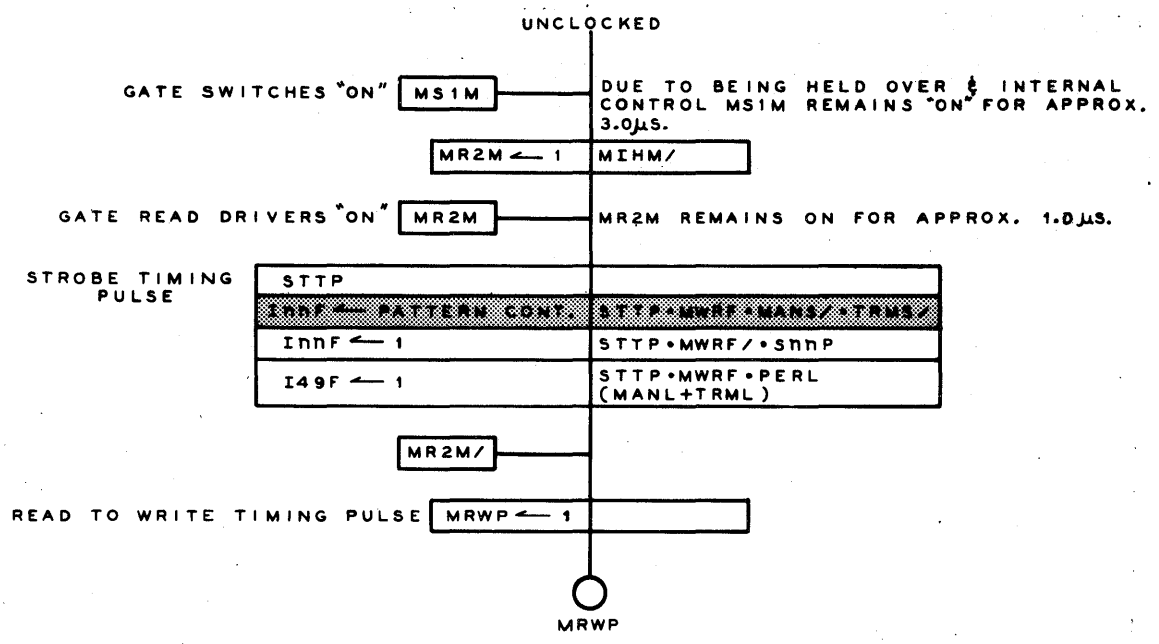


FIGURE 2.1-8
MS1M to MRWP

InnF ← 1

If this is a Memory Read operation (MWRF/), set the Read information into the Information Register at Strobe time (STTP). The information to be placed in the Register is from the Sense Amps (SnnP).

I49F ← 1

If a Parity Error exists in the MIR Register (PERL), set bit 49 of the Information Register at Strobe Time for a Memory Write operation (STTP • MWRF). By this action, the correct Parity is set into the Information Register during a Memory Write operation.

MR2M/

Approximately 300 nanoseconds after the time out of MR2M, the MRWP delay will be set. This is for a 300 nanosecond delay between the Read and Write portions of a Memory operation. The remainder of this description will reference Figure 2.1-9.

MRWP

When MRWP is set, the Inhibit Multi (MIHM) is set to gate on the Inhibit Drivers. Which Inhibit Drivers will drive current through the Stack depends upon the Information in the MIR Register.

MIHM

The Inhibit Multi will be on for approximately 1.55 microseconds. During the time it is set, it will hold-over MS1M to prevent MS1M from timing out. The Inhibit multi will also set the Write Multi (MW2M ← 1) to drive the Write current in the Core Stack. MW2M will remain on for approximately 1.0 microsecond.

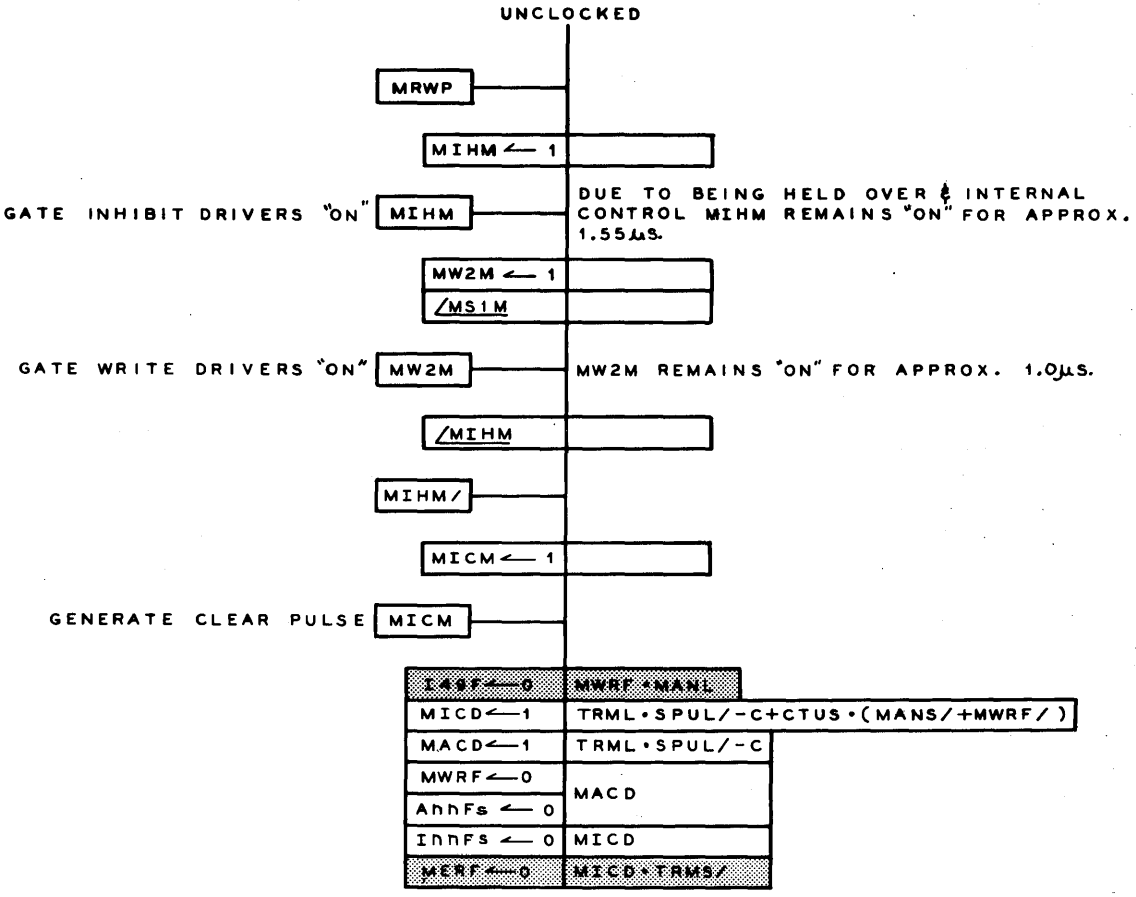


FIGURE 2.1-9
MWRP to MICM

MW2M

To prevent the Inhibit Multi from timing out, MW2M will hold-over the Inhibit Multi (MIHM/).

MIHM/

The Inhibit Multi will time out at the termination of the Write phase of the Memory operation. When it times out, the Memory Information Clear Multi (MICM) is set to generate a Clear Pulse in the Memory Module.

MICM

With MICM TRUE, the following actions will occur in REMOTE:

MICD ← 1

This driver will have a TRUE output if the Memory Module is in REMOTE and the System Clock switch is in the NORMAL position (TRML · SPUL/-C). If the System Clock Mode switch is in single or double pulse, then MACD and MICD will go TRUE with the Pulse Counter equal to three. See Figure 2.1-7.

MWRF ← 0, AnnFs ← 0

Clear the Address Register and the Memory Write Flip-Flop with the MACD level.

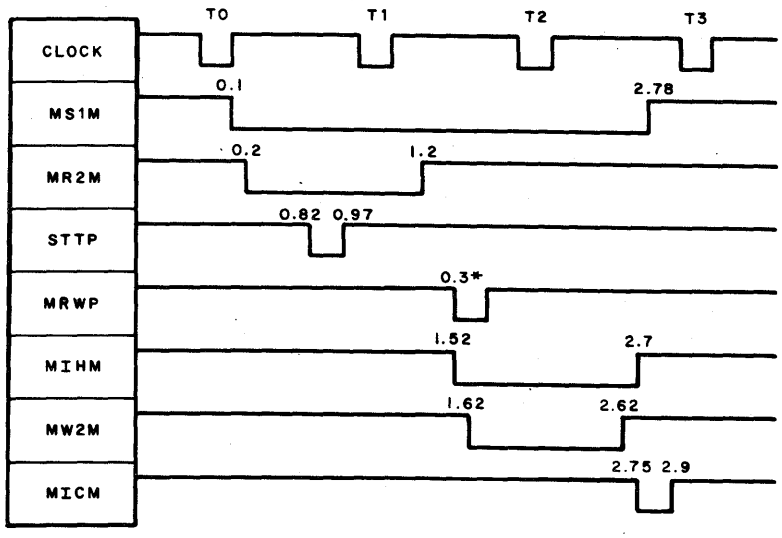
InnFs ← 0

Clear the Information Register with the MICD level.

Figure 2.1-10 is a Timing Diagram of the Multi Timing previously described with the times indicated for each of the Multis. All times indicated are taken from the Leading Edge of T_0.

NOTE

The Times used here are only approximations. The user of this manual is cautioned to use only the timings indicated in Section 5 for adjusting a Memory Module.



*0.3 MICROSECOND FROM TRAILING EDGE OF MR2M, TRAILING EDGE OF MRWP NOT CRITICAL.

FIGURE 2.1-10
MULTI TIMING

2.2 OFF-LINE OPERATION

The B461 Core Memory is designed to operate Off-Line as well as On-Line. The Off-Line Mode of operation is used primarily for testing of the Memory Module.

With the Off-Line Mode of operation, the Information recorded can be manually inserted in the Information Register, or generated within the Memory Module. All Information manually inserted is tested for the proper Parity and all Information generated is tested for specific combinations of bits as determined by the Pattern Control circuitry.

The Memory Maintenance switches are the prime control in the Off-Line Mode of operation. These switches determine the Information to be recorded and the type of operation to be done. For a detailed description of the Maintenance switches, refer to Section 3.27 of this Manual.

The various types of operations which can be done are as follows:

1. Single Cycle/Continuous - Continuous allows the Memory Module to initiate successive Memory cycles. Single cycle will allow only one Memory cycle to be executed.
2. Manual/Auto - In the Manual position, the Information to be recorded is manually inserted into the Information Register and tested for the correct Parity (ODD). In the Automatic position, the Information to be recorded is determined by and checked for the combination of bits specified by the Pattern Control circuitry.
3. Pattern Normal/Pattern Complement - In Pattern Normal (PCNL), the testing of the Module is accomplished with two Memory cycles at each Address. In Pattern Complement (PCCL), the testing is accomplished with four Memory cycles at each Address. The PCCL Mode of operation is also referred to as "Worst Case".
4. Uniform/Checkerboard - This Mode of operation will only determine the type of Information pattern to be developed. When in Checkerboard, this will force the Automatic Mode of operation. For a description of the Checkerboard patterns developed, refer to Section 6.8 of this Manual.

When operating the Memory Module in Off-Line, the Address Register instead of being Set and Reset, is counted up by one. A certain amount of control can be exercised over this counting. Via the Maintenance switches, one can count only the "X" portion of the Address Register, count only the "Y" portion of the Address Register, or inhibit all counting of the Address Register. This Register can also be manually counted by use of the STEP MAR switch.

Two other conditions that have not been previously mentioned that can be used in an Off-Line operation are as follows:

1. STOP ON ERROR - This will stop the operation if an Error condition exists and the IGNORE/STOP switch is in the STOP position.
2. STOP ON FINAL ADDRESS - This switch will stop the Memory opera-

tion when the Address Register is equal to 7777.

The STOP ON ERROR and STOP ON FINAL ADDRESS will stop a Continuous operation with the Pulse Counter equal to three. The Stop due to a Single cycle operation will stop with the Pulse Counter equal to zero.

Multi Timing

The Multi Timing for an Off-Line operation is the same as the timing in an On-Line operation. For this reason, only the portions of Memory Timing that are unique to an Off-Line operation will be discussed at this time.

Referencing Figure 2.2-1, only the occurrences at Strobe Time (STTP) vary for the Read portion of a Memory cycle. These differences are:

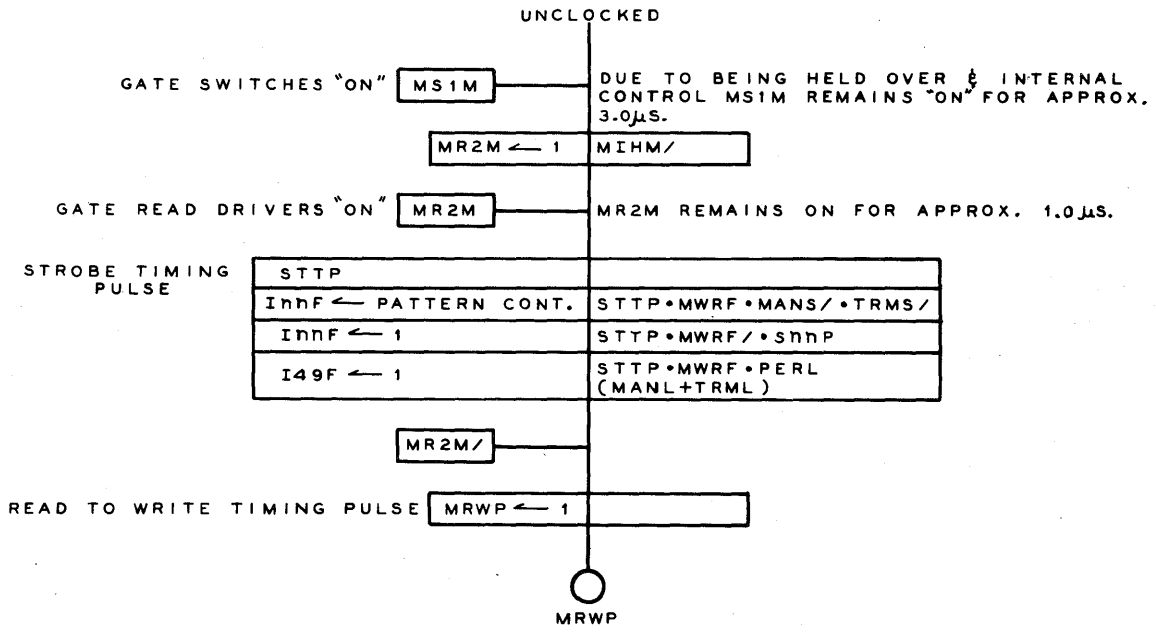


FIGURE 2.2-1
MULTI TIMING (MS1M to MRWP)

1. InnF←PATTERN CONTROL - The Information Register is set to the configuration specified by the Pattern Control circuitry if the following condition exists:

   STTP • MWRF • MANS/ • TRMS/

   This logic states that at Strobe Time (STTP) and the Memory cycle is a Write (MWRF); when in Local (TRMS/), set the Information to the Pattern Control if this is not a Manual operation (MANS/). This is a set of 49 bits of the Information Register.

2. I49F←1 - If the condition of STTP • MWRF • PERL • (MANL + TRML) exists, then set the correct Parity into the Information Register for a Memory Write operation. In an Off-Line operation, the term TRML is FALSE. This action is then enabled by the term MANL. If I49F is to be set, the PERL level will be TRUE to indicate an even number of bits exist in the Information Register.

Referencing Figure 2.2-2, the only differences in the Off-Line operation are at MICM time. The terminations of a Memory cycle are as follows:

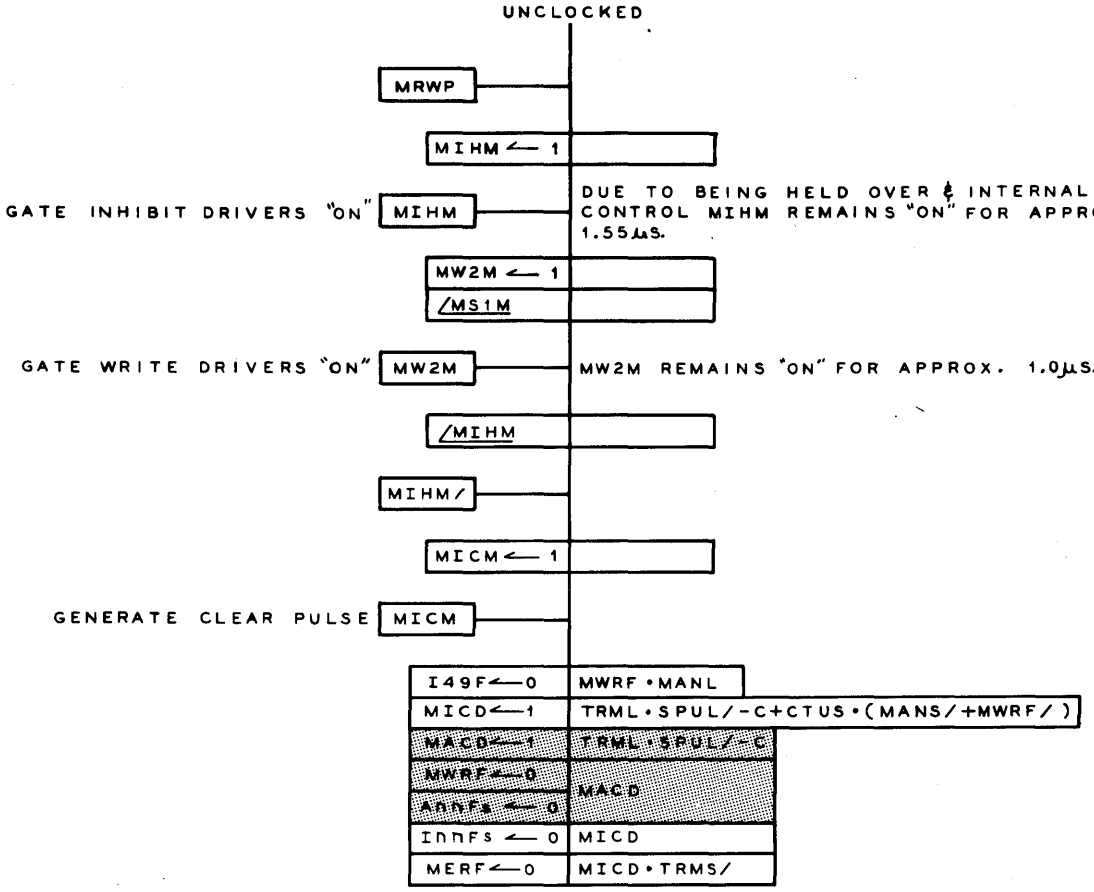


FIGURE 2.2-2
MULTI TIMING (MRWP TO MICM)

1. I49F ← 0 - Clear the 49th bit (Parity bit) of the Information Register if this is a Manual Write operation (MWRF • MANL). This action allows the correct Parity to be generated each time a Memory Write operation is executed in Manual.

2. MICD ← 1 - If the condition of CTUS • (MANS/ + MWRF/) exists, then allow MICD to be developed. The gating for MICD states that the operation is continuous (CTUS) and this is either an Auto operation (MANS/), or, a Memory Read operation is being completed (MWRF/). If the operation is a Manual Write, then MICD will not be developed and the Information Register will not be cleared. This allows the contents of the Information Register to be re-recorded, possibly at the next Address in succession.

3. MACD ← 1 - This level is Inhibited by the term TRML which is FALSE when in Local for the Off-Line operations. See shaded portion of Figure 2.2-2.

4. InnFs ← 0 - If MICD is TRUE, then clear the Information Register.

5. MERF←0 - Clear the Error Flip-Flop with MICD whenever the Memory Module is in LOCAL.

Clocked Control

When operating in LOCAL (Off-Line), certain actions require the one meg. Clock. These actions will vary depending upon the setting of the Maintenance switches.

Figure 2.2-3 is a Timing diagram of a Manual, Write, Single cycle operation. This operation will record the contents of the Information Register and stop at the end of the Memory cycle.

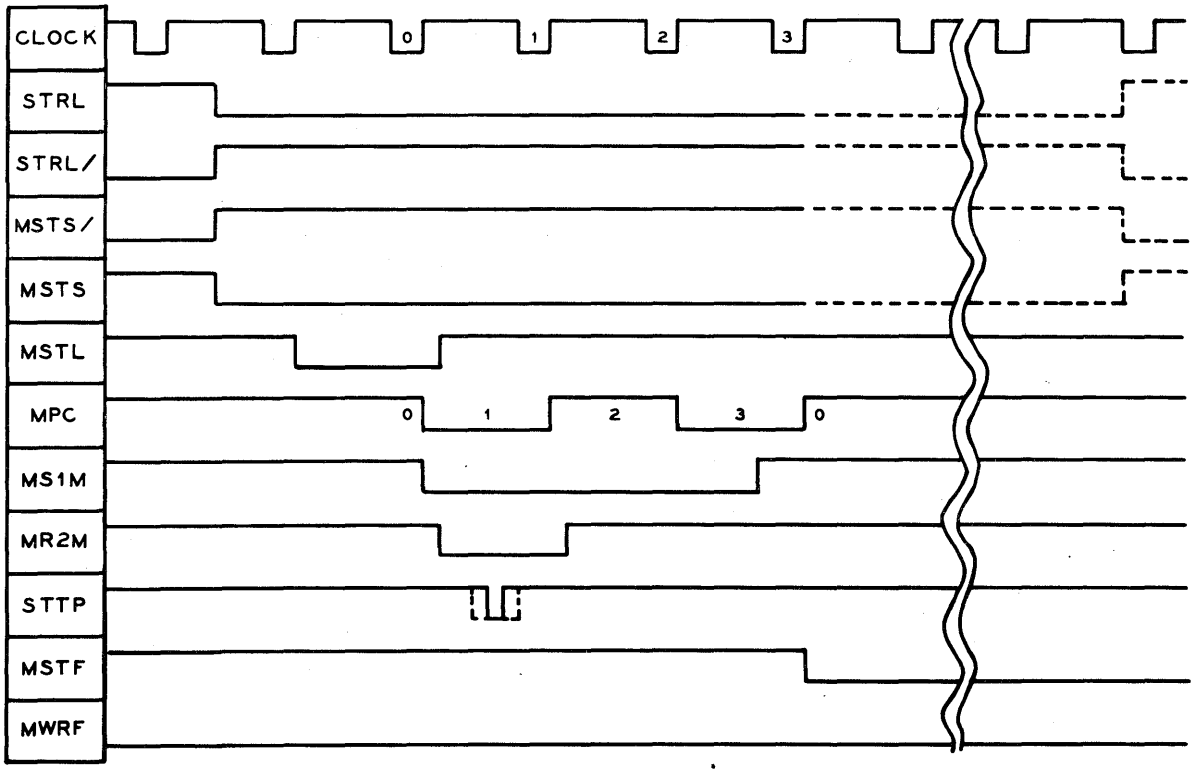


FIGURE 2.2-3
MANUAL - WRITE - SINGLE CYCLE TIMING

The terms STRL and STRL/ are derived from the START button on the Maintenance Panel, developing the MSTS and MSTS/ levels.

MSTL = MSTS • TRMS/

The term MSTS in turn develops MSTL (Memory Start Level) which initiates the Memory cycle by setting the MPC to 1 and triggering MS1M to initiate the Multi Timing. The MSTL level can only be developed when the Memory Module is in LOCAL due to the term TRMS/.

The only action to occur at Strobe Time (STTP) is the generation of the correct Parity in the Information Register. When the operation is terminated, the MPC is set to zero and the Memory Start Flip-Flop is

set (MSTF).

If a second Memory cycle is to be initiated, the START button must be depressed to again develop MSTL which will count the Address Register plus one with MSTF set.

A Manual Read Continuous operation is also initiated by MSTL. See Figure 2.2-4.

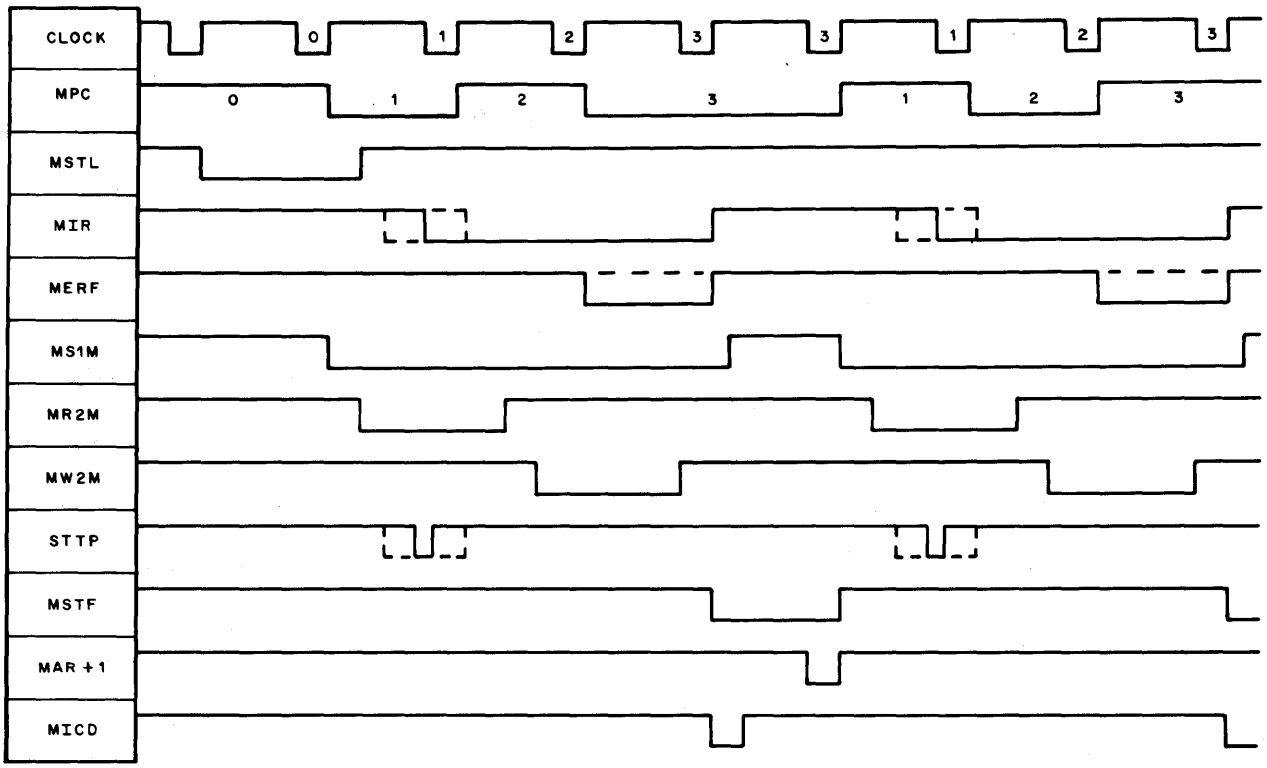


FIGURE 2.2-4
MANUAL READ CONTINUOUS TIMING

At Strobe Time (STTP), the Read information is placed into the Information Register and checked for correct Parity. If a Parity Error should exist, then the Error Flip-Flop (MERF) will be set with Clock Pulse 2. MICD is used to clear the Information Register and to reset MERF if it is set.

MPC = 3 for two Clock Pulses. The first Clock Pulse that occurs when the Memory Pulse Counter is equal to three will set MSTF. The second Clock Pulse will find MSTF = 1 and MPC = 3 resulting in MSTF being Reset and MPC set to 1. MS1M is triggered to start another Memory cycle, and the Address Register is incremented by 1 (MAR + 1).

The Memory Module can also be operated automatically by placing the MANUAL/AUTO switch in AUTO, or by placing the UNIFORM/CHECKERBOARD switch in CHECKERBOARD. When in Auto or Checkerboard, the operation is the same, the only difference is in the pattern generated. For the pattern developed by the UNIFORM/CHECKERBOARD switch, refer to Section 3.28 of this Manual. Only the MANUAL/AUTO switch will be considered

in this Section.

With the MANUAL/AUTO switch in the Auto position, the Memory operation will consist of two or four Memory cycles before counting the Address Register. The two or four cycle operation is determined by the Pattern Normal/Pattern Complement (PCNL-PCCL) switch on the Maintenance Panel. With the switch in the PCNL (Pattern Control Normal) position, the Auto operation is a two cycle operation, first a Read cycle followed by a Write cycle. See Figure 2.2-5.

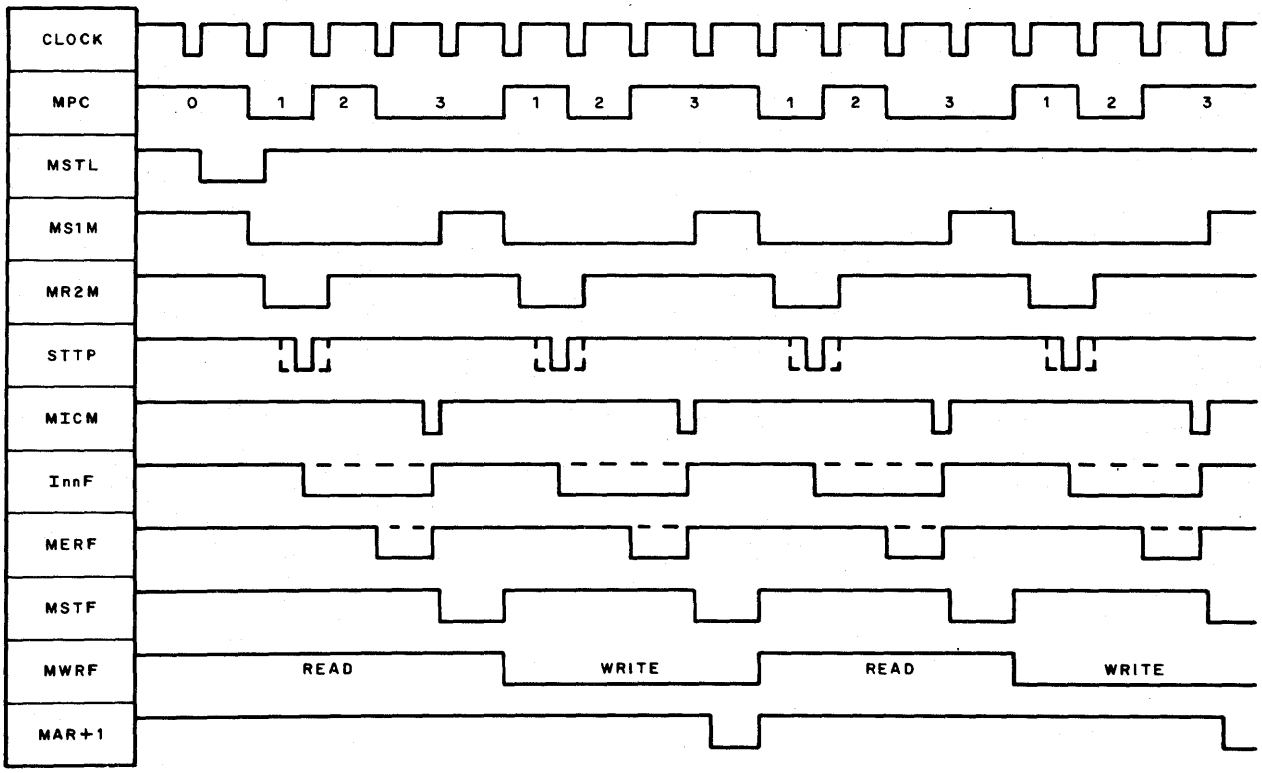


FIGURE 2.2-5
CONTINUOUS AUTO PCNL TIMING

During the Write cycle, the Information Register is set with the configuration indicated by the Pattern Control circuitry. During the Read cycle, the information is checked for the configuration indicated by the Pattern Control circuitry. The configuration of bits indicated may or may not contain a Parity Error, but the Parity Error is disregarded. The Address Register is counted only after the Write cycle (MAR + 1).

If the PCNL-PCCL switch is in the PCCL position, also referred to as "worst case" operation, the Auto operation is a four cycle access at each Address. See Figure 2.2-6.

The first Memory cycle is a Read. The information read must agree with the Pattern Control switch settings or MERF is set. At the end of this Read operation, the Memory Worst Case Flip-Flop (MWCF) is set.

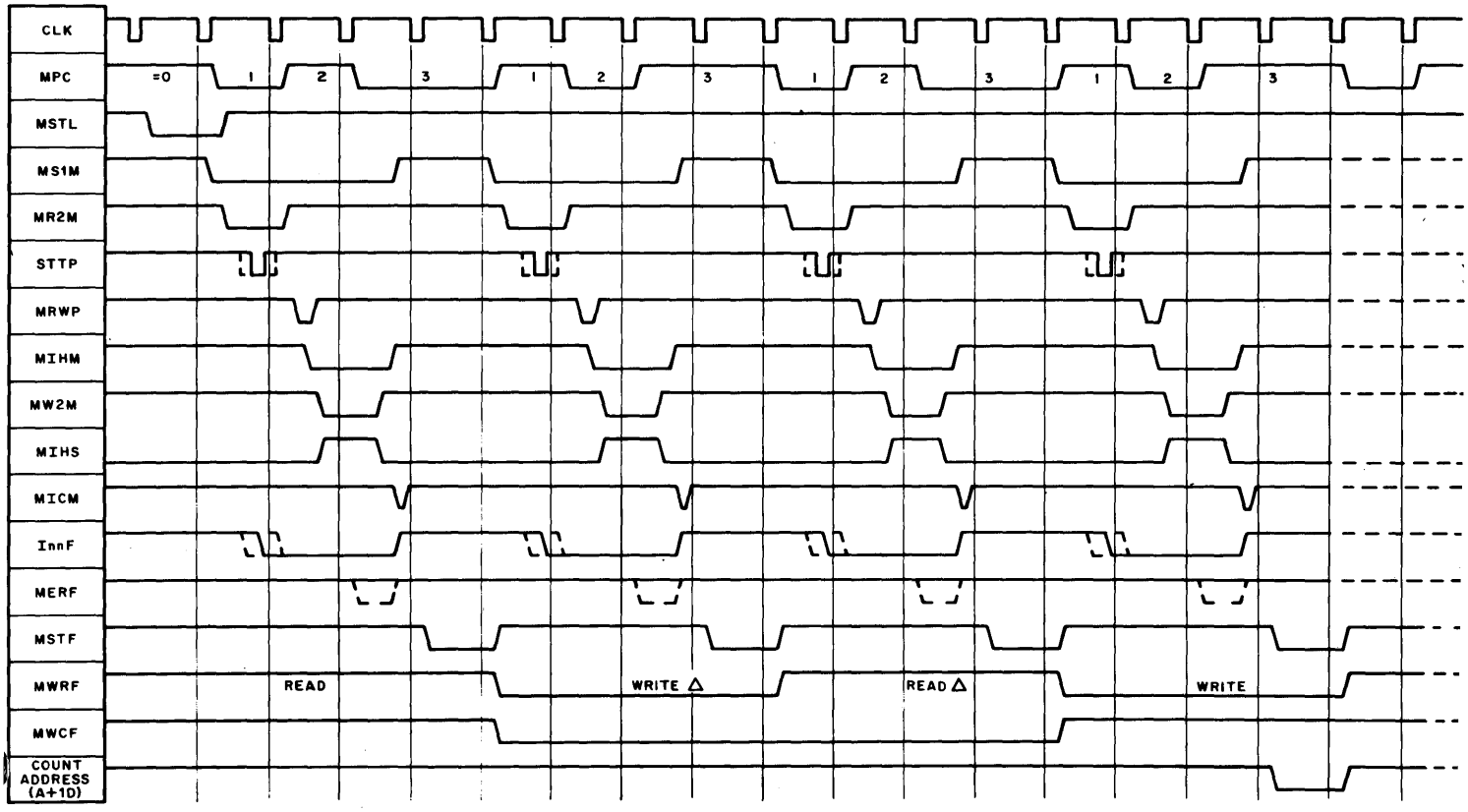


FIGURE 2.2-6
PCCL AUTOMATIC

The second Memory cycle is a Memory Write of the complement of the pattern indicated by the Pattern Control switches.

The third Memory cycle is a Memory Read to check for this complement pattern. If any bits are in the wrong state, then set the Error Flip-Flop (MERF). At the termination of the third Memory cycle, reset MWCF.

With MWCF OFF, the fourth Memory cycle will now Write the true pattern indicated by the Pattern Control switches. At the end of the fourth Memory cycle, the condition of MWCF is OFF, MWRF is ON, and MSTF exists. With this condition, the Address Register is counted up one (MAR + 1) and the four cycles are repeated for the next Address.

Clocked Flows

The following write up will be primarily concerned with the Off-Line functions indicated on the Clocked portion of the flow chart.

MPC = 0

For actions occurring at MPC = 0, refer to Figure 2.2-7.

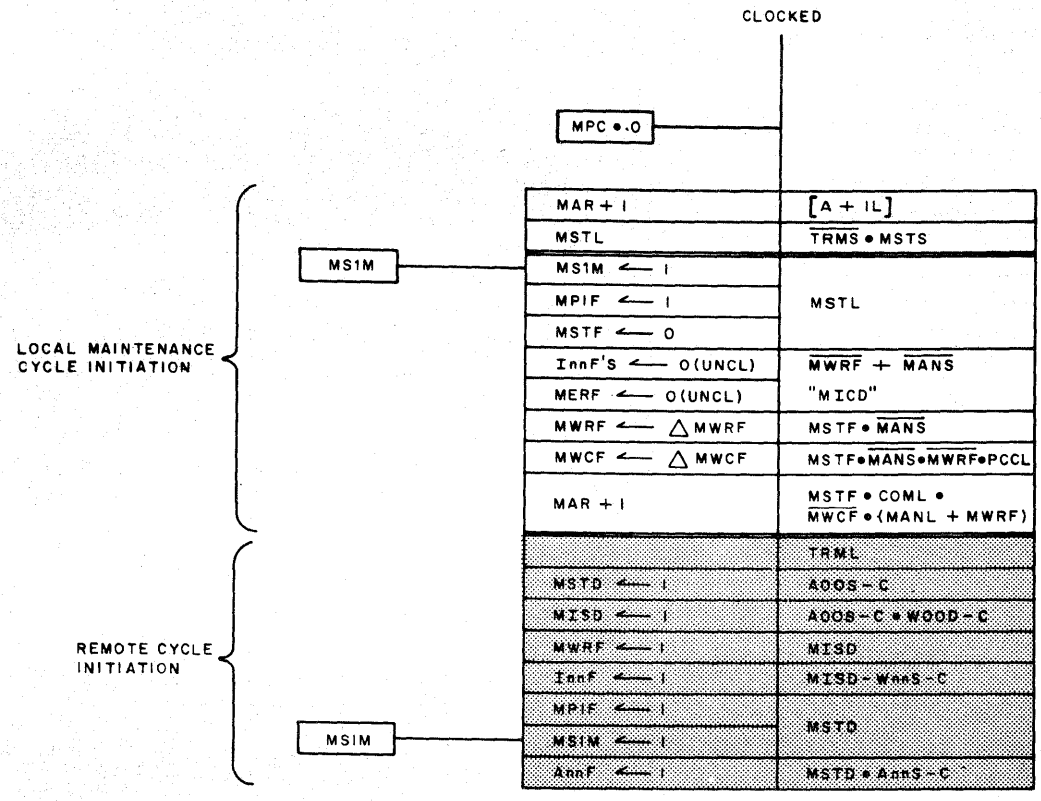


FIGURE 2.2-7
MPC = 0 FLOW

(A + 1L)

By depressing the STEP MAR switch on the Maintenance Panel, the Address Register is incremented by one (MAR + 1). This action does not require the Pulse Counter to be at a count of zero, but it does require that the Memory Module be in LOCAL. (A + 1L = A + 1S • TRMS/) A + 1S is the level developed from the STEP MAR switch.

TRMS/ • MSTS

With the Memory Module in LOCAL (TRMS/) and depressing the START switch (MSTS), the Memory Start Level (MSTL) is developed.

MSTL

When MSTL is TRUE with a Clock Pulse; initiate the Multi Timing (MS1M ← 1), set the Pulse Counter to one (MP1F ← 1), and reset the Memory Start Flip-Flop (MSTF ← 0). MSTF will be set if a previous Memory cycle had stopped due to a Single Cycle operation.

MSTL will also enable all of the actions listed below the double line shown in Figure 2.2-7.

MWRF/ + MANS/ "MICD"

If this is not a Write cycle (MWRF/), or if this is an Auto op-

eration instead of a Manual operation (MANS), then the MICD level is developed. MICD in turn will clear the Information Register (InnFs ← 0) and reset the Error Flip-Flop (MERF ← 0). Both of these actions are Unclocked but are shown here because they require the Pulse Counter equal to zero.

MSTF • MANS/

If the Memory Start Flip-Flop is ON and this is an Auto operation (MSTF • MANS/), then complement the Write Flip-Flop (MWRF ← Δ MWRF). This action will alternate the Read and Write operations when operating in Auto.

MSTF • MANS/ • MWRF/ • PCCL

If the Memory Start Flip-Flop is ON (MSTF) and this is not a MANual operation (MANS/) and the previous Memory cycle was a Memory Read with the Pattern Control switch in the "worst case" position (MWRF/ • PCCL), then complement the "worst case" flip-flop (MWCF ← ΔMWCF). With MWCF ON, the complement of the bit configuration indicated by the Pattern Control circuitry will be written and read in Memory.

MSTF • COML • MWCF/ • (MANL + MWRF)

With the Memory Start Flip-Flop set and the COUNT/INHIBIT switch in the COUNT position (COML) and the "worst case" flip-flop OFF (MWCF/), the Address Register will be incremented by one (MAR + 1) if this is a Manual operation or if the Write Flip-Flop is set (MANL + MWRF). This allows the Address Register to be counted after each Memory cycle when operating in Manual, or if in Auto, only at the end of the Write cycle. The combination of MWCF/ and MWRF will count up the Address Register only after the fourth Memory cycle when doing a PCCL operation. See Figure 2.2-6.

All of the actions shown in the shaded portion of Figure 2.2-7 cannot occur when in LOCAL due to the REMOTE level (TRML) being FALSE.

MPC = 1

The only action to occur at the Pulse count of one is the unconditional setting of the Pulse Counter to two (MP1F ← 0, MP2F ← 1). See Figure 2.2-8.

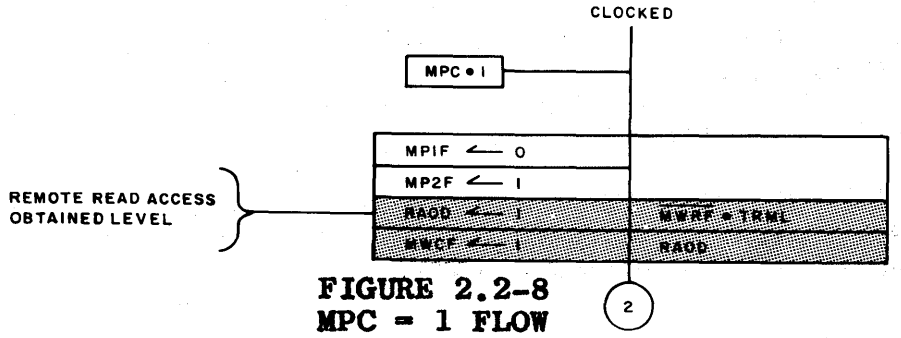


FIGURE 2.2-8
MPC = 1 FLOW

MPC = 2

For the actions which occur at MPC = 2, refer to Figure 2.2-9.

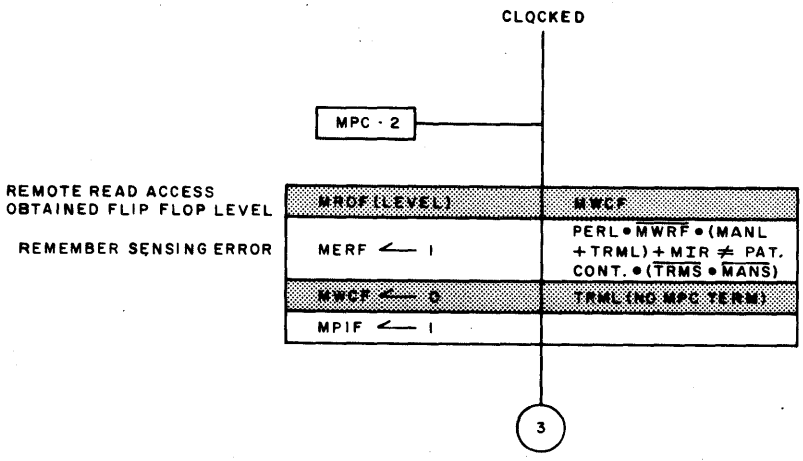


FIGURE 2.2-9
MPC = 2 FLOW

PERL · MWRF/ · (MANL + TRML) + (MIR ≠ PAT. CONT.) ·(TRMS/ · MANS/)

With either of the two conditions TRUE, then the Error Flip-Flop will be set (MERF ← 1). The first of the two OR terms; PERL · MWRF/ · (MANL + TRML) is used when a Parity Error is present during a Memory Read cycle (PERL · MWRF/) with the Memory being operated in Manual or Remote (MANL + TRML).

The second OR term (MIR ≠ PATTERN CONTROL) · (TRMS/ · MANS/) is used if the configuration of bits in the Information Register does not coincide with the configuration indicated by the Pattern Control circuitry and the Memory is being operated in Local and not in Manual (TRMS/ · MANS/).

Unconditionally set the Pulse Counter to three (MPlF ← 1).

MPC = 3

Before going into the actions listed under MPC = 3, the levels TSCL and CTUS should be understood. TSCL is the Test Single Cycle Level and it will be TRUE if the SINGLE/CONTINUOUS switch is in the SINGLE position. This will result in the Pulse Counter being set to zero and the Start Flip-Flop set to one. With these actions, the Memory Module will be at MPC = 0 and MSTF = 1 to enable the logic in Figure 2.2-7 when the START button is depressed.

The mnemonic CTUS is the Continue Level used in a LOCAL operation to allow one Memory cycle to immediately follow a previous Memory cycle. CTUS is made up of the following logic:

-O/-	CTUS	
-I-	+ TRML	REMOTE
	+ TSCL	TEST SINGLE CYCLE
	+ MWCF/ · MWRF · CAG 005 · SFAL	STOP-FINAL-ADDRESS & AUTO
	+ MANL · CAG 005 · SFAL	STOP-FINAL-ADDRESS & MANUAL
	+ MERF · SOEL	STOP-ERROR & ERROR EXISTS

If all of the above inputs are FALSE, then CTUS will be TRUE through a switch to enable the Continuous operation.

Examining the inputs from top to bottom:

1. The LOCAL/REMOTE switch must be in LOCAL to make TRML a FALSE level.

2. TSCL will be FALSE if the SINGLE/CONTINUOUS switch is in the CONTINUOUS position.

3. CAG 005 = AX1S · AX2S · AX3S · AX4S · AX5S · AX6S · AY1S · AY2S · AY3S · AY4S · AY5S · AY6S

   The third input is used in AUTO (or CHECKERBOARD) to STOP-FINAL-ADDRESS. With the condition of MWCF/ · MWRF, the AUTO operation will be at the end of either the two or four cycle operation for any particular Address. If this Address is 7777, then the output of CAG 005 will be TRUE. The inputs to CAG 005 are from the cross-coupled switches of the Address Register. With the STOP-FINAL-ADDRESS switch in the STOP FA position, then SFAL level will be TRUE to inhibit a CONTINUOUS operation when MAR = 7777.

4. The fourth input (+ MANL · CAG 005 · SFAL) is the STOP FA for a Manual operation.

5. The fifth input will be TRUE to inhibit a CONTINUOUS operation if there is an Error as indicated by MERF, and the STOP ERROR/IGNORE ERROR switch is in the STOP position as indicated by SOEL.

If all of the inputs to CTUS are FALSE, then the output of the CTUS switch will be TRUE to allow a CONTINUOUS operation. If any one of the inputs are TRUE, then CTUS will be FALSE and a CONTINUOUS operation will be stopped with the Pulse Counter equal to three.

For the actions which occur at MPC = 3, refer to Figure 2.2-10. The portions of this Figure which are shaded can occur only when in the REMOTE position and have been discussed in Section 2.1.

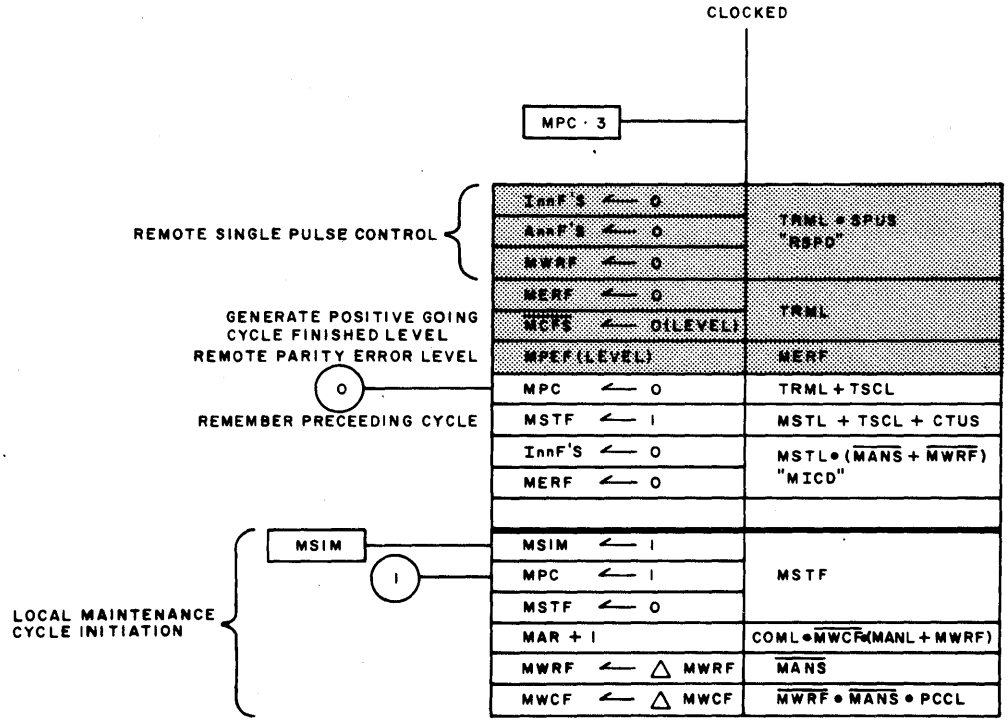


FIGURE 2.2-10
MPC = 3 FLOW

TRML + TSCL

If the Memory Module is in REMOTE (TRML) or if it is in SINGLE CYCLE (TSCL), then set the Pulse Counter to zero, MPC ← 0.

MSTL + TSCL + CTUS

If the Memory Start Level is TRUE from the Start switch (MSTL) or, if this is a SINGLE CYCLE operation (TSCL) or, if the CONTINUOUS level is TRUE (CTUS); then set the Start Flip-Flop to one (MSTF ← 1) to remember a previous operation.

MSTL • (MANS/ + MWRF/) "MICD"

The level MICD, Memory Information Clear Driver, will be TRUE with the MSTL level and either MANS/ (no Manual operation) or MWRF/ (a Memory Read operation). MICD in turn is used to clear the Information Register (InnFs ← 0), and to reset the Error Flip-Flop (MERF ← 0).

MSTF

With MSTF set at MPC = 3(this is the second Clock Pulse at MPC = 3); another Memory cycle will be initiated by setting MSIM ← 1 to initiate the Multi Timing. Also, the Pulse Counter is set to one (MPC ← 1), and the Memory Start Flip-Flop is reset (MSTF ← 0). The Pulse Counter is set to zero instead of one because the actions to initiate a Memory cycle are now done at MPC = 3 instead of at MPC = 0.

With MSTF set to one, all of the actions listed below the double

line shown in Figure 2.2-10 can occur.

COML • MWCF/ • (MANL + MWRF)

With the above conditions, the Address Register will be incremented by one (MAR + 1). The above term states that the COUNT/INHIBIT switch is in the COUNT position (COML) and the "worst case" flip-flop is OFF (MWCF/) and, this is either a Manual operation (MANL) or, the Write flip-flop is set (MWRF). When operating in AUTO, MANL is FALSE. The combination of MWCF/ and MWRF indicates the end of a two or four cycle Memory operation. See Figures 2.2-5 and 2.2-6.

MANS/

If this is not a Manual operation, then complement the Write flip-flop (MWRF $\leftarrow \Delta$ MWRF).

MWRF/ • MANS/ • PCCL

If the operation is the "worst case" (PCCL), and not a Manual operation (MANS/), then complement the "worst case" flip-flop (MWCF $\leftarrow \Delta$ MWCF) at the completion of each Memory Read cycle. The complementing of MWCF allows for the Writing and Reading of the true and complement form of the configuration of bits as indicated by the Pattern Control circuitry.

The previous discussion of the Flow Charts showed only the portions of the flows involved. Figures 2.2-11 and 2.2-12 display the entire flows for the Core Memory.

The columns at the left are the Clocked portion of the flow subdivided by MPC values. The columns at the right display the Unclocked portion of the flow and is subdivided by the individual Multis and the actions that they perform.

SEE PAGE 2.2-14 FOR FIGURES 2.2-11 & 2.2-12.

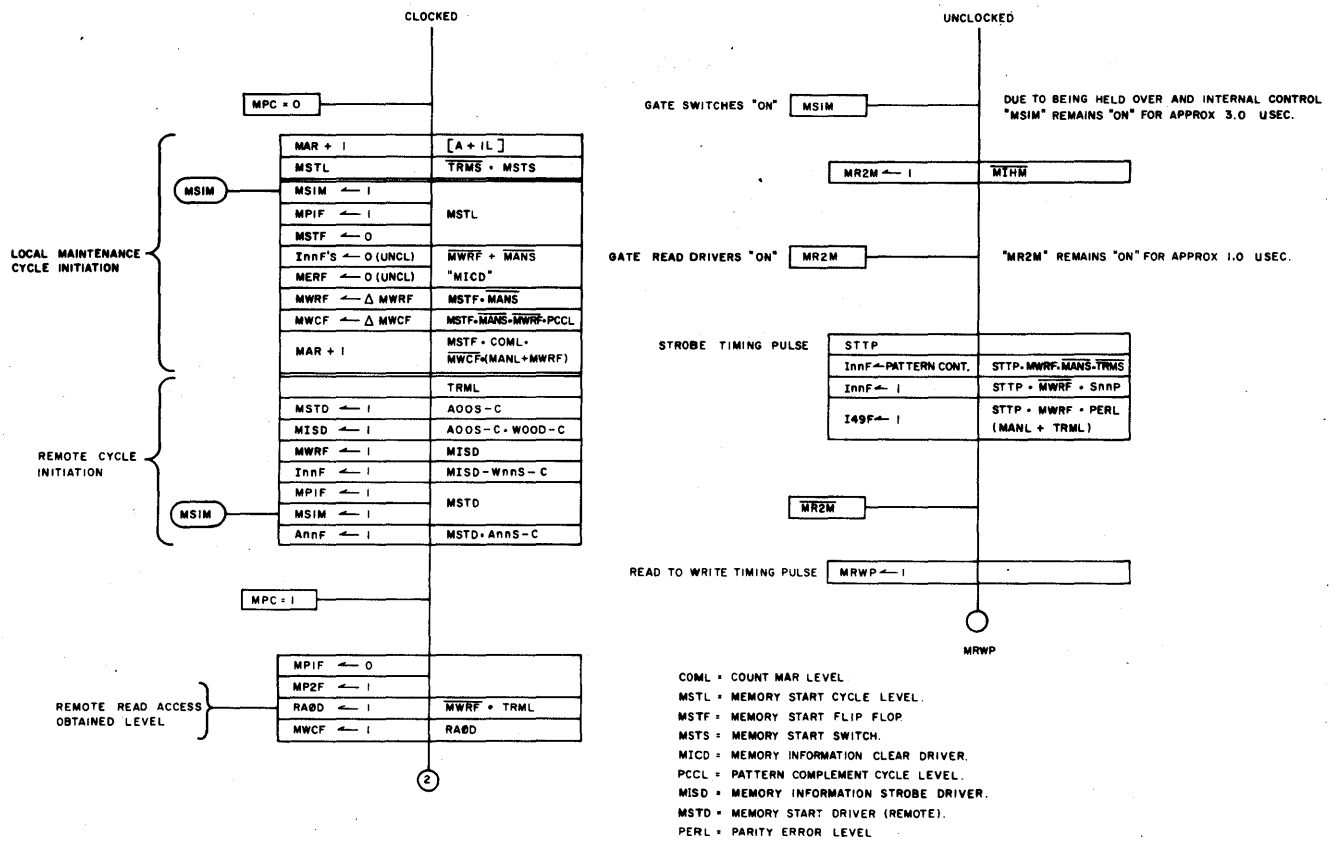
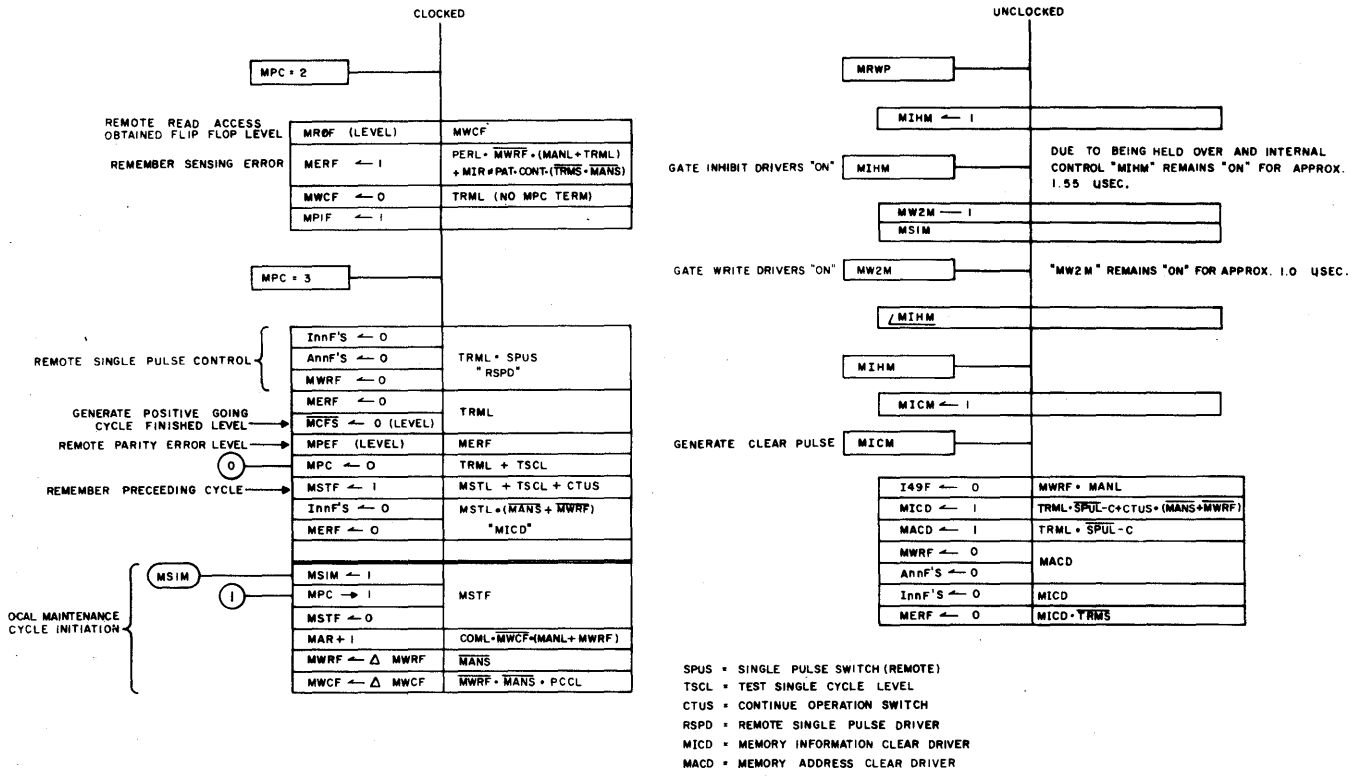


FIGURE 2.2-11
CORE MEMORY FLOW CHART (1 of 2)



SPUS = SINGLE PULSE SWITCH (REMOTE)
TSCL = TEST SINGLE CYCLE LEVEL
CTUS = CONTINUE OPERATION SWITCH
RSPD = REMOTE SINGLE PULSE DRIVER
MICD = MEMORY INFORMATION CLEAR DRIVER
MACD = MEMORY ADDRESS CLEAR DRIVER

FIGURE 2.2-12
CORE MEMORY FLOW CHART (2 of 2)

INDEX - SECTION 3

3 FUNCTIONAL DESCRIPTION - ELECTRONIC

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3.1 CORE STACK

Storage in the B461 Core Memory is based on the principle of magnetizing a toroid core in one direction to record the storage of a binary "one" and in the opposite direction to record a "zero".

The ferro-magnetic material used in the construction of the core has a nearly rectangular hysteresis loop. Since the entire operation of storage in a core is based on the hysteresis loop, an understanding of the magnetic characteristics of a ferro-magnetic material is essential.

Ferro-Magnetism

A current flowing through a conductor will cause a magnetic field to be built up around the conductor. The magnetic lines of force are concentric and lying in a plane which is perpendicular to the plane of the conductor. See Figure 3.1-1.

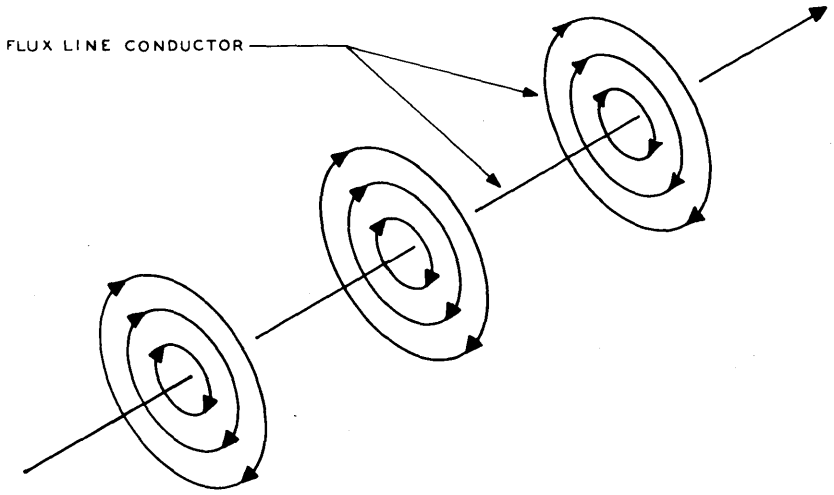


FIGURE 3.1-1
MAGNETIC FIELD

An easy method of determining the direction of the magnetic lines of force is to imagine grasping the conductor with the right hand so that the thumb points in the direction of the current flow. The fingers will then encircle the conductor in the direction of the flux lines.

When a ferro-magnetic material is introduced into the magnetic field, the field becomes distorted in the manner shown in Figure 3.1-2B. This is because the material offers a low resistance path in comparison to the space that surrounds the inductor. The magnetic field will pass through the ferro-magnetic material following the contour of the material as illustrated in Figure 3.1-2C.

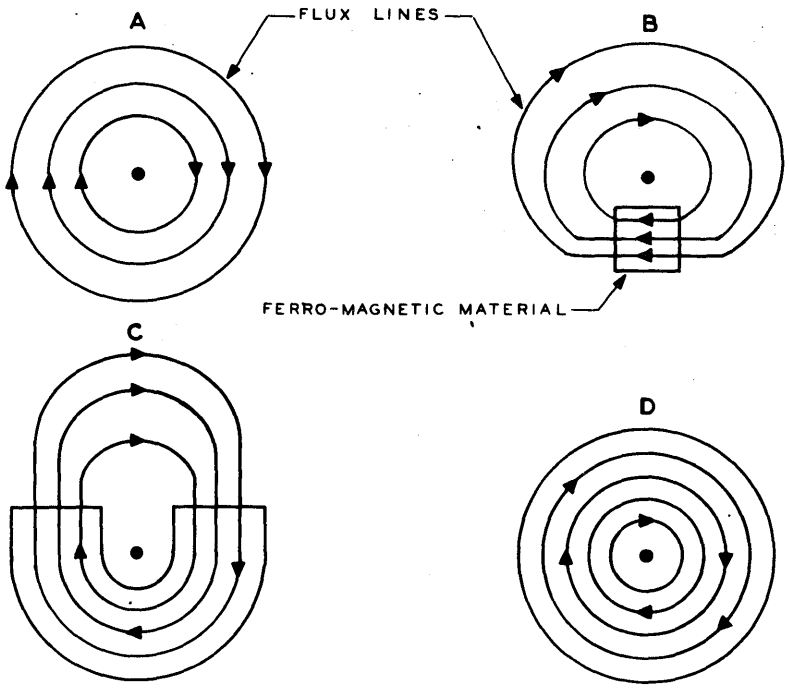


FIGURE 3.1-2
FIELD DISTORTION

When the ferro-magnetic material is fashioned into the form of a closed ring, the magnetic field set up by a magnetizing current is wholly confined to the interior of the ring. No lines of magnetic induction pass through the surface of this material to the space outside the ring. See Figure 3.1-2D. The magnetic intensity (H) in the material of the ring is equal to the product of this magnetization current and the number of turns in the magnetizing winding, divided by the mean circumference of the ring.

$H = Ni/c$

H = Magnetic Intensity
N = Number of Turns
i = Current in the Winding
c = Mean Circumference of Ring

Note that the magnetic intensity does not depend on the type of material of which the ring is formed.

The magnetic flux density (B) within the ring is the product of the magnetic intensity (H) and the permeability (μ) of the ring material.

$B = H\mu$

B = Magnetic Flux Density
H = Magnetic Intensity
μ = Permeability of the Material

The flux density (B) is not a linear function of the magnetic intensity. This is because the permeability of a material is not a constant value. Permeability depends on the type of material, the temperature

of the material, and on how much the material has been previously magnetized.

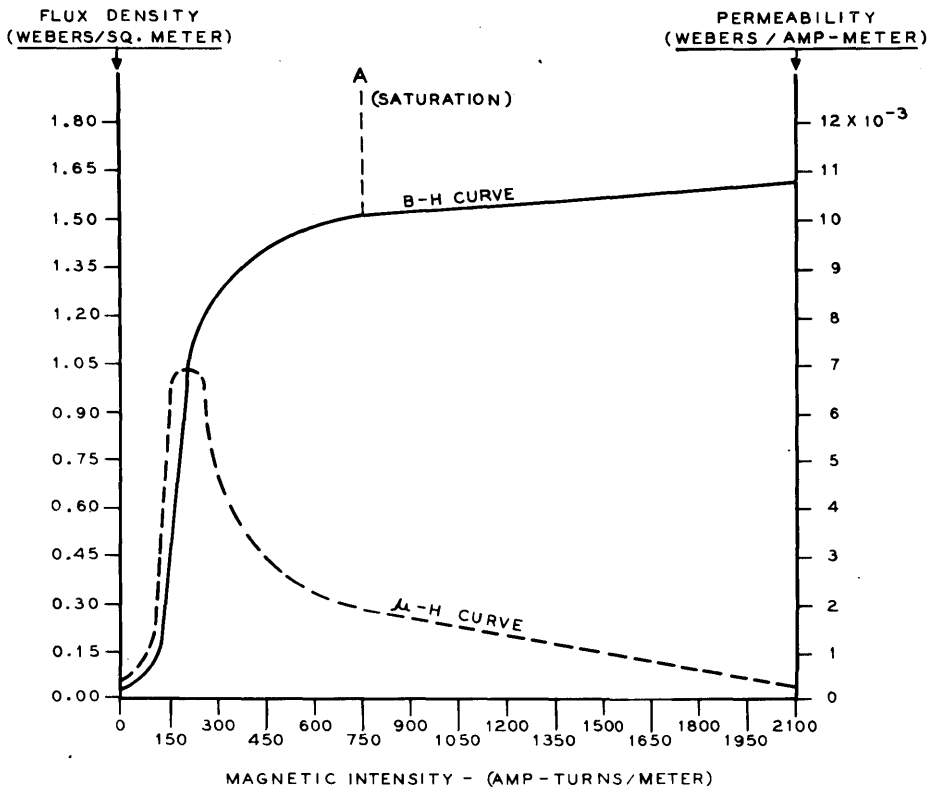


FIGURE 3.1-3
TYPICAL MAGNETIZATION CURVE

Figure 3.1-3 shows the relationship between B, H, and μ for a typical ferro-magnetic material. Notice that beyond point A, even though H is increasing, B remains almost constant. This is the magnetic saturation of the material and is due to the permeability (μ) decreasing at the rate that H is increasing.

Hysteresis

Figure 3.1-3 shows the relationship between the B and H only if the material is initially unmagnetized and H is always increasing.

The magnetization curve shown in Figure 3.1-4 expresses the relationship of B and H for the following conditions.

1. The magnetization current is increased from zero until the magnetic intensity (H) is equal to value A. The flux density (B) for this value of H is given to point B.
2. The magnetization current is increased from 0 until the value of H is D, and then decreased until the value of H is A. Now the flux density for the H value of A is given to point E.
3. The magnetization current is decreased to 0. The value of H falls from point A to 0. The flux density has a value of C

when H has returned to 0.

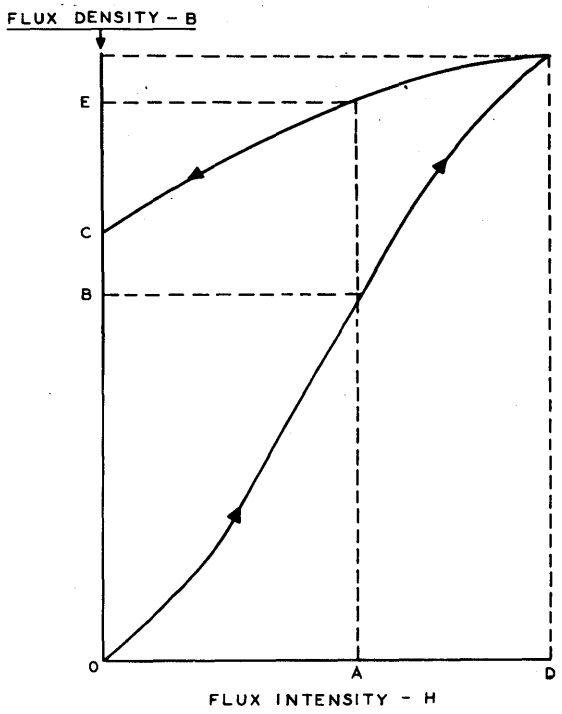


FIGURE 3.1-4
B-H CURVE

The flux density in the material is shown to depend not only on H, but also on the degree that the material has been previously magnetized. This behavior of the material, which causes the curve for a decreasing value of H to depart from the curve for an increasing value of H, is called Hysteresis.

When H is increased from 0 to some maximum value in the opposite direction, then decreased to 0; increased to the same maximum value in the opposite direction, then decreased to 0; the flux density reverses in the manner shown in Figure 3.1-5. This closed magnetization curve is called a hysteresis loop. Points C and F indicate the flux density that remains in the material after H is decreased to 0. These points are usually labeled +Br and -Br and are called the magnetic retentivity of the material. Points A and D show the amount of H required to reduce B to 0 after the material has been magnetized in the opposite direction. This is called the Coercive Force.

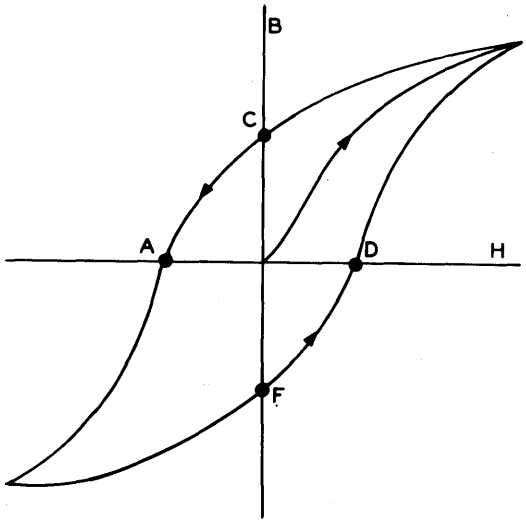


FIGURE 3.1-5
HYSTERESIS LOOP

Square Hysteresis Loop

Ferrite cores are made of special materials that will produce a hysteresis loop which is almost square. This square-loop characteristic allows the ferrite to act as a bi-stable storage element. If the ferrite core whose hysteresis loop is shown in Figure 3.1-6 is magnetized in the negative direction (-Br), and we pulse the winding with a current value of +I/2, the flux density in the core will be changed from -Br to -BrI/2. As illustrated, the change in residual flux is very small, and the core is still highly magnetized in the negative direction. However, if we pulse the winding with a current value of +I, the core will rapidly switch from -Br to +Br and will now be highly magnetized in the positive direction.

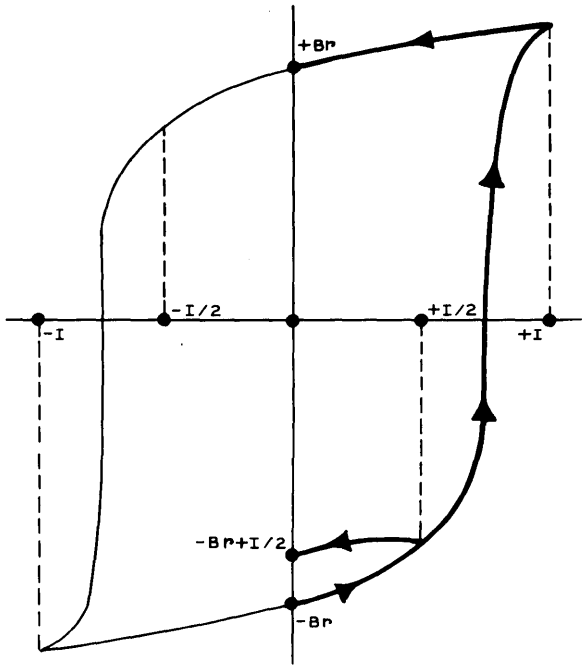


FIGURE 3.1-6
SQUARE LOOP

The square loop discriminates against small values of current in the windings. There is no appreciable change in flux density unless the winding current reaches a value which will cause an H value beyond the knee of the curve. The H current value of + or - I/2 is referred to as a half-select current; and an H current value of + or - I is referred to as a full select current.

Temperature Effect

The permeability of a ferro-magnetic material decreases as the temperature increases. The flux density (B) is the product of the flux intensity (H) and the permeability (μ); therefore, if the permeability decreases, then the shape of the material's hysteresis loop will be changed. This temperature problem demands that the core storage system be operated within a specified range of temperatures.

A core's hysteresis loop tends to become less square as the temperature of the material increases. This means that a winding current of I/2 will cause a larger change in the flux density of the core. To insure that the change in flux density will remain the same within the range of operating temperatures, the core winding drive current is decreased as the temperature is increased.

Core Windings

Each of the cores in the Memory are threaded by four wires, each wire serving as a one-turn winding. See Figure 3.1-7. In order to understand the function of the windings, assume that the core is magnetized in the negative direction and that the X and Y windings have a current

flow that tends to establish a flux density in the positive direction.

To write a binary "one" into the core, that is to switch the state of the core from -Br to +Br, both the X and Y currents must occur at the same time and have a combined value which will cause a sufficient magnetizing force to switch the polarity of the core's flux density.

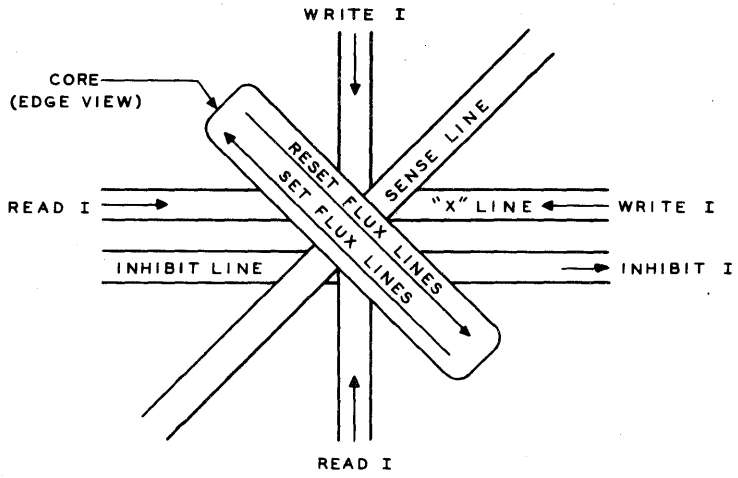


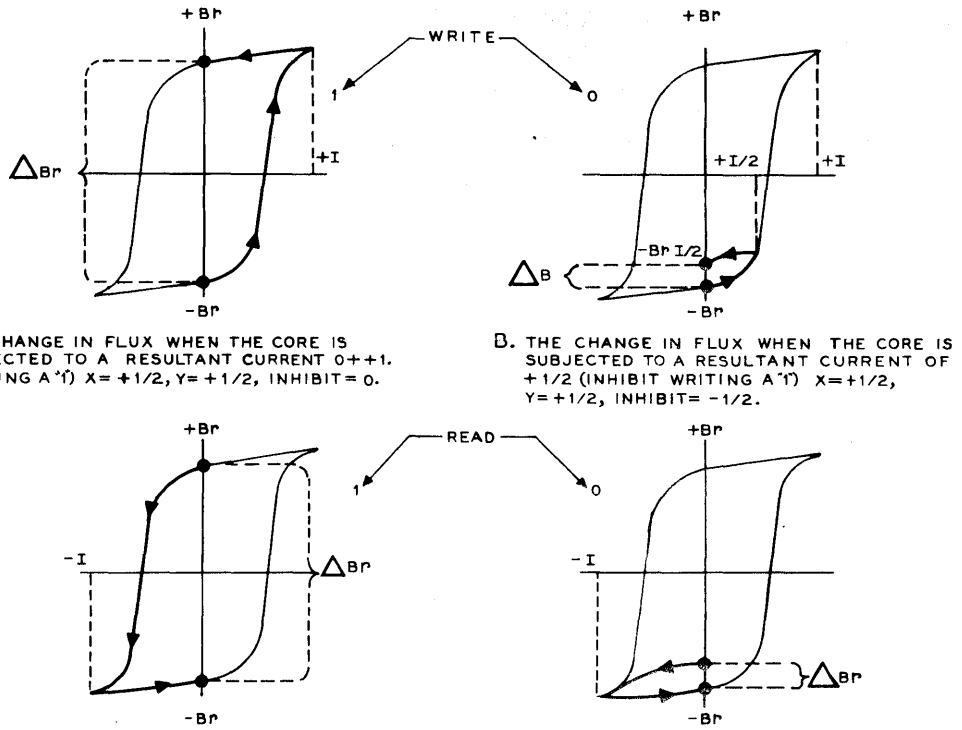
FIGURE 3.1-7
CORE WINDING

If the current flowing through each individual winding is equal to I/2, then the combined value is I. This means that the core will switch states when both currents are present; but, if only one of the currents is present, there is very little effect on the flux density of the core (See Figure 3.1-8A and B), and the core is half-selected.

As shown in Figure 3.1-7, the Inhibit winding current flow when present, will oppose that of the Write currents in the X and Y lines. When all three currents are present, the resulting effect on the core is +I/2 since the -I/2 due to the Inhibit winding current will cancel one of the Write +I/2 currents. See Figure 3.1-8B. The Inhibit-winding Driver is gated by the Information Register and is used to prevent the writing of a binary "one" into the core.

During the Read phase of a Memory cycle, the direction of current flow in the X and Y lines is reversed. If the core is in the "ones" state, coincident currents in the X and Y windings will cause the core to switch its magnetic state. This is shown in Figure 3.1-8C. This rapid change in the flux density of the core will cause a current to be induced into the Sense winding. This is a Read out of a binary "one".

If the core has been originally in the "0" state, the coincident Read currents would merely drive the core further into saturation. As shown in Figure 3.1-8D, there will be very little change in the flux density and little current induced into the Sense winding.



A. THE CHANGE IN FLUX WHEN THE CORE IS SUBJECTED TO A RESULTANT CURRENT 0++1. (WRITING A "1") X= +1/2, Y= +1/2, INHIBIT= 0.

B. THE CHANGE IN FLUX WHEN THE CORE IS SUBJECTED TO A RESULTANT CURRENT OF +1/2 (INHIBIT WRITING A "1") X=+1/2, Y= +1/2, INHIBIT= -1/2.

C. THE CHANGE IN FLUX WHEN A CORE WHICH IS STORING A "1" IS SUBJECTED TO TWO HALF-SELECT READ CURRENTS.

D. THE CHANGE IN FLUX WHEN A CORE WHICH IS STORING A "0" IS SUBJECTED TO TWO HALF-SELECT READ CURRENTS.

FIGURE 3.1-8
READ/WRITE FLUX CHANGES

A core is storing a "one" when it is magnetized in some predetermined direction. Whether it is magnetized in a positive or negative direc-

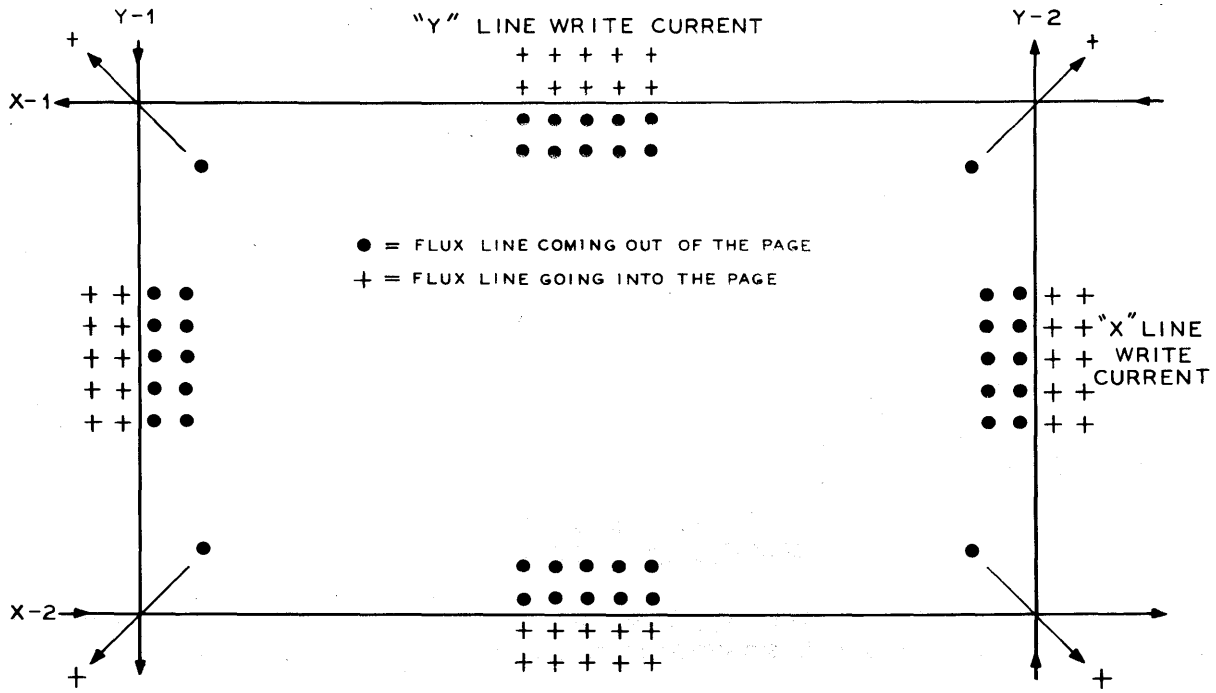


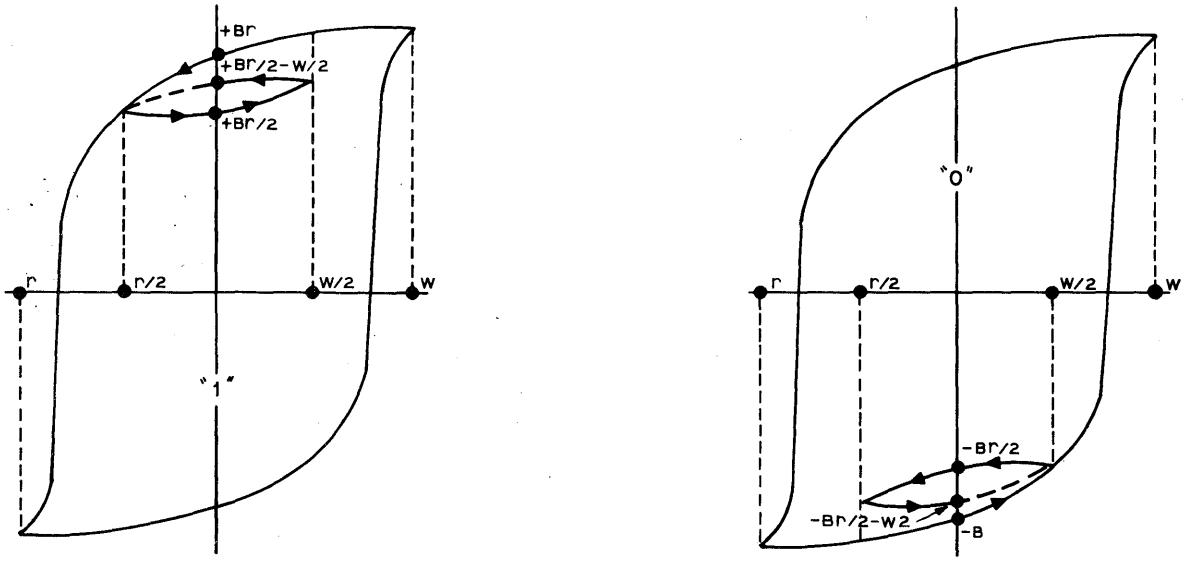
FIGURE 3.1-9
ALTERNATE LINE WRITE CURRENTS

tion will depend on the direction of the Write currents flowing in the X and Y lines. Notice in Figure 3.1-9 that due to the alternate X and Y line Write currents, two of the cores are magnetized in the positive direction and two are magnetized in the negative direction. It does not make any difference in what direction a core is magnetized, since during the Read out of the information, the X and Y line current is reversed.

Noise

Figure 3.1-10 shows a typical hysteresis loop. Because of the curved portions of the loop, a half-select current will disturb the magnetic state of the core. A core is subjected to half-select currents each time another core on the same X or Y line is selected for a Read or Write operation.

When a core that is storing a "one" is subjected to a half-select Read current, the state of the core is changed from +B to +Br/2. Similarly, a core that is storing a "zer0" will be changed from -B to -Br/2. When the information is written back into the selected core, the half-selected cores are subjected to a half-select Write current. This half-select Write current goes from +Br/2 to +Br/2-w/2 and from -Br/2 to -Br/2-w/2 respectively.



A. THE CHANGES IN FLUX OF A CORE STORING A "1" WHEN IT IS SUBJECTED TO A HALF-SELECT READ (r/2) FOLLOWED BY A HALF-SELECT WRITE (W/2).

B. THE CHANGES IN FLUX DENSITY OF A CORE STORING A "0" WHEN IT IS SUBJECTED TO A (r/2) FOLLOWED BY A HALF-SELECT WRITE (W/2).

FIGURE 3.1-10
HALF-SELECT FLUX CHANGES

When half-select currents are applied alternately in the Read and Write directions, the core will transverse a minor hysteresis loop as shown in Figure 3.1-10.

Previously, only the selected core's contribution to the Sense line

current has been considered. However, the same Sense line passes through every core in a plane. Unavoidably, each of the cores threaded by the selected X and Y lines receives a half-select Read current which also contributes to the Sense line current. In a 64 x 64 matrix, 63 cores along the X line and 63 cores along the Y line would receive a half-select current. This accumulation of induced currents from the half-selected cores can amount to an induced current which is much greater than that due to the selected core, thereby causing a Read error if the accumulated half-select induced currents are out of phase with the induced current from the co-selected core.

To minimize this undesirable current flow, the Sense winding is arranged through the cores in a checkerboard pattern so that half of the cores will produce a negative-going pulse in the Sense line, and the other half will produce a positive pulse in the line. See Figure 3.1-11.

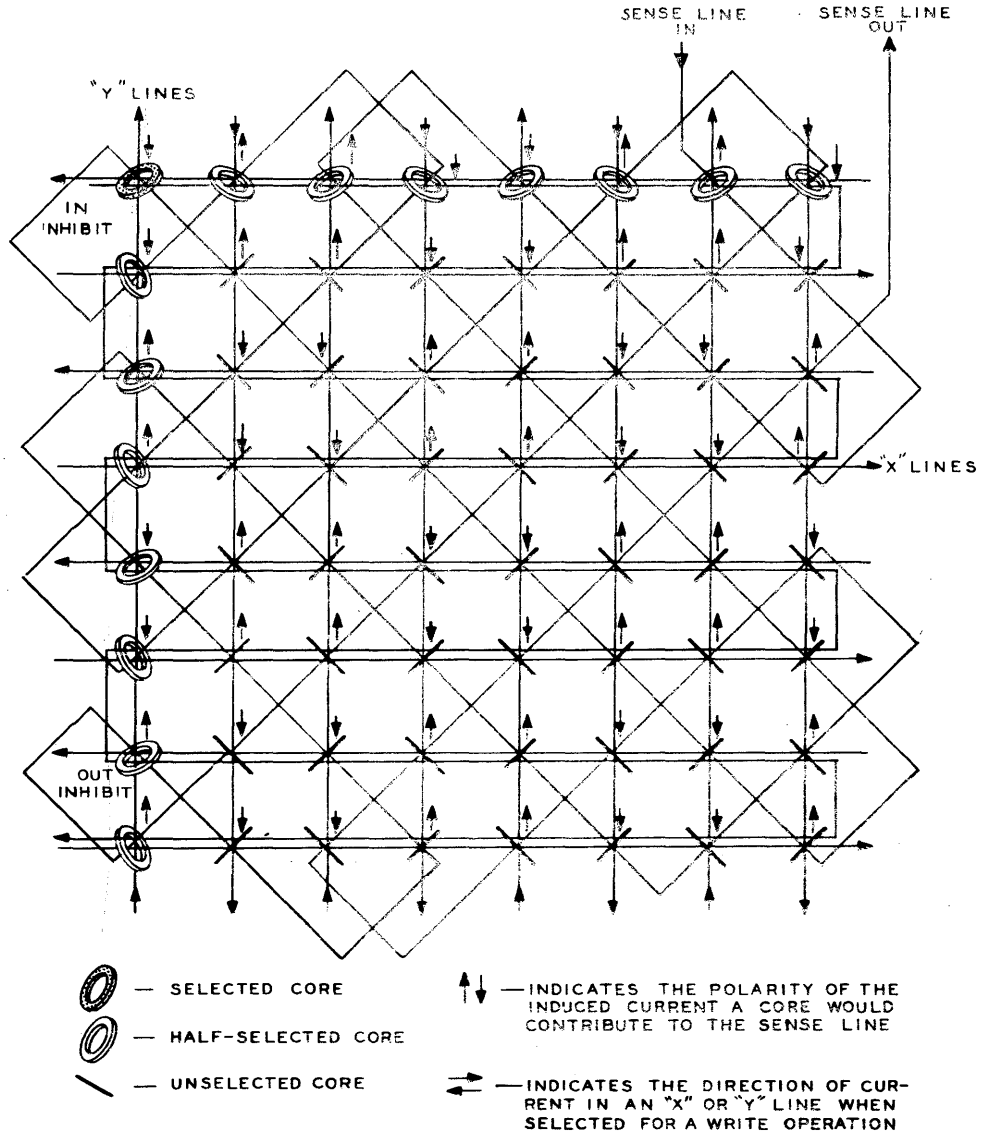


FIGURE 3.1-11
8 x 8 CORE PLANE

When all cores contain the same information (1 or 0), the positive induced current which is contributed by one half of the half-selected cores, will be cancelled by the negative induced current from the other half of the half-select cores.

In actual practice, there is not a complete cancellation of the half-select signals. This is because it is not possible to manufacture cores that all exhibit exactly the same magnetic characteristics. This is also due to the physical layout of the Sense line. There will be two half-select cores left unopposed.

There are 63 half-select cores on each selected line. Of these cores, 32 are contributing a pulse of one polarity and 31 are contributing a pulse of the opposite polarity. This leaves one core on each line that is unopposed. Both of these cores are contributing a pulse that is out of phase with the pulse from the selected core. The resultant signal in the Sense line is the contribution of the selected core, minus the two unopposed half-select cores contribution, plus or minus the difference noise from the remaining half-selected cores.

$R = S - 2hs \pm dn$

R = Resultant Signal

S = Signal due to the selected core

hs = Signal due to the two unopposed half-selected cores

dn = The difference noise signal due to 31 half-selected cores not completely cancelling the other 31 half-selected cores

The worst pattern of storage information would be to have all the cores producing positive-going currents in one state and the other half in the opposite state. In this case, the term dn takes on a maximum value. The reason for this is that at the time that they are both subjected to a half-select Read current, the change in flux density of a core storing a "one" is not equal to the change in flux density of a core storing a "zero".

The cores storing zeros have been subjected to one more half-select current than the cores storing ones. This additional half-select current was applied at the time that the cores storing "ones" were fully selected. Because of this additional half-select current, the residual flux density of a core storing a "one" is not equal to the residual flux density of a core storing a "zero".

One of the factors that determines the permeability of a material is the degree that it has been previously magnetized. Since a core storing a "one" is not magnetized to the same degree as a core storing a "zero", the changes in flux density as the result of the half-select Read will not be the same.

Stack Construction

All the cores for the Memory are mounted into a unit referred to as the Core Stack. The Core Stack is sub-divided into planes. Each plane corresponds to one bit of information in each of the words. As there are 48 Information bits and one Parity bit in a word, the stack consists of 49 planes, plus one blank plane for a total of 50 planes. Each plane has its own Sense and Inhibit windings to make a total of 49 Sense and 49 Inhibit windings, one for each bit in a word.

Every time a Memory cycle is initiated, one core in each plane is selected to access all 49 bits of a word. This is accomplished by the X and Y lines. There are 4096 cores in each plane arranged in a 64 x 64 Matrix, or, each plane is accessed by 64 X lines and 64 Y lines. Any one X line will intersect any one Y line only once in each plane; (refer to Figure 3.1-12), but the X and Y lines are wired to all planes in the Stack. By driving current into one X line and one Y line, both currents being in coincidence, one core will be selected in each plane; a total of 49 cores for an entire word.

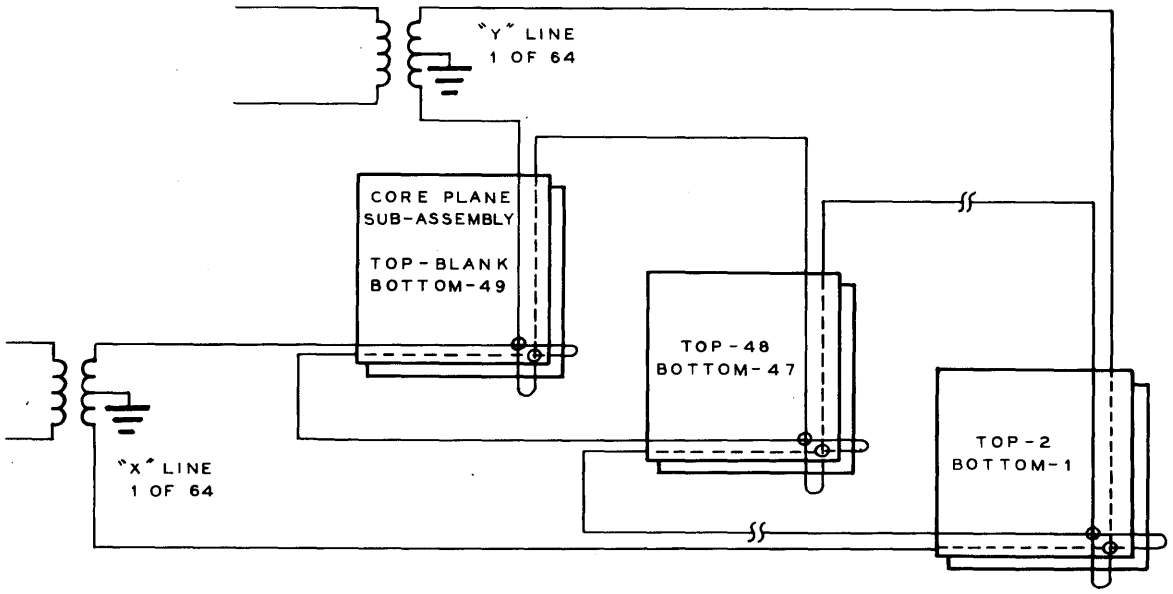


FIGURE 3.1-12
X - Y LINE INTERSECTION

Each X and Y line originates from one side of the secondary of a transformer, loops through the entire stack, and returns to the other side of the same transformer secondary. See Figure 3.1-12. There is one transformer for each of the X lines and each of the Y lines. By driving current through the transformer primary in one direction for a Read, and the other direction for a write, the current in the secondary will also change direction. This in turn will drive current in the X or Y line in one of two directions, depending upon Read or Write.

For a detailed description of the transformer operation, refer to Section 3.2 of this manual.

3.2 ADDRESSING

Addressing is the function of selecting a particular "X" line and "Y" line to access one of the 4096 words in the Core Stack. Figure 3.2-1 is a diagram of the Logical Units of the Core Memory.

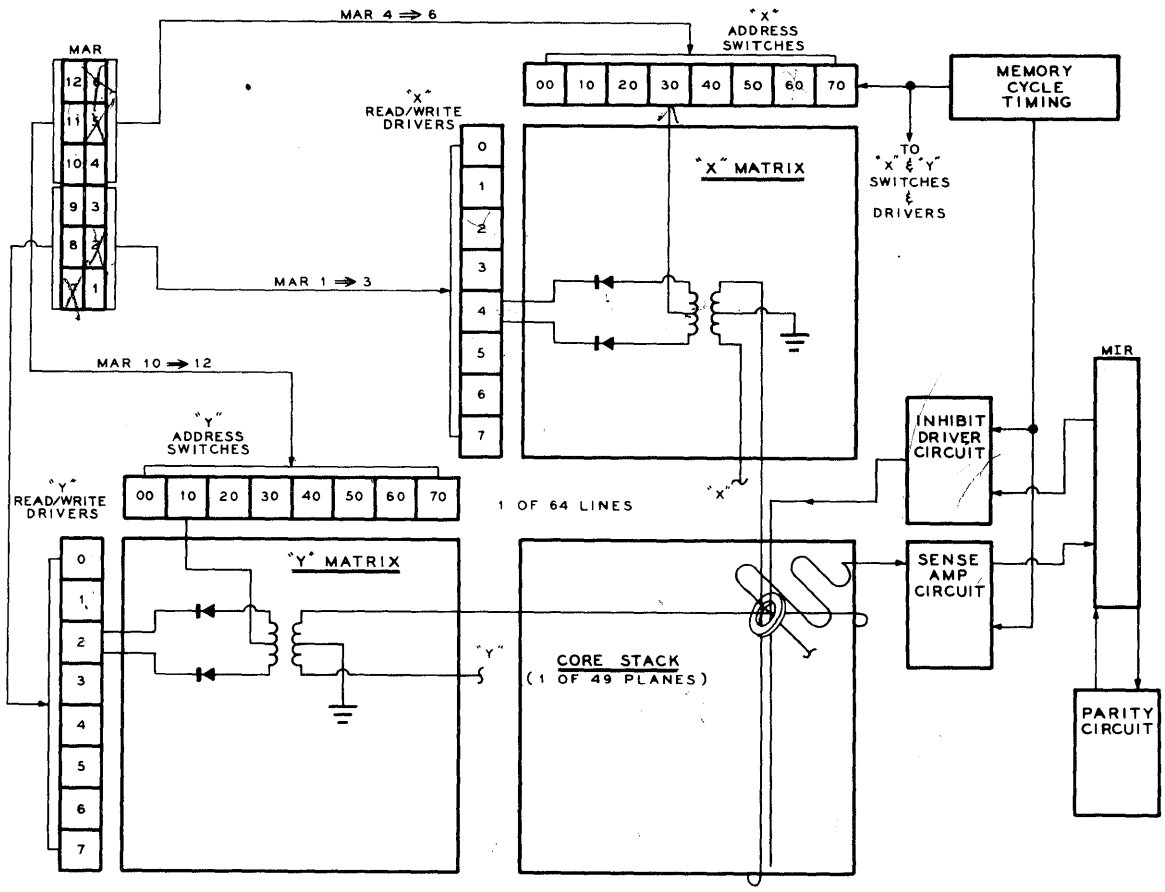


FIGURE 3.2-1
LOGICAL UNITS

The Addressing portion of this diagram consists of the Address Register (MAR), "X" and "Y" switches, "X" and "Y" Read/Write drivers, the "X" and "Y" Transformer Matrices, and the "X" and "Y" lines to the Stack. The Memory Timing circuits go to the "X" and "Y" Address switches and Read/Write drivers as an enabling level to indicate when they are turned ON.

"X" and "Y" line selection is under control of the Address Register which can be of any octal value of 0000 thru 7777. For decoding purposes, the Address Register can be divided into four sections. Refer to Figure 3.2-2.

The six Low order bits of the Address Register (bits 1 thru 6) are used to select the "X" line to the Stack. The six High order bits of

the Address Register (bits 7 thru 12) are used to select the "Y" line to the Stack. The six bits of "X" or "Y" are in turn separated into two groups, Tens and Units, which are also referred to as High (Tens) and Low (Units). The following is a description of the Address Register usage.

MAR 1 thru 3 Units X (Low-X)
Selects "X" Read/Write drivers.

MAR 4 thru 6 Tens X (High-X)
Selects "X" Address switches.

MAR 7 thru 9 Units Y (Low-Y)
Selects "Y" Read/Write drivers.

MAR 10 thru 12 Tens Y (High-Y)
Selects "Y" Address switches.

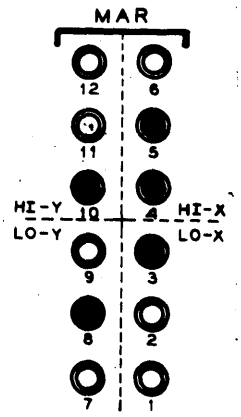


FIGURE 3.2-2
MEMORY ADDRESS REGISTER

Figure 3.2-1 shows the MAR usage with MAR 1 thru 3 gating the "X" Read/Write drivers to select one of the seven drivers (X0 thru X7). MAR 4 thru 6 gates the "X" Address Switches to select one of the seven switches (X00 thru X70). Likewise, the six High order bits of MAR are used to select one "Y" Read/Write driver (MAR 7 thru 9) and one "Y" Address switch (MAR 10 thru 12).

"X" & "Y" Numbering

Core Addresses are comprised of four octal digits of which the "Y" is always the two High order digits, and the "X" is always the two Low order digits. For example: If the Address Register contained the configuration of bits as indicated by the black circles shown in Figure 3.2-2, then the Stack location being accessed is Address 1234. The six High order bits of the Address Register contain a value of Tens 1 and Units 2 for an octal value of 12. This will result in the "Y"-12 line of the Stack being selected.

The six Low order bits of the Address Register contain a Tens 3 and a Units 4 for an octal value of 34. This will result in the X-34 line in the Stack being selected. The Core Address 1234 is located where the "X" and "Y" lines intersect each other in the Stack, once in each Core Plane.

The "X" and "Y" lines are numbered to correspond to the values available in the Address Register. The possible combinations for the "X" or "Y" are 00 thru 77 in the Address Register. The "X" and "Y" lines are also numbered 00 thru 77, with the number of the particular "X" or "Y" line selected corresponding to the configuration in the Address Register.

Matrix Transformers

Each "X" or "Y" line originates at the secondary of a Transformer in the "X" or "Y" Transformer Matrix. Refer to Figure 3.2-1. There are 64 "X" and 64 "Y" Transformers (one for each "X" line and one for each "Y" line) numbered to correspond to the "X" and "Y" lines 00 thru 77.

The Matrix Transformers are mounted on four Transformer boards located at each end of the Core Stack. See Figure 3.2-3.

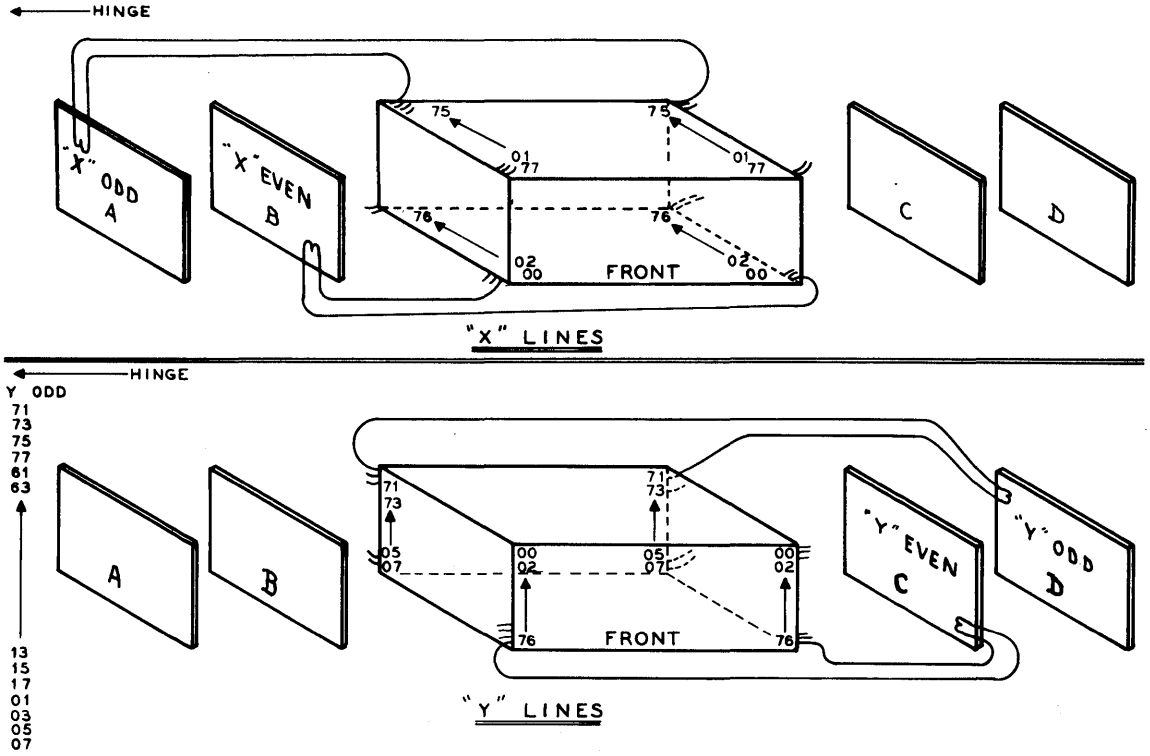


FIGURE 3.2-3
TRANSFORMER BOARD LOCATION

The boards labeled A and B are for the "X" lines, and boards C and D are for the "Y" lines. The two Transformer boards for either the "X" or "Y" contain 32 Transformers on each board. The odd numbered Transformers are on the Odd "X" board A and Odd "Y" board D. The even numbered Transformers are on the Even "X" board B and Even "Y" board C. In both cases ("X" or "Y"), the Odd numbered boards are located furthest from the Stack.

The Transformers on each of the Transformer boards is arranged in a 4 x 8 Matrix with two of the boards combining to form an 8 x 8 Matrix for either the "X" or "Y" line selection. See Figure 3.2-4.

The secondary of each Transformer has its center tap grounded for elimination of noise, and a resistor across the secondary to dampen the signal going into an inductive load. They are grounded through their respective Address Switch Package (SWAD) via the ground lines labeled X00G thru X70G.

The primaries of the Matrix Transformers are connected to the outputs of the Address switches and the Read/Write drivers (DRAC). Each of the SWADs goes to the primary center taps via the lines labeled X00S thru X70S. Each side of the Transformer primary goes to the Read/ Write drivers, one side for the Read (XR0D thru XR7D), and the other side for the Write (XW0D thru XW7D).

Each side of the Transformer primary of each Transformer has a diode (also mounted on the Transformer boards) for isolation purposes. These diodes prevent current from flowing in any Transformer except the Transformer selected by the SWADs and DRACs.

Memory Address Switch (SWAD)

Each SWAD has five inputs, four Address inputs and one Timing input. Refer to Figure 3.2-4. The Address inputs consist of one input from A05F and A06F, and both outputs from A04F of the Address Register. A05F and A06F select which of the SWAD packages will be used, and A04F determines which of the two switch circuits within each of the packages will be used.

X00S = A04F/ · A05F/ · A06F/ · MS1M

X10S = A04F · A05F/ · A06F/ · MS1M

In the X00 SWAD, the Address inputs are A04F, A04F/, A05F/ and A06F/. The above logic indicates that if A04F/ is TRUE, then the switch output X00S will be enabled. If A04F is TRUE, indicated in Odd Tens, then the switch output X10S will be enabled.

The Timing input of MS1M is TRUE during the entire Memory operation, Read and Write portion, to enable the selected switch for the entire Memory operation.

When a SWAD output is enabled, it places +30V at the center tap of each of its Transformers. When the SWAD is NOT enabled, the package output is an open circuit. For a detailed description of the SWAD package, refer to Section 3.7.

Read/Write Drivers (DRAC)

There are 16 DRAC packages in the B461 Core Memory, eight "X" drivers and eight "Y" drivers. Each of the Driver packages has five inputs, three Address inputs and two Timing inputs. The "X" Read/Write Drivers in Figure 3.2-4 are gated by the three Low order bits of the Address Register (A01F, A02F and A03F). The configuration of these bits determines which DRAC package is selected. For example: If the Units "X" position of the Address Register contained a value of 2, then the Address levels A01F/ and A03F/ will be TRUE to select the DRAC with the XR2D and XW2D outputs.

XR2D = A01F/ · A02F · A03F/ · MR2M

XW2D = A01F/ · A02F · A03F/ · MW2M

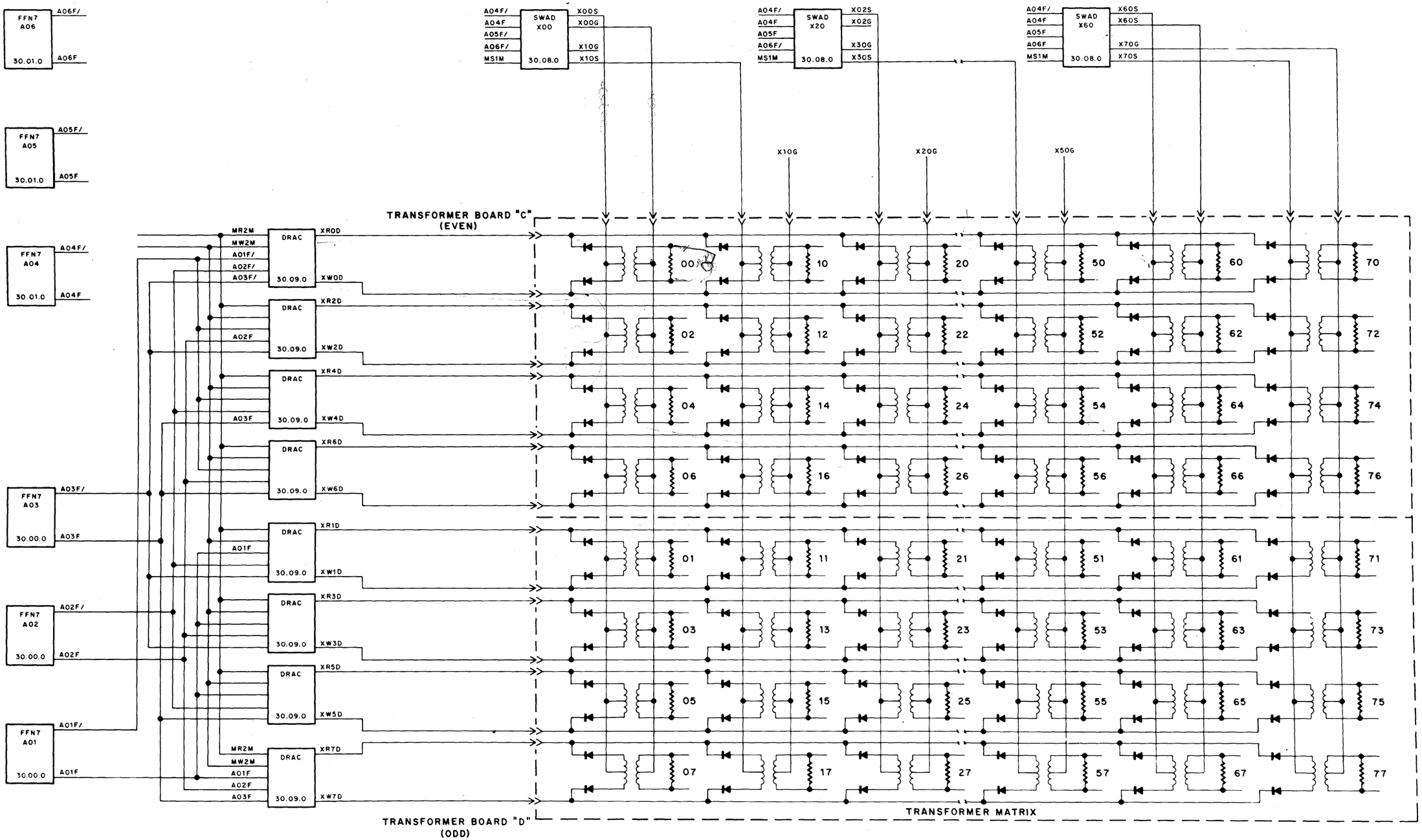


FIGURE 3.2-4
TRANSFORMER SELECTION

Each DRAC contains two individual Driver circuits of which the Address inputs are common. The difference is in the Timing inputs to the package. MR2M (Memory Read 2 Multi) will enable only the Read Current Driver (XR2D). This Timing Multi is TRUE for one microsecond during the Read portion of a Memory operation. The other Timing input is MW2M (Memory Write 2 Multi) which will enable only the Write Current Driver (XW2D) in the DRAC. This Timing Multi is TRUE for one microsecond during the Write portion of a Memory operation.

When a Read or Write Driver is enabled, its output goes toward -30V. This -30V goes to one side of eight Matrix Transformers, one of which will have +30V at the center tap from a SWAD to allow current to flow in that Transformer only. For example: If the Address Register contained an "X" value of 24, the SWAD with the X20S output will be enabled and the DRAC with the XR2D and XW2D outputs will be enabled. Where the outputs of the above two packages intersect, that particular Transformer will be selected. In this example, it would be the Transformer numbered 24 selecting the "X" line of the same number. For a detailed description of the DRAC package, refer to Section 3.6.

The above description and references were made in respect to the selection of an "X" line to the Stack. One should keep in mind that the "Y" line selection with its Address switches and Read/Write drivers is identical to the "X". The only difference is in the mnemonics used. Where the "X" has been used as in X00S, the "Y" line selection will instead use a "Y", as in Y00S.

Matrix Transformer Operation

Figure 3.2-5 is a simplified diagram of the SWAD and DRAC connection to a Matrix Transformer. When all inputs are TRUE to enable the SWAD, its output transistor Q2 will be forward biased to allow it to go into conduction. This will complete a path from the center tap of the transformer primary through Q2 to the +30V Supply. When all inputs to DRAC are TRUE (Read first due to MR2M), Transistor Q2 will go into conduction, turning on Q3.

This will complete a path for current from the -30V Read through Q2 and Q3 of the DRAC, through diode "r" and the Transformer (left to right), out the primary center tap through Q2 of the SWAD to the +30V Supply. The direction of this Read current is indicated in Figure 3.2-5 by the solid arrows. The current induced into the Transformer secondary is the Read current in an "X" or "Y" line connected to this particular Transformer.

After the level MR2M goes FALSE and the Read driver is disabled, the Write driver will be turned ON with the level MW2M. This will turn ON transistors Q2 and Q3 in the Write driver to complete a path for current flow from the -30V Write to the +30V Supply. The current in the primary of the Matrix Transformer will be from right to left to induce the Write current into the secondary of the Transformer and the "X" or "Y" line in the appropriate direction for a Write of binary ones in the Core Stack as indicated by the dashed arrows, in the opposite direction of the Read current.

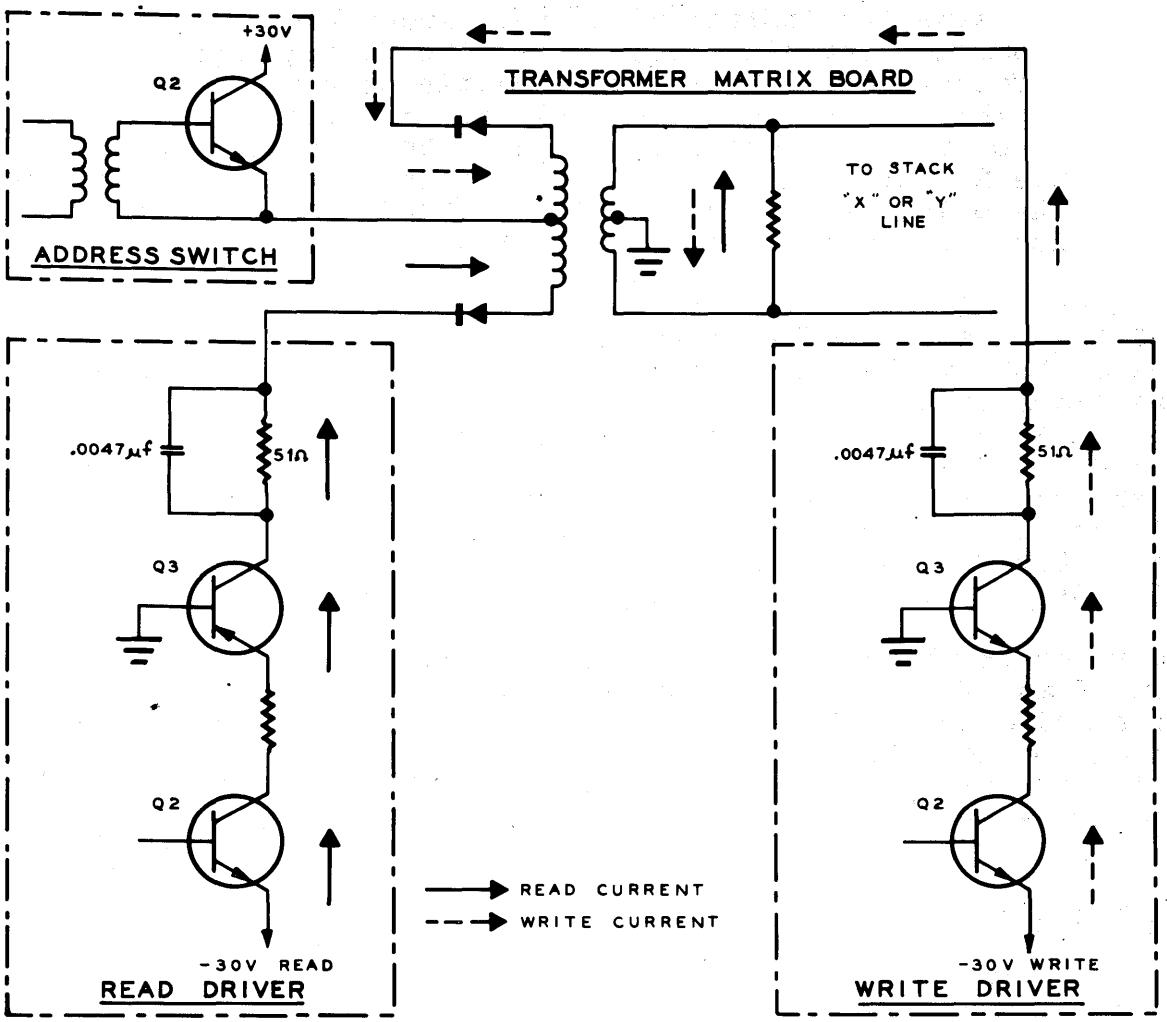


FIGURE 3.2-5
TRANSFORMER CONNECTIONS

Memory Address Register (Set & Reset)

Whenever an external Unit, Processor or I/O request a Memory access, it must provide the Memory Module with a Core Address. This Address is set into the Memory Address Register (single ended) at the start of a Memory operation. When the Memory operation is completed, the Memory Module will clear the Memory Address Register in preparation of a future Memory operation.

Figure 3.2-6 is a Logical Schematic Diagram of the Set and Reset circuitry of any one of the Address Register Flip-Flops. This circuitry is duplicated for each of the 12 bits in the Address Register.

The Address Register Flip-Flop in Figure 3.2-6 is Set when the output of AND gate A is TRUE. The inputs to gate A are AnnS-C and MSTD. The AnnS-C level is one of the 12 Address lines from Central Control (A01S thru A12S) and it will be TRUE when the bit in the Address Register is to be Set.

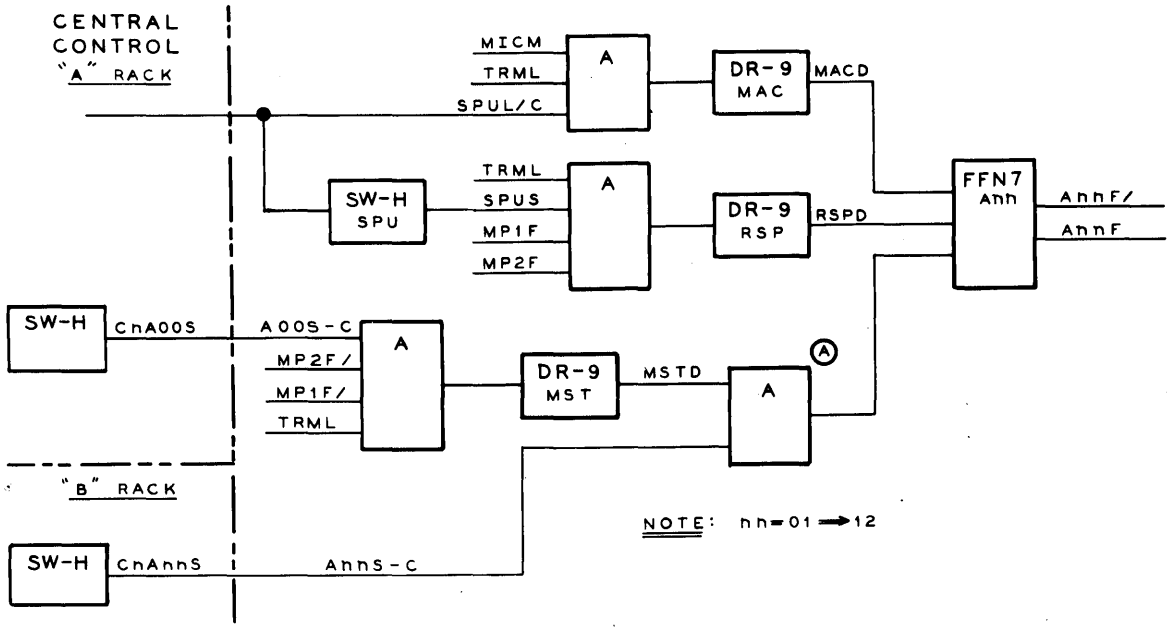


FIGURE 3.2-6
ADDRESS REGISTER SET/RESET

$$MSTD = A00S\text{-}C \cdot MP2F/ \cdot MP1F/ \cdot TRML$$

MSTD is a Control level in the Memory Module used to start a Memory operation when the Memory Module is in REMOTE. It is TRUE only at the start of the Memory operation for one microsecond due to the input A00S-C. The term TRML comes from the LOCAL/REMOTE switch in the Memory Module and is true when the switch is in the REMOTE position.

MP2F/ and MP1F/ are the zero outputs of the Memory Pulse Counter Flip-Flops and they will both be true when the Counter is equal to zero. With MPC = 0, the Memory Module is not completing any previous Memory operation and is ready to begin the next Memory access. A00S-C is the Memory Start Pulse from Central Control to start the Memory operation. It is TRUE for one microsecond after an external Unit, Processor or I/O gains access to the Memory Module.

When all inputs to MSTD are TRUE, MSTD will be gated with AnnS-C. If AnnS-C is also TRUE, then the Address Register Flip-Flop is set via the Clocked set input of the flip-flop.

Resetting of the Address Register Flip-Flops when in REMOTE, is done with either MACD or RSPD. The NORMAL clear is with MACD.

$$MACD = MICM \cdot TRML \cdot SPUL/\text{-}C$$

MACD (Memory Address Clear Driver) will be used to reset the Address Register if the Memory Module is in REMOTE (TRML) and the System is in the NORMAL Clock Mode of operation (SPUL/-C. The term SPUL/-C originates in D & D at the System Clock Control switch (Single-Double-Normal Pulse) and is true when the switch is in the NORMAL position. If the switch is in the Single or Double Pulse position, the level SPUL/ will

be FALSE to inhibit the use of MACD to clear the Address Register.

If the System is in the NORMAL Clock Mode and the Memory Module is in REMOTE (SPUL/ · TRML), then MACD will clear the Address Register when the Timing level MICM (Memory Information Clear Multi) is TRUE. This Timing level will be TRUE at the end of a Memory access with the prime purpose of clearing the Memory Information Register. MACD is to the Unclocked side of the flip-flops in the Address Register.

If the System Clock Control switch is in Single or Double Pulse, the MACD level will be inhibited with SPUL/ being FALSE. SPUL/, through a switch, develops SPUS which will enable RSPD (Remote Single Pulse Driver).

RSPD = TRML · SPUS · MP1F · MP2F

The time that RSPD will occur is determined by the setting of the Memory Pulse Counter instead of MICM. RSPD will be enabled when the Pulse Counter is equal to a value of three. This Clear level goes to the Clocked Reset of all Address Register flip-flops. Using the Pulse Counter for Timing allows the Register contents to remain for visual examination when in Single or Double Pulse.

Memory Address Register Count

All the gating for the Set and Reset of the Address Register contains the term TRML which is TRUE when the Memory Module is operated in REMote. However, when operating the Memory Module with the LOCAL/REMOTE switch in LOCAL, TRML will be FALSE to inhibit all of the Set and Reset circuitry of the Address Register. When in LOCAL, the Memory Address Register is counted as a binary counter from 0000 thru 7777 and back to 0000.

Figures 3.2-7 and 3.2-8 illustrate the Memory Address Register with the necessary gating for Address counting. The Address Register is divided into two parts, "X" and "Y". The "X" portion shown in Figure 3.2-7 consists of bits 1 thru 6 and its associated gating. Figure 3.2-8 shows the "Y" portion of the Register which consists of bits 7 thru 12 and its associated gating. The input gating of the flip-flops requires all Lower order bits of the Register to be in the "one" state before any bit can be complemented.

Counting of the "X" portion of the Address Register is controlled by COXL and A + 1D. Counting of the "Y" portion is controlled by COYD. COXL (Count-X Level) comes from the Count-X switch on the Maintenance Panel. This level will be TRUE with the switch in the Count position. If the counting of bits 1 thru 6 of the Address Register is to be inhibited, the Count-X switch is put into the Inhibit position. COXL will then go FALSE to inhibit all of the Count Logic for bits 1 thru 6. A + 1D (Address Register Plus One Driver) is the controlling level for any Address Register counting. It will be TRUE for one microsecond at the time that the Address Register is to be counted.

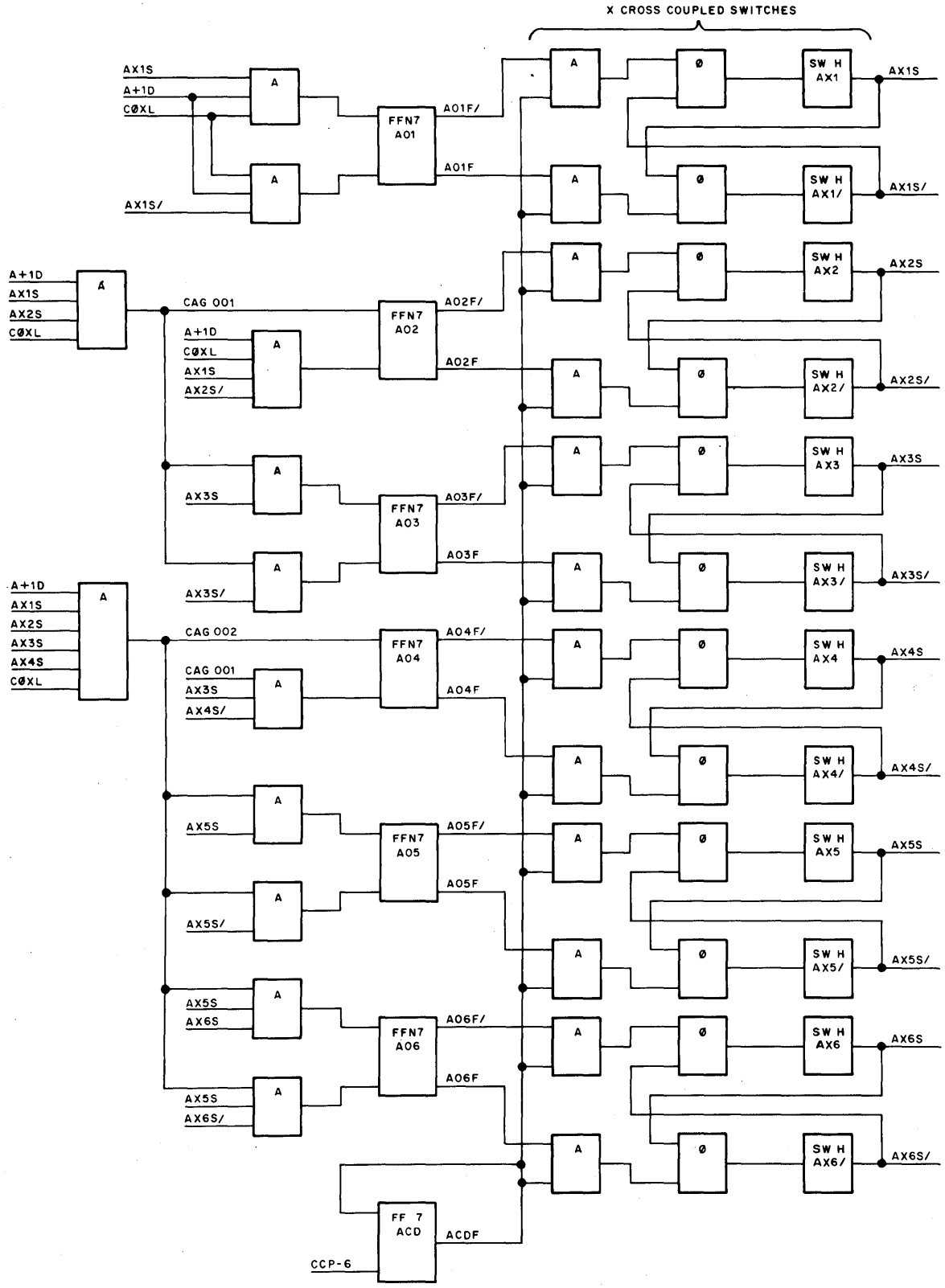


FIGURE 3.2-7
MAR 1 THRU 6 COUNT LOGIC

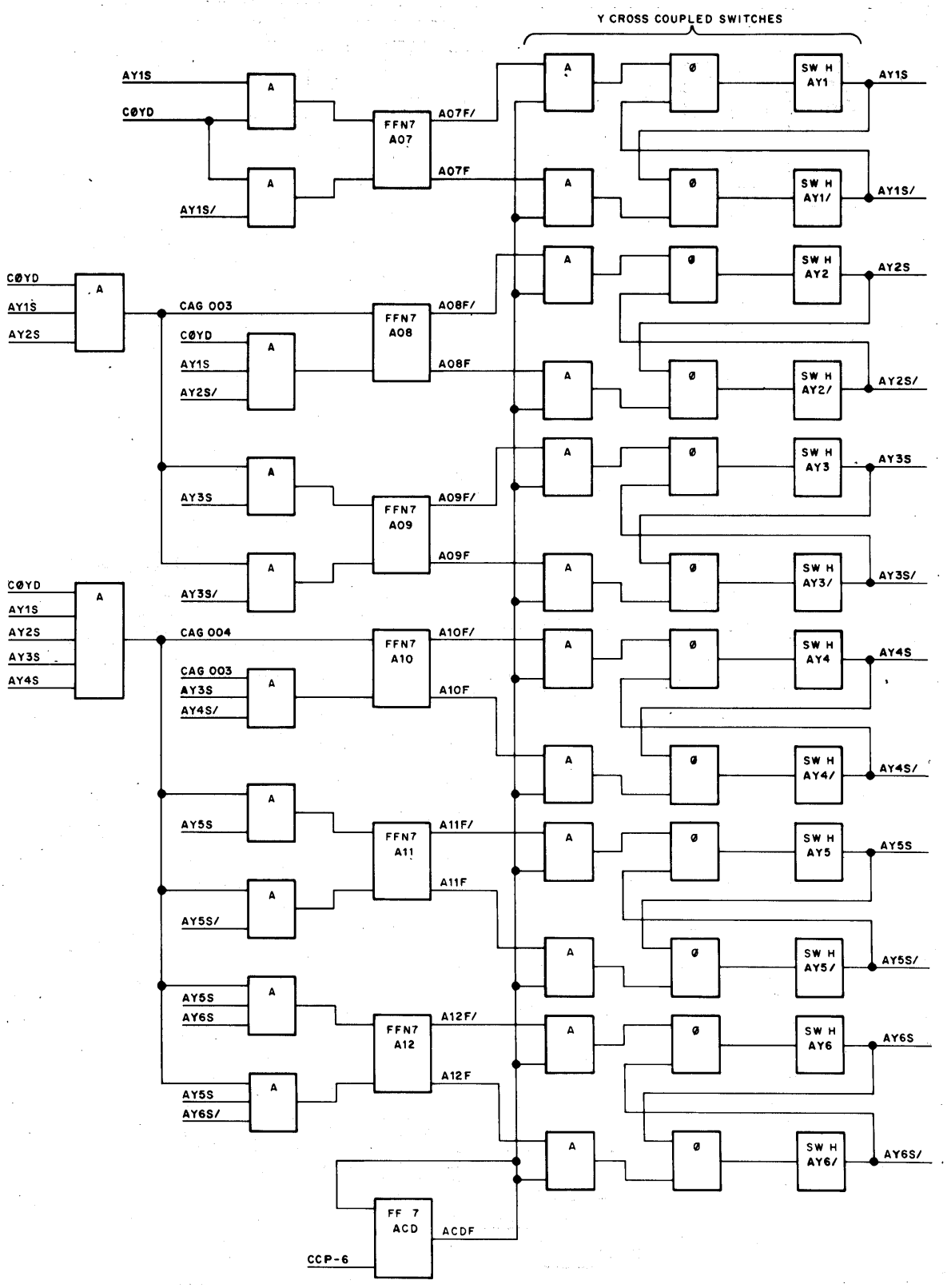


FIGURE 3.2-8
MAR 7 THRU 12 COUNT LOGIC

The remaining inputs to the Count Logic are from the "X" and "Y" cross-coupled switches labeled AX1S thru AX6S for the "X", and AY1S thru AY6S for the "Y". These inputs are used to decode the configuration of bits in the Address Register to determine the next count in the Register. The cross-coupled switch outputs will reflect the setting of the Flip-flops. AX1S will then be TRUE if A01F is TRUE.

CAG 001 = A + 1D · AX1S · AX2S · COXL

Some of the cross-coupled switch outputs are grouped together as a common line via the Common AND Gates. Refer to Figure 3.2-7 and examine CAG 001. Its output will be TRUE when A + 1D is TRUE, the Count-X switch is in the Count position (COXL), and the two Low order bits of the Address Register are both ON.

CAG 002 = A + 1D · AX1S · AX2S · AX3S · AX4S

Common AND Gate 2 (CAG 002) in turn will be TRUE if the four Low order bits are ON with the controlling levels (A + 1D · COXL).

CAG 003 = COYD · AY1S · AY2S

CAG 004 = COYD · AY1S · AY2S · AY3S · AY4S

The two CAGs for the "Y" portion of the Address Register (see Figure 3.2-8) give the same Address values as the CAGs for "X". The difference is in the Control level used, COYD, which includes the A + 1D term.

The cross-coupled switches are used to provide a delay of the flip-flop outputs to the Count gating. This delay is necessary due to the lack of a delay within the FFN7s in the Address Register. Refer to Section 3.10 for a detailed description of the FFN7 circuit.

The outputs of the Address Register Flip-Flops change state as soon as the flip-flop is switched. For correct counting (prevention of double counting), the gating to the Count Logic must be delayed until after the Clock Pulse. The time of this delay is controlled by ACDF (Address Count Delay Flip-Flop). ACDF is a standard type flip-flop (FF7) with the output delayed from the input. ACDF is set (Unclocked input) with each Clock Pulse (CCP-6). The one output goes to the Unclocked Reset to turn ACDF OFF.

Referencing Figure 3.2-9, assume that the flip-flop (A01) is in the "Set" state (A01F is TRUE and A01F/ is FALSE) and the outputs of the cross-coupled switch reflect the status of the flip-flop(AX1S is TRUE and AX1S/ is FALSE). The next count will Reset the Address Register bit (AX1S · COXL · A + 1D), the flip-flop outputs changing when the Clock Pulse arrives. Refer to the Timing chart in Figure 3.2-9. This same Clock Pulse will set ACDF. With ACDF set, the cross-coupled switch will also change state. The top AND gate (A01F/ · ACDF) output will be TRUE to make AX1S FALSE, and the bottom AND gate (A01F · ACDF) will have a FALSE output to make AX1S TRUE. Note that the cross-coupled switch does not change state until after ACDF is set. The next count will set A01F (COXL · A + 1D · AX1S/) and the resulting action with ACDF

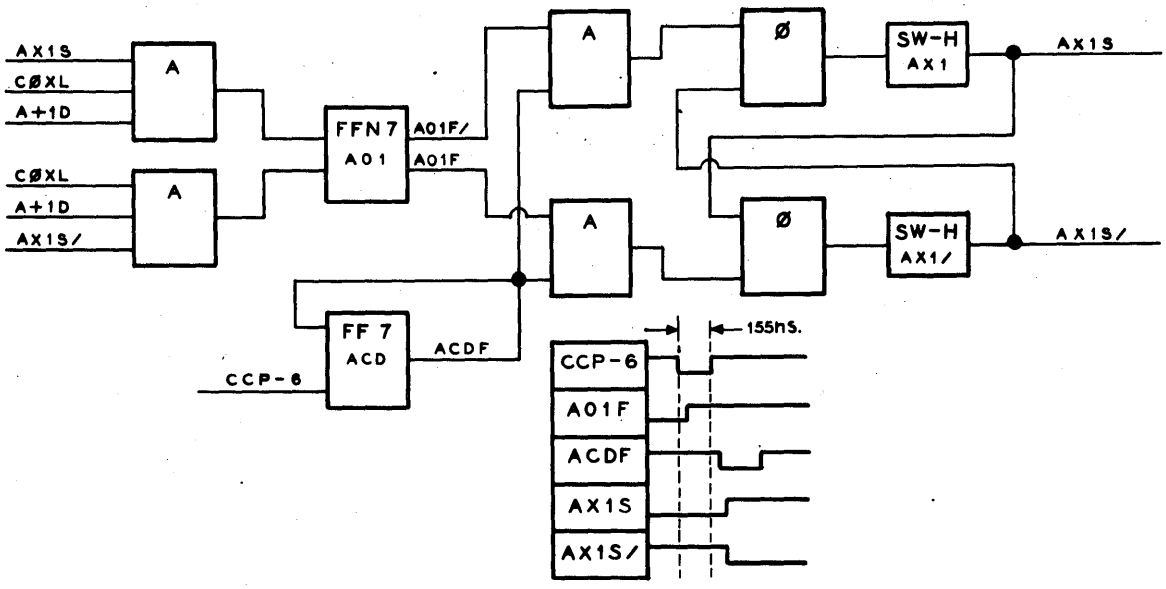


FIGURE 3.2-9
A01F COUNT AND TIMING

will transfer the state of the cross-coupled switch to again reflect the status of the flip-flop. If at any time that ACDF is in the "set" state and the flip-flop had not been changed with the count, then the state of the cross-coupled switch will not change either.

$$A + 1L = A + 1S \cdot TRMS/$$

The A + 1D level is the enabling level for all counting of the Address Register. Refer to Figure 3.2-10. The input to the A + 1 Driver is from an OR gate with two inputs. The top input is A + 1L which is developed any time the STEP MAR switch is depressed and the Memory Module is in LOCAL. A + 1L comes from a Synchronizer circuit which will allow the level A + 1L to be TRUE for only one Clock Pulse.

The bottom input of the OR gate feeding the A + 1 Driver comes from an OR gate with four inputs and a SHUNT AND on its output. The SHUNT AND is made up of the Count/Inhibit level, Memory Start Flip-Flop, and the "Worst Case" Flip-Flop (COML · MSTF · MWCF/). if the counting of the entire Address Register is not to be inhibited (COML is TRUE), and a Memory operation is to be initiated when in LOCAL (MSTF), and the "Worst Case" Flip-Flop is not ON (MWCF/), then the SHUNT AND will allow the output of the OR gate to go TRUE. MWCF/ is used to inhibit any counting of the Address Register when the operation is a "Worst Case" pattern and the last cycle of an Address has not been completed.

The top input to the OR gate from AND gate 2 will be true when the Pulse Counter equals three and the Manual level from the Manual/Auto switch is TRUE.

(MP1F · MP2F · MANL). This gate is used when the Memory is operated in Manual to allow only one Memory access at each Address. Gate 3 is

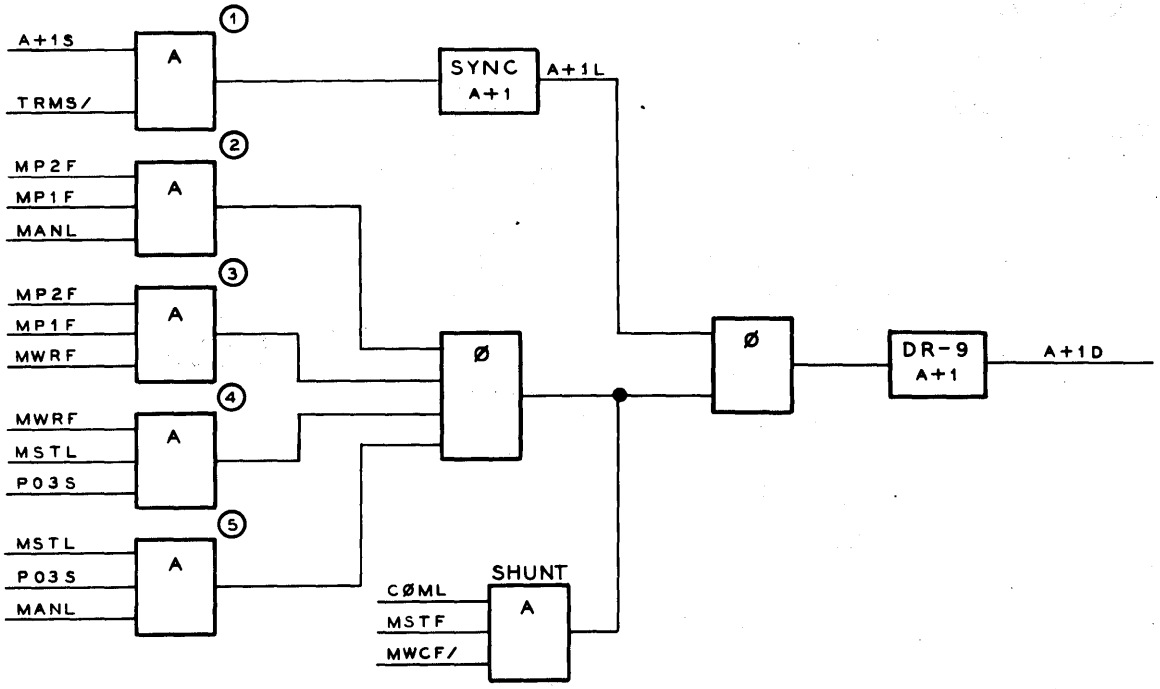


FIGURE 3.2-10
A + 1D LOGIC

used when the Memory is operated in either Auto or Checkerboard and will allow more than one operation at each Address. In this case, the Memory operation that finds the Memory Write Flip-Flop in the "one" state will count the Address Register if the SHUNT AND is also TRUE.

The usage of gates 4 and 5 corresponds to that of gates 3 and 2. The time that they will have a true output is determined by P03S (Pulse Counter Equal Zero or Three). Gates 4 and 5 will then allow the Address Register to be counted at either the beginning or end of a Memory operation. This will provide a count for the Address Register when the Memory Module is operated in Single cycle or if a Stop On Error should occur.

The Count-Y Driver is used to count the "Y" portion of the Address Register. Refer to Figure 3.2-11. The prime control on the input to the COY Driver is the SHUNT AND. The input to the Shunt will be true if the Count-Y switch on the Maintenance Panel is in the Count position as it is shown. Actually, the input will be floating which will give it the same effect as being true.

The OR input from AND gate 1 (top OR input) will be true if the mnemonic COXL/ is true, that is, the counting of the "X" portion of the Address Register is being inhibited. COXL/ ANDED with A + 1D will count the Address Register bits 7 thru 12, irregardless of the configuration of the six Low order bits of the Register.

The normal development of COYD is with AND gate 2. If the A + 1D level is TRUE and all Low order bits of the Address Register are in the "one" state, AX1S thru AX6S, then count the "Y" portion of the Register by

enabling COYD.

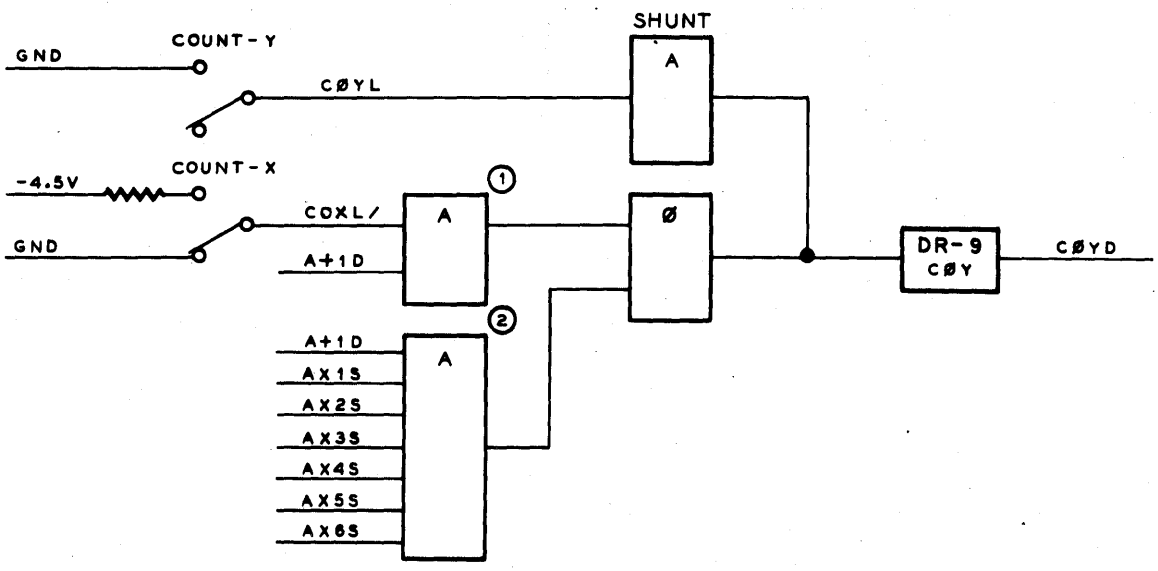


FIGURE 3.2-11
COUNT-Y DRIVER

3.3 READ/WRITE CONTROL

The Memory Module is capable of Reading and Writing Information into the Core Stack. This is accomplished by setting a core to record an Information bit and resetting the core to Read it out. The circuitry for controlling the setting and resetting of the cores consists of:

1. Inhibit Drivers for recording Information.
2. Sense Amplifiers for Reading Information.
3. An Information Register to store the Information until it can be Written, or during a Read, store the Information until it is checked and sent to the Accessing Unit.
4. Control circuitry to control the flow of Information by determining whether a Read or Write operation is being performed.

Figure 3.3-1 is a block diagram of the Core Memory Logic and shows the Read/Write circuitry.

During a Write operation, 48 bits of Information are loaded into MIR at the beginning of a Memory cycle via Central Control. The output of MIR is then sampled by the Parity circuits and the correct Parity is set into MIR-49 (I49F). During this first half of the Memory cycle, the appropriate Address switches and Read drivers are selected from the Address and the cores of this Address are Reset.

During the second half of the Memory cycle, the Information contained in MIR is used to control the cores that are to be set back into this selected Address. If a MIR Flip-Flop is loaded with a zero, the zero side (NOT) output will be TRUE. This true is ANDED with MIHD which is TRUE during the Write portion of the Memory cycle and used to activate the Inhibit Driver. The Inhibit Driver output is used to feed the Inhibit winding of the associated plane in the Core Stack and is physically laid out in such a manner that the effect of current flow through the line will oppose the effect of the current flow in the "X" and "Y" lines. The result is that the Memory core that is receiving a Half-Select current from both the "X" and "Y" lines and an opposing Inhibit Half-Select current will not be set to the "ones" state, since the resulting current effect is only half the required current to set a core.

During the Memory Read operation, the Information flow is somewhat opposite than that of the Memory Write operation. The Read operation is started when the Memory request is received from Central Control (A00S). The Address is decoded and the appropriate Address switches and Read Drivers are selected. These allow the Read current to flow through the "X" and "Y" lines, selecting the proper Address.

All the cores that are set to the "one" state will now be reset to the "zero" state. Each plane in the Core Stack also has a Sense winding. A signal will be induced in the Sense line by any Memory core in that

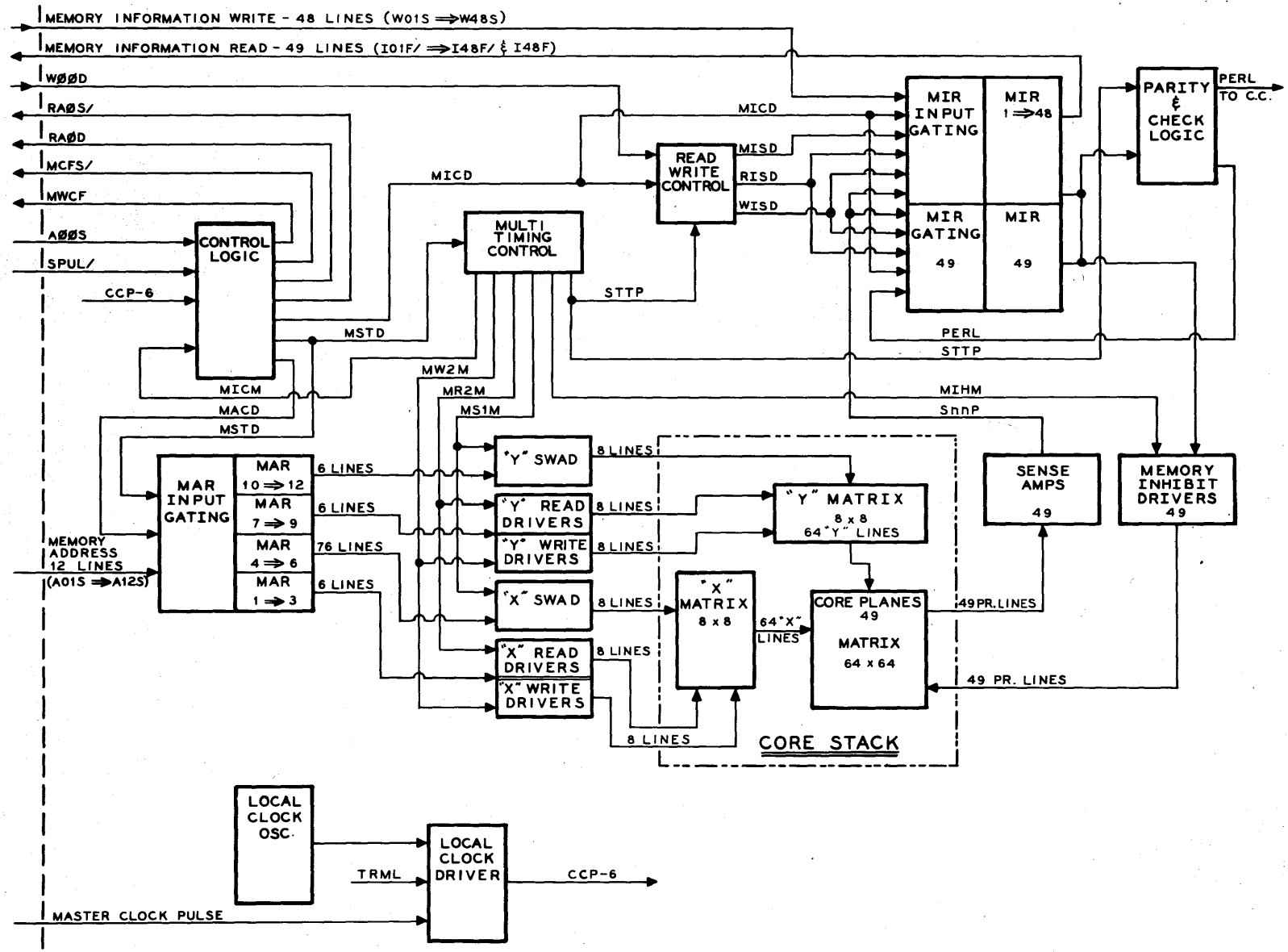


FIGURE 3.3-1
BLOCK DIAGRAM CORE MEMORY LOGIC

plane being driven from a one to a zero. The Sense line passes through all cores in a plane in a checkerboard manner that will permit maximum cancellation of noises that are induced due to Half-Select currents flowing through the cores. The signal induced into the Sense winding from a core being reset, may be either a positive or negative pulse, depending upon the Address and plane of the selected core. The Sense winding is terminated at the Sense Amplifier associated with this winding.

The Sense Amplifier amplifies and shapes the induced signal and is designed to accomodate either positive or negative signals. The amplified signal is gated with the Read Strobe Pulse (RISD) to permit a pulse to set the MIR Flip-Flop (InnF). This Strobe Pulse was inhibited during the Write operation to prevent destroying the Information in MIR.

The Information that has just been set into MIR is now available to the Requesting Unit via Central Control. The Information is also available to the Parity Check circuits to be checked for the correct Parity. An indication of this is also sent to Central Control.

During the rest of the cycle, the Information in MIR is being written back into the Core Stack in the same manner as the Write operation.

A Memory Module must go through a complete Memory cycle regardless of the type of access requested. A Memory cycle consists of a Read phase and a Write phase. During the Read phase, current flows through the selected "X" and "Y" lines in a direction that will reset all selected cores to the "zero" state. This is a destructive type of Read-out.

During the Write phase, current flows through the lines in a direction that will set all selected cores to the "one" state. The Inhibit Drivers which are gated by the NOT side of the MIR Flip-Flops, inhibit the setting of those cores that are to store zeros. A Write phase is required during a Memory Read operation to re-Write the Information back into the cores after the destructive Read-out. A Read phase is required during a Memory Write operation to clear the cores prior to the Write phase of the operation.

Bit 49 of MIR is the Parity bit. Its status is developed within the Memory Module and does not get transferred to Central Control. In the B461 Memory, the Parity used is ODD.

Figure 3.3-2 shows the Read/Write Control circuitry. The gating for MIR bits 1 thru 48 are the same, so only one is shown. The substitution of 1 thru 48 for the nn will give the proper mnemonic for each of these flip-flops.

The MIR flip-flops are of the FFN7 type. This type of flip-flop is the same as the 20-70 except the delay lines and complementing diodes have been removed. The output delay of this type of flip-flop is approximately 80 nano-seconds.

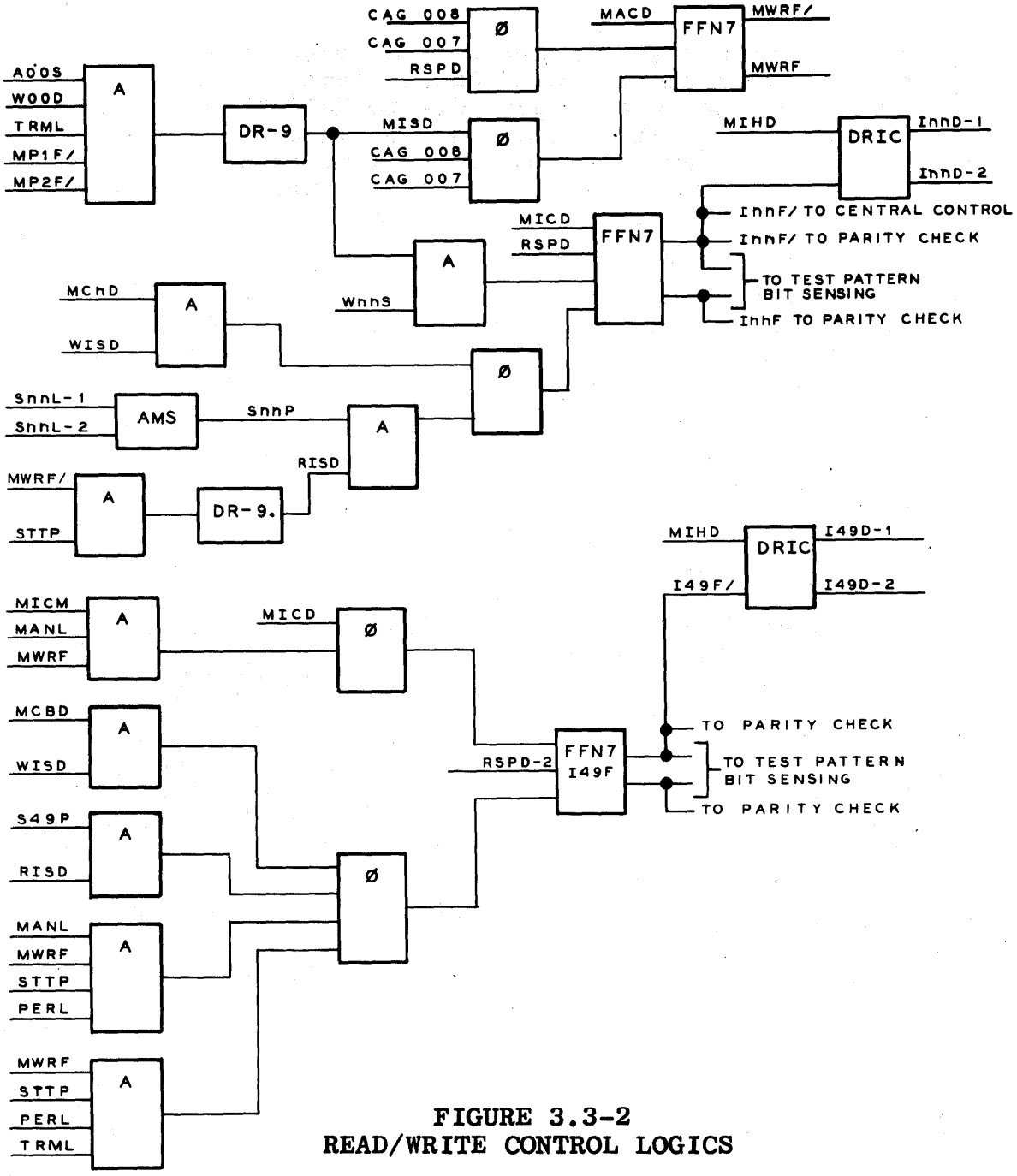


FIGURE 3.3-2
READ/WRITE CONTROL LOGICS

Write Operation

The Write cycle begins when A00S and W00D are received from Central Control. These two levels are ANDED with Remote (TRML) and the Memory Pulse Counter equal to zero (MP1F/. MP2F/) to produce Memory Input Strobe (MISD). MISD being true will be used to set the Memory Write Flip-Flop (MWRF) and gate the Input Information (WnnS) from Central Control into MIR bits 1 thru 48. The outputs of the 48 MIR flip-flops are then available to the Parity Check circuits. If the outputs of MIR are even, the Parity Error Level (PERL) will be TRUE. PERL is then ANDED with MWRF which is TRUE, TRML which is TRUE, and Strobe Timing

Pulse (STTP), which will come true in approximately 830 nano-seconds. The output of this gate will then set I49F. The MIR is now completely loaded and the outputs will be available at the Inhibit Driver Input. When Memory Inhibit Driver Timing Pulse (MIHD) goes TRUE, all MIR Flip-Flops that are not set will enable their associated Inhibit Drivers and prevent the "ones" from being written in these portions of the core.

Read Operation

During a Memory Read operation the Memory cycle is started by the A00S level from Central Control. The W00D level is FALSE to prevent setting MWRF and the MIR Flip-Flops from the WnnS lines. The Read Information is detected on the Sense winding of each core plane during the Read portion of the cycle. Each of the 49 Sense windings is connected to a Sense Amplifier (AMS) where the signal is amplified. The signals are then ANDED with a Read Information Strobe (RISD) and used to set the InnFs. Once the InnFs are set, the zero side output of 1 thru 48 is available to the Accessing Unit via Central Control. The outputs are also available to the Parity checking circuits where they are compared with I49F to insure an odd number of bits have been set. The Information will remain in the MIR until the completion of the Memory cycle when it is cleared by Memory Information Register Clear Driver (MICD). The other gating shown in Figure 3.3-2 is used for Maintenance purposes and will be explained in another Section.

3.4 MEMORY CYCLE TIMING

The Memory Cycle is basically the same for both the Read and Write Memory operations. Information is Written or Read from the Core Stack in a parallel manner. (Complete 49 bits of a word accessed simultaneously.)

Each plane of the Core Stack corresponds to one of the 49 bits of a word that can be stored in Memory. A core plane is designed such that it represents a 64 x 64 Matrix plane. Consequently, this 64 x 64 Matrix can Address any of the 4096 core locations in a plane by the use of "X" and "Y" lines.

To Read a word stored in the Core Stack, the selected "X" or "Y" lines are simultaneously pulsed with a Read current. the 49 Sense lines are individually interrogated for the presence of an induced current pulse. If a pulse is sensed in a line, a flip-flop which corresponds to that bit position is Set to record the fact that a "one" was sensed.

To Write a word into the Core Stack, the polarity of the current pulse in the selected "X" or "Y" lines must be reversed. This tends to Set the selected core in each plane to the "one" state. Generally, some of the Information bits to be stored are "ones" and the others are "zeros". An opposing current is passed through the Inhibit line of all core planes when the Information to be stored is a "zero".

Before Information can be Written into the cores, it is necessary that all cores at the selected Address are in the "zero" state. A Read operation will accomplish this purpose because it will cause all selected cores to be Reset.

Similarly, since a Read operation does destroy the Information stored in the cores, a Write operation is required after every Read operation to restore the Information back into the cores.

A Memory cycle is basically the same operation, whether the purpose of the Memory cycle is to store Information or recover Information previously stored. The only real difference is that during a Memory cycle generated for the purpose of storing, the Sense lines are not interrogated during the Read portion of the Memory cycle.

During the first part of the Memory cycle, Read currents are applied to the selected "X" and "Y" lines. The Sense signal is sampled or Strobed if this is a Memory access for the purpose of recovering previously Written Information. No Strobe is required for a Write access. During the last part of the Memory cycle, the "X" and "Y" line currents are applied in the opposite direction, and if a zero is to be stored, an Inhibit current will be applied to the appropriate planes.

Figure 3.4-1 shows the Memory cycle divided into two phases; the Read phase, and the Write phase. Each Memory operation, whether Read or Write, is made up of these two phases. The Memory operation is started with a level from Central Control that is synchronous with the System Clock. This level, called Memory Start Driver (A00S), is used to start

two separate Memory Timing circuits.

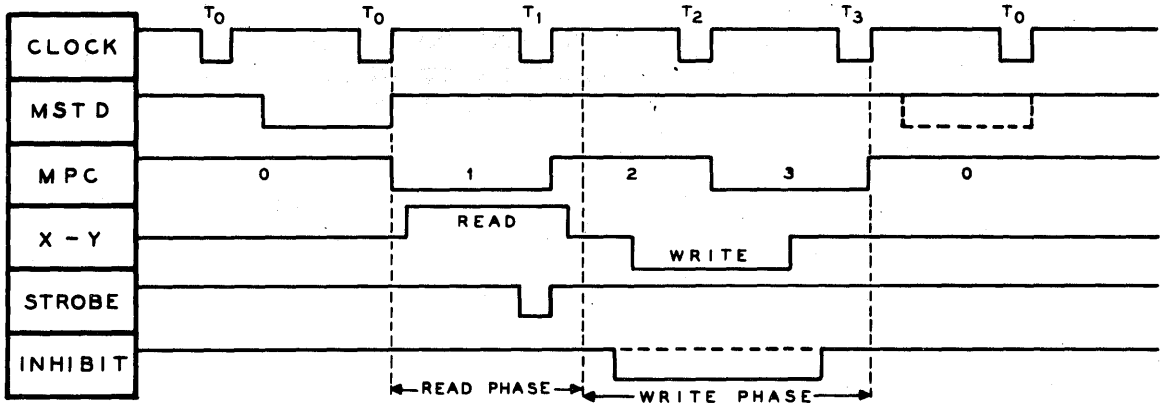


FIGURE 3.4-1
MEMORY TIMING CYCLE

1. Memory Timing that is External to the actual operation of the Core Stack is controlled by the Pulse Counter circuit. These operations consist basically of setting up the initial conditions and generating Control levels that will release the Requesting Unit. The Pulse Counter circuit is synchronous with the System Clock and will be referred to as Clocked Timings.

2. Memory Timing that is required for the Internal operation of the Core Stack is generated from the Multi Timing circuits. These operations consist of selecting the "X" and "Y" lines, Strobing the Sense lines, activating the Inhibit drives, and cleaning up at the completion of the Memory cycle. These timings are asynchronous to the System Clock and are referred to as Unclocked Timings.

Memory Pulse Counter

Refer to Figure 3.4-2.

The B461 Memory cycle is divided into four segments. Each of these segments has a duration of one microsecond. The associated segments are generated by a two-stage binary counter which is made up of flip-flops MP1F and MP2F. The outputs of the Pulse Counter Flip-Flops are used throughout the Memory Module as Control levels and is at a count of "zero" between Memory cycles. They are also decoded into Control levels that are sent to Central Control to synchronize the Memory operation with the System.

The Memory Pulse Counter will start counting with the next Clock Pulse after A00S becomes TRUE. A00S is ANDED with REMOTE (TRML) and Memory Pulse Counter equal to zero (MP1F/ and MP2F/). This pulse, through a driver, then becomes the Memory Start Pulse (MSTD). The next Clock Pulse with MSTD TRUE, will set MP1F. With MP1F Set, the next Clock Pulse will Reset MP1F due to TRML being TRUE, and Set MP2F due to MP1F being TRUE. The third Clock Pulse will set MP1F due to MP2F being

TRUE. The fourth Clock Pulse will set MP1F due to TRML, and Reset MP2F due to MP1F and TRML. Once MP1F and MP2F are both Reset, MSTD will have to become TRUE to start the Counter again.

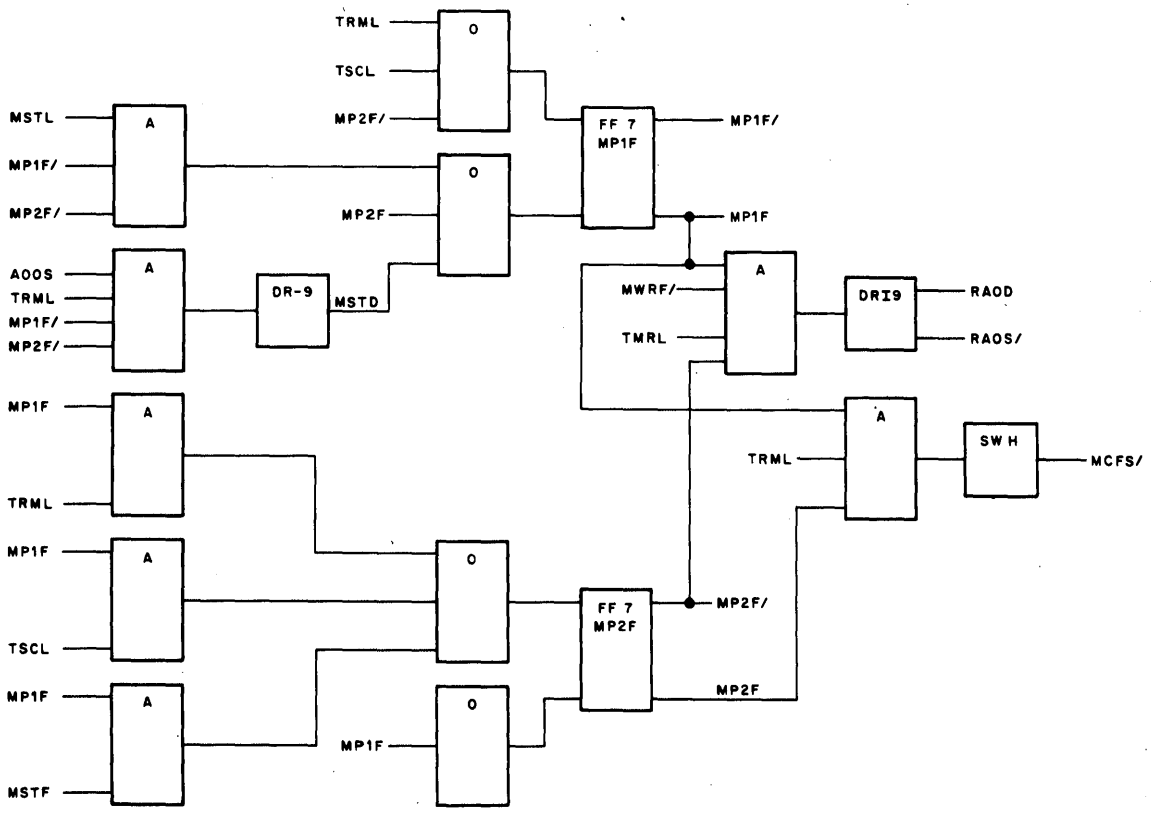


FIGURE 3.4-2
MEMORY PULSE COUNTER

RAOD is MT2F in Central Control. It is used to indicate Information will be available for use after the next Clock Pulse. This level is TRUE only on Memory Read operations. RAOS/ is MT2F/ in Central Control, and is used in resolving I/O conflicts on Memory Read operations.

MCFS/ is MT4F/ in Central Control, and is used to release the Memory at the completion of a cycle by clearing the Control Flip-Flops in Central Control.

Multi Timing Circuit

The Multi Timing circuits are used to generate the timings that are required to Read from, or Write into the Core Stack. Seven different timings are required. Refer to the Timing Diagram in Figure 3.3-3. The following is a list of the Pulses and their uses:

1. MS1M - This Switch Timing Pulse is used as a Control level for the selection of the "X" and "Y" Address switches. The switches are turned ON prior to the Read time and turned OFF after the Write time.

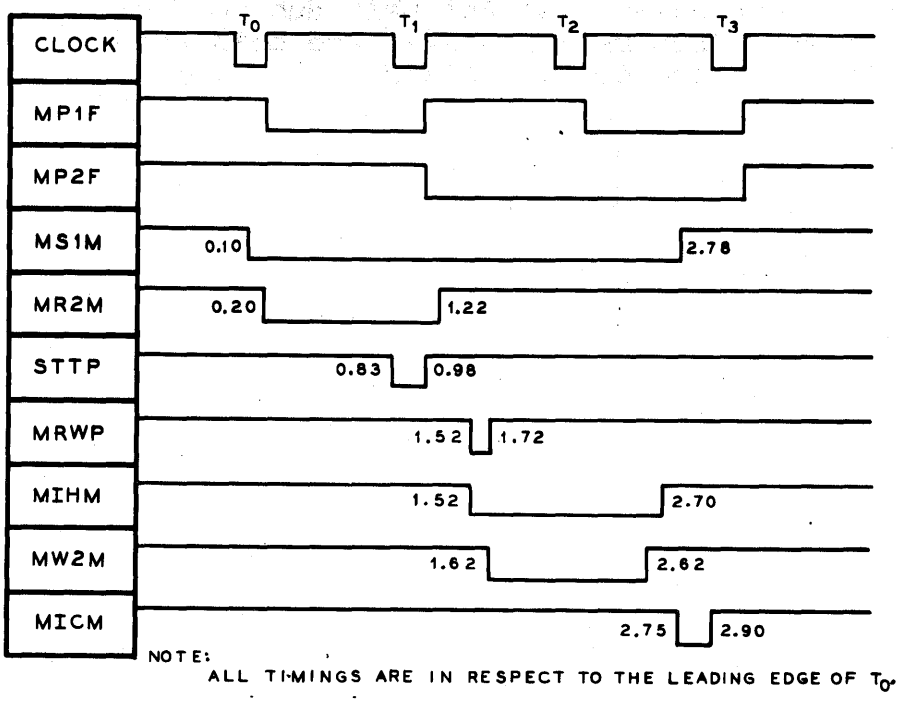


FIGURE 3.4-3
MULTI TIMING DIAGRAM

2. MR2M - This Read Timing Pulse is used as a Control level for the "X" and "Y" lines during the Read phase.

3. STTP - The Strobe Timing Pulse is used to gate the output of the Sense Amplifiers into the Information Register during a Read operation. The Strobe Pulse is also used in a Write operation to gate the Parity Information into MIR-49.

4. MRWP - The Memory Read to Write Pulse is used as a delay between the Read and Write phases.

5. MIHM - The Inhibit Timing Level is used as a Control level for the Inhibit Drivers during the Write phase of a Memory operation.

6. MW2M - This Write Timing Pulse is used as a Control level in the selection of the "X" and "Y" Write Drivers during the Write phase of a Memory operation.

7. MICM - The Memory Information Clear Pulse is used to clear the Memory circuits at the completion of a Memory operation.

The Multi Timing circuits are shown in Figure 3.4-4. The Timing circuits are started when A00S is received from Central Control. This level is used to make up the Memory Start Driver Level (MSTD) and is ANDED with a Clock Pulse (CCP-6) to trigger MS1M. MS1M (Memory Read Switch 1 Multi) is a DSW1 package. This package is a delay-type Multi that when the input goes TRUE, the output will go true 100 nano-seconds later. This Multi would time-out after approximately 2 microseconds if

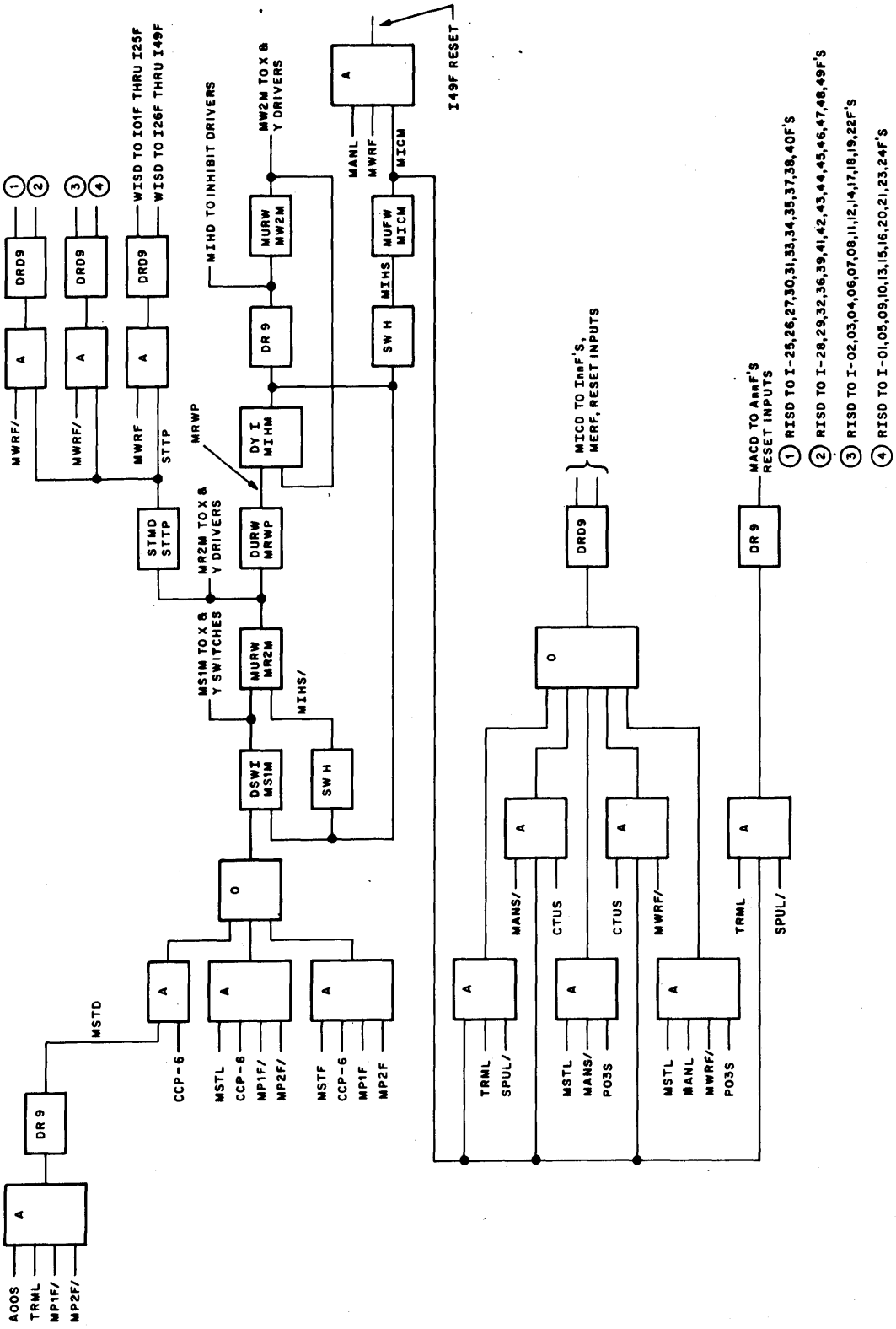


FIGURE 3.4-4
MEMORY TIMING CONTROL

the second input did not go true and hold it on until its normal time-out after 2.68μs. MS1M is used to trigger the next Multi (MR2M), and also as a Control level for the Address switches.

MR2M is a MURW (Read/Write Multi) type package. This package will produce an output pulse 100 nano-seconds after both inputs go true. The duration of the output pulse will be approximately 1μs. The second input to the package is used to prevent MR2M from timing out more than once each Memory cycle. The output of MR2M is used to accomplish the following three operations:

1. Trigger STTP (Strobe Multi, STMD)

2. Trigger MRWP (Read to Write Delay Package, DURW)

3. Enable the appropriate "X" and "Y" Current Drivers for the Read phase of the Memory operation.

The Strobe Multi is used to produce a 150 nano-second pulse that is delayed 630 nano-seconds from the input. The delay is adjustable and used for Maintenance purposes. (See Section 6.6) The output of the Strobe Multi, STTP, is used to gate Information into MIR.

The Memory Read to Write Pulse MRWP, is used to provide a delay between the Read and Write portion of the Memory cycles. The circuit is triggered by the Trailing Edge of MR2M, and the output will go true 300 nano-seconds later. The duration of the output pulse is not critical, but must be greater than 200 nano-seconds. The output is used to trigger the Memory Inhibit Multi (MIHM).

The Memory Inhibit Multi is an Inhibit Delay type package (DYI). The circuit is turned ON when MRWP goes true and the output goes true with very little delay. The input must be held true for the Multi to time-out normally. This is accomplished by MW2M on the second input. The output of the package is used to accomplish the following:

1. To turn ON the appropriate Inhibit Drivers during the Write portion of the Memory cycle.

2. Trigger the Memory Write 2 Multi (MW2M).

3. Retrigger the Memory Read 2 Multi and allow it to time-out normally.

4. Prevent the Memory Read 2 Multi from timimg out again during this cycle.

5. Trigger the Memory Information Clear Multi (MICM).

The Memory Write 2 Multi (MW2M) is an MURW type of package, the same as MR2M. When triggered by MIHD, the output will go true 100 nano-seconds later and remain true for 1μs. The output is used to enable the selected "X" or "Y" Current Drivers for the Write portion of the Memory cycle. The output of MW2M is also used to hold the Inhibit Multi ON.

The Memory Information Clear Multi is a MUFW type of package. This circuit will produce a 150 nano-second output pulse any time the input goes from false to true. The input to the Multi is the switched output of the Inhibit Multi. Therefore, the Memory Information Clear Multi will produce a 150 nano-second output pulse when the Inhibit Multi times out. The output pulse is used as the Timing Pulse to produce the Memory Information Clear and Memory Address Clear Pulses.

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3.5 PARITY

A Memory Module checks the validity of the Information read from the cores by determining whether there is an Odd or Even number of bits set to the "ones" state in MIR. An Odd number of bits indicates that the Information is correct. An Even number indicates the Information is in Error. When an Error is encountered, the MERF (Memory Error Flip-Flop) is Set.

Since there is going to be a check for an Odd bit configuration after the Read operation, the Unit must Write an Odd number of bits into the cores during the Write operation.

The Information transferred to the Memory Module from the Requesting Unit may contain either an Odd or an Even number of bits. This means that the Unit must inspect the Information; determine whether it has an Odd or Even number of bits, and Set an additional bit ON in MIR if the Information has an even bit configuration. This additional bit is called the Parity bit and is contained in MIR-49.

The Odd or Even bit configuration of the Information word is determined by decoding the outputs of the MIR Flip-Flops. Three levels of decoding are used. Refer to Figure 3.5-1.

The first level divides the output from the 48 MIR Flip-Flops in groups of four, and it compares these against each other to produce either an Odd or Even output.

The second level of decoding will take these 12 Odd or Even outputs in groups of four and compare them against each other to produce either an Odd or Even output.

The third level of decoding will take these three outputs and compare them with the output of MIR-49 to produce an output called PERL (Parity Error Level). If the 49 MIR Flip-Flops contain an Even bit configuration, this output will be true. If the bit configuration is Odd, the PERL level will be false.

Figure 3.5-2 shows the logic necessary to decode the first four outputs from MIR. Notice any Odd configuration of these four bits would produce a false level on EAAS and a true level on OAAS. Eleven other identical circuits with different inputs are used to make up the first level decoding.

The second level decoding consists of three circuits to further decode the output of the first level.

The third level consists of one of these circuits and compares the second level outputs with the status of MIR-49.

The PERL output being true during a Write operation is used to Set MIR-49 at Strobe Time to make up the required Odd bit configuration.

If this were a Read operation, MWRF/ would be true and MERF would be Set when the Memory Pulse Counter is equal to two.

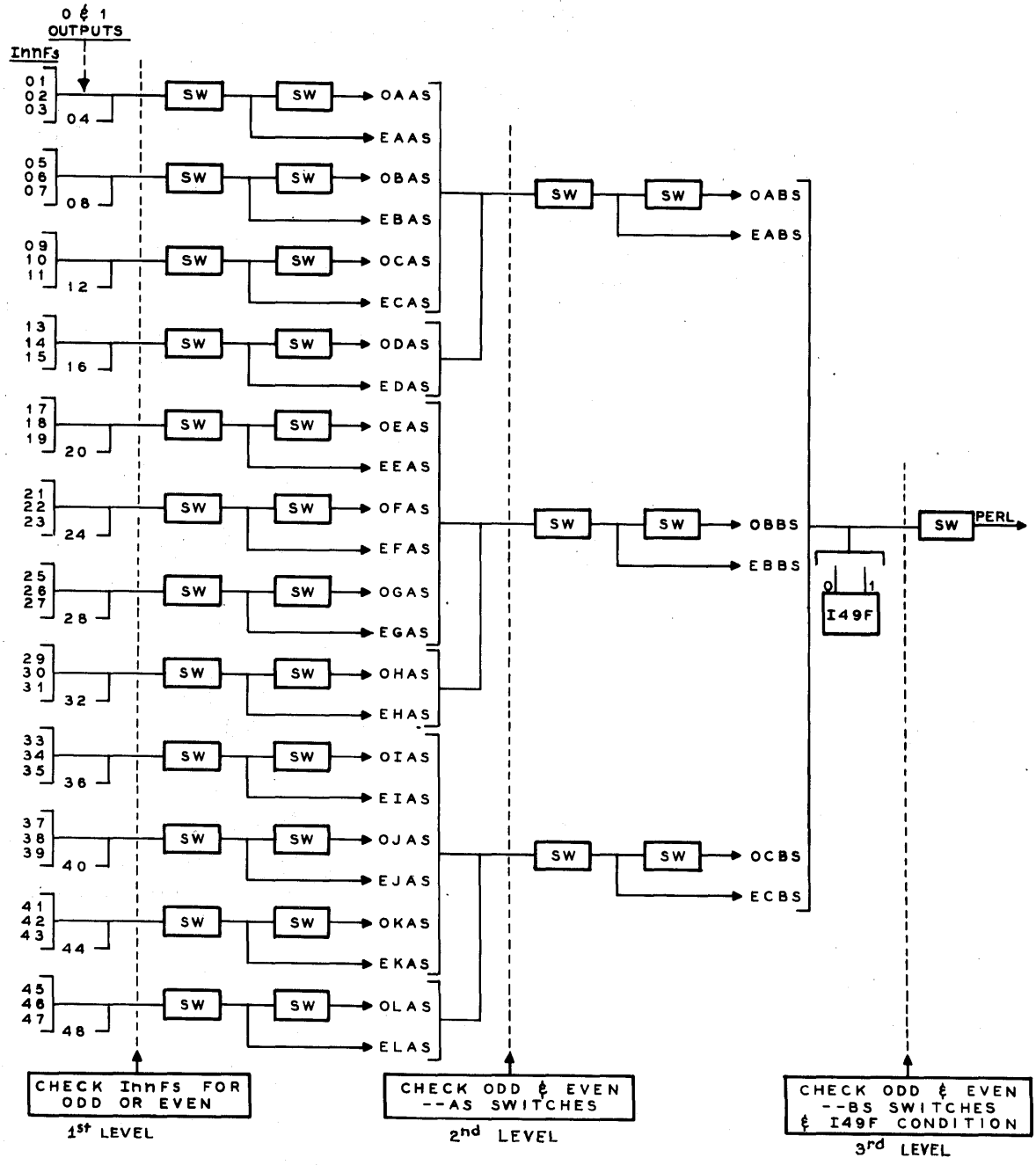


FIGURE 3.5-1
PARITY

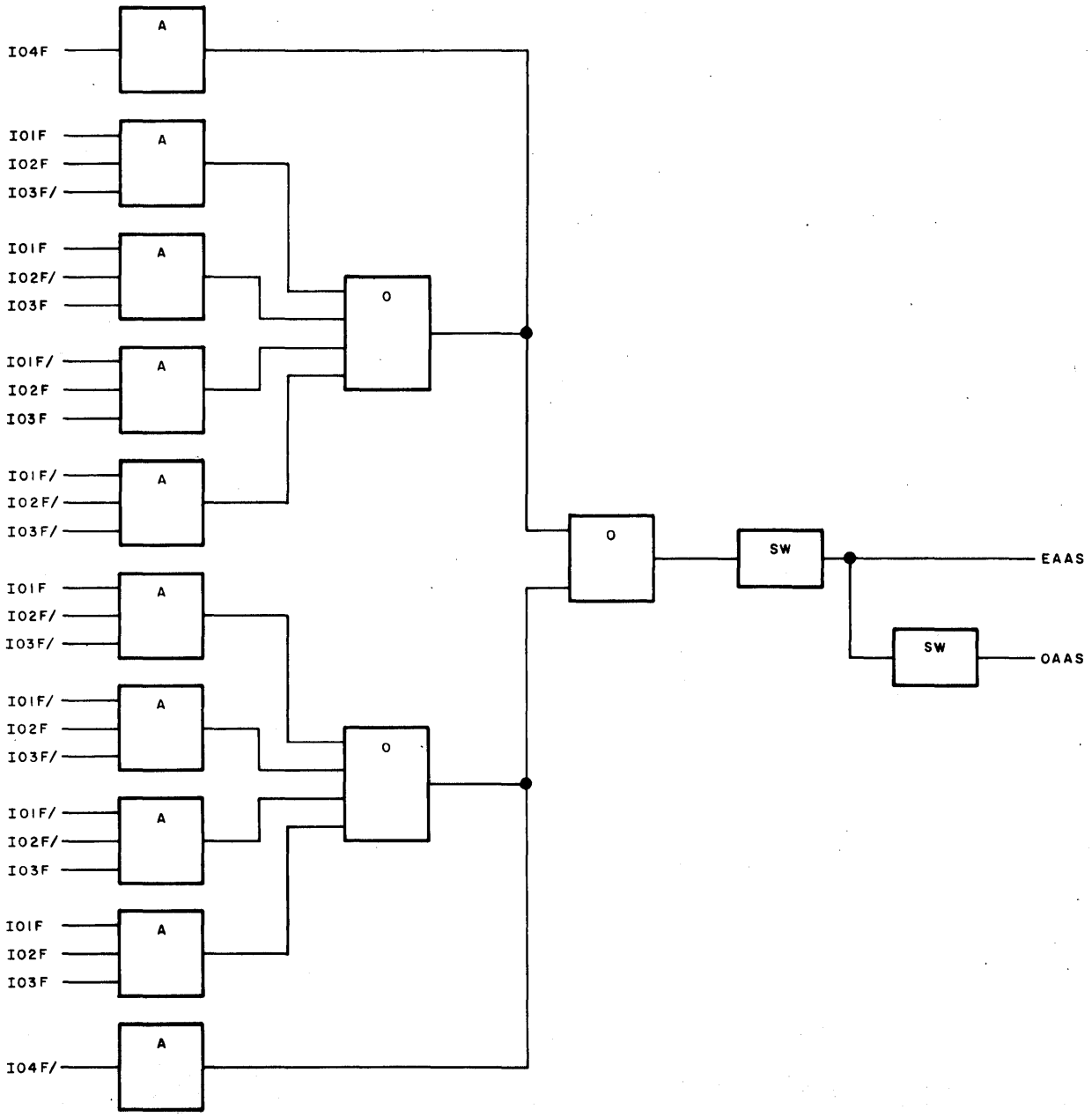


FIGURE 3.5-2
PARITY CIRCUIT

3.6 READ/WRITE CURRENT DRIVER (DRAC)

General

Reference Figure 3.6-1.

There are 32 Current Drivers used in each Memory Module. Sixteen of these are controlled from MAR-1 thru 3 and sixteen from MAR-7 thru 9. The MAR Register is used to select two "X" and two "Y" Current Drivers for each Memory cycle. The Memory Timing circuits will select one "X" and one "Y" for the Read portion of the Memory cycle, and the other "X" and "Y" Current Drivers for the Write portion. Each circuit will supply a constant current of 260ma to the selected "X" or "Y" line.

Circuit Description

Each Flex-o-pac contains two circuits, one for Read and one for Write. The Address (MAR) inputs are common to both circuits. The output of MR2M Multi will be used to turn ON the Read Current Driver and the output of MW2M Multi will turn ON the Write Current Drivers. The Read Current Driver circuit will be connected to the -30V "R" Supply and the Write to -30V "W".

In the quiescent state; Q1, Q2 and Q3 are cut off.

When the inputs to the circuit go true, Q1 will be forward biased and go into conduction. The Positive-Going Signal will be coupled across Transformer T1 (1:1 turns ratio) and forward bias Q2. When Q2 turns on, the -30V through Q2 to the Emitter of Q3 will turn Q3 ON.

The RC network consisting of R6 and C2 is to protect Q3 from overloading due to the 260ma of current through the Address line. On the initial turn on, C2 will short out R6 to allow for fast rise time of the current pulse. Once C2 is charged, R6 will limit the current flow in order to protect Q3 from excessive current. The output pulse will be controlled by MR2M and MW2M Multis (Read and Write respectively). Capacitor C1 is used for filtering.

SEE PAGE 3.6-2 FOR FIGURE 3.6-1.

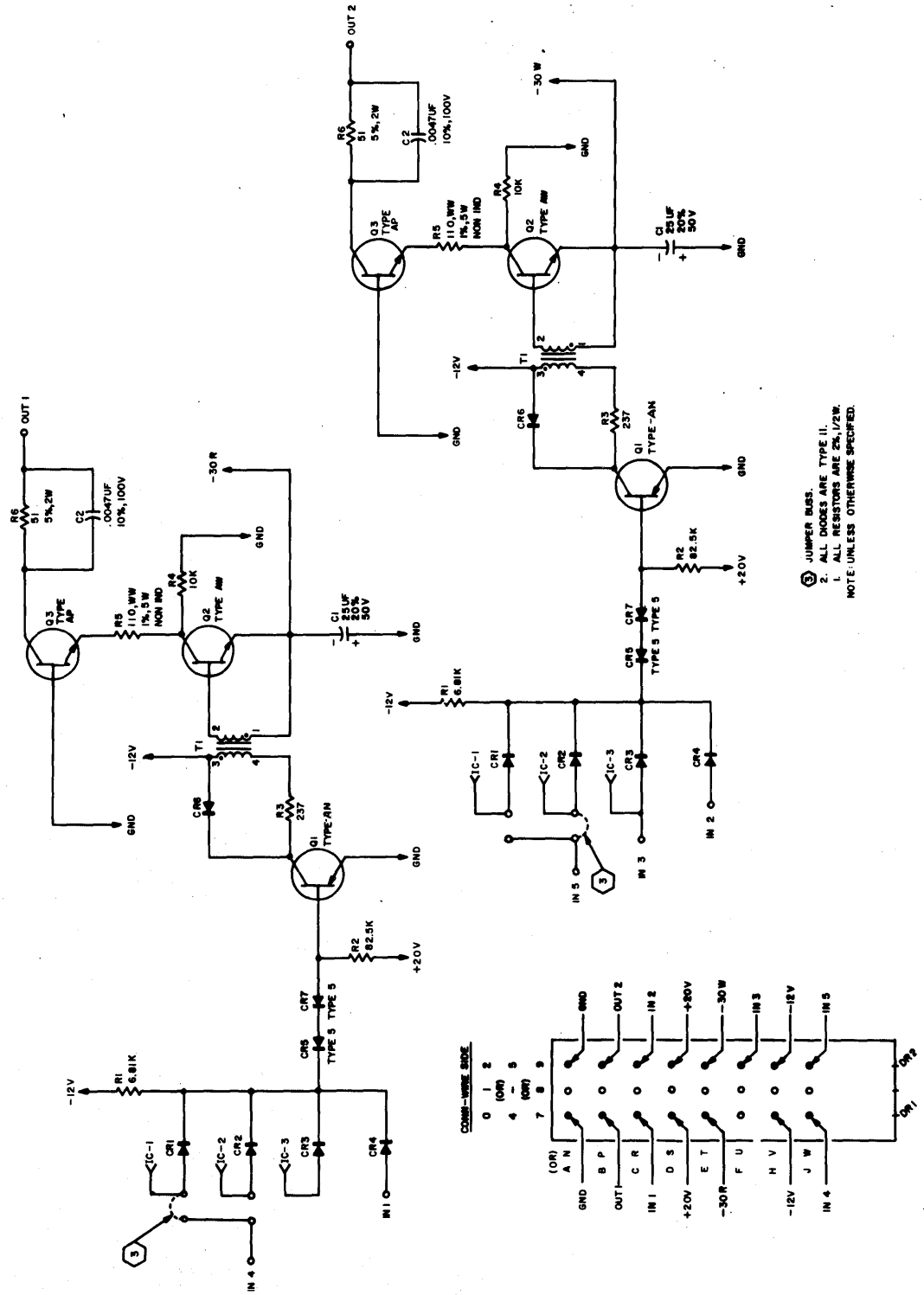


FIGURE 3.6-1
DRAC

3.7 MEMORY ADDRESS SWITCH (SWAD)

General

Reference Figure 3.7-1.

There are sixteen Memory Address Switches contained in each Memory Module. Eight of these are controlled by MAR 4 thru 6, and eight are controlled by MAR 10 thru 12. Those controlled by MAR 4 thru 6 are considered "X" Memory Address Switches, and those controlled by MAR 10 thru 12 are "Y" Memory Address Switches. A more detailed explanation of the Logical Operation of the Memory Address Switches is contained in Section 3.2.

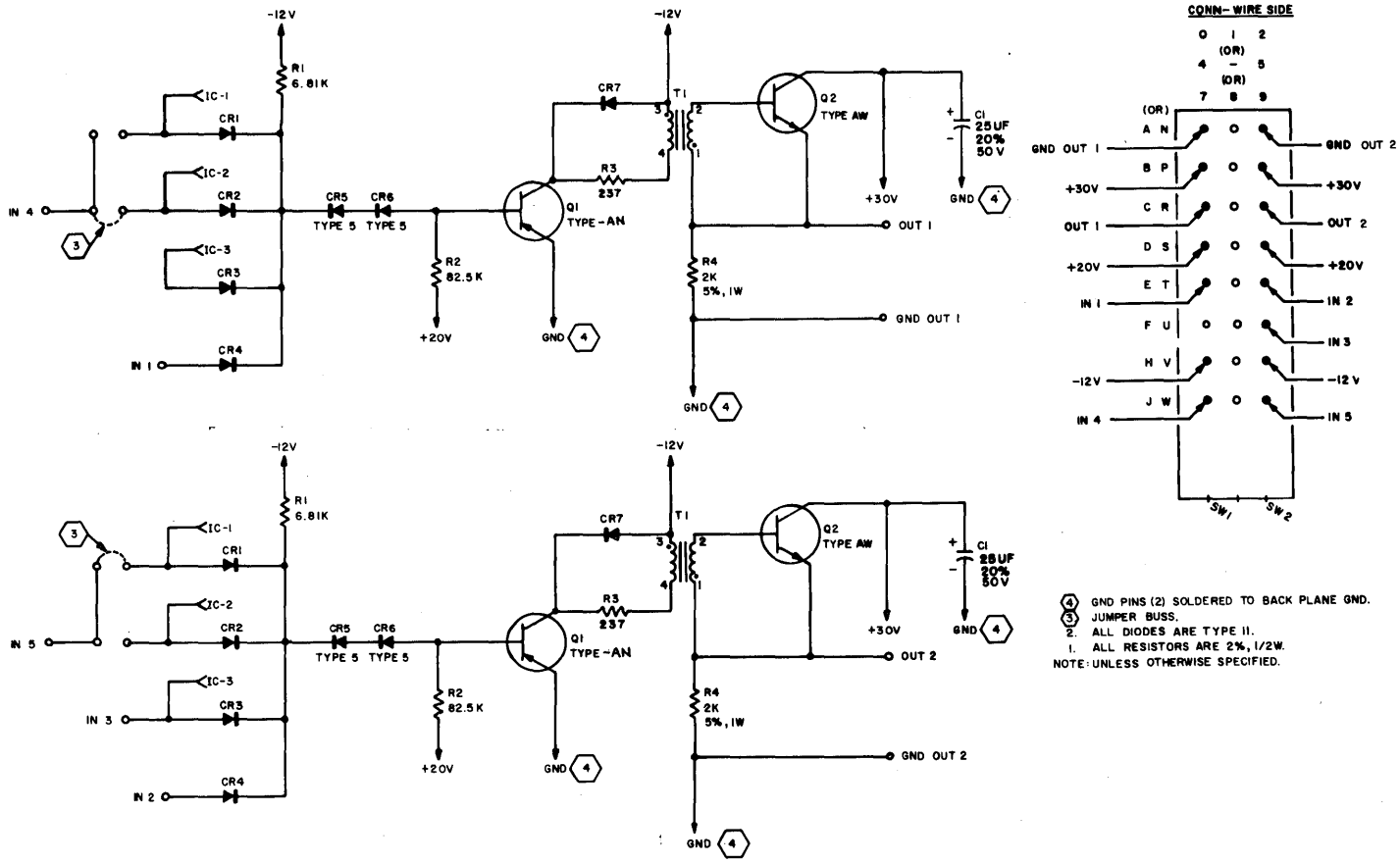


FIGURE 3.7-1
SWAD

Current flow can be in either direction in the "X" and "Y" lines. One direction corresponds to Read, the other to Write. The same Address Switch circuit is used on both Read and Write portions of the Memory cycle. The four inputs make up a four-legged AND gate. Three of these inputs are from the outputs of either the "X" or "Y" tens position of MAR and will decode the Address in the package. The fourth input is the output of MS1M Multi from the Memory Timing circuits.

NOTE

MS1M is ON for both Read and Write portions of the Memory cycle.

Operation

The purpose of the Memory Address Switch circuit is to provide current path to the +30V Supply from the constant current Read and Write Drivers.

When the Memory Address Switch circuit is in the quiescent state, Q1 and Q2 will be cut off. As long as Q2 is cut off, there will be no +30V available for a current path.

When the Input Gating becomes true, Q1 will become forward biased and a Positive-going Pulse will be developed and fed through the Transformer T1 which has a 1:1 turns ratio. The Positive-going Transformer output pulse will saturate Q2, therefore supplying a +30V current path by the Emitter of Q2 (out).

The purpose of R4 is to establish a bias level for the circuit output. The output pulse will be approximately 3 microseconds in duration, which is under control of the MS1M Memory Timing Multi.

Special Components

1. CR7 - clamp diode to keep the type "L" Transistor Q1 from breaking down.
2. C1 - a capacitor used for filtering action.

3.8 INHIBIT CURRENT DRIVER

General

Since each core plane corresponds to one bit of Information, it is necessary to have 49 Inhibit lines. The Inhibit line is a continuous wire that passes through every core in a plane. The Inhibit line is fed by an Inhibit Driver. The line is physically laid out in such a manner that the effect of current flow through the line will oppose the effect of the current flow in the "X" and "Y" lines. The result is that the Memory core that is receiving a +1/2 current from both the "X" and "Y" lines and an Inhibit current of -1/2 will not be set to the "one" state, since the resultant current effect is +1/2 and a +1 is required to set a core. Each Inhibit line has a corresponding Line Driver. The driver is gated by the NOT side of a MIR Flip-Flop and MIHD from the Pulse Timing circuit.

During a Write operation, MIR is LOADED by the Requesting Unit (via Central Control) at the beginning of the Memory cycle. If a MIR Flip-Flop is LOADED with a zero, the zero side (NOT) output will be true. This true is ANDED with MIHD which is true during the Write phase of the operation. The Inhibit Driver will be activated and prevents the writing of a "one" into the core.

The Inhibit Driver Package contains two individual driver circuits called a Flex-o-pac. A Schematic of an Information Driver circuit is shown in Figure 3.8-1.

The following circuit description is in reference to the circuit shown in this figure.

Circuit Description

Quiescent State - When the circuit is in its quiescent state, Transistors Q1 and Q2 are cut off.

Operating State - When the input gating to CR1 and CR2 are true (InnF/ · MIHD), Transistor Q1 will be turned on. A positive-going signal will be developed across T1 (1:1 turns ratio) which will saturate Q2 when the Base becomes more positive than the Emitter. When Q2 saturates, this provides approximately 250ma of drive current to the Inhibit line.

The width of the output pulse is determined by the width of the input pulse. The amplitude of the output-current pulse is approximately 250ma. The exact value of the pulse will be determined by the impedance of the Inhibit line and the Supply voltage from the temperature-compensated -30V "I" Regulator.

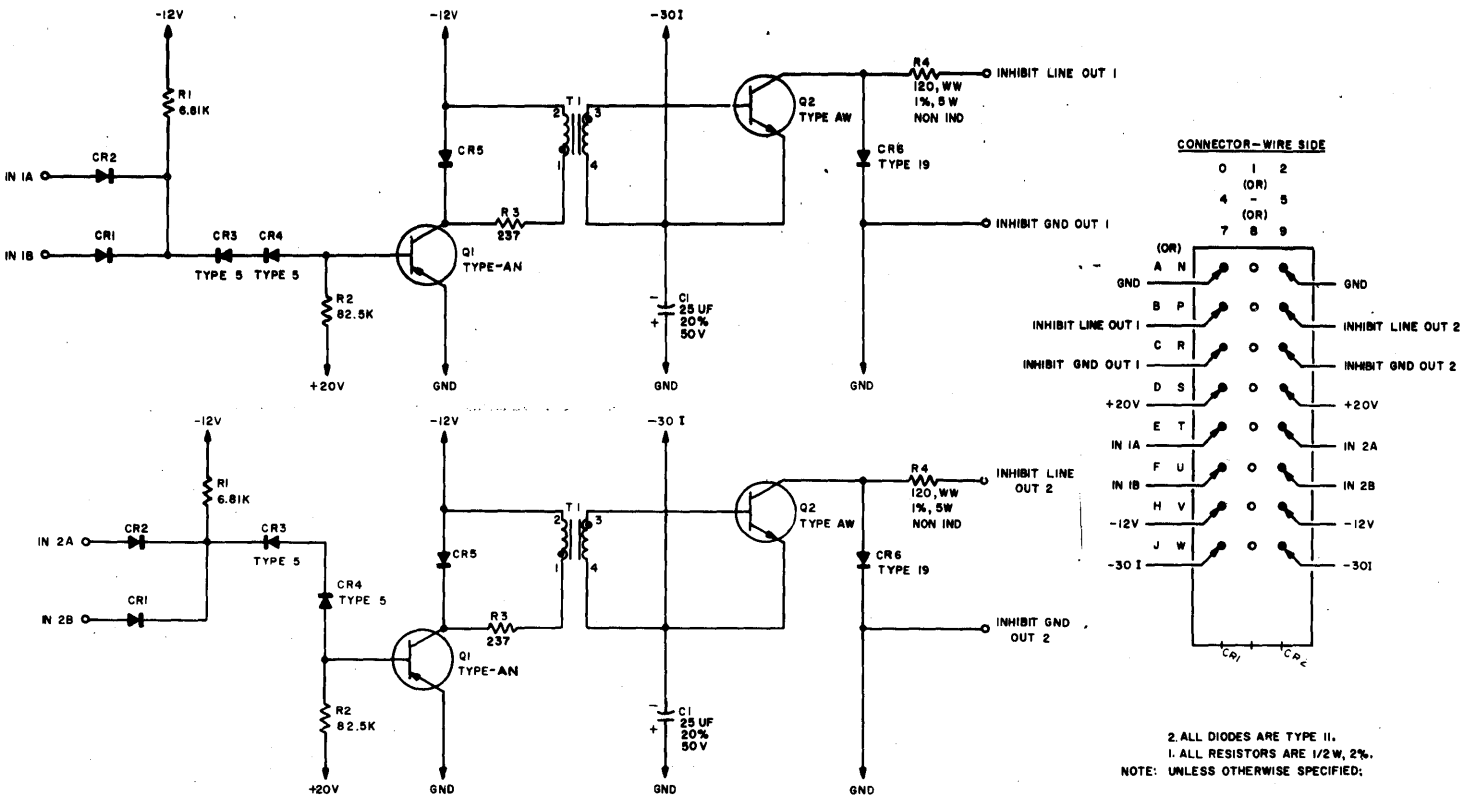


FIGURE 3.8-1
DRIC

Special Components

The characteristic impedance of the Inhibit line is approximately 120 ohms. Due to this impedance, R4 120 ohms has bee used to provide line termination. By putting the Termination Resistor in this position (front end termination), it makes the transmission line appear shorter.

Diode CR6 is used to provide for rapid decay of Inhibit current when the Inhibit Driver is turned off.

Capacitor C1 is used for filtering of the -30V "I" Regulator.

3.9 SENSE AMPLIFIER AMS

General

The Sense Amplifier is a high gain differential amplifier. It is used to amplify the small signals from a core into a voltage usable in Logic Circuitry. This circuit also has a high degree of common mode noise rejection.

Circuit Description

Refer to Figure 3.9-1.

The Input Transformer primary is connected to the Sense line of a core plane. When a core changes state, a signal from the Sense lines will be developed in the primary circuit of the Transformer. The signal is coupled through the Transformer to the bases of the Transistors Q1 and Q2 where it is amplified. A negative signal from either Q1 or Q2 will be coupled through the OR type circuit made up of CR1 and CR2 to the base of Q3. This negative on the base of Q3 will turn Q3 ON, and apply a near ground potential on the base of Q4. Q4 will turn OFF and the output will go to -4.5V.

The Input Transformer has a 1 to 5 ratio. The primary center tap is grounded through R1 to prevent ringing. The secondary center tap is connected to -6T to provide a Threshold level for Transistors Q1 and Q2. Transistors Q1 and Q2 are operated class A.

The high resistance of R7 and R8 in the Emitter circuits functions to minimize any circuit unbalance that could be caused by Q1 and Q2 having slightly different characteristics. The AC signals in R7 and R8 are out of phase, and R6 and C2 provide an AC pass or feedback to stabilize the gain of the circuit.

Common Mode Noise Rejection

Common mode noise enters on both Input lines and is in-phase. There is very little current flow in the Transformer primary, but the noise is capacitively coupled to the secondary. This noise signal causes an in-phase voltage change on the bases of Q1 and Q2. If this signal is negative, the change on the collectors of Q1 and Q2 will be positive.

A positive signal on the cathodes of CR1 and CR2 will increase the back bias and the signal will not be coupled through to Q3. A positive noise signal will cause Q1 and Q2 to increase conduction. The low impedance path from the Emitter of Q1 to the Emitter of Q2, thru R6 and C2, will not be effective now because both Emitters are changing in the same direction. The gain of Q1 and Q2 will be very small due to the degenerative feedback across R7 and R8. Diode CR7 increases the false level (more negative) output of the Sense Amplifier, which reduces the noise on the output lines.

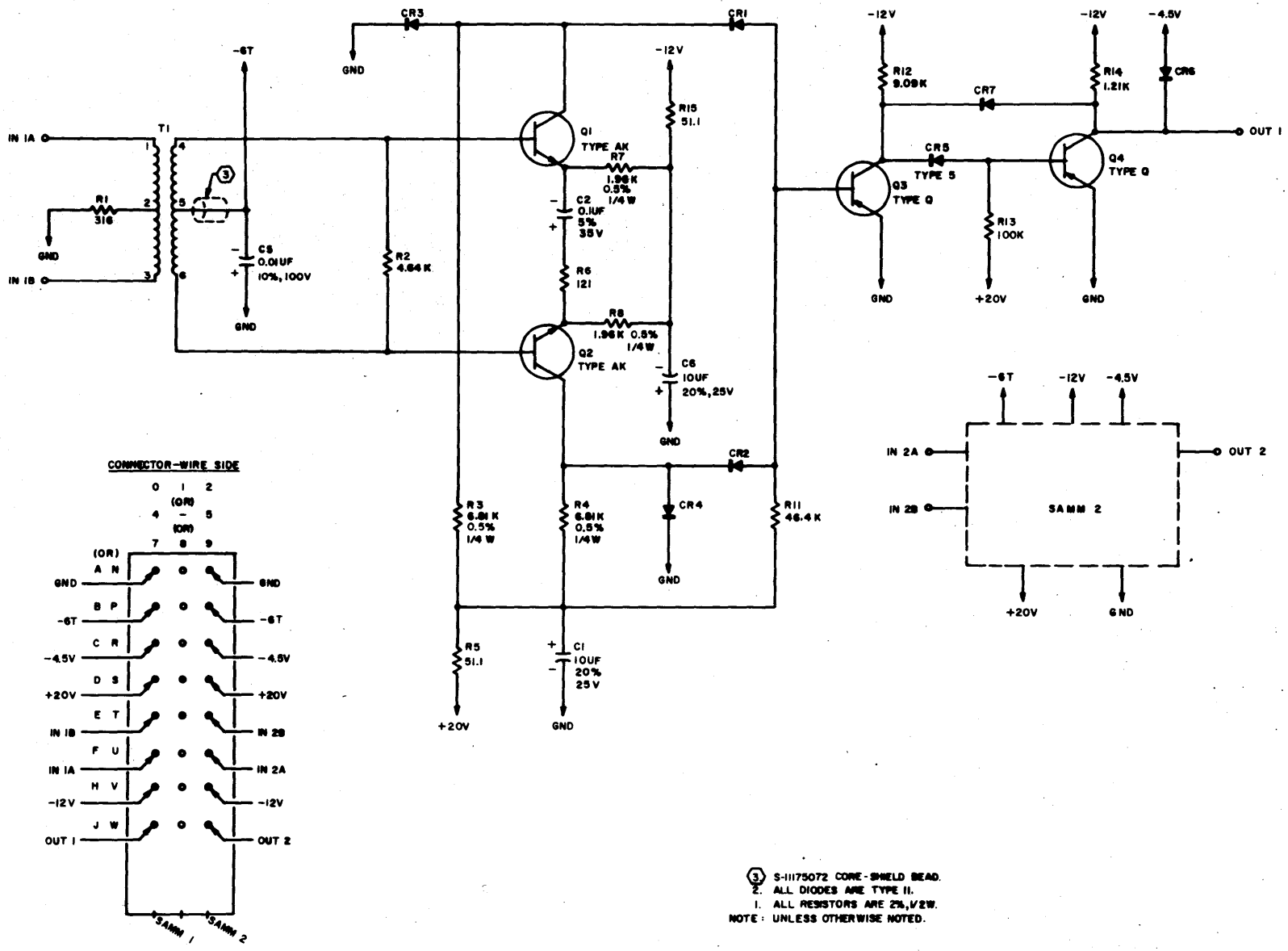


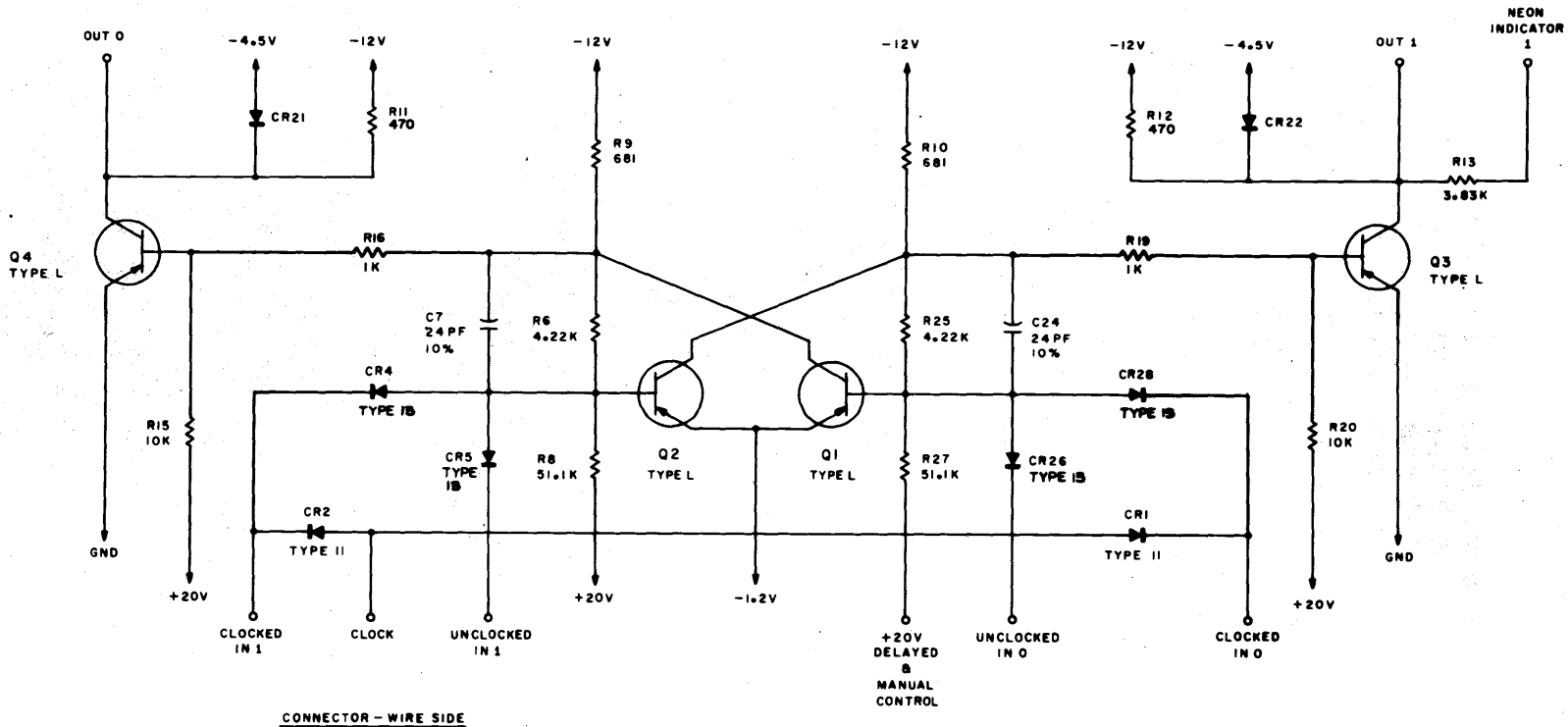
FIGURE 3.9-1
SENSE AMP (AMS)

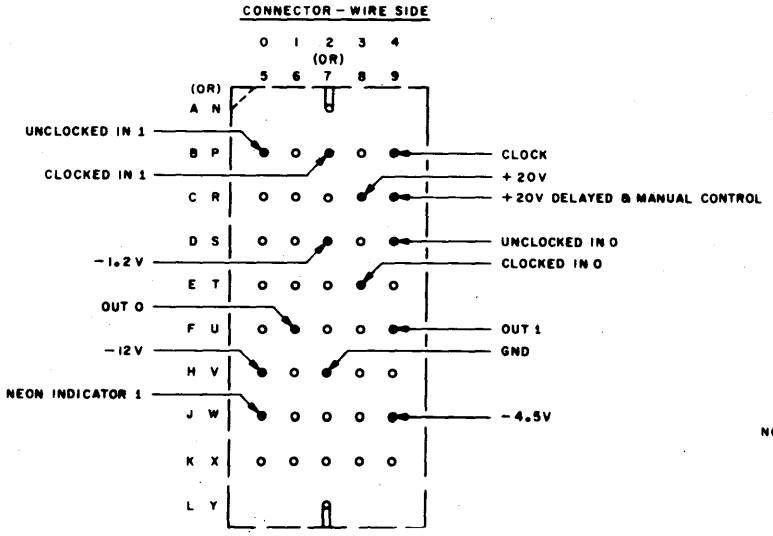
3. S-1117S072 CORE-SHIELD BEAD.
2. ALL DIODES ARE TYPE II.
1. ALL RESISTORS ARE 2%, 1/2W.
NOTE: UNLESS OTHERWISE NOTED.

3.10 NO DELAY FLIP-FLOP (FFN7)

The FFN7 circuit is used in the 49 Memory Information Register Flip-Flop, and the 12 Memory Address Register Flip-Flops. The purpose of this flip-flop circuit is to allow the outputs to change states approximately 80 nanoseconds after the input goes true.

The circuit is shown in Figure 3.10-1. The FFN7 is identical to a 20-70 Flip-Flop with the Delay lines and complimenting diodes removed. Since the operation is so similar, it will not be explained in this manual.





2. ALL DIODES ARE TYPE 6.
1. ALL RESISTORS ARE 1/2W, 2%.
NOTE: UNLESS OTHERWISE SPECIFIED.

FIGURE 3.10-1
FEN7

3.11 READ SWITCH 1 MULTI - DSW1 (MS1M)

General

The purpose of the Read Switch 1 Multi is to provide a timing level that will turn ON the appropriate "X" and "Y" Memory Address Switches.

The Read Switch 1 Multi will receive an input pulse from the logic that is used to start a Memory operation in either a LOCAL or REMOTE condition. From this logical level, a true level will be developed which is somewhat delayed (40 to 100 milliseconds). The output of the Read Switch 1 Multi will stay true throughout the READ and WRITE portion of the Memory cycle, but it must cease immediately after the WRITE portion. To accomplish this, a two-input Multi is used. The first input will turn on the Multi and hold it ON until the second input comes true. The second input will hold the output true until both inputs are false. See Figure 3.11-1.

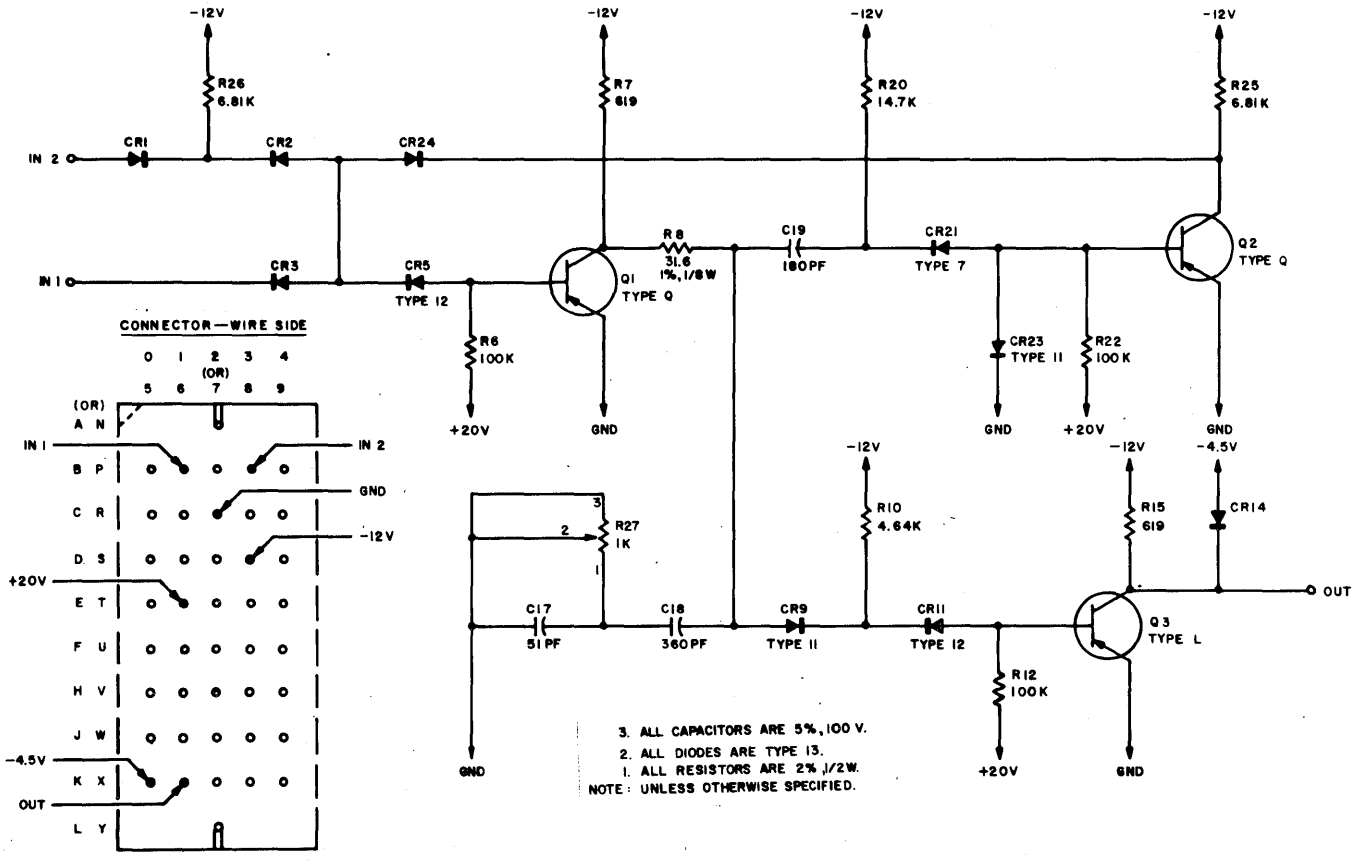


FIGURE 3.11-1
DSW1

Circuit Description

In quiescence, Q1 is cut off, and Q2 and Q3 are ON. When a true pulse is received at Input 1, Q1 turns on bringing its Collector close to

ground. This will discharge capacitors C18 and C19 through R8 and Transistor Q1.

As capacitor C19 discharges, transistor Q2 will turn off. When Q2 turns off, feedback current is applied to the Base of Q1 by Resistor R25 through CR24 and CR5.

When C18 reaches approximately -1.5V, Q3 will turn off causing a true output. Q3 will now remain off as long as Q1 is saturated.

If no input pulse is received at Input 2, Q2 will turn on as soon as C19 charges up through R20. Q2 turned ON would cut off Q1. For proper operation, an input level must be received at Input 2 before Q2 turns on. Q1 will then remain saturated until Inputs 1 and 2 are both false.

When Q1 turns off, C18 and C19 charge through R7 and R8 toward -12V. When C18 and C19 reach approximately -2V, Q3 will turn on, ending the output pulse.

Special Components

R27 is adjustable and determines where the output pulse will be in the Memory cycle. The duration of the output pulse is determined by the input and the length of time Q2 is turned off.

3.12 INHIBIT DELAY - DY I (MIHM)

The purpose of the Inhibit Delay package (DY I) is to turn on the appropriate Inhibit Drivers at the start of the WRITE portion of a Memory cycle and to hold them on past the turn off of the WRITE current.

Operation

Refer to Figure 3.12-1.

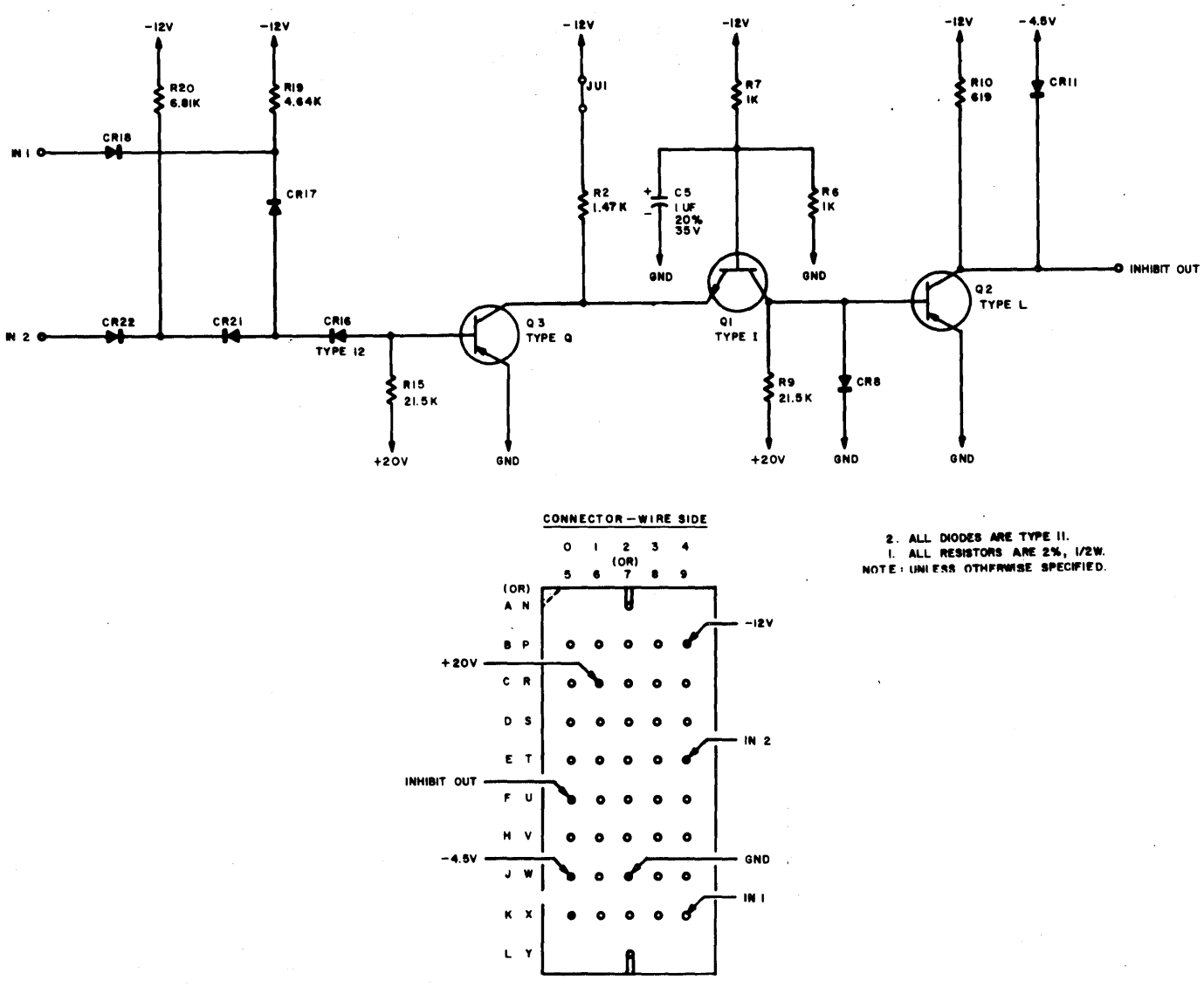


FIGURE 3.12-1
DY I

In the quiescent state, with both inputs false, transistor Q3 is off and Q1 and Q2 are both on. With transistor Q2 on, the output will be false. The circuit is turned on by MRWP going true on Input 1. With

a true on Input 1, transistor Q3 will turn on and discharge capacitor C4. With C4 discharged, Q1 will turn off and the Base of Q2 will go positive. This will turn Q2 off, causing the output to go true.

Due to the fast discharge path of C4 through Q3, there will be no delay on the turn on of the circuit. Once the output goes true, MW2M will turn on and its output will be used to hold Input 2 true. The output of the Inhibit Multi will remain true as long as either input is true.

When MW2M times out and both inputs are false, Q3 will turn off. This will allow C4 to start charging toward -12V through R2 and R27. When C4 has charged to approximately -6V, Q1 will turn on applying a negative on the Base of Q2. With a negative on its Base, Q2 will conduct and the output will go false. The charge path of C4 through R2 and R27 will determine the time the output remains true after both inputs go false.

3.13 READ/WRITE DELAY - DURW (MRWP)

General

The READ/WRITE Delay package is used in the Memory Timing circuits to provide the delay between the READ and WRITE portions of the Memory cycle.

The input to the Delay circuit is the output of MR2M. The delay is triggered on the Trailing Edge of the input pulse and the output pulse will go true approximately 280ns later. The duration of the output pulse is approximately 360ns and is completely independent of the input.

Circuit Description

Refer to Figure 3.13-1.

In the quiescent state, transistor Q1 is cut off and Q2, Q3 and Q4 are conducting. When the input goes true, transistor Q1 will turn on and capacitor C3 will be discharged. Transistor Q1 coming on will cause Q2 to turn off. When Q2 turns off, the Base of Q4 will go positive turning this transistor off. Q4 turning off will charge C17 and apply a negative-going signal to the Base of Q3. The Base of Q3 going negative will have no effect on the output since Q3 is already in conduction.

When the output goes false, transistor Q1 will turn off and capacitor C3 will start to charge through R4 and R27.

Once C13 has charged to approximately -7V, Q2 will turn on. Q2 being on will furnish Base drive to transistor Q4 turning it on. When Q4 turns on, capacitor C17 will start to discharge, removing Base drive to Q3. With Q3 off, the output will be true and remain true for the discharge time of C17 through R16.

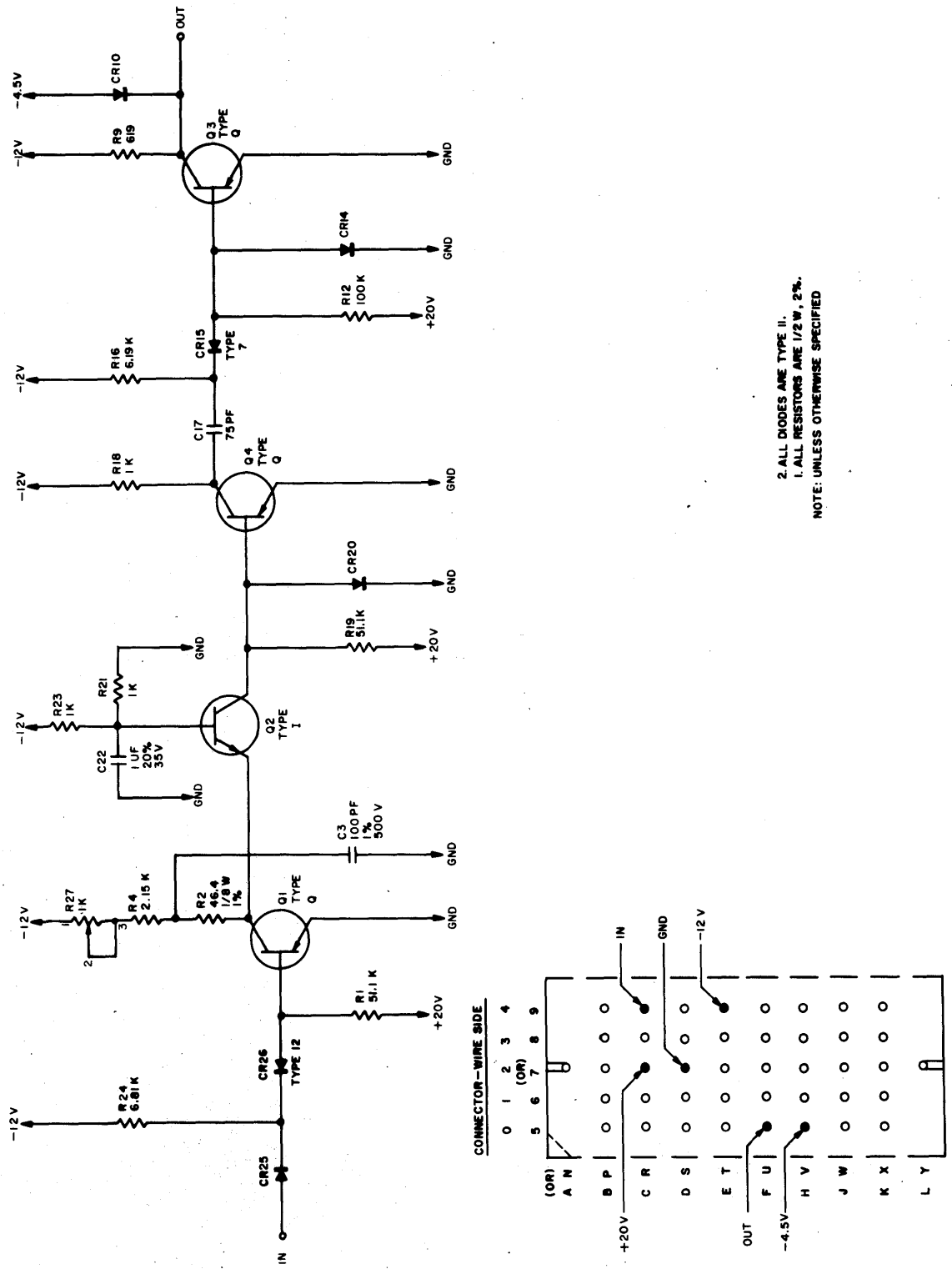


FIGURE 3.13-1
DURW

3.14 STROBE MULTI STMD

General

The purpose of the Strobe Multi is to develop a Timing Pulse output which is used to Strobe the outputs of the Sense Amplifiers into the Information Register during a Read operation, or, Strobe the incoming Information into the Information Register during a Write operation.

Circuit Description

In the quiescent state, Transistor Q1 is off, and Transistors Q2 and Q3 are on. The Inhibit input is not used. The input to CR23 is from Memory Read 2 Multi. With a true input to CR23, Transistor Q1 will turn on and discharge C3. This will apply a positive-going level on the Base of Q2 turning it off.

Transistor Q2 being cut off, will have no effect on Q3, and the output remains false. When Capacitor C3 has charged through R4 and R27, Transistor Q2 will turn on and discharge Capacitors C13 and C15. This will apply a positive-going signal to the Base of Q3, turning it off. Q3 will remain cut off until C13 has charged through R17 and R18.

The duration of the output pulse is determined by the RC time of capacitor C13 and Resistors R18 and R19. The delay of the output pulse from the Leading Edge of the input is determined by Capacitor C3 and Resistors R4 and R27. Capacitor C15 is used to speed up the switching time of Transistor Q3.

SEE PAGE 3.14-2 for FIGURE 3.14-1.

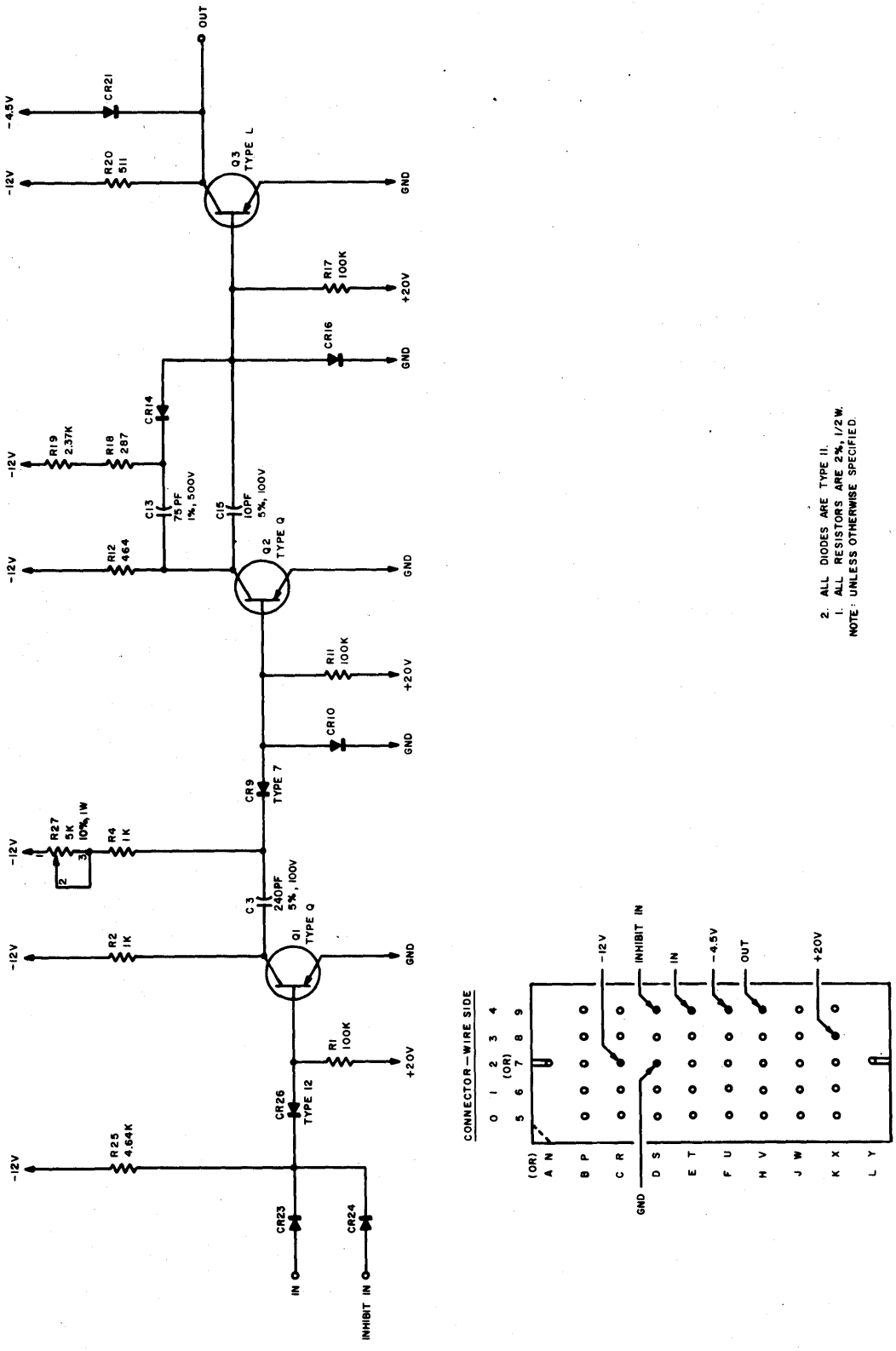


FIGURE 3.14-1
STMD

3.15 READ/WRITE MULTI MURW (MR2M & MW2M)

General

Refer to Figure 3.15-1.

The purpose of the Read/Write Multi is to develop the Timing Pulses used to enable the Read and Write Current Drivers. Two packages are used, one for the Read Timing Pulse, MR2M; the other for the Write Timing Pulse, MW2M.

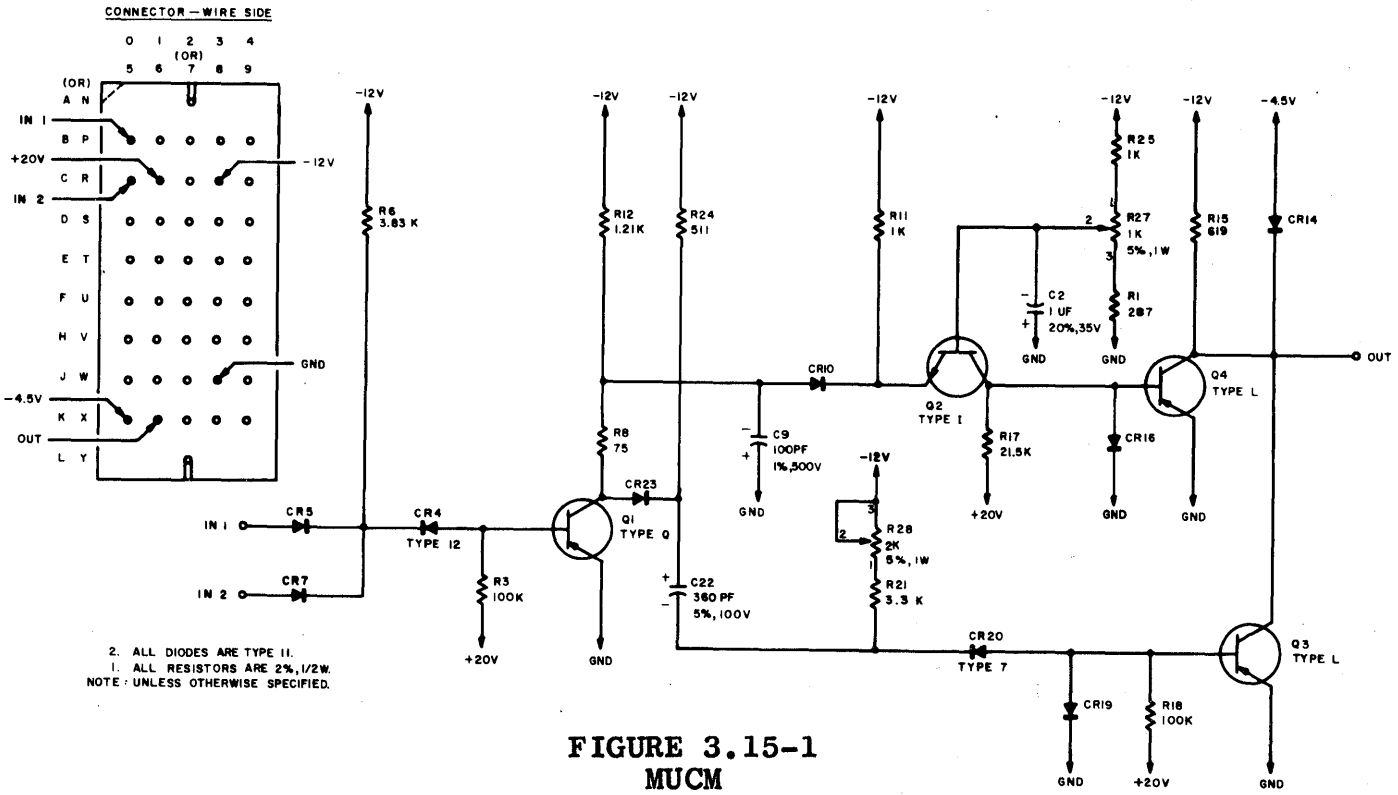


FIGURE 3.15-1
MUCM

Circuit Description

The input consists of a two input AND gate, the second input is only used on the Read Multi to insure the Multi is only triggered once each Memory cycle. In the quiescent state, Transistor Q1 is cut off and Transistors Q2, Q3 and Q4 are conducting. Transistors Q3 and Q4 make up a transistorized AND circuit where both transistors must be cut off before the output will be true.

If both the inputs are true, Q1 will start conducting. This will allow Capacitor C22 to start charging through R21 and R28 and cut Transistor Q3 off. Transistor Q3 will remain off for the charge time of C22. Also, when Q1 starts conducting, Capacitor C9 will start to discharge through R8 and Q1. At a point in the discharge curve of C9, determined by the voltage divider in the Base circuit of Q2, Q2 will be cut off and in turn cut off Q4. With both Q4 and Q3 cut off, the

output will be true. The output will remain true as long as both transistors remain off. Transistor Q4 will remain off as long as the input stays true. The length of time Q3 remains off, is determined by R28 in the charge path of C22. This resistor is adjusted to give the output pulse duration of approximately 1.2μs. The Leading Edge of the output pulse is delayed approximately 1.0 nano-seconds from the input. This is determined by R27 in the Base circuit of Q2.

3.16 MULTI F W MUFW

General

Refer to Figure 3.16-1.

The MUFW Multi is a 150 nano-second Multi that will provide an output pulse each time the input goes from false to true. The package is used in the Memory Timing circuits to provide a clear pulse at the end of each Memory cycle. The MUFW is also used to generate the 150 nano-second output pulses from the Memory Clock oscillator in the Clock Control circuits.

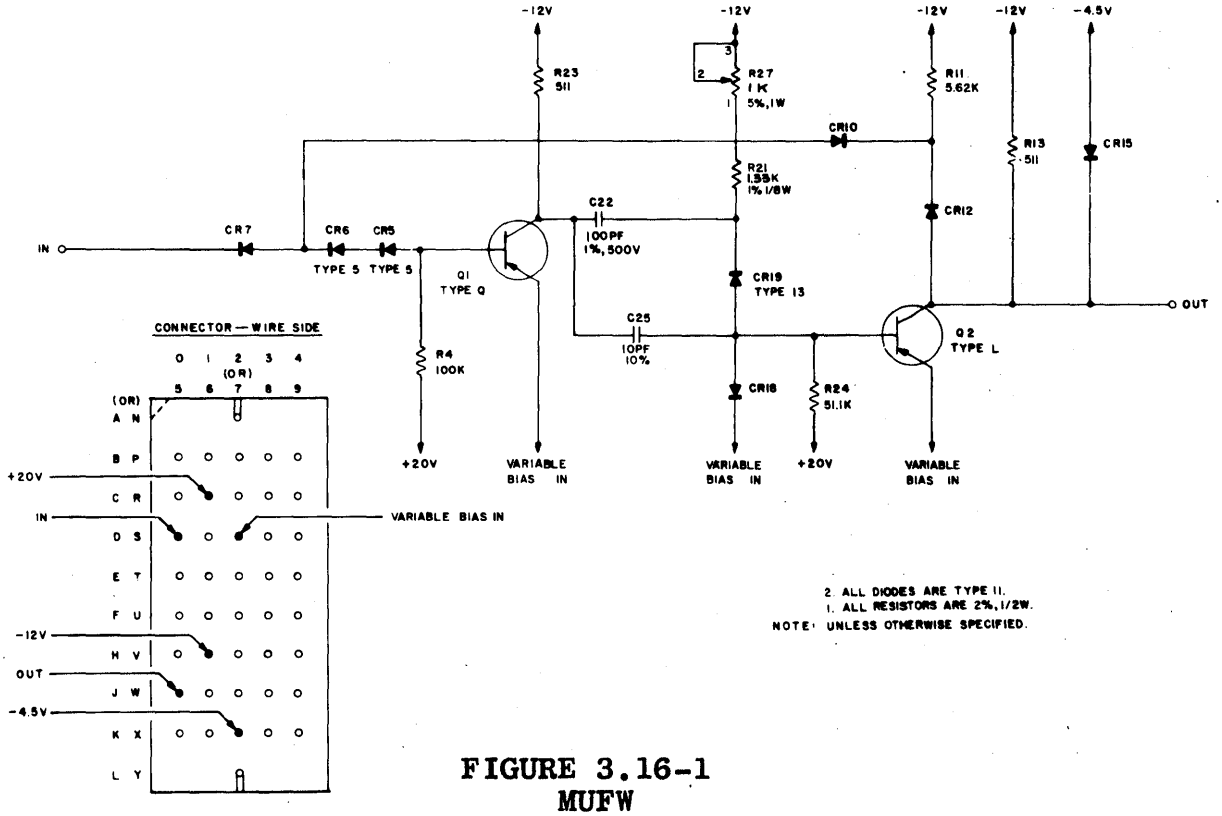


FIGURE 3.16-1
MUFW

Circuit Description

Normally the input is standing by at a true level. Base drive is furnished to Q1 through CR5, CR6 and CR7, causing it to conduct. Q2 will also be in conduction due to the Base drive furnished to it through CR19, R21, and R27 to -12V. With Q2 conducting, the output will be false.

When the input goes false, the positive on the Base of Q1 will cause it to cut off. Q1 cutting off, will have no effect on Q2 since Q2 is already conducting and capacitors C22 and C25 will charge to -12V. When the input goes from false to true, Q1 will again start conducting. With Q1 conducting, Q2 will be cut off and the output will go true. The duration of the output pulse is determined by R27, R21, C22 and C25. Diode CR10 will hold the input true for the duration of the output pulse.

3.17 POWER CONTROL

General

All of the Power used in the B461 Memory Unit is supplied by the B5370 Power Supply Unit. This Power Supply Unit supplies a total of ten voltages that are regulated to 5 percent. Some of these voltages are used directly with no further regulation. They are the +100V, -100V, -120V, +50V, +20V, and -38V.

The -19V Regulator is in the Memory Sub-System Unit and furnishes regulated voltages of -12V, -4.5V, and -1.2V for the Logic circuitry. This Regulator supplies enough regulated voltage for a maximum unit of four Memory Modules. Each Memory Module has a set of Regulators to supply the necessary Memory voltages which are the -30V Read, Write, Inhibit, and the +30V. There are two special Supplies which are the -15V and the -6T. These will be explained later in this manual.

All Power is controlled in the B5500, including the DC ON and OFF. When Power is turned ON, all of the B5500 Supplies except the +20V and +100V, come ON. After a 500ms Delay, +20V is turned ON. The +20V Supply turns ON the EDD Logic Regulators (-12V, -4.5V, -1.2V), which in turn enables the +100V switch. The +100V Supply allows the B461 Memory Regulators to come ON. When Power is turned OFF, a reverse sequence is followed with the Memory Regulators going down first, followed by +20V, the EDD Power Pack, +100V, and the Raw Supplies.

Over-voltage and under-voltage for -12V, -4.5V, and -1.2V is sensed in the B5500. In the event of a failure, the Power is entirely turned OFF, including AC to the Raw Supplies. Over-voltage and under-voltage for the B461 Memory Regulators is sensed in the Memory Unit. In the event of a failure in one of these Regulators, they are all turned OFF, including the EDD Power Pack. However, the Raw Supplies are left ON, except for the +20V and +100V.

"On-Line" Sequencing (REMOTE Operation)

When the Memory Unit is operated "On-Line", the initial sequencing of Power will be controlled by the B5370 Power Supply Unit. All System Supplies will be sequenced including the LOCAL Regulators in each Memory Cabinet or Sub-System.

As the last voltage controlled by the System (+100V) comes ON, each individual Memory Unit will Sense this and sequence its own special Supplies. The order of sequencing will be as listed below.

On Sequence

1. B5370 Power Supply
   a. Group 1 = +50VDC, +19VDC, -100VDC, -120VDC, -38VDC
   b. Group 2 = +20VDC

c. Group 3 = -12VDC, -4.5VDC, -1.2VDC

d. Group 4 = +100VDC

2. Memory Unit

a. Group 5 = -30V Read, Write, Inhibit

b. Group 6 = +30V

Off Sequence (Power Failure or DC Lockout)

1. Group 6 = +30V
2. Group 5 = -30V Read, Write, Inhibit
3. Group 2 = +20VDC
4. Group 3
Group 4 = +100VDC, -12VDC. -4.5VDC, -1.2VDC

System Power cannot be turned OFF from a Memory Unit, except in case a Power Failure is detected in the Unit. Group 1 Power Supplies do not turn OFF under DC failure conditions.

Local Sequencing

When the Memory is "Off-Line", Power may be sequenced independently of System Power Control once System Power is ON. This is accomplished by means of relays contained in the Memory Unit.

On Sequence

1. Group 1 = +20VDC, -24VDC
2. Group 2 = -12VDC, -4.5VDC, -1.2VDC, +19VDC, +50VDC, -38VDC
3. Group 3 = +100VDC, -100VDC, -120VDC
4. Group 4 = -30V Read, Write, Inhibit
5. Group 6 = +30V

Off Sequence

1. Group 6 = +30V
2. Group 5 = -30V Read, Write, Inhibit
3. Group 3 = +100VDC, -100VDC, -120VDC
4. Group 2 = -12VDC, -4.5VDC, -1.2VDC, +19VDC, +50VDC, -38VDC
5. Group 1 = +20VDC, -24VDC

Relay Power Control

Relays K1, K2 and K3 are used in control of bringing up Power in the Memory Unit in either REMOTE or LOCAL operation. By LOCAL, it is meant that once System Power is UP, Power can be brought UP or DOWN on any specific Memory Module without having to sequence System Power up or down. Switch S-1 must be in the DC ON position when bringing Unit Power UP from either a LOCAL or REMOTE condition.

Refer to Figure 3.17-1.

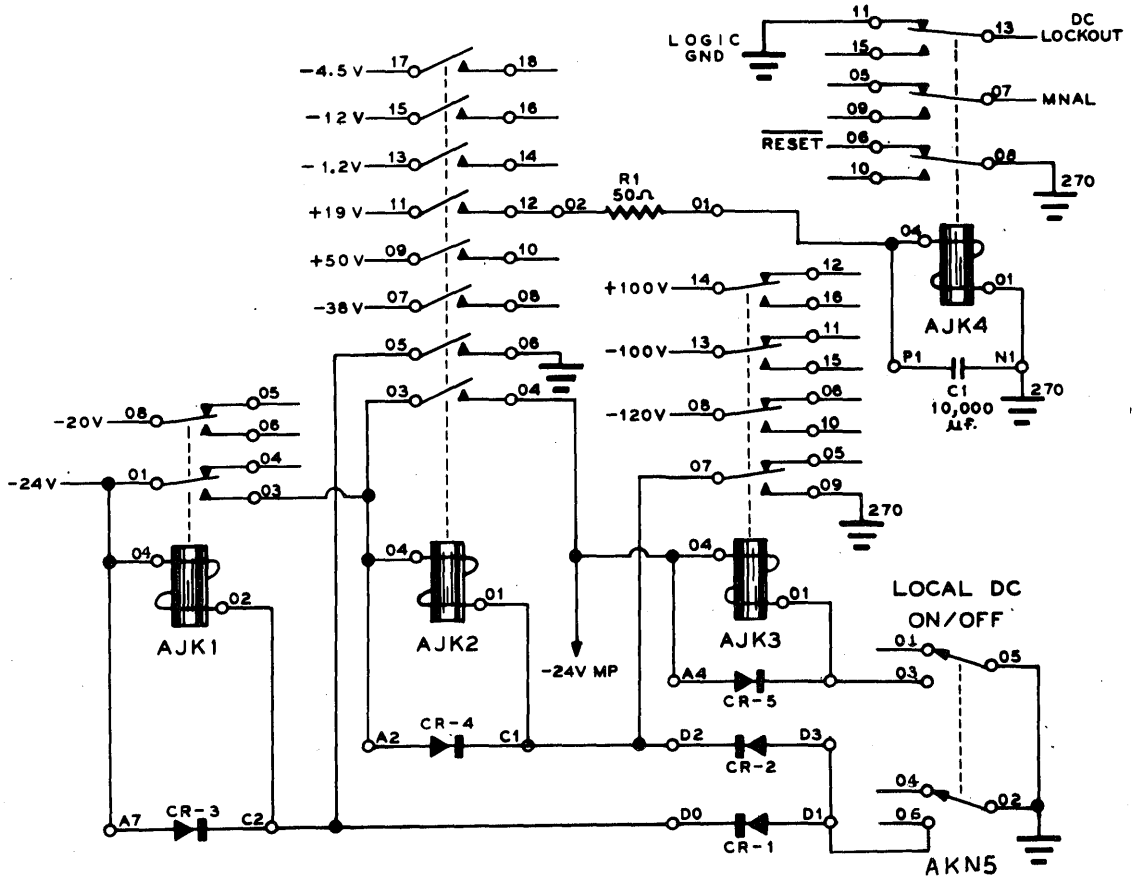


FIGURE 3.17-1
RELAY POWER CONTROL

-24V is available from the B5370 Power Supply which will pick K1 thru CR1 and S-1 to Ground. When K1 picks, this will allow -24V to pick K2 through diode CR-2 and S-1 to Ground. When K2 picks, this allows K3 to pick through S-1 to Ground.

The purpose of Relays K1, K2 and K3 picking in this sequence, is to allow the proper application of the Power Supply and Local Regulator voltages to the Memory Module. K1 supplies +20V; K2 supplies +50V, +19V and -38V (Main Power Supply), -12V, -4.5V and -1.2V (EDD Regulator). K3 supplies +100V, -100V and -120V.

NOTE

K1 is also held by contacts 03 and 04 of K2, and K2 is held by contacts 05 and 07 of K3. This arrangement is used to provide the correct drop sequence of these relays.

When S-1 is in the DC OFF position, the relays will drop in the sequence of K3, K2 and K1. This is due to the holding circuit arrangement explained in the note above.

Relay K4 is picked when +19V from the contacts of K2 become available, delayed 150ms by the RC network consisting of R1 and C1. The reason for the delay of 150ms is to allow enough time for the SWHV circuits to settle down before the over and under voltage indicating circuits become active.

NOTE

SWHV circuits use +19V and -24V.

If this was not accomplished, it would be possible to have a premature Failure indication while the Power Sequencing and the SWHV circuits are settling down. Other purposes of K4 will be explained later in this section.

Logical Power Control

The Regulators of each Memory Module cannot be sequenced UP until the last voltage (+100V) from the B5370 Power Supply has sequenced UP. The Regulators will sequence DOWN any time the +100V is removed.

DC LOCKOUT also controls the sequencing of the Regulators. This level will be true prior to the +100V switch coming ON if the Memory Module is in REMOTE and an over or under voltage has not been detected previously in this Module. Refer to Figure 3.17-2.

With DC Lockout true, and the +100V becomes available from the B5370 Power Supply, the Memory Power ON sequencing can begin. The +100V is divided down between two 10K resistors and fed to the input of the Voltage Sensing Switch (SWVS). The +100UV/ output of this Sensing circuit will be true when +100V is available. This true is then used to trigger the TØDM Multi. The other inputs to this Multi are DC ON/ and DC LOCKOUT which will both be true on initial Power UP.

The output of TØDM is shunt added with +100V UV/ and used to set the DC ON cross-coupled switch. Once this cross-coupled switch has been set, it will remain ON until either the +100V is turned OFF, or DC LOCKOUT goes false.

When TØDM went true, the -30V ON CONTROL went false. This level going false is used to turn on the -30V Regulators. It should be noted,

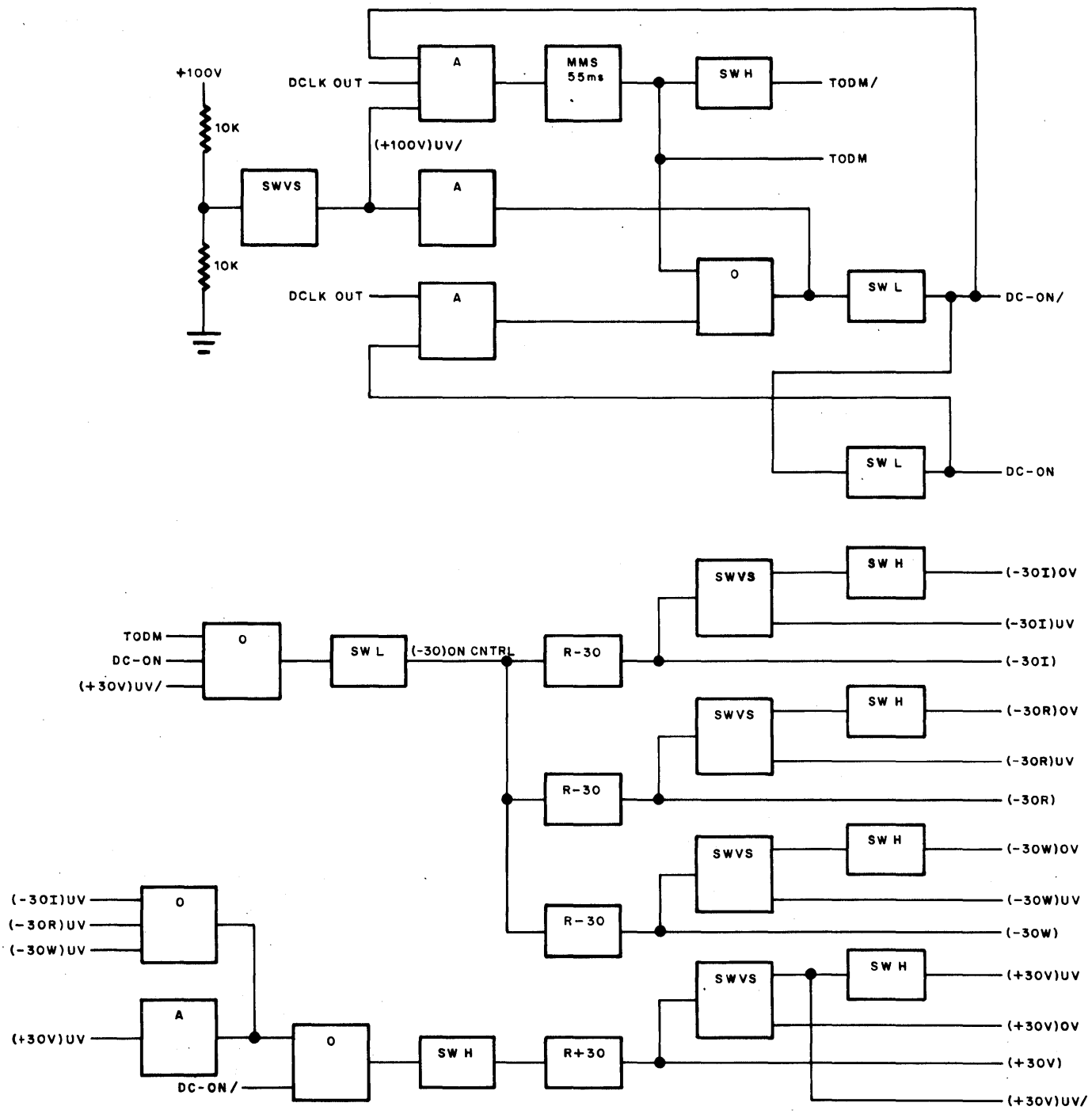


FIGURE 3.17-2
POWER ON CONTROL

when TØDM times out after 30ms, the DC ON level will hold these Regulators ON. The (+30V) UV/ level is used on the Power Down sequence to insure the +30V Regulator goes down before the -30V Regulators.

In order to turn on the +30V Regulator, a true is needed on the Regulator input. This is accomplished by the (-30I) UV, (-30R) UV, and

(-30W) UV all going false when the -30V Regulator outputs have come up. The (+30V) UV input is true when the Regulator is down. The purpose of this input is to shut down the Regulator if a +30V Under Voltage is detected. The DC ON/ input is used for normal Down sequencing of the Regulator. When the +30V Regulator is up, the Power sequencing is complete.

The TØDM Multi output is switched to make up the TØDM/ level. This level is used in the Over and Under Voltage detection circuits to prevent detection of these conditions until Power is completely sequenced up.

The Down sequence of the Regulators is opposite of that of the Up Sequence. Whenever the +100V switch in the B5370 is turned off, the DC ON cross-coupled switch will be Reset. With DC ON/ true, the +30V Regulator will turn off. When the +30V goes off, the (+30V) UV/ level will go false, turning off the -30V Regulators.

The outputs of the Regulators are sent to Voltage Sensing switches. The Under Voltage switch output from the -30V Regulators will go false when the output of the Regulator reaches 70 percent of its nominal values. The switched output from the Over Voltage circuit will be false unless the output increases to approximately 30 percent over the nominal voltage. For the circuit description of the voltage Sensing switch, refer to Section 3.23.

Power Sense

The Power Sense circuits are used to detect either an Over or Under Voltage in any of the four Regulators. (Three -30V Regulators and one +30V Regulator). An excessive current detecting circuit is contained in each of the Regulator packages. This circuit will cause the Regulator output to shut down if an excessive current is detected. With the Regulator output down, an Under Voltage will be detected to sequence down the other Regulators in the Module, and also send a false level to D & D on the DC LOCKOUT line. The false level on the DC LOCKOUT line will cause all the EDD Regulators in the System to Sequence Down.

The Under Voltage Sensing circuit is shown in Figure 3.17-3. This circuit consists of a cross-coupled switch that may be Set once the Power has been sequenced up (DC ON). The Turn On Delay Multi (TØDM) and the Under Voltage output of one of the Voltage Sensing packages goes true. With the cross-coupled switch Set, the IND-UV output will be false and the Under Voltage Indicator will light. The UN-IND output of the cross-coupled switch is sent to the DC LOCKOUT circuit which will be explained in this section.

Once the Under Voltage cross-coupled switch has been Set, it will remain Set until the Reset pushbutton is depressed, or, the LOCAL DC POWER switch is turned off.

NOTE

Depressing the Reset pushbutton will disable all the Voltage Sensing in the Module for as long as the button is depressed.

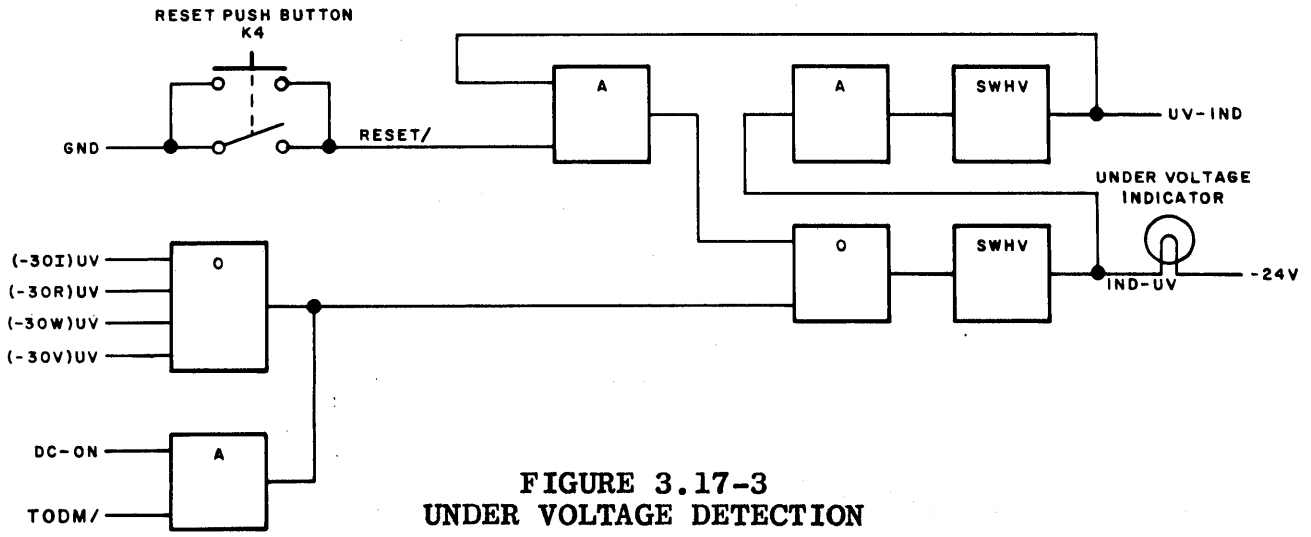


FIGURE 3.17-3
UNDER VOLTAGE DETECTION

The Over Voltage circuit shown in Figure 3.17-4, is identical to the Under Voltage circuit. The cross-coupled switch is Set from the Over Voltage output of the Voltage Sensing packages.

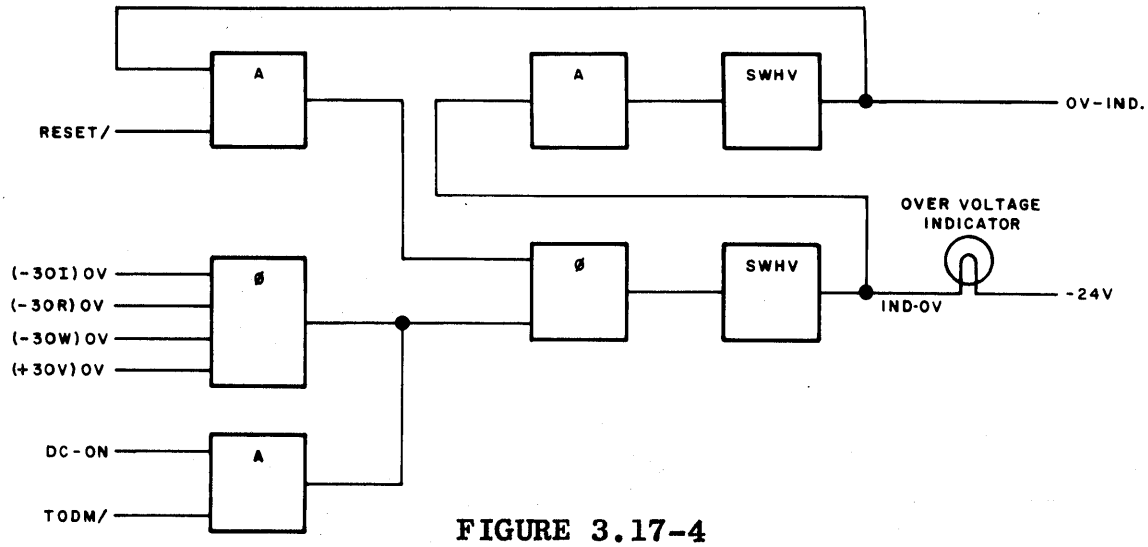


FIGURE 3.17-4
OVER VOLTAGE DETECTION

The detecting circuits for the -30V Read, Write, and Inhibit Regulators are identical cross-coupled switches. A typical circuit is shown in Figure 3.17-5.

The inputs to the cross-coupled switch are the Over and Under Voltage outputs from the associated Voltage Sensing package. The +30V detect-

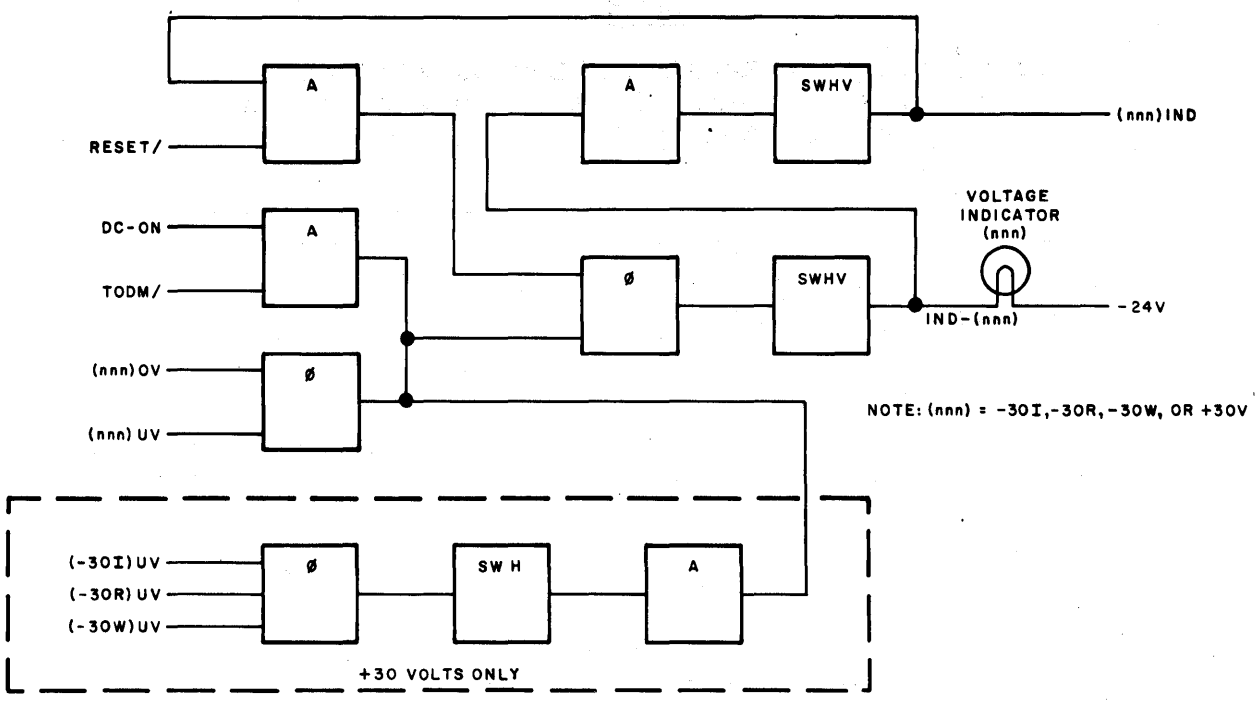


FIGURE 3.17-5
VOLTAGE INDICATOR CIRCUIT

ing circuit is also similar except for an addition of a SHUNT AND gate to prevent false +30V indication when a -30V Under Voltage is detected.

The DC LOCKOUT circuit is shown in Figure 3.17-6.

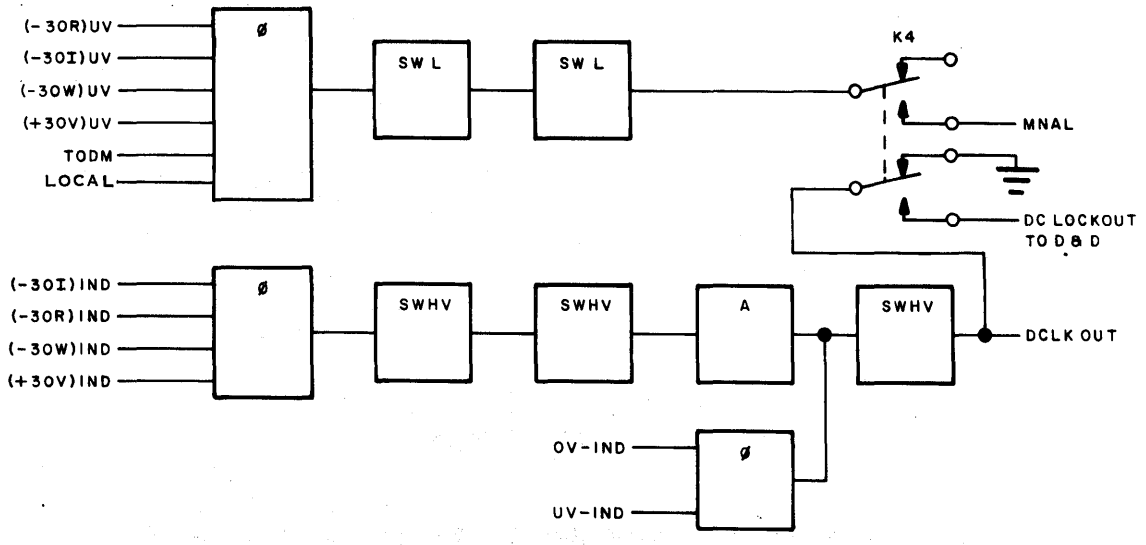


FIGURE 3.17-6
DC LOCKOUT & MEMORY NOT AVAILABLE CIRCUITS

The output of this circuit is normally true to allow Power to be sequenced up. When an Over or Under Voltage occurs, both the cross-

coupled switch associated with the voltage and, either the Over or Under Voltage cross-coupled switch must be Set before the DC LOCKOUT level will go false. The DC LOCKOUT level being False, will cause the System Regulators to sequence down and also prevent the Power On sequence of the Regulators in this Module until the voltage detection circuits have been Reset.

The Memory Not Available circuit also shown in Figure 3.17-6, will be true until the Regulators have completely sequenced up and the Turn On Delay Multi times out (TØDM goes false).

With the Regulators turned ON, all the Under Voltage outputs from the Voltage Sensing packages will be false. When TØDM goes false, the MNAL level will be false. MNAL is sent to Central Control to indicate to the System that the Memory Module is available for System use.

3.18 -15V REGULATOR

General

Reference Figure 3.18-1.

The -15V Regulator is a temperature compensated Regulator which is used to control the three -30V Regulators. This Regulator is controlled by a Thermistor which is mounted near the Core Stack. If the ambient temperature increases, the cores will set and reset with a lower current. To counteract this, the Thermistor is connected to the -15V Regulator in a manner that will cause the -15V Regulator output to go less negative.

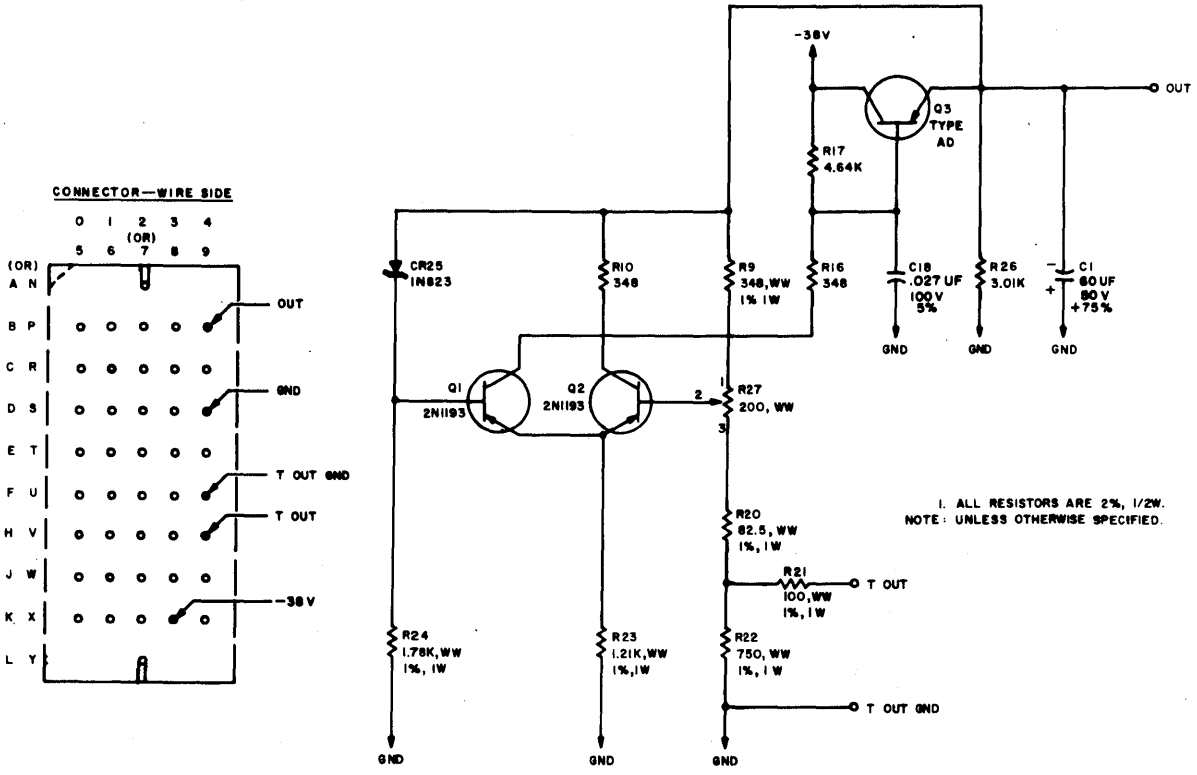


FIGURE 3.18-1
-15V REGULATOR

The -15V Regulator in turn, is connected to the three -30V Regulators in such a manner as to cause the -30V Regulator outputs to go less negative. With the -30V Regulators at a less negative level, less current will be used to set and reset the Memory cores. If the ambient temperature decreases, the opposite will occur. The resistance of the Thermistor will increase, the output of the -15V Regulator will go more negative, and the outputs of the -30V Regulators will go more negative.

Circuit Description

The -15V Regulator contains a Series Regulating Transistor (Q3) and a Differential Amplifier (Q1 and Q2). Transistor Q1 will be in conduction due to the bias potential established by Zener diode CR25 and R24. Q2 will also conduct due to the bias established by R9, R27, R22, and the Thermistor in parallel with R22. With Transistors Q1 and Q2 conducting, Transistor Q3 will conduct at a point established by the conduction of Q2.

The Differential Amplifier circuit controls the regulation and sets the operating point of the Regulator. An increase of ambient temperature will cause the Base of Q2 to go less negative. With the Base less negative, Q2 will conduct less, thus causing the Emitter of Q1 to go less negative.

With the increased bias on Q1, it will conduct harder, causing the Base of Q3 to go less negative. Q3 will conduct less and the output voltage will decrease (less negative). With this increase in temperature, a new operating point has been established for the Regulator. If a decrease in temperature were to occur, the operating point of the Regulator would change in the opposite direction.

3.19 -30V READ/WRITE REGULATOR (250ma)

Reference Figure 3.19-1.

This Regulator is one of two duplicate Regulators. These Regulators supply the Read and Write drive currents to the Core Stack. The input is -38V from the B5370 Power Supply. The output is -30V regulated to better than 1 percent.

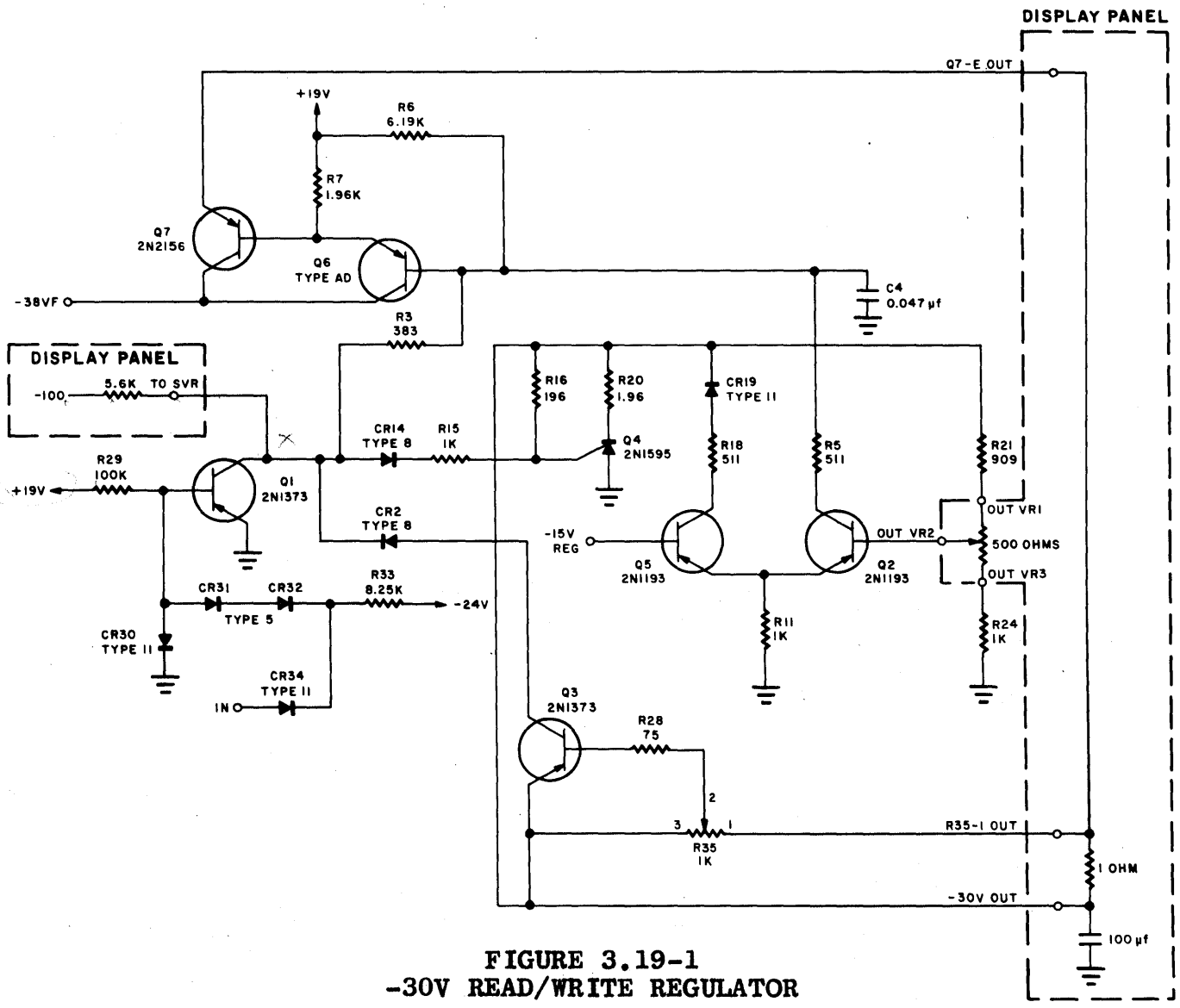


FIGURE 3.19-1
-30V READ/WRITE REGULATOR

Each Regulator contains a Series Regulating Transistor (Q7), a Driver (Q6) for Q7, a Differential Amplifier (Q2 and Q5), the Sequencing ON/OFF Transistor (Q1), and an Over Current Sensing Transistor (Q3).

The Differential Amplifier circuit controls the regulation and sets the operating point of the Regulator. Any variations in the output

will be coupled through CR19 to the Collector of Q5. Any variations felt on the Collector of Q5 will produce varying voltage drops across R11 which consequently controls the current flow of Q2. Any variation is amplified in Q2 and sent to the Base of Q6 through R5. The variation is also amplified in Q6 and direct-coupled from the Q6 Emitter to the Base of Q7.

Q7 will increase or decrease conduction, depending upon whether the original output variations were increasing or decreasing. If the output tried to decrease (go more positive), Q7 would decrease its resistance in order to supply more current to the load and bring the output voltage up to normal.

The Base voltage of Q2 is set by a 500 ohm Variable Resistor located on the Maintenance Panel. This voltage determines the operating point of the Regulator and is usually set so that the output voltage is -30V.

If a sudden load was imposed on the output of the Regulator and the voltage tried to go to -29V, the following would take place.

A fraction of the positive change would appear on the Base of Q2; the amount would depend upon the ration of the resistance in R21, the 500 ohm Variable Resistor, and R24.

The purpose of CR19 is to insure that either change will appear across R18 and on the Collector of Q5. When the Base of Q2 goes positive, Q2 will conduct less. The positive on the Collector of Q5 will cause it to conduct more, causing a lower negative to positive drop across R11 which causes Q2 to conduct even less.

The net effect will be a more positive Base bias on Q2 causing it to conduct less. The Q2 Collector current path is through R5, R3 and a 5.6K Resistor to -100V. When this current decreases, the voltage at the Base of Q6 will go more negative. Q6 is an Emitter Follower, and the Emitter is direct-coupled to the Base of Q7. When the Base of Q7 goes more negative, Q7 will conduct more, thus supplying more current to the load, which will cause the output voltage to return to normal.

The Regulator has a large amount of amplification so the actual output variation will be very small. Capacitor C4 is an anti-oscillation phase shifting capacitor. C4 changes the phase of the feed-back voltage enough that the Regulator does not oscillate.

The -15V feeding the Base of Q5 is a special Regulator that is temperature compensated.

NOTE

The internal functions of this Regulator were explained in Section 3.18.

The -15V Supply is controlled by a Thermistor which is mounted near the Core Stack. If the ambient temperature increases, the cores will set and reset at a lower current. To counteract this, the Thermistor is connected to the -15V Regulator in a manner that will lower the -30V output voltages when the temperature increases.

The Thermistor as used in this circuit, has a negative temperature coefficient. When the temperature increases, the Thermistor resistance will decrease. This in turn will cause the -15V Regulator to put a more positive voltage on the Base of Q5. Q5 will draw less current which in turn causes Q2 to conduct harder. The increased conduction through Q2 will cause the Base voltage of Q6 to go more positive. This positive change will force Q6 and Q7 to conduct less (or raise their resistance). The output voltage will decrease as a result of Q7 conducting less than when the temperature was at a lower level.

Q1 is a part of the Sequencing Control circuitry used to turn the Regulators ON and OFF.

A false input to CR34 is required to sequence ON the Regulator. With a false input, Q1 will be cut off. As long as Q1 is cut off, the Regulator will operate in a normal manner. If the input to Q1 goes TRUE due to a Power shutdown or Power failure, Q1 will conduct. When Q1 conducts, two different effects take place.

1. Q6 will draw current through R6 and R3 putting a false level on the Base of Q6. This will cut off Q6 and Q7, and the Regulator.

2. Q1 will draw current through CR14, R15, and R16 discharging the output voltage down within the 35ms time limit set by the B5370 Power Supply.

The purpose of the controlled Rectifier Q4 and Resistor R20, is to protect the Collector of Q5 on a Power shutdown.

Q3 is used as an over-current Sensing Transistor and will limit the amount of output current. The Base circuit is designed so that Q3 will be activated when a pre-determined amount of current is reached through the one ohm resistor and R35. Q3 will normally be cut off because the small voltage drop across R35 is not enough to forward-bias the Emitter to Base function. If the output current increases, the voltage dropped across R35 will increase. When the Emitter to Base voltage becomes large enough, Q3 will conduct. Q3 will lower the voltage on the Base of Q6 by drawing current through CR2 and the 5.6K resistor to -100V. Q6, having a lower voltage on the Base, will cause Q7 to decrease Collector current flow through the one ohm resistor and R35. The net effect is that Q7 will not be able to conduct more current than maximum as determined by R35, even though the output goes toward ground.

NOTE

All components inside the dotted lines are mounted on the Maintenance Display Panel.

3.20 -30V INHIBIT REGULATOR

The -30V Inhibit Regulator package is identical and interchangeable with the -30V Read and the -30V Write Regulator packages. Although the packages are the same, the operation is slightly different.

When the package is used as a -30V Inhibit Regulator, Transistor Q7 operates as a driver for five Series Regulator Transistors which are located on the Display Panel.

The current limiting load Resistor, also on the Display Panel, is changed to 0.1 ohms. This increases the output current of the Regulator to six amps, and allows the current limiting adjustment to remain compatible with the other -30V Regulators.

SEE FIGURE 3.20-1 ON THE NEXT PAGE.

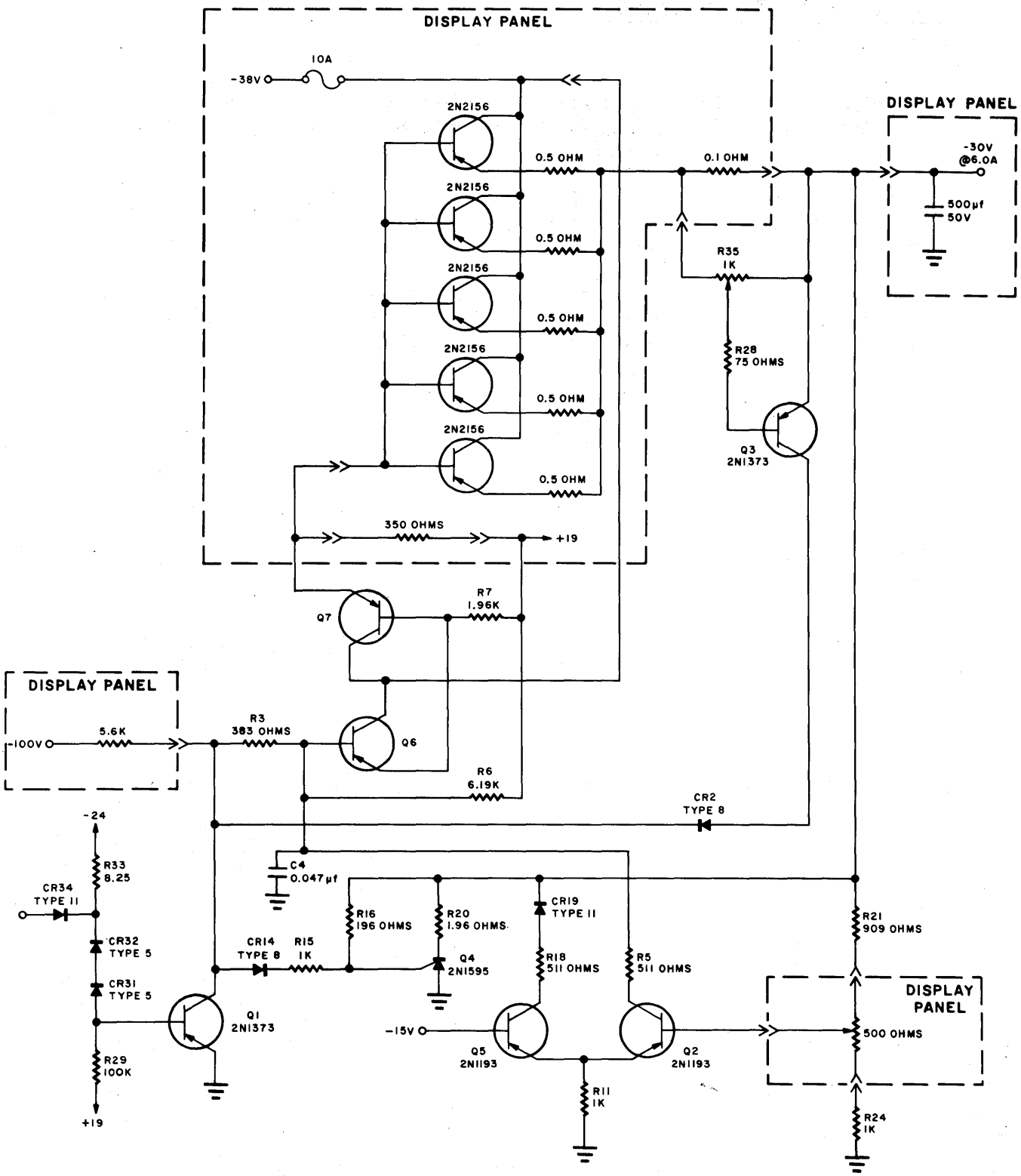


FIGURE 3.20-1
-30V INHIBIT REGULATOR

3.21 +30V REGULATOR

The +30V Regulator is used to supply current to the Address switches (SWAD) and also used in the control of the -6T Regulator.

The Regulator consists of the following circuits:

1. ON/OFF Sequencing Control (Q1 and Q2).
2. Over-Current Sensing Circuit (Q5).
3. Differential Amplifier (Q4 and Q5).
4. Driver Transistor (Q7).
5. Series Regulator (Q6).

The ON/OFF Sequencing Control is used to sequence the Regulator up and down. With a FALSE level on Input 1, the Base of Q2 will be at approximately +5V. This will allow Q2 to conduct harder, applying a positive on the Base of Q1.

With a positive on its Base, Q1 will conduct and hold the Base of Q7 at a near ground potential through diodes CR17 and CR15. Q7 in turn will hold Q6 OFF, and there will be no output from the Regulator. With a TRUE level to Input 1, Transistor Q2 will conduct less, turning Q1 OFF. With Q1 OFF, the Regulator will turn ON.

Resistor R31 and diode CR32 are used to discharge C21 and C22 through Q1 when the Regulator is turned OFF. The output of the Regulator must go to 5.0V or less within 15 milliseconds after it is turned OFF.

The Differential Amplifier circuit controls the regulation and sets the operating point of the Regulator. Any variations in the output are coupled through CR26 to the Base of Q3. Q3 would conduct either harder or less and couple the variation of the Base of Q7. The variation is direct-coupled from the Emitter of Q7 to the Base of Q6. Q6 will increase or decrease conduction, depending upon whether the original output variation was increasing or decreasing.

If a sudden load was imposed on the output of the Regulator and the voltage tried to go toward +29V, the following would take place.

1. The voltage on the Base of Q3 would decrease.
2. Q3 would then conduct less and the voltage on the Base of Q7 would increase.
3. Q7 would conduct harder, increasing the voltage on the Base of Q6.
4. Q6 would also conduct harder, increasing the output voltage to +30V.

The Over-Current Sensing Circuit is adjusted to turn ON Q5 when the output current is 600ma or over. Q5 turning ON will reduce the drive to Q7 which will turn Q6 OFF.

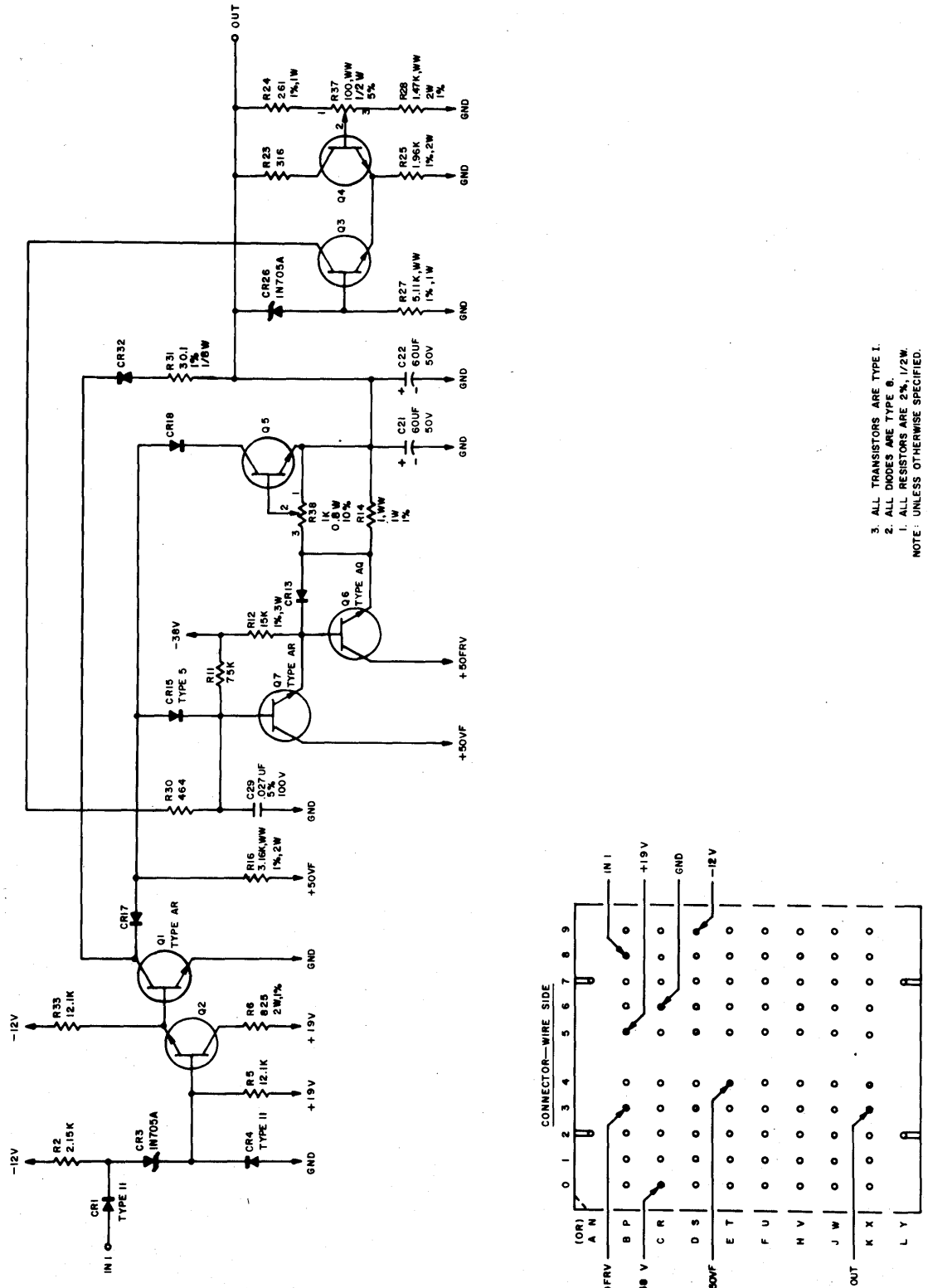


FIGURE 3.21-1
+30V REGULATOR

3.22 -6V THRESHOLD REGULATOR

The -6T Regulator is used to establish a Threshold level for the Sense Amplifiers. The output is regulated from the -12V Supply with the +20V used as a Control voltage. These two voltages are the Supply voltages for the Sense Amp packages. Using these voltages in the -6T Regulator will cause the Threshold level (-6T) to compensate for any changes in the Supply voltages, thereby stabilizing the output of the Sense Amps. If the +20V input goes more positive, or the -12V input goes less negative, the -6T output will go less negative. If the +20V input goes less positive, or the -12V input goes more negative, the -6T output will go more negative. The -6T output is connected to the center tap of the Sense Amplifier Input Transformer to provide the Threshold level for the Class "A" Amplifiers.

See Figure 3.22-1 for -6T circuitry.

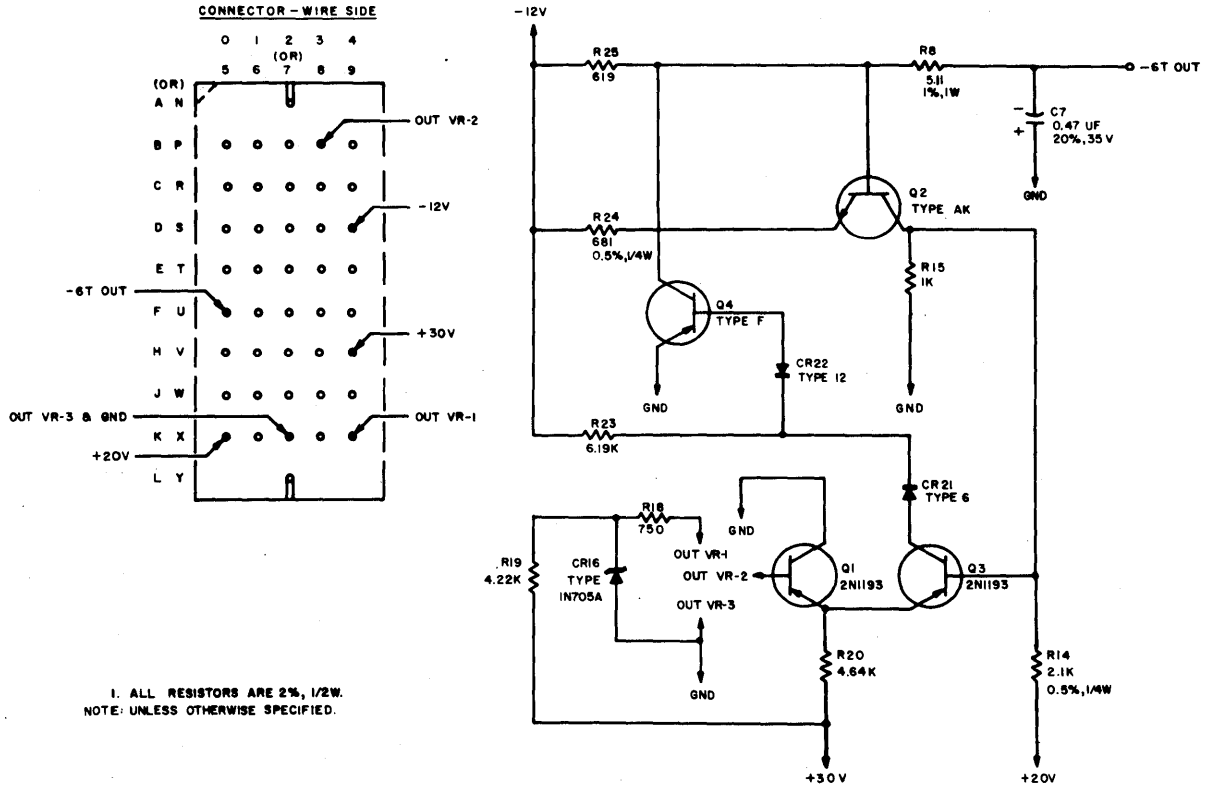


FIGURE 3.22-1
-6T REGULATOR

Circuit Description

The output of the Regulator is adjusted by a variable resistor located on the Maintenance Panel and connected to the Base circuit of Q1. If the resistor is varied to lower the voltage on the Base of Q1, Q1 will conduct harder, lowering the voltage on the Emitter of Q3. Q3 will conduct less, causing the Base of Q4 to go more negative. This will

increase conduction through Q4 and the output will go less negative. The opposite will occur if the voltage on the Base of Q1 is increased (more positive).

When the +20V input goes more positive, the -6T output should go less negative. This is accomplished by the voltage on the Base of Q3 going more positive, thereby reducing the conduction of Q3. This will increase the conduction of Q4, causing the output to go less negative. If the +20V input goes less positive, Transistor Q3 will conduct harder, causing Q4 to conduct less and the output will go more negative.

The -6T output will also follow any variations in the -12V input. If the -12V input goes less negative, the Emitter voltage on Q2 will be less negative. This will decrease conduction through Q3 and the Base of Q4 will go more negative. The Base of Q4 going more negative will increase the conduction through Q4 causing the output to go less negative.

Any variations in the -6T output are also corrected by Transistor Q2 changing the Base drive on Q3.

3.23 VOLTAGE SENSING SWITCH (SWVS)

General

The Voltage Sensing switch circuits are shown in Figure 3.23-1.

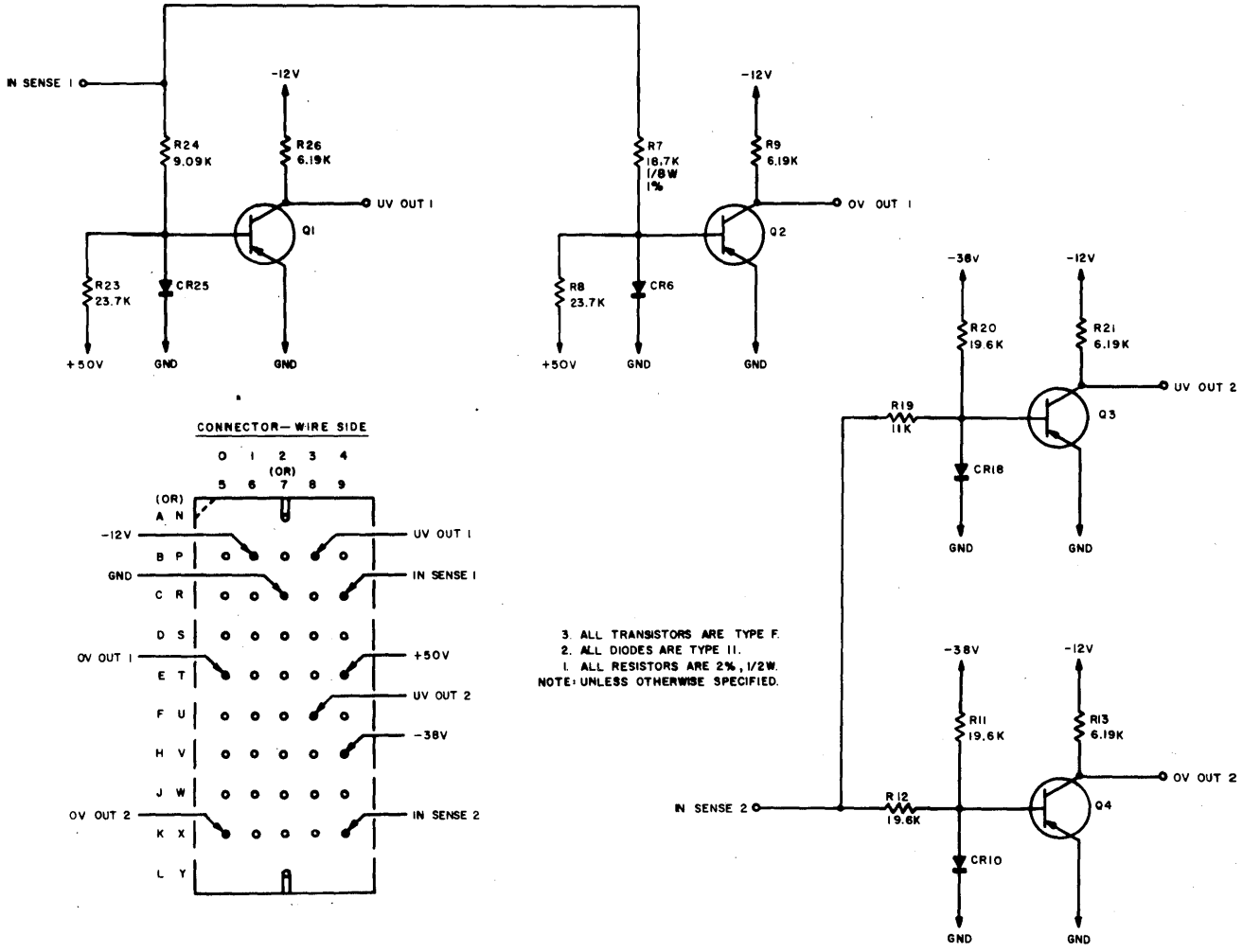


FIGURE 3.23-1
VOLTAGE SENSING SWITCH

Transistors Q1 and Q2 are used for negative voltage sensing (-30 R, W, I), and Transistors Q3 and Q4 are used for positive sensing (+30V, +100V).

NOTE

The +100V is divided down to +30V in order to use the positive voltage Sensing circuit.

Each of these circuits are used for both Over and Under Voltage sensing. The Over Voltage circuitry will give a trouble indication if any of the Voltage Regulators go 25 percent higher than the rated output and the Under Voltage circuitry will give an indication if the output decreases

30 to 35 percent.

Circuit Description Negative Voltage Sensing

Transistors Q1 and Q2 are used for negative voltage sensing. The output of a specific -30V Regulator is fed into the input labeled (In Sense 1). Transistor Q1 senses Under Voltage and Transistor Q2 senses Over Voltage. The input to Q1 has a Voltage Divider circuit, R24 and R23, which is such as to keep Q1 in saturation if the input is at -30V. If the input decreases to approximately -20V, the Base voltage of Q1 will go toward 0 volts, cutting off Q1 and allowing the output (UV out 1) to go true, giving an Under Voltage indication.

Transistor Q2 also has a Voltage Divider circuit consisting of R7 and R8, such that when the input is -30V, the Base of Q2 will be at approximately 0, keeping it cut off and the output true (OV out 1). If an Over Voltage condition develops, Q2 will turn on when the input increases to approximately -38V.

NOTE

The output of Q2 is FALSE on a negative Over Voltage, but is switched to a TRUE by another circuit whose purpose is explained in Section 3.17.

Circuit Description Positive Voltage Sensing

Transistors Q3 and Q4 are used for positive voltage sensing. The output of the +30V Regulator or +100V (divided down to +30V) is fed into the input labeled (In Sense 2). Transistor Q3 senses Under Voltage and Transistor Q4 senses Over Voltage. The Input to Q3 has a Voltage Divider circuit, R19 and R20, which is such as to keep Q3 in saturation if the input is at +30V. If the input decreases to approximately +20V, the Base voltage of Q3 will go toward 0 volts, cutting off Q3 and allowing the output (UV out 2) to go true giving a positive Under Voltage indication.

Transistor Q4 also has a Voltage Divider circuit consisting of R11 and R12, such that when the input is at +30V, Q4 will be in saturation. When the input reaches approximately +38V, the Base of Q4 will go toward 0 volts, due to the action of R11 and R12. Q4 will cut off when the Base is at 0 volts, giving a true output (Positive Over Voltage condition).

3.24 HIGH VOLTAGE SWITCH (SWHV)

General

The High Voltage Switch circuits are shown in Figure 3.24-1.

Five identical circuits are contained in each parallel plate type package. The High Voltage Switch circuits are designed to operate with voltages that are present with the DC Locked Out, and are used in the Over and Under Voltage circuits.

Circuit Description

The circuit consists of one transistor stage with associated components. The two input diodes are silicon diodes (stabistors) with a forward drop of 0.5V.

Assuming the transistor is cut off, the input signal will be at approximately zero volts. The Base of the transistor will be positive due to the voltage drop across the two input diodes. The Base Emitter junction of the transistor is reversed biased and the output will be true. When the input signal becomes more negative, the -1.0V at the Base Emitter junction of the transistor is forward biased and the transistor conducts. With the transistor conducting, the output is at a false or near ground potential.

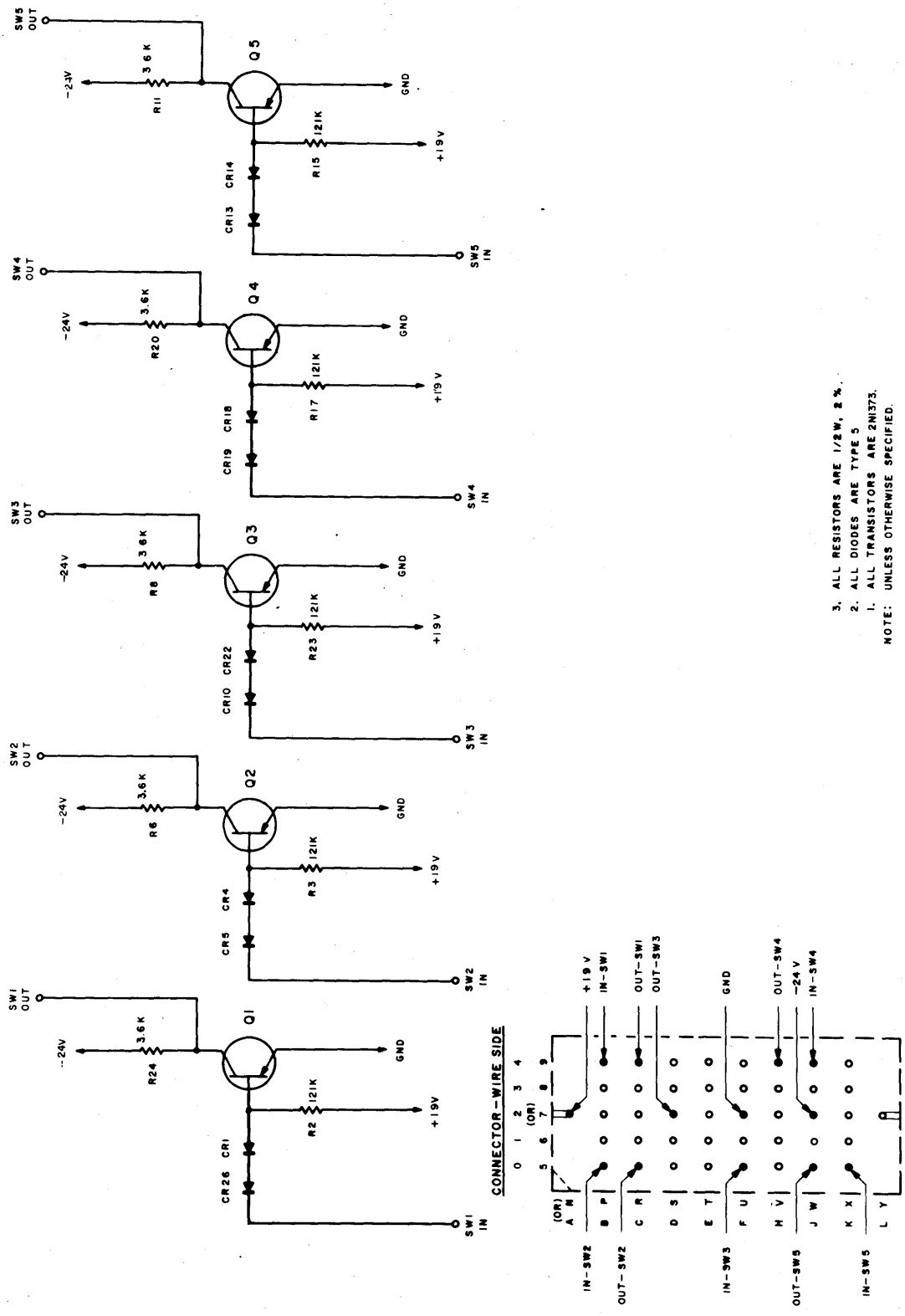


FIGURE 3.24-1
HIGH VOLTAGE SWITCH

3.25 CLOCK & CLOCK CONTROL

The Clock Pulses in a Memory Module are normally generated by the Master Clock in Central Control. Each Memory Module contains additional circuitry to generate its own Clock Pulses while in LOCAL position. This is to allow local testing of the Memory Modules to be completely independent of the Systems.

Figure 3.25-1 shows the Clock Control Logic for one Memory Module. The Master Clock oscillator in Central Control will feed a Blocking Oscillator and Line Driver (DRBL). The DRBL package will furnish the Clock Pulses required for all the Memories in one B5260 Cabinet. The output pulse duration of this package is adjustable. The Inhibit input is controlled by the Single Pulse switch to allow Memory cycles to be Single Pulsed from D & D. The output of the DRBL is sent to the Local Clock Driver in each Memory Unit. This input will be enabled if the Memory Module is in REMOTE (TRML will be true) and the output of the Local Clock Driver will be from the Master Clock.

If the Memory Module is in LOCAL, the Master Clock input is disabled and the Memory Clock input will control the Clock Pulses.

The CLSA package (Memory Clock) in the Memory Module feeds a three-legged AND gate which is made up of TRMS/, Stop Clock Switch, and CLSA. This gate feeds the MUFW Multi and will be true when the Unit is in LOCAL and the Stop Clock Switch is OFF. The Stop Clock Switch will be used for static checking of logic circuits when no Clock Pulses are wanted. The width of the Clock Pulses are determined by the MUFW Multi when the Unit is in LOCAL.

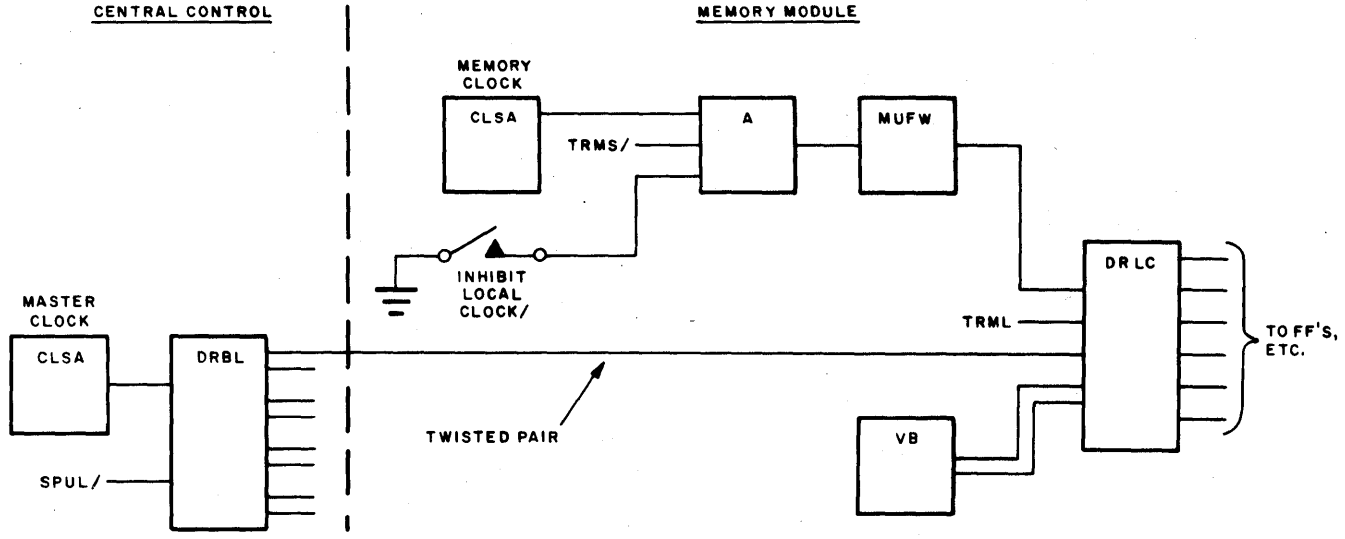


FIGURE 3.25-1
CLOCK CONTROL

3.26 DIRECT-COUPLED LOCAL CLOCK DRIVER (DRLC)

General

Reference Figure 3.26-1.

The Direct-Coupled Local Clock Driver used in the B461 Memory Module is slightly different than the normal DRLC packages due to the additional inputs. An Inhibit input has been added to Inhibit Clock Pulses from the Master Clock when the Unit is in LOCAL. A Local Clock input has also been added to allow Clock Pulses to be received from the Memory Clock circuits.

Circuit Description

In the quiescent state, Q1 and Q2 are cut off. Q3, Q4 and Q5 are conducting.

When a negative Clock Pulse is applied to the input between T/P Input and T/P Ground Input, Q1 will be turned ON. R8 provides termination for this pulse.

The turn ON of Q1 results in its Collector going negative towards its saturation potential, supplying Base drive to Q2 turning it ON.

When Q2 turns ON, its Collector starts toward its saturation potential, removing the Base drive from Q3, Q4 and Q5, cutting them OFF. This action results in a -4.5V Clock Pulse at outputs 1 thru 6 being made available to be used by the circuits within the Unit.

Diodes CR35, CR30, CR39 and CR27, clamp the outputs at -4.5V.

If the Unit is in LOCAL, the Inhibit input will be false and SHUNT the T/P input. The negative Clock Pulses will then be applied through the Local Clock input to the Base of Q2. This will supply Base drive to Q2, turning it ON. The operation is identical from this point on.

Variable Bias

In the flip-flop circuit, the Clocked inputs see the gated circuits as a load if the diodes between the Clock line and the gated levels are not back-biased. This would normally be the case since the gated inputs will tend to be at a lower level than the Clock lines due to the drop through the cascading of gating diodes. The leakage would load the Clock Driver to a greater extent than necessary. Therefore, the false level from the Local Clock Driver is adjusted sufficiently negative by the variable bias input, to back bias the flip-flop gating diodes, reducing the current and loading caused by it.

This variable bias is in the range of -0.5 to -0.8V, and is applied to the two paralleled bias terminals from a variable bias package. There

is a variable bias package associated with each Local Clock Driver package.

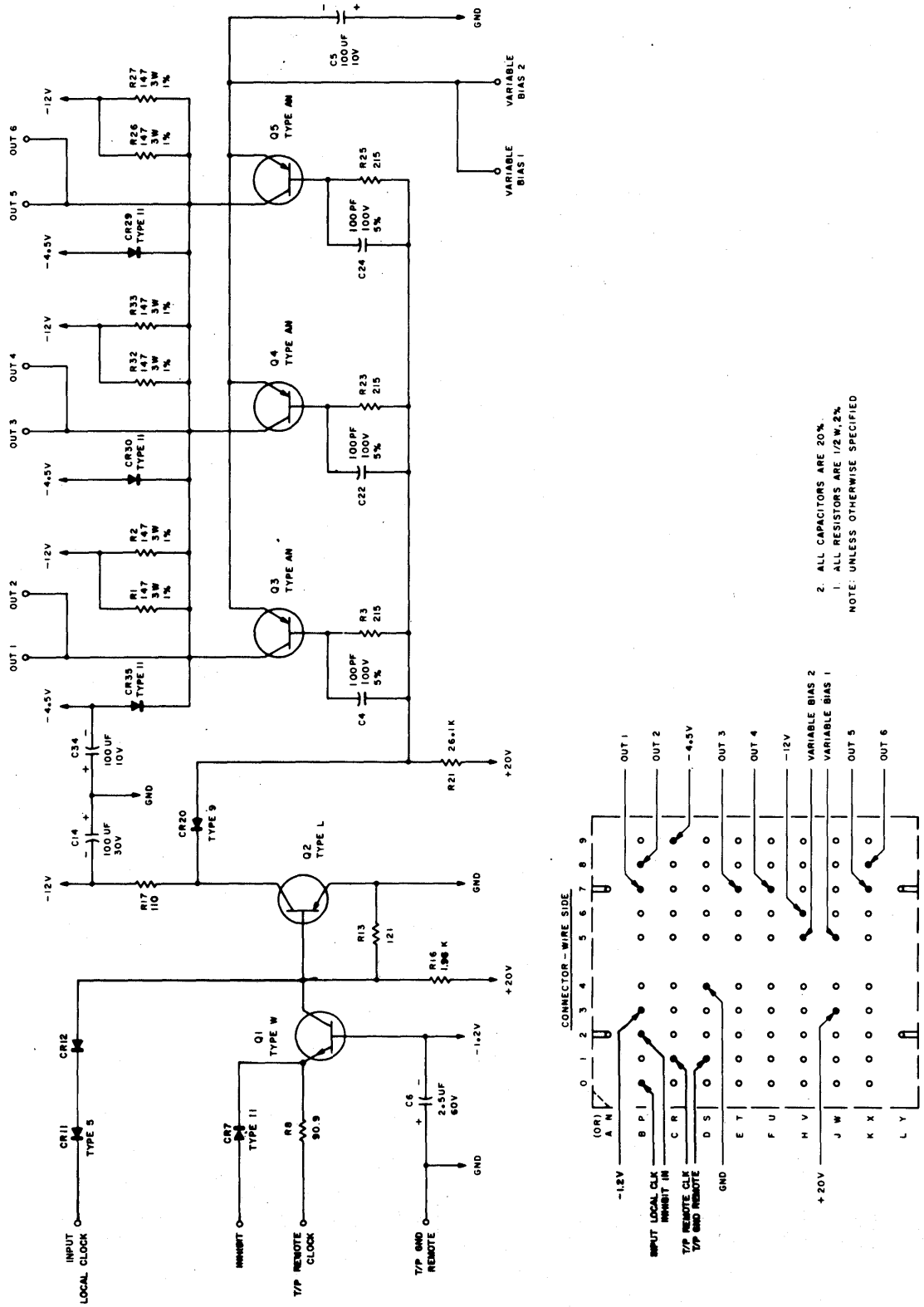


FIGURE 3.26-1
DRLC

3.27 MAINTENANCE CONTROL SWITCHES

The following is a list of the Maintenance Control Switches with a brief explanation of their purpose and the levels that are developed. Refer to Figure 3.27-1.

REMOTE/LOCAL SWITCH

Remote

1. TRML will be TRUE, and TRMS/ will be FALSE to allow this Module to operate with the System.
2. Disables the outputs from the Pattern Control Switch, Uniform/Checkerboard Switch, and the Manual/Automatic Switch.

Local

1. Lights the Local Indicator.
2. TRML will be FALSE, and TRMS/ will be TRUE to prevent the Unit from operating with the System, and allow independent Test operations.

PATTERN CONTROL (Both outputs will be FALSE if Local/Remote Switch is in Remote.)

Normal

1. Pattern Control Normal Level (PCNL) will be TRUE to allow the Pattern controlled by the Uniform/Checkerboard and Manual/Automatic Switches to be checked in a normal two-cycle operation.

Complement

1. Pattern Control Complement Level (PCCL) will be TRUE to allow the Pattern controlled by the Uniform/Checkerboard and Manual/Automatic Switches to be checked in a four-cycle Worst Case operation.

UNIFORM/CHECKERBOARD (Both outputs will be FALSE if Local/Remote Switch is in Remote.)

Uniform

1. Allows the Pattern to be Written or Read to be controlled by the Manual/Automatic Switch.

Checkerboard

1. Allows the Checkerboard or Checkerboard Complement Patterns

to be Read or Written in Memory. Checkerboard Level (CHBL) will be true.

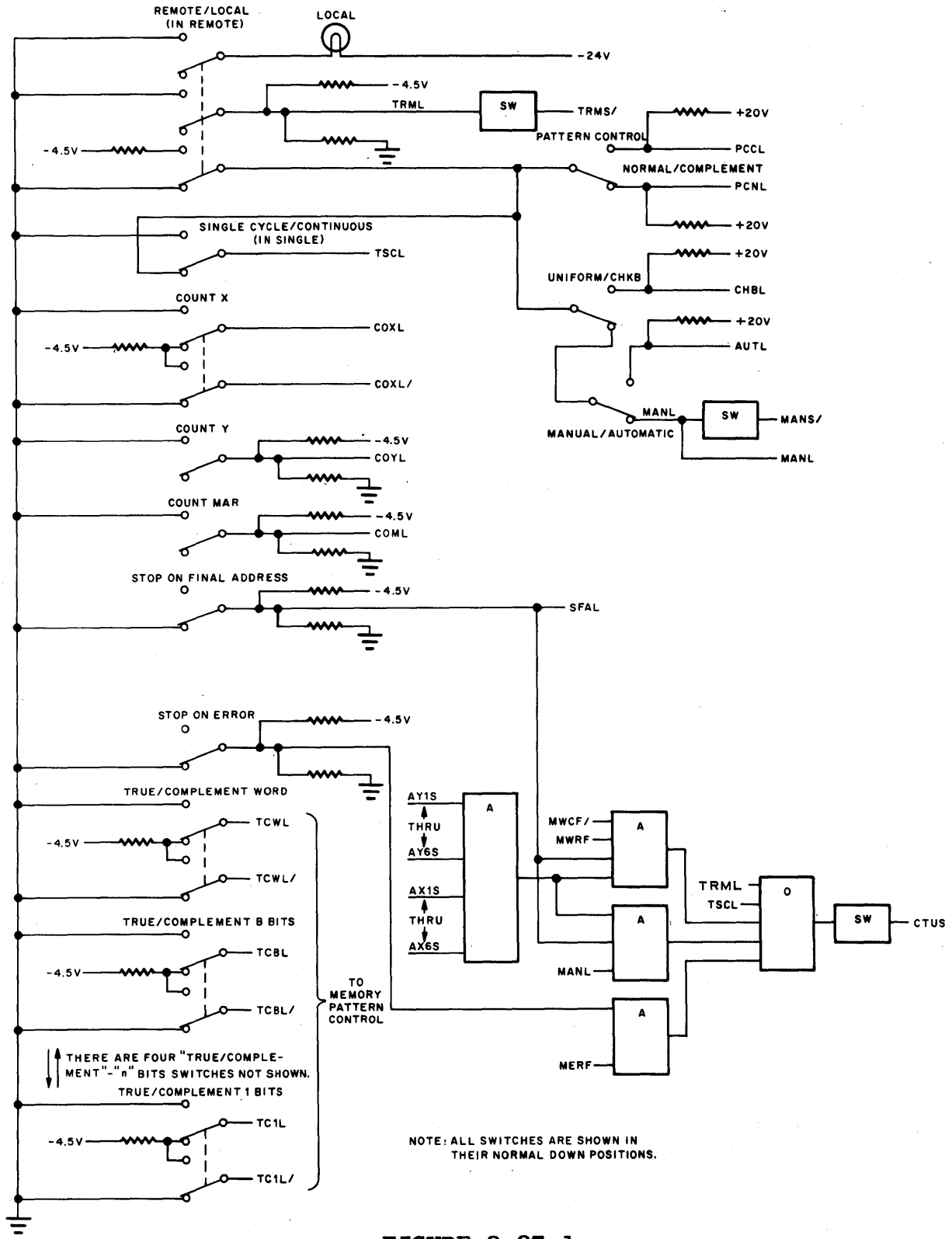


FIGURE 3.27-1
MAINTENANCE CONTROL SWITCHES

MANUAL/AUTOMATIC (Both outputs will be FALSE if the Local/Remote Switch is in Remote, or, if the Uniform/Checkerboard Switch is in Checkerboard.)

Manual

1. Manual Level (MANL) will be TRUE and Manual Switch (MANS/) will be FALSE.
2. Will allow the pattern manually Set into the MIR Flip-Flops to be Written into core with the correct Parity generated.
3. Will allow the Information contained in core to be Read and checked for the correct Parity.

Automatic

1. Automatic Level will be TRUE.
2. Will allow either the pattern Set into bit switches, or, the Complement of this pattern as determined by the Word True/ Complement Switch to be Written into core. Parity is not generated.
3. Will allow the Information Read from core to be checked against either the setting of the bit switches, or, the Complement of the bit switches as determined by the Word True/ Complement Switch. Parity is not checked.

SINGLE CYCLE/CONTINUOUS (Output will always be FALSE if Local/Remote Switch is in Remote.)

Single Cycle

1. Test Single Cycle Level (TSCL) will be TRUE to allow only one Memory cycle for each depression of the Memory Start pushbutton.

Continuous

1. Test Single Cycle Level (TSCL) will be FALSE to allow continuous Memory cycles to be taken whenever the Memory Start pushbutton is depressed.

COUNT "X" (Counting MAR is inhibited if the Count MAR Switch is in the Inhibit position.)

Count

1. Count "X" Level (COXL) will be TRUE and Count "X" Level/ (COXL/) will be FALSE to allow the first six positions of the Memory Address Register (MAR) to count up each Memory cycle.

Inhibit

1. COXL will be FALSE, and COXL/ will be TRUE to inhibit counting of the first six positions of MAR.

COUNT "Y" (Counting MAR is inhibited if the Count MAR Switch is in the Inhibit position.)

Count

1. The Count "Y" Level (COYL) will be TRUE.
2. This will allow the last six positions of MAR to count each Memory cycle if the Count "X" Switch is in the Inhibit position.
3. If the Count "X" Switch is in the Count position, MAR will be counted normally.

Inhibit

1. Count "Y" Level (COYL) will be FALSE.
2. The counting of the last six positions of MAR is inhibited and the first six positions of MAR will recycle after a maximum count is reached.

COUNT MAR

Count

1. Count MAR Level (COML) will be TRUE.
2. MAR will be allowed to count in the manner determined by the positions of the Count "X" and Count "Y" Switches.

Inhibit

1. Count MAR Level (COML) will be FALSE.
2. All MAR counting is inhibited.

STOP ON FINAL ADDRESS

Down

1. Stop On Final Address Level (SFAL) will be FALSE, and the Continue Switch (CTUS) output will remain TRUE.

Up

1. Stop On Fianl Address Level (SFAL) will be TRUE, and allow continuous Memory cycles to be stopped when the Final Address is reached.
2. If a Checkerboard or Automatic operation is being performed,

the Memory cycle will be stopped after the last Write cycle has been performed on the Final Address.

STOP ON ERROR

Down

1. Stop On Error Level (SOEL) will be FALSE, and any Errors detected will not cause Memory cycles to stop.

Up

1. Stop On Error Level (SOEL) will be TRUE, and any Errors detected by setting the Memory Error Flip-Flop will cause Memory cycles to stop by causing CTUS to go FALSE.
2. The Memory Information Register Clear and the Address Register Count Logic is inhibited.

TRUE/COMPLEMENT WORD

True

1. True Complement Word Level (TWCL) is TRUE, and TWCL/ is FALSE.
2. If the Uniform/Checkerboard Switch is in Checkerboard, the Checkerboard Pattern will be Written or Read and checked.
3. If the Uniform/Checkerboard Switch is in Uniform, and the Manual/Automatic Switch is in Automatic, the pattern Written or Read and checked will be determined by the position of the Bit Switches.

Complement

1. The True Complement Word Level (TWCL) will be FALSE, and TWCL/ will be TRUE.
2. If the Uniform/Checkerboard Switch is in Checkerboard, the pattern Written or Read and checked will be the Complement of the Checkerboard.
3. If the Uniform/Checkerboard Switch is in Uniform and the Manual/Automatic Switch is in Automatic, the pattern Written or Read and checked will be the Complement of the Pattern set into the Bit Switches.

TRUE/COMPLEMENT "n" BITS

True

1. The True Complement "n" Level (TCML) will be TRUE, and the TCML/ level will be FALSE.
2. With the True/Complement Word Switch in the True position,

the Information Flip-Flops associated with this Bit Switch will Reset for the Checkerboard and Automatic Patterns.

Complement

1. The True Complement "n" Level (TCML) will be FALSE, the TCML/ level will be TRUE.
2. With the True/Complement Word Switch in the True position, the Information Flip-Flops associated with this Bit Switch will be Reset for the Checkerboard and Automatic Patterns.
3. With the True/Complement Word Switch in the Compliment position, the Information Flip-Flops associated with this Bit Switch will be Set for the Checkerboard and Automatic Patterns.

3.28 PATTERN CONTROL & TEST CIRCUITS

Circuitry has been added to the B461 Memory Unit to provide for certain Memory operations to be performed while the Unit is in LOCAL. These operations allow the reading and writing of various patterns which are controlled by the Test Switches located on the Maintenance Panel (Reference Section 3.27).

There are three main patterns which can be run with many variations. They are as follows:

1. Checkerboard
2. Uniform Automatic
3. Uniform Manual.

Checkerboard Pattern

The Checkerboard Pattern sets four adjacent cores to the same state. With the Bit True/Complement and Word True/Complement Switches in the TRUE position, the Checkerboard Pattern will be as follows:

Y0 + X0 = 0	Y0 + X1 = 0	Y0 + X2 = 1	Y0 + X3 = 1
Y1 + X0 = 0	Y1 + X1 = 0	Y1 + X2 = 1	Y1 + X3 = 1

The pattern is generated by using MAR 2 and MAR 8 as controls to Set the MIR Flip-Flops. If MAR 2 and MAR 8 are both ON or both OFF, gating is generated to Set the MIR Flip-Flops to the "zero" state. If one is ON and the other OFF, gating is generated to Set the MIR Flip-Flops to the "one" state. Figure 3.28-1 shows the Checkerboard Pattern as it would look on one plane of the Core Stack.

The complement of this pattern can be tested by placing the Word True/Complement Switch in the COMPLEMENT position. This will set "zeros" in all cells previously containing "ones", and "ones" in the cells previously containing "zeros". Also, the Bit True/Complement Switches can be used to complement the pattern in all the planes associated with that BIT position. For example: If the True/Complement "B" Bit Switch is in the COMPLEMENT position and all others are TRUE, the Checkerboard Pattern in planes 49, 48, 42, 36, 30, 24, 18, 12 and 6 will be complemented. All other planes will have the Checkerboard Pattern.

Two-Cycle Operations

The Checkerboard Pattern, and variations of this pattern, can be written in Memory and then tested in two different modes of operation. These modes of operation are under control of the Pattern Control Switch (PCCL/NORMAL). With this switch in the NORMAL position, the Checkerboard Pattern is tested in a two-cycle operation.

1. The first cycle will read the Information from the addressed

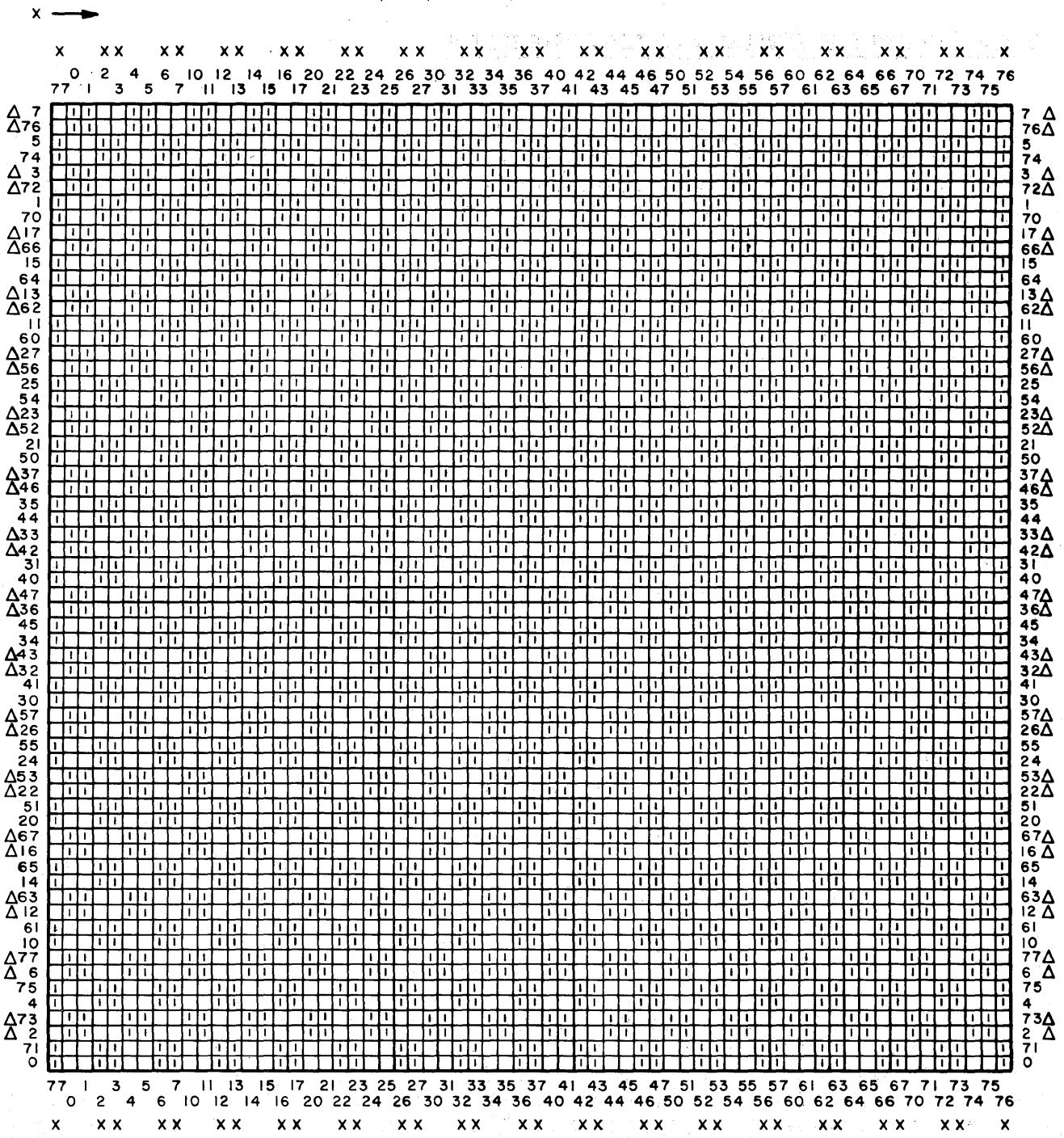


FIGURE 3.28-1
CHECKERBOARD PATTERN

word and check it against the pattern set in the switches. This Information is written back into the word addressed during the Write phase of this Read cycle. The Address Register is not counted up at this time.

2. The second cycle is a Write operation. This cycle will regenerate the pattern set in the switches, and Write it back into the word addressed. At the end of this cycle, MAR will be counted up.

During a complete cycling of Memory in this mode of operation, each Address will be accessed twice.

Four-Cycle Operation

With the Pattern Control Switch in the PCCL (Pattern Control Complement Level) position, the Checkerboard Pattern can be tested in a four-cycle operation. This type of operation is referred to as a Worst Case operation.

1. The first cycle of this operation is the same as in the two-cycle. The Information is read and checked against the pattern set in the switches.
2. The second cycle is again a Write cycle on the same Address, but the Information written is the complement of the pattern set into the switches. The Address is also inhibited from counting in this cycle.
3. The third cycle is a Read cycle, and the Information is checked against the complement of the Information set into the switches. Again, the Address is not counted.
4. The fourth cycle is a Write cycle. The original pattern is taken from the switches and written back into the word addressed. The Address is allowed to count up at the end of the cycle.

To test the checkerboard pattern using one of the previously described modes of operation, the pattern must first be written throughout the Core Stack. To accomplish this, the Maintenance Switches must be in the following configuration:

1. LOCAL/REMOTE Switch - In LOCAL.
2. STOP ON FINAL ADDRESS Switch - in UP position.
3. COUNT MAR - in DOWN position.
4. CONTINUOUS/SINGLE CYCLE - in CONTINUE position.
5. STOP ON ERROR - in IGNORE position.
6. CHECKERBOARD/UNIFORM - in CHECKERBOARD position.

The PCCL/NORMAL, the TRUE/COMPLEMENT WORD, and the TRUE/COMPLEMENT BIT Switches are all in the desired pattern and mode configuration. The AUTO/MANUAL Switch will have no effect and may be in either position.

Depression of the START pushbutton will cause the Information to be written throughout the Core Stack. The operation will stop with the last Address in MAR and the Memory Pulse Counter equal to three.

The MIR will contain the Information written into the last Address. The pattern has now been written throughout Memory.

In order to test the pattern written, the STOP ON ERROR Switch should be placed in the STOP position. When the START pushbutton is depressed, the pattern written in Memory will be tested in the desired mode of operation.

Uniform Automatic Pattern

The Uniform Automatic Pattern consists of the same pattern written throughout Memory. The Information can be varied by the WORD and BIT TRUE/COMPLEMENT switches. With the WORD TRUE/ COMPLEMENT and all the BIT TRUE/COMPLEMENT switches in the TRUE position, an all "ones" pattern will be written or tested in every Address throughout the Core Stack. With the WORD TRUE/COMPLEMENT Switch in the COMPLEMENT position and all the Bit Switches TRUE, the pattern will be all "zeros".

The Pattern Control Switch will control the mode of operation that the Auto Pattern has written and/or tested in the same manner as in Checkerboard. The desired Auto Pattern is written and tested with the same switch configuration as previously described, except the UNIFORM/CHECKERBOARD switch must be in UNIFORM, and the MANUAL/AUTO switch must be in AUTO.

Uniform Manual Pattern

The Uniform Manual Pattern consists of setting the desired bit configuration into MIR, and writing this configuration throughout Memory by manually setting MWRF. The correct Parity is generated automatically through the Parity circuits. After the Manual pattern has been written, it can be read simply by resetting the Memory Flip-Flop (MWRF).

The Read operation will check for the correct Parity. If the STOP ON ERROR Switch is in the STOP position, it will stop the Memory cycles if an incorrect Parity is detected.

The Pattern Control switch will have no effect on this operation and only continuous Write cycles will be taken if MWRF is set, or, continuous Read cycles if MWRF is reset.

The MIR Clear Level is inhibited during the Write cycles so the Information set into MIR will remain there until MWRF is reset.

During the Read cycles, MIR is cleared at the end of each cycle unless the Read cycles are stopped with a Parity Error.

3.29 MAINTENANCE START LOGIC

The Maintenance Start Logic shown in Figure 3.29-1, consists of the logic necessary to start a Local Memory cycle. A Memory cycle is started when the Multi Timing circuits are triggered. Depression of the START pushbutton will also set the Master Start Flip-Flop at the end of each Memory cycle (MPC = 3).

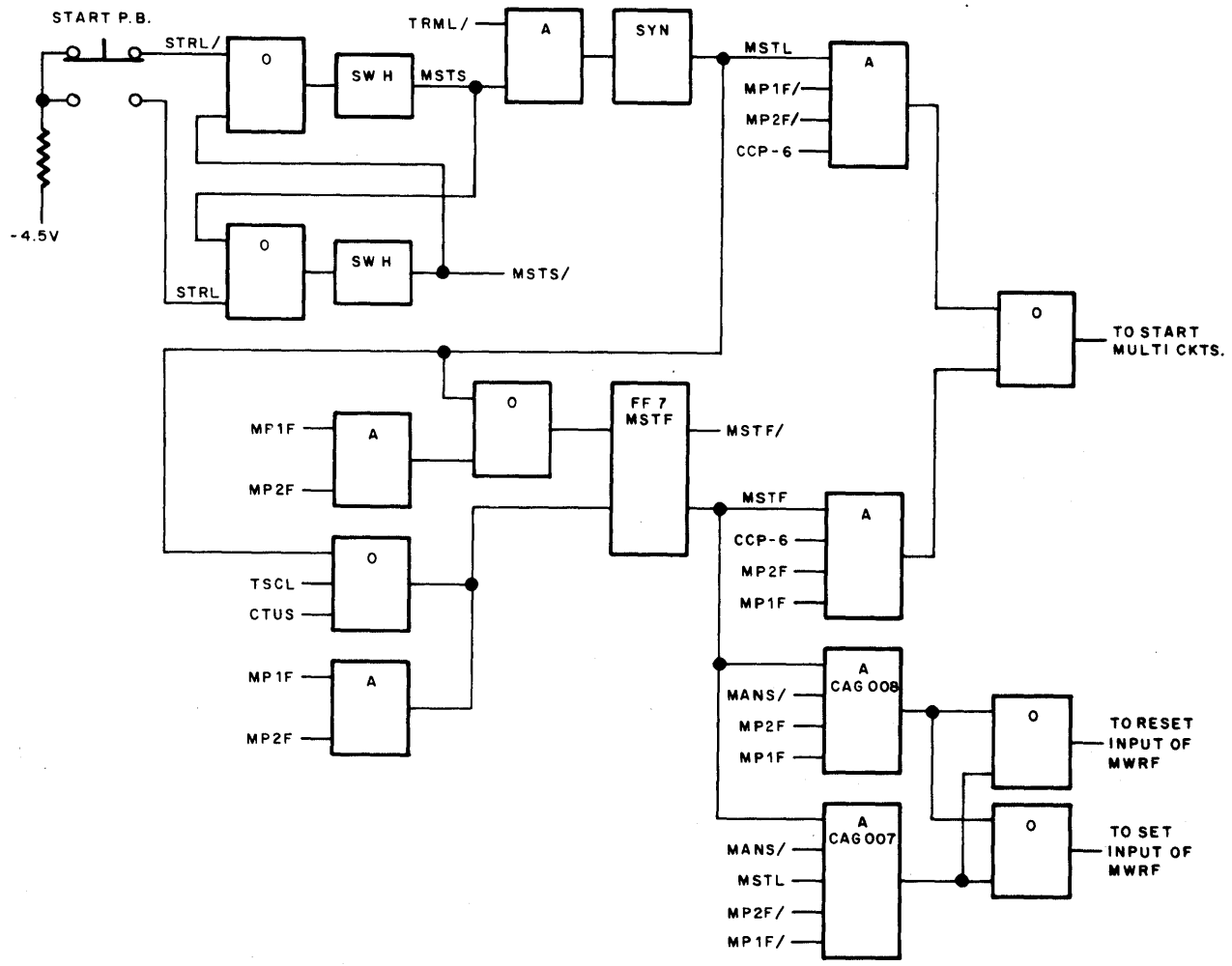


FIGURE 3.29-1
TEST START CIRCUITS

The MSTF flip-flop is used to record the fact that a cycle has previously been executed, and will allow MAR to count up at the start of then next Memory cycle.

During a continuous operation (CTUS is TRUE), MSTF is used to start each additional Memory cycle. MSTF is also used to control the complementing of the Memory Write Flip-Flop during the Checkerboard and Automatic patterns.

When the START pushbutton is depressed with the Memory Module in LOCAL,

the Start Level (STRL) will go TRUE and set the Master Start cross-coupled switch. This crosscoupled switch will remain set as long as the START pushbutton is held down.

With the cross-coupled switch Set, MSTS will be TRUE. This output is ANDED with TRML/ and used to enable a synchronizer circuit. The synchronizer output will go TRUE for the following Clock Pulse. In this way, the Master Start Level (MSTL) will be TRUE for the duration of one Clock Pulse each time the START pushbutton is depressed.

MSTL is ANDED with a Clock Pulse (CCP-6) and Memory Pulse Counter equal to zero (MP1F/ and MP2F/) which are TRUE and used to start the Multi Timing circuits.

If this is a Single cycle operation, MSTF will be set at the end of the cycle by TSCL which is SHUNT ANDED with MP1F and MP2F. The same Clock Pulse that sets MSTS will set MPC to zero and prevent the Multi Timing circuits from being triggered.

The next depression of the START pushbutton will start the Memory cycle in the same manner as before. MSTL will also be used to reset MSTF. MSTF will again be set at the end of the cycle.

If continuous operation is desired, CTUS is TRUE to set MSTF at the end of the first cycle. The following Clock Pulse will start the Multi Timing circuits since the MPC is not reset to zero during a continuous operation and remains at a count of three for two Clock Pulses. The same Clock Pulse that starts the Multi Timing also resets MSTF. As long as CTUS is TRUE, MSTF will be set for one Clock Pulse at the end of each cycle to start the next cycle.

CAG 007 is used to complement the Memory Write Flip-Flop when Checkerboard and Automatic patterns are desired and the Pulse Counter is a zero. CAG 008 will complement the Write Flip-Flop each cycle for the same patterns when in the Continuous mode of operation.

3.30 PATTERN CONTROL LOGIC

The Pattern Control Logic shown in Figure 3.30-1, consists of the logic necessary to generate the Checkerboard and Automatic patterns.

The Checkerboard pattern is generated when the UNIFORM/CHECKERBOARD switch is in the CHECKERBOARD position. The Checkerboard pattern can be generated in both the Normal and Worst Case modes of operation with many variations in the Information due to the TRUE/COMPLEMENT Word and Bit switches.

First, consider the Checkerboard pattern in the NORMAL mode of operation with all Word and Bit switches TRUE. This operation will never Set the Worst Case Flip-Flop (MWCF) since PCCL is always FALSE. The Auto (AUTL) and Manual (MANL) levels will both be FALSE due to the UNIFORM/CHECKERBOARD switch. The Checkerboard Level (CHBL) and True/Complement Word Level (TWCL) will both be TRUE to allow the output of Pattern Control 1 Switch to be TRUE only when MAR 2 and 8 bits are equal (A02F and A08F). The Pattern Control 1 Switch output is then ANDED with MANS/ which is TRUE, and PCNL which is TRUE when in the Normal mode. The output of this gate is sent to Pattern Control 3 Switch. PC3S output again is switched by PC4S.

The Pattern Control 4 Switch output will be FALSE when A02F and A08F are equal, and TRUE when they are NOT equal. This output is ANDED with the with the true output of the six TRUE/COMPLEMENT Bit switches. The outputs of these AND gates are sent to the six Maintenance Control "n" Drivers (MCnD).

The outputs of the Maintenance Control "n" Drivers are used to set the Pattern Control checking circuits where these outputs are compared against the Information read from the Core Stack during the Read cycles.

If the TRUE/COMPLEMENT Word switch is the the COMPLEMENT position, the opposite pattern is generated. The output of PC1S is TRUE when A08F and A02F are equal and the Complement Pattern is generated. The TRUE/COMPLEMENT Bit switches will also cause the pattern to be complemented but only in bit positions associated with the Bit switch. This is accomplished by ANDING TCnL/ with the PC3S output.

When the Pattern Control switch is in the COMPLEMENT position (PCCL is TRUE), the patterns are generated in the four-cycle mode of operation. The Memory Worst Case Flip-Flop is used in this mode of operation. This flip-flop will be set at the start of the second cycle and reset at the start of the fourth cycle. When the flip-flop is set, the Complement pattern is generated by inserting PC2S into the input circuit of PC3S. This will allow the Checkerboard pattern to be generated for the first and fourth cycles, and the Complement pattern for the second and third cycles.

The Automatic pattern is generated by allowing the TRUE/COMPLEMENT Word switch to control the input of PC1S. This will allow the pattern to be the same throughout the entire Memory. The Automatic pattern

can be run in either the two or four cycle modes of operation.

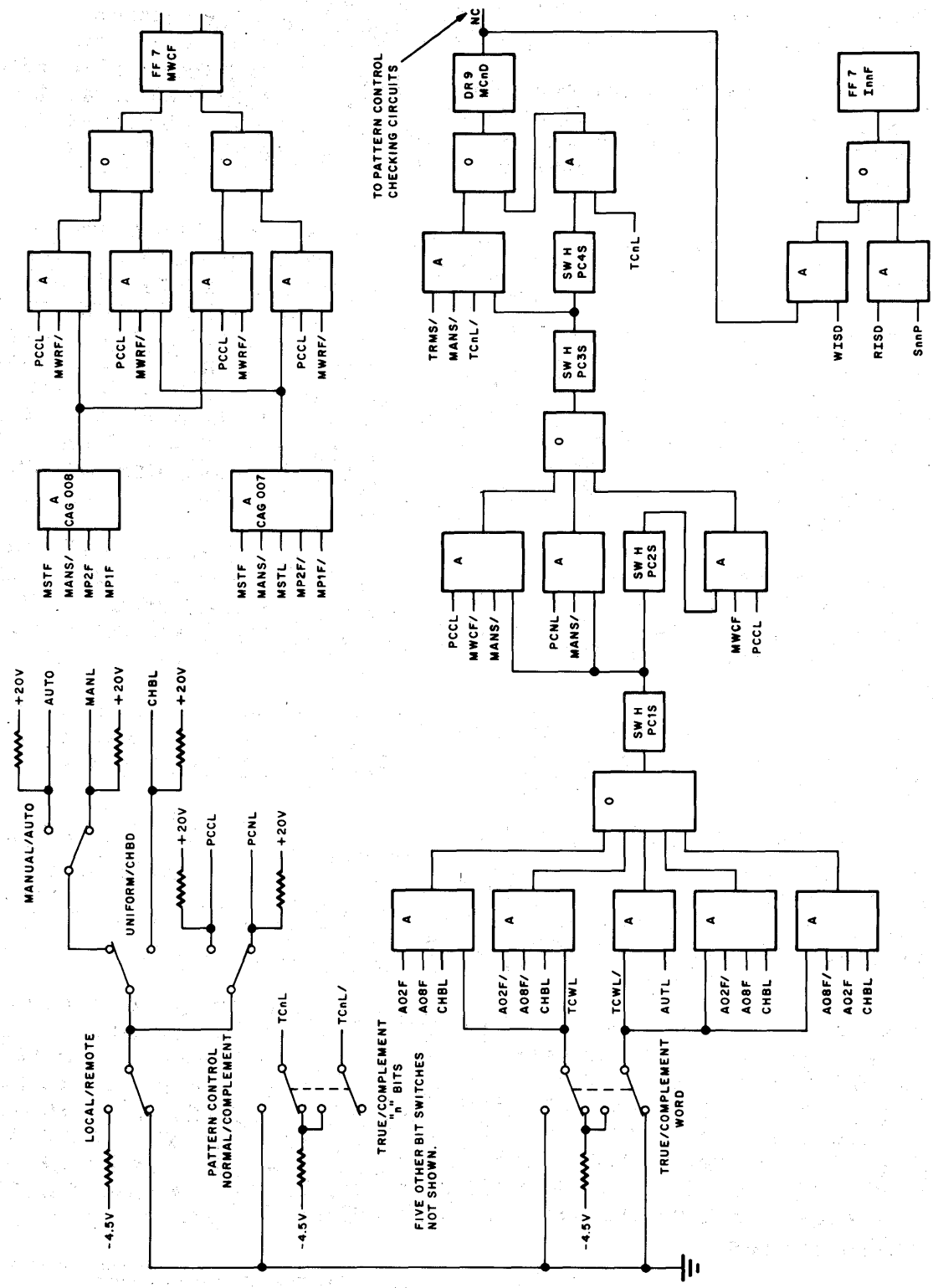


FIGURE 3.30-1
PATTERN CONTROL LOGIC

3.31 PATTERN CONTROL CHECKING CIRCUITS

The Pattern Control Checking Circuits are used to compare the Information read from the core with the output of the Pattern Control circuits. Figure 3.31-1 shows the circuits necessary to compare the "B" Bit Information Flip-Flops output with the Maintenance Control "B" Bit output from the Pattern Control logic. The Checking circuits are only used on the Checkerboard and Automatic patterns.

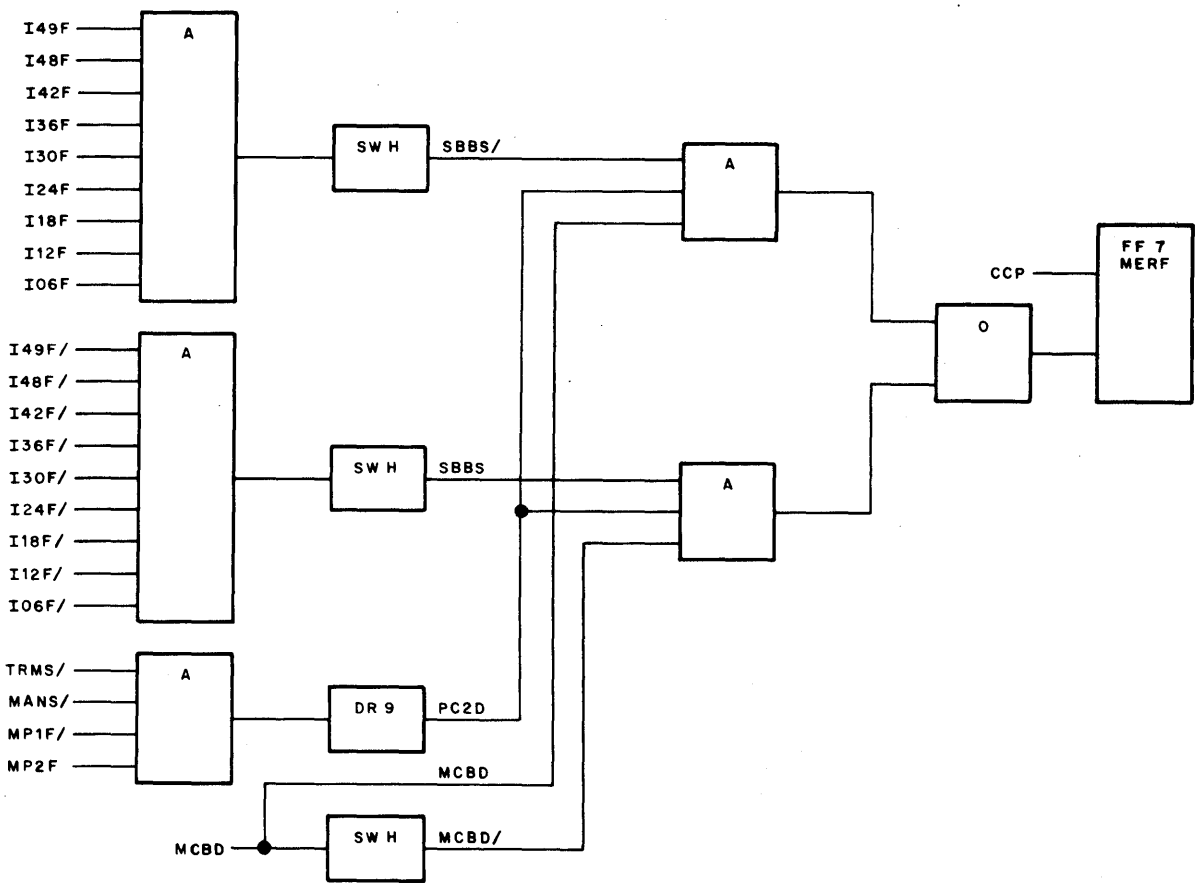


FIGURE 3.31-1
PATTERN CONTROL CHECK CIRCUITS

The Pattern Control 2 Driver (PC2D) output will be TRUE for these patterns at MPC = 2 time. If the Maintenance Control B Driver (MCBD) output is TRUE, the Information contained in the "B" Bit Information Flip-Flops should also be TRUE. If one of the flip-flops are not set, SBBS/ will be TRUE, and the Memory Error (MERF) Flip-Flop will be set when MP2F comes TRUE. If MCBD/ is TRUE, the "B" Bit Information Flip-Flops should be reset and SBBS should be FALSE to prevent the resetting of MERF.

During the Manual operation, MANS/ is FALSE to prevent setting MERF with these circuits. The Parity circuits are used to detect an Error during this type of operation.

The Pattern Control Checking circuits will detect an Error in the MIRs

on both Read and Write operations. If an Error occurred during a Write operation, it would mean the Information was not correctly set into the MIR. If an Error is detected during a four-cycle Worst Case operation, the cycle in which the Error was detected is determined by checking the status of the Memory Write Flip-Flop and the Memory Worst Case Flip-Flop. If both flip-flops are reset, the Error was detected on the first cycle. If both flip-flops are set, the Error was detected on the second cycle. If MWCF is set and MWRF reset, the Error is in the third cycle. If MWRF is set and MWCF reset, the Error was detected in the fourth cycle.

3.32 TEST CONTINUE CIRCUITS

The Continue circuits are used to allow continuous Memory cycles to be taken and to prevent further cycles when certain conditions occur. Reference Figure 3.32-1.

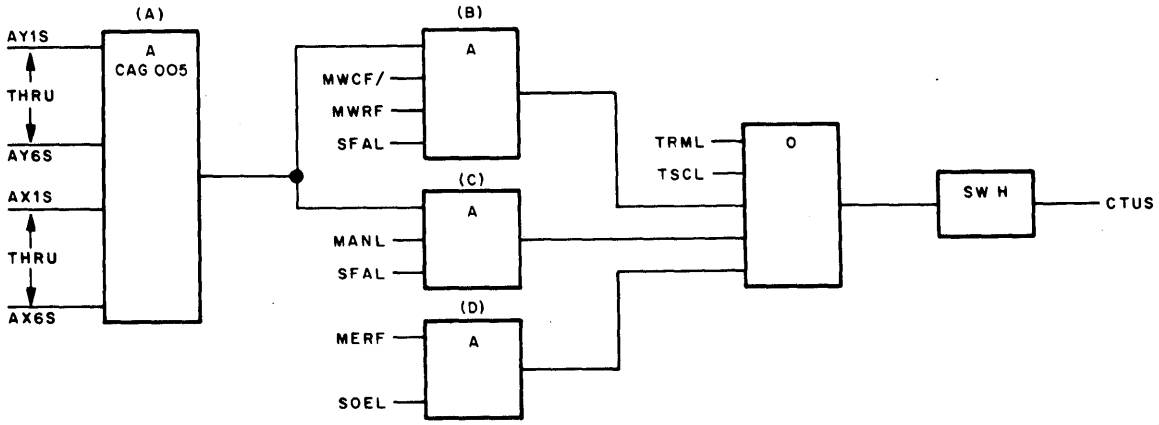


FIGURE 3.32-1
TEST CONTINUE CIRCUITS

The Continue switch output (CTUS) when TRUE, is used to set up conditions at the end of one cycle to start the next.

The output of CTUS is normally TRUE when in LOCAL and the Single cycle switch is in CONTINUOUS.

Three conditions will cause CTUS to go FALSE when in LOCAL. These are as follows:

1. When the Single Cycle switch is placed in the SINGLE position, it will cause the Test Single Cycle Level (TSCL) to go TRUE and keep CTUS FALSE.

2. When an Error is detected and the STOP ON ERROR switch is in the STOP position, the Stop On Error Level (SOEL) will be TRUE and enable one leg of AND gate D. If an Error is detected by either the Pattern Control circuits or the Parity circuits, MERF will be set. This will enable the other leg of AND gate D and cause CTUS to go FALSE.

3. When the STOP ON FINAL ADDRESS switch is in the STOP position and the last word in Memory has been addressed, the STOP ON FINAL ADDRESS switch will cause SFAL to be TRUE to AND gates B and C. CAG 005 will have a TRUE output to gates B and C when all MAR flip-flops are set.

   During a Manual operation, MANL will be TRUE and CTUS will go FALSE. The STOP ON FINAL ADDRESS switch is used to stop the Memory cycles on the last cycle of an operation accessing the last Address in Memory. The Manual operation accesses each Ad-

dress for only one cycle, so CTUS will go FALSE during this cycle.

During a Checkerboard or Automatic operation, each word will be accessed either two or four cycles depending upon the status of the Pattern Control switch. In either case, the last cycle will be a Write cycle with the Worst Case Flip-Flops off. AND gate B is used to cause CTUS to go FALSE under these conditions.

3.33 TEST CLEAR CIRCUITS

The Test Clear circuits shown in Figure 3.33-1, consist of the circuits used to clear the Memory Information Register and Memory Error Flip-Flops under local test conditions.

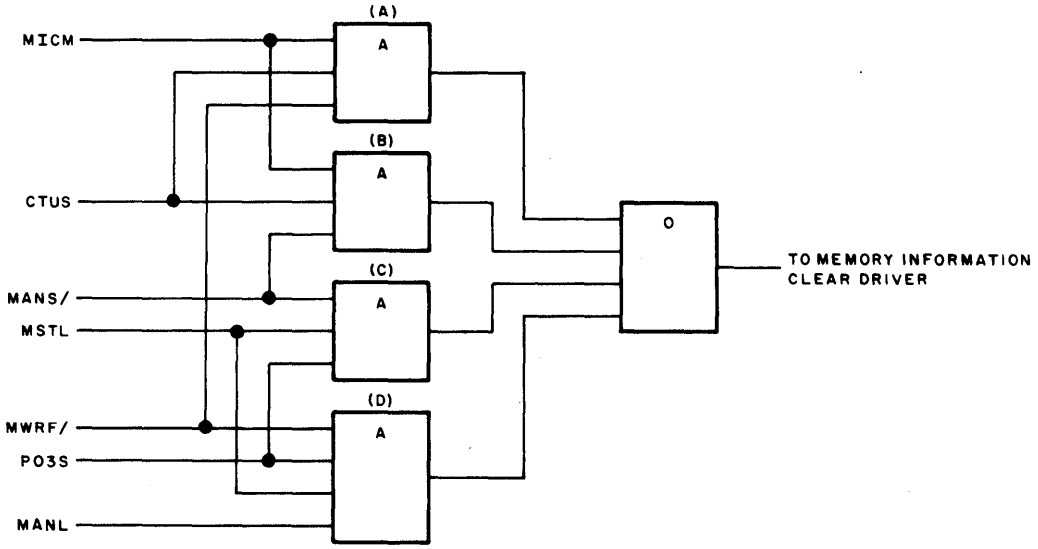


FIGURE 3.33-1
TEST CLEAR CIRCUITS

AND gate A will have a TRUE output that will cause MIR and MERF to be cleared at the end of a Read operation. CTUS is used to prevent this clear if an Error is detected and the STOP ON ERROR switch is in the STOP position. This will allow any Error detected to remain in the Information Register.

AND gate B will cause the clear of MIR and MERF on a Checkerboard or Automatic Write cycle. MIR and MERF are not cleared when in a Manual operation to allow the pattern manually set in MIR to be written throughout the Memory. CTUS is used for the same purpose as in AND gate A.

AND gates C and D are used to clear the MIR and MERF after the Memory cycles have been stopped due to CTUS going FALSE. P03S is TRUE when the Memory Pulse Counter is equal to zero or three. If the operation is a Manual Write, MIR is not cleared to prevent loss of the pattern manually set into MIRs.

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5. ASSEMBLY - DISASSEMBLY - ADJUSTMENTS

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5.1 MEMORY MULTI TRAIN TIMING

Purpose

The purpose of the Memory Multi Train Timing is to adjust the delay and duration of the Memory Timing Pulses and verify correct operation of the Multi Train.

Requirements

All pulses must meet the timing requirements as outlined in Table 5.1-1. Timing measurements should be made at the -2.0V level.

Oscilloscope Set-Up Procedure

With the Memory in LOCAL and running the Uniform - True - Normal pattern, set up the oscilloscope as follows:

	CONTROL	SET TO
1.	CHANNEL "A"	
	a. Volts/cm	0.2 (with X10 probe)
	b. Input	AA C7 B7 (Clock)
2.	CHANNEL "B"	
	a. Volts/cm	0.2 (with X10 probe)
	b. Input	See Table 5.1-1
3.	TIME BASE "A"	
	a. Stability/Triggering Level	Fully Clockwise
	b. Time/cm	0.1μs
	c. Horizontal Display	"A" Delayed by "B"
4.	TIME BASE "B"	
	a. Trigger Input	Connect to AB B1 F9 (MSTF)
	b. Trigger Mode/Slope	External Negative
	c. Stability/Triggering Level	Negative and as necessary for a Steady Trace
	d. Time cm/Delay Time	2.0μs
	e. Delay Time Multiplier	Vary as necessary to see different portions of the Memory cycle

Adjustments

With the oscilloscope set up as previously shown, the Clock Pulse will be on the "A" trace and the desired Multi output on the "B" trace.

To find T_0, look at MS1M on the "B" trace. The Clock Pulse that occurs at the Leading Edge of MS1M is T_0.

TABLE 5.1-1.

SIGNAL	CHECK PULSE AT LOCATION	START TIME FROM T_0	TRAILING EDGE	ALLOWABLE START TIME VARIATION	ALLOWABLE TRAILING EDGE VARIATION	REMARKS
MS1M	AD C0 X6	0.10		0.09 - 0.11		SEE NOTE BELOW*
MR2M	AD C1 X1	0.20	1.20	+0.08 to +0.14 REF. MS1M	1.10 - 1.30	
STTP	AB D2 B5 (RISD-1)	0.83	0.98	0.62 - 0.64 FROM L.E. MR2M	0.95 - 1.01	
MRWP	AD C2 U5	1.50	APPROX. 1.80	1.45 - 1.55		SEE NOTE BELOW**
MIHM	AC C3 V9	1.52		1.50 - 1.60		SEE NOTE BELOW***
MW2M	AD C4 X1	1.62	2.62	1.60 - 1.66	2.52 - 2.72	
MIHM	AC C3 V9		2.70		2.65 - 2.75	
MS1M	AD C0 X6		2.80		2.75 - 2.85	
MICM	AB D2 K4	2.80	2.95	2.80 - 2.90	2.90 - 3.00	

NOTES:

*The Trailing Edge of MS1M is checked after MIHM because of the holdover action from MIHM.

**The width of MRWP is not critical. The width should be greater than 0.30μs and less than 0.50μs.

***The Trailing Edge of MIHM is checked after MW2M because of the holdover action from MW2m.

Some of the adjustments on the Multis are sealed. This is done to insure that these adjustments will not be changed. If any of these adjustments do not meet the specifications outlined in Table 5.1-1, then the Multi should be replaced.

Refer to the Timing Chart in Figure 5.1-1, and the specifications in Table 5.1-1; and insure that all the Timing Pulses meet the prescribed requirements. All Timing Pulses should be checked and adjusted in the order indicated in Table 5.1-1.

If any adjustments are made during the check, repeat the entire Timing Check.

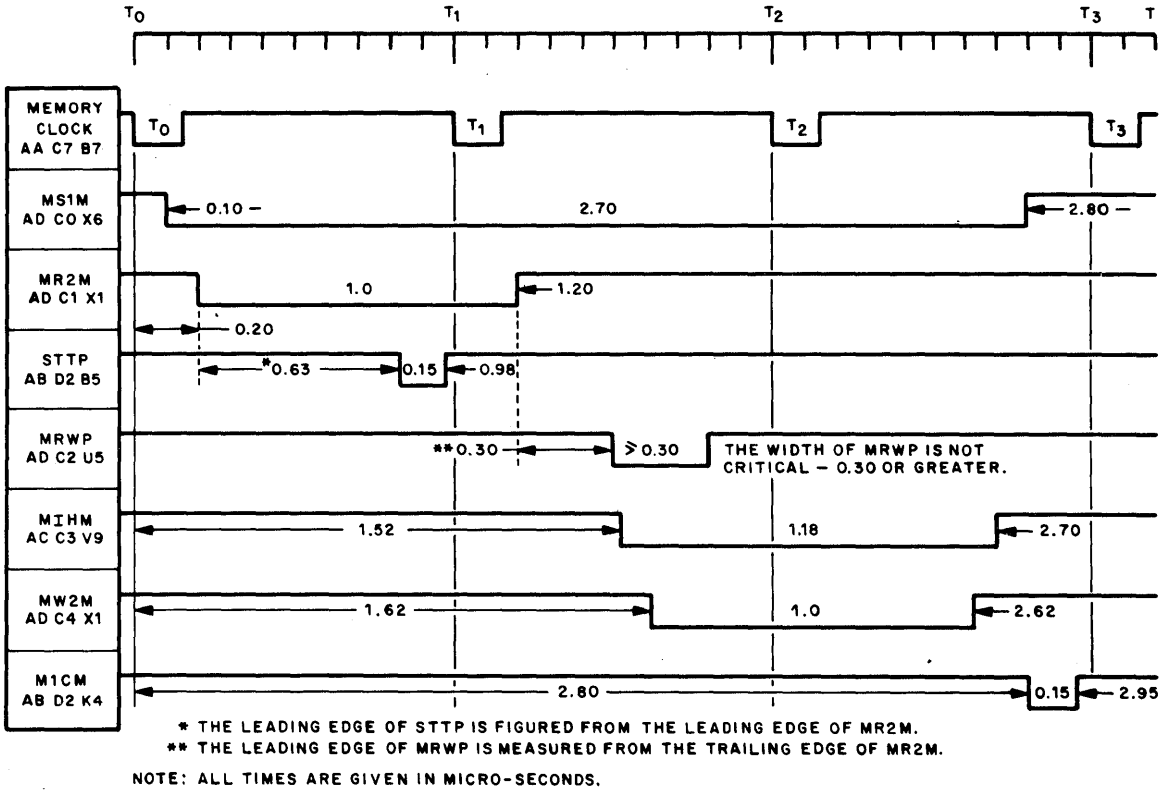


FIGURE 5.1-1
MULTI TRAIN TIMING

The three adjustments listed below are the only ones that will normally have to be changed.

MR2M - The adjustment on MR2M controls the Trailing Edge only. Verify that the Trailing Edge of MR2M falls at 1.20μs ±0.10μs from the Leading Edge of T_0. Insure that the width of MR2M is 1.0μs ±0.10μs.

MW2M - The adjustment of MW2M controls the Trailing Edge only. Verify that the Trailing Edge of MW2M falls at 2.62μs ±0.10μs from the Leading Edge of T_0. Insure that the width of MW2M is 1.0μs ±0.10μs.

STTP The adjustment on STTP controls the Start Time of the Strobe Multi. Verify that the Leading Edge of STTP is set to 0.63μs from the Leading Edge of MR2M.

5.2 VARIABLE CLOCK BIAS & CLOCK ADJUSTMENTS

Purpose

The purpose of the Variable Clock Bias is to prevent LOADING of the Clock Drive Transistors by decreasing unnecessary FALSE current.

Requirement

The Clock lines must have a FALSE level of -0.5V.

Adjustments

1. Connect a scope to AA C7 B7.
2. Adjust the potentiometer on AA C8 A2 to obtain a FALSE level of -0.5V.
3. Refer to Figures 5.2-1 and 5.2-2, and check the Clock pulses for amplitude and shape.

SEE PAGE 5.2-2

Remote Clock

1. The width of the Remote Clock is adjusted in Central Control at location EA D3 A2.
2. Monitor the Clock in the Memory Module at AA C7 B7.
3. Set the pulse width at the -2.0V level to .155 $^{\pm 0.015}\mu s$. The frequency should be one megacycle ±0.1 percent.

Local Clock

1. Adjust the Local Clock at the -2.0V level to a width of .155µs ±0.005µs.
2. Monitor the Clock in the Memory Module at AA C7 B7.
3. Adjust the width at the MUFW Multi at AA C6 A2.

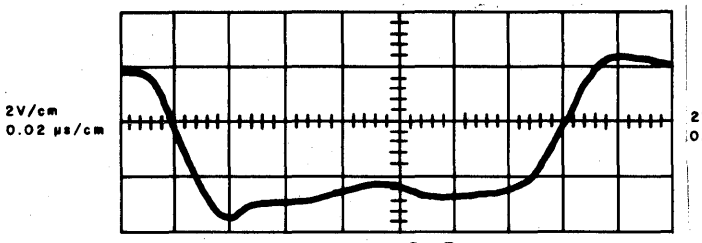


FIGURE 5.2-1
TYPICAL CLOCK PULSE
PANELS "A" & "B"

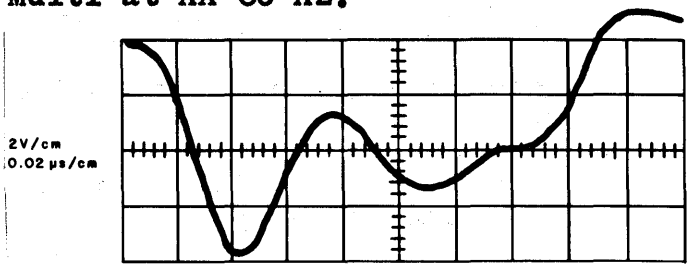


FIGURE 5.2-2
TYPICAL CLOCK PULSE
PANELS "C" & "D"

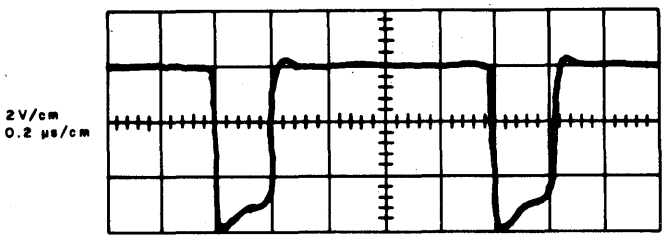


FIGURE 5.2-3
CLOCK PULSE SPACING FOR 1MC FREQUENCY

NOTE that the Clock pulses found on the "C" and "D" Panels of the Module are more distorted than the Clock pulses on the "A" and "B" Panels. This is due to the Clock pulses being coupled through interframe jumpers to the lower panels. See Figure 5.2-1 for typical Clock pulses found on Panels "A" and "B", and Figure 5.2-2 for typical pulses found on Panels "C" and "D".

5.3 REGULATED INPUT VOLTAGE ADJUSTMENTS

Vary each of the following voltages ±10 percent.

1. AA C0 A5 -1.2V
2. AA C0 A6 -12.0V
3. AA C0 A8 -4.5V

The ±10 percent voltage variation should light the proper indicators for each cabinet, voltage condition, and the voltage that failed.

Once all Regulators have been checked, insure that all voltages are returned to their proper value. It is recommended that a precision Voltmeter be used in setting these voltages.

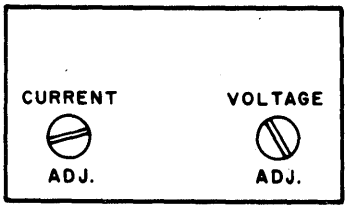
-12V Excess Current Adjustment

The -12V excess current adjustment (R35) will be set according to the number of Memory Modules in the Cabinet.

1. Turn R35 C.C.W. until Power drops.
2. Back off on the adjustment 1/2 turn for each Memory Module in the Cabinet from the trip point.

NOTE

Excess current sensing cannot be obtained with one Memory in the Cabinet. Therefore, turn R35 C.C.W. until a slight clicking can be felt. That is the end of the Pot. Back off on the adjustment 1/2 turn.



5.4 UNIT VOLTAGE REGULATOR ADJUSTMENTS

-15V Regulator

1. Monitor the output of the -15V Regulator at AC D4 B4.
2. Measure the temperature as closely as possible to the Core Stack.
3. Refer to the Graph in Figure 5.4-1 and adjust the -15V Regulator to its correct value for the existing Stack area temperature.

NOTE

The -15V Regulator is set to -15V with the Stack area temperature at 25° C.

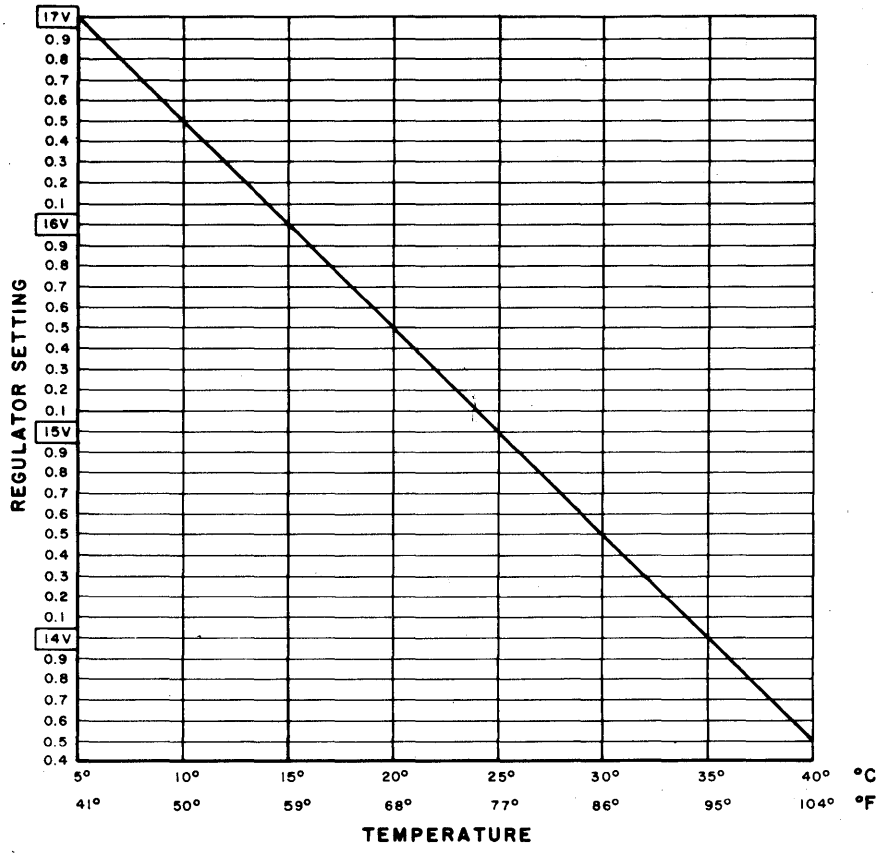


FIGURE 5.4-1
-15V TEMPERATURE VS. VOLTAGE

-30V "I" (INHIBIT) REGULATOR

1. Monitor the -30V "I" at the Test Point on the Display Panel.
2. Measure the temperature as closely as possible to the Core Stack.
3. Refer to the Graph in Figure 5.4-2 and adjust the -30V "I" to its correct value for the existing Stack area temperature.

NOTE

The -30V "I" Regulator is to be adjusted to -32V with the Stack area temperature at 25° C.

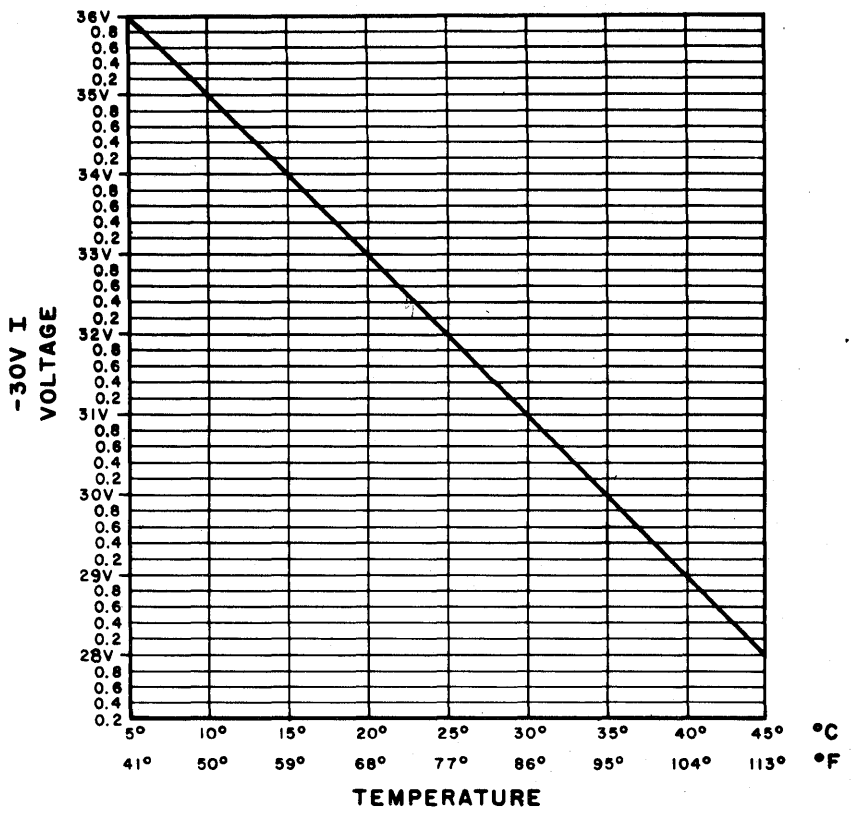


FIGURE 5.4-2
-30V "I" TEMPERATURE VS. VOLTAGE

-6T REGULATOR

1. The adjustment of the -6T Regulator at installation time is covered in Section 7.7 of this manual.
2. For Marginal Testing of the Regulator, See Section 6.6 of this manual.

3. If a new Core Stack is installed, see Section 5.7 of this manual for the -6T Regulator adjustment.

-30V "R" (Read) & "W" (Write) Regulators

1. The adjustment of the -30V "R" and "W" Regulators at installation time is covered in Section 7.9 of this manual.

2. For Marginal Testing of these Regulators, see Section 6.6 of this manual.

3. If a new Core Stack is installed, refer to Section 5.7 of this manual for the correct procedure to establish a new optimum setting for the -30V "R" & "W" Regulators.

TODM (Turn On Delay Multi) Adjustment

TODM should be TRUE for 30 milliseconds after DC is turned ON.

1. Monitor the output of TODM with an oscilloscope at AC D3 U0.

2. Set the TRIGGER MODE/SLOPE SWITCH on the oscilloscope to INTERNAL NEGATIVE.

3. Turn the Memory DC switch ON and verify that TODM remains TRUE for 30 milliseconds.

5.5 ASSEMBLY & DISASSEMBLY - MEMORY CORE STACK & TRANSFORMER BOARDS

General Information

This Section covers the description, orientation and location of the Memory Core Stack and associated items.

All orientation and location is described facing the PLUGGABLE SIDE of the Memory Unit gate.

The ends of the Core Stack are labeled TOP and BOTTOM. The TOP of the Stack faces to the left, toward the latch end of the gate. The BOTTOM of the Stack faces right, toward the hinge end of the gate.

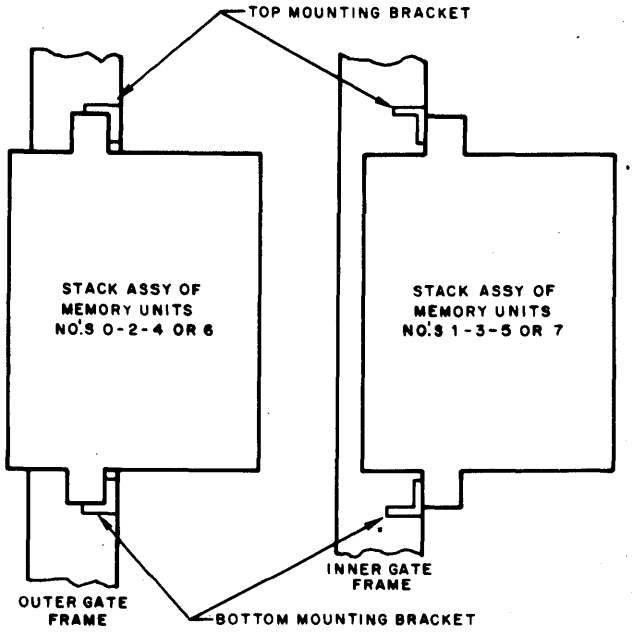


FIGURE 5.5-1
CORE STACK MOUNTING ASSEMBLY

Two Transformer boards are located on each side of the Stack. They are located with their components facing away from the Stack.

Each Transformer board is marked with the following information:

1. Assembly Number
2. Panel Letter (A,B,C or D)
3. TOP is marked on an edge to indicate proper orientation.

Each of the Transformer boards has a number of soldered leads which terminate in two types of connectors. The description and location of these connectors is as follows:

1. STICK TYPE TO BACKPLANE AREA

Each board utilizes 3 Stick-type Connectors. These sticks are to be installed in the backplane as shown in Table 5.5-1.

TABLE 5.5-1

BOARD ASSEMBLY	STICK J1	STICK J2	STICK J3
A	AD A1 L0	AD B1 L0	AD B1 Y0
B	AD A1 L1	AD A1 Y0	AD B1 Y1
C	AC A3 L9	AC A3 L8	AC A3 Y9
D	AC B3 Y8	AC B3 Y9	AC B3 L9

2. 9-PIN CONNECTORS TO THE CORE STACK

Each board uses eight 9-pin Connectors and each connector terminates 8 single conductor leads.

Four connectors on each board have short leads and are installed on the Stack end nearest the board. These connectors are marked M1, M2, M3 and M4.

There are also four connectors on each board with long leads which are installed on the Stack end farthest from the board location. These are marked N1, N2, N3 and N4.

With the "A" board to the left and facing the pluggable side of the gate, the connectors are installed on the Stack connectors in their order of breakout as follows:

a. "A" Board - Leads break out the front of the board.
   1. Connectors marked "M" install on the left front of Stack.
   2. Connectors marked "N" install on the right front of Stack.

b. "B" Board - Leads break out the rear of the board.
   1. Connectors marked "M" install on the left rear of the Stack.
   2. Connectors marked "N" install on the right rear of the Stack.

c. "C" Board - Leads break out the bottom of the board.
   1. Connectors marked "M" install to the bottom right of the Stack.
   2. Connectors marked "N" install to the bottom left of the Stack.

d. "D" Board - Leads break out the top of the board.
   1. Connectors marked "M" install to the top right of the Stack.

2. Connectors marked "N" install to the top left of the Stack.

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5.6 DISASSEMBLY & ASSEMBLY OF THE CORE STACK

The Core Stack can be removed without removing the Transformer Boards. Refer to Figure 5.6-3 for the Mechanical connections to the Core Stack.

Stack Disassembly

1. Remove the 32 "M" and "N" Connectors from the ends of the Stack. There are 16 connectors on each end of the Stack.
2. Remove the 13 Sense Connectors from the upper edge of the Core Stack. See Figure 5.6-1.

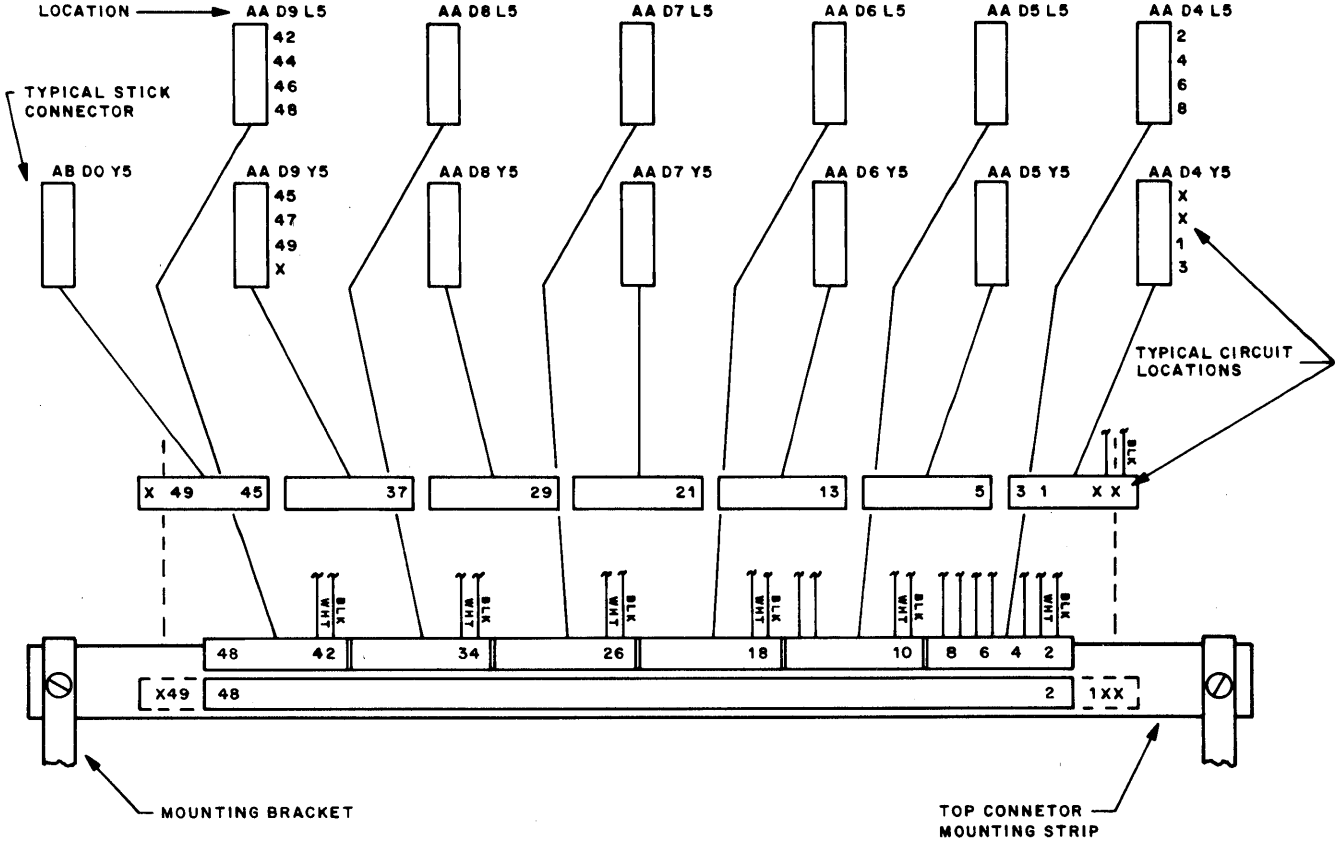

FIGURE 5.6-1
SENSE AMP AREA

3. Remove the 13 Inhibit Connectors from the lower edge of the Core Stack. See Figure 5.6-2.
4. Remove the eight #6-32 Hex Nuts and Washers from the four corners of the Stack Plates. See Item 3 in Figure 5.6-3.
5. With a man on each side of the gate, pull the plate away from the Stack (one corner at a time), to free the plate from the Stack bolts.

6. Remove the Stack by pulling it out toward the Wire Wrap side of the gate.

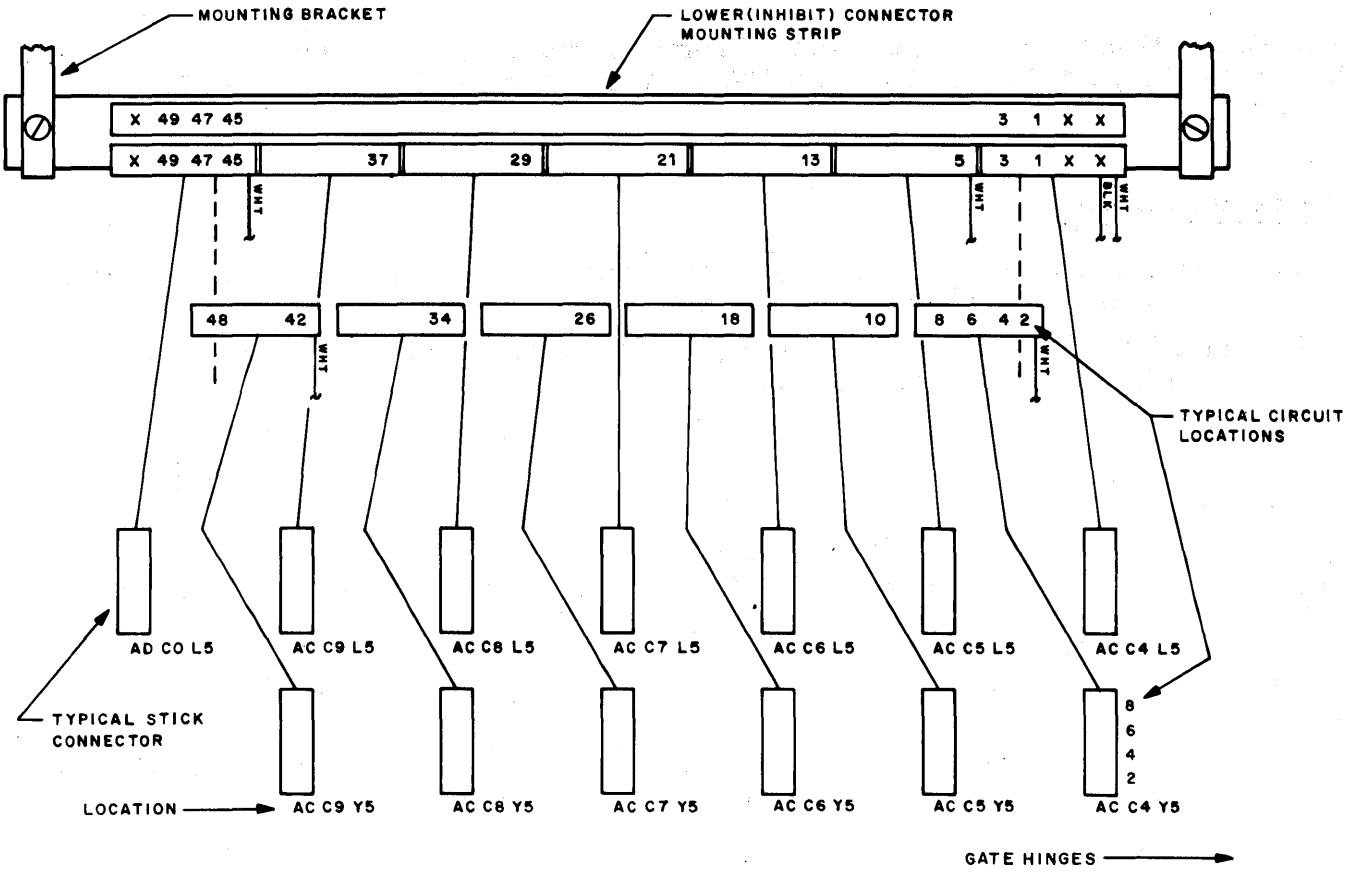

FIGURE 5.6-2
INHIBIT AREA

Stack Assembly

Reverse the above procedure.

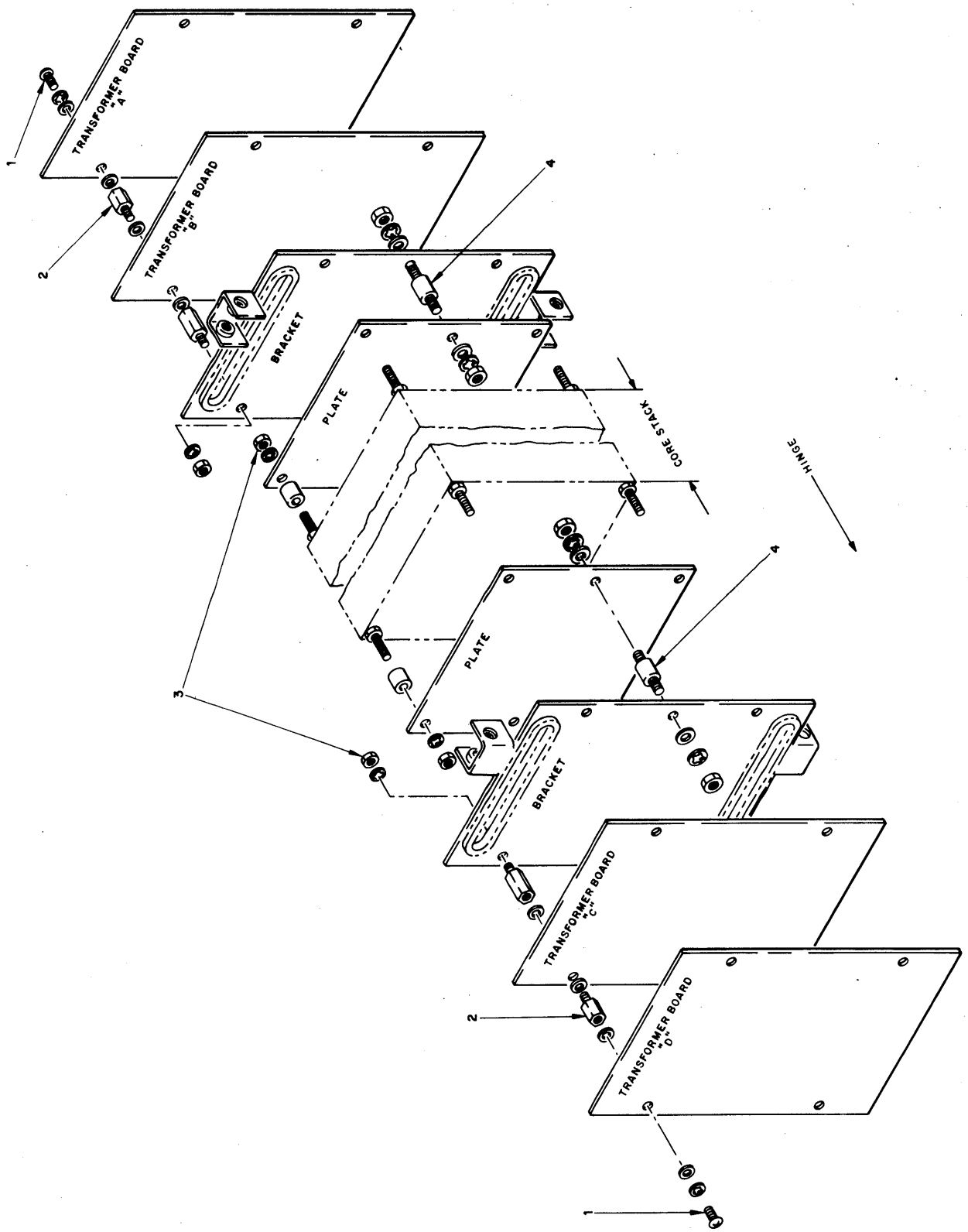

FIGURE 5.6-3
CORE STACK ASSEMBLY

5.7 OPTIMUM SETTINGS FOR -6T & -30V "R" & "W" REGULATORS

After the new Stack has been installed, it is necessary to determine new optimum settings for the -6T and -30V "R" and "W" Regulators.

NOTE

Strobe is set at 630ns, (RISD-1), from the Leading Edge of MR2M. The -30V Inhibit Regulator is set to -32V at 25°C. Refer to Section 5.4 for Temperature vs. Voltage compensation. The -12V should also be checked at the backplane and set to -12V at AA D0 B9.

The new optimum settings for the -6T and -30V "R" and "W" Regulators are determined by a SMHOO Plot. The plot is taken with Strobe and -30V "I" set as indicated in the above note. The variables of the plot are -6T and -30V "R" and "W".

The following procedure is a step by step outline on how to take a SMHOO Plot. See Figure 5.7-1.

1. Set -30V "R" and "W" to -29V.
2. Run the Checkerboard Normal True pattern and set -6T to a value where this pattern will run successfully.
3. Raise -6T until a failure occurs and plot this value on the graph.
4. Lower -6T until a failure occurs and plot this value on the graph.
5. Lower -30V "R" and "W" one volt.
6. Repeat Steps 3, 4 and 5 until Unit will not run the Checkerboard Normal True pattern at any setting of -6T.
7. Set -30V "R" and "W" to -30 volts.
8. Repeat Steps 3 and 4.
9. Raise -30V "R" and "W" one volt.
10. Repeat Steps 8 and 9 until Unit will not run the Checkerboard Normal True pattern at any value of -6T.
11. Refer to Figure 5.7-1 and connect all points on the graph.
12. Draw the largest possible circle inside of the graph lines without crossing any lines.

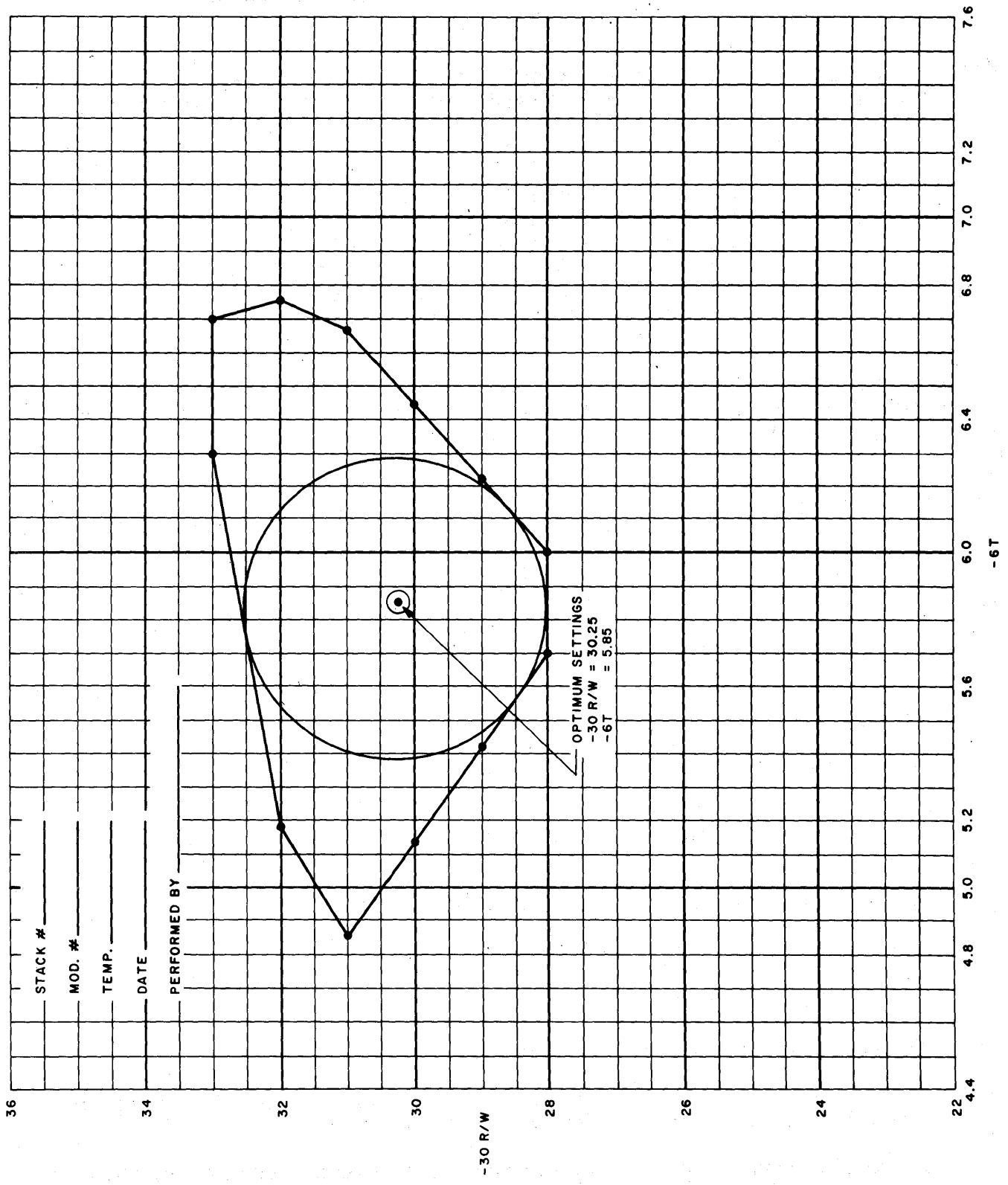

FIGURE 5.7-1
SMHOO PLOT CHART

13. Find the center of the circle and mark it. This mark will give the optimum value of the -30V "R" and "W" on the vertical axis and the optimum value of -6T on the horizontal axis.

14. Write these new optimum values on the tag attached to the front of the Unit and set Regulators accordingly.

15. Reference Section 6.6 and take -6T, -30V "R" "W" and "I" Regulators and Strobe margins as indicated.

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5.8 DISASSEMBLY & ASSEMBLY OF THE STACK TRANSFORMER BOARDS

There are two Transformer Boards located on each end of the Stack. The outer boards can be removed without disturbing the inner boards. If one of the inner boards is to be removed, then the outer board must also be removed. Refer to Figure 5.6-3.

Disassembly of Outer Transformer Board

1. Remove the eight "M" and "N" connectors that connect the board to the Stack.
2. Remove the three stick-type connectors that connect the board to the backplane. See Table 5.5-1.
3. Remove the Ground Lug connection that runs from the Transformer board to the backplane.
4. Remove the four #6-32 x 3/8" Phillips Head Screws from the four corners of the board. See Item 1 in Figure 5.6-3.

NOTE

There are 3 washers on each screw.
INSURE THAT NONE OF THESE WASHERS ARE
DROPPED INTO THE PACKAGES.

5. Lift out the Transformer Board.

Disassembly of Inner Transformer Board

1. Remove the outer Transformer board.
2. Remove the eight "M" and "N" connectors that connect the Transformer board to the Core Stack.
3. Remove the three stick-type connectors that connect the Transformer board to the backplane.
4. Remove the Ground Lug connection that runs from the Transformer board to the backplane.
5. Remove the four #6-32 Hex Standoffs from the four corners of the board. See Item 2 in Figure 5.6-3. Each Standoff has two nylon washers; one on each side of the board.
6. Lift out the Transformer board.

Assembly of Transformer Boards

Reverse the above procedure.

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PROCESSOR "A" | I/O SUBSYSTEM | POWER SUPPLY | DISPLAY & DISTRIBUTION | CENTRAL CONTROL | MEMORY SUB-SYSTEM 1 | MEMORY SUB-SYSTEM 2 | PROCESSOR "B"

POWER SUPPLY: DAL3B2 -19V; DAK2B2 -19V; O'HEAT POWER; +120V SW CONTROL; DAK9 (+74, +100V, -120V, LOGIC, -12VS, -24V AR, PØFL-2, PØFL-0, PØNL-2); DAK8 (+50V, -100V); DAK1 (+19V, -33V, +20V, -38V, -24V); DAM7B2 -19V; DAK5B2 -19V; DAL6B2 -19V; DAM4B2 -19V

CAJ101 -19V; CSK112 +20V; CTN201 -33V; CTN204 +50V

#205; #204; #198; #209; #208; #207; #206; #25-26; #25-23; #25-21; #25-22; #210; #25-25; #25-24; #25-29; #212; #25-28; #25-27; #25-37; #25-36; #25-9; #25-44; #25-41; #25-46; #25-47; #25-43; #25-42; #25-39; #25-38; #25-35; #25-32; #25-30; #25-31; #25-45; #25-33; #25-34; #27; #28

DJL1: O'HEAT POWER; 60~LOGIC; -12VS; -24V AR; +20V SW CONTROL; PØFL-0; PØFL-2; PØNL-2

DBJ4; DBK3; DBL3; DBK2; DBK1; DBJ3; DBJ2; DBL2; DBJ1; DBL1

CENTRAL CONTROL: DCL1 (POWER OFF; POWER INTERLOCK; POWER ON; -12V; POWER CONTROL COMMON; -24VB); #254 DC C0 A7 (A7⇒L7; A9⇒L9; A8⇒L8; A6⇒L6; A5⇒L5); #255 EC A0 N7 (N7⇒Y7; N9⇒Y9; N8⇒Y8; N5⇒Y5; N6⇒Y6)

DCL1: MASTER CLEAR; DC LOCKOUT

HAK2: #25-29A; -38V

HAJ1: #25-28A; #25-27A; -33V; +19V

HAJ2: #25-37A; #25-36A; #27A; -100V; +100V; MASTER CLEAR

HAJ3: #25-39A; #25-38A; #25-45A; #25-9A; #28A; -120V; -24V; +5C; +74 NOT USED; DC LOCKOUT

FIGURE 6.11-6
SYSTEM POWER CABLE ROUTING

INDEX - SECTION 6

6 MAINTENANCE - PROCEDURES & AIDS

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6.1 PREVENTIVE MAINTENANCE - WEEKLY

1. Check Fan operation.

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6.2 PREVENTIVE MAINTENANCE - MONTHLY

1. Check Air Filter and replace if necessary.
2. Clean Unit.

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6.3 PREVENTIVE MAINTENANCE - QUARTERLY

1. Verify margins as specified in Section 6.6 of this manual.
2. Verify Memory Timing (refer to Section 5.1).

6.4 PREVENTIVE MAINTENANCE - SEMI-ANNUALLY

Variable Clock Bias

1. The variable bias circuit associated with the Local Clock Driver (DRLC) shall be adjusted such that the false level of the output from the Local Clock Driver is 0.5V ±0.1V.

Remote Clock

The Remote Clock shall meet the following specifications:

1. Pulse Width: 155 nsec. ± 15 nsec.
2. Frequency: 1 Mc. within 0.1 percent.

Local Clock

The Local Clock shall meet the following specifications:

1. Insure the Memory Unit is in LOCAL Mode.
2. The width of the Local Clock Pulse (CCP) shall be adjusted to 155 nsec. ±5 nsec. by adjusting the MUFW Multi (AA C6 A2).
3. The frequency shall be: 1 Mc within 0.1 percent.

Lubricate all Blowers

1. Oil Injector ..... Part No. 11838588
2. Oil ..... Part No. 11838596

6.5 PREVENTIVE MAINTENANCE - ANNUALLY

Not applicable.

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6.6 MARGINAL TESTING

This Section should be used as specified in Section 6.3, when a large amount of Sense Amplifiers, Address Switches, Address Current Drivers, Inhibit Drivers or the Core Stack itself is replaced.

NOTE

It is recommended to wait approximately 5 minutes after the Sub-System covers are removed, or a Gate is opened to allow the Stack temperature to stabilize.

The marginal conditions specified here shall affect only the B461 Memory Modules. Upon completion of testing, these adjustments must be returned to normal.

Logic Margins

Each of the marginal conditions specified shall be tested individually while operating in the worse case Checkerboard True Mode (PCCL).

1. Set the output of the -12V Regulator to -11V.
2. Set the output of the -1.2V Regulator to -1.3V.
3. Adjust the output of IMCP to 140 nsec.

NOTE

When adjusting the Clock width in the LOCAL Mode, the Clock can be monitored at AA C7 B7 and adjusted at location AA C6 A2 (MUFW Multi).

4. Run Checkerboard True PCCL for 2 minutes.
5. Set the output of the -12V Regulator to -13V.
6. Set the output of the -1.2V Regulator to -1.1V.
7. Adjust the output of the IMCP to 170 nsec.
8. Run Checkerboard True PCCL for 2 minutes.

Strobe Margins

The Checkerboard True Normal pattern should be run when taking this margin. With all voltages set at their nominals, observe that the Strobe Timing Pulse has a minimum of 120 nsec total margin. The setting of the STTP (RISD-1) should be returned to 630 nsec from the Leading Edge of the MR2M Timing Pulse. It should be observed that there is at least 50 nsec margin on each side of the final Strobe setting.

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-30R,-30W,-30I & -6T Margins

With all voltages set at normal, except for the voltage on which the marginal adjustment is being made, observe that all voltages in Table 6.6-1 have the minimum stated total margins on any given tested pattern. Then determine that when all tested patterns are taken into consideration, a minimum total margin still exists for each voltage as indicated in Table 6.6-1.

NOTE

The nominal setting of -30R,-30W, -30I and -6T should be closely observed before any adjustment is undertaken. After each voltage is swung, it should be returned to this nominal setting.

TABLE 6.6-1

VOLTAGE	MINIMUM TOTAL MARGIN	
	ANY GIVEN PATTERN	INDEPENDENT OF PATTERN
-30R	4V	3.00V
-30W	3V	2.25V
-30I	6V	4.50V
-6T	1V	0.75V

The following Test Patterns are deemed necessary while performing the -30R,-30W,-30I and -6T Margins:

1. Checkerboard True
   a. PCCL
   b. Normal
2. Checkerboard Complement
   a. Normal
3. Uniform True
   a. PCCL

The above listed cycles and patterns are considered to be the most difficult and should provide the minimum operating margins. If any other test cycle and/or pattern is found which will not operate within these minimum margins, then that cycle and/or pattern should be used together with those given to determine actual minimums.

TABLE 6.6-2

PATTERN			HIGH				LOW				DELTA			
			-30R	-30W	-30I	-6T	-30R	-30W	-30I	-6T	-30R	-30W	-30I	-6T
CHKB	TRUE	NORM												
CHKB	COMP	NORM												
CHKB	TRUE	PCCL												
UNIF	TRUE	PCCL												

It is suggested that Table 6.6-2 be used to record margin results. By plotting the information in this way, the minimum total Margin Swing on any given pattern and the minimum total Margin Swing independent of pattern can be readily seen.

Again, it is emphasized that the VOLTAGES MUST BE RETURNED TO THE NOMINAL SETTINGS AFTER THE MARGIN TEST HAS BEEN COMPLETED.

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6.7 MAINTENANCE PANEL, SWITCHES & INDICATORS

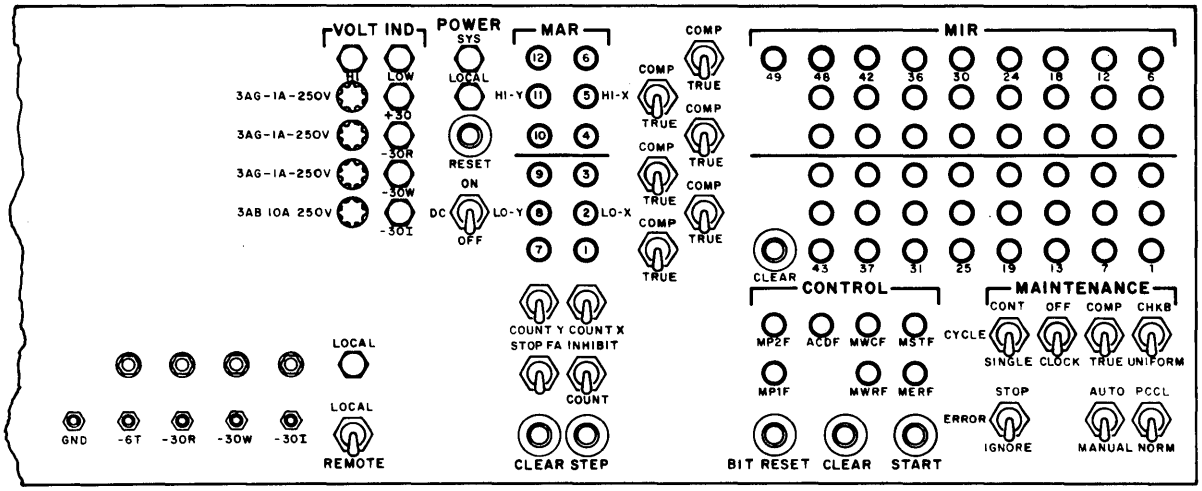


FIGURE 6.7-1
MAINTENANCE PANEL

The Local Mode testing facilities for the 4 μs Core Memory Module are provided by the Maintenance Test switches located on the Display Panel of the Memory Module.

The Address Register, Information Register and other logic flip-flops function normally during a Local Test Cycle; except that they are controlled manually or by the Maintenance Test switches instead of by the Interface provided by Central Control.

LOCAL/REMOTE Switch

This switch, when in the "down" position (Remote), with Power fully sequenced up, shall:

1. Cause the Memory Module to appear available to the B5500 System.
2. Disable the effects of all switches except Neon Power, Bit Reset, Address Register Clear, Information Register Clear, Flip-Flop pushbuttons, Power On/Off, and Power Reset.

In REMOTE, the Local Clock Driver responds to the clock pulse received from the Central Control, and the Memory Module responds to the Master Clear signal generated at the Console or Central Control Display Panel.

This switch, when in the "up" position (LOCAL), with Power fully sequenced up, shall:

1. Cause the Memory Module to appear "not available" to the B5500 System.
2. Enable the effects of all Maintenance Test switches.

The Local Clock Driver responds to the Clock pulse produced in the Memory Module and the Master Clear produced in the Central Control Unit has no effect in the Memory Module.

START Pushbutton Switch

This switch, when depressed, causes the Memory Start Level (MSTL) to be emitted.

STEP MAR Switch

When depressed, this switch causes the Address Plus One Level (A + 1L) to be emitted.

The A + 1L being emitted causes the Address Register to be incremented by one, providing the Count "X" and Count "Y" switches are in their normal "down" position.

STOP FINAL ADDRESS Switch

When in the "up" position, this switch causes the sensing for the maximum address the MAR Register is capable of holding (MAR equal to all ones). When the Maintenance Operation (dependent on the Maintenance Test Operation selected by the operator) on the last address has been completed, all cycling will halt.

COUNT/INHIBIT Count of MAR Switch

When in the normal "down" position, this switch allows the MAR Register to be incremented after each Maintenance Operation has been completed; providing the COUNT "X" and COUNT "Y" switches are in their normal "down" positions.

This switch, when in the "up" position, inhibits the Mar Register from being incremented; except for the depression of the STEP MAR pushbutton.

COUNT "X" Axis Switch

When in the normal "down" position, this switch allows the counting through and/or selection of all the "X" axis drive lines of the Core Memory Stack.

This switch, when in the "up" position, inhibits the counting through and/or selection of all the "X" axis drive lines of the Core Memory Stack and does allow an operator to manually set the MAR flip-flops A01F, A02F, A03F, A04F, A05F and A06F; to select a particular "X" axis drive line of the Core Memory Stack. The switch also allows the counting through and/or selection of all the "Y" axis drive lines (providing

the COUNT "Y" axis switch is in its normal "down" position) while sequencing this one "X" axis drive line.

COUNT "Y" Axis Switch

When it the normal "down" position, this switch allows the counting through and/or selection of all the "Y" axis drive lines of the Core Memory Stack.

This switch, when in the "up" position, inhibits the counting through and/or selection of all the "Y" axis drive lines of the Core Memory Stack and does allow an operator to manually set the MAR flip-flops A07F, A08F, A09F, A10F, A11F and A12F; to select a particular "Y" axis drive line of the Core Memory Stack while counting through and/or selecting all the drive lines of the "X" axis (providing the COUNT "X" axis switch is "down").

STOP/IGNORE ERROR Switch

When in the normal "down" position, this switch allows the Maintenance Test cycles to continue, despite the fact that an ERROR has occurred during operation.

This switch, when in the "up" position, cause all cycling to halt (at the completion of that cycle should an ERROR occur during the Maintenance Test operations. The Address and Information in which the ERROR occurred are displayed.

CONTINUOUS/SINGLE CYCLE Switch

When in the normal "down" position, this switch allows one Memory cycle to take place. In certain modes of Maintenance Test operations, it is necessary to depress the START pushbutton as many as four (4) times in order to complete one Maintenance Test operation when in SINGLE CYCLE.

This switch, when in the "up" position, allows Memory cycles to occur without stopping; providing no ERROR occurs and Unit is not cycling into or out of the last Address of the Stack while Sensing for these conditions to exist.

COMPLEMENT/TRUE Word Switch

This switch, when in its normal "down" position and all bit switches are in their normal "down" positions, allows a "one" to be stored in each of the 49 bits of a word.

When in the "up" position, this switch allows the opposite state ("1" or "0") to be stored in bit locations of a word as selected by the positions of the bit switches.

COMPLEMENT/TRUE 1s Bit

When in the normal "down" position, and the Word switch is in its normal "down" position, this switch allows a "one" to be stored in each of the following 1s bit locations: 1, 7, 13, 19, 25, 31, 37 and 43.

This switch when in the "up" position, allows the opposite state ("1" or "0") to be stored in the 1s bits of a word as selected by the position of the Word switch.

COMPLEMENT/TRUE 2s Bit

This switch, when in the normal "down" position and the Word switch is in its normal "down" position, allows a "one" to be stored in each of the following 2s bits locations: 2, 8, 14, 20, 26, 32, 38 and 44.

This switch, when in the "up" position, allows the opposite state ("1" or "0") to be stored in the 2s bits of a word as selected by the position of the Word switch.

COMPLEMENT/TRUE 4s Bit

This switch, when in its normal "down" position and the Word switch is in its normal "down" position, allows a "one" to be stored in each of the following 4s bit locations: 3, 9, 15, 21, 27, 33, 39 and 45.

When in the "up" position, this switch allows the opposite state ("1" or "0") to be stored in the 4s bits of a word as selected by the position of the Word switch.

COMPLEMENT/TRUE 8s Bit

This switch, when in its normal "down" position and the Word switch is in its normal "down" position, allows a "one" to be stored in each of the following 8s bit locations: 4, 10, 16, 22, 28, 34, 40 and 46.

When in its "up" position, this switch allows the opposite state ("1" or "0") to be stored in the 8s bits of a word as selected by the position of the Word switch.

COMPLEMENT/TRUE As Bit

This switch, when in the normal "down" position and the Word switch is in its normal "down" position, allows a "one" to be stored in each of the As bits locations as follows: 5, 11, 17, 23, 29, 35, 41 and 47.

When in the "up" position, this switch allows the opposite state ("1" or "0") to be stored in the As bits of a word as selected by the position of the Word switch.

COMPLEMENT/TRUE Bs Bit

This switch, when in the normal "down" position and the Word switch is in its normal "down" position, allows a "one" to be stored in each of the following Bs bit locations: 6, 12, 18, 24, 30, 36, 42, 48 and 49.

When in the "up" position, this switch allows the opposite state ("1" or "0") to be stored in the Bs bits of a word as selected by the position of the Word switch.

CHECKERBOARD/UNIFORM Mode

This switch, when in the normal "down" position, activates the Automatic/Manual Mode switch. Depending upon the position of the Automatic/Manual Mode switch, the mode of Maintenance Test operation to be performed is said to be either UNIFORM MANUAL or UNIFORM AUTOMATIC.

When in the "up" position, this switch disables the Automatic/Manual mode switch and the mode of Maintenance Test operation to be performed is said to be CHECKERBOARD.

AUTOMATIC/MANUAL Mode

This switch is only active when the CHECKERBOARD/UNIFORM mode switch is in its normal "down" position. When it is active and in the normal "down" position, the mode of Maintenance Test operation to be performed is said to be UNIFORM MANUAL.

When this switch is active and in the "up" position, the mode of Maintenance Test operation to be performed is said to be UNIFORM AUTOMATIC.

PATTERN COMPLEMENT/NORMAL CYCLE

This switch is only active in the UNIFORM AUTOMATIC and CHECKERBOARD modes.

When it is active and in the normal "down" position, a two Memory cycle Maintenance Test operation is allowed to take place on each Address location of the Stack. A READ Memory cycle is followed by a WRITE Memory cycle. The pattern to be read and written into Memory is the NORMAL test pattern which is determined by the mode of test operation being performed.

When this switch is active and in the "up" position, a four Memory cycle Maintenance Test operation is allowed to take place on each Address location of the Stack. A NORMAL READ Memory cycle is followed by a COMPLEMENT WRITE which is followed by a COMPLEMENT READ which is followed by a NORMAL WRITE Memory cycle. The patterns to be read and written into Memory are the NORMAL test pattern and the COMPLEMENT of the NORMAL test pattern, which is determined by the mode of test operation being performed.

Controls and Displays

1. SWITCHES - POWER ASSOCIATED - When the Memory Module is operated in conjunction with the System (On-Line), the initial sequencing of Power shall be controlled by the B5370 Power Supply. The normal sequencing of System Supplies takes place, including the LOCAL Regulators in each Memory Module Cabinet. When the last voltage is sequenced ON by the System (+100), each individual Memory Module will Sense this and sequence its own special Supplies.

   System Power cannot be turned OFF from a Memory Module, except in the case of a special voltage Power Failure being detected in that Module. In this case, the DC Lockout line is grounded in the Module detecting failure.

   When the Memory Module is operated in LOCAL Testing Modes (Off-Line), its Power may be sequenced independently of System Power Supply. This is done by means of the Power ON/OFF switch in the Memory Module. The Power ON/OFF switch controls a series of relays (K1, K2, K3 and K4) in the Memory Module.

2. POWER RESET - This switch should be pressed only momentarily because all Power Failure Sensing circuits are Inhibited while this switch is depressed.

3. POWER LIGHTS - Both the LOCAL and SYSTEM Power lights should be ON when Power is completely sequenced ON. The SYSTEM Power light gets power from +100V. The LOCAL light should come ON when -30VI sequences ON. The LOCAL light should be OFF with a loss of LOCAL Power.

4. LIGHTS - All lights shall correctly display the state of associated flip-flop, Power state, and/or LOCAL/REMOTE status which they are intended to display. This includes lighting for the appropriate state as well as extinguishing for the opposite state.

5. CLOCK CONTROL - The STOP CLOCK switch in the OFF position stops all Clock pulses when the Memory Module is in LOCAL. This provides for static checking of logical areas when it is helpful to have all Clock pulses disabled.

6.8 FERRITE MEMORY CORE CHARACTERISTICS

Introduction

The purpose of this section is to provide a general knowledge concerning core characteristics that should prove helpful for a better understanding of the B461 Memory Unit and its Maintenance Panel operation. Before this section is studied, it is suggested that the reader have a good understanding of basic core theory presented in Section 3.

In the past, the testing of a Core Memory Unit has been limited to the following characteristics:

1. Switching Time (t_s)
2. Peaking Time (t_p)
3. "One" output signal (uV_1 or dV_1)
4. "Zero" output signal (dV_z)

These characteristics are important. However, they are not the only core properties of importance to be considered. As the speeds of the Memory Systems increase, the secondary core characteristics become increasingly important too; and can make the difference between the success or failure of a Memory System.

In this section, the primary and secondary core characteristics will be explained to show how they relate to the overall performance of a completed Memory Unit. The procedures that involve the generation of information patterns which create the core signal and noise conditions for a Memory Unit will be examined.

The major portion of the material used in this section has been condensed from the Engineering Technical Report No. 20, Electrodata M & E Division.

GLOSSARY OF CORE TERMS & DEFINITIONS USED IN THIS SECTION

Current Pulse Logic Terms

These terms describe the logic function of a current pulse. When the letter n or t is used as a prefix (as in nI_w or tI_n), they refer to nominal (n) or test (t) current magnitude for the core or array under consideration.

I_w - Write Current: a current pulse in the positive sense, of sufficient magnitude to fully switch a core from the "zero" state to the "one" state.

I_{pw} - Partial Write Current: a current pulse in the positive sense, but of insufficient magnitude to cause appreciable flux switching. This is nominally $\frac{I_w}{2}$ in magnitude (half-select current).

I_r - Read Current: a current pulse in the negative sense, of sufficient magnitude to fully switch a core from the "one" to the "zero" state.

I_{pr} - Partial Read Current: a current pulse in the negative sense, but of insufficient magnitude to cause appreciable flux switching. This is nominally $\frac{I_r}{2}$ in magnitude (half-select current).

I_i - Inhibit Current: a current pulse in the negative sense which is not of sufficient magnitude to cause appreciable flux switching, but is large enough to partially cancel an I_w and prevent flux switching. This is used to write "zero".

I_x - X Current: the current in an X selection line - normally an I_{pw} or an I_{pr}.

I_y - Y Current: the current in a Y selection line - normally an I_{pw} or an I_{pr}.

I_z - Z Current (Inhibit Current): the current pulse in the Z axis wire of a core plane. This line is also called the Inhibit line.

I_f - Full Current: the magnitude of the sum of the I_x and I_y currents in a Memory Plane.

Core Disturb States

These terms describe the quasi-stable states of disturbance which a core can encounter when being operated with normal drive currents.

uz - Undisturbed Zero: the pure "zero" state reached by subjecting a core to an I_r pulse.

dz - Disturbed Zero: the state reached by first setting a core to the uz state and then subjecting it to a long train of I_{pw} pulses.

wz - Write Disturbed Zero: the state reached by setting the core to the uz state and then subjecting it to a train of alternating I_{pr} - I_{pw} pulses, the last pulse being an I_{pw}.

rz - Read Disturbed Zero: a state reached by setting a core to the wz state when driving it with an I_{pr} pulse. When subjected to the I_{pr} - I_{pw} sequences of pulses, the core will cycle between the rz and wz states on a stable minor loop.

ul - Undisturbed "One": the pure "one" state reached by subjecting the core to an I_w pulse.

dl - Disturbed "One": the state reached by first setting a core to the ul state and then subjecting it to a long train of I_{pr} or I_i pulses.

wl - Write Disturbed "One": the state reached by setting a core to the ul state and then subjecting it to a long train of alternating I_{pr} - I_{pw} pulse pairs.

rl - Read Disturbed "One": the state reached by setting a core to the wl state and then driving it with an I_{pr} pulse. When subjected to the I_{pr} - I_{pw} pulse pair sequence, the core will cycle between the rl and wl states on a stable minor loop.

Primary Core Signal Characteristics

uV_1 - Undisturbed "One" Voltage: the signal generated when a core is driven from the ul state to the uz state by an I_r pulse.

dV_1 - Disturbed "One" Voltage: the signal generated when a core is driven from the dl state to the uz state by an I_r pulse.

dV_z - Disturbed "Zero" Voltage: the signal generated when a core is driven from the dz state to the uz state by an I_r pulse.

t_s - "One" Switching Time: the time between the 10 percent point of the I_r pulse and the second 10 percent point of a "one" output signal (uV_1 or dV_1).

t_p - "One" Peaking Time: the time between the 10 percent point of the I_r pulse and the peak of the "one" output signal (uV_1 or dV_1).

Secondary Core Signals

These terms describe signals generated when a core is subjected to an I_{pr} pulse after being set to different disturb states.

uV_{hz} - Undisturbed "Zero" Half-Select Signal: the signal generated when a core in the uz state is driven by an I_{pr} pulse.

wV_{hz} - Write Disturbed "Zero" Half-Select Signal: the signal generated when a core in the wz state is driven by an I_{pr} pulse.

rV_{hz} - Read Disturbed "Zero" Half-Select Signal: the signal generated when a core in the rz state is driven by an I_{pr} pulse.

dV_{hz} - Disturbed "Zero" Half-Select Signal: the signal generated when a core in the dz state is driven by an I_{pr} pulse.

uV_{hl} - Undisturbed "One" Half-Select Signal: the signal generated when a core in the ul state is driven by an I_{pr} pulse.

dV_{hl} - Disturbed "One" Half-Select Signal: the signal generated when a core in the dl state is driven by an I_{pr} pulse.

wV_{hl} - Write Disturbed "One" Half-Select Signal: the signal generated when a core in the wl state is driven by an I_{pr} pulse.

rV_{hl} - Read Disturbed "One" Half-Select Signal: the signal generated when a core in the rl state is driven by an I_{pr} pulse.

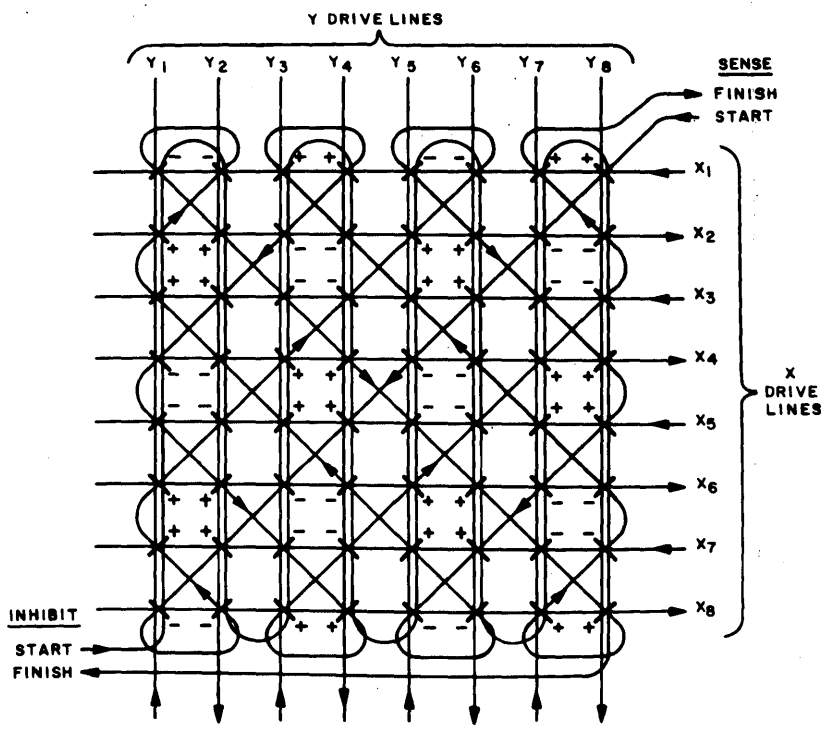
V_{hs} - Core Half-Select Signal: the generalized term for the signal generated when a core is driven by a half-select current (I_{pr}, I_{pw}, or I_i).

Memory Array Configuration

To understand the significance of core characteristics, it is first necessary to consider the completed core plane. Figure 6.8-1 shows the wiring of a typical coincident current Memory plane with diagonal sense winding. The 8 x 8 plane shown contains four sets of wires: 8 "X" and 8 "Y" selection wires, each threading 8 cores in a given row or column; an Inhibit wire threading all cores in the same phase as the "X" and "Y" wires; and a Sense wire threading half the cores in phase with the Inhibit winding and the other half in the opposite phase to the Inhibit wire.

To select an Address, one "X" and one "Y" wire are driven with a half-select current in such a direction that they add up in phase in the core at the intersection of the wires.

When the "X" and "Y" wires are driven, voltages are induced into the Sense wire by the cores on the selected "X" and "Y" wires. One of these cores is full-selected and the others are half-selected.



NOTE: ARROWS SHOW POSITIVE CURRENT FLOW. SIGNS SHOW PHASING OF CORE AND SENSE LINE RELATIVE TO DRIVE LINES.

FIGURE 6.8-1
8 x 8 MEMORY PLANE

In the case of the 8 x 8 example, 14 half-selected cores are involved. For any array with dimension N by N, there are 2N-2 half-selected cores. Of these, N cores are in one phase and N-2 cores are in the opposite phase. This can be seen by examining Figure 6.8-1, and counting cores along any line. Because of this phase cancellation, the net resulting signal is a function of the magnitude of the plus and minus signals which are in turn a function of the prior magnetic history of the cores involved. This is discussed in detail later (Secondary Core Characteristics).

Another array property which is of considerable interest is the Inhibit noise. This is the noise which is induced into the Sense winding when the Inhibit line is driven. There are N cores (all of the cores in the plane) involved in producing the Inhibit noise. Again, as in the "X" and "Y" drive, there is a measure of cancellation of the signals induced by the Inhibit current. Half of the signals will be plus, and the other half will be minus. The resulting signal depends upon the degree of cancellation which in turn depends upon the magnetic history of the cores.

The last characteristic of the array which will be considered in this section is the drive line impedance, and the resultant power required to drive the line with a given rise time. This is determined by half-select inductance of the individual cores and the inductance and resistance of the wire on which the cores are strung.

Primary Core Characteristics

The characteristics of a core which are most commonly tested for are referred to here as the Primary Characteristics. They are as follows:

1. Switching Time (t_s)
2. Peaking Time (t_p)
3. "One" Output Signal (uV_1)
4. "Zero" Output Signal (dV_z)

A core is normally thought to have only two stable states of magnetization. This is only partly true. An examination of the core hysteresis loop presented in Figure 6.8-2 shows that within the two major states, "one" and "zero", there are minor variations in magnetization which are determined by the sequence of half-select current pulses to which the core is subjected.

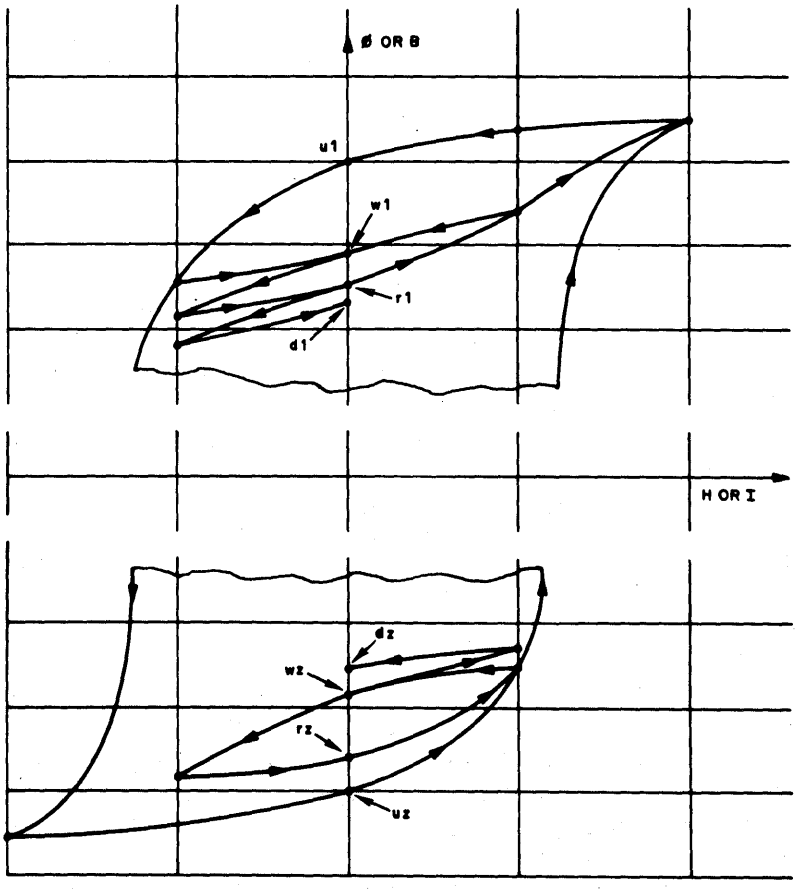


FIGURE 6.8-2
MINOR HYSTERESIS LOOPS OF MEMORY CORE

The first states are the pure undisturbed "one" and "zero" states, ul and uz. The next states are the maximally disturbed states for a given magnitude of half-select current. These states, dl and dz, are reached by subjecting the core (first set to the ul or uz state) to a long burst of half-select pulses in the direction to switch flux in the core. The other disturb states are reached by subjecting a core in the ul or uz state to a series of plus - minus half-select current pairs. The core will stabilize on a minor loop and shuttle back and forth between the rl and wl or rz and wz states.

Figure 6.8-3 shows the core output signals and their characteristics.

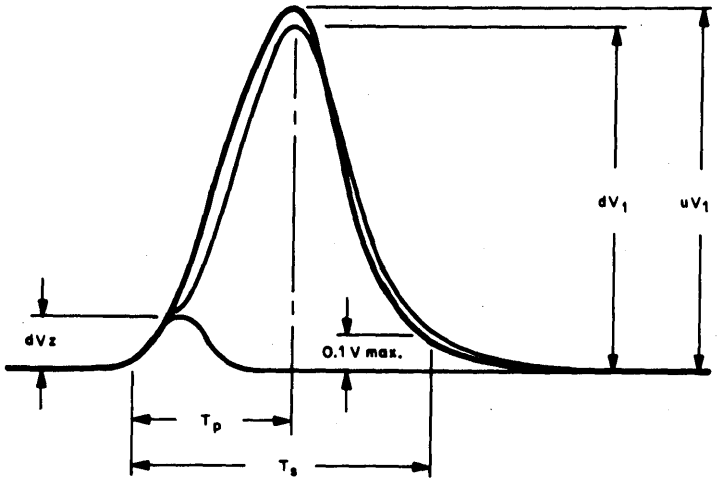


FIGURE 6.8-3
PRIMARY CORE SIGNAL CHARACTERISTICS

The signals depend on the initial state of the core. The pulse pattern used to generate these signals is shown in Figure 6.8-4. It can be seen that the disturbed signals, dV_1 and dV_Z, are reached by reading a core which has been set to the dl or dz state. The difference between the ul and dl or the uz and dz states is used as one test of the quality of a core. The less difference, the better the core. To determine how these primary characteristics relate to a core in an operating Memory System, we should examine the current patterns used in a system.

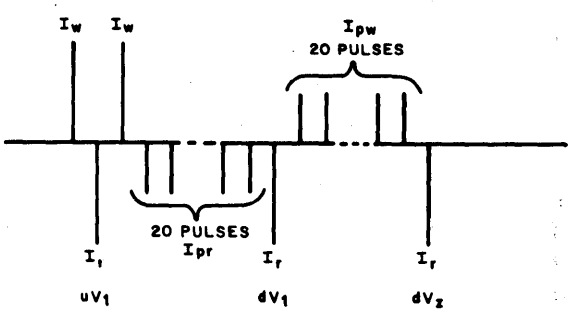


FIGURE 6.8-4
TEST CURRENT PATTERN

The "X" and "Y" drive currents (see Figure 6.8-5) consist of alternating pairs of half-select current pulses, Read (-) and Write (+). The Inhibit consists of a pulse in the Read (-) direction, coming at Write time.

From this, it can be seen that a core can be subjected to several current pulse patterns:

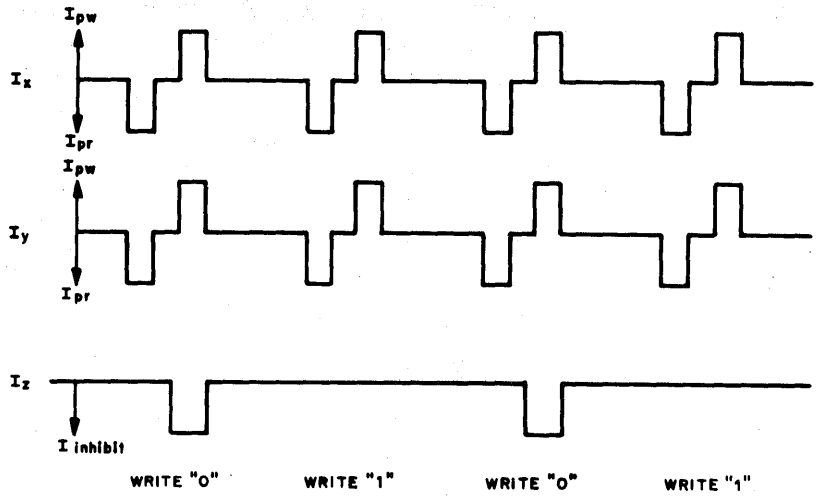


FIGURE 6.8-5
OPERATING CURRENT PATTERNS

1. A string of alternating minus and plus currents, when all "ones" are being written and the core is in one of the selected "X" or "Y" lines (Uniform True Normal "all ones").
2. A string of minus currents when "zeros" are being written and a core is NOT in one of the selected "X" or "Y" lines (Uniform Complement Normal "all zeros").
3. Various combinations of these two basic patterns, depending upon the Information pattern and the location of the core.

Comparing these patterns with those used in core testing (Figure 6.8-4), it can be seen that the pattern used for the dV_1 (Figure 6.8-3) test is actually encountered in operation. The pattern used to generate the dV_Z test can never exist in a normal Memory operation. Therefore, the dV_Z normally talked about is never encountered.

Under certain conditions of current misadjustment, it can be approached. This is the case when the half-select Write current (I_{pw}) is higher than nominal; and the half-select Read current (I_{pr}) is lower than nominal. The disturb pulse pair is then asymmetrical and can walk a "zero" up to the loop toward the disturbed "zero" (dz) state. Normally, however, it will move between the wz state and rz state. The use of this test can be justified primarily on the grounds that it is a sensitive test for the quality of a core. The next section of this test will show that even if the dV_Z was a legitimate operating parameter, it would be completely masked by other signals.

The Time tests (t_p and t_s) are straightforward, and are only slightly affected by the magnetic history of the core. The t_s is usually slightly longer for a dV_1 than for a uV_1. This is contrary to what one would guess, since more flux is switched in a uV_1 and should therefore take longer. The explanation probably lies in the distribution of the flux in the two states.

Secondary Core Characteristics

The primary characteristics previously described are responsible for the signals desired to indicate the stored information. The secondary characteristics on the other hand, create the signals which are NOT desired, and in general, create the bulk of the problems usually encountered in a Core Memory.

The secondary characteristics discussed here are all based on the half-select signal; that is, the voltage produced when a core is given a half-select current.

When a core is driven by a half-select current, a voltage is induced on any wires linking the core. The magnitude of this voltage depends on the state of the core ("one" or "zero") and its magnetic history. For each state of the core, there are four possible stable conditions of disturbances. Refer to Figure 6.8-2 and description given in previous text.

The half-select voltage which is induced in the Sense line is determined by the flux change which results from a Read half-select current. An examination of the hysteresis loops traversed by the core will give some insight into the voltages to be expected.

The flux changes consist of two components: reversible flux, and irreversible flux. From two of the four disturb conditions of each state of the core, there is a significant irreversible flux component. For a "one", the ul and wl states will produce an irreversible flux change when read half-selected. Since the dl and rl states are stable states for most cores, only a reversible flux component is generated. The signals, in order of magnitude, are: uV_{hl}, wV_{hl}, rV_{hl}, and dV_{hl}. The Glossary gives an explanation of the Read voltage symbol notation.

In a similar manner, the "zero" half-select signals differ, depending on the disturb state. The signals in order of decreasing magnitude are: dV_{hz}, wV_{hz}, rV_{hz}, and uV_{hz}. It should be noted that the order is reversed from that of the "one" signals. Examination of the hysteresis loops will reveal nothing about the relative magnitude of the "one" and "zero" half-select signals. However, one can make a good guess that the "one" half-select signals on the average, are larger than the "zero" half-select signals.

Memory Array Characteristics

As was explained earlier (see Memory Array Configuration, Page 6.8-5), the Read output signal is a composite of the signal outputs from one selected core and the 2N-2 half-selected cores. The maximum noise is obtained when the plus phase cores have a larger (or smaller) half-select signal than the minus phase cores. For testing purposes, this pattern is simulated by writing "ones" in all of the plus phase cores and "zeros" in the minus phase cores. For the diagonal Sense winding shown in Figure 6.8-1, this pattern is called the CHECKERBOARD pattern.

The amplitude difference between a "one" half-select signal and a "zero" half-select signal is called the Delta noise (V_0) for a core. There are several possible V_0 conditions for a core depending upon the disturb state of the cores involved. The largest V_0 is $uV_{hl} - uV_{hz}$. However, this is not a V_0 that can easily be generated in a complete plane test, or in normal operation.

The CHECKERBOARD pattern is normally generated for testing purposes by cycling through the Memory and writing "ones" and "zeros" in the proper locations. In the process N^2 2, Inhibit pulses are generated. These Inhibit pulses are in the Read direction and will set all "ones" to the dl state, and all "zeros" to the uz state.

Another Delta noise which is of some interest is intermediate in amplitude between the two listed. This is achieved by setting all "ones" to the wl state and all "zeros" to the uz state. The resultant V_0 is $wV_{hl} - uV_{hz}$. This pattern will not be generated in a NORMAL CHECKERBOARD test, but it can be achieved by programming. This is accomplished by first setting in the Checkerboard, leaving the cores in the dl and uz states. Next, other locations are Addressed so that all of the "ones" in a given row and column are given a Read/Write pair. This amounts to moving along a diagonal in the Memory plane writing "ones". The selected Address is then Read.

The combination of the signal from the full selected core and the 2N -2 half-selected cores can take several forms under test. When all "ones" are written, the V0 is "zero" and the "one" can be either plus or minus, depending upon the location.

When all "zeros" are written, the V_0 is also zero, and the "zero" signal can be plus or minus.

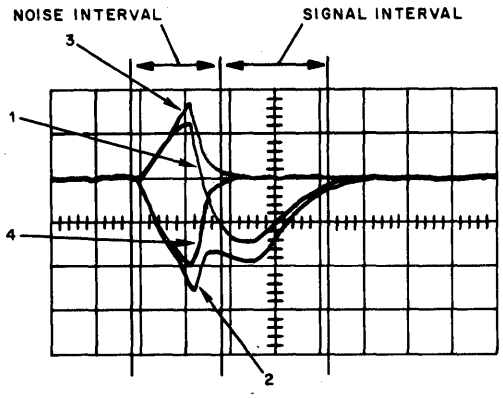
With the Checkerboard pattern written with "ones" in plus locations and "zeros" in minus locations, the "one" signal and the V_0 will be plus. In this case, the V_0 adds to the "one" signal. The "zero" signal will be minus, thus subtracting from the plus V_0. It can be seen that neither of these will be a worse case test.

To achieve a worse case condition, it is necessary to insert a bit into a location inverse to that which the Checkerboard indicates. This results in a negative "one" with positive V_0 and a positive "zero" with positive V_0. (Checkerboard True PCCL)

Figure 6.8-6 shows an oscillogram of the four combinations just discussed:

1. Negative "one" with positive V_0
2. Negative "one" with negative V_0
3. Negative "zero" with positive V_0
4. Negative "zero" with negative V_0

It can be seen that the V_0 can reduce significantly the amplitude of the "one" in the worse case situation.



FOUR TRACES SHOWING POSITIVE AND NEGATIVE CHECKERBOARD WITH NEGATIVE "ONE" AND "ZERO."

FIGURE 6.8-6
CORE PLANE CHECKERBOARD NOISE

Other characteristics of the array which are controlled by the core half-select characteristics are the Inhibit noise, Inhibit drive inductance, and the "X" and "Y" drive inductance. The Inhibit noise is the voltage in the Sense line which results from a current in the Inhibit line. Since there is a signal cancellation between the N^2 cores which link the two wires, the noise is a function of the Information state and the V_0 for the cores. In this case, there are $N^2 \div 2$ core pairs contributing noise voltages. When all cores are set to the same state, the only noise is that which is caused by a slight nonconformity of core characteristics or, a slight unbalance of the air coupling between the windings. This noise is generally much less than a "one" signal and can therefore be ignored.

When the cores are set to the Checkerboard pattern, the situation is quite different. The $N^2 \div 2$ V_{0s} create quite a healthy signal which can be over 10 times a normal "one" signal. This large signal can cause problems in the recovery of the Sensing system from one Write cycle and force the delaying of the next Read cycle. In this case, the bulk of the "ones" in the Checkerboard will be in the dl state and the "zeros" will be in the uz state.

The Inhibit drive impedance consists of the core and wire inductance, and the wire resistance. In the worse case, the core inductance is that of a core in the dl state. The wire inductance is a function of the wire diameter and length, and the spacing between adjacent wires.

The "X" and "Y" drive line inductances are also made up of the core inductance and the wire inductance. The core inductance can take several values depending upon the state of the core and the polarity of the drive current. For a Read (-) current, the worse possible case is with the core in the wl state. If a post Write disturb is used, the worse state will be dl. For a Write current, the worse case is with the cores in the uz state. For very fast rise current pulses, the core array windings look like transmission lines with a well defined characteristic impedance and a definite Delay time.

6.9 COMPONENT LOCATOR PICTORIALS

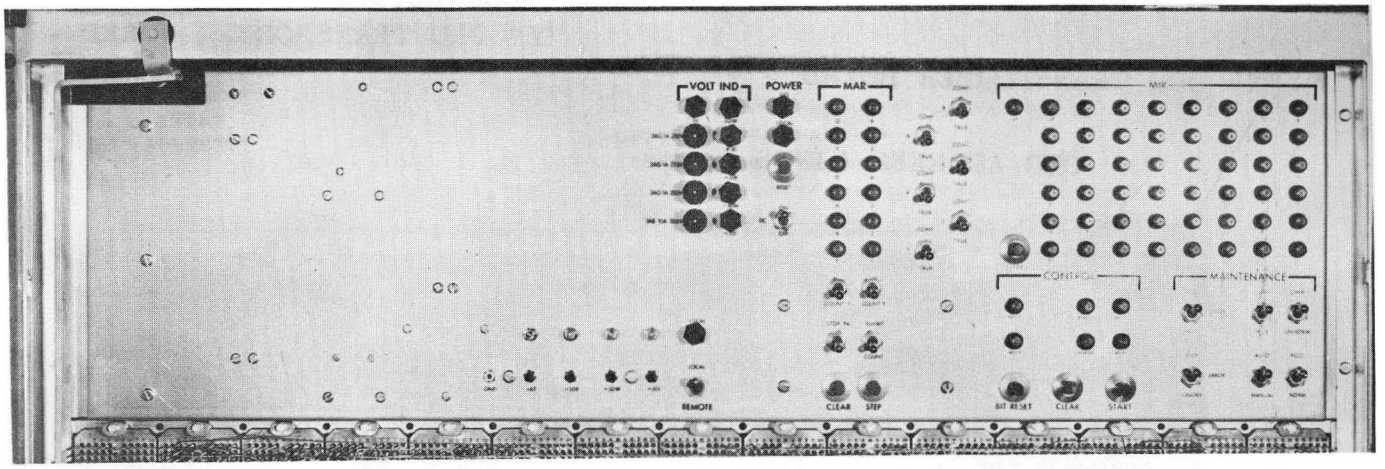


FIGURE 6.9-1
MAINTENANCE PANEL - FRONT VIEW

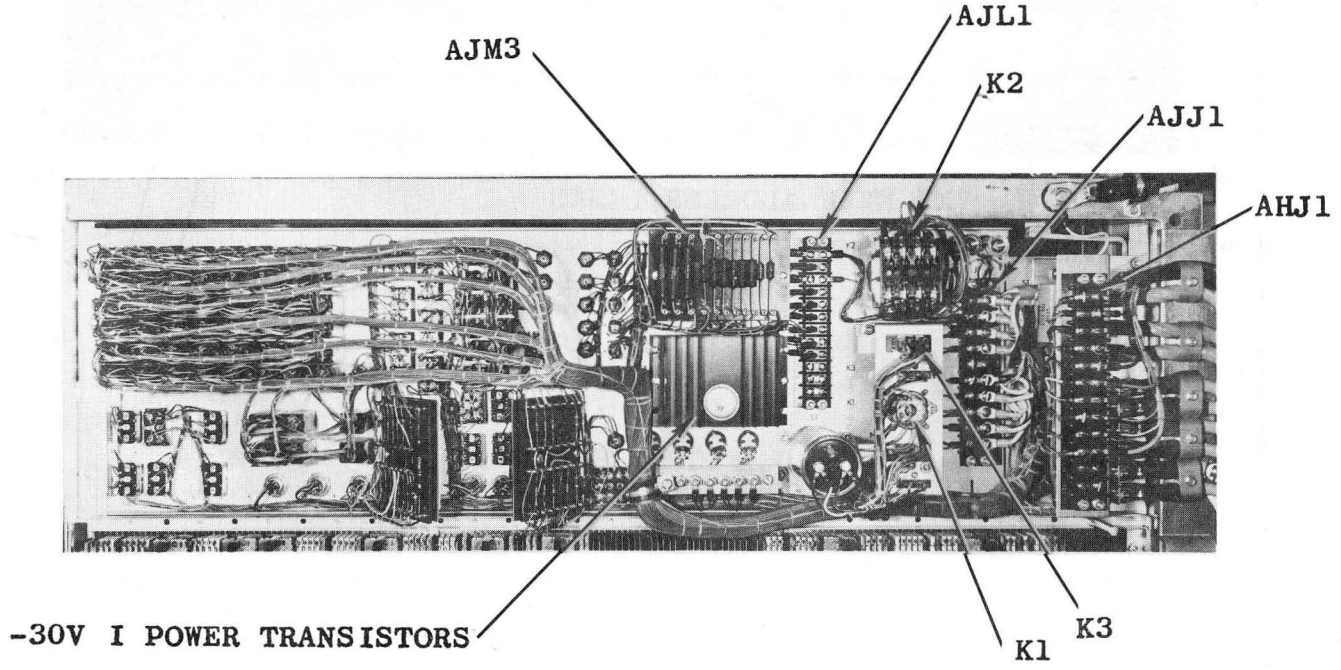


FIGURE 6.9-2
MAINTENANCE PANEL - REAR VIEW

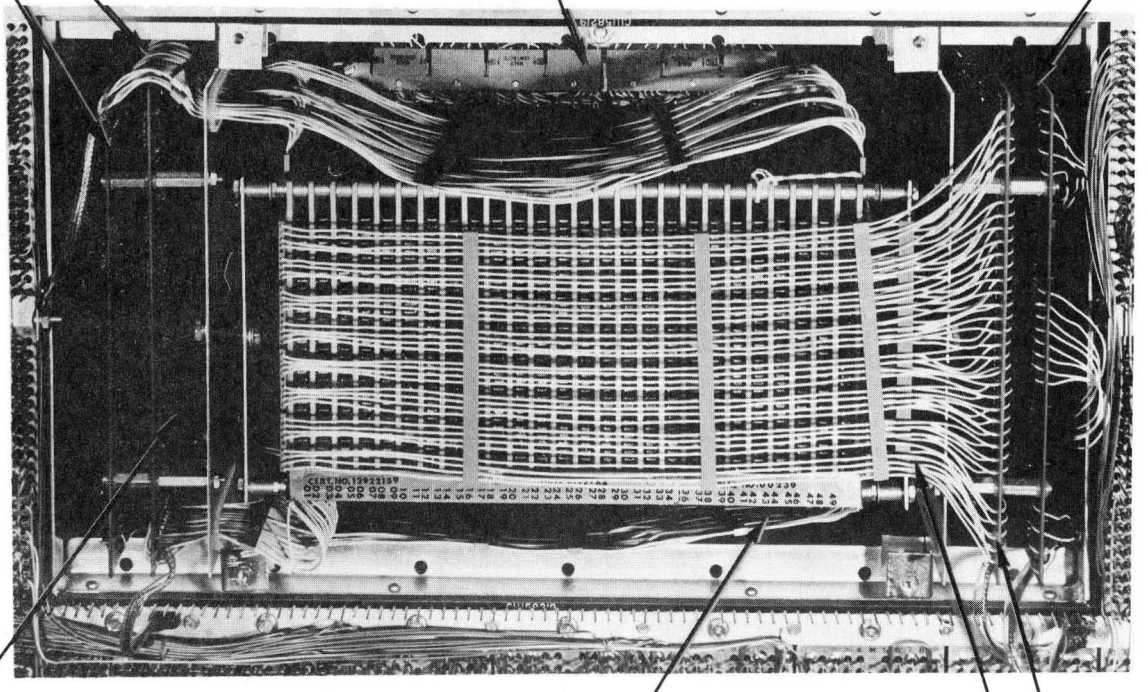


FIGURE 6.9-3
CORE STACK - FRONT

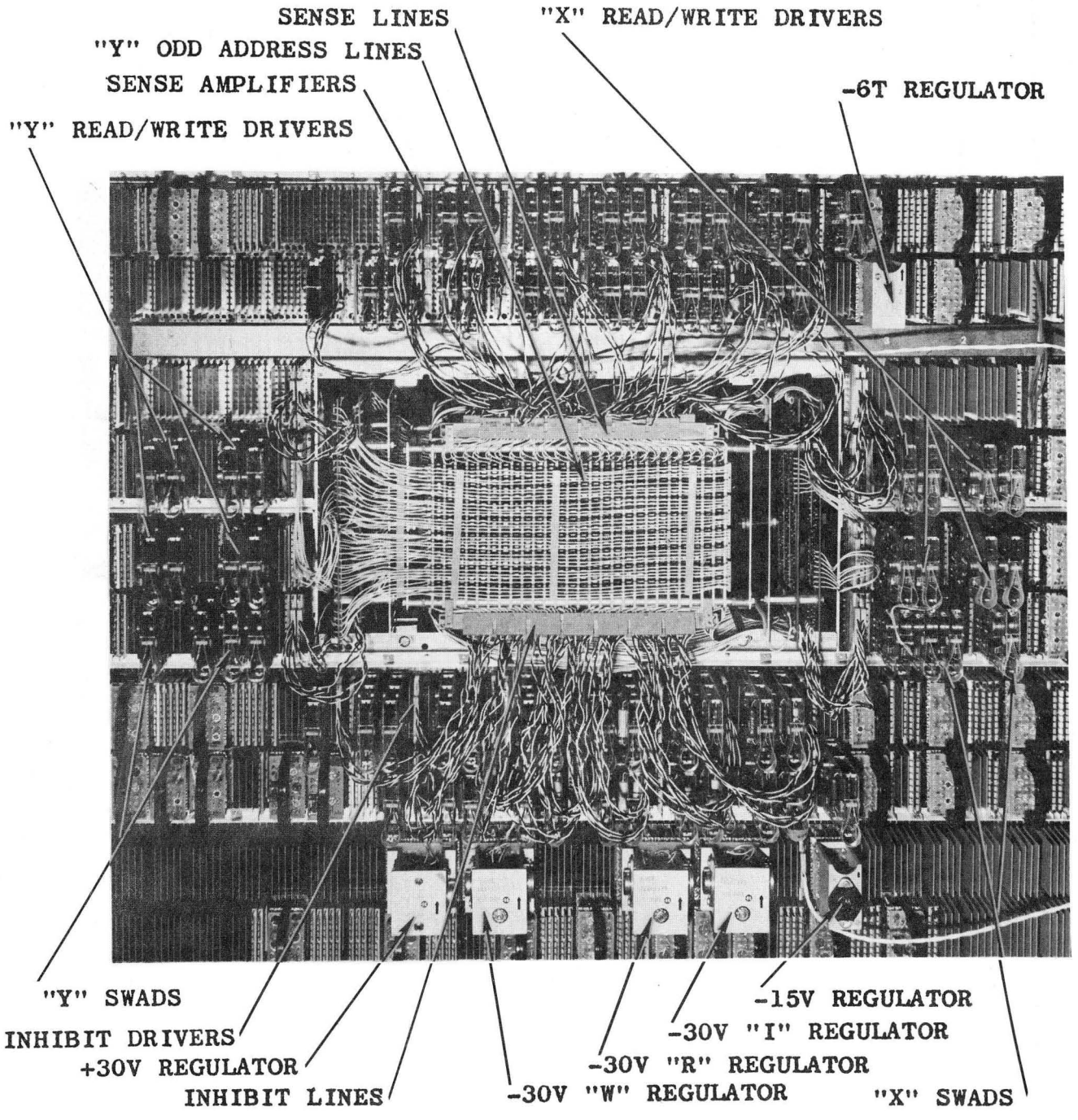
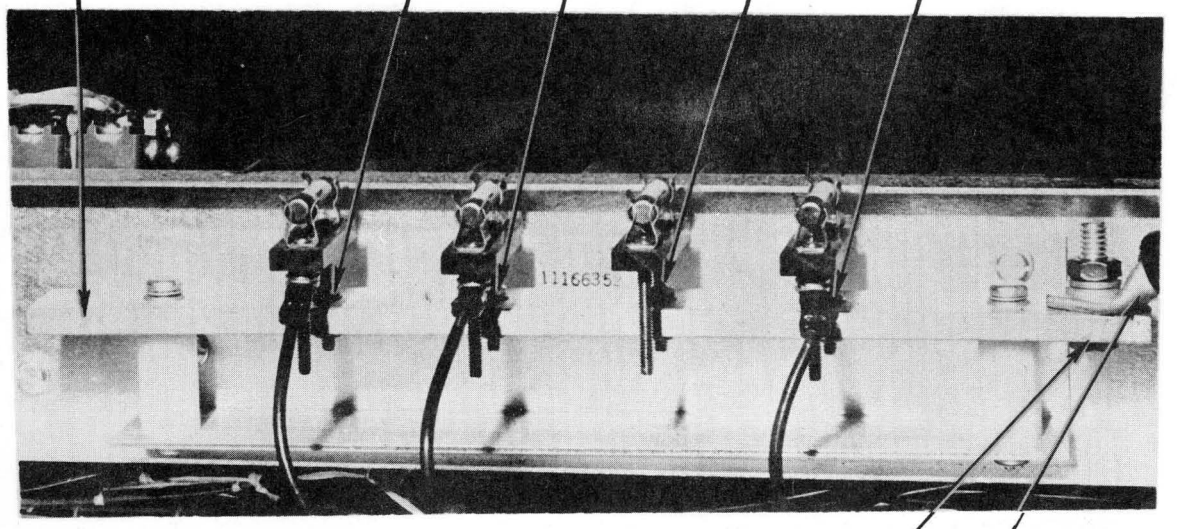


FIGURE 6.9-4
CORE STACK & VOLTAGE REGULATORS
(REAR VIEW)



NOTE: THIS CABLE IN A 6μs MEMORY SUBSYSTEM WENT TO HAJ1-02.

FIGURE 6.9-5
-38V FUSES

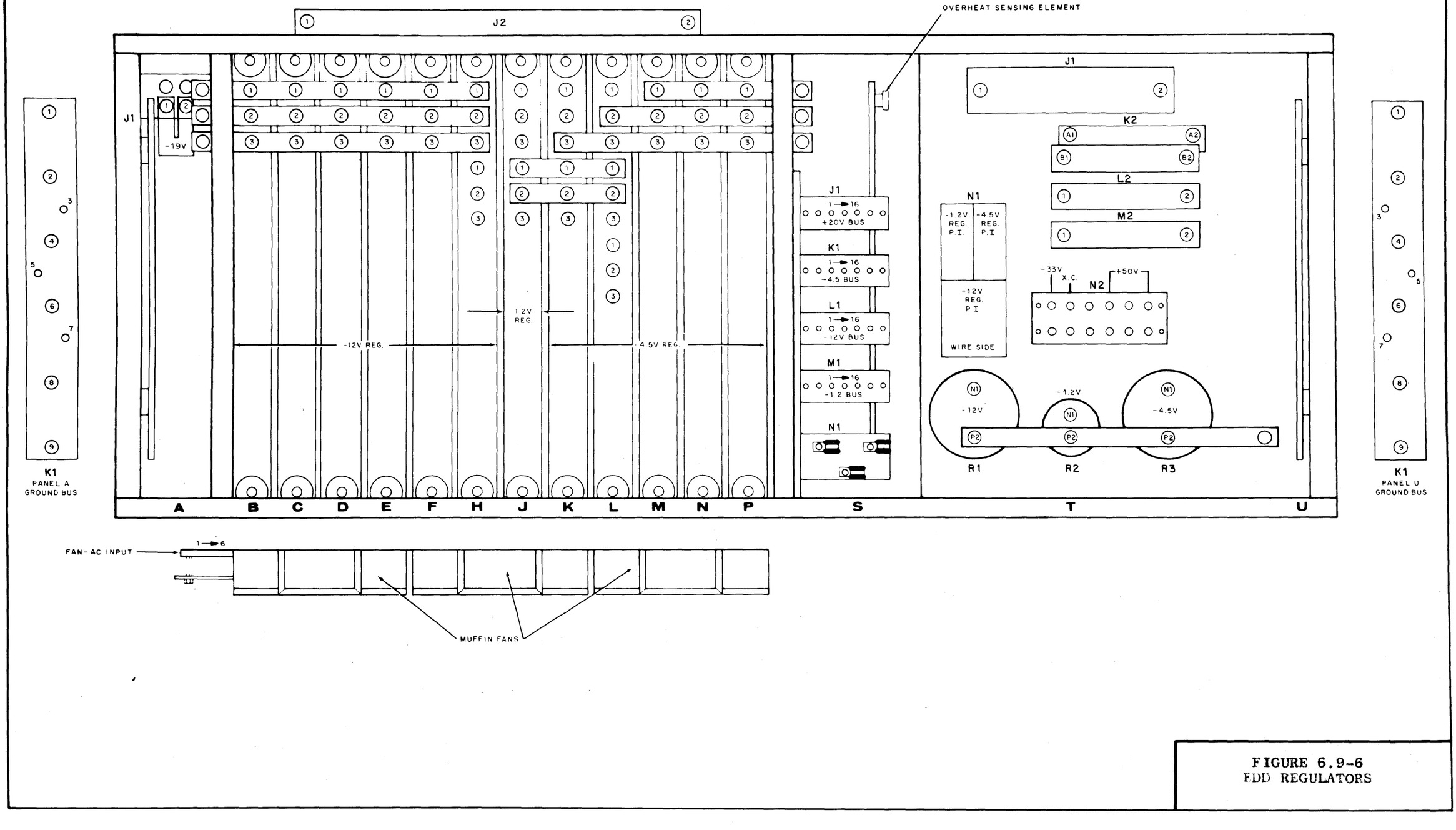


FIGURE 6.9-6
FDD REGULATORS

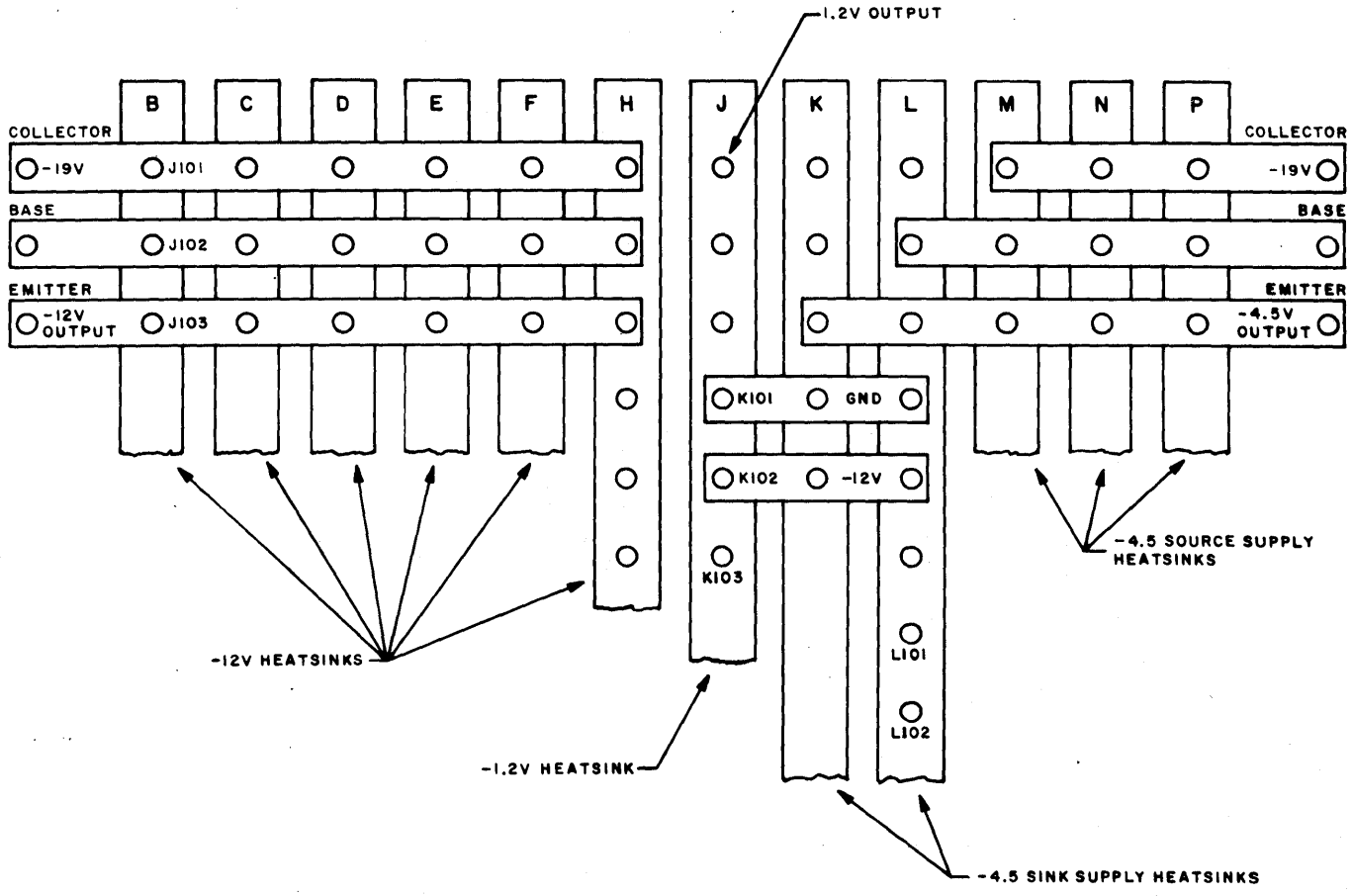


FIGURE 6.9-7
EDD REGULATOR VOLTAGE TERMINALS

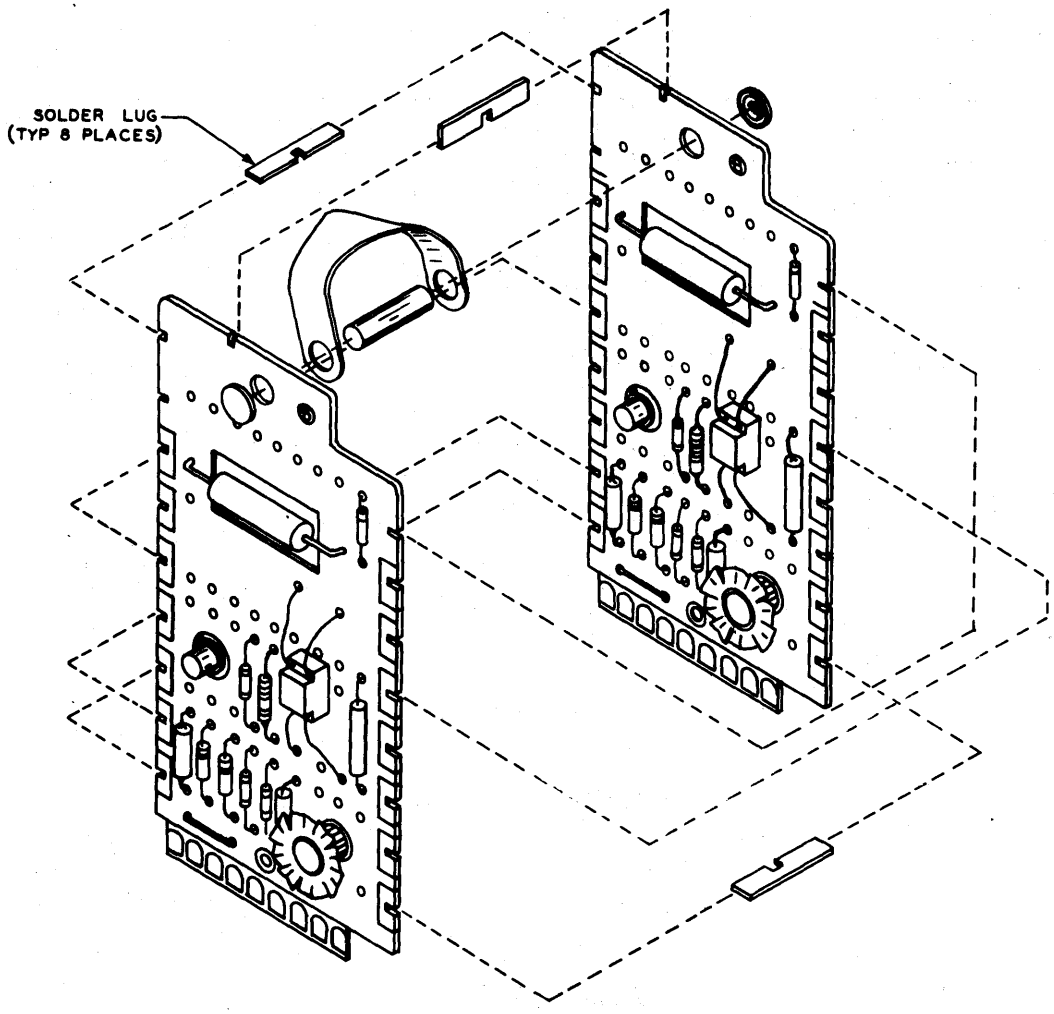


FIGURE 6.9-8
FLEX-O-PAC CONSTRUCTION

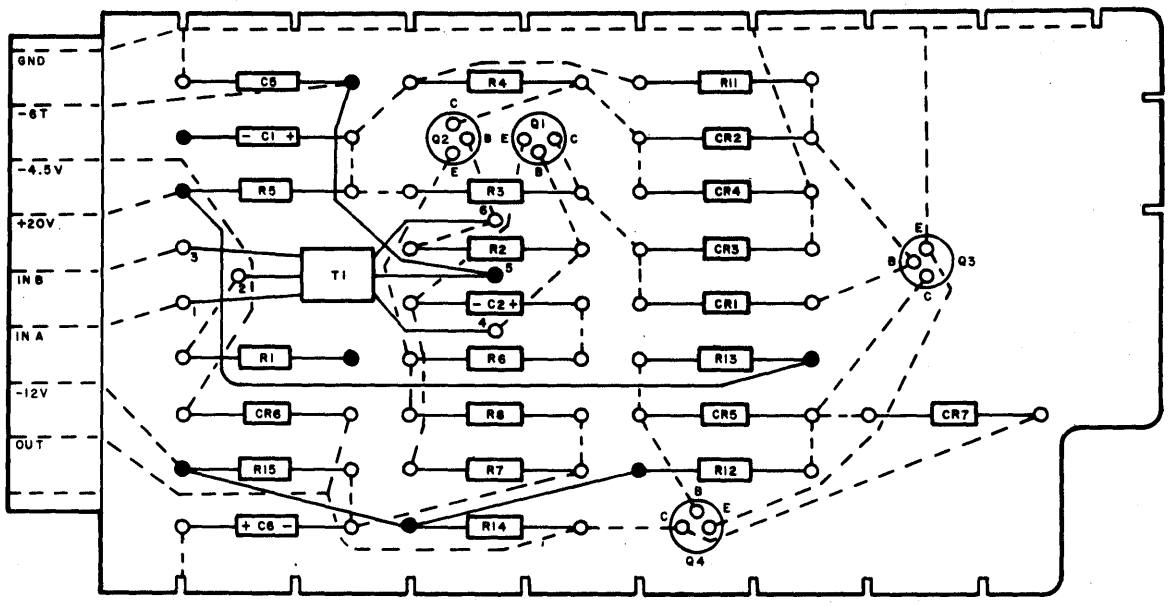


FIGURE 6.9-9
COMPONENT LOCATOR - SENSE AMPS

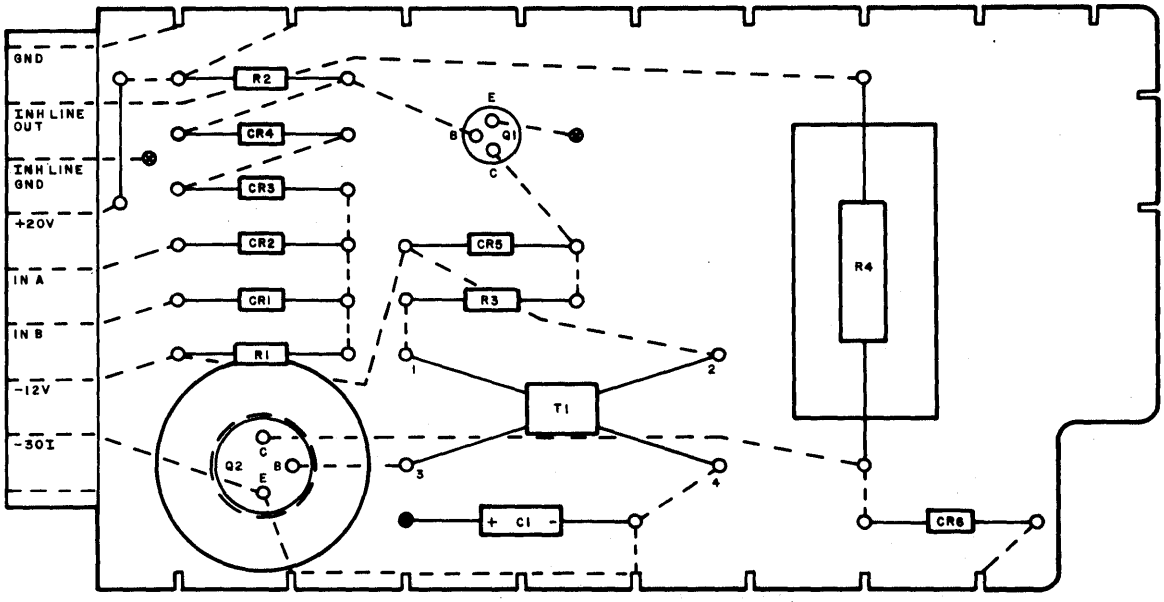


FIGURE 6.9-10
COMPONENT LOCATOR - INHIBIT CURRENT DRIVERS

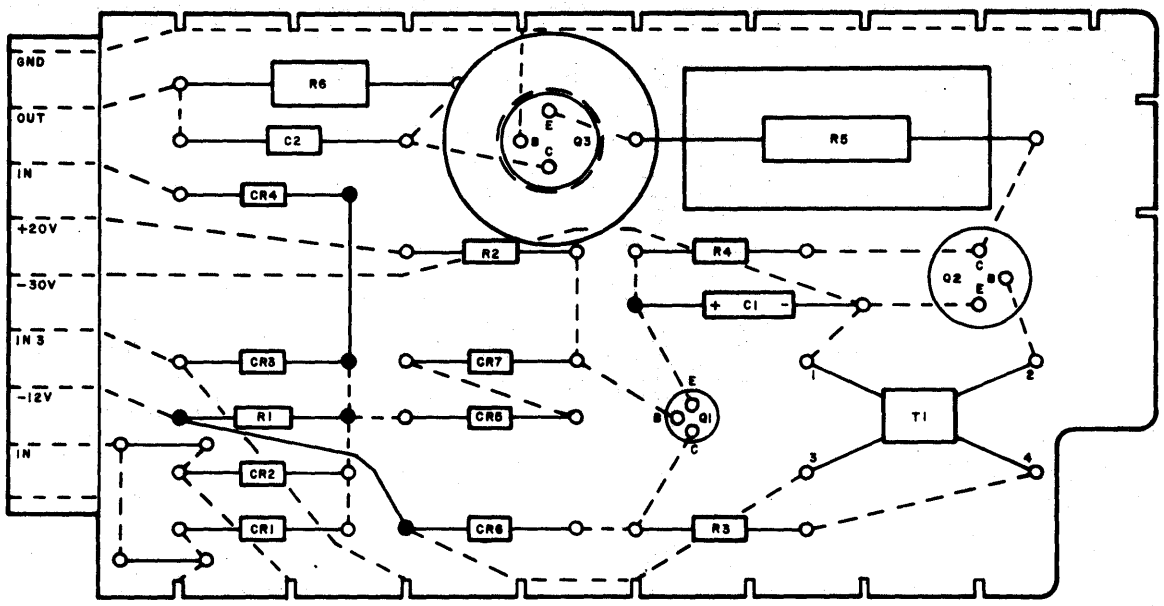


FIGURE 6.9-11
COMPONENT LOCATOR - ADDRESS CURRENT DRIVERS

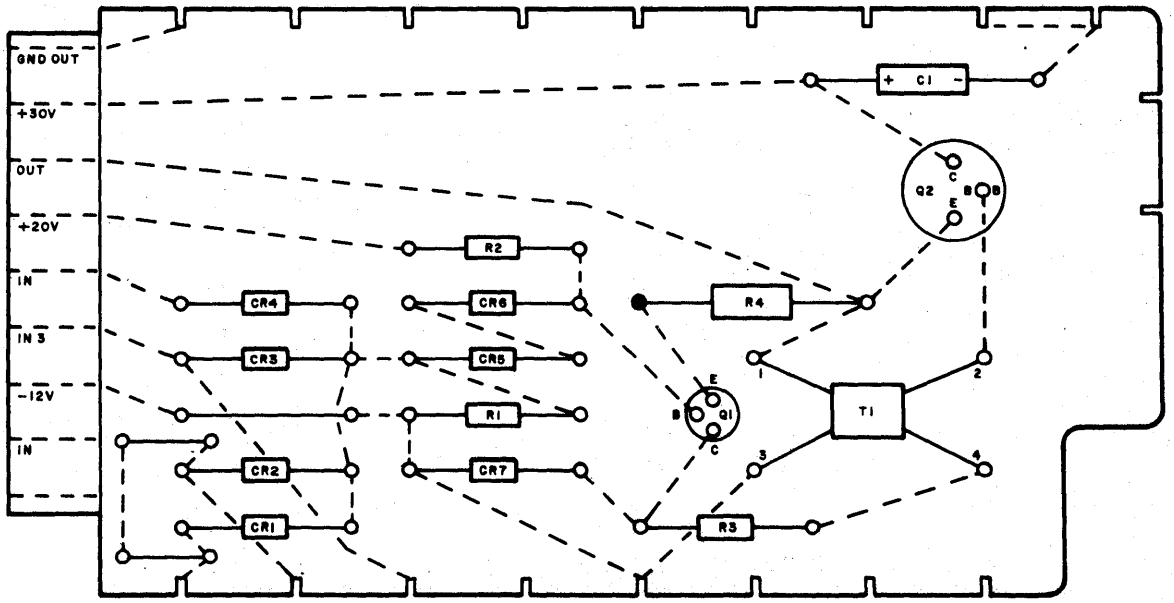


FIGURE 6.9-12
COMPONENT LOCATOR - MEMORY ADDRESS SWITCHES

	PANEL B										PANEL A										
	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0					
A		SW-H	DR9	DR9		SW-H	SW-H	SW-H	SW-H			SW-H		SW-H							A
		SW-H			SW-H		SW-H			SW-H		SW-H		SW-H		SYN MSTL					
			MERF		MSTF	MWCF		MWRF	MP2F	MP1F		I23F	I20F	I15F		I09F		I05F	I01F		78
B		I47F	I44F	I41F	I38F	I36F	I32F	I29F	I28F	CLSA CLCK		I24F	I21F	I16F	I13F	I10F		I06F	I02F	406	79	B
																				C50	C50
		I48F	I45F	I42F	I39F	I37F	I33F	I30F		VB	DRLC		IMCP	I22F		I17F	I14F		I11F	I07F	I03F	372 PWR	80
C																				C50	C50
	I49F		I46F	I43F	I40F		I35F	I34F	I31F	I27F	I26F	I25F			I19F	I18F			I12F	I08F	I04F	414	81	C
																				C50	C50
				DRD9	DRD9			S48P/S46P	S44P/S42P	S40P/S38P	S36P/S34P	S32P/S30P	S28P/S26P	S24P/S22P	S20P/S18P	S16P/S14P	S12P/S10P	S08P/S06P	S04P/S02P	DRD9	SW-H	DRI9	2-0A	1-0A
D																						C50	C50	D
						S49P	S47P/S45P	S43P/S41P	S39P/S37P	S35P/S33P	S31P/S29P	S27P/S25P	S23P/S21P	S19P/S17P	S15P/S13P	S11P/S09P	S07P/S05P	S03P/S01P		-6T	DR9		2-0B	1-0B
																						C50	C50	

FIGURE 6.10-2
PACKAGE LOCATOR
PANELS "A" & "B"

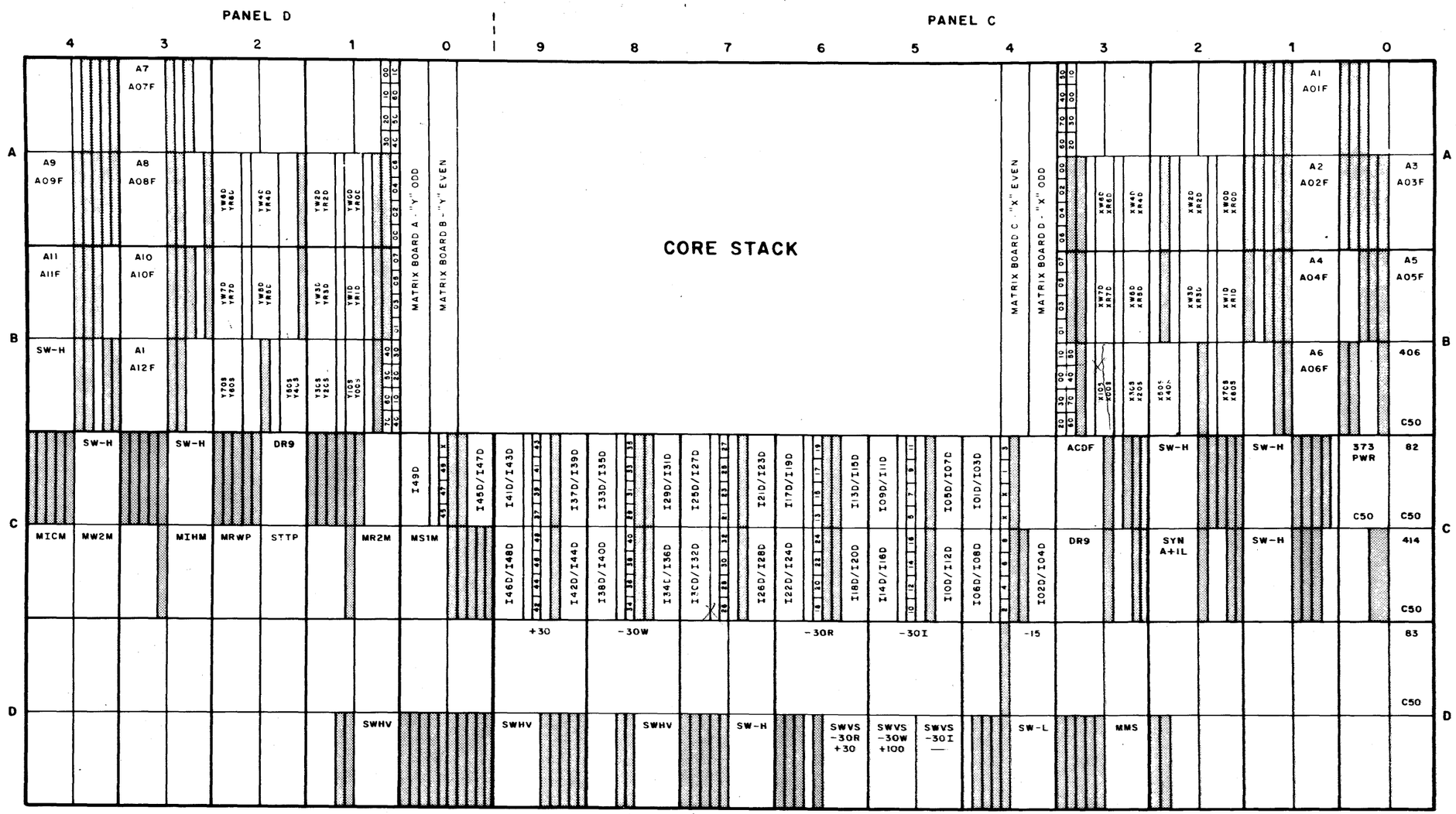


FIGURE 6.10-3
PACKAGE LOCATOR
PANELS "C" & "D"

6.10 ASSEMBLY LOCATIONS

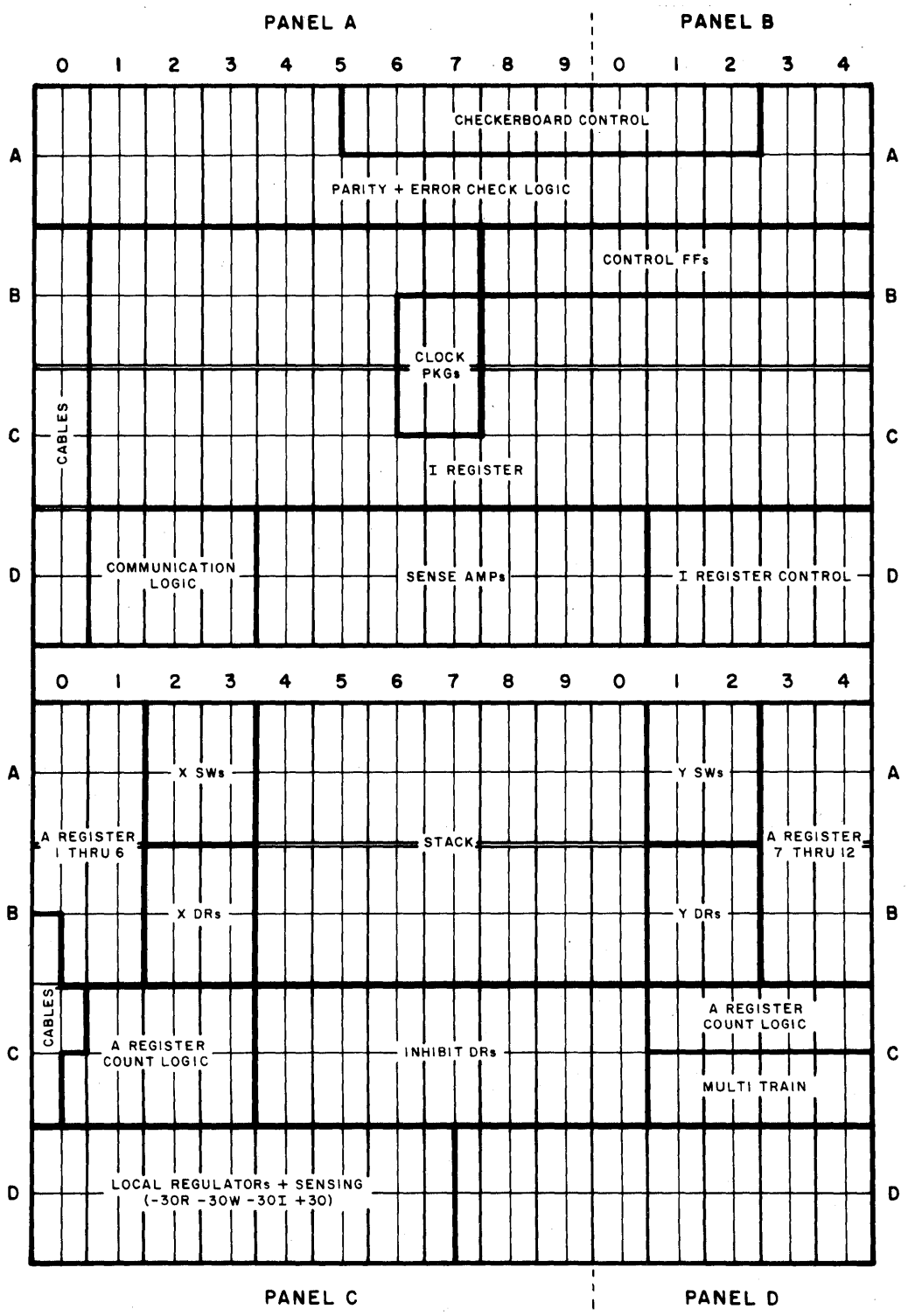


FIGURE 6.10-1
BASIC LOGICAL & FUNCTIONAL AREAS

6.11 TERMINATIONS & ROUTINGS

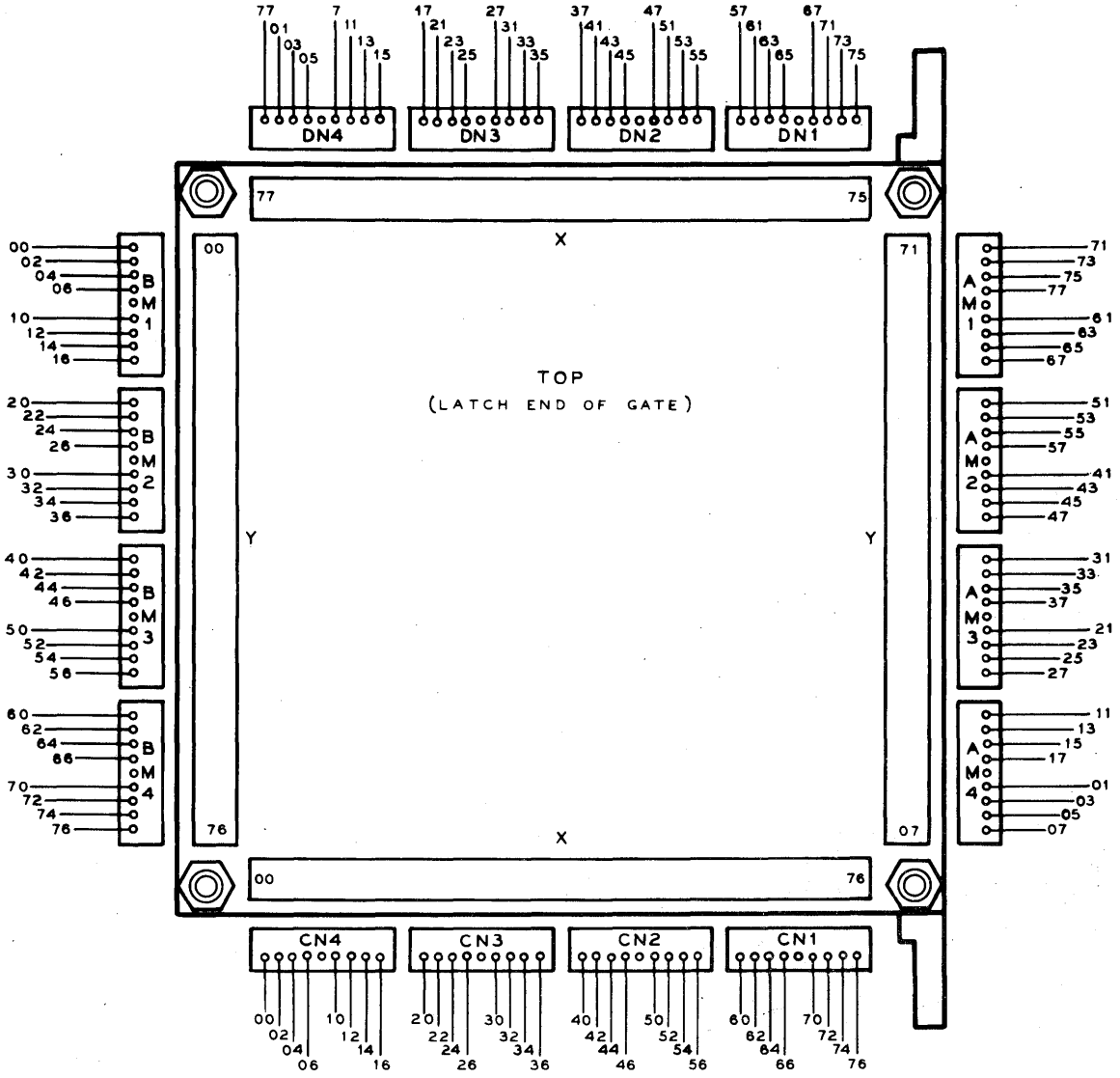


FIGURE 6.11-1
ADDRESS LINES - TOP OF STACK

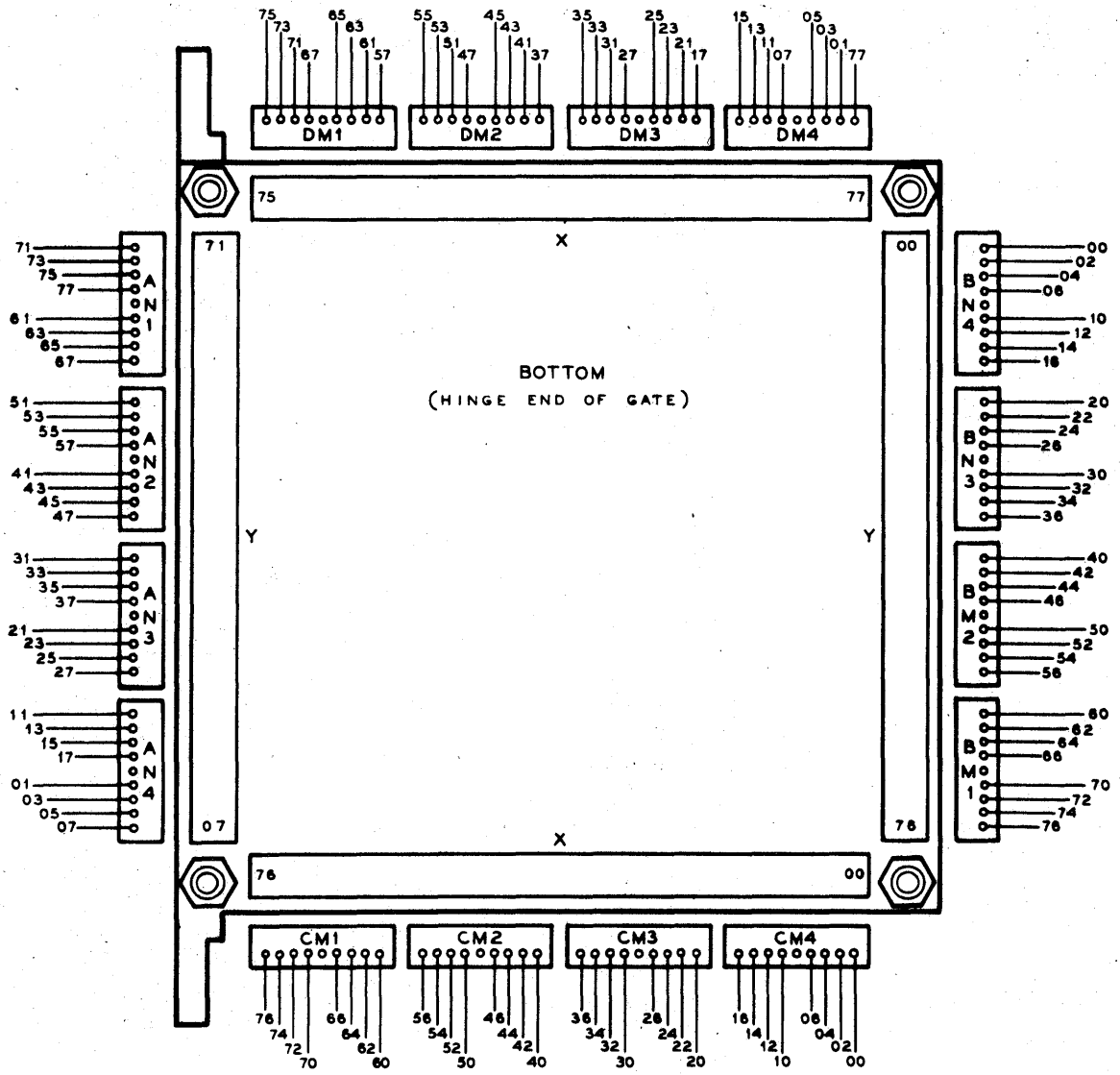


FIGURE 6.11-2
ADDRESS LINES - BOTTOM OF STACK

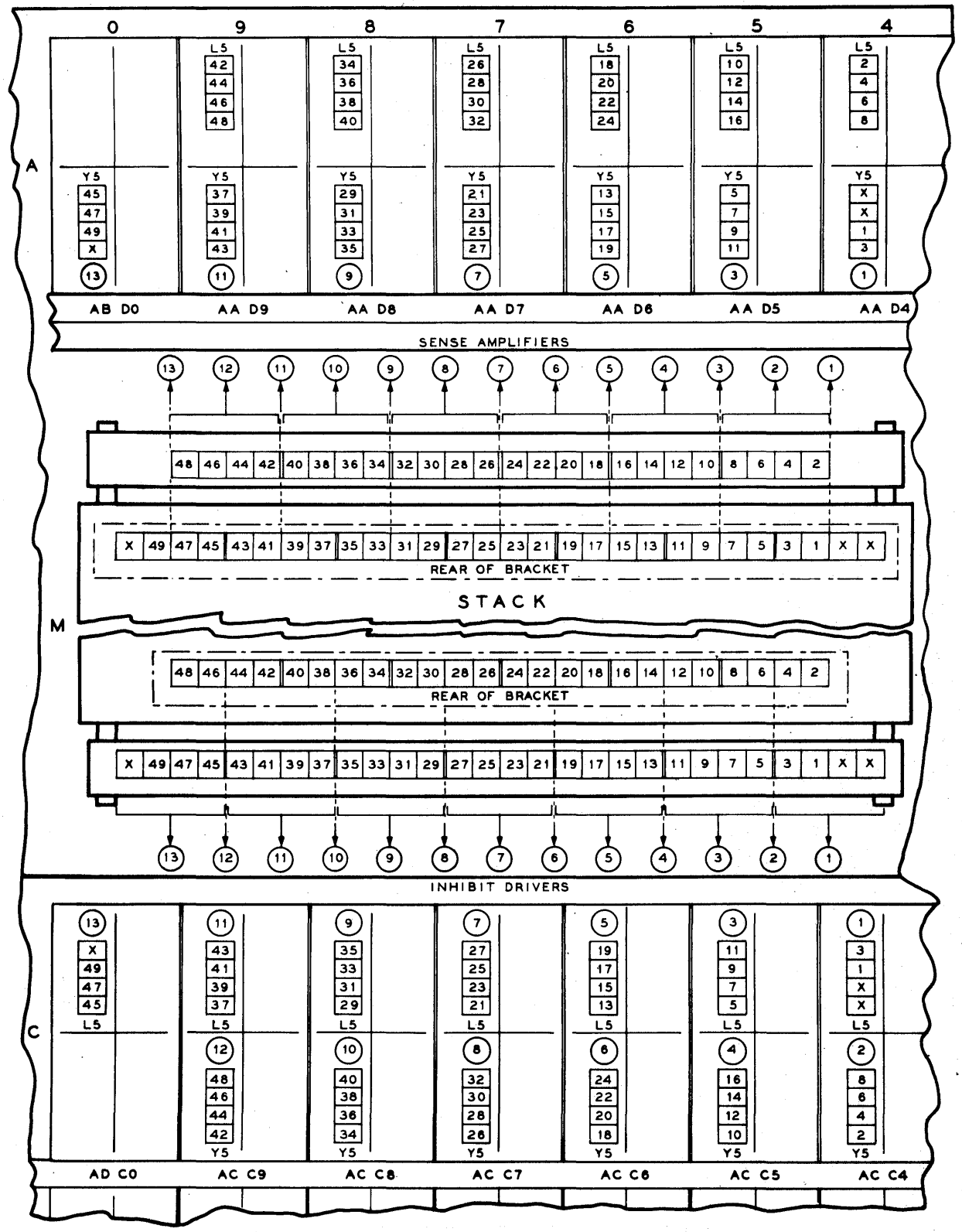


FIGURE 6.11-3
SENSE AMP & INHIBIT DRIVER CONNECTIONS

D & D

CENTRAL CONTROL

DAJ1 13

MEMORY SUB-SYSTEM 1 (4μS MEMORY 0 ⇒ 3)

#25-40

RELAY GROUND

HAK2: +38V
HAJ1: +19V
HAJ2: 100V, +100, MAST. CLEAR
HAJ3: -120V, -24, +50, DC LOCKOUT

FUSE	UNIT
HA K2 02	4μs M-0
HA K2 03	4μs M-1
HA K2 04	4μs M-2
HA K2 05	4μs M-3

AHJ1

-120V (1), -100V (2), -38 (3), -24 (4), +19 (5), +50 (6), +100 (7), MASTER CLEAR (8), DC LOCKOUT (9), GROUND (10)

(ON EACH MEMORY UNIT)

CABLE NOS.
NO. 388 (4μS M-0)
NO. 389 (4μS M-1)
NO. 390 (4μS M-2)
NO. 391 (4μS M-3)

GATE LOGIC GROUND
CU K1 01 397 4μS M-0 GATE "E"
CU K1 02 398 4μS M-1 GATE "D"
CA K1 01 399 4μS M-2 GATE "A"
CA K1 02 400 4μS M-3 GATE "B"

VOLTAGE REGULATOR
WHITE/RED +20V CSK1
WHITE/GREEN -4.5V CSL1
WHITE/BLACK -12V CSM1
WHITE -1.2V CSN1

CABLE NOS.
NO. 364 (4μS M-0)
NO. 365 (4μS M-1)
NO. 366 (4μS M-2)
NO. 367 (4μS M-3)

AJJ1
+20V (1), -4.5V (2), -12V (3), -1.2V (4), (5), -30Z WHITE/ORANGE (6), +20V WHITE/RED (7), -4.5V WHITE/GREEN (8), -12V WHITE/BLACK (9), -1.2V WHITE (10)

(ON EACH MEMORY UNIT)

CABLE NOS.
NO. 373 4μS M-0
NO. 375 4μS M-1
NO. 377 4μS M-2
NO. 379 4μS M-3

AC C0 A7: -4.5V, -12V, +20V, -30Z, -1.2V (9 8 7 6 5)

CABLE NOS.
NO. 372 4μS M-0
NO. 374 4μS M-1
NO. 376 4μS M-2
NO. 378 4μS M-3

AA C0 A7: -12V, -4.5V, -1.2V, SPACE, +20V (5 6 7 8 9)

MEMORY SUB-SYSTEM 2 (4μS MEMORY 4 ⇒ 7)

#25-40A

HAK2: -38V
HAJ1: +19
HAJ2: -100V, +100, MAST. CLEAR
HAJ3: -120, -24, +50, DC LOCKOUT

FUSE	UNIT
HA K2 02	4μS M-4
HA K2 03	4μS M-5
HA K2 04	4μS M-6
HA K2 05	4μS M-7

AHJ1

-120V (1), -100V (2), -38 (3), -24 (4), +19 (5), +50 (6), +100 (7), MASTER CLEAR (8), DC LOCKOUT (9), GROUND (10)

(ON EACH MEMORY UNIT)

CABLE NOS.
NO. 392 (4μS M-4)
NO. 393 (4μS M-5)
NO. 394 (4μS M-6)
NO. 395 (4μS M-7)

GATE LOGIC GROUND
CU K1 01 401 4μS M-4 GATE "E"
CU K1 02 402 4μS M-5 GATE "D"
CA K1 01 403 4μS M-6 GATE "A"
CA K1 02 404 4μS M-7 GATE "B"

VOLTAGE REGULATOR
WHITE/RED +20V CSK1
WHITE/GREEN -4.5V CSL1
WHITE/BLACK -12V CSM1
WHITE -1.2V CSN1

CABLE NOS.
NO. 368 (4μS M-4)
NO. 369 (4μS M-5)
NO. 370 (4μS M-6)
NO. 371 (4μS M-7)

AJJ1
+20V (1), -4.5V (2), -12V (3), -1.2V (4), (5), -30Z WHITE/ORANGE (6), +20V WHITE/RED (7), -4.5V WHITE/GREEN (8), -12V WHITE/BLACK (9), -1.2V WHITE (10)

(ON EACH MEMORY UNIT)

CABLE NOS.
NO. 381 (4μS M-4)
NO. 383 (4μS M-5)
NO. 385 (4μS M-6)
NO. 387 (4μS M-7)

AC C0 A7: -4.5V, -12V, +20V, -30Z, -1.2V (9 8 7 6 5)

CABLE NOS.
NO. 380 (4μS M-4)
NO. 382 (4μS M-5)
NO. 384 (4μS M-6)
NO. 386 (4μS M-7)

AA C0 A7: -12V, -4.5V, -1.2V, SPACE, +20V (5 6 7 8 9)

FIGURE 6.11-7
MEMORY SUB-SYSTEM
POWER CABLE ROUTING

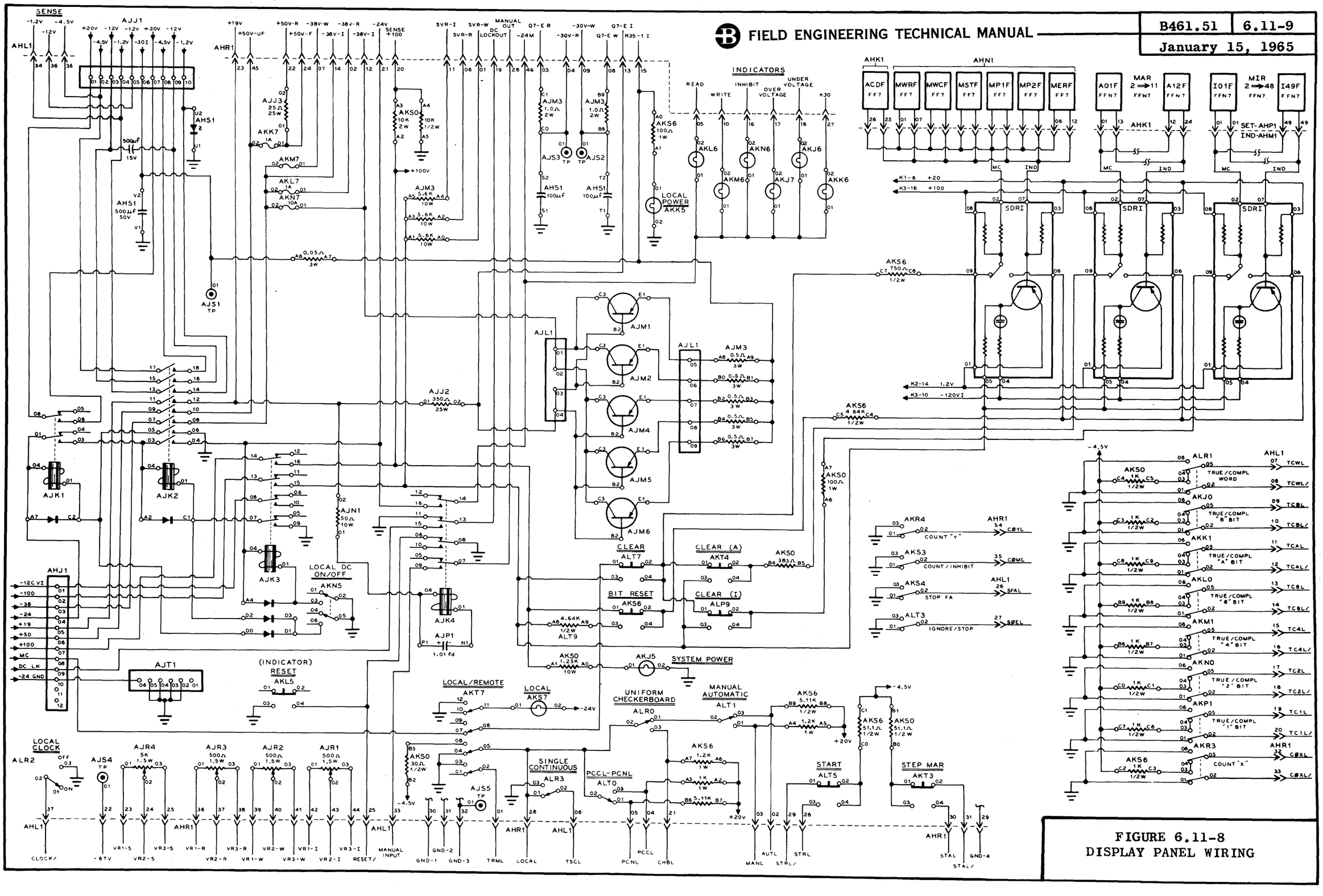


FIGURE 6.11-8
DISPLAY PANEL WIRING

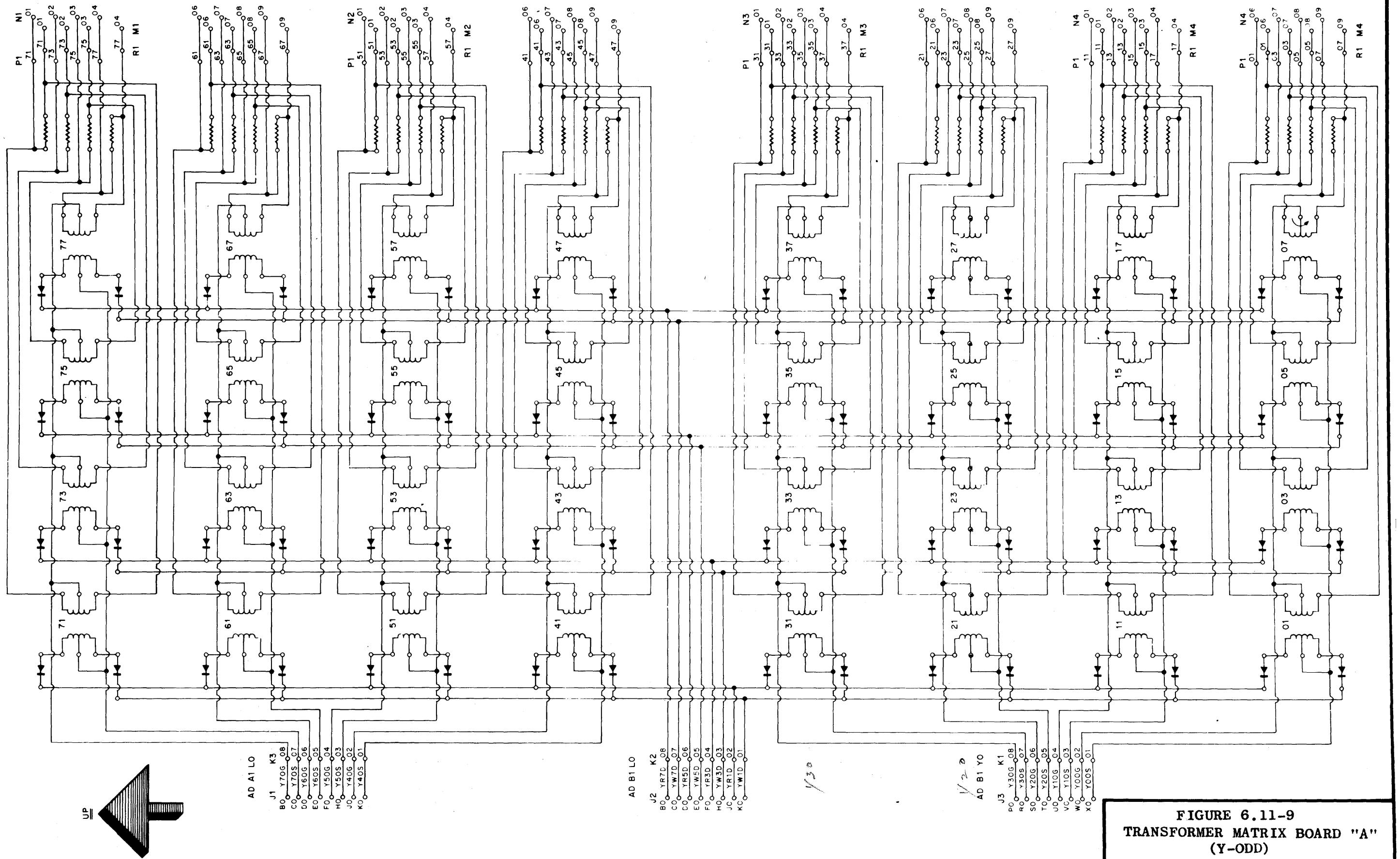


FIGURE 6.11-9
TRANSFORMER MATRIX BOARD "A"
(Y-ODD)

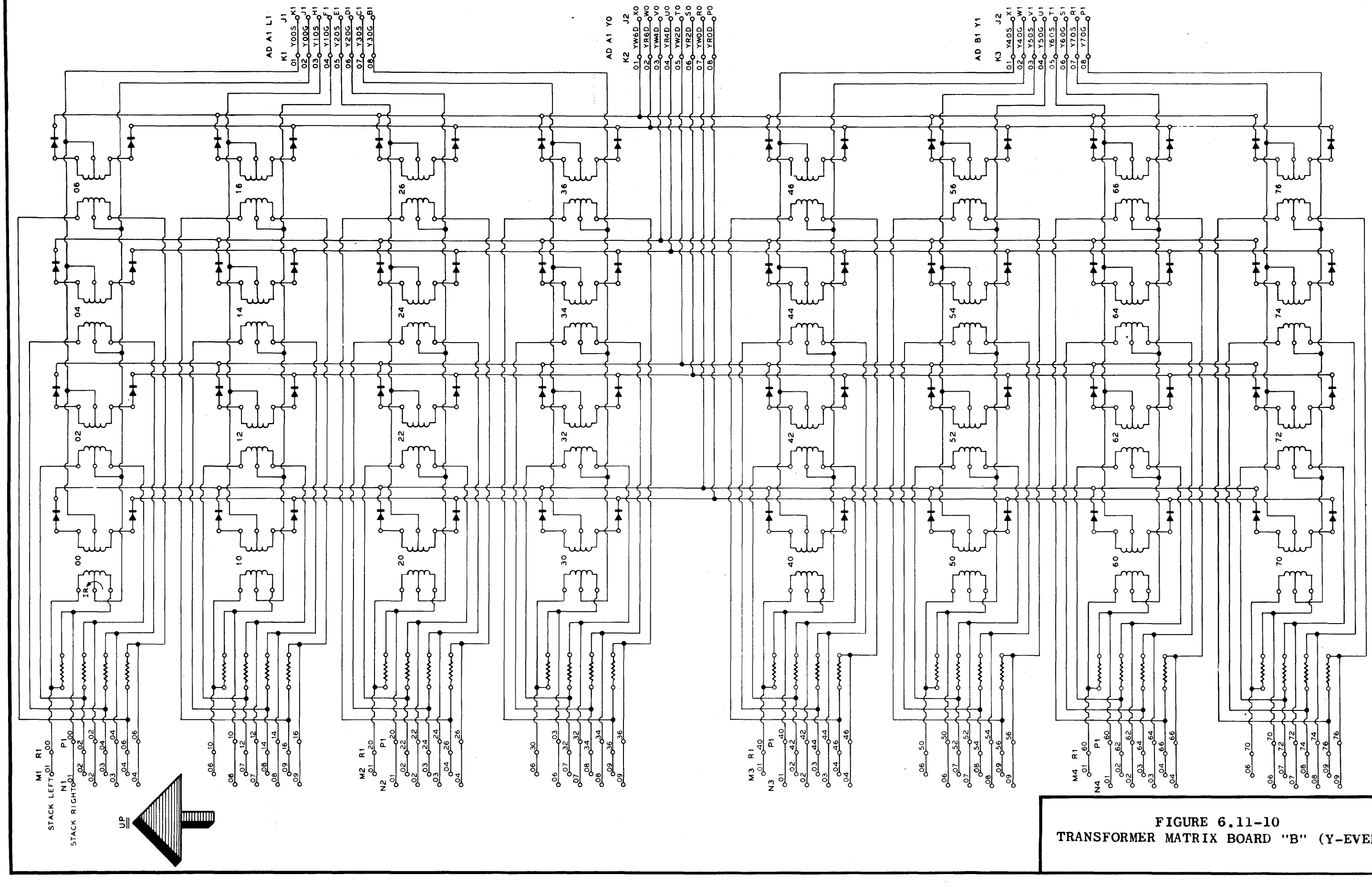


FIGURE 6.11-10
TRANSFORMER MATRIX BOARD "B" (Y-EVEN)

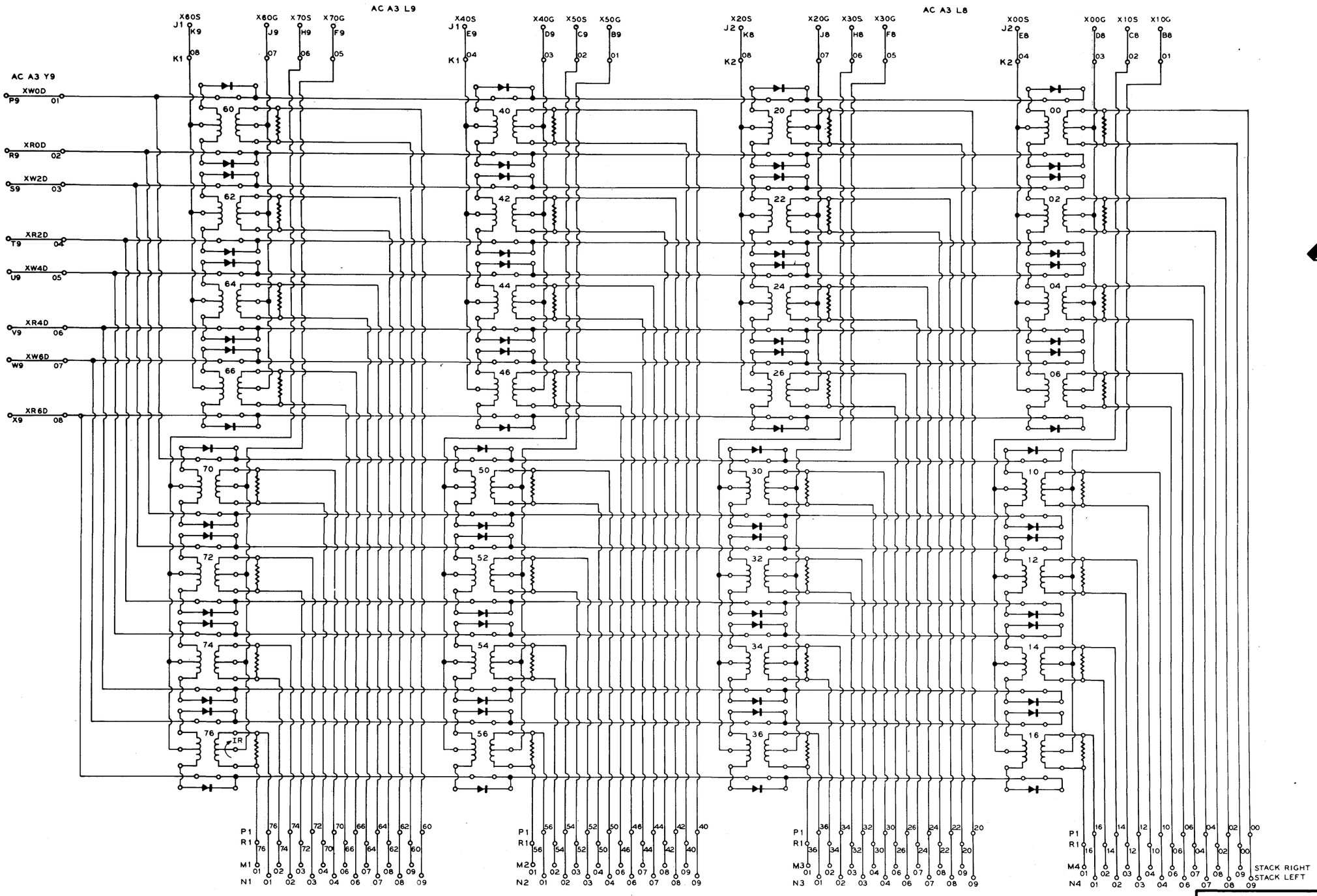


FIGURE 6.11-11
TRANSFORMER MATRIX BOARD "C"
(X-EVEN)

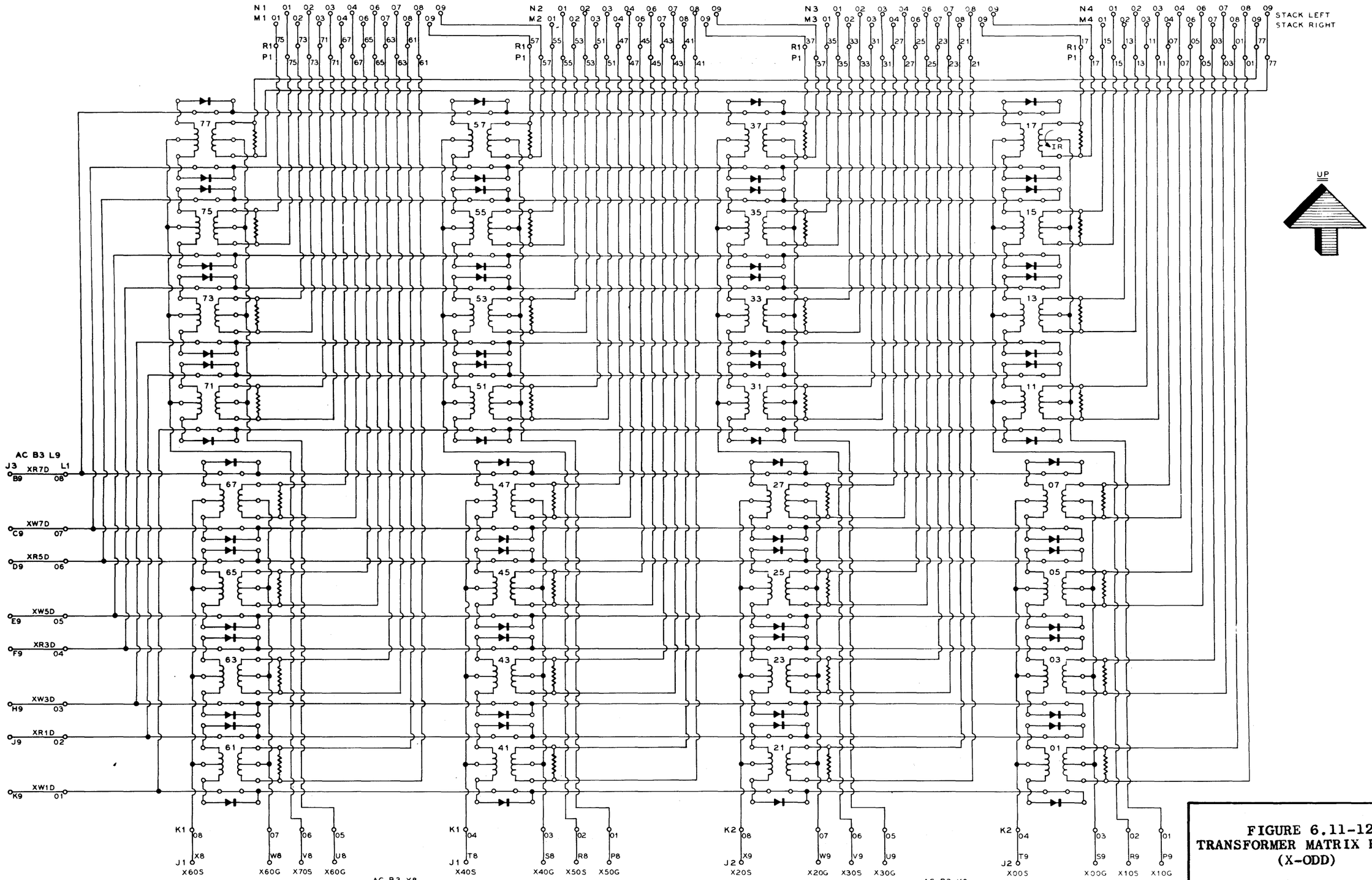
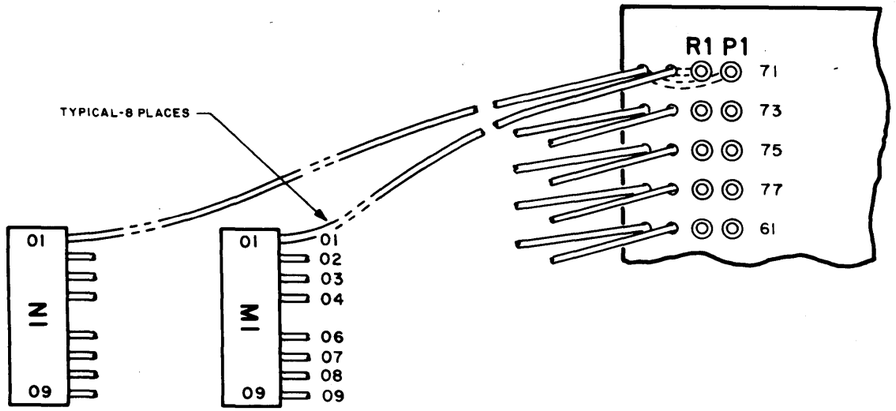
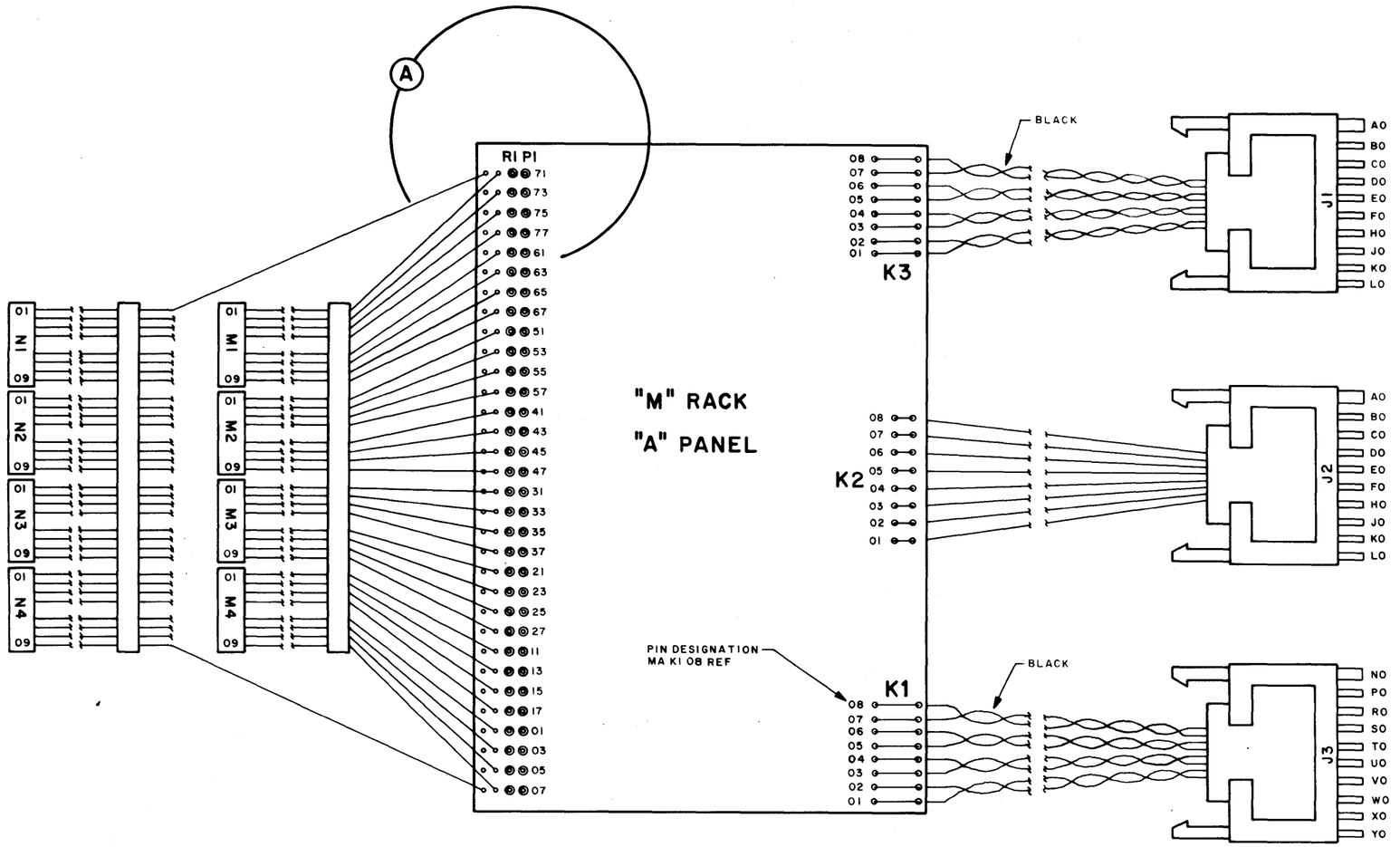


FIGURE 6.11-12
TRANSFORMER MATRIX BOARD "D"
(X-ODD)

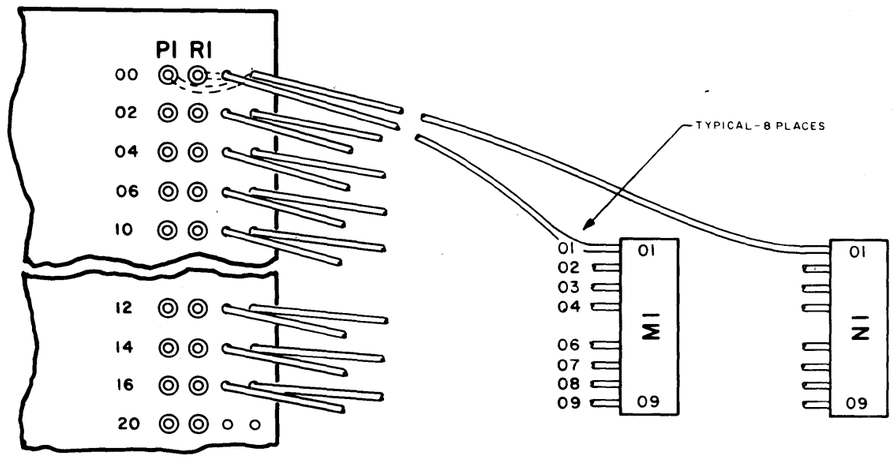


DETAIL A

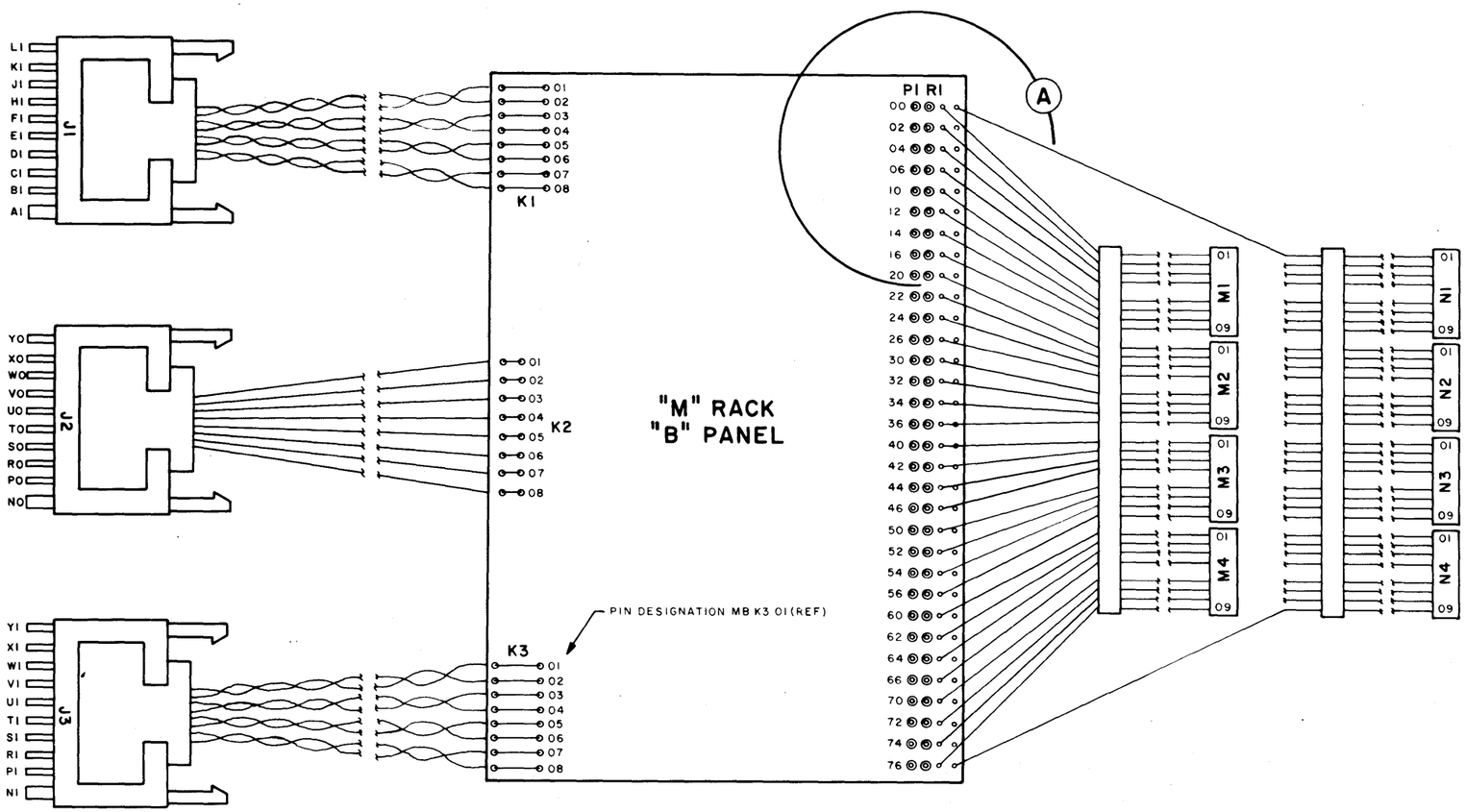


FROM	TO	
MA K1 01	MA J3 XO	ADDRESS SWITCHES — TWISTED PAIR
MA K1 02	MA J3 WO	
MA K1 03	MA J3 VO	TWISTED PAIR
MA K1 04	MA J3 UO	
MA K1 05	MA J3 TO	TWISTED PAIR
MA K1 06	MA J3 SO	
MA K1 07	MA J3 RO	TWISTED PAIR
MA K1 08	MA J3 PO	
MA K2 01	MA J2 KO	ADDRESS CURRENT DRIVERS
MA K2 02	MA J2 JO	
MA K2 03	MA J2 HO	
MA K2 04	MA J2 FO	
MA K2 05	MA J2 EO	
MA K2 06	MA J2 DO	
MA K2 07	MA J2 CO	
MA K2 08	MA J2 BO	
MA K3 01	MA J1 KO	ADDRESS SWITCHES — TWISTED PAIR
MA K3 02	MA J1 JO	
MA K3 03	MA J1 HO	TWISTED PAIR
MA K3 04	MA J1 FO	
MA K3 05	MA J1 EO	TWISTED PAIR
MA K3 06	MA J1 DO	
MA K3 07	MA J1 CO	TWISTED PAIR
MA K3 08	MA J1 BO	
MA R1 71	MA M1 01	
MA R1 73	MA M1 02	
MA R1 75	MA M1 03	
MA R1 77	MA M1 04	
MA R1 61	MA M1 06	
MA R1 63	MA M1 07	
MA R1 65	MA M1 08	
MA R1 67	MA M1 09	
MA R1 51	MA M2 01	
MA R1 53	MA M2 02	
MA R1 55	MA M2 03	
MA R1 57	MA M2 04	
MA R1 41	MA M2 06	
MA R1 43	MA M2 07	
MA R1 45	MA M2 08	
MA R1 47	MA M2 09	
MA R1 31	MA M3 01	
MA R1 33	MA M3 02	
MA R1 35	MA M3 03	
MA R1 37	MA M3 04	
MA R1 21	MA M3 06	
MA R1 23	MA M3 07	
MA R1 25	MA M3 08	
MA R1 27	MA M3 09	
MA R1 11	MA M4 01	
MA R1 13	MA M4 02	
MA R1 15	MA M4 03	
MA R1 17	MA M4 04	
MA R1 01	MA M4 06	
MA R1 03	MA M4 07	
MA R1 05	MA M4 08	
MA R1 07	MA M4 09	
MA P1 71	MA N1 01	
MA P1 73	MA N1 02	
MA P1 75	MA N1 03	
MA P1 77	MA N1 04	
MA P1 61	MA N1 06	
MA P1 63	MA N1 07	
MA P1 65	MA N1 08	
MA P1 67	MA N1 09	
MA P1 51	MA N2 01	
MA P1 53	MA N2 02	
MA P1 55	MA N2 03	
MA P1 57	MA N2 04	
MA P1 41	MA N2 06	
MA P1 43	MA N2 07	
MA P1 45	MA N2 08	
MA P1 47	MA N2 09	
MA P1 31	MA N3 01	
MA P1 33	MA N3 02	
MA P1 35	MA N3 03	
MA P1 37	MA N3 04	
MA P1 21	MA N3 06	
MA P1 23	MA N3 07	
MA P1 25	MA N3 08	
MA P1 27	MA N3 09	
MA P1 11	MA N4 01	
MA P1 13	MA N4 02	
MA P1 15	MA N4 03	
MA P1 17	MA N4 04	
MA P1 01	MA N4 06	
MA P1 03	MA N4 07	
MA P1 05	MA N4 08	
MA P1 07	MA N4 09	

FIGURE 6.11-13
TRANSFORMER BOARD LAYOUT "A"
(Y-ODD)

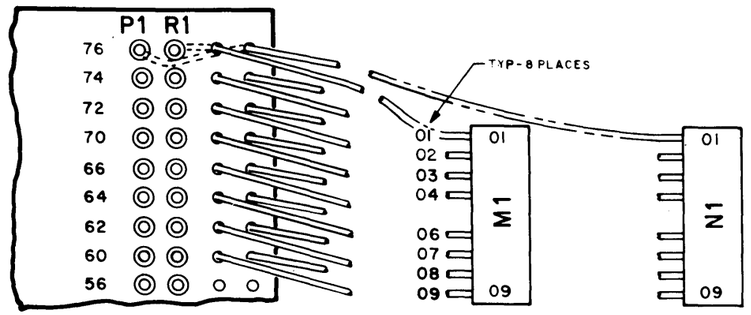


DETAIL A

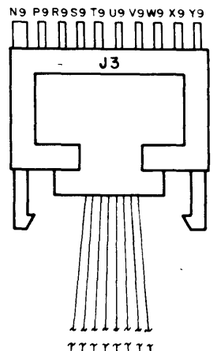


FROM	TO	
ADDRESS SWITCHES	MB K1 01	MB J1 B1 } TWISTED PAIR
	MB K1 02	MB J1 C1
	MB K1 03	MB J1 D1 } TWISTED PAIR
	MB K1 04	MB J1 E1
	MB K1 05	MB J1 F1 } TWISTED PAIR
	MB K1 06	MB J1 H1
	MB K1 07	MB J1 J1 } TWISTED PAIR
	MB K1 08	MB J1 K1
ADDRESS CURRENT DRIVERS	MB K2 01	MB J2 P0
	MB K2 02	MB J2 R0
	MB K2 03	MB J2 S0
	MB K2 04	MB J2 T0
	MB K2 05	MB J2 U0
	MB K2 06	MB J2 V0
	MB K2 07	MB J2 W0
	MB K2 08	MB J2 X0
ADDRESS SWITCHES	MB K3 01	MB J3 P1 } TWISTED PAIR
	MB K3 02	MB J3 R1
	MB K3 03	MB J3 S1 } TWISTED PAIR
	MB K3 04	MB J3 T1
	MB K3 05	MB J3 U1 } TWISTED PAIR
	MB K3 06	MB J3 V1
	MB K3 07	MB J3 W1 } TWISTED PAIR
	MB K3 08	MB J3 X1
	MB R1 00	MB M1 01
	MB R1 02	MB M1 02
	MB R1 04	MB M1 03
	MB R1 06	MB M1 04
	MB R1 10	MB M1 06
	MB R1 12	MB M1 07
	MB R1 14	MB M1 08
	MB R1 16	MB M1 09
	MB R1 20	MB M2 01
	MB R1 22	MB M2 02
	MB R1 24	MB M2 03
	MB R1 26	MB M2 04
	MB R1 30	MB M2 06
	MB R1 32	MB M2 07
	MB R1 34	MB M2 08
	MB R1 36	MB M2 09
	MB R1 40	MB M3 01
	MB R1 42	MB M3 02
	MB R1 44	MB M3 03
	MB R1 46	MB M3 04
	MB R1 50	MB M3 06
	MB R1 52	MB M3 07
	MB R1 54	MB M3 08
	MB P1 56	MB M3 09
	MB R1 60	MB M4 01
	MB R1 62	MB M4 02
	MB R1 64	MB M4 03
	MB R1 66	MB M4 04
	MB R1 70	MB M4 06
	MB R1 72	MB M4 07
	MB R1 74	MB M4 08
	MB R1 76	MB M4 09
	MB P1 00	MB N1 01
	MB P1 02	MB N1 02
	MB P1 04	MB N1 03
	MB P1 06	MB N1 04
	MB P1 10	MB N1 06
	MB P1 12	MB N1 07
	MB P1 14	MB N1 08
	MB P1 16	MB N1 09
	MB P1 20	MB N2 01
	MB P1 22	MB N2 02
	MB P1 24	MB N2 03
	MB P1 26	MB N2 04
	MB P1 30	MB N2 06
	MB P1 32	MB N2 07
	MB P1 34	MB N2 08
	MB P1 36	MB N2 09
	MB P1 40	MB N3 01
	MB P1 42	MB N3 02
	MB P1 44	MB N3 03
	MB P1 46	MB N3 04
	MB P1 50	MB N3 06
	MB P1 52	MB N3 07
	MB P1 54	MB N3 08
	MB P1 56	MB N3 09
	MB P1 60	MB N4 01
	MB P1 62	MB N4 02
	MB P1 64	MB N4 03
	MB P1 66	MB N4 04
	MB P1 70	MB N4 06
	MB P1 72	MB N4 07
	MB P1 74	MB N4 08
	MB P1 76	MB N4 09

FIGURE 6.11-14
TRANSFORMER BOARD LAYOUT "B"
(Y-EVEN)

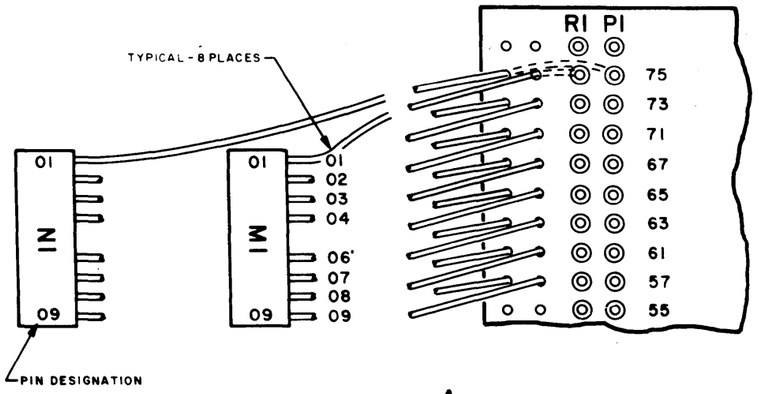


DETAIL A

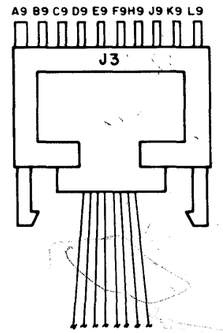


	FROM	TO	
ADDRESS SWITCHES	MC K2 01	MC J2 B8	TWISTED PAIR
	MC K2 02	MC J2 C8	
	MC K2 03	MC J2 D8	TWISTED PAIR
	MC K2 04	MC J2 E8	
	MC K2 05	MC J2 F8	TWISTED PAIR
	MC K2 06	MC J2 H8	
	MC K2 07	MC J2 J8	TWISTED PAIR
	MC K2 08	MC J2 K8	
ADDRESS SWITCHES	MC K1 01	MC J1 B9	TWISTED PAIR
	MC K1 02	MC J1 C9	
	MC K1 03	MC J1 D9	TWISTED PAIR
	MC K1 04	MC J1 E9	
	MC K1 05	MC J1 F9	TWISTED PAIR
	MC K1 06	MC J1 H9	
	MC K1 07	MC J1 J9	TWISTED PAIR
	MC K1 08	MC J1 K9	
ADDRESS CURRENT DRIVERS	MC L1 01	MC J3 P9	
	MC L1 02	MC J3 R9	
	MC L1 03	MC J3 S9	
	MC L1 04	MC J3 T9	
	MC L1 05	MC J3 U9	
	MC L1 06	MC J3 V9	
	MC L1 07	MC J3 W9	
	MC L1 08	MC J3 X9	
	MC R1 60	MC M1 09	
	MC R1 62	MC M1 08	
	MC R1 64	MC M1 07	
	MC R1 66	MC M1 06	
	MC R1 70	MC M1 04	
	MC R1 72	MC M1 03	
	MC R1 74	MC M1 02	
	MC R1 76	MC M1 01	
	MC R1 40	MC M2 09	
	MC R1 42	MC M2 08	
	MC R1 44	MC M2 07	
	MC R1 46	MC M2 06	
	MC R1 50	MC M2 04	
	MC R1 52	MC M2 03	
	MC R1 54	MC M2 02	
	MC R1 56	MC M2 01	
	MC R1 20	MC M3 09	
	MC R1 22	MC M3 08	
	MC R1 24	MC M3 07	
	MC R1 26	MC M3 06	
	MC R1 30	MC M3 04	
	MC R1 32	MC M3 03	
	MC R1 34	MC M3 02	
	MC R1 36	MC M3 01	
	MC R1 00	MC M4 09	
	MC R1 02	MC M4 08	
	MC R1 04	MC M4 07	
	MC R1 06	MC M4 06	
	MC R1 10	MC M4 04	
	MC R1 12	MC M4 03	
	MC R1 14	MC M4 02	
	MC R1 16	MC M4 01	
	MC P1 60	MC N1 09	
	MC P1 62	MC N1 08	
	MC P1 64	MC N1 07	
	MC P1 66	MC N1 06	
	MC P1 70	MC N1 04	
	MC P1 72	MC N1 03	
	MC P1 74	MC N1 02	
	MC P1 76	MC N1 01	
	MC P1 40	MC N2 09	
	MC P1 42	MC N2 08	
	MC P1 44	MC N2 07	
	MC P1 46	MC N2 06	
	MC P1 50	MC N2 04	
	MC P1 52	MC N2 03	
	MC P1 54	MC N2 02	
	MC P1 56	MC N2 01	
	MC P1 20	MC N3 09	
	MC P1 22	MC N3 08	
	MC P1 24	MC N3 07	
	MC P1 26	MC N3 06	
	MC P1 30	MC N3 04	
	MC P1 32	MC N3 03	
	MC P1 34	MC N3 02	
	MC P1 36	MC N3 01	
	MC P1 00	MC N4 09	
	MC P1 02	MC N4 08	
	MC P1 04	MC N4 07	
	MC P1 06	MC N4 06	
	MC P1 10	MC N4 04	
	MC P1 12	MC N4 03	
	MC P1 14	MC N4 02	
	MC P1 16	MC N4 01	

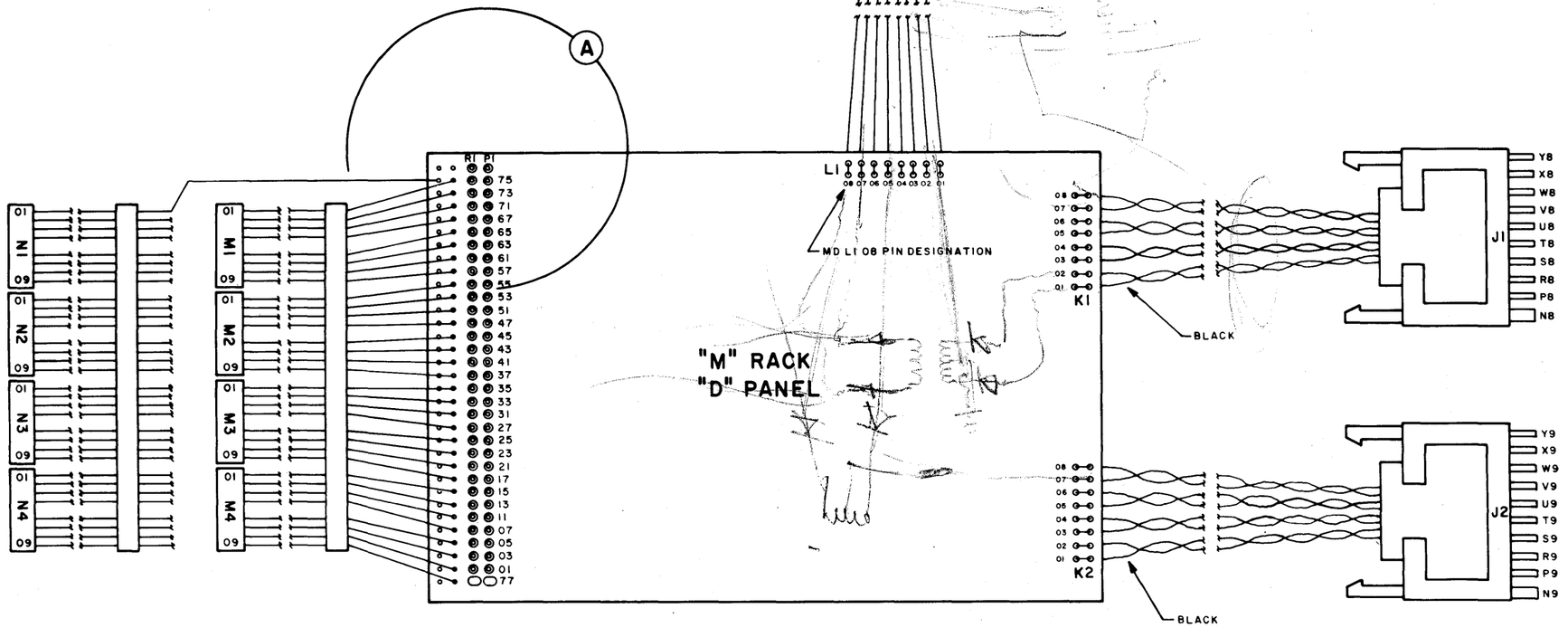
FIGURE 6.11-15
TRANSFORMER BOARD LAYOUT "C"
(X-EVEN)



DETAIL A



DRAC



	TO	FROM	
ADDRESS SWITCHES	MD K2 01	MD J2 P9	TWISTED PAIR
	MD K2 02	MD J2 R9	TWISTED PAIR
	MD K2 03	MD J2 S9	TWISTED PAIR
	MD K2 04	MD J2 T9	TWISTED PAIR
	MD K2 05	MD J2 U9	TWISTED PAIR
	MD K2 06	MD J2 V9	TWISTED PAIR
	MD K2 07	MD J2 W9	TWISTED PAIR
	MD K2 08	MD J2 X9	TWISTED PAIR
ADDRESS SWITCHES	MD K1 01	MD J1 P8	TWISTED PAIR
	MD K1 02	MD J1 R8	TWISTED PAIR
	MD K1 03	MD J1 S8	TWISTED PAIR
	MD K1 04	MD J1 T8	TWISTED PAIR
	MD K1 05	MD J1 U8	TWISTED PAIR
	MD K1 06	MD J1 V8	TWISTED PAIR
	MD K1 07	MD J1 W8	TWISTED PAIR
	MD K1 08	MD J1 X8	TWISTED PAIR
ADDRESS CURRENT DRIVERS	MD L1 01	MD J3 K9	
	MD L1 02	MD J3 J9	
	MD L1 03	MD J3 H9	
	MD L1 04	MD J3 F9	
	MD L1 05	MD J3 E9	
	MD L1 06	MD J3 D9	
	MD L1 07	MD J3 C9	
	MD L1 08	MD J3 B9	
	MD RI 75	MD M1 01	
	MD RI 73	MD M1 02	
	MD RI 71	MD M1 03	
	MD RI 67	MD M1 04	
	MD RI 65	MD M1 06	
	MD RI 63	MD M1 07	
	MD RI 61	MD M1 08	
	MD RI 57	MD M1 09	
	MD RI 55	MD M2 01	
	MD RI 53	MD M2 02	
	MD RI 51	MD M2 03	
	MD RI 47	MD M2 04	
	MD RI 45	MD M2 06	
	MD RI 43	MD M2 07	
	MD RI 41	MD M2 08	
	MD RI 37	MD M2 09	
	MD RI 35	MD M3 01	
	MD RI 33	MD M3 02	
	MD RI 31	MD M3 03	
	MD RI 27	MD M3 04	
	MD RI 25	MD M3 06	
	MD RI 23	MD M3 07	
	MD RI 21	MD M3 08	
	MD RI 17	MD M3 09	
	MD RI 15	MD M4 01	
	MD RI 13	MD M4 02	
	MD RI 11	MD M4 03	
	MD RI 07	MD M4 04	
	MD RI 05	MD M4 06	
	MD RI 03	MD M4 07	
	MD RI 01	MD M4 08	
	MD RI 77	MD M4 09	
	MD PI 75	MD N1 01	
	MD PI 73	MD N1 02	
	MD PI 71	MD N1 03	
	MD PI 67	MD N1 04	
	MD PI 65	MD N1 06	
	MD PI 63	MD N1 07	
	MD PI 61	MD N1 08	
	MD PI 57	MD N1 09	
	MD PI 55	MD N2 01	
	MD PI 53	MD N2 02	
	MD PI 51	MD N2 03	
	MD PI 47	MD N2 04	
	MD PI 45	MD N2 06	
	MD PI 43	MD N2 07	
	MD PI 41	MD N2 08	
	MD PI 37	MD N2 09	
	MD PI 35	MD N3 01	
	MD PI 33	MD N3 02	
	MD PI 31	MD N3 03	
	MD PI 27	MD N3 04	
	MD PI 25	MD N3 06	
	MD PI 23	MD N3 07	
	MD PI 21	MD N3 08	
	MD PI 17	MD N3 09	
	MD PI 15	MD N4 01	
	MD PI 13	MD N4 02	
	MD PI 11	MD N4 03	
	MD PI 07	MD N4 04	
	MD PI 05	MD N4 06	
	MD PI 03	MD N4 07	
	MD PI 01	MD N4 08	
	MD PI 77	MD N4 09	

Switches Swads

Switches Swads

FIGURE 6.11-16
TRANSFORMER BOARD LAYOUT "D"
(X-ODD)

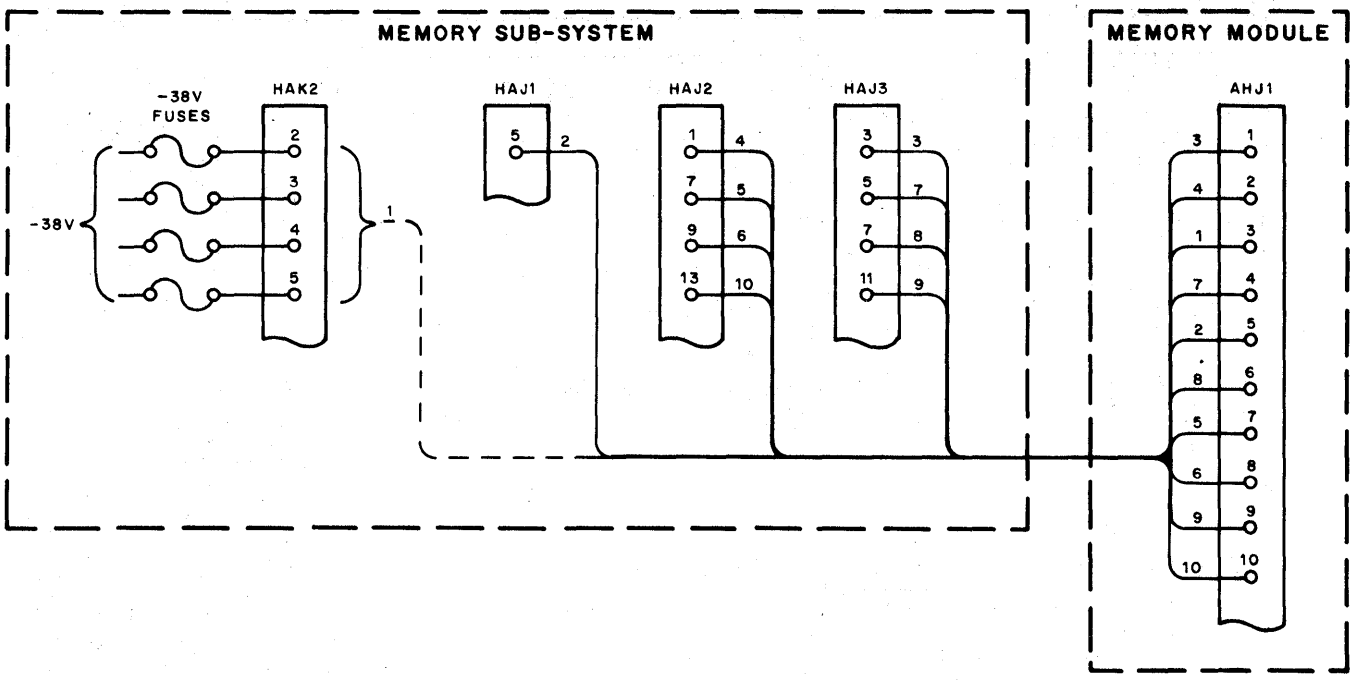


FIGURE 6.11-4
CABLE ASSEMBLY - MODULES 0, 1, 4 & 5

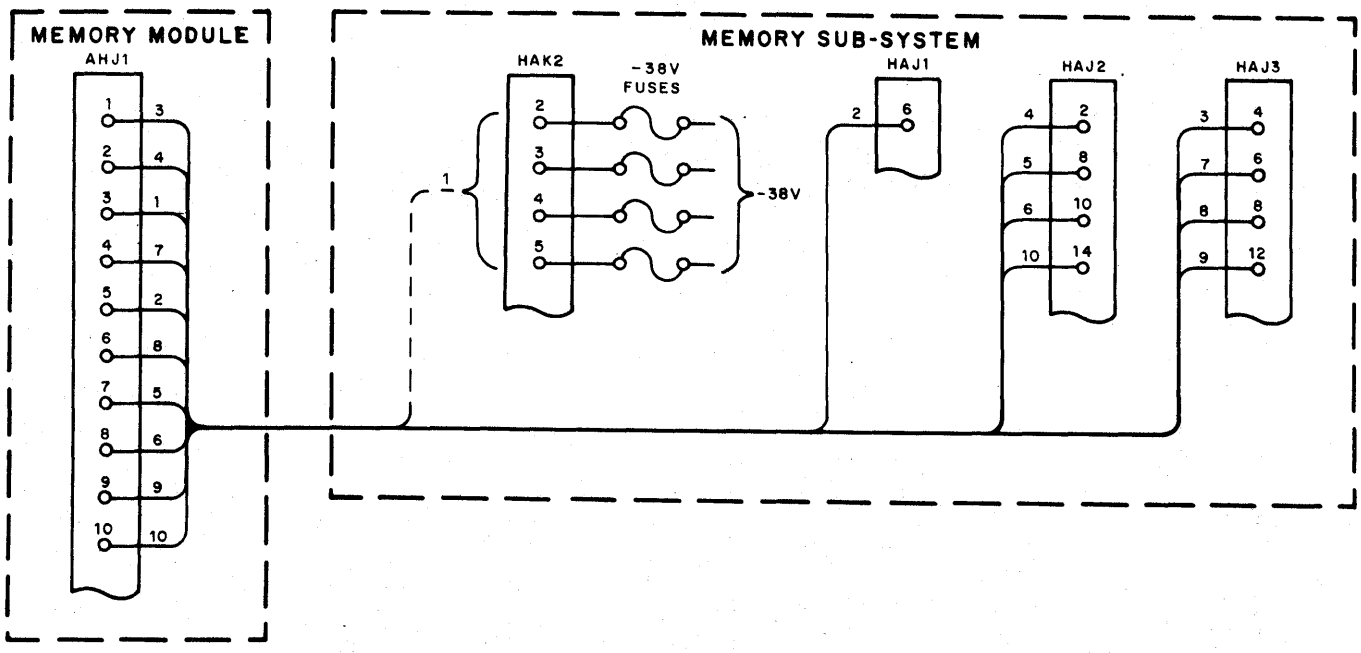


FIGURE 6.11-5
CABLE ASSEMBLY - MODULES 2, 3, 6 & 7

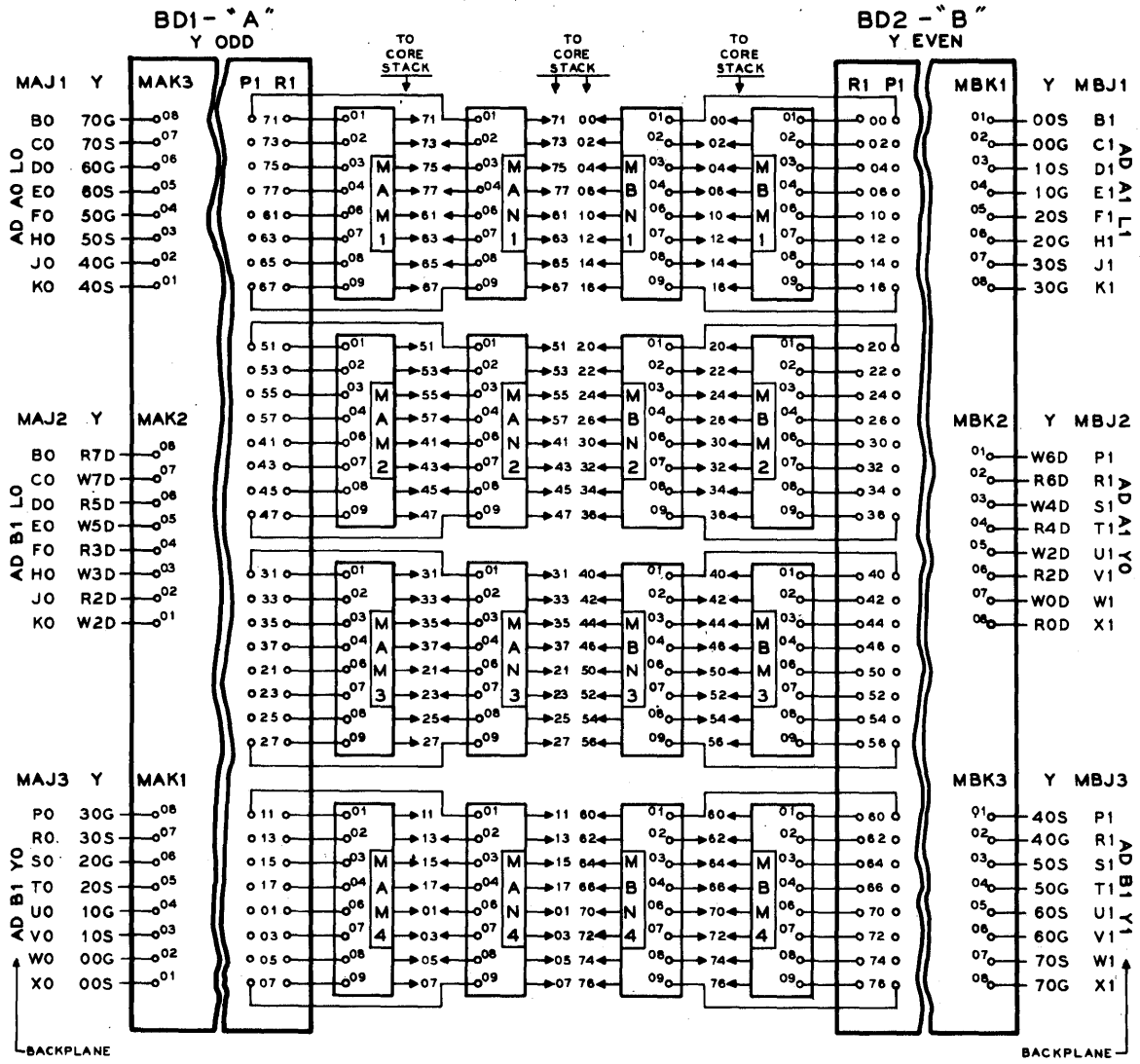


FIGURE 6.11-17

TRANSFORMER BOARD CONNECTORS "A" & "B"

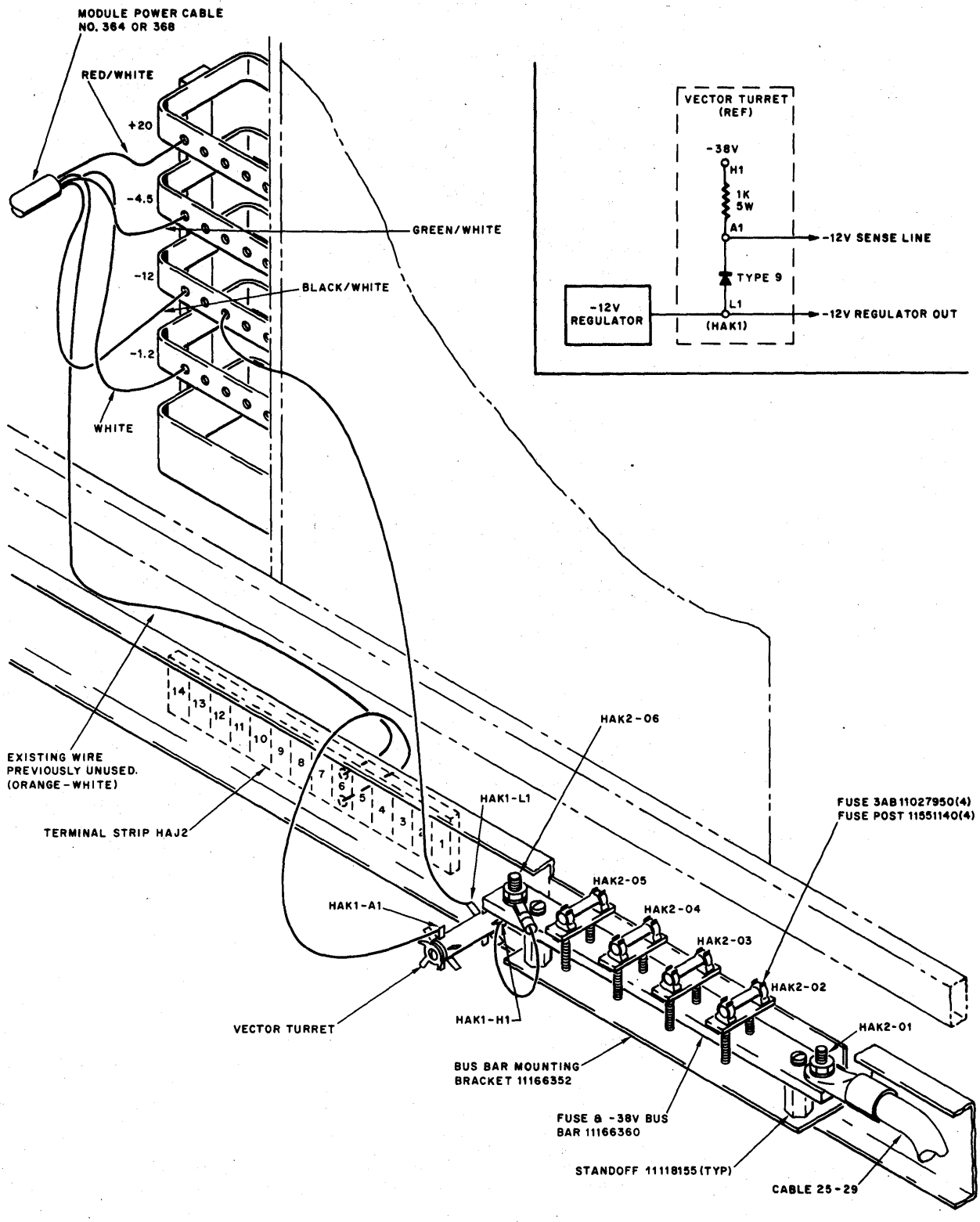


FIGURE 6.11-18
-12V SENSE WIRING & -38V FUSES

6.12 SWEEP DELAY ADJUSTMENT

Some marginal troubles occur only when the CYCLE switch is in the continuous position. If the scope is SYNCED on the Zero Address, then there will be a large amount of trace jitter in a high Address location. In order to use the smallest amount of Sweep Delay and display the correct Address on the scope, the following procedure may be used:

1. Decode MAR octally.
2. Add the numbers from Table 6.12-1.
3. Set the Delay to the total established from Table 6.12-1.
4. Sync on the pin indicated by Table 6.12-1 (External Positive Sync).
5. The desired waveshape will be displayed near the start of Sweep.

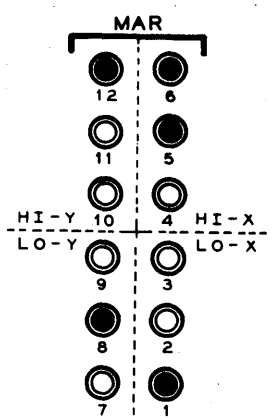
TABLE 6.12-1.

LOW X	HIGH X	LOW Y	HIGH Y SYNC		
0 = 0	0 = 0	0 = 0	0 = SWAD	Y00S	AD B1 R4
1 = 4	1 = 32	1 = 256	1 = SWAD	Y10S	AD B1 R5
2 = 8	2 = 64	2 = 512	2 = SWAD	Y20S	AD B1 R7
3 = 12	3 = 96	3 = 768	3 = SWAD	Y30S	AD B1 R9
4 = 16	4 = 128	4 = 1024	4 = SWAD	Y40S	AD B2 R0
5 = 20	5 = 160	5 = 1280	5 = SWAD	Y50S	AD B2 R2
6 = 24	6 = 192	6 = 1536	6 = SWAD	Y60S	AD B2 R7
7 = 28	7 = 224	7 = 1792	7 = SWAD	Y70S	AD B2 R9

As an example, assume it is necessary to look at the Sense Amplifier output during Address 4261. This Address can be decoded octally by looking at the MAR Register on the Maintenance Panel.

MAR 1, 5, 6, 8 and 12 are ON (octal 4261), therefore;

LO - X = 1	4μs
HI - X = 6	192μs
LO - Y = 2	512μs
Add individual Delays for TOTAL	708μs
SET SWEEP DELAY TO	708μs



HI - Y = 4 SYNC AD B2 R0

Setting the Sweep Delay to 708μs is a problem in itself. The Time/cm or Delay Time switch could be set to 500μs and the Delay Time Multiplier set to 1.41:

$$1.416 = \frac{708\mu S}{500\mu s}$$

or, the Delay could be set to 100μs and the Multiplier set to 3.54:

$$3.54 = \frac{708\mu s}{200\mu s}$$

In any event, the desired waveshape will be displayed near the start of the Sweep.

6.13 USEFUL TEST POINTS

TABLE 6.13-1

LEVEL	MONITOR POINT	LEVEL	MONITOR POINT
-15V	AC D4 B4	MIHM	AC C3 V9
+30V	AC D9 K3	MW2M	AD C4 X1
MS1M	AD C0 X6	MICM	AD C4 W5
MR2M	AD C1 X1	TØDM	AC D3 U0
STTP	AD C2 V4	VARIABLE BIAS	AA C7 B7
MRWP	AD C2 U5	ACDF	AC B4 V3

NOTE: ACDF SHOULD BE ON OR TRUE FOR ABOUT 240ns TO 270ns AND SHOULD OCCUR AT CLOCK FREQUENCY.

Use Table 6.13-2 for Test Points that can be used to check the Clock lines at the end of their respective circuits.

TABLE 6.13-2

CLOCK PACKAGE OUTPUT	CIRCUIT LIST NO.	MONITOR POINTS	
AA B1 P0	68.00.00 H68	AA C7 B7	CCP-1
AA B1 R0	68.00.00 H78	AA C7 B8	CCP-2
AA B1 S0	68.00.00 H88	AA C7 E7	CCP-3
AA B1 T0	68.00.00 H98	AA C7 F7	CCP-4
AA C3 P1	68.00.00 J18	AA C7 K7	CCP-5
AD C0 R1	68.00.00 J28	AA C7 K8	CCP-6

The Clocks should be .155μs $^{\pm 5\mu s}$ wide, occurring 1μs apart, measured at the -2V level.

6.14 POWER SUPPLY TROUBLESHOOTING

The Regulator Packages may be operated with no LOAD. The LOAD can be removed by taking out all Circuit Packages associated with a specific Regulator.

To help locate a short circuit, groups of cards can be removed without causing any damage, such as all of the Sense Amplifiers, Address Current Drivers, Address Switches and Inhibit Current Drivers. Flip-flops can be removed in Logical Units, such as all of MIR, etc.

If DC Power does not stay ON, and a Power Supply Failure is indicated in the Memory Unit, the following procedure can be used:

1. Remove all critical packages; DRIC, DRAC, SWAD, Sense Amplifiers, Address Current Drivers, etc.
2. Remove the High Voltage Switch Package at AD D1 N2. This will prevent DC from dropping on a Power Failure.
3. Locate the trouble causing Power to drop, and then replace the High Voltage Switch Package in AD D1 N2.

Check Tracking of the -6T with -12V

This can be done by putting a meter between -6T and -12V. The difference should remain constant within 0.1V, as -12V is varied from -11V to -13V.

Overcurrent Sensing

The over current potentiometers are pre-set and should NOT be adjusted. Pre-selection of Parallel Resistors located on the Display Panel allow any -30V Regulator package to be interchangeable between READ, WRITE and INHIBIT.

Under Voltage Sensing

1. Check Under Voltage Sensing on EACH -30V Regulator and the +30V Regulator by individually removing each Regulator fuse in the Display Panel. When a fuse is removed, DC Power should drop. The corresponding Voltage Indicator and the Low Indicator should come ON.
2. The System and Local Power lights should be OFF.
3. Replace the fuse, and Power should remain OFF.
4. Depress the RESET button and the Failure Indicators should go OFF, and Power should come UP.

Over Voltage Sensing

Over Voltage Sensing can be checked as follows:

1. Short out the Series Regulator Transistors on the Regulator under test.
2. With Power ON, momentarily ground the points indicated in Table 6.14-1.
3. DC should drop, and the corresponding Voltage Indicator and the High Indicator should come ON.

TABLE 6.14-1

PIN TO GROUND	FUNCTION	INDICATOR
AC D5 T0	-30I OV	-30I and Hi
AC D5 T5	-30W OV	-30W and Hi
AC D6 T0	-30R OV	-30R and Hi

To check the +30V Over Voltage Sensing, a 50 ohm 5W Resistor can be momentarily placed between AC D9 K3 and AC D9 B3. Use extreme care, the above mentioned points on the Backplane are +30V and +50V respectively. Power should drop and the +30V Indicator and High Indicator should come ON.

Proper Sequencing of Regulators

The following procedure can be used to insure that the +30V Regulator turns ON after all three -30V Regulators have turned ON.

1. Sync the scope (+) on AC D8 B9 (-30V on Control).
2. Place B probe on AC D9 K3 (+30V).
3. Move A probe to the indicated Test Points and turn DC ON and OFF each time.

   AC D5 H6 -30VI

   AC D6 H6 -30VR

   AC D8 H6 -30VW
4. Each of the -30V Regulators should turn ON before the +30V Regulator.

-1.2V, -12V, and -4.5V Sensing

Sensing of these Memory Sub-System Voltages are provided through Module "0". If there is a second Sub-System, it is provided for through Module "4".

Table 6.14-2 should be checked to insure the circuitry for this sensing.

1. Check the following points for voltage:

MONITOR POINT	VOLTAGE	FUNCTION
AD D0 A9	-1.2V	-1.2 Sense
AA D0 B9	-12V	-12 Sense
AA D0 D9	-4.5V	-4.5 Sense

2. Check for continuity between the following points:

   a. AA B0 A5 to Ground - Sense Ground
   b. AA B0 B5 to AA D0 E9 - Thermal Sense
   c. AA B0 C5 to AA D0 C9 - -12VI Sense

TABLE 6.14-2. Terminal Board Voltage Locations.

	LOCATION	VOLTAGE	LOCATION	VOLTAGE
REGULATORS	CSN1	-1.2	AHJ1-01	-120.0
	CSM1	-12.0	AHJ1-02	-100.0
	CSL1	-4.5	AHJ1-03	-38.0
	CSK1	+20.0	AHJ1-04	-24.0
BARRIER STRIPS	HA K2 01	-38.0	AHJ1-05	+19.0
	HA J1 03	-33.0 (6μs Mem.)	AHJ1-06	+50.0
	HA J1 05	+19.0	AHJ1-07	+100.0
	HA J2 01	-100.0	AHJ1-08	+20/-100(MC)
	HA J2 03	-120.0	AHJ1-09	-24.0(DC LOCKOUT)
	HA J2 05	-100.0	AHJ1-10	GROUND
	HA J2 07	+100.0	AJJ1-01	+20.0
	HA J2 09	+20/-100(MC)	AJJ1-02	-4.5
	HA J3 07	+50.0	AJJ1-03	-12.0
	HA J3 09	+74.0 (6μs Mem.)	AJJ1-04	-1.2
	HA J3 11	-24.0(DC LOCKOUT)	AJJ1-07	+20.0
			AJJ1-08	-4.5
			AJJ1-09	-12.0
			AJJ1-10	-1.2

6.15 MEMORY STACK CURRENT REQUIREMENTS

READ Address Currents

The Read current pulses in all "X" and "Y" Address lines shall meet the following specifications:

1. The Read current in any "X" or "Y" Address line shall be within 15 ma of the Read current in any other Address line, measured at 800 ns from the Leading Edge of the MR2M Timing pulse.
2. The droop of the current as measured from the 500ns point (from the Leading Edge of MR2M) to the point that the current turns OFF, shall be less than 5 ma at any "X" or "Y" line.

WRITE Address Currents

The Write currents shall meet the same specifications as called for in the Read currents listed above.

INHIBIT Currents

All the Inhibit shall meet the following specifications:

1. All the Inhibit currents shall be within 10 ma of each other as measured at a point 800 ns from the Leading Edge of the Inhibit Timing pulse (M1HM).
2. The current droop, as measured from the 500ns point (from the Leading Edge of the M1HM pulse) to the point the current turns OFF, should be less than 5 ma at any bit.

6.16 CURRENT DRIVER & ADDRESS SWITCH TROUBLESHOOTING

This Section will verify current flow from the Address Current Drivers (DRAC) to the Memory Address Switches (SWAD).

1. Set the Maintenance Switches as indicated .
   a. Ignore Error
   b. Continuous Cycle
   c. Manual
   d. Count "X" and "Y"
   e. Stop On Final Address OFF

2. Step 2 verifies the LO order X to the HI order X EVEN circuits.
   a. Sync a scope on AD C2 H0 (CØYD).
   b. Set the horizontal sweep for 5μs/cm.
   c. Place a current probe around the cable from AC A3 Y9 to Matrix Board "C".

      These lines are XW0D, XR0D, XW2D, XR2D, XW4D, XR4D, XW6D, and XR6D.

      The Wave Form displayed should be similar to Figure 6.16-1.

      Each group of 2 current pulses is a Read and Write current from one of the above mentioned drivers.

      The current amplitudes should be approximately 250ma.
   d. Place the remaining probe on AD A4 U0 (CØYD) and switch to Alternate Mode.
   e. Adjust the horizontal sweep so that 2 pulses of CØYD are displayed on the screen. (CØYD occurs every 256μs.)

      The pulse train should be a group of eight current pulses occurring every 32μs.

      The current Wave Form should be similar to Figure 6.16-3.

      NOTE

      See Step 8 for Troubleshooting hints.

3. Step 3 verifies the LO order X to the HI order X ODD circuits.
   a. Set the horizontal sweep for 5μs/cm.
   b. Place a current probe around the cable from AC B3 L9 to Matrix Board "D".

      These lines are XW1D, XR1D, XW3D, XR3D, XW5D, XR5D, XW7D, and XR7D.

The Wave Form displayed should be similar to Figure 6.16-2.

The current amplitudes should be approximately 250ma.

c. Adjust the horizontal sweep so that the two pulses of CØYD are displayed on the screen. CØYD occurs every 256μs.

The pulse train should be a group of eight current pulses occurring every 32μs.

The current Wave Form should be similar to Figure 6.16-3.

NOTE

See Step 8 for Troubleshooting hints.

d. With the horizontal sweep set as in Step 3c (CØYD displayed twice on the screen), scope the output of the "X" SWADs and check that they are on their correct times.

Each SWAD output will be a group of eight pulses (lasting for 32μs) occurring at the time stated in Table 6.16-1, in reference to CØYD.

TABLE 6.16-1

SWAD	TEST POINT	START	FINISH
X00S	AC B3 R4	0 μs	32 μs
X10S	AC B3 R5	32 μs	64 μs
X20S	AC B3 R0	64 μs	96 μs
X30S	AC B3 R2	96 μs	128 μs
X40S	AC B2 R7	128 μs	160 μs
X50S	AC B2 R9	160 μs	192 μs
X60S	AC B2 R0	192 μs	224 μs
X70S	AC B2 R2	224 μs	256 μs

4. Set the Maintenance Switches as indicated.
   a. Ignore Error
   b. Continuous Cycle
   c. Manual
   d. Inhibit Count "X"
   e. Count "Y"
   f. Stop On Final Address OFF
   g. X01F thru X06F ON
5. Step 5 verifies the LO order Y to the HI order Y EVEN circuits.
   a. Sync the scope (+) on AC A1 L8 (CAG 005).
   b. Set the horizontal sweep for 5μs/cm.
   c. Place a current probe around the cable from AD A1 Yo to Matrix Board "B".

These lines are YW0D, YR0D, YW2D, YR2D, YW4D, YR4D, YW6D, and YR6D.

The Wave Form displayed should be similar to Figure 6.16-1.

Each group of 2 current pulses is a Read and Write current from one of the above mentioned drivers.

The current amplitudes should be approximately 250ma.

d. Place the remaining probe on AC A1 N8 (CAG 005).

e. Adjust the horizontal sweep so that the 2 pulses of CAG 005 are displayed on the screen. CAG 005 occurs every 256μs.

The pulse train should be a group of eight current pulses occurring every 32μs.

The current Wave Form should be similar to Figure 6.16-3.

NOTE

See Step 8 for Troubleshooting hints.

6. Step 6 verifies the LO order Y to the HI order Y ODD circuits.

a. Place a current probe around the cable from AD B1 LO to Matrix Board "A".

These lines are YW1D, YR1D, YW3D, YR3D, YW5D, YR5D, YW7D, and YR7D.

The Wave Form displayed should be similar to Figure 6.16-2.

The current amplitudes should be approximately 250ma.

b. Adjust the horizontal sweep so that the 2 pulses of CAG 005 are displayed on the screen. CAG 005 occurs every 256μs.

The pulse train should be a group of eight current pulses occurring every 32μs.

The current Wave Form should be similar to Figure 6.16-3.

c. With the horizontal sweep set as in Step 6b (CAG 005 displayed twice on screen), scope the output of the "Y" SWADs and check that they are on at their correct time.

Each SWAD output will be a group of eight pulses (lasting for 32μs) occurring at the time stated in Table 6.16-2, in reference to CAG 005.

TABLE 6.16-2

SWAD	TEST POINT	START	FINISH
Y00S	AD B1 R4	0 µs	32 µs
Y10S	AD B1 R5	32 µs	64 µs
Y20S	AD B1 R7	64 µs	96 µs
Y30S	AD B1 R9	96 µs	128 µs
Y40S	AD B2 R0	128 µs	160 µs
Y50S	AD B2 R2	160 µs	192 µs
Y60S	AD B2 R7	192 µs	224 µs
Y70S	AD B2 R9	224 µs	256 µs

7. Step 7 verifies the Address Current Amplitude.

   a. Place the Memory in a Continuous Manual Mode and observe the current in the Stack.

   b. Sync the scope on MS1M, AD C0 X6.

   c. Set the horizontal sweep for 1µs/cm, and 200ma/cm.

   d. With a current probe, observe each "X" and "Y" drive line in the Stack for the appropriate signal.

   Points to look for:

   1. Approximate amplitude 250ma.
   2. Correct polarity of signal relative to adjacent lines.
   3. Wave Form should be similar to Figure 6.18-5.

   NOTE

   The Wave Form may have opposite polarity depending upon how the probe is placed around the wire.

8. Troubleshooting Hints

   a. When observing Wave Forms similar to Figure 6.16-3 and any group of eight pulses are missing, it is most likely the Address Switch (SWAD) used at that time which is bad.

   Use Table 6.16-3 to determine which SWAD may be bad.

   b. When observing Wave Forms similar to Figure 6.16-3 and any one current pulse is missing every 32µs, most likely a Read or Write Driver of the group being observed is bad.

   c. When observing Wave Forms similar to Figure 6.16-3 and any one current pulse is missing, most likely a diode on the Matrix Board is bad.

   Further reference to one of the following Schematics may be helpful.

Matrix Board Schematic - Panel "A" Figure 6.11-7.
Matrix Board Schematic - Panel "B" Figure 6.11-8.
Matrix Board Schematic - Panel "C" Figure 6.11-9.
Matrix Board Schematic - Panel "D" Figure 6.11-10.

TABLE 6.16-3

TIME IN μs		STEP NO.	SWAD	LOCATION
FROM	TO			
0	32	2	X00S	AC B3 N4
		5	Y00S	AD B1 N4
32	64	3	X10S	AC B3 N4
		6	Y10S	AD B1 N4
64	96	2	X20S	AC B3 N0
		5	Y20S	AD B1 N7
96	128	3	X30S	AC B3 N0
		6	Y30S	AD B1 N7
128	160	2	X40S	AC B2 N7
		5	Y40S	AD B2 N0
160	192	3	X50S	AC B2 N7
		6	Y50S	AD B2 N0
192	224	2	X60S	AC B2 N0
		5	Y60S	AD B2 N7
224	256	3	X70S	AC B2 N0
		6	Y70S	AD B2 N7

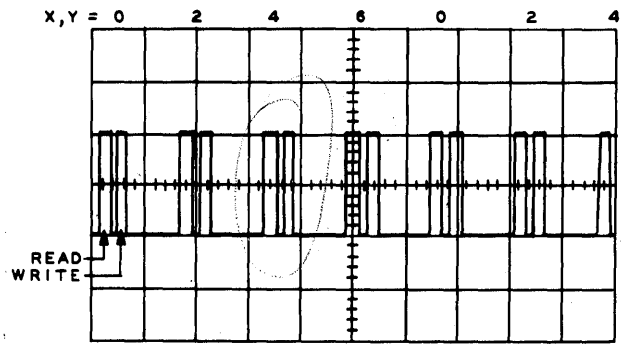


FIGURE 6.16-1

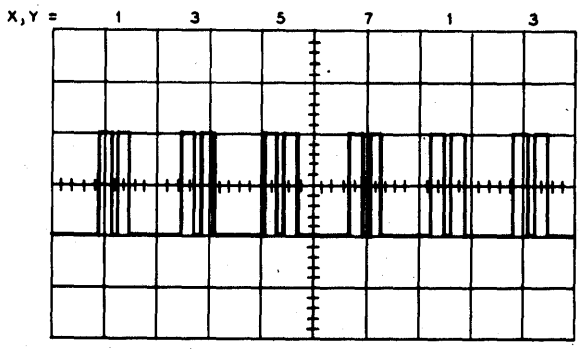


FIGURE 6.16-2

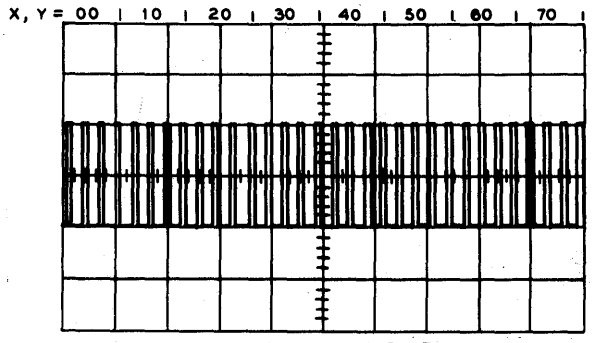


FIGURE 6.16-3

6.17 MEMORY ERROR LOGIC CHECK (MERF)

This procedure gives the Logical Condition set-ups to test the complete ERROR Logic.

NOTE

* Indicates the switch output should be TRUE with the conditions stated.

MP = Monitor Point

OP = Output Point

D.A. Page 68.20.00.0

1. * Ø/ ØAAS SW. H MP - AB A2 T2 OP - AA A2 R0

-I- + I04F • (+ I01F • I02F • I03F/
+ I01F • I02F/ • I03F
+ I01F/ • I02F • I03F
+ I01F/ • I02F/ • I03F/)
+ I04F/ • (+ I01F • I02F/ • I03F/
+ I01F/ • I02F • I03F/
+ I01F/ • I02F/ • I03F
+ I01F • I02F • I03F)

2. * Ø/ ØBAS SW. H MP - AB A2 P2 OP - AA A2 V4

-I- + I08F • (+ I05F • I06F • I07F/
+ I05F • I06F/ • I07F
+ I05F/ • I06F • I07F
+ I05F/ • I06F/ • I07F/)
+ I08F/ • (+ I05F • I06F/ • I07F/
+ I05F/ • I06F • I07F/
+ I05F/ • I06F/ • I07F
+ I05F • I06F • I07F)

D.A. Page 68.20.01.0

1. * Ø/ ØCAS SW. H MP - AB A2 X1 OP - AA A2 C0

-I- + I12F • (+ I09F • I10F • I11F/
+ I09F • I10F/ • I11F
+ I09F/ • I10F • I11F

```
                                + I09F/ • I10F/ • I11F/)
                    + I12F/ • ( + I09F • I10F/ • I11F/
                                + I09F/ • I10F • I11F/
                                + I09F/ • I10F/ • I11F
                                + I09F • I10F • I11F)
```

2. * Ø/ ØDAS SW. H MP - AB A1 P7 OP - AA A2 H4

```
        -I-  + I16F  • ( + I13F • I14F • I15F/
                        + I13F • I14F/ • I15F
                        + I13F/ • I14F • I15F
                        + I13F/ • I14F/ • I15F/)
                + I16F/ • ( + I13F • I14F/ • I15F/
                        + I13F/ • I14F • I15F/
                        + I13F/ • I14F/ • I15F
                        + I13F • I14F • I15F)
```

D.A. Page 68.20.02.0

1. * Ø/ ØEAS SW. H MP - AB A0 X3 OP - AA A4 C0

```
        -I-  + I20F  • ( + I17F • I18F • I19F/
                        + I17F • I18F/ • I19F
                        + I17F/ • I18F • I19F
                        + I17F/ • I18F/ • I19F/)
                + I20F/ • ( + I17F • I18F/ • I19F/
                        + I17F/ • I18F • I19F/
                        + I17F/ • I18F/ • I19F
                        + I17F • I18F • I19F
```

2. * Ø/ ØFAS SW. H MP - AB A0 X1 OP - AA A4 H4

```
        -I-  + I24F  • ( + I21F • I22F • I23F/
                        + I21F • I22F/ • I23F
                        + I21F/ • I22F • I23F
                        + I21F/ • I22F/ • I23F/)
                + I24F/ • ( + I21F • I22F/ • I23F/
                        + I21F/ • I22F • I23F/
                        + I21F/ • I22F/ • I23F
                        + I21F • I22F • I23F)
```

D.A. Page 68.20.03.0

1. * Ø/ ØGAS SW. H MP - AB A0 S6 OP - AA A4 R0

```
-I- + I28F  • ( + I25F • I26F • I27F/
               + I25F • I26F/ • I27F
               + I25F/ • I26F • I27F
               + I25F/ • I26F/ • I27F/)
    + I28F/ • ( + I25F • I26F/ • I27F/
               + I25F/ • I26F • I27F/
               + I25F/ • I26F/ • I27F
               + I25F • I26F • I27F)
```

2. * Ø/ ØHAS SW. H MP - AB A0 P1 OP - AA A4 V4

```
-I- + I32F  • ( + I29F • I30F • I31F/
               + I29F • I30F/ • I31F
               + I29F/ • I30F • I31F
               + I29F/ • I30F/ • I31F/)
    + I32F/ • ( + I29F • I30F/ • I31F/
               + I29F/ • I30F/ • I31F
               + I29F/ • I30F • I31F/
               + I29F • I30F • I31F)
```

D.A. Page 68.20.04.0

1. * Ø/ ØIAS SW. H MP - AB A3 T1 OP - AA A6 R5

```
-I- + I36F  • ( + I33F • I34F • I35F/
               + I33F • I34F/ • I35F
               + I33F/ • I34F • I35F
               + I33F/ • I34F/ • I35F/)
    + I36F/ • ( + I33F • I34F/ • I35F/
               + I33F/ • I34F • I35F/
               + I33F/ • I34F/ • I35F
               + I33F • I34F • I35F)
```

2. * Ø/ ØJAS SW. H MP - AB A3 P1 OP - AA A6 V9

```
-I-  + I40F  • ( + I37F • I38F • I39F/
                + I37F • I38F/ • I39F
                + I37F/ • I38F • I39F
                + I37F/ • I38F/ • I39F/)
     + I40F/ • ( + I37F • I38F/ • I39F/
                + I37F/ • I38F • I39F/
                + I37F/• I38F/ • I39F
                + I37F • I38F • I39F)
```

D.A. Page 68.20.05.0

1. * Ø/ ØKAS SW. H MP - AB A2 X9 OP - AA A9 R0

```
-I-  + I44F  • ( + I41F • I42F • I43F/
                + I41F • I42F/ • I43F
                + I41F/ • I42F • I43F
                + I41F/ • I42F/ • I43F/)
     + I44F/ • ( + I41F • I42F/ • I43F/
                + I41F/ • I42F • I43F/
                + I41F/ • I42F/ • I43F
                + I41F • I42F • I43F)
```

2. * Ø/ ØLAS SW. H MP - AB A2 P6 OP - AA A9 V4

```
-I-  + I48F  • ( + I45F • I46F • I47F/
                + I45F • I46F/ • I47F
                + I45F/ • I46F • I47F
                + I45F/ • I46F/ • I47F/)
     + I48F/ • ( + I45F • I46F/ • I47F/
                + I45F/ • I46F • I47F/
                + I45F/ • I46F/ • I47F
                + I45F • I46F • I47F)
```

D.A. Page 68.20.06.0

1. * Ø/ ØABS SW. H MP - AB A4 T7 OP - AB A1 R0

```
-I-  + I16F  • ( + I04F • I08F • I12F/
                + I04F • I08F/ • I12F
```

```
                                + I04F/ • I08F • I12F
                                + I04F/ • I08F/ • I12F/)
                        + I16F/ • ( + I04F/ • I08F/ • I12F
                                + I04F/ • I08F • I12F/
                                + I04F/ • I08F/ • I12F
                                + I04F • I08F • I12F)
```

2. * Ø/ ØBBS SW. H MP - AB A4 P7 OP - AB A1 V4

```
        -I-  + I32F  • ( + I20F • I24F • I28F/
                        + I20F • I24F/ • I28F
                        + I20F/ • I24F • I28F
                        + I20F/ • I24F/ • I28F/)
                + I32F/ • ( + I20F/ • I24F/ • I28F
                        + I20F/ • I24F • I28F/
                        + I20F • I24F/ • I28F/
                        + I20F • I24F • I28F)
```

D.A. Page 68.20.07.0

1. * Ø/ ØCBS SW. H MP - AB A4 X6 OP - AB A3 R5

```
        -I-  +I48F  • ( + I36F • I40F • I44F/
                        + I36F • I40F/ • I44F
                        + I36F/ • I40F • I44F
                        + I36F/ • I40F/ • I44F/)
                + I48F/ • ( + I36F • I40F/ • I44F/
                        + I36F/ • I40F • I44F/
                        + I36F/ • I40F/ • I44F
                        + I36F • I40F • I44F)
```

2. * Ø/ PERL SW. H MP - AB C4 U4 OP - AB A3 V9

```
        -I-  + I49F  • ( + I16F • I32F • I48F/
                        + I16F • I32F/ • I48F
                        + I16F/ • I32F • I48F
                        + I16F/ • I32F/ • I48F/)
                + I49F/ • ( + I16F • I32F/ • I48F/
                        + I16F/ • I32F • I48F/
                        + I16F/ • I32F/ • I48F
                        + I16F • I32F • I48F)
```

6.18 WAVE FORMS

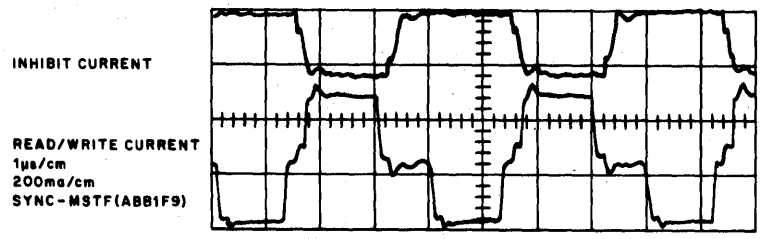


FIGURE 6.18-1

Running Uniform Complement Normal (All Zeros)
Inhibit Count of Address
Current Probe on Inhibit Line
Current Probe on Selected Address Line

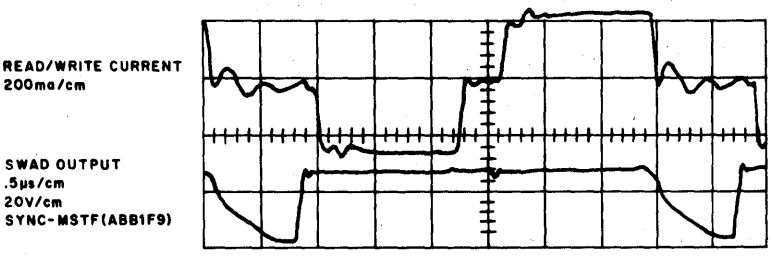


FIGURE 6.18-2

Running Uniform Complement Normal (All Zeros)
Inhibit Count of Address
Current Probe on Selected Address Line
Voltage Probe on Selected SWAD Output

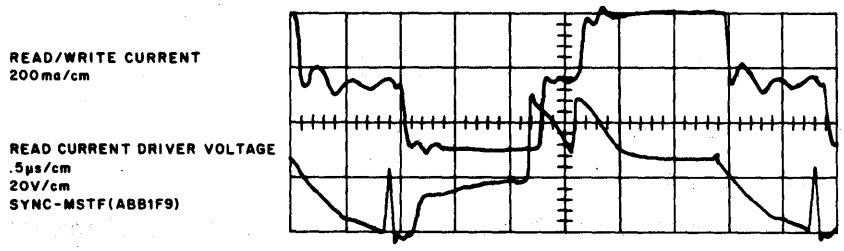


FIGURE 6.18-3

Running Uniform Complement Normal (All Zeros)
Inhibit Count of Address
Current Probe on Selected Address Line
Voltage Probe on Selected Current Driver Output

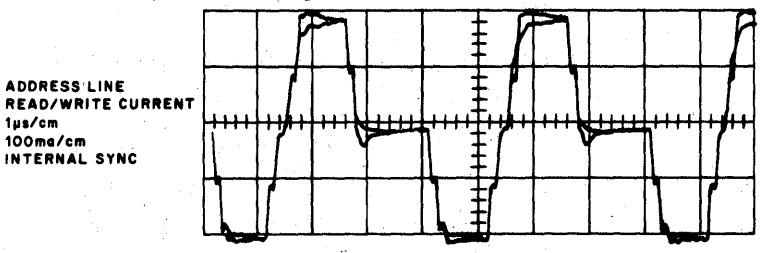


FIGURE 6.18-4

Current Probe on Address Line Y - 00
Running Worse Case Checkerboard (PCCL) Through All Addresses

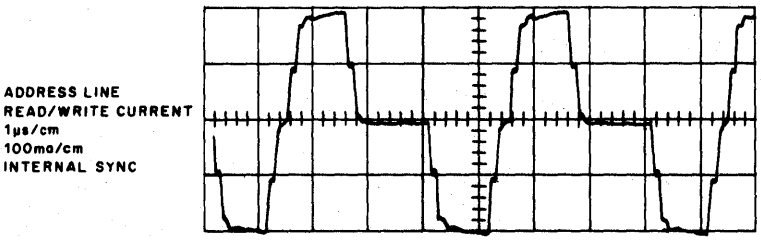


FIGURE 6.18-5

Current Probe on Address Line Y - 00
Running Uniform True Normal (All Ones) Through all Addresses

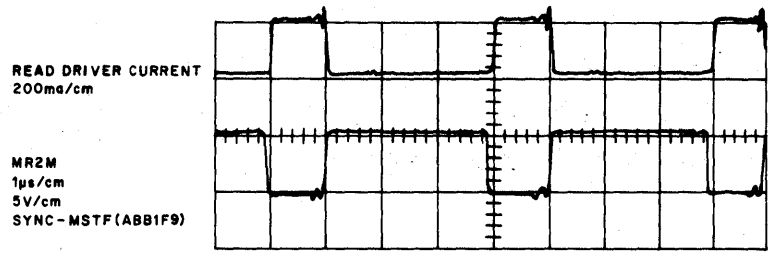


FIGURE 6.18-6

Running Uniform True Normal (All Ones)
Inhibit Count of Address
Current Probe on Read Current Driver Line to Transformer Board
Voltage Probe on MR2M Output

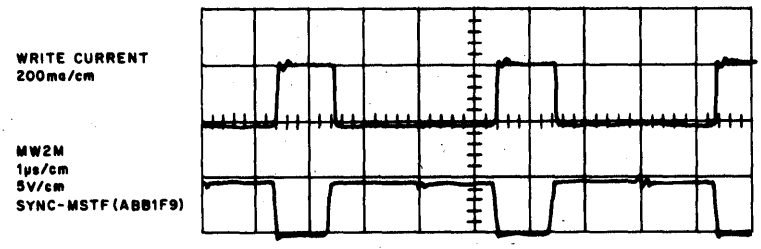


FIGURE 6.18-7

Running Uniform True Normal (All Ones)
Inhibit Count of Address
Current Probe on Selected Write Driver Line to Transformer Board
Voltage Probe on MW2M Multi Output

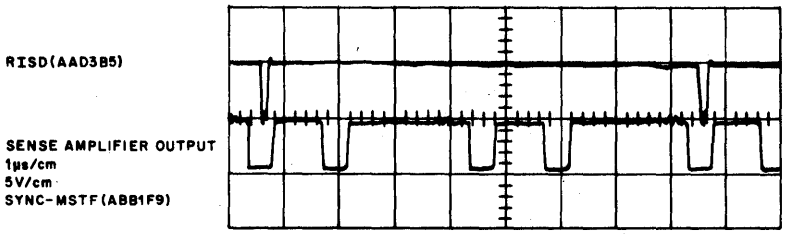


FIGURE 6.18-8

Running Uniform True Normal (All Ones)
Cycling Through All Addresses

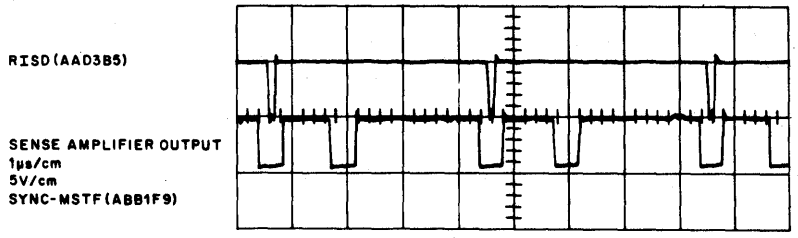


FIGURE 6.18-9

Manually Reading All Ones
Cycling Through All Addresses

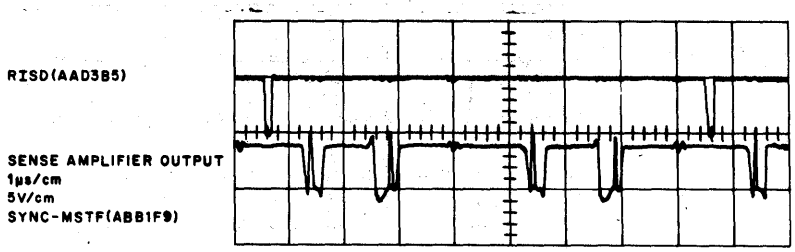


FIGURE 6.18-10

Running Uniform Complement Normal (All Zeros)
Cycling Through All Addresses

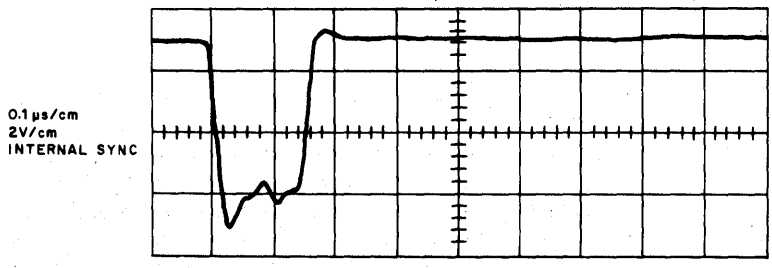


FIGURE 6.18-11

Clock Pulse On "A" and "B" Panels

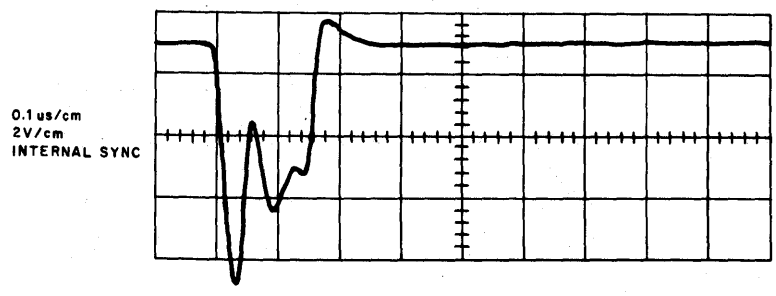


FIGURE 6.18-12

Clock Pulse On "C" and "D" Panels

6.19 MISCELLANEOUS TROUBLESHOOTING HINTS

Address Register Count Logic Check

The following procedure can be used to check the Address Count Logic circuits:

1. Select mode of operation: LOCAL - UNIFORM - MANUAL - CONTINUOUS CYCLE - STOP ON FINAL ADDRESS.

   a. Sync scope on MSTL (AD C1 F7).

   b. Observe the time that it takes for CAG 005 (AC A1 L8) to go TRUE each time the START button is depressed.

   NOTE

   CAG 005 will be TRUE on Final Address, all flip-flops = 1.

   c. Using the 2ms/cm sweep, CAG 005 should go TRUE at approximately 16.4ms (1 cycle per Address). Any discrepancy over 400μs should be investigated.

2. Select mode of operation: LOCAL-UNIFORM-AUTOMATIC-CONTINUOUS CYCLE-PCCL-STOP ON FINAL ADDRESS.

   a. Sync scope on MSTL (AD C1 F7).

   b. Observe CAG 005 (AC A1 L8).

   c. Set scope for 10ms/cm. Depress START button and CAG 005 should go TRUE in approximately 65.5ms (4 cycles per Address).

INDEX - SECTION 7

7. INSTALLATION

Printed in U.S.A.

7.1 INTRODUCTION

Installation procedures outlined in this section are for the B5261 and the B461 Units. Site preparation (as covered in the Installation Planning Manual) is assumed to be completed in accordance with customer specifications and pre-installation planning.

All packing material used for shipping should be removed and discarded or returned as directed. Further information such as power, floor space, and layout requirements may be obtained from the installation Planning Manual.

Installation and check out of the Memory Storage Unit will follow the physical location, leveling, and bolting together of the Main Frame Cabinets. It also includes the check out of Primary Power and Cabinet Regulators as described in the B5370 Power Supply Manual, Section 5.

The following installation procedure pertains to the B461 Memory Module and the B5261 Memory Core Storage Unit.

1. A B5500 System may consist of from 1 to 8 B461 Units, making up 1 or 2 B5261 Units.
2. Addition of one or more B461 Units may take place at any time.
3. When a fifth B461 Unit is installed, a second B5261 Core Memory Sub-System must also be installed.
4. Information necessary for installation or addition of all eight B461 Units (two complete B5261 Units) is included in Section 7 of this manual.
5. A complete Cable List is included for eight Modules (two cabinets). The Cable Lists are for a maximum System; therefore, those cables for units which are not part of a specific System will not be present in this shipment.

7.2 POWER CABLING

Power is fed to the B5261 Memory Cabinet from the D & D Unit. The only exception is the -19V raw power for the Regulators. The -19V cable runs directly from Power Supply thru D & D to each Power Pack.

The cabling and check out of the B5261 Regulator is to be completed in accordance with Section 5.5 of the B5370 Power Supply Technical Manual. Install the following cables in each B5261 Cabinet. These cables go to the Voltage Regulator, Fans, and the Barrier Strips in the Cabinet.

NOTE: INSURE THAT SYSTEM POWER IS OFF AT THIS TIME.

TABLE 7.2-1

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
25-1	GROUND (#00 AWG)	D & D	DA J1 04	MSS1	CA K1 07	2R
25-3	GROUND (#00 AWG)	D & D	DA J1 05	MSS2	CA K1 09	2R
25-2	GROUND (#00 AWG)	D & D	DA J1 04	MSS1	CU K1 07	2R
25-4	GROUND (#00 AWG)	D & D	DA J1 05	MSS2	CU K1 09	2R
25-21	+20V (#10 AWG)	D & D	DB J4 06	MSS1	CS K1 12	2F
25-22	+20V (#10 AWG)	D & D	DB J4 07	MSS2	CS K1 12	2F
25-27	+19V RAW (#4 AWG)	D & D	DB L3 02	MSS1	HA J1 06	2R
25-27A	+19V RAW (#4 AWG)	MSS1	HA J1 05	MSS2	HA J1 05	2R
25-29	-30V (-38V RAW) (#0 AWG)	D & D	DB K3 02	MSS1	HA K2 01	2R
25-29A	-30V (-38V RAW) (#0 AWG)	MSS1	HA K2 06	MSS2	HA K2 01	2R
25-30	+50V (#12 AWG)	D & D	DB L1 06	MSS1	CT N2 04	2F
25-31	+50V (#12 AWG)	D & D	DB L1 07	MSS2	CT N2 04	2F
25-36	+100V (#12 AWG)	D & D	DB K1 02	MSS1	HA J2 07	2F
25-36A	+100V (#12 AWG)	MSS1	HA J2 08	MSS2	HA J2 08	2F
25-37	-100V (#12 AWG)	D & D	DB K2 02	MSS1	HA J2 01	2R
25-37A	-100V (#12 AWG)	MSS1	HA J2 02	MSS2	HA J2 02	2R
25-38	-24V (#12 AWG)	D & D	DB J1 02	MSS1	HA J3 06	2R
25-38A	-24V (#12 AWG)	MSS1	HA J3 06	MSS2	HA J3 06	2R
25-39	-120V (#12 AWG)	D & D	DB L2 02	MSS1	HA J3 04	2R
25-39A	-120V (#12 AWG)	MSS1	HA J3 04	MSS2	HA J3 04	2R
25-40	RELAY GROUND	D & D	DA J1 13	MSS1	HA J2 13	1F
25-40A	RELAY GROUND	MSS1	HA J2 14	MSS2	HA J2 13	1F
25-45	+50V (#12 AWG)	D & D	DB L1 07	MSS1	HA J3 07	2F
25-45A	+50V (#12 AWG)	MSS1	HA J3 08	MSS2	HA J3 08	2F
25-46	-33V (#12 AWG)	D & D	DB J2 06	MSS1	CT N2 01	2F
25-47	-33V (#12 AWG)	D & D	DB J2 07	MSS2	CT N2 01	2F
27	MASTER CLEAR (#12 AWG)	D & D	DC L1 07	MSS1	HA J2 09	2F
27A	MASTER CLEAR (#12 AWG)	MSS1	HA J2 10	MSS2	HA J2 10	2F
28	DC LOCKOUT (#12 AWG)	D & D	DC L1 08	MSS1	HA J3 11	2F
28A	DC LOCKOUT (#12 AWG)	MSS1	HA J3 12	MSS2	HA J3 12	2F
208	-19V (#0 AWG)	PS	DA K5 B2	MSS1	CA J1 01	2R
207	-19V (#0 AWG)	PS	DA L6 B2	MSS2	CA J1 01	2R
226	115VAC CAB FAN CKT (#14 AWG)	CC	FA K1 06/07	MSS1	FA K1 06/07	NT
227	115VAC CAB FAN CKT (#14 AWG)	MSS1	FA K1 06/07	MSS2	FA K1 06/07	NT
236	115VAC REG FAN CKT (#14 AWG)	MSS1	FA K1 01/12	MSS1	CR J1 03/04	NT
237	115VAC REG FAN CKT (#14 AWG)	MSS2	FA K1 01/12	MSS2	CR J1 03/04	NT

Insure that the Memory Module Fans are connected as shown in Figure 7.2-1.

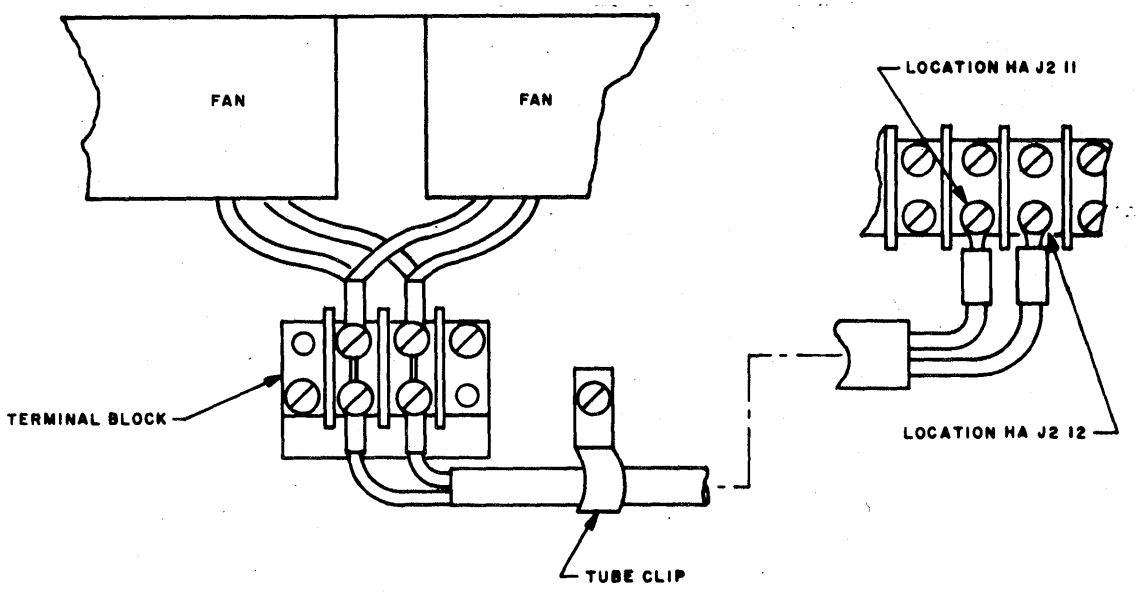


FIGURE 7.2-1
MEMORY MODULE FAN CONNECTIONS

7.3 ADDING A MEMORY MODULE

After unpacking and bolting a new Memory Module into its proper position within the B5261 Cabinet, Power and Information cables will be connected in accordance with the tables listed in this section.

Each table lists the connections to be made for one Memory Module. For instance, Table 7.3-1 references the connections to be made for Module "0"; Table 7.3-2, for Module "1", etc. The cables should be installed in the order listed in that table.

If the Module to be added is the fifth Module, it will require the installation of an additional B5261 Cabinet. The cables to be installed in this case will be designated first by Table 7.2-1 (Cabinet 2), then by Table 7.3-5 (Module "4"). Again, the cables will be installed in the listed order.

It is possible that the new B5261 could be installed in a System that contains two Processors. This would require new cables for Processor B. This will be corrected by separate installation instructions.

Before installing the cables to the Memory Gate, insure that no less than 1 Megohm of resistance exists between DC Logic Ground and the Frame.

Refer to the following tables and install the applicable cables for all available Memory Modules.

TABLE 7.3-1. MODULE "0"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-0A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA A0 A7	M-0	EA D0 A2	3R
1-0B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA A0 N7	M-0	EA D0 N2	3R
2-0A	MEMORY READ EXCHANGE	M-0	EA D0 A7	CC	AC A0 A2	3F
2-0B	MEMORY READ EXCHANGE	M-0	EA D0 N7	CC	AC A0 N2	3F
24-29	HEAT SENSE & -12V I SENSE	M-0	EA B0 L5	MSS1	VOLTAGE REGULATOR	2F
78	DISPLAY	M-0	AHL1	M-0	EA B0 A2	NT
79	DISPLAY	M-0	AHM1	M-0	EA B0 N2	NT
80	DISPLAY	M-0	AHN1	M-0	EA C0 A2	NT
81	DISPLAY	M-0	AHP1	M-0	EA C0 N2	NT
82	DISPLAY	M-0	AHR1	M-0	EC C0 A2	NT
83	DISPLAY	M-0	AHK1	M-0	EC D0 A2	NT
187	CLOCK CABLE	CC	EA D2 L2	M-0	EA C6 L8	2F
364	REGULATED POWER - M-0	M-0	AJJ1 1/2/3/4	MSS1	CS -- 16	1R
372	"A" PANEL POWER	M-0	EA C0 A7	M-0	AJJ1 7/8/9/10	NT
373	"C" PANEL POWER	M-0	EC C0 A7	M-0	AJJ1 6/7/8/9/10	NT
388	SPECIAL POWER	MSS1	HA J1/J2/J3/K2	M-0	AH J1 01 → 10	NT
397	GATE GROUND	M-0	GATE GROUND BUS	MSS1	CU K1 01	NT
406	INTER-GATE	M-0	EA B0 N7	M-0	EC B0 N2	NT
414	INTER-GATE	M-0	EA C0 N7	M-0	EC C0 N2	NT

TABLE 7.3-2. MODULE "1"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-1A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA B0 A7	M-1	DA D0 A2	4R
1-1B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA B0 N7	M-1	DA D0 N2	4R
2-1A	MEMORY READ EXCHANGE	M-1	DA D0 A7	CC	AC B0 A2	6F
2-1B	MEMORY READ EXCHANGE	M-1	DA D0 N7	CC	AC B0 N2	6F
84	DISPLAY	M-1	AHL1	M-1	DA B0 A2	NT
85	DISPLAY	M-1	AHM1	M-1	DA B0 N2	NT
86	DISPLAY	M-1	AHN1	M-1	DA C0 A2	NT
87	DISPLAY	M-1	AHP1	M-1	DA C0 N2	NT
88	DISPLAY	M-1	AHR1	M-1	DC C0 A2	NT
89	DISPLAY	M-1	AHK1	M-1	DC D0 A2	NT
188	CLOCK CABLE	CC	EA D2 L3	M-1	DA C6 L8	2F
365	REGULATED POWER - M-1	M-1	AJJ1 1/2/3/4	MSS1	CS -- 15	1R
374	"A" PANEL POWER	M-1	DA C0 A7	M-1	AJJ1 7/8/9/10	NT
375	"C" PANEL POWER	M-1	DC C0 A7	M-1	AJJ1 6/7/8/9/10	NT
389	SPECIAL POWER	MSS1	HA J1/J2/J3/K2	M-1	AH J1 01→10	NT
398	GATE GROUND	M-1	GATE GROUND BUS	MSS1	CU K1 02	NT
407	INTER-GATE	M-1	DA B0 N7	M-1	DC B0 N2	NT
415	INTER-GATE	M-1	DA C0 N7	M-1	DC C0 N2	NT

TABLE 7.3-3. MODULE "2"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-2A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA C0 A7	M-2	AA D0 A2	3R
1-2B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BA C0 N7	M-2	AA D0 N2	3R
2-2A	MEMORY READ EXCHANGE	M-2	AA D0 A7	CC	AC C0 A2	5R
2-2B	MEMORY READ EXCHANGE	M-2	AA D0 N7	CC	AC C0 N2	5R
90	DISPLAY	M-2	AHL1	M-2	AA B0 A2	NT
91	DISPLAY	M-2	AHM1	M-2	AA B0 N2	NT
92	DISPLAY	M-2	AHN1	M-2	AA C0 A2	NT
93	DISPLAY	M-2	AHP1	M-2	AA C0 N2	NT
94	DISPLAY	M-2	AHR1	M-2	AC C0 A2	NT
95	DISPLAY	M-2	AHK1	M-2	AC D0 A2	NT
189	CLOCK CABLE	CC	EA D2 L4	M-2	AA C6 L8	NT
366	REGULATED POWER - M-2	M-2	AJJ1 1/2/3/4	MSS1	CS -- 01	1R
376	"A" PANEL POWER	M-2	AA C0 A7	M-2	AJJ1 7/8/9/10	NT
377	"C" PANEL POWER	M-2	AC C0 A7	M-2	AJJ1 6/7/8/9/10	NT
390	SPECIAL POWER	MSS1	HA J1/J2/J3/K2	M-2	AH J1 01→10	NT
399	GATE GROUND	M-2	GATE GROUND BUS	MSS1	CU K1 01	NT
408	INTER-GATE	M-2	AA B0 N7	M-2	AC B0 N2	NT
416	INTER-GATE	M-2	AA C0 N7	M-2	AC C0 N2	NT

TABLE 7.3-4. MODULE "3"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-3A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC A0 A7	M-3	BA D0 A2	8R
1-3B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC A0 N7	M-3	BA D0 N2	8R
2-3A	MEMORY READ EXCHANGE	M-3	BA D0 A7	CC	AC D0 A2	7F
2-3B	MEMORY READ EXCHANGE	M-3	BA D0 N7	CC	AC D0 N2	7F
96	DISPLAY	M-3	AHL1	M-3	BA B0 A2	NT
97	DISPLAY	M-3	AHM1	M-3	BA B0 N2	NT
98	DISPLAY	M-3	AHN1	M-3	BA C0 A2	NT
99	DISPLAY	M-3	AHP1	M-3	BA C0 N2	NT
100	DISPLAY	M-3	AHR1	M-3	BC C0 A2	NT
101	DISPLAY	M-3	AHK1	M-3	BC D0 A2	NT
190	CLOCK CABLE	CC	EA D2 L5	M-3	BA C6 L8	NT
367	REGULATED POWER - M-3	M-3	AJJ1 1/2/3/4	MSS1	CS -- 02	1R
378	"A" PANEL POWER	M-3	BA C0 A7	M-3	AJJ1 7/8/9/10	NT
379	"C" PANEL POWER	M-3	BC C0 A7	M-3	AJJ1 6/7/8/9/10	NT
391	SPECIAL POWER	MSS1	HA J1/J2/J3/K2	M-3	AH J1 01→10	NT
400	GATE GROUND	M-3	GATE GROUND BUS	MSS1	CU K1 02	NT
409	INTER-GATE	M-3	BA B0 N7	M-3	BC B0 N2	NT
417	INTER-GATE	M-3	BA C0 N7	M-3	BC C0 N2	NT

TABLE 7.3-5. MODULE "4"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-4A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC B0 A7	M-4	EA D0 A2	4R
1-4B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC B0 N7	M-4	EA D0 N2	4R
2-4A	MEMORY READ EXCHANGE	M-4	EA D0 A7	CC	AE A0 A2	4R
2-4B	MEMORY READ EXCHANGE	M-4	EA D0 N7	CC	AE A0 N2	4R
24-30	HEAT SENSE & -12V I SENSE	M-4	EA B0 L5	MSS2	VOLTAGE REGULATOR	2F
102	DISPLAY	M-4	AHL1	M-4	EA B0 A2	NT
103	DISPLAY	M-4	AHM1	M-4	EA B0 N2	NT
104	DISPLAY	M-4	AHN1	M-4	EA C0 A2	NT
105	DISPLAY	M-4	AHP1	M-4	EA C0 N2	NT
106	DISPLAY	M-4	AHR1	M-4	EC C0 A2	NT
107	DISPLAY	M-4	AHK1	M-4	EC D0 A2	NT
191	CLOCK CABLE	CC	EA D2 L6	M-4	EA C6 L8	2F
368	REGULATED POWER - M-4	M-4	AJJ1 1/2/3/4	MSS2	CS -- 16	1F
380	"A" PANEL POWER	M-4	EA C0 A7	M-4	AJJ1 7/8/9/10	NT
381	"C" PANEL POWER	M-4	EC C0 A7	M-4	AJJ1 6/7/8/9/10	NT
392	SPECIAL POWER	MSS2	HA J1/J2/J3/K2	M-4	AH J1 01→10	NT
401	GATE GROUND	M-4	GATE GROUND BUS	MSS2	CU K1 01	NT
410	INTER-GATE	M-4	EA B0 N7	M-4	EC B0 N2	NT
418	INTER-GATE	M-4	EA C0 N7	M-4	EC C0 N2	NT

TABLE 7.3-6. MODULE "5"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-5A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC C0 A7	M-5	DA D0 A2	8R
1-5B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BC C0 N7	M-5	DA D0 N2	8R
2-5A	MEMORY READ EXCHANGE	M-5	DA D0 A7	CC	AE B0 A2	8F
2-5B	MEMORY READ EXCHANGE	M-5	DA D0 N7	CC	AE B0 N2	8F
108	DISPLAY	M-5	AHL1	M-5	DA B0 A2	NT
109	DISPLAY	M-5	AHM1	M-5	DA B0 N2	NT
110	DISPLAY	M-5	AHN1	M-5	DA C0 A2	NT
111	DISPLAY	M-5	AHP1	M-5	DA C0 N2	NT
112	DISPLAY	M-5	AHR1	M-5	DC C0 A2	NT
114	DISPLAY	M-5	AHK1	M-5	DC D0 A2	NT
192	CLOCK CABLE	CC	EA D2 L7	M-5	DA C6 L8	2F
369	REGULATED POWER - M-5	M-5	AJJ1 1/2/3/4	MSS2	CS -- 15	1F
382	"A" PANEL POWER	M-5	DA C0 A7	M-5	AJJ1 7/8/9/10	NT
383	"C" PANEL POWER	M-5	DC C0 A7	M-5	AJJ1 6/7/8/9/10	NT
393	SPECIAL POWER	MSS2	HA J1/J2/J3/K2	M-5	AH J1 01→10	NT
402	GATE GROUND	M-5	GATE GROUND BUS	MSS2	CU K1 02	NT
411	INTER-GATE	M-5	DA B0 N7	M-5	DC B0 N2	NT
419	INTER-GATE	M-5	DA C0 N7	M-5	DC C0 N2	NT

TABLE 7.3-7. MODULE "6"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-6A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BE A0 A7	M-6	AA D0 A2	5R
1-6B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BE A0 N7	M-6	AA D0 N2	5R
2-6A	MEMORY READ EXCHANGE	M-6	AA D0 A7	CC	AE C0 A2	6F
2-6B	MEMORY READ EXCHANGE	M-6	AA D0 N7	CC	AE C0 N2	6F
115	DISPLAY	M-6	AHL1	M-6	AA B0 A2	NT
116	DISPLAY	M-6	AHM1	M-6	AA B0 N2	NT
117	DISPLAY	M-6	AHN1	M-6	AA C0 A2	NT
118	DISPLAY	M-6	AHP1	M-6	AA C0 N2	NT
119	DISPLAY	M-6	AHR1	M-6	AC C0 A2	NT
120	DISPLAY	M-6	AHK1	M-6	AC D0 A2	NT
193	CLOCK CABLE	CC	EA D2 L8	M-6	AA C6 L8	2F
370	REGULATED POWER - M-6	M-6	AJJ1 1/2/3/4	MSS2	CS -- 01	1F
384	"A" PANEL POWER	M-6	AA C0 A7	M-6	AJJ1 7/8/9/10	NT
385	"C" PANEL POWER	M-6	AC C0 A7	M-6	AJJ1 6/7/8/9/10	NT
394	SPECIAL POWER	MSS2	HA J1/J2/J3/K2	M-6	AH J1 01→10	NT
403	GATE GROUND	M-6	GATE GROUND BUS	MSS2	CU K1 01	NT
412	INTER-GATE	M-6	AA B0 N7	M-6	AC B0 N2	NT
420	INTER-GATE	M-6	AA C0 N7	M-6	AC C0 N2	NT

TABLE 7.3-8. MODULE "7"

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-7A	MEMORY WRITE & ADDRESS EXCHANGE	CC	BE B0 A7	M-7	BA D0 A2	9R
1-7B	MEMORY WRITE & ADDRESS EXCHANGE	CC	BE B0 N7	M-7	BA D0 N2	9R
2-7A	MEMORY READ EXCHANGE	M-7	BA D0 A7	CC	AE D0 A2	9F
2-7B	MEMORY READ EXCHANGE	M-7	BA D0 N7	CC	AE D0 N2	9F
121	DISPLAY	M-7	AHL1	M-7	BA B0 A2	NT
122	DISPLAY	M-7	AHM1	M-7	BA B0 N2	NT
123	DISPLAY	M-7	AHN1	M-7	BA C0 A2	NT
124	DISPLAY	M-7	AHP1	M-7	BA C0 N2	NT
125	DISPLAY	M-7	AHR1	M-7	BC C0 A2	NT
126	DISPLAY	M-7	AHK1	M-7	BC D0 A2	NT
194	CLOCK CABLE	CC	EA D2 L9	M-7	BA C6 L8	2F
371	REGULATED POWER - M-7	M-7	AJJ1 1/2/3/4	MSS2	CS -- 02	1F
386	"A" PANEL POWER	M-7	BA C0 A7	M-7	AJJ1 7/8/9/10	NT
387	"C" PANEL POWER	M-7	BC C0 A7	M-7	AJJ1 6/7/8/9/10	NT
395	SPECIAL POWER	MSS2	HA J1/J2/J3/K2	M-7	AH J1 01→10	NT
404	GATE GROUND	M-7	GATE GROUND BUS	MSS2	CU K1 02	NT
413	INTER-GATE	M-7	BA B0 N7	M-7	BC B0 N2	NT
421	INTER-GATE	M-7	BA C0 N7	M-7	BC C0 N2	NT

7.4 PRE-POWER CHECK FOR THE B5261 CABINET

Insure that the following packages are installed in the D & D Power Sense Panel.

NOTE

Do NOT install MSS2 packages until the MSS2 Cabinet is installed.

MSS1	ELEMENT	LOCATION	FUNCTION
	Package	AE B5 A2	Voltage Sense
	Package	AE A7 N2	Voltage Sense
	Package	AE B7 N2	Voltage Sense

MSS2	ELEMENT	LOCATION	FUNCTION
REMOVE if USING one VOLTAGE REG.	Package	AE B5 N2	Voltage Sense
	Package	AE A8 N2	Voltage Sense
	Package	AE B8 N2	Voltage Sense

When MSS2 is installed, insure that the Grounds listed below (normally removed at factory) are removed in D & D.

1. Delete: AF B0 B2 AF A0 Z8
2. Delete: AC A2 E2 GROUND

7.5 APPLYING POWER TO THE B5261 CABINET

Use the following procedures to apply Power to the B5261 Cabinet:

1. Place the DC Lockout switch on the Central Control Display Panel in the DC ON position.
2. Insure that DC is OFF on all Memory Modules.
3. Turn ON System Power and check for Regulator and Cabinet Fan operation.
4. Check for Voltage at the following points:

LOCATION	VOLTAGE
HA K2 01	-38V
HA J1 03	-33V
HA J1 05	+19V
HA J2 01	-100V
HA J2 03	-120V
HA J2 05	-100V
HA J2 07	+100V
HA J2 09	+20V / -100V (Master Clear)
HA J3 07	+50V
HA J3 09	+74V
HA J3 11	-24V (DC Lockout)

This completes the initial power on checks for the B5261 Sub-System.

7.6 APPLYING POWER TO THE B461 MEMORY MODULE

After checking the raw voltages in the B5261 Cabinet, Power is ready to be applied to the B461 Module. During the initial installation, Local DC Power should be applied to one Memory Module at a time; starting with Module "0", then Module "1", etc.

1. Turn the Local DC switches on the B461 Memory Modules to OFF.
2. Turn System Power ON at the Console.
3. Turn System DC ON at the D & D Display Panel.
4. Monitor the following points on AJJ1 for the proper voltage:

AJJ1 - 1	+20V
AJJ1 - 2	-4.5V
AJJ1 - 3	-12V
AJJ1 - 4	-1.2V

5. Turn the Memory DC switch to ON.

The System Power and Local Power lights on the Memory Display Panel should come ON.

7.7 -6T REGULATOR CHECK

The tag attached to the front of the Memory Module lists the optimum Factory setting for the -6T Regulator.

Monitor the -6T Regulator at the Test Point on the Display Panel and insure that it is setting at the above mentioned optimum value.

NOTE

The output of the -6T Regulator will vary with the outputs of the -12V and the +20V Regulators. If the output of the System +20V Regulator is different than the +20V Regulator output listed on the tag, then the value of the Modules -6T Regulator will differ also.

The -6T Regulator will track the +20V according to the following formula:

$$\Delta V_{-6T} = 0.324 \Delta V_{+20}$$

This means that with a 1.0 volt change in the +20V, the --6T will change approximately 0.3 volts in direct proportion.

7.8 -15V REGULATOR CHECK

The -15V Regulator is a temperature compensated regulator which is used to control the three -30V Regulators.

The tag attached to the front of the Memory Module lists the Factory setting of the -15V Regulator along with the Stack area temperature at the time.

Monitor the temperature as closely as possible to the Core Stack area and insure that the -15V Regulator is tracking correctly for the existing room temperature.

Monitor the output of the -15V Regulator at AC D4 B4.

Refer to Figure 7.8-1 to determine what the correct setting should be.

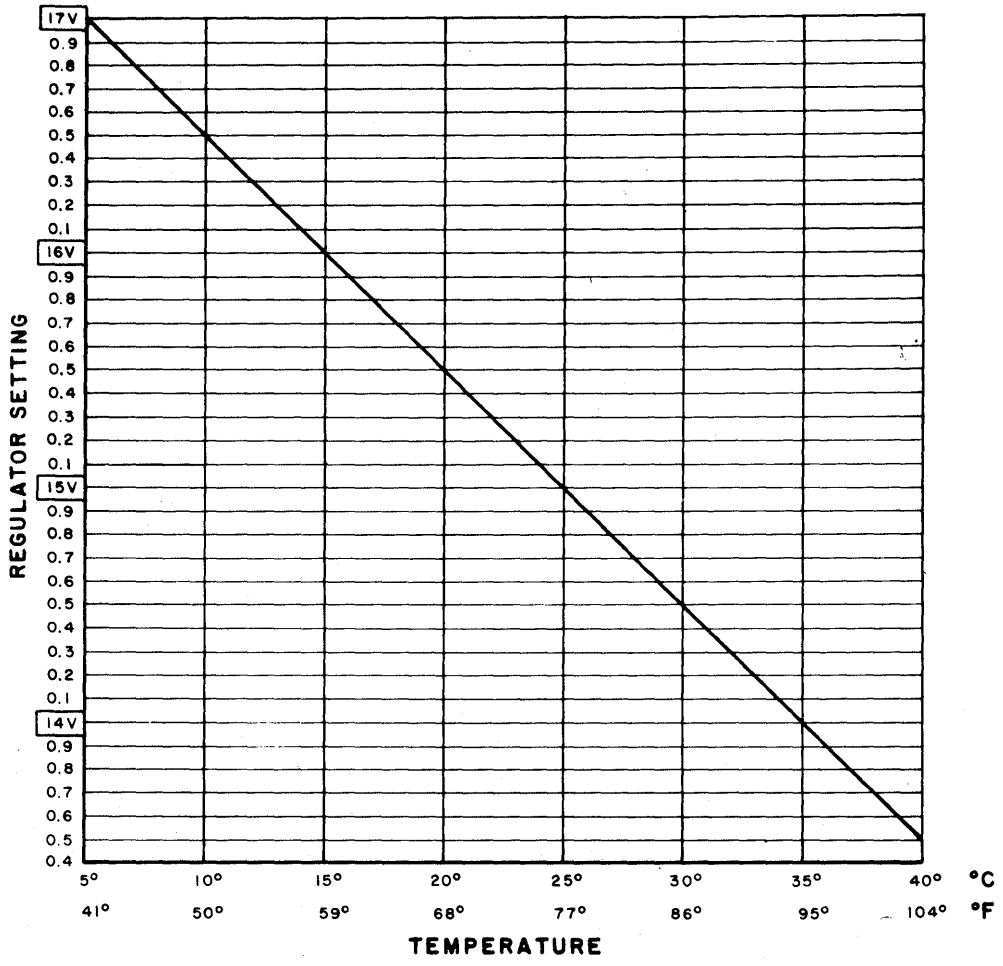


FIGURE 7.8-1
TEMPERATURE VS. VOLTAGE

7.9 -30V READ (R), WRITE (W), & INHIBIT (I) REGULATOR CHECK

The tag attached to the front of the Memory Module also lists the optimum Factory setting of the -30V "R","W" and "I" Regulators.

The output of the three -30V Regulators should vary in direct proportion with the output of the -15V Regulator. For each 0.1V variation in the -15V Regulator, the three -30V Regulators should vary 0.2V.

Monitor the outputs of the three -30V Regulators at the Test Points on the Display Panel, and insure that they are set properly for the existing room temperature.

EXAMPLE: Assume that in the Factory, the -15V Regulator was set to -15V with the Stack area temperature at 25°C. Assume also, that the optimum value for the -30V "R", and "W" Regulators was found to be -30V and that the -30V "I" was set to -32V.

When the Module arrived in the field, assume that the Stack area temperature was found to be 20°C. In this case, the -15V Regulator output should have tracked to -15.5V. The -30V "R" and "W" Regulators should have tracked to -31V, and the -30V "I" should have tracked to -33V.

7.10 MANUAL CHECK

Use the following procedure for manual check on the B461 Memory Module:

1. Place the Memory Module in LOCAL and inhibit the LOCAL CLOCK.
2. Manually SET and RESET each Flip-flop on the Memory Display Panel.
3. Set all the Flip-flops ON.
4. Verify correct operation of the three CLEAR switches.
5. Clear the Registers and turn the INHIBIT LOCAL CLOCK switch to OFF, (LOCAL CLOCK RUNNING).
6. Depress the STEP MAR switch. MAR should count once each time the switch is activated.

7.11 INSTALLATION CORE STACK MOUNTING ASSEMBLY

At time of shipment from the factory, the Core Stack Mounting Assembly is removed (this includes the Transformer Boards). This is done in order to protect the Core Stack from physical damage due to shock during shipment.

Prior to installing the Stack Assembly, POWER should be turned OFF. The reinstalling of this assembly should be accomplished as indicated in Figures 7.11-1, 7.11-4 and 7.11-5.

NOTE

It is important to insure that the correct Stack is reinstalled in the same Module as that in which it was tested at the factory. The Stack is tagged with the corresponding information.

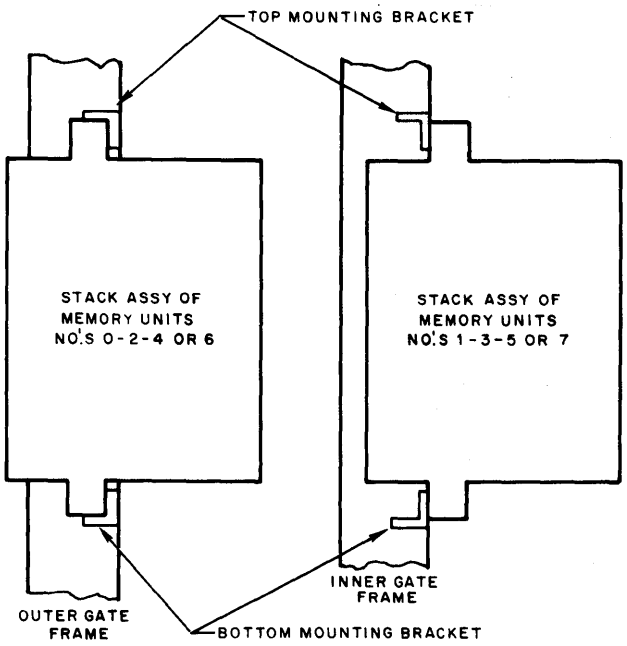


FIGURE 7.11-1
CORE STACK MOUNTING ASSEMBLY

All orientation and location is described facing the PLUGGABLE SIDE of the Memory Unit gate.

The ends of the Core Stack are labeled Top and Bottom. The Top of the Stack faces to the left, toward the latch end of the gate. The Bottom of the Stack faces right, toward the hinge end of the gate.

Two Transformer Boards are located on each side of the Stack. They are

located with their components facing away from the Stack.

Each Transformer Board is marked with the following information:

1. Assembly Number
2. Panel Letter (A,B,C or D)
3. TOP is marked on an edge to indicate proper orientation.

Each of the Transformer Boards have stick-type connectors and should be installed as indicated in Table 7.11-1.

TABLE 7.11-1

BOARD ASSEMBLY	STICK J1	STICK J2	STICK J3
A	AD A1 L0	AD B1 L0	AD B1 Y0
B	AD A1 L1	AD A1 Y0	AD B1 Y1
C	AC A3 L9	AC A3 L8	AC A3 Y9
D	AC B3 Y8	AC B3 Y9	AC B3 L9

Sense line and Inhibit line stick-type connectors should be installed as indicated in Figures 7.11-2 and 7.11-3 respectively.

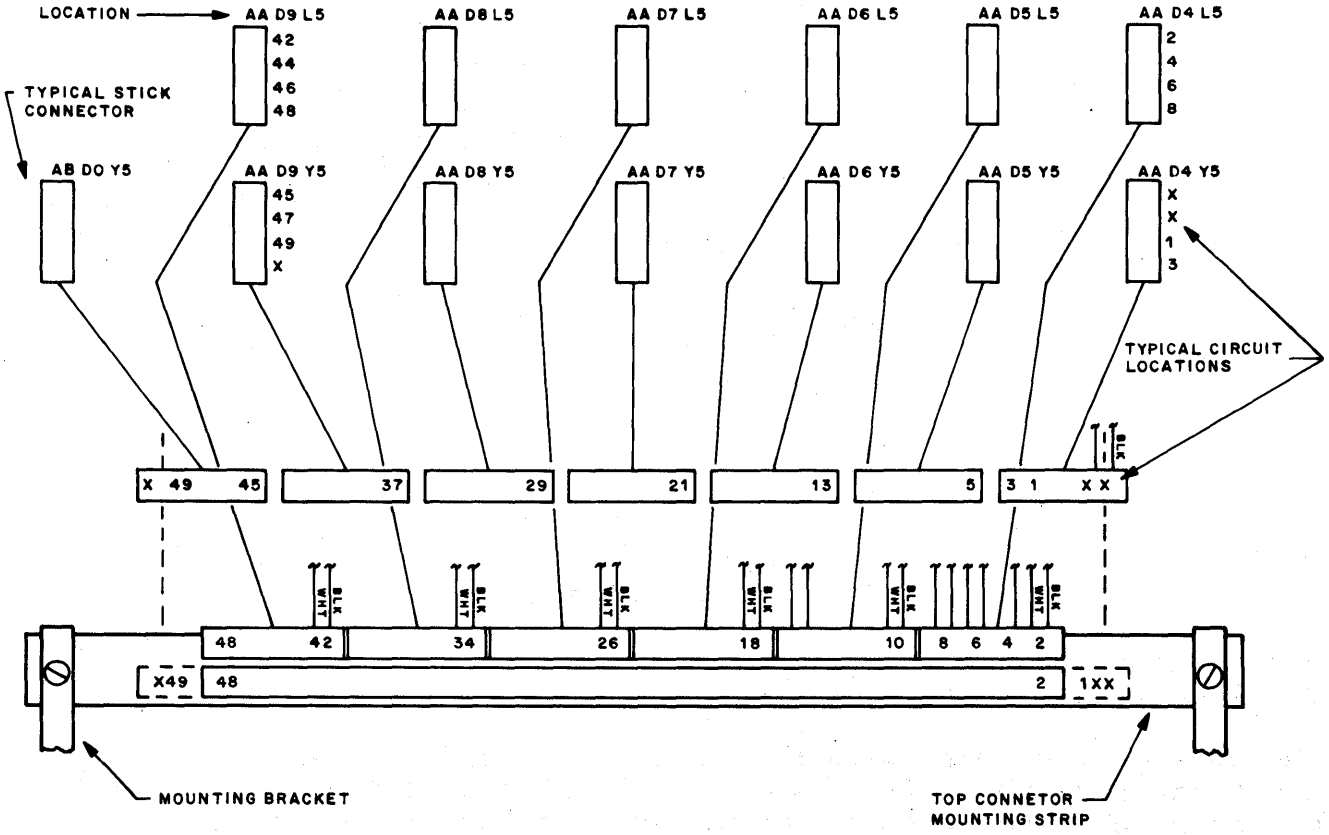


FIGURE 7.11-2
SENSE AMP AREA

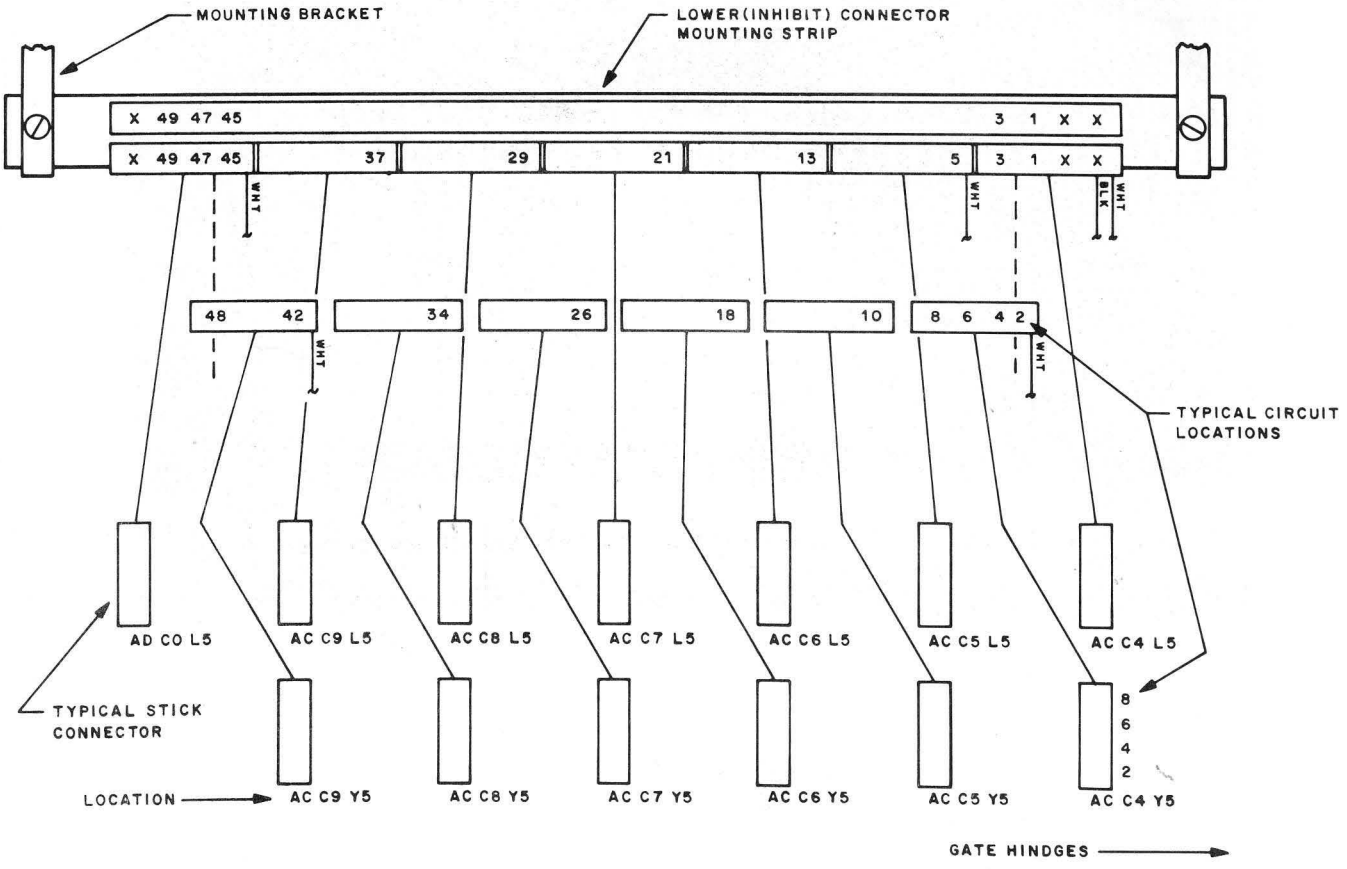


FIGURE 7.11-3
INHIBIT AREA

Install Transformer Board Ground Wires as indicated in Figures 7.11-4 and 7.11-5.

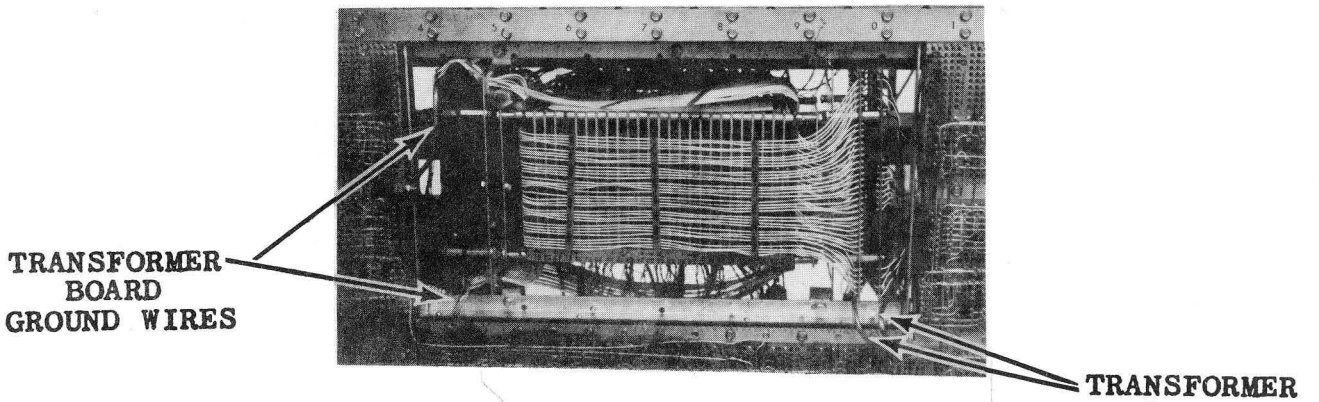
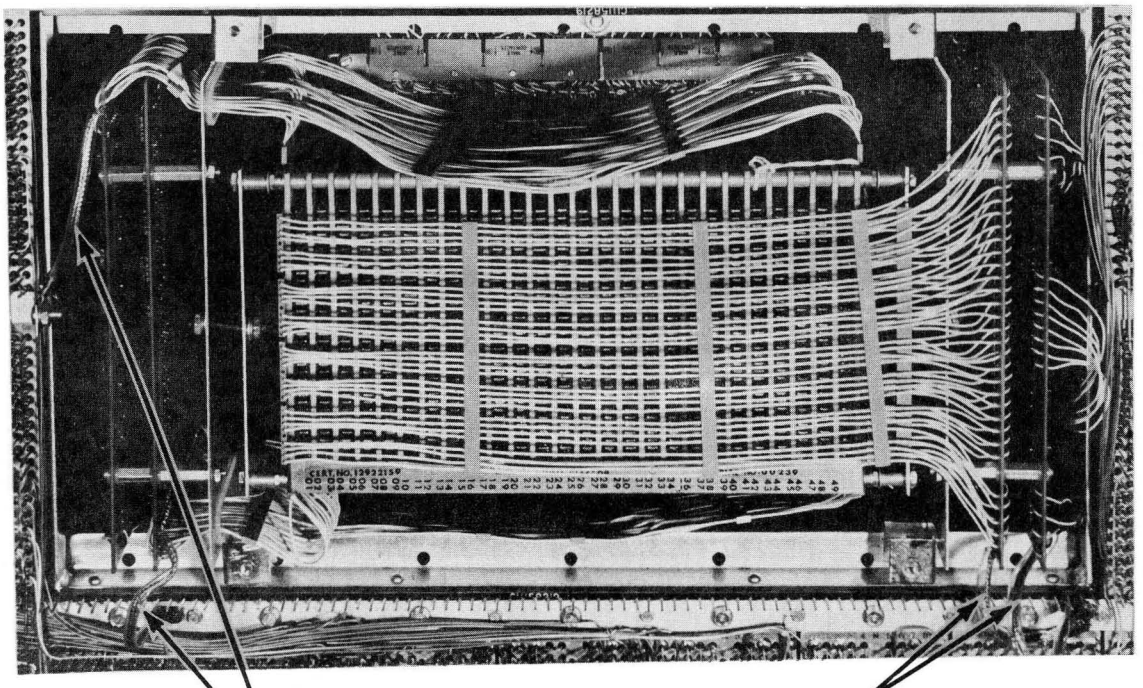


FIGURE 7.11-4
OUTER GATE CORE STACK



TRANSFORMER BOARD
GROUND WIRES

FIGURE 7.11-5
INNER GATE CORE STACK

7.12 LOCAL OPERATIONS CHECK

Verify proper operation of the following Local Maintenance Operations by running each with STOP ON ERROR Switch ON. Leave the TRUE/COMP bit switches in the TRUE position. Run each test for thirty seconds.

1. Manual Write - All Zeros - All Addresses
2. Manual Read - All Zeros - All Addresses
3. Manual Write - All Ones - All Addresses
4. Manual Read - All Ones - All Addresses
5. CONT: TRUE: UNIFORM: AUTO: NORM
6. CONT: COMP: UNIFORM: AUTO: NORM
7. CONT: TRUE: UNIFORM: AUTO: PCCL
8. CONT: COMP: UNIFORM: AUTO: PCCL
9. CONT: TRUE: CHKD: AUTO: NORM
10. CONT: COMP: CHKD: AUTO: NORM
11. CONT: TRUE: CHKD: AUTO: PCCL
12. CONT: COMP: CHKD: AUTO: PCCL

While running one of the above tests, verify the proper operation of the STOP ON FINAL ADDRESS switch, INHIBIT COUNT switch, and the COUNT "X" and COUNT "Y" switches.

NOTE

Refer to Section VI of this manual for a detailed explanation of the Maintenance switches.

7.13 REMOTE OPERATION CHECK

Use the following procedure for the REMOTE operation check:

1. Place the Memory Module in REMOTE.
2. Manually SET the MAR and MIR Flip-flops and CLEAR them with the MASTER CLEAR pushbutton on the D & D Panel.
3. Perform a REMOTE WRITE and READ from the I/Os and Processor to the Module under test.
4. Run the Memory Test Routines with the Module on the line.