B 1700 DISK FILE CONTROLS I AND II TECHNICAL MANUAL

Burroughs

FIELD ENGINEERING

Printed in U.S. America

1/76

For Library Binder 114B
Form 1066867

AA505319

Correspondence regarding this document should be forwarded using the Remarks Form at the back of the manual, or may be addressed directly to Systems Documentation, Technical Information Organization, TIO-Central, Burroughs Corporation, Burroughs Place, Detroit, Michigan 48232

1066867

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

INTRODUCTION AND OPERATION

INTRODUCTION

This section provides information on the B 1700 Disk File I/O Controls I and II. The Disk File Control is a part of the B 1700 Disk File Subsystem. The Disk File Subsystem consists of the following units:

a. A B 1700 Disk File Control I or II.

b. A Disk File Electronics Unit (DFEU).

c. A Disk File Storage Unit (DFSU).

d. A 1 x 2 Disk File Exchange (DFE).

e. A 2 x 4 Disk File Exchange (DFE).

Examples of possible Disk File Subsystem configurations are shown in figures 1-1 through 1-3.

DISK FILE CONTROL I

The B 1700 Disk File Control I consists of four standard B 1700 size logic cards located in an independent 4-card backplane. This control is designed for use with the following disk file units:

a. 1A DFEU and 1A-3 DFSU.

b. 1C DFEU and 1C-3 DFSU.

c. 1C DFEU and 1C-4 DFSU.

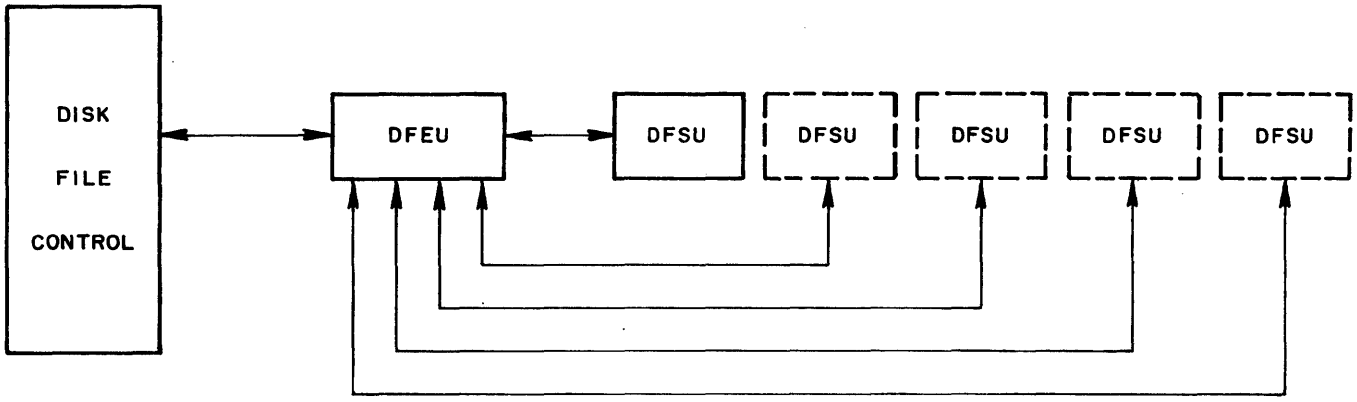


Figure 1-1. Minimum Disk File Subsystem

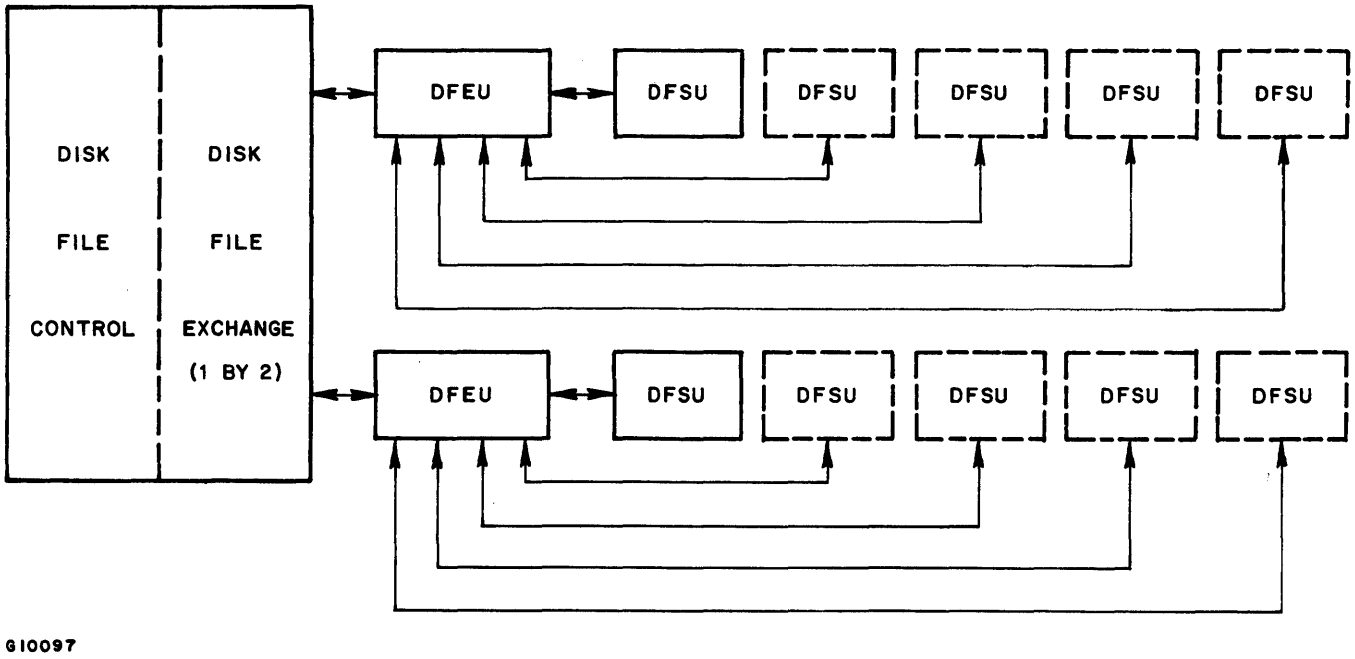


Figure 1-2. Disk File Subsystem (1 x 2 Exchange)

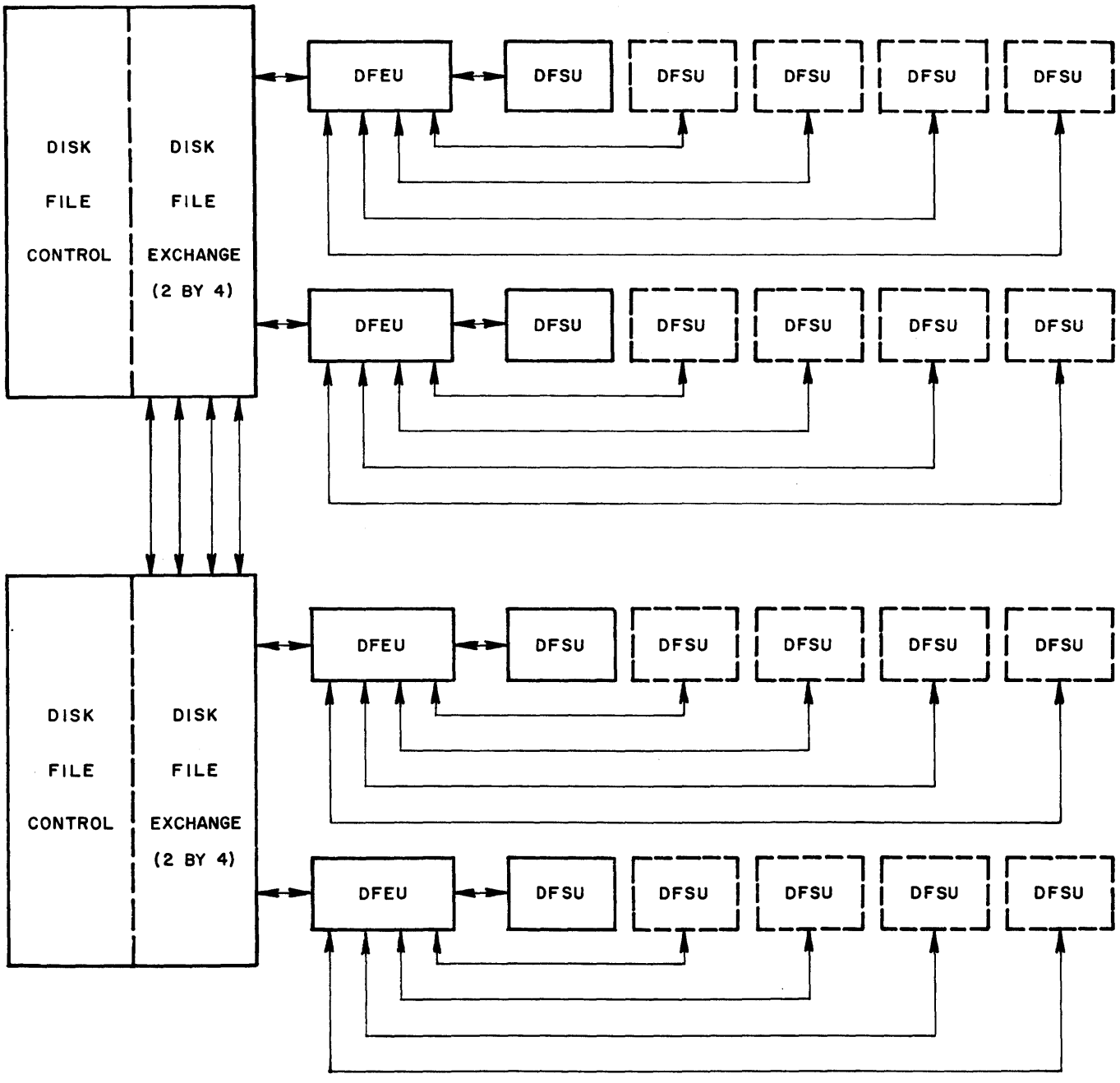


Figure 1-3. Disk File Subsystem (2 x 4 Exchange)

DISK FILE CONTROL II

The B 1700 Disk File Control II consists of four standard B 1700 size logic cards located in an independent 4-card backplane. This control is designed for use with the following disk file units:

a. 1A DFEU and 1A-3 DFSU.

b. 1A DFEU and 1A-4 DFSU.

c. 1C DFEU and 1C-3 DFSU.

d. 1C DFEU and 1C-4 DFSU.

e. 1B Systems Memory.

DISK FILE ELECTRONICS UNIT

The Disk File Electronics Unit provides an interface between a Disk File Control and up to five Disk File Storage Units. A 1A DFEU is used to interface to 1A-type DFSU's. A 1C DFEU is used to interface to 1C-type DFSU's.

DISK FILE STORAGE UNIT

The Disk File Storage Unit is used to provide additional program or information storage in a B 1700 System. The storage facilities and average access times are listed in table 1-1.

Table 1-1. Disk File Storage Units

DFSU	Average Access Time	Storage Capabilities (in Megabytes)
1A-3	20 ms.	8.1
1A-4	40 ms.	14.4
1C-3	23.8 ms.	20
1C-4	40 ms.	20

1 x 2 DISK FILE EXCHANGE

The 1 x 2 Disk File Exchange allows two DFEU's to be connected to one Disk File Control, providing up to 10 DFSU's on a Disk File Subsystem (see figure 1-2).

2 x 4 DISK FILE EXCHANGE

The 2 x 4 Disk File Exchange (DFE) allows four DFEU's to be connected to two Disk File Controls, providing up to 20 DFSU's on the Disk File Subsystem (see figure 1-3). The 2 x 4 DFE can be installed only in a B 1726 or B 1728 System.

OPERATION

Information flow between the Disk File Storage Unit and the B 1700 system main memory is controlled by means of I/O descriptors. The I/O descriptor used for the B 1700 Disk File Control I or II consists of 10 possible 24-bit fields, as shown in figure 1-4.

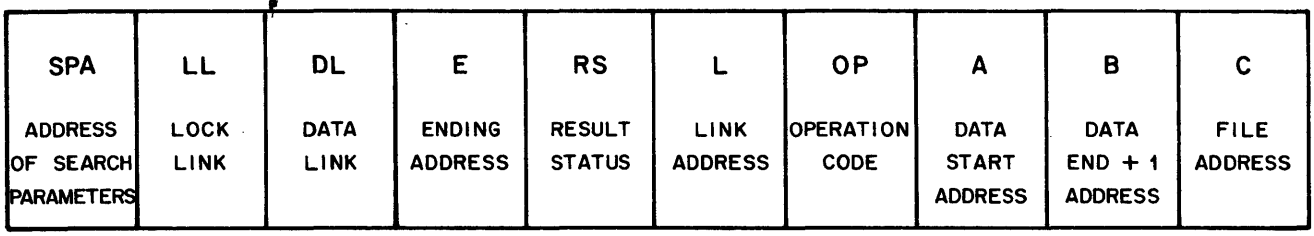


Figure 1-4. Disk File Control I/O Descriptor

The number of fields required for each I/O descriptor is variable. The function of each field is as follows:

SEARCH PARAMETERS ADDRESS (SPA) FIELD

The SPA field contains the address of the search parameters used in the Search operation.

LOCK LINK (LL) FIELD

The LL field contains a 24-bit address that points to the RS field of a Lock descriptor. The I/O driver will exit by means of this link if an exception condition is reported in the Result descriptor, provided the I/O driver is in a "lock" status.

DATA LINK (DL) FIELD

The contents of the DL field are not used.

E-FIELD

At the completion of an I/O operation, the I/O driver stores the final A-address that points to the memory location where the next bit of data normally would be stored. For Search, Read, and Write operations, this address is equal to the B-address unless the operation is terminated due to a not-ready or write-lockout condition. For certain operations, the E-field is also used to save the incremented A-address between buffer transfers to the I/O control.

RS FIELD

Prior to and during an operation, the first 15 bits of the RS field are used to store temporary flags for the I/O driver. The first two bits are used to provide a "lock" for the I/O descriptor. A "lock" condition is indicated by 01 in the first two bits of the RS field; an "unlock" condition is indicated by 00. The last nine bits of the RS field are used to store dynamic interrupt information.

After the completion of an operation, the I/O driver exchanges the result status information in the RS field with the interrupt control information.

L-FIELD

After storing the Result descriptor information and after returning any requested interrupt message, the I/O driver normally exits by means of the L-field link address to the RS field of the next I/O descriptor to be executed. The following exits may be used, however, under the following conditions:

a. The SPA link address may be used during a Search operation.

b. The B-address is used for a Lock operation.

c. The LL address is used if an exception condition exists or if the I/O descriptor is not ready to be executed.

OP FIELD

The OP field contains the operation code, variants, and unit number. The first three bits designate the operation (OP) code, and the last four bits designate the unit number. The remaining bits designate variants.

A AND B FIELDS

For all operators except the Lock operator, the A and B fields contain the beginning and ending addresses, respectively, of the data for the operation. The B address must always be larger than the A address. For a maintenance segment Read or Write operation, the address field must be equal to or less than 180-bit bytes.

C-FIELD

The C-field contains the file address specifying the starting segment in the DFSU. For the reading or writing of a maintenance segment, the file address must be the starting address of a maintenance segment.

The Disk File I/O descriptors are generated by the Master Control Program (MCP) into a linked list. Once initiated, the I/O driver continually checks and executes I/O descriptors until (1) stopped by a Stop OP or (2) stopped by the detection of a memory parity error during the fetch of the starting address.

The I/O driver is initiated by receiving a 24-bit address pointing to the RS field of an I/O descriptor. The I/O driver reads the first two bits of the RS field, checking for a "unlocked" condition (00). If an unlocked condition is not found, the I/O driver exits, by means of the L-field address, to the RS field of the next I/O descriptor. If an unlocked condition is found, an attempt is made to lock the I/O descriptor by setting an 01 into the first two bit positions and transferring the previous contents back to the I/O driver.

If the "lock" is not successful (00 not received by the I/O driver), the I/O driver exits by means of the L-field address.

If the "lock" is successful, the I/O descriptor is executed. After execution, the I/O driver exits by means of the L-field address. The Disk File Control checks for the presence and disposition of the DFEU prior to a Read or Write operation. If the DFEU is busy and the Wait variant is specified, the I/O Control will wait until the unit becomes available. If the DFEU is not present or if it is busy with the Wait variant not specified, the I/O Control returns a Result descriptor with bit 17 off. This condition indicates to the I/O driver that the Result descriptor should not be stored and the program is to proceed to the next I/O descriptor RS field.

At the completion of an operation, after the ending data address has been stored, the previous information in the RS field is sent to the I/O driver, and the Result descriptor bits from the operation are transferred to the RS field. The bit configuration of the prior RS field information sent to the I/O driver is shown in figure 1-5.

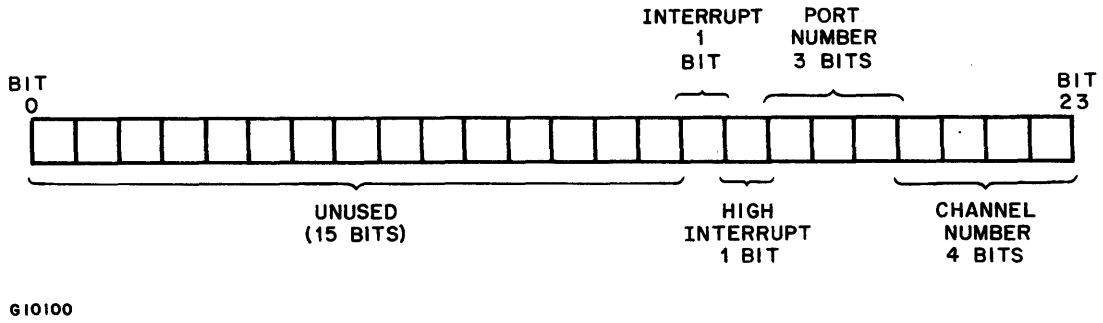


Figure 1-5. Result Status Bit Configuration Prior to the Result Descriptor

If the Interrupt bit is set, the I/O driver generates the appropriate interrupt message to the port indicated. The interrupt will be a High Interrupt, if the High Interrupt bit is set.

If the Interrupt bit is not set, the I/O driver will generate an interrupt message only if an exception condition exists (i.e., bit 2 of the Result descriptor is set).

The interrupt message is a 24-bit address pointing between the Result descriptor and the link address. The channel number previously contained in the RS area is returned to the port indicated.

I/O DESCRIPTOR OPERATORS

The I/O descriptor operators for the B 1700 Disk File Control are listed as follows:

a. Read.

b. Write.

c. Test.

d. Pause.

The special I/O descriptors (software only) for the B 1700 Disk File Control are listed below:

a. Search.

b. Stop.

c. Lock.

READ

The Read operator and associated I/O descriptor fields are shown in figure 1-6.

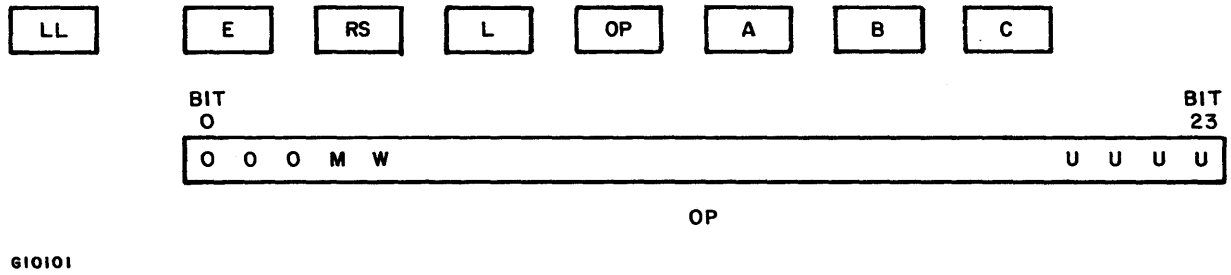


Figure 1-6. Disk File Read Operator

The first three bits of the operator provide the code for Read (000). This operator provides logic to read data from the disk file, starting at the given file address, C, into ascending memory locations beginning at the location specified by the A address and continuing up to the end address specified by the B address. The data can consist of less than a segment or more than a segment (180 eight-bit bytes). The variants and associated meanings for this operator are as follows:

M = 1 Causes one maintenance segment to be read. The difference between the A and B addresses must be less than or equal to one segment length.

W = 1 Signifies a wait for a busy DFSU to become not busy.

UUUU Unit number (0 through 15).

WRITE

The Write operator and associated I/O descriptor fields are shown in figure 1-7.

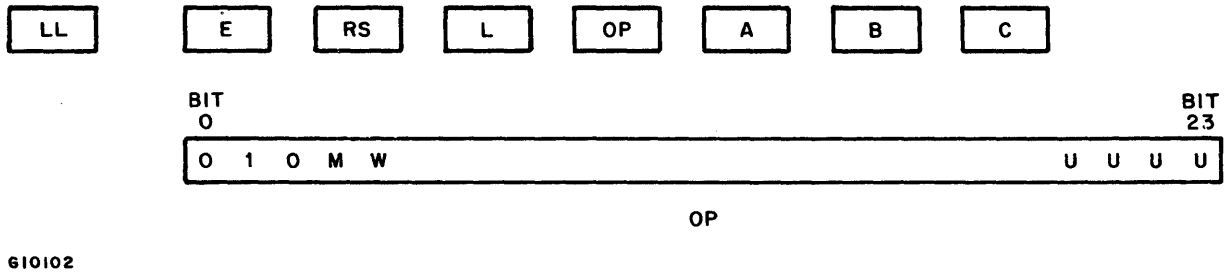


Figure 1-7. Disk File Write Operator

The first three bits of the operator provide the code for Write (010). This operator provides logic to write data to the disk file, starting at the given file address, C, from ascending memory locations beginning at the location specified by the A address and continuing up to the address specified by the B address. Zeros are written in the trailing bit positions to complete the last segment. The variants and associated meanings for this operator are as follows:

M = 1 Causes one maintenance segment to be written.

W = 1 Signifies a wait until a busy DFSU becomes not busy.

UUUU Unit number (0 through 15).

TEST

The Test operator and associated I/O descriptor fields are shown in figure 1-8.

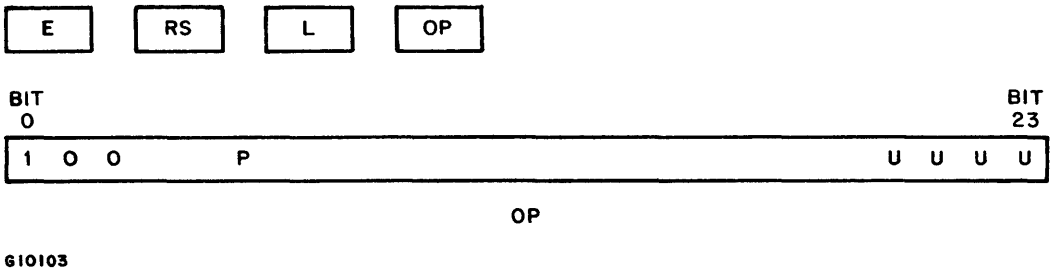


Figure 1-8. Disk File Test Operator

The first three bits of the operator provide the code for Test (100). This operator provides logic to test the Disk File Control for the following information:

a. Unit Identification (ID).

b. Configuration.

c. Control number.

d. Control type identification.

The variants and associated meanings for this operator are as follows:

P = 1 Detection of P = 1 by the I/O driver initiates the Pause operator rather than the Test operator. No Result descriptor is produced.

UUUU Unit number (0 through 15).

PAUSE

The Pause operator is shown in figure 1-9. The Pause I/O descriptor consists only of an OP field.

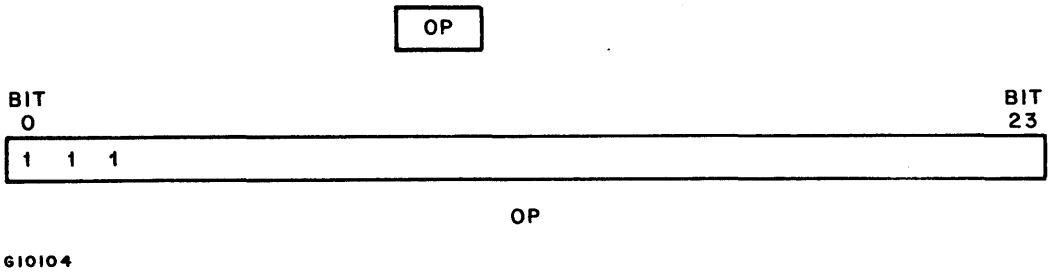


Figure 1-9. Disk File Pause Operator

This operator provides logic for the system to pause three to four milliseconds before it proceeds to the next I/O descriptor in the linked list. The operator is generated by the I/O driver upon detection of the P bit set in the Test operator. There is no actual Pause operator in the linked list of I/O descriptors. The I/O Control returns a service request to the system at the completion of the Pause operation and indicates, by resetting bit 17 of the Result descriptor, that no result is to be stored.

SEARCH

The Search operator and associated I/O descriptor fields are shown in figure 1-10.

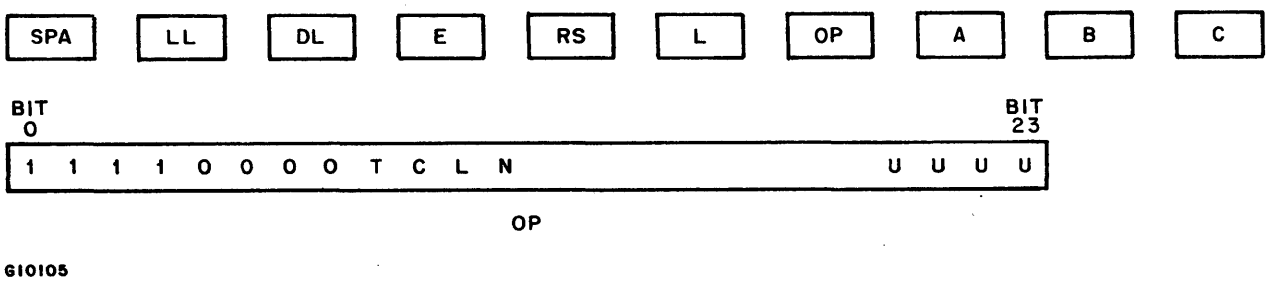


Figure 1-10. Disk File Search Operator

The first eight bits of the operator provide the code for Search (11110000). This operator provides logic to read data from the disk file, starting at the given file address, C, into ascending memory locations beginning at the location specified by the A address and continuing up to the address specified by the B address. As the data is being read, the key field located in the memory location specified by the SPA field is compared with the key field in each table entry until an equal condition is detected or until the entry list is exhausted, whichever occurs first. Detection of an equal condition does not terminate the storing of data. The variants and associated meanings for this operator are as follows:

T = 1 As described above (under Search operator).

T = 0 Only the table entry which terminated the search is stored. If there is no table entry, only the control information is stored following the last table entry.

C = 1 Terminates the comparison portion of the operation if a key field is encountered that is less than the key given in memory.

L = 1 Causes exit from the operation, using the M-link address if a match is detected and if the first bit of the 17-bit file address displacement in the matched entry is a 0. If the M-link address is taken, the file address, C, is modified in memory by adding to it the 17-bit address displacement obtained from this operation.

N = 0 The number of table entries is given in the Search Parameter Address (SPA) field of the I/O descriptor.

N = 1 The number of table entries is determined by the first 16 bits read from the disk file.

The format and usage of the Search parameters pointed to by the SPA are as follows:

a. 8 bits: Byte displacement from the start of table to table entry 0.

b. 16 bits: Entry number of the first table entry to be searched.

c. 12 bits: Reserved for I/O driver and Disk File Control use.

d. 12 bits: Length (in bytes) of a table entry.

e. 12 bits: Bit displacement from the start of table entry to the key field.

f. 12 bits: Length (in bits) of the key field.

g. 16 bits: Total number of table entries. This parameter is set to 0 at the end of the operation if no match is detected; otherwise, it is set to 1 plus the number of table entries left to be searched.

h. 24 bits: Memory address of key.

i. 12 bits: Bit displacement from the start of the table entry to a 17-bit segment displacement field that is to be added to the base segment address in the I/O descriptor pointed to by the M-link, if the M-link branch is taken.

j. 24 bits: M-link address that points to an I/O descriptor to be executed if a match is encountered and if the first bit of the 17-bit segment displacement field in the matched entry is equal to 0.

NOTE

If the Search operator is among a series of I/O descriptors controlled by a Lock descriptor, the M-link address must point to an I/O descriptor controlled by the same Lock descriptor.

STOP

The Stop operator and associated I/O descriptor fields are shown in figure 1-11.

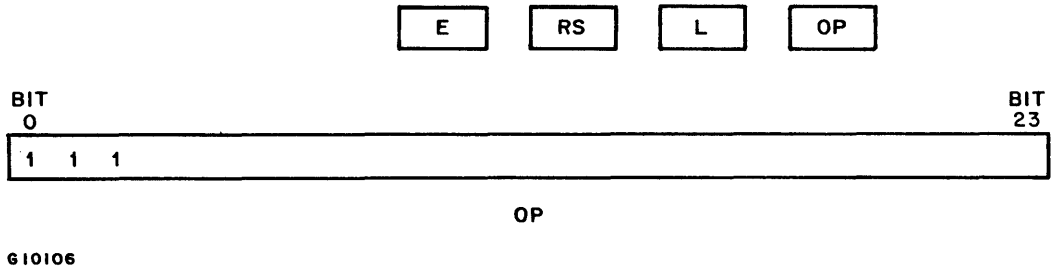


Figure 1-11. Disk File Stop Operator

The first three bits of the operator provide the code for the Stop operator. This operation is performed only by the I/O driver. Execution of this operation will cause the I/O driver to stop linking and return a Result descriptor.

LOCK

The Lock operator and associated I/O descriptor fields are shown in figure 1-12.

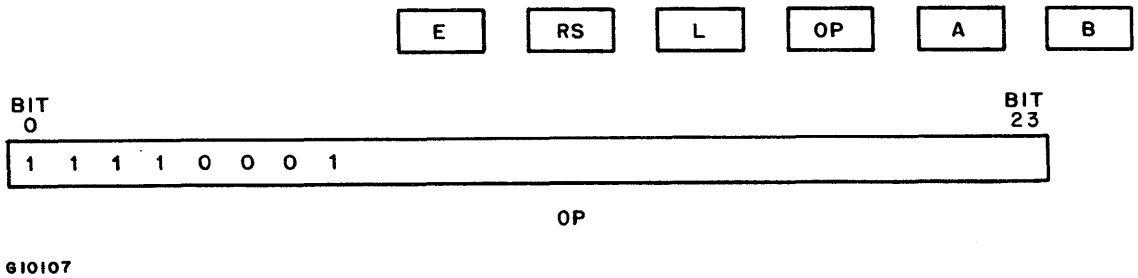


Figure 1-12. Disk File Lock Operator

The first eight bits of the operator provide the code for Lock. Execution of this command sets the I/O driver to a "locked" state, and results in an exit to the next I/O descriptor by means of the B-address. If the next I/O descriptor is not ready for execution (i.e., first two bits of the RS field are not equal to 00), the pointer to the RS field is saved by storing it into the B-field of the Lock descriptor; the Lock descriptor is unlocked and an exit is made, by means of the I/O descriptor LL field, to the next I/O descriptor.

If the next I/O descriptor is ready for execution, it is executed. After execution if no exception condition exists, an exit is caused, by means of the L-field address, to the next I/O descriptor. If the execution resulted in an exception condition, an interrupt is returned, the pointer to the RS field of the I/O descriptor is saved and an exit is made, by means of the LL field, to the Lock descriptor. The Lock descriptor is then "unlocked"; the I/O driver is set to the "unlocked" state, and an exit is made, by means of the Lock descriptor L-field address, to the next I/O descriptor.

If a Lock descriptor is encountered while searching for an I/O descriptor and the I/O driver is in the "locked" state, the I/O driver will move the RS pointer from the A field of the Lock descriptor to the B field. This move re-establishes the pointer to the current descriptor. The I/O driver then "unlocks" the Lock descriptor, sets the I/O driver to the "unlocked" state and exits, by means of the L-field, to the next I/O descriptor.

RESULT DESCRIPTOR

The Result descriptor consists of a 24-bit field that is stored in the RS field of the I/O descriptor at the completion of a Disk File Control operation. The storing of the Result descriptor in the RS field is accomplished by bit 16 (Operation Complete bit) of the Result descriptor being set. The Result descriptor is stored for Read, Write, Search, Test, and Stop operations. Pause and Lock Result descriptors are not stored or used.

The Result descriptor bit configuration and usage are shown in tables 1-2, 1-3, and in the following in-text table:

Bit Number	Description
0	Used to indicate that the operation is completed.
1	Indicates that an exception condition exists (one or more bits, 3 through 7, are set). Bit 2 will never be on for a Test Result descriptor.
2	Used to indicate that a not-ready condition existed during a Read or Write operation.
3	Used to indicate that a parity error was detected during a Read operation. The I/O Control generates an 8-bit parity check code for each segment. During a Write operation, the parity character is written following the last data bit in a segment. During a Read operation, the I/O Control creates a new parity character from the data read and compares it with the parity check character read from the disk file. If the two parity characters are not identical, bit 4 of the Result descriptor is set.
4	Reserved for future use.
5	Used to indicate that a memory parity error was detected during a Write operation.
6	Used to indicate that a Write operation was attempted but had to be terminated due to a Write lockout signal.
7-9	Used to provide disk file unit type identification during a Test operation. Identification is as follows: 000 Unit not present. 001 Systems memory. 010 Reserved. 011 1C-3. 100 1C-4. 101 1A-3. 110 1A-4. 111 Reserved.

Bit Number	Description
10-11	Used to indicate the Disk File Subsystem configuration for Test operation. System configurations are as follows: 00 No exchange. 01 Exchange number 1. 10 Exchange number 2. 11 Exchange number 3.
11	Used to indicate that a timeout condition has occurred during a Read or Write operation. A timeout is defined as a failure to receive clocks from the disk file unit after address coincidence has been achieved.
12-13	Used to indicate the Disk File Control identification. 00 Control number 0. 01 Control number 1. 10 Control number 2. 11 Control number 3.
14-15	Reserved for future use.
16	Used to determine if the Result descriptor is to be stored in the RS field of the I/O descriptor. If bit 17 is set, the Result descriptor will be stored. Bit 17 is also named "operation complete."
17-23	Used to indicate the I/O control type identification for a Test operator. For a B 1700 Disk File Control I or II, the bit configuration will be 0011000.

Table 1-2. Result Descriptor (All Operators Except Test)

Bit	Function
0	Operation complete.
1	Exception condition exists (one or more bits (2 through 6) are set).
2	Not ready (Read or Write operation).
3	Read parity error (Read operation).
4	Reserved.
5	Memory parity error (Write operation).
6	Write lockout (Write operation).
7-10	Used for Test only.
11	Timeout (Read or Write operation).
12-13	Control number (00 equals 0; 11 equals 3).
14-15	Reserved.
16	Operation complete.
17-23	Used for Test only.

Table 1-3. Disk File Control Test Operator Result Descriptor

Bit	Function
0	Operation complete.
1-6	Not used for Test.
7-9	Type of disk file: 000 Not present. 001 Systems Memory. 010 Reserved. 011 1C-3. 100 1C-4. 101 1A-3. 110 1A-4. 111 Reserved.
10-11	Disk File Subsystem configuration: 00 No exchange. 01 Exchange 1. 10 Exchange 2. 11 Exchange 3.
12-13	Control number: 00 0 01 1 10 2 11 3
14-15	Reserved.
16	Operation complete.
17-23	Control-type identification will always be 0011000 for Disk File Control I or II.

GLOSSARY OF TERMS

Logic Name	Card Schematic Page	Backplane, Testpoint, Chip/Pin	Function
1USB	1-2	OLY	1-Microsecond Bus.
4USB	1-2	OMY	4-Microsecond Bus.
32USB	1-2	OSX	32-Microsecond Bus.
1024USB	1-2	OTX	1024-Microsecond Bus.
AC=1...0	4-7	OKX	Address Counter.
AC=2...0	4-7	1HX	Address Counter.
AC=3...0	4-7	1GY	Address Counter.
ADCL...0	3-5	1MX	Address Compare Level. High for each digit of address which compares with address from disk.
BFARCO(N)	3-6		Binary File Address
BFAR#0.0	3-6	OYX	Register. Used to store and decode file address.
BFARHI	3-6		Buffer Ready.
BUFRDY	2-5	A6-K	Buffers Empty. Flags that
BUFSEMPO	2-5	1FX	buffers are empty on Write.
BUFSFLF1	2-5		Buffers Full. Flags that buffers are full on Read.
CHANHI	1-7	1SY	Channel Hi. Flags that a message has been decoded for this channel.
CLRCHANO	1-2,3,5	OFY	Clear Channel.
CLKENB(N)	2-7		MOS Clock Enable Levels.
CMDR(N)F..	2-4	E8-K,N,P	Command Variant Register.
CNLUR(N)F1	2-4	E9-K,N,P	Channel Variant Register.
COHI...0	3-6	1SY	Carry Out High Position. Causes a carry or borrow from MSB in BFAR.
COH1L..0	3-8	OQY	Carry Out High Latch. Used to "remember" that COHI occurred during a cycle.
CT1L...0	4-7	OKY	Character Transfer Levels.
CT2L...0	4-7		Used to sync data transfer clock (FCLP) from disk.
DABC	3-5	A9	Disk Type levels.
DF(N)F...1	3-4	C6	Disk Face Register/Center.

GLOSSARY OF TERMS (Cont)

Logic Name	Card Schematic Page	Backplane, Testpoint, Chip/Pin	Function
DSM....0	3-5	OHY	Disk Systems Memory level (Disk Type).
DTMR=1,2,4	4-6	D9	The Disk Timer is used to: a. Provide for a program exit if a timeout occurs. b. Count head-settling time. c. Count the delay time of a Pause OP.
DUMP(X)..0	2-5	D3	Dump counter and decoder.
EU(NN)F...	3-5	B8	Electronics Unit register.
EUBUSY..	4-4	F3-P	Electronics Unit Busy level.
EXIL			External Exchange Present level.
EX1TF..1	2-3	G8	Exit flip-flop.
FCLP...0	3-1	1NX	File Character Clock Pulse; one per byte of data transferred to/from disk.
HASF.1.1 HBSF.1.1	4-4 4-4	G9) G9)	Hub A and B Select flip-flops. Used to select one or the other side of 1 x 2 exchange.
INXL...0 INXF...0	4-6 4-6	1CX OMY	Index level. 1-clock sync level.
INXP...0	3-1	1EY	Index Pulse. Comes from disk (located between last segment on track and maintenance segment).
ITSF.1.1	4-7	C3H	Information Track Select. Switches from address to information tracks.
LOAD(X)..0	2-5	D4	Load Counter and Decoder.
LPC1F, LPC2F	4-5	E8	Longitudinal Parity Character 1 and 2 Flip-Flops. Used to synchronize LPCP.
LPCP...0	3-1	OEY	Longitudinal Parity Clock Pulse; from disk at end of each segment (1 FCLP wide for read and 2 FCLP's wide for write on disk).

GLOSSARY OF TERMS (Cont)

Logic Name	Card Schematic Page	Backplane, Testpoint, Chip/Pin	Function
LPR(N)...	4-5	G6	Longitudinal Parity Register.
LPTL			Longitudinal Parity Transfer Level. A synchronized 1-clock level after LPCP goes false.
MA INT..0	2-4	OTX	Maintenance segment operation variant.
(NN)BUT...	3-6		Parameters NN = 00 through 16. Represent number per "unit" being decoded during address decode time.
OPR(N)...1	2-4	E6	OP Register.
QL(N)L.1.0	4-1		Read Lines (8 from DFEU).
RD+WR	2-6	JOK	Read or Write term. Used to differentiate from Test and Pause to start segment counts.
SACP...0	3-1	KOJ	Segment Address Clock Pulse (just prior to each segment address on disk).
SAEF	4-7	C4H	Segment Address Equal Flip-Flop. During address compare, it stays set for each digit of address from disk that compares with desired address.
SAFL..	4-7	OPY	Segment Address Found Level. True for 1 clock when segment address fully compares.
SAFL...0	4-7	OPY	Segment Address Found Level. True for 1 clock when all three digits of segment address have compared with segment address on disk.
SAHIF...	3-5	BO	Segment Address Register (hundreds, tens, and units digits).
SAT(N)F...	3-5	B1	
SAU(N)F...	3-5	B2	
SC(N)F...0	2-3	G7	Sequence Counter - NN = 00 through 15.

GLOSSARY OF TERMS (Cont)

Logic Name	Card Schematic Page	Backplane, Testpoint, Chip/Pin	Function
SSF....0	3-8	OLY	Suppress Set Flip-Flop. When on during address decode, suppresses the clock to BFAR.
SS2F...0	3-8	ONY	Suppress Set 2 Flip-Flop. Extends duration of SS Flip-Flop to two clocks during address decode.
STC(N)...	2-2		Status Counter (NN = 00-23)
SU(N)F...1	3-4	C7	Storage Unit level.
SUBTIME.	3-8	L6K	Subtract Time. Used to gate parameters to BFAR.
SURF			Storage Unit Ready Flip-Flop (set by SURL).
SURL...0	3-1	OYY	Storage Unit Ready level (from disk).
TERM....	2-4	D9H	Terminate Variant Level.
TSR....1	2-4	D9J	Test Variant Level.
TSTCLR..	2-4	D9N	Test and Clear Variant Level.
TT(N)F...1	3-4	C5	Track Tens Digit.
TU(N)F...1	3-4	C4	Track Units Digit.
WAIT...0	2-4	OUX	Wait Variant level. Causes program to do this OP if DFEU is busy.
WDCT 1011	2-5	A5K	Word Counter Level.
WDCT 88.1	2-5	C1N	Word Counter Level.
WDCT 90.1	2-5	C1K	Word Counter Level.
W1SL....	4-7	B5K	Write Information Select Level to disk indicates a Write operation.
WL(N)L...0	1-6		Write Lines (8 to disk).
WLOF...0	4-4	1SY	Write Lockout Flip-Flop - set by WMLL.
WMLL.A..	3-1	K1P	Write Manual Lock Level. (True if any of the lockout switches are on in the DFEU.)
XFRIN..1	2-4	D8K	Transfer In. Used with state counts to gate information to Input Register.
XFROTA.1	2-4	D8P	Transfer Out. Used to gate out of register.
ZN(N)F...0	3-4	C3	Zone Select Levels.

SECTION 2

FUNCTIONAL DETAIL

INTRODUCTION

This section provides information on the operation and function of the B 1700 Disk File Controls I and II. The primary difference between the two controls is that the Disk File Control II can accommodate more types of Disk File Storage Units than the Disk File Control I. Both Disk File Controls consist of four B 1700 size logic cards. Cards 1 and 2 of both controls are identical; cards 3 and 4 of the Disk File Control II have internal changes to accommodate additional disk file devices. The disk file devices and the associated Disk File Controls are listed in table 2-1.

Table 2-1. Disk File Devices

Disk File Electronics Unit	Disk File Storage Unit	Disk File Control
IA	IA-3	I,II
IA	IA-4	II
IC	IC-3	I,II
IC	IC-4	I,II
NA	Systems Memory	II

PROCESSOR-TO-I/O-CONTROL FLOWS

The operation of the Disk File Control is determined by the I/O descriptor operator and the Status Counter (STC). An overall description of the Status Counter functions, in conjunction with various disk file operators, is shown in figure 2-1. Individual disk file operators and the applicable status counts are shown in figures 2-2 through 2-4. In addition to the Status Counter, a Sequence Counter (SC) is used to define certain operations (such as address decoding) within a status count. A flow chart of the Disk File Control Sequence Counter is shown in figure 2-5.

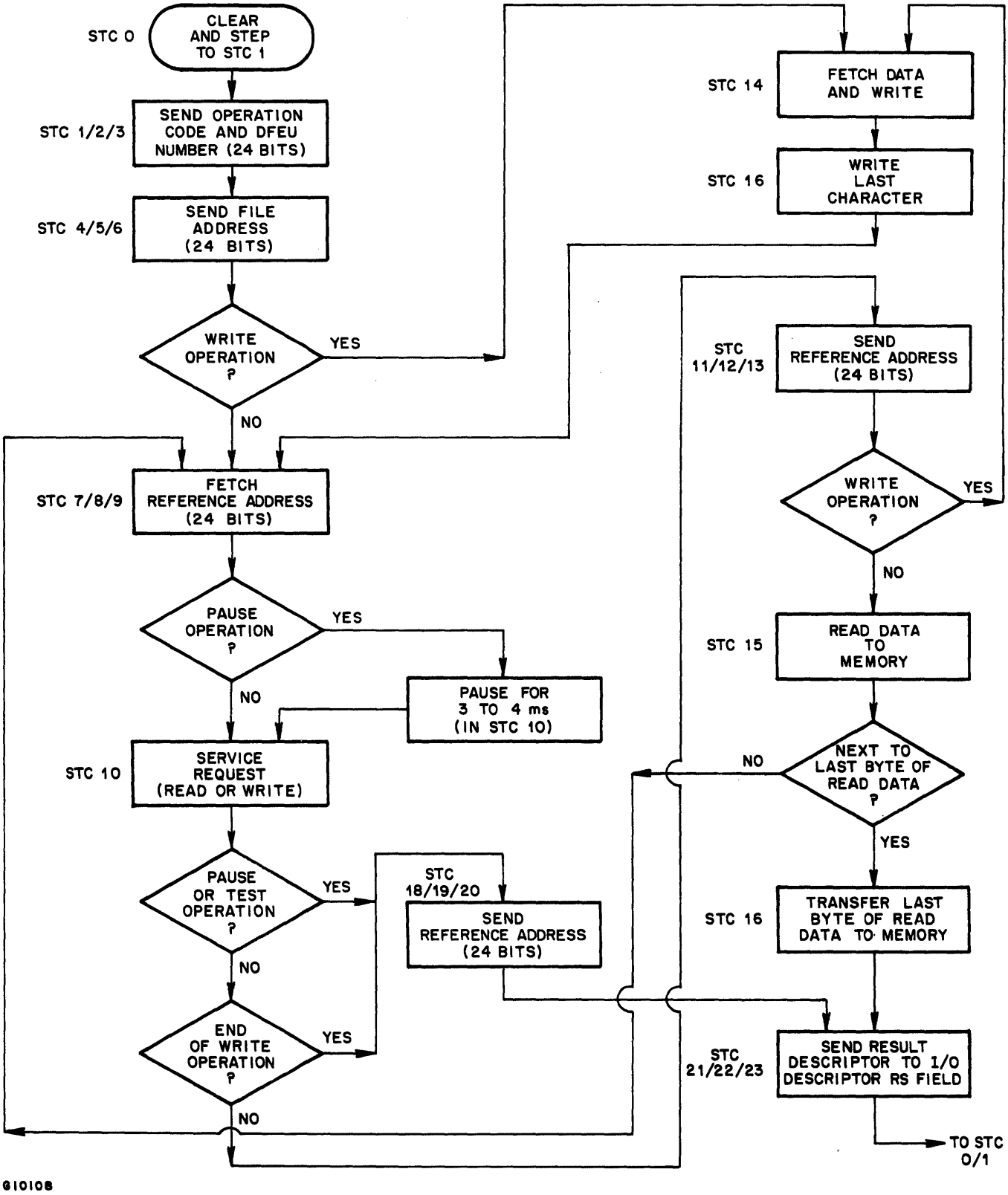


Figure 2-1. Processor-to-Control Flow Chart

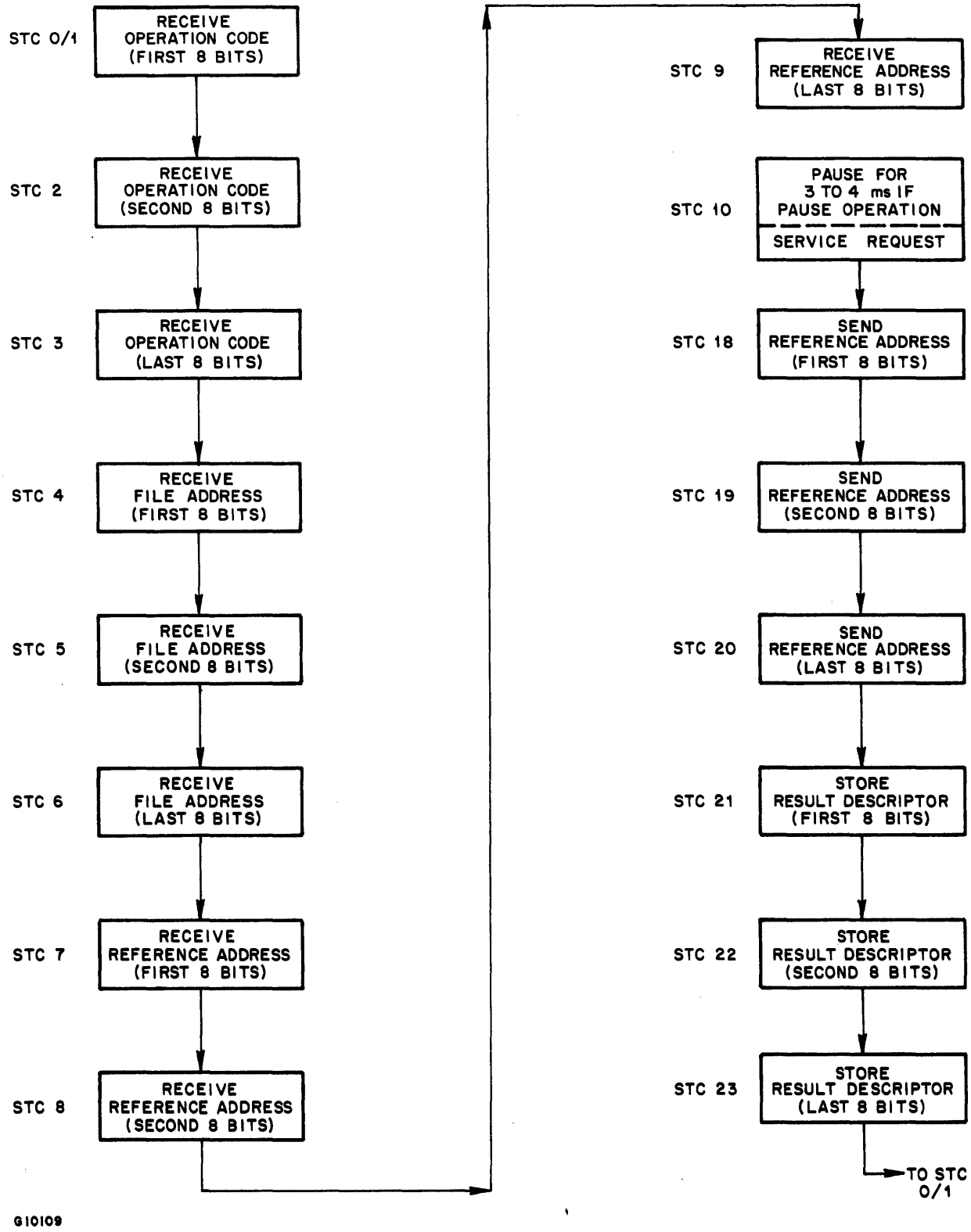


Figure 2-2. Pause/Test Processor-to-Control Flow Chart

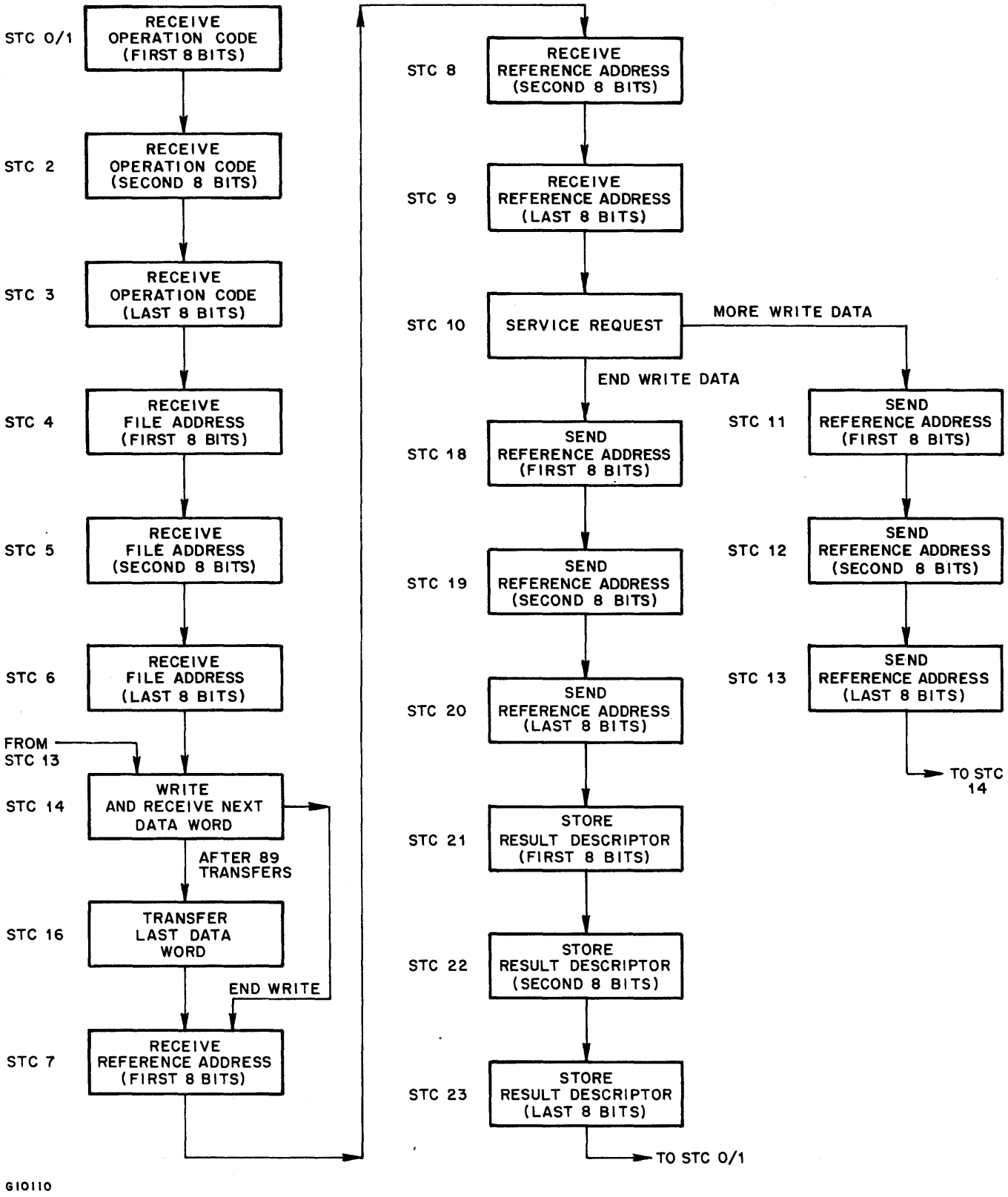


Figure 2-3. Write Processor-to-Control Flow Chart

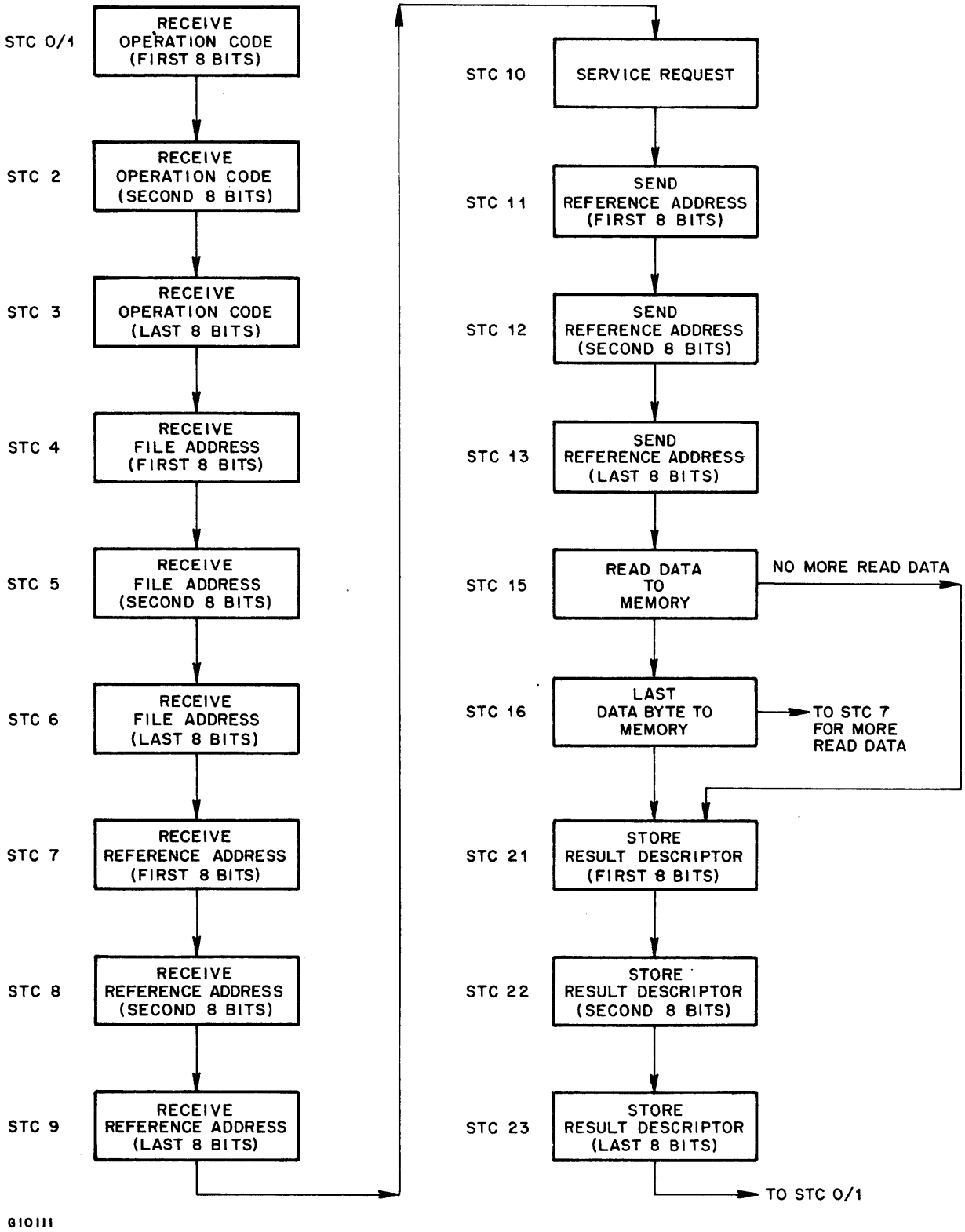


Figure 2-4. Read Processor-to-Control Flow Chart

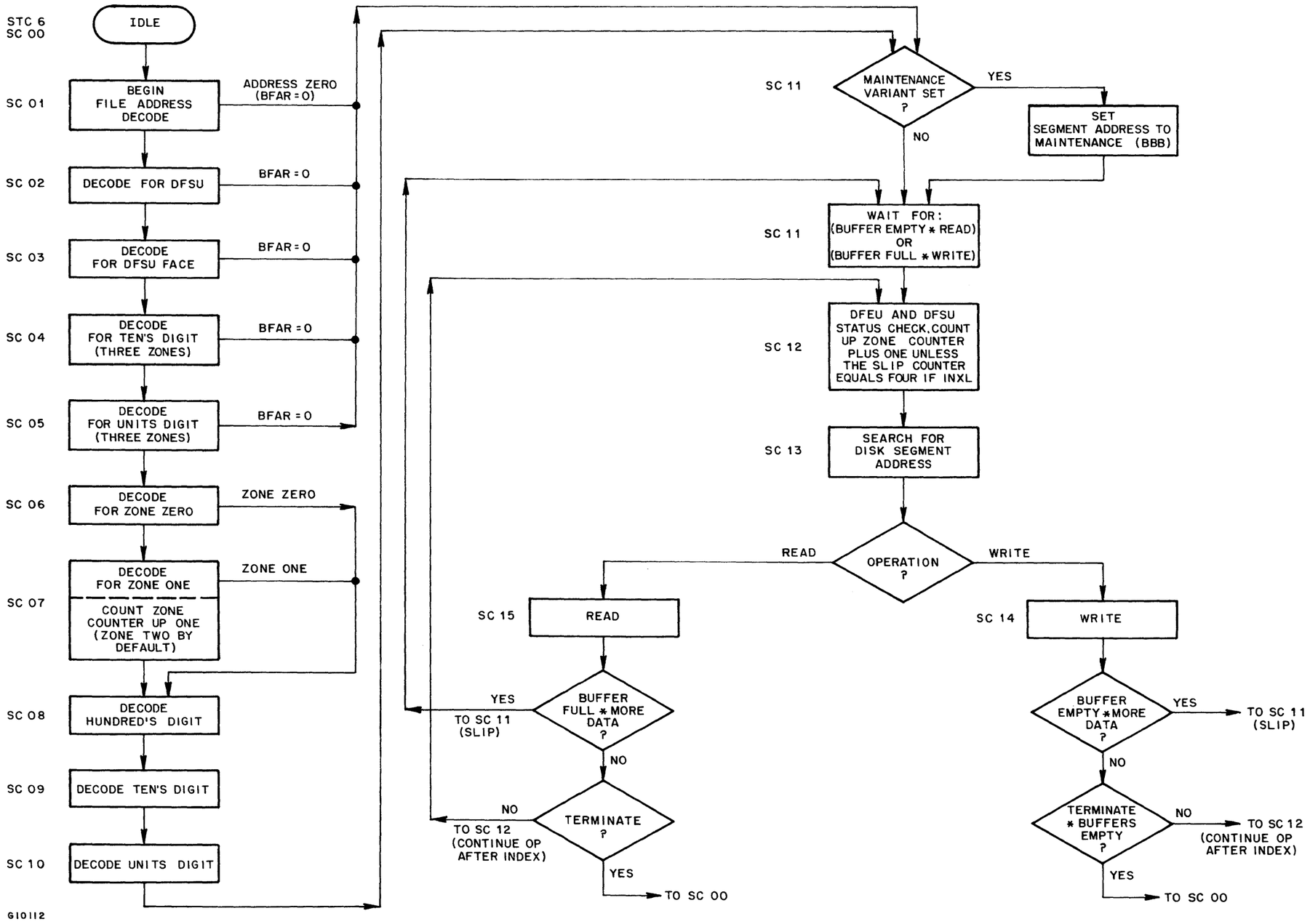


Figure 2-5. Disk File Control Sequence Counter Functions

DISK FILE CONTROL FLOWS

The following flows depict the detailed description of logic controlled by the Sequence Counter (SC). The sequence counter is initiated at Status Count 6 (STC6). At STC6 time, the I/O Control has received the operation code (OP) associated variants and the disk address to be accessed. The "Sequence Count Any" (SCANY) logics are floating logics that can occur at any time during the flow.

SCANY

SC ← 0 ITSF ← 0	EXITF	This logic clears the Sequence Counter and stops all information flow from the exchange to the DFEU.
SURF ← 0	SC=02/ *SURL/	This logic resets the Storage Unit Ready flip-flop if the DFSU is not-ready.
WLOF ← 1	(SC4F) *WMLL *WRITE	
EXITF ← 1	(SURF/ *WLOF) *(SC4F+SC8F)	The control exits the flow if the DFSU is not-ready or locked out.
HASF.1.1 ← 1	EXILF +MCTRL *EU=00 * HASF/1 *HASF/22 *SETEUZO +SLVCTL *EU=02 *HASF/1 * HASF/22	This logic provides DFEU selection through a master or slave I/O control, using either hub A or B of each I/O control.
HASF.2.1 ← 1	MCTRL *EU=02 * HASF/12 +SLVCTL *EU=00 *HASF/2 * HASF/12 *SETEUZO	
HBSF.1.1 ← 1	MCTRL *EU=01 *HBSF/1 * HBSF/22 +SLVCTL *EU=03 *HBSF/1 HBSF/22	
HBSF.1.1 ← 1	MCTRL *EU=02 *HBSF/12 * HBSF/2 +SLVCTL *EU=01 *HBSF/12 *	

(Cont)

SCANY (Cont)

	HBSF/2	
MCTRL	MASTER *EXILF/	
SLVCTL	SLAVE *EXILF/	
SETEUZO	STC04 *CA	
EUBUSY ← 1	MCTRL *EU=01 *HBSF.221 +SLVCTL *EU=03 *HBSF.221 +MCTRL *EU=03 *HBSF.121 +SLVCTL *EU=01 *HBSF.121 +MCTRL *EU=00 *HASF.221 +SLVCTL *EU=02 *HASF.221 +MCTRL *EU=02 *HASF.121 +SLVCTL *EU=00 *HASF.121 +EUBL	DFEU Busy flip-flop.
INXPF ← 1	INXP	This logic provides index pulse sensing and generation that is used for syncing the control to the DFSU.
INXPF1 ← 0	INXP/	
INXPF2 ← 1	INXPF1	
INXPF2 ← 0	INXPF1/	
EXITF ← 1	DTMR=T0 *SC=11/	This logic causes an exit from the flow. The exit for an open or erased track (time-out) is shown at STC11.

The following logic consists of the sequence counts that handle the interaction between the I/O Control and the disk file unit. The logic primarily concerns Address Search, Read or Write data transfers, and error checking.

SC=00 Wait

SC+1	RC *STC06 *SFROTA *(EUBUSYF/ +WAIT) *(READ +WRITE)	The Sequence Counter is equal to 00 during STC counts 1 through 5. The following SC counts are accomplished at STC06 time.

SC=01 Address Decode Start

SURF+1		The disk file control assumes the DFSU is ready by setting the Storage Unit Ready flip-flop.
COHIL ← 1	COHI *SSF/	SSF and SS2F are used to suppress the clock to the binary file address register for two clock periods during address decode. Refer to BFAR DETAIL.
COHIL ← 0 SS2F ← 1	SSF	
SS2F ← 0 SSF ← 0	SS2F	
SSF ← 1 SC+1	BFAR≠0 *SSF/	The Sequence Counter changes from SC 1 to SC 2.
SC ← 11	BFAR=0	The control transfers to SC 11 if address is found (no decoding is necessary, since address equals 0).

SC=02 FIND SU (SUBT. SEG./SU)

This logic is used to determine the DFSU.

BFAR-PRM01	COHIL/	The control subtracts parameter 01 from BFAR to determine Disk File Storage Unit.
COHIL ← 1	COHI *SSF/	These delays are used for propagation of the carry level. Refer to BFAR DETAIL.
COHIL ← 0 SS2F ← 1	SSF	
SS2F ← 0 SSF ← 0	SS2F	
SU+1 SSF ← 1	SSF/ *COHIL/ *BFAR≠0	
SSF ← 1 SC+1	SSF/ *CHOIL *BFAR≠0	
SC ← 11	BFAR=0	SC is incremented by 1 if further decoding is necessary. The control goes to SC 11 if no further decoding is required.

SC=03 FIND DISK FACE (SUBT. SEG./SU)

BFAR-PRM02	COHIL/	This logic is used to determine the disk face. The 02 parameter is subtracted from BFAR to determine disk face.
COHIL ← 1 COHIL ← 0 SS2F ← 1	COHI *SSF/ SSF	
SS2F ← 0 SSF+0	SS2F	Refer to BFAR DETAIL.
DF+1 SSF ← 1	SSF/ *COHIL/ *BFAR≠0	
SSF ← 1 SC+1	SSF/ *COHIL *BFAR≠0	
SC ← 11	BFAR=0	The control goes to SC 11 if no more decoding is required.

SC=04 FIND SEG. IN 10TRKS03 ZONES

BFAR-PRM03	COHIL/	This logic is used to determine the tens digit of track. The 03 parameter is subtracted from BFAR to determine tens digit of track.
COHIL ← 1	SSF/ *COHI	
COHIL ← 0 SS2F ← 1	SSF	
SS2F ← 0 SSF ← 0	SS2F	Refer to BFAR DETAIL.
TT+1 SSF ← 1	SSF/ *COHIL/ *BFAR≠0	
SSF ← 1	SSF/ *COHIL *BFAR≠0	
SC+1		SC is incremented to SC 5 if further decoding is needed.
SC ← 11	BFAR=0	The control goes to SC 11 if no more decoding is required.

SC=05 FIND SEG. IN 1TRK-3 ZONES

This logic is used to determine the units digits of track.

BFAR-PRM04	COHIL/	The 04 parameter is subtracted from BFAR to determine ones digit of track.
COHIL ← 1	SSF/ *COHI	Refer to BFAR DETAIL.
COHIL ← 0 SS2F	SSF	
SS2F ← 0 SSF ← 0	SS2F	
TU+1 SSF ← 1	SSF/ *COHIL/ *BFAR≠0	
SSF ← 1	SSF/ *COHIL *BFAR≠0	
SC ← 11	BFAR=0	SC is incremented to SC 6 if further decoding is required. The control goes to SC 11 if no further decoding is required.

SC=06 FIND SEG. IN ZONE 0

This logic is used to determine if the address is in zone 0.

BFAR-PRM05	COHIL/	The 05 parameter is subtracted from BFAR to determine if address is zone 0.
COHIL ← 1	COHI *SSF/	Refer to BFAR DETAIL.
COHIL ← 0 SS2F ← 1	SSF	
SS2F ← 0 SSF ← 0	SS2F	
ZN+1 SSF ← 1 SC+1	SSF/ *COHIL/ *BFAR≠0	The address is not in zone 0. The control goes to SC 7 to check for zone 1.
SSF ← 1 SC ← 08	SSF/ *COHIL	The control goes to SC 8 if the zone is 0.

SC=07 FIND SEG. IN ZONE 1

BFAR-PRM06	COHIL/	This logic is used to determine if the address is in zone 1. The 06 parameter is subtracted to determine if address is in zone 1.
COHIL ← 1	COHI *SSF/	
COHIL ← 0 SS2F ← 1	SSF	Refer to BFAR DETAIL.
SS2F ← 0 SSF ← 0	SS2F	
ZN+1 SSF ← 1 SC+1	SSF/ *COHIL/ *BFAR≠0	The address is not in zone 1. SC is incremented to SC 8.
SSF ← 1 SC ← 08	SSF/ *COHIL	If the address is zone 1, the zone counter remains at 1 and the control exits to SC 8.

At this point in the flow, DFSU face and track have been determined. Segment address must now be converted from binary to address line representation.

SC=08 CONV. SEG. HUNDREDS TERM

BFAR-100	COHIL/ *BFAR≠0	This logic is used to determine the segment address hundreds digit. The control subtracts 100 from BFAR to determine hundreds digit.
COHIL ← 1	COHI *SSF/	Refer to BFAR DETAIL.
COHIL ← 0 SS2F ← 1 SS2 ← 0 SSF ← 0 SAH+1	SSF SS2F SSF/ *COHIL/ *BFAR≠0	The control upcounts segment address hundreds digit by 1 for each subtraction.
SSF ← 1	SSF/ *BFAR≠0	Refer to BFAR DETAIL.

(Cont)

SC=08 CONV. SEG. HUNDREDS TERM (Cont)

SC+1	SSF/ *COHIL *BFAR≠0	SC is incremented to SC 9, since the hundreds digit has been determined.
SSF ← 0 SC ← 11	BFAR=0	SC is set to SC 11, since no further decoding is required.

SC=09 CONV. SEG. TENS TERM

This logic is used to determine tens digit of segment address.

BFAR-10	COHIL/ *BFAR≠0	The control subtracts 10 from BFAR to determine tens digit.
COHIL ← 1	COHI *SSF/	
COHIL ← 1 SS2F ← 1	COHI *SSF/	Refer to BFAR DETAIL.
SS2F ← 0 SSF ← 0	SS2F	
SAT+1	SSF/ *COHIL/ *BFAR≠0	The control increments segment address tens counter by 1 for each successful subtraction.
SSF ← 1	SSF/ *BFAR≠0	Refer to BFAR DETAIL.
SC+1	SSF/ *COHIL *BFAR≠0	When tens digit is determined, the control increments SC to SC 10.
SSF ← 0 SC ← 11	BFAR=0	The control goes to SC 11 if no further decoding is required.

SC=10 CONV. SEG. UNITS TERM

BFAR-1	COHIL/ *BFAR≠0	This logic is used to determine units digits of segment address. The control subtracts 1 from BFAR to determine file address units digit.
COHIL ← 1	COHI *SSF/	
COHIL ← 0 SS2F ← 1	SSF	Refer to BFAR DETAIL.
SS2F ← 0 SSF ← 0	SS2F	
SAU+1	SSF/ *COHIL/ *BFAR	The control upcounts segment address units digit plus 1, for each successful subtraction.
SSF ← 1	SSF/ *BFAR≠0	
SC+1	SSF/ *COHIL *BFAR≠0	SC is incremented to SC 11 because the units digit is determined.
SC ← 11	BFAR=0	The control goes to SC 11 if no further decoding is required.

At SC 11 time, the control has completely decoded the field address.

SC=11 HOLD TILL READY

SAH ← 11 SAT ← 11 SAU ← 11	MAINT	This logic is used to allow the control to wait (Slip) until the buffers are ready. The control sets the segment address for a maintenance segment operation (1011 1011 1011).

SC=11 HOLD TILL READY (Cont)

SC+1	(BUFRDY *WRITE + READ *BUFSFLF/) *LPTL *CTIL	The control upcounts SC to SC 12 when buffers are ready, allowing the operation to continue.
SLTMR+1	SLTMR ≠ *32USB *DLIPG	The control upcounts Slip timer by 1. Refer to SLIP DETAIL.
INXF ← 1	SLIPF *INXPSY *SLTMR ≠ 4	The control sets Index Pulse flip-flop during Slip cycle.
ITSF ← 0	(BUFRDY *WRITE + READ * BUFSFLF/) *LPTL *CT1L +DTMR=TO	The control resets track select to switch from information track to address track.
LPC1F ← 1	LPCP	This logic is used to synchronize the Longitudinal Parity Character (LPC).
LPC1F ← 0 LP2F ← 0	LPC2F (LPTL)	The control resets Longitudinal Parity (LP) flip-flops after LP time.
SLIPF ← 0 DTMR ← 0 SLTM ← 0	LPTL +DTMR=TO	The control resets Slip flip-flop, Disk timer, and Slip timer at LP time.
CT1F ← 1	FCLP	
DTMR+1	(BUFRDY *WRITE + READ *BUFSELF/) *1024USB	The control flags a disk timeout condition.
SC+1 INXF ← 0	DTMR=TO	The sequence counter is incremented to SC 12, providing an exit under timeout conditions.
CT2F ← 1	CT1F	This logic is used to synchronize character transfers with disk file clock pulses.
CT1F ← 0	FCLP/	
CT2F ← 0	CT1F/	
CT1L	CT1F *CT2F/	

SC=12 EU/SU STATUS CHECK

This logic checks DFEU/ DFSU status, allows head-settling time, enables LP register and sets up address counter upcount for crossover.

SLIPF ← 0		The control resets Slip flip-flop to take the control out of Slip mode.
EUBUSYF ← 0 HTMR+1	EUBUSY/ EUBUSYF/ *32USB *HTMR=7F	The DFEU is busy. The control counts Head-Settling timer by 1.
TSDL ← 1	HTMR=7F/	The Track Select Delay is set.
SURF ← 0	SURL/	The DFSU is not ready.
SACF ← 1	SACP *HTMR=7F *DTMR≠ TO *DFCOF/	The control waits for Segment Address clock pulse plus 200 microseconds, then goes to SC 13 for address search.
SACF ← 0 LPR ← 1 SC+1	SACF	The control enables LP register to be set to 1. SC is incremented to SC 13.
AC ← 02	SACF *DSM	The control sets Address Counter to 2 for a Systems Memory disk subsystem.
AC+01	SACF *UABC	The control sets Address Counter to 1 for disk types A or C.
DTMR+L	HTMR=7F *1024USB *(WRITE *BUFRDY + READ *BUFSFLF/)	Refer to TIMER DETAIL.
HTMR=7F ← 1	DTMR=7	
INXF ← 0 SEGREG ← 0	INXF	The control resets the Index flip-flop and the Segment register at index time.
INXL	INXF	INXL is set by Index pulse.

(Cont)

SC=12 EU/SU STATUS CHECK (Cont)

ZN+1	INXL *DABC
TU+1	INXL *DSM
SU+1	DFCOF *(WRITE + READ) *BSFSEMP *TERMF/ *STC10 *JUSTF/
DFCOF ←1	DFCO
DFCOF ←0	SU+1

The control upcounts the appropriate counter if the control entered this sequence count completing a zone, track, or DFSU decode operation.

SC=13 DISK ADDRESS SEARCH

During SC=13, each digit of the segment address is compared with the segment address digits read from disk. When both segment addresses are equal, the DFC is notified that the correct address is found. The control will stay in SC 13 until the segment address is found.

SACF ←1	SACP *HTMR=7F *DTMR≠TO *DFCOF/	Segment Address Compare flip-flop is set to 1.
LPR ←1 SACF ←0	SACF	The control resets Segment Address Compare flip-flop.
AC ←01 SAEF ←0	SACF *DABC	The control compares the first segment address digit of the next address with that of the file address.
AC+1	CT1L	The control upcounts the Address Counter with Character Transfer level.
AC ←02 SAEF ←0	SACF *DSM	The control sets AC = 2 for the first digit of next address.
SAEF ←1	CT1L *ADCL *(AC=01 +AC=02 *DSM)	The Segment Address Equal flip-flop is set when the first digit of the segment address compares with the first address digit read from disk (AC = 2 for Systems Memory).

(Cont)

SC=13 DISK ADDRESS SEARCH (Cont)

SAEF ← 0	CT1L *AC=02 *ADCL/	The Segment Address Equal flip-flop is reset if the second digit does not compare.
SAFL ← 1 SAEF ← 0 AC ← 0	CT1L *AC=03 *ADCL *SAEF	The Segment Address Found level is true if the third digit compares; also, the Segment Address Equal flip-flop is reset and the Address Counter is set to 0.
ITSF ← 1	SAFL *(WRITE *BUFRDY +READ *BUFSFLF/)	The control switches from address track to information track when the address is found.
SC ← 14	SAFL *WRITE *BUFRDY	The control goes to SC 14 if this is a Write operation.
SC ← 15	SAFL *READ *BUFSFLF/	The control goes to SC 15 if this is a Read operation.
DTMR+1	1024USB *HTMR=7F * (WRITE *BUFRDY + READ *BUFSFLF/)	The Disk timer is set.
SURF ← 0	SURL/	The control enables SCANY logic SURF to exit if the DFSU goes not ready.
INXF ← 0	INXL	The control upcounts track and zone if Index is encountered.
INXL	INXF	
ZN+1	INXL *DABC	
TU+1	INXL *DSM	
CT1F ← 1	FCLP	Character Transfer level is used to synchronize disk data transfer with the disk file clock.
CT2F ← 1	CT1F	
CT1F ← 0	FCLP/	
CT2F ← 0	CT1F/	
CT1L	CT1F *CT2F/	
CT2L	CT1F/ *CT2F *LPC1F/	

SC=14 WRITE

At SC 14 the control has found the complete disk address and will now transfer Write data to the disk.

SLIPF ← 1		
WISL ← 1	ITSF *ITSK/	Write Information Select level is sent to disk file, indicating a Write operation.
STPWR	TERMF *BUF=01	The control stops the Write operation because this is the last record.
STPWRF ← 1	STPWR *CTlL *LPTMF *LPCP	The Stop Write flip-flop is set with STPWR at LP Clock pulse.
STPWRF ← 0	LPTL	The Stop Write flip-flop is reset at LP transfer time.
ITSK	(ITSF ← 0 +STPWRF)/	
WL ← OUTREGN0	LPClF/ *WDPTF/ *DUMP(N)	The control transfers the contents of the output registers to the write line. OUTREGN0 equals the upper register; OUTREGN1 equals the lower register.
WL ← OUTREGN1	LPClF/ *WDPTF *DUMP(N)	
WDPTF ← WDPTF/	CTlL *LPClF/	The control resets Word Pointer during LP write (no more data in buffer).
OUTREGN ← MOS(N) SHIFO(N)	 WDPTF *CTlL *DUMP(N) WDPTF *CTlL *DUMP(N)	The control shifts data through the buffer to the output register.
CLKENB(N) ← 1	SHIFO(N)	
LPClF ← 1 LPC2F ← 1	CTlL *LPCP LPCP/ *LPClF	The control generates Longitudinal Parity Time level to write LP character.
LPTL ← 1	LPClF *LPC2F	
LPClF ← 0 LPC2F ← 0 SA+1	LPTL	LPT logic is reset at LP time. The control increments the Segment Address register plus 1 for next segment address.

(Cont)

SC=14 WRITE (Cont)

WL ← LPR	LPC1F *BRKFBL/	The control shifts LP register to write lines.
LPR ← 1	LPTL	The LF register is reset after shifting information to write lines at LP time.
INXF ← 1	INXPSY *MAINT/	The control clock synchronizes with the Index pulse.
SC ← 12 ITSF ← 0	INXF *EXITF/	The control goes to SC 12 for next compare at Index pulse.
EXITF ← 1	LDTLDYF *BUFSEMP *TERMF *WDCT=0 *JUSTF/ +MAINT *LPTLDLY +DTMR= TO	The control resets Information Track Select to check for address. Sets Exit flip-flop since Write operation is complete (no more data from the processor).
LPR @ WL	CT2L	The information in the LP Character register is transferred to write lines at Transfer-2-level time.
ITSF ← 0	EXITF	The control resets Address Track Select if exit conditions exist.
CTLF ← 1	FCLP	This logic is used to synchronize data transfer with the disk clock.
CT2F ← 1	CT1F	
CT1F ← 0	FCLP/	
CT2F ← 0	CT1F	
CT1L	CT1F *CT2F/	
CT2L	CT1F/ *CT2F *LPTMF/ + LPTLDYF	
DTMR+1	1024USB	This logic provides a time-out condition if open or erased track occurs.

(Cont)

SC=14 WRITE (Cont)

LPTMF ← 1	LPC1F	The control goes to SC 11 to slip one revolution if the address is found but no write data is available from the buffer.
LPTMF ← 0	LPC1F/ *CT1L	
SC ← 11	LPTLDYF *BUFSEMP	
LPTLDYF ← 1	LPTL	This logic provides a delay time between the end of information and the LP character.
LPTLDYF ← 0	LPTLDYF	
DTMR ← 0 HTMR ← 0	LPTL	The control resets the Head and Disk timers at LP transfer time.
ITSF ← 0	LPTLDYF *BUFSEMP *WDCT=0 *JUSTF/ *TERMF	The control selects address track at the completion of an LP Write following the data Write.

At SC 15 the control has found the complete file address and is ready to accept the Read data from the disk file.

SC=15 READ

SLIPF ← 1		
INLCH0 ← RDLNS INCH1 ← RDLNS	CT1L *WDPTF/ *LPCP/ CT1L *WDPTF *LPCP/	The control gates the Read lines from the disk file to the input register. INLCH0 is the lower buffer area; INLCH1 is the upper buffer area.
WDPTF ← WDPTF/	CT1L *LPCP/	This logic controls the delay and the Read of the LP character.
LPR @ RDLNS	CT1L *ITSF	
LPC1F ← 1	CT1L *LPCP	
LPC2F ← 1	LPCP/ *LPC1F	
LPTL ← 1	LPC1F *LPC2F	
LPC1F ← 0 LPC2F ← 0 SA+1 LPR ← 1	LPTL	At LP time (LP stored in the LP register), the control resets LP timing logics, increments the segment address plus 1 to the next segment, and clears LP register for the next LP character.

(Cont)

SC=15 READ (Cont)

OPENF ← 1	ERR *LOADN	The control enables R/D bit to indicate parity error.
DPEF ← 1	DPENF *DUMPN	This logic is used to indicate a Read Parity error.
ERR	LPC1F *LPR≠0	This logic senses LP error (LPR≠0).
SC ← 12 ITSF ← 0	INXF *EXITF/	The control goes to SC 12 for address search of the next segment after Index.
INXF ← 1	INXPSY *MAINT/	This logic flags Index pulse time.
SHIFI(N)	CT1L *WDPTF *LOAD(N)	This logic controls shifting of Read data through the input register and MOS buffer.
CT1F ← 1	FCLP	
CT2F ← 1	CT1F	
CT1F ← 0	FCLP/	
CT2F ← 0	CT1F/	
CT1L	CT1F *CT2F/	
EXITF ← 1	DTMR=TO	EXITF = 1 provides logic to set the Sequence Counter to 0 (SCANY logics).
HTMR ← 0 DTMR ← 0	LPTL	This logic resets Head and Disk timers at end of LP time.
SC ← 11	LPTL *BUFSFLF *TERMF/	The control goes to Slip mode if buffers are full and more data is to be read.
DTMR+1	1024USB	This logic provides disk time-out if an erased (no data) track occurs.

READ AND WRITE FLOATING LOGIC

The following logic is used both for Read and Write operations. This logic provides for data flow between memory and the Disk File Electronics Unit, through the Disk File Control.

BOTH (READ AND WRITE)

CLOCK ENABLE TO SHIFT MOS	CLKENB(N)	SHIFI(N) +JUST(N) +SHIFO(N) +CLRCHANO	This logic enables MOS clocks to shift data through the MOS buffers.
SHIFT IN MOS	SHIFI	LOAD(N) *(STC14+16 * RC *WRITE *XFROTA +STC=15 *CT1L *WDPTF +FINJSTF)	This logic enables data shift into buffers A through D from the processor or DFSU.
JUSTIFY MOS	JUST(N)	LOAD(N+1) *JUSTF	This logic is used during a Read or Write to shift data in the buffer so that the first byte of data is available at the output register (11 shifts required).
	JUSTF ← 1	WDCT90 *TERMF/ *WRITE + READ *LPTL	
	JUSTF ← 0	JUST11	
JUSTIFY CTR	JUSTC+1	LOAD(N+1) *JUSTF *PH(N(1F *PH(N)2F/	
SHIFT OUT MOS	SHIFO(N)	DUMP(N) *(STC15+16)* RC *XFRIN +(SC=14 * CT1L *WDPTF)	This logic enables data shift out of buffers A through D to processor or DFSU.
FIN JUSTIFY	FINJSTF ← 1	TERM *WDCT≠0 *WRITE	This logic enables the move of data to place the first byte of data into the output latches.
PARTIAL BUFF	FINJSTF ← 0	WDCT101	
WORD CTR	WDCT+1	PH(N)1F *PH(N)2F/* (DUMP(N) *READ * STC15+16 +7TIMFF) +LOAD(N) *WRITE *(FINJSTF +STC14+16 +7TIMFF))	The word counter tracks the shift of data through the buffer.

(Cont)

BOTH (READ AND WRITE) (Cont)

	7TIMFF ← 1	RC *STC16	The 7TIMFF set to 1 indicates the last buffer shift time.
	7TIMFF ← 0	7TIMFF	
DUMP CTR	DUMPC+1	LPTL *WRITE +DPOLYF *STC08 *READ	This logic controls which buffer is to be dumped.
DUMP DELAY	DPDLYF ← 1	WDCT90 *READ	This logic delays upcount of the dump counter until 90 words are loaded.

TRANSFERS TO AND FROM THE I/O CONTROL

The Status Count Any (STCANY) logic is floating logic that can occur at any status count. Primarily, this logic enables transfer of information to or from the Disk File Control by means of the Exchange lines.

STCANY

CHAN≠ DURING CA COMPARES	CHANHI	CA *(JPRCHP /EXCH16-19 * TESTER)	This logic sets CHANHI if the command is for this channel.
	SETCMR	CHANHI +CA *EXCH20 * EXCH21/ *EXCH02 *EXCH00	This logic sets SETCMR to enable receipt of command and variant bits into control logic.
	XFROTA ← 1	SETCMR *EXCH21 *EXCH20/ *EXCH22/	This logic sets XFERIN or XFEROTA according to the Exchange lines which represent the current command.
	XFRIN ← 1	SETCMR *EXCH22 *EXCH21/ *EXCH20/	
	CTRLVAR ← 1	SETCMR *EXCH21/ *EXCH20 * EXCH22/	This logic sets CTLVAR on a Test, Test-and-Clear, or Test SR to determine which command is required.
CHAN ACTIVE	CHAL	XFRIN +XFROTA +CTRLVAR	CHAL indicates that the channel is active.
	CMDREG ← 0	RC +CLRCHANO	This logic clears the Command register upon completion of an operation.
	TERM ← 1	CTRLVAR *EXCH01 *EXCH02 * EXCH00/	This logic sets TERMF if Terminate Data command is on Exchange lines.
	TERM ← 1	TERM	

(Cont)

STCANY (Cont)

TSR ← 1	CTRLVAR *EXCH00 *EXCH02 * EXCH01/	This logic sets Test Service Request as designated by Exchange lines.
TSTCLR ← 1	CTRLVAR *EXCH00 EXCH01 * EXCH02/	This logic sets Clear-and-Test-Status as designated by the command on the Exchange lines.
TSTS ← 1	CTRLVAR *EXCH00 *EXCH01/ *EXCH02/	This logic sets Test Status according to the command on the Exchange lines.
VAR REG ← 0	RC +CLRCHANO	This logic clears the variant register, upon Operation Complete.
EXCH0-15 ← CHNLMSK	CHAL *SRF *TSR *TESTER/ *JPRCHP	This logic returns channel indicator in response to a Test Service Request command.
EXCH16-20 ←	CHAL *TSR/	This logic sets status of control on the Exchange lines during Test, or Test Status.
EXCH3-4 ← 1	CHAL *(TSTS +TSTCLR)	This logic returns control ID on Test, or Test-and-Clear.
IOS ← 1	CHAL	This logic enables I/O Send if this channel is active.
CLRCHANO	CLRCTL +CLRB +RC *TSTCLR	This logic clears registers in the control.
EU BUSY	EXILF *FCLPEUB	This logic is used as a flag, indicating that DFEU is busy.
EXITF ← 1	READ *TERMF	This logic sets Exit flip-flop when Read operation is complete.

READ/WRITE/PAUSE AND TEST FLOW

These flows provide a detailed description of the flow depicted in figures 2-2 and 2-4. The letters located to the right of the status count indicate which operations use the logic contained in the associated block. Coding of these letters is as follows: R - Read, W - Write, P - Pause, and T - Test.

STC00 — R/W/P/T

STC+1	

The control will only be at STC00 in a Clear state. It will immediately, upon removal of the clear term, upcount STC to the idle state of STC01.

STC01 FETCH OP CODE — R/W/P/T

OPREG ← EXCH7-3	CHANHI
STC+1	RC *XFROTA

This logic gates the first byte of the Operation code into the Operation register if the operation is for this control.

This logic upcounts STC to STC02.

STC02 DUMMY CYCLE — R/W/P/T

STC+1	RC *XFROTA

This logic provides a dummy transfer-out cycle, as no information is transferred from processor to control for the second byte of the operation code. This logic also upcounts STC to STC03.

STC03 FETCH HUB NUMBER — R/W/P/T

EUREG ← EXCH3-0 EUSF ← 1	CHANHI
EX1LF ← 1	CHANHI * LPCPEUB
STC+1	RC *XFROTA

The third byte of the operation code (hub or DFEU number) is set into the operation register from the exchange lines.

The EX1L flip-flop is set if the DFEU is busy.

STC is upcounted to STC04.

STC04 FETCH FILE ADD (HI) — R/W/P/T

BFAR19-16F ← EXCH3-0 ITSF ← 1	CHANHI
SETEUZO	CA
STC+1	RC *XFROTA

This logic sets the two most-significant digits of file address into the Binary File Address register. Information Track Select is used to blank out spurious Index pulses.

STC is upcounted to STC05.

STC05	FETCH FILE ADD (MID)	R/W/P/T
BFAR15-8F ← EXCH 17-0	CHANHI	This logic sets the middle byte of the file address into the File Address register.
STC+1	RC *XFROTA	STC is upcounted to STC06.
EUBUSYF ← 1	EUBUSY *(READ +WRITE) * CHANHI	This logic sets the EU Busy flip-flop if the designated DFEU is busy.

STC06	FETCH FILE ADD (LOW)	R/W/P/T
BFAR7-OF ← EXCH	CHANHI	This logic sets the two least-significant digits of file address into the Binary File Address register.
SC+1	RC *XFROTA *(READ +WRITE) *(WAIT +EUBUSYF/)*EUPRES	The Sequence Counter is initiated at this time.
EXITF ← 1 EUSF ← 0	EUBUSYF *WAIT/	The Exit flip-flop is set if the DFEU is busy and no "wait" variant is set.
STC+1	RC *XFROTA *(WRITE/ + EUBUSYF *WAIT/+ EUPRES/)	STC is incremented to STC07 if this is a Read, Pause, or Test operation.
STC ← 14	RC *XFROTA *WRITE *(EUBUSYF/ +WAIT) *EUPRES	The control goes to STC14 if this is a Write operation.

STC07	FETCH REF ADD 1	R/P/T
ADDMEM1 ← EXCH7-0	TESTER/ +CHANHI *TESTER	This logic allows the first byte of the reference address to be stored into the Address Memory chips.
WRENBLE ← 1	TESTER/ *CHANHI *DSCP +WETEST	This logic enables Address Memory.
STC+1	RC *XFROTA	STC is upcounted to STC08.
STC ← 21	RC *TERMF *READ	STC is set to 21 if no more Read data is needed.

STC08	FETCH REF ADD 2	R/P/T
ADDMEM2 ← EXCH7-0	TESTER/ +CA *TESTER	This logic allows the second byte of the reference address to be stored into the Address Memory chips.
WRENBLE ← 1	TESTER/ *CHANHI *DSCP +WETEST	This logic enables Address Memory.
STC+1	RC *XFROTA	STC is upcounted to STC09.

STC09	FETCH REF ADD 3	R/P/T
ADDMEM3 ← EXCH7-0	TESTER/ +INXF *TESTER	The third byte of the reference address is stored into the Address Memory chips.
WRENBLE+1	TESTER/ *CHANHI *DSCP +WETEST	This logic enables Address Memory.
STC+1	RC *XFROTA	This logic upcounts STC to STC10.

At this point in the Read flow, the control transfers to STC10 and waits until the sequence counter has enabled the control to decode, access, and read the contents of one buffer of information.

STC10	CALL PROCESSOR	R/P/T
SRF ← 1	EXITF +READ *BUFRDY *TERMF/ +WRITE *BUFLF/ *TERMF/	This logic sets Service Request for a Read OP when the first buffer has been filled and more data must be read.

(Cont)

STC10 (Cont)

STC+1	WRITE *BUFLF/ *TERMF/ *EXITF/ +READ *BUFRDY *TERMF/ *EXITF/	STC is upcounted to STC11, which allows data to be transferred to processor if more data is to be read.
STC ← 18	EXITF	A Pause or Test operator causes an exit to STC18 at this point. The pause is approximately 3 to 4 milliseconds.
EXITF ← 1	PAUSE *DTMR=4 +TEST +INVAL +EUPRES/	This logic sets Exit flip-flop for a Pause, Test, or invalid operator, or if a designated DFEU is not present.
DTMR+1	PAUSE *DTMR≠4 * 1024USB	The Disk timer is counted, to create the Pause operator delay time.

At this point in the flow, the control is beginning to send read data from the disk file to the processor.

STC11 SEND REF ADD1 R

EXCH7-0 ← ADDMEM1	XRIN (TESTER/ +CHANHI * TESTER)	The first byte of the reference address is returned to the processor.
STC+1	RC *XFRIN	STC is upcounted to STC12.
SRF ← 0		The Service Request flip-flop is reset.

STC12 SEND REF ADD 2 R

EXCH7-0 ← ADDMEM2	XFRIN (TESTER/ +CA *TESTER)	The second byte of the reference address is returned to the processor.
STC+1	RC *XFRIN	STC is upcounted to STC13.

STC13 SEND REF ADD 3 R

EXCH7-0 ← ADDMEM3	XFRIN (TESTER/ +INXF *TESTER)	The third byte of the reference address is returned to the processor.
STC+1	RC *XFRIN *WRITE	STC is upcounted to STC14 if this is a Write operator.

(Cont)

STC13 (Cont)

STC+2	RC *XFRIN *READ	STC is set to STC15 if this is a Read operator.
STC15	XFER TO PROCESSOR (READ OP)	R
OUTREGN ← MOSN	PH(N)1F *PH(N) 2F/ * DSCP	Read data is shifted from the MOS buffer to the Output register.
EXCHO-15 ← OUTREGN	DUMP(N) *XFRIN	The control shifts the contents of the Output register to the Exchange lines.
STC+1	RC *XFRIN *WDCT88	STC is upcounted to STC16, allowing the transfer of the last data byte from the buffer.
STC ← 21	RC = TERMF	STC is set to 21 if no more data is needed.
SHIFO(N)	DUMP(N) *RC *XFRIN	MOS clock control logics.
CLKENB(N)	SHIFO(N)	
STC16	LAST XFER TO/FROM PROCESSOR	R
OUTREGN ← MOSN	PH(N)1F *PH(N)2F/ *DSCP	The last data byte is shifted to the Output register.
EXCHO-15 ← OUTREGN	DUMP(N) *XFRIN	The last byte is shifted from the Output register to the Exchange lines.
INREG ← EXCH15-0	CHANHI *CHAL/ *WRITE	Refer to Write flow.
STC ← 07	RC *XFRIN *READ	STC is set to 7 to receive more read data.
STC ← 07	RC *(XFROTA +TERMF) *WRITE	Refer to Write flow.
STC ← 21	RC *READ *TERMF	STC is set to 21 if a terminate condition exists (no more read data required).
SHIFI(N)	RC *XFROTA * LOAD(N)	Refer to Write flow.
MOS ← INREG	TERMF/	(Cont)

STC16 (Cont)

SHIFO(N)	DUMP(N) *RC *XFRIN	MOS buffer clock control.
CLKENB(N)	SHIFI(N) +SHIFO(N) +CLRCHANO	

After the transfer of the last byte of the last buffer load, the control is set to STC21 and starts to transfer the Result descriptor to the processor.

STC21 (SUBSTATE CONT) R/T

EXCHOO ← 21	XFRIN *TEST *RD08	This logic transfers Result descriptor byte 1 to the processor. Refer to STC22, RD09 and 10.
STC+1	RC *XFRIN	STC is upcounted to STC22.

STC22 SEND RD BYTE 2 R/T

EXCH07 ← 1	XFRIN *TEST *RD09	This logic is used to transfer the Result descriptor to the processor. This logic is also used in conjunction with RD02 to indicate disk type, as shown below.
EXCH06 ← 1	XFRIN*TEST *RD10	

Result Descriptor Bits			Disk Type Used
8	9	10	
0	0	0	Unit not present.
0	0	1	System-A Memory.
0	1	0	Reserved.
0	1	1	1C-3.
1	0	0	1C-4.
1	0	1	1A-3.
1	1	0	1A-4.
1	1	1	Reserved.

EXCH05 ← 1	EXT.EXCH *TEST *XFRIN	This logic indicates an external exchange on Test operator only. R/D bit 11 indicates a 2 x 4 exchange on Test operator only (R/D bit 12).
EXCH04 ← 1	2x4EXCH *TEST *XFRIN	
EXCH03 ← 1	CTL2+3 *XFRIN	
EXCH02 ← 1	CTL1+3 *XFRIN	
STC+1	RC *XFRIN	STC is incremented to STC23.

STC23 SEND R/D BYTE 3 R/T

		This logic transfers the third byte of the result descriptor to the processor.
EXCH07 ← 1	XFRIN *((PAUSE +EUBUSYF *WAIT/ +EUPRES/ *WAIT/(/ + TEST)	Bit 16 of the R/D is set to indicate OP complete.
EXCH04 ← 1 EXCH03 ← 1	XFRIN *TEST	This logic is used to indicate a Test OP.
STC ← 01	RC *XFRIN	This logic clears the control and sets STC to STC01.

STC14 is the branch taken at STC6 for a Write operation. The Write operation branches back to the common flow status counts at STC7 and STC21. The common flow status counts have been duplicated for the Write operation to define the action taken during a Write. Refer to figure 2-3.

STC14 FETCH PROCESSOR WORD W

INREG ← EXCHO-15	CHANHI *CHAL/	This logic transfers Write data from the processor to the Input register in the control.
STC+2	RC *XFROTA *WDCT88	STC is incremented by 2, to receive last byte of buffer load. (WDCT88 indicates that the last byte is in the Input register but not yet in the MOS buffer.)
STC ← 07	RC *TERMF	STC is set to 7 if there is no more Write data for the control.
STC+2	RC *XFROTA *(WLOF +SURF/)	STC is incremented by 2 if lockout or DFSU not-ready conditions exist.
SHIFI(N)	LOAD(N) *RC *XFROTA	This logic is used to control shift and input of data to the control.
CLKENB(N)	SHIFI(N)	

STC16 LAST XFER TO/FROM PROCESSOR

OUTREGN ← MOSN	PH(N)1F *PH (N)2F/ *DSCP	(Cont)

STC16 (Cont)

EXCHO-15←OUT REGN	DUMP(N) *XFRIN	Refer to Read flow.
INREG←EXCH15-0	CHANHI *CHAL/ *WRITE	This logic is used to load the last data byte for this buffer load into the Input register.

STC←07	RC *XFRIN *READ	Refer to Read flow.
STC←07	RC *(XFROTA +TERMF) *WRITE	This logic is used to receive the reference address from the processor.
STC←21	RC *READ *TERMF	Refer to Read flow.
SHIFI(N)	RC *XFROTA * LOAD(N)	This logic is used as control logic for load, dump, and shift of data in buffers A through D.
SHIFO(N)	DUMP(N) *RC *XFRIN	
CLKENB(N)	SHIFI(N) +SHIFO(N) + CLRCHANO	

STC07	FETCH REF ADD 1	W
ADDMEM1←EXCH7-0	TESTER/+CHANHI *TESTER	The control sets the first byte of the reference address into Address Memory.
WRENBLE←1	TESTER/ *CHANHI *DSCP +WETEST	
STC+1	RC *XFROTA	STC is incremented to STC08.
STC←21	RC *TERMF *READ	Refer to Read flow.

STC08	FETCH REF ADD 2	W
ADDMEM2← EXCH7-0	TESTER/ +CA * TESTER	The control sets the second byte of reference address into Address Memory.

(Cont)

STC08 (Cont)

WRENBLE ← 1	TESTER/ *CHANHI *DSCP	This logic provides Write-enable control logic for Address Memory.
STC+1	RC *XFROTA	STC is incremented to STC09.

STC09	FETCH REF ADD 3	W
ADDMEM3 ← EXCH7-0	TESTER/ *INXF * TESTER	The control sets the third byte of the reference address into Address Memory.
WRENBLE ← 1	TESTER/*CHANHI *DSCP +WETEST	This logic enables a Write of Address Memory.
STC+1	RC *XFROTA	STC is incremented to STC10.

STC10	CALL PROCESSOR	W
SRF ← 1	EXITF *READ *BUFRDY *TERMF/	This logic sets Service Request during a Write when more data is required.
STC+1	WRITE *BUFLF/ *TERMF/ * EXITF/ +READ *BUFRDY *TERMF/ *EXITF/	STC is incremented to STC11 during a Write, to accept more write data from the processor.
STC ← 18	EXITF	The control exits to STC18 when the operation is complete and returns the reference address and Result descriptor to the processor.
EXITF ← 1	PAUSE *DTMR=4 +TEST + INVAL + EUPRES/	Refer to Read/Pause/Test flow.
DTMR+1	PAUSE *UTMR≠4 1024USB	Refer to Read/Pause/Test flow.

The control is set to STC11 if more data is required to be written, or to STC18 if no more data is to be written.

STC11	SEND REF ADD 1	W
EXCH7-0 ← ADDMEM1	XFRIN (TESTER/ +CHANHI *TESTER)	The control sets the first byte of the reference address into the Exchange lines to the processor.
STC+1 SRF ← 0	RC *XFRIN	STC is incremented to STC12. The Service Request flip-flop is reset.

STC12	SEND REF ADD 2	W
EXCH7-0 ← ADDMEM2	XFRIN (TESTER/ +CA * TESTER)	The control sets the second byte of the reference address into the Exchange lines and to the processor.
STC+1	RC *XFRIN	STC is incremented to STC13.

STC13	SEND REF ADD #	W
EXCH7-0 ← ADDMEM3	XFRIN (TESTER/ +INXF *TESTER)	The control sends the third byte of the reference address to the processor.
STC+1	RC *XFRIN *WRITE	STC is incremented to STC14.
STC+2	RC *XFRIN *READ	Refer to Read flows.

The control exits from STC13 to STC14 if there is more data to be written.

STC18	SEND REF ADD BYTE L (LAST)	W
EXCH7-0 ← ADDMEM1	XFRIN (TESTER/ +CHANHI *TESTER)	The control returns byte 1 of the reference address to the processor.
SRF ← 0 STC+1	RC *XFRIN	The Service Request flip-flop is reset and STC is incremented to STC19.

STC19	SEND REF ADD BYTE 2 (LAST)	W
EXCH7-0 ← ADDMEM2	XFRIN (TESTER/ +CA * TESTER)	The control returns byte 2 of the reference address to the processor.
STC+1	RC *XFRIN	STC is incremented to STC20.

STC20	SEND REF ADD BYTE 3 (LAST)	W
EXCH07- ←ADDMEM3	SFRIN (TESTER/ +INXF *TESTER)	The control returns byte 3 of the reference address to the processor.
STC+1	RC *XFRIN	STC is incremented to STC21.

STC21	SEND RD BYTE1	W
EXCH07 ← 1	XFRIN	The control sends the first Result descriptor byte to processor. Exchange line 7 is the Operation Complete bit.
EXCH06 ← 1	EXCPBIT *XFRIN	This logic provides the exception bit.
EXCPBIT	(DPEF +DTMR=TO +WLOF +SURF/ +EUPRES/ *WAIT) * (READ +WRITE) *XFRIN	This logic is used to determine if an exception condition existed.
EXCH05 ← 1	XFRIN *(READ +WRITE) * SURF/ +EUPRES/ *WAIT +DTMR=TO	This logic provides Not-Ready-DFSU or not-present-DFEU exception condition.
EXCH04 ← 1	XFRIN *DFEF	This logic provides a Read parity exception condition.
EXCH01 ← 1	XFRIN *WLOF	This logic provides a Write lock-out exception condition.
EXCH00 ← 1	XFRIN *TEST *RD08	This logic provides the first bit of DFSU type for a Test operator.
STC+1	RC *XFRIN	STC is incremented to STC22.

STC22	SEND RD BYTE 2	W
EXCH07 ← 1	XFRIN *TEST *RD09	The control sends the second byte of the Result descriptor to the processor. This logic provides the second and third bit of DFSU type for a Test operator.
EXCH06 ← 1	XFRIN *TEST *RD10	

(Cont)

STC22 (Cont)

EXCH05 ← 1	EXT.EXCH *TEST *XFRIN	This logic indicates that an external exchange exists during a Test operator.
EXCH04 ← 1	2x4EXCH *TEST *XFRIN	This logic indicates a 2 x 4 exchange exists during a Test operator.
EXCH03 ← 1	CTL2+3 *XFRIN	This logic indicates the control number.
EXCH02 ← 1	CTL1+3 *XFRIN	
STC+1	RC * XFRIN	STC is incremented to STC23.

STC23	SEND RD BYTE 3	W
EXCH07 ← 1	XFRIN *((PAUSE +EUBYSYF* WAIT/ +EUPRES/ *WAIT/(/+ TEST)	The control sends the third byte of the Result descriptor to the processor. The second Operation Complete bit is suppressed for a Pause OP, or a Read OP/Write OP if the DFSU is busy.
EXCH04 ← 1	XFRIN *TEST	This logic indicates that the DFSU is not present and no wait is required.
EXCH03 ← 1		This logic indicates the control ID for a Test operator.
STC ← 01	RC *XFRIN	STC is set to STC01.

BFAR DETAIL

Since the B 1700 Disk File Control can be used to access several types of head-per-track Disk File Units, a means of decoding the field address must be provided. Decoding is accomplished by the use of a parameter generator that provides binary equivalents of the segment addresses. The number of segments varies between disk file types as to face, zone, and Disk File Storage Unit. During Sequence Counts 2 through 7 these parameters are subtracted (repeatedly) from the Binary File Address Register (BFAR) until an underflow condition occurs. The terms COHI and COHIL are used to indicate that the parameter subtracted from BFAR is larger than BFAR. An attempt to do a subtraction under these conditions will result in an underflow condition. The underflow condition is flagged by COHI set to true. Since COHI is only true for a short time, COHIL is set true to indicate that COHI was set true during the previous subtraction. Refer to figures 2-6 through 2-8.

Since the underflow condition can result from the least-significant bit contained in BFAR, 3 clock periods are provided to sample for this condition before completing the subtraction. To prevent the subtraction that would result in an underflow, terms SSF and SS2F are used to control the clock to BFAR. If COHI occurs during a subtraction, the result of the subtraction will not be latched into BFAR, and BFAR will contain the bit configuration established prior to the attempted subtraction. The control then steps to the next sequence count to decode the next division of the file address.

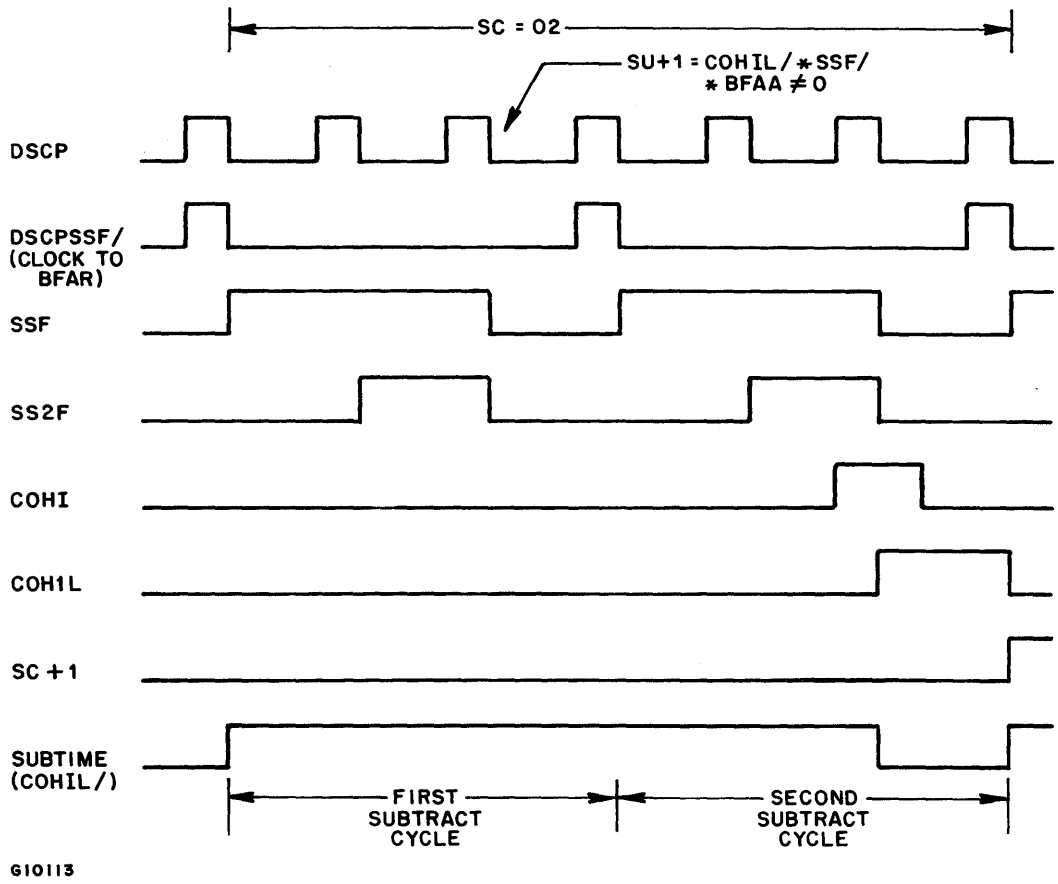


Figure 2-6. Timing Diagram of Sequence Count 2

In the following example, assume that three modules of IC-3 type DFSU's are attached to DFEU number 0 and the field address required is 115260. Refer to figures 2-1 through 2-4 and to the Disk File Control flows.

At SC 1, BFAR is checked to ascertain if it is equal to 0. If BFAR is equal to 0, the Sequence Counter is set to 11 to bypass decoding. If the maintenance segment option is set, the address lines are forced to the maintenance segment address, which consists of hundreds (1011), tens (1011), and units (1011). If the maintenance segment option is not set, an access of segment 0 is initiated.

If the maintenance segment option is not set and the address is not equal to 0, the control upcounts the Sequence Counter to 2 and initiates the decoding sequence.

At SC 2 the control subtracts the first parameter from BFAR to determine which DFSU contains the file address. The first parameter (parameter 01) denotes the number of segments per DFSU. Since the file address in the example is located in the second DFSU (module 1), two subtractions of the first parameter are required to cause an underflow condition. The first subtraction from BFAR does not leave BFAR equal to 0 and does not cause an underflow. As a result, the DFSU value is incremented by 1. During the second subtraction, COHIL comes true, indicating that the parameter is larger than the contents remaining in BFAR. This action result(s) in the prior contents of BFAR remaining in BFAR; the selected DFSU is unit number 1.

SC 01
BFAR = 115260 — BFAR ≠ 0 → SC + 1

SC 02 (Find DFSU) First Subtraction	BFAR ..... 115260 PRM 01.... -111200 BFAR 4060	DFSU Counter .. 00 COHIL/.... +1 01	First subtraction did not cause COHIL. SU is upcounted by 1 and the second subtraction is initiated.
Second Subtraction	BFAR ..... 4060 PRM 01..... -111200 BFAR 4060	DFSU Counter.. 01 COHIL.... +00 01	Second subtraction caused COHIL. The DFSU counter is not upcounted. BFAR remains at 4060, and SC is upcounted by 1.
	COHIL * BFAR ≠ 0 = SC+1		
SC 03 (Find FACE) First Subtraction	BFAR ..... 4060 PRM 02 .. -13900 BFAR 4060	FACE .... 00 COHIL.... +00 00	First subtraction caused COHIL. FACE is not upcounted, but SC is upcounted by 1.
	COHIL * BFAR ≠ 0 = SC+1		
SC 04 (Find TRACK tens digit) First Subtraction	BFAR..... 4060 PRM 03.... -2780 BFAR 1280	TRACK Tens .... 00 COHIL/... +1 01	First subtraction did not cause COHIL. TT is upcounted by 1 and second subtraction is initiated.
Second Subtraction	BFAR ..... 1280 PRM 03.... -2780 BFAR 1280	TT ..... 01 COHIL.... +00 01	Second subtraction caused COHIL. TT is not upcounted but SC is upcounted by 1.
	COHIL * BFAR ≠ 0 = SC+1		
SC 05 (Find TRACK units digit) First Subtraction	BFAR ..... 1280 PRM 04.... -278 BFAR..... 1002	TRACK Units ... 00 COHIL/... +1 01	First subtraction did not cause COHIL. TU is upcounted by 1 and second subtraction is initiated.
Second Subtraction	BFAR ..... 1002 PRM 04.... -278 BFAR 724	TU ..... 01 COHIL/... +1 02	Second subtraction did not cause COHIL. TU is upcounted by 1 and third subtraction is initiated.

Figure 2-7. Address Decoding, SC 01 Through SC 11 (Sheet 1 of 2)

SC 05

Third Subtraction	BFAR..... 724 PRM 04 ..... -278 BFAR 446	TU ..... 02 COHIL/ .. +1 03	Third subtraction did not cause COHIL. TU is upcounted by 1 and the fourth subtraction is initiated.
Fourth Subtraction	BFAR ..... 446 PRM 04 ..... -278 BFAR 168	TU 03 COHIL/ +1 04	Fourth subtraction did not cause COHIL. TU is upcounted by 1 and the fifth subtraction is initiated.
Fifth Subtraction	BFAR ..... 168 PRM 04 ..... -278 BFAR 168	TU 04 COHIL +00 04	Fifth subtraction caused COHIL. TU is not upcounted but SC is upcounted by 1.

COHIL * BFAR ≠ 0 = SC+1

SC 06 (Determine if address is in Zone 0)

BFAR ..... 168 PRM 05 ..... -73 BFAR 95	Zone ≠ 0 ZN+1 SC+1	Since this subtraction did not cause COHIL, the address is not in zone 0. ZN and SC are both upcounted by 1.

COHIL/ * BFAR ≠ 0 = ZN+1 * SC+1

SC 07 (Determine if address is in Zone 1)

First Subtraction	BFAR ..... 95 PRM 06 ..... -95 BFAR 00	ZN..... 01 COHIL/.. +1 02	First subtraction did not cause COHIL. ZN is upcounted by 1 and the second subtraction is initiated.
Second Subtraction	BFAR ..... 00 PRM 06 ..... -95 BFAR 00	ZN..... 02 COHIL... +00 02	Second subtraction caused COHIL. ZN is not upcounted but SC is upcounted by 1.

SC 08	Segment Address hundreds digit is converted from binary to hexadecimal. Since BFAR = 0, SC is set to 11 (no more decoding is necessary.
SC 09	Segment Address tens digit is converted from binary to hexadecimal. Since BFAR = 0 at SC 08, this decoding step is bypassed.
SC 10	Segment Address units digit is converted from binary to hexadecimal. Since BFAR = 0 at SC 08, this decoding step is bypassed.
SC 11	Address decoding complete.

Figure 2-7. Address Decoding, SC 01 Through SC 11 (Sheet 2 of 2)

PRM 01 (DFSU)	1C3 - 111,200 1C4 - 111,200 1A3 - 45,200 1A4 - 80,000 SM - 16,384
PRM 02 (FACE)	1C3 - 13,900 1C4 - 13,900 1A3 - 5,650 1A4 - 10,000 SM - 2,750
PRM 03 (TRACK TENS)	1C3 - 2,780 1C4 - 2,780 1A3 - 1,130 1A4 - 2,000 SM - 550
PRM 04 (TRACK UNITS)	1C3 - 278 1C4 - 278 1A3 - 113 1A4 - 200 SM - 55
PRM 05 (ZONE 0)	1C3 - 73 1C4 - 79 1A3 - 27 1A4 - 50 SM - 64
PRM 06 (ZONE 1)	1C3 - 95 1C4 - 89 1A3 - 36 1A4 - 64 SM - 64

Figure 2-8. Disk File Parameters

Since there is a remainder in BFAR, the control upcounts the Sequence Counter to SC 3 to determine the disk file face. The control steps from SC 3 through SC 7 to determine disk file face, track tens digit, track units digit and zone. Repetitive subtractions occur in each sequence count until COHIL comes true, indicating an underflow condition. Prior to stepping to the next sequence count, a check is made to determine if BFAR is equal to 0. If at the completion of any subtraction cycle, BFAR is equal to 0, no further decoding is required and the Sequence Counter will be set to 11.

At Sequence Count 8 the binary file address is converted to a digital file address by successively subtracting 100 from BFAR and storing the number of successful subtractions. This process provides the digital hundreds bit of the file address. In the same manner as described above, the tens bit is determined by successively subtracting 10 from BFAR during SC 9. At SC 10, the units digit is determined by successively subtracting 1 from BFAR, until BFAR equals 0.

When the control enters SC 11, the entire file address has been decoded. At SC 11, the control starts an address search for the decoded file address.

SLIP DETAIL

The Slip mode allows the interruption of a Write or Read operation to provide time for the processor to fill or empty a buffer so that the operation may continue. Refer to figures 2-9 through 2-11.

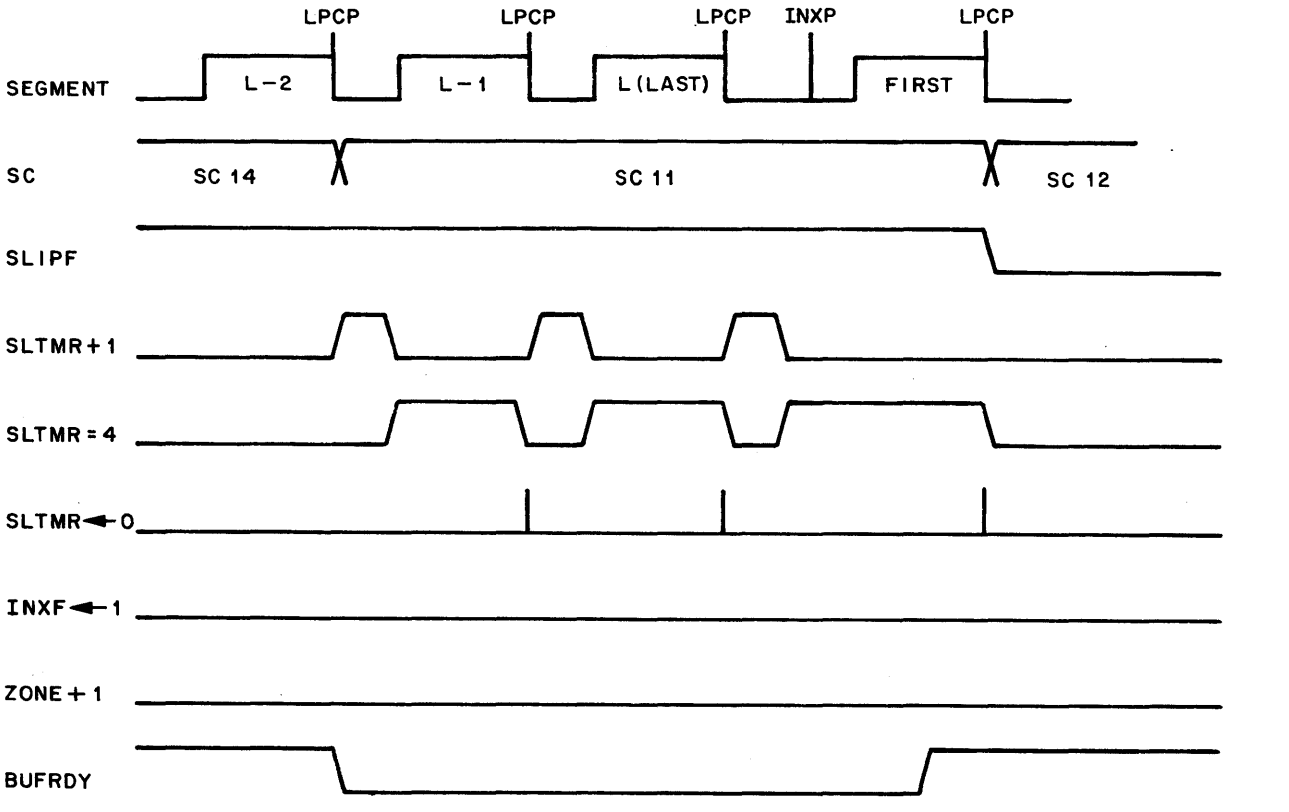
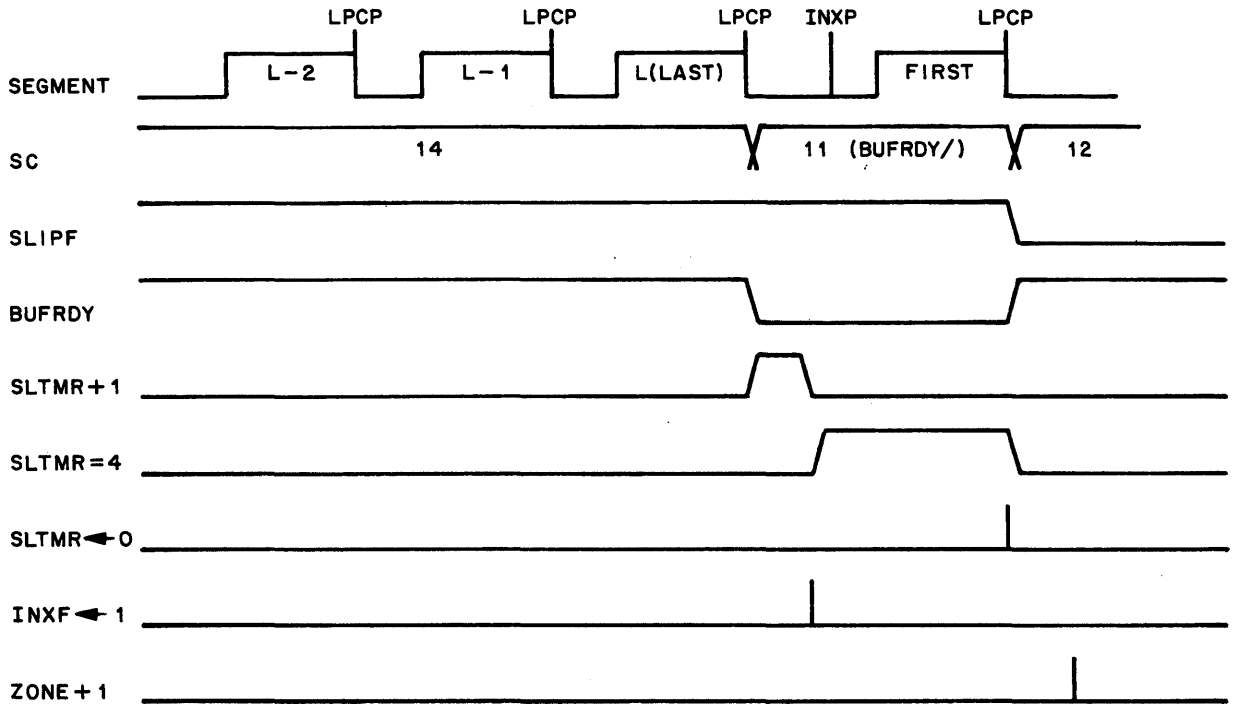


Figure 2-9. Slip Timer with BUFRDY/ Prior to the Last Segment of the Track/Zone



Note: The control changes to Zone+1, to continue the write operation.

Figure 2-10. Slip Timer with BUFRDY/ After Write of the Last Segment on Track

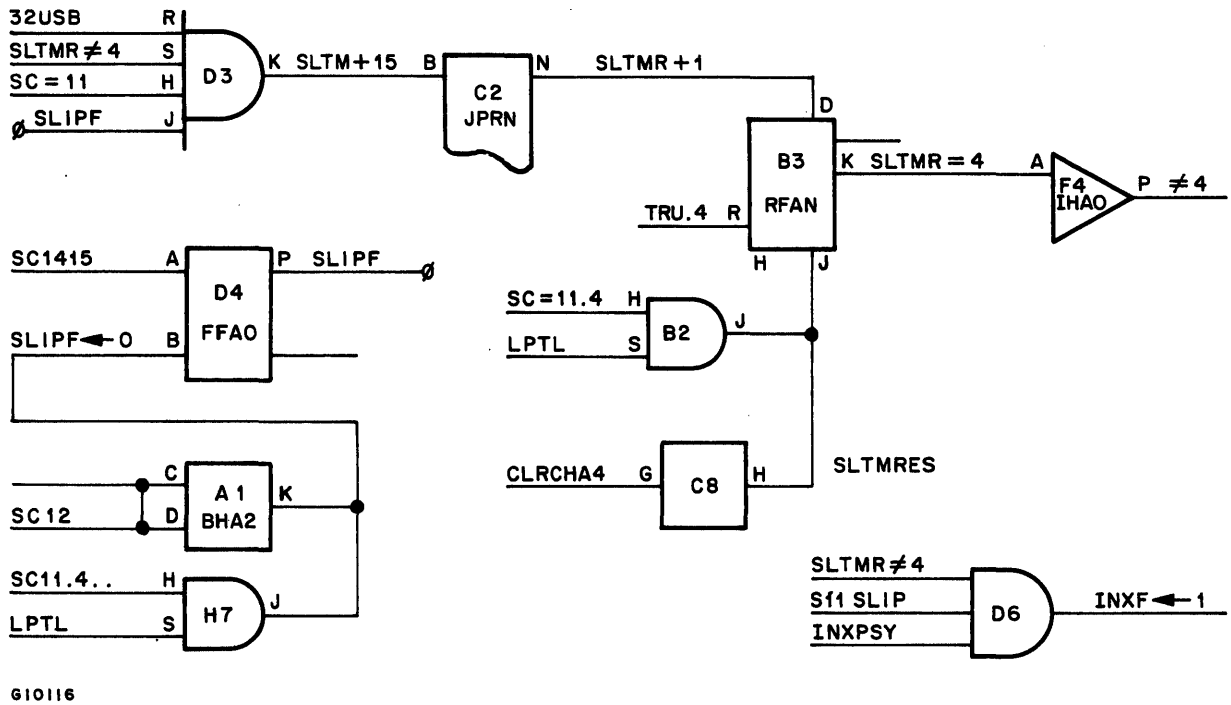


Figure 2-11. Slip Timer Count-up Logic

For example, assume the control is in SC 14 during a Write operation, and that all buffers have been written, causing BUFSEMP to go true. SLIPF was set to 1 upon entering SC 14 and now the control goes to SC 11 (SC← 11 = LPTLDLY *BUFSEMP). Also assume that the Write operation which caused the control to go into Slip mode addressed a segment other than the last segment of the track. As long as the control is in SC 11, and SLIPF = 1, the Slip timer will count to 4 (approximately 128 microseconds) through gate 03 (figure 2-10) and will then be cleared to 0 by LPTL (gate B2). When the last segment of the track goes past the head, the Slip timer will be set to 0 by LPTL of this last segment and again count to 4 before INXP time. With SLTMR= 4, INXF is not set at SC 11 time. (The term INXF causes the upcounting of the zone during SC 12.) In this manner the Slip timer prevents the upcounting of the zone to ensure that the Write operation will continue in the same zone and track in which it was interrupted.

If the control goes into Slip mode after the last segment of a track has been written, the 128 microseconds provided by the Slip timer will not occur prior to INXP, thereby allowing INXF to be set at SC 11 time. When the buffer becomes ready and the control begins to resume the Write operation, writing will continue in the same track but in the next zone.

The logic is the same for a Read operation except that the buffers are full and must be emptied before the Read operation can continue.

DISK TIMER FOR HEAD-SETTLING TIME (TSDL)

At SC=12 a delay of approximately 200 microseconds is provided by the Head timer to allow a period of head-select line settling time (TSDL). Refer to figures 2-12 and 2-13. For this purpose, the Disk timer is upcounted through gate D5 at every 32 USB..0. When DTMR=7 comes true (approximately 200 microseconds) FF G7 is set to indicate the completion of this delay period. During this delay the control steps to SC 13 and waits to begin the segment address search. When HTMR=7 comes true, the segment address search will begin

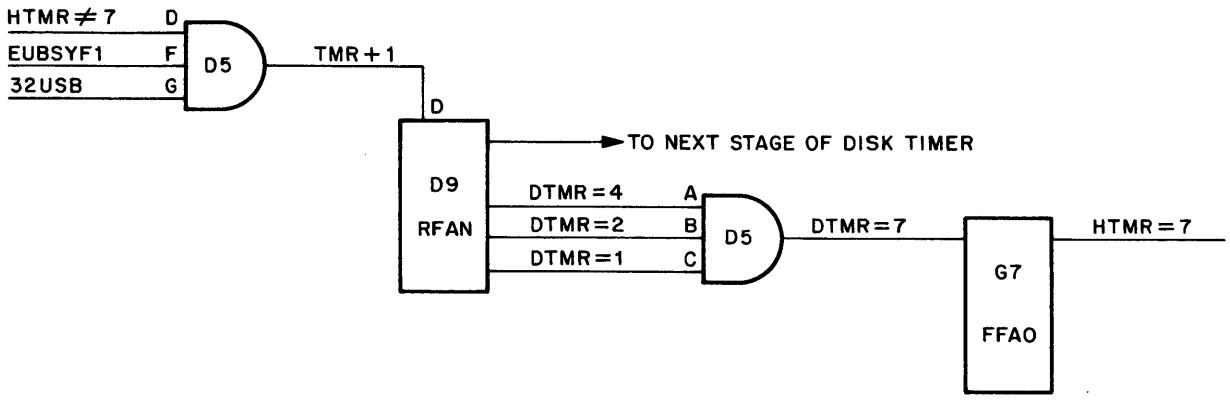


Figure 2-12. Disk Timer Logic

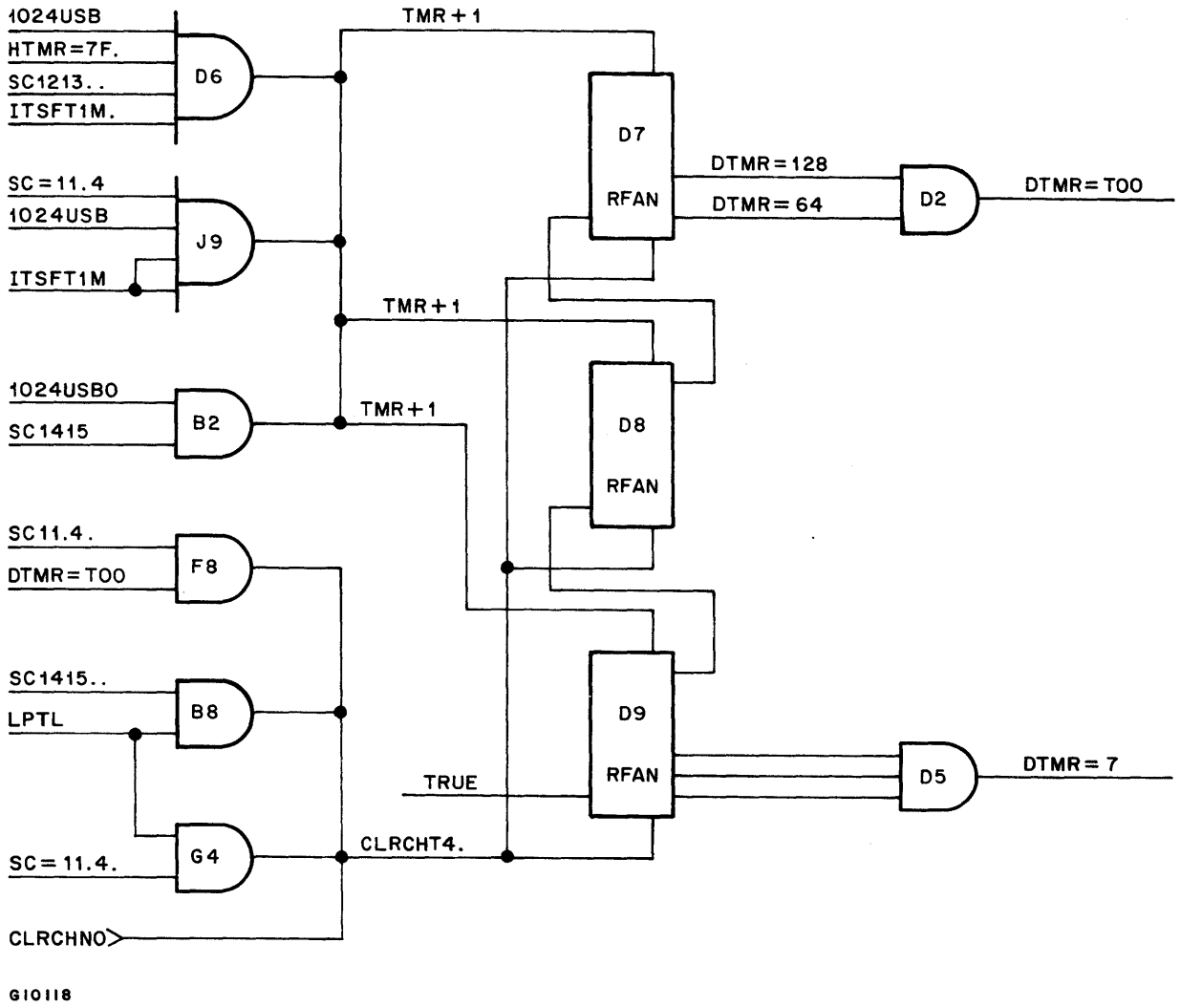


Figure 2-13. Disk Timer Detail

During SC 11 the Disk timer, upcounted through gate J9 every 1024 microseconds, is used only to step the control to SC 12 if no FCLP's are received from the DFEU. The Disk timer provides a pause of up to approximately 200 milliseconds to ensure at least one revolution to receive FCLP's and LPCP's from the disk. No action is taken during SC 11 to exit the flow and report a time out, since logic in the STCANY block of the flows prevents EXITF from being set during SC 11.

During SC 12 and SC 13 the Disk timer is upcounted by 1 every 1024 microseconds by gate D6 as follows: After the Head timer times out (HTMR=7F) at SC 12, the control waits for SACF before upcounting to SC 13. If no SACP is received from the disk before DTMR=TO (approximately 192 milliseconds), the control will exit the flow (EXITF 1) = (DTMR = TO* SC=11/) and report the timeout in the Result descriptor. If the control takes its normal step to SC 13 the Disk timer will continue to be counted until the segment address is found. The 200 milliseconds required to get DTMR=TO is sufficient time to allow a full revolution for address comparison. This comparison takes

place during SC 13, although some of this time is used in SC 12 to count the HTMR to 7 and also check for SACP's. (Normally the SACP will occur within one segment time after HTMR=7F goes true.) If, however, the segment address is not found within this time, the control will exit the flow, by means of the STCANY logic, and report the timeout. (This is the point at which the control will exit if no FCLP's or LPCP's are received from the disk, as stated above under SC 11.)

During SC 14 (Write) or SC 15 (Read), the Disk timer is upcounted, (through gate B2), every 1024 microseconds. If the control fails to complete the Write or Read operation prior to DTMR=TO coming true, the control will exit the flow and report a timeout condition in the Result descriptor. Loss of either FCLP or LPCP can cause this to happen. During SC 14 and SC 15 the Disk and Head timers are reset to 0 at the completion of a segment operation (DTMR ← 0 * HTMR ← 0 = LPTL) and a new count is started for each segment operation.

If the DFSU finds an open data Read head or dc-erased data track, the control completes a Write operation correctly, but does not report the condition. This type of error will be identified as a Read parity error when the open Read head is accessed on a Read operation. No error will occur if the track was dc-erased prior to the Write.

In review, the Disk timer is counted during SC 11 to ensure at least one revolution to receive an LPCP from the disk. The timer is reset to 0 upon going to SC 12. During SC 12 the timer is restarted, allowing approximately 200 milliseconds to complete the DFEU/DFSU status check in SC 12, the head-settling time in SC 12 and SC 13, the disk address search in SC 13, and the Write or Read of one segment in SC 14 or SC 15. The timer is allowed to count up during the Read or Write of each segment thereafter (SC 14 and SC 15) and is reset at the completion of each segment access.

SECTION 3

CIRCUIT DETAIL

GENERAL

A detailed description of the logic circuitry used in the B 1700 Disk File Control I or II is contained in the B 1700 Hardware Rules book. This book is issued as part of the Field Test and Reference documentation.

SECTION 4

ADJUSTMENTS

GENERAL

There are no adjustments required for either the Disk File Control I or the Disk File Control II. Refer to Field Test and Reference documentation and to section 5 of this manual for information concerning the control channel number and subsystem configuration.

SECTION 5

MAINTENANCE PROCEDURES

INTRODUCTION

The purpose of this section is to provide information on maintaining B 1700 Disk File Controls I and II. These controls are used in conjunction with 1A-type Disk File Subsystems, 1C-type Disk File Subsystems or a Systems Memory Subsystem.

PREVENTIVE MAINTENANCE

There is no preventive maintenance required for B 1700 Disk File Controls I and II.

SPECIAL MAINTENANCE TOOLS REQUIRED

The following tools and test routines are required to maintain a B 1700 Disk File Control I or II:

a. I/O Debug Test Routine (I/O Debug).

b. Disk File Control Diagnostic Routine (DISK FILE).

c. B 1700 Field Card Tester.

d. Tektronix type-453A oscilloscope or equivalent.

e. Triplett type-630 VOM or equivalent.

MAINTENANCE CONCEPT

The B 1700 I/O controls are soft controls and do not contain any off-line testing capabilities. The B 1700 I/O maintenance concept is structured around the use of diagnostic test routines used in conjunction with the B 1700 Field Card Tester. Hardware interface test points are also provided.

DISK FILE DIAGNOSTIC ROUTINE

Instructions for the use of the Disk File Diagnostic Routine are provided as part of the Field Test and Reference (FT&R) documentation. The routine consists of the seven sections (0 through 6) listed below.

SECTION 0

Writes and reads maintenance segments only. The Write must be keyed with a segment address. The Read checks the read data against the write data. After the Write/Read pass is completed, a check is made for overwrite.

SECTION 1

Performs a Write/Read of partial segments.

SECTION 2

Performs a Write/Read of multiple segments.

SECTION 3

Performs an interlaced Write/Read of two to nine interfaces and two to nine segments for each Write/Read.

SECTION 4

Dumps the contents of the specified disk file segments to the line printer.

SECTION 5

Allows Write only or Read only of a specified number of segments.

SECTION 6

Allows the entry of 1 to 26 segment addresses by means of the console printer. The program writes 10 segments of the tracks pointed to by addresses having a hexadecimal "F0" pattern. Upon completion of the Write, the program reads the first address and waits until a not-ready condition is sensed on the unit. The program then steps up to the next address and performs a Read. This sequence allows the Field Engineer to adjust the read, bit, and address preamplifiers in the DFSU by means of a switch that causes a temporary not-ready condition on the DFSU.

I/O DEBUG TEST ROUTINE

The I/O Debug Test Routine is a general-purpose troubleshooting test routine written in Micro-Implementation Language (MIL). The operation (OP) code and the control identification (ID) for the applicable peripheral device must be inserted into the appropriate registers. Specific information concerning the operation of this test routine is contained in the I/O Debug program listing issued as part of the B 1700 Field Test and Reference documentation.

The I/O Debug Routine contains no-op instructions between subroutines and also within certain routines. These no-op instructions can be replaced by Halt operators that stop the program at predetermined sections. The Field Engineer also has the option of single-stepping the routine as a troubleshooting procedure.

I/O DEBUG TROUBLESHOOTING PROCEDURE

The following procedure is used to troubleshoot failures that occur in the B 1700 Disk File Controls I and II.

a. Load the I/O Debug Routine tape cassette into the console cassette reader. Press the CLEAR pushbutton, then the START pushbutton. After the program is read in, the program will Halt with a hexadecimal 000001 displayed in the LR register (Halt 1).

b. Load the Device ID number into the X register. The Device ID number for a B 1700 Disk File Control I or II is a hexadecimal 000018.

c. Load the binary (24-bit) operation code and variants into the T register. Applicable operation codes and their variants are listed in section 1 of this manual.

d. Load the desired program toggles into the L register. (This must be done only at Halt 1 time.) The program toggles are arranged from left to right on the console panel. Program toggle 0 is assigned to the left-most position. Applicable program toggles and their basic functions are listed in the I/O Debug program listing supplied as part of the Field Test and Reference documentation.

e. Load the data field length into the FL register. Refer to the I/O Debug program listing for applicable data-field-length coding.

f. Load the File Address into the Y register. Refer to the I/O Debug program listing for bit significance.

g. Press the START pushbutton after the registers are loaded, to initiate the program. When the program halts, check the Result descriptor contained in the T register. The 24 Result descriptor bits and their functions are described in section 1 of this manual.

STEPPING PROCEDURES

Two means of stepping are provided.

a. If the PROGRAM TOGGLE STEP is selected, the processor is kept in the RUN mode and START button is pressed. The processor halts, with the data sent to the exchange lines in one register and the data read into another register. This halt occurs for every transfer to the I/O.

b. The other means of stepping is obtained by placing the MODE switch to position STEP. There are certain levels in the disk control that are true for CA time only. By using this stepping procedure and the program listing, the Field Engineer can step the control to the proper sequence and observe hardware test points.

USE OF HALTS

The I/O Debug routine contains a number of NO-OPs that can be changed to halts. These operators are placed at subroutine levels to enable the Field Engineer to halt the system after certain functions such as transfer out OP code.

TRACE OPTION

This program toggle traces the disk operation on the line printer. The trace shows the state of the 24 exchange lines, in hexadecimal. For each I/O operation, the program listing gives three sets of states: CA time, RC time, and the third is a status indicator which does not reflect Exchange lines. The status indicators display the state to which the control went following the RC time.

FILE ADDRESS

The parameters used by the Disk File Control to decode the file address are listed in section 2 of this manual.

FRONTPLANE CONNECTORS

The frontplane connections for the Disk File Control I and II are listed in tables 5-1 through 5-5.

Table 5-1. Card 1 Frontplane Connectors $X and #X

Pin	Logic	Pin	Logic	Pin	Logic
A	EXCH00.1	I	EXCH08.1	R	EXCH16.1
B	EXCH01.1	J	EXCH09.1	S	EXCH17.1
C	EXCH02.1	K	EXCH10.1	T	EXCH18.1
D	EXCH03.1	L	EXCH11.1	U	EXCH19.1
E	EXCH04.1	M	EXCH12.1	V	EXCH20.1
F	EXCH05.1	N	EXCH13.1	W	EXCH21.1
G	EXCH06.1	P	EXCH14.1	X	EXCH22.1
H	EXCH07.1	Q	EXCH15.1	Y	EXCH23.1
				Z	

$X is the interface between the distribution card and card 1.

#X is the interface between card 1 and the next Disk File Control card 1 backplane.

Table 5-2. Card 1 Frontplane Connectors $Y and #Y

Pin	Logic	Pin	Logic
A	RC....R1	I	1US...R1
B	CA....R1	J	4US...R1
C	CLRB..R1	K	32US..R1
D	SR....R1	L	1024USR1
E	PWRON..1	M	
F		N	
G		P	
H	8MHZ..R1	Q	

$Y is the interface between the distribution card and card 1.

#Y is the interface between card 1 and the next Disk File Control card 1 backplane.

Table 5-3. Card 2 Frontplane Connectors $X, #X, $Y, and #Y

$X					
Pin	Logic	Pin	Logic	Pin	Logic
A	DUMPA..0	I	BUFSFLF1	R	CLKENB.0
B	DUMPB..0	J	BUFSEMPO	S	CLKENC.0
C	DUMPC..0	K	WDCT=0.1	T	CLKEND.0
D	DUMPD..0	L	WDCT88.1	U	WDPTF..0
E	LOAD...0	M	WDCT90.1	V	LPTL...0
F	LOAD...0	N	WDCT1011	W	CHANHI.0
G	LOAD...0	P	CLRCHANO	X	DTMR=T00
H	LOAD...0	Q	CLKENA.0	Y	SURF/..1
				Z	COHIL/21

#X					
Pin	Logic	Pin	Logic	Pin	Logic
A	STC01F.1	I	SC4F...0	R	TERMF.21
B	STC02F.1	J	SC8F...0	S	PAUSE..0
C	STC04F.1	K	EXITF..1	T	INVAL..1
D	STC08F.1	L	XFRIN..1	U	TEST...0
E	STC16F.1	M	XFROTA.1	V	WRITE..0
F		N	CHAL...0	W	READ.2.1
G	SC1F...0	P	TSR....1	X	MAINT..0
H	SC2F...0	Q	TST+TCR1	Y	WAIT...0
				Z	SR.....0

$Y					
Pin	Logic	Pin	Logic	Pin	Logic
A	OPR3...1	I	CMDR2F.1	R	
B	OPR2...1	J	CMDR4F.1	S	
C	OPR1...1	K	CLRWDC.1	T	
D	CNLVR4F1	L	CNT+1..1	U	
E	CNLVR2F1	M	JUSTC+11	V	
F	CNLVR1F1	N	JUSTF 11	W	
G	3BUFULL1	P		X	
H	CMDR1F.1	Q		Y	
				Z	

#Y: Not Used

Table 5-4. Card 3 Frontplane Connectors $X, #X, $Y, and #Y

Pin	Logic	Pin	Logic	Pin	Logic
A	DF1F...1	I	TU4F...1	R	LPCP...0
B	DF2F...1	J	TU8F...1	S	INXP...0
C	DF4F...1	K	TT1F...1	T	FCLP...0
D	SU1F...1	L	TT2F...1	U	
E	SU2F...1	M	TT4F...1	V	
F	SU4F...1	N	WMLL...0	W	
G	TU1F...1	P	SURL...0	X	
H	TU2F...1	Q	SACP...0	Y	
				Z	

The X connector provides the interface between two Disk File Controls if the system configuration contains a 2x4 exchange. Otherwise (for a 1x2 or 4x16 exchange) the connector provides only test points.

Pin	Logic	Pin	Logic	Pin	Logic
A	DF1F.2.1	I	TU4F.2.1	R	LPCP.2.1
B	DF2F.2.1	J	TU8F.2.1	S	INXP.2.1
C	DF4F.2.1	K	TT1F.2.1	T	FCLP.2.1
D	SU1F.2.1	L	TT2F.2.1	U	
E	SU2F.2.1	M	TT4F.2.1	V	
F	SU4F.2.1	N	WMLL.2.1	W	
G	TU1F.2.1	P	SURL.2.1	X	
H	TU2F.2.1	Q	SACP.2.1	Y	
				Z	

#X is the interface between two Disk File Controls for a 2x4 Exchange.

Pin	Logic	Pin	Logic	Pin	Logic
A	FCLP.B.1	I	T02L.B.1	R	T01L.B.1
B	LPCP.B.1	J	T04L.B.1	S	SU1L.B.1
C	SACP.B.1	K	T08L.B.1	T	SU2L.B.1
D	SURL.B.1	L	T10L.B.1	U	SU4L.B.1
E	WMLL.B.1	M	T20L.B.1	V	DF4L.B.1
F	INXP.B.1	N	T40L.B.1	W	
G		P	DF1L.B.1	X	
H		Q	DF2L.B.1	Y	
				Z	

$Y is the DFEU-1 cable for a 1 x 2/2 x 4 Exchange or Exchange cable 3 for a 4 x 16 Exchange.

Table 5-4. Card 2 Frontplane Connectors $X, #X, $Y, and #Y (Cont)

Pin	Logic	Pin	Logic	Pin	Logic
A	FLCP.A.1	I	T02L.A.1	R	T01L.A.1
B	LPCP.A.1	J	T04L.A.1	S	SU1L.A.1
C	SACP.A.1	K	T08L.A.1	T	SU2L.A.1
D	SURL.A.1	L	T10L.A.1	U	SU4L.A.1
E	WMLL.A.1	M	T20L.A.1	V	DF4L.A.1
F	INXP.A.1	N	T40L.A.1	W	
G		P	DF1L.A.1	X	
H		Q	DF2L.A.1	Y	
				Z	

#Y is the DFEU-1 cable for a 1 x 2/2 x 4 Exchange, or Exchange cable 1 for a 4 x 16 Exchange.

Table 5-5. Card 4 Frontplane Connectors $X, #X, $Y, and #Y

Pin	Logic	Pin	Logic	Pin	Logic
A	WL1L.1.1	I	ZN1F.1.1	R	RL3L.1.1
B	WL2L.1.1	J	ZN2F.1.1	S	RL4L.1.1
C	WL3L.1.1	K	W15L.1.1	T	RL5L.1.1
D	WL4L.1.1	L	ITSF.1.1	U	RL6L.1.1
E	WL5L.1.1	M	HTMR≠7.1	V	RL7L.1.1
F	WL6L.1.1	N	HBSF.2.1	W	RL8L.1.1
G	WL7L.1.1	P	RL1L.1.1	X	HASF.1.1
H	WL8L.1.1	Q	RL2L.1.1	Y	HASF.2.1
				Z	HBSF.1.1

$X is the interface between two Disk File Controls for a 2 x 4 Exchange.

Table 5-5. Card 4 Frontplane Connectors $X, #X, $Y, and #Y (Cont)

Pin	Logic	Pin	Logic	Pin	Logic
A	WL1L.2.1	I	ZN1L.2.1	R	
B	WL2L.2.1	J	ZN2L.2.1	S	
C	WL3L.2.1	K	WISL.2.1	T	
D	WL4L.2.1	L	ITSL.2.1	U	
E	WL5L.2.1	M	TSDL.2.1	V	
F	WL6L.2.1	N	HBSF.221	W	
G	WL7L.2.1	P		X	HASF.121
H	WL8L.2.1	Q		Y	HASF.221
				Z	HBSF.121

#X is the interface between two Disk File Controls for a 2 x 4 Exchange.

Pin	Logic	Pin	Logic	Pin	Logic
A	RL1L.B.1	I	WL1L.B.1	R	WISL.B.1
B	RL2L.B.1	J	WL2L.B.2	S	Z02L.B.1
C	RL3L.B.1	K	WL3L.B.1	T	ITSL.B.1
D	RL4L.B.1	L	WL4L.B.1	U	EUSL.A.1
E	RL5L.B.1	M	WL5L.B.1	V	TSDL.B.1
F	RL6L.B.1	N	WL6L.B.1	W	
G	RL7L.B.1	P	WL7L.B.1	X	
H	RL8L.B.1	Q	WL8L.B.1	Y	Z01L.B.1
				Z	

$Y is the DFEU-2 cable for a 1 x 2 or 2 x 4 Exchange.

Pin	Logic	Pin	Logic	Pin	Logic
A	RL1L.A.1	I	WL1L.A.1	R	WISL.A.1
B	RL2L.A.1	J	WL2L.A.1	S	Z02L.A.1
C	RL3L.A.1	K	WL3L.A.1	T	ITSL.A.1
D	RL4L.A.1	L	WL4L.A.1	U	EUSL.A.1
E	RL5L.A.1	M	WL5L.A.1	V	TSD6.A.1
F	RL6L.A.1	N	WL6L.A.1	W	
G	RL7L.A.1	P	WL7L.A.1	X	
H	RL8L.A.1	Q	WL8L.A.1	Y	Z01L.A.1
				Z	

#Y is the DFEU-2 cable for a 1 x 2/2 x 4 Exchange, or Disk File Exchange cable 2 for a 4 x 16 Exchange.

BACKPLANE CONNECTORS

The backplane connections for Disk File Controls I or II are listed in tables 5-6 through 5-9.

Table 5-6. Card 1 Backplane Connectors

X			Y	
0	1	Pin	0	1
		A		
EXCH00.0	EXCH01.0	B		CHAL...0
EXCH02.0	EXCH03.0	C	ACNTP..0	CLRB...0
EXCH04.0		D	CCNTP..0	
EXCH05.0	EXCH06.0	E	CLKENA.0	RC.....0
EXCH07.0	EXCH08.0	F	CLRCHANO	CA.....0
EXCH09.0		G		SR.....0
		H	CLKEND.0	
		I	BCNTP..0	DCNTP..0
		J	CLKENB.0	
EXCH16.0	EXCH17.0	K		
EXCH18.0	EXCH19.0	L	1US....0	
EXCH20.0	EXCH21.0	M	4US....0	
EXCH22.0		N	8MHZTSTO	TESTER.0
WL81...0	SETIN..0	P		CLRMOS.0
WL7L...0		Q	CLKENC.0	
WL6L...0	DUMPA..0	R	STC14160	WDPTF..0
32US...0	DUMPB..0	S	WRTIM..0	CHANHI.0
1024US.0	DUMPC..0	T	SRVRQN.0	PWRON..0
WL5L...0	DUMPD..0	U	LDIN...0	RL1L./.0
WL4L...0	WL3L...0	V	RL2L./.0	RL3L.1.0
SCPM...0		W	RL4L.1.0	
WL2L...0	WL1L...0	X	RL5L.1.0	
	RL6L.1.0	Y	RL7L.1.0	RL8L.1.0
		Z		

Table 5-7. Card 2 Backplane Connectors

X			Y	
0	1	Pin	0	1
		A	EUSF...0	WRCLEAR0
EXCH00.0	EXCH01.0	B	TERMF/.0	CHAL...0
EXCH02.0	EXCH03.0	C	ACNTP..0	CLRB...0
EXCH04.0		D	CCNTP..0	
EXCH05.0	EXCH06.0	E	CLKENA.0	RC.....0
EXCH07.0	BUFSEMP0	F	CLRCHAN0	CA.....0
LOADD..0		G	CLKENC.0	SR.....0
LOADC..0	SLAVE..0	H	CLKEND.0	DTMR=T00
LOADB..0	DPEF...0	I	BCNTP..0	DCNTP..0
LOADA..0		J	CLKENB.0	
EXCH16.0	EXCH17.0	K	EUPRES.0	EUBUSYF0
EXCH18.0	EXCH19.0	L	SACF...0	
EXCH20.0	EXCH21.0	M	INXF...0	SAFL...0
EXCH22.0		N	DTMR=4.0	TESTER.0
PAUSE..0	SETEUR.0	P	SSF/...0	SETIN..0
TEST...0		Q	COHTL..0	
WRITE..0	DUMPA..0	R	STC14160	CT1L...0
READ...0	DUMPB..0	S	WDPTF..0	CHANHI.0
MAINT..0	DUMPC..0	T	SRVRQN.0	LPTL...0
WAIT...0	DUMPD..0	U	STUAL4.0	WLOF...0
BFSFLF/0	SC8F...0	V	STVAL5.0	ITSF=0.0
SCPM...0		W	STVAL6.0	
STC10..0	SC4F...0	X	21XFR..0	22XFR..0
BFAR≠0.0	SC2F...0	Y	SURL...0	JUSTF/20
	SC1F...0	Z		

Table 5-8. Card 3 Backplane Connectors

X			Y	
0	1	Pin	0	1
	EXCH01.0	A	EUSF...0	
EXCH00.0	EXCH01.0	B	TERMF/.0	HASF.1.0
EXCH02.0	EXCH03.0	C	HASF.220	HBSF.1.0
EXCH04.0		D	HBSF.220	
EXCH05.0	EXCH06.0	E	LPCP...0	INXP...0
EXCH07.0	BUFSEMP0	F	CLRCHAN0	SACP...0
	AC-1...0	G	EUBL...0	EXILF..0
INXL...0	AC=2...0	H	DSM....0	
		I	EU=03.A0	EU=02.A0
		J	EU=01.A0	
AC=3...0	AL2L.1.0	K	EUPRES.0	
RL4L.1.0	ZN2F...0	L	SS2F...0	
ZN1F...0	ADCL...0	M	SSF/TSTO	
	FCLP...0	N	SSF....0	TESTER.0
	SETEUR.0	P	SSF/...0	EU=00.A0
TEST...0		Q	COHIL..0	
WRITE..0		R	DABC...0	BFAR≠0.0
READ...0		S		COHI...0
MAINT..0		T	WMLL...0	LPTL...0
JUSTF/20		U	STVAL4.0	RL1L.1.0
	SC8F...0	V	STVAL5.0	RL3L.1.0
SCPM...0		W	STVAL6.0	
	SC4F...0	X	21XFR..0	22XFR..0
BFAR#0.0	SC2F...0	Y	SURL...0	COHIL/.0
	SC1F...0	Z		

Table 5-9. Card 4 Backplane Connectors

X			Y	
0	1	Pin	0	1
		A	WRITE..0	
DFCOF/.0	BFSEL/0	B	READ...0	HASF.1.1
ITSF 0.0	INXL..0	C	HASF.221	HBSF.1.1
PAUSE..0		D	HBSF.221	
MAINT..0	LPTL..0	E	LPCP...0	INXP...0
LDIN...0	BUFSEMPO	F	CLRCHANO	SACP...0
LOADD..0	AC=1...0	G	EUBL...0	EXILF..0
LOADC..0	AC=2...0	H	DSM....0	DTMR=T00
LOADB..0	DPEF...0	I	EU=03.A0	EU=02.A0
LOADA..0		J	EU=01.A0	
AC=03..0	SLAVE..0	K	CT1L...0	EUBUSYFO
DABC...0	ZN2F...0	L	SACF...0	
ZN1F...0	ADCL...0	M	INXF...0	BRKFB..0
WL1L...0	FCLP...0	N	DTMR=4.0	TESTER.0
WL8L...0	WL3L...0	P	SAFL...0	EU=00.A0
WL7L...0		Q	RL2L.1.0	
WL6L...0	DUMPA..0	R		WDPT...0
32USB..0	DUMPB..0	S	WRTIM..0	WLOF...0
1024USBO	DUMPC..0	T	WMLL...0	PWRON..0
WL5L...0	DUMPD..0	U	STVAL4.0	RL1L.1.0
WL4L...0	SC8F...0	V	STVAL5.0	RL3L.1.0
SCPM...0		W	RL4L.1.0	
STC10..0	SC4F...0	X	RL5L.1.0	RL6L.1.0
WL2L...0	SC2F...0	Y	RL7L.1.0	RL8L.1.0
	SC1F...0	Z		

DFSU SEGMENTS PER TRACK

The number of segments in a logical track for all applicable Disk File Storage Unit types (with the exception of Systems Memory) is shown in table 5-10.

Table 5-10. Logical Track Segments

Zone	1C-3	1C-4	1A-3	1A-4
0	73	69	27	62
1	95	89	36	81
2	110	120	50	103
Total Tracks	278	278	113	246

SYSTEMS MEMORY STRUCTURE

The Systems Memory consists of a single physical disk divided into two "areas" on each side of the disk. Each "area" contains 50 tracks. Refer to figure 5-1.

TRACK SELECT LEVELS

The seven Track Select levels (T01L, T02L, T04L, T08L, T10L, T20L, and T40L) are used to select one of the possible 50 tracks (00 through 49) within an "area." All tracks are numbered from the center side to the outside of the disk.

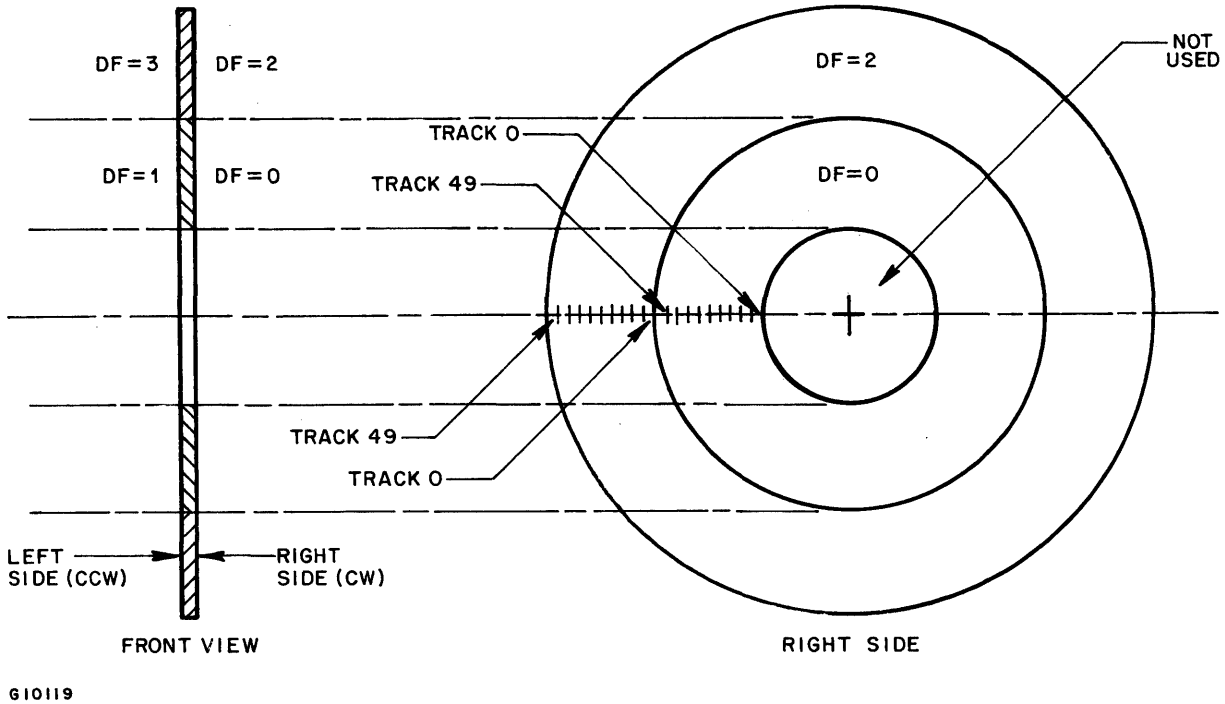


Figure 5-1. System Memory Disk Structure

DISK FACE (AREA LEVELS)

The Disk Face levels (DF1L and DF2L) are used to select the disk face and area. DF1L is used to select the disk face; DF2L is used to select the area on the selected disk face as listed in table 5-11.

Table 5-11. Disk Face Level Selection

DF2L	DF1L	Selected Area	
0	0	DF=0	Inner-right (clockwise) side
0	1	DF=1	Inner-left (counterclockwise) side
1	0	DF=2	Outer-right (clockwise) side
1	1	DF=3	Outer-left (counterclockwise) side

HEAD GROUP ASSIGNMENT

On the right side of the disk (figure 5-1), the head groups are numbered from the center to the rim of the disk and are interlaced as listed in table 5-12.

Table 5-12. Right-Side Disk Head Group Assignment

Inner Face (DF=0)		
Head Number	Head Track	Track Addressed
2	0,2,4.....22	0,2,4.....22
1	1,3,5.....25	1,3,5.....25
4	24,26.....48	24,26.....48
3	27,29.....49	27,29.....49
Outer Face (DF=2)		
6	0,2,4.....22	0,2,4.....22
5	1,3,5.....25	1,3,5.....25
8	24,26.....48	24,26.....48
7	27,29.....49	27,29.....49

On the left side of the disk, the head groups are numbered from the rim to the center of the disk and interlaced as listed in table 5-13. The addressable tracks, however, are numbered from the center to the rim of the disk.

Table 5-13. Left-Side Disk Head Group Assignment

Inner Face (DF=1)		
Head Number	Head Track	Track Addressed
7	49,47.....27	0,2,4.....22
8	48,46.....24	1,3,5.....25
5	25,23.....1	24,26.....48
6	22,20.....0	27,29.....49
Outer Face (DF=3)		
3	49,47.....27	0,2,4.....22
4	48,46.....24	1,3,5.....25
1	25,23.....1	24,26.....48
2	22,20.....0	27,29.....49

STORAGE UNIT LEVEL AND ZONE LEVELS

The Storage Unit Level (SUlL) is used to indicate an overflow condition (which will also cause a not-ready condition). The zone levels are not used for Systems Memory, since the Disk File Control is forced into zone 3.

TRACK SELECT DELAY AND WRITE LOCK LEVELS

Track Select Delay Level (TSDL) and Write Manual Lock Level are not used in the Systems Memory.

TEST PROCEDURES

Since the Disk File Control I or II is a "soft" control, there is no means for off-line operation of the disk file to accomplish adjustments on the disk files. To facilitate such adjustments as read, bit, and address pre-amps, an additional section (section 6) was incorporated into the disk file test.

To make the use of this test section, the Field Engineer can fabricate a button switch to allow the Ready level to the control, from the DFEU, to go false. Figure 5-2 portrays this fabrication for the 1C-type disk:

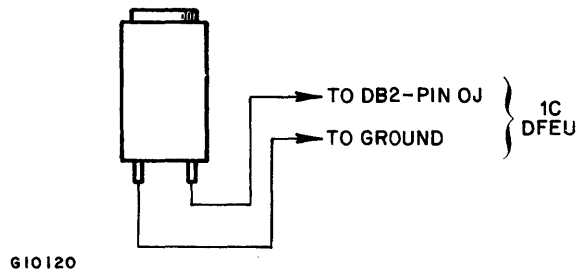


Figure 5-2. DFEU Ready Maintenance Switch

DISK FILE CONTROL TROUBLESHOOTING

VISUAL CHECKS

a. Ensure that all control cards are loaded into the correct slots.

b. Ensure that the cabling is correct.

c. Ensure that the channel number jumper chip has been installed correctly and that no other control has the same number.

d. Ensure that the control type and number jumper chip has been installed correctly.

e. Ensure that the DFSU-type jumper chips have been installed correctly.

EXECUTION OF DISK TEST ROUTINES

a. Ensure that the processor and memory are functioning properly. (If necessary, run appropriate test routines.)

b. Run the Disk File Test routine. If it fails, test control cards in B 1700 Field Card Tester.

c. Isolate failure through the use of I/O Debug Test routine and logical troubleshooting methods if cards pass card tester checks.

d. Attempt to re-create original failure and then troubleshoot by logic methods if control passes all tests.

If steps b. c, and d do not reveal failure, check all cabling for a possible cause of failure.

AREAS OF LOGIC FOR TROUBLE ISOLATION

The four primary problems that can occur in the DFC are misaddressing, data errors, parity errors, and timeouts. The logical areas to be checked for each of these problems are listed below.

a. Misaddressing

Card 3: File Address Register, Segment Address Register, address compare, Binary File Address Register, parameter generator (includes DFSU-type jumper chip).

Card 4: Address counter.

b. Data Errors

Card 1: MOS buffers A through D (can be isolated to one buffer by means of I/O Debug Routine, using a Read or Write operation of one through four segments per operation), input/output gating, MOS clock generation, read/write lines.

Card 2: MOS clock enables, buffer status, justify logic, and load/dump logic.

c. Parity Errors

Card 4: Parity logic (false parity errors, data-errors-listed logic (valid parity errors).

d. Timeouts

Card 4: Disk timers (appear to be no cause for timeouts such as DFEU or DFSU problems), address counter.

All of the preceding areas are affected by control logics such as Status or Sequence Count Failures, Control Clock, Clear logic, OP/CMD registers and decode, interface logic and Result descriptor generation logic.

PROCESSOR-TO-DISK TRANSFER PROBLEMS

Isolation of failing area can be simplified by the use of the I/O Debug Routine and the control flows. (Refer to the block flows for Read/Write/Pause/Test.) By using the STEP toggle and TRACE toggle of I/O Debug routine and following the progress of the control through the listing in comparison to the flows, it can be determined at which Status Count the failure occurs.

DISK FILE CONTROL-TO-DFEU TRANSFER PROBLEMS

The I/O Debug Routine should be used to loop in the failing operation, allowing logic troubleshooting of the control and interface. Figure 5-3 illustrates the logic layout of the disk track.

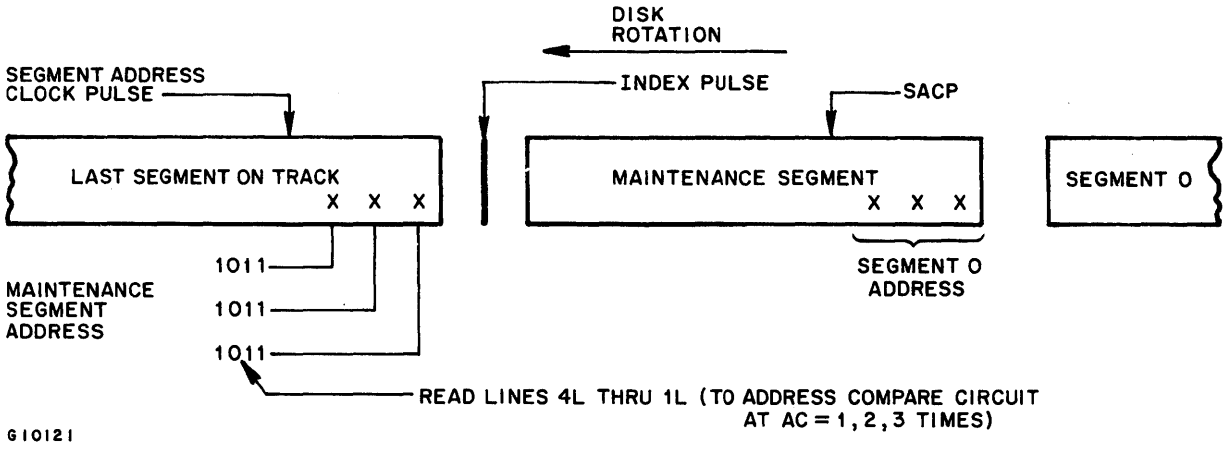


Figure 5-3. Logical Disk Track Layout

SECTION 6

INSTALLATION PROCEDURES

INTRODUCTION

This section (in conjunction with the Field Test and Reference documentation) provides information to install and check out a Disk File Control I or II.

LOGIC PREPARATION

CARD 1

The wire from pin R of jumper chip L4 designates channel number. The wire from pin A of jumper chip L4 signals channels 0 through 7. The wire from pin A of jumper chip K4 signals channel numbers 8 through 15. The channel jumper chip connections are listed in table 6-1.

Table 6-1. Channel Jumper Chip Connections

Jumper Chip Channel	L4		K4
	Pin R to	Pin A to	Pin A to
0	N/A	S	N/A
1	G	H	N/A
2	F	J	N/A
3	G and F	K	N/A
4	E	L	N/A
5	E and G	M	N/A
6	E and F	N	N/A
7	E, F, and G	P	N/A
8	D	N/A	S
9	G and D	N/A	H
10	F and D	N/A	J
11	F, G, and D	N/A	K
12	E and D	N/A	L
13	G, E, and D	N/A	M
14	F, E, and D	N/A	N
15	G, F, E, and D	N/A	P

CARD 2

Jumper chip L5 designates control type and number.

Control Type

a. Control with external exchange present:

Wire pin R to pin P.

b. Control with internal 2 x 4 exchange and control is the slave control:

Wire pin R to pin N and pin S.

c. Control with internal 2 x 4 exchange and control is the master control:

Wire pin R to pin N.

d. Control number: wired on the same chip (L5) and may be used in conjunction with any of the preceding type designations.

Control Number 0 - No wire.
Control Number 1 - Pin R to Pin L.
Control Number 2 - Pin R to Pin M.
Control Number 3 - Pin R to Pin M and Pin L.

CARD 3

Jumper chip A8 is used to designate DFSU types connected to selected DFEU channels 00 through 07 as shown in figure 6-1.

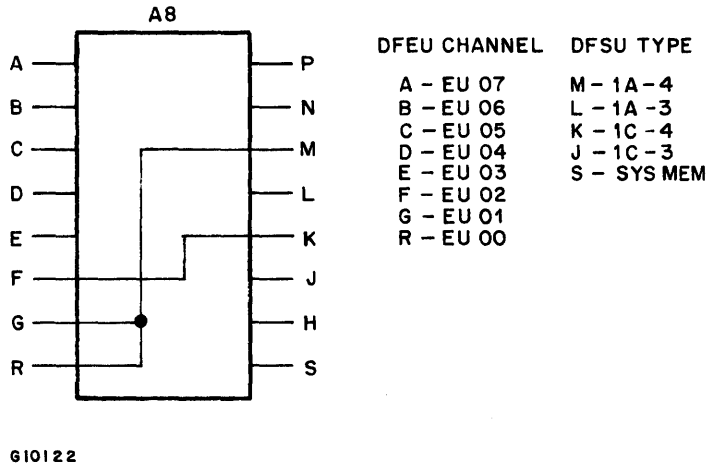
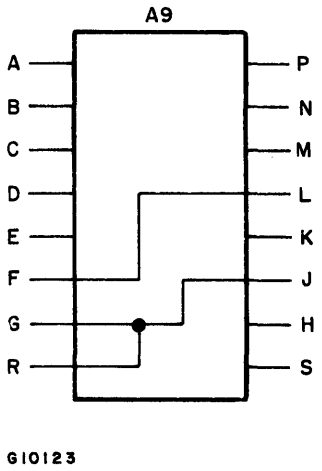


Figure 6-1. Jumper Chip A8

Jumper chip A9 is used to designate DFSU types connected to selected DFEU channels 08 through 15 as shown in figure 6-2.



DFEU CHANNEL	DFSU TYPE
A - EU 15	M - 1A-4
B - EU 14	L - 1A-3
C - EU 13	K - 1C-4
D - EU 12	J - 1C-3
E - EU 11	S - SYS MEM
F - EU 10	
G - EU 09	
R - EU 08	

Figure 6-2. Jumper Chip A9

PHYSICAL INSTALLATION

The Disk File Control occupies a 4-card position area in a card chassis and consists of a 4-card backplane, four logic cards, and the cable assembly to mate with the peripheral cables from one DFEU. With the addition of a 1 x 2 adapter, and an additional cable assembly, a second DFEU can be attached.

A 2 x 4 adapter provides the cable assembly to interconnect two Disk File Controls, allowing either one of two associated controls to communicate, without an external exchange, with any one of up to four DFEU's.

CARD LOADING

The Disk File Control must be installed on its own 4-card backplane. It should be installed next to any existing backplane to allow room for future backplane installations. The cards should be installed with card 1 on the right (frontplane view) to card 4 on the left. The interface is from the distribution card to $X and $Y on card 1. The coaxial clock cable also connects from distribution card to card 1 of the DFC.

CONTROL-TO-I/O ADAPTER PANEL CABLING

1x1 or 1x2 Application

Connect the following two disk file control cables as shown below:

From	To
Card 3, #Y, for DFEU-1	I/O adapter panel.
Card 4, #Y, for DFEU-1	I/O adapter panel.
Card 3, $Y, for DFEU-2	I/O adapter panel.
Card 4, $Y, for DFEU-2	I/O adapter panel.

2x4 Application

Route the control interface cables as follows:

From	To
Control 1, card 3, #X	Control 2, card 3, $X
Control 1, card 3, $X	Control 2, card 3, #X
Control 1, card 4, $X	Control 2, card 4, #X
Control 1, card 4, #X	Control 2, card 4, $X

Route the control-to-DFEU cables as follows:

From	To
Cards 3 and 4, $Y and #Y.	Appropriate DFEU cable mounting on the I/O adapter panel.

Termination

If the Disk File Control is the last control on an exchange, remove the line terminators from the distribution, subdistribution, or control card (located in the last device prior to the Disk File Control). Install the terminating resistors on Disk File Control card 1 at locations B6, B8, and C6 (133 ohms); add a 511-ohm resistor at B7, B9 and C7; and a 133/511-ohm mixed resistor at L2.

Refer to drawing D-22098925, supplied as a part of the Field Test and Reference documentation.

PERIPHERAL/CONTROL CHECKOUT

Upon completion of the physical installation, run the Disk File Diagnostic Test Routine to assure proper operation.

Burroughs Corporation Publications Remarks Form

B 1700 Disk File Controls I and II Technical Manual

Form No. 1066867, January,1976

Comments

From:

Date _____

Name _____

Title _____

Company _____

Address _____

_____

Fold Along Dashed Line

Fold, Staple, And Mail

Postage Will Be Paid by Addressee

No Postage Stamp Necessary If Mailed in the United States

BUSINESS REPLY MAIL
First Class Permit No. 1009; El Monte, CA 91731

Burroughs Corporation
P. O. Box 4040
El Monte, CA 91734

attn: Publications Department
Technical Information Organization

Fold, Staple, And Mail