B 1700
I/O BASE

INTRODUCTION
AND
OPERATION

FUNCTIONAL
DETAIL

CIRCUIT
DETAIL

ADJUSTMENTS

MAINTENANCE
PROCEDURES

INSTALLATION
PROCEDURES

RELIABILITY
IMPROVEMENT
NOTICES

OPTIONAL
FEATURES

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

AA370520
BURROUGHS CORPORATION
Detroit, Michigan 48232

Burroughs

Printed in U. S. America 6-26-72

For Library Binder 81D
Form 1053352

INDEX

INTRODUCTION

The B1700 will have soft I/O controls, in which all I/O operations are controlled by the processor.

INTERFACE

Control is by means of a direct interface between the processor and I/O controls called the "I/O bus interface". This interface may act as a source or sink for certain processor register operations.

I/O BASE

Connected to the I/O bus are from one to two I/O modules, each module containing from one to five I/O controls, plus, a signal distribution card, through which all signals pass going to and from the main I/O bus. The maximum number of I/O controls allowed is eight. Each I/O module also has its own signal distribution bus, known as the "module I/O bus".

I/O CLOCK

(I/O Clk) is provided for the base module via coax cable connection. It is then distributed to all base extensions (via coax cable), as SCPC. Each base extension then has an individual delay line which is used to synchronize SCPC with main system clock, and thus provide synchronized SCPM on each Module I/O Bus.

I/O BASE TO PROCESSOR INTERFACE SIGNALS

Mnemonic	Name	Description
CA	Command Active	Proc I/O. Indicates that a command is being transmitted. Duration is one system clock. Defines Phase A of I/O cycle.
RC	Response Complete	Proc I/O. Orders I/O system to accept command on exchange, Or, signals processor has accepted message. One system clock. Defines Phase B.
SR	Service Request	I/O Proc. Indicates that one or more I/O controls are in need of service. Lasts for as long as a device needs service. (See Test Service Request-Channel)
CLR	System Clear	Proc I/O. Clear I/O controls. Minimum duration three clocks. Asynchronous.
EXCH00 thru EXCH23	Data Exchange	Proc I/O. Transfer data, addresses, control signal etc. Exact use depends on cycle type.
IOS	I/O Send	I/O Control Dist. Switches interface on distribution card to transmit. (Only exchange lines can be switched.) Is an OR function from all controls.
SCPM	System Clock (Synchronized)	I/O Dist To Controls. Early clock, delayed at distribution card to synchronize with main processor clock. (+ – 5ns)

Table I-1

I/O COMMANDS

There are seven types of I/O Command, each consisting of Phase A, during which CA (Command Active) is true, Phase B, during which RC (Response Complete) is true.

COMMAND TYPES

The exact command type is defined by information transmitted on the exchange lines during Phase A. In general, the processor performs all assembly and dis-assembly of computer (24 bit) words, communicating with an I/O control in a byte size convenient to that control, up to a maximum size of one complete computer word.

TRANSFER OUT A

During Phase A of this cycle the processor transmits a command, the channel address of the I/O device to receive the command and, up to sixteen bits of data. The I/O control will accept the data at the end of Phase A. During Phase B the control will transmit its current status.

TRANSFER OUT B

During Phase B of this cycle up to twenty-four bits of data are transmitted to the control, which must accept the data at the end of RC. Not used in present system.

TEST STATUS

This cycle causes the control to transmit during Phase B, the device ID, current control status, and device present bit.

CLEAR AND TEST STATUS

Similar to the Test Status cycle, except that the I/O control is cleared to the reset condition at the end of Phase A. (The reset status is transmitted during Phase B.)

TEST SERVICE REQUEST–CHANNEL

This command is received by all controls connected to the main I/O bus. Its function is to determine which channel(s) is (are) requesting service. The cycle is generally only commanded if the SR (service request) line to the processor is true. During Phase B each control transmits a bit indicating (1) if it is requesting service. The bit location (on the data exchange) is assigned according to channel address.

TERMINATE DATA

Used for output devices which will accept data in variable record lengths. The command indicates that the last data of the record has been transmitted. During Phase B the control transmits status. Also for variable length device, such as disk terminate is required to exit from a read or write operation.

TRANSFER IN

During Phase B up to 16 bits of data are transmitted to the processor.

TIMING

CA and RC must each be one system clock duration (nominal). I.e. only one system clock trailing edge must occur while CA or RC is true. SCPM, the synchronized clock at the backplane of each I/O module is synchronized with the master clock at the processor backplane.

The 500 nsec. minimum spacing from CA to RC indicates two cycles of a 4MHz clock.

The four clock period minimum spacing from RC to CA applies whether the same channel or a different channel is addressed. (See Figure II-3)

I/O SUBSYSTEM CONTROL

Two pseudo registers (Data and Command) are used by the B1700 processor to transfer data or commands to an from the I/O bus.

As we have seen there are seven different types of I/O cycles, and each executes in two phases, Phase A and Phase B. Execution of either a 1C or 2C Micro (CMMD) will initiate an I/O cycle. CA is generated when this occurs. To complete the cycle the execution of the 1C or 2C Micro (move Data to Reg or Reg to Data) will complete the I/O cycle. This causes RC to be generated.

DATA

A twenty-four bit pseudo register used predominately for data transfer to and from the I/O subsystem, via the main I/O bus. It can be used as a source or destination with the RC signal being generated in both cases. At present data is used only as a source (I/O to Processor).

CMND

A twenty-four bit pseudo register which can act only as a destination (Proc. to I/O). It is used to transfer commands to devices on the I/O bus, and, whenever it is used the signal CA is generated to the interface.

BIT CC01

BIT CC01 of the C-register is set whenever the signal SR is true on the I/O interface signifying that an I/O control requires service.

I/O CONFIGURATION AND RESTRICTIONS

The B 1700 I/O configurations and restrictions are as follows:

a. Only one I/O Base (figure I-1) is permitted in a B 1700 system.

b. Only one I/O base extension is permitted in a B 1700 system. An I/O Base Extension-1 (figure I-1), -2 (figure I-1), or -3 (figure I-2) can be used in a B 1700 system.

c. A maximum of six I/O backplanes are permitted in a B 1700 system. The backplanes are connected in parallel to the I/O bus by means of cables that enter and leave the sub-distribution board on each I/O backplane. The sequence of the I/O bus cabling is:

   1. Processor to I/O Base.

   2. I/O Base to I/O Base Extension.

   3. I/O Base Extension to an Independent I/O backplane.

   4. Independent I/O backplane to another Independent I/O backplane.

d. A Dual Single Line control is considered as two independent I/O backplanes.

e. The maximum I/O Bus cable length from the processor to the final I/O backplane must not exceed 23 feet (7 meters).

f. The maximum number of I/O controls on a B 1700 system is 15. The actual number of I/O controls on a B 1700 system is limited due to space, power, and I/O backplane locations.

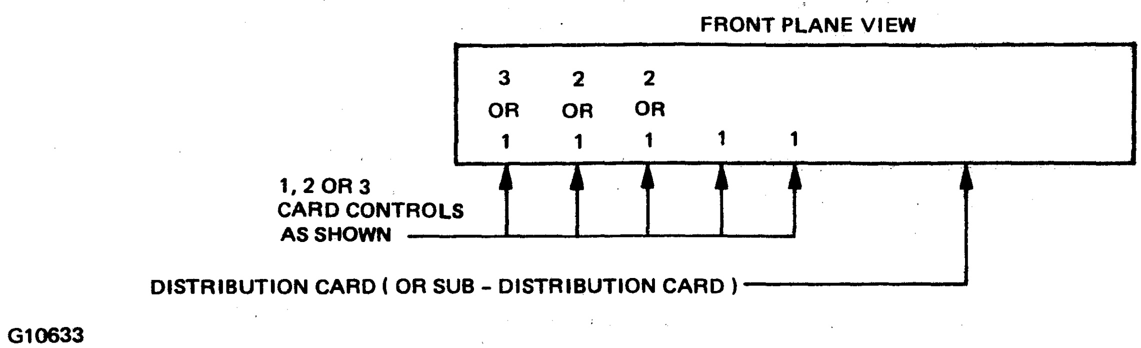


Fig. I-1 I/O BASE, I/O BASE EXTENSION-1, OR I/O BASE EXTENSION-2

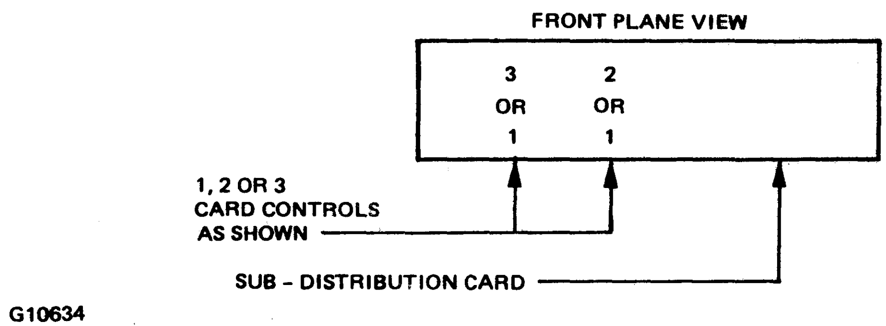


Fig. I-2 I/O BASE EXTENSION-3

g. Certain I/O controls are restricted to the lower eight or upper seven channel numbers. I/O controls subject to channel number restrictions are listed in table I-2.

Table I-2 CHANNEL NUMBER RESTRICTIONS

Channel 0-7

80 Column Multi-Function Control
96 Column Card Read/Punch/Print Control
Operator Display Console Control 2

Channel 8-14

Magnetic Tape Control IV
Magnetic Tape Control V
Disk Pack Control I
Disk Pack Control II
Disk File Control 3

Channel 0-14

All other I/O controls

h. The recommended channel number assignments are listed in table I-3. The channel number assignments for the Single-Line Control, Reader/Sorter Control, Magnetic Tape Control, and the Magnetic Tape Cassette Control must be in the sequence listed in table I-3.

If the system has more than one control of the same type, they normally are assigned adjacent channel numbers. All other controls are assigned or reassigned to the next lower channel number.

MCP system disk pack/disk cartridge controls must have common channel number assignments to permit interchangeability.

Table I-3 RECOMMENDED CHANNEL NUMBER ASSIGNMENT

Channel Number	Control
14	Single-Line control
13	Reader/Sorter control
--	Magnetic Tape control IV
--	Magnetic Tape control 5
12	Magnetic Tape control 2
--	Magnetic Tape control 3
11	Magnetic Tape Cassette control
--	
10	
9	Disk Pack control
8	
7	Disk File control
6	
5	Disk Cartridge control
4	
3	Line Printer
2	96 column or 80 column input/output controls
1	96 column or 80 column input controls
0	SPO control or Operator Display Console control

i. A Multi-Line control is connected to a Port Adapter 1 in the port interchange. A Multi-Line Extension is cabled to the Multi-Line control and must be installed adjacent to the Multi-Line control in the same card chassis. A maximum of two Multi-Line controls and two Multi-Line extensions are permitted in a B 1720 system.

j. All I/O controls except the controls listed in table I-4 include a cable assembly to mate with the peripheral device. The cable assembly for the controls listed in table I-4 is provided with the appropriate adapter for these controls.

Table I-4 CONTROLS WITHOUT CABLE ASSEMBLIES

80 Column Card Punch Control 1
Magnetic Tape Control 1
Magnetic Tape Control 2
Magnetic Tape Control 3
Multi-Line Control 1

An I/O Cable panel is used to mount cable connectors which mate with the peripheral cables. Each panel can accept six plates and each plate can accommodate one of the following:

1. One 75P Winchester connector

2. One 104P Winchester connector

3. Two 50P Standard connectors

4. Three 25P Standard card edge connectors

5. Six 25P Cannon connectors

The number of connectors and the type of connector used by the various peripherals are listed in table I-5.

Table I-5 CABLE CONNECTORS FOR PERIPHERAL DEVICES

75P Winchester	104P Winchester
475/800/1400 CPM Card Reader	Printers on PC-3
150/300/CPM Card Punch M2	1625 DPM Reader-Sorter
100 CPM Card Punch	MT 90-120 IPS NRZ Tape
Paper Tape Reader-1	
Paper Tape Reader-2	
Paper Tape Punch	

25P Standard Card Edge	50P Standard
Printers on PC-5	Disk Cartridge Single or Dual (1)
MT Cluster (2)	96 Col Card Reader (1)
MEC (1)	96 Col Keypunch (2)
SM1B (2)	300/600/800 CPM Card Reader (1)
DFEU 1A (2)	80 Col Keypunch (1)
DFEU 1C (2)	300/500 LPM Printer (1)
Disk Pack (1)	86/150/250 LPM Printer ODEC (1)
150/300 Cd Punch M3 (1)	PEC Magnetic Tape (2)
SPO-1 (1)	Cassette Tape (1)
DF Exchange (3)	
DE-01	

25P Cannon
Data Communications
Data Sets
SPOC-2

k. The following peripheral restrictions and conditions apply to the B 1700 systems:

1. System required controls are:

SPO (TTY or CRT)	-	1 maximum
Disk (Pack, Cartridge, or HPT)	-	1 minimum
Input Device (e.g., Card Reader)	-	1 minimum
Output Device (e.g., Printer)	-	1 minimum

2. The maximum number of Reader/Sorters permitted in the system is dependent upon S-Memory size, the speed of the Reader/Sorter, the time required by the user program, and the time required by the system software to service Reader/Sorter operations.

   If the flow rate is to be maintained, the time required by the software and user procedures must be less than the critical times listed in table I-6. The time to empty the buffer is only significant for the MICR read.

Table I-6 READER/SORTER FLOW RATE TIMING

Unit Speed	Time Allowed To Pocket Select Item After Service Request (MICR)	(OCR)	Time Allowed To Empty Buffer After Service Request
1625 DPM	38 ms	15 ms	17 ms

3. The amount of S-Memory required is a function of the user program size and functions. In general, S-Memory must be large enough to contain the working set of the program code and the system software. For further details, see the documentation supplied with each software release.

The maximum data rate (characters per second) permitted by MT transports on B 1700 systems is:

	MTC-1, -2 2 x N	MTC-3 2 x N	MCT-4, -5 2 x N
B 1712	36K	40K	80K
B 1714	72K	100K	120K
B 1720	100K	100K	200K

4. Interaction of a magnetic tape record (>800 bytes with MTC-1, >400 bytes with MTC-2, >800 bytes with MTC-3, >900 bytes with MTC-4 and >1800 bytes with MTC-5) with a long S-Instruction occasionally results in an access failure.

5. Interaction of SLC record greater than 26 bytes at a data rate of 9.6K bits/sec (1.2K bytes/sec) with a long S-Instruction (greater than 8.5-9.0 ms) occasionally results in an access failure on input data. Higher data rates may result in failures with proportionally shorter S-Instructions. The maximum number of SLC's per system is restricted by data rates as listed in table I-7.

Table I-7 SINGLE LINE CONTROL PER SYSTEM

Speed (bits/sec)	Maximum Number of SLC's
9.6K	4
19.2K	2
50.0K	1

6. The 205/206 Disk Pack Drive, the Industry Compatible Mini-Disk, and the MICR Reader/Sorter are not permitted on certain B 1700 systems. These exclusions are listed in the EDP Equipment Price Book.

l. Either an I/O Base-1 or an I/O Base Extension-1 is required for DCC-1.

m. Either an I/O Base-2 or an I/O Base Extension-2 is required for DCC-2 or -3.

n. The I/O Base Extension Conversion Kit-1 permits conversion from -1 to -2 or from -2 to -1.

o. The 96 Column Card Reader-Card Punch Control-1 is functionally equivalent to -2. Later systems use Control-2.

p. The PTRC-1 is used with Paper Tape Reader-1 and -2R. Systems using PTRC-1 are limited to reading an integer number of 96 characters. Later systems use PTRC-2 which provides for reading any number of characters.

q. The Printer Control-2, Printer Control -2K and Katakana Mod Kit-1 (for Printer Control-2) are used with the B 9247 400/750 LPM Printers. Printer Control-2K is a Printer Control-2 with the Katakana Mod Kit installed. Later systems use Printer Control-5 which also provides for the B 9247 1100/1500 LPM Printers.

r. The Reader/Sorter Control-1 provides for 4-bit MICR reading only. Later systems use Reader/Sorter Control-2 which also provides for numeric OCR reading. Reader/Sorter Control-2 also provides for enabling programming non-impact endorsement. It does not provide for loading non-impact endorsement data, a feature of the B 1937 Phase-2 Reader-Sorter.

s. The DCC-1 and -2 are used with the 32 sector Disk Cartridge Drives. Later systems use DCC-3 which can be used with 32 and 64 sector drives.

t. The DFC 1 is used with the 1C-3, 1C-4, and 1A-3 DFCU's. The DFC 2 is used with 1C-3, 1C-4, 1A-3, 1A-4, SM1B and the 2x4 adapter.

u. The MTC-2 and its associated adapters are used with NRZ 9T tape. Later systems use MTC-3 which provides additional buffering.

v. The MTC-4 is used with PE 9T tape. Later systems use MTC-5 which, although smaller, provides additional buffering.

w. The DPC-1 is used with Disk Pack Drives. Later systems will use DPC-2 which is smaller.

DETAILED INTERFACE (PROCESSOR/DISTRIBUTION CARD/I/O CONTROL)

EXCHANGE LINES

Figure II-1 illustrates the interface between the Processor, the Distribution Card and an I/O Control located within the I/O Base. The 24-bit I/O Bus (BUS 23 thru BUS 00IE1) is shown as 24 bi-directional lines from the Processor (Card E) to the Distribution Card in the I/O Base.

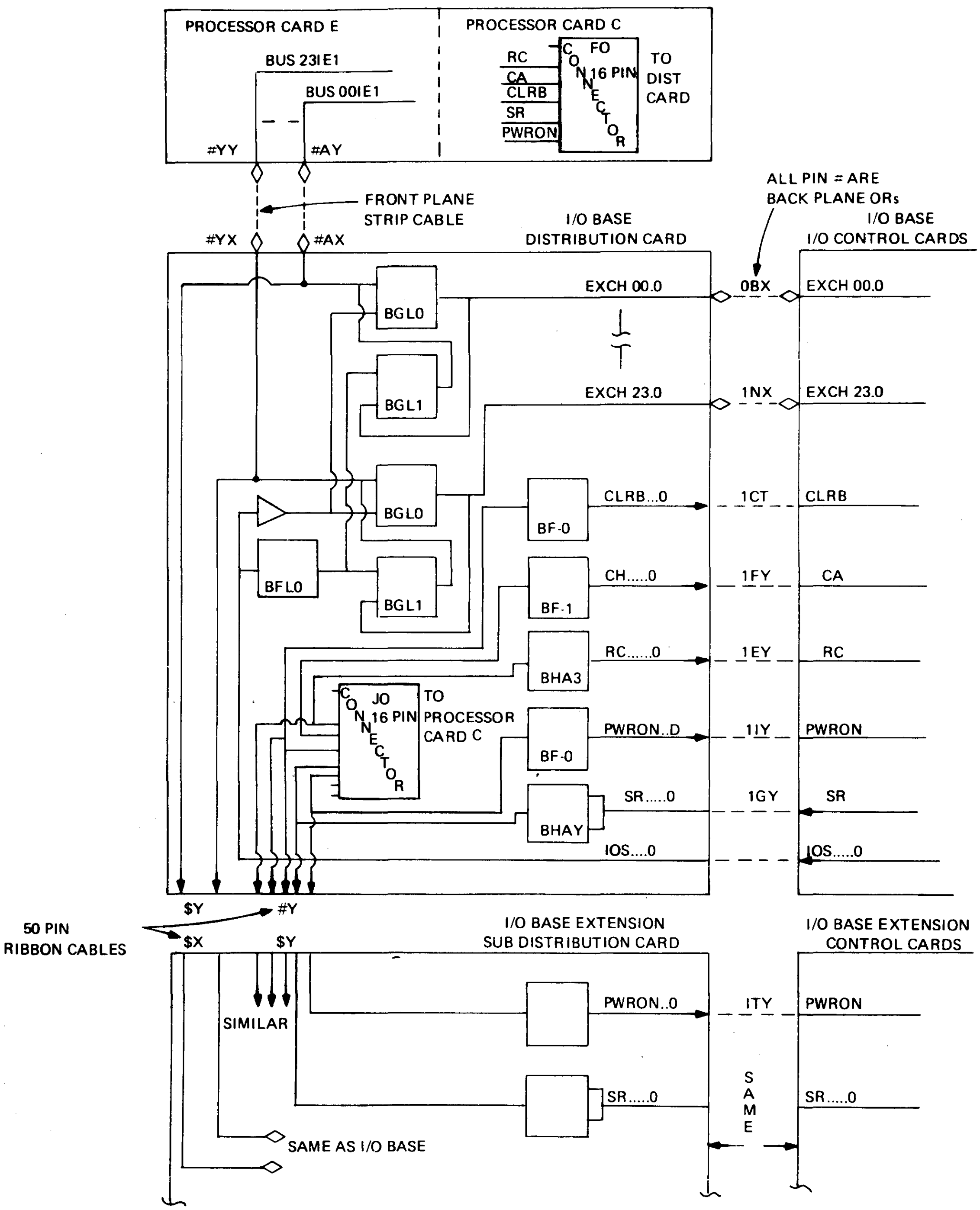


Fig. II-1 DETAILED INTERFACE

The 24-bit I/O is also shown distributed from the Distribution Card to a Sub or "Extension" Distribution Card in an Extension I/O Base if present. The 24-bit I/O Bus from the Processor (Card E) to the Distribution Card is contained within a Strip Cable connected to the front plane of each card.

From the Distribution Card to a Sub Distribution Card the 24-bit I/O Bus is also bi-directional and again transmitted through a Strip Cable. The direction of transmission (to or from the Processor) is controlled by the level I/O Send (IOS. . . .0) which is generated in each of the I/O Controls located within the I/O Base as well as in each of the I/O Controls located within an I/O Base Extension. IOS. . . .0 is normally false which allows the information on the 24-bit I/O Bus to be received from the Processor.

When a particular I/O Control is requested to send data to the Processor as the result of a command being transmitted during CA time, the I/O Control will cause IOS. . . .0 to be true at the proper time.

CONTROL LINES

The five control levels are shown as unidirectional levels between the Processor (Card C) and the Distribution Card in the I/O Base A 16 connector Cable provides the transmission of these levels and is connected to a chip socket on each card.

The control levels are also distributed to each of the I/O Controls within the I/O base as well as the I/O Controls located within an I/O Base Extension. Note that although the five control levels are unidirectionally transmitted either to all I/O Controls or from all I/O Controls, in the case of CA and RC, a particular I/O Channel can be designated during CA time as six of the seven cycle types designate a particular Channel to receive the Command, refer to Command Types.

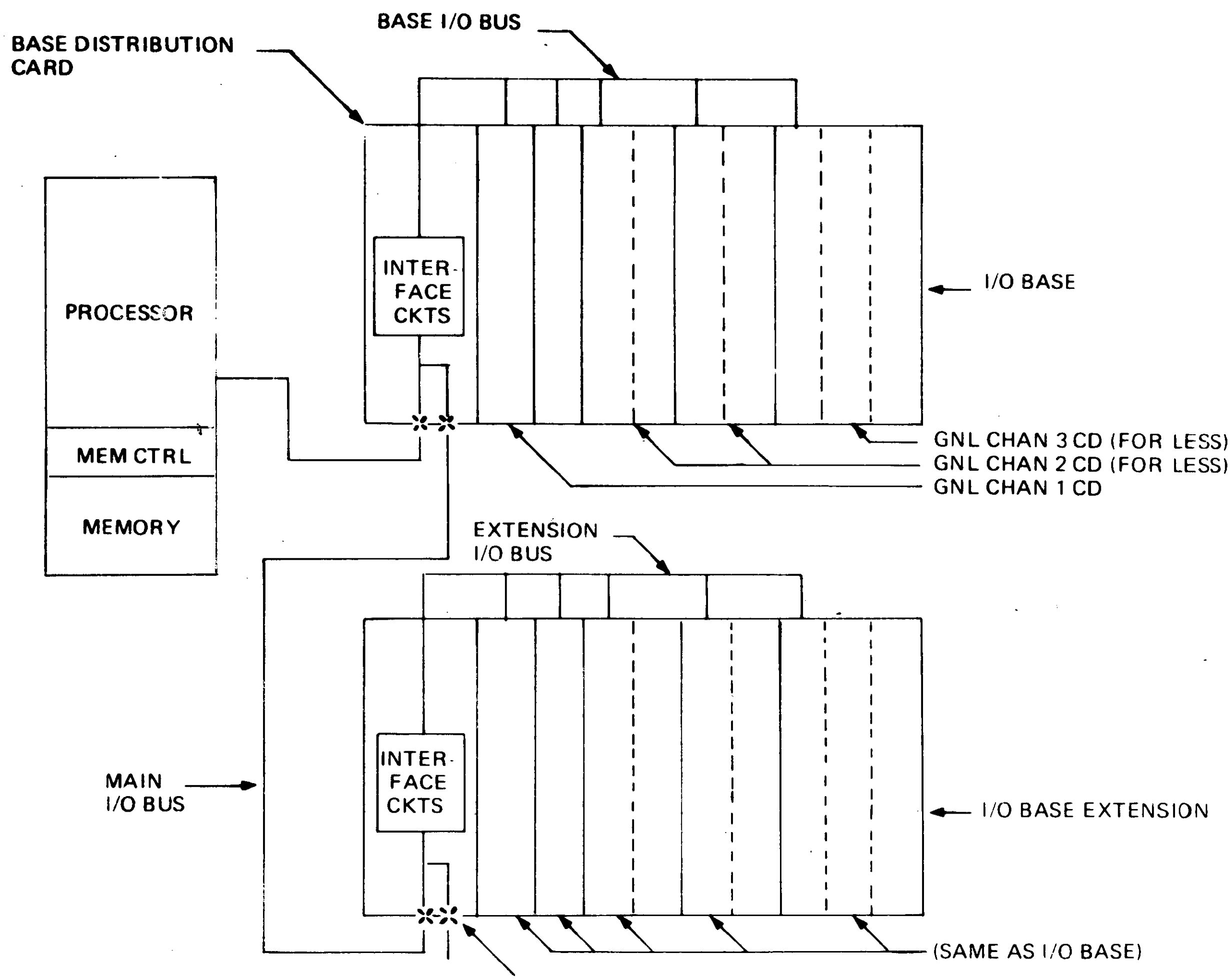


Fig. II-2 I.O. SUBSYSTEM BLOCK DIAGRAM

I/O BASE SIGNAL DISTRIBUTION

The Block Diagram of an I/O Subsystem shown in Figure II-2 illustrates basically the distribution of interface levels to I/O Base Extensions. Two strip cables are again used to transmit both the 24-bit I/O Bus and the five control levels. The strip cable used to transmit the control level also transmits the 1, 4, 32, & 1024 μs slow clock pulses developed in the Distribution Card (I/O Base) to the Sub Distribution Cards in the I/O Base Extensions.

The 4 MHz System Clock is distributed to the Sub Distribution Cards via Coaxial Cable, one to each Sub Distribution card present. The Interface Circuits shown in the Sub Distribution Cards is similar to those in the Distribution Card which is illustrated in Figure II-1. Only the Distribution Card in the I/O Base has the Slow Clock Circuitry which is distributed via strip cable to the Sub Distribution Cards.

I/O SYSTEM

MAXIMUM NUMBER OF CONTROLS AND I/O BASE EXTENSIONS

The maximum number of Controls which can be installed in either the I/O Base or an I/O Base Extension is restricted to five. One I/O Base and one I/O Base Extension is permitted; however, the total number of I/O Controls is restricted to 15.

SPECIAL CONTROLS

I/O Controls requiring more than 3 cards must be installed in their own I/O Base Extension with their own Backplane.

COMMAND TYPES

GENERAL

Seven cycle types or "command types" have been developed which control data transfers between the Processor and the I/O Subsystem on the 24-bit I/O data exchange. Each cycle consists of a phase A and phase B portion. As a software requirement, each phase A portion of a cycle must be followed by phase B portion of the cycle in order to successfully operate an I/O Control. During the phase A portion of any of the seven cycles, Command Active (CA) will be true for one clock period. CA is true during S1 time of the sequential timer.

During the phase B portion of any cycle, Response Complete (RC) will be true for one clock period. RC is also true during S1 time of the sequential timer. CA is generated during S1 time when either the 1C or 2C Micro is executed and CMND is sink. RC is generated during S1 time when either the 1C or 2C Micro is executed and DATA is sink, or when the 1C or 2C Micro is executed and DATA is source. The following timing diagram, Figure II-3 illustrates the basic relationship between the Micro in the M-Register, the time the "data" is on the I/O Bus and the time when either CA or RC is true.

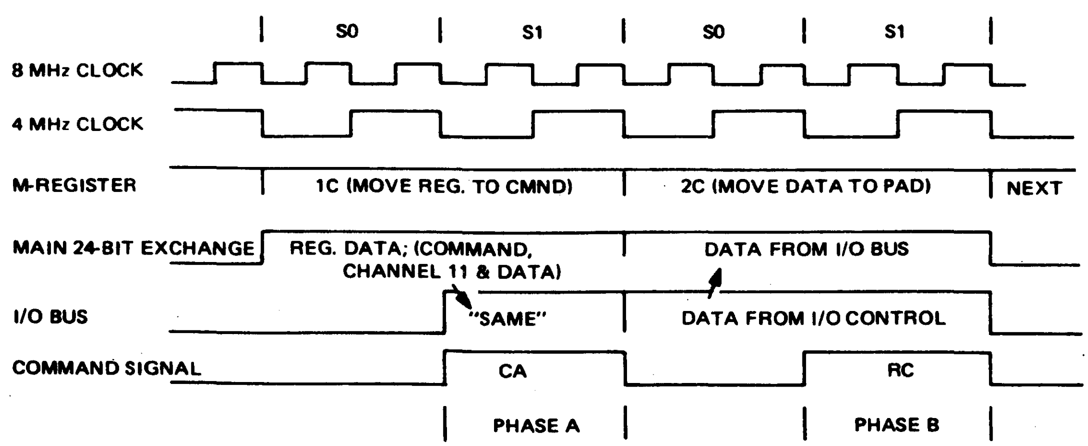


Fig. II-3 XFRONT PHASE A, COMMAND TYPE

EXECUTION

When the 1C Micro is executed in Figure II-3, the data in the Register which is moved to CMND determines that the cycle type is XFROUT Phase A type. The 24-bits of data gated to the Main 24-bit Exchange during the time the 1C Micro is in the M-Register will contain the information shown in Figure II-4 (Assuming a XFROUT Phase A type) MSB of MEX (Bit 23)

LSB of MEX (Bit 00)

0 0 1 0 X X X X d d d d d d d d d d d d d d d d

D = Data Bits

Data Bits (the 8 LSB of this data could contain the 8 MSB of the OP-Code.

X indicates the number of the Channel designated to receive the command.

0 0 1 0 indicates the cycle type is XFROUT PHASE A.

Fig. II-4

When CA is true, the Main Exchange data is then gated to the 24-bit I/O Bus as shown. The particular I/O Control is designated to receive this command will then receive the same when CA is true. The execution of the 1C Micro in Figure II-3 illustrates only the ØA portion of a two phase cycle required. Following the 1C Micro with the 2C Micro or another 1C will complete the cycle. The execution of the 2C Micro is considered ØB of the XFROUT A type cycle. The 2C Micro when executed will move DATA (the 24-bits of information on the I/O Bus, which is also gated to the Main 24-bit Exchange) to a word of Scratch Pad. The 24-bits of information on Main Exchange from the I/O Device will contain because the cycle type is XFROUT A, the Status Count of the particular I/O Control which received the initial command. The information on the Main Exchange is shown in Figure II-5.

MSB of MEX (Bite 23) LSB of MEX (Bit 00)

n n n S S S S S n n n n n n n n n n n n n n n n

n = No Significance

S = Status Count of the I/O Device.

Fig. II-5

The cycle type is therefore determined by the bit configuration of the information on the Main 24-bit Exchange when either the 1C or 2C Micro is executed and CMND is the sink. Figure II-6 illustrates the seven types of cycles designated, only six of which are used at present. Each cycle has both a Phase A and Phase B portion; CA is true during S1 time of the Phase A portion and RC is true during the S1 time of the Phase B portion. All I/O Controls provide the logic to decide the bit configuration received on the I/O Bus and therefore determine the particular type of command designated by the Processor during ØA time. As the result of this decoding, each I/O Control will respond appropriately to the command during ØA time as well as during ØB time. The six cycle types used are defined as follows: Refer to Figure II-6.

XFROUT A — During ØA time, the MSB of the I/O Bus will contain 0 0 1 0, which indicates a XFROUT. The next four bits will indicate the Channel Number of the I/O Control designated to receive the command. The 16 LSB of the I/O bus can contain up to 16-bits of data from the Processor (e.g., in the case of the SPO Control, bits 07 thru 00 can contain Byte 1, of the OP-Code, bits 15 thru 08 would have no significance at this time).

COMMAND TYPE	PHASE	SIGNAL	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
XFROUT A	OA	CA	0	0	1	0	C	C	C	C	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
	OB	RC	X	X	X	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
XFROUT B	OA	CA	0	0	1	1	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NOT USED AT PRESENT
	OB	RC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
XFRIN	OA	CA	0	1	0	0	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
	OB	RC	X	X	X	S	S	S	S	S	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
TEST STATUS	OA	CA	0	0	0	1	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	
	OB	RC	X	X	X	S	S	S	S	S	X	X	X	X	X	X	X	X	X	I	I	I	I	I	I	X	
CLEAR & TEST STATUS	OA	CA	0	0	0	1	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	
	OB	RC	X	X	X	S	S	S	S	S	X	X	X	X	X	X	X	X	X	I	I	I	I	I	I	X	
TEST SERVICE REQUEST	OA	CA	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1	
	OB	RC	X	X	X	X	X	X	X	X	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	
TERMINATE DATA	OA	CA	0	0	0	1	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0	
	OB	RC	X	X	X	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

C = CHANNEL NUMBER
D = DATA
X = NO SIGNIFICANCE
S = STATUS COUNT
I = IDENTIFICATION NUMBER OF CONTROL
M = MASK BIT (ONLY ONE BIT WHICH CORRESPONDS TO THE CHANNEL NUMBER)
0 & 1 = I/O BUS 23 THROUGH 20 (BASIC COMMAND)
I/O BUS 03 THROUGH 00 (SUB COMMAND WHEN BASIC COMMAND = 0 0 0 1)

NOTE: DURING THE OB PORTION OF A CYCLE (RC TIME) BIT 21 = 1 INDICATES READ REVERSE TO THE I/O DRIVER ROUTINE. THIS IS TRUE ONLY WHEN THE STATUS IS RETURNED.

Fig. II-6 I/O BUS (COMMANDS, DATA TRANSFER & SIGNALS)

During ØB time, the I/O Control gates the Status Count to bits 16 thru 20 of the I/O Bus. When RC is true at S1 time, it signals the Control to remove the Status Count information from the I/O Bus. The control generates to 5 during phase B time.

XFROUT B

Not Used, although some controls check for its absence.

XFRIN

During ØA time, the four MSB of the I/O Bus will contain 0 1 0 0, which indicates XFRIN. The next four bits indicate the Channel designated to receive the command. The 16 LSB are not used.

During ØB time, up to 16-bits of data is gated to the I/O Bus from an I/O Control plus the five Status Bits are also sent. RC true again signals the Control to remove data from the I/O Bus. Pos is true during phase B time.

TEST STATUS

During ØA time, the four MSB of the I/O Bus will contain 0 0 0 1 and the four LSB of the I/O Bus will contain 0 0 0 1, which indicates TEST STATUS. Note that four of the cycle types require the four MSB of the I/O Bus to contain 0 0 0 1. It is in these cases that the command variants (bits 03 thru 00) of the I/O Bus will determine the type of cycle. The Channel Number of the I/O Control is designated by bits 19 thru 16 and bits 15 thru 04 are not used.

During ØB time, the I/O Control designated to return the TEST STATUS will return the following to the Processor via the I/O Bus. Five bits of Status and six Control Identification Bits. Each Control has its own ID. RC true signals the Control to remove data from the I/O Bus. IOS is true during phase B time.

CLEAR & TEST STATUS — During ØA time, the four MSB of the I/O Bus will contain 0 0 0 1 and the four LSB will contrain 0 0 1 1, which indicates CLEAR & TEST STATUS. Bits 19 thru 16 designate the Channel and bits 15 thru 04 are not used.
During ØB time, the I/O Control transmits to the Processor, the current Status to which it has been switched. At the end of Phase B time the control designated is cleared to reset condition. It also transmits the Device Type (ID) as in the TEST STATUS cycle. RC signals control the same. IOS is true during phase B time.

TEST SERVICE REQUEST — During ØA time, the four MSB of the I/O Bus will contain 0 0 0 1 and the four LSB will contain 0 1 0 1 which indicates TEST SERVICE REQUEST. All other bits are not used.
During ØB time, Each I/O Control connected to the I/O Bus responds by sending a bit corresponding to its Channel Number if the I/O Control is requesting service by the Processor. Channel 08 will send a bit on bit 08 of the I/O Bus, Channel 03. . . .bit 03 of the I/O Bus. . .etc. RC is the same. IOS is true during phase B time.

TERMINATE DATA — During ØA time, the four MSB of the I/O Bus will contain 0 0 0 1 and the four LSB of the Bus will contain 0 1 1 0 which indicates TERMINATE DATA. Bits 19 thru 16 designate the Channel to which the command is designated. The terminate Data command signals a Control capable of receiving variable length data that the last of the record has been transmitted.
During ØB time, the status is transmitted to the Control. IOS is true during phase B time.

I/O CONTROL STATES

Control operations are completed by following a standard set of 23 states or conditions. These state sequences will be different for input devices than output devices, and for variable record length devices versus fixed record length devices. However, two fixed record output devices will follow the exact same path. These states are used within the Processor (by use of the I/O Driver Routine) to trace the Control.

STATE COUNT 0 (00000): "NOT READY" (Control not present)

STATE COUNT 1 (00001): READY. Ready to receive the first transmission from the processor, OP-code byte 1.

STC 2 (00010): Ready to receive OP-code byte 2.

STC 3 (00011): Ready to receive OP-code byte 3.

STC 4 (00100): Ready to receive File Address byte 1.

STC 5 (00101): Ready to receive File Address byte 2.

STC 6 (00110): Ready to receive File Address byte 3.

STC 7 (00111): Ready to receive Reference Address byte 1.

STC 8 (01000): Ready to receive Reference Address byte 2.

STC 9 (01001): Ready to receive Reference Address byte 3.

STC 10 (01010): BUSY. Control has accepted instructions and is performing the operation. Usually, upon completion of the operation, the control switches to a different status and transmits Service Request to the processor.

STC 11 (01011): Ready to transmit Reference Address byte 1. (In preparation for data transfer, either input or output.)

STC 12 (01100): Ready to transmit Reference Address byte 2.

STC 13 (01101): Ready to transmit Reference Address byte 3.

STC 14 (01110): Ready to receive one byte of data (two bytes for certain types of control).

STC 15 (01111): Ready to transmit one byte of data (two bytes for certain types of control).

STC 16 (10000): Ready to receive or transmit last byte of data in current buffer load, with additional buffer load to follow.

STC 17 (10001): Ready to receive or transmit last byte of data in last buffer load (including single buffer load devices).

STC 18 (10010): Ready to transmit Reference Address byte 1 (in preparation to transmit Result Descriptor and to end cycle).

STC 19 (10011): Ready to transmit Reference Address byte 2.

STC 20 (10100): Ready to transmit Reference Address byte 3.

STC 21 (10101): Ready to transmit Result Descriptor byte 1. (Transmission of Result Descriptor is always last action of a sequence.)

STC 22 (10110): Ready to transmit Result Descriptor byte 2.

STC 23 (10111): Ready to transmit Result Descriptor byte 3, which ends the sequence. The control then switches to status zero and will go automatically to one.

Table II-1

BASIC COMMANDS

0010	Transfer Out Phase A
0011	Transfer Out Phase B (Not significant)
0100	Transfer In
0001	Control Variant (Command is defined in EXCH bits 00-03)

LSB COMMAND bit is EXCH bit 20
MSB COMMAND bit is EXCH bit 23

Table II-2

CONTROL VARIANTS

(Only significant if Basic Command = Control Variant)

0001	Test Status
0011	Clear and Test Status
0101	Test Service Request-Channel
0110	Terminate Data

LSB VARIANT bit is EXCH bit 00
MSB VARIANT bit is EXCH bit 03

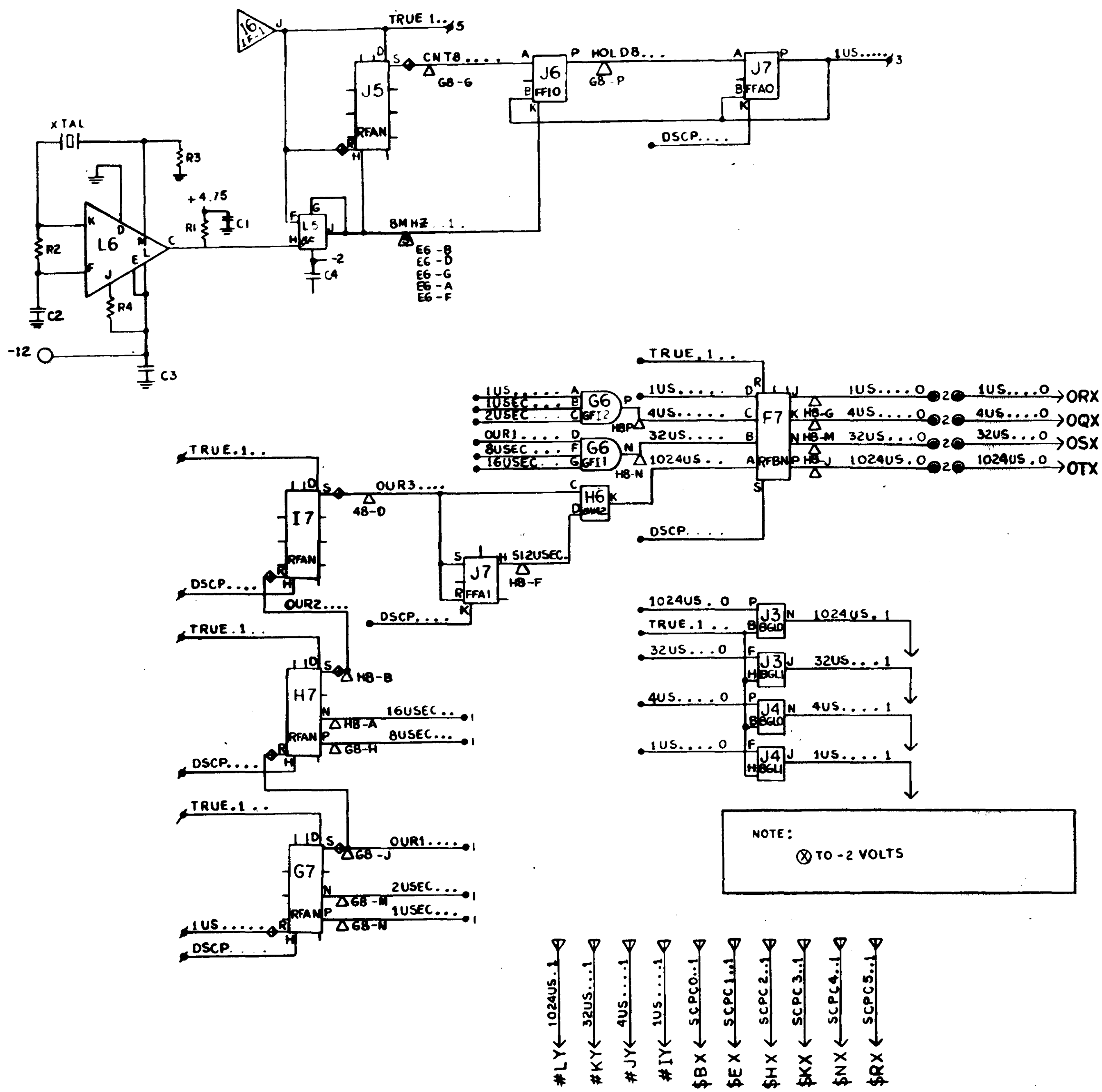


Fig. II-7 DISTRIBUTION CARD SLOW CLOCK GENERATION

The Distribution Card distributes five clocks to the I/O Base Backplane. These are 4mhz (scpm. . .0), lus.˙. . .0, 4us. . . .0, 32us. . .0 and 1024 us.0. In addition, these are sent out the frontplane to a Subdistribution Card.

Figure II-7 shows the clock generation circuit. An 8 mhz crystal oscillator drives the Video Amp at location L6. The Video Amp Output is inputed to Buffer L5. This output called 8mhz. . .1. goes to J5 and J6. J5 is a FRAN 3 bit register Chip. J5 is held in the add mode by the true level on pin D. The carry in is tried true also (pin R). In this mode the chip acts as a counter. A carry out will occur every eight 8mhz. . .1. clock pulses and lasts for a clock period. This carry out is inputed to F/F J6. J6 provides a "hold" for one more 8mhz. . .1. period. This Hold 8. . . level is inputed to J7 where it is synced with DSCP. . . . (System Clock). The output of this F/F is called 1us. . . . . . This clock is sent out the backplane as lus. . . .0 and to chip G7. G7, H7, and I7 work in a similar manner to J5. These chips are held in the add mode with carry in held high. This results in a binary add of the lus clock. 512 clocks are required to progate through the three chips. 1024us. . , 32us. . . . , and 4us. . . . . are generated by gating adder levels at G6. Figure II-8 shows the timing of these clocks.

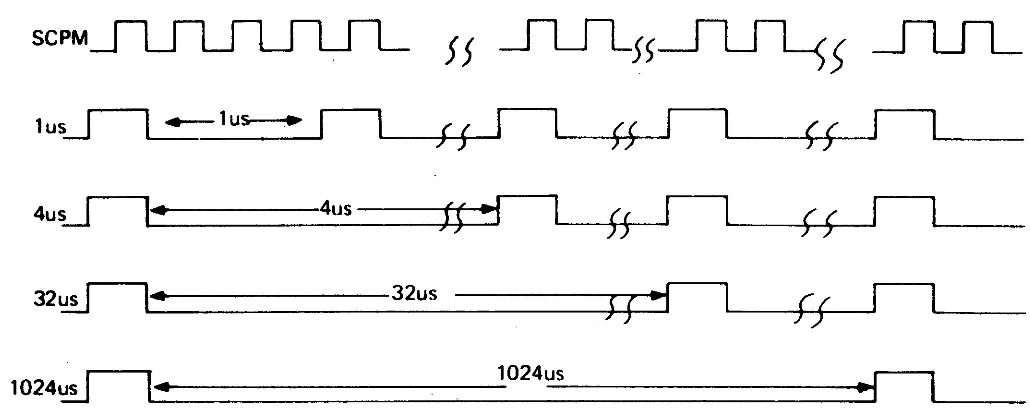


Fig. II-8 I/O BASE CLOCK TIMING

INTRODUCTION

This section provides information to adjust the I/O Base or I/O Base Extension Clock.

I/O BASE CLOCK ADJUSTMENT

The purpose of this adjustment is to adjust the clock at the I/O Base backplane to occur 25 nanoseconds late (+ 7ns) in relation to the system clock. System clock will be referenced at Card K, pin OXX for a B1712 or B1714. On a B1726, the system clock reference is pin OWX of memory control card B.

The clock sent to the I/O Base is an early clock. In a B1712/B1714 this clock is received from K card and is actually the 4Mhz/ clock delayed. In the B1726, early clock is obtained by an output on the clock module assembly.

CLOCK ADJUSTMENT PROCEDURE

Refer to Figures IV-1 through IV-7 and Table IV-1.

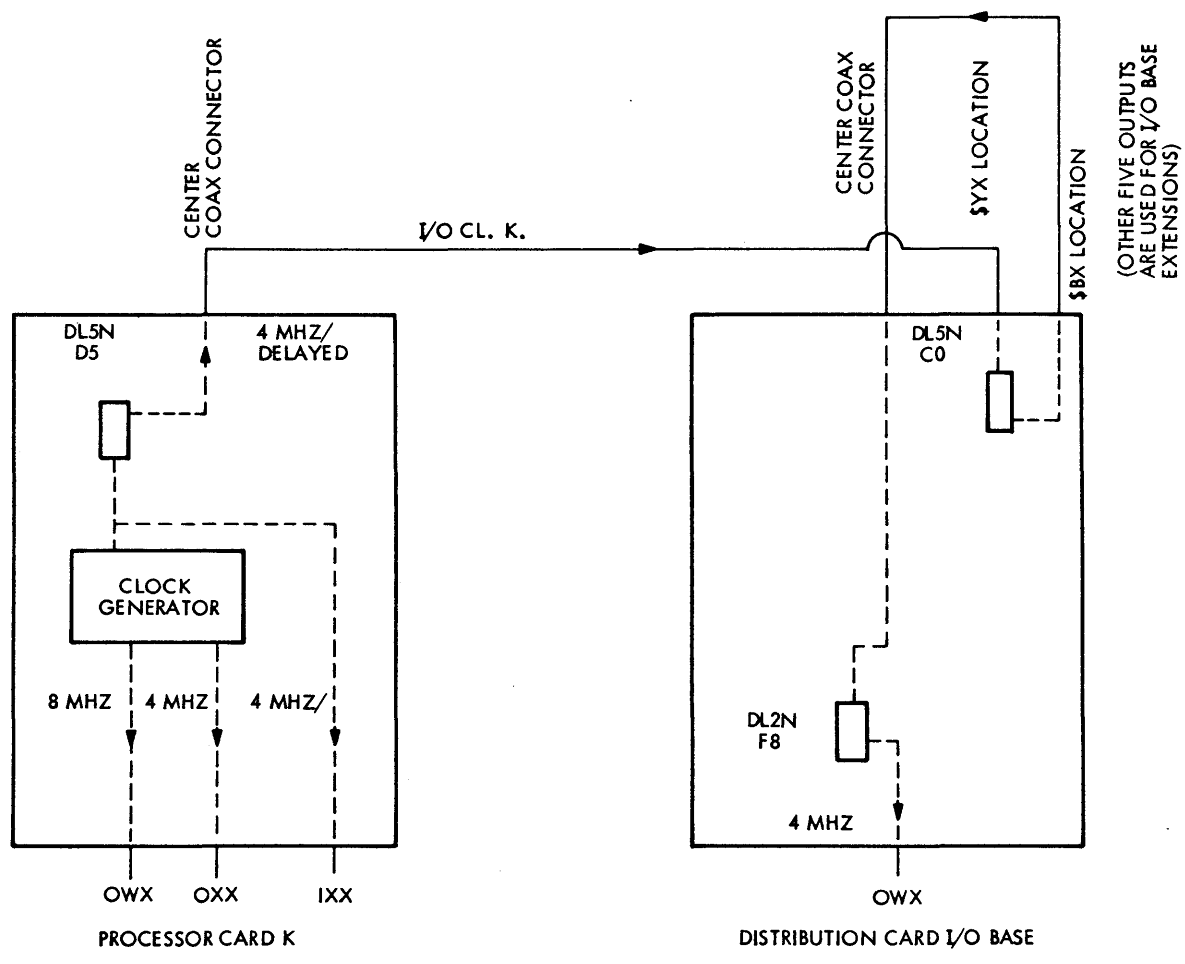


Fig. IV-1 B1714 CLOCK PATH

1. Extend the distribution card.

2. Assure that a standard clock coax connects the clock doghouse $YX of the distribution card to either card K for a B1712/B1714 or to an early clock output of the clock module assembly for a B1726.

3. Set up an oscilloscope as follows:

   Vertical: .lv/cm (using X10 probes)
   Horizontal - .lus/cm (100ns)
   Channel 1 - CLK..KO (Card K, pin OXX) for a
   B1712/B1714. SCPM..BO (Memory control Card B,
   pin OWX for a B1726)
   Channel 2 - refer to text
   Mode - Alternate
   Trigger - channel 1

4. Check scope probes and preamps by placing channel 2 probe on the same clock pin as channel 1 and overlaying the two traces. Place X10 mag. on. Traces should be identical.

5. Using the horizontal control, position the channel 1 trace to have the 1 volt level cross the center cross-hairs. Do the same for channel 2.

6. Place the channel 2 probe on chip F8G. Connect a standard 4-foot clock coax from one of the six clock output doghouses ($BX, $EX, $HX, $KX, $NX, $RX) to the center doghouse connector.

   The two clock traces will be overlayed as shown in Figure IV-2.

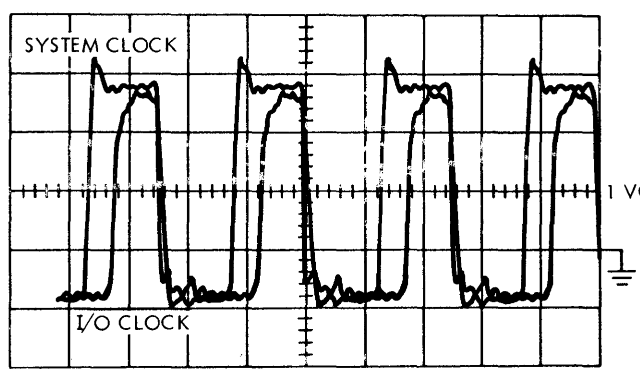


Fig. IV-2 SYSTEM CLOCK + I/O CLOCK (F8G) 100ns/cm

Turn on the X10 mag., using the horizontal control; position the trailing edge of the system clock on the center crosshair. Refer to Figure IV-3.

7. The trailing edge of the channel 2 input referenced to the trailing edge of the channel 1 (system clock) input should be from 5ns early to 10ns late.
   To adjust the clock at F8G, there are two different procedures, depending if the distribution card is of the wire-wrapped type or the etched type.

   a. For the wire-wrapped board, move the tap for net SCPED1.. on delay line CO. This is the wire going to BOB.

b. For the etched board, jumper chip BO controls the delay taps of CO. Pin R is the SCPED... output of the jumper chip and will be connected to either E, F, G, H or J.

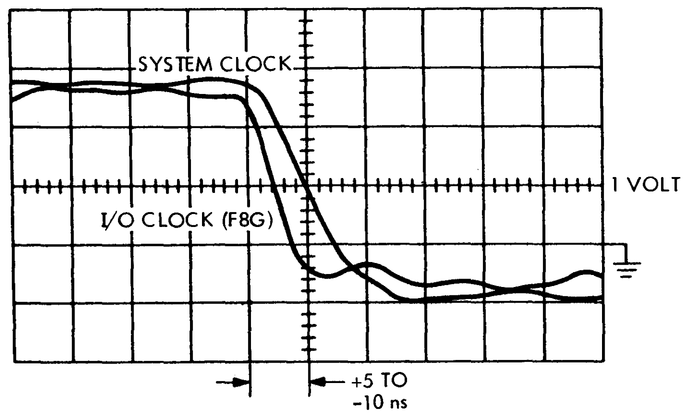


Fig. IV-3 SYSTEM CLOCK + I/O CLOCK (F8G) 10ns/cm

Alternately move the input clock to each of the six output doghouses. Check that they are all in spec.

8. The next step is to check the pulse width of the clock at F8G. The minimum pulse width is 40ns. The maximum pulse width is as follows:

   B1712 - 160ns
   B1714 - 80ns
   B1726 - 60ns

The pulse width is measured at the lv level. With the X10 mag on, use the horizontal control to position the clock at F8G to measure the pulse width. With a B1712, go to 20ns/cm. Refer to Figure IV-4.

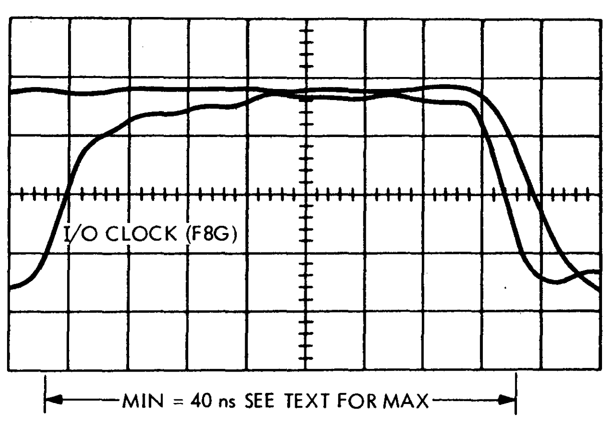


Fig. IV-4 I/O CLOCK PULSE WIDTH AT F8G (10ns/cm)

The pulse width is controlled by Delay chip CO. It is adjusted as follows:

1. For the wire-wrapped board, move the top SCPED2.. on delay CO. This is the wire going to BOP. Note that pins N and P are connected together. If the tap to BOP is moved off, on, or onto these pins, leave N to P connected.

2. For the etched board, jumper chip BO controls the taps of CO. Pin S is the SCPED2.. output of the jumper chip and will be connected to either pin B, C, D, L or M.

Alternately move the input cable (SCPS....) to each of the six output doghouses (SCPMA's). Check that they are all in spec.

a. Connect the 4-foot clock coax from the center doghouse (SCPS....) to one of the six output doghouses (SCPMn's). This will be the permanent connection for the system.

b. Using system clock for a reference, check pin OWX of each occupied card slot in the I/O Base. Measuring trailing edge to trailing edge, the I/O clock should be 25 + 7ns late. Use Figures IV-5 and IV-6 for reference.

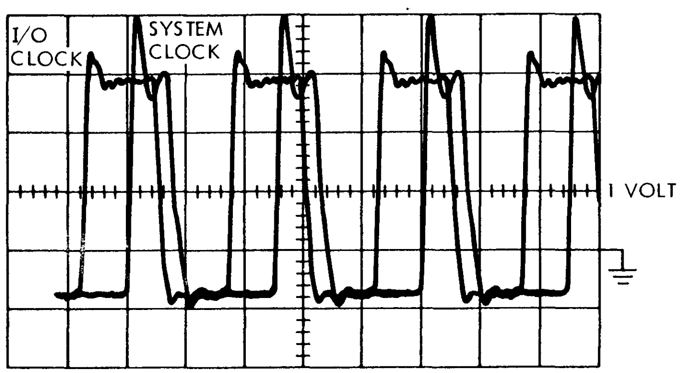


Fig. IV-5 SYSTEM CLOCK + I/O CLOCK 100ns/cm

c. To adjust the backplane clock, do the following:

   1. On the wire-wrapped board, move the tap on delay line F8. This is net SCPD.... going to F9P.

   2. On the etched board, jumper chip E8 controls the delay taps of F8. Pin R is the output of the jumper chip and will be jumped to either pin B, C, D, E, F, G, H, J, L or M.

I/O BASE EXTENSION CLOCK ADJUSTMENT

Use the Backplane Adjustment called out under Backplane Adjustment paragraph. The chip locations on the subdistribution card are the same as for the distribution card.

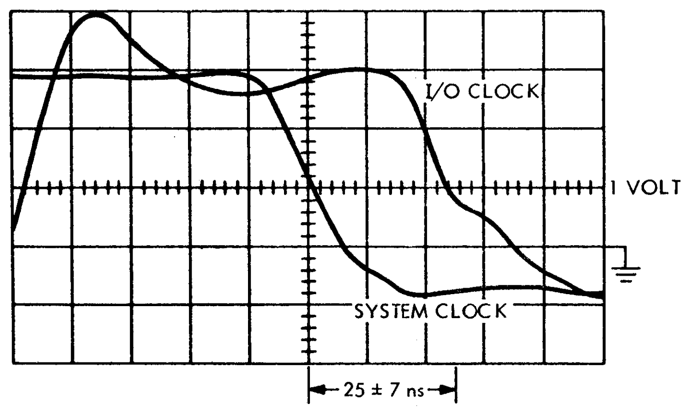


Fig. IV-6 SYSTEM CLOCK + I/O CLOCK 10ns/cm

Table IV-1

DLCN - CO		DL2N - F8	
Pin G Input		Pin G Input	
Tap	Delay	Tap	Delay
Pin H	10 ns	Pin H	2 ns
F	20	F	4
J	30	J	6
E	40	E	8
D,K	50	D,K	10
L	60	L	12
C	70	C	14
M	80	M	16
B	90	B	18
N	100	N	20

#Y

Control lines and slow clocks to subdistribution card.

A	RC 1	I	1US. . . . 1	R	
B	CA 1	J	4US. . . . 1	S	
C	CLRB . . . 1	K	32US. . . 1	T	
D	SR 1	L	1024US. 1	U	
E	PWRON. . 1	M		V	
F		N		W	
G		P		X	
H	8 MHZ. . . 1	Q		Y	
				Z	

Unique 16 Conductor Connector

Unique 16 conductor connector located at chip position JO actually a chip socket

Control levels to processor card C

A	not used	P	not used
B	RC 1	N	ground
C	CA 1	M	ground
D	CLRB. . . 1	L	ground
E	SR 1	K	ground
F	PWRON . 1	J	ground
G	not used	H	not used
R	not used	S	not used

Subdistribution Card Frontplane Connectors

$X

Exchange Lines to Distribution Card

A	EXCH.001	I	EXCH.081	R	EXCH.161
B	EXCH.011	J	EXCH.091	S	EXCH.171
C	EXCH.021	K	EXCH.101	T	EXCH.181
D	EXCH.031	L	EXCH.111	U	EXCH.191
E	EXCH.041	M	EXCH.121	V	EXCH.201
F	EXCH.051	N	EXCH.131	W	EXCH.211
G	EXCH.061	P	EXCH.141	X	EXCH.221
H	EXCH.071	Q	EXCH.151	Y	EXCH.231
				Z	SPARE1.1

#X

Exchange Lines to Another Subdistribution Card

A	EXCH00.1	I	EXCH08.1	R	EXCH16.1
B	EXCH01.1	J	EXCH09.1	S	EXCH17.1
C	EXCH02.1	K	EXCH10.1	T	EXCH18.1
D	EXCH03.1	L	EXCH11.1	U	EXCH19.1
E	EXCH04.1	M	EXCH12.1	V	EXCH20.1
F	EXCH05.1	N	EXCH13.1	W	EXCH21.1
G	EXCH06.1	P	EXCH14.1	X	EXCH22.1
H	EXCH07.1	Q	EXCH15.1	Y	EXCH23.1
				Z	SPARE.11

Maintenance Procedures

INTRODUCTION

The purpose of this section is to provide directions and aids in maintaining the I/O Base and the I/O Base Extension.

PREVENTIVE MAINTENANCE

The 4 mhz I/O clock adjustment should be checked every three months. Refer to I/O Base Section IV for the clock procedure.

SPECIAL MAINTENANCE TOOLS REQUIRED

I/O control test routines
B 1700 field card tester
Tektronix 453A oscilloscope or equivalent
Tripplet 630 VOM or equivalent

MAINTENANCE CONCEPT

B 1700 controls are soft controls. No outline capability is built into the control. The B 1700 Maintenance Concept is centered around the use of test routines used in conjunction with the Field Card Tester. Hardware test points are provided for conventional trouble shooting.

TEST ROUTINES

The I/O Base with the Distribution Card is transparent to test routines. Therefore, the I/O Base and distribution card must be tested with an I/O Control. For the particular control used, run the controls confidence routine.

TEST PROCEDURES

It is assumed that troubleshooting the I/O Base implies a failure of one or more I/O. I/O Base Troubleshooting should follow these basic steps:

Visual Checks (Refer to I/O Base Section VI)

1. Assure that the distribution card and all controls are loaded into valid slots.
2. Assure that the I/O Base cabling to processor and control cabling to peripherals is proper.
3. Assure that all controls have channel number jumper chips installed and that no two controls have the same number.
4. Assure that the terminator chips for the I/O Base Control lines are installed in the proper locations of the distribution card or subdistribution card if used.

Voltage Checks

Check voltage on the I/O Base backplane.

Table V-1

Backplane Pin	Voltage
OAX, 1AX	+4.75v
OZX	-12v
1AY	-12v
1LY	+12v
OZY, 1ZY	-2v

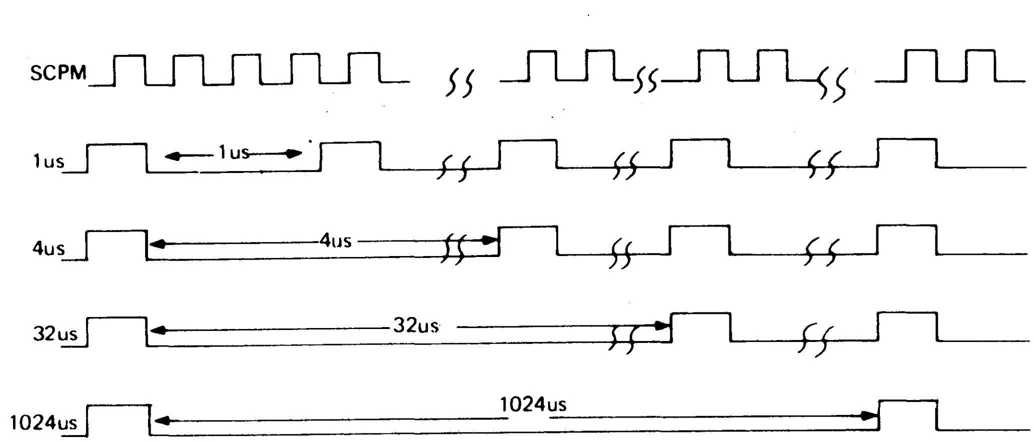


Fig. V-1 I/O BASE CLOCK TIMING

Clock Checks

I/O Base Backplane carries 5 clocks: 4mhz, 1024 μs, 32 μs, 4 μs and 1 μs. Table V-2 shows the pin locations of the clocks on the Distribution Card slot, backplane locations A0 and A1. The Distribution Card slot is unique because it brings out system clock on 10 pins. Pin XAOW is for reference only. Pin XOW is SCPM on all other backplane connectors.

Check each pin in table V-2 for the proper clock. Refer to Figure V-1 for proper timing.

Display XAOW on channel one of a 453 scope. Sync on this channel.

Channel two will be connected to the backplane pins listed in Table V-2.

Table V-2

DISTRIBUTION CARD CLOCK OUTPUTS

Backplane Pin	Mnemonic	Type Clock
XAOW	SCPM. . .0	4mhz
XAOY	SCPM0. .0	4mhz
XA1Y	SCPM1. .0	4mhz
XAOX	SCPM2. .0	4mhz
XA1X	SCPM3. .0	4mhz
XAOV	SCPM4. .0	4mhz
XA1V	SCPM5. .0	4mhz
XAOU	SCPM6. .0	4mhz
XA1V	SCPM7. .0	4mhz
XA1T	SCPM8. .0	4mhz
XAOQ	4us 0	4 μsec
XAOR	1us 0	1 μsec
XAOS	32us . . . 0	32 μsec
XAOT	1024us . 0	1024 μsec

Test Distribution Card

For problems not resolved by the previous steps, the Distribution Card should be tested in the B 1700 Field Card Tester. Refer to the B 1700 Field Card Tester manual.

If problem is found and repaired, reinstall distribution card in the I/O Base and connect frontplane cables. Run all I/O confidence routines.

If card checks OK in the tester or the problem cannot be resolved with the tester, reinstall the Distribution Card in the I/O Base. Connect frontplane cables. Proceed to I/O. Debug routine paragraphs.

I/O DEBUG ROUTINE

GENERAL

Figure V-2 is a breakdown of the Processor to I/O flow. The I/O Debug Routine is a basic routine that follows the path shown in the figure. This routine may be used for any I/O Control. The OP Code and control channel number have to be manually loaded. The instructions on the program listing give the FA value where these commands are placed.

STEPPING

By stepping this program 1 micro at a time, the Field Engineer can observe hardware testpoints and determine the internal SPO Control Operation.

Each time this program sends out a basic command to the I/O it will read in the status of the 24 exchange lines to the L Reg. By displaying L at the proper time the Field Engineer can observe what status count the control is at and what data is returned to the processor. By looking at T Reg. at the proper time the FE can observe the commands and data sent to the control.

USING HALTS

Figure V-2 shows the basic sub-routines within the boxes. For example, send OP Code is a sub-routine. The Debug Program has no-op micros placed between sub-routines and within certain routines. These allow the Field Engineer to manipulate the program to his liking. For example, a halt could be put after the 1st byte of REF ADD has been transferred to the control. The Field Engineer could then check at the storage buffer in the control for this byte of data. Another example would be placing a halt after the first result Descriptor Byte is transferred in. The L Reg could then be checked for the data.

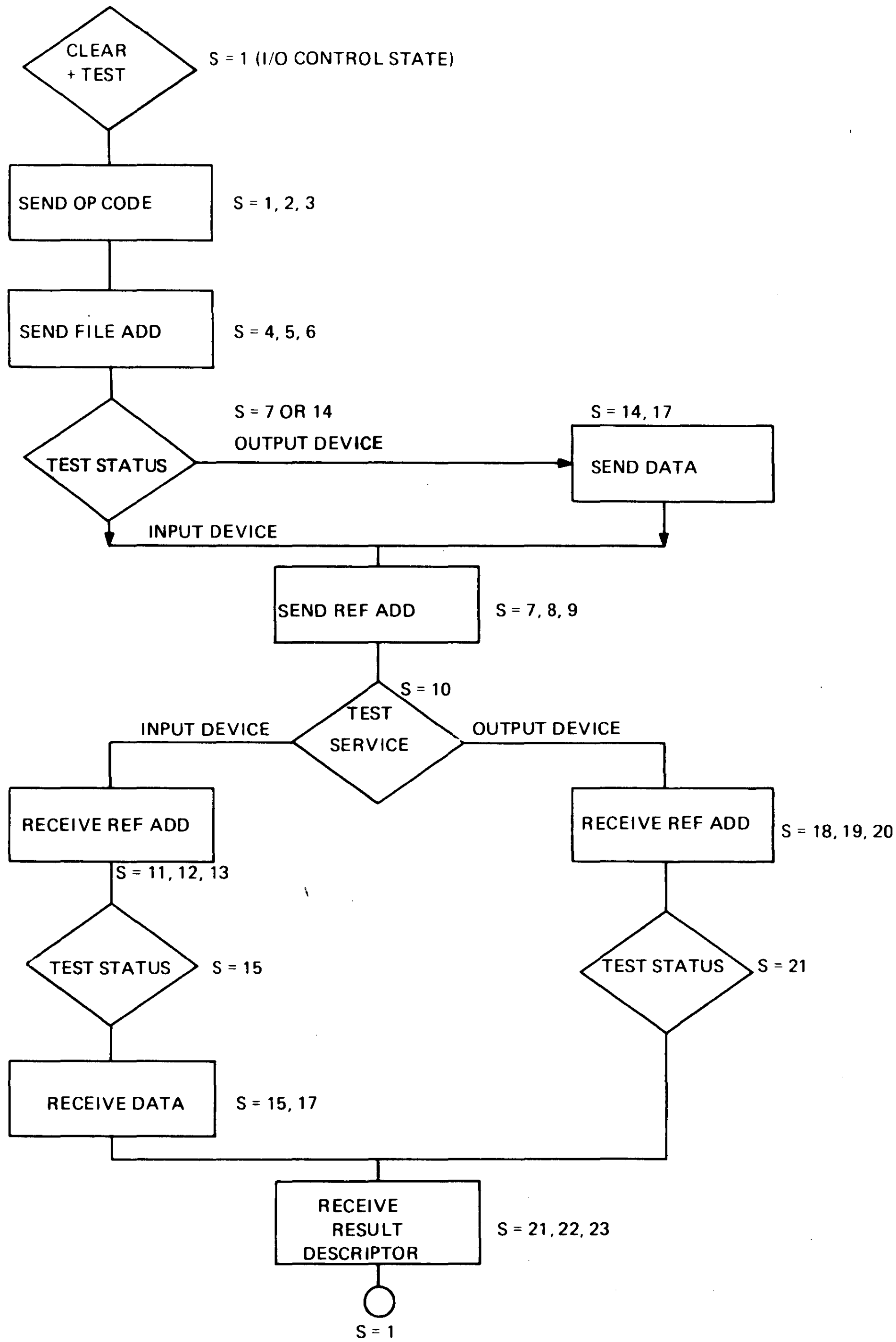


Fig. V-2 PROCESSOR TO I/O FLOW

USE OF I/O DEBUGGING ROUTINE

The Distribution Card is basically a buffer between the processor and I/O control. A Distribution Card fault should reflect itself as an improper command or invalid data.

The best method for finding the fault would be to step the program using a simple device such as SPO.

Monitor the L Reg as the exchange lines are read in. Hardware test points can be monitored on the Distribution Card or the I/O control.

HARDWARE TEST POINTS

Distribution Card Front Plane Connectors

$X

$X location is used to mount the clock connector "doghouses".
Clock connectors are listed below.

$BX Clock output. Will be connected to center coax connector of this card for distribution card clock.

$EX Clock output for subdistribution card

$HX Clock output for subdistribution card

$KX Clock output for subdistribution card

$NX Clock output for subdistribution card

$RX Clock output for subdistribution card

$YX Clock input from processor card K.

#X

Exchange lines to processor card E

A	EXCH00.1	I	EXCH08.1	R	EXCH16.1
B	EXCH01.1	J	EXCH09.1	S	EXCH17.1
C	EXCH02.1	K	EXCH10.1	T	EXCH18.1
D	EXCH03.1	L	EXCH11.1	U	EXCH19.1
E	EXCH04.1	M	EXCH12.1	V	EXCH20.1
F	EXCH05.1	N	EXCH13.1	W	EXCH21.1
G	EXCH06.1	P	EXCH14.1	X	EXCH22.1
H	EXCH07.1	Q	EXCH15.1	Y	EXCH23.1
				Z	SPARE.11

$Y

Exchange lines to subdistribution card

A	EXCH.001	I	EXCH.081	R	EXCH.161
B	EXCH.011	J	EXCH.091	S	EXCH.171
C	EXCH.021	K	EXCH.101	T	EXCH.181
D	EXCH.031	L	EXCH.111	U	EXCH.191
E	EXCH.041	M	EXCH.121	V	EXCH.201
F	EXCH.051	N	EXCH.131	W	EXCH.211
G	EXCH.061	P	EXCH.141	X	EXCH.221
H	EXCH.071	Q	EXCH.151	Y	EXCH.231
				Z	SPARE1.1

#Y

Control lines and slow clocks to subdistribution card.

A	RC 1	I	1US. . . . 1	R
B	CA 1	J	4US. . . . 1	S
C	CLRB . . . 1	K	32US. . . 1	T
D	SR 1	L	1024US. 1	U
E	PWRON. . 1	M		V
F		N		W
G		P		X
H	8 MHZ. . . 1	Q		Y
				Z

Unique 16 Conductor Connector

Unique 16 conductor connector located at chip position JO actually a chip socket

Control levels to processor card C

A	not used	P	not used
B	RC 1	N	ground
C	CA 1	M	ground
D	CLRB. . . 1	L	ground
E	SR 1	K	ground
F	PWRON . 1	J	ground
G	not used	H	not used
R	not used	S	not used

Subdistribution Card Frontplane Connectors

$X

Exchange Lines to Distribution Card

A	EXCH.001	I	EXCH.081	R	EXCH.161
B	EXCH.011	J	EXCH.091	S	EXCH.171
C	EXCH.021	K	EXCH.101	T	EXCH.181
D	EXCH.031	L	EXCH.111	U	EXCH.191
E	EXCH.041	M	EXCH.121	V	EXCH.201
F	EXCH.051	N	EXCH.131	W	EXCH.211
G	EXCH.061	P	EXCH.141	X	EXCH.221
H	EXCH.071	Q	EXCH.151	Y	EXCH.231
				Z	SPARE1.1

#X

Exchange Lines to Another Subdistribution Card

A	EXCH00.1	I	EXCH08.1	R	EXCH16.1
B	EXCH01.1	J	EXCH09.1	S	EXCH17.1
C	EXCH02.1	K	EXCH10.1	T	EXCH18.1
D	EXCH03.1	L	EXCH11.1	U	EXCH19.1
E	EXCH04.1	M	EXCH12.1	V	EXCH20.1
F	EXCH05.1	N	EXCH13.1	W	EXCH21.1
G	EXCH06.1	P	EXCH14.1	X	EXCH22.1
H	EXCH07.1	Q	EXCH15.1	Y	EXCH23.1
				Z	SPARE.11

$Y

Control Lines from Distribution Card

A	RC R1	I	1US . . . R1	R
B	CA R1	J	4US . . . R1	S
C	CLRB . R1	K	32US . . R1	T
D	SR R1	L	1024US R1	U
E	PWRON . .1	M		V
F		N		W
G		P		X
H	8mhz . . . 1	Q		Y
				Z

#Y

Control Lines to Another Subdistribution Card

A	RC 1	I	1US 1	R
B	CA 1	J	4US 1	S
C	CLRB. . . 1	K	32US . . . 1	T
D	SR 1	L	1024US . 1	U
E	PWRONI. 1	M		V
F		N		W
G		P		X
H	8mhz . . . 1	Q		Y
				Z

Maintenance Procedures

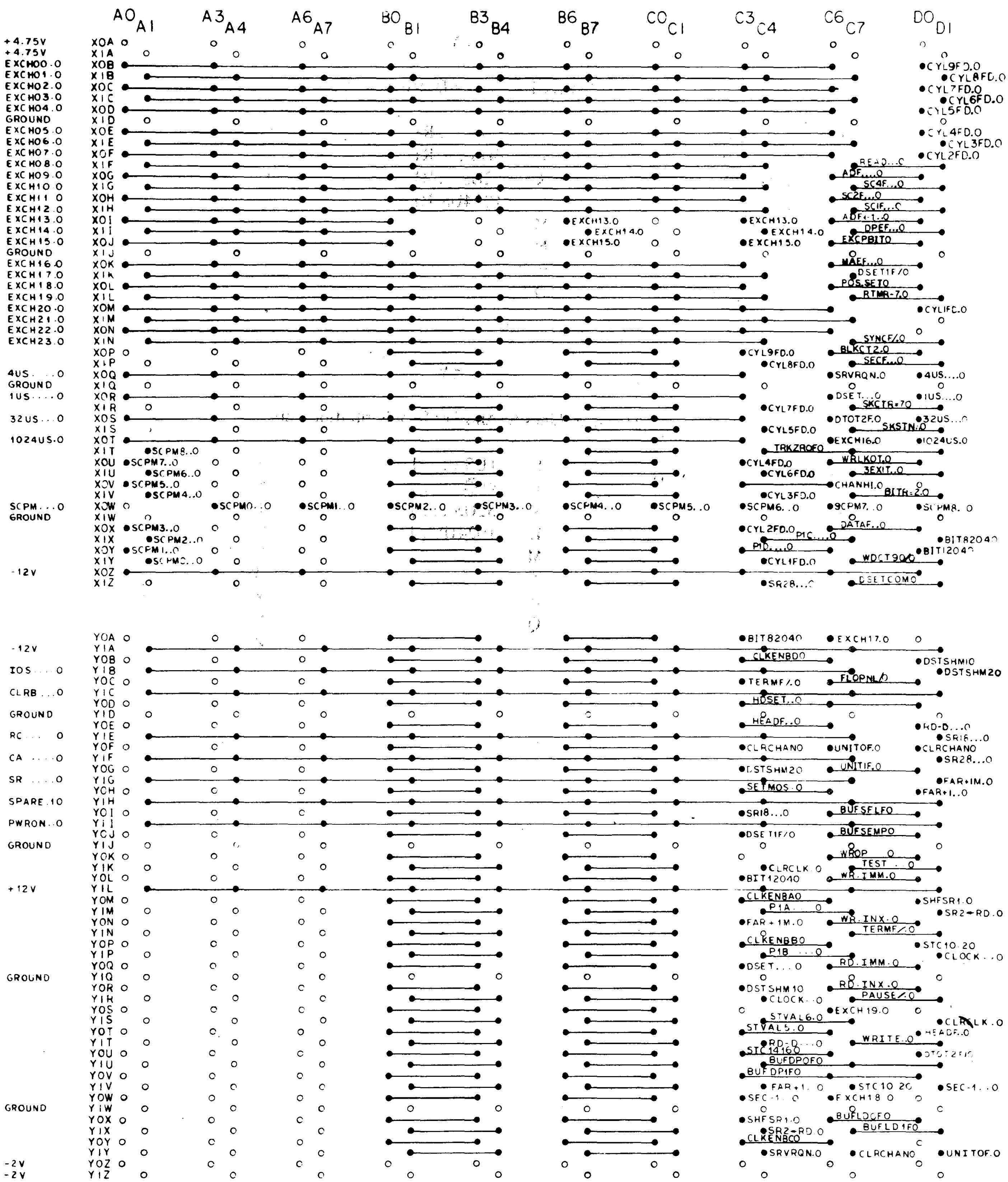


Fig. V-3 I/O BASE BACKPLANE

CLOCK GENERATOR TEST POINTS

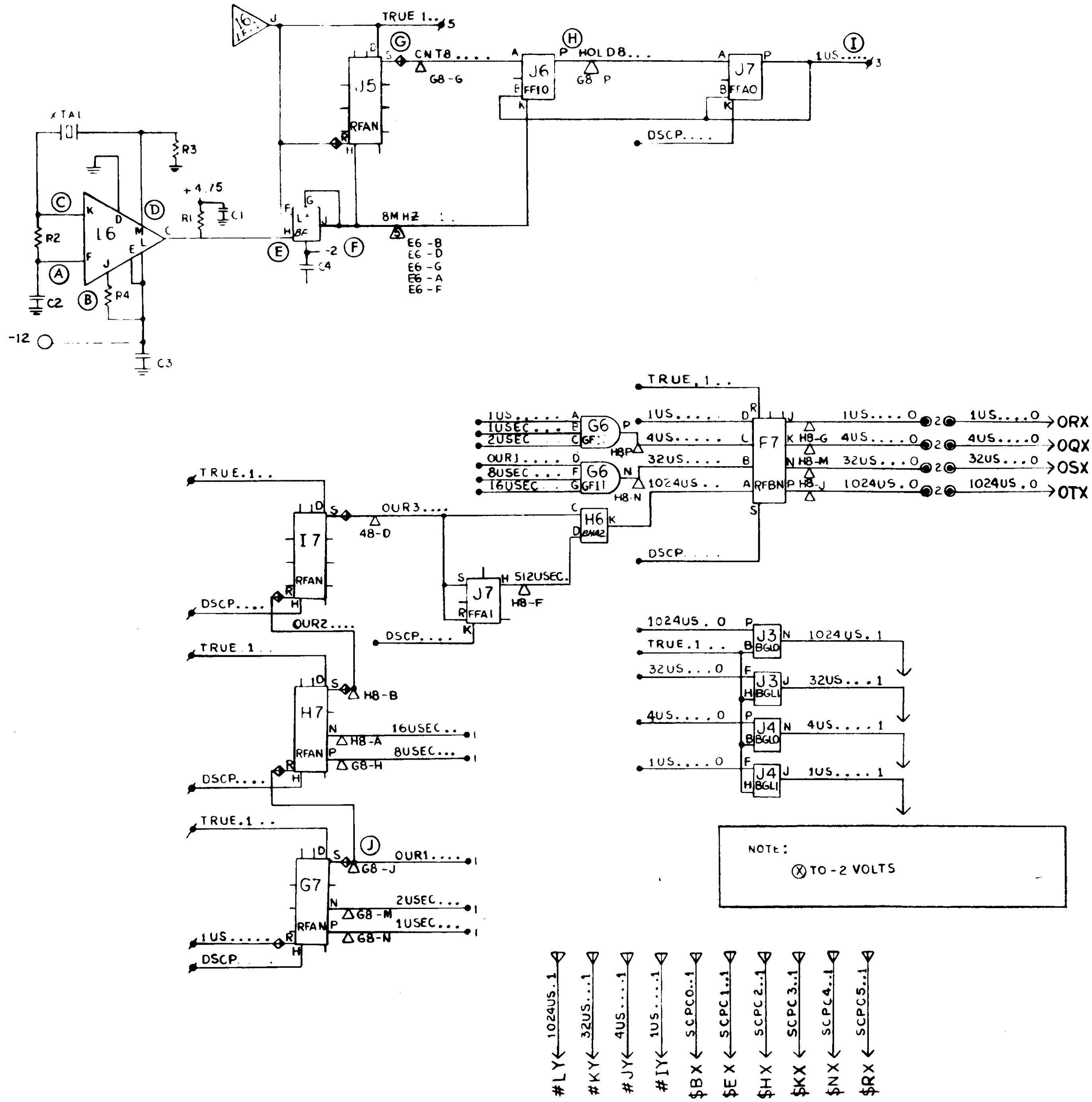


Fig. V-4

The following testpoints should enable the field engineer to troubleshoot the slow clock generator circuit on the Distribution Card.

8mhz Crystal/Video Amp

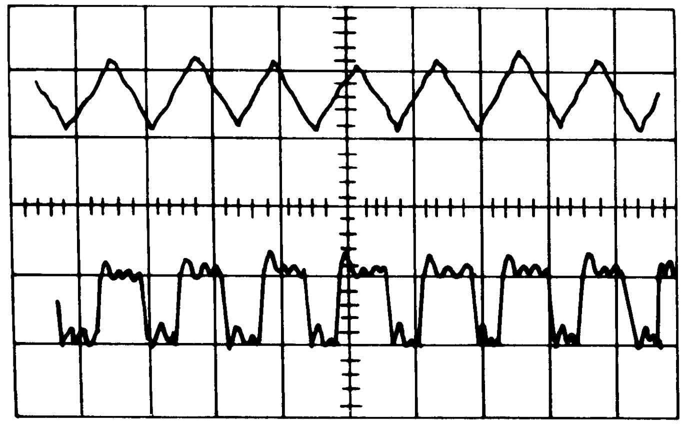
Testpoint A (L6-F) -8V

Testpoint B (L6-J) -9V

Refer to Figure V-4

Testpoint C
L6k
Channel 1
Crystal
Output

Testpoint D
L6M
Channel 2
Cyrstal Output

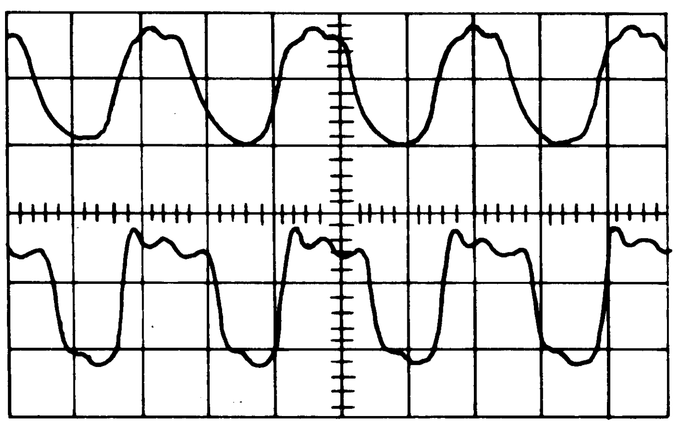


Scope Setting
Vert .2v/cm
Horz .1μs/cm

Fig. V-4A

Testpoint E
L5H
Channel 1
Video Amp
Output

Testpoint F
L5J
Channel 2
1st Buffer
Output

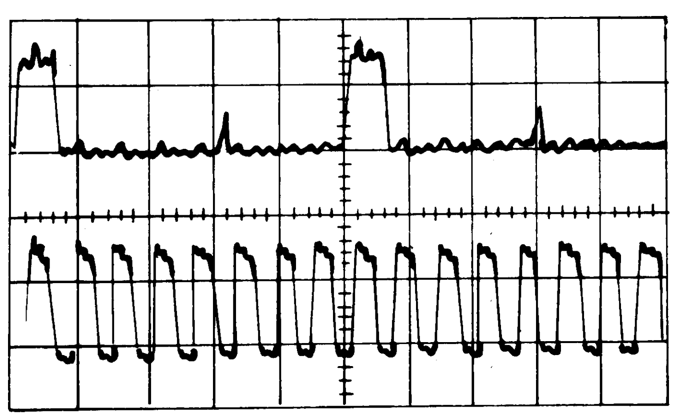


Scope Setting
Vert 2v/cm
Horz 50ns/cm

Fig. V-4B

Testpoint G
J5S
Channel 1
1mhz output

Testpoint F
J5H
Channel 2
8mhz input



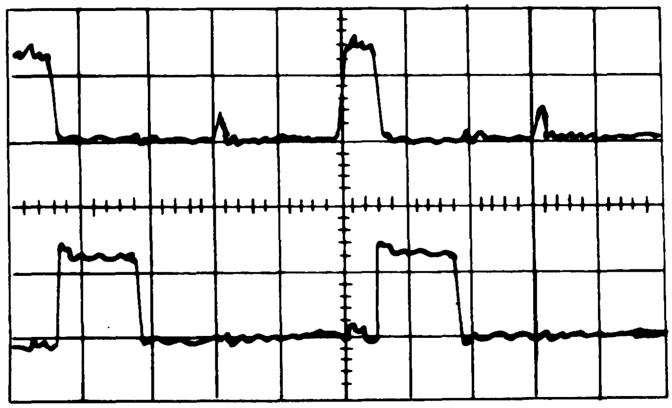
Scope Setting
Trigger ch1
Vert 2v/cm
Horz 12μs/cm

Fig. V-4C

Refer to Fig. V-4

Testpoint G
J5S
Channel 1
1mhz input

Testpoint H
J6P
Channel 2
1mhz output

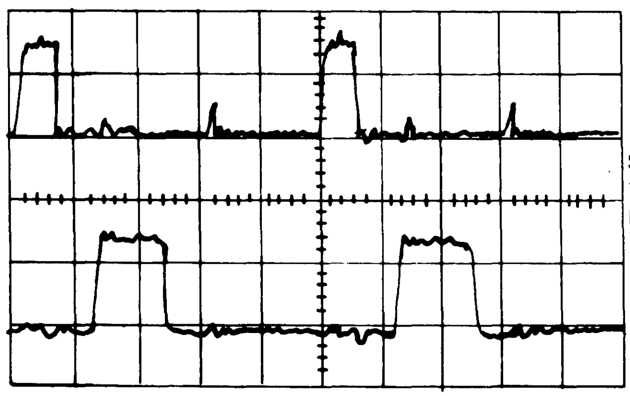


Scope Setting
Trigger ch 1
Vert 2u/cm
Horz .2μs/cm

Fig. V-4D

Testpoint G
J5S
Channel 1
1mhz reference

Testpoint I
J7P
Channel 2
1μs....

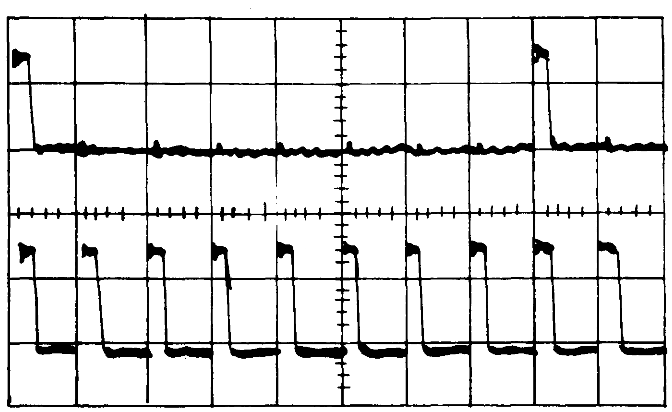


Scope Setting
Vert 2v/cm
Horz .2μs/cm

Fig. V-4E

Testpoint J
G7S
Channel 1
OUR1....

Testpoint I
G7R
Channel 2
1μs.....



Scope Setting
Vert 2v/cm
Horz .2μs/cm

Fig. V-4F

INTRODUCTION

This section provides information to install and check out an I/O Base or I/O Base Extension.

LOGIC PREPARATION

TERMINATOR CHIPS

During installation of an I/O Base or I/O Base Extension Terminator chips are installed. With a system having one I/O Base the Terminators go on the Distribution card. When adding an I/O Base Extension the Terminators should be moved to the Subdistribution card. For a system with more than one I/O Base Extension the Terminators would go at the end of the "daisy chain".

Table 1 shows the location of the jumper chip in the Distribution card and the location where it should be moved to in the Subdistribution card.

Table VI-1

Termination Resistor Value	Distribution Card Chip Location	Subdistribution Card Chip Location
	GO	AO
133	HO	BO
	IO	CO
	G1	A1
511	H1	B1
	I1	C1
133 511	J1	GO (Install this chip with the 133r resistors on pins B,C,+D)

PHYSICAL INSTALLATION

BACKPLANE INSTALLATION

The I/O Base consists of a 10 card backplane mounted within the lower card housing assembly. The I/O Base backplane is installed on the card housing using 20 8-32 by 1/2" screws. The I/O backplane is installed from the rear of the card housing assembly with backplane location A0 matching to slot 10 of the card housing assembly. This means the I/O base is installed to the far right of the card housing assembly looking from the rear.

With the exception of the subdistribution card the I/O Base Extension is identical to the I/O base. The I/O Base Extension will be mounted in slots 11 through 20 of the lower card housing assembly.

Mounting the backplane automatically picks up the two logic voltages and ground. The unique voltages are on wire wrapped pins. These are pin locked and go to each card slot. To obtain voltage on these pins a #16 wire is soldered to the voltage pin at backplane connector D1 and run over to the unique voltage bus bars. Table 2 gives pin locations and proper voltages.

Table VI-2

Pin 0ZX	-12V
1AY	-12V
1LY	+12V

With the system power off insert a card carefully into the backplane. If the connector does not line up with the card it will be necessary to loosen the backplane mounting screws and line the connector up. Try the card in slot 1 and slot 10. After alignment tighten screws down.

DC POWER CHECK

Remove card. Power system up. Check voltages on the following pins of the I/O base or I/O Base Extension.

Table VI-3

Backplane Pin	Voltage
0AX	+4.75V
0ZX	-12V
1AY	-12V
1LY	+12V
0ZY	-2V

CARD LOADING AND CABLING

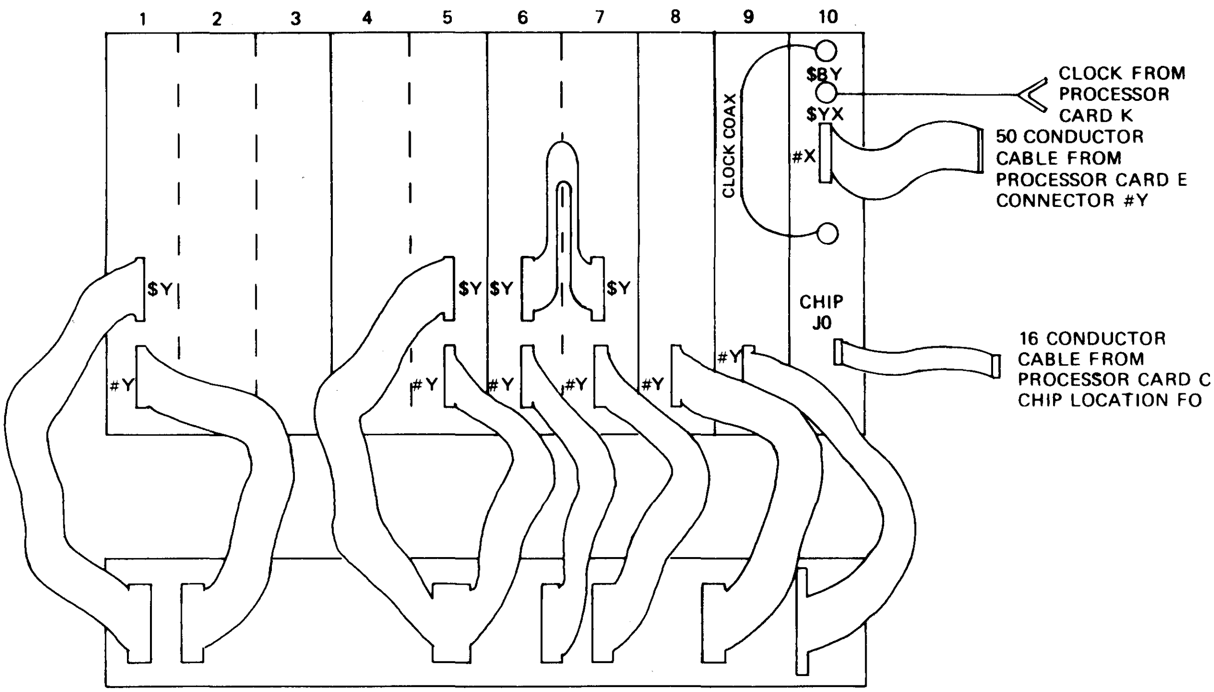
Reference Figures VI-1 and VI-2

After power check insert the distribution card in slot 10. Connect a 50 conductor ribbon cable from distribution card #X to processor card E #Y. Connect a 16 conductor ribbon cable from chip location J0 on the distribution card to chip location F0 of processor card C. Connect a standard clock coaxial cable from,coax connector $YX on the distribution card to the center coax connector on processor card K. Connect a standard clock coaxial cable from coax connector $BY of the distribution card to the center coax connector on the distribution card.

If an I/O Base Extension is installed insert the subdistribution card into slot 10. Connect a 50 conductor ribbon cable from $Y of the Distribution card to $X of the Subdistribution card. Connect a 50 conductor ribbon cable from #Y of the Distribution card to $Y of the Subdistribution card. Figure VI-1 shows a typical I/O system loaded into the I/O Base.

Figure VI-2 provides a definition for each of the 10 slots in the I/O Base and indicates if a slot is dedicated to a particular control.

FRONTPLANE VIEW



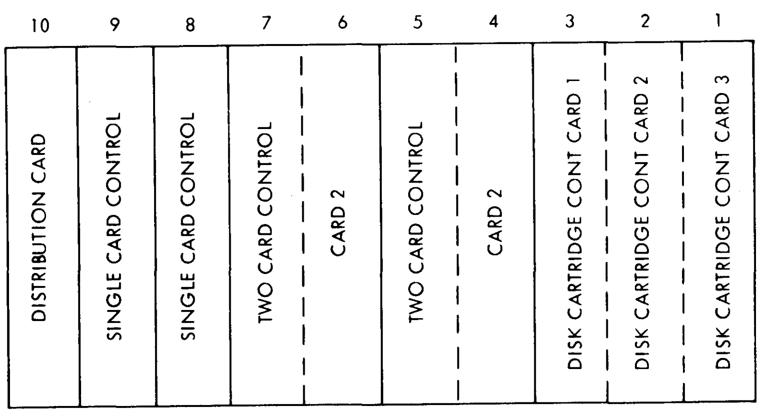
I/O INTERFACE PANEL

CARD LOADING CHART

10. DISTRIBUTION CARD	5. PRINTER
9. SPO	4. NOT USED
8. 80 COLUMN READER	3. DISK CARTRIDGE CARD 1
7. 96 COLUMN MFCM CARD 1	2. DISK CARTRIDGE CARD 2
6. 96 COLUMN MFCM CARD 2	1. DISK CARTRIDGE CARD 3

Fig. VI-1 TYPICAL I/O SYSTEM CARD AND CABLE LOCATION

LOADING CHART



SINGLE CARD CONTROLS
1. SPO
2. CARD READER
3. PRINTER

TWO CARD CONTROLS
1. MULTIFUNCTION CARD UNIT

THREE CARD CONTROLS
1. DISK CARTRIDGE CONTROL

BACKPLANE VIEW

POSITION 10	DISTRIBUTION CARD
POSITION 9	SINGLE CARD CONTROL
POSITION 8	SINGLE CARD CONTROL
POSITION 7	SINGLE CARD CONTROL OR CARD 1 OF A TWO CARD CONTROL
POSITION 6	CARD 2 OF A TWO CARD CONTROL
POSITION 5	SINGLE CARD CONTROL OR CARD 1 OF A TWO CARD CONTROL
POSITION 4	CARD 2 OF A TWO CARD CONTROL
POSITION 3	DISK CARTRIDGE CONTROL CARD 1
POSITION 2	DISK CARTRIDGE CONTROL CARD 2
POSITION 1	DISK CARTRIDGE CONTROL CARD 3

Fig. VI-2 B1700 I/O BASE

I/O BASE CHECKOUT

Assure that the I/O clock is adjusted properly. Refer to Section IV for this adjustment. Further checkout of the I/O Base or I/O Base Extension will require installation of an I/O Control.

GENERAL

CHANNEL NUMBER ADJUSTMENT

Control channel number is used by the processor to address a control. During a service request by a control the channel number is used to determine priority in the advent two or more controls need service. High number has priority.

A jumper chip on each control is wired to determine the channel number. Channel numbers will vary with different system configuration and uses. Refer to Figure VI-3 for an example of wiring the channel number.

An example of a typical system is listed below:

Table VI-4

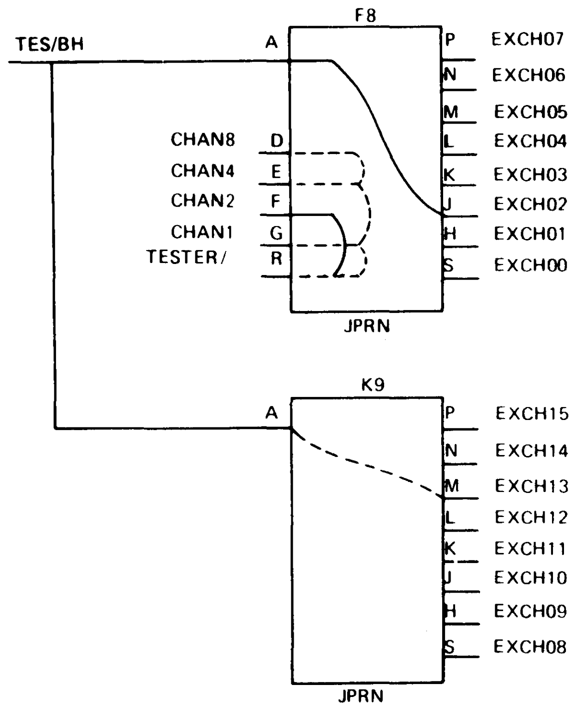
Control	Channel #
Sorter Reader	7
Mag Tape	6
Disk cartridge	5
Data Comm	4
Line Printer	3
96 Column MFCM	2
80 col. card reader	1
SPO	0

Table VI-5 shows the channel number jumper chip location for currently available controls. SPO and Disk are shown as being 0-15 channel controls. System configuration at present has a maximum of 8 controls.

Table VI-5

Control	Jumper Chip Location
SPO	F8-CH 0-7
	K9-CH 8-15
96 Col MFCU	Card 1 A9-CH 0-7
Printer	B8-CH 0-7
80 Col Card reader	A9-CH 0-7
Disk Cartridge	Card 1 H0-CH 0-7 K0-CH 8-15
Sorter Reader	Card 1 B8-CH 0-7 A9-CH 8-15

CHANNEL NUMBER JUMPER CHIP EXAMPLE



Example 1

In this diagram the SPO Control is used as an example. The solid heavy line from F8 pin A to pin J. This is used to generate the service request mask. Pin R is connected to pin F. This level goes to a 4 bit comparator. This is used to determine if the channel address on the exchange lines matches the control. This chip is now wired for channel 2.

Example 2

The dotted lines show how channel 13 would be wired. On F8 pin R is connected to pin G, pin E and pin D. On K9 pin A is connected to pin M.