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MAY 1, 1989

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THE FIRST MAGAZINE OF SYSTEM DESIGN,
DEVELOPMENT AND INTEGRATION

Distinctions blur
between DSP solutions

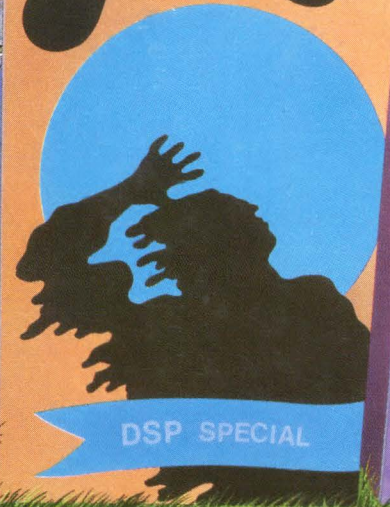


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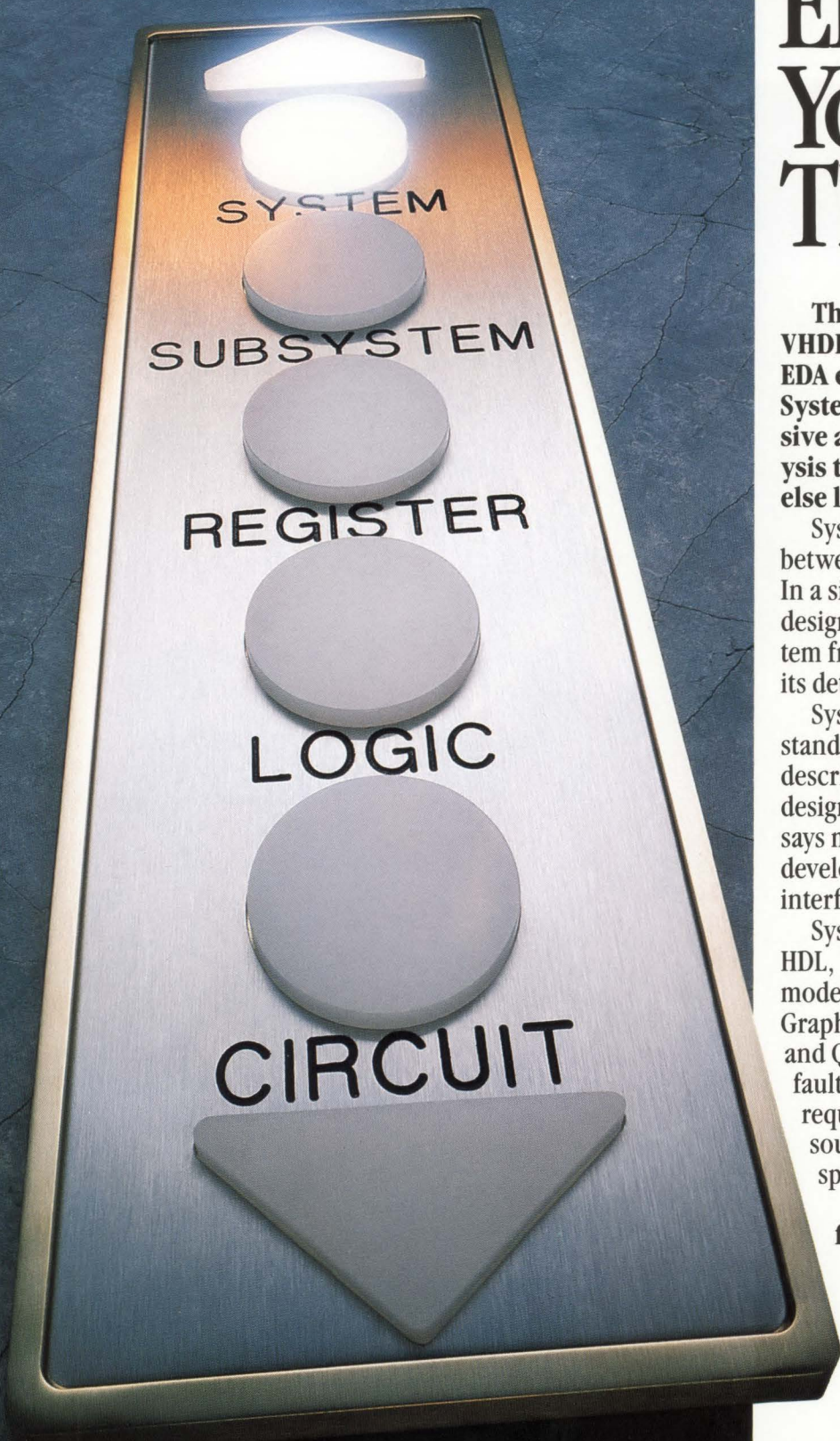


DSP SPECIAL

■ 80486 carries
complex instruction set
to RISC speeds
Page 18

■ Designers
hang on
to Multibus I
Page 69

■ Mixed-signal
simulator eases
system integration
Page 103



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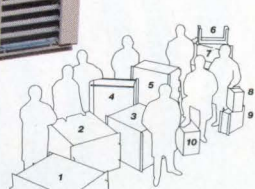
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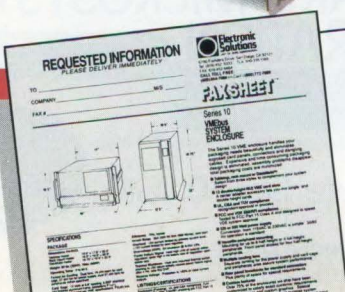


—Dr. Leonid R. Besprozvanny
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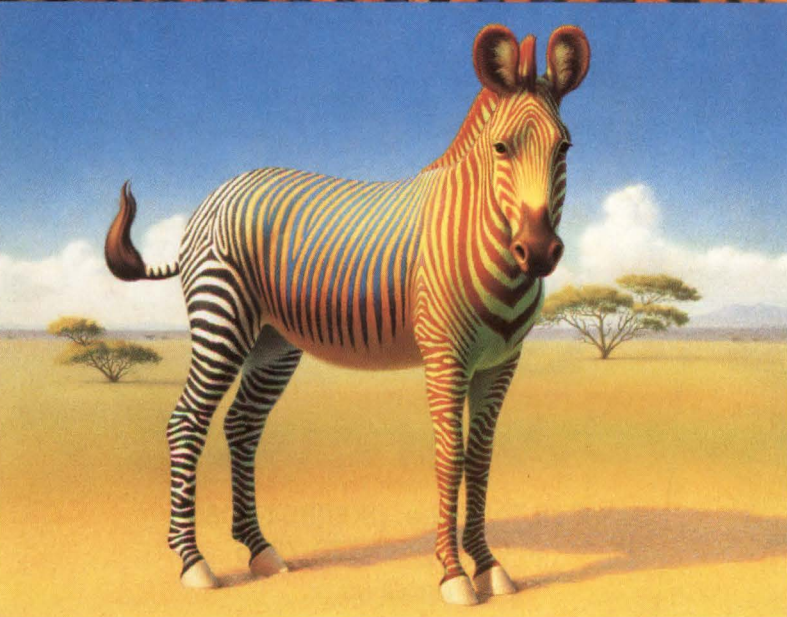
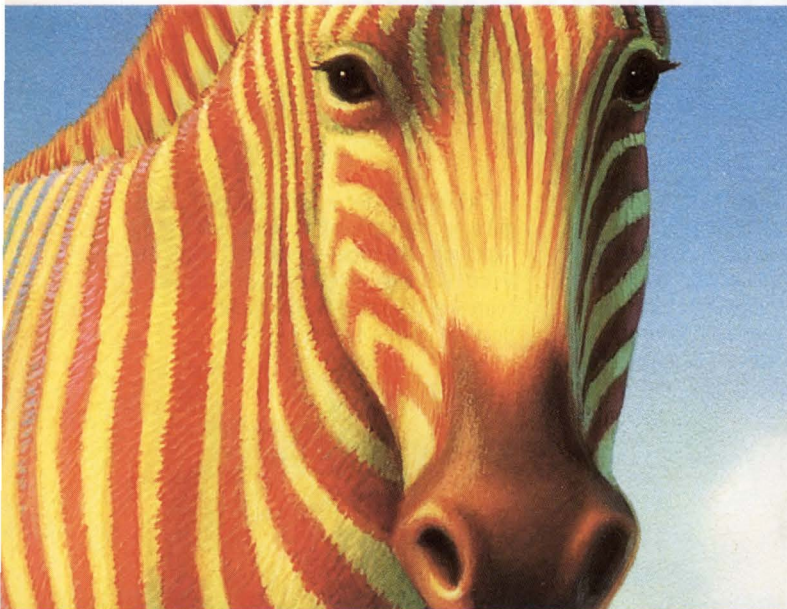
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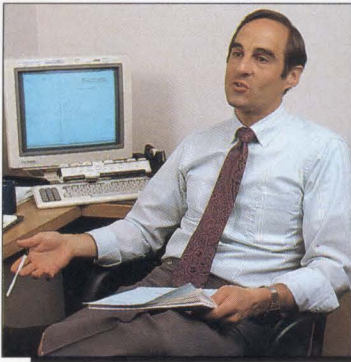
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CIRCLE NO. 3

THE FIRST MAGAZINE OF SYSTEM DESIGN,
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TECHNOLOGY UPDATES

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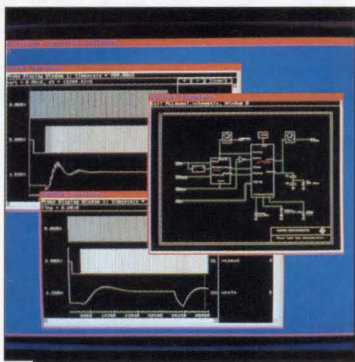
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At about strange things happen to

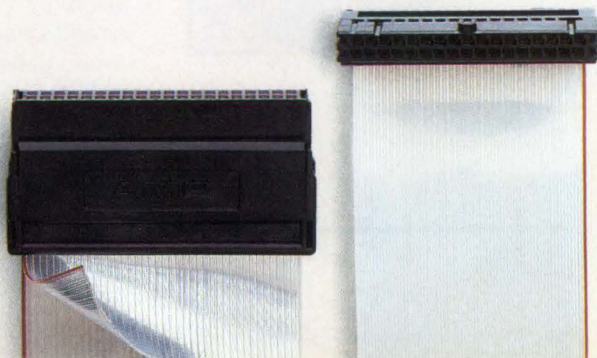
As rise times approach 3ns, all cable/
connector assemblies become trans-
mission line assemblies.

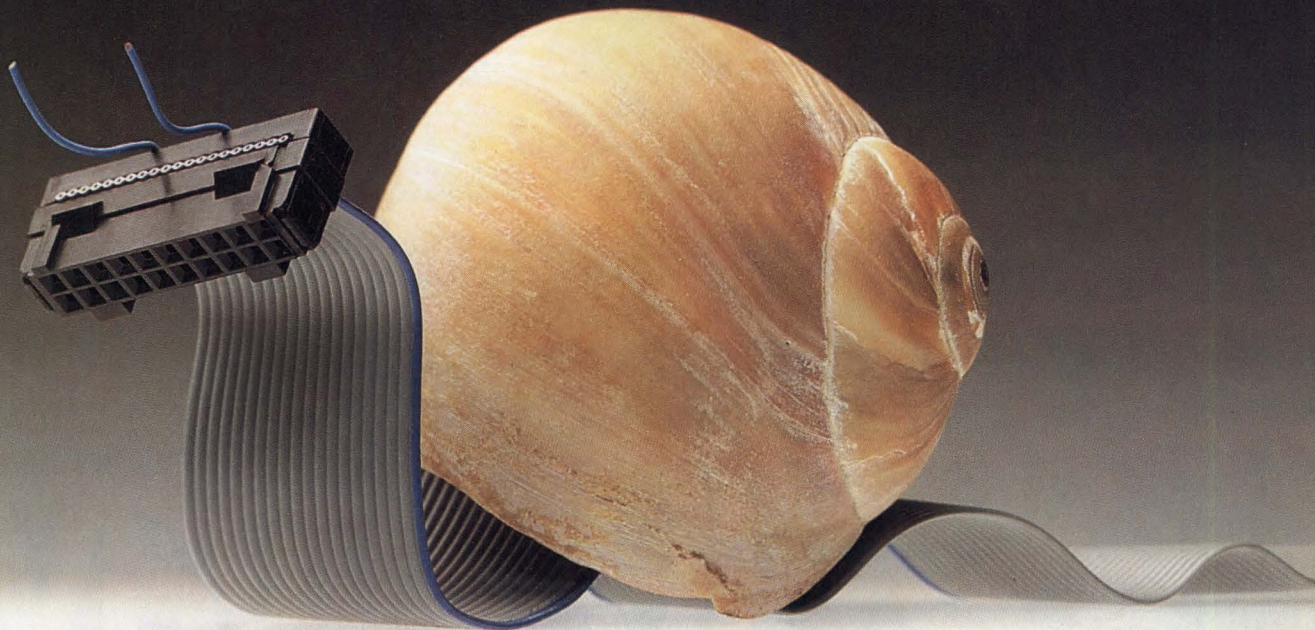
But not necessarily good ones.

Newer, faster logic families require
controlled impedance cable assem-
blies. Designed for high-speed per-
formance. Engineered for controlled
impedance and propagation rate. And
manufactured for absolute conformity
to specifications.

Creating controlled impedance
assemblies to these standards demands
extensive CAD/CAE use. Plus a wide
range of specialized connector choices.
Plus the capability to custom design
quickly. Plus intimate knowledge of
the various termination techniques,
including advanced wire attachment
techniques.

Our people are equipped to work





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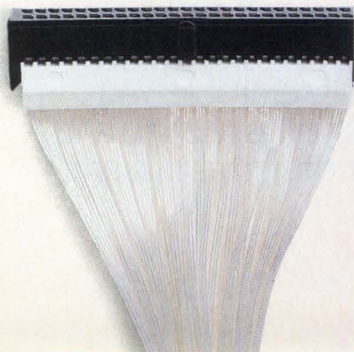
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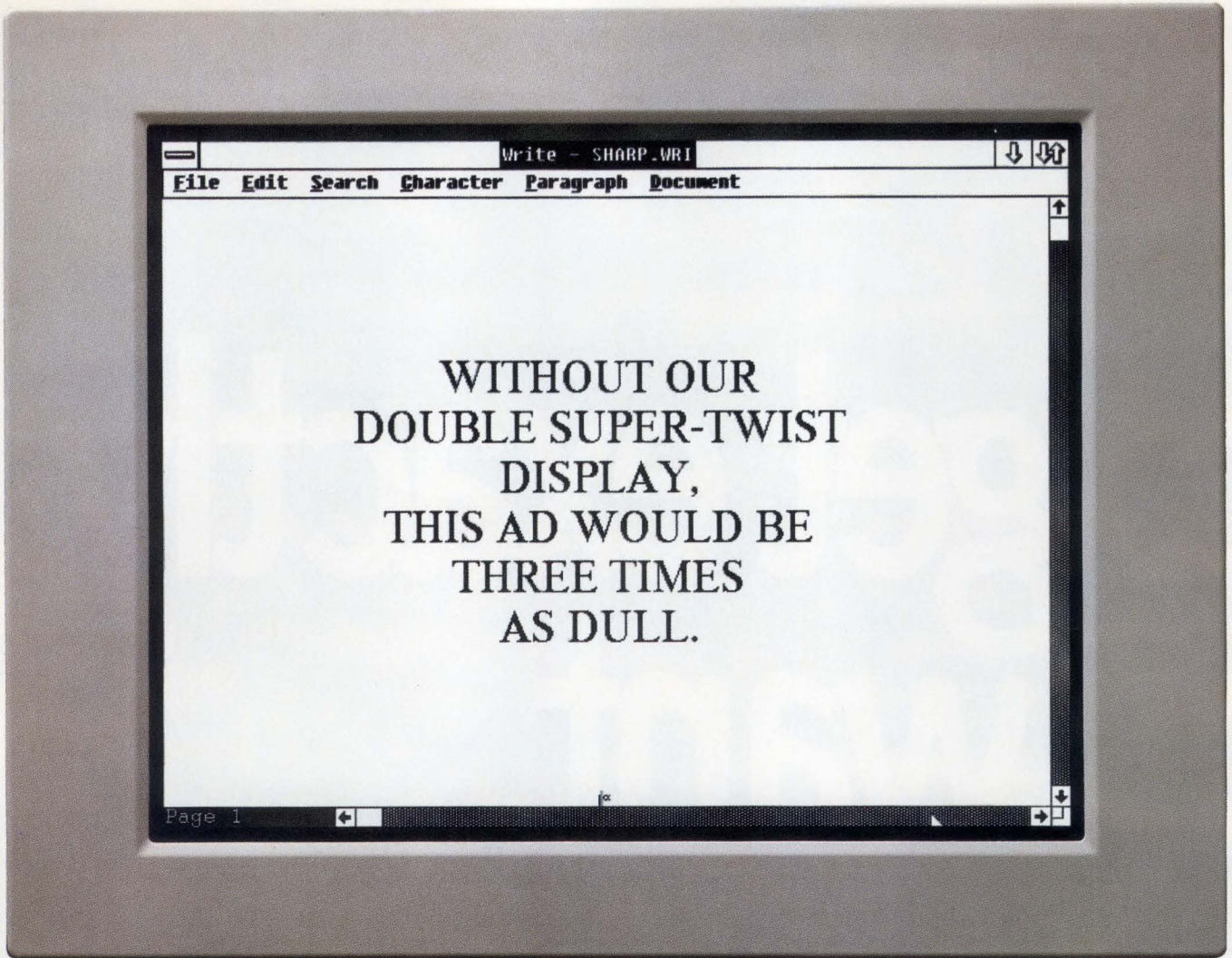
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LM64135Z	640x400	300x166x26	218x139	0.30x0.30
LM64148Z	640x480	280x180x25.5	205x155	0.28x0.28
LM64048Z	640x480	310x240x25	237x180	0.33x0.33
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Motorola unwraps 32-bit single-chip microcontroller

Motorola (Austin, TX) has unveiled its long-awaited 32-bit, single-chip controller, the 68332. The chip, designed around General Motors' requirements, surrounds a modified 68020 CPU core with a variety of intelligent peripheral modules and 2 kbytes of static RAM. Additional family members under development will add on-chip ROM to the design.

In the 68332 design, the latent power of the 68020 CPU core is unleashed by protecting the core from event-driven interrupts. This is accomplished by upgrading the traditional serial, parallel and timer I/O devices into full-blown programmable processors in their own right, capable of performing even complex application-specific operations without CPU intervention. The timer module, for example, can accelerate, drive, coast and halt a stepper motor on its own, without CPU intervention.

Major modules on the 68332 include the CPU core, the programmable timer module, an intelligent synchronous/asynchronous serial communications module, the SRAM, and a system integration module (which contains most of the bus, control and debug functions normally implemented in off-chip logic).

—Ron Wilson

Western Digital publishes 8514/A register specs

Third-party graphics software developers eager to write more efficient code to the IBM 8514/A display adapter will be able to get register specifications for the IBM silicon through Western Digital (Irvine, CA). IBM has declined to publish the register specification and has insisted instead that graphics developers write to a software protocol layer called the adapter interface (AI). Since many feel that the AI imposes a performance penalty, several companies have been rushing to discover the IBM register details and produce functionally equivalent silicon.

Western Digital is releasing the IBM registers that the AI uses, so developers can bypass the AI and

write directly to the registers. The chip set Western Digital is developing, called the PWGA-1, will have extended registers. Specifications for these extended registers will be offered to Western Digital's OEMs under nondisclosure agreement.

In addition to discovering the register specifications, Western Digital claims to have uncovered a memory conflict between the range used by IBM's 8514/A BIOS EPROM and that used by third-party extended VGA. The conflict could cause a system crash if both extended VGA and 8514/A are used in the same system. Western Digital is proposing standardization on BIOS address ranges for extended VGA and third-party 8514/A systems. In addition, the PWGA-1 will eliminate the need to use an interlaced monitor, a major hindrance of IBM's 8514/A. No availability date for the chip set has been announced.

—Tom Williams

VESA approves extended VGA standards

The Video Electronics Standards Association (VESA) has reached preliminary agreement on a standard BIOS interface for the 800- x 600-pixel 16-color Super VGA mode. The VESA standard is significant because Super VGA, a natural extension of IBM's 640- x 480-pixel 16-color VGA mode, isn't an IBM standard. Each Super VGA card from every vendor, therefore, has required a different set of application drivers. The VESA standard has established a common mode number (6Ah) that will let software developers write one driver for all cards that follow the VESA standard.

Not addressed in the preliminary document is the issue of BIOS memory-range conflict reportedly discovered by Western Digital (Irvine, CA) in its research into the IBM silicon (see story above). Since the document covers software standards only, it likewise doesn't address the issue of differing monitor frequencies. According to VESA, these issues may be raised under new business when the association meets to formally organize and to vote on the standards document.

—Tom Williams

HP buy of Apollo draws mixed reaction

The \$476 million purchase last month of workstation pioneer Apollo Computer (Chelmsford, MA) by Hewlett-Packard (Palo Alto, CA) both surprised competitors and reassured customers. The move came as a shock to Apollo's competitors, notably Sun Microsystems (Mountain View, CA), which had been exploiting the financial uncertainty surrounding Apollo. Conversely, major Apollo customers cheered the move, saying the purchase removes any financial doubts about a supplier they perceive to be a technology leader.

Perhaps most directly affected by the purchase will be Apollo's major customer, Mentor Graphics (Beaverton, OR). "We can't imagine a better combination than Apollo's technology and HP's financial, market and support strengths," says Gerard Langelier, president and chief operating officer of Mentor. "It will make Mentor customers feel better about using Apollo products."

Mentor anticipates no conflict from HP's growing presence in the electronic CAE market. "They have handled a similar situation quite well already in their relationship with McDonnell-Douglas in the mechanical area," Langelier notes.

—Ron Wilson

Sun shows new lineup of Sparc workstations

The next generation of workstations announced by Sun Microsystems (Mountain View, CA) includes a number of firsts, including Sun's first response to Digital Equipment Corp's challenge in the under-\$10,000 arena and Sun's first use of the Cypress 7C601 Sparc processor.

Two lines of Sparc products were introduced: the Sparcstation 1, with a 20-MHz LSI Logic-supplied Sparc CPU based on the familiar Fujitsu Sparc implementation, and the Sparcstation 300, using the Cypress Semiconductor Sparc integer unit at 25 MHz.

The Sparcstation 1 seems intended as a direct challenge to DEC's R2000-based DECstation 3100. The Sun system starts at \$8,995 for a

(continued on page 10)

(continued from page 9)

desktop unit with small monochrome monitor and no disk, and quickly moves up the price curve to a still-impressive \$15,495 for a system with color display and disk. Sun rates the unit at 12.5 Mips. The Sparcsystem 300, meanwhile, is rated at 16 Mips, with prices ranging from roughly \$30,000 to \$74,000.

Many design automation vendors have already announced their support for the new machines. Vendors supporting the new systems include Valid Logic Systems (San Jose, CA), Teradyne EDA (Santa Clara, CA), Cadence Design Systems (San Jose, CA) and Daisy/Cadnetix (Mountain View, CA).

—Ron Wilson and Bill Harding

Active-matrix LCD displays 16 colors

At this month's SID (Society for Information Display) conference, IBM Japan and Toshiba America (Irvine, CA) will demonstrate a large, high-resolution active-matrix LCD that doubles the color capability of displays of this type. Whereas color LCDs typically use a triad of RGB filters to generate eight basic colors, this prototype 14.26-in.-diagonal, 720- x 550-pixel display uses a quad-filter arrangement with a fourth, white filter that lends two brightness levels to whatever color is generated by RGB combinations. "You can, for example, have a deep, saturated red or a kinder, gentler red," says Denis Arvay, manager of information for IBM's Research Division (Yorktown Heights, NY).

Although the 16 colors possible with this display are nowhere near the 256-color capability that would make the thin-film LCD a viable CRT replacement for today's color graphics applications, its pseudo-grayscale capability should give it an advantage when true grayscale versions compete on the grounds of the depth of their color palettes.

—David Lieberman

Heavy investment pays off for Toshiba

The recent success of Toshiba (Tokyo, Japan) in the memory IC arena

is proof that long-term, steady investment can earn formidable dividends. In five of the last six years, the company has outspent its rivals on semiconductor manufacturing and on research and development. Not surprisingly, the Japanese manufacturer has maintained a dominating 30 percent market share of the 1-Mbit dynamic RAM market over the last two years. That's an uncommon achievement in the rapidly maturing and cost-sensitive DRAM market.

Toshiba appears ready to accomplish a similar feat in the 4-Mbit DRAM market. The company has already gained a lead in these next-generation memories with the introduction of twenty-four 4-Mbit parts in various speeds and configurations. Company officials expect to begin production on faster 60- and 70-ns devices shortly.

Toshiba is also staking a claim to the high-speed SRAM pie. At Electro last month, Toshiba unveiled a series of 1-micron CMOS, 256-kbit SRAMs with speeds of up to 20 ns. The parts come in two 64k x 4-bit versions, one with output enable and one without. The company also offers a 32k x 8-bit configuration and a 32k x 9-bit part that allows for bit parity. —John Mayer

Parallel computing gets serious...and friendly

During the next three years, the Defense Advanced Research Projects Agency (DARPA) will reportedly sink \$7.6 million into a project on a massively parallel computing system. The system will link from 20 to 2,000 processing nodes based on Intel's recently announced 80860 chip.

Hypercube manufacturer Intel Scientific Computers (Beaverton, OR) will be responsible for developing the first prototype, code-named Touchstone, which is slated for first demonstration by the end of 1991. In its maximum configuration, Touchstone is expected to be able to crunch through more than 128 billion 64-bit Flops.

A significant portion of the DARPA funds will go toward making the prototype as easy to use as a garden-variety workstation, according to Justin Rattner, director of technology at Intel Scientific. "We

expect Touchstone to improve parallel-computing performance levels 100 times over what they are today," he says, "as well as to create a software environment to give these powerful machines the look and feel of conventional systems."

—David Lieberman

Widebus doubles I/O functions

Texas Instruments (Dallas, TX) will provide twice as many I/Os as standard 24- and 28-pin devices by using a space-saving, very small outline package in its new Widebus Series ICs.

Fabricated in 1-micron CMOS technology, the products will operate at speeds comparable to those of advanced bipolar chips but will effectively reduce the amount of board real estate needed for line drivers, transceivers, flip-flops and registers by using 25-mil center-to-center pin spacings.

Designers will be able to use each Widebus function at its full width or as dual, independently controlled 8-, 9- or 10-bit functions. TI hopes to have engineering samples by the third quarter of 1989, with production slated for the fourth quarter.

—Mike Donlin

High-speed NuBus boards debut at Electro/89

In addition to the April Electro/89 introduction of its MXIbus backplane bus, National Instruments (Austin, TX) chose the same conference to introduce two very high-speed data-acquisition board additions to the company's line of Macintosh II NuBus products. One of these boards samples waveforms on one of four available channels at rates of up to 1 Msample/s with a 12-bit resolution, says Audrey Harvey, engineering manager. Use of all four channels simultaneously allows sampling at 250 ksamples/s on each channel.

In addition, a 32-bit block-mode DMA interface board offloads some of the work of the Macintosh II coprocessor by transferring data from a compatible data-acquisition board directly to memory. This offloading also lets the Mac II function as a GPIB controller.

—Syd Shapiro

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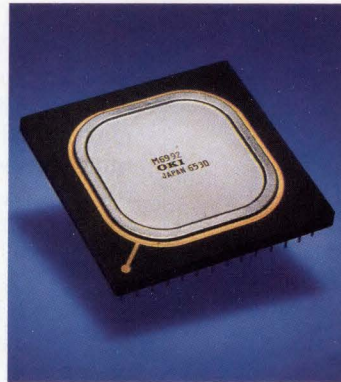


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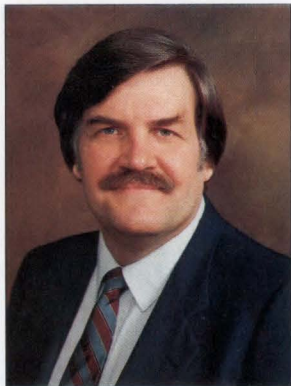
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Editor-in-Chief

Where can you go to kick the tires?

If you're interested in ICs, that's a tough question to answer. The second and third weeks in April brought the spring blossoming of electronics/computer shows. There was Electro in New York City, Comdex Spring in Chicago and NCGA in Philadelphia. But there's been a shift in focus in these shows over the past few years, which is making it hard for a designer or a design manager whose primary interest lies in ICs—microprocessors, SRAM and DRAM, A-D converters, op amps, PLDs, etc., etc.—to find enough to make it worthwhile to trek to the Big Apple, the Windy City or the place where W.C. Fields would rather be.

In this regard, Electro was a complete bust with no more than a half-dozen IC vendors showing their wares, among them Advanced Micro Devices, Analog Devices, Harris and Toshiba. An interest in design and development tools goes hand in hand with an interest in ICs, and here the representation was equally sparse with only Data I/O, P-CAD, Orcad and a few smaller players making a showing. And if you wanted to “kick the tires” at each of these vendors' exhibits, you had to hunt them out from a Miracle Mile of connector, cable, cabinet, switch, power supply and passive component vendors.

It's not that I have anything against cabinet, power supply and switch vendors; after all, you don't power up the microprocessor until you've turned on the switch. But there's no conference or exhibition running today—not Electro, not Wescon, not Comdex, not even the Design Automation Conference—whose primary appeal is to the designer or design manager who wants to talk about, learn about or sample the full breadth of the latest architectural components. By architectural components, I mean those components that determine the intrinsic functions, performance and features of an electronic/computer product or system. Microprocessors, RAMs, EEPROMs, peripheral interface or controller chips, for example, are architectural components. So are single-board computers, graphics controller boards, digital-signal processor boards and I/O boards. And so, too, is software—operating systems and real-time kernels, for example.

From studies we've done of our readers, the odds are better than 60/40 that if a designer is using off-the-shelf boards, he (or she) is also designing boards or subsystems using standard ICs or ASICs. The reverse is also true; a large percentage of designers developing their own boards or subsystems are interested in off-the-shelf board-level products because there's no point in building what you can go out and buy.

For the most part, designers and, especially, design managers can no longer be pigeonholed into chip-level or board-level, or even hardware or software. More often than not, their responsibilities and interests span the complete spectrum of architectural concerns and architectural components. The time's arrived for something we'd call the Architectural Components Conference and Exposition. The time's arrived for a show where *system* designers can kick *all* the tires.

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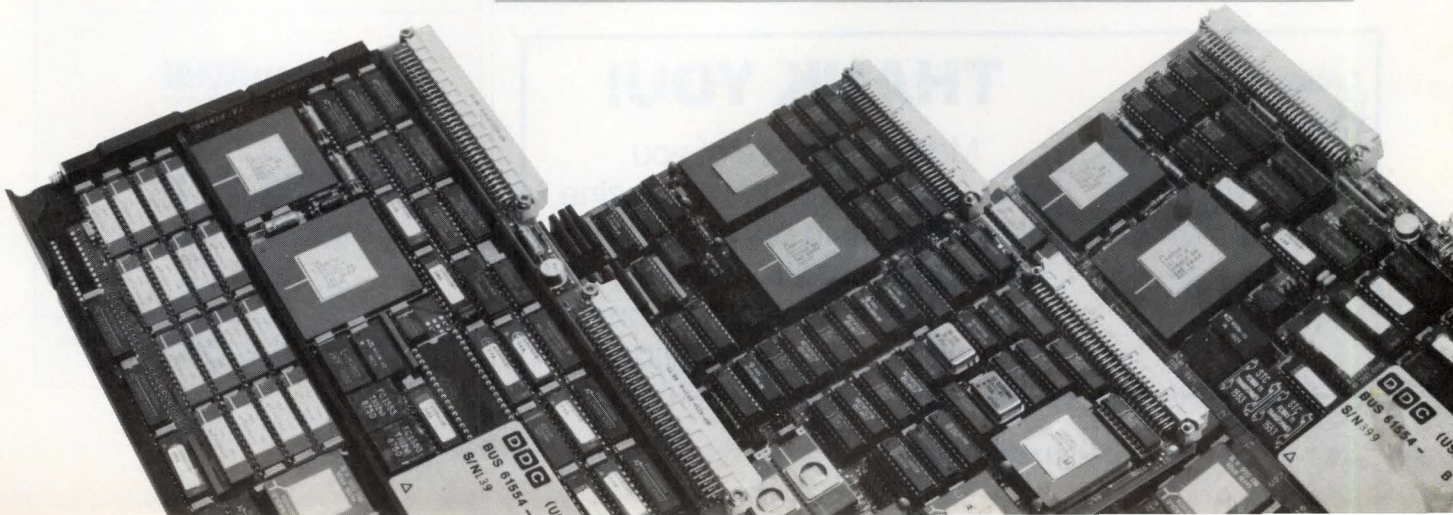


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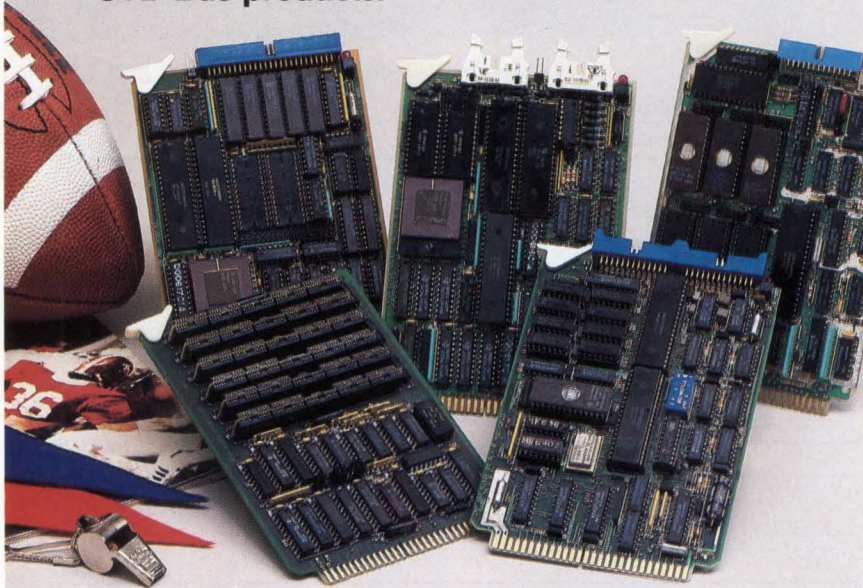
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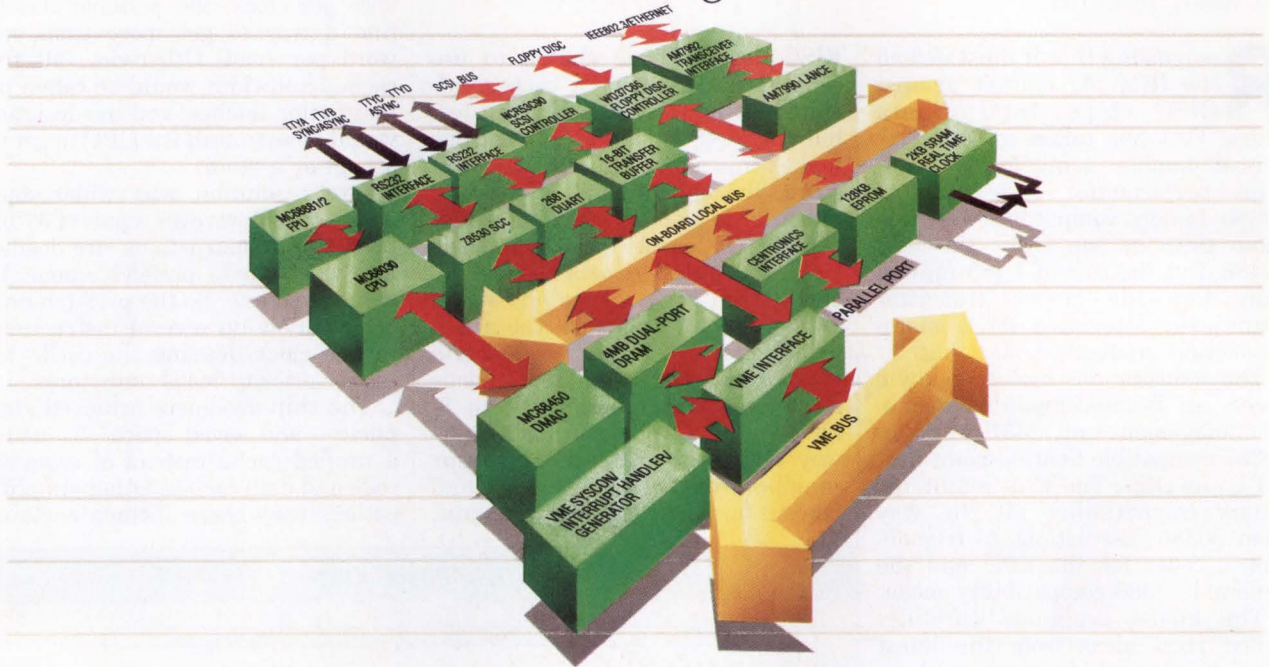
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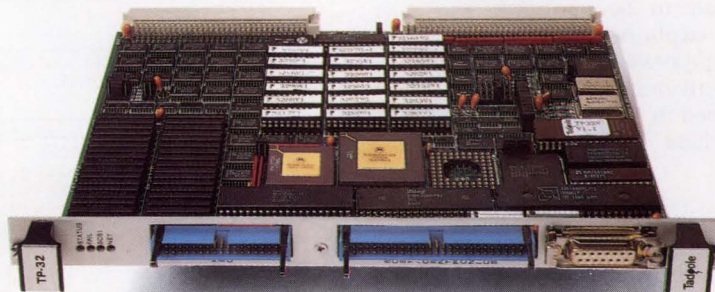
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Intel 80486 carries complex instruction set to RISC speeds

Ron Wilson, Senior Editor

Recognizing that it must defend the IBM PC market against RISC chips, Intel (Santa Clara, CA) has taken an unprecedented gamble: going for both 20-Mips performance and complete 80386 binary compatibility at the same time in one CPU: the new 80486. But the cost of 1.185 million transistors—the largest transistor count ever attempted for a mass-production product—is startling.

The monster die has an 8-kbyte cache, an 80386-compatible memory-management unit (MMU) and an 80387-compatible floating-point unit (FPU) on-chip. The chip maintains binary compatibility all the way from 80386 instructions to trigonometric codes for the FPU and the venerable 8086 compatibility mode.

The 80486 designers carefully culled good ideas from the latest RISC CPUs and incorporated those notions into a machine that would execute the 80386 instruction set. The innovations begin with sharply reduced clocks per instruction in the execution units of the 80486. But this RISC-like timing forced the designers to carefully nurture bandwidth throughout the CPU and memory system.

The first challenge for the designers was to reduce the number of clock cycles per instruction on the existing instruction set. As in RISC machines, most 80486 register-to-register operations require only one clock cycle. Load and store instructions also take a single cycle, with the loaded data available to the next instruction. "This data had to be available immediately," explains Bill Rash, 32-/64-bit microprocessor product manager, "because in many 386 programs, the data is used in the instruction right after the load."

Fighting for bandwidth

The ability to execute one instruction per clock puts enormous stress on memory bandwidth. Clearly, the execution unit's speed can only be maintained by using caches with very good hit rates. Most recent

RISC designs have chosen to use separate code and data caches, off-chip, to keep the execution unit fed, but the 80486's single external bus makes this approach impossible. Instead, the chip architects chose to put a large primary cache on-chip.

Once the cache moved onto the CPU, cache design became a trade-off between performance and space. To select their approach, the architects took traces of existing OS/2 and Unix codes, and simulated various strategies. Their choice was an 8-kbyte unified, code and data, four-way set-associative cache. "On our samples, this cache delivers a 1 to 5 percent miss rate on DOS programs,

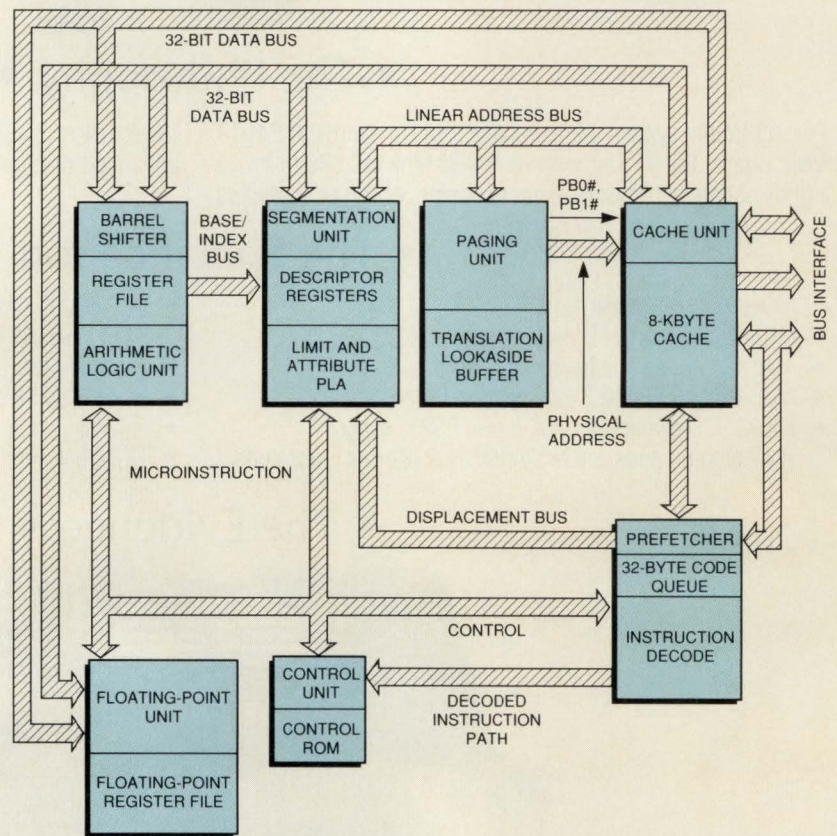
and only 6 to 8 percent on Unix programs," claims Rash.

With only a single cache, though, there's still a throughput problem. Since the cache can only be read once per clock, the designer has to find a way to get more than one word per read. Otherwise, all the cache bandwidth would be taken by instruction fetches, and the designer would have to stall the CPU to get in a load or a store.

Intel's solution was wider data paths: data flows over a pair of 32-bit buses, and instructions are loaded into the 32-byte prefetch queue 16 bytes at a time. So the prefetch unit can swallow up several instructions in one clock, leaving the cache for higher-priority loads and stores.

The chip designers achieved simplicity—and saved space—by using a unified cache instead of separate code and data caches. Other simplifications they chose include a clever

THE 80486 CPU



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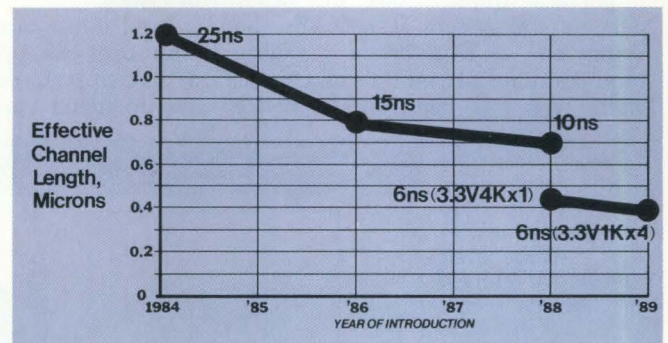
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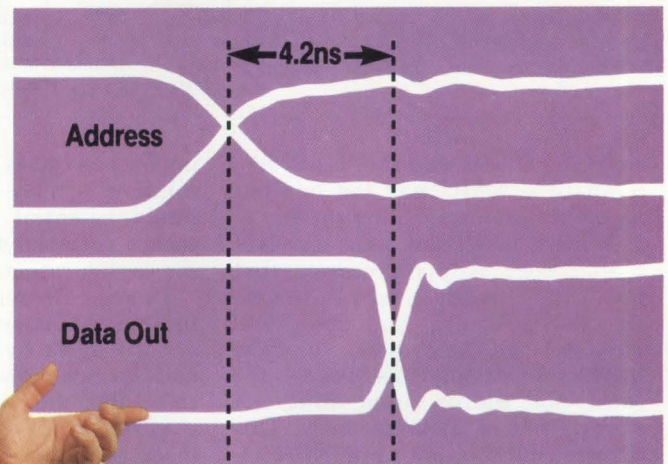
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"sort-of least-recently-used" replacement algorithm, as design manager Pat Gelsinger describes it, and a write-through, rather than copy-back, policy.

Dealing with on-chip cache

But putting the cache on-chip has important implications for other parts of the system design. For one thing, the on-chip cache virtually requires that the MMU be on-chip as well. This has been Intel's policy

great improvement in performance." Intel claims the chip is capable of 6.1 MWhetstones.

Another serious challenge posed by the on-chip cache involves only a few Intel customers: those who use multiple CPUs in servers or parallel computers. Here there are a number of issues.

First is the bus bandwidth. If one chip uses 50 percent of the bus, a five-chip multiprocessor system should spend most of its time wait-

cache's four-word write buffer and the paging unit's translation buffer, that need to be kept coherent. Any of these devices could have its data invalidated by another processor. The 80486 solution is extensive bus snooping, using the chip's address pins as inputs when another device is driving the external bus.

The 80486 approach to multiprocessing contrasts sharply with that of the 64-bit 80860 CPU, which relies entirely on software for coherency management. The difference turns out to be another reflection of Intel's commitment to compatibility: "We felt we had to support the 80386 customers who were using the chip in tightly coupled multiprocessing architectures," explains Rash.

That commitment to compatibility is one of the most remarkable threads running through the 80486 architecture. Binary code compatibility is an essential component of the commitment. But it's evident from the details of the design that the 80486 architects attempted to preserve not only the function, but even the performance of existing 80386 software.

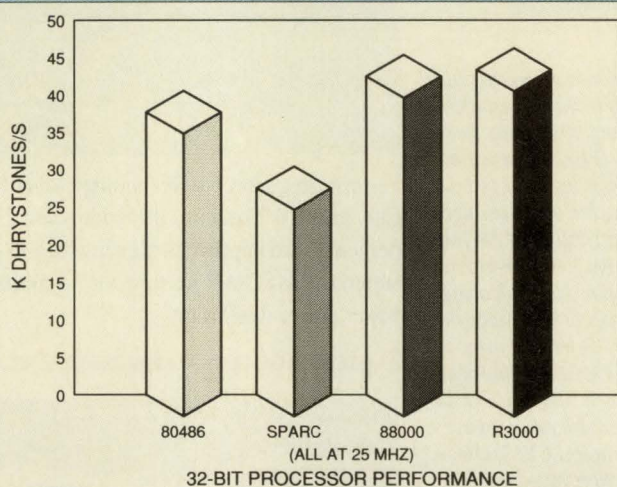
A memory-to-register add takes the same number of cycles as a RISC-style register load followed by a register-to-register add, for example. Software vendors won't have to change coding techniques, or compilers, to get excellent performance from the new chip, despite the 80486's focus on pipelining and single-cycle instructions.

In perspective, the new CPU is an object lesson in the application of new technology. The Intel architects have studied at the temple of RISC, but they haven't worshiped there. Instead, they have systematically taken the best lessons in system design from the RISC school and applied them in the context of the most widely used architecture in the computer industry. The result is a microprocessor that will carry the enormous body of PC software into the performance range once occupied only by the best of the RISC CPUs. □

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A PERFORMANCE COMPARISON



Using ideas from RISC architectures, Intel's 80486 reaches performance levels previously reserved for RISC purists but maintains 80386 object compatibility.

since the 80386, and the full 80386-compatible MMU has the familiar segmentation and paging units.

A more important issue involves coprocessors. Any coprocessor that has to have ready access to the instruction stream at high speed will have to be on the chip too, since the instruction stream runs between the cache and the execution unit, not directly out of main memory. This required Intel to put an 80387-compatible FPU on the chip.

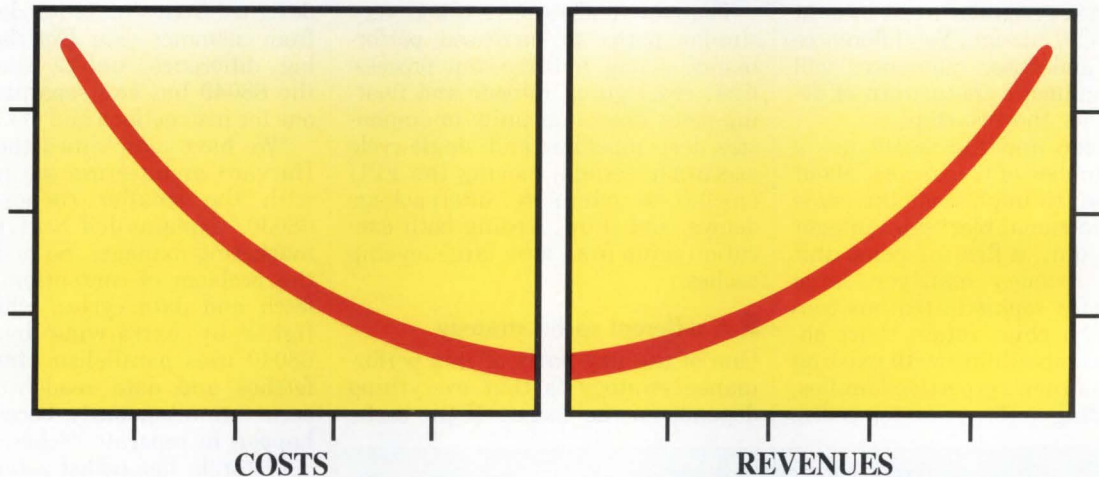
Rather than just duplicate the existing coprocessor, the design team decided to reimplement the FPU from a functional description. The unit executes the 80387 instructions, but with entirely new hardware. One result is a substantial decrease in clock cycles. "We were able to cut down on cycles per instruction in the FPU by a factor of 2.5 to 3," Gelsinger says. "That improvement, together with eliminating the off-chip handshaking and having a 64-bit path into the cache, has meant a

ing for bus cycles—hardly ideal. The solution is more caches. "It's absolutely essential to use secondary caches with the 486 in multiprocessor configurations," says Gelsinger.

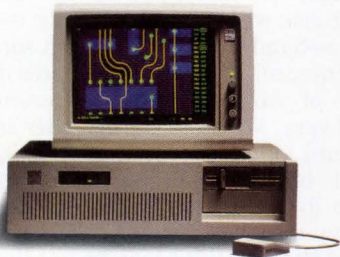
To keep the demands manageable in shared-memory systems, designers will need to deploy large copy-back caches between the 80486 and the central memory. "In addition, it's very important to support the burst-mode operation of the memory bus, and to do everything possible in the memory design to keep write cycles down to at most one wait state," says Gelsinger. In practice, that means using nibble-mode or page-mode dynamic RAM, or interleaving, to provide the 106-Mbyte/s bursts the voracious CPU demands, and providing write buffers in the memory system to keep the DRAM write cycle time from holding up the bus.

The second major design issue in multiprocessor systems is coherency. There are lots of subsystems in the 80486, including the cache, the

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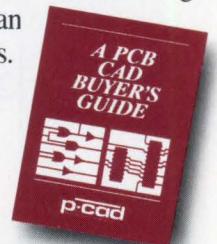
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68040 moves toward RISC camp with redesigned pipelines, caches

Ron Wilson, Senior Editor

While many of the architectural details aren't yet available, it's clear from early information that the 68040 from Motorola (Austin, TX) and the 80486 from Intel (Santa Clara, CA) have gone down very similar roads in most aspects of CPU design. Yet differences do exist, and these differences will probably influence the pattern of design wins for the two chips.

The 80486 and the 68040 use a similar number of transistors, about 1.2 million, to implement the same on-chip functional blocks: an integer execution unit, a floating-point unit (FPU), a memory manager, large caches and a sophisticated bus controller. Both chips retain strict object-level compatibility with existing members of their respective families, while adding a few new op-codes.

And both chips boast significant performance improvements over their previous-generation relatives. Motorola hasn't released official figures, but rumor puts the 68040 speed at around 13 Mips.

The two vendors have taken very similar paths to increased performance, using a three-step process: first, redesigning integer and floating-point execution units to emphasize deep pipelines and single-cycle execution; second, moving the FPU on-chip to eliminate interpackage delays; and third, feeding both execution units from very large on-chip caches.

A different cache strategy

One of the key parts of this performance strategy is that everything depends on the caches. If the cache

miss rate is high for a particular application, that application will be slow on the new chip at any clock frequency. So both Intel and Motorola teams have paid careful attention to cache design. And in this one area, their strategies have diverged significantly.

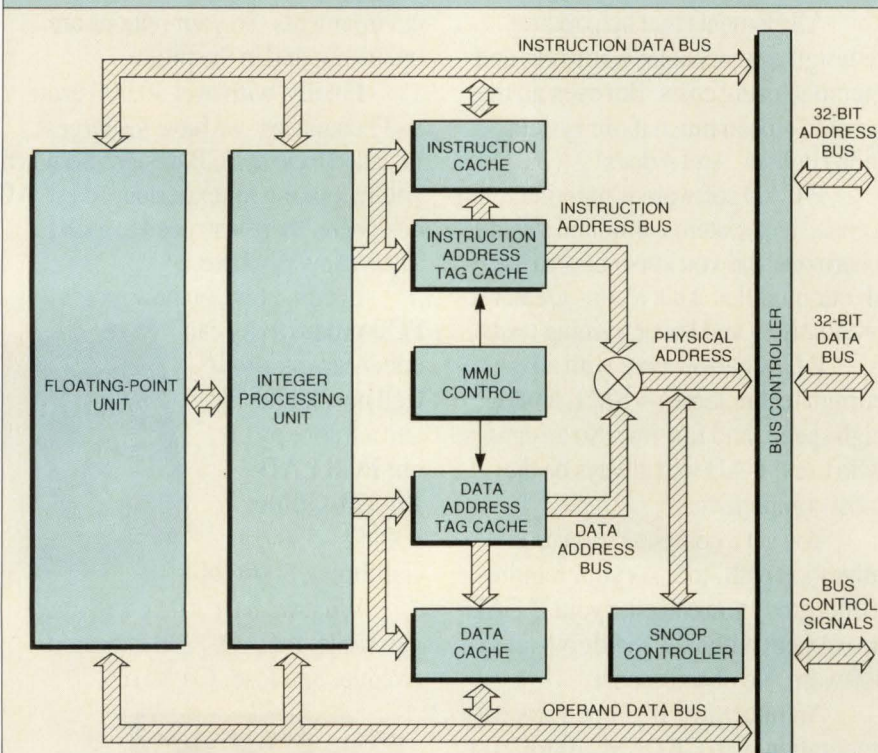
Both the 80486 and 68040 caches are organized as four-way set-associative systems. Each chip reportedly has a total of 8 kbytes of cache. And the caches in both chips were designed from simulation data taken from customer code. But there's one big difference—unlike the 80486, the 68040 has two separate caches: one for instructions and one for data.

"We have maintained the on-chip Harvard architecture we pioneered with the smaller caches in the 68030," explains Jeff Nutt, technical marketing manager. So to deal with the problem of contention between fetch and data cycles, which Intel fights by extra-wide buses, the 68040 uses parallelism. Instruction fetches and data reads/writes can occur simultaneously because they happen in separate caches.

Motorola has added a further degree of sophistication to the 68040 cache controllers. The chip can operate its caches in either write-through or copy-back mode. This difference would appear to help lessen bus-bandwidth problems on some routines, although it complicates design of on-chip cache coherency hardware. Motorola claims other significant advances in bus management but is unwilling to discuss them due to patent requirements.

The most important observation about the two chips may be not their differences, but their similarities. Both have taken a CISC architecture to a new level of performance by reducing not the instructions, but the clocks per instruction. And because CISC architects have learned from their enemies, both designs may succeed in fending off challenges from RISC CPUs. □

THE MOTOROLA 68040



The 68040 maintains the dual-bus Harvard architecture Motorola introduced with the 68030 CPU. But the new CPU brings floating point on-chip and enlarges the on-chip caches.

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CIRCLE NO. 15

INTEGRATED CIRCUITS

Vendors ponder interconnect schemes in search for new PLD architectures

Ron Wilson, Senior Editor

The avalanche of programmable logic architectures started with one bright idea: that sum-of-products combinatorial logic could be embedded in a chip's interconnecting circuitry. Since those original combinatorial devices, PLD vendors have shifted their attention from the interconnecting logic to the I/O macrocells, resulting in an almost obsessive fascination with increasingly complex macrocell designs. But recent product announcements from such vendors as Intel (Folsom, CA), Signetics (Sunnyvale, CA) and International CMOS Technology (San Jose, CA) have focused attention back on the interconnection scheme as a way to beat the growing complexity of PLD designs.

Several vendors, most recently Intel, have observed that in some applications only part of the interconnecting logic is really needed in a PLD. In address-decoding applications, the full sum-of-products structure isn't necessary—the product terms are used directly to enable the other chips in the system. So by stripping away all of the OR circuitry from the typical PAL design, these vendors can build an extremely fast address decoder.

The Intel 85C508 address decoder illustrates this principle. From 16 dedicated inputs, the chip derives eight product terms, via a single AND array. Each of these *p* terms goes unmodified through a transparent latch, clocked by an address-latch-enable signal, to one of eight dedicated outputs. The design's extreme simplicity liberates most of the potential speed of Intel's CHMOS IIIIE process, resulting in a 7.5-ns propagation delay.

Back to the full OR array

In its most recent device, Signetics has reexamined the sum-of-products interconnection for a different set of reasons. To meet the special needs of state-machine designers, the company has pioneered the use of fully programmable OR arrays, feedback

terms and buried registers. These innovations have mostly been offered in proprietary sequencer designs rather than in standard PAL-like formats.

But designers haven't exactly flocked to the proprietary Signetics sequencer designs. "People are still building sequencers out of conventional 22V10 PALs," laments Joel Rosenberg, PLD marketing manager at Signetics, "even though it means giving up all of the features intended specifically for state-machine designs."

Upon investigation, the Signetics team discovered that several factors contributed to this obstinate response. Some designers were simply unaware of the Signetics family. Others didn't understand the issues,

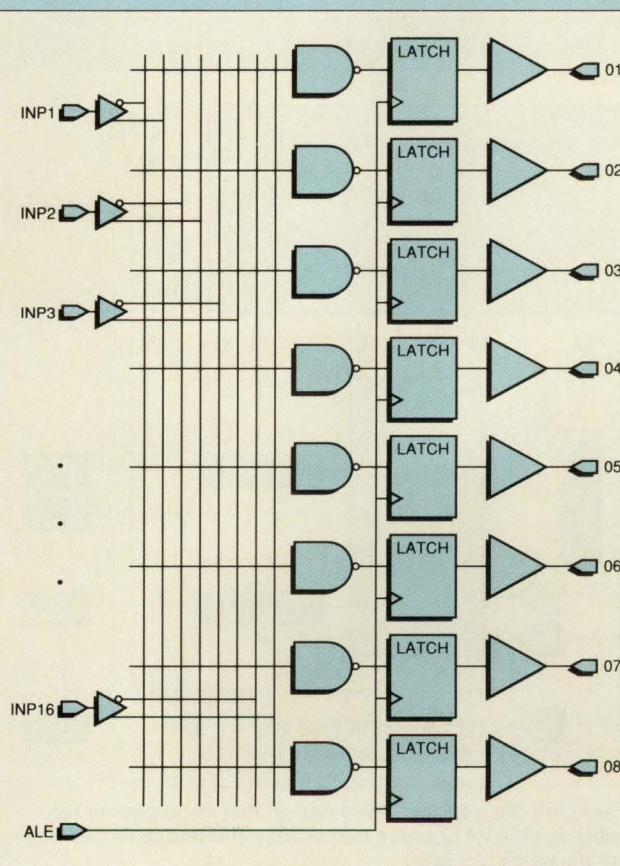
or didn't want to learn a whole new—and admittedly complex—part when they could get the job done with something familiar.

So Signetics decided not to fight it. The design team created a programmable sequencer, with all of the usual Signetics features, in the format of the ubiquitous 22V10. The part, called the 42VA12, may be the industry's first attempt to deal with both design problems and designers' problems.

The new part has the pinout of a 22V10. In fact, according to Rosenberg, the VA12 can use the same development tools and JEDEC files as a 22V10 when the new part's unique features aren't in use. "That compatibility, combined with the internal sequencer design features, should make the VA12 the next generic multifunction part," says product manager Kathryn Douglas.

In addition to the standard 22V10 AND array and configurable macrocells, the 42VA12 adds a number of specific improvements. Most obvious

THE INTEL 85C508



Programmable address decoders such as the Intel 85C508 eliminate one whole stage from the conventional PAL design, leaving a very fast device that brings *p* terms directly to the chip outputs. Via a single AND array, the chip derives eight *p* terms from 16 dedicated inputs.

INTEGRATED CIRCUITS

is the OR array, replacing the 22V10's notorious p-term allocation scheme with complete PLA flexibility. The new part also provides a complement-array term, as used in Signetics' sequencers, and elaborate control over macrocell flip-flop function and clocking.

Perhaps most significant for designers who must bury registers within their chips, the VA12 has altered the macrocell to completely isolate the flip-flop from the I/O pins. Each macrocell contains not only a flip-flop, driven by a pair of OR terms, but an additional, "bypass" OR term.

This latter term feeds back into the AND array, but it can also be routed past the flip-flop to the I/O pin. A macrocell thus can still drive its I/O pin with a combinatorial output, even if the macrocell is already being used as a buried register and a combinatorial feedback path.

Signetics hopes that the part's similarity to the 22V10, together with the added sequencer features, will appeal to designers who haven't used programmable sequencer parts

in the past. In many designs, the added features save not just p terms but whole packages.

Halfway toward gate arrays

While Signetics is working to widen the audience for its ideas on sequencers, International CMOS Technology (ICT) has also been reexamining the all-important interconnect of PLDs, but for yet another reason. ICT wanted to bridge a perceived gap between conventional PALs and denser field-programmable gate array designs.

"Users of programmable gate arrays have great flexibility and circuit density," says Robin Jigour, director of marketing at ICT. "But they often have to redesign and retest the circuit several times before it works, because the timing effects of automatic placement and routing can be so unpredictable."

These timing discrepancies can creep up in at least two ways, says Jigour. First, since the individual logic elements on field-programmable gate arrays have low fan-in, designs must use many levels of logic

to emulate a high-fan-in gate. Second, the placement and routing process itself can introduce significant unanticipated—and unsimulated—delays into a circuit.

ICT wanted to develop a PLD that could combine the density of gate array-like devices with the timing predictability and wide fan-in of conventional PALs. The company's pursuit took it back once again to the design of PLD interconnecting logic, to develop a synthesis of gate array and PLA architectures.

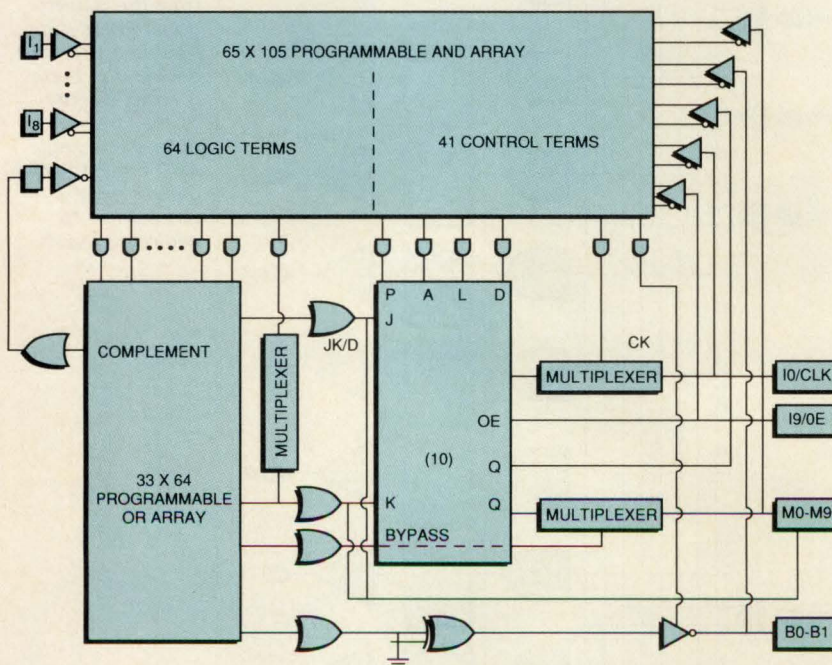
The result is the Peel array family. Like all other PLDs, the Peel arrays use a combination of interconnect and logic cells. But the topology of the new devices is unlike any other in the industry. Instead of a chip composed of a large AND array, perhaps an OR array, and a group of I/O macrocells attached to I/O pins, the Peel arrays are—like field-programmable gate arrays—an array of macrocells. But unlike field-programmable gate arrays, which don't embed logic functions in their interconnect, the Peel arrays use PLA-style sum-of-products interconnect.

Perhaps the most helpful way to visualize the device is as a huge conventional PLA, with both AND and OR arrays, but with a very large number of logic macrocells. The smallest Peel array has 20 cells, the largest 40. These logic cells aren't dedicated to any particular pin: a signal can be taken from either the flip-flop or an OR term in any logic cell to any pin. Similarly, any pin can serve as an input to the AND array. The design results in a dense, extraordinarily flexible logic array that retains the virtues of high fan-in and predictable delays.

The physical implementation of the device is quite elegant. There isn't a single AND array, but rather a series of AND array strips that go horizontally across the chip. Similarly, the OR array is broken into a series of vertical strips. This lattice of arrays forms a matrix of open spaces on the die, into each of which is placed a logic cell.

Each logic cell in a column draws four OR terms from the vertical OR strips to its left. Outputs from the logic cells in a column can go either to a pin-driver cell or to a vertical strip of input lines immediately to the right of the column. These input

THE SIGNETICS PLC42VA12



The Signetics PLC42VA12 may look like a typical 22V10 PAL on first inspection. In fact, the device is 22V10-compatible. But the VA12 adds a full OR array and several details in the macrocell design to increase the part's flexibility.

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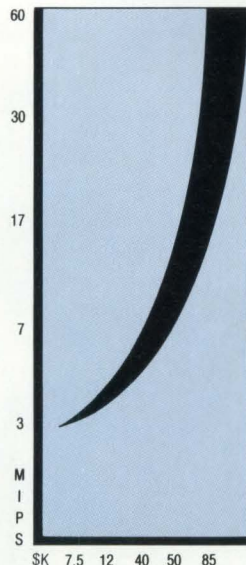
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INTEGRATED CIRCUITS

(continued from page 28)

lines make the logic cell output signals available to the horizontal AND strips, interconnecting the cells with the rest of the chip.

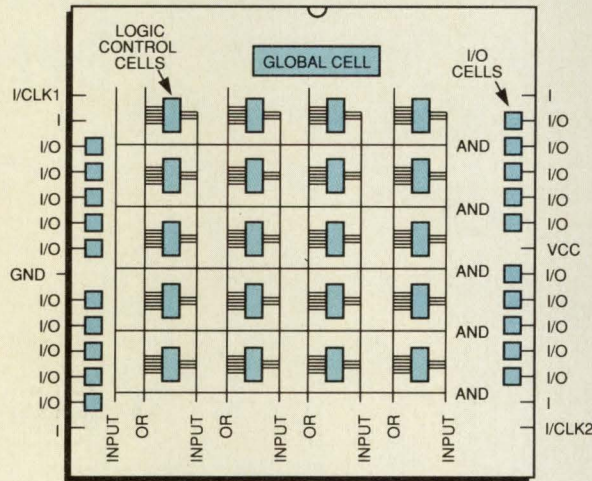
Any signal from an input pin or logic cell output thus can be routed to any logic cell or output pin through the sum-of-products array. ICT claims that the interconnect delay between any two cells is 17 ns,

faster in high fan-in applications such as address decoders or specific, well-ordered functions." Haines suggests that the ability of the PAL-type architecture to adapt to a particular configuration will encourage the development of very fast, application-specific PLDs.

"You can get high gate utilization in a conventional PLD only if you're doing something close to what the

Functionally, ICT's new Peel arrays are just very big PLAs with lots of macrocells. But it's easier to understand the power of this new design by thinking of the part as an array of macrocells embedded within a lattice of AND and OR buses.

THE PEEL ARRAY



independent of routing.

The range of PLD architectures is already somewhat bewildering to the casual observer. It almost seems as if every possible combination of interconnect strategy and logic cell design, from AND array interconnect with no logic cells to passive, gate array-style interconnect with huge macrocells, is available. What isn't available is a clear set of guidelines for choosing an architecture.

"The proliferation of architectures for high-density devices has been fast and furious," says Andy Haines, director of marketing at Actel (Sunnyvale, CA), "but I think this is only the beginning. About the only clear distinction remaining is between programmable gate arrays and conventional PLDs. In the arrays, wires aren't dedicated to logic blocks, so you end up with a more general device, better suited to implementing high fan-out circuitry like arithmetic elements or random logic.

"In conventional PLDs, interconnect gets dedicated to logic blocks. This can make the devices much

designer intended," says Haines. "The farther away you get, the lower the utilization. Programmable gate arrays, on the other hand, can deliver very high utilization over a wide range of applications. So in the end, the decision may come down to a trade-off between high board density and speed."

Of course, most designers would rather not have to make that choice. So we can expect to see further attempts, not only to produce fast application-specific PLDs, but to use innovative PLA structures in the pursuit of high-density, high-speed programmable logic. □

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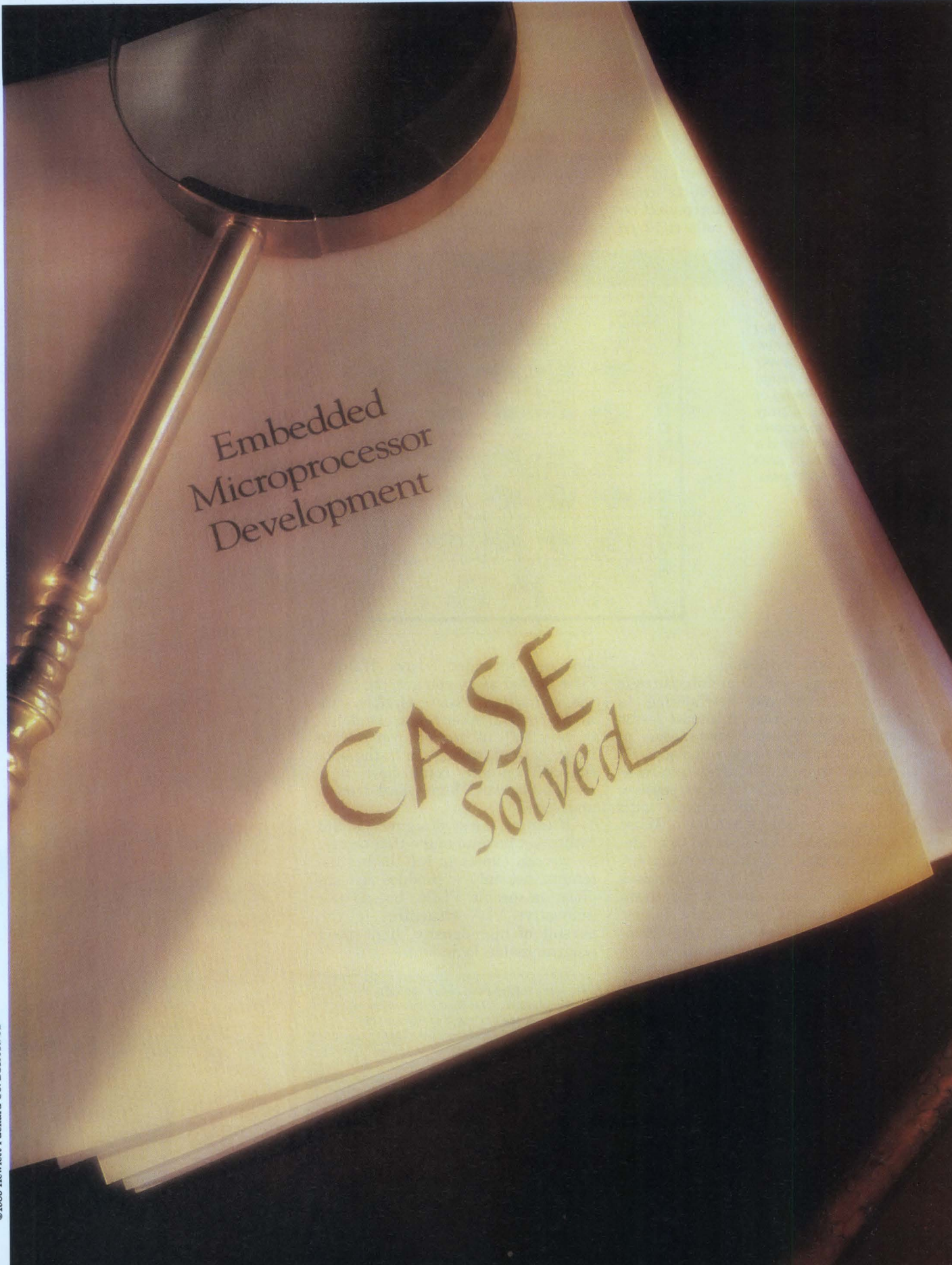
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CIRCLE NO. 19

POWER TOOL.



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CIRCLE NO. 20

RISC CPUs tune up for embedded computing

Ron Wilson, Senior Editor

Most first-generation RISC CPUs were clearly aimed at the Unix workstation market: they were deeply pipelined, register-intensive processors requiring elaborate MMUs and caches. But as vendors began to explore opportunities in embedded computing, they began to see a different set of design requirements. Now some RISC chips are responding more directly to the needs of embedded systems.

"The biggest benefit of RISC CPUs comes in servicing compute-intensive tasks," claims Jerry Fiddler, president of kernel developer Wind River Systems (Emeryville, CA). But speed needs to be blended with responsiveness. "Typically, a system will have some tasks that need to be optimized for throughput and some tasks that need deterministic response. If you're clever, a RISC processor will let you meet both those needs at once," Fiddler says.

The most recent entrant in embedded RISC computing is VLSI Technology (Tempe, AZ), a vendor perhaps better known for its cell-based semicustom products. But in addition to its application-specific IC lines, VLSI Technology has for some time offered what may be both the most imaginative and the most overlooked of the RISC processors, the Acorn RISC Machine (ARM).

Acorn (Cambridge, England), the British personal computing company, developed the ARM to meet the company's own needs in the low-cost PC arena. The chip uses RISC techniques not so much to achieve blinding speed as to achieve startling simplicity, and hence low cost, at the system level as well as in the chip itself. VLSI Technology recognized the potential of the ARM as an embedded processor and picked up North American marketing rights.

With the recent release of a second-generation ARM, Acorn has enhanced the CPU's performance and affordability, as well as added some features that will prove useful to embedded-system architects.

VLSI Technology calls the new

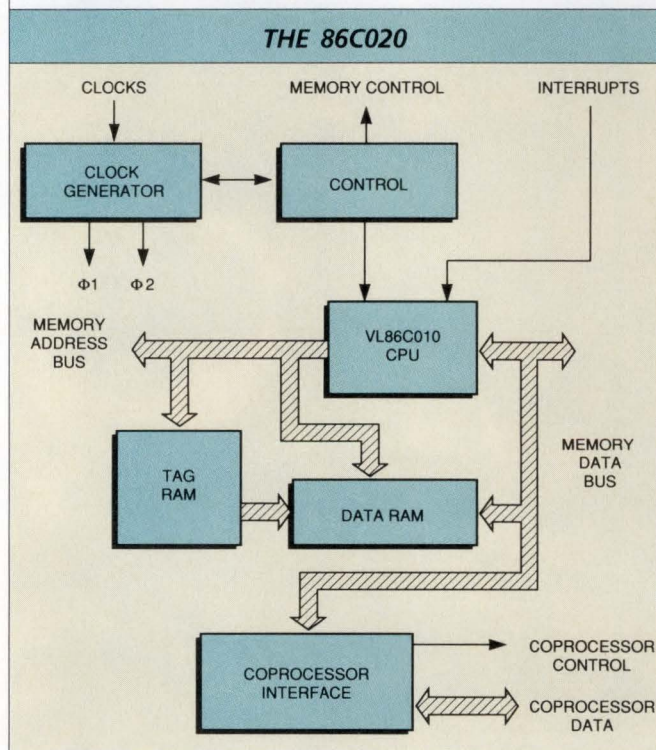
ARM the 86C020. The chip retains the RISC core processor from the earlier 86C010 but adds a 4-kbyte cache. Bringing the cache on-chip has significant advantages for speed, cost containment and chip count control, but it also raises some new issues.

The most obvious effects are on the plus side. "The on-chip cache decouples the CPU clock from the memory speed," explains Ron Cates, RISC program technical manager at VLSI Technology. "It lets us execute

have to cross a chip boundary to get to it, so the cache speed can scale up right along with the CPU speed."

But moving the cache on-chip creates some complications. The first question that comes up is what sort of cache should be built. There are many choices, covering size, organization, contents and so forth. Should there be separate code and data caches? Should the caches be direct-mapped, n-set associative or fully associative? How big should they be?

Not surprisingly, Acorn's research indicated that the best solution for most applications was a large, fully associative combined code and data cache. Unfortunately, the logic overhead for full associativity wouldn't fit on an affordable die. So the company worked out a compromise quite



By moving a sophisticated cache on-chip, the designers of the 86C020 RISC CPU have eliminated one of the nastier design jobs facing designers of embedded computers. In addition, the on-chip cache decouples CPU speed, and to some extent system performance, from main memory speed.

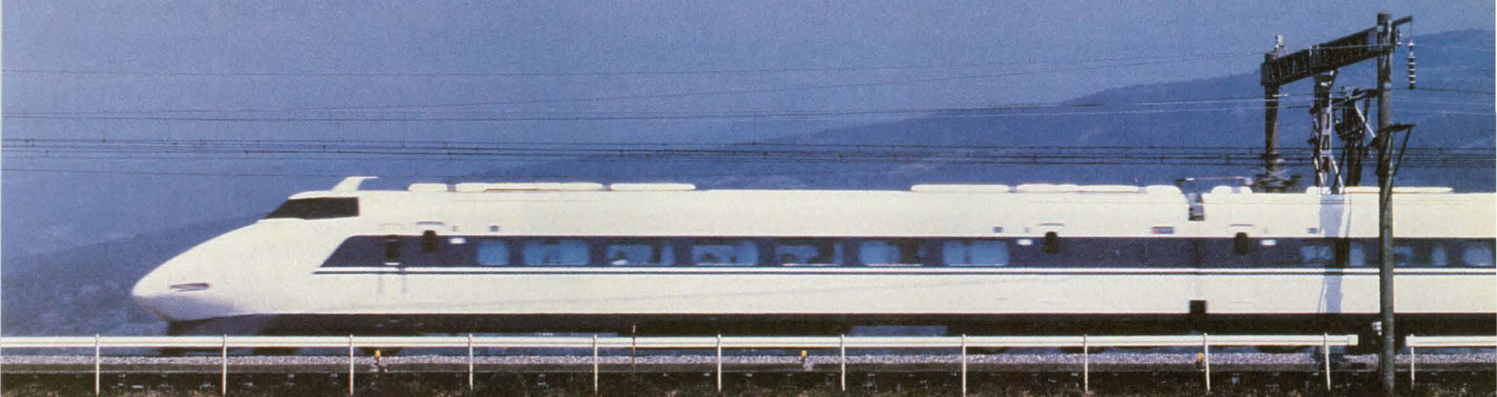
at high speed even with inexpensive slower RAMs, or execute directly from ROM without having to copy the code to faster memory first."

Cates suggests that this decoupling will become more important in the future. "Right now, we're building the 020 in our standard 1.6-micron process. When we go to 1 micron, we expect to see clock frequencies up around 30 to 50 MHz. Since the cache is on-chip, we don't

unlike any other in microcomputing: a mixed code and data, 64-way set-associative, write-through cache.

To minimize logic cost, the cache uses a random replacement scheme instead of the more sophisticated least-recently-used replacement algorithm. Acorn discovered that the difference in performance between the two algorithms was minimal. The fine-grain structure of the cache seems to adapt it to a wide range of

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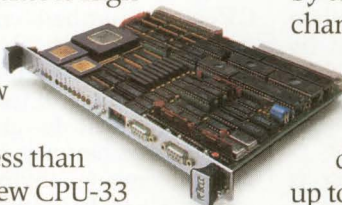
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INTEGRATED CIRCUITS

Despite multiprocessing's current popularity, some vendors wonder whether the applications really justify the added hardware for cache coherency in some chips. "Spending money on cache-coherency hardware that you don't use just doesn't make sense," says Ron Cates, RISC program technical manager at VLSI Technology.



computing needs, from computationally intensive routines to rapid context switches.

■ The coprocessor interface

But the choice of a cache strategy still leaves open some questions. One is what to do about the coprocessor interface. While coprocessors might not be all that common among VLSI Technology's embedded-computing customers, they're vital to Acorn's PC business. So the problem of how to expose the instruction stream to the coprocessor became an issue. Acorn decided to bring a copy of the cache data bus out to pins, so a coprocessor could monitor the instruction stream and trap its own codes. This cost a few pins but proved a much simpler solution than the alternatives.

The other big issue in on-chip caches involves multiprocessing. While multiple-CPU systems are a popular item of discussion in high-end general-purpose computing, they're a way of life in embedded computing. And if multiple devices, such as other RISC chips, microcontrollers or even DMA controllers, can alter system memory, the CPU needs to have some way of warning itself that the data in its cache is no longer valid.

The ARM chip hasn't dealt with this issue in hardware. "It's true that multiprocessing is the hot topic this year," says Cates. "But I wonder whether all the added hardware for cache coherency in some chips is

really justified by the applications."

Cates admits that some symmetric multiprocessors absolutely need bus-snooping hardware. "But most of our applications don't even use a DMA controller," he points out. "By taking advantage of the fast interrupt mode on the chip, our users are even handling high-speed data-moving chores on the single CPU. You can handle up to 100-kHz free-running interrupts with no problem. And when the object is to cut system cost by concentrating tasks on one chip, spending money on cache-coherency hardware that you don't use just doesn't make sense."

In cases where bus snooping is essential, the system designer's best approach is to start with the 86C010 CPU core and construct an ASIC solution that incorporates exactly the right caching strategy and coherency hardware for the application, suggests Cates. "A lot of these situations will be best served by ASIC technology," he claims.

■ RISC as a CPU core

The theme of the RISC CPU as the core in a semicustom chip is popular with at least one other major vendor, LSI Logic (Milpitas, CA). LSI offers standard-product versions of the Fujitsu-style Sparc CPU, the Cypress-style Sparc CPU and the MIPS R3000 CPU. In addition, the company has been offering the MIPS CPU as a library element for some time.

"We have a significant number of customers using the MIPS CPU in

embedded applications, and increasingly, they're asking for optimizations that require ASIC technology," reports John Reno, product manager for LSI's microprocessor group. "One obvious motivation is cost. About half of the MIPS chip is devoted to the MMU. If you're doing an embedded application and don't need an MMU, why not take it out, or maybe subset it to get just the protection features?"

Reno also sees a trend for caches to move on-chip. "A lot of people are putting a small, primary cache on-chip and then using a larger, secondary cache off-chip if they have to handle large data structures." He also observes a trend for designers to push complex control circuitry off the CPU chip. One way of doing this is to make the primary cache a simple write-through design and then use a more complex, copy-back approach in the secondary cache, for example.

Reno expects that the use of RISC cores in ASIC devices will grow slowly, becoming really important in three to five years. "Right now, standard parts are most important to us," he says.

But as the move toward RISC CPUs in embedded computing grows, and as it involves more ASIC designs, system architects will have to face a number of issues. Problems of optimal cache design, the best way to handle coherency in asymmetric multiprocessing environments, and even what to do about memory management remain to be solved.

For many of these issues, there probably are no single answers. Instead, the subjects will be at the center of an increasingly informed dialogue between chip vendors and system architects, two authorities whose turfs are beginning to overlap significantly in the realm of embedded systems. □

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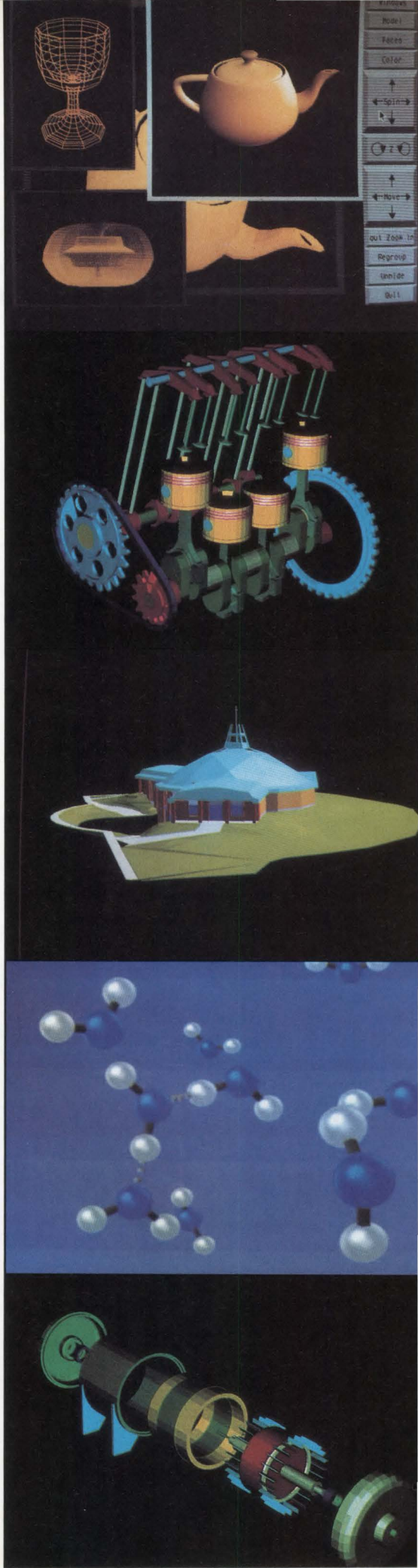
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CIRCLE NO. 24



GRAPHICS AND IMAGING

80860 may force rethinking of graphics system architectures

Tom Williams, Senior Editor

Just a short time after the formal introduction of Intel's 80860 RISC-based 64-bit microprocessor, user evaluations of the chip's potential are looking enthusiastic. Bruce Borden, vice-president of strategic planning for Ardent Computer (Sunnyvale, CA), calls the 80860 "the most interesting development in Silicon Valley in a year, maybe two." The chip's great potential is causing system designers to consider new approaches to system architecture and software.

Even companies that may already be committed to other RISC designs for their main CPUs are seriously evaluating the 80860 for a possible role as a coprocessor. In some cases, that would mean a coprocessor significantly more powerful than a system's main CPU. On-chip, the processor contains not only a RISC core, but also a vector floating-point multiplier, an adder and register set, a memory-management unit, data and instruction caches, and pixel-generation circuitry that's needed for shaded three-dimensional graphics.

Ardent, for example, is looking at the chip as a possible coprocessor for the Titan graphics supercomputer. The Titan has a multiple CPU based on RISC processors from MIPS Computer (Sunnyvale, CA). "We're going to stay with the MIPS chip and the MIPS instruction set for an integer unit," says Borden. "We're very concerned about binary compatibility," While binary compatibility can't be changed midstream, it can be extended without affecting the ability of existing software to run. The 80860 is a good fit for a role as a coprocessor for both number crunching and graphics, and Ardent will begin using the chip in such an auxiliary role.

As a number cruncher, the 80860 has been demonstrated on a Micro Channel card under joint development by Intel and IBM. The card, dubbed the Wizard, will be a Micro Channel master. A Wizard prototype running fractal graphics generated by Mandelbrot equations was on display

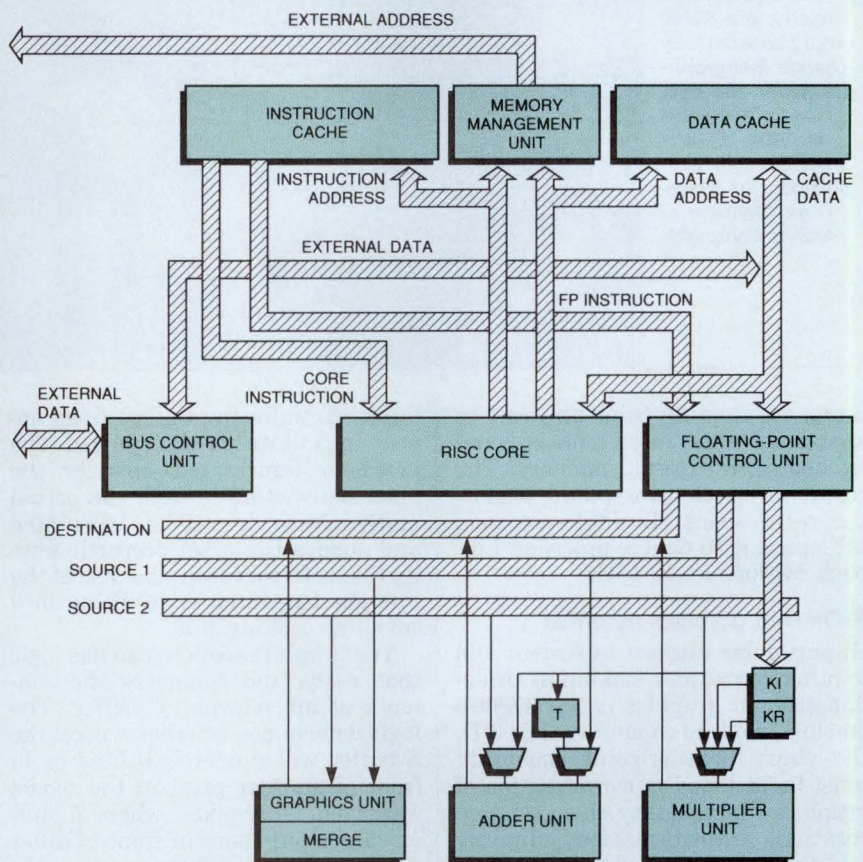
at the recent Uniform show.

Fractals require both heavy floating-point operations and graphics output. In the demo, the 80860 card running in a PS/2 386 machine outstripped several other workstations with RISC processors using externally attached floating-point units. One reason for this ability appears to be a degree of on-chip integration that answers the needs of many potential power users such as Ardent.

The 80860's degree of integration "solves a major problem that I've been harping on for years," says Borden. That problem is the slowdown caused by having to go off-chip for certain functions such as floating point or for memory references. Although the industry knows how to make very fast processors—40 MHz, 50 MHz in CMOS, 80 to 100 MHz with ECL—the speed gets bogged down when one tries to go off-chip. This slowdown is caused by varying combinations of external bus bandwidth, interface logic and the slower speed of memories—all of which have trouble keeping up with the speed of the processor.

Because cache control for both in-

THE 80860 MICROPROCESSOR



The Intel 80860 combines a very high degree of on-chip functional integration with parallelism among functional units to keep all sections occupied for optimal throughput. The on-chip efficiency is forcing designers to rethink their chips' external architectures to make optimal use of the 80860's capabilities, probably by implementing parallelism in the system design as well. The RISC core is rated at about 1.3 instructions/cycle. The 128-bit-wide path between the data cache and the floating-point control unit represents the widest on-chip data path in a microprocessor to date.

GRAPHICS AND IMAGING

structions and data, as well as for cache memory itself, is on-chip, there's enough cache—4 kbytes of instruction and 8 kbytes of data—for most inner loops to run entirely on-chip without tying up the already amazingly wide 128-bit internal data bus with instructions when executing. For floating-point operations, Borden notes, the cache is usually irrelevant since most matrices are larger than any cache.

Still, thanks to a large, flexible register set, a two-stage pipeline, and parallelism among functional

The 80860 is designed for Gouraud shading, in which a surface is defined as a set of connected triangular patches. The values of the pixels at each vertex of a triangle are taken as starting points for calculating the pixel values within the triangle by interpolating values between the vertices. The 80860 graphics section contains interpolation and adder logic to render 50,000 shaded 100-pixel triangles/s.

This same graphics section can also produce 100,000 vectors/s or 50,000 to 60,000 antialiased vec-

about six out of 16 cycles involving off-chip activity. Still, the amount of pixel processing that can be done from the cache represents a considerable speed advantage. The cache contains the pixel addresses and values and will only write pixel data to the frame buffer if the Z buffer comparison tells it that the cache's current pixel is in front of the one in the frame buffer, thus avoiding unnecessary frame buffer writes.

Using multiple 80860s

One might expect that an architecture like that of the 80860 would spawn some innovative design idea, and that is indeed the case. One company, Synergy Microsystems (Encinitas, CA), is developing a graphics controller that will use four 80860s. The chip's high pixel-rendering speed creates a problem in trying to use multiple 80860s to their full potential in a controller design, according to Jim Jonas, graphics manager for Synergy.

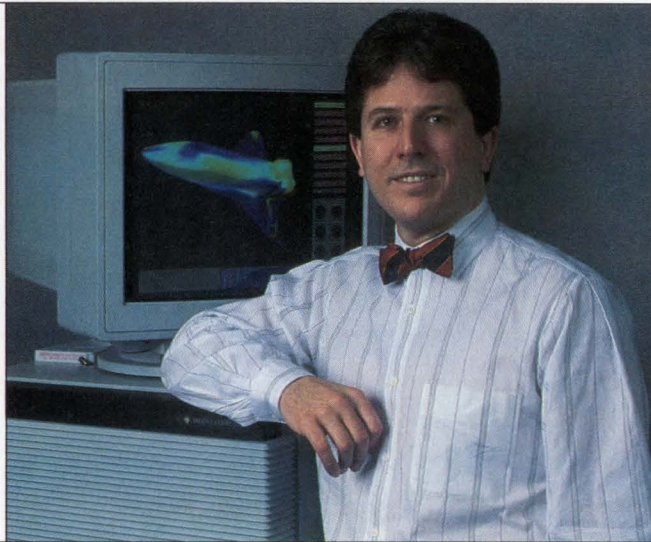
"In Gouraud shading, the problem isn't the calculations; it's the memory references and the burden they place on the hardware," Jonas says. In other words, bandwidth to external memory isn't wide enough to easily accommodate multiple processors trying to reference it. At 40 MHz, a single chip can output 160 million pixels/s.

In the Synergy design, three 80860s are intended for use primarily as drawing engines to render pixel data. A fourth 80860 will be used for floating-point operations to supplement the on-chip floating-point capacities of the other three and will keep the pipeline fed with triangles and vertices to be drawn as pixels.

To provide enough memory bandwidth, Jonas is using every trick in the book, including interleaving references to Z buffer and display memory among the processors, physically splitting the memory bus into two separate paths, and using a multiple page-mode memory scheme. "The thing that's the most trouble is the simple case, the one it's built to do—Gouraud shading," says Jonas. "Because it's so damn good at that, you've really got to stretch to get your memory to take advantage of its capability.

The problem of fully utilizing the

Intel's 80860 RISC chip could fill a need for three-dimensional graphics in the PC platform arena. With its pixel-generation circuitry, the 80860 could substantially change 3-D graphics within the next six to twelve months, predicts Bruce Borden, vice-president of strategic planning at Ardent Computer.



units, the floating-point unit can be kept busy while more data is being fetched from external memory. The result is a floating-point performance of about 80 single-precision MFlops and 10 double-precision Linpack MFlops at 40 MHz.

On-chip graphics potential

Of particular interest to Ardent and to other companies looking at three-dimensional graphics is the 80860's on-chip graphics capability. For 3-D, the chip's floating-point capability must be included in consideration of graphics functionality since scaling, rotation, transformation, clipping and the calculation of lighting models and viewpoints all require heavy amounts of floating-point calculations. But the 80860 also has circuitry to perform pixel calculations for shaded surfaces; the circuitry calculates the values that define the color of individual pixels and writes them to the frame buffer.

tors/s. Antialiasing makes lines appear smooth rather than jagged. The processor figures out how far the pixel it's writing is from the actual mathematical line it has calculated and shades the pixel proportionately. Pixels farther from the axis of the line are less intense, resulting in a smoother-looking line.

The graphics section also has logic that reads and compares the contents of an external Z buffer. The logic determines whether a pixel the Z buffer will render is behind or in front of another pixel in the model displayed. Only pixels whose Z buffer values put them in front of other pixels at the same 2-D screen coordinates are written to the frame buffer. Use of the Z buffer requires that triangle-fill routines access external memory both for Z buffer references and for frame buffer writes, even when executing in the cache.

The need to access Z buffer and frame buffer memory can result in



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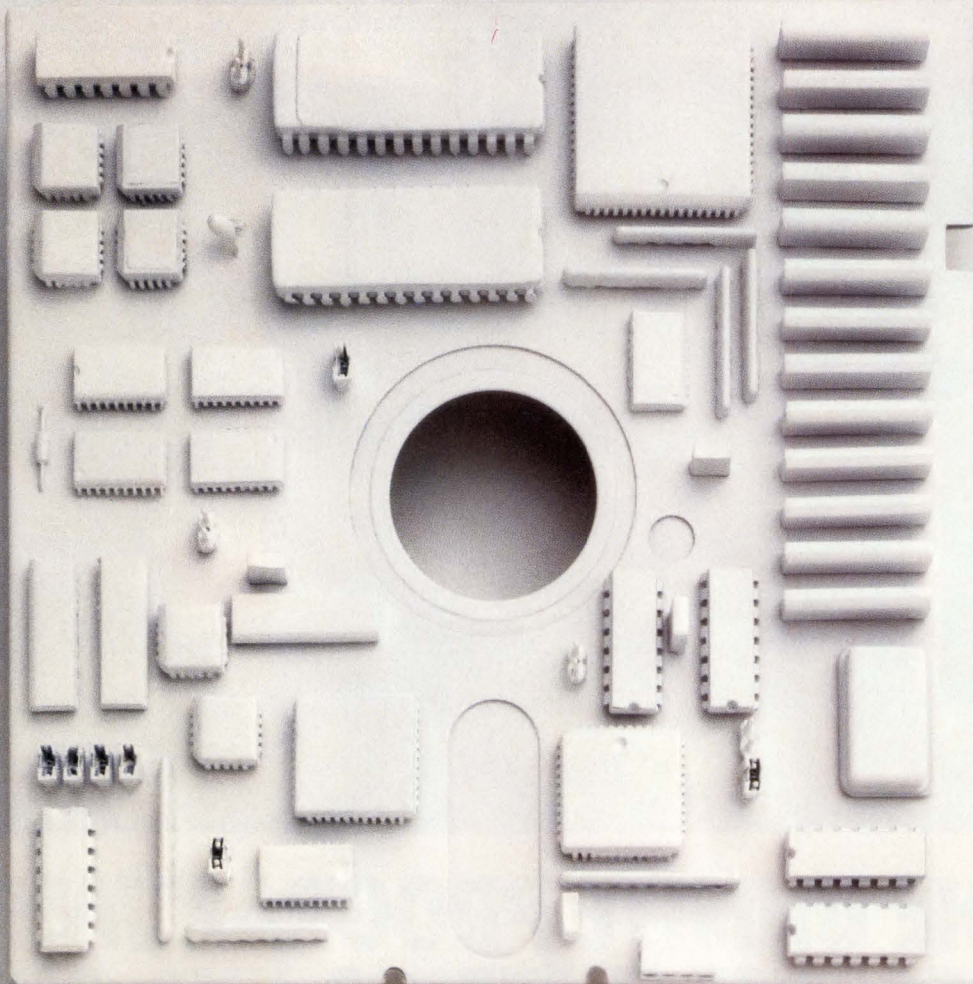
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GRAPHICS AND IMAGING

80860's potential decreases as the complexity of the graphics problem increases. In a more complex shading algorithm such as Phong shading or texture mapping, more of the chip's time is taken up with floating-point calculations, resulting in a closer balance between floating-point and pixel calculations. This leads to a somewhat slower pixel output that's more closely matched to available memory bandwidth.

Phong shading requires multiple floating-point calculations for every pixel rather than the value interpolation across a line of pixels that Gouraud shading requires. The floating-point calculations result in a considerable increase in computation load. "If you want to do a fancy calculation for each pixel, that's fine as far as I—the hardware guy—am concerned," Jonas quips.

Ardent's Borden appears to agree with Jonas's assessment of the pixel bandwidth issue. Ardent plans to increase pixel rates, requiring bandwidth in the Titan well beyond what the 80860 can do, but will take advantage of the chip's floating point and capabilities other than pixel generation. But Borden sees the Intel chip filling a role in the PC platform arena, where there's no serious 3-D graphics to date. "In 3-D today, there's nothing of any real interest on the PC. The 80860 will change that in the next six to 12 months," he says.

■ Economical 3-D color images

The existence of an economical engine that can render 3-D color images will be an important factor in letting 80386- and 80486-based PC platforms operate in the networked Unix environment with machines running the 3-D PEX extensions to the X-Window System. It will also mean that it will be possible to bring graphics software originally targeted at high-end workstations into lower-cost desktop systems.

Ardent has ported its Direct Object Rendering Environment (Dore) to the 80860. Dore is a general-purpose software rendering system that lets the user select the level of detail (for example, wire frame, flat facet, Gouraud or Phong shading, or surface mapping) in which to view an object. Synergy also plans to incorporate Dore in its product, which

will be a VME-based, three-board set consisting of a 68030 single-board CPU, the four-processor graphics controller and a 6-Mbyte, video RAM-based frame buffer board. If the memory access for the three drawing processors can be optimized, a speed of 150,000 Gouraud-shaded triangles/s is possible, Jonas predicts.

Although the user can choose a degree of detail and speed, Dore makes few assumptions about how various levels of rendering are performed. Figuring out how best to use the 80860's resources—essentially, how to implement the levels of rendering Dore can handle, in both single- and multiple-processor designs, will involve a learning process in system software design.

"A lot of the evolution will be in software," says Jonas. When the 80860 is used in a graphics coprocessing role, the host CPU will probably be relegated to very high level setting of global parameters and manipulation of display lists.

"There's no way even the fastest central CPU can think about adding just 1 to all the vertices in the time that this thing can draw the display list. There's no way the hottest processor can even DMA a new list in time on the VMEbus, even if you've already calculated it somewhere else," Jonas says. The host will thus be managing the relationship between clusters of triangles and setting viewpoint registers and global display parameters, for example.

At this point, it sounds as though anything approaching a complaint designers may have about the 80860 stems from the fact that its capabilities call for new design approaches that mean rethinking basic architectural assumptions—in both hardware and system software. As Synergy's Jim Jonas puts it, "The thing that surprises me most about this is that it does have the kitchen sink." □

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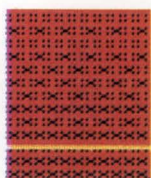
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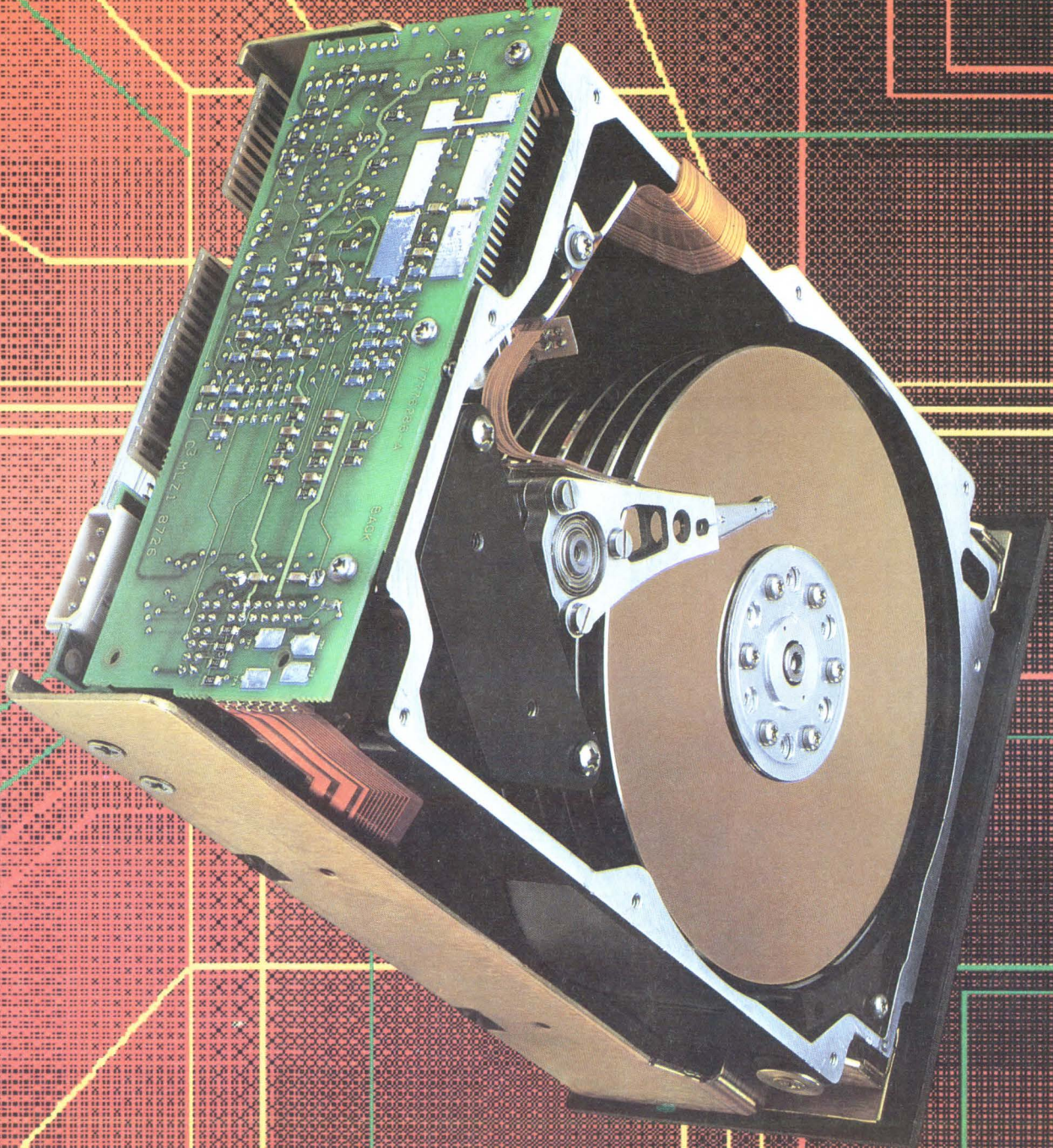
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CIRCLE NO. 28



Integrated environment eases development of military systems

Tom Williams, Senior Editor

A complete environment for developing, characterizing and debugging MIL-STD-1750A computer systems has resulted from the joint efforts of four companies supplying integrated hardware and software development tools.

The environment is built around the Orbiter 1750A coprocessor board from Sabtech Industries (Yorba Linda, CA). The board plugs into an AT-compatible bus and uses a two-chip set from LSI Logic (Milpitas, CA) that fully implements the 1750A instruction set. Grid Systems (Fremont, CA) supplies an 80386-based portable computer for field engineering and development, and Ready Systems (Sunnyvale, CA) provides development software and operating systems for real-time Ada embedded applications.

The 1750A, a 16-bit instruction-set architecture developed by the Society of Automotive Engineers, has been mandated by the U.S. Air Force for use in real-time embedded systems for avionics and control of air- and spaceborne systems. Since MIL-STD-1750A defines an instruction-set architecture, its implementation doesn't place constraints on pin designations or the physical partitioning of functions. Developers thus often have to find or build a computer on which to develop code, then port software development tools to the new environment, a process that can consume several engineer-years. The four-vendor offering is intended to provide a one-stop shopping approach so the OEM can start developing code right away.

The LSI Logic implementation, used on the Orbiter board, is implemented as two chips: the L64500 CPU and the L64550 memory and block protect unit peripheral device. The L64550 contains both a memory-management unit and a block protect unit with protection RAM, a memory fault status register and a start-up ROM interface. Since the military standard specifies compliance with an instruction set, software developed on the LSI Logic

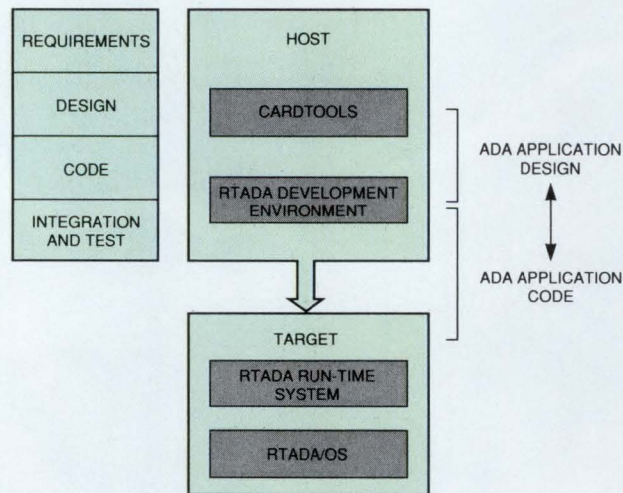
chip set will run on other hardware implementations that fully comply with the MIL-STD instruction-set specification.

The LSI Logic chip set was particularly attractive for use in Sabtech's Orbiter board because of the high degree of integration—MMU and block protect unit in one chip. But the fact that the chip set is a CMOS implementation was even more important, according to Rahim Sabadia, president of Sabtech. "We needed the capability to put more than one board in a single PC without worrying about the power supply," Sabadia says. With multiple boards, designers can more easily model avionics and control systems

The Orbiter itself contains up to 2 Mbytes of dual-ported RAM. The designer has the option of mapping the board into the 384-kbyte memory space above the 640-kbyte DOS limit or into DOS program space. Multiple boards can look into PC memory and pass data among themselves.

The significance of mapping the board into PC memory space is that it gives the designer access to the 1750A's internal registers and memory without disturbing software running on the Orbiter. This transparent access "lets external stimulus be injected into the Orbiter as it would in a real environment," says Sabadia. That permits a different approach to modeling and algorithm verification than just writing and debugging code and then subjecting that code to isolated test cases to check whether it works. With the ability to jump into the system from the PC, random and worst-case scenarios can be tested on

THE RTADA ENVIRONMENT



The RTAda development environment from Ready Systems is a host- and target-based set of integrated tools that span development needs, encompassing everything from requirements analysis to the integration and test of the target hardware. The environment includes Ready's RTAda operating system, adapted especially for the Orbiter 1750A coprocessor board from Sabtech Industries.

that consist of several interacting 1750A-based computers.

The Orbiter is supplied with two 50-pin bus connectors that allow direct access to the native bus of the L64500 CPU for hardware prototype and interface development. But the board is also accessible in a transparent mode via the memory of the PC. The board occupies a sliding 64-kbyte window that can be located anywhere in available PC memory.

very complex systems to see how they hold up.

Software support

Supplementing the Ready Systems software, Sabtech supplies software support in the form of an assembler and debuggers that run on the PC. Sabtech also recognizes that most 1750A development tools are hosted on minis and mainframes, however, and that there's a need to preserve



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COMPUTERS AND SUBSYSTEMS

access to those resources.

Most 1750A programs hosted on VAXes and mainframes are in the Integrated Tool Set (ITS) file format specified by the Air Force. Sabtech's ITS program loader can be used to transfer executable code generated

by compilers on minis and mainframes to the PC environment. Once downloaded to the PC, the code will execute on the Orbiter in real time, according to Sabadia.

The software development contribution from Ready Systems consists

of Ready's Computer Aided Real-time Design Tools (Cardtools) and the Real-Time Ada (RTAda) development environment that provides a range of Ada tools for both the host and target systems. In addition, Ready supplies a real-time Ada operating system (RTAda/OS) to run the LSI silicon on the Sabtech board.

Cardtools is a host-based toolset for support of requirements analysis and real-time design methodologies via a graphical user interface. The user can manipulate data-flow diagrams that also provide exact timing information and show the interaction of code modules via semaphores, mail boxes, flags and so forth.

When Cardtools is used to complete a design, the resulting Ada code can be compiled and debugged using debugger, target environment simulation and profiler tools that run on the host—either a VAX/VMS or Sun-3 workstation. The target simulation environment gives the designer the option of developing software and hardware simultaneously by simulating hardware behavior in software. On the other hand, the RTAda run-time system lets the designer implement deterministic, predictable algorithms on the target hardware itself and provides fixed timing for task rescheduling, synchronization primitives and rendezvous calls and intercepts.

The Sabtech Orbiter with its support software and the Ready Systems' real-time Ada support can run in any PC-DOS-/AT-compatible environment, but Grid Systems also supplies a 12.5-MHz 80386-based laptop computer with a snap-on/off expansion tray that provides for two expansion card slots. The four companies have stated that a bundled system based on the Grid computer will be available in addition to whatever individual components (chips, boards, software) customers need. □

RISC

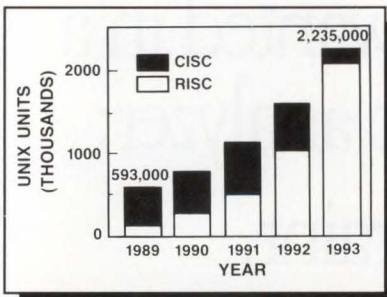
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CIRCLE NO. 30

Timing verifiers branch out to overcome analysis constraints

Bill Harding, Senior Editor

Timing errors, not functional errors, now account for most of the failures that occur when a new application-specific IC is plugged into a system. Locating and identifying timing problems is the job of timing verifiers, but traditional timing verifier technologies suffer from limitations that reduce their usefulness for both ASIC and system timing analysis.

Most timing verifiers are either dynamic or static. Dynamic timing verifiers can analyze any type of circuit, but they require test vectors to excite any path that the designer wants to analyze. Static timing verifiers require no test vectors and locate all timing errors, but they also locate and report errors in paths that are never used.

To overcome the limitations of traditional timing verifiers, some companies now offer hybrid tools that combine the characteristics of dynamic and static timing verifiers in a single package. Gateway Design Automation (Lowell, MA), for example, mixed both types of techniques in its recently introduced Veritime timing verifier. Veritime can be used as a standard static timing verifier or as a simulation-driven path analyzer for timing analysis of designs at the gate level or at higher levels of abstraction.

Epic Design Technology (Santa Clara, CA) took a similar approach with its upcoming Verimill timing verifier, a tool that targets transistor-level timing analysis of digital IC designs. Veritime is available now, while Verimill is scheduled for formal introduction later this year.

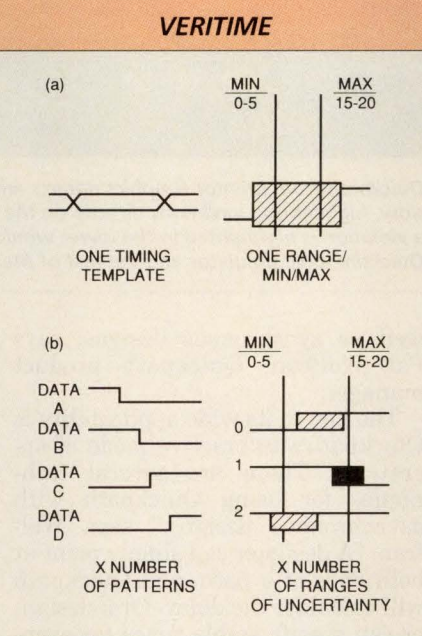
■ Min/max simulators

Dynamic timing verifiers are built into many logic simulators. These so-called min/max simulators have timing characteristics included in device-simulation models, giving them the ability to perform timing verification during simulation. ValidSIM from Valid Logic Systems (San Jose, CA) and Verilog from Gateway Design Automation, for ex-

ample, are min/max simulators.

Dynamic timing verifiers work with just about any type of circuit, either synchronous or asynchronous. The verifiers accurately (within the limits of their models) analyze the paths that are excited by the simulation test vectors.

But the test-vector requirement causes problems in dynamic timing



The Veritime hybrid timing verifier (a) from Gateway Design Automation mixes both static and dynamic timing verification in a single tool. Veritime uses a timing template as stimulus to the dynamic timing verifier rather than the detailed test vectors that are required by min/max simulators (b).

verifiers. The timing verifier won't analyze any path that isn't excited by the vectors, so some critical paths may be missed. As Ben Tang, simulation product manager at Valid, points out, "If you already know that a path is long, you can excite it and cause it to fail. But what happens if you don't know that it's long?" Finding long paths without the need for test vectors is the province of static timing verifiers.

Static timing verifiers use an approach that's completely different from that of dynamic timing verifiers. Static timing verifiers don't require test vectors of any sort, so they can locate and analyze any signal path in a design. A static timing verifier traces all paths between memory elements in a design and calculates their delays. It can analyze only the longest and shortest paths (critical path analysis) or it can analyze all paths (exhaustive path analysis).

The ability to locate all long and short paths is a mixed blessing, however. Static timing verifiers tend to be pessimistic in their analysis of a design; they don't miss any critical paths, but they may report errors on paths that are never used. When that happens, the engineer must interpret the error report accordingly.

A second problem with static timing verifiers is that they can't analyze all designs. A static timing verifier is very fast and very accurate, but it works best on synchronous designs with relatively simple clocks, according to Valid's Tang. "If a designer is willing to abide by very strict synchronous design rules, static timing analysis is a very powerful tool," says Tang. "Computer designs tend to be synchronous, but just about all other designs have asynchronous elements that make it difficult to use static timing verifiers."

■ Combining static and dynamic

Hybrid timing verifiers attempt to overcome the major limitations of both dynamic and static timing verifiers. A designer can use a hybrid timing verifier on any type of circuit, either synchronous or asynchronous. When used on designs containing asynchronous elements, hybrid timing verifiers require test vectors to excite asynchronous control and timing paths, but allow synchronous portions to be analyzed using static techniques.

When Gateway's Veritime is used as a static timing verifier, it requires no test vectors. When it's simulation-driven, however, Veritime needs a small set of test vectors to exercise control and clock logic, and define data states.

"Mixing simulation-driven timing analysis with static timing analysis lets Veritime analyze both synchro-

DESIGN AND DEVELOPMENT TOOLS

nous and asynchronous circuits," says Prabhu Goel, president of Gateway. "It also lets the designer isolate certain segments of a design for analysis."

In its simulation-driven mode, Veritime requires timing analysis "templates" that serve as test vectors to the design. A template usually consists of simulation patterns to activate timing and control signals for the segment of logic to be analyzed, and a description of when data paths are stable and when they may be changing, but no specific data values since Veritime analysis isn't data-dependent.

Veritime simulates the design using the timing analysis templates. When the simulation activates the inputs to a storage device, Veritime traces back along the paths from the storage device to the input sources. Since paths are analyzed only if they cause a change at an input to a storage device, false timing errors are less likely to be reported.

■ Pros and cons of hybrids

Critics of the hybrid approach claim that it suffers from the same limitations as dynamic timing verifiers do because using test vectors means that some critical paths may be missed. Proponents of the hybrid approach point out that while a hybrid timing verifier simulates clocks and

"The move toward synchronous designs means a greater reliance on static timing verifiers."

—Dick Kaiser, Mentor Graphics



control logic fully, it doesn't do full logic simulation. It isn't necessary to apply specific data patterns to data paths, so it's less likely that critical paths will be missed.

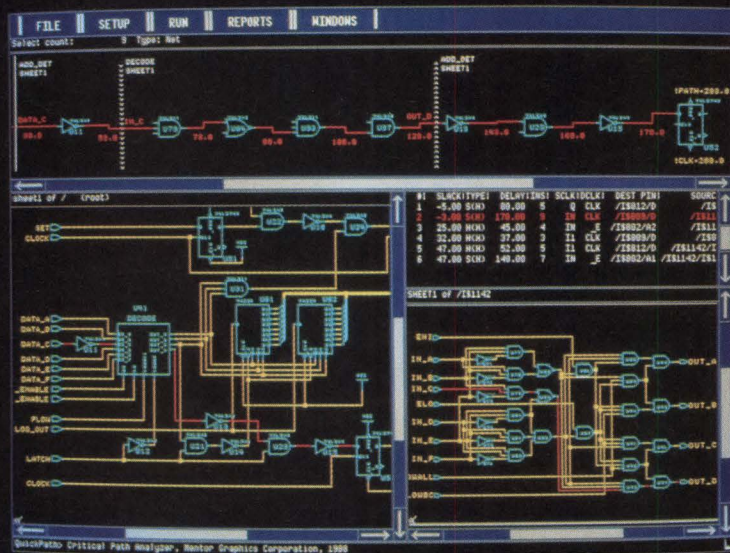
A second criticism of hybrid timing verifiers is that they really aren't that new; some static timing verifiers have many of the capabilities that are claimed as "new" in hybrid tools. Quickpath from Mentor Graphics (Beaverton, OR), for example, is one verifier that can perform timing analysis on asynchronous as

well as synchronous designs, says Pat Wolfran, Quickpath product manager.

The key to its wide applicability is Quickpath's interactive mode of operation. "There are several techniques for using Quickpath with asynchronous designs," says Wolfran. "A designer can simply point at both ends of a path, and Quickpath will calculate the delay. Or a designer can specify stable times for asynchronous paths in a design and then run a Quickpath analysis on the design using those specifications."

Quickpath lets the designer selectively enable and disable the analysis of segments of logic. This lets designers concentrate on troublesome design segments, or turn off segments that are exhibiting false errors.

Graphical displays can help designers evaluate error reports and sort out false errors. Quickpath displays troublesome logical paths in their entirety, including hierarchical moves. This type of display lets a designer evaluate the path and determine whether a reported error on the path is real or false. Such evaluation is much more difficult if the path is displayed only as a text file.



Quickpath from Mentor Graphics detects any design path that's either too fast or too slow, highlighting violations directly on the schematic for easy recognition. The path of a violation is highlighted in the lower window. Quickpath is fully integrated into the Quicksim logic simulator and the rest of Mentor's design and analysis toolset.

The Chiprafter timing verifier from Seattle Silicon (Bellevue, WA) also allows interactive analysis of asynchronous as well as synchronous designs. Part of the company's Chiprafter compiler tools, the timing verifier is a static tool with both critical and exhaustive path-analysis algorithms. To reduce false error reports, a path-disable utility lets designers disable illogical paths. To facilitate asynchronous circuit analysis, users can assign states to primary inputs.

Dick Kaiser, a product manager at Mentor Graphics points out that design managers are moving toward synchronous designs, thus enhancing the appeal of static timing verifiers. "Complex structured designs are easier to implement using synchronous techniques, and synchronous designs can more readily accommodate designed-in testability such as scan paths," he says. "The move toward synchronous designs means a greater reliance on static timing verifiers in the future."

■ Special problems with ICs

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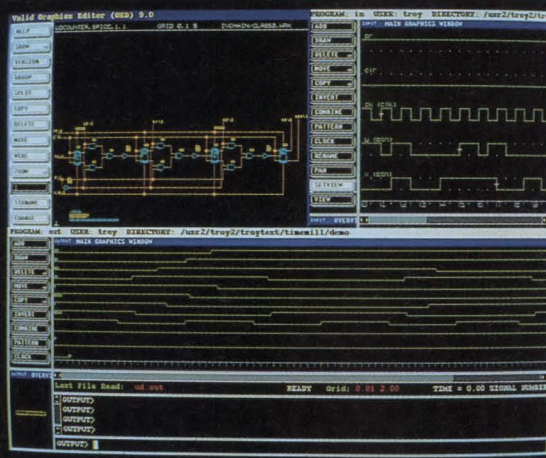
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trol signals. All other signals are handled using static techniques.

A matter of time

The available timing verification tools aren't perfect solutions to timing problems. Dynamic timing verifiers can miss timing errors if the designer doesn't include the right test vectors. Static timing verifiers can report false errors because they report every long signal path, regardless of whether the path is used. With these limitations, a designer who can develop effective test vectors or weed out false error reports will be able to use today's timing verification tools most effectively.

There's no one "right" timing verification tool that will handle every timing analysis problem. Hybrid timing verifiers with their limited use of test vectors and their ability to analyze both synchronous and asynchronous designs may well be the first step toward a more universal class of timing analysis tools. But for pure synchronous designs, a static tool may still be the best solution. In the final analysis, it's up to the engineering manager to match the tools to the tasks at hand. □

customers say that they want to make chips run faster, but they have trouble locating the critical delays that limit performance," says Sang Wang, president of Epic Design Technology. "That's causing a greater interest in timing verifiers among both chip designers and chip manufacturers."

Timing verifiers that work at the gate level can't test full-custom and cell-based IC designs adequately. An individual IC doesn't contain gates; it contains transistors that happen to make up gates and flip-flops. The timing limits on an IC have to do with the characteristics of transistors, so transistor timing must be analyzed to extract maximum performance from an IC design.

For years, IC timing verification depended on the experience and intuition of the design and layout engineers. "You would eyeball an IC layout and try to figure out where the longest path was," says Donna Rigali, Valid's product manager for IC design tools. "Then you would run Spice simulation on that path to determine its timing characteristics." Although Spice simulation could be run on an entire IC and would produce a very accurate picture of the IC's timing characteristics, few designers would want to put a design containing 500,000 transistors through a Spice simulator.

The same timing verification algorithms (dynamic and static) that work at the gate and behavioral levels work at the transistor level, except that the transistor model must include some of the transistor's analog characteristics. "A transistor on an IC looks exactly the same in

an analog circuit as in a digital circuit," says Dave Millman, marketing vice-president at Epic Design Technology. "To determine a transistor's timing characteristics, you must model the analog characteristics that affect timing."

For IC-level timing analysis, Epic provides three tools: Timemill, a dynamic timing verifier; Pathmill, a static timing verifier, and the soon-to-be-introduced Verimill, a hybrid timing verifier. Valid Logic Systems also markets the Epic timing verifiers as part of the Valid set of IC design tools.

Timemill is an event-driven, switch-level simulator that models the resistance and capacitance properties of transistor circuits to determine their timing characteristics. Timemill also keeps track of internal voltages, such as the voltages in RAM sense amps. Because it's event-driven rather than timeslice-driven, and because it doesn't model all of the analog properties of transistors, Timemill is much faster than Spice simulators. A 50,000-gate design, for example, can be evaluated in about 10 minutes on a Sun-3 workstation.

Pathmill is a static critical path analyzer for IC designs. In much the same manner as the tools that work at the gate level and above, Pathmill locates and identifies critical, performance-limiting paths in IC designs.

A hybrid timing verifier, Verimill can handle IC designs with multiple clocks and multiple clock cycles. Similar to Gateway's Veritime timing verifier in both name and capabilities, Verimill will dynamically handle all signals that need states for analysis, such as clocks and con-

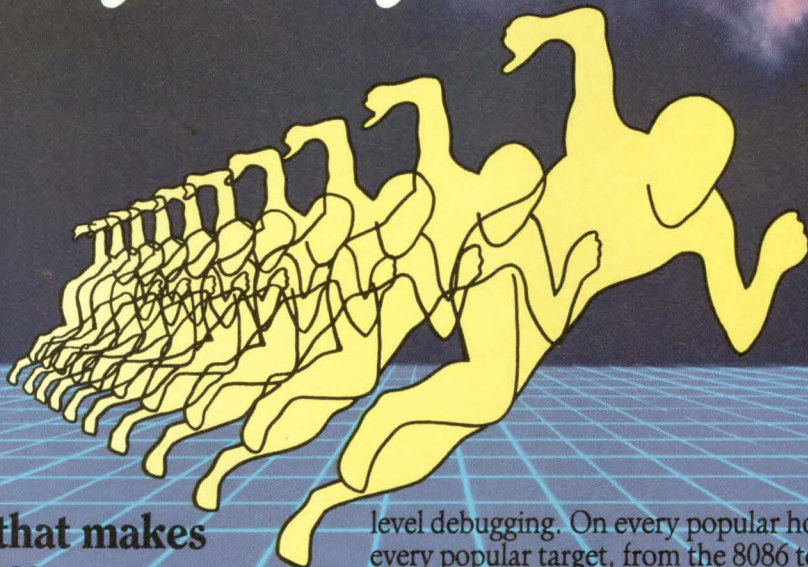
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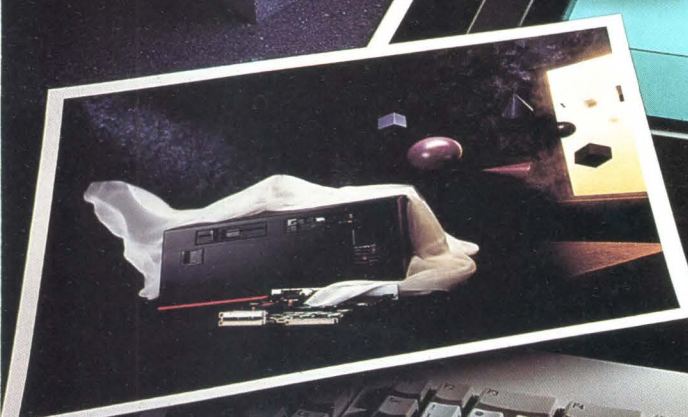
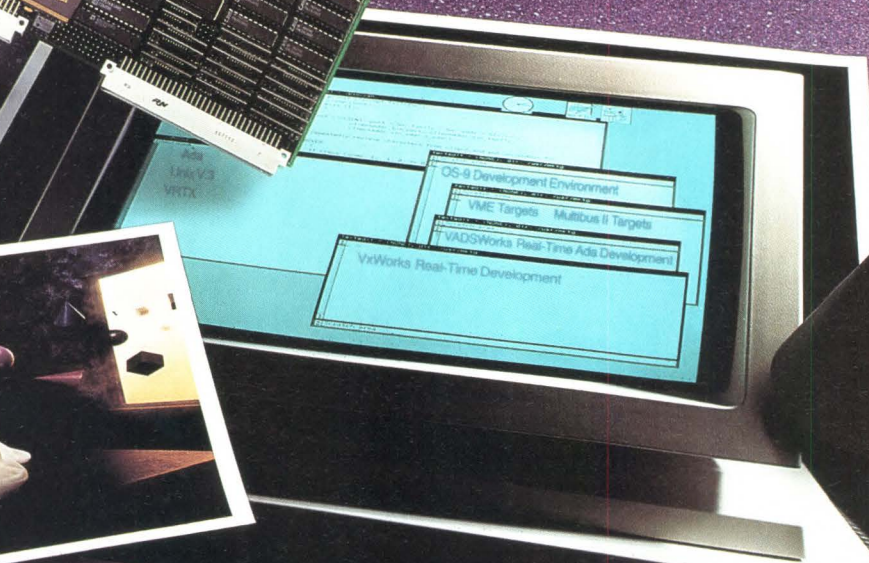
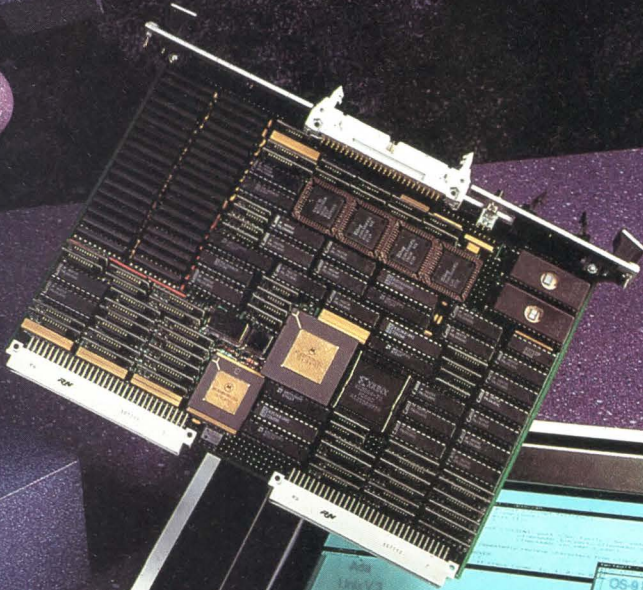
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CIRCLE NO. 32

DESIGN AND DEVELOPMENT TOOLS

Technical publishing tools streamline documentation process

Bill Harding, Senior Editor

Engineering managers are well aware that the job's not over until the paperwork's done, but the paperwork on even a moderately sized design can be staggering. With regulations such as those laid down by the Department of Defense (DOD) for weapons systems and by the Federal Aviation Administration (FAA) for commercial aircraft, an engineering manager may well face a documentation problem that rivals the design job itself.

Runaway design complexity can be blamed for most of the engineering manager's documentation problems. Since it's very likely that designs will become even more complex in the future, the electronic engineering manager can expect to see documentation requirements increasing rather than decreasing.

Electronic technical publishing

The massive problems associated with producing documentation in a timely manner prompted the emergence of a new class of tools called electronic technical publishing (ETP). Don't confuse ETP with desktop publishing. ETP includes many desktop publishing capabilities but goes far beyond the process of generating printable pages.

"At one time, a word processor was an effective technical publishing tool," says Bruce Foster, product line manager in the Context Division of Mentor Graphics (Beaverton, OR). "Today, writing technical documents is a team process that requires group productivity tools. It's also a massive, complex process that requires document management tools, and it's an exacting process that requires tools to help meet contractual requirements or government regulations."

Like a word processor or a desktop publishing system, an ETP toolset must provide certain basic capabilities, according to Foster. Integrated text and graphics, and graphics creation and editing are obvious requirements. For large documents, automatic section numbering with

automatic renumbering following revisions is a necessity.

An ETP system should automatically generate matter such as tables of contents, lists of figures, and indexes. Since many documents, such as parts catalogs, contain large numbers of tables, an ETP system should have a tool that helps with table creation and editing. To bring existing documentation under electronic control, an ETP system should support image scanning and optical character recognition.

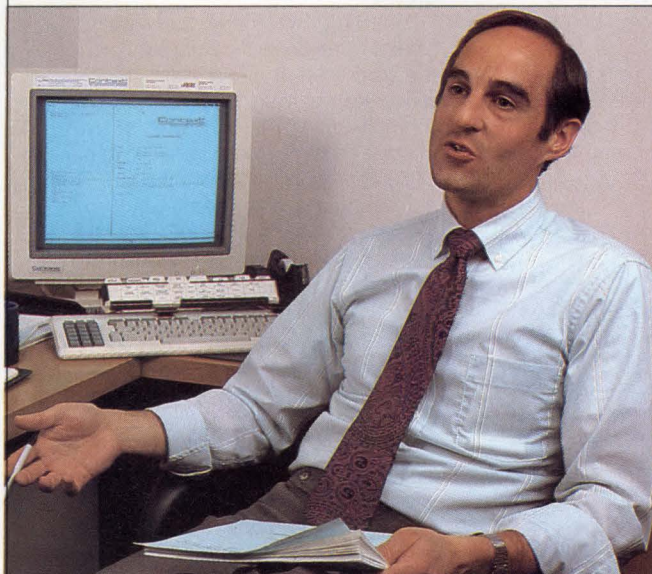
Mentor's Context Division offers a set of ETP tools—Context Writer, Context Editor and Context Documentor—that support a procedure called inclusion by reference. This procedure may be used to handle a schematic that may be kept up to date by the engineering department but needed in a maintenance manual, for example. Rather than copy the schematic from the engineering system to the publishing system, the writer of the manual can include the schematic by simply telling the ETP system the schematic's location. The schematic is then copied only when a manual is ready to print. By maintaining only one master copy of the schematic, the documentation automatically includes any changes

made by the engineer.

ETP tools must provide a way to access data from outside the documentation group. For Context ETP tools and Mentor EDA tools, direct contact can be maintained via the engineering network. But sometimes other tools are used to generate text or drawings. In this case, a graphics gateway is used to import the information. External data brought into the Context system via the gateway can't be included by reference (that data isn't automatically updated in the Context system when it's updated in its original system), but it can be processed and included in finished documents.

If an ETP facility is implemented on a network with access to the engineering network, on-line reviews of documents are feasible. In the Context system, security procedures can be invoked that let reviewers check a document in a read-only mode, but with the ability to add annotations or comments to the document without changing the document's text.

In a manner similar to what occurs in desktop publishing systems, templates can be set up to define the format for documents. If a system is being designed under government contract, the DOD-mandated CALS (Computer-aided Acquisition and Logistic Support) standards may apply (see "DOD standardizes documentation process," p. 60). If that's the case, templates conforming to the CALS standards may be pre-



The engineering documentation process has changed a great deal in recent years. Documentation has become "an exacting process that requires tools to help meet contractual requirements or government regulations," says Bruce Foster, product line manager in the Context Division of Mentor Graphics.

DESIGN AND DEVELOPMENT TOOLS

pared and will automatically be used for all document preparation. The template may effectively outline how a document is to be prepared, thus letting technical writers "fill in the blanks" when preparing segments of a document.

Managing the load

To help manage the documentation effort, ETP tools help with structure maintenance, change control, and file security and access control. ETP systems should provide a means for limiting document access (such as a password or other identification scheme) and should also provide a way to limit what can be done to a document.

Access rights may change as a document progresses through its life cycle. In the very early stages of document preparation, a particular engineer—as well as the author—may have the right to change a document. That right may be changed to read-only as the document approaches the first review

cycle. Once a document is in sign-off, a writer may be denied access rights.

Many elements of structure maintenance are handled automatically in an ETP package. The Context package, for example, automatically rennumbers nested sections and lists whenever changes are made to a document. It also automatically updates embedded references such as a reference to a table or figure. If the table or figure designation is changed, the embedded reference is changed accordingly. Much as a CAE system can automatically generate an engineering netlist, Context can automatically generate a table of contents, a list of tables and a list of figures.

Keeping track of changes

Any product that has a relatively long life, such as a commercial aircraft or a weapons system, will probably undergo numerous changes. Getting the changes documented and distributing the changes and the documentation to the field is a sig-

nificant problem.

"Failing to distribute changes in a timely manner can be very costly to the customer," Context's Foster said. "If an FAA investigator finds written notes in the margins of an airline maintenance manual, for example, the airline is subject to a stiff fine. Mechanics don't define how aircraft should be repaired; engineers do. And they publish their decisions in change notices."

An ETP system helps manage the document change procedure by maintaining an audit trail and keeping a copy of every level of a document. At any point, any revision level of a document can be produced, including all changes made to bring it to the specified level and the changes that took it to the next level. Similarly, during on-line review of changes, both the old text (with strike-overs) and the new text are available to the reviewers.

Variant documents may be created and maintained in a similar manner. A variant document is one that's generally the same as a base document but describes a different version of the system—different configurations of the same basic aircraft, for example. In the Context system, all portions of the base document that aren't changed in the variant document are included by reference rather than being copied to the variant document. The variant document thus contains only text that's different from the base document. Any changes to the base document are automatically made in the variant document.

ETP will grow rapidly

ETP is still a relatively young discipline, but the DOD mandates should cause it to mature very rapidly. Even companies that don't do much DOD work won't escape from documentation standards. Big companies that use a lot of subcontractors are setting up their own documentation standards and electronic document delivery systems.

The C-3 data pipeline from General Motors (Detroit, MI) is a case in point. General Motors works with some 90,000 subcontractors who design various automotive parts. Subcontractors used a variety of design systems, so design data wasn't compatible from one subcontractor to

DOD standardizes documentation process

Although many system manufacturers may consider the Department of Defense a very good customer, the DOD is also one of the strictest customers when it comes to technical documentation. But even with its tough regulations, the DOD still has problems managing the documents it receives from its contractors, even if those documents meet every existing specification and regulation.

To help regulate documentation procedures, the DOD recently mandated the implementation of the CALS (Computer-aided Acquisition and Logistic Support) program. CALS defines how documents will be prepared and delivered, as well as how changes will be accomplished.

In the past, industry has tended to adopt military documentation practices. CALS should be no exception, particularly since companies such as the Context Division of Mentor Graphics (Beaverton, OR) will provide documentation tools aimed directly at helping meet CALS standards.

When CALS is fully implemented, defense contractors will no longer deliver their documentation in printed form.

CALS has a threefold documentation objective. First, digital tapes will be the delivery method of choice for future documents. Second, the DOD must implement internal procedures that will let the DOD use the digital documents. Third, the hoped-for result is that reliability and maintainability will be integrated into designs.

Switching from paper to magnetic tape is a major undertaking on both the contractor and DOD sides of the fence. Recognizing this, the DOD plans to implement CALS standards in two phases. Phase I involves converting paper documentation flow into electronic flow using available technology and industry standards. Phase II is much more ambitious. It involves total integration of product data bases among all contractors, with the data bases maintained by the contractors with on-line access and ownership by the DOD.

To implement Phase I, the DOD is in the process of defining a number of documentation standards. MIL-STD-1840A is the CALS technical publishing subset, covering such things as text formats, graphics formats, and standards for recording and transmitting graphics.

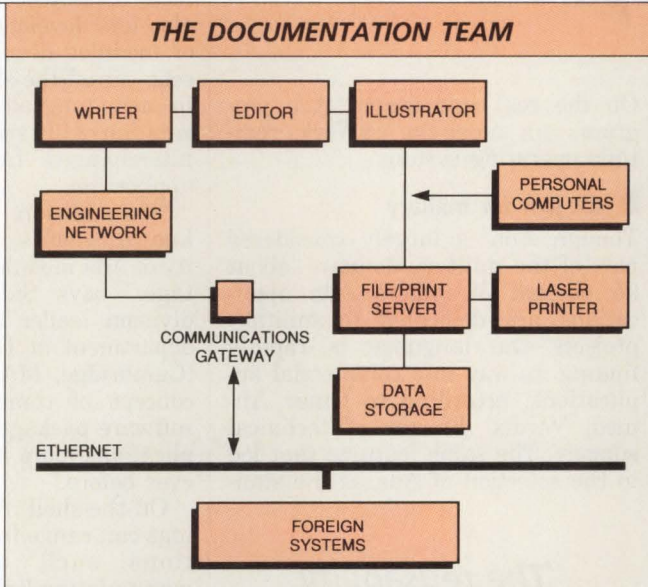
DESIGN AND DEVELOPMENT TOOLS

another, resulting in major integration problems for GM engineers. With the implementation of the C-3

data pipeline, GM subcontractors must submit their designs in electronic formats approved by the company.

While the text and graphics integration of an ETP tool may not be that much greater than what would be possible with a desktop publishing package (which would be less expensive), the documentation management tools should prove to be worth the extra cost. Tools such as access control, inclusion by reference, revision control, audit trails for changes, variant document production and format templates can go a long way toward bringing the engineering manager's documentation problems under control. □

Preparing design documentation is a team effort that involves writers, editors, illustrators and engineers. The documentation team usually works on the same types of workstations as the engineers do. The documentation network should be linked to the engineering network to provide a means for accessing source information and graphics from engineering data bases.



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Industry quartet plays real-time Ada on Sparc

Warren Andrews, Senior Editor

Four industry leaders recently merged workstations, Ada development tools, a real-time operating system and a Sparc-based VMEbus target system into an integrated real-time Ada development and run-time environment. Key to the quartet's development is the smooth integration achieved with the Ada development tools and real-time operating system and the interactive debugging capabilities shared by the workstation and target system. Verdix (Chantilly, VA), Wind River Systems (Emeryville, CA), Mizar (Carrollton, TX) and Sun Microsystems (Mountain View, CA) pooled their efforts to create a smooth-running environment that lets designers interactively write, debug and compile Ada code on a Sun workstation and download it to a Sparc-based target running a real-time operating system.

On the host workstation end is the Verdix Ada Development System (VADS) running on a Sun Workstation. VADS provides tools for handling library management, compilation and program generation, debugging, programming support and customer services. VADS is combined with Wind River Systems' VxWorks network operating system and its network and programming support tools. The resulting product has been dubbed VADSworks.

Program development is done on a Sun 3 or Sparc-based Sun 4 workstation or, alternatively, on Mizar's Hybrid Ada Development System running Unix or the SunOS enhanced version of Unix. The system is used to develop real-time Ada applications that will run on Mizar's line of fully configured Adaserver Systems based on Fujitsu's implementation of a Sparc RISC or Motorola 680X0 microprocessors.

The code developed in the VADSworks software environment is downloaded onto one or more embedded target processors from the Unix host via Ethernet or, in the case of the Mizar development system, directly across the VME backplane.

On the real-time target, Ada programs run under the VxWorks real-time operating system.

Not just for military

Though Ada is largely considered part of the military domain—about 95 percent of today's Ada applications are dedicated to military projects—the language is rapidly finding its way into commercial applications, according to Omar Ahmed, Verdix director of technical support. The same features that led to the selection of Ada as the stan-

"The reusability of Ada modules is a major advantage."

—Sid David, Draper Laboratories



dard for military projects are endearing the language to many commercial applications, he says.

The key features that Ada offers over other languages include manageability, maintainability, discipline and portability, says Ahmed. Ada's modular-oriented design leads to programs that are extremely easy to manage. By creating a division between the definition of a module's interface and its implementation, management teams can define module interfaces from the onset of a project.

With this division, individual engineers can separately develop code for segments of a program with reasonable confidence that the code will function properly when integrated into a final program. In addition to the manageability of program modules, Ada can protect data through its unique capabilities for data abstraction and data hiding.

Because Ada modules are isolated, the programmer can easily identify

changes to any specific module and understand the effect of the modification. According to Verdix's Ahmed, Ada's object-oriented approach also lets developers take advantage of modules developed in past projects—or off-the-shelf—and use them in new programs. Ada allows the creation of libraries that can often be interchanged from application to application.

"In addition to the commonly known benefits of Ada, the reusability of Ada modules is a major advantage," says Sid David, associate division leader of the applications department at Draper Laboratories (Cambridge, MA). "Ada makes the concept of commercially available software packages for embedded applications more a reality today than ever before."

Off-the-shelf Ada software offerings can range from low-level operations such as sorting and manipulating link lists to high-level, application-specific routines for human and graphics interfaces or the manipulation of sophisticated machines.

Program development

In the new development environment, initial Ada coding is done on the Unix-based host system after the programming support environment is set up and the VADS system is configured to the specific application. The configuration depends on the size and complexity of the software product and involves creating the necessary VADS libraries, search lists and library hierarchies. Configuration can vary from a simple, single library for small applications with only a few programmers to a high-level breakdown that determines the number of libraries to create as well as the dependencies and search lists needed. Hundreds, or even thousands, of programmers can be part of the effort.

If necessary, the problem can be further broken down into lower levels after the initial VADS libraries have been set up. Libraries can be completely independent, be fully dependent on one another or share any dependency relationship. If dependent, the libraries can be hierarchical in structure—code developed at higher levels would be independent of the code developed at lower levels,

while lower-level code would be dependent on each higher level.

Some of the functional testing and debugging can be done directly on the Unix-based development system. Other parts of the development, however, must take place on the target processor—in this case, the Mizar Adaserver. During coding,

small segments of the code can be separately compiled, linked, run on the server or in the Sun environment, and debugged. During debugging, the VADS Ada source-level debugger can be used on both the Unix-based host system or the target real-time system. After individual units have been coded, they can be

integrated and debugged as a single unit. The piecewise integration continues until the entire product is integrated, tested and debugged on the Sparc-based target system.

■ Full integration

One of the powerful aspects of this real-time Ada development environment is the full integration that provides efficient tools for code development with a direct connection to a real-time embedded target environment, says Jerry Fiddler, president of Wind River Systems. Integration is accomplished by providing a common user interface and programmer access to key functions such as windowing and networking capabilities, a standard operating system with editors, optimizing compiler technology, downloading and symbolic debugging capabilities.

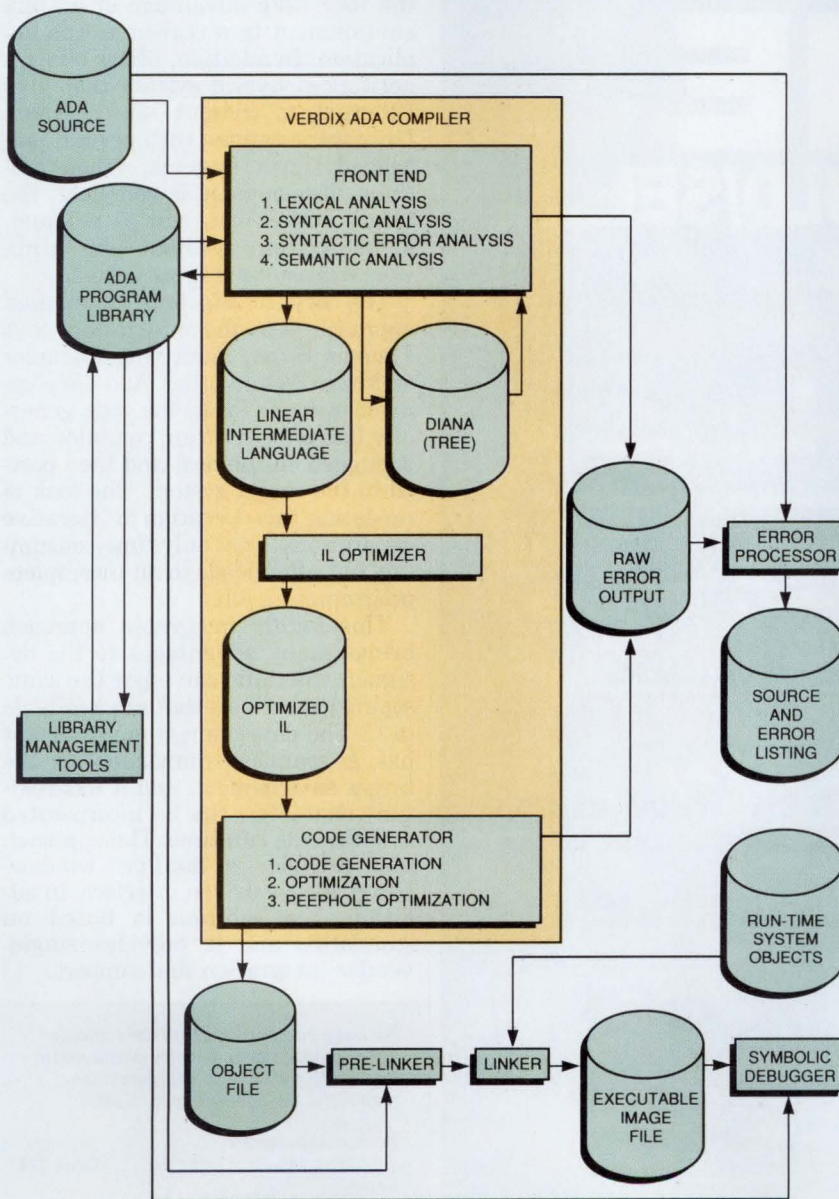
To simplify the entire development cycle and provide a seamless integration of development subsystems, a window-based, mouse-driven interface is provided. It serves to simplify Ada applications development by saving the programmer from having to remember the large assortment of Ada commands and options. Further, the interface lets users execute programs by using a mouse to select the necessary commands and options from a menu or other graphics display.

In addition to the conventional productivity tools, the development environment gives designers a fully interactive window into the execution and debugging of their application. With the Ada tasking model, tasks need to be examined and debugged concurrently. Debugging of a multitasking Ada program thus becomes not just a process of sequentially examining the state of each executed statement from the top to the bottom of a program, but also a process of manipulating objects.

Most debuggers provide only the capability of examining and viewing the program being debugged as a list of statements executed in sequence. Debugging should allow the examination—or even modification—of a task's state at any time when that task becomes active, however. The windowed environment of VADS-works provides this capability.

The need for integration between the host and target environment be-

THE VERDIX ADA DEVELOPMENT SYSTEM



The Verdex Ada Development System incorporates a variety of development tools to accompany its optimizing Ada compiler. These include a program library, library-management tools, error processing, object linking and symbolic debugging. The library-management tools let either off-the-shelf or custom-developed modules be easily incorporated into larger Ada programs.

SOFTWARE

comes increasingly critical as users demand that code will run similarly on both the target and host. This prompted Verdex and Wind River to integrate the development process with the real-time operating system and thus support Ada at both the

target and host sides. To round out the environment, Mizar provides the high-performance target hardware. It offers several levels of integration and support ranging from a single-board target processor to the company's hybrid server approach (using

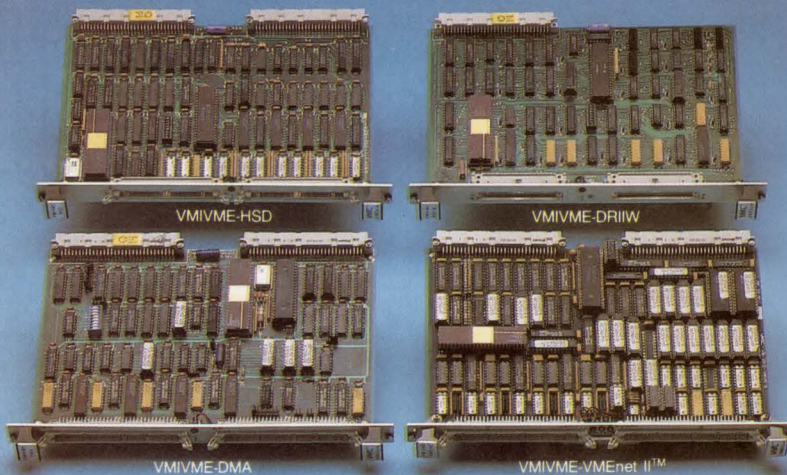
Sun VME processor cards to substitute for the workstation and work across the same backplane as the target system) to real-time embedded systems.

One of Mizar's fully packaged hybrid servers incorporates the capabilities of a Unix workstation and Ada software development tools with a real-time subsystem running a real-time operating system—Vx-Works. The server philosophy lets the user take advantage of a Unix environment in a real-time Ada application. In addition, Mizar offers a networked hybrid system that uses Ethernet to connect one or more Unix workstations with several embedded target systems. When program development is complete, the target system can run as a stand-alone system without the Unix workstation serving as a host.

The key to the four companies' approach is in the integration, says Thomas Kane, marketing manager at Mizar. While other Ada development systems exist, the code generally has to be written, compiled and debugged on the host and then ported to the target system. The task of repeating this operation for iterative generations is not only time-consuming, but often leads to an incomplete programming job.

This highly integrated approach brings many advantages to the designer. One, Ada can enjoy the same sophisticated tools that are available in C. The development environment has a seamless connection to the target environment, and it lets real-time characteristics be incorporated into the Ada run-time. The approach also provides a familiar window-based, mouse-driven interface. In addition, the solution is based on standards, and it provides single-vendor integration and support. □

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CIRCLE NO. 34

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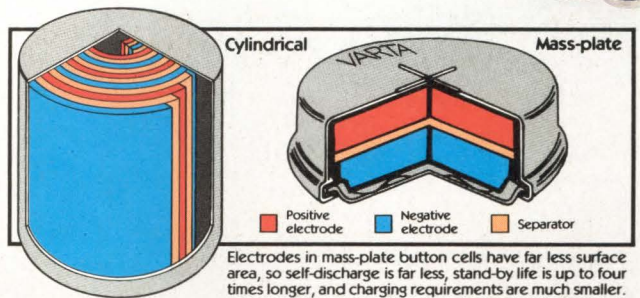


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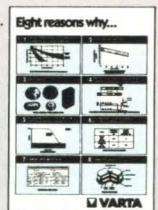


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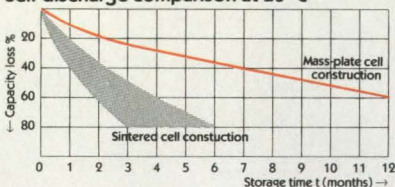
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CIRCLE NO. 35



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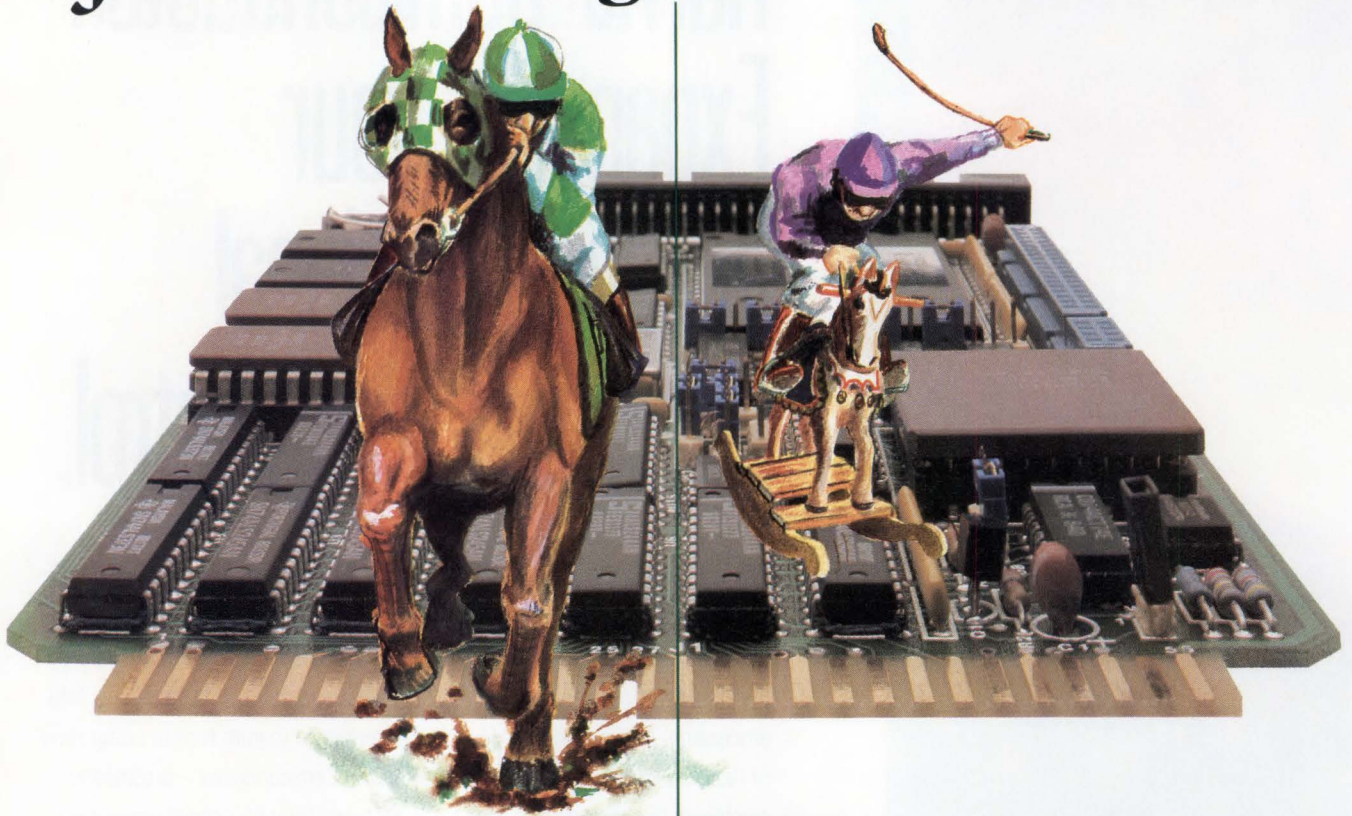
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Designers hang on to Multibus I

A seemingly interminable upgrade path. The sometimes irresistible appeal of familiarity. This old bus is—at least for now—still in its prime.

David Lieberman
Senior Editor

How is it that the 12-year-old Multibus is posting record revenues? And why, when design wins are so clearly few and far between, is this old 16-bit bus architecture now reaching record volumes?

The *Computer Design* 1988/1989 Bus Board Survey showed that roughly 22 percent of our readers who use boards are designing with Multibus I today, down from at least a 32 percent share in the past.

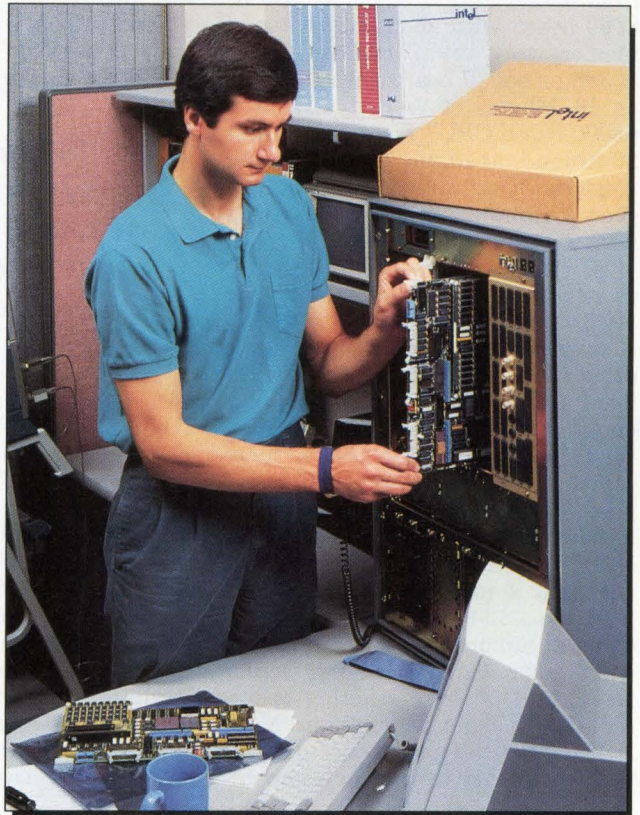
By 1991 or so, the survey respondents told us, only about 10½ percent of them will be doing new Multibus designs. Yet, despite this decline in design wins, most marketing figures show Multibus to have the largest market share of any open-architecture bus today, representing at least a \$600 million market, and it's not expected to top out until the mid-1990s.

Where are all those dollars going? It appears that most of them are going into upgrades and enhancements to existing designs, into new models in scalable product families and into field enhancements accomplished with simple board swaps. Running out of processing headroom? Swap out an 80286 or 68020 CPU board and swap in an 80386 or a 68030. Hitting an I/O wall? Swap in a denser communications board. Needing faster access to disk? Swap out an ST506 subsystem and swap in ESDI or SCSI.

The machines of the early and middle '80s are due for their mid- or late-life kickers, and it was Multibus I that captured most of the design-ins back then, before VMEbus and Multibus II had become viable alternatives.

Some of the dollars, though, are also going into real design wins for Multibus I, and the capabilities of systems using Multibus I are being stretched in some interesting ways. Here, the appealing aspects of using an old bus—above all, no learning curve or substantial software reinvestment—are enticing many designers to hang on.

Two major strengths of the Multibus I standard are that it's relatively easy to design to and lacks compatibility problems. It has been an exemplary story of bus success, attracting hundreds of vendors with



The board swap is a quick and easy way to upgrade an existing Multibus I system without making a substantial reinvestment in new software.

MULTIBUS I

thousands of products. Although it's now clearly an old-technology bus, vendors have continually applied the latest semiconductor and packaging technology to their boards to give Multibus I customers a seemingly interminable upgrade path. Over time, as limited bandwidth has become a hindrance, the Multibus I spec itself has also evolved.

If you're looking for a Multibus I CPU today, you can get everything from a multi-hundred-dollar Z80 or 8080 board with about 64 kbytes of memory to a multi-thousand-dollar 80386 or 68030 board with as much as 16 Mbytes of memory. Want a 68000-based CPU? There are almost 20 around, available from about 10 vendors. Need an 8086? You can choose from about 30 8086 CPUs from 15 companies or so.

Will the strengths of Multibus I, then, be able to carry it through the 1990s? Probably not, though it may survive in some niche or other. Some designers, in expectation of a Multibus I decline, are moving to a different 16-bit bus—the PC/AT—where the third-party support is even more copious and the dollars required far less. But more of them are going 32 bits, where bang for the buck is so clearly superior. “Most companies currently shipping Multibus I product have a 32-bit bus either in development, announced or beginning to ship,” says Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA).

Then, too, the appeal of Multibus I will lessen over time as new genera-

tions of engineers, brought up on the 32-bit buses, take over the bench, and the “I've used it before” appeal of Multibus I will no longer be a significant factor.

And there's the embarrassment factor. The marketing departments of over half of the Multibus I users contacted for this article either insisted on anonymity or declined to participate. “We don't want our company name publicly associated with old technology,” one source explained. “That's not the image we want to project.”

“Isn't it amazing!” says Russ Gam-

“There are a tremendous number of closet Multibus I users out there.”

—Russ Gamble, Zendex



ble, general manager at Zendex (Dublin, CA). “There are a tremendous number of closet Multibus I users out there.”

Why not change?

Despite the unwillingness of some to admit they use Multibus I, there's no question that the bus retains a strong following. “The majority of our customer base is sticking with Multibus,” reports Jack Blevins, director of new product development at Central Data (Champaign, IL). “We haven't seen anybody change

over to Multibus II in a big way, and the changeover to VMEbus stopped being significant over a year ago.”

“I'm surprised at the strength of the Multibus I market,” says Tom Powell, director of marketing at Syn-ergy Microsystems (Encinitas, CA). “Engineers don't change the bus unless they're doing a new project.”

Don Peterson, director of marketing at Ciprico (Plymouth, MN), sees it this way: “It's a time-to-market thing a lot of companies went through. A lot of people took on VME in 1983 or 1984, and the boards didn't play together as well as expected. Also, there weren't as many vendors and boards as in Multibus I, so people may have had two or three more types of boards to build themselves, which some lacked the expertise to do. Development took a lot longer than expected, and a lot of projects ran very late. Meanwhile, there was the old Multibus I system, working just fine.”

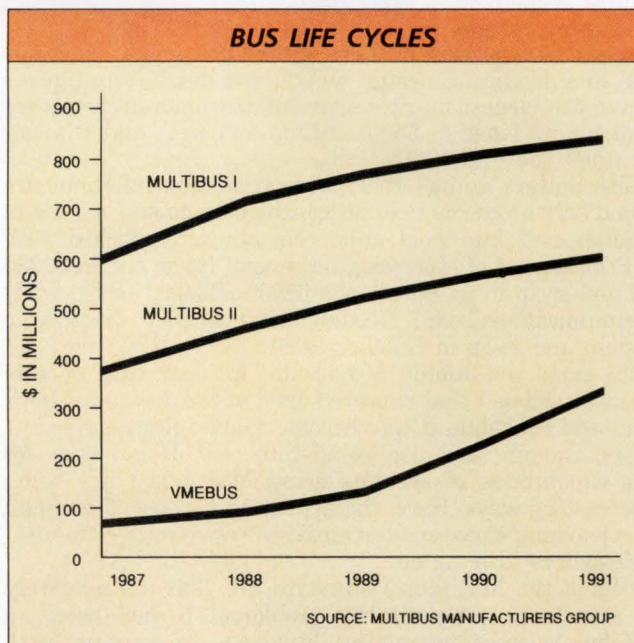
Then, too, Multibus I has been popular for government and military programs, which tend to be long-term. “Because of the government's way of doing business, the product life cycle there is longer and there's more of a desire to keep a product out there longer, supporting it and maintaining it and extending its life and spreading the cost of the program over a longer period,” says Michael Wells, president of Metacomp (San Diego, CA).

Customizing the bus

Like a number of other board vendors, Micro Industries (Westerville, OH) is seeing a lot of Multibus I activity, reports president Michael Curran. “We're seeing a lot of new custom board designs,” he says. “Many of our OEM customers are reducing cost or adding features to existing systems, and most are still anticipating getting quite a few more years out of the products. There's a strong tendency to combine the functions of, say, three boards into one. It's a real selling point that we can do the software so, where necessary to maintain compatibility, on-board accesses look just like off-board accesses.”

Other board companies also report a lot of demand for customization of board-level Multibus I products. Microbar Systems (Sunnyvale, CA), for example, has had success with the company's “application-specific processor” prototyping program, according to spokesperson Jacqueline

The VMEbus and Multibus I and II buses are at different stages of their life cycles. Although Multibus I is in its mature phase, it continues to resist market decline by supporting performance upgrades, and its revenues aren't expected to level off until the mid-1990s.



Goddard. The program is based on a CPU concept that populates about half of a board with basic CPU functionality and leaves the rest free for memory modules, a daughter board and a large wirewrap area. Prototyping in this fashion, says Goddard, is a real boon to time-to-market.

According to Synergy's Powell, "The level of board integration is now very aggressive. People want slightly custom things, they want it quickly and they don't want to have to buy an extra card. Today, it's usually possible to put any critical function you'd normally go to the bus for on the board or a daughter board instead," he says.

■ Leveraging through upgrades

The greatest appeal of "a bus I've used before" is the ability to leverage past investments—in hardware, software and staff expertise—that were made when the bus was first taken on. And some, who took on Multibus I as their first open-architecture bus in the mid-'80s, think it's a bit early to give it up, choosing instead to upgrade. "Those people whose applications are running fine on Multibus I but could use some additional processing power are upgrading," says Blevins. "Upgrading lets you postpone a bus decision. If you can avoid the expense of changing buses and still make your customers happy, there's no reason to change."

Gamble concurs. "The marketing figures say Multibus I is capturing only about 7 percent of design wins, but that doesn't include upgrades. There's a continuous flow of upgrades going into established markets. That's why there's a groundswell of activity in Multibus I."

Multibus I users are upgrading with 68020/68030 and 80286/80386 CPU boards, intelligent peripheral boards and network boards and/or denser I/O boards. And many are moving from ST506 disk controllers to SCSI host adapters. "Customers are seeing that they can upgrade from an ST506 disk to a SCSI disk that costs about the same, has lower access time, higher data rate and a lot more capacity," Peterson says. "SCSI also lets them hook up all sorts of other peripherals and write a single driver that can support them all." While the customer making such a change will need to write a SCSI driver, if he moved to a new bus instead of upgrading an existing one, he'd need at the very least to

Real estate and relative economics

William Gage, president of SBE (Concord, CA), recounts a story of a customer in the mid-1980s who geared up for VMEbus, then decided to stick with Multibus I instead. "He discovered that, because of the real estate needed for the VME interface and the smaller form factor, he'd need to do two VME boards to do what he did on one Multibus board," says Gage.

Although the economics are shifting, VME real estate is a good deal more expensive than Multibus I real estate. DIN connectors, front panels, shielding and various machined parts, tapped screw holes and bolts all add cost. The appearance of VME interface chips from a number of vendors has opened up some real estate, but with the cost of the chips factored in, a VME board can still run several hundred dollars more than a Multibus I equivalent.

The VMEbus real-estate penalty and the need to stay competitive have pushed board technology and, simultaneously, raised costs. "Because it's a smaller card, it ends up having more layers and requiring a more complex assembly process," says Gage. "Our most popular Multibus I card is just four layers, while we never do less than eight layers for VME and have had to do some 10- and 12-layer boards." The need to move to application-specific ICs and/or surface-mount technology to get the needed functions on-board also extracts its price.

Fierce competition in VMEbus markets, however, has exerted an opposite influence on pricing. Pete Czuchra, marketing manager at Omnibyte (West Chicago, IL), sees nearly comparable pricing between Multibus I and VMEbus at the board level. "VME has matured a little more and, consequently, development costs of designs built in the past four years or so have pretty much been paid back," he says.

A simple, Multibus I-to-VME comparison of price doesn't get at the price/performance issue, however. And because of the differences between the two buses, truly equivalent products are fairly rare. "In the markets we serve," says Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA), "price isn't the main issue since VME gives more performance and throughput and I/O throughput per dollar than Multibus I does. If a VME disk controller lets you use one file server instead of two, who cares if it costs 10 percent more?"

Price/performance aside, the reports are extremely disparate on the relative economies of putting together a Multibus I vs. VMEbus system, running from rough parity to about a 100 percent VMEbus cost premium. "Whatever the difference is, it's relatively insignificant," says Tom Powell, director of marketing at Synergy Microsystems (Encinitas, CA), "since most of the cost of VME is in switching over."

write drivers for all his new boards—no small task.

Intel reports ongoing upgrades from ST506 to ESDI, and Xylogics' Cory notes that some designers are upgrading from 10-MHz to 15-MHz ESDI disk subsystems. "Some people are also trying to move down from SMD class drives to 5¼ inchers," Cory adds. "They're downsizing to a more compact version of an existing machine."

As with other buses, the movement toward ever higher board functionality on Multibus I has culminated in the workstation-on-a-card concept. "With multimegabytes of memory, SCSI, Ethernet and/or full graphics on the board itself, you can get much better performance than anything you can get on the VMEbus," claims Powell.

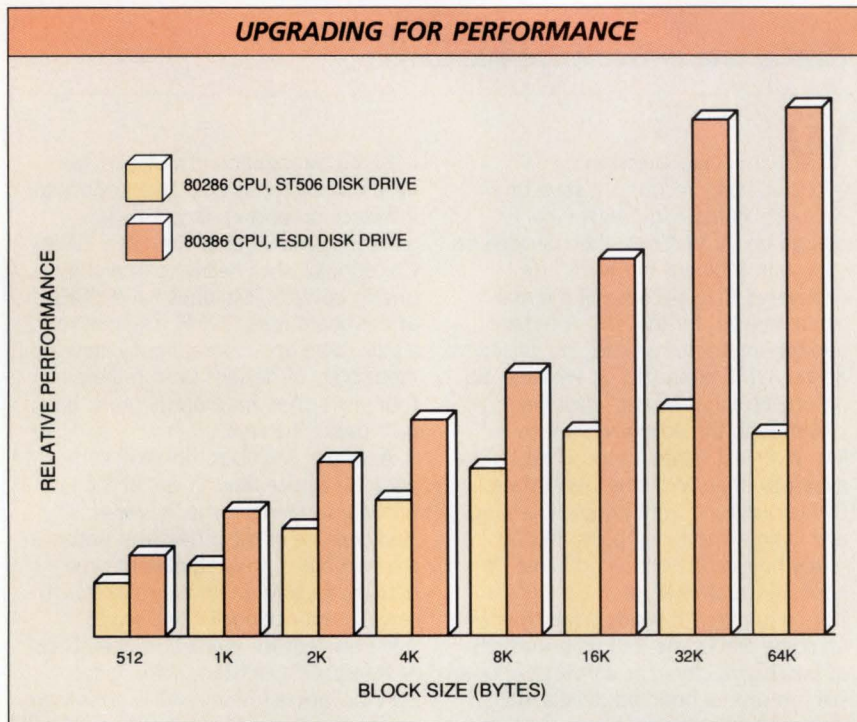
Pete Czuchra, marketing manager

at Omnibyte (West Chicago, IL), notes a movement toward upgrading with intelligent I/O. Not only does the strategy offload the CPU, he says, but it also reduces the traffic that would occur normally between a CPU and dumb I/O controllers.

Granted, there are many systems out there for which a 16-bit bus is no hindrance. Where it is, though, Multibus I designers have moved memory traffic off the bus onto an auxiliary bus or kept the bulk of the traffic on the CPU board itself. "If your board has a 32-bit processor with a 32-bit local bus to lots of 32-bit memory, a 16-bit data bus isn't an issue as far as execution time goes," says Blevins.

■ Who is hanging on?

"Those people who need to maintain software compatibility with a previ-



When a system based on an old bus starts to run out of steam, substantial performance improvements can be made by swapping the CPU and, if necessary, one or more I/O subsystems. To get the full force of upgrade potential, however, it's usually necessary to tweak the system software. As shown here, for example, if an operating system can request data in larger chunks, more of the potential performance possible with a more advanced processor and disk drive subsystem can be reached.

ous system or maintain some continuity in enclosure design are staying with Multibus I," says William Gage, president of SBE (Concord, CA), "unless they're running out of horsepower. One strong reason to continue with an old bus is the ability to upgrade systems in the field. If you can stay with the same packaging and merely change boards, then you have the relatively easy prospect of boosting performance for existing customers by just swapping some boards."

"Sure, the Multibus I boards are slow and the window on timing is wide," admits Gamble, "but it's easy to design a compatible board and it gives you reliability down the road."

"There are always tradeoffs when deciding between a previously used bus and a new bus," says Michael Pritchard, product marketing manager at Intel's OEM Modules Operation (Hillsboro, OR). "If the attraction of staying is greater than the cost of going, why throw away something that's making money?"

It appears that designers locked into the Intel processor architecture have been among the most reticent to bite the bullet and move on from Multibus I to a 32-bit bus. While the

VMEbus, conceptually similar to Multibus I, abounds with Motorola processor architecture products, there are only a handful of CPU companies in VME who serve the Intel camp.

"There doesn't seem to be a lot of cross-pollination between buses and processors," Peterson says. On the other hand, Multibus II is not a "quick and easy" transition for the Intel processor world. It suffers from a relative dearth of product, high entry costs and a narrower appeal than either VME or Multibus I.

■ The problem with multiprocessing

One area in which Multibus I does not fare well is multiprocessing. "It's obvious that anybody doing any kind of distributed or parallel multiprocessing has got to get off Multibus I," says Gamble. "The bus simply won't support it. Multibus I is a dog for doing any kind of interprocessor communications. For I/O-intensive things, though, it's the king."

Intel's Pritchard puts the issue in a different light. "If you look at the architecture of a typical multiprocessing Multibus I system, it's what I'll call 'functional,' as opposed to 'distributed', multiprocessing: that

is, there's only one real master and maybe three or four intelligent slaves," he says. "That method doesn't take up much backplane bandwidth, and it suits a lot of applications. We don't run into many Multibus I backplanes that are saturated."

One large industrial controls company continues to put its new operator console designs on a multiprocessing Multibus I. The engineering group leader clearly prefers Multibus II but, he says, "I've got an installed base to support." Atypically, the company is substantially modifying its software architecture to incorporate concepts being used in VMEbus and Multibus II architectures. In the new architecture, six CPUs will use the Multibus I only for I/O, for access to a global data base, and for short message bursts among themselves. "There's nothing to say that you can't put Multibus II-like message passing on a multiprocessing Multibus I," says the group leader. "It has nothing to do with the backplane. You could do message passing on S-100 if you wanted to!"

Another factor dictating against successful distributed multiprocessing on Multibus I is its lack of a fairness algorithm in its arbitration protocols. Such an algorithm prevents low-priority masters from suffering bus starvation. In functional multiprocessing, though, lack of fairness represents no hindrance.

As one source explains: "If all the processors have exactly equal priori-

"Upgrading lets you postpone a bus decision. It buys you time."

—Jack Blevins, Central Data



ties, then fairness makes sense. But if certain processors are dealing with real-time data channels, such as an Ethernet data link or something like that, you need different priority levels, so a fixed priority system makes sense. If Multibus I had fairness, I'd have to go to the trouble of disabling it to get my system to work."

■ Evolution and mutation

Multibus I has continually mutated outside of the standards committee

arena. In late 1987, for instance, the Tru-32 32-bit Multibus I extension scheme from Zendex appeared and, in mid-1988, the Multibus Plus extension scheme arrived from Synergy, which added a burst-mode transfer function to an extended 32-bit capability. Titan SESCO (Chatsworth, CA) has been working with a militarized Multibus I for some time, as has Radstone Technology (Montvale, NJ) with a Euro Multibus. According to Doug Patterson, military product marketing manager at Radstone, new military designs are running about 80 percent VMEbus, 20 percent Multibus I.

Siemens (Munich, West Germany) and Micro Industries also market a Euro Multibus for the factory automation arena. "Some Multibus II customers were upset when they found out about the Advanced Multibus System," says Curran, "because they paid a heavy price to change when all they needed was the Euro-card and a little more capabilities on the boards."

Gamble reports that three or four Zendex customers are working with the Tru-32.

As for Multibus Plus, Powell says: "It got tremendous reception, but hardly anyone is actually interested in using it. There's some interest in Multibus Plus at one customer doing parallel processing, which is where you'd see the most performance gain."

"Since a lot of people don't optimize their code when they move to the 68020, they'd have to do a little bit more software work than they might like to take advantage of an extended Multibus," Powell adds. "It would be less trouble than switching over to VMEbus and changing all the drivers. But many will just keep going with the Motorola processor family and Multibus I because they're very familiar with it and it's a lot less work."

One director of engineering has done his own 32-bit Multibus I "bastardization" for a small business computer. Getting third-party boards to use in his mutation was no problem, he reports; Ciprico and his other vendors made the required adaptations on their boards for the new design. His next design, however, will be on VMEbus. "Multibus I is too restrictive for the kind of multiprocessing I want to do," he says.

■ Where it's thriving

Many companies have chosen to hang on to Multibus I as long as it's

feasible (and profitable) to do so. The old bus is alive and well, to mention just a few examples, in data communication controllers in Disneyland, in pipeline control systems for Texaco, in the security system at Lawrence Livermore Labs, in the manufacturing operation at Sumitomo Metals, in medical instrumentation from Nicolet Biomedical Instruments, in flight simulators from Frasca International, and in IC

test equipment from Semiconductor Test Solutions.

When Ford Aerospace (Beltsville, MD) needed a bus to get its Tracking Processing System developed quickly, it chose Multibus I. "To drive the antenna that tracks low earth orbit satellites for the Goddard Space Flight Center network, we needed 5 to 10 Mbytes/s of bandwidth," says Herb Emerson, senior system engineer. "We did an extensive evalua-

The life cycle of Multibus I



Products and technologies go through five distinct phases in their life cycle:

1. Research and development and initial introduction phase. Sales growth is indeterminate in this period. Most inquiries aren't from those working on a funded project. Rather, those making inquiries are seeking information for future projects or are building a system for internal evaluation.
 2. Market development phase. Sales growth below 50 percent.
 3. High growth phase. Sales growth above 50 percent.
 4. Maturity. Sales growth between 10 and 30 percent.
 5. Decline. Sales growth below 10 percent, eventually becoming negative.
- Multibus I is clearly in the mature

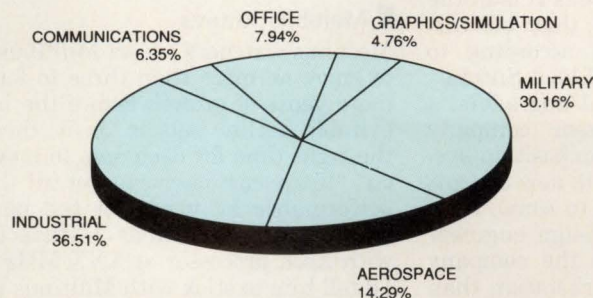
In this phase of a bus's life cycle, the project-driven systems integrator buy is dominant. OEMs are generally going to newer bus technologies such as Multibus II, which is still in the market development phase of its life cycle.

A market research study by the Multibus Manufacturers Group (Aloha, OR) released late last year revealed some interesting patterns of bus usage. In military and aerospace markets, for example, there's a clear migration from Multibus I to Multibus II. In the factory automation arena, on the other hand, Multibus I and II participate in two distinct subsegments of the market. Multibus I manufacturing process control applications are almost universally traditional single-point control applications where programmable logic controllers and micros have been widely employed in the past. Multibus II applications are almost universally multipoint applications where minis and main-

frames had been the norm.

Likewise, there's a difference in the use of Multibus I and II in the office automation/commercial data processing segment of the market. The use of Multibus II here is almost exclusively at the departmental

MULTIBUS I MARKET SEGMENTS

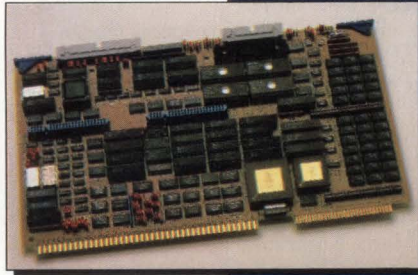


phase of its life cycle, but it's showing no signs of entering the decline phase at this time. It has received midlife kickers with the introduction of 80286 and 68000 processors and again, just recently, with the introduction of 80386 and 68020/30 processors.

computer and high-end engineering workstation level. The Multibus I position appears to be almost exclusively in the area of Unix/Xenix-based departmental computers serving fewer than 12 simultaneous users.

Daniel Fink, executive director, the Multibus Manufacturers Group

MULTIBUS I



Semiconductor Test Solutions (Santa Clara, CA) builds its midrange IC testers around the Multibus I using the M68CPU board set from SBE and the Regulus operating system from Alcyon (San Diego, CA). The company chose a bus based on compatibility, reliability and a moderate pricing structure.



tion of Multibus I, VMEbus, STD Bus and the AT bus, and chose Multibus I. Part of the reason was that everyone in the Goddard network is familiar with the bus, which reduced the learning cycle tremendously, and that was an important factor."

Clearly, however, Multibus I won't live forever. When Redondo Systems (Torrance, CA) needed "a well-supported, well-defined industry-standard bus with lots of available product" on which to build its radar simulators, it chose Multibus I. Nevertheless, Multibus II is in the company's future as that bus attracts more support, according to company spokesman Lloyd Sutton.

Among the habitual upgraders, a raster image processor company making newspaper composition systems will be putting its new designs on VMEbus in times to come. As a company hardware design engineer explains, it will cost the company less to buy a Sun workstation than to manufacture its own Multibus I system.

Harris Graphics (Dayton, OH) will also be moving on to VMEbus as its bindery equipment automates more functions in that industry, explains Andy Bruce, member of the company's software group. One important issue in the decision to change over was the availability of a Unix link for VMEbus systems to the real-time

operating system the company has been using.

Even such a strong Multibus I advocate and habitual upgrader as Nicolet (Madison, WI) will be moving onto a PC platform, says software project manager Michael Christie. "The PC bus supports the operating system we've been using, we can get comparable performance with some careful planning and design, and there will be fewer types of boards we'll have to design internally," he says.

■ Multibus futures

Most bus watchers expect Multibus I to enjoy no more than three to four more years of growth before the inevitable decline sets in. Is it, then, the right time for designers to move on? "If my customer can get all the performance he needs for the next five years on Multibus I—that is, with XXX processor at XXX MHz—I'd tell him to stick with Multibus I," says Pete Yeatman, vice-president of marketing at Radstone. "If it won't suffice or his competition will beat the pants off him with a 32-bit bus, I'd say it's time to switch."

"I can't think of a situation where I'd recommend Multibus I today," says Powell, "but the people who stay with it have compelling reasons for doing so. Obviously, changing from a 68020 CPU to a 68030 is a

very cheap way of getting tremendous compute power without making a whole lot of changes. When Motorola introduces the 68040, you'll see another resurgence in Multibus I interest because those people are going to want to upgrade again. It's the cheapest thing to do." □

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Ada tools mature, but users debate language standards

Ada development tools improve for building real-time and distributed systems, but can the remaining language problems be resolved without defying rigid standards?

Howard Falk
Contributing Editor

```
- SRC: module DP -scroll-source
5:  -- main program of dining philosophers
6:
7:  PHILS : ARRAY(1..4) of PHIL_TASK;
8:  begin
9:
10:   for I in PHILS'RANGE
11:   loop
-> 12:   PHILS(I).IDENTITY(I);
- INST: routine DP
: JSR      (00016A20).L
Line 10: MOVE.L #1,D1
->ne 12: LEA   -56(A6),A5
: MOVEA.L (-4,A5,D1.L*4),A5
: MOVE.L  #16,D0
: MOVE.L  D1,-60(A6)
- OUT
D0 : 00000000
D1 : 00000001
D2 : 00000001
FP0 : FFFFFFFF
FP1 : FFFFFFFF
FP2 : FFFFFFFF
FP3 : FFFFFFFF
FP4 : FFFFFFFF
FP8 : 7FFF0000
FP1+4: FFFFFFFF
FP1+8: 7FFF0000
FP2+4: FFFFFFFF
FP2+8: 7FFF0000
FP3+4: FFFFFFFF

- PROMPT -error-program-prompt
XDDBC> examine I
DP.LOOP$10.I: 1
XDDBC> █
```

The Ada language has had a reputation for awkwardness, primitive development tools, and poor real-time performance. Yet, during the past year there has been considerable progress in providing more adequate Ada development tools. Debuggers comparable to those for C language are now available. Ada vendors have also been concentrating on improved software products for real-time and embedded systems. At the same time, Ada development efforts are striving to meet the needs of distributed and parallel system applications. Finally, changes in the Ada language itself are being tentatively considered.

Validation by the Department of Defense is the entry ritual every Ada compiler must pass through on its way to the military software market. Now that over 200 compilers have successfully passed that ritual, users are realizing that validation is no guarantee that a compiler will provide code that has the speed or efficiency required by their application. Under pressure from these users, Ada vendors are producing more efficient compilers and, even more important, are accompanying their compilers with the kind of development tools that users of popular computer languages have come to expect.

C-language compilers are typically designed, implemented, and sold as stand-alone products, and users may select other tools from other vendors to form the development environment of their choice. Such selectable toolsets, however, aren't yet available for Ada, so users have to depend on the development toolsets provided by compiler vendors.

The typical Ada toolset for embedded system work is hosted on a VAX/VMS computer. Sun workstations are also popular Ada hosts. In addition to host- and cross-compilers, Ada toolsets typically include libraries for storage of object code modules, as well as library managers that let users create, move, copy, delete and view library objects, and to generate reports on library contents. Binders convert compiler-generated object units so they can be linked to other Ada objects. Importers transform non-Ada object code units so they can be used together with Ada object units. Linkers determine the valid order in which library units, compiler-generated object code units and imported units can be combined, and then they form these diverse units into modules that can be executed on the host computer. Formatters convert host object modules into target

A key item in any Ada toolset is a debugger. With the XD Ada debugger from System Designers Software, users can stop execution with breakpoints and tracepoints, and they can halt execution when selected variables change. Register contents can be examined and altered. Source code can be accessed, and debugging commands have a familiar Ada syntax.

ADA

computer format. Locaters assign object code and data to desired memory locations.

Some vendors include these functions in their Ada compilers, while others offer them as separate tools. Ada toolsets also typically include Ada language tools such as cross-referencers, which show where symbolic names are declared and referenced. Source dependency listers identify the connections of an Ada package to other packages, and source formatters present Ada source code using standard language conventions. Most Ada compilers include optimizers to increase code efficiency.

This Ada Symbolic Debugger screen from Intermetrics shows a highlighted line of Ada source code at which a breakpoint has taken place. In the lower window, a debug command follows the dbg > prompt. The table lists tasks within the source code, along with their status at the breakpoint.

```
1 dbg>
====SOURCE WINDOW====moretasks.ada====(-PF1 PFS)====
0036 # procedure putb (s: string) is
0037   begin
0038     put_line("BUFFER: " & s);
0039   end;
====COMMAND WINDOW====(-PF7 PFB)====
dbg> show dependents *
Task ID  Object or Type Name  Status
-----
TASK#10  MORETASKS             CALLER IN RENDEZVOUS
TASK#2   . BUFFER               RUNNING priority 12
TASK#3   . BUFFER               ACCEPTOR WAITING
TASK#4   . EXCEPTION_RAISER    ACCEPTOR WAITING
TASK#5   . B2                   CALLER IN RENDEZVOUS
TASK#6   . WAIT                 ACCEPTOR TERMINABLE
TASK#7   . WAIT_2               CALLER DELAYED until 17:03:44.702
TASK#8   . WAIT_3               CALLER DELAYED until 17:03:44.697
TASK#9   . . . WAIT_4          DELAYED until 17:03:44.694
TASK#10  . BUFFER               RUNNABLE priority 0
TASK#11  . BUFFER               RUNNABLE priority 0
TASK#12  . BUFFER               RUNNABLE priority 0
TASK#13  . BUFFER               RUNNABLE priority 0
=====
```

Finally, a key item in any toolset is the debugger, which now typically operates at the source level. For example, the Adaview debugger from Intermetrics (Cambridge, MA) uses a full screen display that allows users to inspect Ada objects, types, and units, as well as registers and memory, the run-time stack, task status, program sources and other files. Breakpoints and tracepoints can be set on Ada source lines, exceptions and tasks. There are commands to list tasks, inspect a particular task context, and to display task, entry and call status.

In addition to these typical tools, Ada vendors are turning to a variety of special techniques to improve their offerings. For example, to meet embedded system debugging requirements, System Designers Software (Cambridge, MA) makes use of a kernel at the target computer that serves as a component of its XD Ada Debugger. The kernel lets tools at the host load, start and debug code that runs in the target. When debugging is completed, this kernel can be removed.

Another special feature of the XD Ada compiler and related tools from System Designers Software is their close relationship with VAX/VMS host computers. Thus, developers who use XD Ada tools can also access an impressive array of VAX Ada tools, including the VAX language-sensitive editor, code-management system, source-code analyzer, performance and coverage analyzer, and test manager.

All these are tools that can be used for Ada source code development on the host. The XD Ada Debugger isn't the only one that makes use of a kernel at the target comput-

For users who want to load Ada code into the target over a simple communications link, Tartan Laboratories (Pittsburgh, PA) provides an optional Hot Bench interface that uses an RS-232 connection for both loading and assembly language debugging. The Hot Bench facility first loads a software kernel that communicates with interface software on the host, and then loads the application along with optional symbolic information for debugging. Telesoft (San Diego, CA) and Ready Systems provide similar downloading and receiving capabilities.

Analyzing code

Code analysis tools, to help users identify code that may need improvement, are also now available in Ada toolsets. The Adatune tool from Alsys (Waltham, MA), for example, provides profiling analysis that identifies portions of the code that are hogging execution time. Adatune also does coverage analysis to identify which paths through the code have been tested, and which remain unexplored.

Telesoft provides a similar tool called the Execution Profiler. Profiler results are statistical, based on sampled data, with reports that display the execution times for the slowest procedures. Call chains are displayed, all calls to and from subroutines are reported, and recursive calls are flagged. Using Profiler data, estimates can be made of performance improvements that can be expected with program speedups.

In a move indicative of growing collaboration among Ada tool vendors, Verdix (Chantilly, VA) has combined its Ada Development System (VADS) with the VxWorks real-time operating system from Wind River Systems (Emeryville, CA). With the combined tool, called VADS/Works, Ada applications are developed on a Unix host, using a VADS Ada compiler and related tools. Then the code can be downloaded to a target system, using the standard 4.2 BSD Unix socket interface and TCP/IP protocol.

On the target, the code is executed under the VxWorks real-time operating system. Ada tasking and rendezvous are implemented through calls to the VxWorks real-time kernel. Debugging of code on the target can be done with the VxWorks symbolic debugger. Alternatively, debugging can be done from the Unix host, using the VADS source-level

er. The ARTX real-time kernel from Ready Systems (Sunnyvale, CA) also provides debugging facilities similar to those of the XD Ada Debugger, and for its Ada 386 cross-compilation package, Intel (Hillsboro, OR) uses a debugging kernel that resides in a PROM on the target board.

Some vendors offer target simulators to users who want to do as much as possible of their Ada code development on a host computer. The 1750A simulator from Interact (New York, NY), for example, models target instruction timing, I/O capabilities and other features, as specified by the user, on a VAX/VMS host. Simulators are typically slow, compared to target chip operation, but the Interact simulator is said to run at the respectable rate of 300 to 350 VAX Ada instructions for each 1750A instruction.

The Ready Systems' RTAda-Sim software simulates a 68020 target, including the ARTX real-time kernel. RTAda-Sim lets the user define I/O device behavior and then debug Ada programs on a VAX/VMS or Sun/Unix computer.

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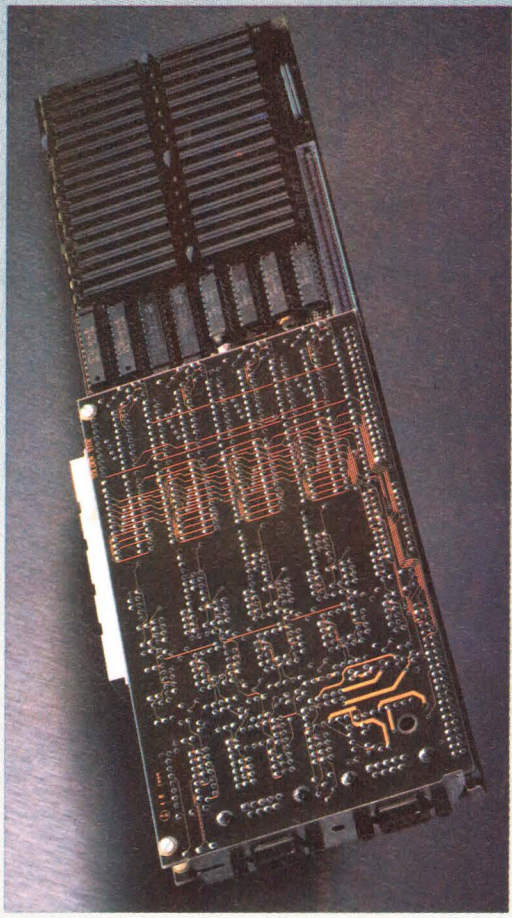
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■ ADA

debugger. VADS/Works is available in versions for a number of different standard CPU boards from vendors including Heurikon (Madison, WI), Motorola (Phoenix, AZ), and Force Computers (Los Gatos, CA).

■ Limiting run-time size

One of the key requirements of embedded systems is that programs must take up as little target memory space as possible. Ada is a very large language, however, that includes many different features, and early Ada compilers retained all those features, making run-time systems bulky. Today, many Ada compilers are designed to selectively link and load only those run-time features needed by the application at hand.

The Tartan cross-compiler for the 1750A, for example, automatically configures a 750-byte Ada root, which is the Tartan's smallest 1750A run-time system. The complete Tartan Ada run-time system for the 1750A totals 7,698 bytes. Inclusion of run-time features can be performed automatically by the Tartan compiler, based on what is needed by the application. Thus, if exception handling or tasking isn't used, portions of the run-time system that handle those functions will be omitted.

An alternate approach is to let users limit run-time size by choosing compiler features. Tartan allows this, as do cross-compilers from Softech (Waltham, MA), for which users can modify run-time system size by selecting or omitting such compiler features as memory partitioning, stack sizes, clock speed and stubs used for power-up testing.

■ Distributed and parallel systems

To those system developers who believe that the future of computing lies in distributed and parallel systems, current Ada capabilities look inadequate. Gerry Fisher, research staff member at IBM (Yorktown Heights, NY), for example, says that the Ada model for distributed computing "seems nice at first look" but the language provides only for a single memory system, not for distributed processors, each of which has its own memory. People who want to use the existing Ada language for distributed computing "haven't the foggiest idea of how to begin," Fisher says.

Issues include which task will be assigned to which processor, and which memory should be used. Fisher

also finds problems with the pragma (compiler directive) used for sharing data, scaling data and synchronizing access to it. Fisher also cites lack of asynchronous transfer of control as a related issue that arises when one Ada task stops and another resumes.

To demonstrate the feasibility of using Ada for distributed computing, the Software Engineering Institute (Pittsburgh, PA) has been developing a Distributed Ada Real Time Kernel (Dark). This kernel supplies primitives needed for interprocess communication on a single processor or across multiple processors. With Dark, applications code written in the Ada language can be readily moved from one distributed processing configuration to another. To make such a move, physical system unit names have to be associated

with kernel logical names, and this is done using Dark reconfiguration procedures, so that the Ada code itself doesn't have to be altered.

Dark implementation is essentially complete, according to Judy Bamberger, member of the technical staff at the Software Engineering Institute (SEI). System testing is under way, and copies went to select beta sites in February. More copies will go out to beta sites in May, and a Dark demonstration will take place later in 1989. Bamberger notes, however, that Dark doesn't provide a full Ada run-time system, nor does it allow for use of Ada tasking commands. In the future, the kernel may include such features, but right now the emphasis is on its interprocess communication capabilities.

Although performance of a single Dark primitive has been measured

Ada = language + standard features + run time

To understand arguments about future changes in Ada, it may help to picture Ada rules as encompassing not only the language itself, but also interface features and options, and run-time systems.

An Ada catalog of interface features and options is being developed by subgroup 3 of ARTWEG, which is a part of the Association for Computing Machinery (New York, NY) Special Interest Group on Ada. The subgroup is chaired by Charles McKay, director of the NASA Software Engineering Research Center at the University of Houston (Clear Lake, TX). This subgroup tries to identify issues that may arise repeatedly in different Ada applications and that should therefore be handled by standard methods, according to McKay.

The subgroup has adopted an option, for example, that places bounds on delays specified in applications programs. The official Ada language reference manual makes no provision for placing such bounds, and some users perceive this as a weakness of the Ada language. McKay disagrees, reasoning that the language is the law and it shouldn't be violated. However, his subgroup deals with Ada features outside the language, so the subgroup's software, which McKay terms "systems software," is legal.

Run-time code can consist of Ada language software and non-Ada soft-

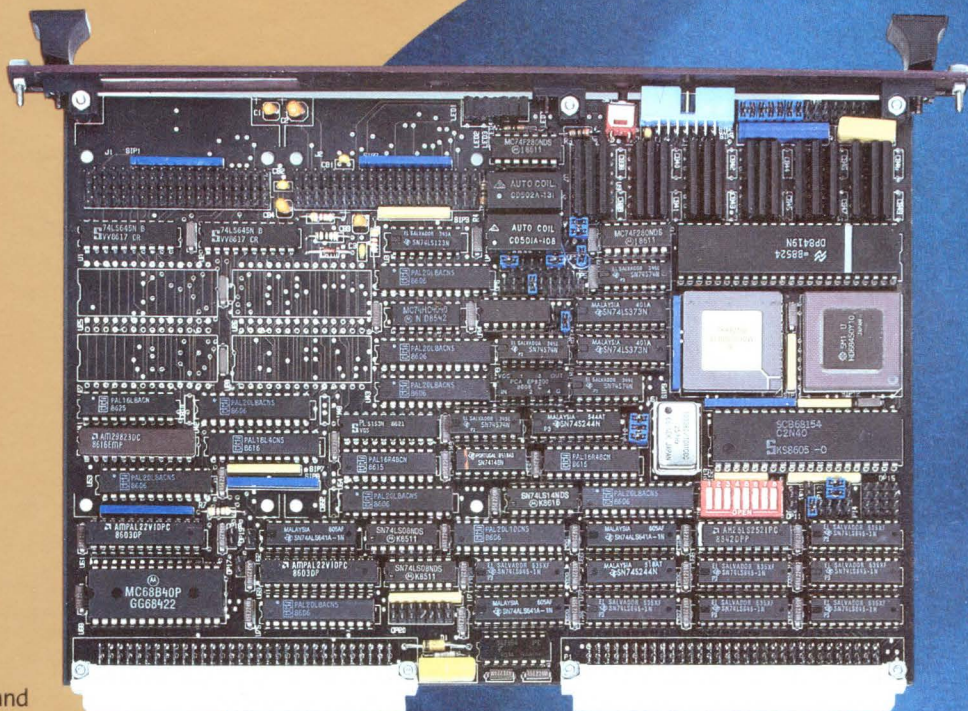
ware. Ada allows, for example, a non-Ada real-time kernel to be used in the run time to perform tasking. The run time can thus be used as a catch-all to provide functions that aren't in the Ada language standard. Such added functions will be unique to the particular application in which they are used, however, and will have to be rewritten if that application is to be moved to another computer.

Some Ada users want the language to include hard-deadline real-time scheduling, and bounded delay statements associated with those deadlines, or they want means for handling critical sections of code. McKay's response to those users is that such capabilities shouldn't be part of the Ada language specification, but should be provided by standard interface features and options, by the run-time environment, or by some combination of the two. The Ada language, he believes, shouldn't have to accommodate the requirements of an operating system or a real-time kernel that doesn't function well with existing Ada paradigms.

"The question I ask about a proposed Ada language change is whether it needs to be visible to applications programmers," McKay says. If a standard interface feature or option, or the run time, can be used to meet users' needs, that is preferable to changing the language to accommodate those needs, according to McKay.

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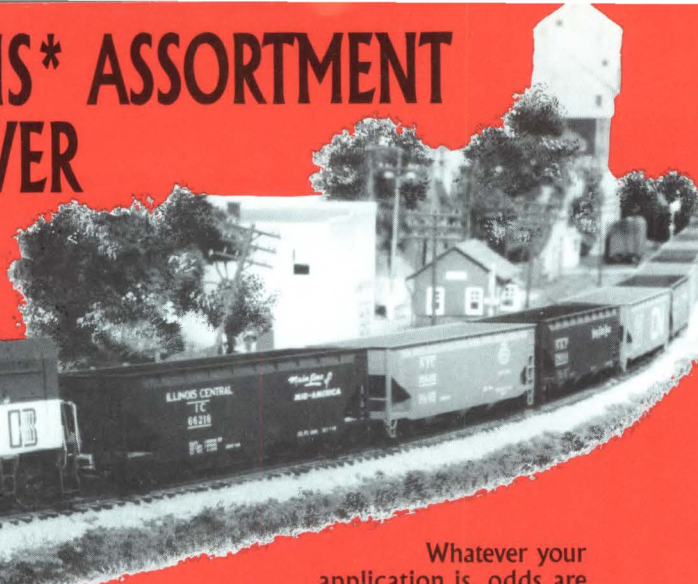
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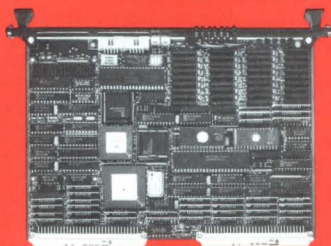


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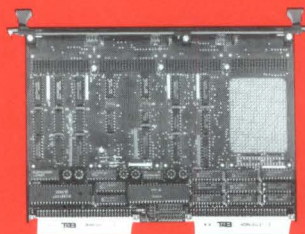
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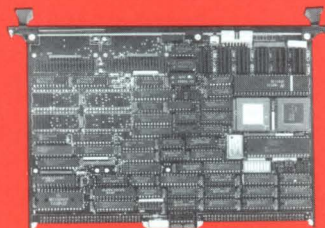
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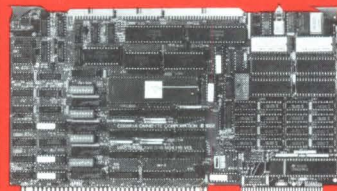
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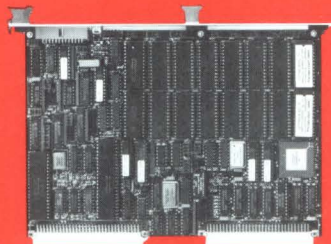
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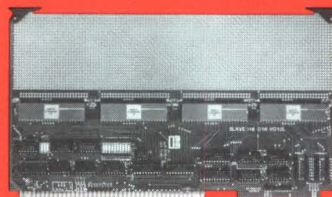
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to demonstrate measurement techniques, there haven't yet been any significant performance measurement results. SEI hopes that Dark will demonstrate the feasibility of real-time distributed Ada applications, serve to educate users in evaluating kernels, and encourage development of similar commercial kernels.

Ada users who need to immediately implement distributed processing systems can turn to the ARTX kernel from Ready Systems. ARTX allows use of Ada real-time tasking semantics, or of Ready Systems' own tasking commands, and ARTX supports multiprocessing. But ARTX works only with processors that use a single, shared memory. In addition, communication in ARTX looks different when software runs on one processor, as compared to running across several processors. This means that Ada programs written for one system configuration will usually have to be changed before they can be run on another.

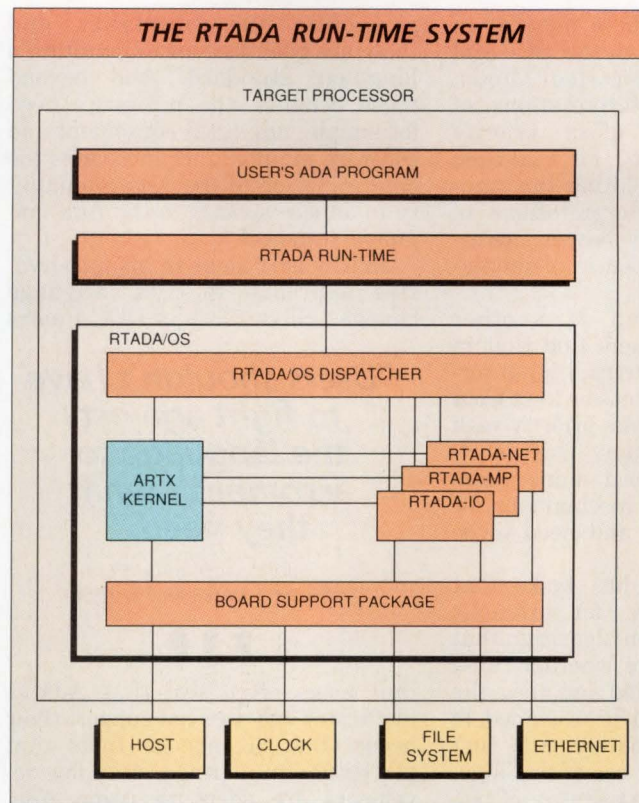
Industrial Programming (Jericho, NY) offers a package called MTOS-UX/Ada. This package, based on the company's MTOS real-time kernel, allows Ada programs to be run on multiple processors and accepts normal Ada tasking commands. Ada programs are handled transparently by MTOS-UX/Ada, so that Ada code can be handled with automatic load balancing over up to 16 processors, each of which has its own memory, according to Bernard Mushinsky, IPI sales manager.

MTOS-UX/Ada is, however, a rather specialized solution to the Ada distributed computing problem. Each processor must run the MTOS kernel, and MTOS-UX/Ada can be used only with code produced by Telesoft Ada compilers.

Those who note that Ada users must turn to facilities outside the language itself to meet distributed and parallel system needs have probably entertained the thought that revision of the Ada language itself should be considered.

■ Debate to shape Ada's future

Few outside the Ada community are aware that, sometime in the 1990s, a new version of the Ada language, provisionally called Ada 9X, will be officially adopted. The shape of Ada 9X is now under debate among Ada standards makers, vendors, and users. The basic issue in the debate is how to untie some of the knots that



The RTAda run-time system allows an embedded Ada program to make use of the RTAda/OS operating system, which provides the Ada program with the real-time capabilities of the ARTX real-time kernel from Ready Systems. ARTX functions are similar to those of the popular VRTX kernel. RTAda/OS features include RTAda-IO for target file and stream I/O, RTAda-MP for multiprocessing, and RTAda-Net for networking.

make Ada difficult to use.

One of those knots is that only FIFO (first-in, first-out) queues are permitted within the Ada language. Lee Silverthorn, president of DDC-I (Phoenix AZ), is among those who believe that the Ada language itself should permit the use of other types of queues as well. FIFO queues are appropriate for time sharing, but for many real-time systems, priority queuing is preferable. After careful consideration, Silverthorn and his colleagues have concluded that the Ada language requirement for FIFO queues should be dropped, since that would open the language not only to priority queues but to other types of queues as well.

Silverthorn notes, however, that with the FIFO requirement removed from Ada, users of FIFO queues will have to do some reprogramming with each new implementation, because the queues would no longer be a part of the Ada language standard.

With no particular type of queuing specified in the language, says Silverthorn, module portability and 80 to 90 percent overall portability could still be achieved for Ada software. There would have to be some reengineering when the software was ported to a new microprocessor or a new computer, and Ada users would have to know that queuing

was one of the language's implementation-dependent features. In any case, Silverthorn believes, Ada portability has been oversold; naive users may expect Ada programs to be completely portable, but that is unrealistic, given the current state of the software art.

■ Priority queuing already supported

Another, quite different solution to the problem of using priority queues with Ada is proposed by a report from SEI, which states that priority queuing can already be supported in Ada. The reasoning is that a task can be preempted while attempting to make an entry call, but before its call is queued.

Suppose, for example, that a low-priority task is in rendezvous with task S when a medium priority task, M, is preempted just before the call is made, so M is suspended, and the rendezvous continues. Now suppose a high-priority task, H, starts to execute and also attempts to call S. H is similarly suspended just before the call, and L's rendezvous with S continues. Now when the rendezvous is completed, the highest priority task that is ready to run is H—that is, in effect, calls are made in order of priority.

This sequence of preemptions is allowed by the standard, according

■ ADA

to John Goodenough, a member of the technical staff at the SEI and chair of the Ada Rapporteur Group, which develops interpretations of the Ada rules. In effect, priority queuing can be used for real-time systems without violating the standard. Legalistic interpretations of this kind apparently become necessary to provide needed implementation flexibility.

Priority inversion is another source of debate. Users find that in their Ada-based systems, high-priority tasks can sometimes be kept from running while a lower priority task occupies the computer. This shortcoming has convinced many users that Ada language mechanisms for tasking are flawed and need to be changed.

When a system has tasks that execute periodically, for example, there is a well-known algorithm that is used to determine whether those tasks can be scheduled and, if so, the priority that should be assigned to each task. Unfortunately, Ada isn't able to make proper use of this algorithm because the possibility of priority inversion is always present. According to IBM's Fisher, the most difficult priority inversion problems arise when periodic and nonperiodic tasks are mixed together.

Fisher believes that it might be a good thing to have some Ada options that allow scheduling with priority inheritance to avoid priority inversion. At the same time, he isn't sure that Ada language changes are needed to solve this problem.

Fisher notes that SEI's Goodenough and Lui Sha, professor of computer science at Carnegie-Mellon University (Pittsburgh, PA) have proposed a priority ceiling protocol, which minimizes priority inversion effects, while avoiding any need for changes in the Ada language. However, says Fisher, this approach works for only a limited set of problems, and more work is needed to find out about situations where both periodic and nonperiodic tasks have to be scheduled.

■ Opposing Ada changes

Ada guardians, such as Charles McKay, director of the NASA Software Engineering Center (Clear Lake, TX), insist that there should be only minimal change in the Ada language because the standard language definition is perhaps Ada's most basic strength. A firm standard implies a capability for software

portability and reusability, and these are good reasons to maintain a language standard. And beyond these benefits, the military's need for simple, universal equipment and software maintenance motivates the determination of the Ada community to adhere strictly to the Ada language standard.

McKay isn't alone in his conservative approach to Ada language changes. Silverthorn of DDC-I notes

"Users shouldn't have to fight against the language to accomplish what they need."

—John Goodenough,
Software Engineering Institute



that users often feel that Ada is inefficient and does not support their needs. But Silverthorn finds that perception uninformed, since few developers are adept at using Ada. Silverthorn believes that Ada "is actually pretty good" for those who learn to use it effectively. To increase knowledge of Ada, he says, better documentation is needed, as are clear practical examples of how the language can be used.

IBM's Fisher concurs. "At this point it's desirable to make minimal changes in the Ada language, particularly in areas that aren't well understood."

SEI is studying certain specific areas of potential changes to Ada,

including possible changes to better support real-time applications. SEI's Goodenough isn't yet clear on which proposals for change are properly language concerns and which should be handled by run-time implementations.

For example, says Goodenough, initial discussions of priority inversion revealed that, when programming in a certain style in Ada, priority inversions can frequently occur. Subsequent study has shown, however, that there are ways to get around that problem and that changes to the Ada language may not be needed to minimize the priority inversion problem.

The Ada language allows a lot of run-time flexibility, Goodenough notes, and system developers need to understand how to exploit that flexibility to get what they need.

Goodenough and his colleagues are trying to analyze what applications programmers' real requirements are, and why they find it difficult to meet them in Ada. That knowledge will, he believes, lay a basis for decisions on where language changes are needed, and where there should be more direction given to implementers.

Goodenough recognizes, however, that even if virtually everything users need to do can be done with the Ada language as it exists today, that still doesn't solve the practical problems users face as they search for economical system designs. As he puts it, "Users shouldn't have to fight against the language to accomplish what they need. The language should work with them." □

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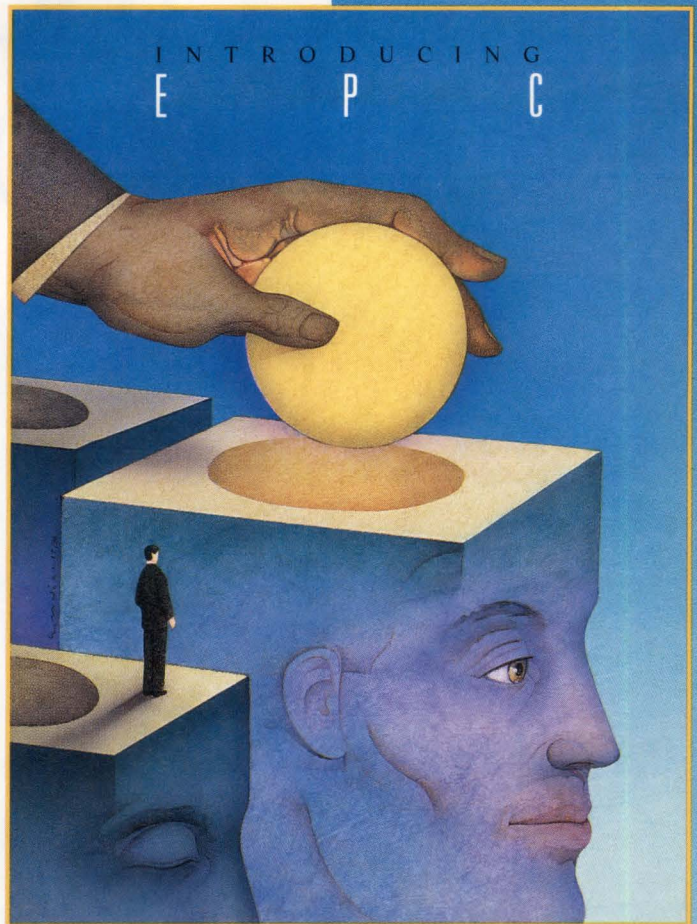
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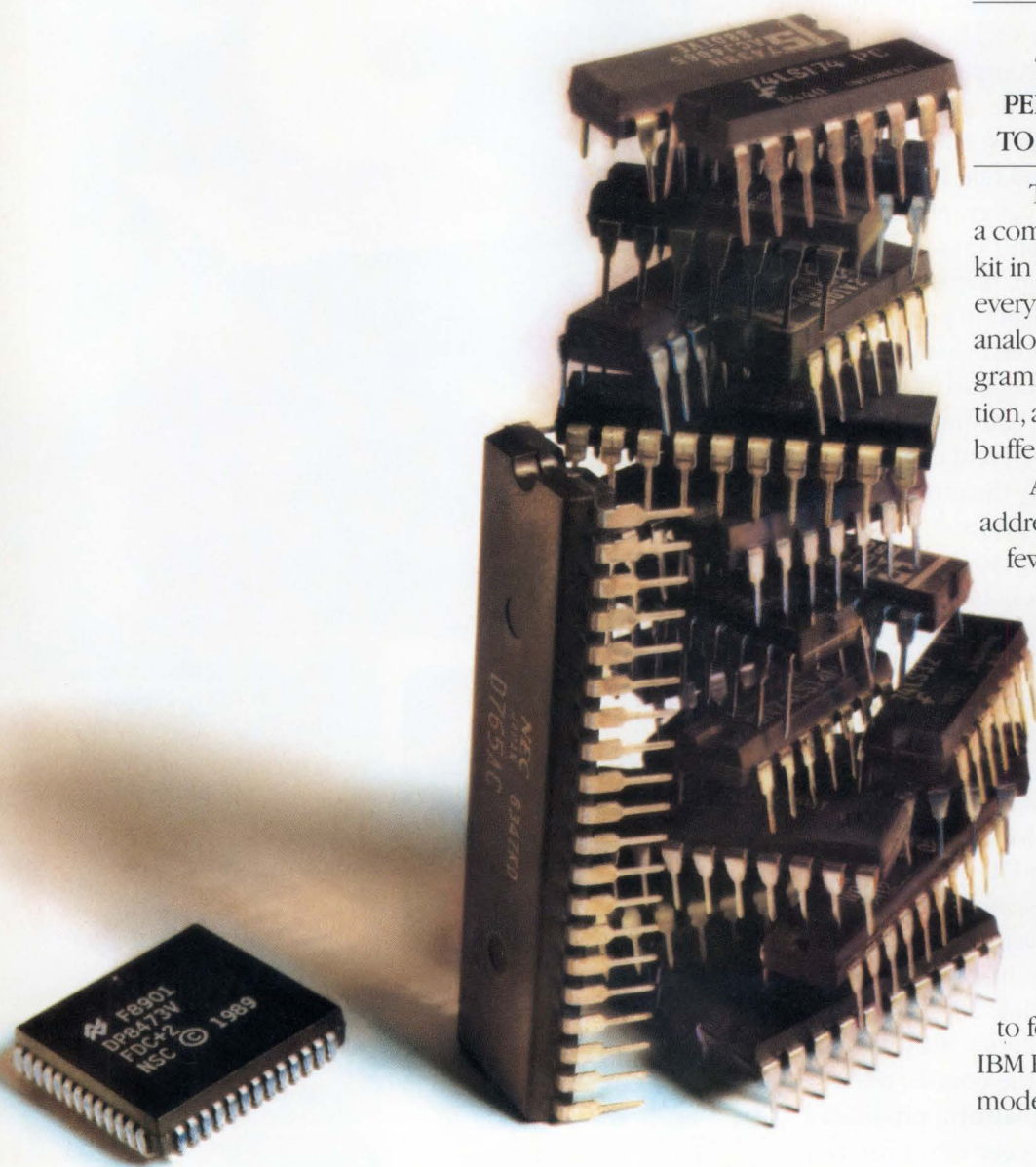
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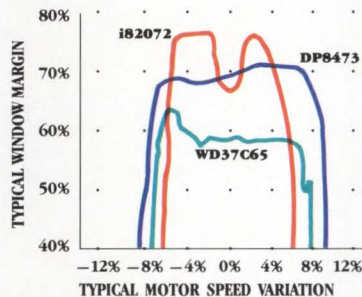
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Distinctions blur between DSP solutions

Warren Andrews
Senior Editor

A wide variety of chips move to higher levels of integration, making previous distinctions ambiguous and heralding a new generation of DSP technology.

Digital signal processing techniques have emerged from the laboratory and are rapidly being put to work in real-world applications. The implementation of such techniques, however, has been anything but orderly and predictable. DSP functions have migrated from bit-slice processors to building-block approaches to microcontrollers and single-chip DSPs. Now, the introduction of high-performance microcontrollers, combined with the emergence of the latest-generation RISC and CISC processor chip sets and improved application-specific IC technology, greatly clouds over distinctions in applications—perhaps heralding yet another generation of DSP.

Ultimately, the application itself—and a determination of some kind of price/performance ratio—will determine the particular DSP implementation. Early DSP applications were primarily in the military and very high end array processing where the emphasis was on the performance rather than on the price end of the equation. Implementations of such applications usually took the form of boards full of the highest-speed logic and DSP building blocks available.

“The underlying thrust now in the

DSP arena is to try to match the cost and performance of the DSP solution to the application,” says John Reimer, marketing manager for microcomputer and communications products at Fujitsu Microelectronics. “But this hasn’t always been so easy since many of the emerging applications are in extremely cost-sensitive consumer areas such as digital audio and television.”

Steve Brightfield, DSP product marketing manager at Plessey Semiconductors (Scotts Valley, CA), agrees, citing high-definition TV as a leading driver of DSP technology. Brightfield believes, however, that the HDTV and computer imaging applications will soon use the same DSP technology.

■ The verge of a new technology

The confluence of faster and denser silicon with the increasing sophistication of DSP algorithms has resulted in many DSP applications previously handled by boards now being taken over by single-chip solutions. In addition, as these single chips advance along the cost/volume learning curve, they begin to yield cost-effective DSP solutions to problems that have traditionally—and until now, most economically—been han-

dled using analog techniques. But even as these new parts emerge, we seem to be on the edge of yet another generation of DSP technology.

Only a year ago, DSP applications were neatly divided among building-block approaches, algorithm-specific (special-function) DSP chips and general-purpose DSPs. The key to selecting an approach was then, as it is now, almost completely a price/performance judgment. Over the past year, though, a host of new products have been changing the complexion of the industry.

At the low end, DSP-based microcontroller products are starting to resemble more conventional microcontrollers. Microchip Technology (Chandler, AZ), for example, incorporated the core of the 320C10 from Texas Instruments (Dallas, TX) with the I/O normally found in conventional microcontrollers. The resultant chip has found broad-based applications in everything from servo control for disk drives to talking dolls. And the addition of such things as an on-board analog-to-digital converter and EEPROM may well put DSP-based controllers in contention for sockets in automotive engine control, an area now dominated by such popular microcon-

trollers as the 68HC11 from Motorola (Austin, TX) and the 80C51 from Intel (Santa Clara, CA).

At the higher end of the spectrum, the latest generation of floating-point processors are starting to look more like conventional microprocessors. The four leading contenders in the 32-bit floating-point field, the DSP32C from AT&T Microelectronics (Berkeley Heights, NJ), the 320C30 from TI, the 96000 from Motorola, and the 86XXX from Fujitsu, for example, all address up to 16 Mbytes of memory—up almost tenfold from previous generations.

And while general-purpose DSP chips are starting to resemble conventional microprocessors, conventional—and not-so conventional—processors are starting to look a lot like DSP chips. The chip architectures in some of the recent RISC offerings begin to look suspiciously like a DSP, and many versions of RISC devices are being designed to attack embedded-control applications.

■ Three DSP approaches

There are three fundamental approaches to solving DSP problems: using building blocks, using standard, general-purpose single-chip



■ DSP

DSPs, and using one or more of the custom and semicustom approaches available. Building-block devices continue to provide the highest level of performance, but at a sacrifice of cost, board space and development time. And while makers of building blocks such as multipliers, adders and address generators continue to expand their performance, capabilities and level of integration, cost and system complexity often limit the range of applications.

In the single-chip, general-purpose DSP arena, a variety of vendors both here and abroad have joined Texas Instruments—the leader in single-chip DSPs—in offering such chips. These vendors include AT&T, Motorola, Analog Devices, Fujitsu, Oki Semiconductor, NEC and others, each attempting to sheer off a

portion of what is estimated to be a gigantic market—well over \$1 billion in 1989 and anticipated to grow at 30 percent rate. Most recently, Zoran (Santa Clara, CA) joined the fray, introducing a high-performance floating-point processor that is more adaptable to general-purpose applications than is its previous family of products.

But despite the high level of activity in standard components, some kind of ASIC approach will undoubtedly win in many DSP areas. The applications now emerging will mandate the use of a custom approach, simply because the volumes will be so high, according to Fujitsu's Reimer. He adds, however, that these custom devices will likely take the form of custom versions of standard DSPs.

This trend is already well estab-

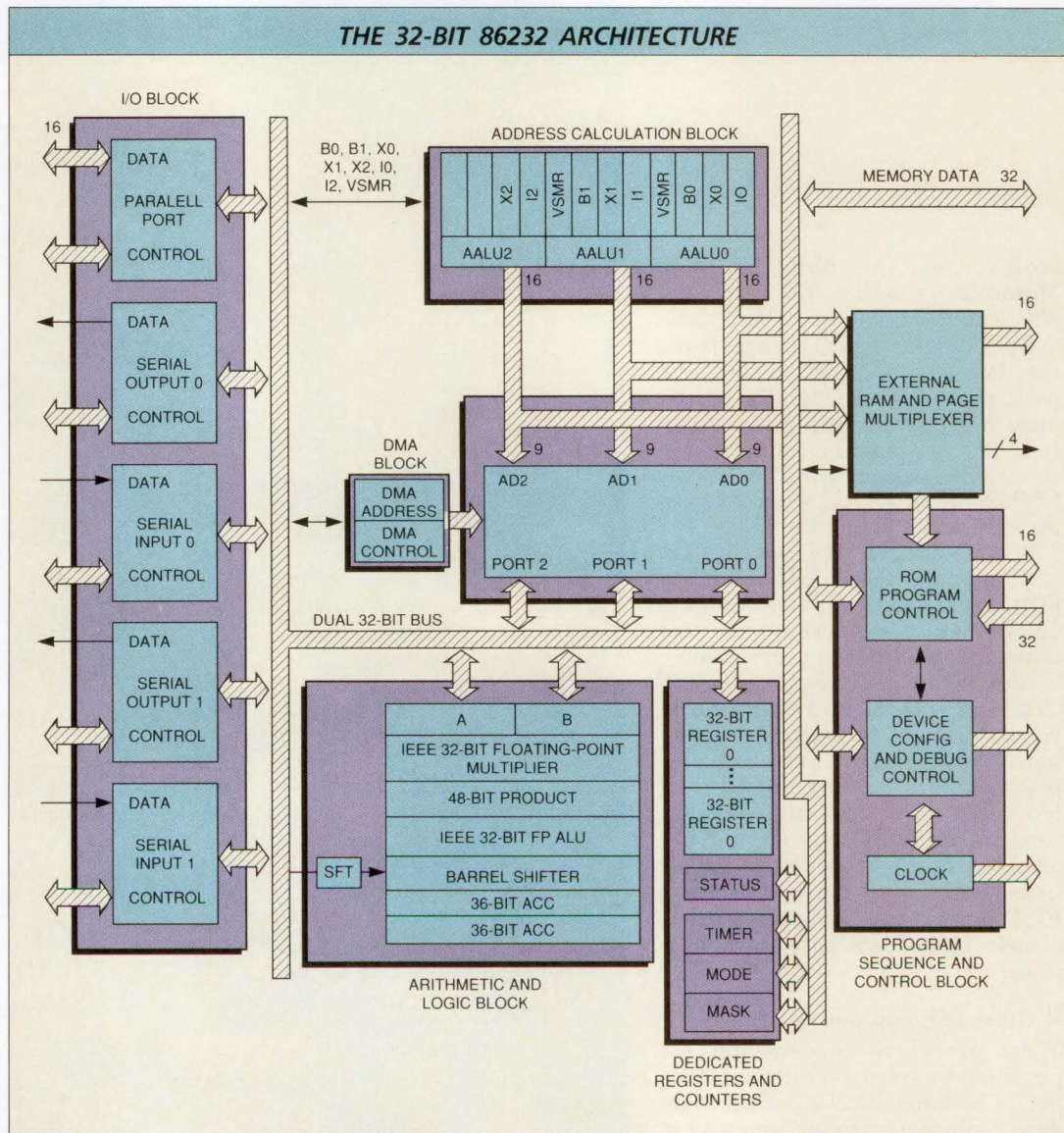
lished in the single-chip arena, where TI has an estimated 70-plus percent of the market. Of this business, some analysts calculate that more than 60 percent of this represents customized versions of standard products in the 320 family of DSPs.

In the truly semicustom DSP arena, an approach pioneered by LSI Logic (Milpitas, CA) involves the placement of a number of multiplier/accumulators (MACs) on a die surrounded by a gate array for customizing the blocks into a function. Subsequently, Plessey Semiconductors developed its own version, providing similar capabilities but with more flexible blocks.

■ General-purpose DSPs

General-purpose DSPs come in two basic flavors: integer and floating-

Fujitsu's second-generation 32-bit floating-point chip, the 86232, is targeted at high-performance applications. It supports 32-bit floating-point, 32-bit fixed-point and 24-bit integer data formats and lets all three formats co-exist within a single program, with type conversion handled by the instruction.



point. Fixed-point devices, or those performing only integer arithmetic, are the fastest and least expensive. It's no surprise, therefore, that they dominate the market. Texas Instruments has been the leader in this area with its 320 family, a variety of NMOS and CMOS devices.

In the fixed-point arena, TI has elected to remain in the 16-bit area, going after a host of applications in speech synthesis/recognition and telecommunications. AT&T Microelectronics also participates in the 16-bit, fixed-point business with its DSP-16 and DSP-16A processors. Boasting the fastest cycle time of any 16-bit DSP (33 ns), the DSP-16A has endeared itself to many designers requiring the fastest possible performance in a single-chip DSP.

Motorola was somewhat behind AT&T and TI in introducing its DSP device, the 56000, to the market, but it incorporated a few twists not available on either the AT&T or TI devices. "For one," says Jane Bates, business manager for Motorola DSP devices, "the 56000 is a 24-bit integer device allowing for 24×24 -bit multiplication with an internal 56-bit accumulator." The greater resolution, says Bates, provides the wide dynamic range required for many speech applications and digital audio.

In addition, says Bates, the 56000 uses a high level of parallelism with three different execution units; a data ALU, address arithmetic units and a program controller. The chip also has six on-board memories, three on-chip microprocessor unit-style peripherals (serial communication interface, synchronous serial interface and host interface), a clock generator and three address and four data buses.

Motorola has also just introduced a companion chip that provides a complete analog-to-digital conversion function as well as an interface directly to the 56000. Called the 56ADC, the chip combines a 16-bit analog converter providing a full 96-dB dynamic range with a digital interface to the Motorola as well as other DSP devices.

Because of the relatively low cost and simplicity of the fixed-point chip, "there will always be a lot of applications for them," says James Flynn, technical product support engineer for AT&T (Allentown, PA).

■ DSP controllers

Yet another area of applications was opened for DSP-based devices when

Microchip, a wholly owned division of General Instruments (Hicksville, NY), introduced its 320C14, a DSP-based microcontroller. Microchip developed the controller in cooperation with TI and surrounded a 320C10 core with I/O and peripheral circuits.

The new architecture represents a revolutionary change in the way engineers will look at control functions—many of whom continue to use analog circuitry because the DSP horsepower hasn't been available at a reasonable price, according to Rahul Sud, vice-president of marketing for Microchip. The ability to perform single-cycle multiplications,

***"There will always
be a lot of
applications for
fixed-point chips."***

—James Flynn, AT&T



says Ajay Padgaonkar, design engineering manager, lets the 320C14 perform many advanced control algorithms such as adaptive control, Kalman filtering and state controllers in real time.

One promising application area for the DSP controller is in closed-loop control where a feedback loop is used to improve control accuracy by compensating for system characteristics. Traditionally, these compensation loops have been built using analog circuitry.

Using digital techniques, such control loops are generally implemented using second-order finite impulse response (FIR) and infinite impulse response (IIR) filters. These digital approaches bring higher reliability, noise immunity and flexibility to such applications. Complex digital filters require, however, computationally intensive sum-of-products calculations, which have traditionally been poor performers, too expensive, or both.

Conventional microcontrollers lack the hardware arithmetic capability and can't compute such filter algorithms in anywhere near real time. Instead, they rely on approximate values obtained by accessing lookup tables—resulting in an inflexible system, often lacking the necessary accuracy. DSP chips, on

the other hand, have the computational capability, but until now, lacked the I/O and peripheral functionality for a practical implementation. Such systems are burdened with enough extra glue logic to make their implementation impractical due to size, cost and/or environmental factors.

■ Floating-point DSPs

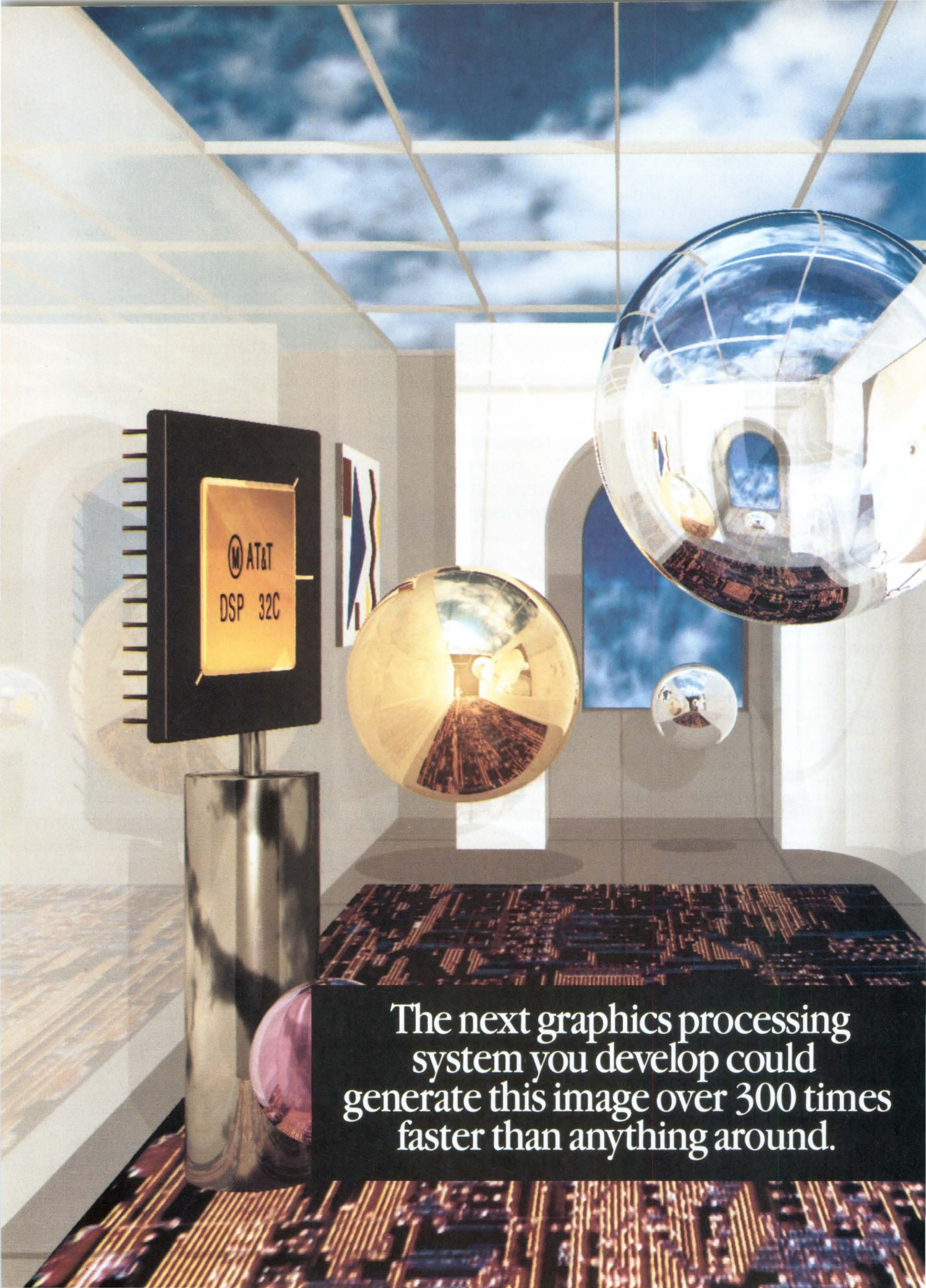
Though fixed-point DSPs will continue to dominate a large part of the very low end market, there are some inherent limitations when doing integer mathematics. The results of multiplications and additions must be scaled, for example, because they will quickly go out of range. Operations to perform this type of scaling are complex and can take many processor cycles, thus greatly reducing system throughput. In addition, there are many algorithms that are extremely difficult or impossible to program into fixed-point devices.

The obvious solution to these problems is to use a floating-point unit. Because of their added complexity, however, floating-point chips have traditionally been slower and as much as two to three times more expensive.

But clearly there are factors that favor the selection of a floating-point device. Floating-point chips are far easier to program and frequently require considerably fewer support chips to integrate into a system. Some of the trade-offs that must be considered in designing a DSP system include development/programming time and other nonrecurring engineering costs, which often offset the higher price of floating-point parts.

The first of the general-purpose floating-point devices to hit the market was AT&T Microelectronics' 32-bit DSP32. The chip comprises a full 32-bit floating-point processor operating at 25 MHz and capable of performing 12.5 MFlops. In addition, it includes a 16-bit address space, a 12.5-Mbit/s serial I/O port and an 8-bit serial port.

The second generation of the part, fabricated in 1-micron CMOS, as opposed to the original NMOS part, doubles the operating frequency to 50 MHz, letting the chip perform 25 MFlops. In addition, the address space was increased from 16 to 24 bits, the speed of the serial I/O port increased from 12.5 to 16 Mbits/s and that of the parallel I/O port increased from 8 to 16 bits.



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Note: The AT&T DSP line now also includes a new 16-bit, fixed point, CMOS device—the DSP 16A—that runs at a record 33ns, and offers more on-chip memory than any other fixed point DSP.

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Image created at R/Greenberg Associates on Pixel Machines' PXM 900 Series graphics workstation, using AT&T's first generation floating point DSPs.

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The right choice.

Combining RISC and DSP for high-performance imaging and control

RISC-based microprocessors, such as the Am29000 from Advanced Micro Devices (Sunnyvale, CA), and digital signal processors, such as the DSP32 from AT&T Microelectronics (Berkeley Heights, NJ), are at the cutting edge of today's technology. Both evolved from a common CISC heritage of 8-bit, then 16-bit, general-purpose microprocessors, but their paths diverged in response to the specialized needs of their intended markets.

The Am29000 is a high-performance embedded controller and is optimized for moving vast quantities of data between memory and I/O devices with only minimal operational processing of that information. The DSP32 is optimized to perform mathematical transformations on blocks or streams of digital data, but it doesn't have the flexible data movement or interrupt response that marks the Am29000.

Both processors have in common the ability to function in tightly coupled multiprocessor systems. We can point out the differences and complementary strengths of these devices by looking at an example application.

We are going to design a RISC- and DSP-based mail delivery robot (see figure at right) for a hypothetical high-technology company that never stops asking, "What if..." The robot will be able to wander the building, looking out for objects in its path with dual video cameras that provide location and depth information. In addition, the robot will recognize several basic spoken words,

such as "stop," "go," "slow" and so forth. It will also speak phrases such as "Excuse me," "Any mail for delivery?" and "Do you want that with double cheese?"

The DSP32 will be responsible for the visual and aural signal processing, while the Am29000 will coordinate the overall operation of the robot. This latter function includes operation of the drive motors and steering, generation of the synthesized voice, and control of the information streams from the DSP system.

Two video cameras, with charge coupled device (CCD) image sensors, provide a stereoptic view of the path ahead. The output of the CCD array passes through video analog multiplexing gates, followed by a low-resolution (6-bit) analog-to-digital converter. A frame grabber then captures the image and shifts it out serially. This data stream, which represents a grayscale for the image on each of the pixels of the CCD array, is fed directly into the serial I/O (SIO) port of the DSP32. There, it's reconstructed into bytes of data and placed directly into an image buffer in memory, utilizing the DMA feature of the SIO. The images are taken into memory at a rate just slower than the time required by the DSP32 to process an image.

The DMA provides for images to be brought into the "background" while the processor is working on the previous image. The instruction set of the DSP, which is optimized for the math-

ematical operations of multiply and accumulate, rapidly produce the Fourier-transformed image analysis of the video scene. The relevant elements of these transforms are then stored in local memory.

The Am29000 is also doing what it does best. Addressing the parallel I/O (PIO) port of the DSP as an I/O peripheral, it sends an updated block of previously stored video information to the DSP through the built-in DMA within the PIO. This preprocessed video information is used by the DSP to compare current video data with preprogrammed data.

When the difference calculation is completed by the DSP, it indicates this in the mailbox within the PIO, thus interrupting the Am29000. The Am29000 then retrieves the Fourier difference data from a buffer within DSP memory, while the DSP proceeds to process the next image that has already been placed in its buffer. The Am29000 then uses this data as course update and correction information.

Periodically, the DSP checks its audio frame buffer for any information needing to be processed. The audio buffer is a simple microphone, amplifier, A-D converter and local memory, all under the control of a processor such as an 8052. The 8052 is memory-mapped into the DSP's address space. If the DSP sees that a verbal command has been given to the robot, it places a message in the mailbox of the PIO, interrupting the Am29000 and causing

Marc Davidson, software engineer, and **Arnie Berger**, R&D project manager, Hewlett-Packard Logic Systems Division

One of the novel features of the DSP 32, says Kreg Ulery, technical product support engineer at AT&T (Holmdel, NJ), is that the memory can be used for either program or data; it doesn't have a strictly defined program or data section. There is a separate parallel port on-chip, which lets one program load via DMA into the address space while the chip is still executing another program. This feature is used to dynamically download a different application while the first application is still running. This permits close to real-time context switching.

Another feature of the DSP32, preserved on the 32C, is that the

address space is byte-addressable. This means it isn't necessary to waste a complete 32-bit location to store an 8-bit pixel value or, in telecommunications, an 8-bit word as used in companded u- or a-law calculations.

In addition to having a larger memory address space, the 32C has an enhanced memory interface that has a flexible wait-state mechanism, which lets the chip talk to slower memory. The typical way to do a wait state on a DSP, says Ulery, is to add an entire instruction cycle in addition to the normal memory access time for each wait state. In a conventional DSP chip, Ulery says,

the memory access time might be 35 ns while the instruction cycle time might be 100 ns. Thus, the access time would run 135 ns for memory that needed only slightly more than the 35-ns access.

In the 32C, by contrast, wait states are segmented into one-quarter of a cycle. A single wait state of the 32C, therefore, is only 20 ns (80 ns total cycle time), according to Ulery. Wait states can therefore be incremented in quarters of an instruction cycle.

Yet another modification in the 32C is its ability to use more than one type of external memory. Thus, the 32C was designed with two inde-

an immediate change in action.

The Am29000 is controlling all of the locomotive functions of the robot, as well as monitoring all systems' functionality. With its large, internal instruction and data caches, it easily digests the large quantity of course information coming back from the DSP, as well as

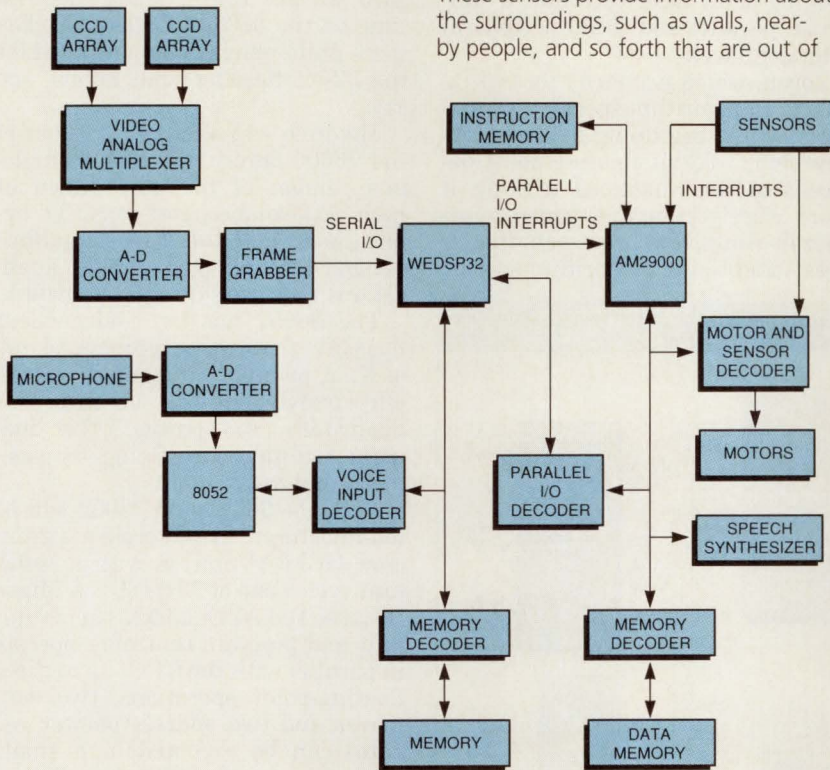
sending down large amounts of the prestored course data. (A 30-MHz Am29000, with its instruction and data buses performing simultaneous burst-mode transactions, can move information at 240 Mbytes/s.)

Also connected to the Am29000 are the numerous tactile sensors located around the periphery of the robot. These sensors provide information about the surroundings, such as walls, nearby people, and so forth that are out of

view of the TV cameras. Certain high-priority sensors, such as the built-in smoke detector, cause an interrupt to the Am29000 requesting immediate attention. The Am29000 also operates the speaker and speech-synthesis circuitry. Using its block move and rapid interrupt response capabilities, the Am29000 provides a safe-operations envelope for dangerous situations.

The data in each processor is organized in a way that provides the most efficient use of the processor buses. On the DSP, the program that operates on the data is stored in internal RAM and the image data is stored in external RAM. This lets the processor access a piece of image data while it's setting up the internal bus for the next instruction fetch. The Am29000 takes advantage of separate program and data memories, which allows the processor to read the status of the attached peripherals while the instructions cache is filling up with the next instructions to be executed. These memory configurations help achieve the maximum processor bandwidth.

Finally, a word about how one might go about developing a product such as this. The design of systems that depend upon tightly coupled multiple microprocessors depends, in turn, upon development tools that are designed to be used in a multitool environment. It's false economy to attempt to design a sophisticated multi-processor system without development tools of comparable sophistication.



pendent speed partitions so it's possible to run part of the memory very fast while running other parts of the memory at a much slower rate. This is advantageous in programs where speed is critical for most of the program being run, but where there is some data that is accessed only every few instructions. Adding wait states to the regular program execution could be fatal, dropping total throughput below acceptable levels. Adding a wait state or two only every few instructions, however, wouldn't cause a major performance penalty yet would permit the use of slower, less expensive memory.

Like AT&T's 32C, TI's flagship

product, the 320C30 32-bit floating-point processor, incorporates many of the functions found in many conventional microprocessors, such as memory addressing range, interrupt and DMA features.

The 320C30 tops AT&T's 32C with a 33-MFlops performance, which translates into a 60-ns cycle time. Key features of the C30 include a pair of 1k×32-bit single-cycle, dual-access RAM blocks; a 4k×32-bit, single-cycle dual-access ROM block; a 64×32-bit instruction cache; 32-bit instructions and data words; a 24-bit address space; a 32-/40-bit floating-point integer multiplier; and a 32-/40-bit floating-point

integer.

Fabricated in a 1-micron CMOS process, the C30 makes it through the 1,024-point fast Fourier transform benchmark in only 1.67 ms. Other benchmarks noted by TI include an FIR filter tap with data shift performed in 60 ns, and a cascaded IIR biquad filter element with five coefficients performed in only 360 ns.

■ 32- and 24-bit floating point

Fujitsu's latest entries into the single-chip, general-purpose DSP market include a 32-bit floating-point device, the MB 86232, and a 24-bit floating-point part, the MB 86220.

■ DSP

The 32-bit part supports 32-bit floating-point, 32-bit fixed-point and 24-bit integer data formats and allows all three formats to coexist within a single program with type conversion handled by the instruction.

The 32-bit chip comprises six functional blocks: program sequence control; address calculation; data RAM; arithmetic and logic; dedicated registers/counter; and the I/O interface. All blocks are tied to the internal twin 32-bit data buses, which handle data transfer between registers and memories.

While the 86232 is the flagship of Fujitsu's DSP family, competing head to head with the 32-bit floating-point parts from TI, AT&T and Motorola, the part that has attracted the most interest is Fujitsu's 24-bit floating-point device, according to Reimer. With the same 75-ns cycle time as the 32-bit device, the 24-bit part uses a Harvard architecture,

has $2k \times 30$ bits of on-chip program memory, and can address an additional $64k \times 30$ of external program memory.

"What's most exciting about the 86220," says Reimer, "is the level of performance it delivers for the price. The chip sells for \$30 each in quantity, making it the lowest-priced floating-point DSP chip available." In addition, the chip has been developed with what Reimer calls "an innovative ASIC DSP design approach." The part consists of a 24-bit, floating-point DSP core and a universal parallel and serial peripheral interface block.

Zoran, which primarily focuses its efforts on algorithm-specific DSP devices, is just beginning to sample its new 34325 32-bit floating-point device that has functions making it more closely resemble general-purpose floating-point processors than it does traditional algorithm-specific

devices. Designed to operate at 25 MHz, with some of its speed distribution expected to fall in the 30-MHz speed range, the part will perform a complex 1,024-point FFT in about $1,400 \mu s$ and a 32-tap FIR of 128 real points in $318 \mu s$. These performance specifications place Zoran's 34325 squarely in competition with the parts from AT&T, TI, Fujitsu and Motorola.

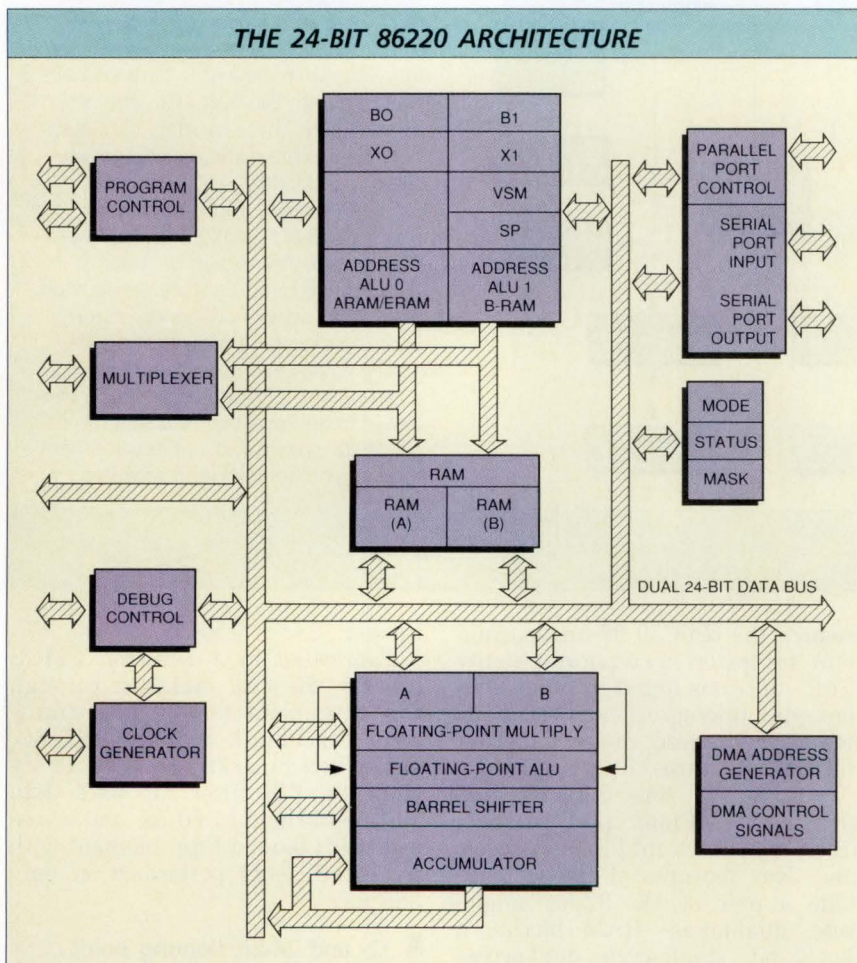
Motorola has been slow in getting its floating-point processors up and going. "We took our time to make sure we got things right the first time on the 56000," Bates says. The same philosophy is being adopted for the 32-bit floating-point 96000, she says.

Motorola will offer two versions of the 96000 family: the 96001 single-bus version of the part aimed at high-performance, cost-sensitive applications, and the 96002 dual-bus version for high-performance applications requiring a high bandwidth.

The 96002 has two independent bus ports that can be assigned to any of X, Y, or program memory spaces, effectively doubling off-chip bus bandwidth. In addition, the dual ports facilitate interfacing to page-mode and video RAMs.

Both the 96001 and 96002 will be manufactured in Motorola's 1.2-micron HCMOS process with a resultant cycle time of 75 ns (13.33 Mips). Because the ALU, address generator unit and program controller operate in parallel with the CPU, up to three floating-point operations, two data moves and two address pointer updates can be executed in a single instruction cycle. This parallelism lets peak performance on the chip reach 40 MFlops. Twin DMA controller channels operate in parallel with the CPU to provide memory-to-memory and memory-to-peripheral transfers. Benchmark results for a 1,024-point complex FFT, says Bates, come in at less than 2 ms. And, she adds, the chip can process over 2 million interrupts/s.

The ALU on the 96000 family conforms with the IEEE 754-1985 standard for binary floating-point arithmetic and supports all four rounding modes. The data ALU also supports integer arithmetic, including a 32×32 -bit multiplication with a full, nontruncated, 64-bit product.

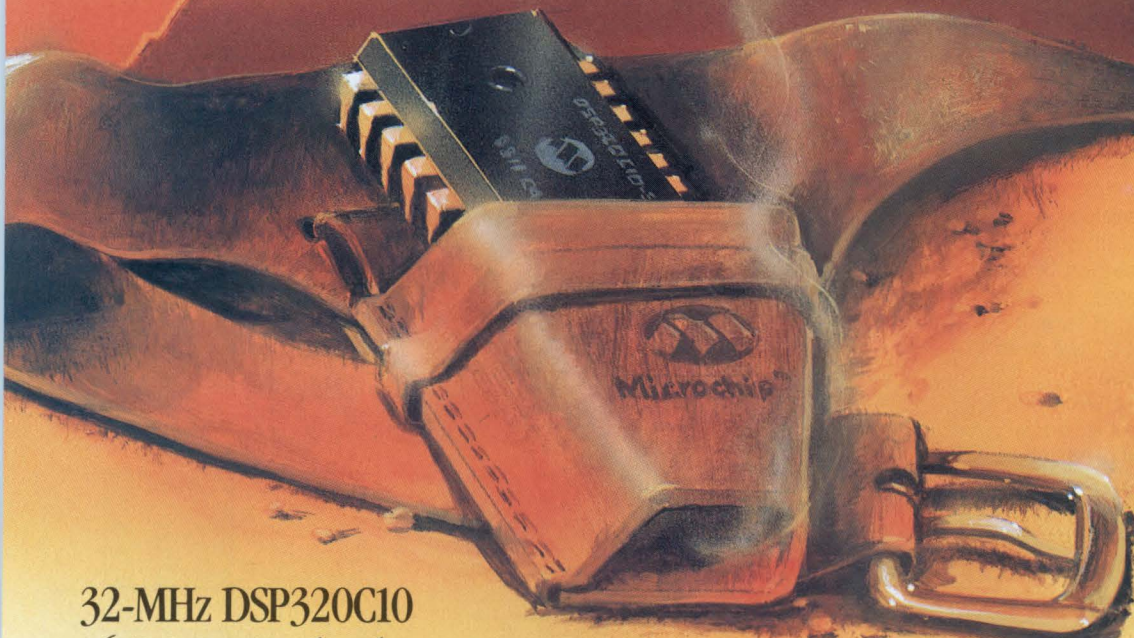


Fujitsu's latest entry in the floating-point DSP market, the 24-bit floating-point 86220, is likely to raise some eyebrows with its \$30 price tag. Like Fujitsu's 32-bit floating-point chip, the 86220 has a 75-ns cycle time. The chip has been designed using a proprietary ASIC approach so the DSP core can be surrounded with other peripheral and I/O circuits for a customized version.

■ ASIC interpretations

"Though standard parts continue to proliferate, the nature of DSP applications will dictate that many of the

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DSP320C10-25B/QX	25.6	40L CER SIDE-BRAZE	5962-8763302QX
DSP320C10-25B/UX	25.6	44L CER LCC	5962-8763302XX
DSP320C10/P	20.5	40L PLA DIP	
DSP320C10/L	20.5	44L PLCC	
DSP320C10-B/QX	20.5	40L CER SIDE-BRAZE	5962-8763301QX
DSP320C10-B/UX	20.5	44L CER LCC	5962-8763301XX
DSP320C10-14/P	14.4	40L PLA DIP	
DSP320C10-14/L	14.4	44L PLCC	
DSP32010-B/QX	20.0	40L CER SIDE-BRAZE	8405301QX
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DSP and RISC merge in 80860

Though DSP chips are widely considered to be a special subset of RISC technology, the distinction between DSP devices and general-purpose microprocessors has generally been relatively well defined—until now, that is. The announcement of the megatransistor 80860 RISC processor from Intel (Santa Clara, CA) may usher in a new generation of DSP devices.

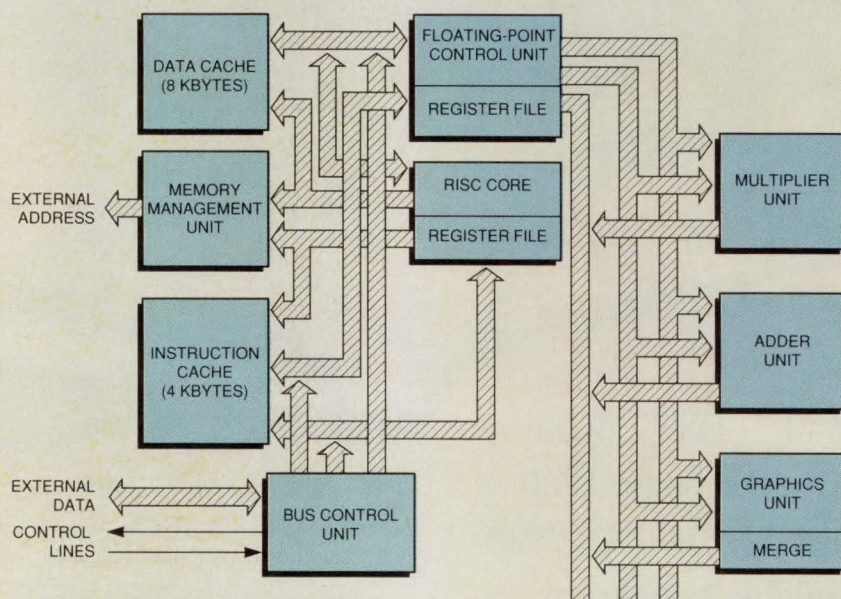
Since its announcement, the 80860 has received an almost unprecedented amount of press coverage from both the trade and international business press, which heralded it almost as a "second coming" of the microprocessor. This coverage, combined with the previously generated excitement over RISC architectures, prompted at least one observer to comment, "I haven't seen so much media hype in one place since the Volkswagen Beetle."

But as the media dust settles down a little and the 80860 is subjected to closer scrutiny, it's interesting to take a look at how closely it maps—particularly in certain areas—to more traditional DSP architectures. The 80860 comprises two processing units, each with its own set of 32, 32-bit registers. One processing unit handles integer operations while the other handles floating-point and graphics operations. The two can operate independently or work together to provide some high-power DSP-class performance.

With its highly parallel architecture

and tight coupling of the integer and floating-point units (similar to the architectures found in the leading 32-bit floating-point DSPs), the 80860 is capable of generating a new result each cycle. Thus, operating at 40 MHz, the chip can theoretically crank at a rate of 40 integer Mips and 80 single-precision MFlops. Benchmarks claimed by Intel peg the peak performance of a 40-MHz 80860 at 105 kDhrystones and 26 MWhetstones—performance to be envied by many DSP chips.

The 80860's floating-point units, the FPU adder and FPU multiplier, are designed to operate in parallel as well as exchange data between each other. Once again, this shows a similarity to many conventional DSPs. And unlike classical RISC implementations that have a fixed number of stages, the FPU on the 80860 has a set of pipelined stages that can be invoked depending on the precision and operation required. The FPU adder delivers a 32-bit or 64-bit result for each clock cycle, and the



solutions will be implemented in some custom or semicustom technology," says Plessey's Brightfield. The evidence strongly suggests his conjecture may be correct. Certainly in the low-end applications of speech synthesis and recognition systems, cost pressures will bear heavily on DSP decisions. And in consumer audio and video products, the same cost pressures will continue to push vendors into ASIC solutions.

TI's experience in providing volume DSP solutions to modem manufacturers, and using them in its own speech products and other consumer items is evidence of this trend. The fact that Fujitsu initiated an entirely new design for its 24-bit floating-point chip so it could be a "core" cell in an ASIC approach is additional testimony to the direction in which the company believes the DSP busi-

ness is migrating.

AT&T, says Flynn, is also looking to incorporate its DSP functions as cells in its ASIC library for fast turnaround of ASIC DSP chips. And Microchip's incorporation of the 320C10 into its 320C14 microcontroller is only the beginning of a new family of DSP controller chips likely to emerge in coming months.

Plessey, says Brightfield, has been carefully looking at applications in image processing, with the obvious implications for digital TV and HDTV. Plessey's approach, similar to that of LSI Logic, calls for an array of MACs combined with a gate array and surrounded by mask-programmed I/O. To illustrate the concept, and to provide a vehicle for customers to exercise the technology, Plessey has developed a few standard products, including a sin-

gle-chip convolver that has integral line delays.

The convolver, for use in image processing, incorporates a MAC array that can be multicycled at double or quadruple the pixel rate. This lets the array be configured in a variety of ways with different window size, depth and pixel rates. While the part is designed for a specific job, it's intended to demonstrate the performance capabilities of the MAC arrays with associated logic. The gate array incorporated with the device is Plessey's sea-of-gates approach, which provides flexibility for incorporating a variety of additional functions on the chip.

"One of the main advantages of using a multiple MAC array," says Brightfield, "is that the sample rate can be pushed well above the current limit of 100 KHz imposed by proces-

multiplier can produce a 32-bit answer in a single clock period, or a 64-bit result each two clock periods.

■ Equipped for graphics

Three-dimensional graphics is one of the more computationally intensive chores for which conventional DSP chips are often called in to manage. The 80860 not only provides the math capability to handle graphics processing, but also adds a graphics processor to help in transforming and manipulating images. Object information is normally stored as a list of three-dimensional vertices. A 4x4 matrix representing the translate, scale, and rotate operations is used to calculate the parameters of the image.

The 80860 is well adapted to executing such chores, holding key values of the transform matrix in the floating-point register and applying them to the display list passing from memory through the data cache and into the FPU register file. Intel estimates that 3-D transform rates can peak at over 500,000/s for 3-D matrices with clipping tests and perspective.

The graphics capabilities are further enhanced by the graphics processor, which handles pixel interpolation and Z-buffer checking. The graphics unit handles pixel data, operating on data concurrently by adding a word with multiple pixels to another word—all in a single cycle.

The graphics processor resides in parallel with the FPU adder and multiplier units, using the chip's internal buses to connect to the floating-point registers.

The computational-intensive capabilities of the 80860 give rise to speculation that the N in the original code name for the part, N-10, referred to its "numeric" capabilities and that the part was initially conceived of as a numeric and graphics processor. Though vehemently denied by Intel, there is some strong evidence to support the rumor that the part was initially designed as a coprocessor for the 80386/486, according to an article by John Wharton in Mike Slater's *Micro-processor Report* newsletter.

Wharton points to the constraints on the 80860 MMU that were required to make it compatible with the 80386 so that it can share memory page tables with the 386 and 486. Also, he points out, the relatively small (4-kbyte) cache with no provision for a second-level cache is inconsistent with general-purpose programming, yet it can manage a floating-point library or set of graphics routines with no trouble.

While design motivation remains a matter of speculation, there is little room for speculation that the 80860 fits within the architectural and performance area of a high-performance DSP device. The fundamental differences lie in the memory architecture and addressing scheme, which remains strictly in the

general-purpose RISC processor realm.

One need only look at the overall trend in general-purpose DSP machines, however, to see that memory addressing schemes and control logic are moving in the direction of more "conventional" RISC processors.

■ An emerging trend

Intel isn't alone in leaning toward DSP-like architectures. The approach to RISC machines taken by Apollo Computer (Chelmsford, MA) in its Prism has an architecture that starts to look something like the 80860. It uses a 64-bit bus to tightly couple a RISC processor and FPU. And, like the 80860, it uses a 64-bit pluck of two 32-bit instructions simultaneously, one for the RISC processor and one for the FPU.

Though there seems to be an evolutionary pattern emerging, with DSP chips merging into general-purpose processors and general-purpose processors looking like RISC machines, the 80860 represents the first giant step in melding of the two technologies.

And while we know of no major architectural developments on the horizon now, we can expect that this trend will continue. We might even be seeing versions of some of the more popular RISC architectures, such as the MIPS or Sparc, emerge with increased emphasis on signal processing capabilities.

sors using a single MAC. Though advancing technology is likely to push rates to 1 MHz in the near future, the type of sample rates we're looking for now in video applications are in the 10-MHz range; and this is likely to increase to well over 50 MHz for HDTV." This type of performance, he says, will be available only through some kind of array architecture. The MAC array in Plessey's device can, for example, perform a 1,024-point FFT in only 100 μ s, compared with the 1- to 2-ms performance of the single-MAC devices, according to Brightfield.

■ DSP meets RISC

"A DSP," says Reimer, "is nothing more than a specialized RISC machine dedicated to performing math-intensive algorithms. And as conventional RISC chips continue to

mature, there will be less and less differentiation between DSP, RISC and even conventional CISC processors and microcontrollers" he says.

The DSP approach used in any given application, he stresses, is dependent on the all-important price/performance ratio. As a result, designers will "not vote along party lines" for using a DSP chip simply because they're doing a DSP-like function, he says. Increasingly, DSP and RISC processors—and even CISC processors and microcontrollers—will almost be interchangeable in many applications.

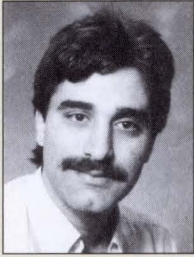
AT&T's Flynn agrees that there are many similarities in architecture between RISC and DSP chip architectures, but he stresses that there's a fundamental difference: a DSP architecture is totally dedicated to providing a multiply/accumulate

in a single instruction cycle. "Almost all DSP applications," he says, "are in embedded control providing some kind of filtering, which requires fast processing of math-intensive algorithms that can't be done using conventional processors."

Flynn points out that applications in disk servo control, radar, cellular telephone, V.32 modems, digital telephone switches, and graphics are "slow to impossible" to accomplish using conventional processors. In addition, he says, DSP devices communicate well with each other, greatly simplifying designs requiring multiple processors.

Despite Flynn's contention that DSP chips have a unique foothold in signal processing applications, many contenders are now vying for some dedicated DSP chip sockets. The most obvious of these is Intel's re-

High-level programming tools guide DSP into mainstream computing



Though initially developed to handle real-time signal processing, DSPs are finding increased use in a variety of mainstream computing applications.

From telecommunications and CAD/CAM to image processing and graphics, designers are using DSPs to tackle a broad range of computationally intensive applications.

As designers apply DSPs in more complex applications, the process of DSP software development is changing. In the past, designers have developed their DSP algorithms on a mainframe in a high-level language and then recoded in DSP assembler to maximize code efficiency and throughput. Increasingly, however, growing application complexity and time-to-market pressures have made assembly-language programming less practical.

With software productivity becoming continually more critical, designers are turning to higher-level programming tools that can slash their development cycles. Semiconductor and third-party software vendors, in turn, are responding with a host of support software. This ranges from simulators, debuggers, compilers and subroutine libraries, to window-based application generators that enable novices to develop DSP applications without writing a single line of code.

■ Optimizing compilers

DSP semiconductor vendors typically provide the base-level software support upon which OEMs, VARs, and end users build more robust application-level software. For the AT&T DSP32, for example, AT&T provides an assembler with a C-like syntax, a simulator, a linker, and a library of commonly used assembly-language math, signal-processing, and matrix routines.

Probably the most significant addition to this toolkit is a Kernighan and Ritchie C compiler. Until recently, a lack of DSP processing power and poor efficiency have stemmed the use of compilers. Significant advances in both processor performance and compiler quality, however, have made the use of

high-level languages practical. In fact, the DSP32's C compiler can often generate code that's as efficient as hand-coded assembler. Designers may still opt to use an assembler to handle speed-critical portions of their applications. They can still use a high-level language, however, to code the bulk of their application.

To boost compiler efficiency even further, AT&T is working on a number of optimizations that, until now, have been used primarily in mainframe compilers. One technique that the compiler uses is to take advantage of the DSP32's high-speed registers. Because register accesses are considerably faster than main memory accesses, the optimizer can greatly speed program execution by identifying and moving often-used arguments, local variables, and loop variables from main memory to registers.

To make the most of its register resources, the optimizer uses register overloading. Often, two variables that use different registers are active at different times. To conserve register space and eliminate unnecessary register save and restore operations, the optimizer stores both variables in the same register. This improves performance because it allows the optimizer to fit more variables into scratch registers, which don't have to be saved and restored by the functions that use them.

In addition to taking advantage of a processor's registers, an optimizing compiler should be able to benefit from the processor's instruction set. For example, to reduce the overhead for looping, a common operation in DSP applications, the compiler takes advantage of the DSP32's single-cycle, low-overhead loop control instruction, which modifies a register and does a branch based on the result.

■ Higher level tools

While DSP compiler technology is improving, steady gains are being made in many other areas. In signal processing, vendors such as Sonitech (Wellesley, MA) are building upon AT&T's subroutine library to provide higher-level signal processing functions such as Burg Spectral Estimation (a technique that provides better frequency separa-

tion than fast Fourier transforms do in the presence of noise), two-dimensional Discrete Cosine and Fourier transforms, and Cepstrum.

In image-processing and graphics applications, vendors such as Causal Systems (Englewood, CA) are adding library functions that support coordinate transformations, the manipulation of wireframe images, Gouraud shading, Phong shading, and even ray tracing.

At an even higher level, vendors are providing menu-driven environments that let designers develop programs without writing a single line of either assembly or C code. Menu-driven DSP software from Burr-Brown (Tucson, AZ), for example, lets designers develop their application by configuring a functional block diagram using library functions such as correlation, signal sources, filters, windows and FFTs. Once designers have completed their block diagram and signal analysis, the DSP software will automatically generate a DSP32 assembly language program.

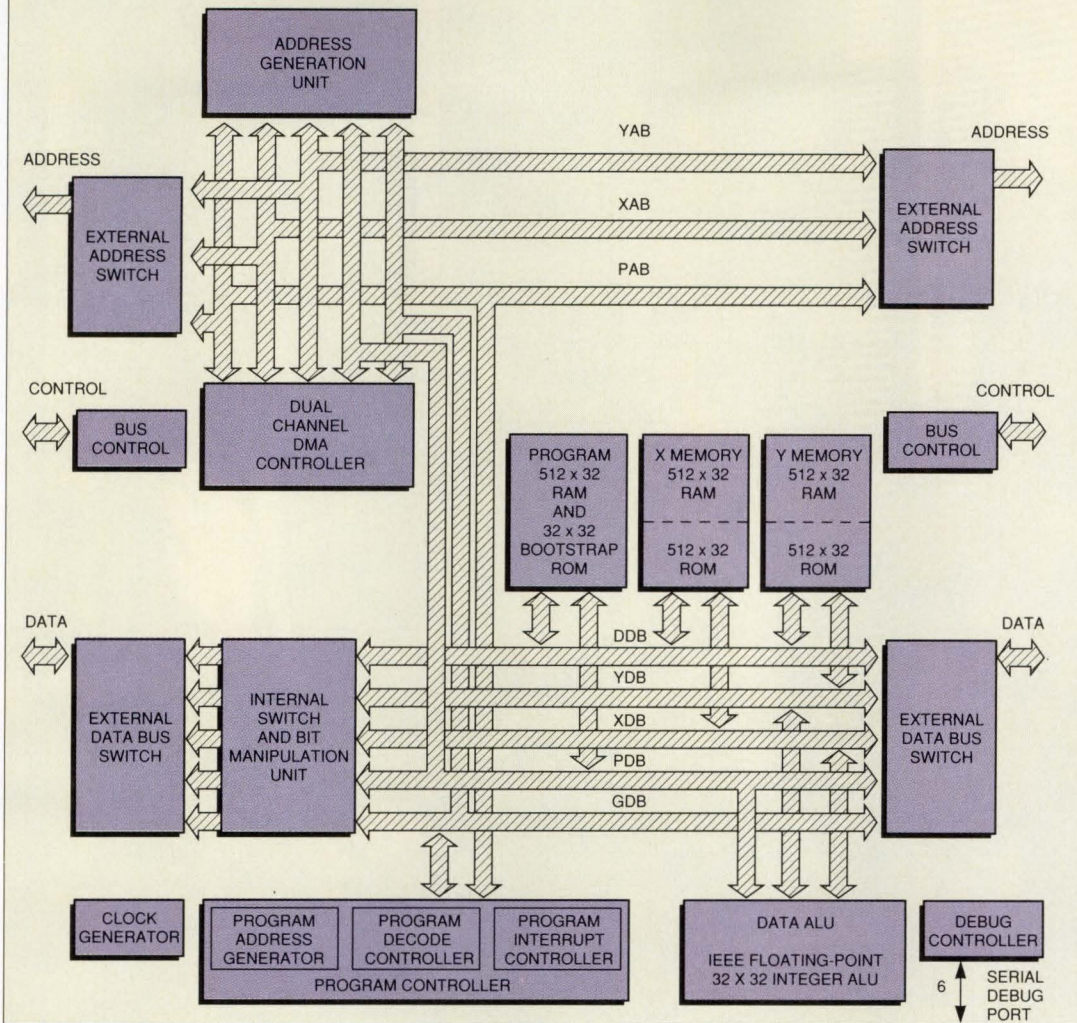
For Macintosh users, Spectral Innovations offers a package called MacDSP. Using the company's data-acquisition card, it can acquire data at up to 100 kHz, operate on that data using a variety of signal-processing functions, and display the results in real time.

To select a function, users simply click on the appropriate icon. In response, MacDSP immediately applies the function and displays the results in real time. The resulting data can be displayed using a variety of viewing modes including magnitude, phase, color spectrogram, or waterfall formats. By clicking on a different function, designers can change the type of function that they are applying (and its parameters) on the fly. By stringing MacDSP's icons together and editing customizable menus, designers can build a complete application without writing a single line of code.

With programming tools such as compilers, and application packages such as DSPplay and MacDSP, designers who have little knowledge of DSP hardware can interactively develop applications. This separation of hardware and application software will make DSPs widely accepted in mainstream computer applications.

Dave Trulli, technical product support engineer, AT&T Microelectronics

THE MOTOROLA 96002 ARCHITECTURE



Motorola's first entry into the floating-point DSP market will be its 32-bit 96002 device sporting dual buses. The 96002 has two independent bus ports that can be assigned to any of X, Y, or program memory spaces, effectively doubling off-chip bus bandwidth. The Motorola dual-bus approach represents one area in which DSP chips tend to mimic conventional microprocessors.

cently announced 80860 RISC processor (see "DSP and RISC merge in 80860," p 96).

And Cypress Semiconductor (San Jose, CA) is readying a version of the Sparc processor that will be dedicated to embedded control applications—many of which are the exclusive domain of DSP devices. And many DSP-like chores, such as laser-printer controllers, once considered to be jobs for DSP chips, are going to RISC processors.

■ The price/performance factor

With quantity prices ranging from \$150 to well over \$500, high-performance DSP chips (except for Fujitsu's 86220) haven't traditionally been priced as commodity items. Though these prices are expected to drop over the coming months, the anticipated volume will probably not accelerate them along the cost/volume curve as fast as more conven-

tional RISC processors.

The implication here is that while chips such as the 80860 start out with price tags in the \$740 range, these chip prices will probably drop faster than the price of other dedicated DSP devices. Zoran's 34325, for example, has an initial price of \$695, but the company claims that volume pricing will drop to the \$400 range within a few quarters.

Motorola's 96000 family will also start out as a pricey gambit, with samples running in the \$500 area. And while volume pricing is expected to significantly reduce that figure, it's not likely it will drop below the \$100 range anytime soon.

As DSP applications continue to emerge, we can expect to see the number of both standard and ASIC DSP solutions swell. And while the RISC "phenomena" sometimes looks like "more smoke than fire," architectures such as Intel's 80860 and

other RISC chips may provide cost-effective solutions to many signal-processing problems. □

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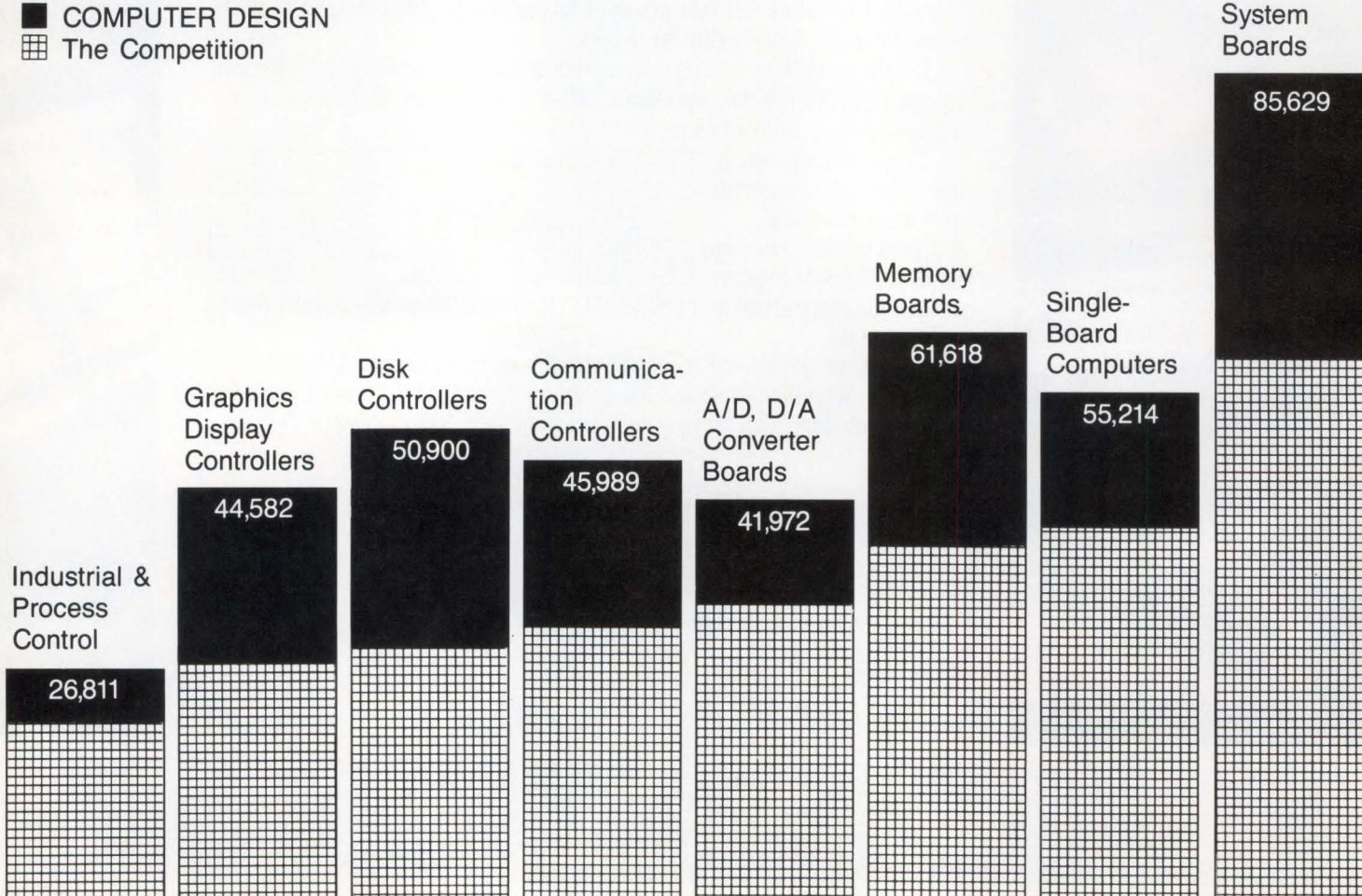
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CIRCLE NO. 46

Mixed-signal simulator eases system integration

System designers need an integrated simulator that can be used to quickly evaluate complex, mixed analog/digital VLSI chips without requiring analog expertise.

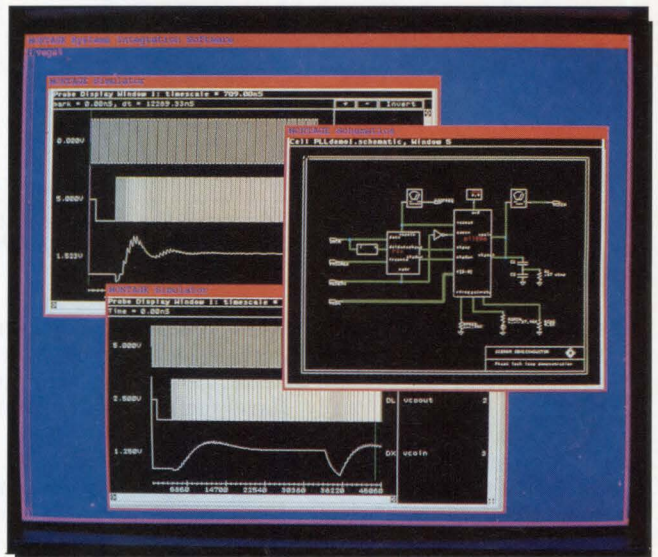
Tom Tormey, MSEE

The trend in system design has been to pack major portions of electronic systems into VLSI chips. To continue in this direction, designers need to be able to integrate a system's analog functions into those chips. But getting analog/digital ASICs to work the first time is difficult. For that task, designers need a simulator that quickly exercises the analog and digital portions together and provides sufficient analog/digital feedback. And because system designers are better versed in digital issues than in analog issues, the simulator shouldn't demand knowledge of IC-specific, transistor-level analog effects.

Digital simulators have played an important part in the success of semicustom ICs. But almost every system includes some analog circuitry—which digital simulators can't handle. The only alternatives have been tools for transistor-level analog experts to use for simulating relatively small analog subcircuits. Unfortunately, such tools simulate complex analog circuits far too slowly to be of much value to system designers.

Until recently, the analog portion of a mixed-signal ASIC had to be created by an analog IC expert. The system designer could then develop the digital portion of the chip using a digital simulator. Because no unified simulation environment existed, however, the resulting ASIC often failed to function correctly, usually due to problems at the analog/digital interface, where no simulation was performed. This lack of unified simulation environment has prevented mixed analog/digital ASICs from enjoying the same first-time success rate as pure digital ASICs.

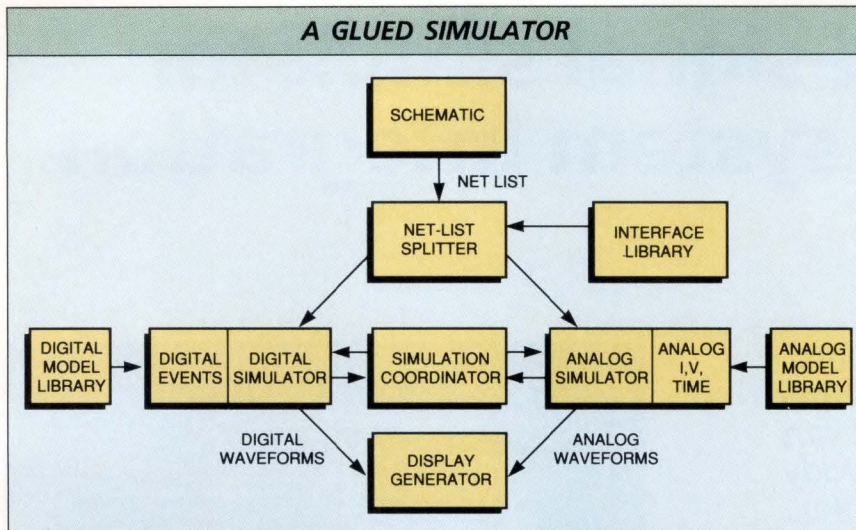
Most system designers have therefore avoided mixed analog/digital ASICs. As a consequence, systems include analog circuitry in discrete form, causing even fairly simple analog functions to take up a disproportionate amount of board space. Moreover, simulation can't check the way the analog circuitry interacts with the digital logic, thus postponing system testing until the prototype stage.



The ability to quickly simulate complex mixed analog/digital semicustom ICs will be key to the growth of system-level integration in the 1990s. To meet the needs of highly integrated system chips, Sierra Semiconductor's Montage uses an event-driven, behavioral-level approach. Montage performs and displays multiple simulations on universal hardware platforms.

Tom Tormey is the director for semicustom products at Sierra Semiconductor (San Jose, CA).

MIXED-SIGNAL SIMULATOR



The glued approach to simulating analog and digital components together involves running separate analog and digital simulators concurrently and then feeding each simulator's results to the other.

Traditional analog simulators aren't known for their speed. To create and simulate semicustom analog ICs, system designers really have had only one option: Spice. Developed more than a decade ago by the University of California at Berkeley, Spice and its permutations have spread through the industry. In fact, most commercially available analog simulators on the market today are based on, or are derivatives of, the Berkeley simulator.

For analog IC experts who want to simulate circuits that have up to several hundred transistors, Spice is an ideal simulation tool. But for system designers, who generally don't have analog IC transistor-level experience, Spice presents major limitations.

Spice's most basic limitation is speed. For a reasonably complex analog circuit, such as a 10-bit analog-to-digital converter, Spice is inappropriate for simulating the circuit's overall function. To simulate just one conversion on a 10-bit converter at the transistor level, Spice takes about 24 hours of workstation time. This simulation supplies all the details that an IC designer might want for fine tuning the converter, but the simulation is worthless for dealing with the converter as a system-level component.

In an attempt to improve the speed with which Spice tackles the large design problem, Spice supporters have used high-speed computer systems, often with sophisticated co-processing boards. Although the efforts have yielded modest perfor-

mance gains, the limited success hasn't produced a simulator that can effectively simulate large analog or mixed analog/digital systems.

Spice's speed limitations stem largely from its transistor-oriented approach. Simulating the operation of every transistor and passive component in a circuit naturally takes a great deal of time. In addition, Spice produces far more detail for each analog waveform generated than an analog/digital simulation generally requires. This is especially true where an analog component drives a digital one; even though the digital component cares about only its switching threshold, Spice generates every part of the analog waveform in equal detail.

Also important in creating a mixed analog/digital simulator is the need to avoid a requirement for specialized analog knowledge. This challenge reveals another Spice limitation: Spice demands that users have extensive knowledge of the analog parameters involved.

Designers working on the analog transistor level certainly must have such knowledge to create a circuit such as a 10-bit converter. But when simulating the converter as one component among tens of analog and thousands of digital functions, system designers shouldn't have to concern themselves with transistor-level details such as the biasing of the transistors in an operational amplifier. Rather, system designers should concern themselves with the point at which that amplifier begins clipping or when its common-mode

input range has been exceeded.

But after dealing with the speed requirement and working around the digital designer's lack of extensive analog knowledge, the designer must get the analog and digital functions to interact. This challenge would be easy to overcome if one simulator were used for both types of functions. With traditional simulators, this would mean using an analog simulator, which could handle the digital logic by treating it as analog functions at the transistor level. But this approach would merely inflict Spice's analog speed limitations on the digital logic.

Glued simulators limit success

The approach usually taken to simulate analog and digital components together is to run separate analog and digital simulators concurrently and feed each simulator's results to the other. This glued-simulator approach creates a variety of problems. The two most basic problems are preparing the separate net lists for the two simulators and coordinating the simulators' results so that each can drive the other.

Splitting the net list for the glued simulators can require a great deal of manual work from the user. Even when the separation process is more or less automatic, users pay penalties in extra net-list generation time or simulation start-up time.

In addition to splitting the net lists, interface elements must be inserted at every point where digital meets analog. A phase-locked loop circuit, for example, might require interface elements between the phase detector and the frequency generator.

An interface element translates output signals so that they're meaningful for the component receiving them. More precisely, an interface element converts signals so that the appropriate simulator can handle them.

In the case of a phase-locked loop circuit, for instance, the analog simulator generates the frequency generator's output as an analog waveform. This waveform can't drive the digital simulator directly. An interface element is required to convert the analog waveform to an appropriate digital representation. Similarly, an interface element must convert the phase detector's simulated digital output to a representation that will drive the analog model of the frequency generator.

Fine tuning the phase-locked loop

While a phase-locked loop circuit can present problems for a glued simulator, the single-simulator approach can handle this type of design. In developing an ASIC containing the PLL, for example, the designer would assign values to the resistors and capacitors that control the loop's operation. These values theoretically set the PLL to handle the frequencies with which the PLL must synchronize. In simulation, the designer can make sure that the PLL synchronizes as anticipated.

One resistor, Rcharge, is especially important because it controls the current on the loop filter charge pump, and thus determines the speed with which the voltage-controlled oscillator (VCO) responds to phase changes. With

Rcharge set at 0.55 M Ω , the PLL synchronizes slowly; the VCO input appears to be underdamped and oscillates around its final value.

To achieve critical damping, so that the PLL synchronizes faster, the designer changes Rcharge to 2.2 M Ω . When the simulation is rerun, the PLL synchronizes much more quickly.

Because the single simulator can simulate the PLL in seconds, the designer gets immediate information on how well the circuit is working. In a few minutes, the designer can try several resistor and capacitor combinations to make sure the PLL achieves the best possible performance. The same approach works with a complex ASIC, of which the PLL might be only a small part.

After the separate net lists are prepared with their interface elements, the glued simulators must be run in a coordinated way. This is difficult because Spice wasn't designed to work with another simulator. The fundamental coordination problem is that Spice has its time base, and the digital simulator has its own separate time base.

When the frequency generator drives the phase detector, the interface element at the frequency generator's output waits for a signal event to occur. When an event occurs within the analog simulator's time frame, the simulation coordinator must look back in the digital time frame to make sure that the digital simulator hasn't run too far ahead of the analog simulator on false information. Sometimes the digital simulation must be reset to an earlier time step and rerun with correct information. Such back-and-forth comparisons must be made for most time steps and for every point where analog and digital meet.

Coordinating the glued simulators thus slows the simulation process further, adding to slowdowns due to dealing with analog circuits at the transistor level. When the ASIC is finally simulated, the analog and digital results—each in the format of its simulator—must be merged and displayed in a common time frame.

■ Coordinating analog and digital

As an alternative to the glued simulators, a single simulator can be

used to handle both analog and digital component models. This approach has several advantages. It doesn't require separate analog and digital net lists, for example, and the analog and digital components are always in synchronization because there's only one time base. The first mixed analog/digital simulator to use this architecture is the Montage simulator from Sierra Semiconductor (see "Simulator expedites mixed-signal IC development," p 106).

In addition to the inherent advantages of the single-simulator architecture, the simulator makes it possible to handle analog responses in a way that's particularly useful for mixed analog/digital simulation. Using behavioral, rather than transistor-level, modeling results in a massive speedup, for example. The behavioral modeling shields design-

ers from transistor-level effects; it also provides detailed error messages when an ASIC cell is used in a way that violates its data sheet specifications.

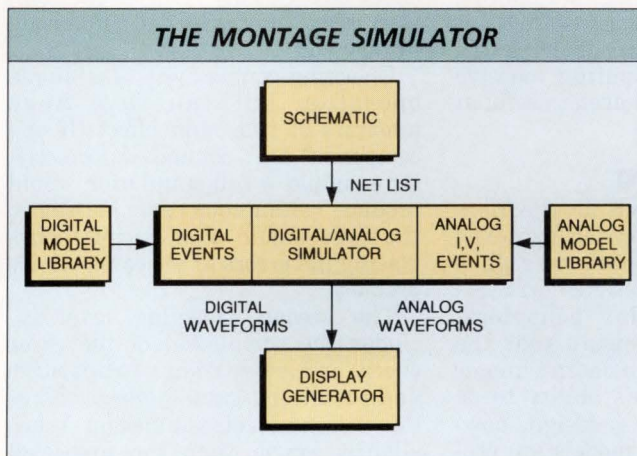
Another advantage of behavioral modeling is that each component can generate either analog or digital outputs. Each component therefore produces an output suitable for the components it feeds. A comparator model, for example, receives analog signals on its inputs and generates digital signals for its output, thus eliminating the need for interface elements.

■ A distributed time base

The use of a single simulator simplifies timing issues because only one time base is needed. A further refinement is to have the component models adjust their response to suit other components. In an ASIC where an operational amplifier feeds an A-D converter, for instance, the A-D converter knows its reference voltage and its resolution (say, 8 bits). The A-D converter therefore knows its accuracy is $\frac{1}{2}$ least significant bit (LSB) and tells the op amp to feed changes only when they're $\frac{1}{2}$ LSB or greater.

When the op amp doesn't have this much change to report, it reports nothing, thus saving the computations that would be needed if the A-D converter had to determine that a change wasn't significant. With the component models adjusting their outputs in this manner, it's as though there are time-step controllers everywhere in the schematic.

There are a number of effects that the component models have to account for in adjusting their outputs. On a node connecting several components, for example, the component



Sierra's Montage mixed-signal simulator is a single-simulator, event-driven engine that handles both analog and digital components using behavioral-level standard-cell ASIC models.

Simulator expedites mixed-signal IC development

For designers who need to quickly evaluate "what if" trade-offs on highly complex, mixed analog/digital VLSI chips, Sierra Semiconductor offers a complete design environment called Montage. The simulator underlying the Montage environment is Lsim from Silicon Compiler Systems (San Jose, CA). Lsim serves as a strong basis for a mixed analog/digital ASIC simulator because it was designed to handle both digital and analog component representations. To develop the Montage simulator, Sierra added its proprietary analog simulation algorithm and sophisticated models to Lsim.

The Montage simulator is significantly faster than previous simulators. While Spice took 24 hr to simulate one conversion of a 10-bit analog-to-digital converter, for example, the Montage simulator required only 10 s to simulate the converter's entire operation cycle—a 1,000-to-1 speed advantage. Users of conventional simulators will also appreciate the fast connection between the Montage schematic capture facility and the simulator. These speed advantages let system designers extensively analyze trade-offs to quickly fine tune complex analog/digital ASICs.

In addition to a schematic capture facility and the simulator, Montage includes a circuit screener. This expert-system software checks for errors that a simulator can't find. Other Montage features include a user environment shell that shields users from the operating system; a back-annotation tool that inserts physical layout information into simulations; software installation tools; and design transfer tools.

The Montage analog/digital simulator is descended from an earlier mixed-mode simulator that Sierra used within the company. Sierra designers exercised and proved some of the fundamental concepts behind the Montage simulator for more than two years. Sierra extensively enhanced the earlier system to create the Montage simulator, which runs on Sun workstations.

Montage also has complete libraries of Sierra's 1.5-micron Triple Technology analog, digital and EEPROM component cells. These cells include 245 digital cells, 23 analog cells such as 65-MHz phase-locked loops and 10-bit data converters, and nine EEPROM cells. Sierra doesn't restrict other vendors from porting their libraries to the Montage environment.

pass, users can save time by using the first-level simulation to resolve as many basic errors as possible.

Once satisfied with the results from the first two passes, the designer is ready to implement the final modeling level, which adds analog uncertainty. Analog uncertainty is the equivalent of the digital "unknown" state for mixed analog/digital simulation. More specifically, analog uncertainty provides a way to deal with the analog behavior of a function whose digital controlling inputs go into an unknown state. In addition, analog uncertainty provides some measure of worst-case analysis with respect to min/max data-sheet parameters.

The Montage simulator reports analog uncertainty as a plus/minus error term known as the signal's uncertainty value. An analog signal whose value is known has an uncertainty value of zero. On the other hand, an analog signal whose value is completely unknown has an uncertainty value equal to the signal's nominal value: $2.5 \text{ V} \pm 2.5 \text{ V}$, for example.

Because the models encompass many sophisticated capabilities, creating them is a complex process that requires expertise in understanding cells and the way the cells might be applied. Once the behavioral models have been created, however, the system designer needs no IC design expertise to apply them.

Developing a useful analog/digital simulator and model libraries requires several years of work and careful consideration of system designers' needs. Now that the tools are available, they promise to open up extensive new space and cost savings for complex analog/digital systems. Just as all-digital semicustom chips have moved systems to higher density levels, the ability to integrate analog components in a reliable way will again revolutionize system design. □

that needs updating most often is the one that determines the update rate for the entire node. And because the state of components such as capacitors changes continuously over time, the simulator must compute their response regardless of whether they receive input updates. Users can also set any node's update rate manually.

This event-driven approach is unique among analog simulators. The approach provides significant time savings because it frees the simulator from computing massive amounts of data that aren't useful at the system level.

■ **Multilevel modeling**

The component models for the Montage simulator's approach to mixed analog/digital simulation are sophisticated, furnishing detailed error reporting and complex behavioral characteristics. To ensure that the models' sophistication doesn't impair the system engineer's ability to do an initial debug of a design, however, three levels of models are pro-

vided. The levels start with a basic functional model and progress to a full-featured simulation model when appropriate.

At the first level of modeling, the simulator checks basic functional issues and connectivity. The basic functional check that's done at this stage verifies that the user has applied the analog components within their specified ranges, an important check that quickly resolves the common error of specifying the wrong library cell.

Checking connectivity is a simple operation but can save huge amounts of time and effort. If one component isn't connected correctly, for example, a full simulation would produce voluminous error messages; the user would then spend hours tracing the errors to the connectivity problem.

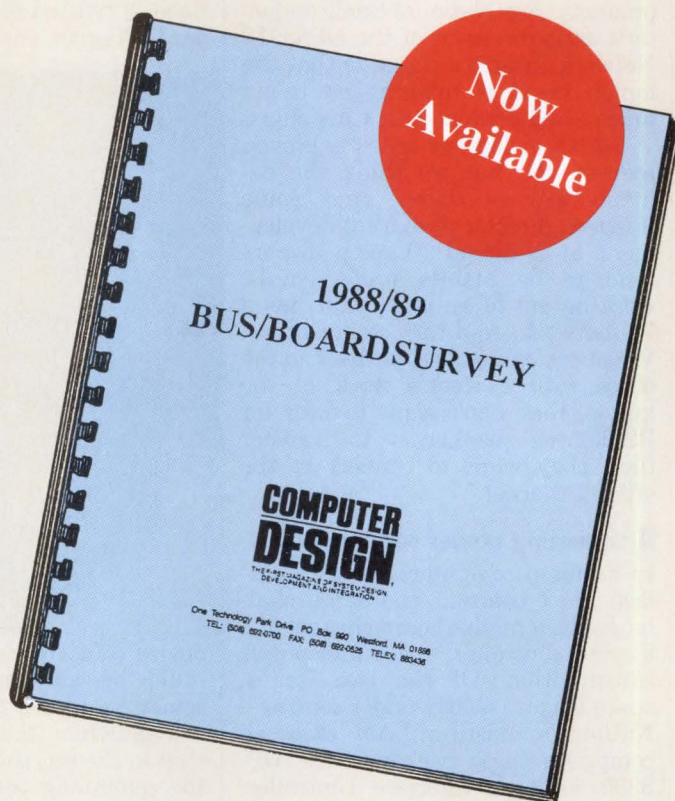
The second modeling level includes the completion of the error check and evaluation of capacitive and remaining timing effects. Since this second-level simulation takes slightly longer than the first-level

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INTEGRATED CIRCUITS

National shrinks power needs for LAN interfaces in laptop applications

The projected huge growth in laptop computer sales has caught the attention of CPU, motherboard chip set and disk controller vendors. Designers of these chips are increasing integration, reducing power consumption and implementing power-saving sleep modes for their products. But National Semiconductor's announcement of the DP83910 Network Interface suggests that the laptop trend is catching on in an unexpected product line: LAN chips.

"LANs in laptops aren't a proven market yet, but we think the demand will be there," says Anne Wagner, director of market development at National. "Laptop owners tend to be mobile professionals, working out of an office that has a PC network. And they're impatient. When professionals come back to the office with a week's work in the laptop, they don't want to wait for RS-232 or sneakernet to transfer files: they want to connect to the office Ethernet."

Squeezing power consumption

In a laptop computer, a LAN interface must confront the same challenges as a motherboard chip set of a display controller: space and power consumption. Of the two issues, space is more nearly under control—National's existing LAN chip set comprises three packages: the DP-8390 network interface controller, the DP8391 network interface and the DP8392 coaxial transceiver. But each of these packages has an appetite for current that works against battery life in the laptop environment. So National set out to lower the power requirements of the complete interface.

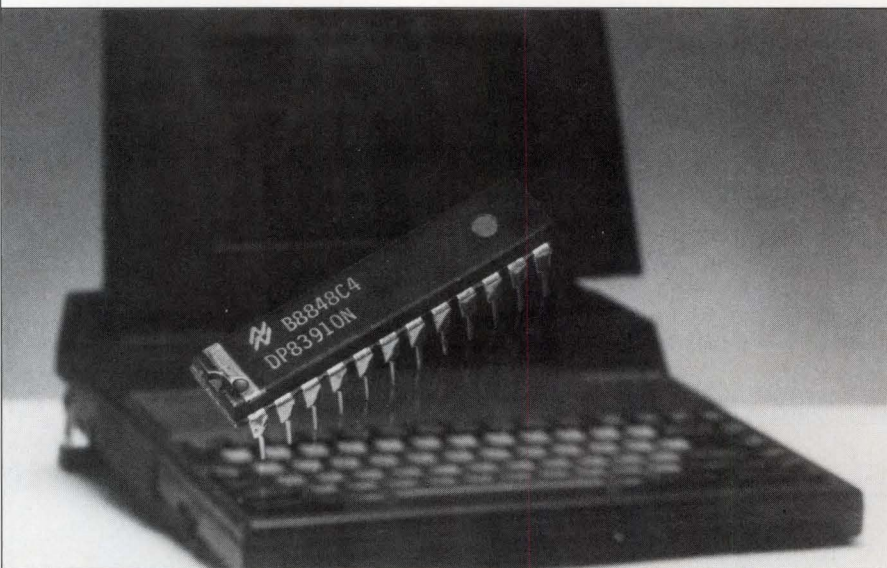
The interface microcontroller has been the easiest piece of the power-conservation puzzle. Since it handles the data in parallel, 1-Mbyte/s format, the controller can be fabricated in moderate-speed CMOS without risking lost messages. The DP8390 controller draws only 40 mA.

At the opposite end of the chain, the Ethernet transceiver is constrained by speed and signal requirements. Wagner believes that only bipolar circuits can comply with Eth-

ernet requirements for 10 Base 5 or 10 Base 2 networks for the foreseeable future. "Consequently, the power consumption of the transceiver is fairly high—about 180 mA," she says. When relief comes, it will probably be in the form of a transceiver adapted specifically for the new 10 Base T twisted-pair Ethernet standard. Wagner suggests that such a

replacing the 8391's digital phase-locked loop with an analog one, the company has significantly reduced the power consumption of the part. The new CMOS device, the DP-83910, dissipates only 70 mA.

Running at 10 MHz, the part is a direct replacement for the bipolar 8391. As such, the new device can be used in interfaces to 10 Base 5, 10 Base 2, or new 10 Base T LANs, in conjunction with the 8390 controller and the appropriate transceiver chip. The combined offering gives



device could be done in CMOS and could be announced by National sometime in the near future.

Meanwhile, that leaves the third chip in the set, the data interface, as the remaining possible site for saving power. This chip takes the analog signal coming off the transceiver, extracts data from it and runs the data through Manchester decoding and serial-to-parallel conversion to produce bytes for the microcontroller. (The sequence is reversed when the interface is transmitting, of course.) In the past, the high data rate and the requirement for a precise phase-locked loop and complicated codec state machine led vendors to implement the part in bipolar silicon. In fact, National's existing DP8391 is bipolar.

Revising the interface chip

But National has made a significant step forward in the battle against milliamps. By reimplementing the 8391 in CMOS, and in the process

National a unique approach to meeting the power constraints of forthcoming laptop designs.

Available now in 24-pin dual in-line packages or 28-pin plastic leaded chip carriers, the DP83910 sells for \$19.50 and \$20.75, respectively, in 100-piece quantities. —Ron Wilson

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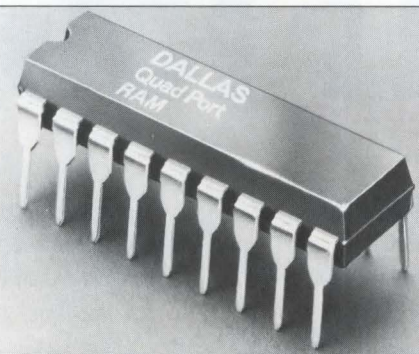
Quad Port message center loosely couples small groups of CPUs

The task of loosely coupling a small number of CPUs can appear deceptively simple. Many of the obvious solutions, such as shared parallel buses, point-to-point wiring, tagged first-in, first-out registers or multi-master serial buses, can run into problems by being either too expensive or too slow. Now Dallas Semiconductor has developed an innovative single-chip approach, dubbed the Quad Port, that could be just the answer for most small message-passing multiprocessor systems.

The company's idea is based on fast three-wire serial connections, instead of a much more expensive parallel bus. Using speeds up to 4 MHz, the buses can get a sizable message between processors quite quickly. The Quad Port runs the

serial buses from each of the CPUs into a central message center. This four-port device provides contention-free connection from any CPU to any set of other CPUs, through a set of data registers and some flag logic.

"Each of the four ports contains an 8-byte block of data registers," ex-



plains Matt Adams, design engineer at Dallas. "Only computer A can write into block A, but any computer can read the data from block A." To prevent contention problems, the data registers use a Dallas-created five-port static RAM cell: each bit cell has a write-port and four independent read-ports.

A set of flags synchronizes the flow of data. Each port on the chip has a single flag byte that manages handshaking. When a message comes into Port A destined for Port B, for example, two flags change. A message-sent flag will be set in Port A, and a message-waiting flag will be set in port B.

In each case there are four flags, so the bit position of the set flag indicates the destination or source, respectively, of the message. When the device connected to Port B reads the message out of Port A's data register, both flags are cleared. In addition to the 8 data bytes in each block, there's a ninth byte that acts as a data integrity check.

A 3-byte protocol

The CPUs deliver messages to and pick up messages from the chip by means of a 3-byte command protocol. The first byte, sent from the CPU to the chip, contains the port address. The second byte, which goes from the chip to the CPU, contains the port flag byte. The third byte, sent from the CPU to the chip, is a command. After the third byte, the string of from 1 bit to 8 bytes of data moves in the appropriate direction.

Since the three-wire buses are externally clocked, all these bits can be completely asynchronous. When the chip is transferring data, it moves a bit on the data wire for each clock on the clock wire, until either all 8 bytes have moved or the enable wire goes inactive. Either cause will end the transfer.

The Quad Port Memory comes in either an 18-pin dual in-line package or a surface-mount package. Now available, it's priced at \$6.25 in 100-piece lots. —Ron Wilson

Dallas Semiconductor

4350 Beltwood Pkwy S
Dallas, TX 75244
(214) 450-0400

Circle number 100

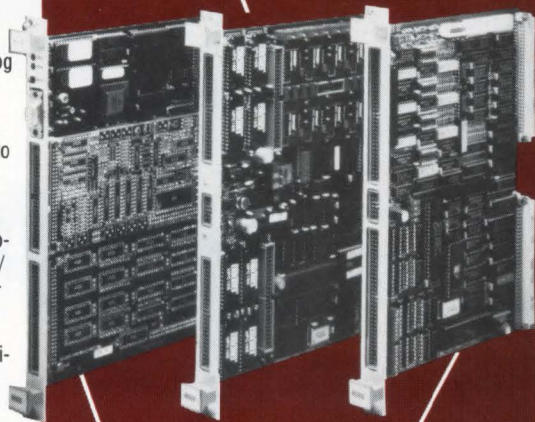
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MPV940 10 MHz 68000 CPU Controller board can be fitted with two Burr-Brown analog or digital multichannel I/O modules and still occupy one VMEbus slot.



MPV941 Analog I/O expansion board provides 128 input channels & 8 output channels.

MPV942 Digital I/O expansion board provides 32 I/O lines plus 32 input lines with change of state monitor.

CIRCLE NO. 49

"Fuzzy" logic processor speeds embedded AI control applications

A new VLSI coprocessor for embedded control applications can make decisions based on "fuzzy sets"—data that represents a degree of certainty about a problem rather than a binary yes/no decision. The FC110 digital fuzzy processor by Togai Infralogic can support up to 128 kbytes of ROM/EPROM as knowledge-base memory.

A knowledge base contains data representing expert knowledge about a subject and rules for making decisions based on that data. The FC110 can handle rules for decision making that contain variable numbers of I/O parameters. All inputs to a rule are evaluated together to produce a degree of certainty about results.

To date, practical artificial intelligence (AI) systems have been mostly software-only systems built on conventional processor architectures and deemed too expensive or too slow for widespread use in embedded control applications. In addition, rules-oriented knowledge-base systems on which AI applications depend need a systematic approach to managing uncertainty—of making decisions based on imprecise or incomplete information. Fuzzy logic assigns a value between 0 and 1 to represent a "degree of belief" about a given premise, rather than treating uncertainty as a random true or false probability.

The concept that a person is "young"—an imprecise term—would have a high degree of certainty if that person's age were 0 years, for example. The certainty of "youthfulness" diminishes with increasing age to a point where 25 years, for example, might be considered no longer young in the context of the problem. An AI rule about youth might also contain other considerations, such as "young in what sense?" The fuzzy processor must evaluate combinations of possibilities to come up with an approximate answer.

The FC110 uses a reduced instruction set with a twist—a small set of complex instructions. One very important instruction evaluates the "left hand side," or the IF side, of an

AI rule. Another instruction evaluates the "right hand," or THEN, side. Knowledge-base rules can have varying numbers of IF and THEN parameters that the processor evaluates as a whole. Every parameter impacts the result value in some way, depending on how the rule is written. Running at 10 MHz, the FC110 can perform 28,600 fuzzy logical inferences/s. This amounts to about 200,000 rule evaluations/s.

■ A coprocessor role

In most applications, the FC110 will be used in the role of a coprocessor to a general-purpose host. The host would take care of polling sensors and converting the data into the format used by the FC110.

The host would then download the data to the FC110 and send a message for it to initiate inferencing—making decisions about the input based on the rules stored in the knowledge base. The resulting output would then be sent back to the host for conversion and transmission to the system's output devices, such as servo motors on a robot arm.

Applications for the FC110 are developed using Togai's Fuzzy-C compiler. With the compiler, programmers can write and debug applications and develop knowledge bases with their rules on a PC, as well as integrate these knowledge bases into existing C applications.

In addition to the compiler and the FC110 chip, Togai will supply a PC AT evaluation board for developing applications for host-based systems.

The FC110 is priced at \$80 in quantities of 1,000. The AT processor board with the assembler is priced at \$3,499. The Fuzzy-C compiler costs \$4,950 for PCs and compatibles, and a version for Sun Apollo and Sony workstations is available for \$9,900. The FC110, AT board and assembler will be available in August. The Fuzzy-C compiler is available now. —Tom Williams

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Circle number 102

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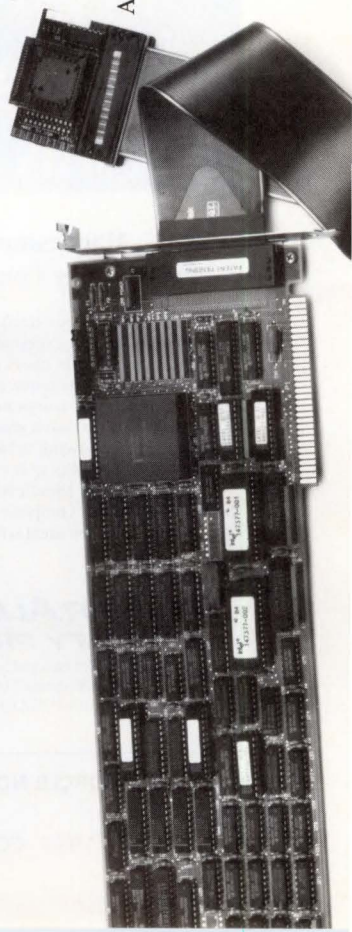
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CIRCLE NO. 50



Magnetics library, Monte Carlo analysis expand analog simulator's capabilities

The Saber simulator from Analogy is an analog simulator with built-in digital simulation capability. Like any analog or digital simulator, Saber may be tailored to certain applications through its model libraries. Analogy is expanding Saber's capabilities with a recently introduced magnetics library that moves Saber into the power supply design arena. The company is also adding a statistical modeling and Monte Carlo analysis capability that helps predict manufacturing yields.

The power supply design package includes magnetics models, pulse-width modulators, cores, transformers, power MOS devices and digital switches—all the components necessary to simulate power supply designs. Analogy gains significant

speed advantages by using Saber's mixed-mode simulation capability to provide digital models of certain parts in its power supply design library.

Certain transistors in a power supply, for example, never operate in their linear range but are always driven to saturation; thus, they function as switches rather than as amplifiers. Using event-driven digital models for such devices provides a speed advantage of up to 35 times over simulations using analog transistor models.

Once the basic structure of a power supply design is determined, the user can change to analog MOS device models rather than digital models for final simulation to determine the exact performance of each element in the design.

Magnetics models

In power supply design, magnetic elements take up significant physical space and weight, making their design particularly important. One technique for developing magnetics models is to calculate selected points on a curve and then create a curve to fit the points. This technique is accurate for only one frequency and one temperature.

Saber provides highly accurate nonlinear magnetics models by basing its models on the solutions of physical equations. The models are accurate over a wide range of frequencies and temperatures and support integrated magnetics (multiple windings on one core).

In addition to magnetics and digital switches, the power supply library contains about 20 pulse-width modulator models (1524, 494, 1825 families) that are written in Saber's behavioral modeling language so they can be reconfigured easily to meet new needs.

The other added capability, Monte Carlo analysis of an analog design, helps determine potential manufacturing yields based on a standard distribution of parts used in the manufacturing process. Monte Carlo analysis simulates a design using a random selection of parts that fit the manufacturer's specifications, and

the results are plotted to see how many combinations fall within acceptable operating ranges and how many fall outside that range. The percentage that falls within acceptable bounds is the predicted manufacturing yield.

Monte Carlo analysis accuracy depends on the accuracy of the statistical models used in the simulations. In the Saber statistical modeling package, Analogy considered deviations in the statistical distribution of parts, and the correlation of parameters that may vary in a part.

Statistical distribution

One way to develop statistical distribution models is to use minimum/typical/maximum values. While this technique is acceptable for some parts, others don't necessarily follow the model. Resistors, for example, are often tested to select those that meet a particular set of specifications. A batch of 10 percent resistors will generally fall in the -10 to -5 percent range and the +5 to +10 percent range, with no parts falling in the -5 to +5 percent range.

Resistors that fell in the ± 5 percent range are sold as 5 percent resistors, leaving a gap in the ranges of 10 percent parts that could be used in manufacturing. Using a "typical" resistor value (no deviation from the nominal value) produces overly optimistic results.

The addition of probability distributions of parameter values addresses this problem and lets Saber's Monte Carlo analysis take on statistically meaningful values by providing interparameter correlations. A standard library of probability distribution functions (PDFs) is provided with the Monte Carlo and statistical modeling packages, or users can specify their own PDFs.

The power supply design package is available as an add-on to the Saber simulator. The package costs \$3,600 for a one-year subscription. The Monte Carlo package is also available, and is priced at \$5,000 to \$10,000 on workstation platforms.

—Bill Harding



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CIRCLE NO. 51

Analogy

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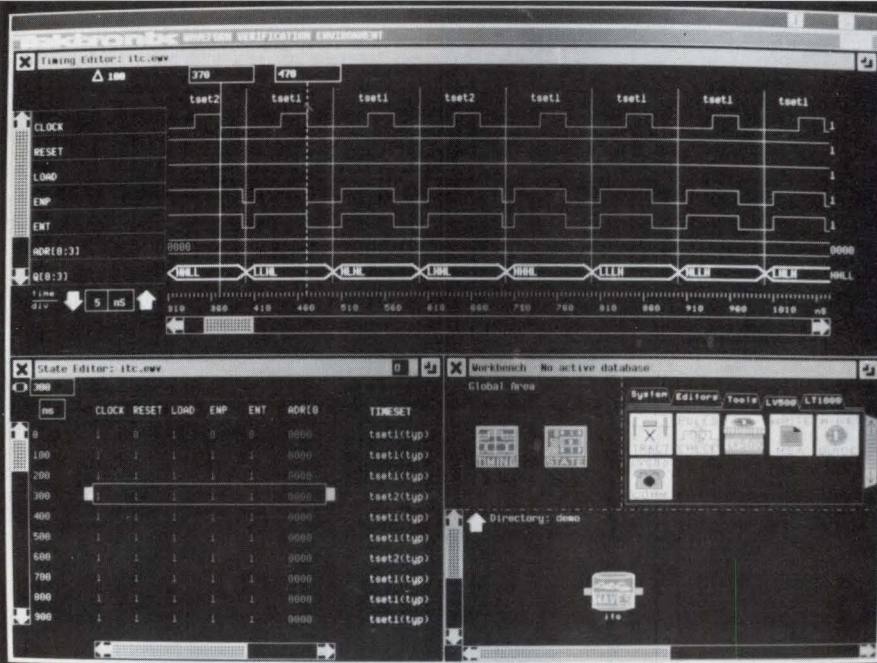
Circle number 103

Testing package helps designers develop ASIC verification programs

Tekwaves, a new test program generation package from Tektronix, is based on the idea that many ASIC designers must develop test programs for their prototype designs. Tekwaves (for Tektronix Waveform Analysis and Verification Environment) is one part of a two-pronged ASIC prototype verification solution.

can develop tests for the LV 500 without being very familiar with it. Utilities such as the tester rules checker ensure that the test vectors will be compatible with the LV 500.

A Tekwaves on-screen card file identifies major categories such as editors, files, translators and testers (the LV 500). Each card contains



The other part is the previously introduced LV 500 ASIC verification tool, a 256-pin benchtop tester for use in a design lab. Tekwaves helps designers develop ASIC test programs to run on the LV 500.

While a designer may develop test programs from scratch using Tekwaves, it's more efficient to use simulation vectors developed during the design cycle. Tekwaves supports input from most popular simulators.

Tekwaves includes bidirectional links to logic simulators, so vectors can be imported to Tekwaves, or Tekwaves can develop vectors and export them to simulators. A graphical stimulus creating and editing capability is used to edit simulator-developed vectors, or to generate vectors from scratch.

Because tester-specific knowledge is built into Tekwaves, a designer

associated tools and files. By assembling cards in an on-screen work area, the user identifies the processes and files to be used.

Once the user determines the functions that must be performed to create a test program, Tekwaves automatically creates the test program, executes the program development functions, and puts the test program in the format required by LV 500. The output of the automatic test generation phase is typically a test fixture wiring diagram and a test program for the LV 500.

The base price for Tekwaves is \$5,000.

—Bill Harding

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Circle number 104



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- DSP56001 System Board \$3,495
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- ADSP-2100 System Board \$2,595
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CIRCLE NO. 52

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COMPUTERS AND SUBSYSTEMS

Programmable serial I/O controller targets Micro Channel systems

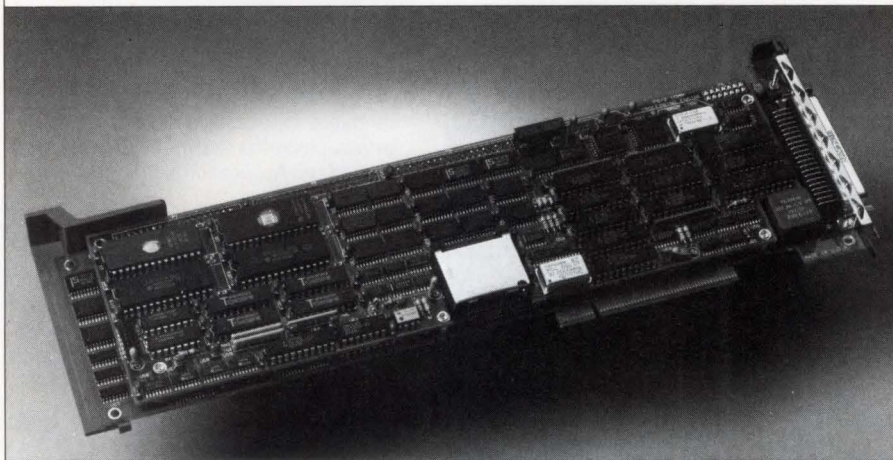
The PScomm2/4 from Metacomp is an intelligent serial I/O controller designed for use with the IBM PS/2 Models 50, 60, 70, 80 and compati-

bles. Built around an 80C186 16-bit microprocessor running at 16 MHz, the board offers two (or optionally four) programmable communica-

tions channels supported by full duplex direct memory access (DMA) circuitry. Two channels can operate at full duplex with a data rate of up to 2.48 Mbits/s.

The microprocessor on the board provides programmable intelligence to offload link-level and other high-level data communications processing from the PS/2 host, relieving the CPU of the overhead normally associated with complex data communications protocols such as Bisync, SNA and X.25.

Four EPROM sockets allow a maximum of 512 kbytes of nonvolatile storage. Two of the EPROM sockets may be configured for 256 kbytes of EEPROM or static RAM. In addition, the PScomm2/4 has 512 kbytes of parity-protected dynamic RAM that's triported between the on-board processor, the local DMA communications controllers and the Micro Channel. Serial DMA may be



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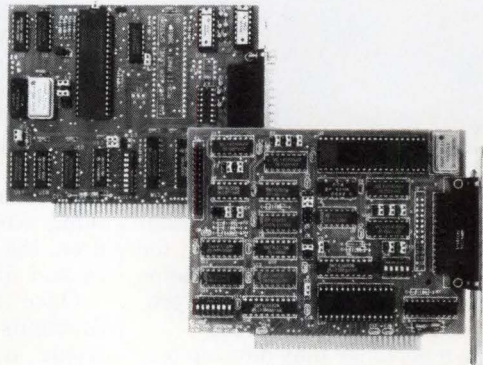
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CIRCLE NO. 53

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CIRCLE NO. 54

located anywhere in the DRAM. Eight light-emitting diodes indicate diagnostic and software status.

The triported RAM is available for sending and receiving data and messages between the PS/2 host processor and the on-board 80C186. Communication between the host processor and the local processor is implemented by the shared memory and a 16- \times 4-bit first-in, first-out (FIFO) mechanism. The FIFO lets both the host processor and the local processor interrupt and notify the other of pending messages or data located in the shared RAM.

In a typical application, the PS/2 host communicates with the serial channels by first placing the data into the triported RAM, and then writing information to the FIFO, thus notifying the on-board processor of a pending message.

Under system control, the PScomm2/4 can act as a bus master or a slave resource. The master mode supports physical addressing and implements DMA arbitration of the Micro Channel. Data transfers between the host processor and the controller can be by the DMA resource resident in the controller or in the host processor.

The 85C30 serial communications controllers on the board may be programmed to operate in polled, interrupt and DMA modes. Each 85C30 device contains two independent transmitters and two receivers that are programmable for async, bisync or bitsync protocols.

The PScomm2/4 contains all the necessary circuitry to support most popular electrical and mechanical interface standards without the need for add-on modules or additional Micro Channel slots.

Metacomp's data communications software and firmware solutions for the PScomm2/4 include standard protocol packages such as X.25, debug and development toolkits, and a real-time executive package.

Single-unit pricing is \$1,495 for the four-channel version of the board and \$1,395 for the two-channel model.

—Mike Donlin

Metacomp

15175 Innovation Dr
San Diego, CA 92128
(619) 673-0800

Circle number 108

Powerful MS-DOS CPU rides 8- or 16-bit STD Bus

The Model 8850 from Systek is a densely integrated CPU board that runs MS-DOS applications and functions with both standard 8-bit STD Bus boards and extended 16-bit cards. Built around an 8- or 10-MHz 80186-compatible NEC V50 CMOS microprocessor, the board has 512 kbytes of dynamic RAM, 256 kbytes of EPROM and 128 kbytes of battery-backed SRAM. Specifically targeted at real-time multiprocessing control applications, the board features a multimaster bus interface and supports both serial and parallel arbitration on the STD Bus.

"A high level of integration is important in a multimaster computer system," says Tom Seim, Systek president, "because it minimizes the use of the bus for routine peripheral I/O. More of the bus bandwidth can be devoted to interprocessor communication and control.

"A multiprocessing capability makes MS-DOS a viable contender for real-time control applications. One processor, for example, can be dedicated to the MS-DOS interface, performing disk and operator I/O, while other processors are responsible for real-time I/O functions. This eliminates concerns over worst-case

interrupt latency," says Seim.

A proprietary MS-DOS ROM basic I/O system is available for the board and includes extensive RAM and ROM disk utilities for embedded control systems that don't use floppy or hard disk peripherals. The board includes a pair of RS-232 serial ports mapped to match COM1 and COM2 ports of PC-compatible computers, an RS-422/449 serial port and a parallel printer port. An 8080 emulation mode is provided, letting existing applications easily migrate to a more powerful platform.

Transfers between the Model 8850 and other extended 16-bit STD boards occur at the full data width. To maintain compatibility with existing STD boards, the Model 8850 converts all word transfer to 8-bit boards into double-byte transfers.

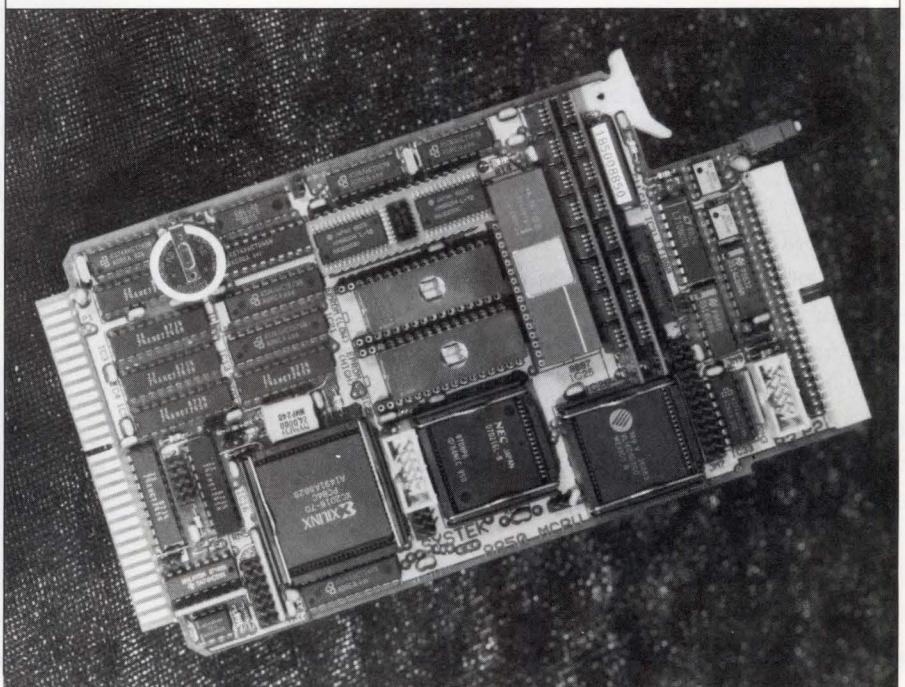
Documentation for the Model 8850 includes a comprehensive user's manual with sample startup and peripheral initialization code. Pricing is \$774 in OEM quantities.

—David Lieberman

Systek

1027 N Kellogg St
Kennewick, WA 99336

Circle number 109



MAJOR SYSTEM COMPONENTS

Virtual SCSI controller matches new drives to range of interfaces

Today's SCSI-based peripherals—especially disk drives—have small idiosyncrasies that make them incompatible if the drives are used as direct plug-in replacements. These small but important differences are due to the fact that manufacturers have given their own interpretations to certain aspects of the SCSI specification, especially in the way that commands are implemented in code on the controller as well as in the drive electronics.

An intelligent disk controller from Toshiba America has implemented a "Virtual SCSI" for use on its high-capacity 5¼-in. Winchester disk drives to allow easy adaptation to different interpretations of the SCSI command set. This addresses the long-standing problem of matching

available inventory with the customer's needs without causing prolonged downtime during field upgrades, according to David Tovey, director of marketing. "Most disk manufacturers find that they have to offer specific customized products for different major customers—usually a different ROM," Tovey says.

One example of incompatibility might be a case where a customer wants a personalized inquiry response so that when the system queries the drive, it answers with the customer's brand name rather than with Toshiba's. Other incompatibilities involve mode settings for buffer control, specialized read/write opcodes for security purposes and codes that tell the drive whether to execute vendor-unique commands.

The Toshiba virtual SCSI controller is produced with a single version of the drive electronics and controller, but has different versions of the command set resident on tracks of the disk not normally accessed by the host system. Depending on the version of SCSI used by the host system and its interface, the drive will bring the corresponding version of the command set off disk and load it into the controller RAM at boot-up. The drives have sufficient storage capacity to handle the many different versions of the resident command set.

The result, says Tovey, is that the drive manufacturer has a single product in inventory that can easily be customized to look like any other drive or can be tailored to a customer's specific requirements via software. Such flexibility benefits the customer since special requirements can be implemented in the field

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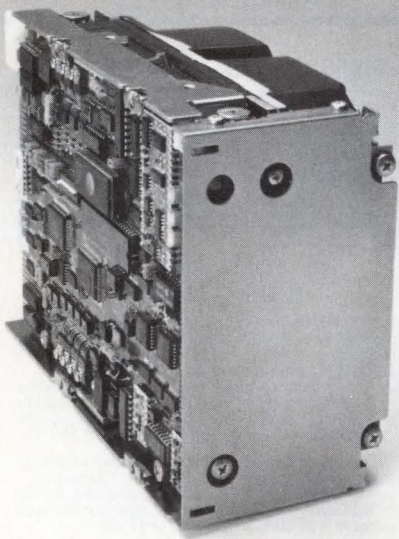
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without removing the drive from the system. Changes can be simply downloaded from the host.

Tovey notes that though standardization efforts are keeping SCSI stable, the need remains to support its many different interpretations. There's a certain amount of inertia because people often qualify a drive, and then assume vendor-unique commands and idiosyncrasies. When they get to the next-generation drive, they find it doesn't work with the drivers they have. Evolution for existing systems is easier to track



with drive-resident command sets. The virtual SCSI controller supports the standard 4.B SCSI command set and will support SCSI II. The controller has a 65-kbyte buffer and read look-ahead caching algorithms for zero-latency read/write operations. The SCSI connect/disconnect algorithm, which ensures efficient use of the bus by multiple peripherals, is controlled using buffer fill pointers that can be set to match bus speed and utilization characteristics.

The virtual SCSI controller is supplied on the Toshiba MK-350 FB 760-Mbyte drive, which sells for \$2,645. All subsequent SCSI-based disk drives from Toshiba will also host the controller. —Tom Williams

Toshiba America

9740 Irvine Blvd
Irvine, CA 92718
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Circle number 105

Multiscan monitor boasts single-scan performance

Designed for applications that require switching between formats with different resolutions, the MX-210 EZ from Monitronix is a 19-in. noninterlaced color graphics monitor that provides the same picture quality as a single-scanning monitor. When a user switches between applications with different resolutions—from high-resolution CAD programs to lower-resolution PC applications, for example—the monitor automatically aligns itself to the frequency of the display controller.

“One of the problems with multi-sync monitors has been that they're set up at the factory to work perfectly at one frequency,” says Roger Nielsen, president of Monitronix. “When a user switches applications and frequencies, the picture quality suffers with reduced image size, geometric distortion or some other imperfection. Our monitor solves that problem because it can accommodate four different frequencies.”

The MX-210 EZ automatically adjusts to any horizontal scan frequency from 30 to 74 kHz, or video formats ranging from 600 × 480 pixels to 1,280 × 1,024 pixels. Using multiple adjustment points, the monitor can automatically set both horizontal and vertical size, image position, and linearity precisely to the specifications of each different video format.

According to Monitronix, the MX-210 EZ offers the fastest sync switch speeds available on a multisyncing monitor—0.5 s—a considerable improvement over the conventional 4 or 5 s. This switch speed eliminates the flashing, waving or blank screens that usually occur when changing formats.

The monitor works with any graphics display controller, VGA and up, including Macintosh standards, and features a 200-MHz video bandwidth and a brightness of 40 to 55 fl. Vertical refresh rates of 60 to 120 Hz ensure a flicker-free display. In addition, the MX-210 EZ accepts analog RGB video input and boasts a full screen linearity of better than 1 percent over the entire display to provide accurate stability and dimensional measurement for intri-

cate drawings and data.

Available immediately, the monitor costs \$3,795. OEM discounts are available. —Mike Donlin

Monitronix

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Circle number 106

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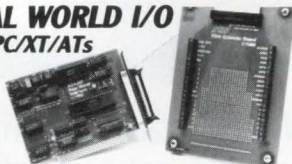
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CIRCLE NO. 170

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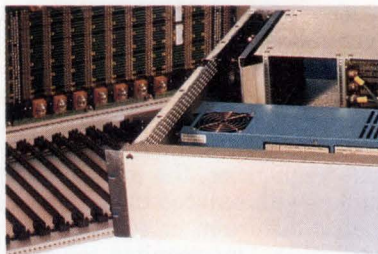
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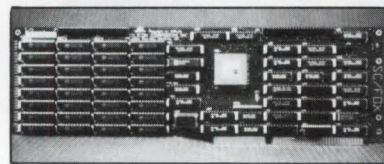
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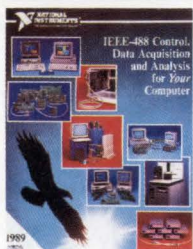
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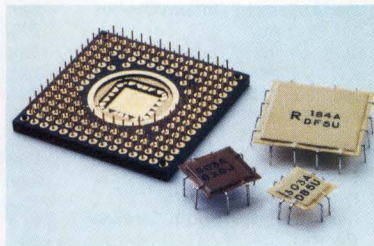
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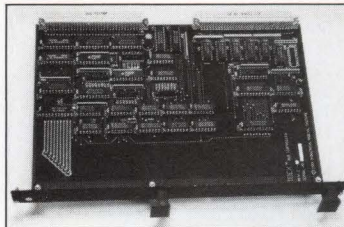


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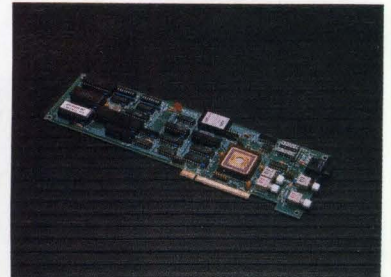
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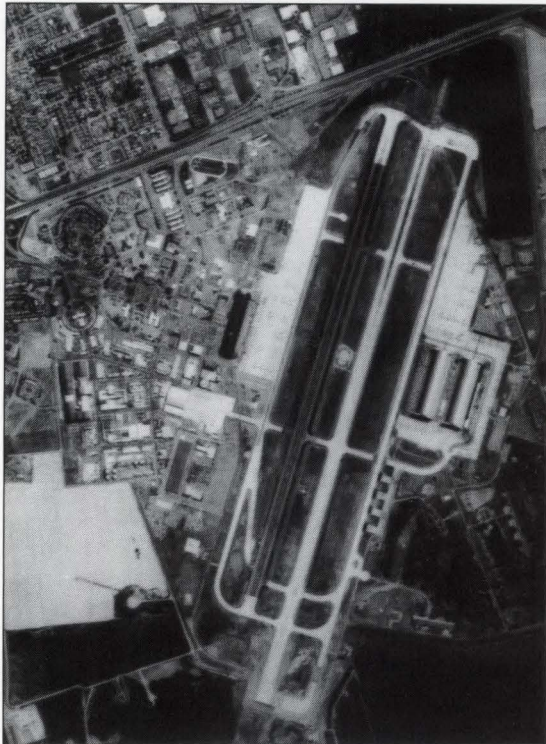
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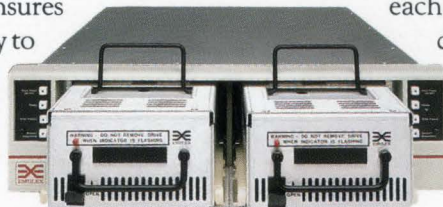
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