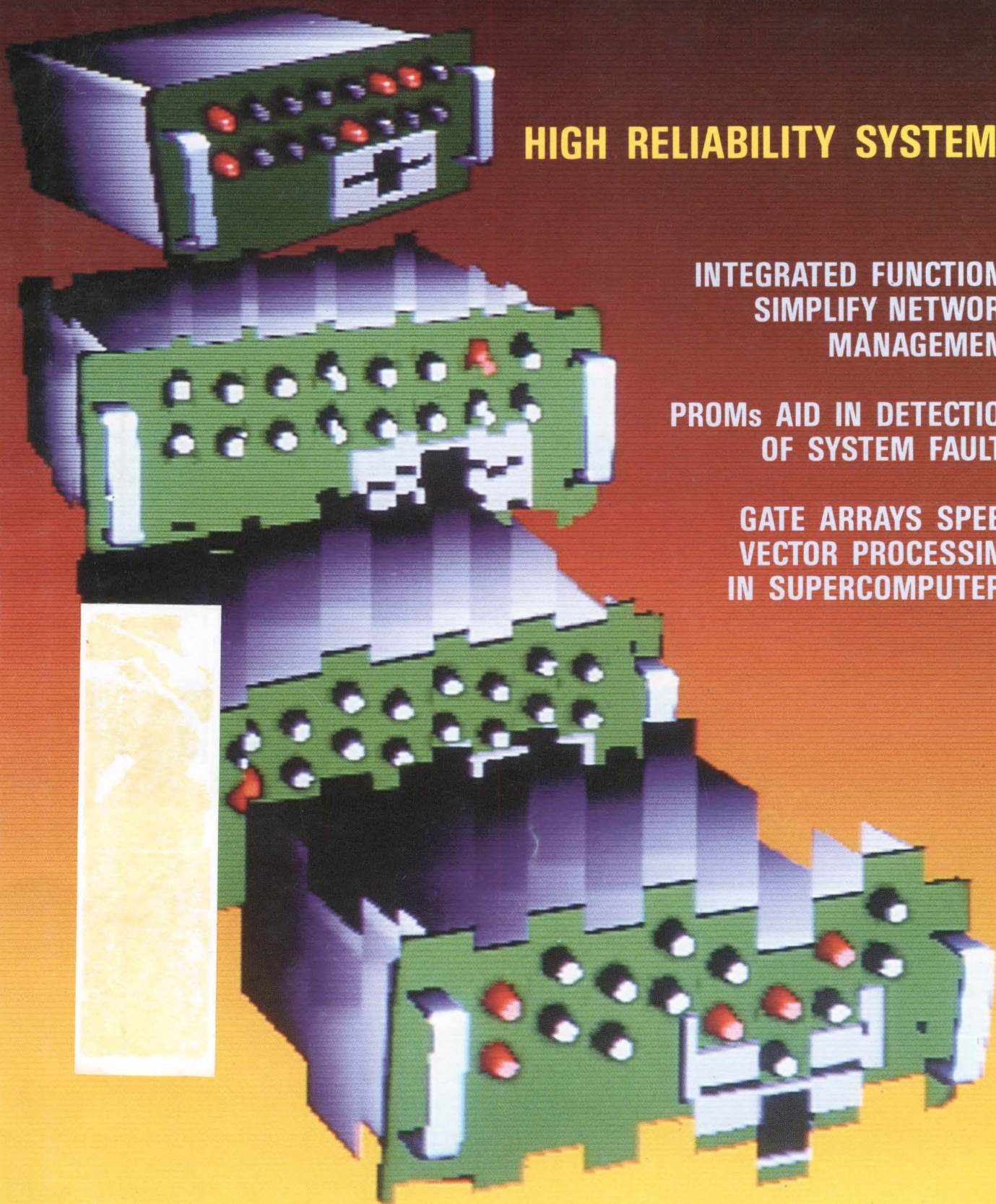


COMPUTER DESIGN



HIGH RELIABILITY SYSTEMS

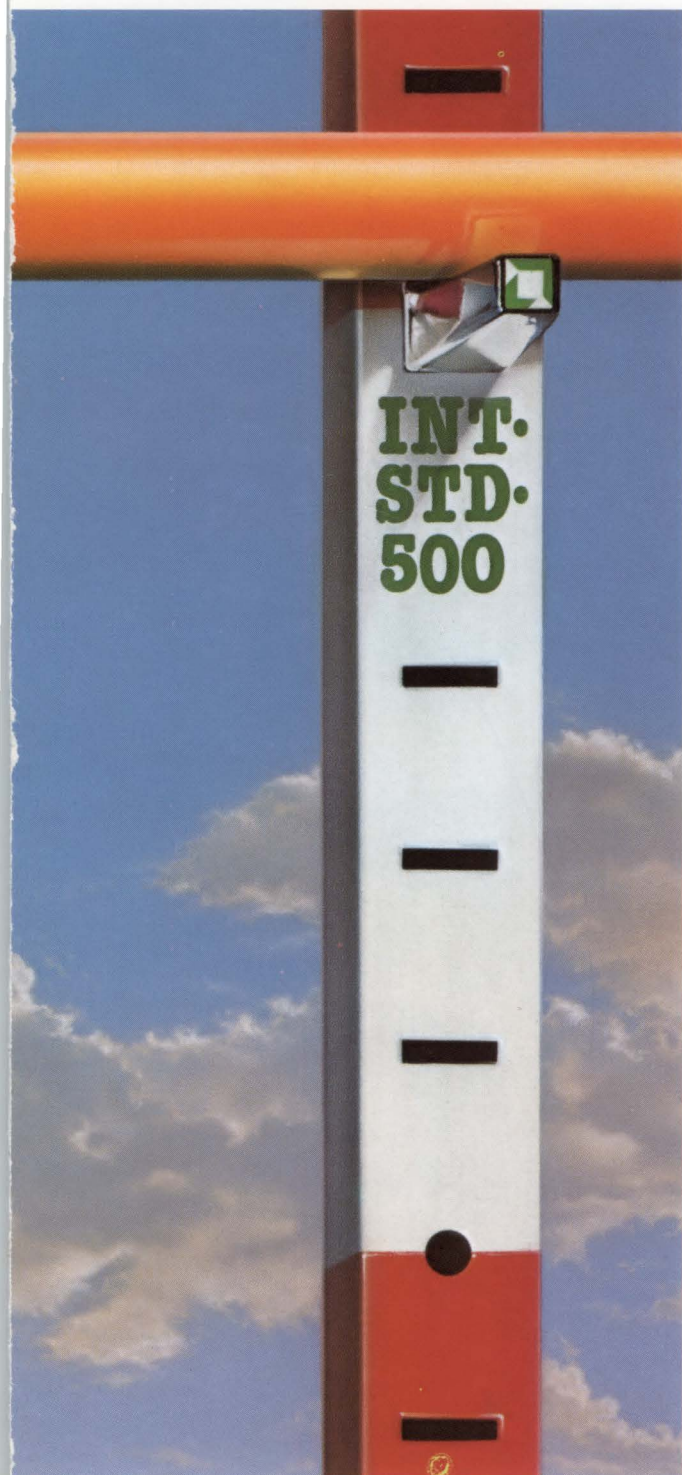
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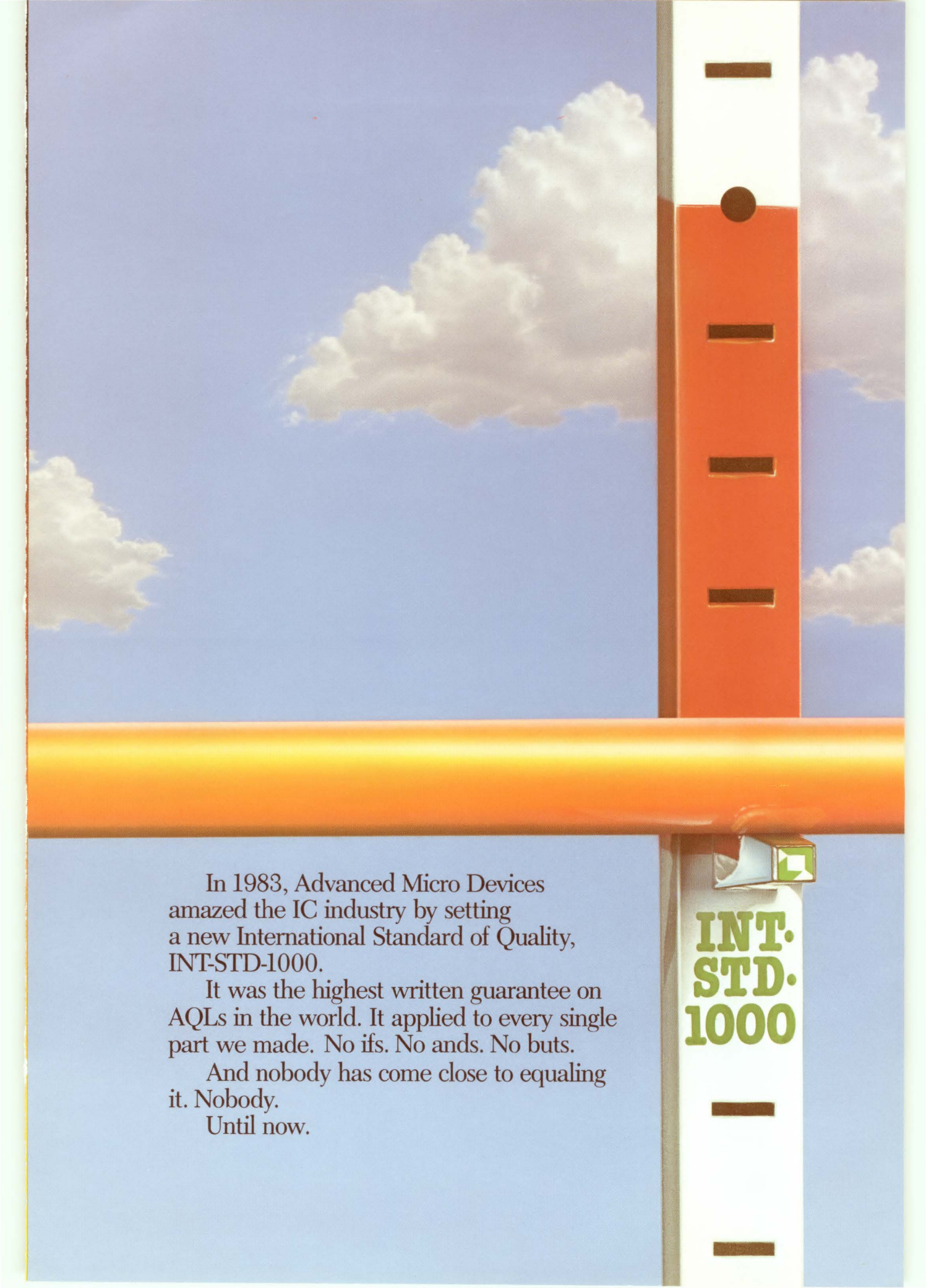
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Announcing

STC interface for the Kennedy Model 9400

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Not an adaptor, the STC interface is an integral part of Model 9400.

Finally, Model 9400 is a proven, mature product from Kennedy, the leader in peripheral tape products for over 20 years. And we deliver—in product, price and quality.

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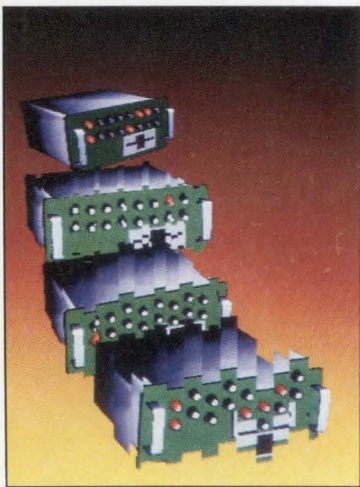
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CIRCLE 3

COMPUTER DESIGN[®]



This month's cover was designed by Jay Gordon. It was executed by Mary Codd at Codd Barrett Associates using computer-generated two-dimensional and three-dimensional solid models.

SPECIAL REPORT ON HIGH RELIABILITY SYSTEMS

- 101** What makes a system highly reliable is a function of the application and the user's perspective. For manufacturers, high reliability means longer mean time between failures and fewer repairs in the field. When life depends on a system, such as an aircraft or artificial respirator, it means the system must never fail. Every stage of the design process must come under tough scrutiny where high reliability is a concern.
- 103** **Fewer connections translate into fewer failures**
A major source of system failures—interconnects—can be alleviated by using more VLSI components and more careful consideration of connection and cabling schemes.
- 121** **Redundant modules may be best for control systems**
Despite the apparently higher price, triple redundancy can be the optimal trade-off of cost versus reliability in digital control applications.
- 129** **Shadowing boosts system reliability**
Using advanced data protection capabilities offered by shadowing techniques, designers can bypass conventional memory backup procedures.
- 139** **CMOS VLSI increases life expectancy of complex systems**
Low power consumption is usually touted as the major advantage of CMOS over bipolar. But CMOS provides the bonus of lower failure rates.
- 143** **Monitored burn-in improves VLSI IC reliability**
Device testing during burn-in provides information that can improve design and fabrication processes and pave the way for increased device yields and reliability.



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SYSTEM TECHNOLOGY

- 33** **Software:**
Graphics standards gain ground slowly
- 41** **Packaging & power:**
Power supply vendors cut size and cost
- 59** **Integrated circuits:**
Concurrent computers make scientific computing affordable
- 65** **Software:**
Languages promote parallel processing
- 75** **Interface:**
Eurocard bus takes a test drive in the United States
- 76** **Memory systems:**
Emerging QIC standards aim to enhance tape flexibility



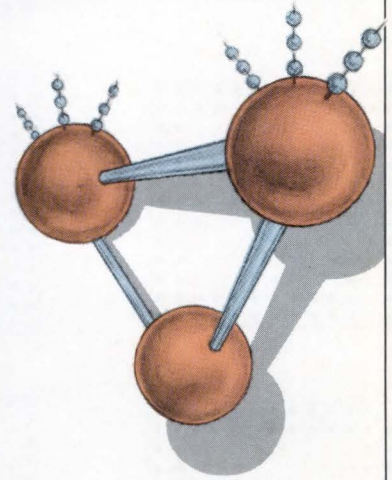
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Symposium sessions, seminars, and evening panel discussions will come together at SID '85 to cover the full range of information display technology. Speakers will emphasize both the industry of the future and the products and techniques available today.

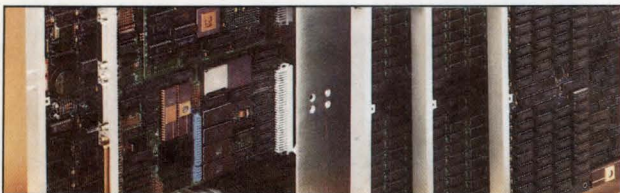
POSTMASTER: CHANGE OF ADDRESS FORM 3579 to be sent to COMPUTER DESIGN, Circulation Department, P.O. Box 593, Littleton, MA 01460 (UPS 127-340).

SYSTEM DESIGN

- 149 Data communications: Network management simplified through combined functions**
Integrating intelligent monitoring and control facilities into network nodes permits customized control, reporting, and management facility expansion as the network grows.
- 157 Integrated circuits: Registered PROMs help identify system faults**
Diagnostics, previously unavailable in a single chip, were done using SSI/MSI chips, or were ignored. Now, PROMs with registered output provide speed and on-chip diagnostics in pipeline, testable, microprogrammed systems.
- 169 Computers: Supercomputer breaks price barrier for vector processing**
By using off-the-shelf logic and semicustom gate arrays for vector processing, a supercomputer delivers high performance with a bargain price tag.
- 179 Memory systems: Standalone unit satisfies storage and backup needs**
Designers need more intelligent and flexible memory systems. Such units could take advantage of technological improvements in disk drives and have only a minor impact on existing hardware and software.



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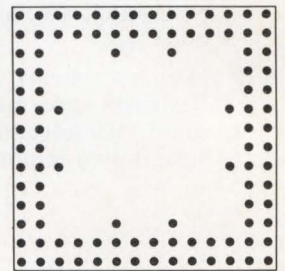
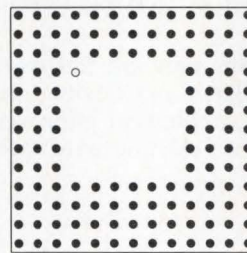
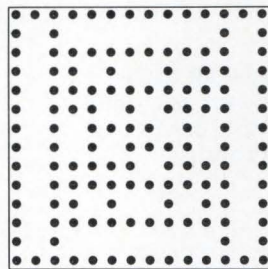
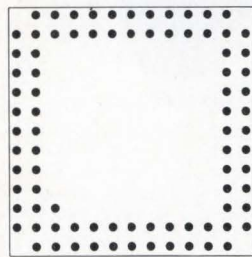
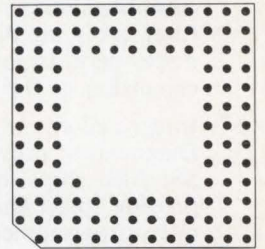
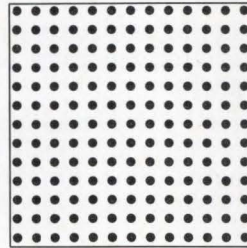
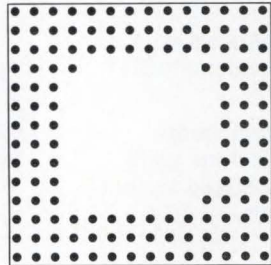
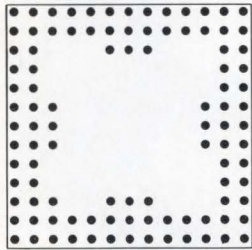
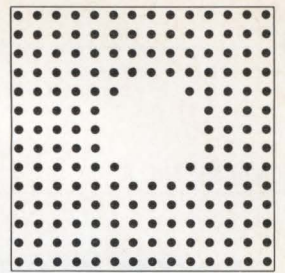
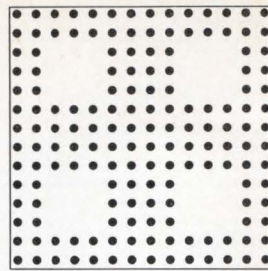
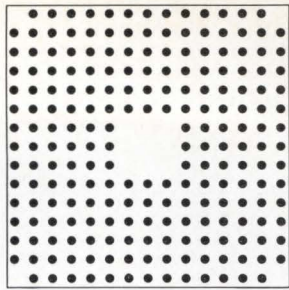
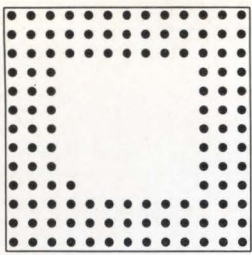
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SYSTEM COMPONENTS

- 187 Computers:**
Multibus II products support next-generation 32-bit multiprocessing
- 188 Test & development:**
Software CAD system provides realtime assembler
- 188 Test & development:**
Instrument family runs under PC control
- 189 Software:**
Development system enables speedy migration to C
- 190 Data communications:**
Compact communication processor built around a 32-bit chip
- 190 Interface:**
Communication boards adhere to OpenNET strategy
- 191 Test & development:**
State-of-the-art pattern generators enhance logic analysis system

DEPARTMENTS

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- 213 System showcase
- 214 Advertisers' index
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- 219 Reader inquiry card
- 219 Change of address card



Tell us wh

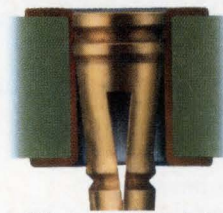
This is no psychological test. Rather, it's a sample of just a few Pin Grid Array Socket pin out combinations from Augat.

You see, with over 200 semiconductor pin out variations, Augat makes over 100 thousand socket combinations. More than any other manufacturer. And some people think we're crazy to offer so many. But what you see in every

one are the quality and innovation that set us apart.

Only Augat PGA's have 4 self-clinching pins that lock the socket tightly to the board —before soldering— for automatic or manual insertion. Plus all Augat PGA pins feature unique machined inner contacts with four-finger configuration, crafted to demanding tolerances.

For solderless applications,



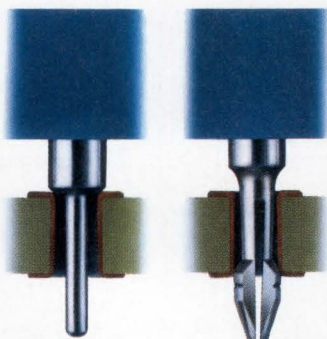
Why package from just one side of the board? Holtite gives you the same profile as a soldered IC.

take a look at our Holtite® zero-profile PGA's on mylar. It gives you the same profile as soldered IC.

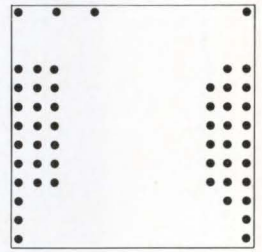
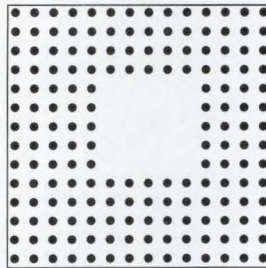
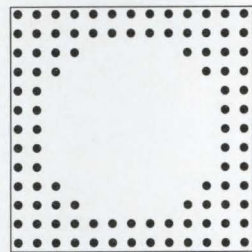
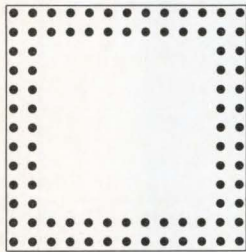
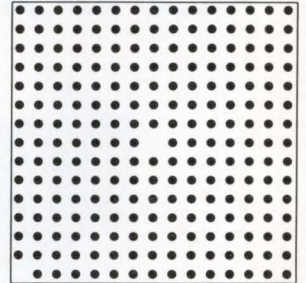
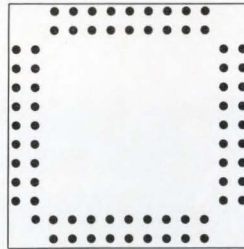
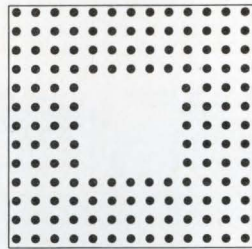
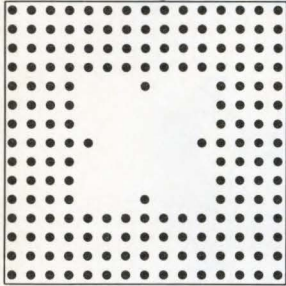
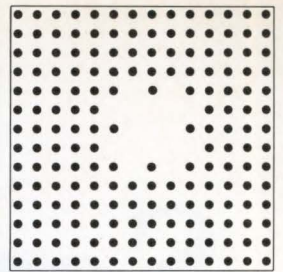
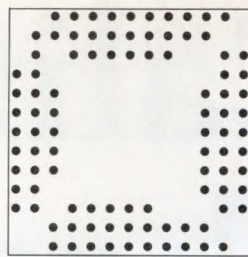
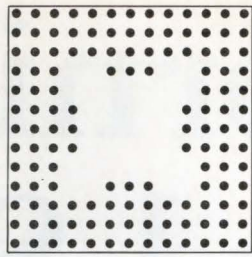
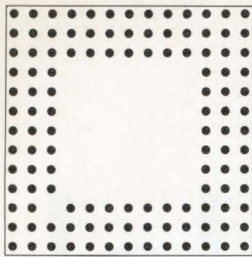
You can package from both sides of the board, too.

To make PGA's insertion and extraction a snap, there's our EZ-I/O™ tool. Unlike traditional tools, the EZ-I/O uses the socket shoulders or board surfaces as a stable lifting platform. There's no slippage or misalignment.

Our self-clinching pin can help your operation from falling apart during production.



Conventional pin. Augat pin. (cutaway)



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The Augat PGA prototyping kit (PPK1-1G1) lets you design the PGA's you need instantly. Included is a

Our EZ-I/O inserter/extractor, the right tool for the job.

back-up board, universal socket forms, socket pins, spring loaded seating tool and seating tip.



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A prototyping kit for designers who love to tinker. And who doesn't?

of sockets is faster than you think.

Send in the coupon for our newly revised PGA catalog. Because if you haven't seen our selection of Pin Grid

Array Sockets, you haven't seen anything yet.

I'd like to see a copy of your catalog of Pin Grid Array Sockets. Yes, the one with 6 variations of over 250 pin out combinations and an offer for free socket samples.

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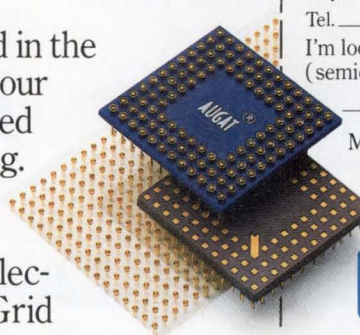
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I'm looking for Pin Grid Array Sockets to fit (semiconductor device & mfg.) _____

Mail to: AUGAT, INC., Interconnection Components Division, 33 Perry Avenue, Attleboro, MA 02703. (617) 222-2202. TWX: 710.391.0644.

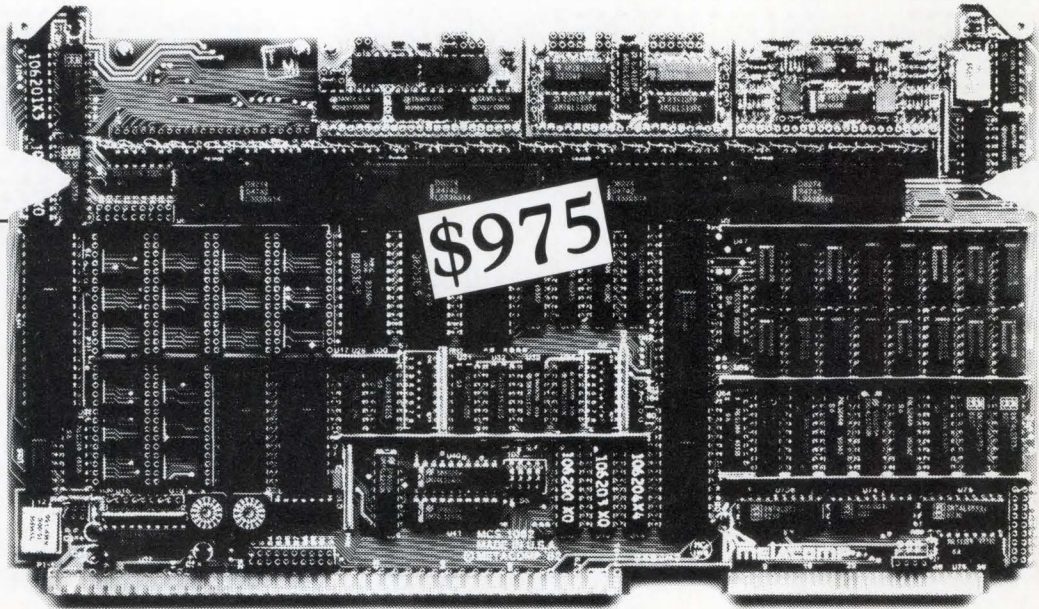


AUGAT INTERCONNECTION COMPONENTS

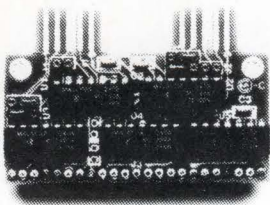
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CIRCLE 4

California Serfboard Sale!



Get eight channels of intelligent slave serial I/O with this new wave Multibus controller



The versatile California Serfboard, MCS-1062, is the first serial I/O controller with eight intelligent slave channels. Plus all the features highlighted below.

Product Highlights:

- Eight individual channels, programmable for ASYNC, SYNC, or BITSYNC.
- Programmable timers for ASYNC data rates to 76.8K Baud.
- Wide range of modular interface adapters available, each field interchangeable. RS-232, RS-422/RS-423 Optical Current Loop, MIL 188-114.
- On-board Intel 8088 CPU. 96K bytes EPROM (using 27128's), 128K bytes RAM.
- Simple "handshake" architecture for user software interface.

- Dual Port RAM. Supports 8 or 16 bit memory accesses, 24 bit Multibus addressing.
- Standard Multibus architecture. One unit load, single card slot, vectored or nonvectored Bus Interrupts.
- Terminal I/O firmware available.

And, right now, the MCS-1062 is available at an unbelievably low trial price. Only \$975. That's more than a 20% discount. If you've wanted to evaluate the MCS-1062 here's your chance to do so inexpensively.

For complete specifications and ordering information, call or write: METACOMP, Inc., 9466 Black Mountain Road, San Diego, California 92126, (619) 578-9840, TWX 910-335-1736 METACOMP SDG. Ride the new wave of high technology. Get your California Serfboards while they last!

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THE MULTIBUS BREAKTHROUGH PEOPLE

UP FRONT

DEC defends exclusive rights to MSCP

Digital Equipment Corp (Maynard, Mass) is defending its patented mass storage control protocol for the Q-bus and the Unibus. DEC has sent letters warning companies manufacturing products to the MSCP specification that marketing MSCP products may constitute patent infringement. The letter also says DEC did not intend to license MSCP to anyone. "We really don't think DEC is going to do anything," said Paul Getty, senior product manager for Cyclone, a Q-bus and MSCP-compatible Winchester/tape system for the MicroVAX made by Qualogy (San, Jose, Calif). "DEC was just exercising 'due diligence' under the law as they were obligated, to protect their patents." Getty admitted that Qualogy had received such a letter, but said the letter advised the company of DEC's patents and did not really constitute a "cease and desist" order. Other companies manufacturing MSCP controllers include Emulex (Costa Mesa, Calif), Spectra Logic (Sunnyvale, Calif) Sigma Information Systems (Anaheim, Calif), and Distributed Logic Corp (Garden Grove, Calif).—*T.R.W.*

AT&T unveils 7300 desktop computer, add-on developers ready

Finally letting its lions loose against IBM's AT, AT&T formally announced its 7300 "Safari" computer. Meanwhile, add-ons were already available to increase the machine's basic capabilities. Bell Technologies (Fremont, Calif), for example, had already announced its B40 40-Mbyte hard disk and its Bell Screen Editor for the AT&T machine. "We think AT&T has underestimated the emphasis corporate buyers place on ease of use," says Bell Technologies president Kathleen Farley. "When we heard AT&T thought business users would be happy with the Unix editors *ed* and *vi*, we doubled our sales forecasts." Likewise, Farley anticipates a significant market for its 40-Mbyte disk to replace the 7300's 10- and 20-Mbyte drives. "A 20-Mbyte maximum capacity is just not enough in a competitive Unix environment that includes IBM," Farley commented.—*W.E.S.*

Tektronix spins off gallium arsenide facility

TriQuint (Beaverton, Ore), the semiconductor house Tektronix spun off late in February, is bragging about its eight-week turnaround time for gallium arsenide semicustom parts. The company's first standard part is an MSI cell array. But company president Alan Patz says a full line of analog and digital chips will surface in the fall.—*B.F.*

Speech recognizer uses 3000 tokens to understand 1000 words

Look for the next step towards the talking typewriter at Speech Tech '85 in New York, April 21-23. Kurzweil Applied Intelligence (Waltham, Mass) will preview its 3000-token system that recognizes more than 1000 spoken words or phrases. The KV 3000 uses speech normalization, a form of high level pattern recognition that handles words or phrases up to a few seconds in length. The recognition occurs in virtually real time—generally

(continued on page 8)

(continued from page 7)

within 100 ms. Custom digital filters provide 99-percent recognition accuracy, according to company president Ray Kurzweil. The KV 3000 is available in Multibus, IBM PC bus, RS-232-C link, and single-board configurations. The company is also working on its VoiceWriter, a 10,000- to 15,000-word voice-activated word processor, which should be available in sample quantities during the second half of this year.—*N.M.*

Processor executes Forth in microcode

A processor to execute the Forth language directly has been developed by Novix Corporation (Cupertino, Calif). The chip, designed in part by Forth inventor Charles Moore, executes the Forth language in microcode, allowing it to perform many of Forth's instructions in a single machine cycle. The slowest instruction, a 16- x 16-bit multiply, takes 16 cycles, according to Novix general manager John Golden. The processor sets up two RAM-resident stacks and a main memory. Novix hopes to have development system boards that link serially to the IBM PC available for shipping by the end of May. Developers will write their software on the PC, then download it to the board for testing. The board will include 128 bytes of main memory and 8 Kbytes of programmable ROM. The Forth processor, now being manufactured for Novix by Mostek (Dallas, Tex), comes in a 124-pin package and runs at 7.5 to 8 MHz. Forth, Inc (Hermosa Beach, Calif) is providing software support for the chip.—*T.R.W.*

CAE, CAD manufacturers set to collide

Computer aided engineering tools, such as schematic capture and simulation, have developed independently from computer aided design tools for IC and printed circuit board layout. Now, CAD and CAE tool companies are invading each other's markets. For example, traditional CAD vendors that include Cadnetix, Applicon, Telesis, and Computervision are showing their first-generation CAE products. Meanwhile, CAE vendors are demonstrating IC layout tools, including MegaGatemaster from Daisy (Mountain View, Calif), a package for gate array layout, and the Concorde silicon compiler from Valid Logic (San Jose, Calif). Leading CAE vendors are expected to introduce printed circuit board layout tools this year. They could grab 50 percent of the printed circuit board CAE/CAD market by 1987, according to the Technology Research Group (Boston, Mass). "It's going to be a slugfest," predicts Mentor Graphics (Beaverton, Ore) vice president Gerald Langelier.—*R.G.*

Semicustom library added to workstation design tools

Signetics (Sunnyvale, Calif) will supply library software for semicustom chip design using Daisy CAE workstations by the end of the third quarter. Customers will be able to enter schematics, simulate designs, and generate netlists that will interface with Signetics internal CAD tools. Signetics' libraries of semicustom parts will include the ISL Flexx array, ECL macrocell arrays, CMOS Flexx array, and CMOS standard cells. Texas Instruments, Motorola, Mostek, Intel, and National Semiconductor already provide design tools to run on Daisy workstations.—*N.M.*

(continued on page 10)

Three Good Reasons Why Your Next MULTIBUS® Should Be Multi 286 . . .

It's Three Boards In One!

Multi 286 is everything you want in a MULTIBUS Computer. Multi 286 has . . .

- CPU
- MEMORY
- FLOPPY CONTROLLER

PLUS, much more - all on a single card! Multi 286 is truly the MULTIBUS Computer of tomorrow. But, if those three reasons weren't enough to convince you of that fact, here are three more. Multi 286 . . .

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- Offers the Software Interface of Your Choice
- Has Three Times the Processing Speed**

Whether you are a design engineer, O.E.M. or Systems Development Organization, Multi 286 is the solution you've been looking for. Designed around the powerful 80286 CPU, the Multi 286 has either 256K or 1MB built-in memory. Additional features such as numeric processor extension, four separate built-in controllers, programmable multiple protocol, and the ability to address 16 MB of physical and 1 gigabit of virtual memory make this truly the MULTIBUS Board of tomorrow. Check these predominant features listed below:

- Intel 80286 CPU
- 256/1MB configurable dual ported RAM with byte parity
- 16K to 128K of ROM space - with built-in diagnostics and loader
- Four channel DMA controller with 16MB physical addressing range (82258)
 - 5 1/4" and 8" floppy controller
 - Four programmable serial I/O interface
 - Numeric processor extension 80287
 - Centronics - compatible parallel interface
 - LBX & SBX Interface
 - RMX & Xenix and Concurrent DOS will be available soon
 - 16 levels of vectored interrupt control
 - Counter timer
 - Down load from your IBM PC, AT or Intel Series III
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Future Solutions Today!

Single-board computer ties DEC chip to VMEbus systems

An upcoming VMEbus CPU card features Digital Equipment Corp PDP-11 software compatibility. The board should extend the VMEbus's inroads into OEM markets. The card, dubbed the VME-1120D by its maker (The Logical Design Group of Raleigh, NC), is a 16-bit single board computer based on DEC's J-11 microprocessor. The J-11 sports 32-bit internal data paths and a 15-MHz clock. System designers can configure the double-Eurocard VME-1120D as a VMEbus controller, and it can be used in multiprocessor systems. The Logical Design Group claims full software compatibility with the whole range of PDP-11 computers from the 11/03 to the 11/70, and says it hopes to tap the existing DEC software base.—*J.V.*

Signetics will use Zymos ZyP design system

Adding itself to the growing list of semiconductor manufacturers using Zymos's (Sunnyvale, Calif) ZyP design system, Signetics announced it will design semicustom peripheral circuits under a second-source agreement with Zymos. The circuits will serve for data communications protocol controllers, bus interfaces, CRT controllers, and similar applications. Intel and General Instruments are among the semiconductor manufacturers already using the ZyP system.—*N.M.*



Standard cell libraries multiply

More semiconductor manufacturers are offering standard cell libraries. Among them are Mostek (Carrollton, Tex) and Motorola (Austin, Tex). Mostek's SA series library includes user-configurable RAMs, ROMs, and programmable logic arrays. Customers design their parts by linking to the company's Highland 2 design system. Expected lead time from design release to prototype shipment is 12 to 14 weeks. Motorola should announce its standard cell entries next month. Both Mostek and Motorola will offer "super cells," such as core processors and large memory blocks, as standard cells sometime in 1986.—*N.M.*

C compiler allows hybrid memory models on 8086

Whitesmith's Ltd. (Concord, Mass) has just announced a new version of its C compiler. The compiler allows programmers to choose among the available 8086/8088 memory addressing schemes directly from the C source code, a feature the company claims is unique. The package includes a source-level interactive debugger that allows the programmer to set breakpoints and examine variables.—*W.E.S.*

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WHEN THE GOING GETS TOUGH

A long-held axiom holds that when business is brisk almost anyone can make money, but when business is slow only the best-managed and most enterprising companies succeed. The axiom has held true throughout the short history of the computer industry. During each recession, the best computer and component companies increased their market share, while dynamic startups grew to replace the dying dinosaurs. Even though the current slowdown is mild or nonexistent by traditional economic measures, it is taking an unusually heavy toll from our industry. Perhaps the computer business has accelerated to the point where survival is the best we can expect during lean years. For company managers, the struggles resemble those nightmarish video games that allow you to play again if you win—while the degree of difficulty increases exponentially in each succeeding game.

The more perceptive managers have no illusions about problems they face. For example, warning his stockholders to expect reduced profits for the current fiscal year, Ray Stata, chairman and president of Analog Devices, recently stated: "A well-managed company in a volatile market must exhibit wide swings in financial performance." He explained that trying to produce consistent profits through downturns in the semiconductor industry is a bad long-term strategy. It prevents essential investments in research and development, increases in production capacity, and staff development. Obviously, Stata's concept of a "well-managed" company differs from some traditional views—possibly because he was trained as an engineer and, therefore, knows that investments in new technology are the key to survival. He is prepared to pay the price of extreme earnings volatility in return for a high rate of average long-term growth. The investors' ideal scenario of smooth and rapid growth no longer seems sustainable in the components segment of the computer industry.

Although Stata identifies market volatility as the root cause of earnings instability, he does not explain why the swings tend to grow progressively more violent. Perhaps he did not want to alarm his stockholders with economic horror stories. We are sure he knows, however, that fundamental changes in the industry have greatly increased the risks and costs that must be incurred to reap the rewards. Perhaps only high rollers should get involved; widows and orphans should seek a more secure haven.

The reasons for increased market volatility have been widely analyzed. Faced with intense price competition, rapid product obsolescence, and the "fad factor" in consumer markets, equipment builders inflated their orders

for components. Most of them overestimated their needs—and they all wanted to ensure availability and hold down costs. This set up a boom-or-bust scenario in which massive orders were cancelled or companies went out of business and were unable to pay their suppliers.

What is less widely understood, however, is why market fluctuations now cause such extreme swings in profitability. A major reason is that, over the years, computer and electronics companies have become more highly leveraged. Their fixed costs have grown so huge that a small change in sales produces a large change in earnings. Some industries, such as airlines and steel producers, have always been highly leveraged. Consequently, they have exhibited cyclical patterns in their profits. For computer companies, however, the phenomenon is quite recent.

What happened was that, with increasing product complexity, design automation was needed to lower development costs, minimize design errors, and speed up new product introductions. In some areas of activity, such as documentation and software development, much larger staffs had to be recruited to handle tasks that could not be heavily automated. Simultaneously, production automation was required to lower costs and maintain quality control of the increasingly complex products. The high costs and rapid obsolescence of the capital equipment, in turn, combined to boost the fixed-cost burden.

Because of fundamental changes in the computer industry, therefore, both corporate and engineering managers now face probably the toughest challenges of their careers. For engineering managers, increasingly complex technical decisions must be made in an increasingly risky economic environment. Once again, only the best-managed companies will succeed. And, more of the surviving managers should turn out to be engineers—like Ray Stata. But, this time, those engineers who fully understand the changing dynamics of the industry should have the edge.



Michael S. Elphick
Editor in Chief

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HP 64000	EMULATION	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
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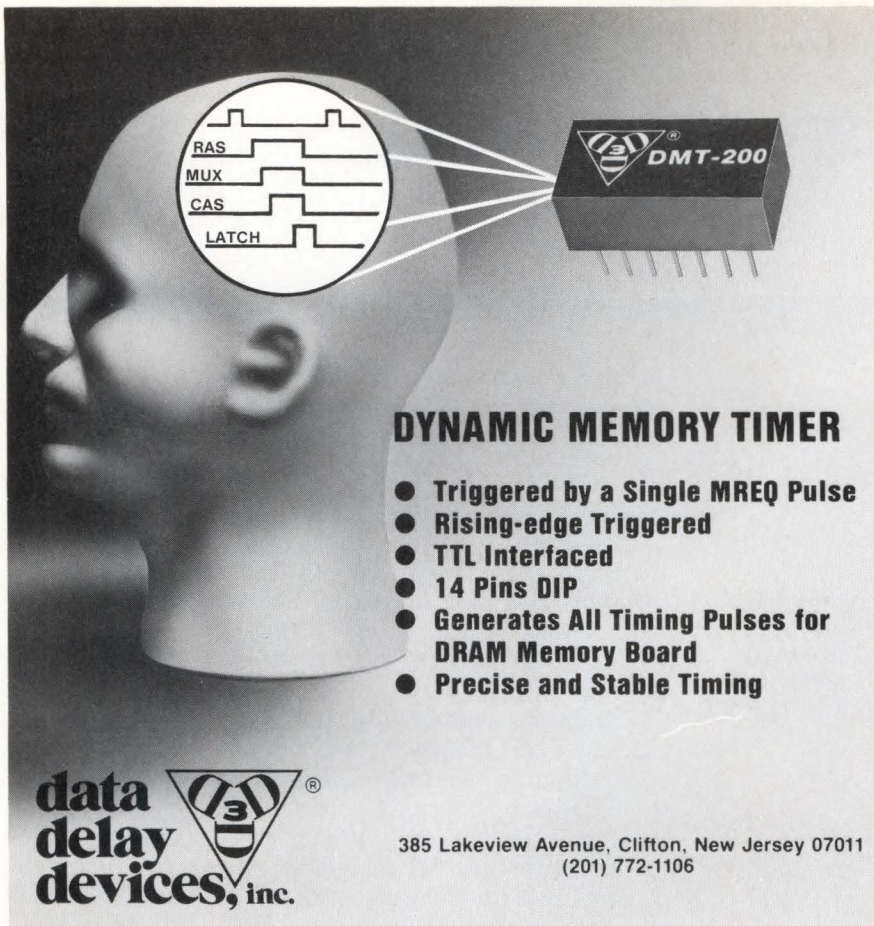
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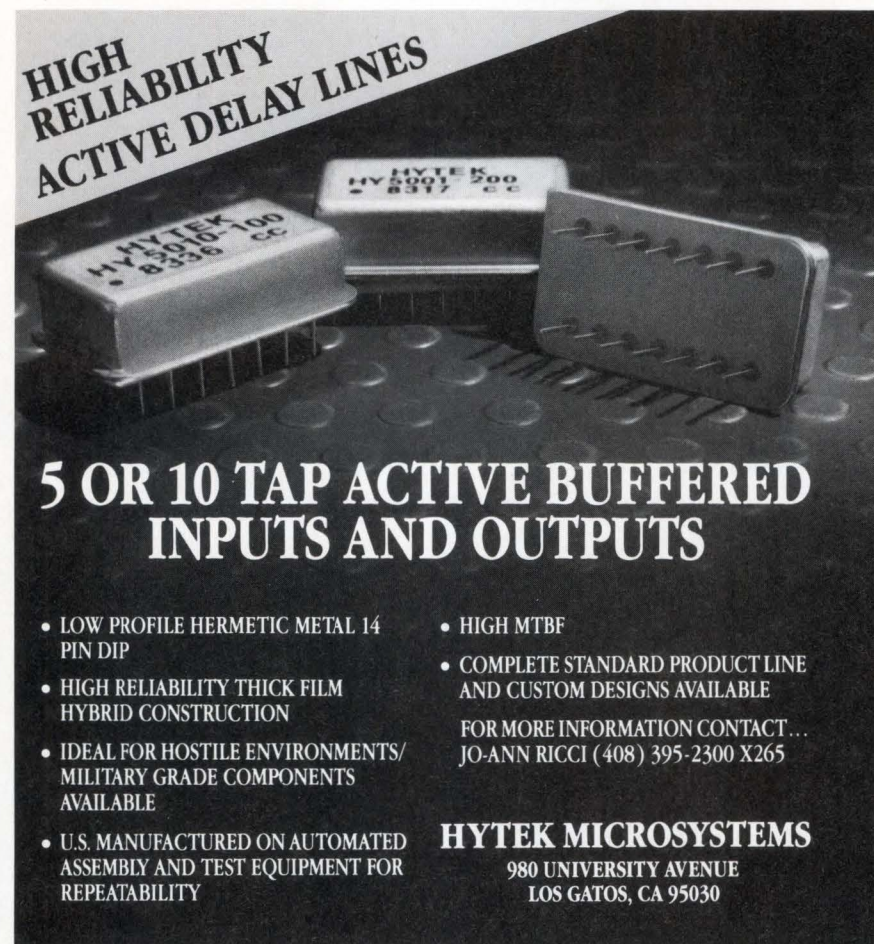
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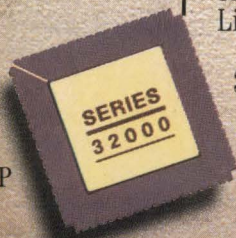
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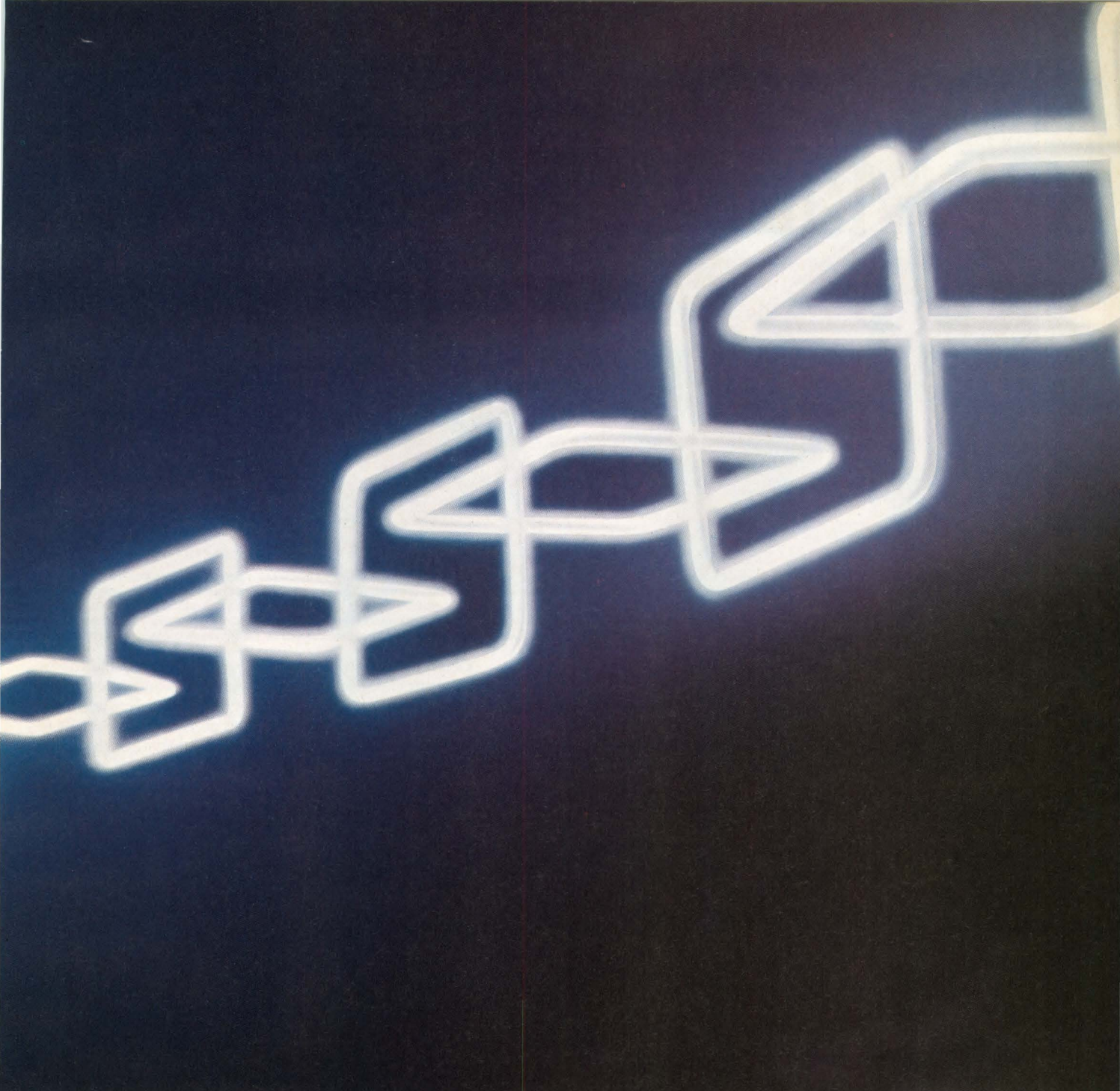
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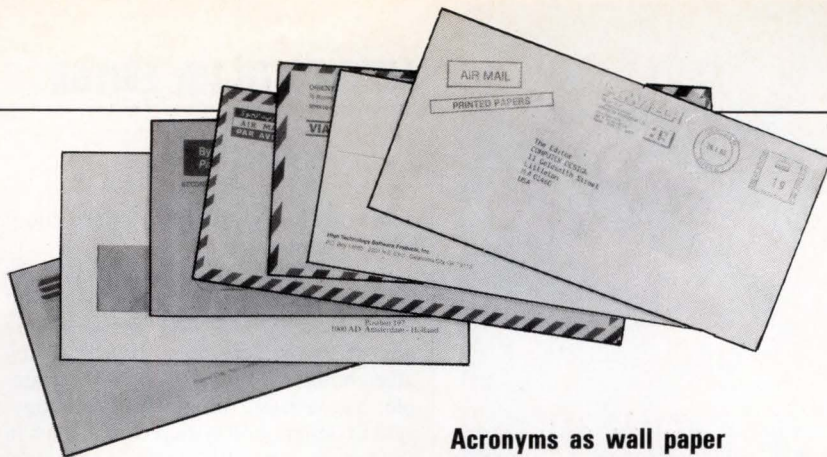
In the Oct 15, 1984 issue ("Artificial Intelligence Concepts are Being Put to Practical Use," p 45), *Computer Design* incorrectly quoted DM Data as estimating the artificial intelligence market to reach \$10 billion by 1990. In fact, the number we have published is approximately \$3 billion by 1990, with the dedicated expert systems market comprising approximately \$800 million of that total. AI military applications will continue to increase every year, but will drop proportionately compared with amounts spent for industrial, commercial, and research applications.

The expert systems market will probably grow to about \$57 million in 1985, with other AI-related markets such as visual recognition boosting the 1985 AI market to about \$240 million in total.

Harvey P. Newquist III
DM Data, Inc
6900 E Camelback Rd, Suite 1000
Scottsdale, AZ 85251

Just can't wait

I enjoyed reading the article on the potential of current and future multiprocessor architectures in providing added processing power ("Multiple CPUs and More Memory Define Next Generation," Dec 1984, p 83). Of particular interest to us and our clients is the chart on p 84, showing the price/performance of IBM 43XX machines and predicting just where the next generation product(s) might fit in.

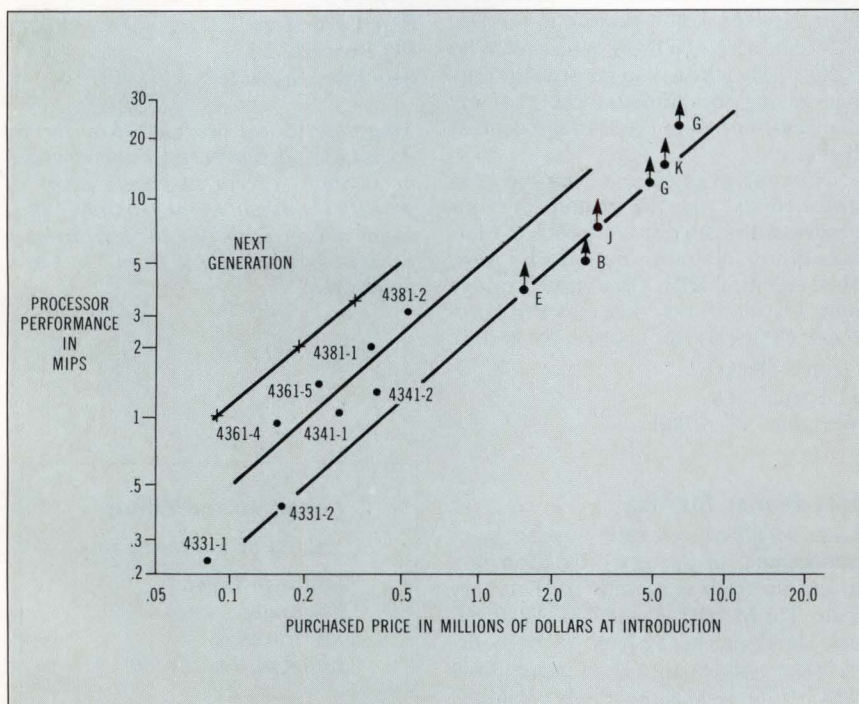


Our clients are waiting with bated breath for the next generation machine which will provide 3- to 4-MIPS performance for 6 times the price/performance of IBM 4381-2. They can't wait, as well, for the low end of the next generation which is shown to provide 1-MIPS performance (about a third of the 4381-2) for about \$800,000 (about half again the price of the 4381-2). Or, comparing it to the 4341-1, about the same level of performance for close to three times the price.

Other than the aforementioned problem, your article was of great interest and indicative of the tremendous acceleration of performance per dollar increase made possible by the newer generations of VLSI building blocks and microprocessors.

Peter B. Pitsker
North & Donahoe
1800 E Garry Ave, Suite 114
Santa Ana, CA 92705

As Mr Pitsker suggests, customers will show more enthusiasm for systems introduced at \$100,000 per MIPS (shown on the corrected curve).



Acronyms as wall paper

Sitting here at my desk real late reviewing pubs, I do not have a chance to look at during the day, I read the Jan 1985 editorial—the best I've seen in years.

As a marketing and communications exec (whatever that means), I constantly have to read something over and over or run to engineering to clarify an acronym so I can try to understand what's written.

I've asked many reps to see if they can get me a listing of these acronyms or abbreviations that I can paper my walls with for easy reference—no luck yet. Any suggestions?

Regards and TKS from JES sitting here OMA at FDC.

John E. Scolamiero
Florida Data Communications
600 D John Rodes Blvd
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Several reference books provide definitions for abbreviations, acronyms, and terms used in the computer and electronics industries. Computer Design's primary source is the IEEE Standard Dictionary of Electrical and Electronics Terms, published by the Institute of Electrical and Electronics Engineers, New York, NY. Another source that may interest Mr Scolamiero and other readers is the IBM Vocabulary for Data Processing, Telecommunications, and Office Systems. Be advised that definitions and acronyms may vary, depending on the source.

Keeping the balance

The January editorial sure hits at one of my pet peeves. I have written to editors about this myself and don't know if you might have been one. The problem arises, of course, where different technologies come together. PCs (printed circuits) go to make up PCs (personal computers) that are used as PCs (programmable controllers).

The editorial touched on, but did not elaborate on another author/editor pet peeve. That is the failure to define an acronym the first time it appears in an article, or to do so inconsistently. I actually read an article where the author defined RAM and ROM and then went merrily on using more state-of-the-art

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LETTERS TO THE EDITOR

acronyms freely with nary a peep about what they stood for.

You did mention the need for a publication to define its audience. I agree, but there's the rub. Audiences change and are almost always somewhat mixed for any given book. *Computer Design*, for example, has sections on system technology, system design, and system components in the January issue. We creatures of the real world get boxed into the cells (sometimes called fields or disciplines) we work in. We try to keep up with the action in other cells by reading the likes of *Computer Design*. That leads to an editorial problem.

As I seek cross-pollination from the other cells, I read as an outsider, not totally familiar with the latest jargon. I appreciate the efforts of an author to take me along, without boring the reader whose cell is being reported on. A balance is needed; you have to set the pivot point and see that your readers stick with it.

Enough crabbing! I like *CD* and enjoy reading selected articles but seldom get an opportunity to do a cover-to-cover. The ads are informative too. But, by the way, ad writers are about the worst offenders when it comes to unidentified symbology.

John E. Thompson
908 Burns Ave
Flossmoor, IL 60422

What's what from a who's who

I thank you most sincerely for stealing my thunder—whose intensity is admittedly many decibels below yours—in the Dec 1984 editorial, "Who is Who and Who is Not." My wife has so far been the only one having the dubious benefit of my diatribes regarding the Entrepreneur of the Year.

The concept of entrepreneur has been distorted as was the matter of your gender, with both distortions due to Marquis Who's Who (in whose flock I now, alas, count myself). On a more positive note, I have for some time regarded *Computer Design* as my favorite of its ilk.

George Hacken
12 Shepard Dr
Wanaque, NJ 07465

Fast Fourier fits fine

I was delighted to see Bill Suydam's announcement of our new FFT algorithm in the Up front section of the February issue. The MADCAP and TMS320 Product Development System software described are generating a lot of interest from designers and signal processing engineers.

The algorithm is called Practical Transform Lengths (PTL). It computes 97 different FFT lengths between 2 and 1024. It will process a 1001-point FFT two and a half times faster than the nearby 1024-point standard FFT, in less time than a 512-point standard FFT, and in less than double the time of the 256-point standard FFT. This processing time savings is only one of the several advantages of this next-generation FFT algorithm. It offers seven times the number of places that a filter can be placed at specific frequencies, and it eliminates padding samples with up to hundreds of zeros in order to reach the next power of two that standard FFTs compute. Therefore, there are severalfold savings in I/O time, processing time, and memory requirements. PTL allows you to match your processing to the problem, not shoe-horn the problem into the existing processing lengths.

Joanne Smith, President
Whitman Engineering, Inc
520 S Maitland Ave
Maitland, FL 32751

A matter of style

The January editorial made some excellent observations regarding acronyms, etc. For accuracy, however, I must take exception to your suggestion that the symbol μ would be an abbreviation (refer to ISO-1000 standard).

Since it is a symbol, it does not take a period (yes, that is why!) the way abbreviations do.

Perr Cardestam
PO Box 32572
San Jose, CA 95152

Your observation is correct. However, we do not use a period in either abbreviations or symbols, except to clarify areas of potential ambiguity. For example, "in." as an abbreviation for inches carries a period to distinguish it from "in" as a preposition.

Letters to the Editor

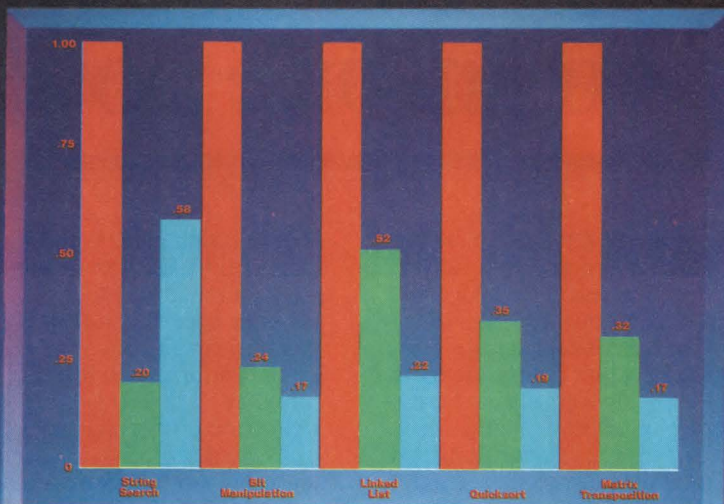
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MC68020, NS32032 and IAPX 286 data as reported in Systems News, Fall 1984 issue. No higher clock speed on the IAPX 286 was available.

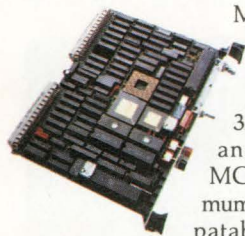
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Intel IAPX 286 8 MHz

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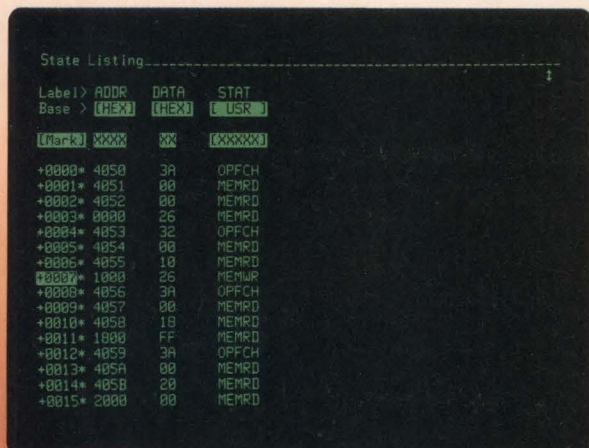
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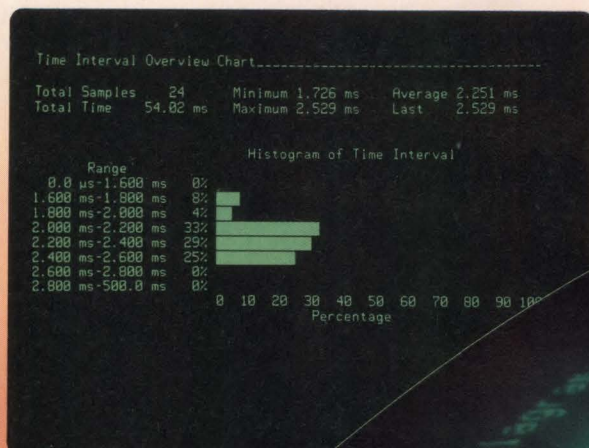
lyzer section gives you up to 16 channels of simultaneous acquisition. You can set the HP 1631A/D to capture single shot, cumulative mode, or even continue acquisition until your special conditions are met, for fully automatic "babysitting". Extensive pattern triggering and trigger qualification capabilities further extend your diagnostic horizons. The HP 1631A/D also includes a wide array of real-time processing and post-processing options such as mean and standard, min/max, state indexing and storage, and software performance analysis histograms.

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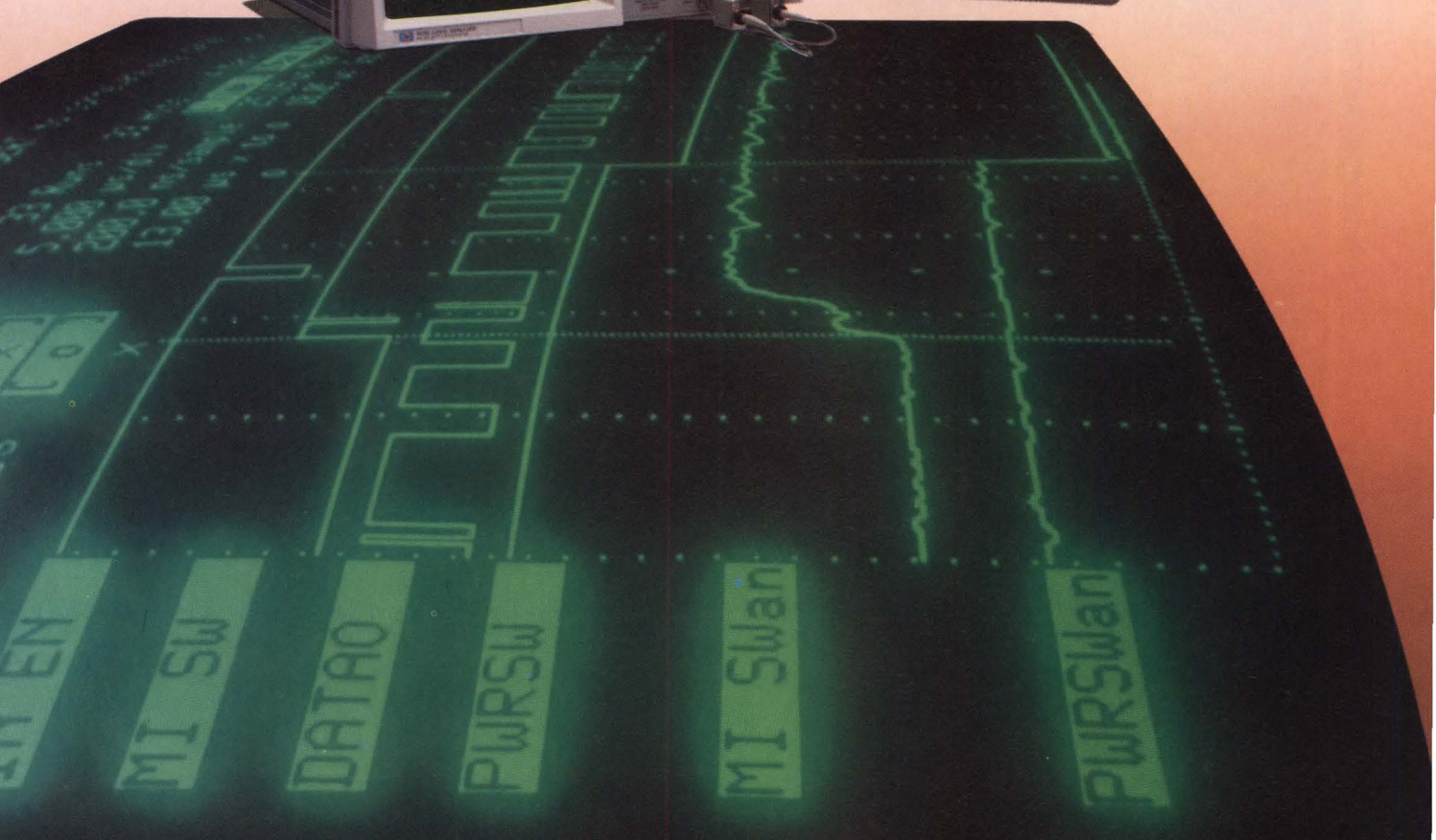
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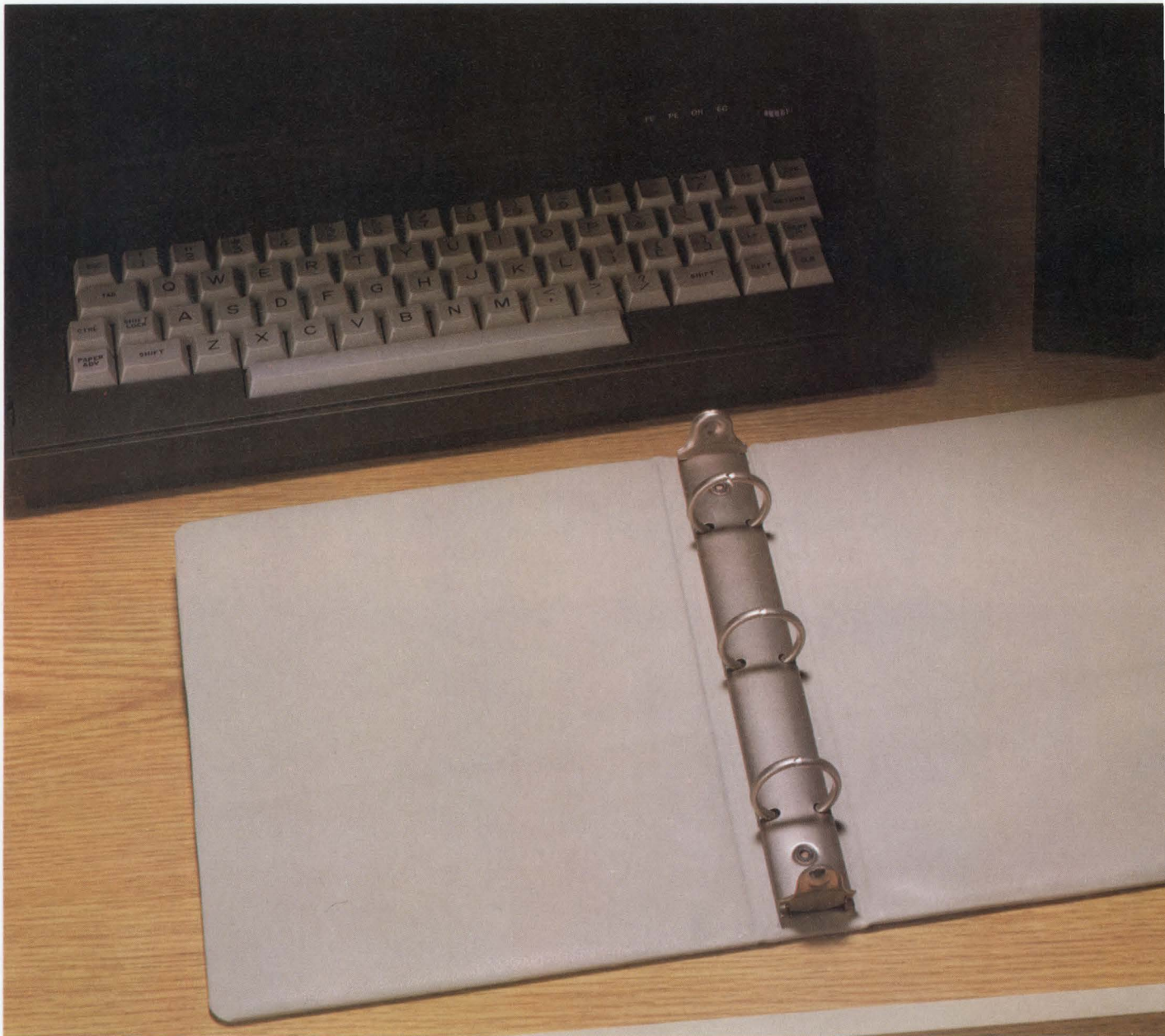


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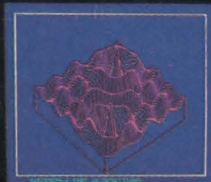
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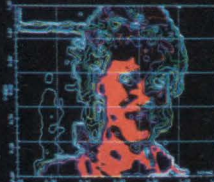
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Graphics standards gain ground slowly

The world of graphics standards resembles an uncharted swamp, interspersed with pieces of ground solid enough to gain a foothold. Individual graphic systems makers can plot their courses with the aid of a vague map showing the size and shape of accepted and proposed standards. Progress is slow, however, because interested parties have yet to agree on an interpretation of the map.

Nevertheless, along the way a great deal has been accomplished in computer graphics. This has happened despite the complexity of the technology as a whole, the variety of standards (proposed, *de facto*, proprietary, and official), and the range of competing commercial interests driving the industry.

Among the more important landmarks is the apparent resolution of whether the Graphics Kernel System or the Association for Computing Machinery's SIGGRAPH Core definition would become the official standard of the American National Standards Institute and the International Standards Organization. The winner is GKS, which should be adopted very soon. ACM has formally withdrawn its support of the proposed Core definition as an international standard.

All politics and pressures aside, certain implications are clear. One is that some companies, notably Tektronix, which had built up product lines based on their own implementation of Core, are hastening to develop GKS-based versions of the same products. Tektronix' formidable Plot-10, which some regard as a standard in its own right, has appeared again in the form of Plot-10 GKS.

This has been a problem for Tektronix because the Core-based version, like Core itself, supports three-dimensional graphics, while GKS thus far is a two-dimensional standard. It is no surprise, therefore, that Tektronix is very active on the GKS three-dimensional committee.

Tektronix' situation illustrates how important it is to implement the standards rapidly—customers cannot wait for current standards disputes to

be resolved. Constant, dynamic tension exists between the deliberations of committees and the needs of companies to provide quality products. If agreement is not reached soon, companies will have to second-guess the standards committees to manufacture the products demanded by their customers.

GKS is so compelling as a standard because whatever its functional limitations, it is precisely and completely defined. Core, though richer in functions than GKS, does not have the exact calling conventions and language bindings that are indispensable to applications portability.

For example, GKS has a definite syntax and sequence to be used in calling, say, the poly line function (defined by naming the points of the line) from the Fortran language. This is not specified in any Core definition, except in one that an individual company (such as Tektronix) produced. Anyone writing applications for Tektronix products would use that convention, but could not be sure it would be the same for other manufacturers' products.

GKS provides solid ground

The definition and adoption of GKS is going to provide a firm footing. Like Core, it supports a set of drawing primitives and attributes as

well as input functions. All two-dimensional graphics functions can be built up from the set of drawing primitives: poly line, polygon, marker, text, and cell array.

GKS, on the other hand, allows programs to use advanced device capabilities via a generalized drawing primitive. This permits function numbers and parameters of GKS primitives, such as one to draw a circle, to be passed through GKS directly to the device. The graphics device then will execute the function in its hardware and firmware.

GKS also supports device independence by use of a workstation descriptor table. When a workstation is opened, GKS determines what its capabilities are by looking at the entries in the table. It can then use all entries that describe the workstation. It can also figure out how to best handle capabilities that are called for by an application but are not supported by the workstation.

For instance, if a program calls for a color fill on a monochrome device, GKS may substitute a fill pattern of some sort. The programmer need not worry about specific display capabilities, but can simply concentrate on the application.

One of the things GKS does not yet provide is a hierarchy of macrofunctions within the application. Such a

INPUT LEVEL \ OUTPUT LEVEL	A	B	C
0	NO GRAPHICS INPUT. MINIMAL CONTROL. PREDEFINED BUNDLES ONLY.	REQUEST INPUT. MODE SETTING. INITIALIZE INPUT DEVICE. NO PICK. NO INPUT PRIORITY.	SAMPLE AND EVENT INPUT (NOT SUPPORTED BY FORTRAN 77).
1	FULL OUTPUT INCLUDING FULL BUNDLE CONCEPT. MULTIPLE WORKSTATION CONCEPT. GRAPHICS SEGMENT SUPPORT. METAFILE STORAGE.	ALL OF 0B ABOVE. PLUS REQUEST PICK MODE. SETTING AND INITIALIZE FOR PICK.	SAMPLE AND EVENT INPUT (NOT SUPPORTED BY FORTRAN 77).
2	ALL OF 1A ABOVE. PLUS WORKSTATION INDEPENDENT SEGMENT STORAGE.	ALL OF 1B ABOVE.	SAMPLE AND EVENT INPUT (NOT SUPPORTED BY FORTRAN 77).

The Graphical Kernel System standard is defined in three input and three output levels to meet different system needs, for a total of nine possible combinations. Addition of a third dimension and hierarchy would create a level 3-C.

Status of Graphics Standards Projects *		
Project	International Standards Organization status	American National Standards Institute status
Graphical Kernel System	Know as DIS7942. Seven comments received from Draft International Standard ballot. Responses approved at June 1984 WG2 meeting. IS 7942 published by ISO by July 1985.	Known as dpANS X3.124. Eight comments received from public review. Responses approved by X3H3 at its Oct 1984 meeting. ANS X3.124-1985 published mid-summer 1985.
GKS Language bindings: Fortran	Draft proposed Feb 1985. Circulate for comment.	Part of dpANS X3.124.
Pascal	Draft proposed Dec 1984. Circulate for comment.	Public review in fall 1985.
Ada	Draft proposed Feb 1985. Circulate for comment.	Public review in fall 1985.
C	Not an ISO standard language.	Working draft within X3H3. Public review in 1985, if X3J11 circulates dpANS C in 1985.
GKS three-dimensional extensions	Draft proposed in Feb 1985. Circulate for comment within ISO.	Participating in drafting effort within WG2. Will comment on ISO draft proposed when DP8805 circulated in spring 1985.
PHIGS	Base document being circulated for comment. Accepted as ISO work item in TC97, Feb 1985. Draft proposal in Jan 1986.	Working draft nearly complete. Public review in winter 1985-1986.
Virtual device metafile (Computer graphics metafile)	Known as ISO DP8632. DP8632 circulated for draft proposed ballot in summer 1984. Second draft proposed ballot closed March 15, 1985. DIS expected Oct 1985.	Know as dpANS X3.122. Thirteen comments received during public review. Responses approved at X3H3 meeting in October. Second public review period between Nov 15, 1984, and Jan 15, 1985. Third public review, fall 1985 on ISO changes.
Virtual device interface (Computer graphics interface)	New work item proposal voted on in spring 1985 with ANSI as sponsor.	New working draft available in Jan 1985. Public review in Feb 1986.

*Status Report prepared by Peter R. Bono, chairman ANSI X3H3

hierarchy would allow an application to call a circle with its parameters including radius and color. This would, in turn, call the appropriate GKS drawing primitives to create the circle.

Companies that are using GKS as a basis for their present products, therefore, feel a need not only to provide specific applications software based on GKS, but also to give a set of application software building tools. As a result, GKS becomes the basis of subroutine libraries upon which the application designer can base programs that think in such terms as "bar," "pie," and "text string," rather than as a bewildering series of GKS primitives.

Because applications based on calls to these subroutine libraries are all ultimately based on GKS, they will be portable among GKS environments. One such library, Visual C-Chart by Visual Engineering (San Jose, Calif), is built of GKS primitives from the company's Unix-based GKS. The Visual C-Chart, in turn, is used to build a set of commercial graphing and drawing tools. However, Visual C-Chart proved to be so useful in its own right that it too is offered as a commercial product.

GKS extensions

Since GKS does not yet provide hierarchy or three-dimensions, an effort is under way to add another level to the existing GKS standard definition. This would be called Level 3-C. At this point, the ANSI X3H3 committee is debating whether to add this new level as a pristine outgrowth of GKS or to adapt the independently emerging Programmers' Hierarchical Interactive Graphics Standard to the existing GKS structure.

PHIGS, as it is being proposed within the TC97 working group of the X3H3 committee, already provides hierarchy and three-dimensional transforms that approximate GKS techniques. This makes adaptation of PHIGS attractive to some. It is often said that PHIGS hierarchy has good control granularity. This means that, though PHIGS output primitives are very close to those of GKS, they can be grouped into structures along with attributes, transformation

specifications, and invocations of other structures to form pictures.

In such an organization, picture structures and segments inherit attributes from their parent structures unless they are explicitly changed. Because the definition granularity and the control granularity are the same, it is easy to edit a picture interactively by working with the actual visual elements. The picture can thus be modified and edited after the program is written.

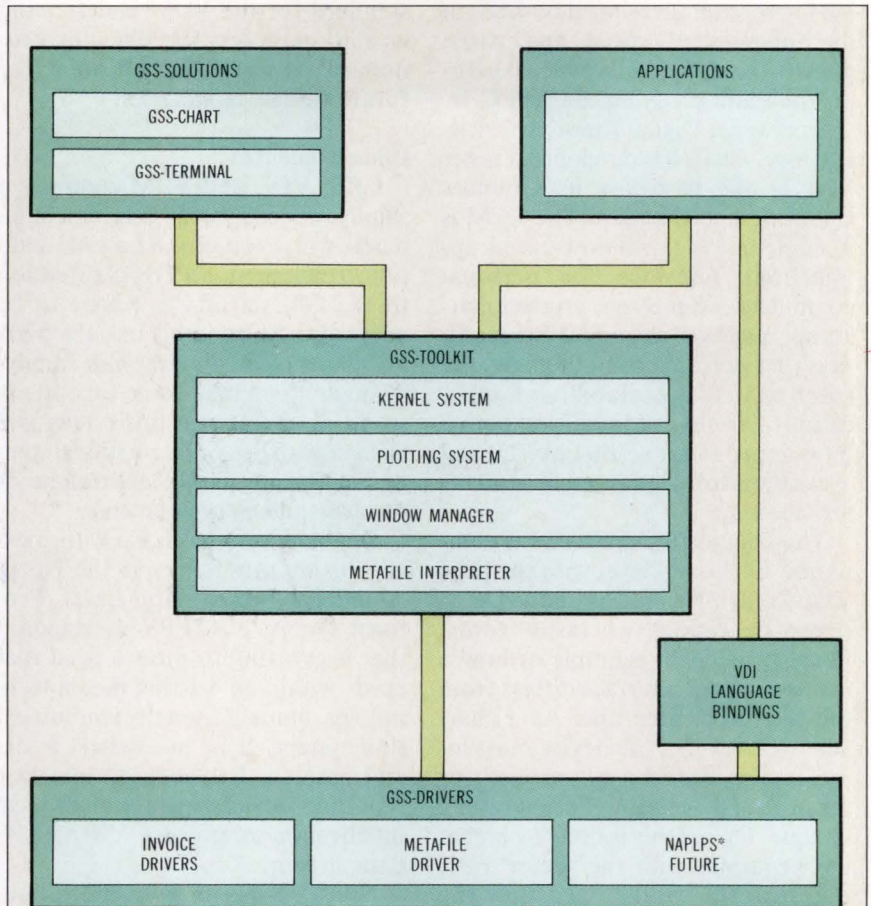
PHIGS uses an abstract workstation that is defined by a table, as does GKS. But PHIGS adds a workstation type known as the metafile. The metafile concept is also the subject of the ANSI technical committee X3H3, which is trying to define a standard format known as the virtual device metafile. The VDM, it is hoped, will be a hardware-independent data structure for storing all the information about a graphics file. This will enable the file to be transported and used by any device.

The three-dimensional functions defined in PHIGS rely heavily on those defined for Core. In fact, PHIGS functions are called elements and tend to be at a higher conceptual level than GKS primitives. This is a good thing, given the complexity of the transformation and viewpoint definitions.

To date, PHIGS has not appeared in the form of any commercial product, but that may change soon. Lack of commercialization is due mostly to the fact that it was defined relatively recently and that it has stopped at a functional specification. PHIGS does not now have the language bindings and calling definitions that have recently made GKS a usable model, if not yet an official standard.

Virtual device interface

Even though GKS and PHIGS seem to have a long way to go, another equally important standards issue is not nearly as close to resolution. This is the so-called virtual device interface, which has just appeared as a new working item in ANSI and ISO. VDI is essentially a definition by which a set of coordinates describing a picture can be made into an output to some idealized physical device.



*North American Presentation-Level Protocol Syntax

In the configuration of the GKS products by Graphic Software Systems (GSS), an application can either use the GKS kernel and interfaces or talk directly to the drivers via the prescribed virtual device interface (VDI) standard bindings.

This ideal output is then read by a real device driver to drive a specific display or plotter. The idea is, once a picture is transmitted through the VDI, the device driver is the only software that needs to be modified to adapt the picture output to a new graphics device.

At this point, though, no standard has been accepted for a VDI. Two companies have produced virtual device interfaces—Visual Engineering and Graphic Software Systems (Wilsonville, Ore). The GSS VDI is the one adapted by IBM for use with PC DOS. The GSS VDI—more properly, the language bindings that tie the application to the driver in accordance with the VDI definition—is a separate entity. Thus, it could be

used with different kinds of operating systems.

Because it is aiming at the Unix world alone, Visual Engineering has embedded VDI into its GKS. When working within a single operating system, this makes sense because applications languages call the operating system that passes standard parameters through its built-in VDI. To adapt a new peripheral to the Unix GKS world requires only the modification or writing of the device driver.

Because VDI is an interface definition, a trade-off exists between supporting the standard by translation in software and not supporting the standard and writing a program to access a given device directly. The trade-off is speed. Even IBM bypassed its own

VDI definition (developed by GSS) in the interests of speed and wrote directly to the hardware when designing the Paint program for the PC Jr.

Since then, Digital Research (Pacific Grove, Calif) has developed a raster VDI as the basis for its Graphics Environment Manager. The GEM is a single-tasking, window-based applications interface for personal computers. Tom Byers, product marketing manager at Digital Research, says that personal computers require speed as well as portability of applications. He claims, therefore, both a bit-mapped raster version of VDI and a standard for window environments are needed.

The Digital Research VDI is compatible at the call level with the IBM VDI Controller, but has added such raster operations as raster fonts. Fonts provide an example of how a raster-oriented interface differs from the vector-oriented one. As a character is enlarged, the device must increase the number of strokes (or raster scans) needed to keep it totally opaque. Unless this is done by higher level routines with the vector VDI, the area fill would open up. The drawing would be slower in any event. Digital Research is adamant that users of personal computers will not wait for an area to fill so they can get on with their task.

Virtual device metafile

GKS and PHIGS are concerned with creating pictures, VDI with interfacing the pictures to graphic devices, and the virtual device metafile is the standard proposed to handle transfer and storage of picture description information. Since the VDM cannot know what kind of device or devices will eventually use the picture information, it must be able to contain all possible picture elements in terms of the combined attributes of all current device technology.

In order to use the VDM, a system must support a VDM generator or driver (which places the information into storage in the defined standard format) and a VDM interpreter (which reads the data and turns it back into the actual GKS primitives for output to a device). Of course, the main problem in arriving at a

standard for the VDM is determining how to compress the data for economical storage and allowing for future device capabilities.

Other standards

GKS, VDI, and VDM comprise a family of proposed graphics standards, with PHIGS as a possible addition. If adopted, a PHIGS extension to the GKS efforts will have to be adapted to fit smoothly into the overall structure of the graphics family. Though it will take some time, there seems no doubt that this family will become a system of international standards. But it will not exist alone or displace other developments.

One standard that is likely to coexist outside this family is the North American Presentation-Level Protocol Syntax. NAPLPS is a standard that is evolving to meet a need that exists within an existing media technology, namely the telecommunication system. It is, in essence, a text and graphics transmission interface requiring devices with enough local intelligence to process a NAPLPS data stream.

NAPLPS has its own set of primitives and attributes called a picture description instruction set. PDI is intended for narrow bandwidth transmission environments, primarily teletext and videotex terminals. It is so well defined, however, that it is attracting attention for other low cost applications.

Another attractive feature is NAPLPS's raster scan technique—although it is not nearly as versatile as the raster VDI proposed by Digital Research. How and when it may be incorporated into the greater GKS family of standards efforts, or at least have interfaces defined between the two, will probably depend on market pressure. At present, Videotext, at least in the United States, is not moving very rapidly. Since NAPLPS is designed specifically for the needs of telephone transmission, wider acceptance of Videotext will be needed to bring NAPLPS under the roof of the GKS family.

In addition, the force of *de facto* standards will continue for a long time. Andrew Davis, graphic software marketing manager at Tektronix,

stated that although his company is fully participating in the ANSI standards efforts, it has an enormous commitment to customers using the Core-based products. So, not only will Core-based systems be around for a long while, new and useful applications will continue to be developed for that existing base.

There is also some disparity between the American effort towards standards being carried on by the ANSI X3H3 committee and the ISO's efforts. Some American standards may be declared before international ones and there may be slight and subtle differences between them. The ANSI version of GKS, for instance will make a more complete effort at installation independence than will the ISO version, but it is generally agreed that the differences are so minor that they will not cause much trouble.

The outlook for graphics standards is for a lot more work, but the efforts are taking shape in a way that may change the nature of the graphics swamp. Instead of occasional firm patches, we may eventually have a large amount of well-mapped solid ground. Then only a few adventurers, whose needs and market interests compel them, will venture off the solid ground—at their own peril.

—Tom Williams,
West Coast Managing Editor

SYSTEM TECHNOLOGY
(continued on page 41)

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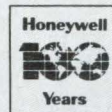
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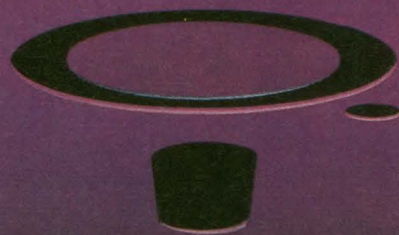
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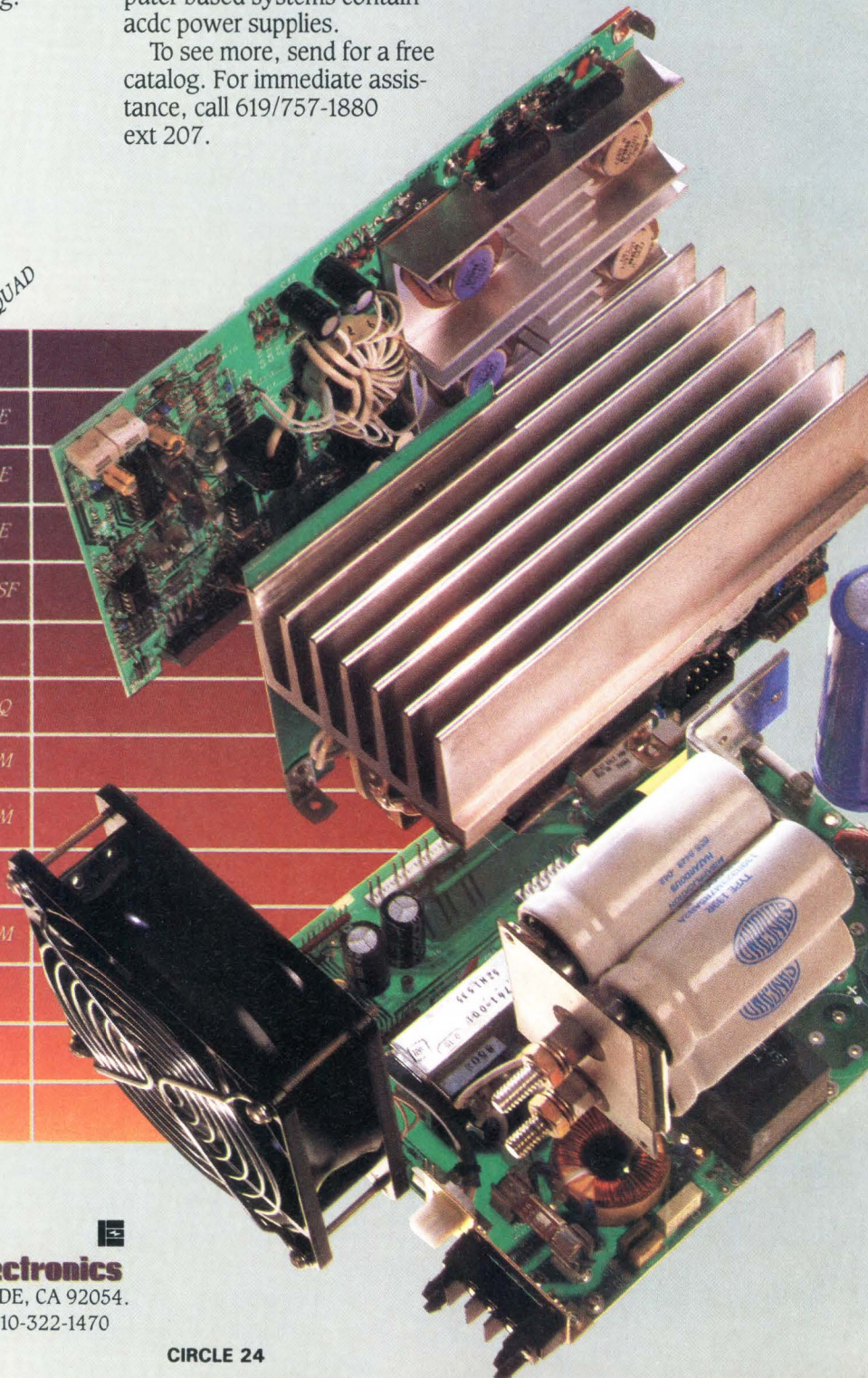
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Power supply vendors cut size and cost

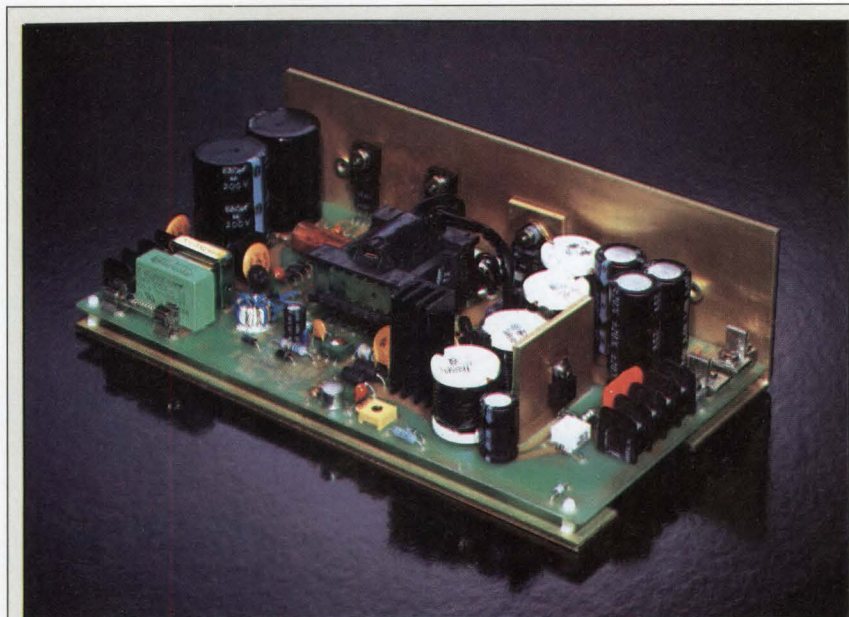
Power supply vendors are under increasing pressure to make their products more compact, reliable, and inexpensive. At the same time, tough international standards are forcing power supply designers to increase board spacing and add expensive components. As a result, an industry that has often been viewed as slow moving is becoming more innovative, and presenting a variety of choices for system designers.

European safety standards now require a 3750-Vac withstand voltage between inputs and outputs, and mandate larger creepage and clearance requirements than Underwriters' Labs. In addition, strict electromagnetic interference standards require bulky filters. Since anyone who wants to sell in Europe must meet international standards, power supply vendors are biting the bullet and designing them into most new power supplies.

"We're caught between a rock and a hard place," says Ken Piper, director of engineering for Standard Power (Anaheim, Calif). "On one hand, we have to get volume down. On the other hand, we have to meet safety requirements." This dilemma has forced switching power supply vendors to use a number of techniques—including surface-mount technology, custom hybrids, and power MOSFETs—to squeeze the maximum amount of well-regulated power into a smaller package.

Power supply manufacturers are also pursuing higher frequencies to bring about a significant reduction in power supply size. Higher frequencies are the only way to dramatically shrink bulky transformers, capacitors, and heat sinks. While most switching power supplies today are in the 20- to 50-kHz range, some 100-kHz models are available, with 200 kHz or more expected in the future.

Because more than 900 companies compete in the power supply business, a substantial amount of innovation can be expected over the next few years. And the standard product lines these companies offer are only the tip of the iceberg. Approximately



Todd Products uses surface-mount technology to shrink the size of its open-frame switchers. This 220-W, 60-kHz, multiple-output switcher is housed in a 5- x 9- x 2½-in. (12.7- x 22.86- x 6.35-in.) package.

75 percent of the power supply industry is captive, meaning that power supplies are made in-house by the manufacturers of the systems they power. In the noncaptive market, many supplies are designed on a custom basis. The most technologically advanced power supplies are likely to be unannounced products in the captive or custom markets.

Meeting tough specs

The West German association of electrotechnical engineers, the Verband Deutscher Elektrotechniker, is the driving force behind strict safety and emi standards. Any products that do not comply with the VDE can be banned from sale in Germany. Moreover, VDE standards are the basis for International Electrotechnical Commission standards, which most European countries follow.

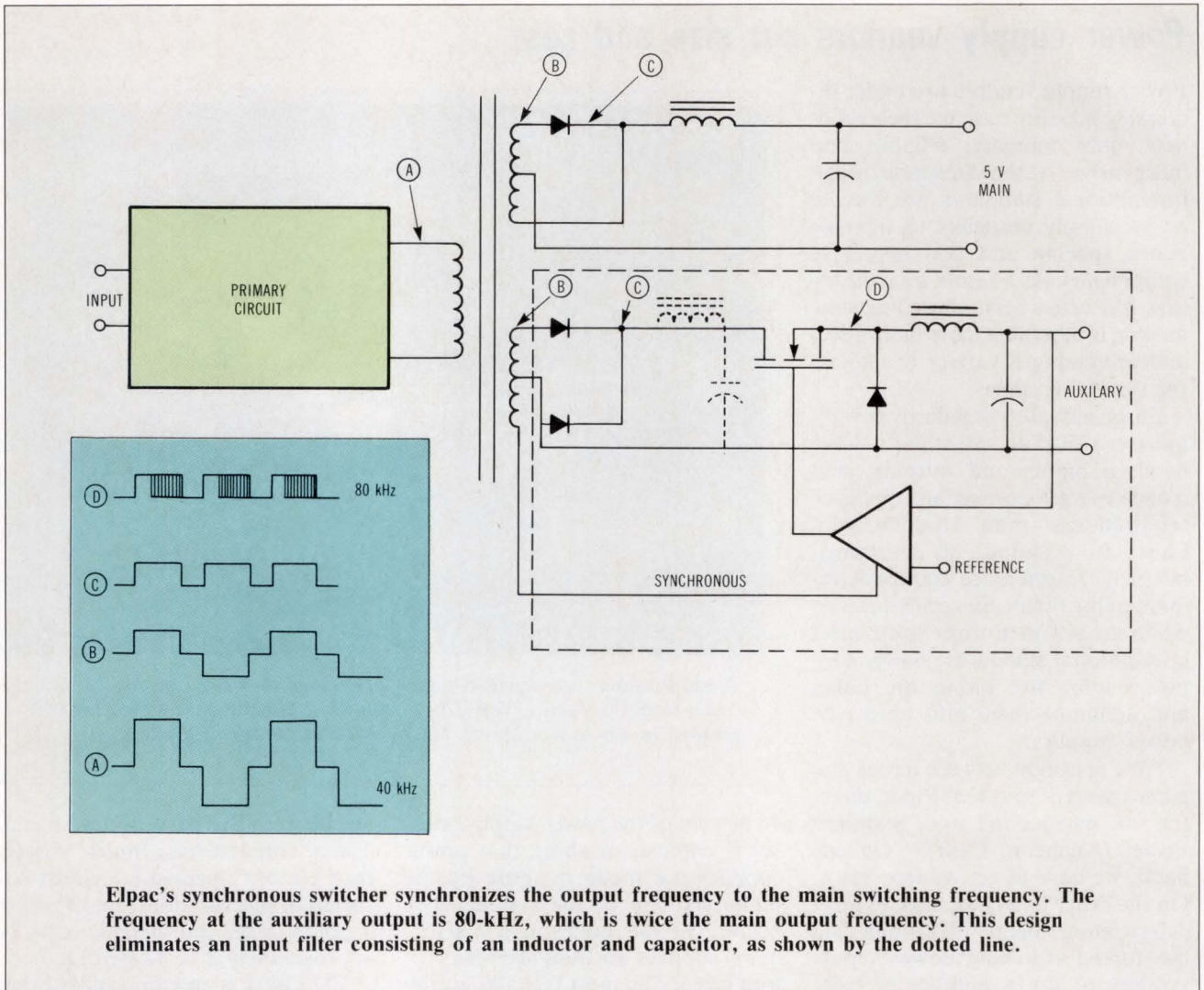
The IEC 380 safety standard is essentially equivalent to VDE 0806. To enforce a 3750-Vac withstand voltage between inputs and outputs, these standards require a minimum spacing of 8-mm between primary and secondary circuitry, with 3-mm creep-

age between live parts to dead metal. These requirements, much stricter than UL or Canadian Standards Association specifications, make power supplies larger and increase costs by approximately 8 to 12 percent.

VDE 0871 is an emi standard that is equivalent to recent U.S. Federal Communications Commission requirements. However, level "B" of VDE 0871, which took affect in January 1985, extends those requirements from 150 kHz down to 10 kHz. Since emi requirements are enforced on the subsystem rather than the power supply alone, how the power supply is installed can be as critical as adequate emi filtering.

VDE compliance "won't be a trend in the future, it will be an absolute necessity," says Ed Bennett, director of marketing for Boschert (Sunnyvale, Calif). "Even if a systems integrator is only targeting North America, at some point he'll want to sell overseas. If he doesn't have his specs up front, his chassis will have to be redesigned."

Several manufacturers, including Sierracin (Chatsworth, Calif), Conver



Elpac's synchronous switcher synchronizes the output frequency to the main switching frequency. The frequency at the auxiliary output is 80-kHz, which is twice the main output frequency. This design eliminates an input filter consisting of an inductor and capacitor, as shown by the dotted line.

(Cupertino, Calif), Power-One (Cam-arillo, Calif), and Switching Systems International (Orange, Calif) are obtaining VDE safety certification on their standard product lines. Certification is not strictly necessary, but it simplifies approval of the final product. Most manufacturers now have product lines that are "designed to meet" VDE and IEC specifications, although many manufacturers cannot yet meet level B of the VDE 0871 specification.

Lambda Electronics (Melville, NY), the largest manufacturer of standard power supplies, tailors its designs for the country of use. Thus, domestic power supplies meet UL and CSA requirements only, while supplies destined for Europe meet VDE and IEC. According to Lambda's marketing vice president, Irving Gut-

man, "If 70 percent of their business is domestic, they're better off buying two products."

Powertec (Chatsworth, Calif) has three "levels" of compliance with international safety standards, including one level that drops the Safety Extra Low Voltage portion of the VDE requirements. These supplies cannot be used in products going to Germany, but they might be acceptable elsewhere in Europe.

Making it smaller

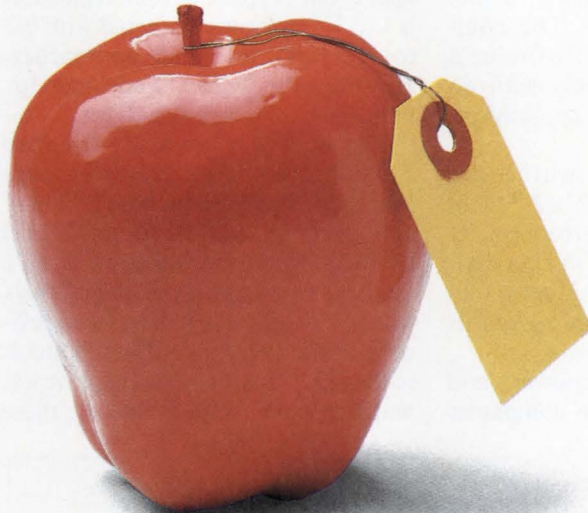
Since VDE and IEC specifications tend to make power supplies larger, and the computer industry needs power supplies that are compact, vendors are going back to the drawing boards to increase their power densities. While some manufacturers are using new technologies, others

are offering "no-frills" power supplies that cut out often unnecessary features.

Todd Products (Brentwood, NY) has a line of multiple-output switchers built with surface-mount technology. Todd's 220-W, 60-kHz, multiple-output switcher offers full VDE compatibility in a 5- x 9- x 2½-in. (12.7- x 22.86- x 6.35-cm) high package. Marketing vice president Frank Sposato says a size reduction of about 15 percent can be obtained from surface-mount technology.

Boschert has packaged its low level control circuitry in a custom hybrid. Lambda's "custom monolithic" puts the equivalent of 40 or 50 components on a single chip. Zenith (Glenview, Ill), a high volume custom supplier, has its own custom hybrid facility for power supplies.

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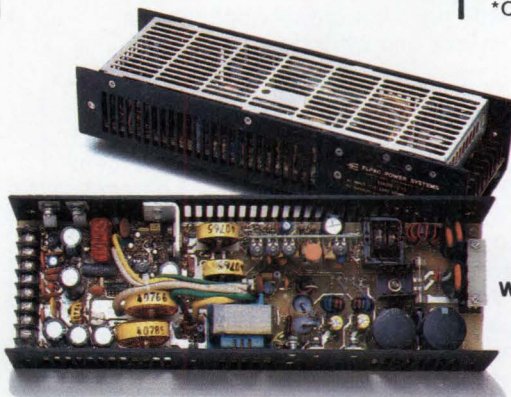
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Power General (Canton, Mass) offers what it calls the "world's smallest" 40-W switchers in 3- x 5- x 1.8-in. (7.62- x 12.7- x 4.57-cm.) high packages. These VDE-compatible switchers provide single, triple, and quadruple outputs. The company achieves this size by offering a "bare-bones power supply with no bells and whistles," says applications manager Bob Butler.

A triple-output, 40-W switcher in a 3- x 5- x 1-in. (7.62- x 12.7- x 2.54-cm) high package has been introduced by Compower (San Jose, Calif), a division of Computer Products Inc. Miniaturized components make this Micro40 switcher smaller.

Power General, Compower, and Sierracin are among the companies

that use flyback converters to keep size and costs down. The flyback converter is noisier and less efficient than forward or push-pull converters, but it has a much lower cost and component count. Typical flyback regulation is 1 to 1.5 percent, compared with 0.2 to 1 percent for other approaches. However, the flyback is adequate for many low power applications.

The only way to really decrease size, many vendors say, is to increase the switching frequency. "These cute tricks with custom hybrids and surface-mount technology aren't really addressing the problem," says Matt Winston, marketing vice president at Conver. "You're still stuck with big transformers, capacitors, and heat sinks. With frequency, these

components will shrink." Higher frequency will also decrease output ripple and improve transient response times. However, an increase in frequency does not translate into a linear decrease in power supply size. VDE creepage and clearance restrictions do not change, emi filtering is still needed, and heat must be dissipated across the supply. Multiple-output switchers will not shrink as much as single-output supplies.

KEC Electronics (Torrance, Calif) provides an example of what one might expect from a fourfold increase in frequency. KEC's single-output, 55-W, 25-kHz switcher is 1.93- x 8.8- x 3.94-in. (4.9- x 22.35- x 10.01-cm) high. The company's enclosed single-output, 60-W, 100-kHz switcher is 1.73- x 6.65- x 3.94-in. (4.39- x 16.89- x 10.01-cm) high. This translates into about a 32 percent decrease in volume, plus a slight increase in power.

The next breakthrough in power supplies may be frequencies of 1 MHz or more. To get there, capacitors and transformers will require radical redesign. In theory, a 10-MHz switcher could pack 50-W of power into a single 48-pin DIP—a completely monolithic power supply.

New components

For some time, semiconductor companies have been pushing power MOSFETs as the way to provide higher frequencies, and thus reduce the size of power supplies. Although bipolar transistors can be used as switching devices, anything beyond 100 kHz requires MOSFETs. In addition, MOSFETs can reduce the number of magnetic components, minimize switching losses, and improve efficiency.

However, most power supply vendors say MOSFETs are not yet cost effective. High on-resistance (which generates heat) and relative sensitivity to reverse voltage spikes have limited the use of MOSFETs in the past. The technology and the price are improving, and most vendors expect to use MOSFETs in the future.

ETA Power Systems (Signal Hill, Calif) uses MOSFETs in its 500- to 2000-W power supplies. Norm Weatherford, director of marketing and sales, says MOSFETs have

Why switchers are taking over the market

Switching power supplies use a high speed switching element to regulate voltage through pulse-width modulation. More lightweight, compact, and efficient than the older linear supplies, switchers have become the technology of choice for most computer system applications. The market split between switchers and linears is now about half and half; by 1990, switchers are expected to grab 90 percent of the computer power supply market.

With the compactness demanded by today's computer market, it is easy to see why switching power supplies are favored. A switcher typically weighs one-quarter and occupies one-third the volume of comparable linears. While a linear power supply is about 40 percent efficient in terms of input power to output power, switchers can achieve 70 percent efficiency. Switchers are now cost-effective down to about 50-W.

However, the linear market is not about to disappear. Linears have much better line and load regulation, and lower output ripple and noise. Such tight regulation is rarely necessary for digital circuitry. In the future, the linear market will be confined to such areas as sensitive analog circuitry and industrial process control applications.

Many engineers have been uncomfortable about switchers in the past, but improving reliability is erasing most of these concerns. Still, some vendors say engineers chronically overspecify switchers, as a holdover from linear power supply days. They ask for circuitry that was necessary for linears, but generally is not needed for switchers, such as foldback current limiting. They may also specify more ripple and noise regulation than they really need for digital applications.

Typical specifications for linears and switchers are:

Specification	Linear	Switcher
Line regulation	0.02 to 0.05 percent	0.05 to 0.1 percent
Load regulation	0.02 to 0.1 percent	0.1 to 1.0 percent
Output ripple	0.5 to 2 mV rms	25 to 100 mV p-p
Input voltage range	± 10 percent	± 20 percent
Efficiency	40 to 55 percent	60 to 80 percent
Power density	0.5 W/in. ³	2.3 W/in. ³
Transient recovery	50 μs	300 μs
Holdup time	2 ms	32 ms

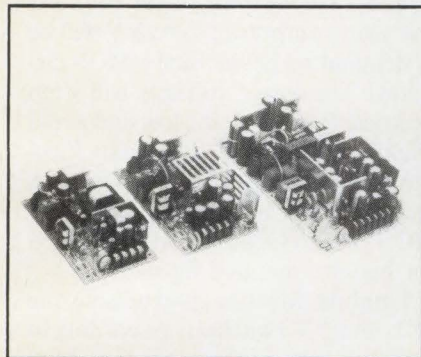
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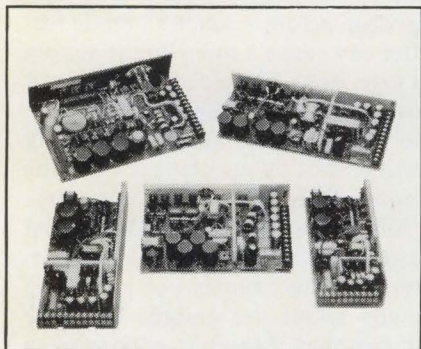
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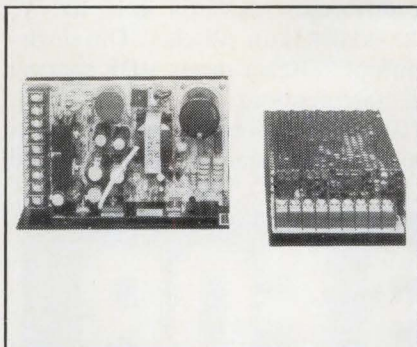
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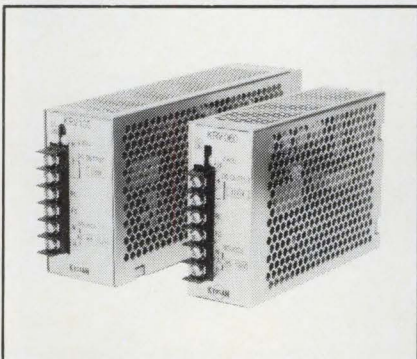


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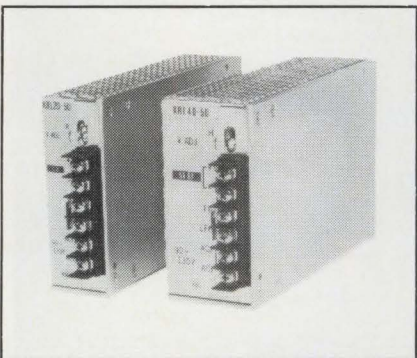
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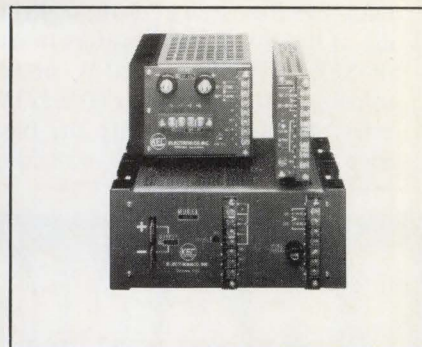
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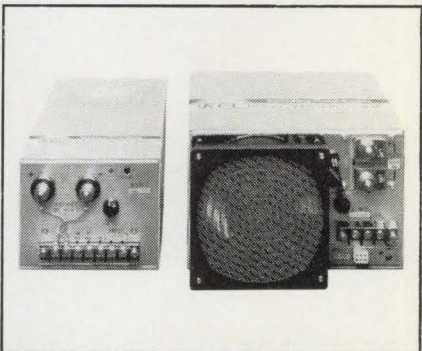
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reduced the component count significantly and allowed the supplies to run 12 to 15 °F cooler than competing units. LH Research (Tustin, Calif) is one of the first manufacturers to use MOSFETs in 50- to 120-W power supplies. In the company's 60 kHz IM series, MOSFETs simplify the base drive circuitry and cut switching

losses, according to vice president of technology Chandra Mehta.

ACDC Electronics (Oceanside, Calif) uses a MOSFET in its 100-W, 100-kHz RH101 switcher. This single-output switcher meets VDE spacing requirements in a 4- x 8- x 2.2-in. (10.16- x 20.32- x 5.59-cm) high package. Space savings are also provided

by U-shaped construction and a double-sided printed circuit board. At \$172, this supply is aimed at a highend scientific and business computer market.

Other components that could shrink power supplies are chips that integrate logic and power devices. Generically called smartpower, these chips are manufactured by such companies as Motorola (Phoenix, Ariz) and Siliconix (Santa Clara, Calif). At a recent power sources conference, Siliconix representatives described how a smartpower IC could integrate the main power switch, current sensing, startup circuit, and all standard controls in a low power telecommunication supply.

Dropping the voltage

Most switching power supplies have 5- and 12-V outputs. Over the next few years, outputs of 2- to 3-V will be in demand to power dense MOS circuitry. The lower voltages will keep electrical field strengths low and avoid reliability problems. The Joint Electron Devices Engineering Council has recommended a 3.3-V guideline for MOS circuitry and a 2.8-V standard for battery-operated devices.

Lambda now has an extensive line of 2- and 3-V switchers. According to Irving Gutman, there has not been much action in the 3-V area because "there's not enough VLSI out yet." However, considerable demand exists for 2-V supplies to power ECL circuitry, Gutman says.

Rectifier losses are a big problem with low voltage supplies. The voltage drop across a Schottky diode rectifier can cause a low voltage supply to lose 20 to 30 percent of its input power. Synchronous rectifiers reduce the voltage drop, and consequently rectifier loss, by switching at the same frequency as the driver circuitry.

Siliconix is working with selected customers on a MOSFET synchronous rectifier, but is not providing details about the design. Unitrode (Watertown, Mass) is marketing a specialized bipolar transistor called BISYN that can be used as a synchronous rectifier. The BISYN is three times slower than a MOSFET, but according to designer Raoji Patel, it controls switching losses better and

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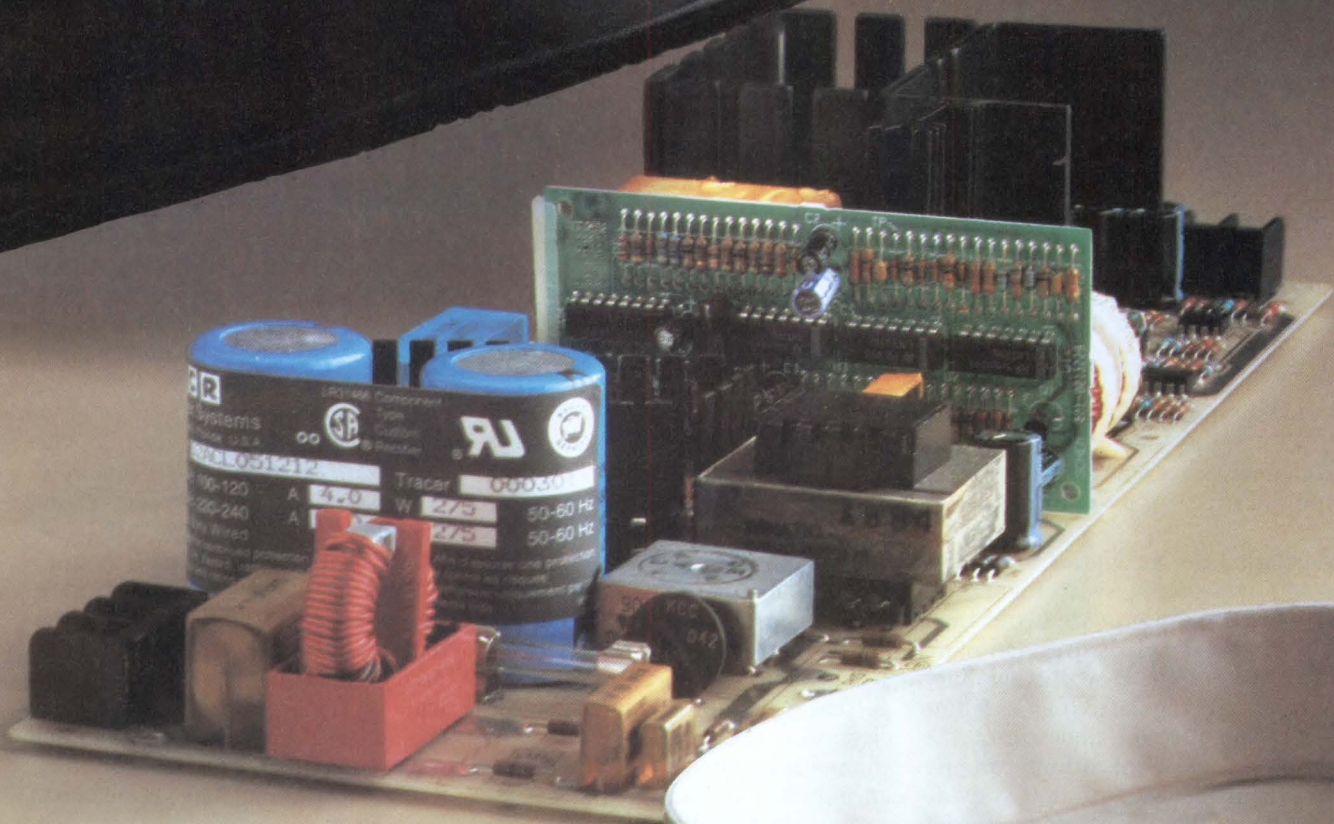
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Power Systems

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CIRCLE 35



Higher frequency reduces the size of this 100-kHz, 100-W, single-output switcher from ACDC Electronics. This 4- x 8- x 2.2-in. (10.16- x 20.32- x 5.59-cm) supply is one of the first on the market to use power MOSFETs.

is much more cost effective. The BISYN boasts low on-resistance and a capability to block both positive and negative input voltages.

Regulating the auxiliaries

Multiple-output switching power supplies usually provide better than 1-percent line and load regulation on the main output. How the auxiliary outputs are regulated has a major impact on the cost and size of the supply. Some applications can use semiregulated outputs that provide tight line regulation but no load regulation. Such outputs can be used for low power MOS memories, motor drives, relays, or any application that can tolerate a ± 7 percent output voltage change.

Linear post regulators provide tight regulation, but are bulky and relatively inefficient. Switch-mode regulation increases efficiency (a measurement of the amount of power dissipated by the output) to about 75 percent. Magnetic amplifiers reduce the size of the power supply, and provide efficiencies of up to 90 percent on auxiliary outputs. However, the technology is difficult, and Elpac (Santa Ana, Calif) and Conver are

among the few companies that are using it.

Elpac has introduced a "synchronous switcher" that uses synchronous pulse-width modulation on auxiliary outputs. This technique synchronizes the output frequency to the main switching frequency. Designed primarily for disk drive applications, the synchronous switcher provides 0.1-percent regulation at 90-percent efficiency on the auxiliary output. It eliminates an input filter consisting of an inductor and capacitor.

According to Walt Nareshni, vice-president of engineering, the synchronous switcher is about 25 percent smaller than competing units that provide similar regulation. The auxiliary output frequency is double the main frequency; Elpac's EDS135 dual-output, 135-W switcher provides 40 kHz on the 5-V main output, and 80-kHz on the 12-V auxiliary output.

The bottom line

The decision to purchase a power supply generally comes down to one of two factors: cost or reliability. The cost per watt of switching power supplies is steadily decreasing, and many customers are turning to standard

product lines to avoid the time and expense of custom designs.

Vendors caution that dollars per watt should not be the only criterion for selecting a power supply. "I think there's some lowering of cost at the expense of quality," says Boschert's Ed Bennett. "In the future, we may have some real problems with cheap power supplies."

On the other hand, many vendors complain that engineers overload power supplies with specifications, adding unnecessarily to the cost and size. Areas often specified to excess include ripple and noise, over-voltage and over-current protection, and output power. And such "bells and whistles" as remote inhibit, power fail or power good outputs, and current monitors may not be needed.

Reliability of switching power supplies has increased dramatically, and many manufacturers quote high mean time between failure figures. Buyers should be aware that MTBF is almost always a theoretical value, calculated from MIL-HDBK-217. MTBF can be calculated from a parts count or a worst-case stress analysis. The methods provide very different results. For example, the parts count method will favor a supply with fewer components, even if it runs hotter.

System designers who specify power supplies should research the market thoroughly, and see if a standard product line can solve their problem. In any case, the power supply should be specified early in the design cycle, and only features that are absolutely necessary should be included. With so many vendors in the power supply business, buyers can find the best possible combination of size, regulation, cost, reliability, and conformance to international standards.

—Richard Goering,
Field Editor
SYSTEM TECHNOLOGY
(continued on page 59)

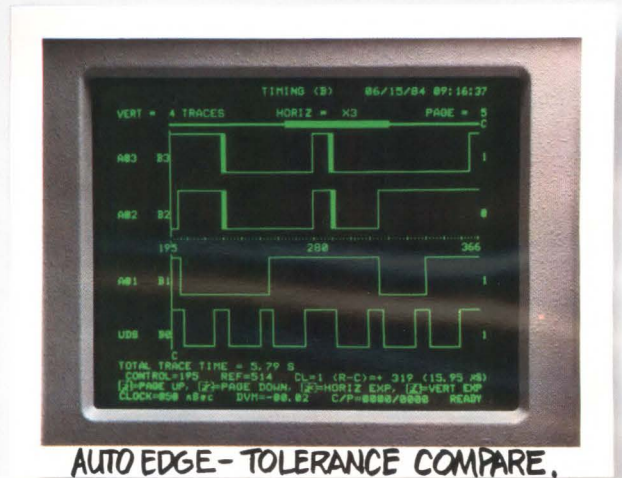
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Take a quick look through these pages. Notice anything unusual? Anything you might not have suspected appearing on these pages of Gould advertising?

If you said something like, "Wow, I didn't know Gould made that many logic analyzers," you've got sharp eyes.

But if you figured out, that in each case, the Gould analyzer is helping a senior design engineer slug it out with the toughest, nastiest, most frustrating logic problems, you really know your stuff.

Because that's what makes a Gould a Gould.

Consider, for example, the K105-D



ONE-STEP NOISE MARGIN ANALYSIS.

microprocessor analyzer. It makes short work of debugging even long programs. Because it gives you the most sophisticated triggering in its class. Which means you can capture the signals you need to capture. Go with the flow, if you will. And isolate errors in a lot less time, with a lot less frustration.

Here's another reason there's nothing like a Gould. Intermittent failures in discrete logic. Before you pull your hair out, pull out the K205-D. Among other life-savers, it has an Auto Save mode that lets you set up and go home. The analyzer will track and record anything out of the ordinary. Compare it to a

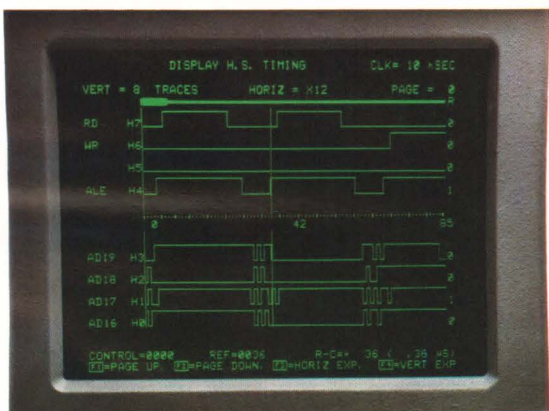
pattern you design (so you don't waste time on unwanted compares). Even add a time stamp. All at very high speed.

And while we're on the subject of speed, consider the K500. It's the analyzer high-speed mainframe and super-mini designers need. Because it has the clockrate (500MHz) and active probe bandwidth to guarantee signal fidelity. What's more, you get individual high frequency probes so you can stretch across large ECL boards and get to the signals you want to analyze.

Finally, there's our behind-the-scenes hero: the T-12 communicator. It lets field service organizations keep their best brains close to



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5 ns GLITCH CAPTURE.

home. With a T-12 and a Gould logic analyzer (in particular the K100-D), at each end of a standard phone line, remote diagnostics are fast, easy and economical.

If you're suspicious by nature, find out why so many designers won't settle for a less competent analyzer. Call your Gould representative today. Get all the latest news about the full line of Gould logic analyzers. Along with some very revealing pictures.

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Engineer disappears without a trace.

Tragic. A fine, upstanding young engineer gone. No more project. No more work. All because he used a logic analyzer that just couldn't cut it.

So rather than let a bug come back to haunt the program, the senior engineer took out his trusty K105-D and took over. End of bug. End of story. Beginning of a beautiful software/hardware relationship.

Of course, we've left a few details out of the above plot summary.

For instance, there was the Trace Control™ incident. It let the problem-solver find out exactly where the bug was. And why it happened.

Trace Control is the most sophisticated triggering scheme around. It let our hero set more triggering conditions and walk

away.

The K105-D followed every turn and loop in the program, then recorded only what needed to be seen. It captured even widely separated slices of code, ignoring what was right and zooming in on what was wrong. And saved an astonishing amount of time.

Of course, the solution to the language problem also helped bring about the bug's demise. The K105-D speaks assembly.



So triggering conditions are set in mnemonics. Not complex object code. Special disassembly modules for many popular microprocessors including the 68000, 8086, 8080, 8085A, and Z80® meant the K105-D was the only logic analyzer needed. Especially when its 100 MHz high speed link was used to see how timing affected software execution.

If you'd like to rid yourself of the toughest, most pesky bugs software has to offer, call your Gould representative today. He'll appear with the whole story.



Designer saved by faults alarm.

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It was a dark and stormy night. A random, intermittent glitch was wreaking havoc with the top designer's hardware team. With no time left for sympathy, the top designer took out his K205-D and sent it bug hunting.

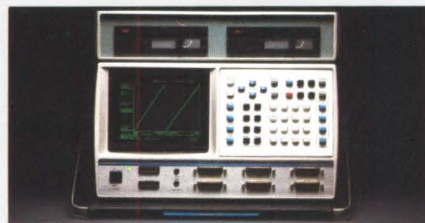
And in the middle of another dark night, the fault was located and captured. And held until the top designer came to work the next sunny morning.

The cure started with the K205's no-compromise, no-mercy attitude toward faults. It ran at 100MHz across all 48 channels. So there was no double-probing. It used its glitch mode on all 48 channels without requiring probes to be reconnected. It used Trace Control™ to set 16 independent



triggering levels. It used its unique tolerance compare capability (which compared timing sequences to stored references) to eliminate sampling error differences inherent in asynchronous analysis.

And it used its user-definable



disassembler (UDD, if you need to catch your breath) to easily translate binary signal flow into simple mnemonics. Which, by the way, was connected through its user-definable interface. Without a hitch.

When the fault was found, the K205 automatically stored the data. And let the top designer get right to work solving the problem.

Of course, even if you don't have need of the most sophisticated triggering in the business you can still save yourself a lot of time and frustration by using the K205 merely for its unrivaled combination of speed and power. Either way call your Gould representative today.



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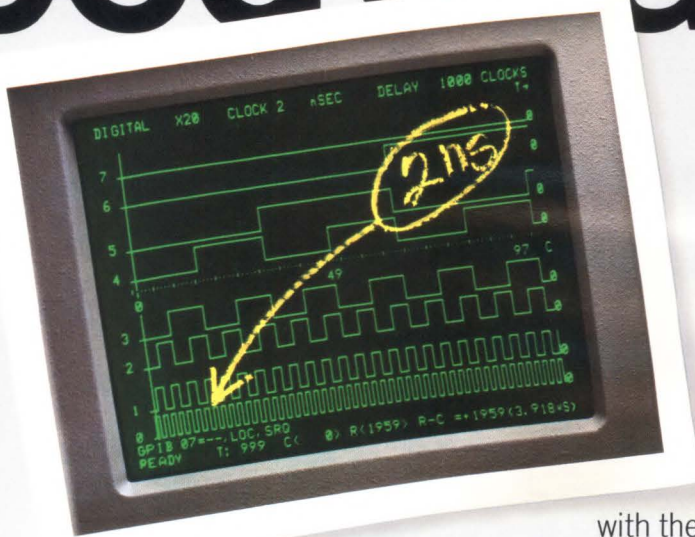
Glitch captured after high speed chase.

© 1985 Gould Inc.

It almost got away. But because someone made the smart decision to use the Gould K500, one more glitch bit the dust.

Speed was essential. So all eight channels of the K500 were racing along at 500MHz. Resolution also had to be tight enough to narrow down the escape routes. Two nanoseconds brought things under control.

And, of course, a lot of territory had to be covered. So the K500's individual hybrid probes made the job easy. Their 900MHz frequency response also assured accurate signal capture and unmatched signal



clarity. So the innocent were left alone. And the guilty glitch was discovered.

Sounds simple, but a lot of power was directed at this particular chase. The K500's Search



Mode was used to examine data in the vicinity of particular loop addresses. Random glitches (some guilty, some not) were found and identified

with the Compare Mode — a very fast method for defining a pattern and checking data fields against it. Finally, some very flexible recording and display talents were called in to support the complex timing and state analyses which led to the ultimate capture.

If you'd like a complete run-down that will help you in your own high speed chase, call your Gould representative today. Before another glitch gets away.



GOULD
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Higher intelligence now a remote possibility.

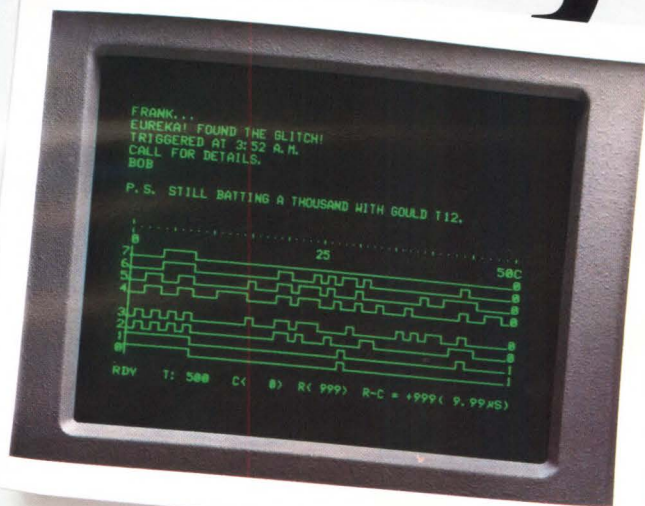
Long distance is now better than being there. So long as your field service organization is using the Gould T-12 Communicator.

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Finally, let your top technical specialists solve those really tough problems from the comfort of their offices.

That's the how. Now here's the why. Reduced mean down time (MDT) by 40%. Slashed travel budgets by 50%. Increased



productivity in the home office. Fewer board swaps. Less run-around-related burn-out and talent loss. Happy, satisfied customers.



The T-12/K100-D combination also provides convenient baby-sitting, recording patiently while everyone sleeps. In fact, if you're searching for intermittent, random failures, this team is perfect. The T-12 has its own error-checking electronics so bits aren't lost. You can even set up a monitor situation that auto dials your central service facility when the fault occurs. Leaves an on-screen message on your analyzer. And transfers all the recorded data on command.

To make this remote possibility come true, call your Gould representative today. You'll see that the T-12 provides an extraordinary way to communicate with a higher intelligence.



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Concurrent computers make scientific computing affordable

A major step toward reducing the cost of scientific computing is expected to take place this June. At that time, Intel (Santa Clara, Calif) will introduce its iPSC family, the first commercially available group of concurrent computers. Price tags will be far lower than those on currently available supercomputers.

The combination of efficient architecture and powerful VLSI chips will result in \$150,000 to \$520,000 units that have peak performance of 2.5- to 10-million floating point instructions per second. Supercomputers, such as the Cray models, can perform 100 times faster, but their prices exceed \$1 million. And the Cray machines are not based on the concurrent architecture.

Intel's initial iPSC machines perform about 0.1 to 0.4 percent as fast as the Cray 1 at no more than one-tenth the cost. Reports from Cray 1 users cite a performance range typically at 10 to 35 MFLOPS on common problems. This translates into an

efficiency rate of about 5 to 20 percent of peak performance. By contrast, Intel claims that the iPSC operates between 80 and 99 percent of efficiency. Moreover, the iPSC family is 6 to 24 times as powerful as a VAX 11/780 (which costs about \$225,000).

The higher costs of supercomputers will be only one of the factors limiting their use, according to Ed Slaughter, general manager of Intel development operations in Hillsboro, Ore. "Conventional supercomputer architecture shows clear signs of reaching its theoretical performance limits within the next 5 to 10 years," says Slaughter. "Demand for performance in some application areas is typically 10 times, and more often 100 times, the projected limit of 3000 MFLOPS for current supercomputer architecture."

A common strategy for solving scientific problems is to divide the problem into blocks, process those blocks simultaneously, and recombine the partial results to derive a final

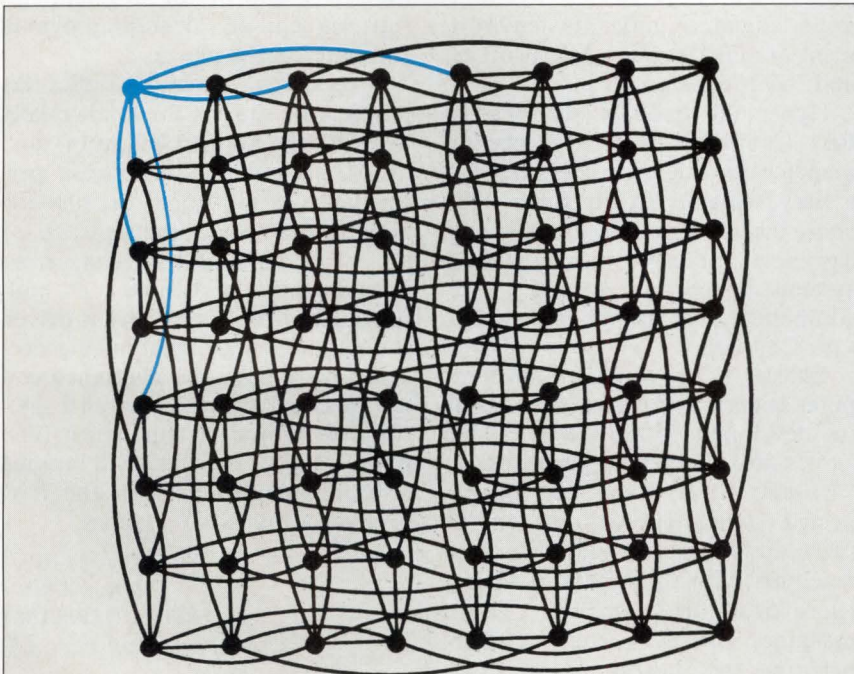
answer. Such concurrent computing usually requires an efficient parallel architecture with supercomputer performance. Many parallel architectures have been developed, but most are either paper designs or geared toward the university research environment (see "Parallelism makes strong bid for next generation computers," *Computer Design*, Sept 1984, page 104).

Hypercube architecture

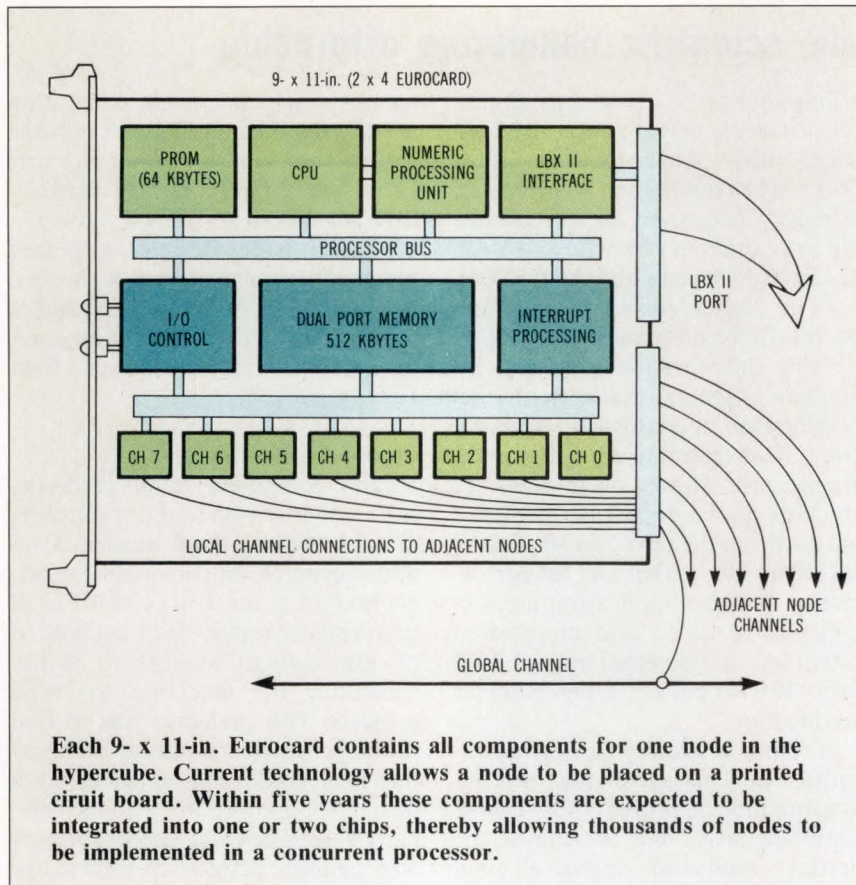
Intel concluded from predesign studies that scientists and researchers in both industry and academia require accessible and affordable supercomputers in the 1- to 100-MFLOP performance range. But they need to be low enough in cost to justify dedicating the machines to single projects. The challenge was to find the appropriate computer architecture to meet the requirement—and to match that architecture with the company's forte in VLSI microprocessor and memory design—to yield a low cost machine.

Final design of the iPSC is based on the hypercube architecture developed at the California Institute of Technology in Pasadena. Intel became familiar with that architecture in 1981 when it first donated 8086 and 8087 microprocessors for development of what is known as the Cosmic Cube. The company later collaborated with Cal Tech on many of the details of the machine, licensed the architecture from the university, and redesigned the computer around second generation parts—the 80286 and the accompanying 80287.

Hypercube architecture consists of tightly coupled processor/memory nodes (in the iPSC case, 32, 64, or maximum of 128) that work concurrently on parts of a large problem and coordinate their computations by sending messages to each other. In a 128-node system, each node is connected through bidirectional, asynchronous, point-to-point communication channels to eight other nodes. Together, these form a communications network that follows the plan of an eight-dimensional hypercube.



A hypercube connects $N = 2^n$ small computers, called nodes, through point-to-point communication channels. This two-dimensional projection is of a six-dimensional hypercube, or binary six-cube, which corresponds to a 64-node machine.



An operating system kernel in each node schedules and runs processes within the node, provides system calls for processes to send and receive messages, and routes the messages that flow through the node.

Each node in Intel's machines consists of an 80286 CPU, an 80287 floating point numeric processing unit, 512 kbytes of CMOS DRAMs and 64 kbytes of PROM. All this fits on a single 9- x 11-in. standard Eurocard. Another Intel chip, the 82586 LAN coprocessor, moves messages between nodes via dedicated point-to-point communications channels with integrated direct memory access to RAM on the associated node.

All nodes are connected via a global communications channel to the Cube Manager, an Intel 286/310 microcomputer running under the Xenix operating system. It supports both the programming environment and system management.

The Cube Manager consists of a 2-Mbyte memory, 40-Mbyte Winchester disk drive, and a 320-Kbyte floppy disk drive. Principal program-

ming languages under this environment are Fortran 286, Microsoft C, and the 286 Assembler.

Hypercube topology, according to Roy Coppinger, Intel's marketing manager for scientific computers, is a very scalable architecture. "We chose the hypercube because the user can expand to larger, more powerful systems as needs increase or VLSI-component technology improves," says Coppinger.

Charles Seitz, professor of computer science at Cal Tech and one of the developers of the Cosmic Cube agrees with Coppinger. He also says, "Cosmic Cube nodes can be expected to be integrated onto one or two chips within five years." Future machines with thousands of nodes, therefore, are feasible. These machines should be able to outperform the fastest uniprocessor systems for many demanding computer problems.

Intel expects to attract two types of users: scientists doing research and researchers developing application software. The basis for this expecta-

tion is that concurrent architectures effectively exploit the parallelism inherent in the physical structure of the computational problem.

Seitz presents a molecular dynamics application as an example. Diffusion of one group of molecules is observed through the medium of another group of molecules, such as salt dissolving in water. "Concurrent machines solve this kind of problem much faster and more efficiently than vector or array processors," says Seitz, "because concurrency exhibits properties that are fundamental aspects of nature. A concurrent machine can thus become an 'electrical' model of the physical system."

Vector and scalar are separate

In the diffusion problem, two components must be solved separately. One is a scalar portion of the calculations necessary to proceed through the simulation of the mixture enclosed in the vessel. The other is a vector portion that models the behavior of the molecules during diffusion. A vector or array processor takes care of the vector portion. But the scalar end of the problem still runs sequentially, degrading overall computer performance.

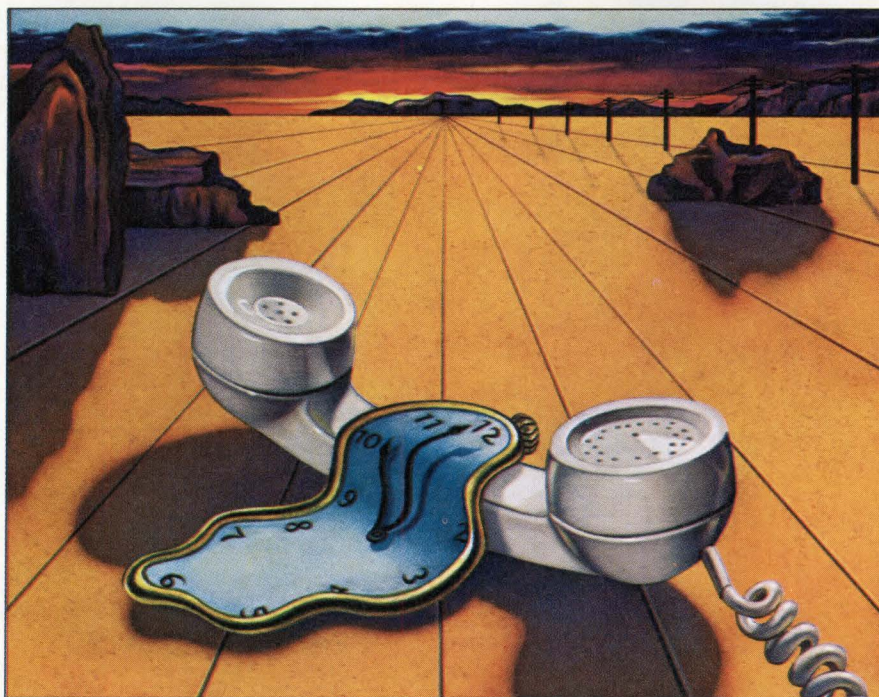
A concurrent machine handles this problem by sharing the load equally over a large number of processors. This keeps both vector and scalar performance proportional because the architecture mimics the structure of the problem itself. A concurrent machine can also handle such non-numerical problems as event-driven simulation and artificial intelligence, Seitz says. Finally, a concurrent architecture is well-suited for parallel algorithm development, for which Intel hopes its iPSC products will become a foundation to develop the next generation of Cosmic Cubes.

—Nicolas Mokhoff,
Senior Editor

SYSTEM TECHNOLOGY
(continued on page 65)

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.



“LATER” IS TOO LATE.

The window of opportunity in voice applications processing is wide open.

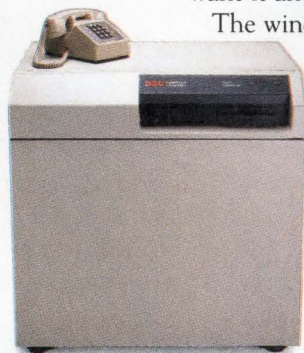
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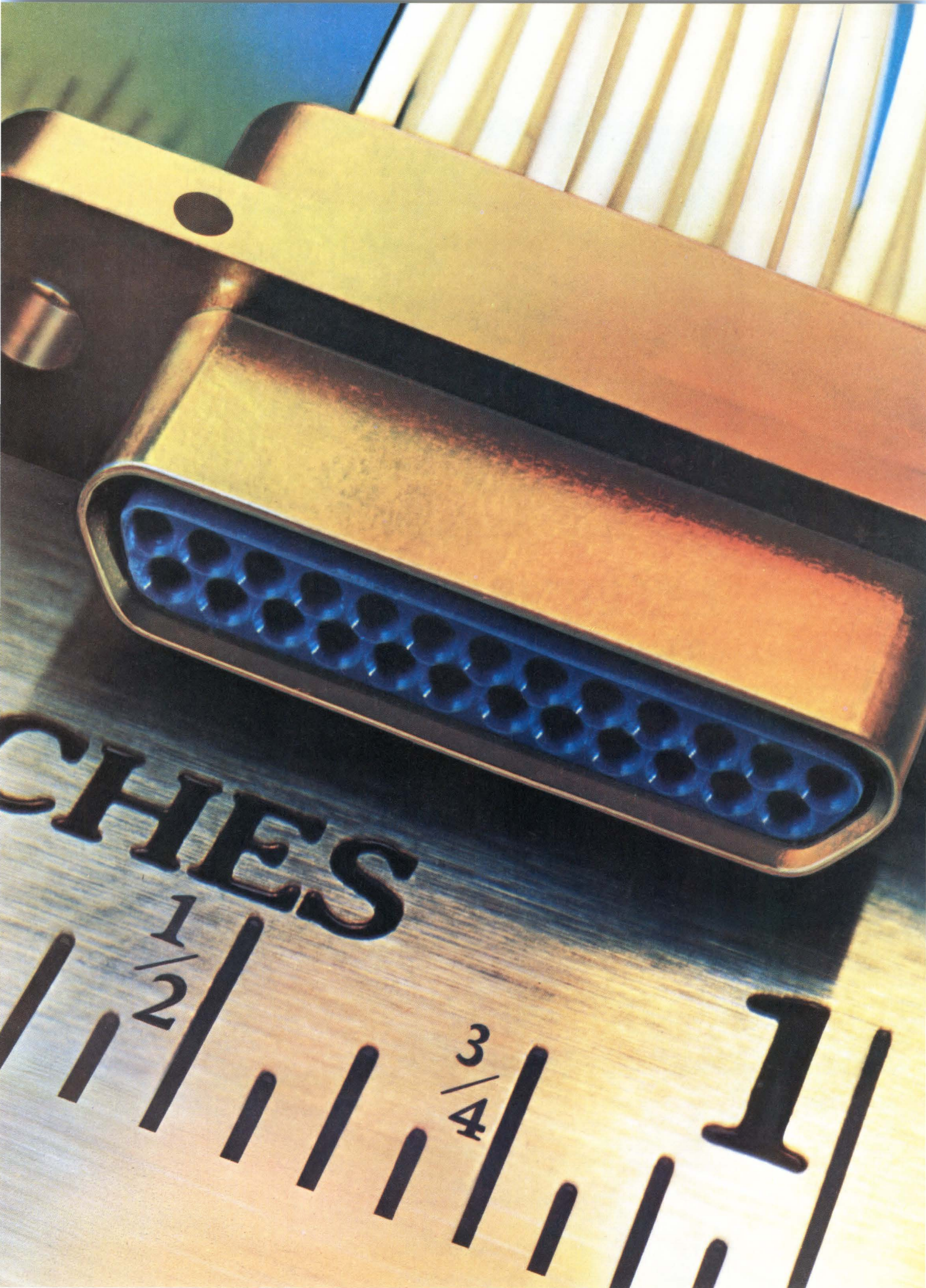
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AMP Micro Series 50.

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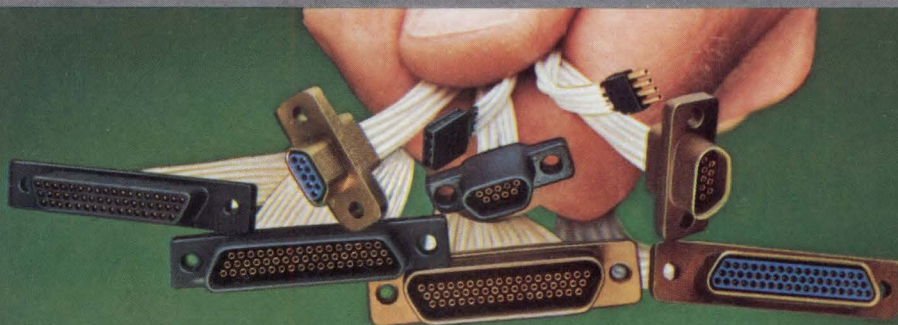
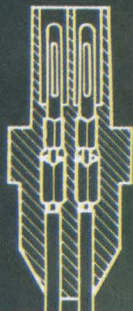
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AMP Interconnecting ideas



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14.4 TRELLIS

The UDS Trellis Supports OEMs At 14.4 kbps

UDS has applied the latest in trellis coding technology to a new OEM card modem for leased-line networks. It supports three coded data rates (14.4, 12, and 9.6 kbps), as well as uncoded traffic at 14.4 and 12 kbps. V.29 may also be specified.

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If your system is feeling the weight of a growing throughput requirement, support it with a UDS trellis coded modem. Specifications and prices are available from Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone 205/837-8100. Telex: 752602 UDS HTV. Inquiry hotline: 800/633-2252, ext. 370

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Languages promote parallel processing

Hardware designers now have two chips at their disposal for designing parallel systems. First released for nonmilitary use in 1984, NCR's Geometric Arithmetic Parallel Processor chip was the first true systolic processor chip to reach the general market. Inmos' T424 silicon transputer (announced over a year ago), will be available in sample quantities around the middle of this year.

When programming computer systems with numerous individual elements that process in parallel, at least two difficulties become apparent. While conventional von Neumann machines process data according to a list of serial instructions, parallel machines partition instructions and data among processing elements. The logic of a program—hard enough to decipher in a serial system—becomes much more complex in a parallel machine. Communication among independent processes or processing elements also becomes even more complicated.

Both these difficulties stem from the logical and physical configuration of the parallel computer. Without a high level language compiler to address some of these concerns, the programmer can become mired in hardware. Furthermore, there is no direct way of converting programs designed for serial execution to run efficiently on parallel computers.

High level language serves transputers

Fortunately for the engineer who has to program a system under development, the transputer was designed with high level languages in mind. The transputer has been optimized to execute Inmos' Occam language, which was created to program parallel computers. Thus, it offers an existing set of development tools. Meanwhile, NCR, with its hardware already on the market, is busy generating a set of software-development tools.

Paul Sullivan, director of Digital Signal Devices at NCR's Microelectronics Division, Fort Collins, Colo, feels NCR's hardware-first approach is fully justified. "Our chip is much easier to program than the trans-

Chip-level parallelism will cut supercomputer costs

Predictions that it will take years to compress parallel architectures onto one or two chips may prove conservative, since some semiconductor manufacturers have already cast parallel architectures in silicon.

They have done so on a limited scale and their success is far from proven, however. Inmos, whose announced transputer represents the most ambitious parallel-processing chip to date, has yet to deliver the chip in sample quantities, though the company claims its production is on schedule. If that claim holds true, computers designed around the transputer should soon rival Intel's iPSC series performance at a much lower price (see "Concurrent computers make scientific computing affordable," page 59).

The iPSC's performance works out to 78 thousand floating point operations per second, per node. Privately, Inmos has been showing block diagrams for double Eurocards with one, four, and eight transputers capable of 10, 40, and 80 million instructions per second on a double Eurocard. All but the 80-MIPS boards include external RAM; and each transputer has its own on-chip store of 4 Kbytes of RAM. Depending on the system configuration, each transputer board can be considered roughly equivalent to a node—one board—in the Intel system.

Performance figures circulated internally at Inmos indicate that a single T424 chip running at 10 MIPS can achieve 50 thousand to 60 thousand FLOPS in software. (That is using a yet-to-be announced floating point version of Occam.) Thus, each transputer board could achieve from 50 thousand FLOPS to just under 500 thousand FLOPS performance without the addition of hardware floating point.

Using a high speed floating point chip, such as the Weitek series, each T424 chip can perform 500 thousand FLOPS to 1 MFLOPS. That puts transputer boards using just one 10-MIPS T424 chip in the same performance range as Intel's iPSC boards. These transputer boards would have space for megabytes of RAM. While chip-maker Inmos will not be marketing such boards, it is safe to suppose someone will.

If the price and configuration of competitors' boards are pure speculation, the programming language choices available at present are clear. Although using Inmos's Occam does require programmers to learn a new language, it maps directly to the transputer architecture and could be implemented on the iPSC series.

Intel so far has chosen to keep using the languages to which most programmers are accustomed, particularly C and Fortran. Indeed, if Occam does not catch on, C may well turn out to be the most popular language for parallel programming. It has already succeeded Pascal as the language of choice for most nonmilitary projects.

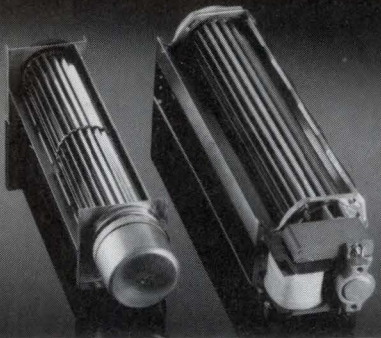
It is ironic that Intel, a semiconductor manufacturer, should introduce a parallel computer implemented at the board level. Intel's adaptation of its current technology to parallel computing is a major stride for the interim. Yet it seems to make more sense to approach parallel programming with a new set of tools designed specifically for the task. In that regard, Inmos's efforts to provide a parallel language and chips seem well aimed. They should lead to uncluttered systems that are economically programmed.

puter," he claims, because it is a single instruction, multiple data processor. It therefore uses one sequential stream of instructions. Sullivan sees software support as less important for the Geometric Arithmetic Parallel Processor (GAPP) chip than

for the Inmos (Colorado Springs, Colo) transputer. The GAPP chip, he adds, is oriented to working on two-dimensional arrays of data, such as images or matrices.

As Sullivan points out, the chips do not compete directly. They differ

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significantly in their design, programming, and applications. In contrast to the GAPP chip's single instruction, multiple data systolic architecture, Inmos' chip exemplifies the more complex multiple instruction, multiple data architecture. Despite its inherently greater complexity, this chip holds a promise of parallel processing that is readily programmed using Occam.

Occam is designed to overcome most of the obstacles presented by parallel processing. Wherever processes can clearly execute in parallel, the programmer can specify that they should. Yet the programmer need not worry about the physical configuration of the processor that will execute the code. Occam is a high level language that can run on a traditional von Neumann processor, such as the 68000, just as readily as on an array of transputers.

Since the language the transputer will execute has already been defined, designers can start building systems that will be tested on the Eurocard version of the transputer expected out the middle of this year. For those impatient to start with the software, Inmos' Occam Programming System is already available for the VAX/VMS.

New package

NCR's GAPP Simulator/Assembler package, currently in beta test, will be announced for release some time this month. The package consists of two utilities that run under the Unix operating system. The assembler translates GAPP instruction mnemonics and address specifications into object code for downloading into RAM. The simulator allows the user to execute GAPP programs. It also provides basic debugging facilities, such as the ability to examine GAPP RAM contents and view the state of processor element registers.

Users will eventually be able to write and test GAPP programs using the GAPP Evaluation Module. The module, currently scheduled for release in October, is a two-part system. The first part is a board for the IBM PC that contains a 12- x 12-GAPP array. The second is software that permits the user to program the GAPP array in a high level language,

and then interactively debug the resulting program.

The new language that NCR is introducing for the GAPP is called GAL—for GAPP Algorithm Language. GAL is a subset of C that supports all arithmetic, logical, and assignment operators that apply to integers. The language supports sub-routines and integer functions, as well as the If, If-Else, For, and While control statements.

Specifics of GAL

Besides these C-like aspects, GAL includes some features unique to GAL itself. Among these are a new variable type used to refer to sets of adjacent RAM locations within a processing element. The "image" variable defines such RAM locations by specifying a starting address and a number of bits. This is a bit-level analog to byte array structures in languages such as C.

A major difference occurs in the use of the image variable type. Since each instruction is executed by every processing element in the GAPP array, the GAPP environment is inherently two-dimensional—as is appropriate for image-processing applications. Image variables represent the third dimension, which contains attributes of the data array, or pixels. The most obvious use of image variables is to specify color or shades of gray.

The value for that processing element's pixel is stored in each processing element's RAM. That local value is referred to by the image variable. Image variables are defined:

```
image SCRATCH : 3 : 7 ;  
or image SCRATCH : 5 ;
```

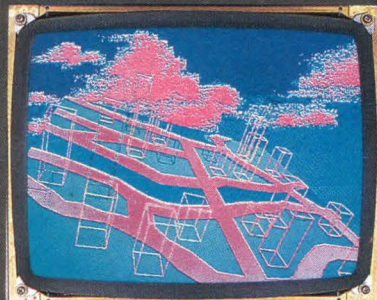
The first statement defines an image variable Scratch with 7 bits starting at address 3. The second statement defines the location of an image variable Scratch with 5 bits, but leaves the location up to the compiler. These image names can then be used in a manner similar to integers, and a programmer can define and call an image function.

Unlike GAL, Occam is not designed as a hardware-specific language. It is used less for hardware-specific variable types than for

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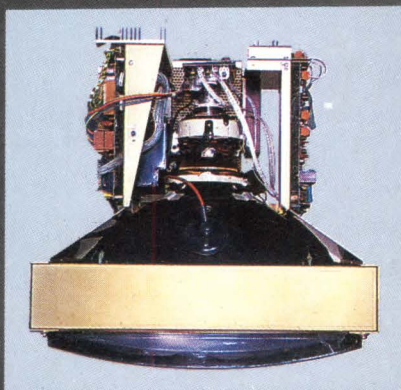
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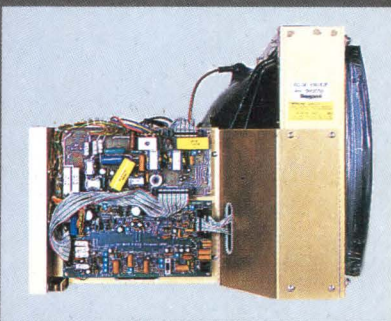
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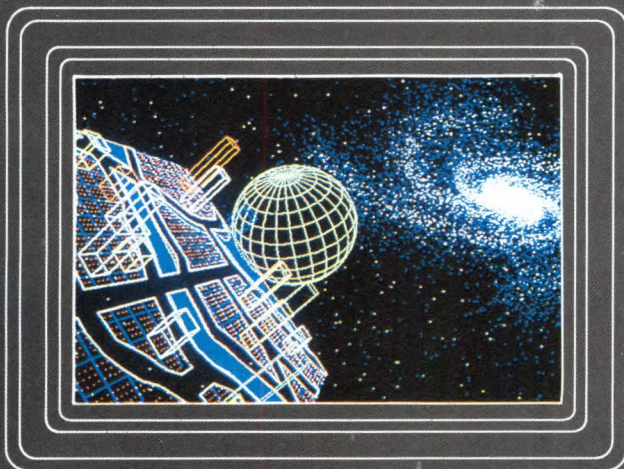
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dividing procedures into parallel processes. Occam includes interprocessor communication and the primitives for parallel processing.

A parallel procedure

A classic example of parallel processing is the multiplication of N pairs of numbers, all of which are known initially. This allows the numbers to be processed in parallel. Therefore, the entire process executes in the time required for the slowest multiplication. Such instances of parallelism use parallel processors in the most efficient way possible.

Such an operation can be programmed on the GAPP chip in GAL only if all the multiplicands were multiplied by the same multiplier. Thus, in applications that are not inherently systolic, the Occam/transputer combination provides a more hospitable environment. In purely systolic applications, such as image enhancement, the transputer's other capabilities might be wasted.

In practice, relatively few applications allow parallel processor to run at full efficiency. Sequential operations creep into all but the most inherently parallel procedures. For

this reason, Occam includes primitives for programming sequential operations simply.

Operations such as assignments and procedure calls are considered processes in Occam. While it supports procedures, Occam does not support functions or recursion. Procedures receive their arguments either as values or variable addresses. Variable address arguments permit the procedure to return a value to the calling process.

Future versions of Occam will support more general data types. But currently, Occam supports integers, arrays of integers, byte arrays, channels, and channel arrays. Channels are one-way streams of synchronized data that provide physical or logical connections between processes. A special case is the time channel, which provides each process access to a freely running clock. Thus, Occam supports the programming of processes that operate at specific times.

A real option for designers

At present, system designers have a real choice between the GAPP systolic chip designed for image processing (and similar applications) and the transputer designed for more general parallel tasks. With effective programming languages available for both processors, they can begin conceiving a new generation of computers to handle tasks that have resisted handling by previous systems.

While the GAPP chip represents a finished product for which the supporting software tools are being put in place, the transputer is the first in a related series of products. A link adapter that interfaces the transputer to other devices—including universal synchronous receiver/transmitters, DMA controllers, and other transputers—is planned as well. Cascadable hardware will be available for configuring diverse systems with applications that will include graphics, database, and scientific applications. Meanwhile, the current set of software tools will continue to evolve.

—William E. Suydam, Jr.
Senior Editor

Understanding Occam

Occam's syntax is best understood by example. Taking a multiplication example, N sets of numbers in parallel are to be multiplied. In Occam, the operation is expressed as follows:

```
PAR i = [0 FOR N]      [1]
  a[i] := b[i] * c[i]
```

If, however, the same instructions were to be executed on a conventional von Neumann computer, the operation would be expressed in Occam as a sequence:

```
SEQ i = [0 FOR N]      [2]
  a[i] := b[i] * c[i]
```

To divide the operation between two sequential computers, the operation could be specified:

```
PAR
  SEQ i = [0 FOR N/2]  [3]
    a[i] := b[i] * c[i]
  SEQ j = [N/2 FOR N]
    a[j] := b[j] * c[j]
```

While it is theoretically valid to divide the original parallel expression [1] between two parallel processors, no speed would be gained. The notation, however, helps clarify Occam's syntax:

```
PAR
  PAR i = [0 FOR N/2]
    a[i] := b[i] * c[i]
  PAR j = [N/2 FOR N]
    a[j] := b[j] * c[j]
```

Channels are a variable type not found in conventional languages. A simple example will illustrate their use. A procedure to double the data read from a channel input and transmit it to the channel output can be defined:

```
PROC two_times(CHAN input, output) =
  VAR x,y:
  SEQ
    input ? x
    y := 2 * x
    output ! y
```

The ? operator reads the channel input; the ! operator writes the channel output. Calling the procedure `two_times` accomplishes the desired multiplication across the channel.

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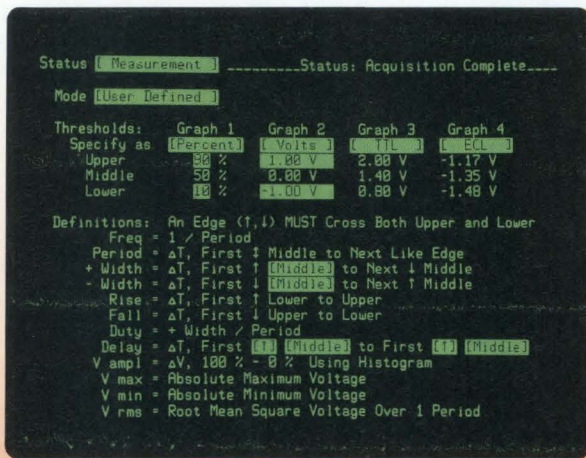


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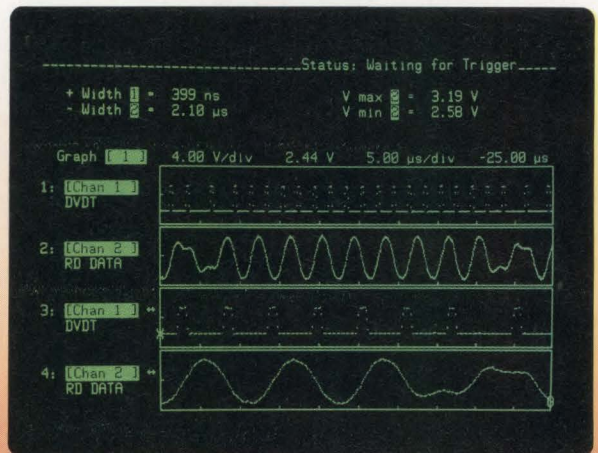
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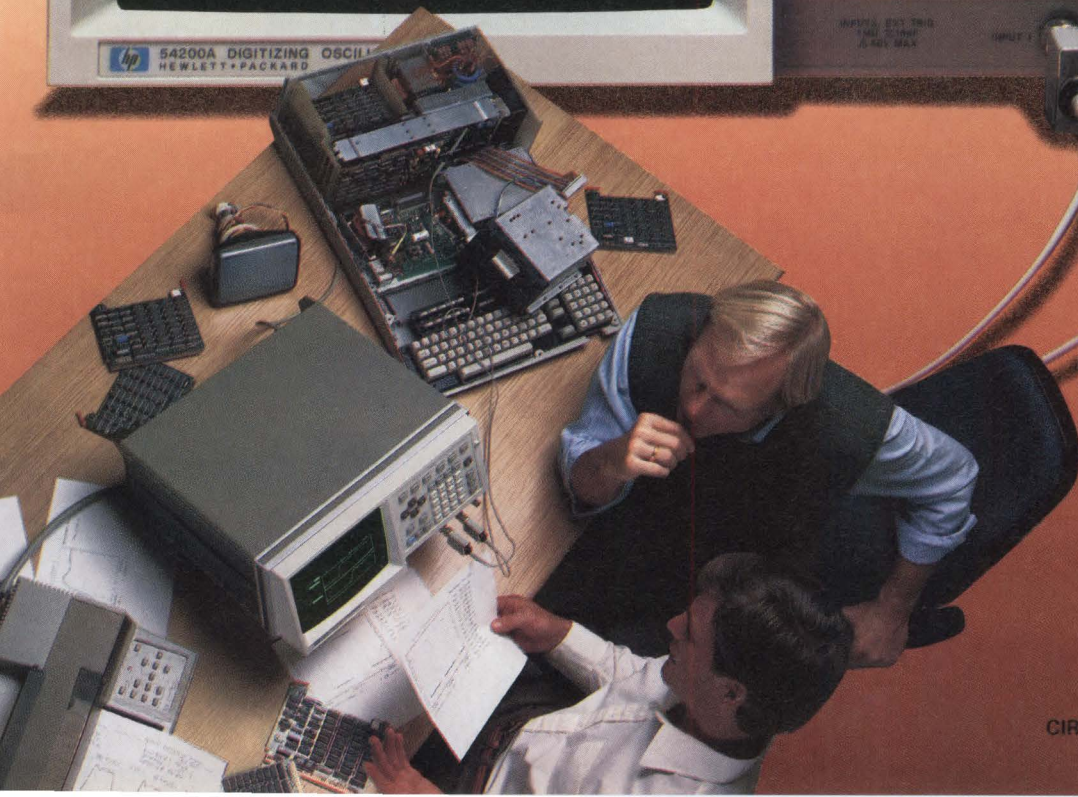
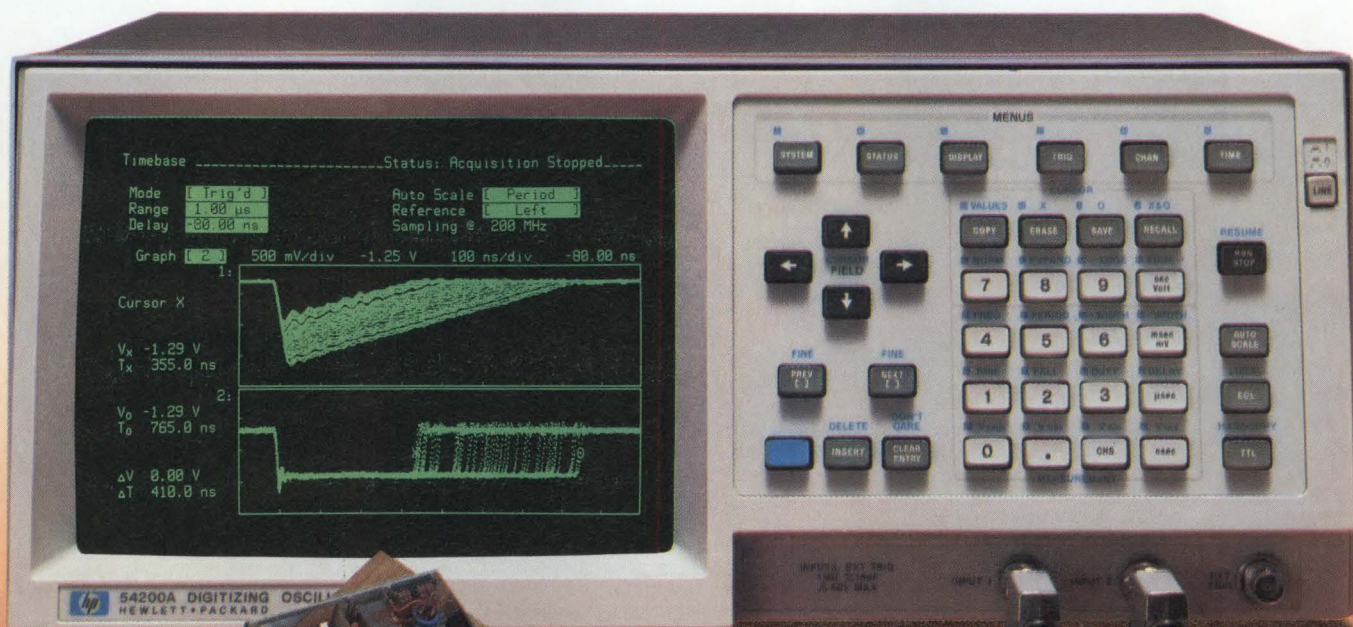
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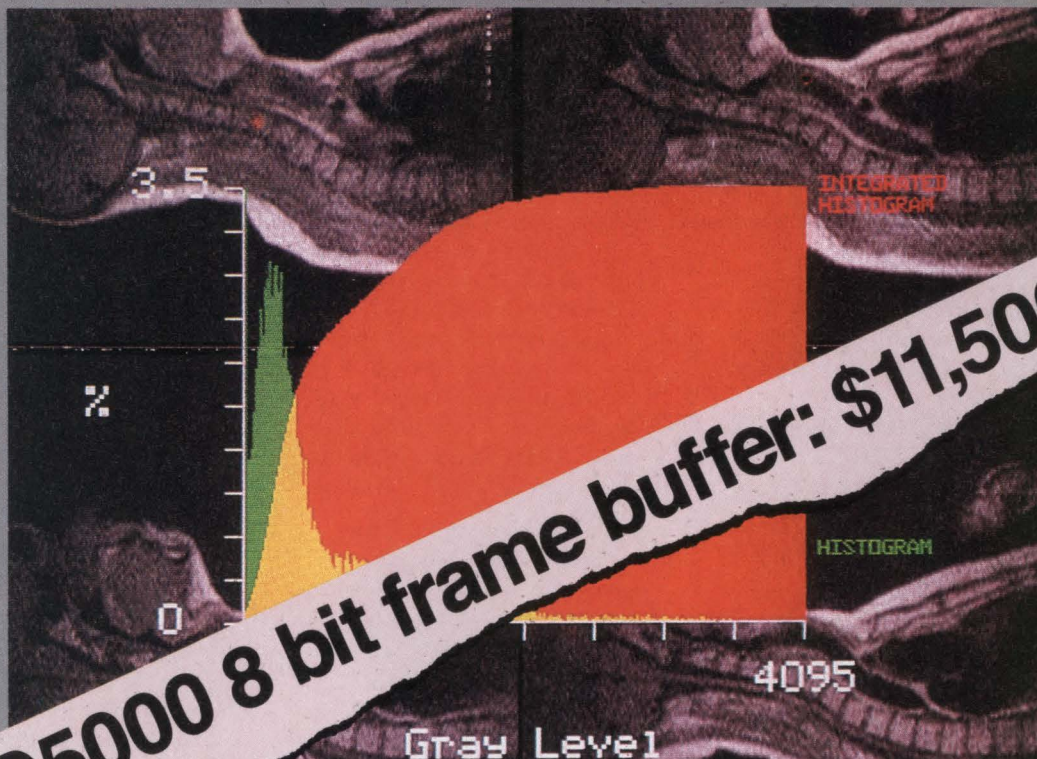
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Eurocard bus takes a test drive in the United States

A 16-bit bus designed on a single-height Eurocard is traveling the roads of America in its quest for cost-sensitive, 16-bit control applications. The growing popularity of large-format, 16- and 32-bit bus designs has created a gap between highend applications and dedicated control functions long dominated by the 8-bit STD bus in the United States.

While some attempts have been made to force 16-bit designs on the STD bus, it remains an 8-bit bus. It will never fully accommodate 16-bit processors without fancy multiplexing schemes. The European entry for this niche is the G-64 bus from Gespac (Mesa, Ariz), a subsidiary of Gespac, SA, of Geneva, Switzerland.

Gespac introduced the G-64 bus in Europe in 1980, where it received a big boost from a second-sourcing by the French giant, Thompson CSF. Thompson CSF is also establishing a significant presence in the United States. But simply shipping products—even high quality, reliable products—is not enough to gain wide acceptance. Several other factors must work together. These include product support, a base of software specific to the various boards, and module-development support. Moreover, in order to attract other manufacturers, the bus specification must be placed in the public domain.

Factors encouraging acceptance

The need for, and eventual acceptance of, a 16-bit bus on a small form factor in the United States is without dispute. The G-64 bus is but one of a number of European candidates that could fit the bill. Since the large-format VMEbus (a double-height Eurocard with DIN connectors) has already attracted major manufacturers in the United States, there appears to be no American resistance to Eurocard designs *per se*.

G-64 has 16 nonmultiplexed data lines and 16 address lines, plus a page-signal and memory-select line. These allow it to address up to 256 Kbytes without multiplexing. DMA is supported by three DMA control signals and one daisy chain line used

for DMA and interrupt priority control. Interrupts consist of three interrupt signals and one interrupt acknowledge signal.

The G-64 design now uses the 64-pin DIN 41612 type B connector. But Cosma Pabouctsidis, president of Gespac in the United States, has said his company will develop boards incorporating the current G-64 specification with a 96-pin DIN connec-

tor. This will provide a full 32-bit address space for those microprocessors able to use it, as well as seven levels of interrupt. According to Pabouctsidis, the 32-bit design would be backward compatible with current specifications, preventing loss of design investment.

Current 8- and 16-bit processors supported by Gespac on the G-64 bus include the 6800, 6809, Z80, 8085, 68000, 16032, 8088, and J-11. The company also offers a broad range of memory boards, interface boards, controllers for floppy and hard disks, and transducer boards. To date, however, no U.S. manufacturers other than Gespac are producing G-64 board products. About 16 to 20 companies in Europe manufacture competitive products. The G-64 bus specification is in the public domain, however, and Gespac apparently offers support and information to other manufacturers through a users' and manufacturers' group in Geneva.

Software library eases design

Two other major requirements for any *de facto* acceptance of the bus are availability of software and development support. The case of the STD bus provides a clear example of how important this can be. The existence of software modules has greatly eased the task of designing with, and developing systems based on STD boards.

In the case of G-64, the lack of large libraries of software modules could be regarded as either a deficit or an opportunity for U.S. companies. Gespac itself supplies some modules, such as software drivers for its IEEE 488 boards. But the company is nowhere near ready to support software for all the boards in its product line. It does supply CP/M operating systems and utilities for most of the processors that work on the bus. And some development software is available—notably a 16032 cross development package that runs under Z80 CP/M. Nevertheless, it looks as though true development support will have to come from elsewhere.

Development systems based on floppies or Winchesters have been

ROW B		ROW A	FUNCTION
GND	1	GND	Power (2)
A8 A9 A10 A11 A12 A13 A14 A15	2 3 4 5 6 7 8 9	A0 A1 A2 A3 A4 A5 A6 A7	Address line A0 to A15 (16)
BRQ DS1 BGACK Enable RES NMI IRQ FIRQ IACK	10 11 12 13 14 15 16 17 18	BGRT DS0 HALT SYCLK VPA RDY (DTACK) VMA (AS) R/W Halt Ack	Control lines (18)
D12 D13 D14 D15	19 20 21 22	D8 D9 D10 D11	DATA 2nd Byte (8)
D4 D5 D6 D7	23 24 25 26	D0 D1 D2 D3	DATA 1st Byte (8)
Parity error (BERR) Chain in	27 28	Page Chain Out	Miscellaneous (4)
+ 5V Battery -12V + 5V GND	29 30 31 32	- 5V +12V + 5V GND	Power (8)

The 16 address lines of the G-64 bus can access up to 256 Kbytes with the help of the Page and Valid Memory Address (VMA) lines. By using a 96-pin dual-inline connector, a third row of pins (Row C) could be added for 32 bits of address and additional control signals.

built around a given processor and packaged in a G-64 card cage. CP/M editors, assemblers, debuggers, and compilers presumably would help develop the drivers and system software for a given design. Thus, a great deal of work needs to take place if G-64 is to assume a position as an accepted bus in U.S. industry.

Second-sourcing of G-64 products in the United States does appear to be happening with the help of another European company. Thompson CSF is not only second-sourcing some of Gespac's board products, it is also producing G-64 boards that include designs based on Thompson CSF ICs.

There is, for example, a graphics module that incorporates the 9340/41 alphanumeric and graphics processor chip set, as well as a graphics board using the 9367 graphics processor. Turnabout being "good" play, Gespac is likewise second-sourcing some Thompson CSF designs.

In the support and development, Thompson provides ROM-based software with its boards and an 8-bit development system for G-64 cards. The Themis development system is primarily aimed at 6800/6809 processor family and OS-9 operating system.

At this point, the G-64 appears to have a head start on the road to

acceptance. It is charting a course through an area where a definite need exists for a small-format, 16-bit bus design to be used in control applications. Its ultimate success will depend on attracting more manufacturers, and on the appearance of a broader base of software development support. To date, two European manufacturers are driving the bus in the United States—one a very major company at that. And the path is straight toward making the G-64 a naturalized American.

—Tom Williams, West Coast
Managing Editor

MEMORY SYSTEMS

Emerging QIC standards enhance tape flexibility

New standards for quarter-inch magnetic tape, now under consideration by the Quarter-Inch Compatibility Committee, will provide more options for system integrators and end users. One proposed standard will double the storage capacity of 600-ft tape. Another proposed standard, designed primarily for the 3½-in. Winchester backup market, will probably be a variation of the Tallgrass Technologies (Overland Park, Kans) Personal Computer/Tape format. This controversial new approach gives magnetic tape some of a floppy disk's features.

The QIC committee, which includes representative from 14 companies,

has so far approved a set of standards for 9-track tape. QIC-24 is a formatting standard for 3M Corp (St Paul, Minn) DC300XL or DC600A tape, or equivalent. This standard, designed for streaming magnetic tape, allows the 600-ft DC600A tape to store 60 Mbytes. QIC-2 is an intelligent interface standard that supports QIC-24, and QIC-36 is a device-level interface standard.

With support from 3M, Tallgrass's PC/T format has been accepted as a starting point for development of a QIC-100 standard. Designed for 3M's yet-to-be introduced DC2000 tape, this standard will allow 40

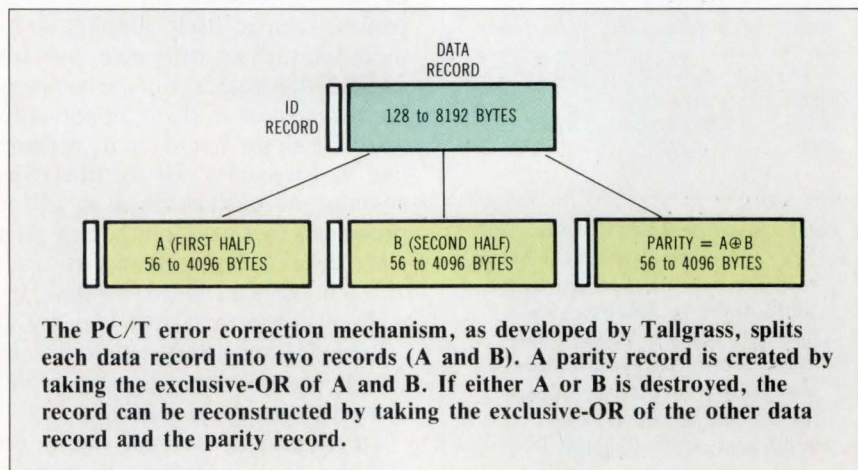
Mbytes of storage on a 24-track, 200-ft tape. Unlike other standards proposed by the QIC, PC/T allows individual data blocks to be overwritten without prior erasure. It also supports an extensive error correction mechanism, and does not require read-after-write verification.

A new approach

The proposed QIC-50 standard, originated primarily by Qantex (Hauppauge, NY), is a recording format that places 20 tracks and 120 Mbytes on DC600A or equivalent tape. Although QIC-50 has the same block format as QIC-24, it adds an error correction mechanism. QIC-59 is a device level interface similar to QIC-36.

No QIC-50 products are available at this time. However, Tallgrass recently announced a series of PC/T products that use DC600A and DC1000 tape. Hewlett-Packard's Greeley, Colo division is believed to be working on a line of PC/T products, but project manager Mike Tremblay would not comment on such reports. Tremblay affirmed Hewlett-Packard's support for PC/T, however.

By allowing overwrite of individual blocks, PC/T allows the user to



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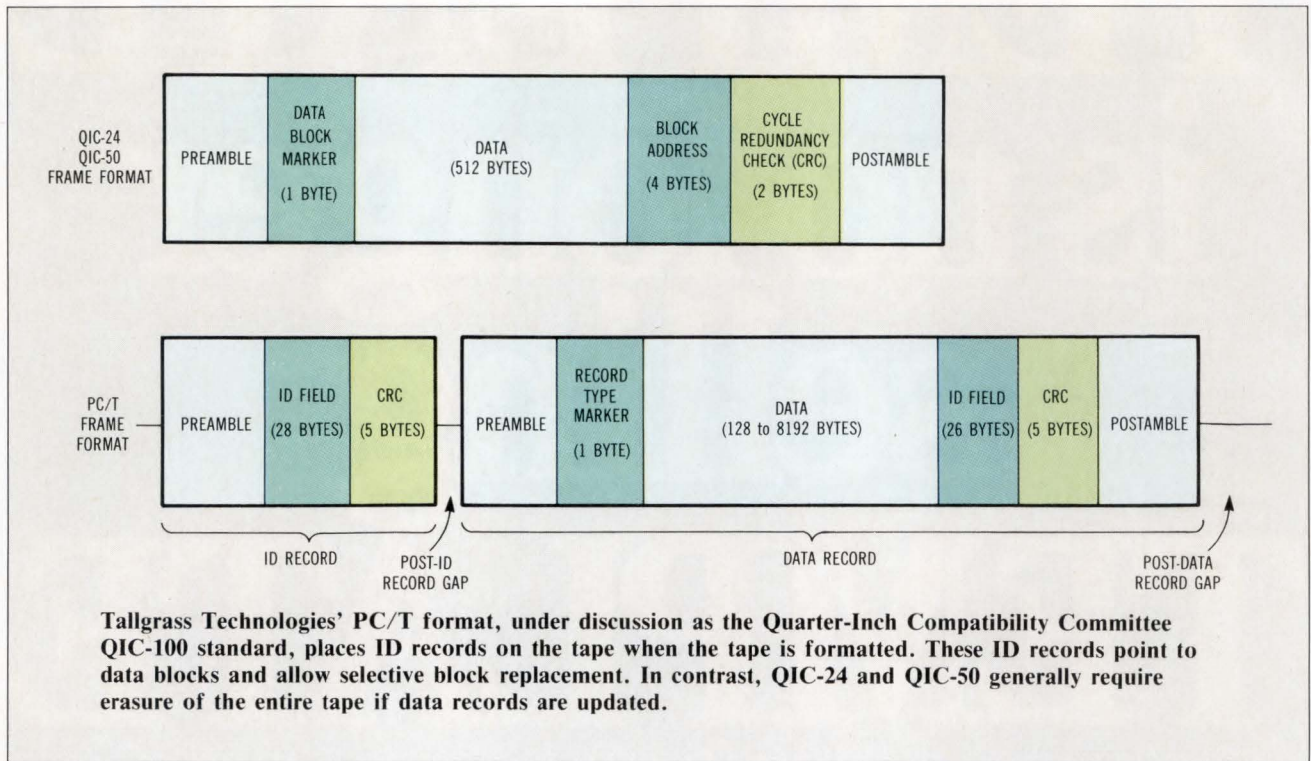
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CIRCLE 47



update files without rerecording the entire tape. Although access is slower, the tape behaves much like a floppy disk. "We're not selling it as a streamer, we're selling it as online archival storage," says Tallgrass's marketing vice president Steve Volk. "I don't think tape will survive only as a backup device."

To allow overwrite, PC/T puts ID records on the tape when the tape is formatted. These records, which are never changed, serve as guideposts to the data blocks that follow them. In the Tallgrass implementation, a tape operating system provides a directory structure that links data blocks to files. Since data blocks have their own internal ID records, the directory structure can be reconstructed by scanning the tape.

In contrast, neither QIC-24 nor QIC-50 tapes are preformatted with ID records, and QIC-24 does not permit overwrite at all. According to Mario DiFede, author of the QIC-50 specification and product manager for magnetic tape products at Qantex, block replacement could be implemented with QIC-50 in software. QIC-50 allows penetration of the oxide layer to overwrite the tape—the technique used by PC/T. DiFede does

not see block replacement as a likely implementation of QIC-50, however.

PC/T allows the systems integrator to set data block length from 128 to 8192 bytes. To simplify controller electronics, the system integrator can interleave blocks. Although PC/T has been suggested as QIC-100, it is not device dependent and can be used for any type of magnetic tape. For this reason, Tallgrass representatives vigorously deny claims that PC/T is a "low end" format.

Read-after-write controversy

PC/T format provokes heated reactions because it was designed for use with single-gap heads. These heads simplify drive electronics, but do not permit the read-after-write verification provided by dual-gap heads. To verify after a write, the entire tape needs to be rewound.

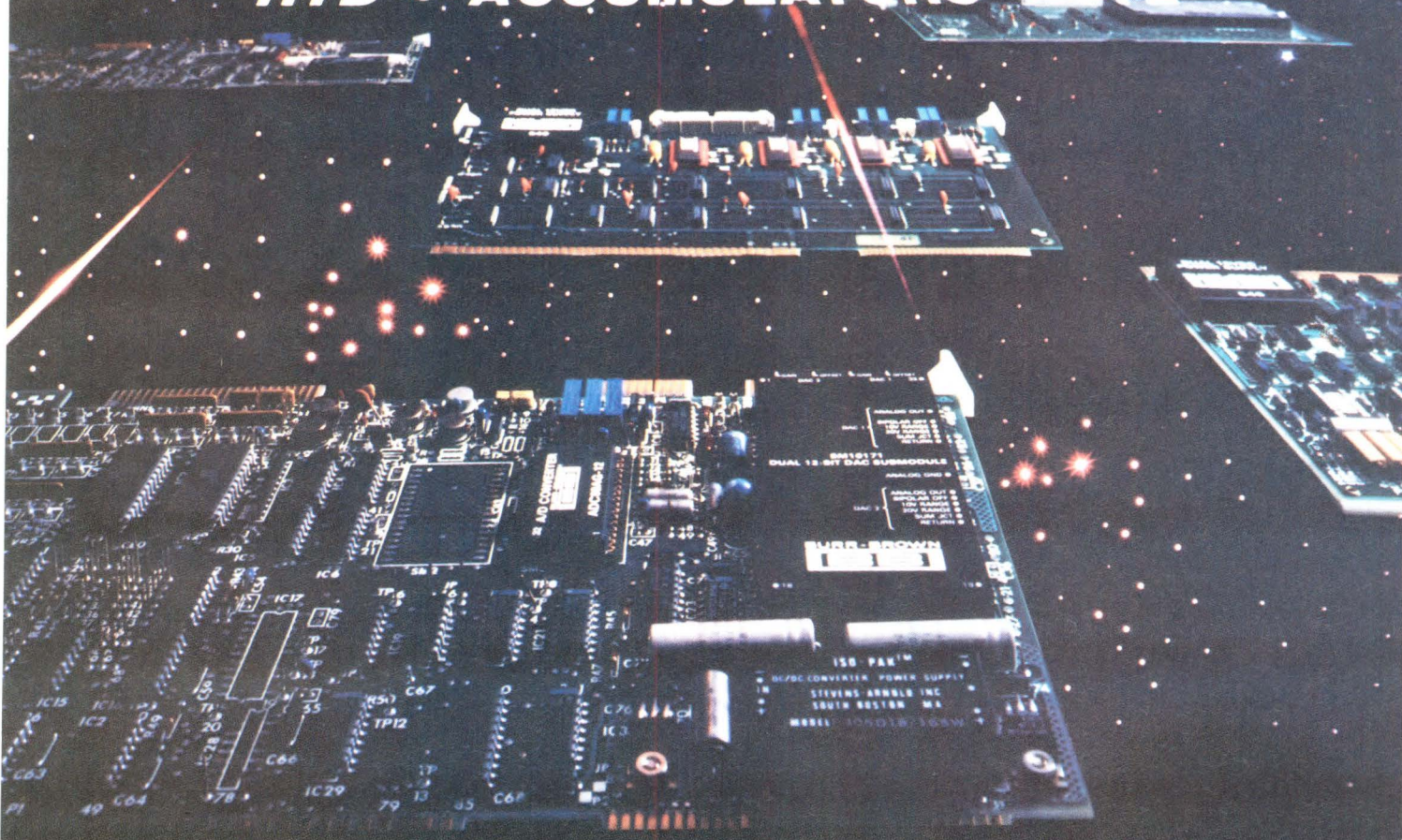
PC/T does not prohibit dual-gap heads. But it does include an extensive error correction mechanism that is not dependent on read-after-write. "With adequate error correction, there's really no purpose for read-after-write," says Tallgrass president Dave Allen. "But that's really a hot potato. The tape drive industry has grown up on read-after-write."

The PC/T error correction mechanism, based on a 3M error correction scheme, splits each data record into two data records. A parity record is created by taking the exclusive OR of the two data records. If either data record is destroyed, it can be reconstructed from the other data record and the parity record. With an original data block length of 8192 bytes, this plan allows correction of 4096-byte segments.

Allen says this level of data correction is necessary in the personal computer market. Read-after-write is insufficient, he maintains, because tapes can be easily damaged or contaminated. Critics say it requires too much overhead, and does not replace the need for read-after-write. "You don't need anywhere near that depth of error correction with a read-after-write head," says Richard Gorgens, president of Alloy Computer Products (Framingham, Mass). "And without a verification pass, even with parity, I wouldn't trust it."

QIC-24 has error detection, but no error correction. QIC-50 allows correction of up to two 512-byte data blocks out of any 30 blocks. The PC/T format could conceivably be used without error correction—but

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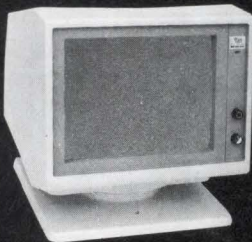
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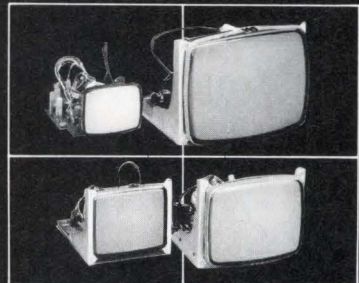
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SYSTEM TECHNOLOGY/MEMORY SYSTEMS

Tallgrass is determined to keep it in the QIC-100 specification, Allen says.

Into the market

Although PC/T is only a starting point for QIC-100, it appears the eventual standard will look much like PC/T. Heavy backing from 3M, the dominant manufacturer of quarter-inch tape, is one factor in PC/T's favor. "We believe it's the most powerful and most versatile of the various formats proposed," says William Crammatte, product planning supervisor for 3M's data cartridge product line. In particular, Crammatte supports PC/T's error correction method and its ability to update files.

Meanwhile, Tallgrass has gone ahead and introduced a line of MS/DOS-compatible PC/T products. These include the 5000 and 6000 series HardFile products, which combine a 5¼-in. Winchester with a 60-Mbyte tape. The Grasshopper, a PC/T tape drive that fits into a 3½-in. form factor, has been introduced to the OEM market. Tallgrass has a formatter chip that implements PC/T, and expects to offer PC/T controllers eventually.

In the Tallgrass implementation, tape is "online"—meaning users do not have to exit programs to access the tape. Tallgrass is also working on software that will make the tape operating system totally transparent to the user. This scheme allows the tape operating system to capture all MS/DOS function calls, and route tape and disk requests to the proper source.

Tallgrass will have to overcome buyer resistance in two areas: overhead and speed. Because of the error correction method, a 90-Mbyte unformatted tape yields only 60 Mbytes of storage. The backup rate is about 1 Mbyte/min, while a QIC-24 tape can process 2 to 3 Mbytes/min.

An evolutionary approach

With a block format identical to QIC-24, the proposed QIC-50 standard is not a radical departure from existing tape standards. Like QIC-24, it is basically a streaming, gapless format that requires read-after-write. Compatibility with QIC-24 is an important criterion. "We want to

allow QIC-24 users to be able to read their old tapes," says DiFede.

An error correction mechanism has been added to QIC-50. Like PC/T, an exclusive-OR method is used to build parity blocks. However, there are only two parity blocks for each 30 data blocks, permitting reconstruction of up to two 512-byte blocks.

QIC-59, as a device level interface, is basically QIC-36 with only a few changes. QIC-2 can still be used for an intelligent interface. However, new interface standards will have to be developed for QIC-100. The 50-conductor cable used by QIC-36 is not designed for a 3½-in. form factor.

DiFede speaks respectfully of PC/T, but notes that QIC-50 is more accessible to system integrators. "PC/T is probably the best format around in terms of the amount of information contained," he says. "But it's the hardest to implement. Only one company has a formatter chip, and the ability to use it is restricted. With QIC-50, there's no licensing and no limitations."

A low cost alternative to QIC standards, the FloppyTape format from Cipher Data (San Diego, Calif), provides block replacement by simulating the data structure of a floppy disk drive. The format is implemented directly by the floppy disk controller. This poses such limitations as low format efficiency, but FloppyTape does not require a specialized formatter chip. While PC/T, QIC 24, and QIC 50 use group codes recording, FloppyTape uses the lower density modified frequency modulation favored by the disk drive industry.

Like all standardization efforts, the QIC process is subject to divisive arguments and proprietary conflicts. Once standards are approved, however, system integrators will have more alternatives in the tape backup market, with support from controller and tape drive manufacturers.

—Richard Goering,
Field Editor

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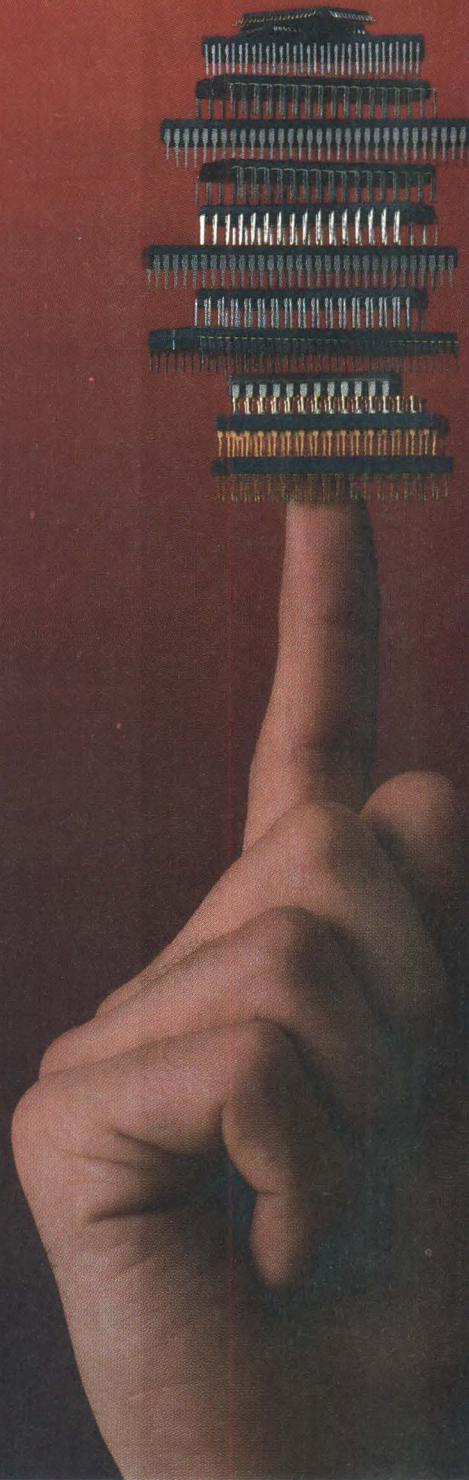
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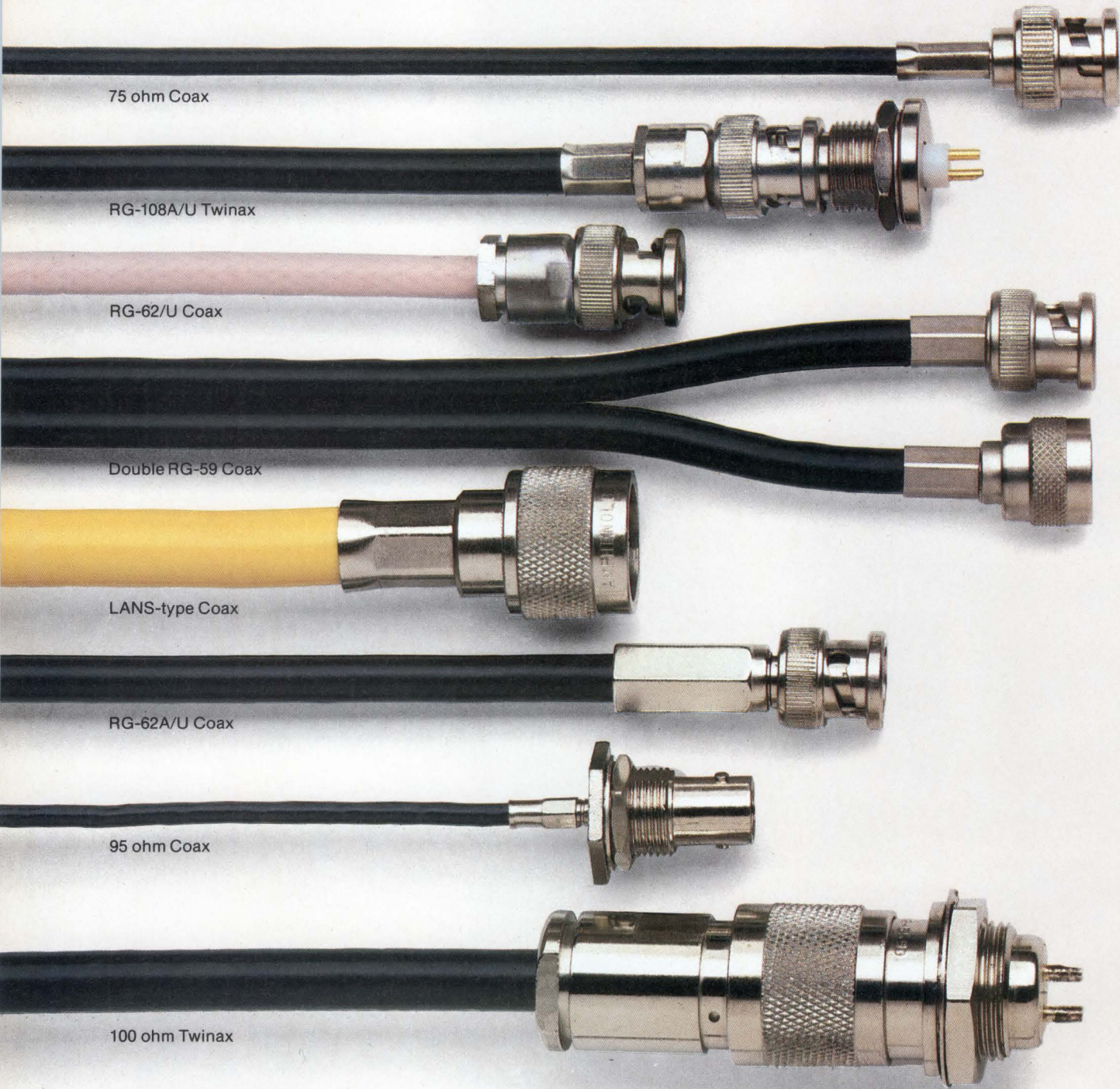
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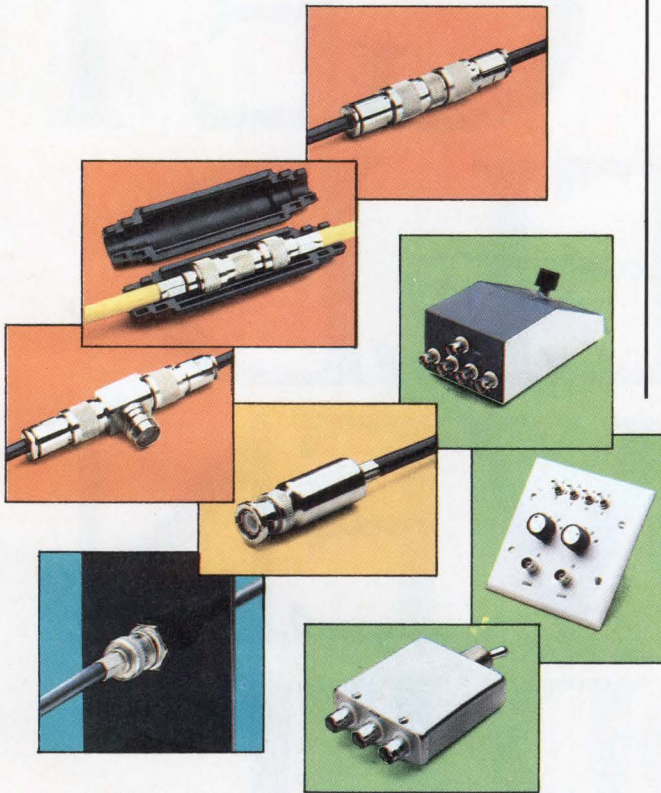
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SID '85 displays variety of information

This year's annual meeting of the Society for Information Display will be as diverse as its membership. To encompass all phases of the industry from chemistry to physics and from engineering to human psychology and ergonomics, SID '85 (April 29 through May 3 at the Sheraton Twin Towers, Orlando, Fla) will consist of three parts. The standard symposium sessions (Tuesday, Wednesday, and Thursday), evening panel sessions (Tuesday), and half- or full-day seminar sessions (Monday and Friday) will demonstrate that SID '85 is not a marketing symposium masquerading as a technical conference.

The largest area of growth in information display through the past several years has been in systems and applications, according to the conference's general chairman James N. Price. (He is supervisory engineer and project manager at the Naval Ocean System Center in San Diego.) Earlier emphasis has been put on the development of devices, "but many of those products are no longer in the R & D pipeline," he says. "Users now can present papers on how to apply those devices in real world situations."

Price says he finds this trend "very exciting to watch." With industry predictions of sales for display devices in computer systems alone ranging to as high as \$457 million for 1986 (an annual growth rate of 36.1 percent from 1981), that excitement is very real.



Former R & D devices can now be discussed in SID '85 sessions as viable products—James N. Price.

SID focuses on fresh ideas, according to symposium chairman Aris K. Silzars, general manager of hybrid components operations at Tektronix in Beaverton, Ore. Intent of the conference, he says, "is to present new research, new devices, new concepts. One of the strongest criteria is that all papers cover things that have not been published elsewhere before. Everything must be unique." He claims that SID is "the premier international technical display conference in the world." Several other conferences—some also sponsored by the Society—do take place in various countries, but "SID is the only one that serves as an umbrella for all the interests."

Originally, the conference placed seminar sessions as a side issue. Last year, however, more than half of those who attended signed up for supplementary sessions. Seminar chairman Howard L. Funk, director of technical resources programs at IBM in White Plains, NY, says this year's seminars are designed for both experts and novices.

Expert systems now a factor

The subset of artificial intelligence known as expert systems has become a factor in the design of display devices. These systems now solve many of the problems inherent in so-called intelligent products.

The graphics for intelligent workstations, for example, usually depended upon an associated minicomputer. Carl Machover, president of Machover Associates Corp of White Plains, NY, says that increasing use of microprocessors has significantly increased the intelligence available at workstations. No longer does the intelligence have to be concentrated in a maxi or minicomputer. "In fact," he says, "in the not-too-far distant future I would be very much surprised if there were any dumb or smart terminals left; almost everything will be intelligent workstations."

In the seminar session, Display Systems and Applications, Machover will provide an overview discussion of current and future directions in



SID '85 symposium papers are unique and cover all display areas—Aris K. Silzars.

computer graphics. He will include perspectives on both applications and hardware technology. "The largest application area for graphics is CAD/CAM, followed by business," says Machover. "Requirements of these applications have had major impact on the technology. In turn, the availability of certain technologies has made some of the applications more feasible."

In the last few years, he adds, computer graphics have moved aggressively toward raster display, while storage tubes have become much less of a factor, Machover adds. "The resolution of raster systems has increased so that image quality as well as line quality are much improved. The rationale and advantages of vector refresh are, therefore, gradually diminishing."

The degrees of function of raster systems have increased through a series of hardware processors that perform near realtime manipulation of solid images. This has resulted in prices two orders of magnitude less than that of classic simulators, Machover says.

Moreover, the technology has been greatly affected by enormous reductions in memory cost and by the ability to turn out very low cost special purpose chips, he adds. "This permits designers to build special functions into systems in quantities that we couldn't think of doing before," he says. "In the cost of chip design today, this capability also has

brought about a reduction of two orders of magnitude.”

Display technology will also be covered in a number of other SID presentations. For example, speakers in a total of four seminars on Display Technology Fundamentals will discuss several subsets of display technology, including CRTs, liquid crystal devices, flat panels, and electroluminescence.

In the seminar discussing CRT systems, Carlo Infante of Saber Technology will examine both monochrome and the rush toward color displays. He will also include such diverse associated technologies as electron optics, phosphors, color guns, ergonomics, and system trade-offs, plus predictions for the future. As part of the same seminar, Satish Gupta of IBM's Research Center in Yorktown Heights, NY will cover factors that influence advanced display architectures, such as rapid advancements in memory technology. The discussion, in particular, will review such inventions as the video RAM and developments of sophisticated VLSI controllers.

Progress of “The Flat Channel Multiplier CRT” will be discussed in

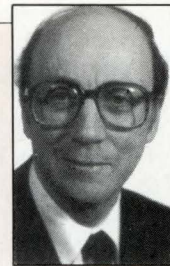
a paper by A. W. Woodhead and others from the Philips Research Labs, Surrey, England. Woodhead will show how improvements in the flat deflection system have resulted in experimental monochrome tubes that have 12-in. diagonal displays and are 3-in. thick. There are indications that a full-color range is also possible.

Woodhead will explain how difficulties in making a thin, flat CRT are reduced by separating the conflicting needs of the beam scanning process from those of the generation of light at the fluorescent screen. Resolution was enhanced by increasing the number of channels in the multiplier from 50,000 to 170,000.

LCDs to the forefront

Research analysts differ widely on numbers, but agree that market growth for liquid crystal devices will be explosive over the next several years. Fabrication techniques for these devices, however, must be improved just as drastically in order to make this forecast a reality. Most of the papers in the LCD Technology session indicate how that will occur.

In one of these papers, “Polymer Encapsulated Nematic Liquid Crystals



*Both experts and novices
will be served by SID
'85 seminar sessions—
Howard L. Funk.*

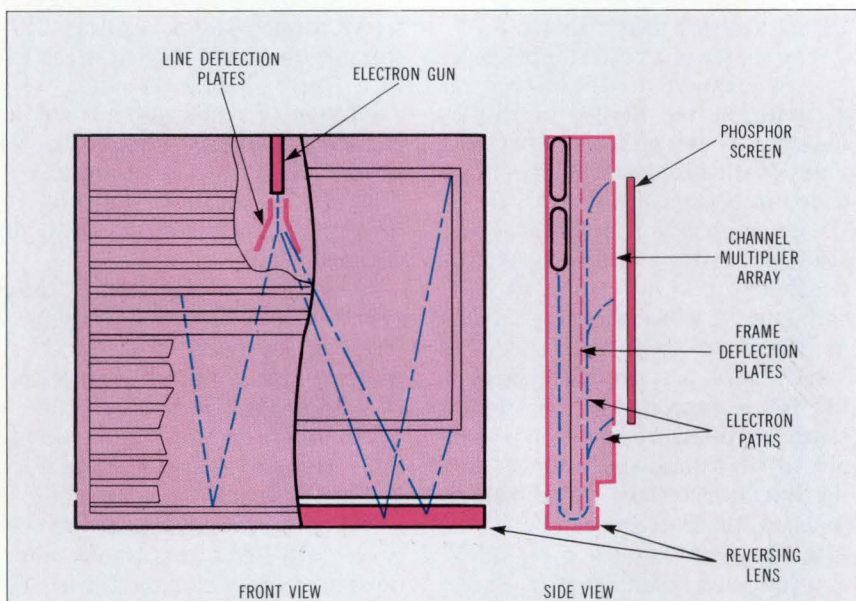
tals for Display and Light Control Applications,” James L. Ferguson of Raychem Corp in Menlo Park, Calif, will explain how to make LCDs with the liquid crystal in a binder that generates a curvilinear orientation for production of very large area displays. Such devices will be approximately 25-microns thick and have resolutions of up to 1000 lines/in.

Ferguson claims his paper is “the first to describe this technique. It will represent a change in the state of the art that will lead to a major expansion in the application of LCDs into areas where they previously have not been useful.” He says that even existing application areas will be affected.

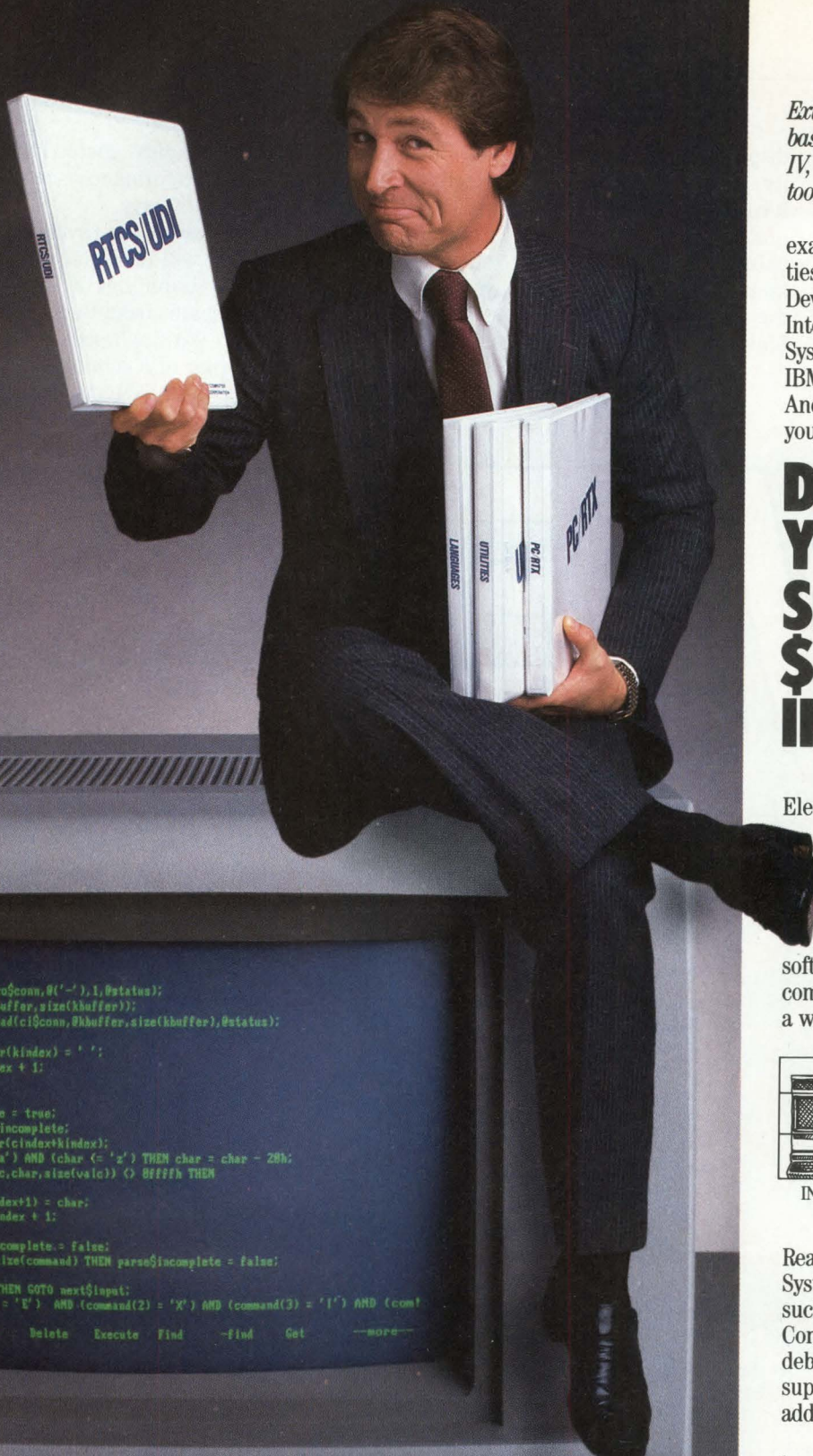
In the paper, “Study on Improvements in Contrast Made by Polarizers for Liquid Crystal Displays,” Tatsuki Nagatsuka and others from Nitto Electric Industrial Co of Toyohashi, Japan will describe the use of a polarizer to improve the contrast in LCDs. This polarizer, still in the laboratory stage, shows 10 times the contrast ratio of conventional ones, according to Nagatsuka.

Concern for human factors

General chairman Price says the area of human factors will be stressed this year at SID because it is of concern to most users of display systems. Price defines human factors as more than ergonomics. “It concerns how the information is presented to viewers. Designers have to worry about the size of the characters on the screen, recognition of colors (contrast between colors), operator fatigue, display standards, and environmental



In the flat channel multiplier described by session speaker A. W. Woodward of Philips Research Labs, the rear mounted electron gun lies parallel to the screen. Path of the electron beam is between a pair of electrostatic line deflection plates to the bottom of the tube. A reversing lens turns the beam 180 degrees and projects it to the front section.

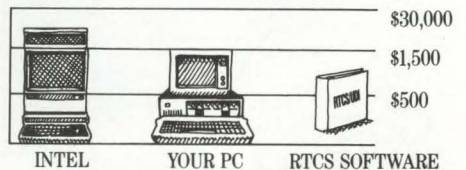


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```

write(c0$conn, @(' '), 1, @status);
TB(0, @kbuffer, size(kbuffer));
= dq$read(c0$conn, @kbuffer, size(kbuffer), @status);
= 0;
LE kbuffer(kindex) = ' ';
ix = kindex + 1;

= 0;
incomplete = true;
LE parse$incomplete;
= kbuffer(cindex+kindex);
char >= 'a' AND (char <= 'z') THEN char = char - 20h;
MDB(@valc, char, size(valc)) O 0ffffh THEN

command(cindex+1) = char;
index = cindex + 1;

parse$incomplete = false;
(index = size(command) THEN parse$incomplete = false;

index = 0 THEN GOTO next$input;
command(1) = 'E' AND (command(2) = 'X') AND (command(3) = 'I') AND (com

Block Delete Execute Find -find Get -more-

```

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factors such as ambient light or glare," he says.

In a paper that emphasizes Price's statements, Wanda Smith, manager of corporate human factors engineering at Hewlett-Packard in Palo Alto, Calif., will discuss the role of ergonomics in the design and use of color

displays. "Color can enhance usability, but only if it is used correctly; it can just as readily degrade performance if used unwisely. Correct choice of color depends on the knowledge of visual psychophysics by the designer of the color system. Unless the designer applies visual

psychological principles correctly, productivity—and performance—can be degraded," Smith says.

Further discussion of the psychophysics of display will take place in the session on Psychophysics of Displays, with participants from Boeing, IBM, Tektronix, Westinghouse, the New York Institute of Technology, the Naval Underwater Systems Center, and the Naval Submarine Medical Research Lab.

Development of a high resolution, flicker-free color display will be reported by Kunio Ando and others from Hitachi, Ltd of Yokohama, Japan in a paper titled, "A 2448- x 2048-Dot High Resolution Flicker-Free Color Display." Ando claims that "this is the world's first flicker-free color product able to display more than four million dots.

The CRT has a resolution of 2448 x 2048 dots at the noninterlaced scanning mode—as opposed to 1280 x 1024 for a current high resolution 360- x 270-mm display. Dot pitch is 0.15 mm rather than 0.21 to 0.31 mm, and video output is 240 MHz at 50-V peak-to-peak, rather than 100 MHz at 55 V. Horizontal scanning frequency is 130 kHz for the new system and 64 kHz for the present one. Vertical scanning frequencies are 60 kHz for both. And misconvergence is only 0.1 mm for the new version compared to 0.3 mm for the current device.

The paperless society?

Hard copy continues to play a major part in graphics—as evidenced by four separate symposium sessions and one evening panel discussion. For example, Machover says, "We talk pretty glibly about the paperless office of the future—but we use more paper than ever." He sees a definite move toward the color world, however. "From 70 to 90 percent of all terminals delivered are color—and that trend reflects itself on the hard copy field." Although new monochromatic hard copy devices are still being introduced, most of the developments are in color printers or plotters.

Machover says surprising growth has occurred over the past few years in low cost multiple-pen plotters, those that handle 8½- x 11-in. sheets of paper. "Influence of the personal

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*Patent Pending

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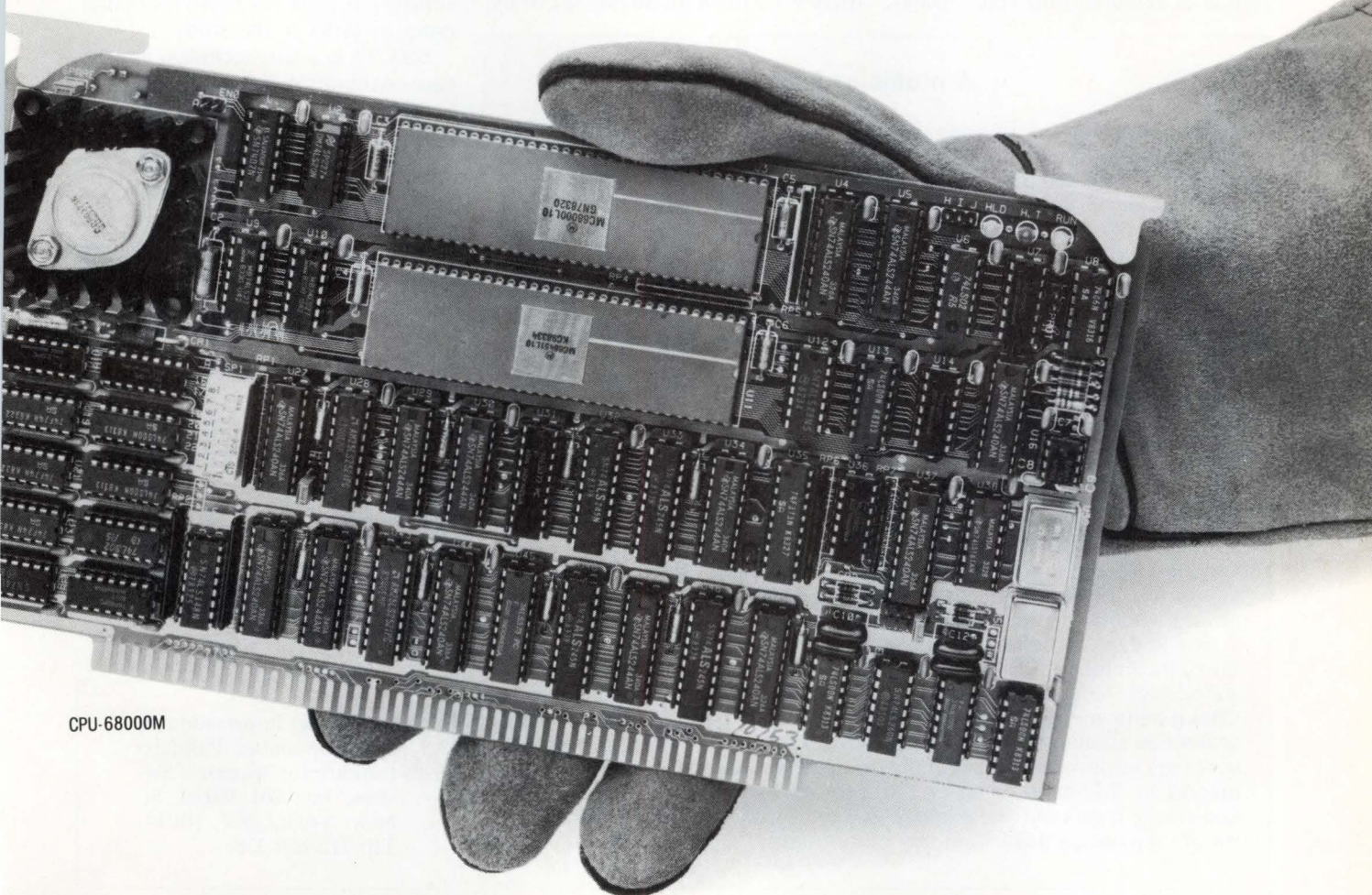
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computer has resulted in sales of small plotters now in excess of 300 thousand each year," Machover adds. "This is an astonishing number when you consider that it amounts to about ten times the number of conventional plotters installed in the last five to eight years."

Input devices

A relatively new subject covered at SID '85 will be operator input devices. The seminar session, Display Systems and Applications: Voice Entry and I/O for Display, will include discussions of several different devices, but the most unique is likely to be voice recognition. Input pointing devices, such as light pens, mice, and touch screens, have been accepted for some time—as has the keyboard. Now, voice recognition also comes under the heading of input devices.

Steven DeGennaro, a research staff member at the IBM Thomas J. Watson Research Center, will present results of research into voice recog-

nition as input. He will discuss an experimental system developed at the Center that allows human voice input to create office documents such as letters and memos.

DeGennaro says that this is a real-time, isolated-word, speaker-dependent system. It can recognize sentences composed from a 5000-word vocabulary—and identify more than 95 percent of the words correctly. He indicates that speech recognition is one of the fastest growing technologies in the field of human-machine interfaces.

In the paper, "Voices Versus Multifunctional Control: A Comparison of Three Control Logics," David G. Curry and others from the Flight Dynamics Lab at Wright-Patterson Air Force Base, Ohio, will compare voice recognition input to manual techniques for cockpit control. They will report on a study that they say shows "contrary to some conclusions in previously published literature, there is no inherent advantage to us-



CAD/DAM is the largest user of graphics today and provides the greatest influence—Carl Machover.

ing either voice recognition or multifunctional [manual] controls." Actually, they will show that the voice system produced better results but that the measurement procedures differed. They decided, however, "that there appears to be no integral superiority (in terms of speed and accuracy) for either voice or manual control, at least for these particular types of tasks in the study."

SID '85 is a true technical conference. Areas of discussion in Tuesday evening panels complement both symposium and seminar sessions. Subjects include active matrix addressed versus multiplexed flat panels, the prospects for color flat panel displays, competitive printing technologies for future workstations, and human factors issues in input devices.

—Sydney F. Shapiro,
Managing Editor

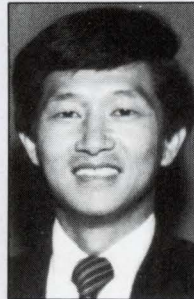
A profile of SID

The Society for Information Display is a small, highly specialized professional organization. I. F. Chang, current president of the society, says the group began 25 years ago, but rose to prominence more recently "because of computer advancements and the information explosion."

The present 2500 members design or use display equipment or investigate the technology. Their society, in its own statement, "promotes the use of information display, encourages its advancement, maintains a library of display information, exchanges and disseminates knowledge, promulgates definitions and standards, and stimulates new ideas in information display by providing a forum."

SID's early membership was drawn from the television electronics industry, and that influence is still felt. Refinements of TV technology are now used in many areas of computer displays. Advancements in TV displays remain the largest area of interest within the society. The second largest single element of SID at present is the military—and again, the technological developments in that area are relevant to advancements in the computer industry.

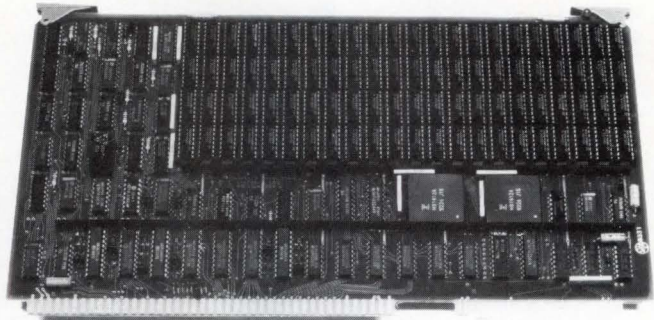
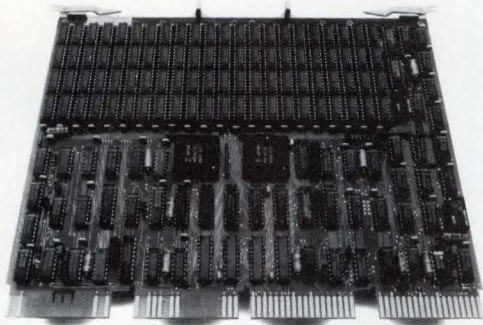
Chang says he believes SID's success can be attributed to the profile of its members. "SID," he says, "is made up of members with wide varieties of interests. But all are intimately tied to information display." Chang believes that "larger societies do not focus onto single areas as well as smaller societies such as SID can. They, therefore, cannot serve the information display field interests as well as SID. People who belong to SID need to draw the interdisciplinary information and knowledge base from one another. And they cannot get that broad spectra of knowledge base from any other source."



For further information on SID '85, contact Palisades Institute for Research Services, Inc, 201 Varick St, New York, NY 10014. Tel: 212/620-3388

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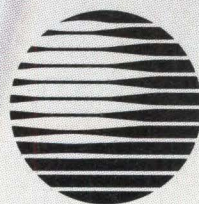
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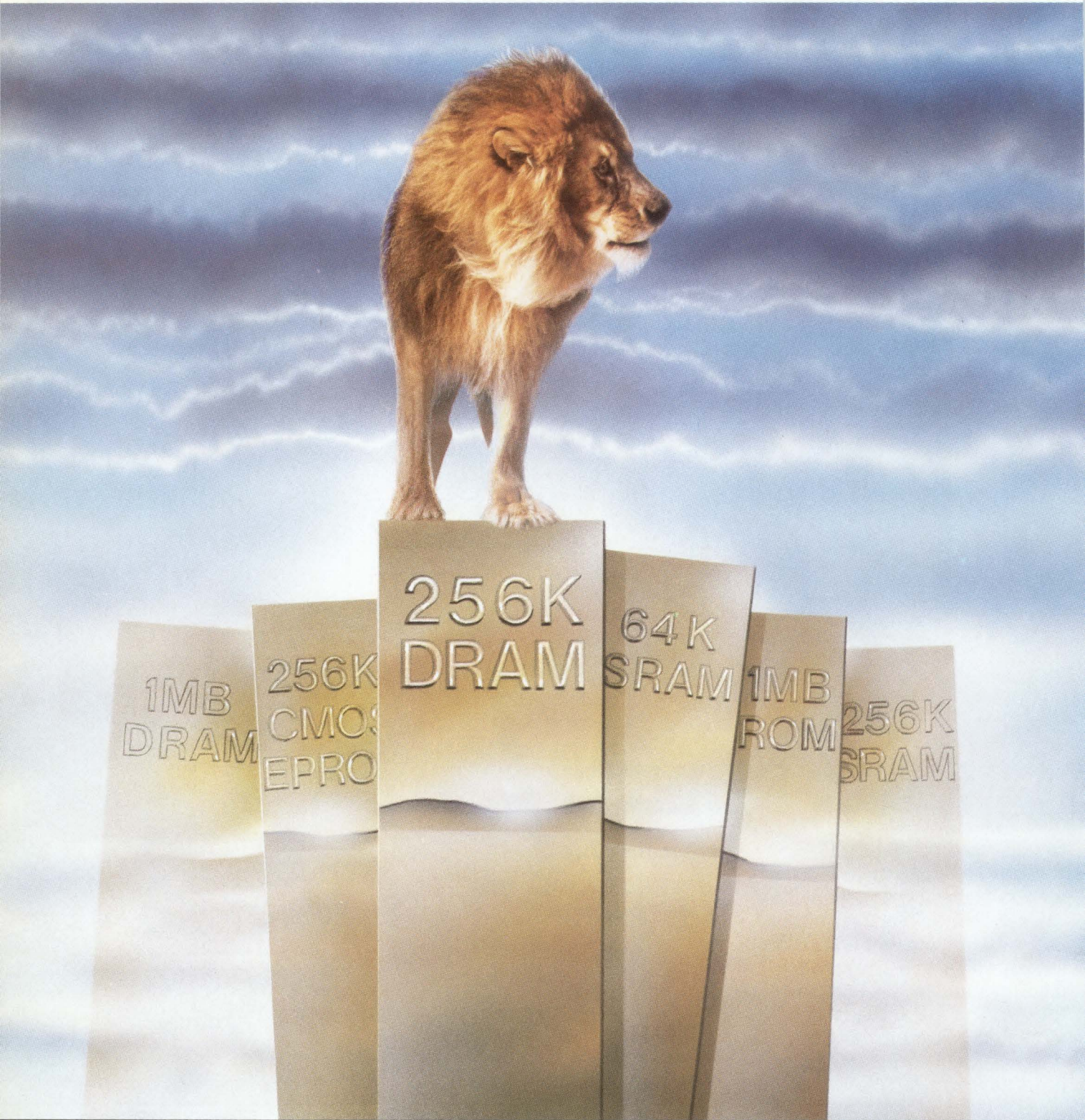
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TMM4164AP	64KX1	NMOS	YES	YES	120	150	200	P	
TMM41256C	256KX1	NMOS	YES	YES	150	200		C	
TMM41256P	256KX1	NMOS	YES	YES	120	150		P	
TMM41257P	256KX1	NMOS	YES	30'85	120	150		P	
TMM41464P	64KX4	NMOS	YES	30'85	120	150		P	
N-CHANNEL STATIC RAMS									
TMM2114A	1KX4	NMOS	YES	YES	120	150		P	
TMM2016AP	2KX8	NMOS	YES	YES	90	100	120 150	P	
TMM2015AP	2KX8	NMOS	YES	YES	90	100	120 150	P	
TMM2018D	2KX8	NMOS	YES	YES	35	45	55	D	
TMM2068D	4KX4	NMOS	YES	4'85	35	45	55	D	
TMM2064P	8KX8	NMOS	YES	YES	100	120	150	P	
TMM2063P	8KX8	NMOS	YES	3'85	100	120	150	P	
CMOS STATIC RAMS									
TC5504AP	4KX1	CMOS	YES	YES	200	300		P	
TC5514AP	1KX1	CMOS	YES	YES	200	300		P	
TC5516/17AP	2KX8	CMOS	YES	YES	200	250		PFY	
TC5517/18BP	2KX8	CMOS	YES	YES	200	250		PFY	
TC5565P	8KX8	MIX	YES	YES	120	150		PFY	
TC5564P	8KX8	CMOS	YES	YES	150	200		PF	
TC5561P	64KX1	MIX	20'85	30'85	55			P	
EPROMS									
TMM2764D	8KX8	NMOS	YES	YES	200	250		D	
TMM27128D	16KX8	NMOS	YES	YES	200	250		D	
TMM27256D	32KX8	NMOS	YES	YES	150	200		D	
CMOS EPROM									
TC57256D	32KX8	NMOS	YES	YES	200	250		D	
NMOS ROM									
TMM23256P	32KX8	NMOS	YES	YES	150			D	
CMOS ROM									
TC5364P	8KX8	CMOS	YES	YES	250			P28	
TC5365P	8KX8	CMOS	YES	YES	250			P28	
TC5366P	8KX8	CMOS	YES	YES	250			P24	
TC53257P	32KX8	CMOS	YES	YES	200			P28	
TC531000P	128KX8	CMOS	YES	YES	200			P28	
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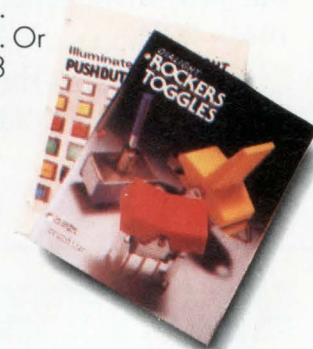


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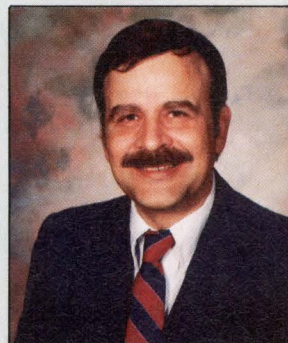
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SPECIAL REPORT ON HIGH RELIABILITY SYSTEMS

Defining high reliability is difficult because what makes a system "high reliability" depends entirely on the application and the user. For a component or systems manufacturer, high reliability often means keeping the field service requirements and warranty repairs low so that the product is profitable. For the end user, it means minimal system downtime in order to expect a reasonable return on the investment. For an astronaut, an airline pilot, an artificial heart patient, or someone whose life or health depends on a system, high reliability means the system must never fail.

In short, the customer and the competition set the standards for reliability—and, the standards keep getting tougher. To meet and beat the competition that is coming at them from every direction, system designers have to design reliability into every system. High reliability enters into almost every step of the design—from correct component selection and screening to environmental testing programs to system architectures.

Even with the most carefully laid out design, however, reliability is never a sure thing. This is because all systems are designed and built within some set of guidelines. Nevertheless, reliability is constantly improving, and customer expectations are high. In the cost-sensitive consumer arena, for example, buyers have come to expect years of trouble-free operation. And, in industrial control applications, where downtime can cost \$1 million a day or \$100 million in lawsuits, "fault-intolerance" is the new watchword.

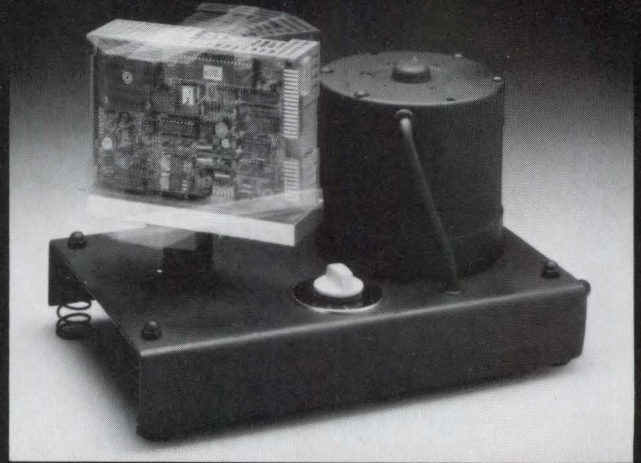
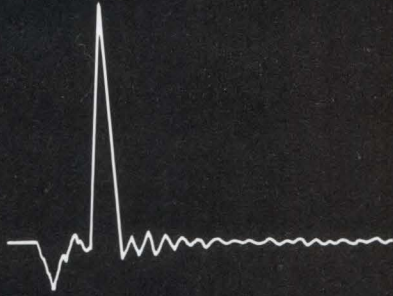
What follows are a few up-to-the-minute thoughts on high reliability. Some articles explain how replacing bipolar VLSI with CMOS can improve system reliability. Another discusses how determining the least amount of burn-in testing can catch device failures early in the design process. Other articles provide a direct cost analysis of hardware redundancy systems and show how a memory management technique can increase data reliability.

Bill W. Furlow

Bill Furlow
Senior Editor

LAPINE

TECHNOLOGY — IS SHAKING UP THE DISK DRIVE BUSINESS



Would you test the reliability of your disk drive in a paint shaker?

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We're Industry Standard 412/ST506 interface compatible, of course. So any system currently using full or half height bulky 5 1/4" disk drives can take advantage of our smaller and rugged 3 1/2" RANGER. We can even supply you with 5 1/4" form factor mounting brackets to make your disk integration that much easier. When you consider the manufacturing strength of our multi-billion dollar partner, Kyocera Corporation, and the financial support of Prudential Bache Trade Corporation, you can be sure of high quality, large volume product availability when you need it.

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FEWER CONNECTIONS TRANSLATE INTO FEWER FAILURES

A major source of system failures—interconnects—can be alleviated by using more VLSI components and more careful consideration of connection and cabling schemes.

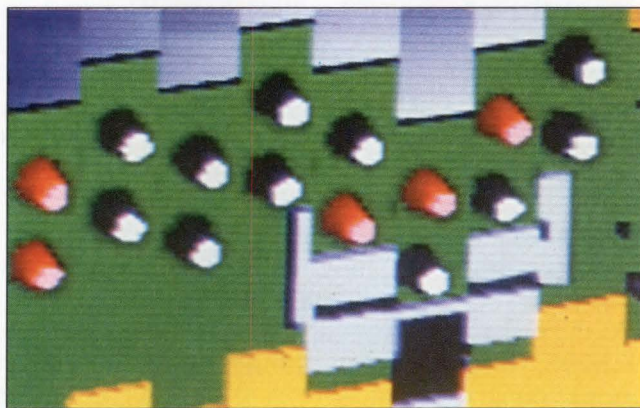
by Bill Furlow, Senior Editor

High reliability begins with the initial selection of components and it must be a primary consideration at every level of design. Much is at stake—after all, a company's ability to compete and survive depends on the reputation and reliability of its products.

Nowhere is a company's survival more dependent upon product reliability than in semiconductor manufacturing, where the customers are very astute at calculating true costs versus parts costs. "VLSI may drive down the initial purchase price and the manufacturing costs," says Rex Chappell, product marketing engineer at Hewlett-Packard (Palo Alto, Calif), "but the cost of fixing something in the field makes the cost of the failed component pale in comparison."

It follows that the least costly time to find a faulty component is at incoming inspection. Chappell pegs the cost of detecting a faulty IC, before it goes into inventory, at about \$4 to \$5. Once that component is mounted on the printed circuit board, replacement costs rise to about \$10. If the failed IC were discovered during the final system test, it could cost as much as \$30 to replace. And replacement costs in the field are at least \$300.

As designers turn to standard or semicustom VLSI ICs to solve their design problems, most industry observers expect overall system reliability to improve as well. "VLSI improves basic reliability," notes



Tony Moroyan, strategic marketing manager for Hitachi America (San Jose, Calif), "because reliability is a direct reflection of the number of chips the system uses, and perhaps more importantly, the number of interconnects. Every pin of every socket or every solder joint is a potential manufacturing defect, and a possible failure. Thus, with fewer interconnections, the potential reliability is higher."

Fortunately, both VLSI manufacturers and users agree that reliability is key to profitability. "A one percent increase in yields can mean the difference between profit and loss," says Moroyan, "and a 1-percent decrease in returns is even more dramatic." Consequently, gains in VLSI complexity for the semiconductor industry will help increase system reliability for the entire computer industry.

Percent of Defective ICs on First Inspection			
Logic Family	Low	Average	High
DTL	0.10	0.22	0.34
ECL	0.80	1.30	2.60
TTL	0.72	0.80	0.90
TTL low power Schottky	0.60	1.00	1.36
TTL Schottky	0.80	1.10	1.40
CMOS	1.00	1.59	3.00
Memories	1.00	1.30	1.80
Transistor	1.60	1.80	2.60
Diodes	0.90	1.20	1.30
Linear	2.00	3.30	4.60
Overall (by volume)	1.18	1.25	1.30

Viking Labs, part of the Honeywell Test Instruments Division (San Jose, Calif), has provided military parts qualifications for many years. Gene Hnatek, marketing manager, notes a marked improvement in the quality and reliability of ICs. One customer began using Joint Army-Navy qualified parts in 1975, with a 5-percent failure rate. By 1984 that failure rate was well under 1 percent. These figures were gathered in the testing of millions of ICs and are cited as typical quality improvements seen in the semiconductor industry over the last decade.

Data collected by Hewlett-Packard similarly spans the testing of about 50 million parts. During tests run at incoming inspection, IC defect rates ranged from 0.1 to 3.0 percent. If Chappell's estimated field service cost of \$300 per repair were applied and these defective parts were put into service, the impact would be severe.

Low power devices helping

Changing to not only VLSI ICs, but also low power CMOS systems, is improving system reliability. As the speed and complexity of CMOS chips increase, CMOS technology can compete effectively with power hungry bipolar systems. As a result, designers can reduce the size and capacity of both power supplies and cooling systems. This volume reduction can be traded for smaller system size or enhanced system features. Whatever the trade-off, a cooler running system pays big dividends in system reliability.

According to Ralph Cognac, marketing manager at Integrated Device Technology (Santa Clara, Calif), this bodes well for CMOS manufacturers. "In the military high reliability market, speed is the primary requirement," says Cognac. "Since CMOS parts are now approaching the highest speeds available, they will begin to be accepted in those markets. After speed, power, weight, and size are the major attributes that military designers look at."

But designers do not have to turn to military standard components in their search for higher reliability. According to Jack Handen, manager of high reliability

ICs at RCA's Solid State Division in Somerville, NJ, "It is inappropriate to go automatically to JAN qualified parts just for high reliability. Other levels of reliability enhancements exist. In fact, the designer's ability to select parts that are of adequate reliability without paying unwarranted premiums is a test of skill."

Some designers suggest that commercial market segments, especially the automotive sector, are more adept at finding high reliability at a low price than the military is. "I'd be very surprised if that were true," says Handen. "There is no doubt that the automotive companies face a very harsh environment, and that they are demanding customers. But I doubt that they are achieving higher reliability at a lower cost. They simply have the power of volume purchasing, which helps to drive their unit costs down. And automotive manufacturers operate on another part of the price/performance curve. In short, they don't need the speed that is so important in military systems." Handen also adds that "there is far less bureaucracy involved in some commercial markets. In many cases, one or two people decide on the part, technology, or vendor that will be used. Those are committee decisions on military projects."

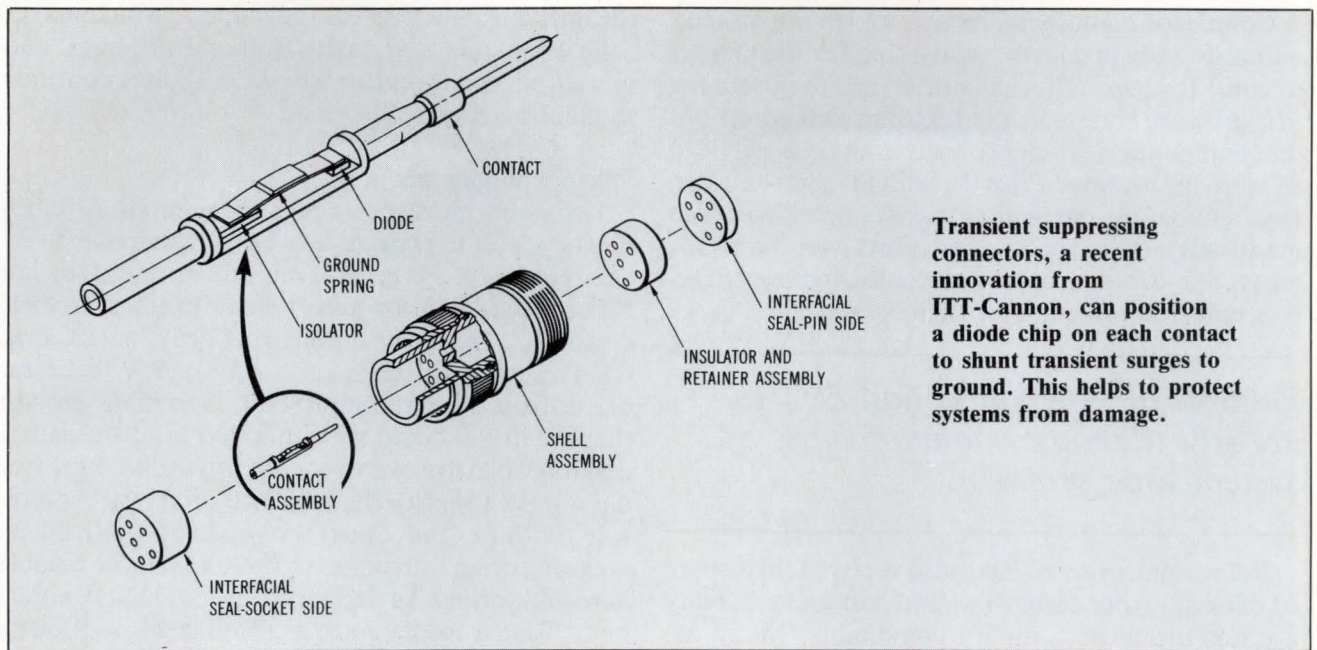
Screening out the bad

When deciding what level of screening may be required for a particular project, Viking's Hnatek offers these two tips. First, most makers of semiconductors and ICs develop processing "glitches" from time to time. Most problems are going to be "lot" problems, not overall production or design defaults. Second, new technologies need to be screened more thoroughly. Design flaws will show up in early production runs, and the processes are harder to control. As production experience is gained, these problems are worked out. Mature products have proven to be the most reliable.

Radiation resistant applications are also gaining speed. While the requirements for radiation resistance

Comparison of Two Microprocessors		
Parameters	HD64180	Z-80
Chip count	1	4 to 6 LSI and 6 to 10 TTL
Size	3 in ²	8 to 10 in ²
Power	75 mW	3 W (NMOS) 500 mW (CMOS)
Number of pads/pins	64	150 to 200
Cost	\$15	\$50

By reducing device and pin counts and lowering power requirements, VLSI design has improved reliability for the HD64180 microprocessor.



Transient suppressing connectors, a recent innovation from ITT-Cannon, can position a diode chip on each contact to shunt transient surges to ground. This helps to protect systems from damage.

may be critical to military and nuclear plant operation, many other earthbound systems and spacecraft are being designed to be resistant to nuclear and cosmic radiation. RCA's radiation hardness work began as a part of early research with silicon-on-sapphire substrates for CMOS ICs. "The insulating substrate provides the isolation required to prevent latchup of CMOS," explains Handen, "because the n- and p-channel devices are built on silicon islands on this insulating sapphire. Conventional CMOS doesn't have this protection."

But even "conventional" CMOS and NMOS devices are becoming more radiation resistant as the device sizes grow smaller, according to recent studies conducted by Intel Corp (Phoenix, Ariz). So are bipolar ICs, according to Joe Bradford, high reliability manager at Micro Power Systems (Santa Clara, Calif), where radiation effects have been under close study for over 10 years. Micro Power has just completed a study on its products' radiation resistance, and the results substantiate these observations. They show that ionizing radiation reduces the device gain of bipolar junctions. Micro Power has developed a silicon nitride passivation technique that significantly slows this degradation and a high temperature annealing process that also aids the radiation resistance of its ICs.

Mechanical problems

Passive components have taken their share of criticism because of poor reliability. But, of all of these components, systems designers seem most frustrated with interconnection devices, such as sockets and plugs. One solution has focused on reducing the number of connections in the system. As mentioned

earlier, VLSI helps to reduce the number of interconnects required on the board. But the problem of board-edge and intersystem connectors still remains. "Connector failures are still the most common cause of system-wide difficulties," claims Peter Beckett, senior product manager at Zilog Systems in Campbell, Calif.

In cases where a connector is essential, connector manufacturers are making efforts to limit connector failures. Joel Urban, marketing manager for ITT-Cannon (Fountain City, Calif) claims that it is "very likely that the reliability that computer designers have been asking for has been available all along. But many commercial companies have been confused about what is available." Urban emphasizes that there are over 72 companies now marketing connectors. "Too many companies" he says, "don't have any manufacturing facilities of their own, let alone a design department or a test facility. They just buy shells from one place, insulators and contacts from another, and go into the connector business."

Cannon's director of new product development, Judd Clark, adds that quality leads to reliability. "Know the vendor, not just their prices," he advises. "For example, know the packaging method—is each connector shipped individually within a crate or a box; or are they packed 50 pieces to the bag?" Clark maintains that the company that packs its connectors in a bag is begging for bent and pushed pins. Urban agrees and traces many of the bent pin problems back to vendors that do not have control of the parts manufactured for its connectors. The alloys used for pins is critical, for example, because if it is not controlled carefully it can result in pins that are too soft.

Connector manufacturers are not resting on their military-grade products and waiting for the market to come to them. They cannot afford to ignore the fast-growing computer field. Urban also points out that competition among connector makers will lead to more innovation. Price declines in metal-shielded D-subminiature connectors, for example, have lead many designers to specify these parts over the plastic parts. The shielding ability makes them more attractive, and the price makes them practical.

Failures of interconnection devices are still the most common cause of system-wide problems.

Relays and switches have also received their share of criticism from designers—and cost and reliability are not the most common complaints. Many designers use older electromechanical devices, instead of solid state relays, because of power requirements, driving ease, physical size, and contact resistance. The internal resistance of solid state relays causes considerably more heat to be generated during operation than metallic contacts.

But designers are turning to solid state relays for other reasons. Jim Antrim, president of Antex Electronics (Gardena, Calif) attests, "Many designers are finding that some of the unique attributes of solid state relays really enhance their system's performance. Features such as zero-crossing switching, photo-isolation, and very fast switching times more than make up for the minor inconveniences. Add

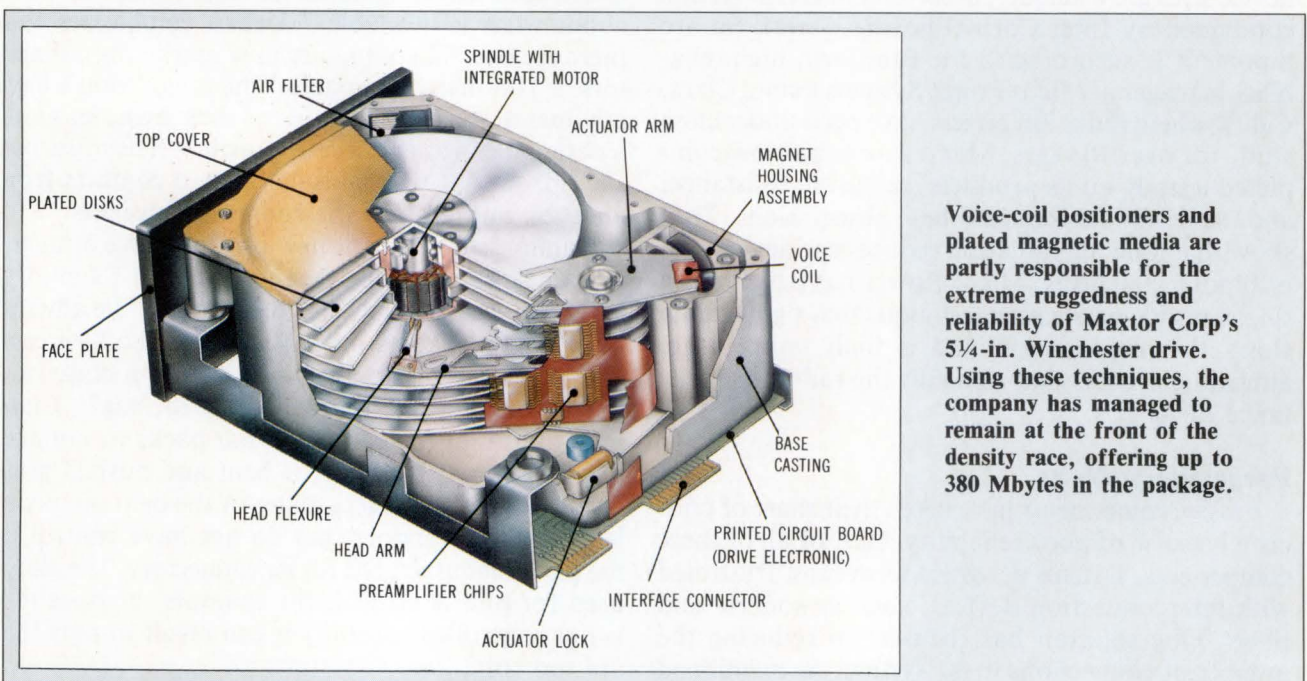
the unrivaled mechanical ruggedness, which makes solid state relays virtually immune to shock and vibration, and it is clear why sales figures continue to climb each year."

Reliable peripherals

Reliability must be sought throughout development cycle, if the system is to be of higher than average reliability. Peripheral manufacturers, too, are being pressed to bring more reliable products to their customers. Designers at Maxtor Corp (Santa Clara, Calif) performed tests on a series of Winchester drives from several manufacturers to make certain that the drives could withstand a 6-in. drop onto a desktop while they were running. Several of the drives did not even survive the half-inch drop test. As a result of those and other tests, Maxtor refined its manufacturing techniques to produce a more reliable hard disk drive. As designer Dave DeLauter points out, "Plated media and voice coil head positioners play a big part in the ruggedness of Maxtor's drives."

Maxtor is not the only manufacturer working to develop more reliable hard disk drives. But there is a word of caution on the subject. "The 5¼-in. drive makers are only now beginning to accumulate reliability figures, and there is no way the 3½-in. mean time between failures (MTBF) figures can be realistic," cautions Allen Taylor, a consultant with Computer Power (Midway City, Calif). Taylor believes that MTBF numbers for any disk drive have been guesses in the past. "If those numbers are important, it is best to verify the manufacturer tests," he says.

Taylor has witnessed several reliability problems with disk drives, such as one lot of drives with





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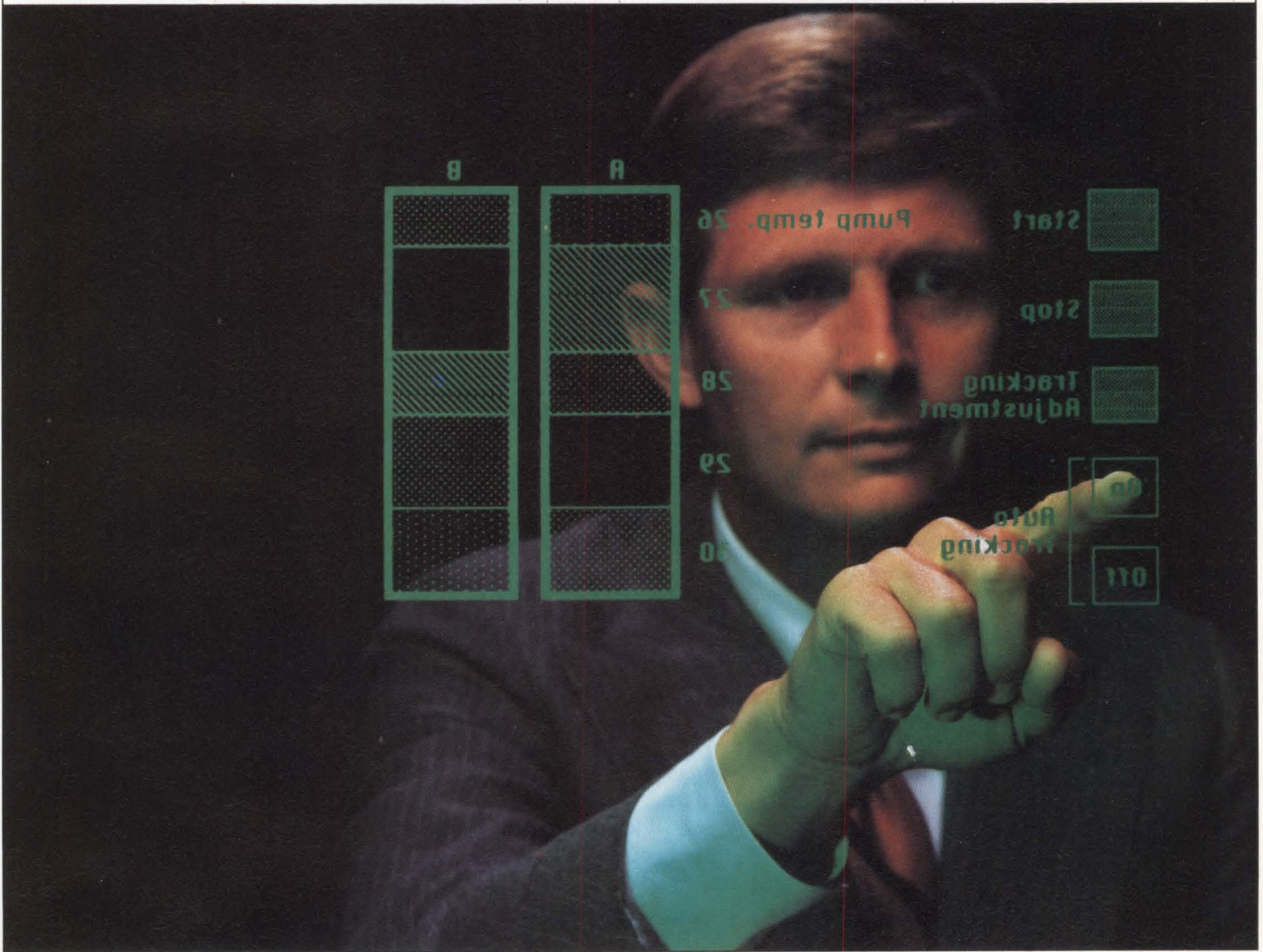
Which is the main reason Carroll Touch completely redesigned its line of touch input products.

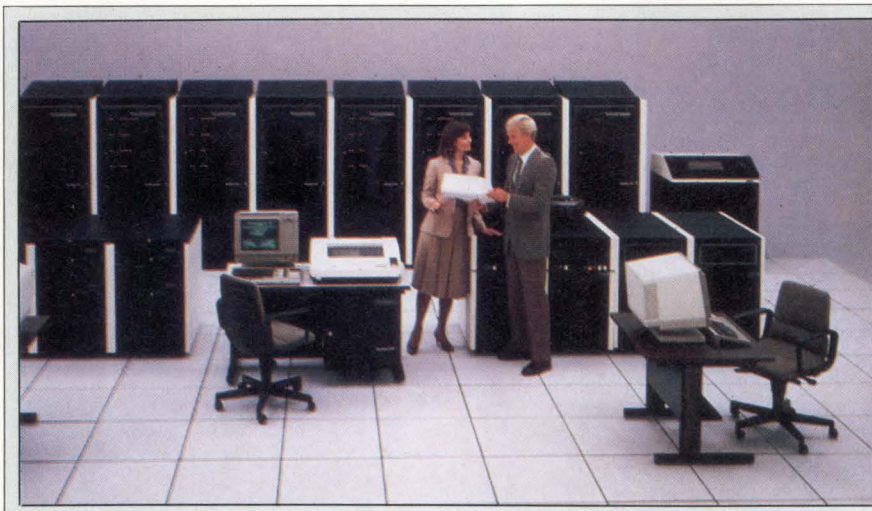
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uncured epoxy that eventually found its way into the read head, or one production run of disk controller ICs that were incorrectly sealed and later failed in the field. "But such problems are limited to specific production lots," he says, "and there is no better protection against these sorts of field failures than to find a disk drive vendor that stands behind its customers."

More hardware, better protection

In the physical implementation of high reliability systems, hardware redundancy has been an obvious approach for years. Adopted by NASA in the mid-1960s, the cost of hardware redundancy is a drawback for others. Some designers feel that it is better to pay for premium components and use careful screening techniques than to spend time and money repeating a task two or more times. Bucking that trend is Tandem Computers (Cupertino, Calif), which touts dual processors as a way to ensure maximum uptime on Tandem's transaction processing equipment. Taking the redundant hardware concept one step further, Tandem and other companies are now either producing or looking at system designs that use a higher level of redundancy.

According to John Wensley, founder of August Systems (Tigard, Ore), greater reliability can be gained by taking the redundancy scheme past two or three units. "But in almost every case there are cost limits. Triple redundancy is the optimal price/performance level at this time," he says. August has pioneered triple modular redundancy, in which "voting" is done by each of three processors. If a failure or even a disagreement occurs, the two agreeing modules can control the system, while the faulty module is replaced.

Zilog's Peter Beckett explains that reliability is a concern even in products that are not normally viewed as "high reliability." During the development

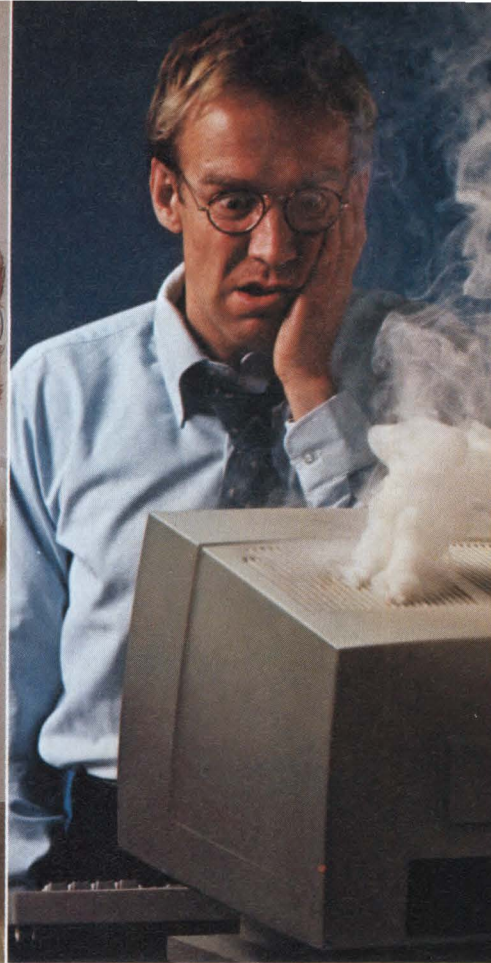
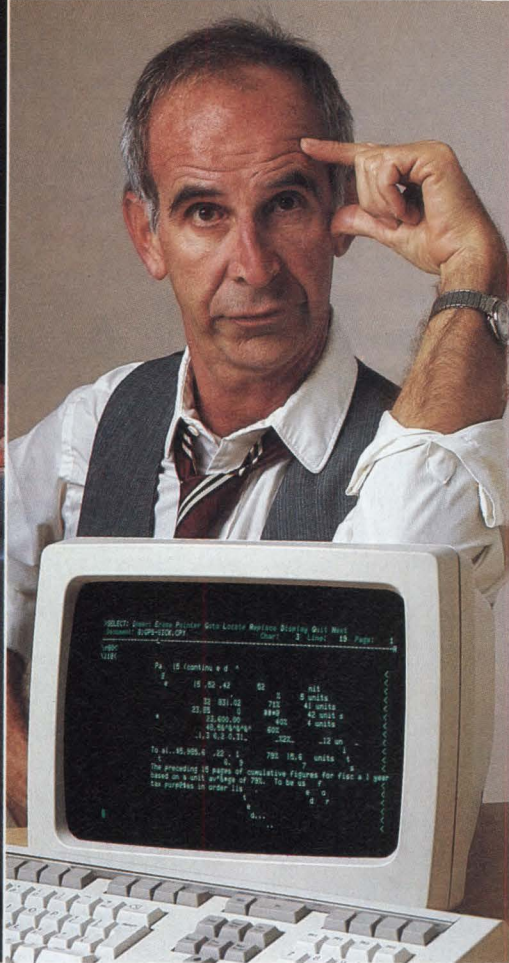
of the Zilog Series 2, for example, design decisions were made to enhance its reliability, although the Series 2 is destined for an office environment. "Supermicro computer users look for higher performance and more options, as well as high rates of dependability when purchasing new equipment," says Beckett. "Reliability is a broad term that can be interpreted in various ways depending upon the user. But in general, it means reduced routine maintenance and longer mean times between failure." Beckett believes this is extremely important to his company; "These improvements promote customer confidence in computer equipment, and continue to take on greater importance at the same time that the performance curve continues rising."

Three design aspects get attention

Reliability enhancements for the Zilog Series 2 were focused on three aspects of design—power supplies, cabling and connector protection, and system cooling. First, the use of centralized power supplies was increased in order to reduce problems associated with interactions between various independent power supplies within the system. Greater use of centralized supplies has been achieved without sacrificing support for satellite power supplies where control is enclosed to a centralized power distribution unit.

Second, the design engineers moved cabling inside the system chassis, in effect removing it from underfoot. They also have taken steps to reduce the number of connections between the active peripherals controllers of the system and the peripherals themselves. This effort includes internally mounted devices, such as disks and tapes, and external devices, such as terminals and printers.

Finally, the design includes specific steps taken to ensure consistent and even air flow over the active electronics within the system, including the main system boards, the power supplies, and all peripherals.



A. Once you're in the dark? B. During a total memory loss? C. After the smoke clears?

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By comparison with earlier designs, the Series 2 models provide a significant set of gains in even cooling and also in the noise levels associated with fans and blowers.

Emphasis on high capacity power supplies

Power distribution remains one of the most sensitive areas in any system. Random power surges often contribute to the loss of data or breakdown of a system. A key design goal for the Series 2 was to immunize the system as much as possible from external electrical interference. Historically, Zilog has used several single and multirail power supplies in its systems. But, in the newer design, there is a greater emphasis upon high capacity, multirail power supplies. This change minimizes the interaction caused by differential turn-on, turn-off times.

The system employs peripheral supplies where they are necessary. Thus, it operates with a control signal that originates in the main master power distribution unit. This unit controls all power satellites, including the system's nine-track streaming tape and any supplementary disk modules. Many new system designs feature low voltage circuitry—ac power can be applied to individual power supplies with the low voltage switch. This makes the low voltage switch less susceptible to having its contacts welded shut by the high currents encountered when applying full ac power through one contactor circuit.

The Series 2 also features near-simultaneous activation, in which the entire system starts up at the same time, rather than in two or three intervals. This activation process helps eliminate problems that can occur when signals pass from a controller to a device whose dc power is not yet within tolerance. This

near-simultaneous activation thus lessens the chance that a peripheral might "latch" and hold, leaving the user in a state of suspended abeyance. In addition, using solid state switching for ac into power units and controlling those solid state switches with a central control signal, significantly lowers the level of system interference susceptibility from ac line surges. Thus, when a peripheral is turned off it will not shut the system down.

High reliability translates into reduced routine maintenance and longer mean times between failures.

Series 2 functional specifications require the system to host more peripherals and users than its predecessors. This makes the dc power demand from boards mounted within the CPU greater than in previous Zilog systems, as well as in many other supermicro computers. The 5-V rail of the Series 2 CPU (the CPU also includes - 5-, 12-, and - 12-V rails) is rated to deliver up to 90 A. This lets the system support up to 40 user channels and a broad range of disk drives, cartridge tape drives, and industry-standard, half-inch, nine-track tape. The system also accommodates high speed, floating point processor hardware. Zilog's processor hardware accelerator consumes up to 18 A at 5 V. The improved dc demand capacity in the Series 2 removes constraints upon floating point hardware that existed in earlier supermicro models.

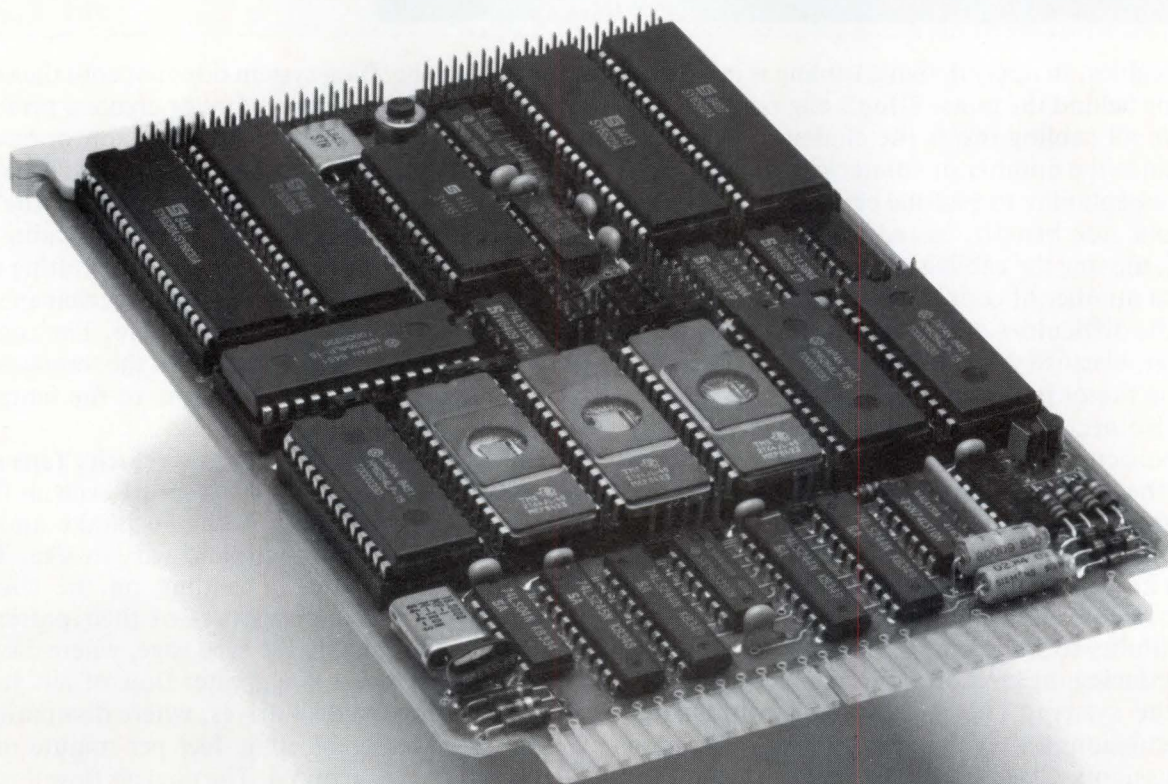
Another major consideration in the reliability of the new system was the placement and storage of



Triple modular redundant (TMR) hardware is offered by August Systems for applications that cannot tolerate a failure in the control system. In TMR, there are three control computers. If one of these computers fails, the two remaining computers can control the system while the failed unit is being repaired.

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CIRCLE 65



Outside cabling webs from the earlier Zilog system have all been moved inside the chassis of the new Series 2. Since the system is destined for an office environment, the chances of accidental unplugging is reduced, and the radio-frequency integrity of the system is improved.

system cables. In many designs, cabling is in disarray under or behind the units. Zilog's engineers decided to move all cabling inside the chassis of the Series 2 to reduce the number of connectors, limit the system's susceptibility to external electrical interference, and, as a side benefit, to reduce costs.

First, moving the cabling inside the chassis reduces the total number of connectors in the system, which limits the difficulties associated with connectors. In addition, because wear and failure of connectors is a critical factor in system malfunction, design engineers also decided to continue using the DIN standard Euroconnectors. Beckett calls this connector one of the highest quality industrial class of connectors currently available.

Second, having the cabling inside transforms the cabinet into a Faraday cage and creates a metallic closed system. This grounds the system, reducing its susceptibility to static interference while simultaneously reducing the level of radio frequency emissions from the system. The reduced susceptibility and lower emissions satisfy the Federal Communications Commission's Class B specifications.

Efficient cooling system

An efficient cooling system is another important design goal. In any high performance system, stress results if temperatures are not controlled. Thus, producing an even, adequate, and quiet flow of air over the cards housed in the CPU, and over boards, power supplies, and peripherals, is important in an effort to reduce heating.

Although the Zilog system does not cool the entire cabinet to a single temperature or create a perfectly even air flow, it does provide flow appropriate to dissipation levels. The design also prevents hot spots within and around key peripherals, such as the cartridge tape drive. In terms of temperature rating, the tapes in the cartridge have the lowest operating temperature (approximately 30 °C) of any element and are the weakest link within the system. The cooling system essentially tries to maintain the temperature at the fringes of the drive as close to the temperature at the center.

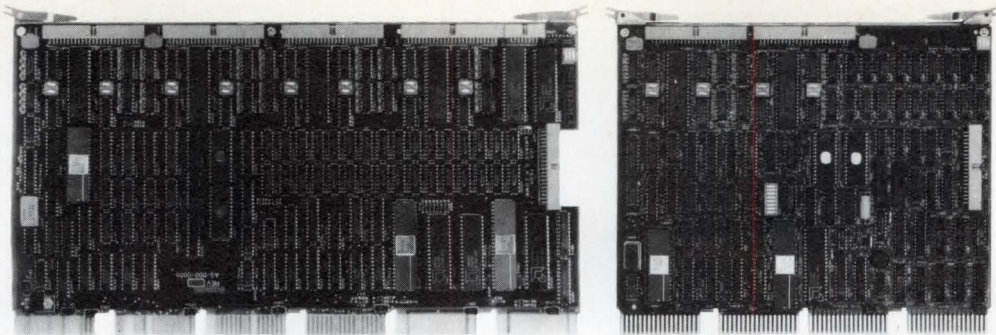
The system includes nine, low velocity fans strategically located and directed to ensure even air flow. The fans are located on both the intake and the exhaust sides of the system and vary in size. They operate differentially, depending on the cooling requirements and temperatures of their particular target. For example, in the card cage, where dissipation is highest, there is a greater flow of air. In the region housing the disk drives, where dissipation is lower, the number of cubic feet per minute of air flowing through is reduced. The even air flow through the card cage and across peripherals is a major feature of this new design.

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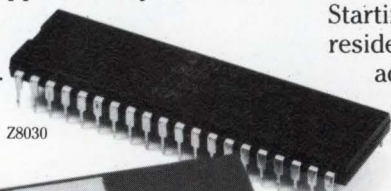
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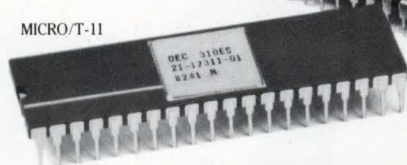
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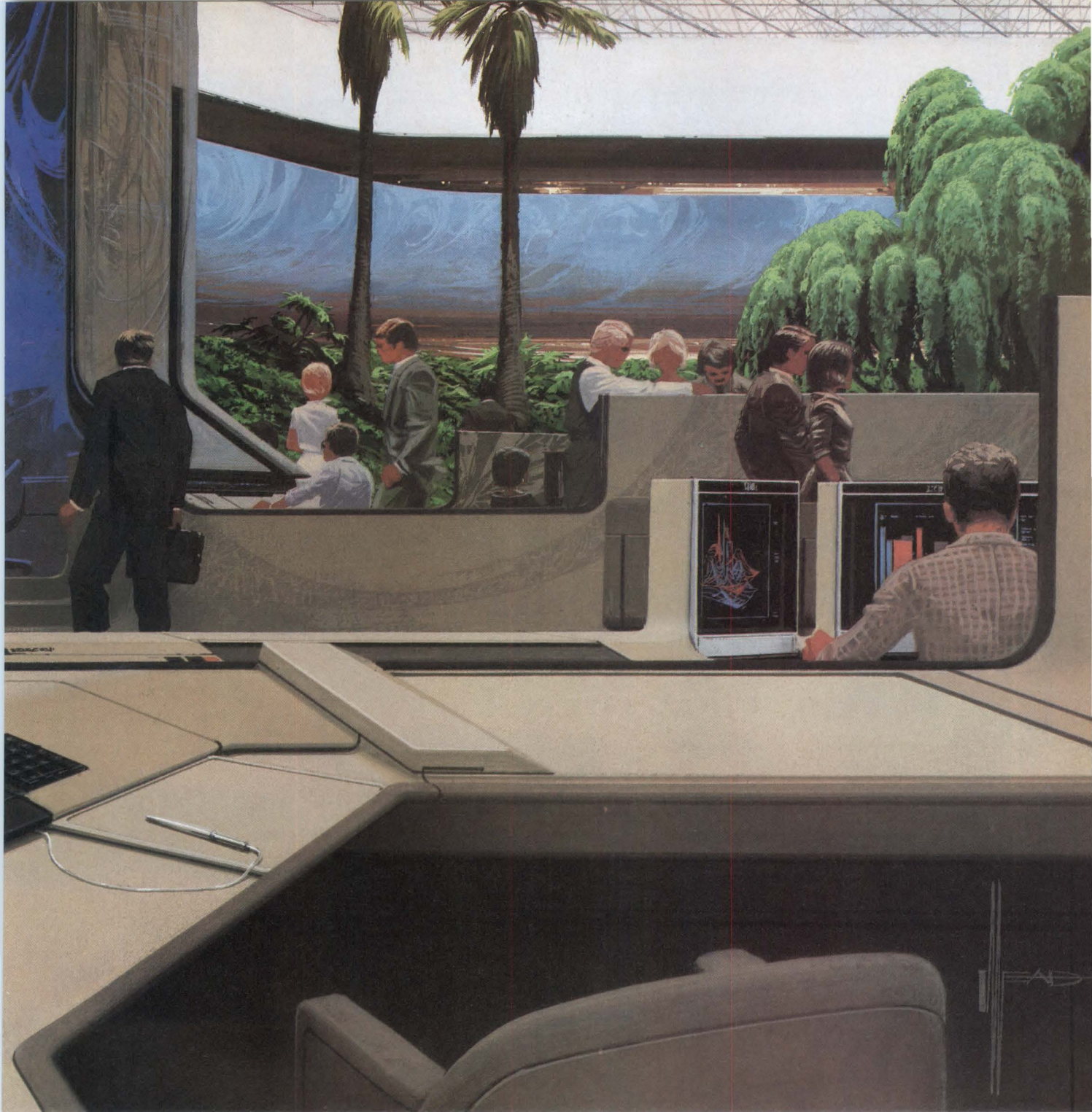
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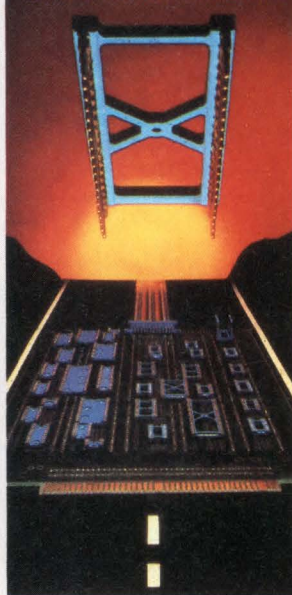
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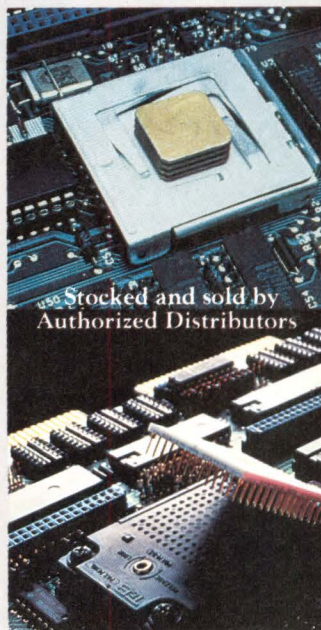
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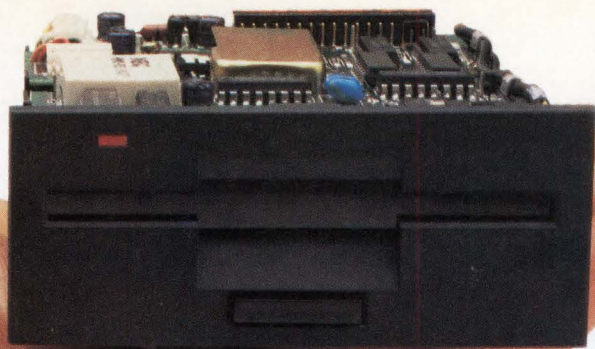
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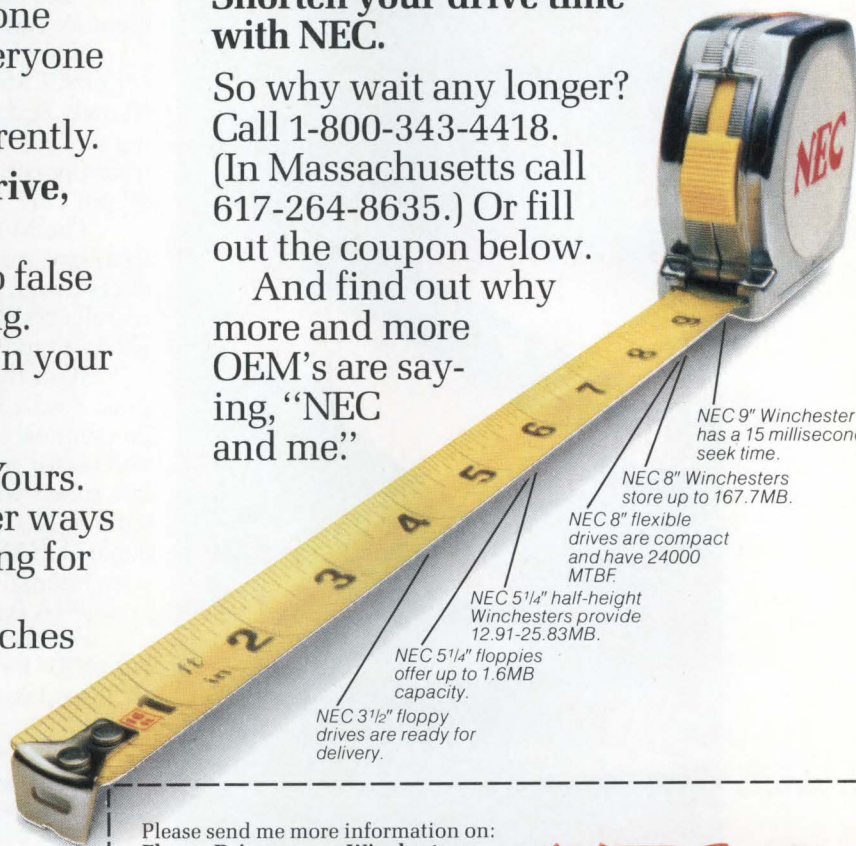
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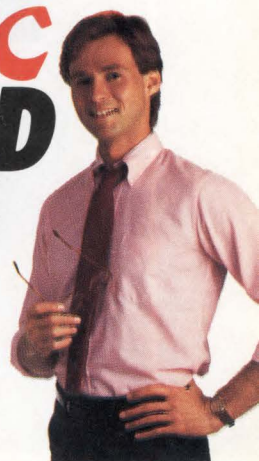
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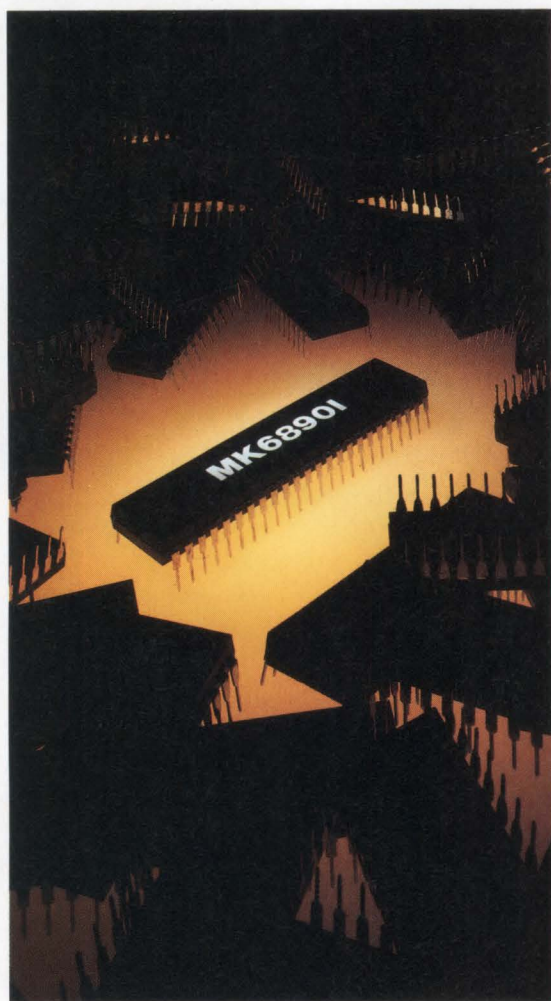
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CIRCLE 70



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REDUNDANT MODULES MAY BE BEST FOR CONTROL SYSTEMS

Despite the apparently higher price, triple redundancy can be the optimal trade-off of cost versus reliability in digital control applications.

by **John H. Wensley**

Faults are undesirable in every practical application. Once that proposition is accepted, the issue becomes how much should be spent to attain an "adequate" level of fault tolerance for a particular system. Because systems and applications differ widely, the techniques used to achieve fault tolerance differ just as widely. But one technique, redundancy, can be applied across the board.

Redundancy has a lot going for it. Redundancy can be applied not only at the processor or computer level, but also at any system level that may be critical—even down to sensors and cables. It also allows for some important trade-offs: uptime can be traded for cost efficiency, or cost can be traded for system errors where reliability is critical. In applications involving turbines, chemical reactors, or oil and gas separators, for example, even a momentary lapse in the continuous, accurate control of critical equipment can cause very costly damage or loss of life. In these cases, highly fault-tolerant controllers are the best choice, and the added cost is justified.

Dual redundancy is the most common fault-tolerant scheme. When a failure is detected in the pri-

mary system, a switch over to the secondary system is made. Then, repairs can be made on the primary system, allowing it to resume operation. In a dual redundant system, however, there is a discrete period when the system is in a failure mode and is not operational. During the switchover, there is a loss of control by the system and, possibly, corruption of data—both of which may later cause incorrect control of the process. And after the switchover, any corrupted data must be corrected and any lost messages must be retransmitted before control can be fully regained.

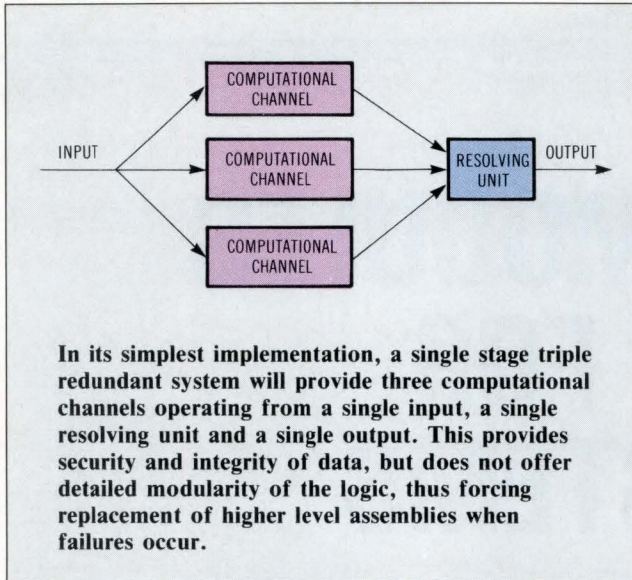
Since some time is needed to detect a fault and to switch from the primary system to the secondary system, system availability is less than 100 percent. The percentage of time that the system is available is determined by

$$A = 100 \text{ tt}/(\text{tt} + \text{st})$$

The time interval between failures is denoted by tt . The switchover time (st) consists of the time required to detect the failure, to switch over to the secondary system, and to start up the secondary system in a manner that recovers the control process. If the switchover is manual, this time can be several minutes, depending on operator alertness.

In some control applications, the time spent in the switchover or the momentary corruption of data cannot be tolerated. An approach to fault tolerance that addresses this problem is triple modular redundancy (TMR). In TMR, the control computer is triplicated

John H. Wensley is chairman and founder of August Systems, Inc (Tigard, Ore). He holds a BA and an MA in mathematics from Cambridge University.



and each of the three computers performs the same tasks and computations. At periodic intervals, they rendezvous and “vote” the results. If one of the computers fails in some way, a disagreement occurs and a majority selects the proper result. As a result, the system always provides the correct answer or instruction and the system’s operation is never delayed by a switchover. System availability with this approach is extremely close to 100 percent.

Fault-intolerant control systems

Some applications requiring this degree of system availability include: hazardous processes manufacturing, control of exothermic reactions (chemical or petrochemical), and the control of nuclear fuel reactors; processes that involve toxic substances, such as semiconductor manufacturing or nuclear waste treatment; processing of expensive products, such as drugs or fine metals; and remote or unattended installations, such as security, offshore oil and gas production, oil and gas transmission, and some in-plant rotating equipment. These applications cannot tolerate failure in the control system.

An example of a TMR fault-tolerant control system is the CS-330 from August Systems, Inc. The CS-330 uses three processors, three memory subsystems, and three I/O subsystems. The design includes the multiplexers and voters needed to implement TMR fault tolerance. Each processor can read the memory in the other two processors, but cannot write to it. This ability lets each processor check, but not corrupt, the computed results and data.

Voting occurs on all input data, computed results, interrupt responses, and output commands. Output commands can be monitored by additional inputs to verify that commands were sent and interpreted properly by the process under control. Voting is

accomplished in the control system’s hardware and in its operating system’s software. The application control software that the user develops is not cognizant of the computer system’s fault tolerant nature.

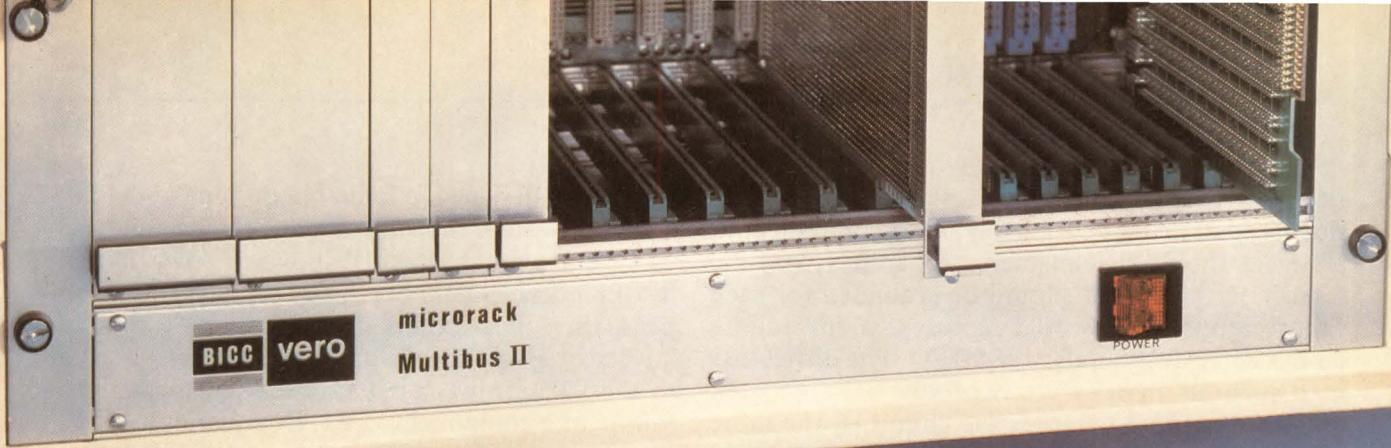
One diagnostic feature of the CS-330, called latent fault detection, allows the detection and identification of faults in the computer system before faults can accumulate and become an unrecoverable dual fault. The functional ability of each module is tested to guarantee the availability and reliability of the system while the process under control is in operation. If a module or component in the system fails, it can be repaired or replaced without interrupting control or stopping the process under control. After this “hot repair,” the still-functioning portion of the computer system brings the repaired or replaced module online and provides the data necessary to reestablish a three-way agreement.

All of the features outlined—TMR, latent fault detection, and hot repair—are required to produce a computer control system that can handle applications whose failure cannot be tolerated.

In the simplest, or single-stage TMR system, data is presented uniformly to three independent computational channels. At the conclusion of a computation by each channel, the results are sent to a voting unit to resolve any disagreement between the results computed by each channel. With all three channels operating correctly and with no fault in the voter, the result from the three channels will be delivered from the system. Also, if one computational channel delivers an incorrect result, and if the voter contains no faults, then the output will be the same as produced by the two good computational channels. In addition, if all computational channels are free of faults, and produce the same results, but if the voter contains a single, internal fault, then the output will agree with the results from the three computational channels.

A more complex, multistage TMR system can be devised where each computational channel is broken down into a sequence of subsystems or stages. Data from each subsystem in a channel is exchanged with data from the corresponding subsystems in the other channels and a resolution takes place, according to the principles outlined for a voter, for each subsystem. Greater reliability can be achieved with this architecture because it can tolerate many combinations of double faults. For example, a fault in a subsystem combined with a fault in some other subsystem in another computational channel will not corrupt the output. Although such an architecture has great merit, a simpler structure lends itself to analyzing the benefits of fault tolerance more easily.

Components can fail in many different ways. Even a simple component, such as a resistor, can fail open



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circuit or short circuit; or the resistor can shift outside its specified value. Ideally, each component in a system should be considered separately, and the effects on the system should be evaluated for each failure mode. This would represent a full failure modes and effects analysis (FMEA). The difficulties with such an analysis are twofold.

First, the more complex the circuit is, the more costly the analysis will be in terms of manpower and time. Second, the specifications for all the components used in a system may not be known. Even if the specifications for a particular component were known, the manufacturer can change them without notification. Such changes may totally alter the failure modes and their effects on the system. For these reasons, a completely detailed FMEA is usually impractical. A more limited analysis can be carried out, however, in which certain conservative assumptions are made about the failure modes. In such an analysis, it is assumed that every failure mode produces the worst system effect. With this assumption, an estimate is made of the extent of a failure.

In a multistage, triple redundant system, such an analysis might evaluate the effects of a failure of the resolving unit between the first and second subsystems in a channel (A1 and B1, for example). Each component of that unit is analyzed to see if it can corrupt the operation of the units that it is connected to; namely, the preceding subsystems in the other channels (A2 and A3) and A1 and B1. If the circuit

is properly designed, a failure in this unit should not adversely affect the subsystems A1, A2, and A3.

A failure could affect B1, however, by providing it with incorrect data or control signals. If this happens, then those components of the unit that can adversely affect the operation of B1 are allocated to the B1 unit because the effect is the same as a failure of a component in B1. Boundaries may then be drawn around portions of the total system to show the extent of a fault. In this example, the boundary would include B1 plus those portions of the preceding resolving unit that could corrupt the operation of B1. Having drawn such boundaries, it is now possible to compute the failure rate of all the components within the boundary.

Evaluating reliability models

Reliability models can be used to derive predictive data for the two most important reliability measures: the probability of system failures per hour (P_f) and the system availability (A), which is defined as the ratio of the length of time the system is operational to the total time the system has been in use.

These models are similar to Markov models, in which nodes represent the states in which the system can reside, and arcs (or paths) between the states represent the transitions from one state to another. In a pure Markov model, the transition from one state to another must depend only on the current state of the system and must be independent of the

Calculating key measures of reliability

Two important measures of reliability, system failure rate (P_f) and system availability (A) can be calculated using a three-state reliability model. In the first state, the system operates with all channels, producing correct results. The system remains in this state until a fault occurs. If the rate of faults occurring in each of the three channels is p , the rate at which the system enters the second state is $3p$. A single fault exists in the second state, but it is tolerated and the system as a whole continues to produce correct results. Repair action begins on entering this state and takes a time equal to the mean time to repair (T_r). During this time, a fault could occur in one of two remaining faultless channels. The possibility of this occurring is $2pT_r$, while the probability of successful repair is $(1-2pT_r)$. If a second fault occurs, the system enters the third state and system failure occurs. If P_3 is the probability (over time, t) of being in the failed state, the state model yields

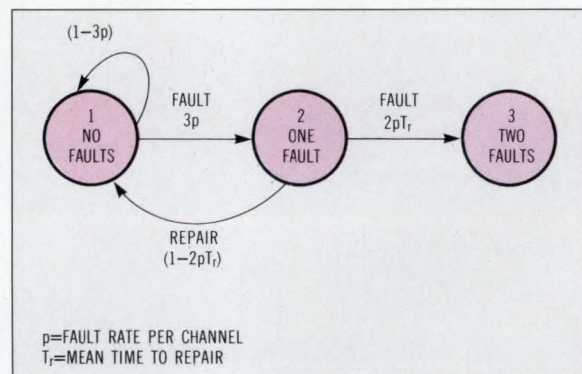
$$P_3 = 1 - e^{-6p^2T_r t} \approx 6p^2T_r t$$

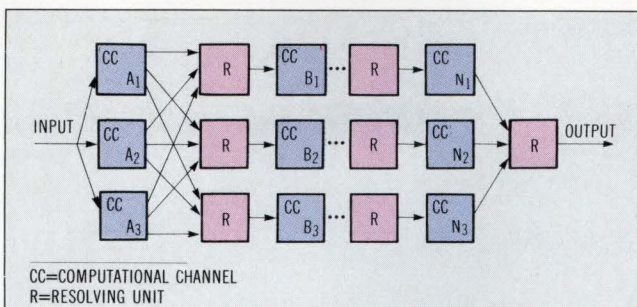
This approximation is justified under the assumption that $6p^2T_r$ is much less than 1. The next assumption made is that when the system enters

the third state, a new repair action is initiated that will require the time T_r (the second failure can be repaired in parallel with the first). Other assumptions concerning repair times could be made, however, based upon the availability of personnel and spares and other logistic factors. The key reliability measures, P_f and A , can now be derived:

$$P_f = 6p^2T_r \text{ per unit time}$$

$$A = 1 - 6p^2T_r^2$$





A more modular, but more complex approach to redundancy allows more thorough cross checking of results. Replacement and repair costs can also be minimized since lower level units are replaced.

prior state transitions that may have taken place in the system.

This is not true for all "transitions" involved in the models for redundant systems. If the system is in the state of being repaired, for example, then it will leave that state when the repair has been accomplished. This depends on the time at which it entered the state and thus is dependent on the prior state history. The analysis technique used makes sufficiently accurate predictions under certain conditions. For example, the probability that a second fault could occur while a first fault is being repaired is often considered, but the probability that a third fault occurs in that period is usually ignored.

Spare parts model

For any realtime control system, it is common policy to maintain an inventory of spare parts at the installation. A spare parts model deals with the logistics of the spare parts inventory and ways to reduce inventory costs to a minimum. If too few parts are kept, however, a plant shut down because of parts unavailability could become an excessive operating cost. The real objective is to minimize the total cost.

For a particular system design, let

- m_i = number of part type i in system
- n_i = number of part type i in spares inventory
- c_i = cost of spare type i
- t_i = delivery time of part type i
- p_i = probability of failure of part type i
- n = total number of different types of parts
- C_d = cost per hour of downtime of the system
- I = interest rate (expressed as a fraction) prevailing.

The costs associated with spare parts inventory are composed of two components: the cost of the spares, and the downtime costs because of unavailable spares. The cost of spares is

$$C_s = I \sum_{i=1}^n n_i c_i$$

The cost due to lack of spares is

$$C_{ls} = 8760 C_d \sum_{i=1}^n (m_i p_i t_i)^{n_i + 1} \text{ per year}$$

One more model that is important is a financial one that analyzes the initial capital costs associated with the acquisition of a particular system, fault-tolerant or otherwise, and the annual costs (which include the operating costs, maintenance costs and failure costs) associated with the system.

The acquisition costs and operating cost are, in principle, the most straightforward to determine. The acquisition cost is the simple sum of the hardware cost, software cost, training costs, installation costs, commissioning costs and initial spares costs. The annual operation costs consist of essentially the personnel costs and the supplies costs.

The determination of maintenance costs is more complicated and requires the evaluation of the cost of repairs per year:

$$C_r = 8760 \sum_{i=1}^n m_i p_i (l_i + C_r)$$

and the total cost of spares— $C_s + C_{ls}$ (defined earlier)—where l_i is the labor cost associated with repair of unit i . The annual cost of maintenance is the sum of the cost of repairs and the cost of spares. Failure cost is composed of two parts: the cost due to system failure, such as spoiled material, damage to equipment and so on; and the costs associated with the downtime that occurs after failure. These include repair of any damaged equipment, and not just repair of the control system. Also included in these costs are such factors as lost revenue, excess labor, loss of orders due to nondelivery. If C_d denotes cost per hour of downtime, and C_c denotes the one-time cost of system failure, the total cost of a failure, C_t is

$$C_t = 8760 6p^2 T_r (C_c + C_d T_r) / \text{year}$$

It is now possible to determine, for each possible system (fault-tolerant or otherwise) the total annual costs and derive from it the return on investment of the original acquisition cost. By this means, alternative system approaches can be examined objectively. In particular, the savings derived from the use of a fault-tolerant system, through a reduction in the total cost of failures, can be balanced against the extra cost of such a system.

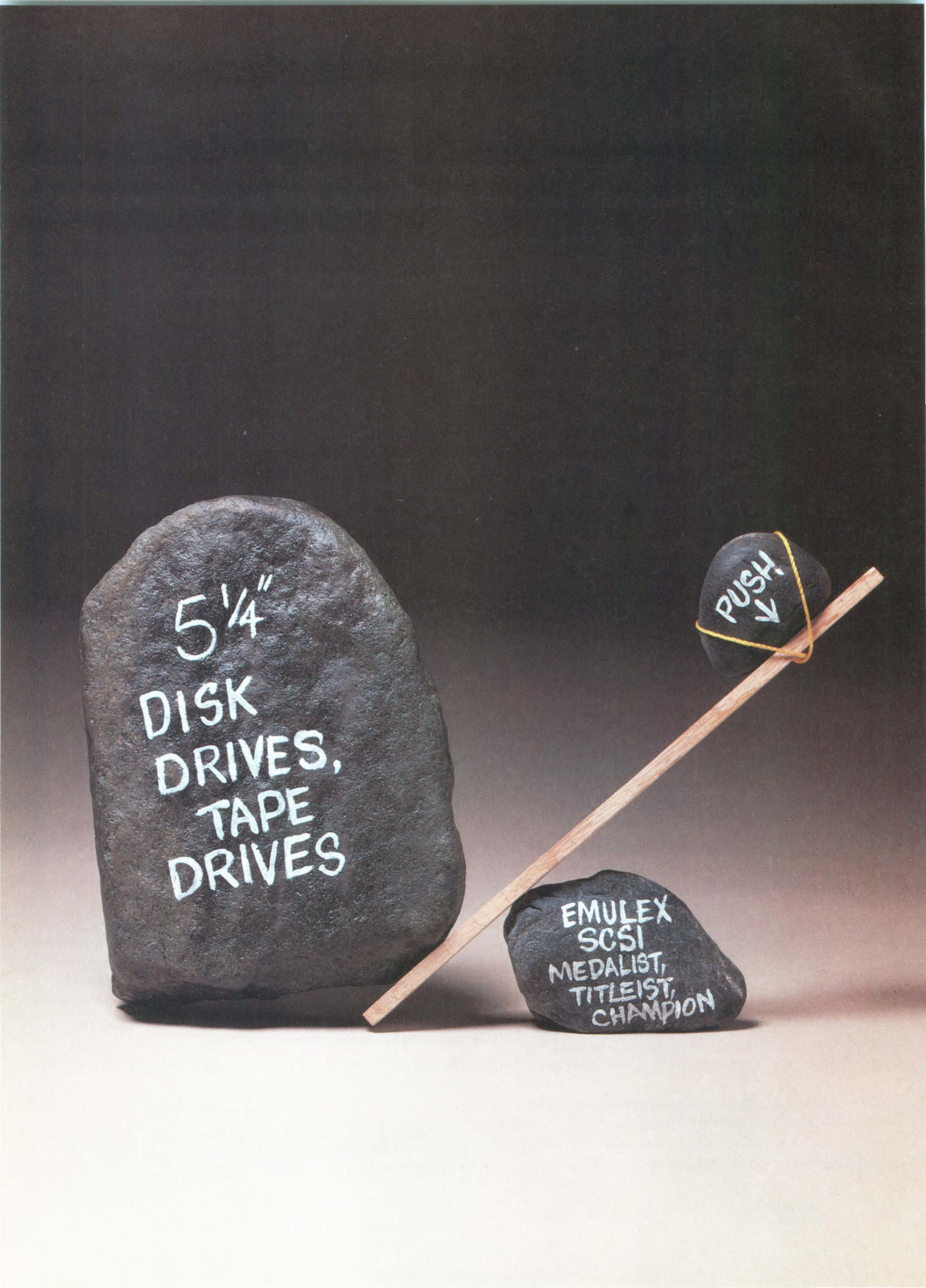
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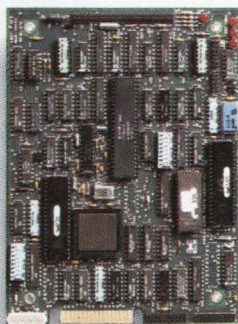
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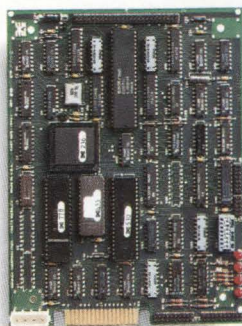
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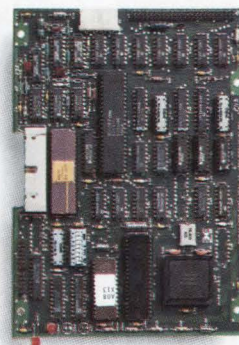
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SHADOWING BOOSTS SYSTEM RELIABILITY

Using the advanced data protection capabilities offered by shadowing techniques, designers can bypass conventional memory backup procedures.

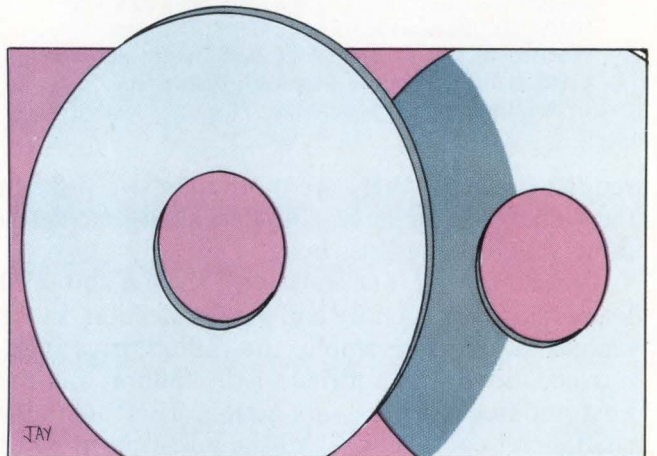
by **Kenneth H. Bates** and
Marvin TeGrotenhuis

Shadowing, a method of online backup storage, offers high data reliability and protection in disk drives without burdening the host computer. The shadowing technique can also improve response time and data throughput while increasing the number of I/O requests handled per second. The technique achieves these performance gains because it dynamically creates and constantly maintains identical data images on two or more magnetic disks. It does not copy disk images onto backup disks either continuously online or periodically offline. Except for human error or multiple failure, shadowing provides enough data protection to eliminate the need for conventional backup procedures.

One mass storage server that uses the shadowing technique is the HSC50 from Digital Equipment Corp. This server marks the first implementation of off-host shadowing at DEC, and server-based shadowing is featured as part of the enhanced VMS operating system. As an intelligent standalone controller, the HSC50 can manage a subsystem comprising as many as 24 magnetic disk units. The server

Kenneth H. Bates is a principal software engineer at Digital Equipment Corp (Colorado Springs, Colo). He is responsible for the HSC50 disk and tape controller.

Marvin TeGrotenhuis is a consulting software engineer at DEC. He implemented shadowing in the HSC50 server.

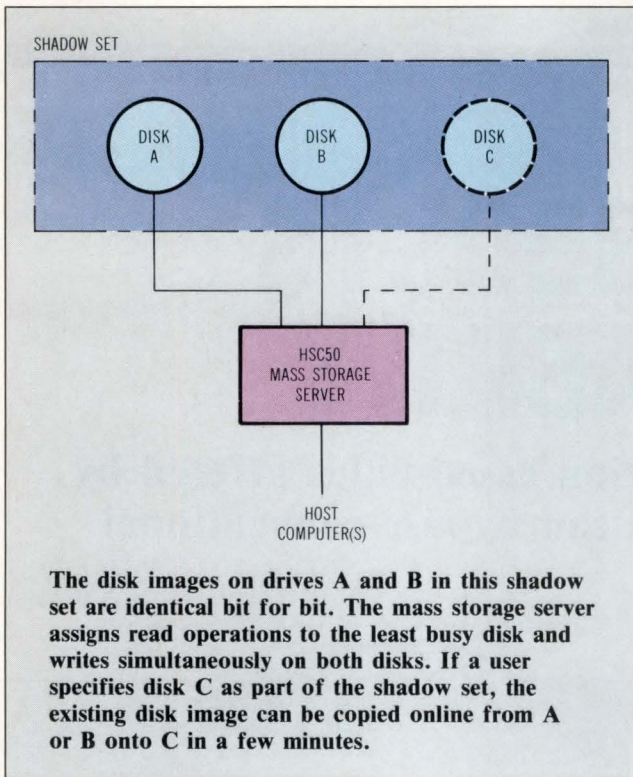


can also handle tape units, although tape shadowing is not provided. Moreover, the server performs the error handling, availability, diagnostics, and maintenance functions defined by DEC's Digital Storage Architecture (DSA).

Inside the shadow set

Shadowing uses a set of two or more disk images that are identical bit for bit. The set is maintained continuously by writing on all disks and is accessed by reading from any one of them. One or more hosts can consider a shadow set a single disk unit. All data transfer tasks beyond standard read/write commands are handled within the mass storage subsystem. Among other tasks, a mass storage server such as the HSC50 copies a write request onto all disks and selects the optimal disk for a read.

The process of reading a shadow set takes place at three levels. At the first level, the server assigns a read operation to the disk that is the least busy when a read request is taken off the server's master



request queue. If there are more than two disks in the shadow set, the server considers all disks to determine which is the least busy.

The shadowing functions at the second and third levels improve reliability and data protection. In the second level, for example, the failing drive is removed, the host is notified of the failure, and the host initiates any necessary action. This maintains shadow set consistency, and the host is notified of the change. Even if data cannot be read from a particular logical block on one drive, the server will shift the read for that block to another drive in the shadow set.

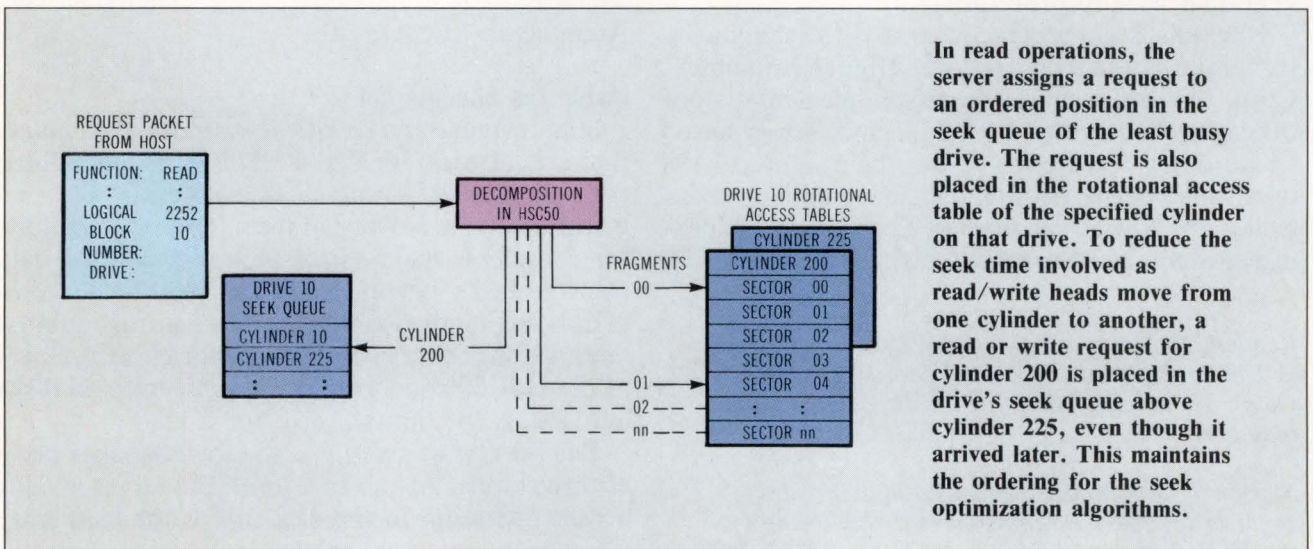
To maintain the shadow set, a third level of shadowing provides self-repair. Besides shifting reads to another drive, shadowing will write the good data on the second drive back into the unreadable block on the first drive. This process is transparent to both the host computer and the user. For the sake of reliability and data protection alone, designers rarely need to have more than two disks in a shadow set.

Handling transfer requests

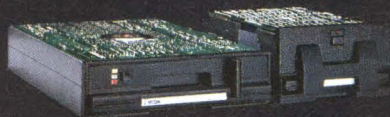
The HSC50 server, for example, maintains a constantly changing master request queue that has potentially hundreds of read/write command packets. The packets, formatted according to the DSA's mass storage control protocol (MSCP), may all come from a single host or from any host in a VAXcluster system. Each MSCP packet identifies the individual disk or shadow set to be accessed, the logical block number that will begin the transfer, the number of bytes to transfer, and whether the access is a read or a write.

With or without shadowing, the server can accelerate data transfers between a host computer and mass storage subsystem by using two DSA-defined capabilities: cylinder-to-cylinder seek optimization and minimized rotational latency on the target cylinder. Transfer requests, for example, are taken from the master queue on a first in, first out basis. The server then puts each new transfer request in an ordered position in the seek queue of the assigned drive. Each new transfer request is also put in the rotational access table for the specified cylinder in that drive. Since data transfer time is relatively short, the main objective in seek optimization is to reduce the seek time involved when the read/write heads travel from one cylinder to another.

Rotational latency is minimized by ordering the requests in the cylinder's rotational access table.



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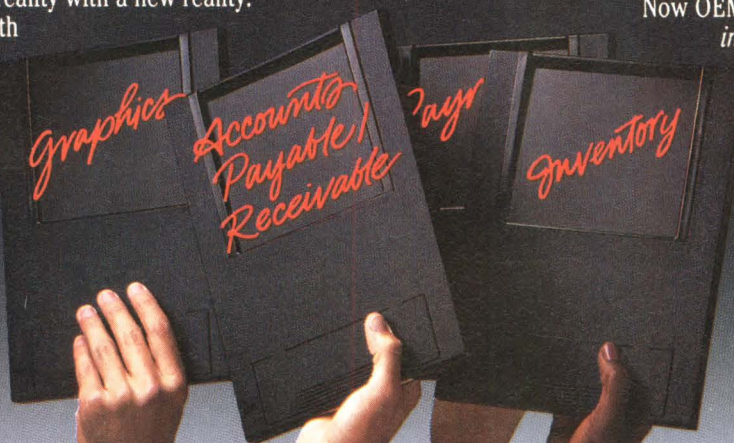
The central issue is no longer just more data. It's *more data dynamics*. And Winchester's aren't really dynamic at all. Consider "wait your turn" access, or the need for lots of user "system savvy." Consider time-consuming backup and restore. And consider the ever-present risk of expensive head crashes.

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IOMEGA HAS REMOVED CAPACITY AS THE MASS STORAGE ISSUE.

(Rotational latency is measured as the time from when the heads reach the cylinder to when the data transfer begins at the first sector on the designated track.) The sector closest to the head position is the first transfer executed. Other reads around the track are then handled in first-sector sequence. A sector contains 512 bytes, the block size in data storage for VAX computers. Longer requests can mean longer rotational latency—requests spanning a full track of data average one-half track or one disk revolution of latency. In DEC's RA81 drive, for example, one track contains 51 data sectors with a total data capacity of 26,112 bytes.

Longer requests are decomposed into equal fragments, each a few sectors long. The read or write transfer then begins at the first sector of the next fragment that becomes available under the appropriate head, rather than at the first sector of the entire request. For long transfers, the four-sector fragments

mean that average rotational latency is reduced to two sectors (about $653 \mu s$ on an RA81 drive).

Requests are transferred from a seek queue to the drive according to the more effective of two seek optimization algorithms: the elevator algorithm and the C-scan algorithm. The server chooses the appropriate algorithm according to the number of requests in the seek queue. For seek queues with fewer than five requests, the elevator algorithm goes from low to high cylinder numbers and then back again in sequence from high to low. In other words, it changes direction like an elevator. For seek queues with more than seven requests, the C-scan algorithm proceeds from low cylinder numbers to high, going directly low again to repeat the sequence. The sequence is, therefore, in one direction only. A queue depth of six maintains the algorithm previously in effect.

Requests going to a drive from the seek queue are placed at the end of a drive queue that is only two

Performance figures tell shadow story

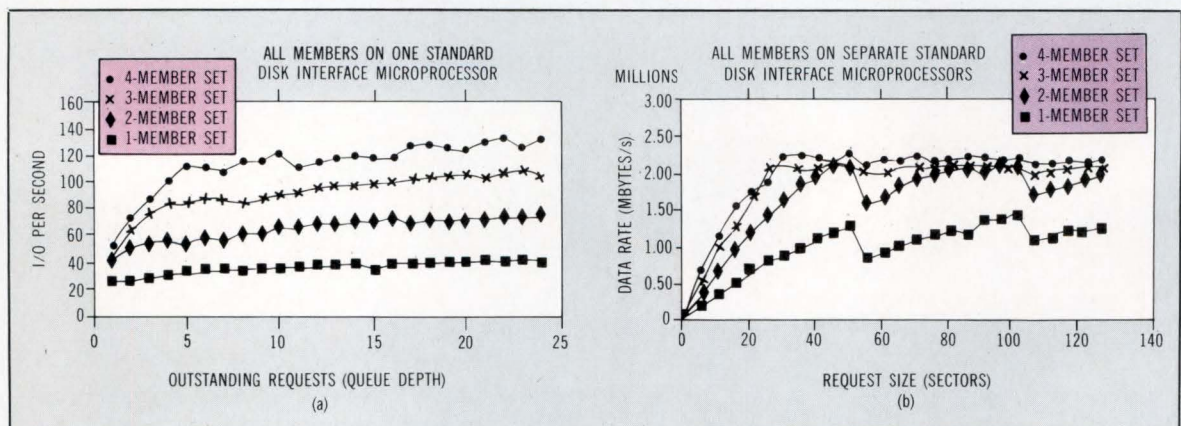
Shadowing improves performance by handling read requests in parallel. Consider, for example, when read operations per second are plotted as a function of "seek queue" depth for shadow sets with one (unshadowed), two, three, and four members (a). In this case, the disk drives are DEC's own RA81 units linked via a high speed computer interconnect to a VAX-11/780.

Due to seek optimization (which functions with or without shadowing), the more work the server has to do (for instance, the more requests there are in the seek queue), the more read requests it handles per second. The difference in performance between one-member and two-member sets results from the server's added function of selecting the least busy drive. This function becomes more effective as the number of drives in the shadow set increases to four. In this case, performance triples.

To analyze the data transfer performance for reads, the data rate in megabytes/s can be plotted

as a function of request size in sectors (b). In the test, 1000 I/O requests were run for each rate measurement. With or without shadowing, the overall data throughput increases with request size. Adding members to the shadow set increases the throughput progressively. There is very little difference between two-, three-, and four-member shadow sets because the transfer rate has reached the capacity limit of the single VAX-11/780 host. If more than one host were linked to the computer interconnect, the curves for three- and four-member sets would be significantly higher.

Individual tests on writes show that I/O operations per second are essentially unaffected by shadowing. Data rates for writes are also unaffected for request sizes up to about 20 sectors. Above that, the available number of data buffers somewhat limits multiple writes. As a result, the write transfer rate actually decreases relative to the size of the shadow set.





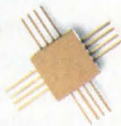
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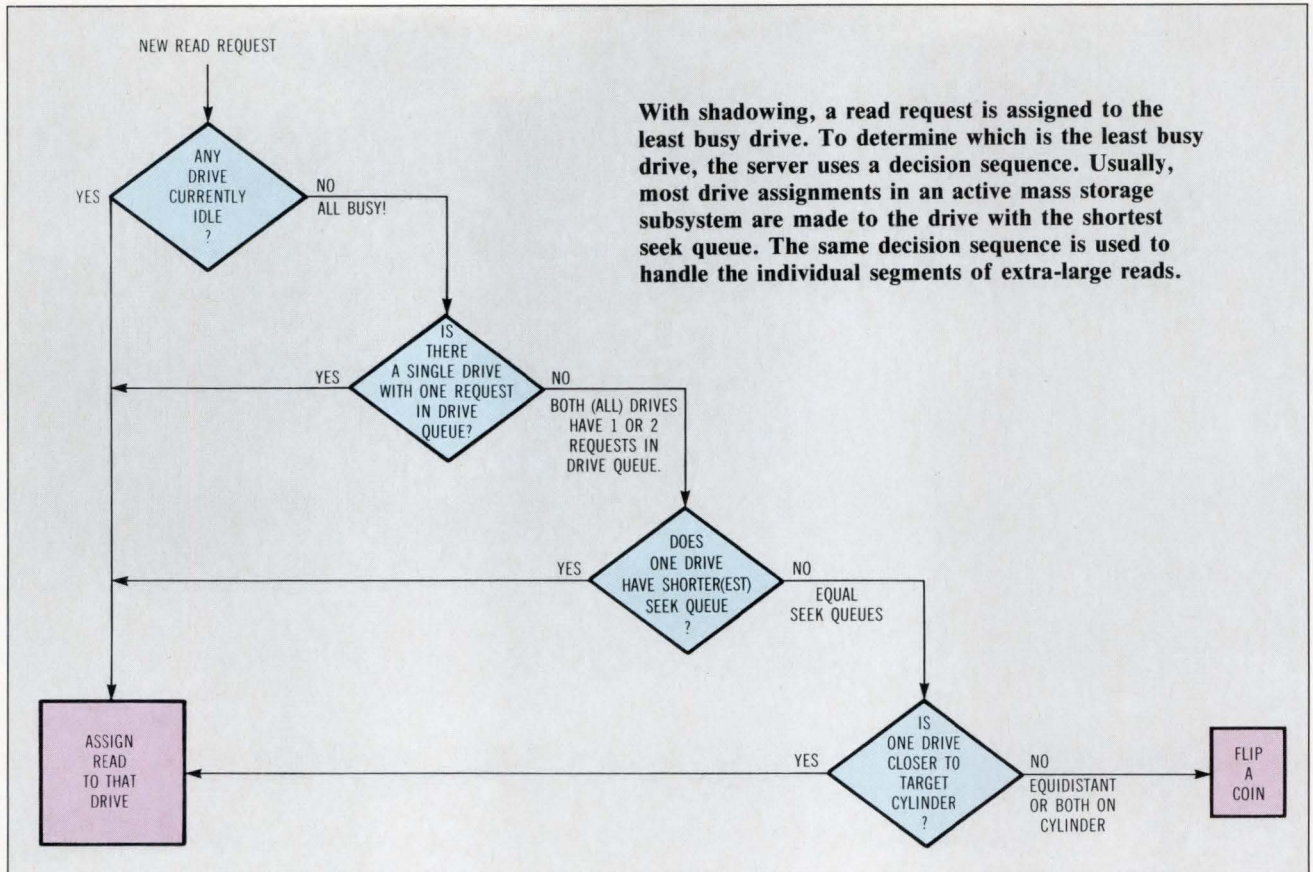
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requests deep. The next request selected by the seek algorithm is always ready at the end of the drive queue. Having such a short drive queue ensures that the transfer sequence on a drive is always sensitive to changes in the order of requests within the seek queue.

Read requests and the least busy drive

Requests may involve reading large amounts of data that extend beyond the sectors on a single track. Such data may even cross cylinder boundaries one or more times. For example, the RA81 drive has 14 platters and thus has 714 sectors per cylinder. Without shadowing, a read spanning three cylinders involves a sequence of seek-transfer/seek-transfer/seek-transfer on the same disk. This neglects the short rotational latency before each transfer. In a shadow set, the same large transfer breaks into segments whenever cylinder boundaries are crossed. Each segment is treated as an independent read request.

In a three-disk shadow set, the read requests involving cylinders 1, 2, and 3 are likely to be assigned to separate disks. Total read time equals the time required by the disk with the longest seek-transfer time. Clearly, the reduction in total seek time for extra large reads is substantial. The effect of transfer time is negligible because it is far shorter than seek time.

Another consideration is how requests are assigned to the disks controlled by the server. Without shadowing, a read or write request is assigned to the single drive that is addressed. With shadowing, however, a write request is duplicated for all drives; a read request is assigned to the least busy drive.

The server determines the least busy drive through a decision sequence. Most of the drive assignments in a typically active mass storage subsystem will probably be made to the drive with the shortest seek queue. Although the read requests in the seek queues can vary widely in length (and thus in transfer time), minimized seek time remains the prime goal. Once in its assigned seek queue, a read request is chosen for the drive queue according to the appropriate seek optimization algorithm.

Individual segments of extra-large reads are handled through the same decision sequence. When a read operation reaches the end of a cylinder (or when the server's decomposition resources are temporarily exhausted), the remainder of the read is treated as a new request. It is placed in the seek queue for the least busy drive. If that segment also reaches a cylinder boundary, its remainder is evaluated and assigned. The process ends when the remainder is less than a cylinder long.

A mass storage server manages the shadowing process according to policy established by the user

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system. The user system creates and dissolves shadow sets; the host recognizes each set as having a unique virtual unit number. All members of a shadow set must be controlled by the same server.

Users can add and remove disks from a current shadow set and shift removable disks in a set from drive to drive. For example, if one drive goes down for an extended time, the disk can be moved to another drive (after redefining the shadow set). If a disk fails, a new disk can be mounted on the drive and copied online from another disk in the shadow set.

Shadow set members can be configured to hold data in areas not recognized as part of the shadow set. Hosts can write and read in these areas (which can be any size and in any storage location) by addressing the disk itself rather than the virtual unit number. Data in an excluded area might include the unique name of the disk, the disk's operating history, and the identities of the other disks it is associated with in the shadow set.

If a new disk is added to a shadow set, an exact image could be made in the traditional way by shutting down the drives and copying the current disk image offline from a drive already in the set. To avoid losing mass storage subsystem availability for a minimum of 15 minutes of offline copying, the user can request online copying—the mass storage server continues to write new data on both disks. At the same time, the server transfers stored data from an existing shadow disk to the new disk. Reads are made from the shadow disk or from the new disk during copying, as long as the area to be read has already been copied.

Online copying is very fast—it can reach the theoretical speed of disk I/O transfers. It can thus minimize the performance degradation caused by added server tasks. Host-managed offline copying is necessarily much slower because of the extensive communication involved.

While server-based shadowing is provided with the HSC50, host-based shadowing is provided by DEC's micro-based UDA50 intelligent disk controller. Although it performs most of the same DSA-specified functions as the HSC50 server, the UDA50 does not itself have shadowing capability. Shadowing is therefore controlled by a shadowing server embedded in the VMS operating system's disk class driver on the host.

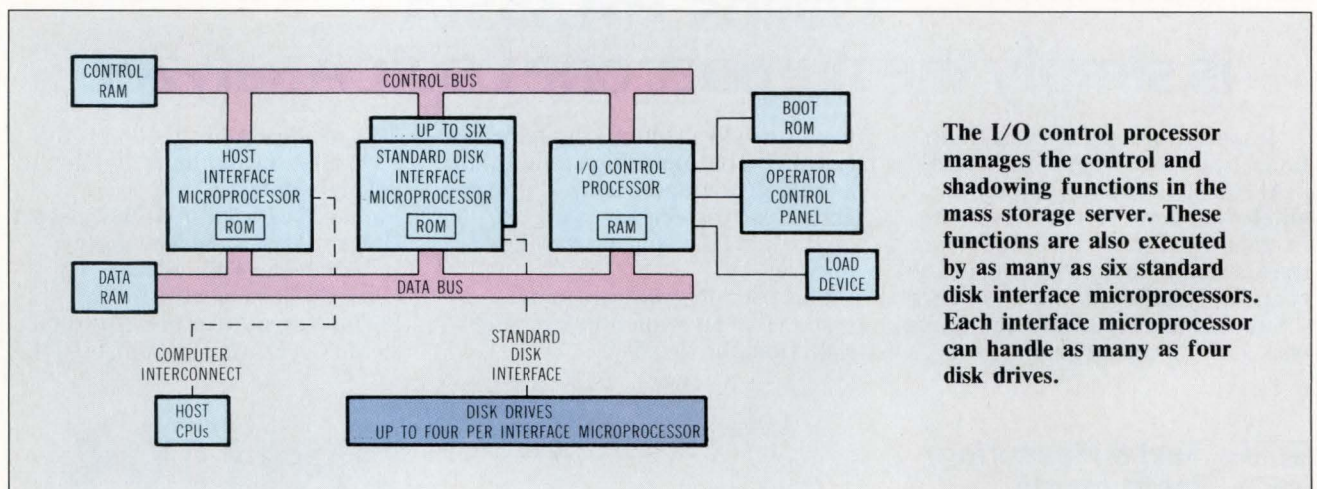
Managing server functions

The parallel processors in the server have access to all the status information they need to share the server's control and shadowing functions. These functions are managed by a single I/O control processor and executed by as many as six standard disk interface microprocessors. Each interface microprocessor handles as many as four disk drives.

The I/O control processor interprets mass storage control protocol requests from hosts and places them in the seek queues of control memory. The I/O control processor is a general-purpose processor based on DEC's F11 chip set and executes the full PDP-11 instruction set. It cannot, however, be programmed by the user. The interface microprocessors, which carry out the read and write requests in the seek queues, each have two 2901 bit-slice microsequencers.

At initialization of the server, the shadowing software is loaded with diagnostics and utility functions from a DEC TU58 tape cassette in the server cabinet into the I/O control processor's 256-Kbyte dedicated RAM. Shadowing code comprises less than 15 Kbytes of about 180 Kbytes of firmware in the RAM.

The I/O control processor provides for duplicate writes by placing copies of write requests for all the drives in the shadow set. On reads, once the I/O control processor locates a read request in the seek queue of the optimal drive, the request is forwarded to the drive queue controlled by the appropriate interface microprocessor. In general, performance is optimized

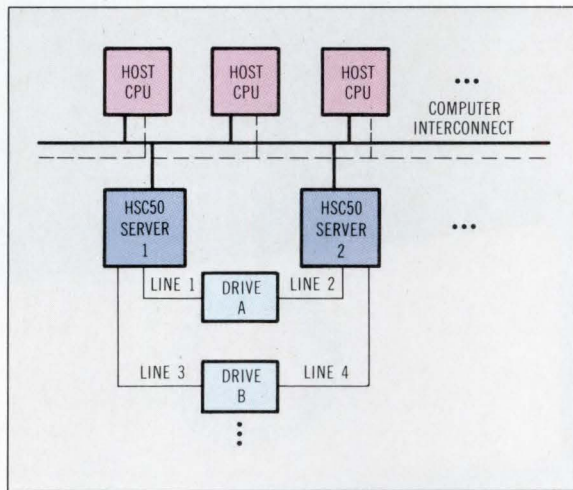


The I/O control processor manages the control and shadowing functions in the mass storage server. These functions are also executed by as many as six standard disk interface microprocessors. Each interface microprocessor can handle as many as four disk drives.

Shadowing in extended systems

While shadowing can achieve high reliability when a failure occurs in a single disk or disk drive, it can also be effective in multiprocessing systems that provide built-in redundancy. Such systems, besides combining the computing power of two or more processors, would use built-in redundancy to protect against failure in various system components.

For example, one small VAXcluster system might include three VAX host CPUs and a pair of HSC50 servers, all linked over a high speed computer inter-



connect. The servers would be connected to two (or more) dual-ported disk drives, A and B. Without shadowing, server 1 might normally handle transfers to both disk drives A and B, with server 2 standing by as backup. If line 1 or 3 broke, line 2 or 4 (respectively) would automatically close and server 2 would take control of drive A or B. There can be as many as 24 drives on either server.

A more efficient approach would be to have lines 1 and 4 normally closed (2 and 3 normally open) so that server 1 controls drive A and server 2 controls drive B. Any failure in line 1 or 4 will close line 2 or 3. In this way, the servers back up each other for as many as 24 drives. Here, however, each server normally handles only 12 drives, an arrangement that offers better performance than when one server normally handles all drives.

Drives A and B can form a shadow set also, so can as many as 12 pairs of drives. If lines 1 and 3 both open when server 1 is handling the shadow set, lines 2 and 4 both close and server 2 automatically takes over the shadow set. But if only line 1 opens (and line 2 therefore closes), a shadow set no longer exists because the two drives are no longer connected to the same server (only lines 2 and 3 are closed). Should that occur, both servers report the event to the host. The host immediately opens line 3 so that line 4 will close. Then, the shadow set is switched from server 1 to server 2.

by assigning the disks in a shadow set to different interface microprocessors.

Self-repair and error management

Shadowing's self-repair function follows two error management processes that occur, with or without shadowing, in a DSA mass storage server. First, error correction circuits detect and recover errors that can develop between writing data to a disk and reading the same data from the disk. Without the hosts' knowledge, the server corrects transient errors induced randomly by electrical noise. Errors caused by common progressive defects such as holes, inclusions, and thin spots in the magnetic media are also corrected automatically. When errors exceed a predetermined severity threshold, they are reported to the hosts' VMS operating system for information only.

A second error management process is bad block replacement. This occurs when repeated errors in a block (the logical data stored in a physical sector) indicate that the sector is defective and should be discarded. After replacement, further accesses to the original sector address are "revector" to the replacement address. To minimize revectoring time, one replacement sector is always available on the same track as the bad sector. (Because the distribu-

tion of bad sectors is not likely to be the same in any two disks, shadow set members must be described as logically identical, not physically identical.)

Shadowing repair backs up both error correction and bad block replacement. If the server's error correction circuits fail to detect and recover a read error in a sector of one disk, the correct data is sent automatically to the host from another member of the shadow set. At the same time, the correct data is written into the error-holding sector so that the block can be properly read in the next access. A sector thus repaired may be either at its original address, or (if a bad block has been replaced) at its revector address. The replacement of a bad block, however, only makes a nondefective sector available. Shadowing repair is needed to write the correct block of data into the replacement sector. Only data that was erroneous to begin with is known to the bad block replacement circuits.

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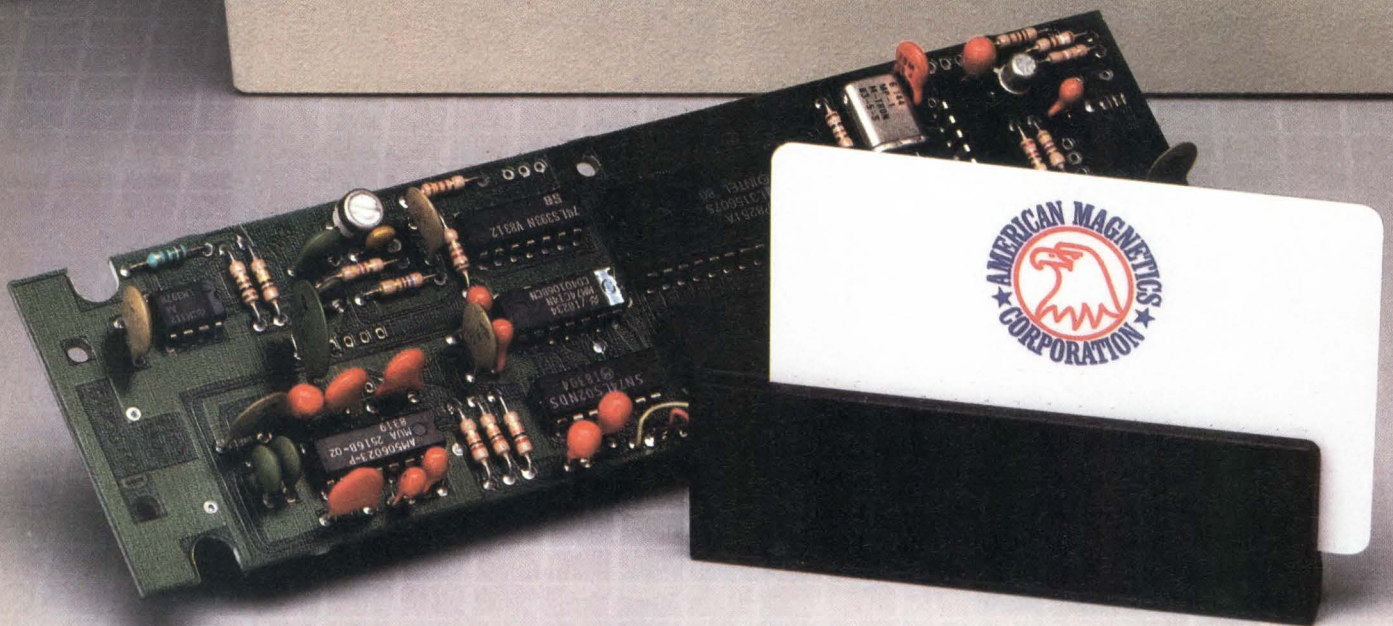
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CMOS VLSI INCREASES LIFE EXPECTANCY OF COMPLEX SYSTEMS

Low power consumption is usually touted as the major advantage of CMOS over bipolar. But CMOS provides the bonus of a lower failure rate.

by Al Kadis

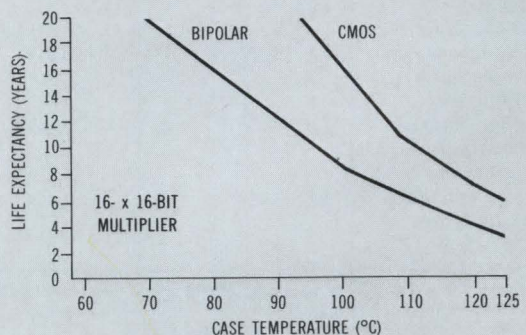
The heat generated by a running IC limits the number of gates that can be designed into a single package, especially for bipolar ICs. This makes CMOS parts that couple extremely low power consumption with ever-increasing performance well suited to applications requiring a large number of gates. In addition, recent developments of complex CMOS ICs with speeds comparable to equivalent bipolar devices, such as 16- x 16-bit parallel multipliers, register ALUs, multiplexers, and RAMs, allow the design of extremely fast CMOS systems.

The system reliability gained with CMOS becomes obvious when the power and heat dissipation requirements of typical high performance bipolar ICs are compared to equivalent CMOS ICs. Bipolar systems require larger power supplies, so they demand more weight, size, and raw energy. Also, the system and the power supply generate heat that must be removed. This only adds more mass and space requirements for cooling instruments. CMOS power consumption, on the other hand, is proportional to speed. Users operating at lower frequencies, therefore, can save additional power by running the IC slower—where system requirements permit. This

lowers the junction temperature and further increases life expectancy.

In many cases, therefore, it may be possible to replace a bipolar system with a CMOS system, providing three to five times greater capability, or to use the power savings to reduce the size of power supplies and enhance another part of the system. But to increase reliability greatly and take full advantage of low CMOS power dissipation, new systems should be designed from scratch.

Failure rates for semiconductor ICs have typically been measured in tens of years in life expectancy, regardless of the technology involved. As ICs have become more complex, the increased number of gate



As a direct result of its lower heat buildup, a typical CMOS part can be projected to endure higher ambient operating temperatures than its bipolar equivalent and provide longer service life.

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counts has increased the power dissipation and resulted in greater failure rates. For bipolar ICs, typically running at many times the power dissipation levels of CMOS ICs, self-heating becomes an even greater problem. This problem can be solved by designing packages with efficient heat dissipation, and by placing the IC chip in a package in a way that efficiently transfers the heat of the die to the outside environment.

As the gate count of bipolar parts becomes greater than 2000, the increase in junction temperature becomes significant, which reduces the mean time to failure. As an example of the life expectancy of a larger die, an analysis is made of a bipolar 16- x 16-bit parallel multiplier (mounted in a 64-pin DIP with an internal heat sink) and the equivalent CMOS part from Integrated Device Technology, the IDT7216. Both parts perform identical functions at equivalent speeds.

The operating temperature of an IC junction is determined by the simple formula:

$$T_j = (K_{jc} + K_{ca}) P_d + T_a$$

where K_{jc} is the thermal coefficient between the junction and case; K_{ca} is the thermal coefficient between the case and the ambient environment; P_d is the power dissipated by the IC; and T_a is the ambient temperature. The sum, $K_{jc} + K_{ca}$, is also equal to K_{ja} , the thermal coefficient between the junction and ambient.

Operating Parameters for Typical 16- x 16-bit Multipliers

Operating Parameters	Bipolar Multiplier* 64-pin DIP with internal heat sink 5.5 V	CMOS Multiplier IDT7216 64-pin DIP 5.5 V
Maximum voltage	960 mA	80 mA
Maximum operating current	125 °C	125 °C
Ambient temperature	12 °C/W	40 °C/W
Junction-to-ambient temperature coefficient	7.9 °C/W	15 °C/W
Junction-to-case temperature coefficient	4.1 °C/W	25 °C/W
Case-to-ambient temperature coefficient		

*The bipolar die is placed close to an internal heat sink to reduce the junction-to-case temperature coefficient to 7.9 °C/W and junction-to-ambient to 12 °C/W. This is not required with the CMOS IC.

The junction-to-ambient thermal coefficient (K_{ja}) for the IDT7216 is 40 °C/W, so that at a maximum operating voltage of 5.5 V and a maximum operating current of 80 mA, the temperature rise of the die

Failure Factors for 16- x 16-bit Multipliers*

Factors Utilized	Bipolar	CMOS
Ambient temperature	95 °C	95 °C
Case temperature	100 °C	100 °C
Case-to-junction temperature rise	42 °C	6 °C
Junction temperature	142 °C	106 °C
Quality (f_Q)	6.5	6.5
Circuit complexity failure rate (C_1)	0.071	0.037
Temperature acceleration (f_T)	25	23
Voltage derating (f_V)	1.0	1.0
Circuit complexity failure rate (C_2)	0.0027	0.0014
Device learning (f_L)	1.0	1.0
Application environment (f_E)	9.0	9.0
Package	64-pin DIP with internal heat sink	64-pin DIP
Package complexity failure rate (C_3)	0.025	0.025

* Approximately 2100 gates of random logic 64-pin dual-inline top braze package (internal heat sink on bipolar only).

above ambient is 17.6 °C. Since the junction-to-case thermal coefficient for the IDT7216 is 15 °C/W, the temperature rise of the junction above the case, at the same power dissipation, is only 6 °C.

Temperatures on the rise

This calculation, carried out for a typical bipolar 16- x 16-bit multiplier with a junction-to-ambient thermal coefficient of 12 °C/W, a maximum operating voltage of 5.5 V, and a maximum operating current of 960 mA, gives a temperature rise for the die above ambient of 63 °C. And since the junction-to-case thermal coefficient is 7.9 °C/W, the temperature rise of the junction above the case is 42 °C.

Bipolar manufacturers usually recommend that the maximum junction operating temperature does not exceed 175 °C. With a calculated junction-to-case temperature rise of 42 °C, the case temperature must not exceed 133 °C. At an ambient of 125 °C, system air flow must be sufficient to hold the case temperature rise to less than 8 °C. This is a significant difference, since the allowable CMOS case-to-ambient temperature rise is 44 °C.

This analysis, performed on a typical bipolar and CMOS IC, clearly shows how the junction temperature for the die is affected by power dissipation, the thermal resistance of the package, and the ambient temperature. The best circumstances for controlling reliability and circuit performance is to allow the junction temperature to remain as close as possible to ambient. This demands that the power dissipated or the package's thermal resistance (or both) should approach zero.

The mean time between failures (MTBF) is a direct function of the operating environment and junction temperature. The junction temperature rise calculations can help determine the MTBF and the life expectancy of bipolar versus CMOS circuits.

The type of data needed to derive failure rates and the MTBF for the typical multipliers discussed here can be found in Military-Handbook-217D, January 15, 1982 and updated June 12, 1983, section 5.1.

According to 217D, the device failure rate, R_f , expressed in failures per million hours, is given by:

$$R_f = f_Q [C_1 f_T f_V + (C_2 + C_3) f_E] f_L$$

where,

f_Q = quality factor

f_T = temperature acceleration factor based on device technology

f_V = voltage operating stress factor

f_E = application environment factor

C_1 and C_2 = circuit complexity failure rates based on bit counts

C_3 = package complexity failure rate

f_L = device learning factor

and the MTBF is equal to $10^6/R_f$.

At an ambient temperature of 95 °C, and assuming that air flow and heat sinking will maintain case temperature at 100 °C for both the bipolar and CMOS part, the above equation yields an R_f of 13.2 and 6.8, respectively. The life expectancy, L_E , in years, can be calculated by dividing the MTBF (in hours) by 8760, the number of hours in a year. This gives an L_E of 8.6 years for the bipolar multiplier and 16.8 years for the CMOS equivalent.

The 42 °C junction-to-case temperature rise of the bipolar IC points out that bipolar ICs are approaching their maximum chip size limitation. For example, if the chip size were increased to incorporate the functions of two multipliers, the power would double. Assuming both a CMOS and bipolar IC of this complexity were placed in the identical heat sink package used in the previous bipolar example, the following characteristics may be developed.

Operating Parameters for a 4200-gate Multiplier		
Parameters	Bipolar	CMOS
Power supply current	1.92 A	160 mA
Maximum voltage	5.5 V	5.5 V
Power dissipation	10.6 W	0.9 W
Thermal temperature coefficient	7.9 °C/W	7.9 °C/W
Junction temperature heat rise	84 °C	7 °C

With the rapidly growing acceptance of high density CMOS ICs, the packages used to house these chips are also changing. High speed CMOS technol-

ogy has initiated the shift from bulky packages to smaller ones that result in much greater board densities. These innovative packages are not practical or reliable with bipolar VLSI parts because of their high power dissipation.

Packaging options

Thermal resistance—the measure of a package's ability to dissipate the heat generated by a die—is determined by package material (ceramic or plastic), package size, and die size. CMOS circuits can operate reliably in much smaller packages than bipolar circuits can. Packaging technology has advanced to reduce package size by nearly 90 percent from the 64-pin DIP to the 68 "pin" leadless chip carrier (LCC) measuring 560 x 560 mils, while maintaining acceptable device junction temperatures for the 16- x 16-bit multiplier example above.

Surface-mount technology also is becoming a popular packaging alternative with the advent of CMOS and the smaller packages, such as LCCs. One approach is the permanent attachment of an LCC to a substrate by matching the thermal coefficients of expansion. This technique relies on the low self-heating characteristics of CMOS to minimize the thermal differential between the chip and the substrate. With techniques such as these, system designers can now achieve a twofold improvement in system package density.

Low thermal expansion between the LCC and the substrate is an important consideration in surface-mount technology. Expansion of the LCC and the substrate, $L_{LCC \text{ exp}}$ and $L_{SUB \text{ exp}}$, respectively, can be calculated as follows:

$$L_{LCC \text{ exp}} = (L) (C_{LCC}) (T_{LCC})$$

$$L_{SUB \text{ exp}} = (L) (C_{SUB}) (T_{SUB})$$

Here, C_{LCC} and C_{SUB} are the thermal coefficients of expansion for the LCC and the substrate, respectively, and T_{LCC} and T_{SUB} are the temperatures of the LCC and the substrate, respectively. For maximum reliability, the thermal coefficients of expansion for the LCC and the substrate should be matched. The temperature rise of the die determines T_{LCC} . CMOS is the only technology practical for use in surface-mount applications because it allows the LCC temperature to remain close to the substrate temperature.

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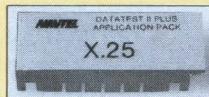
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MONITORED BURN-IN IMPROVES VLSI IC RELIABILITY

Device testing during burn-in provides information that can improve design and fabrication processes and pave the way for increased device yields and reliability.

by Michael Campbell

Reliability of VLSI ICs has become as hot a topic today as performance. Every semiconductor manufacturer is striving to balance the demands for increased complexity, higher volume, lower cost, and higher reliability (quality)—and still make a profit. One way to balance the cost/reliability equation is through the accurate characterization of the infant mortality for each type or lot of devices. Infant mortality is typically called burn-in fallout and is often accepted as a matter of standard manufacturing fallout.

Reliability is directly related to the design and fabrication processes. Consequently, a mistake in either area can lead to disastrous long-term device problems. Even the best design and fabrication techniques will sometimes produce less than perfect results. While perfecting techniques in these areas can help to increase device reliability, other effective approaches exist. Production screening techniques, such as monitored burn-in (the combination of conventional burn-in techniques and parallel device testing), can quickly eliminate the devices that would suffer from infant mortality. Studies of the failures

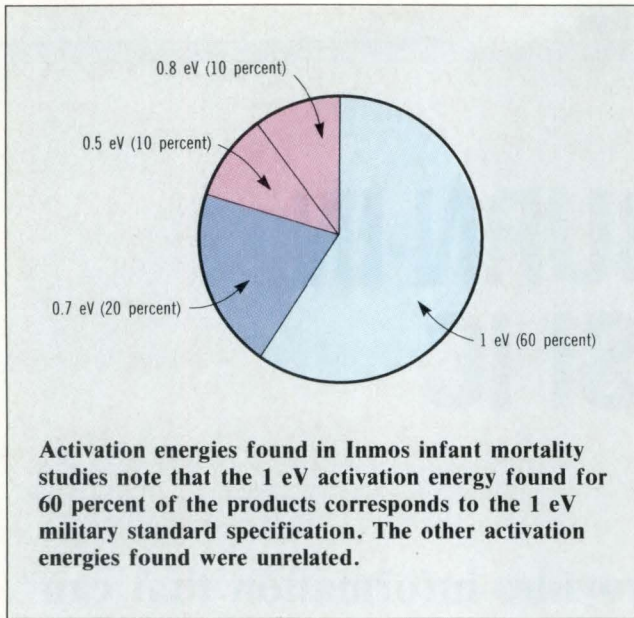
causing infant mortality can then be used to further improve reliability through feedback mechanisms to fabrication and design groups.

By screening out marginal devices, burn-in and testing have been used for years to improve the quality of ICs. Burn-in standards are based on either military standards or production standards for a particular device technology. For the most part, burn-in conditions are set by either simple small scale experiments or manufacturing necessity. Military standards specify 1 eV as the activation energy for projections of burn-in time. Studies on Inmos products, however, indicate that this 1 eV activation energy is accurate for 60 percent of infant mortality failures found and is probably the correct activation energy for only a portion of all manufacturers' products. The dogmatic use of this activation energy to project burn-in times at alternate temperatures, therefore, may not be as precise as needed.

The Inmos study began as an investigation into the infant mortality characteristics of VLSI memories. The driving force behind these experiments was a desire to cut the cost and cycle time for the testing and screening of VLSI memories by reducing the long-term failure rate through burn-in.

An NMOS 16-Kbit static RAM, the IMS1400, was tested in the first experiments. A total of 94,000 devices were monitored by the end of last year. In early 1982, the infant mortality mean time to failure was determined to be 34.47 hours. Worse case devices usually failed in 94 hours during the monitored

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VLSI memory testers. This correlation proved to be the key to understanding device infant mortality and effectively reducing the failure levels.

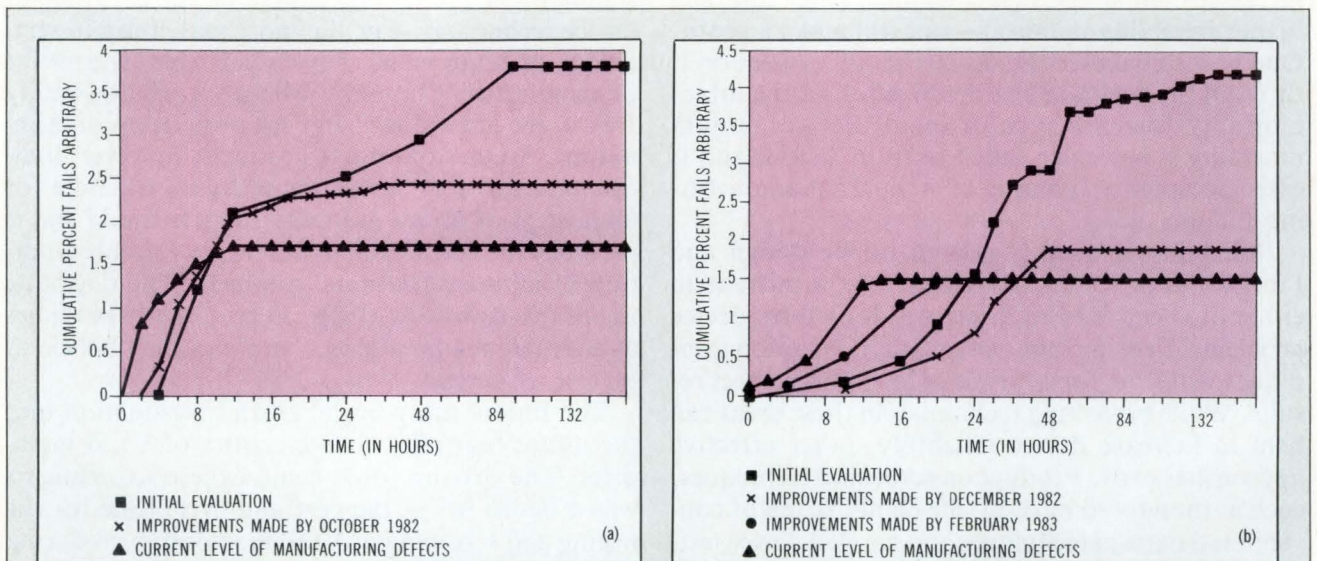
Reducing production burn-in time

Failures were analyzed and traced to limiting features in the critical dimensions and device process tolerance windows of the IMS1400. After a series of corrective measures, the standard burn-in time was scaled down to 48 hours and the long-term failure rate was reduced to 79 FITs with no failures in the first military-specified 168 hours of life test. As long-term corrective actions took effect during late 1982, the mean time to failure was further reduced to 6.74 hours, and the long-term failure rate dropped to 35.47 FITs. In addition, burn-in time was cut to 24 hours. Recently, 35,000 devices have been sampled, finding no significant deviation in terms of failure modes or time to failure characteristics.

burn-in. The total burn-in time for those devices was 168 hours. This data was statistically consistent across 23,298 devices representing 28 production lots. At this point in time, the long-term failure rate (1000 hour life test) on the IMS1400 was 91 failures in time (FITs) at 55 °C, where the time equals 10^9 hours.

The failures found through the monitored burn-in test system initially were not correlatable to the final electrical test specifications. After numerous iterations of pattern and timing changes, a 95 percent correlation was achieved on commercially available

The success of the SRAM program led to a similar study of the IMS2600, a 64-K x 1-bit dynamic RAM. The IMS2600 was initially offered with a minimum of 160 hours of burn-in and a long-term failure rate of 127 FITs. An infant mortality analysis revealed a multimodal failure distribution. The multimodal distribution was broken down by time dependent fallout mechanisms. As the fabrication and design modifications were identified for each mechanism, the infant mortality dropped 25 percent from the original levels, and the mean time to failure fell from 90 hours to 38 hours. Using this data,



In the initial evaluation of the 16-Kbit static RAM at 125 °C, the worst case failure was at 94 hours. As corrective actions were implemented, the time to last failure was reduced to 6.74 hours (a). Similar advances were made in studies on a 64-Kbit dynamic RAM at 125 °C, cutting time to the last failure from 90 to 10.5 hours (b). In both cases, the cumulative percent defectives were driven downward, implying an increase in device yield.

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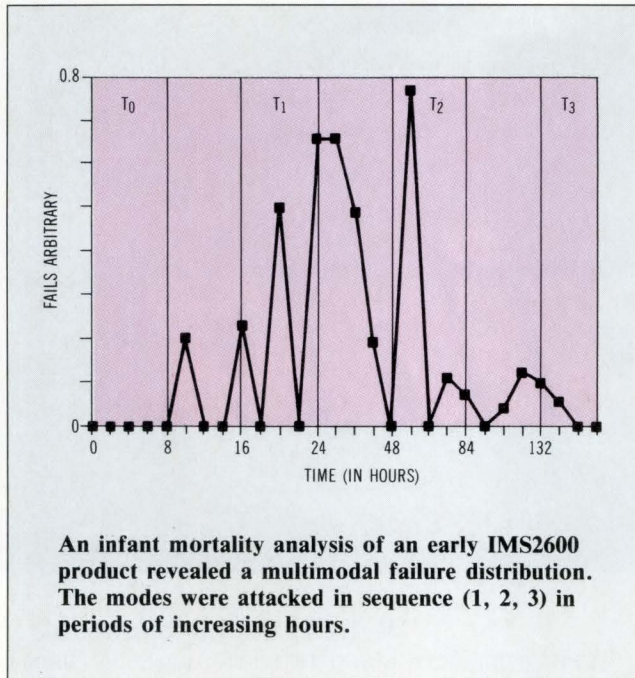
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burn-in was reduced to 48 hours. After six more months, the meantime to failure was 10.5 hours. The production burn-in was 24 hours at 125 °C with a long-term failure rate of 26.44 FITs.

The IMS2620 (16-K x 1-bit) and IMS2630 (8-K x 8-bit) have been exposed to monitored burn-in testing as well. Similar reliability and yield enhancements were possible for each device. Due to earlier work on the IMS2600, however, burn-in time reduction and lower life-test failure rates were accelerated greatly.

Activation energy analysis

In attempt to reduce burn-in further, analysis was continued on the six major product types that could benefit from monitored burn-in. Since the existing residual failure rate could not be reduced easily in a short term, alternate temperature studies were used to reduce the burn-in time. Infant mortality activation energies (E_a) for the major failure modes observed varied between 0.5 and 1.03 eV across all product types. Instead of applying a blanket activation energy, a calculated effective energy was used for device projections. The calculated E_a was 0.857 eV.

This study encompassed 35,000 devices at 125 °C and 140 °C. Final burn-in time introduced into production was 12 hours at 140 °C.

Monitored burn-in has proved to be a very useful and cost efficient tool for improving device reliability and production. First, burn-in times and temperatures can be set accurately with no adverse impact on a customer's system. Second, significant improvements in failure rates and device yields are possible. The IMS1400, for example, improved 61 percent in

time to last failure and 5 percent in yield. Also, reliability goals can be set early in the design and manufacturing cycle, rather than waiting for long-term stress test evaluations.

Evaluating new products can provide insight into long-term reliability and the problems that might arise within the design and fabrication processes. Applying unique test patterns, stresses, and loading conditions to devices during monitored burn-in will not only detect failures, but also allow them to be traced to the exact point at which the devices failed. In addition, why and how the device failed can then be answered. Instantaneous feedback eliminates some of the guess work involved in burn-in techniques, and allows for more accurate reliability figures. This feedback when extended to include fabrication and design also shortens the time required to make changes to the standard product. Finally, monitored burn-in can reduce overall test time and production costs.

The history of the DRAM family (eg, 16-Kbit, 64-Kbit, and ultimately the 1-Mbit) provides a vivid example of the savings possible when using monitored burn-in. According to industry sources, it should have taken about 30 s to test a 64-Kbit DRAM, with a test cost of about 60 cents per part. Using monitored burn-in techniques, the test cost could have been cut to 10 to 15 s without any loss in patterns or testing accuracy. This implies a 50 percent savings in cost/time. Most 64-Kbit manufacturers chose, however, to reduce testing time by using design and layout data and eliminating patterns. While this makes sense at the 64-Kbit level, other alternatives must be explored at the 256-Kbit level and beyond. Projections for the 256-Kbit DRAM indicate a test time of well over a minute, making test cost prohibitive.

Monitored burn-in, with the parallel testing of thousands of devices, can reduce these test requirements. Since most companies perform burn-in as a part of their standard process flow, this "dead time" in the process could be used to test devices, when using monitored burn-in systems. This option provides the opportunity to run complex and time consuming test patterns that would not normally be done because of time constraints. In particular, monitored burn-in testing could find pattern/timing sensitivities without tying up massive amounts of production tester time.

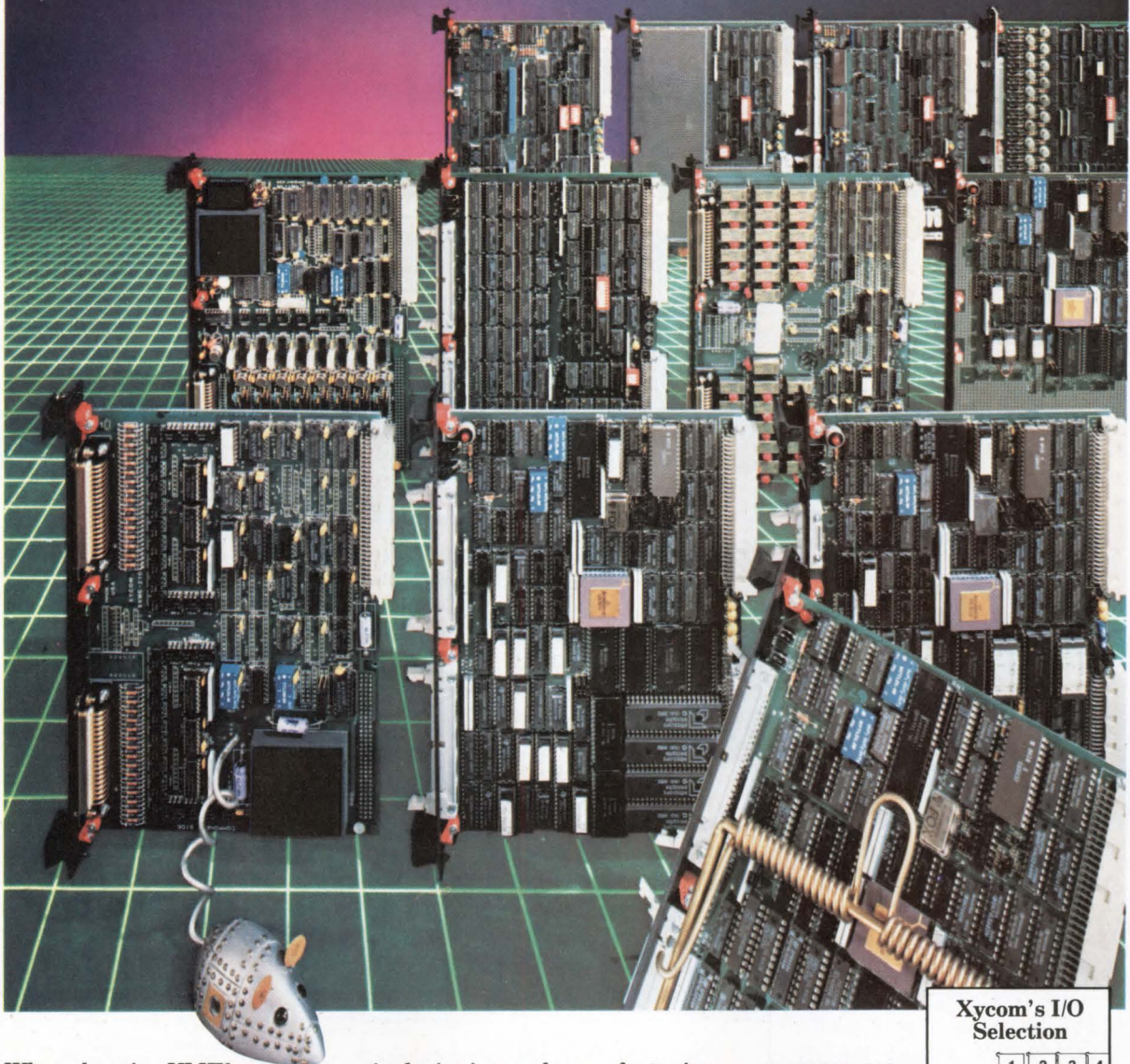
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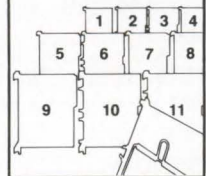
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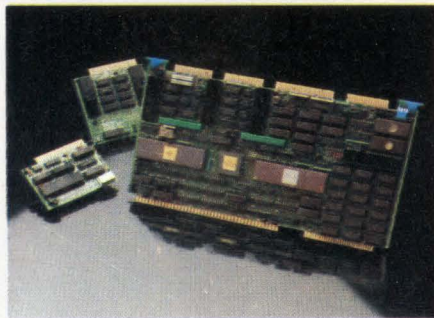


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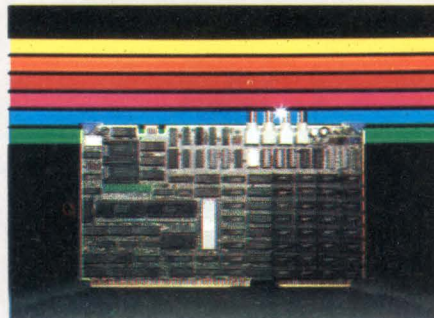
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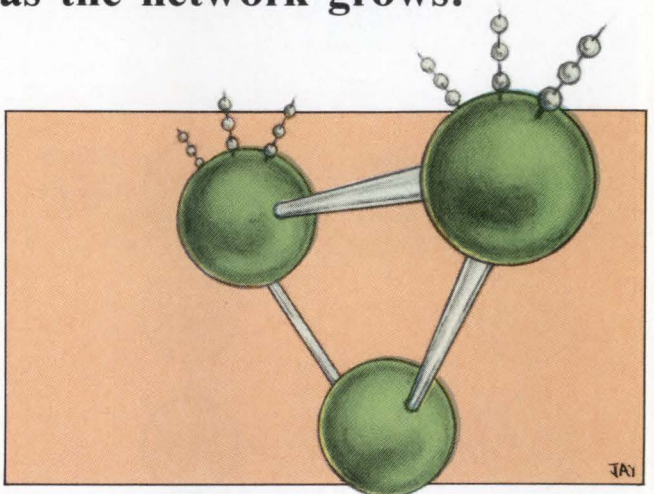
Integrating intelligent monitoring and control facilities into network nodes permits customized control, reporting, and management facility expansion as the network grows.

by Daniel M. Profant

As data communication networks become more complex, there is an increased need to recognize and collect information from the network operation as well as to maintain control. A network management facility can meet this need while residing in a workstation—sharing the workstation's resources—or in the node of a data communication network. Such an integrated network management facility, which operates in a shared or integrated environment, depends on techniques that make it adaptable to the peculiarities of the network. It should also assist in the development of the facility.

Doelz Networks, Inc has designed such an integrated function facility known as the Interpreter States Machine, with its own computer language. This machine and language work together to develop network management programs for a network environment. A management facility with an open-ended design allows for the growth of network management capabilities including increased network capacity, the addition of new capabilities (both planned and unforeseen), and the introduction of specialized user-defined features.

Independent of network size, the network management facility monitors network activities and communicates network statistics and conditions to

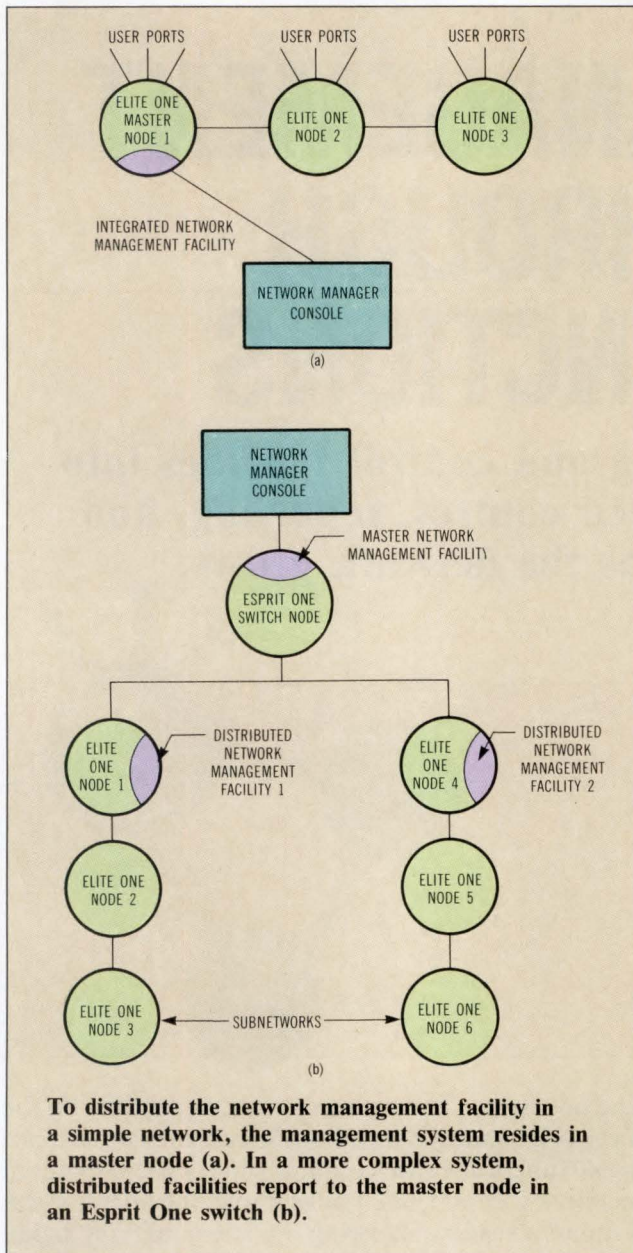


the operators. The operators can, depending on the network conditions, call out specific network manager functions and communicate with individual network components. For example, the operator can request a readout showing the line quality or signal strength of the line segment between two nodes in the network. The operator can also request collected node statistics. Moreover, the management facility supports configuration of user ports through a terminal or host processor, the configuration of network connections, and the assignment of network node identifiers.

Configuration of user ports provides for assignment of terminal/host-specific information. Within the network, there are more than 100 different parameters for a single port. These parameters include port speed, port address, protocol type, permanent versus temporary (dial-up), rotary member, and multipoint (slave or master).

Network configurations are "learned." Thus, the network management facility automatically determines the network node connections. The network

Daniel M. Profant is a software development manager at Doelz Networks, Inc (Irvine, Calif). He is responsible for product development of the Elite One concentrator switch. He holds a BS in mathematics from Long Beach State College.



operator may supersede the automatically determined configuration, however, and install exception or standby connections. Installing or removing the analog/digital loopbacks around selected modems in a specific node removes or includes a line segment in the network link.

Through the network management facility, the network operator assigns unique identifiers to system elements such as nodes, path connections between ports, and port addresses. The operator can then refer to any node by the name assigned to it (most likely the site identification). It also allows the network user to connect the port to a port selected by the port address (the local phone number for the port).

The supervisory console (attached to a specific node designated as the master or network manager)

displays impending or current fault conditions from any network node in the form of alarms. The alarm is similar to an unsolicited report. It presents the source of the recognized fault condition, the identifier for the node that reports the determined fault condition, the date and the time when recognized, and the nature of the fault condition.

With an impending fault condition, the network management facility automatically investigates the identified node and performs self-diagnostics to test the condition of the fault area. Operating from a current fault alarm that signals a communication cut-off, the network management facility can self-heal to restore communication service in the event of a line outage, modem failure, or node failure. System self-healing seeks alternate transmission routes for nodes whose existing line segment connections are no longer valid. This type of service is particularly valuable when performed automatically for minimal system outage.

The presentation of various status reports can provide operators with valuable information on network operations. These reports include statistics on traffic through each node (block counts, discard rate), line quality at each connection point, directory of port addresses, current node connections, and individual port configurations.

Inside the network environment

The network, from the network management system's view, consists of both a distributed and a centralized element. In the distributed element, each nodal processor in the network monitors communication traffic passing through that node, maintains traffic statistics, and performs online diagnostics. In the Doelz network, an ongoing subsystem, known as the ALL CALL facility, periodically reports to the network management controller. This facility gives updated traffic statistics, any recognized alarm conditions, the current hardware complement and configuration, and node type.

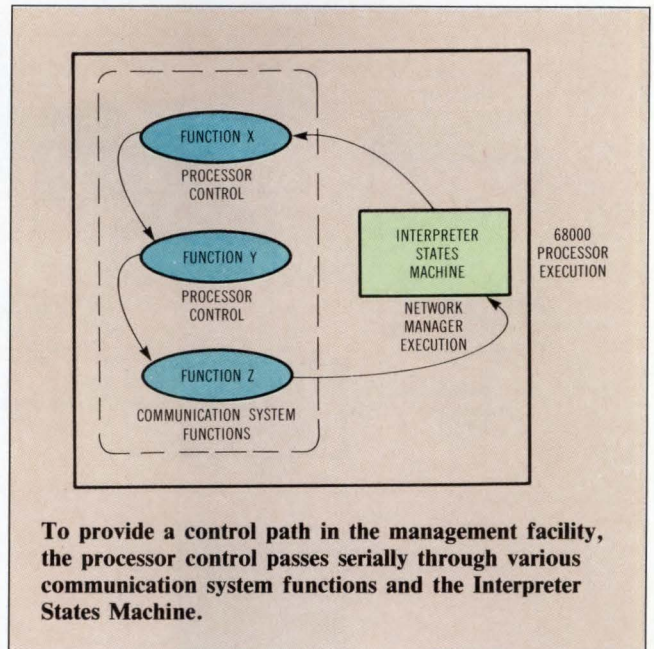
For the centralized element, a selected node within the network serves as a master to execute the network management facility. This node also shares processing with the ongoing communication operations. In a simple network (two or more nodes), this facility can reside in a master node. A node can serve as both a communication node and host to the integrated network management facility. Thus, while the network management operational facility resides in a single centralized processor, the network management function is distributed throughout the nodes in the network. In a more complex network (several subnetworks interconnected through a switching node), the network management facility is distributed to the subnetworks, with a master network

management facility. This facility resides in a switch that controls the separate, distributed facilities. A complete network would consist of multiple switch networks interconnected via trunk lines with the network management facility located at a selected switch node's network management facility.

The network management programs execute under control of the firmware function known as the Interpreter States Machine. The interpreter executes one instruction of the management system language, or a partial instruction per loop through the function set. The processor is then released to perform its other communication functions between instructions. Thus, at most, one interpretive instruction will be executed per entry and exit of the interpreter.

An interpreter instruction executes only after each major operational function has had an opportunity to execute. Because the operational functions demand more processor time as the communication load increases, the interval between successive interpreter instructions lengthens as the load increases. Thus, the facility adjusts automatically to the communication demands of the network. Program logic written for each network management function need not consider the communication loading of the network.

The interpreter runs in two modes, background and foreground. In background mode, a continuously operating program written in the management

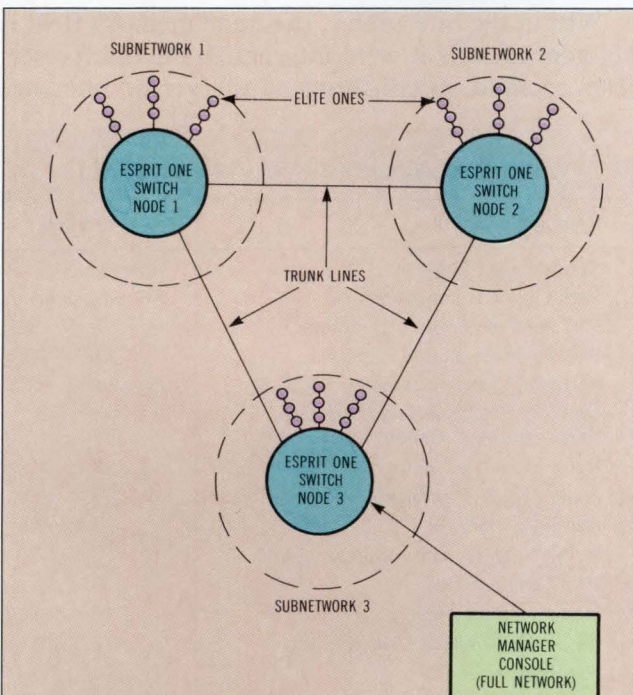


system language monitors all responses from nodes within the network. Executing under the control of the Interpreter States Machine, the background program can do several things. It can manipulate logical registers assigned to the machine, examine and transform the input presented to the network management subsystem, and prepare and output reports to a network management display device. In addition, the Interpreter States Machine allows access to pertinent data residing within any node connected to the network.

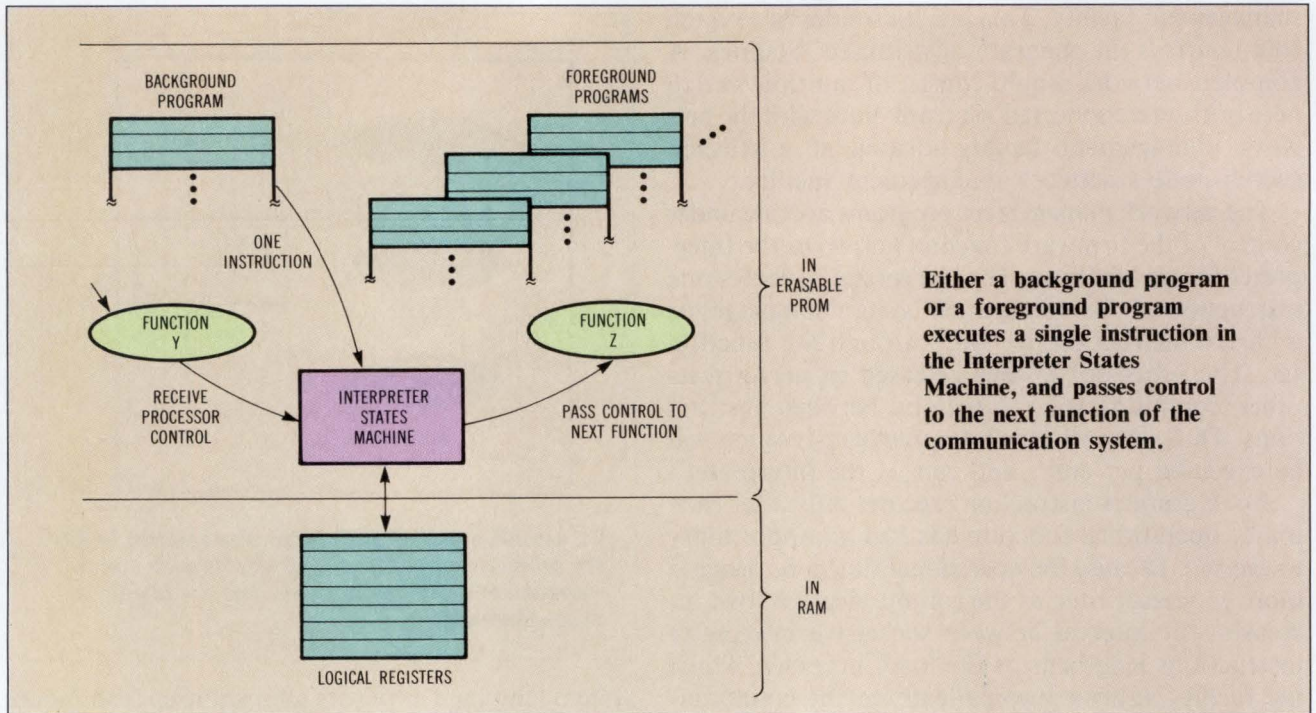
The network operator activates the foreground mode through the control console. The background program permits the operator to enter the foreground mode at specified points during the background program's execution. Thus, a network operator console request, called an operation command, is associated with a foreground program. A simple interrupt releases control from the background program to the foreground program. The process of transferring from background to foreground modes requires that the logical registers be saved in a holding area while the foreground program executes. In this way, a foreground program will have complete access to the logical registers. After completion of the foreground program, the logical registers are restored for the continued execution of the background program.

Inside the interpreter

The interpreter architecture consists of a set of logical registers through which the interpreter controls execution and the program manipulates data. The logical registers reside in dynamic RAM and are categorized into two groups—interpreter control and



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program registers. Interpreter control registers include a function states counter, function clock, program level register, program instruction counters ($n = 0$ to 6), and an interrupt save area. Program registers are called special, general, holding, and accumulator.

The function states counter identifies the current state of the interpreter. Possible states include executing a background or foreground program instruction, and waiting for completion of timed event while in background mode, foreground mode, or keyboard entry (command request), and command lookup.

The function clock register times out expected responses, while the program level register identifies the program instruction counter currently in effect. The program level register is associated with a nesting level of subroutine calls. The counter for the current program instruction points to the current or next program instruction to be executed. Finally, the interrupt save area retains a copy of the entire register complement for a background program in progress while executing in the foreground mode.

Vector registers

Special program registers are categorized as vector, vector reference, iteration control, and working. The interpreter's set of vector registers permits access to the memory of each node in the network. A vector register has the following components: area network, nodes structure position number, table set within the node, table within the node, entry within the table, and field within the entry.

The vector register set serves as a complex address register that identifies the field to be

accessed. All accesses automatically adjust (normalize) the accessed field between the interpreter registers and the memory position that the field occupies in the node. Thus, in writing program logic, the program designer need not pay attention to positional information.

Within the interpreter, the node memory field is referenced as if it were internal to the interpreter. The operand specification of the vector reference

Possible Access Level Assignments	
Command/Report	Access Level
Net-Manager Sign-On	None required
Help List of Commands	None required
Port Address Routing Directory	1
Port Interface Status Report	1
Port Configuration Report	1
Network Structure and Hardware Reconfiguration Report	2
Node Statistics Report	2
Assign Node Identification	3
Configure Port	3
Install Network Link Configuration	3
Heal Network Link	3
Modem Status Report	3
Loopback Network Link Modem	3
Loopback User Port	3
Node Reset	3
Enable/Disable Standby Line Segment	3
Isolate/Attach Network Link Segment	3
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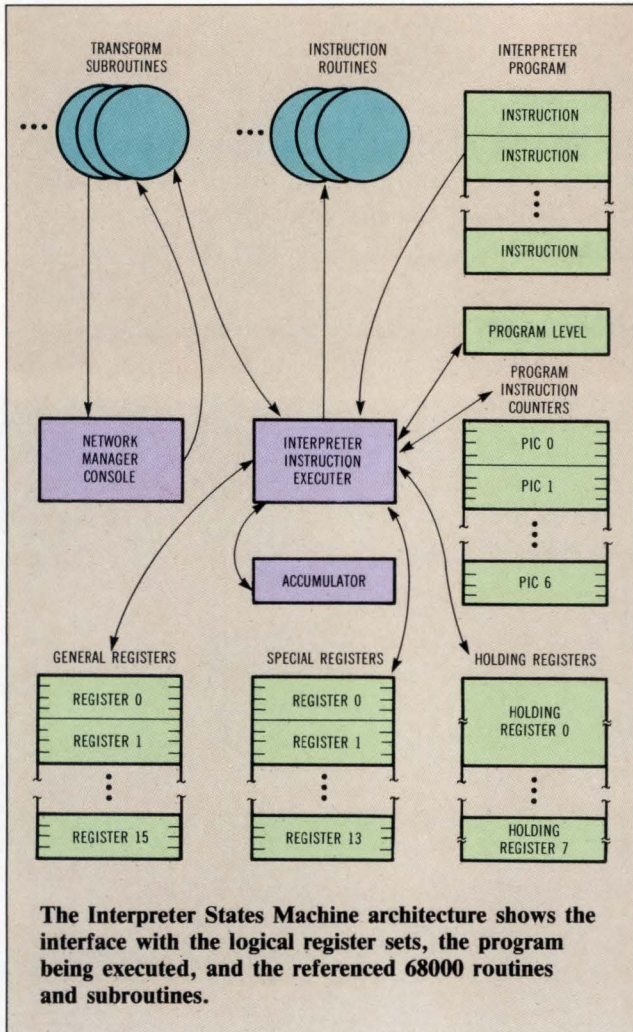
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register indicates input from the network management control console keyboard. Special register 15 indicates output to the network management control console screen. An additional register set is available to the interpreter for temporary data storage. These registers store data between the accumulator and the processor. Specialized instructions save and restore the vector set, and up to eight vector sets can be retained in a holding area. As a result, a program can retain the address of several selected nodes in the network and reestablish any vector set with a single instruction.

The reports and alarms developed by a network management program have strings of command text interspersed with the display form of variable values. In this approach, the program logic uses a dictionary of words and phrases that are likely to be repeated in various messages for output of the command text portion. To conserve memory, the program logic points into the dictionary, rather than into a complete table of text strings.

The language incorporates elements called transforms. These transforms provide an instruction set

that can convert variable data from its internal form to external form or vice versa. This is done simply by referencing the field to be transformed or the appropriate transform. There are two types of transforms in the Doelz network management language—input and output.

For cases where the network management language may not be effective in the execution of a function, the language provides the ability to escape in-line to machine code for short bursts. Thus, two or three lines of instruction can be taken from the real processor to fill in when a function cannot be easily performed through the instruction repertoire of the management language.

The network management control console is the interface between the operator and the network management subsystem. The network management language provides the facility to develop programs for the man/machine interface. To make the program development task easier, intrinsic functions have been made universal.

Although the control console is usually connected to the supervisory port, a path can be made from any user port in the Doelz network to the network management facility. Such a path provides the network operator with access to the facility from any remote port in the network. This is achieved by designing the network management facility to act as a port (a pseudo port) with its own unique port address to enable connection from any port in the network.

Restricted access to the network management facility is also possible. In this way, selected reports and commands are reserved for specific users, while other reports and commands are available for other users. Restriction of use is accomplished by identifying four access levels. Each command or report that can be requested is assigned an access level (1 to 4). An access level of 0 implies that there is no prohibition of access.

The sign-on to the integrated network management facility requires the specification of a unique access key (password) for each possible level of access. Once signed on, only those commands and reports at the presented access key level and below are available to the signed-on user. As an example, a manager of network operators would have an access key classification of 4, network operators—3, selected management personnel—2, and system users—1.

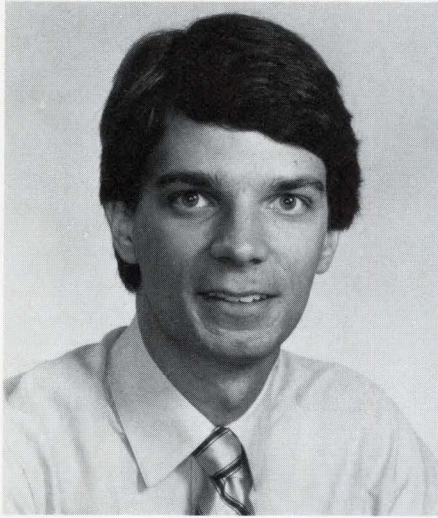
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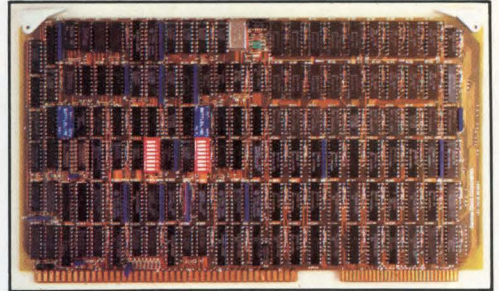
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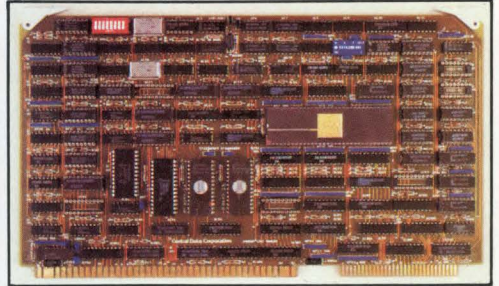
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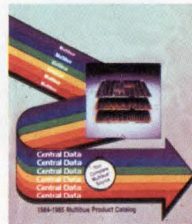
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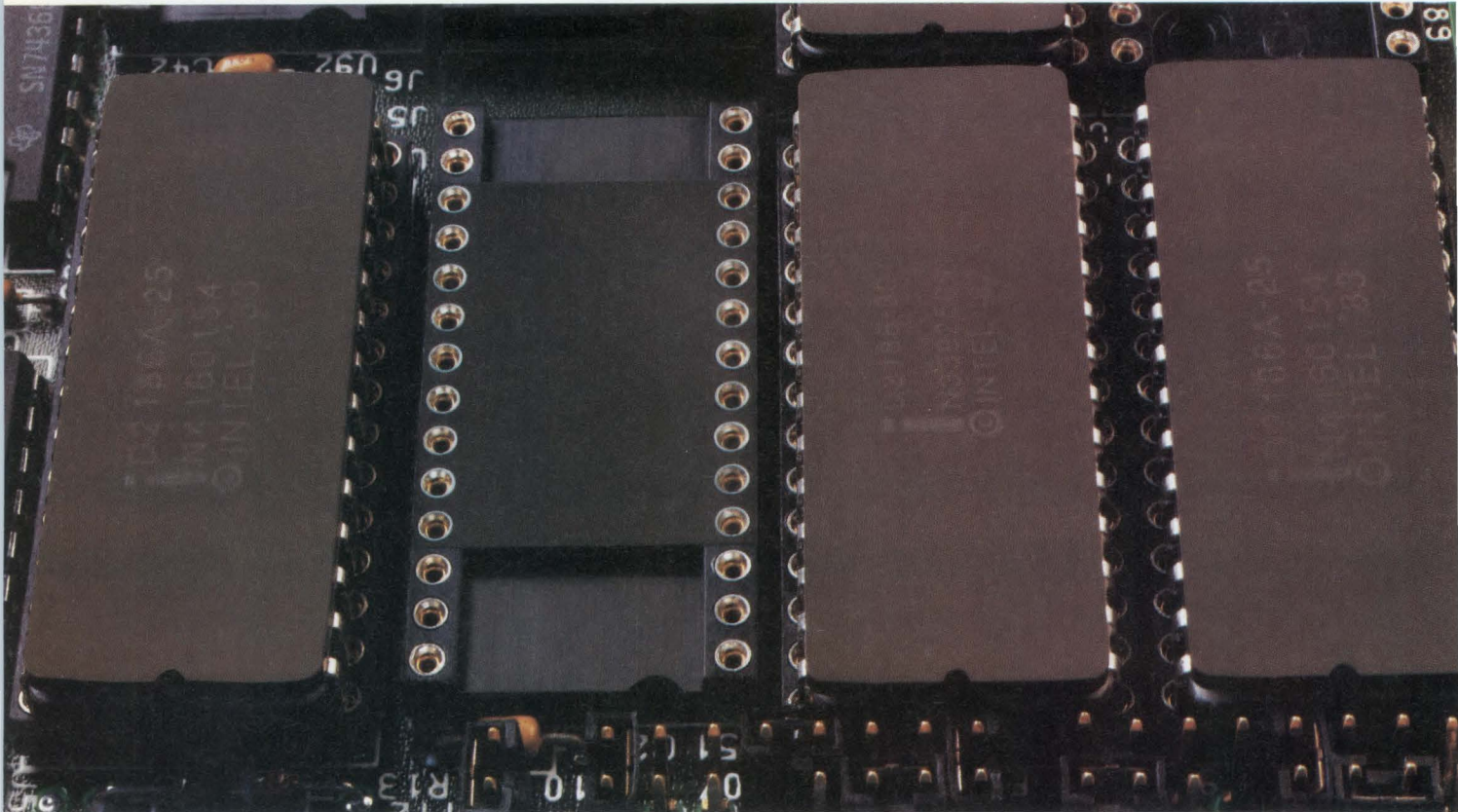
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REGISTERED PROMs HELP IDENTIFY SYSTEM FAULTS

Diagnostics, previously unavailable in a single chip, were done using SSI/MSI chips, or were ignored. Now, PROMs with registered output can provide speed and on-chip diagnostics in pipelined, testable microprogrammed systems.

by Om Agrawal

Microprogram memory, or control store memory, is one of the most critical resources in a microprogrammed system. While microprogram memory can be very deep and quite wide, it is usually limited to 1000 to 16,000 words deep and 16 to 100 bits wide. A variety of memory types (such as ROMs, PROMs, or RAMs) can implement microprogram memory, depending on the speed or degree of function desired.

ROM used to be the most prevalent type of control store because it was relatively cheaper and faster than other types of memories. In certain situations, implementing microprogram memory in ROM is ideal. ROM is the best choice, eg, in systems where the microprogram has a fixed function (such as interpreting fixed machine languages); when debugging is complete and system designers can incorporate the codes in ROM; and when the volume justifies the use of ROMs, because of expensive mask costs.

PROMs have also been widely used in microprogrammed systems because they are field programmable. Obviously, fast read/write RAMs offer more flexibility for building alterable/writable control stores. And, microprogram development usually requires writable control store. Once a system is fully debugged, however, a design can be transferred to

PROMs or ROMs, based on cost/volume/performance considerations.

PROMs and SSI/MSI elements can be used for both the control sequencing and the control store sections of the system. But using registered PROMs, both with and without on-chip diagnostics, results in cost-effective, high performance microprogrammed system design. This design also has lower package counts, lower power dissipation, and faster cycle times than SSI/MSI solutions. Using the Am27S65/75/85 series of registered PROMs, the PROM's access time and the register setup time will determine the cycle time of a control section. For standard versions, an effective cycle time of 47 ns can be obtained (for fast A versions, 37 ns).

Using a diagnostic test technique

On-chip diagnostics, comprising a structured test technique, provide a systematic way to control and observe all portions of a digital system under test. The technique also provides control by allowing the user to set input conditions and system register values. Selected outputs can be monitored to determine whether or not the system is functioning properly. Control and monitoring can also be used at intermediate points in a system.

On-chip diagnostics requires four extra device pins, a duplicate (shadow) of each system flipflop in an additional register, and an extra multiplexer at the input of each system register. The internal system register is accessible through this shadow register in parallel with the normal system register. These two registers serve as the control/observation point and provide the flexibility of parallel operation.

Om Agrawal is department manager of customizable logic in product planning at Advanced Micro Devices, Inc (Sunnyvale, Calif). He holds a PhD in electrical engineering/computer science from Iowa State University.

One of the on-chip diagnostics functions uses the mode input pin which controls the source data for both sets of registers. In a normal mode of operation, mode input is low. When the mode input is low, two things happen. First, the normal system register is loaded with the normal data inputs, under the control of the normal clock input. Second, the shadow register can be shifted independently by clocking its diagnostic clock input. The serial data input serves as the least significant bit of the serially shifted data, and the serial data output serves as the most significant bit of the serial data.

Mode input high allows transfer of data for diagnostics testing. When the mode input is high, several things can occur. The normal system register can be loaded from the shadow register. This initializes the desired register with the proper diagnostic value, which is essential for control. Or, the serial data input pin can become a control pin instead of a data input pin. In this case, if the serial data input is low, the shadow register can be loaded from the system register, effectively sampling the register values. Once the data to be sampled is in the shadow register, it can be shifted out serially for examination. This flexibility of operating the shadow register and the normal system register in parallel allows normal system operation and diagnostics shifting at the same time. Dynamic snapshots of machine states make it possible to diagnose machine malfunctions.

The size of the control store is critical. When diagnostics are incorporated with the macroinstructions

in the microprogrammed memory, the size of the control store grows. On-chip diagnostics eliminate the need for storing diagnostics code in the microprogram memory, thus saving the total control store space. Along with the 4-bit parallel data register (which is intended for normal registered data operations), the Am27S65, Am27S75, and Am27S85 each have a 4-bit shadow register with serial bit-shifting capability. This shadow register is intended to be a copy (shadow) of the normal output register. It can be used in a systematic way to control and observe the output data register in order to exercise any desired system function during a diagnostic test mode.

Using the serial shadow register

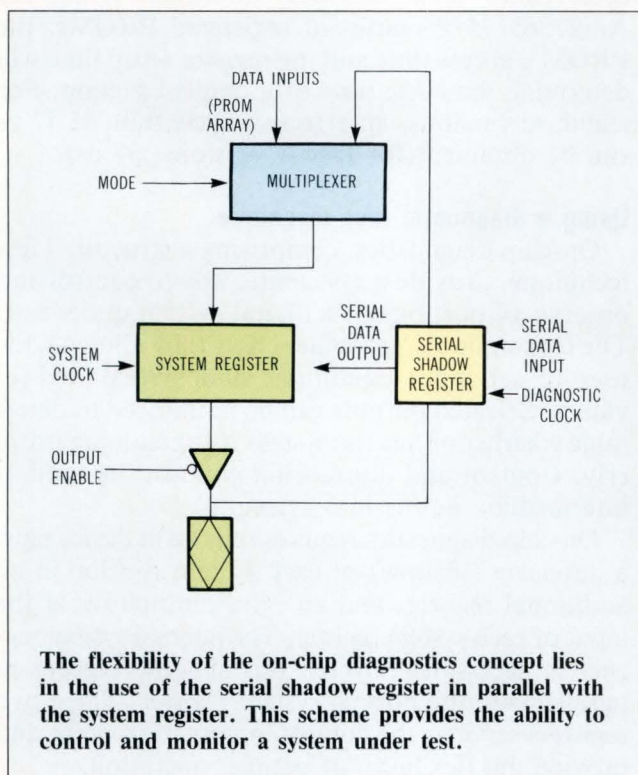
For system control, user defined vectors can be serially shifted into the shadow register and transferred later to the parallel output register. These test vectors can be any microinstruction defined by the user. Once they are loaded in the serial shadow register, they can then be transferred to the microinstruction pipeline register and executed as a normal microinstruction.

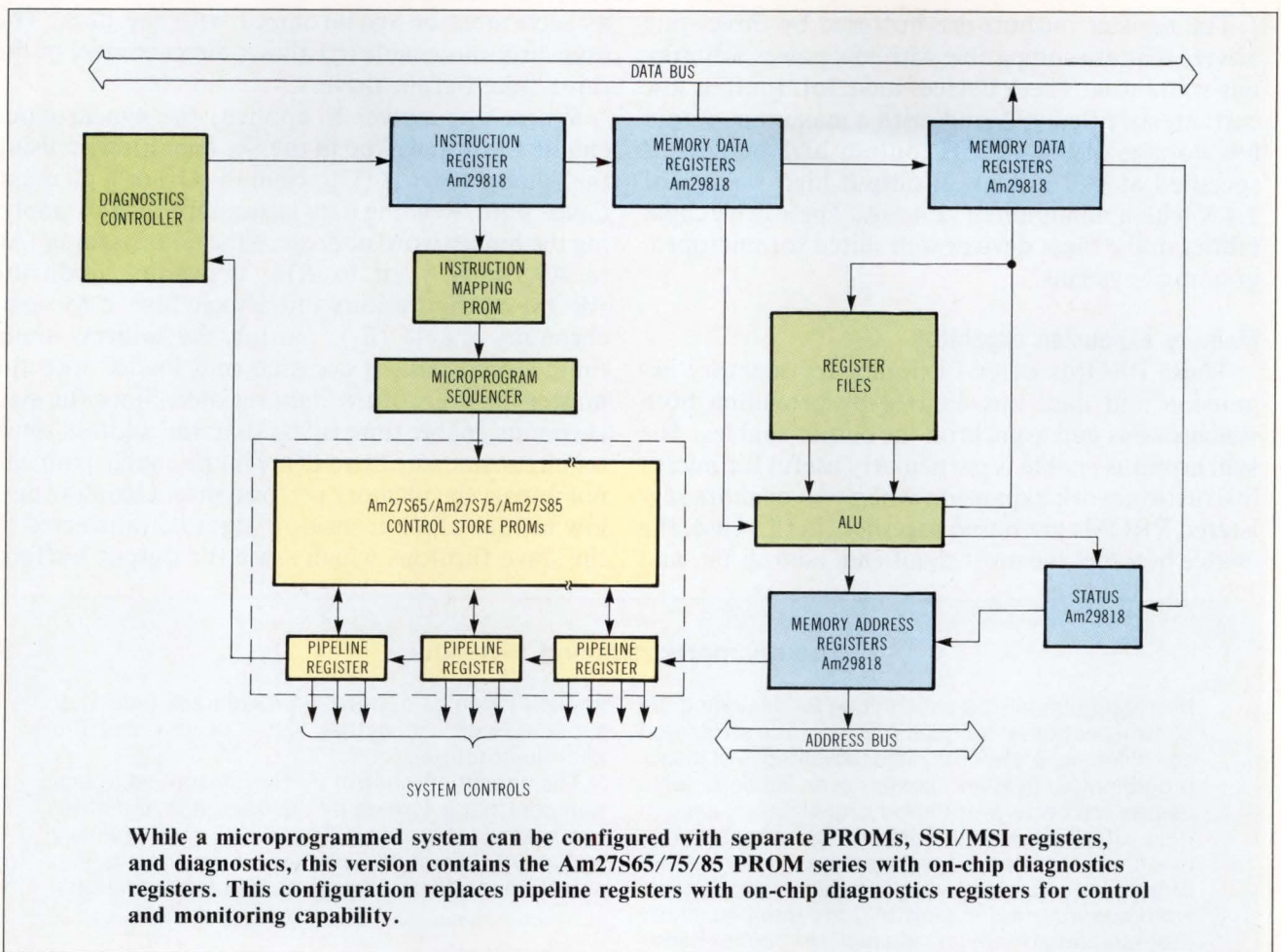
The serial shadow register can take data from the output register or other serial scan paths to test either the PROM contents or the contents of other system elements (for system integrity). The PROM contents can be transferred to the serial shadow register by controlling the output enable signal. To observe other system path elements if the output enable is disabled, the serial shadow register can be loaded with necessary state information.

To fully test the state machines, all possible state transitions must be activated to determine whether or not recovery from illegal states is possible. Inputs to the state circuits can be derived from signals shifted into the microinstruction pipeline register. These signals set the circuit states. Serial loading of the shadow register is equivalent to application of the test vectors. With the application of the clock, the microinstruction is executed, and new states will appear at the outputs for observation.

The on-chip diagnostics capability of the registered PROMs provides advantages for microprogrammed system design. It conserves micromemory size by eliminating the diagnostic code in the control store and increasing application code density. It also allows all internal machine states to be controlled by inserting serial diagnostic control information in the microinstruction register. Register data and snapshots of various machine states with separate on-chip diagnostics in series are available.

In systems where user microprogrammability is desired, serial shadow register concepts can be incorporated to design and build a fully testable microprogrammed system. Most of the macro/micro status





registers can be built with Am29818 devices. The control store memory (which is intended not to change) can be built with the Am27S65/75/85 family. And, the portions to be microprogrammed by users can be designed with the 9151 static RAM (1 Kbit x 4 with a serial shadow register). (The SRAM has the same speed as the diagnostic PROMs.)

Expansion capability

Both user programmable synchronous and asynchronous register initialize and enable (for flexibility and memory expansion) are available in these chips. The programmable initialize capability has been a function of conventional registered PROMs. Built-in initialize allows the contents of an additional user programmable control word to be loaded into the on-chip register. Since each bit of the extra control word is programmable by the user, the initialize function can be used to load any desired combination of highs and lows into the register. This feature can ease implementation of other functions, such as built-in "jump start" addresses.

Applying a low to the asynchronous initialize output enables an immediate load of the programmed initialize word into the master flipflops of the reg-

ister only. This application is independent of all other inputs (including the clock pulse). Applying a low to the asynchronous initialize input loads the programmed initialize word into the slave flipflops of the register independent of all other inputs. To bring the data to the device outputs, the synchronous enable should be held low until the next low-to-high transition of the clock. Following this, the initialize data will appear at the device outputs after the asynchronous enable is brought low.

Initialization serves as a superset of both Preset and Clear functions, since it can be used to generate any arbitrary microinstruction for system reset or interrupt. If all bits of the initialize word are programmed, activating Init performs a register preset with all outputs high. In the unprogrammed state, activating Init performs register clear.

On-chip edge-triggered registers, unlike latches which have gated flipflops, have master/slave flipflops. The on-chip edge-triggered registers simplify system timing since the PROM clock can be derived directly from the system clock without introducing race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The register outputs are buffered by three-state drivers that are compatible with low power Schottky bus standards. These devices have IoL (output low current) specified at 24 mA with a maximum output low voltage of 0.5 V. IoH (output high current) is specified at -3.7 mA at an output high voltage of 2.4 V with a minimum of -2.4 mA. These drive capabilities make these devices well suited for microprogrammed systems.

Memory expansion capability

These PROMs offer flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. The synchronous enable is particularly useful for microinstruction work expansion when two or more registered PROMs are bused together. In this case, the enable becomes the most significant address bit, and

as such must be synchronized with the data. The asynchronous enable (E) allows direct control of the three-state output drivers.

When V_{CC} power is applied, the synchronous enable flipflop will be in the Set condition, causing the outputs (Q0 to Q3) to be in the Off or high impedance state. Reading data is accomplished by applying the binary word address to the address input (A0 to A9, to A10, or to A11, depending upon the PROM configuration) and a logic low to the synchronous enable (E_S). During the address setup time, stored data is accessed and loaded into the master flipflops of the data register. Since the synchronous enable time is less than the address setup requirements, any extra delay in the enable path will not impact the memory performance. Upon the next low to high clock transition, data is transferred to the slave flipflops which store the output buffers.

The microprogramming technique

Microprogramming is a technique for designing the control section of a digital machine in a structured and systematic way. The major advantages of microprogrammed system design over random logic design are better structured organization, ease of field changes, adaptability of microprogrammed machines for different architectures, development of both hardware/software in parallel, and variable word and instruction length. Conceptually, microprogramming offers an "elastic" or "rubber band" machine architecture.

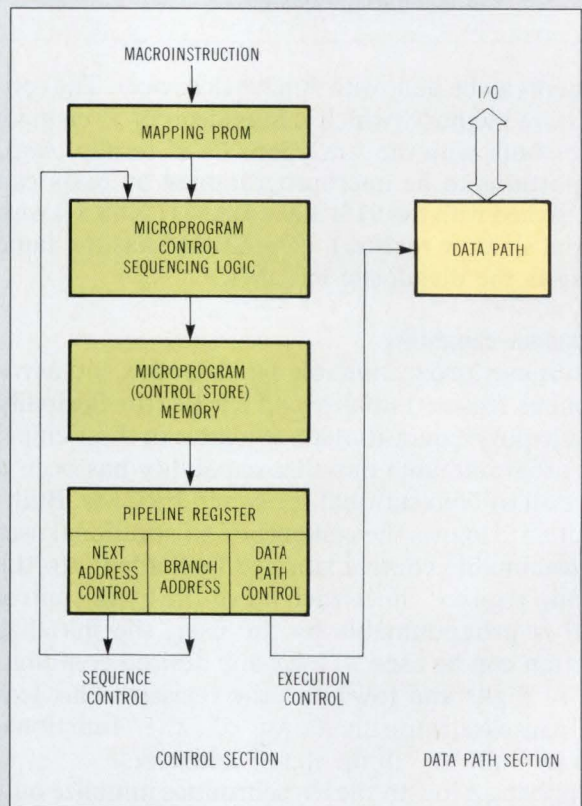
A microprogrammed system has two levels. At the first level are the machine-level instructions—called macroinstructions which are stored in main memory. A row of microinstructions or a sequence of microinstruction rows corresponds to this macroinstruction. Collectively, these microinstructions are a microprogram which resides in the microprogram memory or control store memory.

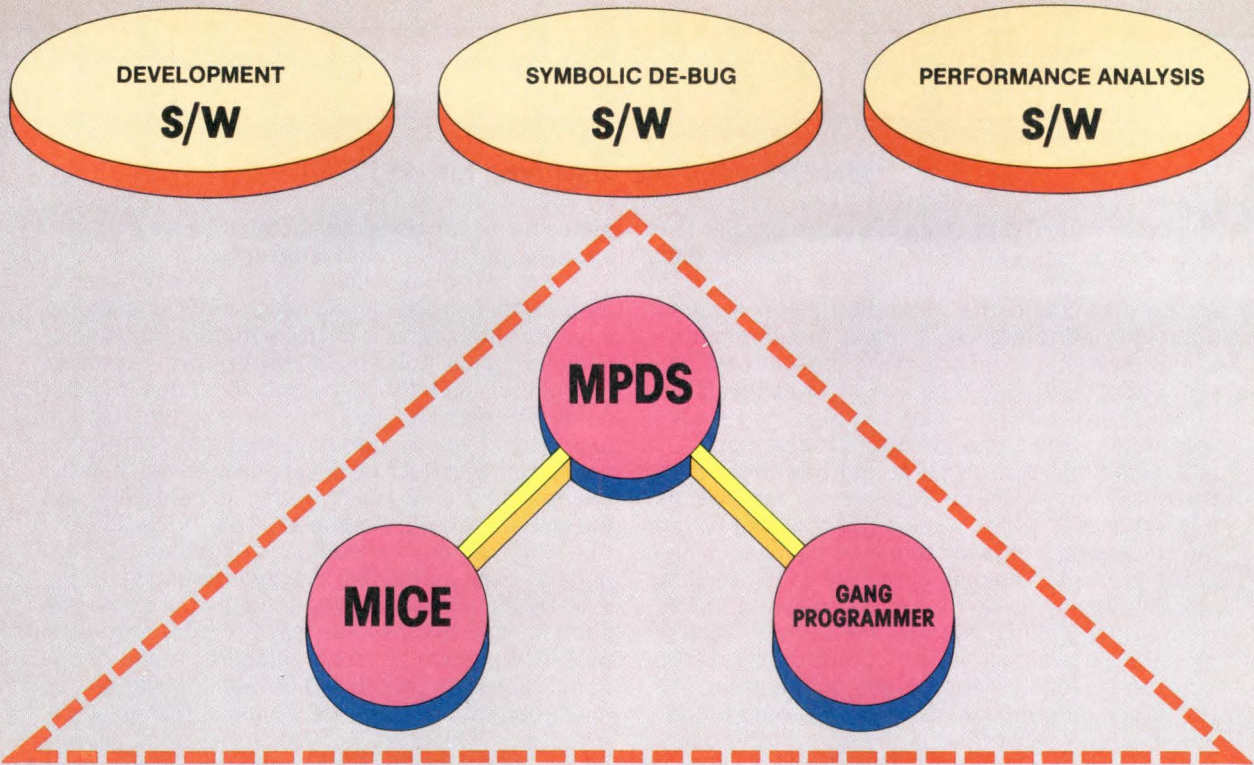
A microprogrammed system consists of a control section and a data path section. The control section has a microprogram sequencer (sequencing logic), a microprogram memory (for storing all microinstructions), and usually some pipeline registers at the output of the microprogram memory for higher performance. The data path section consists of a register file, ALU, and status register. Both the sequencing logic and the execution logic are controlled by appropriate microinstruction bit fields.

The microprogram memory is an N-word deep by M-bit wide memory array—structured to hold all the microinstructions. Each microinstruction is partitioned into user defined fields of various lengths. These microinstruction fields exercise control over all internal resources of the system. Usually a microinstruction must contain sequential control and execution control information. Sequential control information includes the address of the next microinstruction to be executed. This can be either

implicit (such as current micro-address plus 1) or explicit (such as actual value of the specific microinstruction).

The execution control portion describes operation control performed by the data path and other system logic functions. These functions typically include ALU function selection, source/destination selection, shift/rotate control, and I/O operations.





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Pipelining and the registered PROM

The basic idea of pipelining is to split a major task into N subtasks and dedicate hardware for each subtask. Pipelining techniques can be used both at the macro and the microinstruction level for improving performance. If some function can be executed with a straightforward design technique (without pipelining) in T ns and, if the design is partitioned into N stages, then the pipelined system can perform the same function at rates up to T/N ns—resulting in up to an N -fold performance increase. It may not be feasible to achieve the maximum rate either because of the hardware or the nature of the function that is being implemented in the pipeline. The maximum rate of the pipeline clock is obviously limited by the slowest stage.

In a nonpipelined system, the current microinstruction is available at the output of the control store and is fed into appropriate points of the control sequencing section and the processing section. The machine cycle time is the sum of the delays for these three sections. One major disadvantage of this simple approach is that not all internal resources can be used concurrently.

The concept of pipelining can be applied to this system to improve performance. Depending upon where the pipeline registers are used, the architecture of the microprogrammed systems can conceptually result in one of the following: microinstruction-based, micro-address-based, microstatus-based, micro-address instruction-based, microinstruction

status-based, micro-address status-based or micro-address instruction status-based.

In a micro-address instruction status-based system, the microinstruction pipeline register holds the address of the current microinstruction, the micro-address register holds the address of the next microinstruction, and the micro/macro status register holds the result of the previous microinstruction execution. Even though micro-address instruction data-based architecture is supposed to result in the shortest machine cycle time, its microprogramming becomes somewhat complex. This is particularly true when a branch condition is encountered. Care must be used in flushing the pipeline and restoring it to its initial status. Even though cycles may be shorter, more microcycles may be necessary in the pipelined system because comparison and conditional branches would require two instead of one microinstruction (as in a nonpipelined system). However, the increase in microcycles can be alleviated by careful design of the microprogram.

For micro-program systems, a microinstruction status-based architecture is recommended for flexibility and higher performance. Although the control store and microinstruction register can be constructed from standard PROMs and SSI/MSI registers (for instruction pipeline registers), the single-chip register PROM solution of the Am27S65/75/85 series offers performance, reduced package size, and power savings.

If the asynchronous enable is low, the stored data will appear on outputs Q0 to Q3. If synchronous enable is high when the positive clock edge occurs, outputs go to the Off or high impedance state regardless of the value of the asynchronous enable. The outputs may be disabled at any time by switching asynchronous enable to a high level.

Following the positive clock edge, the address and synchronous enable inputs are free to change. Changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications, either enable may be eliminated effectively by tying it to ground.

Microprogrammed system configuration

In this serial shadow register PROM configuration, the Am29818 on-chip diagnostics registers combine the SSI/MSI registers and diagnostics functions, and the advanced PROMs combine PROMs, pipeline register, and the on-chip diagnostics functions. For better control and monitoring, all pipeline registers are replaced by on-chip diagnostics registers.

Incorporating serial scan accessibility in all the macro/micro system registers makes it easier to control/observe and thus diagnose all system failures. Such a diagnosis is accomplished by breaking the feedback paths and by turning a sequential state machine into a number of combined logic blocks.

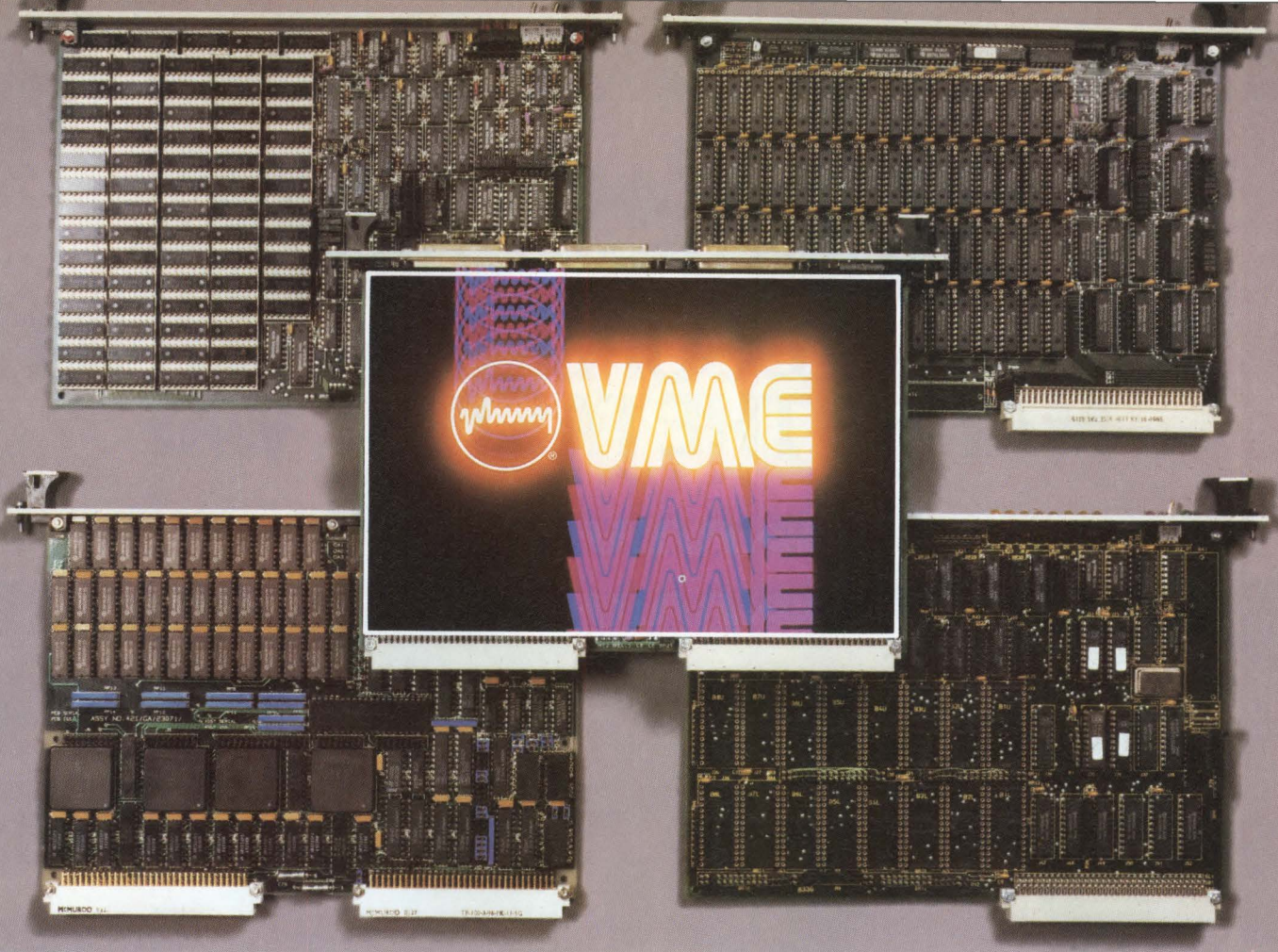
To control/observe a section (such as an ALU), first the microinstruction register is loaded with appropriate microcommands. Then the desired function is executed, and the status information is captured in the status register. The status information can then be serially shifted out and observed to check proper function. Incorporating serial scan capability in most of the major state registers makes it possible to break the major loop into multiple miniloops, and thus reduce the serial scan time. The scan time is proportional to the length of the path the data has to travel serially.

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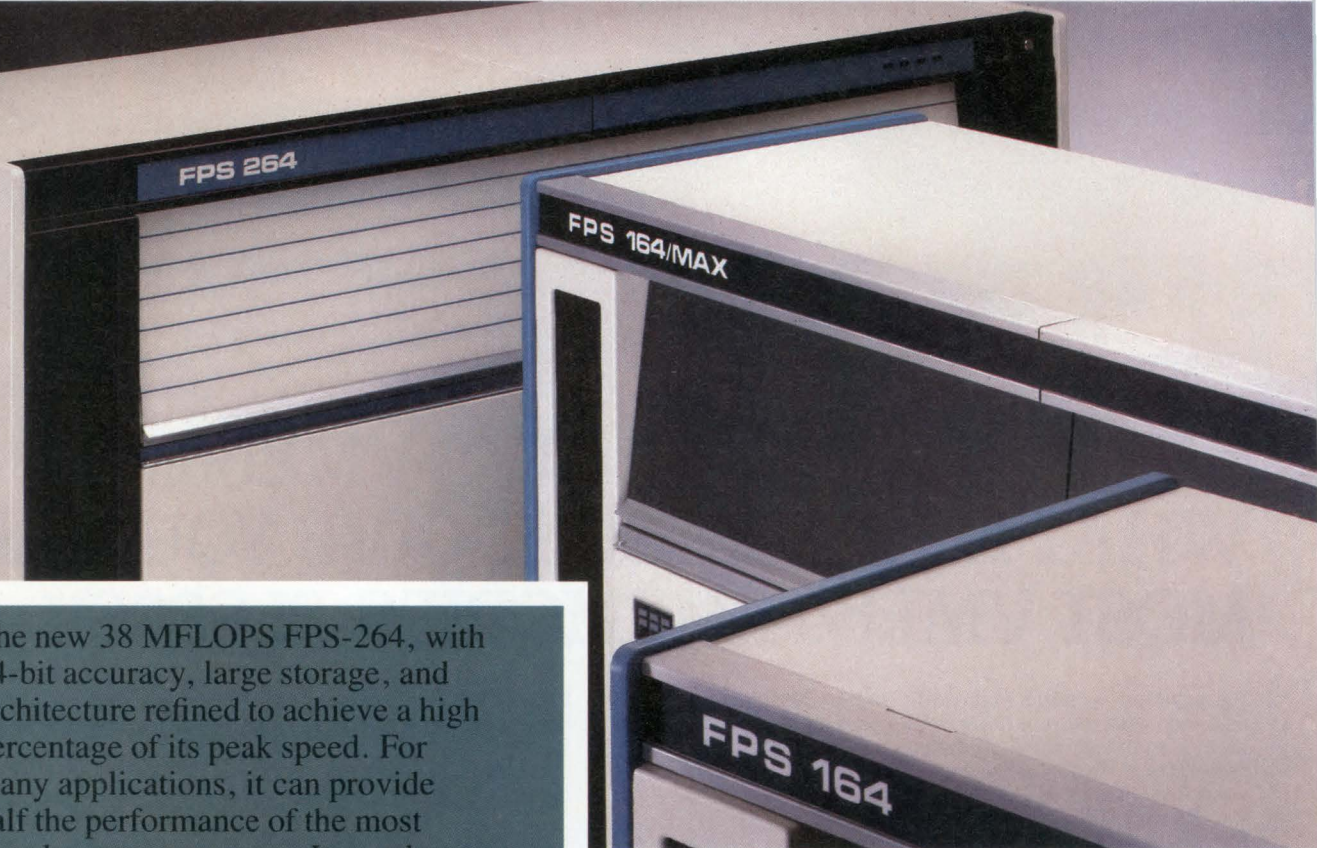
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Logic format	64 bits	64 bits	64 bits
Main memory capacity	4.5 MWords	15 MWords	7.25 MWords
Maximum disk storage capacity	16 Gbytes	3 Gbytes	3 Gbytes
Precision	15 decimal digits	15 decimal digits	15 decimal digits
Vector registers	4 x 2K	124 x 2K (max.)	4 x 2K
Scalar registers	64	184 (max.)	64
Host interfaces	IBM, DEC	IBM, DEC, Sperry, Apollo	
Program Development Software	FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger.		

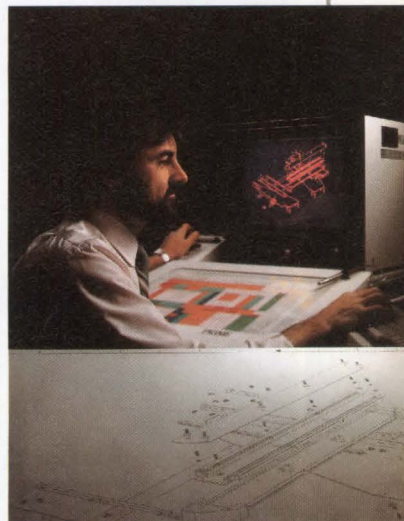
Family Performance Measures

	FPS-264	FPS-164/MAX	FPS-164	
		15 accelerators	1 accelerator	
Peak MFLOPS	38	341	33	11
Peak MOPS	190	1705	165	55
Peak MIPS (Multi-instruction parcels)	19	5.5	5.5	5.5
Typical MFLOPS, LINPACK Benchmark	9.9	20.0	6.0	2.6
Whetstones (64-bit)	20,100	5800	5800	5800
1000x1000 matrix multiply, seconds	53	10	66	189
\$K/MFLOPS (system price/peak speed)	\$16.8K	\$2.5K	\$12.3K	\$27.1K

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TC15G042	4200	156	3	2.5	5.0
TC15G060	6000	180	3	2.5	5.0
TC17G005	540	44 48	2	1.5	3.0
TC17G008	880	52 68	2	1.5	3.0
TC17G014	1400	68 86	2	1.5	3.0
TC17G022	2200	82 106	2	1.5	3.0
TC17G032	3200	98 128	2	1.5	3.0
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NOTES:

¹ For a 2 input NAND gate having a fan out of 2 and 2mm of metal interconnect.
² At 70°C and V_{dd} = 5v \pm 5%

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and Jeff Gruger

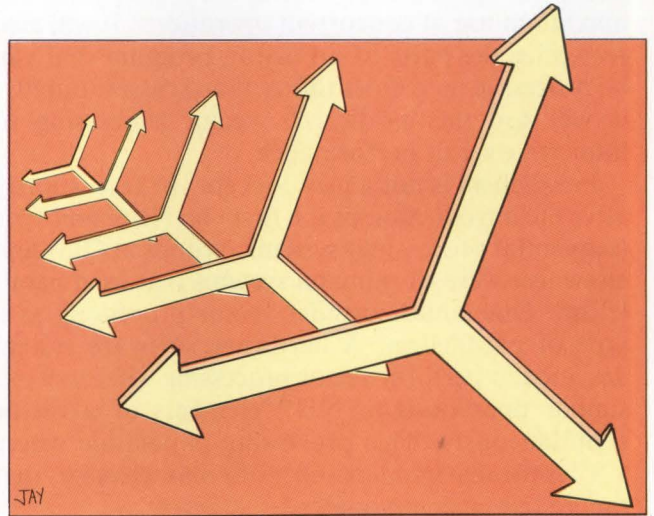
A computer that supports vector processing can perform operations on arrays of data simultaneously. In contrast, the scalar processing used by most computers deals with only one element at a time. In nearly all fields of scientific and engineering research, the ability to perform vector operations rather than scalar operations can mean significant time savings or a more thorough evaluation of a problem. Up to now, however, vector processing has generally been found only in multimillion dollar supercomputers, such as Cray Research's Cray-1 or Control Data Corp's Cyber 205.

By relying on standard technology, Convex Corp has built a supercomputer with concurrent processing and vector processing for approximately \$500,000. The vector processing portion, for example, is built with off-the-shelf logic components and some semi-

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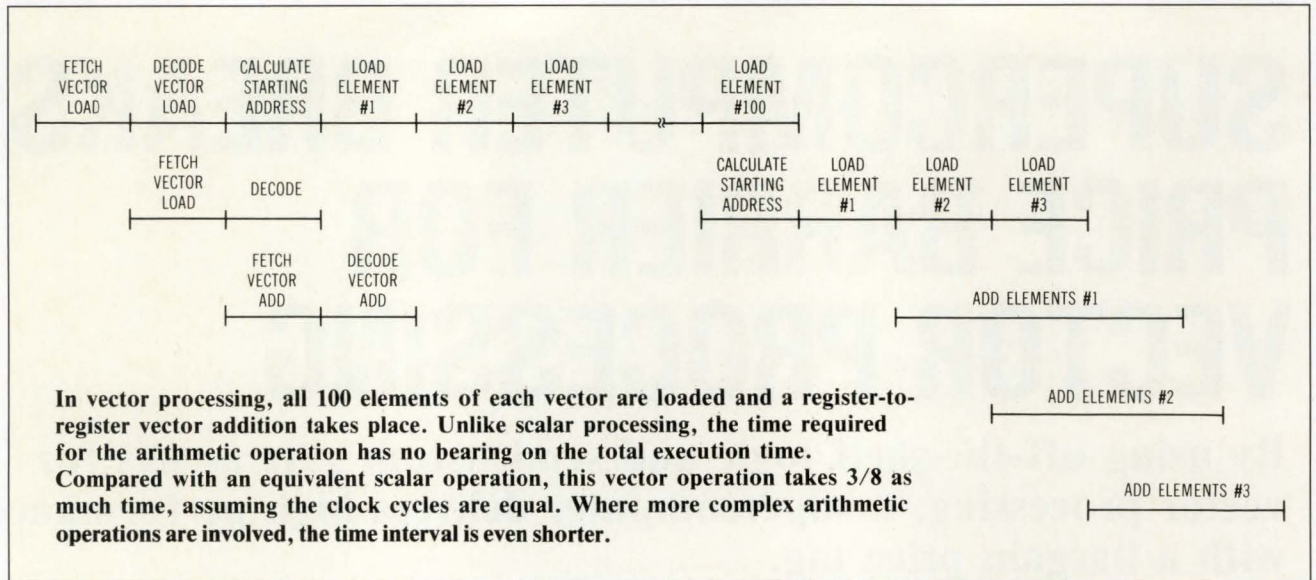
Jeff Gruger is a principal engineer at Convex Computer Corp. He holds an MS in electrical engineering from Southern Methodist University.



custom, low power CMOS gate arrays. This part of the CPU is especially critical in meeting the performance and functionality standards for supercomputer systems.

To attain the degree of functioning and performance needed for supercomputers, Convex designers created an asymmetric parallel processing machine. In essence, the hardware consists of multiple processors for different operations. Thus, the machine can handle instruction decoding, arithmetic computation, and address translation concurrently. Multiple functional units provide concurrent or pipelined processing of specific tasks.

Parallelism (or concurrent operations) can boost computer performance substantially. Taking full advantage of hardware-supported parallel processing requires software designed to use such hardware. Convex developed a globally optimizing and vectorizing Fortran 77 compiler for its machine, which will



automatically schedule instruction execution for maximum use of concurrent operations. It will also recognize the parts of a Fortran program that can be processed as vectors rather than scalars. Finally, it will use the hardware's vector processing to improve overall performance.

Parallelism is not a new concept. In fact, shortly after the introduction of the first von Neumann-type (sequential processing) systems, groups at IBM and elsewhere were working on systems that used parallelism. One could consider vector processing as a type of parallelism. A hardware/software system designed to perform vector processing will carry out similar operations on "N" elements of a vector simultaneously. This processing is possible where "N" is the maximum number of vector elements that the system accommodates.

Advantages of vector processing

As mentioned, most existing computers are scalar processing systems. They add two numbers by loading one number into one register and the other number into a second register. They perform the addition and store the results in a single register. Then they generally store the result register contents in memory. Even in a case where the system has to add a matrix column of 100 elements to a row of 100 elements, it would have to do redundant load, load, add, and store operations on each element sequentially.

Even in a highly pipelined machine, certain tasks have to wait while previously initiated instructions are completed. Thus, while the effective execution time of a load, load, add, and store may be less than the sum of the execution times of the individual instructions, the execution time is still significant. In most machines, the most important portion may be the arithmetic operation itself. This effective execu-

tion time can then be multiplied by the number of successive operations (100 in this example) to determine the total execution time.

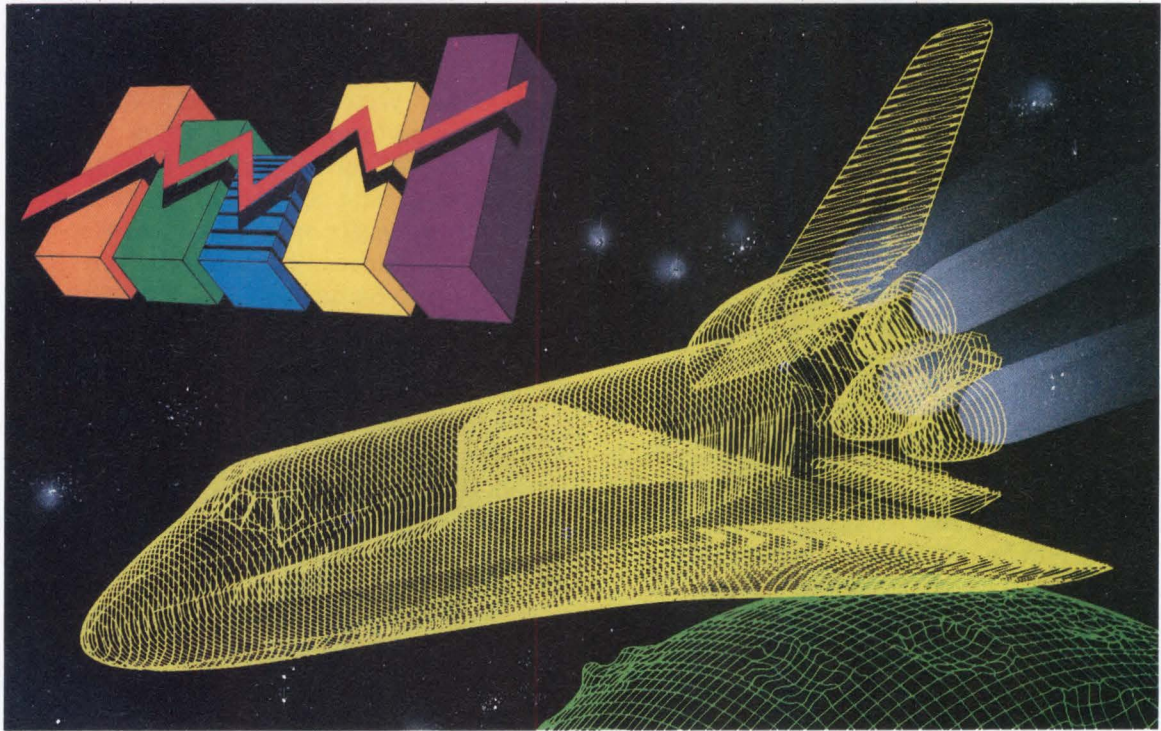
In contrast, a vector processing system that can accommodate 100 or more elements in its vector registers (or accumulators) is more efficient. It loads all matrix column elements, loads all matrix row elements, does additions across all elements at once, and stores the full set of result elements in a single vector register. There are no redundant loops, and the entire calculation is accomplished much faster than in the case of a scalar system.

This process begins when the vector operation initiates the load of the first 100 elements. As soon as it is complete, the load of the second set of 100 elements begins. The addition of the first elements of each set begins as soon as both are loaded, even if successive elements are still being loaded.

Similarly, as soon as the last element of the second set of data is loaded and the memory bus is free, the store of the first calculated result can take place, the result having been long since calculated. The effective execution time basically reduces to the time required to load each set of elements and store the results and a few additional cycles of initial startup overhead. If an element can be loaded or stored per cycle, the total time for this vector process would be 300 cycles. Note also that the time for the arithmetic operation does not count in the total required execution time.

A more complex operation, such as a floating point multiply that requires two more clocks, results in an effective execution time for the sequential, scalar process that is 1000 cycles instead of 800. However, in the vector process, since the arithmetic operation time has no bearing on total execution time, the results remain at 300 cycles.

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Scientific programs in Fortran source code are written to be run on a scalar machine. Thus, the statements

```
DO 10 I=1,N
C(I)=A(I)+B(I)
10 CONTINUE
```

call for the addition of two vectors, A and B, using an iterative sequence. For a vector processing system, this set of statements would normally have to be rewritten to take advantage of the vector processing hardware capabilities. The Convex Fortran 77 compiler, however, does that automatically. It compiles that set of statements to allow the use of vector instructions and registers. The programmer makes no changes to the original source code.

Vector processing offers a benefit that is usually only as good as the programmer's ability to restructure programs that can take advantage of it. The Convex Fortran 77 compiler takes much of that pressure off the programmer. In effect, there exists a symbiotic relationship between the compiler and the hardware system. Because they were developed simultaneously, matching them up for optimal performance is possible.

Flexible processing

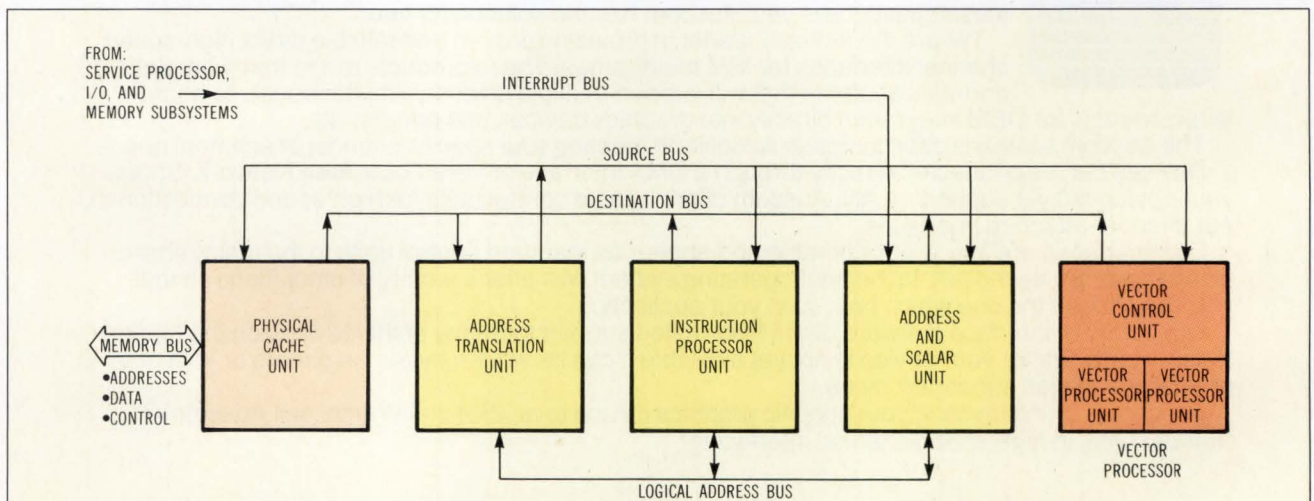
The Convex C-1 supercomputer is a memory-centered machine comprised of three main subsystems—memory, I/O, and a CPU. The CPU contains five asymmetric processors that can execute their tasks concurrently. One of these processors is the vector processing unit.

The vector processing unit consists of three independent microprogrammed processors. One handles loads and stores, one handles vector addition and logical operations, and one performs vector multiplication and division. The vector processing unit will work in conjunction with the scalar processing unit and permits vector/scalar operation.

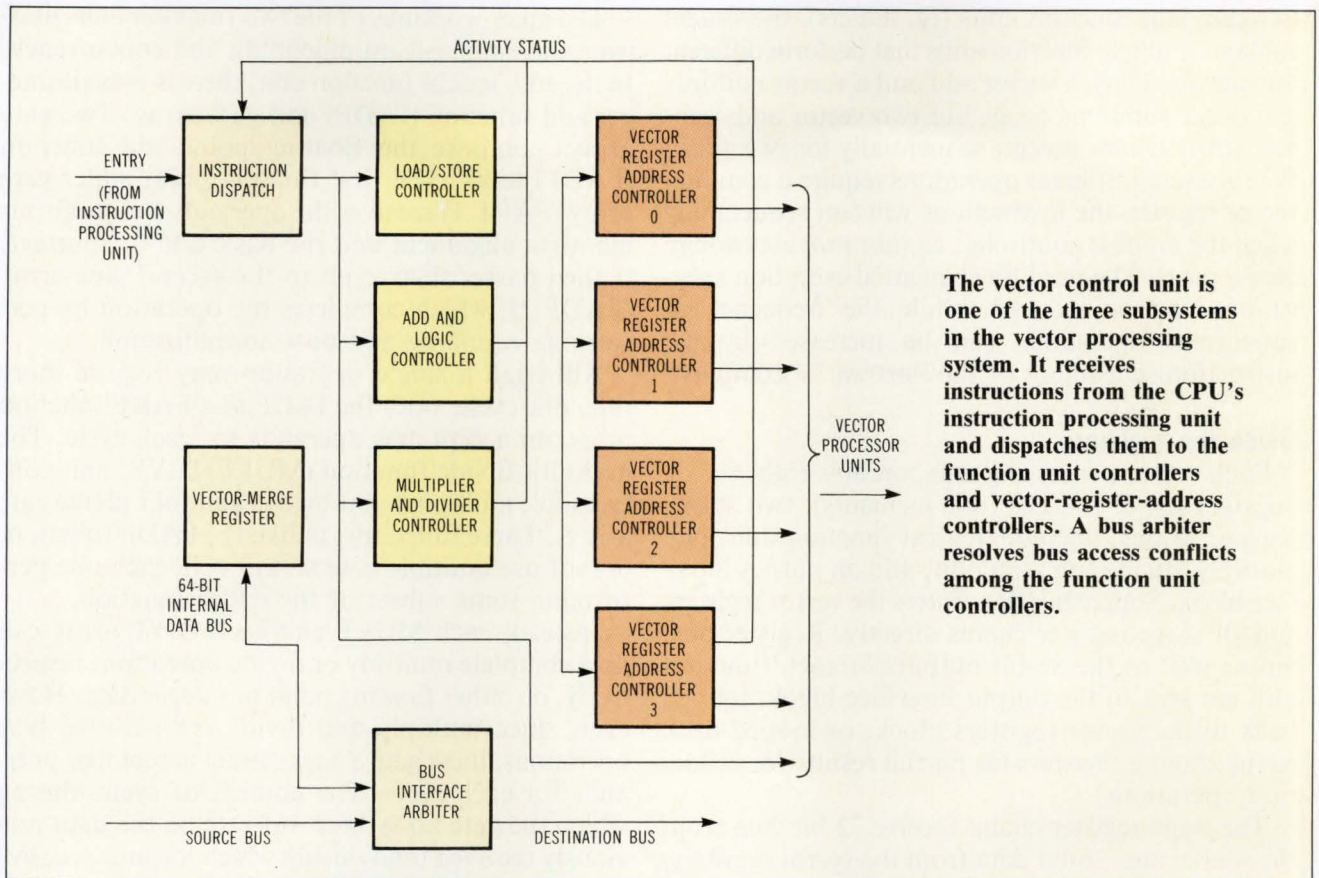
Whether performing vector/vector or vector/scalar operations, the supercomputer first loads operands in the appropriate accumulators. Then it performs a register-to-register operation. Each of the eight vector accumulators can accommodate up to 128 operands of up to 64 bits each. These operands can be integer, logical, or floating point data types.

Three special registers support vector operations. A 128-bit vector-merge register supports element-by-element comparisons and manipulations for vector compression, masking, and merge operations. The 32-bit vector stride register specifies the distance in bytes between adjacent array elements located in memory. Finally, the 8-bit vector-length register specifies the number of elements contained in a vector accumulator. Thus, if a vector of less than 128 elements is loaded, its actual length is specified by vector length and the remaining elements in the accumulator are left unchanged. The vector-length register plays a role in the C-1's ability to "strip mine" or process arrays that are larger than 128 elements.

The vector processing unit is a combination of three subsystems: the vector control unit and two vector processor units. The vector control unit controls vector instruction dispatching, the four vector address controllers, and their eight vector registers. The vector control unit also handles destination and



The Convex C-1 CPU is made up of five subsystem units—physical cache unit, address translation unit, instruction processor unit, address and scalar unit, and vector processing system. The interface to memory is via the physical cache unit and the memory bus. Internally, the CPU subsystems are linked via a dual-bus structure—the source and destination buses. This structure reduces the chance of bus contention and increases overall data bandwidth.



The vector control unit is one of the three subsystems in the vector processing system. It receives instructions from the CPU's instruction processing unit and dispatches them to the function unit controllers and vector-register-address controllers. A bus arbiter resolves bus access conflicts among the function unit controllers.

source bus arbitration and determines the microprogram sequences for the load/store, addition/logical, and multiply/divide controllers. In effect, the vector control unit provides all addressing, data-path selection, opcodes, and synchronization for the vector processing unit.

One of the two vector processor units is designated "odd," and the other is "even." The supercomputer has a 72-bit data path for load and store operations (64 bits plus parity). For data types of 32 bits, such as single-precision floating point data, two elements can be stored during a single clock cycle. Thus, the "odd" vector processor unit receives the odd numbered elements (elements 1,3,5 and 7) and the "even" vector processor unit receives the even numbered elements (elements 2,4,6 and 8). Once the arithmetic operations are complete and a vector store begins, both vector processor units store data simultaneously. (One sends its data out on the lower bits and the other sends its data out on the higher bits.) This doubles the performance for vector operations with data types of 32 bits or less.

How subsystems communicate

The instruction dispatch block of the vector control unit receives vector register specification fields, operand size, processor-status-hazard, and entry address information from the instruction processing

unit. It sends microcoded entry address, function-unit opcodes, and address controller reservation information to the appropriate functional controllers and/or vector register address controllers.

The load/store controller works concurrently with the other controllers. It specifically handles vector merges, masks, compresses, moves, loads, and stores, and contains a 4 x 56-Kbit control store. The add/logical and multiply/divide controllers each contain a 4 x 48-Kbit control store. Both controllers fetch source operands and format them for processing. Adds are sent on to either the floating point or integer functional units. The multiply/divide controller sends formatted operands for multiply or divide operations to multiply or divide function units.

Four vector register address controllers provide addresses to the vector registers on vector processor units. Each controller serves two vector registers. Each of these controllers can generate two independent addresses for independent read or write accesses of the vector register within a processor clock cycle. Finally, a bus interface arbitration block permits movement of data between the internal (64-bit) data bus and the source or destination buses. It also decides which of the three function controllers has access rights to these buses.

The vector processing unit permits concurrent operations on multiple operands. As an alternative

to redundant function units (eg, adders), the system contains multiple function units that perform different operations. Thus, a vector add and a vector multiply can occur simultaneously, but two vector adds cannot. (Instructions execute sequentially for two adds.) When several different operations require a common vector register, the instructions will run sequentially when the address controllers cannot provide enough access ports. The need for sequential execution reservations can be reduced, while the frequency of concurrent operations can be increased by the instruction-scheduling of the Fortran 77 compiler.

Inside the registers

Each vector processing unit contains eight vector registers (64 of the 128 total elements), two stage-register chains, one add/logical function unit, one multiply/divide function unit, and an output interface block. Source bus data enters the vector registers and/or stage-register chains directly. Register output as well as the 36-bit outputs of each function unit are sent to the output interface block, looped back to the vector registers block, or looped back to the staging registers (as partial results for reduction operations).

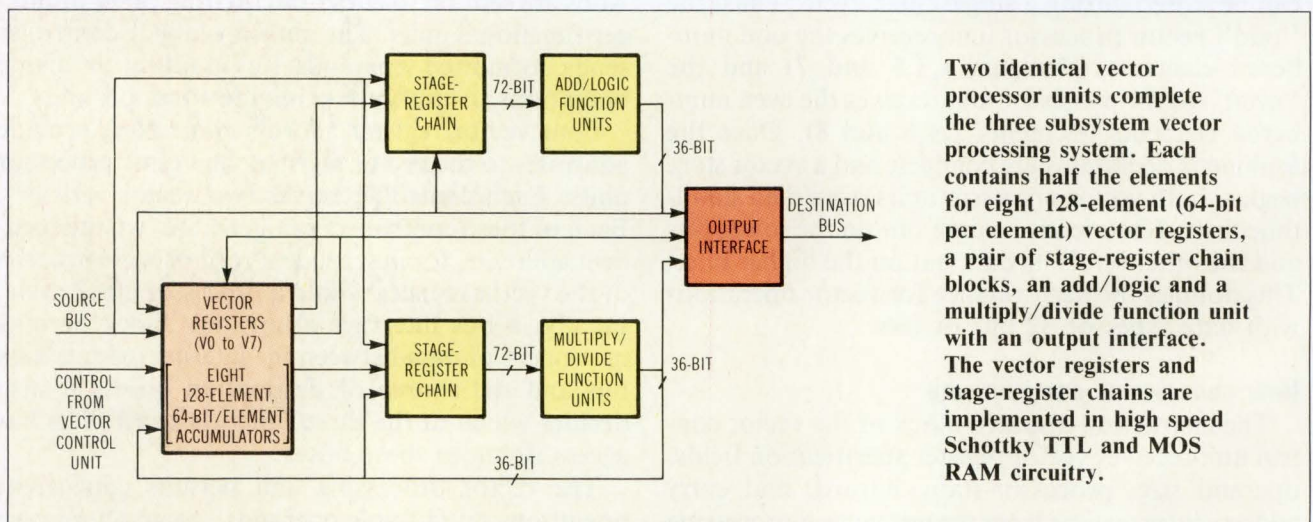
The stage-register chains receive 72-bit data from the source bus, 36-bit data from the vector registers, and 36-bit data from the function units. This data enters an input multiplexer whose output proceeds through staging registers to a word-swap multiplexer. Then it goes through a parity checker and on to the appropriate function units. These stage-register chains hold scalar values transferred from the address and scalar unit (via the source bus). These values are then used in vector/scalar or scalar/scalar operations. In addition, these blocks assemble two 36-bit operands into one 72-bit operand for input to one of the function units. They also store partial results for vector reduction operations.

The inner workings of the two function units illustrate the emphasis on pipelining and concurrency. In the add/logical function unit, there is a single integer add function (IADF) unit gate array. Two gate arrays compose the floating point add function (FADF) units. The first floating point adder gate array (FADF 1) receives the operands and performs mantissa alignment and the basic add or subtract. It then passes that result to the second gate array (FADF 2), which completes the operation by performing rounding and post-normalization.

Although a single operation may require more than one cycle, both the IADF and FADF function units can accept new operands for each cycle. The multiply/divide function (MULF/DIVF) unit contains five multiplier gate arrays and four divide gate arrays. These functions, unlike the FADF function, do not use multiple gate arrays with each one performing some subset of the entire function.

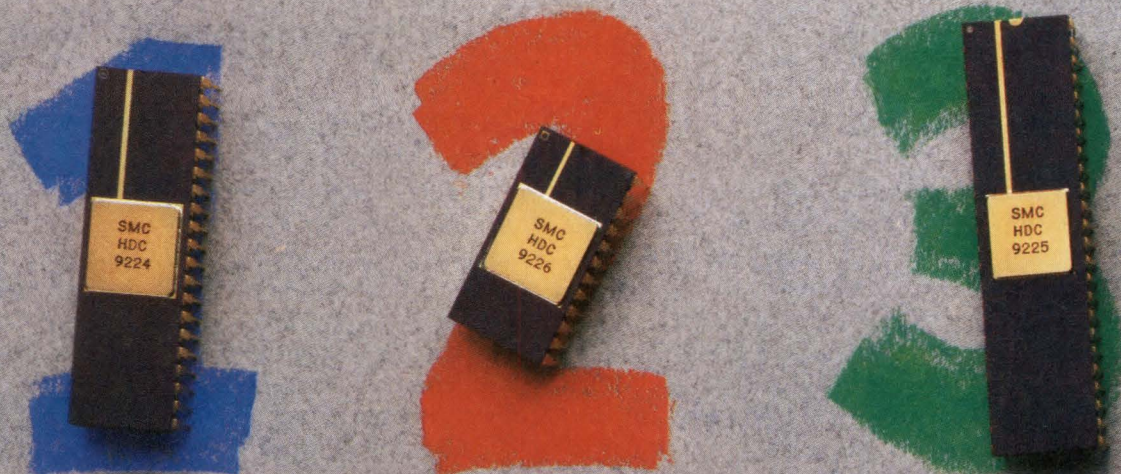
Instead, each MULF and each DIVF array can do a complete multiply or divide operation, respectively, on either floating point or integer data. However, since multiply and divide are iterative type operations, these gate arrays cannot accept new operands for each cycle. The number of cycles during which the gate array must operate on the data previously received (and during which it cannot receive a new operand) depends on the data type.

In multiplication, the greatest number of cycles during which any MULF gate array cannot accept new data is four. Therefore, five MULF gates are used. While the first MULF is busy for up to four clock cycles, the other four MULFs can each accept a set of operands, one each per cycle. When the fifth succeeding cycle occurs, the first MULF is then ready to accept that fifth set of operands. Thus, the five MULFs insure that a set of operands for multiplication operations are accepted on every clock. A similar interface is used with the four DIVFs, although



Two identical vector processor units complete the three subsystem vector processing system. Each contains half the elements for eight 128-element (64-bit per element) vector registers, a pair of stage-register chain blocks, an add/logic and a multiply/divide function unit with an output interface. The vector registers and stage-register chains are implemented in high speed Schottky TTL and MOS RAM circuitry.

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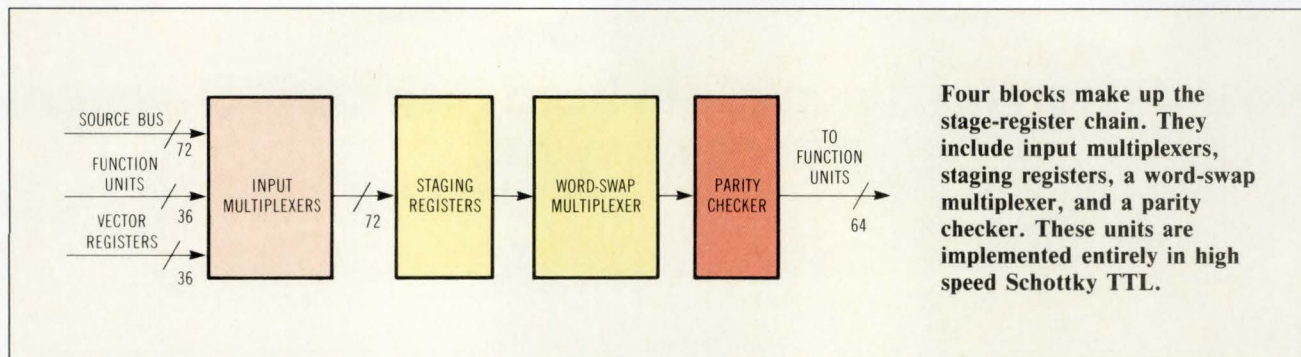
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these operate at a slower operand rate. Both function units receive their input from the stage-register chains and pass their outputs through parity generators to the output interface block.

Creating a winning combo

A combination of high speed Schottky TTL components, high speed MOS RAMs, and 8000-gate CMOS gate arrays implement the vector processing system. The TTL components are used for control logic, whereas the CMOS gate arrays are used in the arithmetic data paths. There are five distinct CMOS designs: a pair for the FADF, and one each for the IADF, MULF and DIVF units. CMOS was partitioned this way so that the strictly arithmetic and well-understood functions are done in semicustom form while the rest is implemented in off-the-shelf logic.

Chiefly by virtue of its hardware design (particularly its vector processing unit), the C-1 system can execute the Livermore loops benchmark at more than 6 million floating point operations per second. For comparison, the Cray-1 performs the same benchmark at a rate of 26 MFLOPS.

A pipelined system architecture allows design instructions to be overlapped, thus decreasing overall execution time. For example, while one instruction is being fetched, an earlier one is being decoded and a still earlier one is being executed. In effect, three instructions are in various stages of being carried out simultaneously, instead of sequentially.

A similar approach can be designed into a vector processor to permit overlapping of operations. In essence, it is a form of pipelining on an operand rather than an instruction basis. In a case where two vectors of "N" elements each are to be added, and the sum multiplied by a third vector of "N" elements, the usual process would be for the addition to be completed first. The multiplication would then follow. In chaining, as each element in the first vector is added to each element in the second, that sum can be multiplied by the appropriate element in the third vector. Thus, the multiplication operation follows closely on the heels of the addition operation, element-by-element, instead of being delayed until

the complete vector-to-vector sum has been calculated and stored.

Because of the independent function unit design of the C-1 supercomputer, chaining can occur among all three. For example, load, add, and multiply operations can be chained. Similarly, add, divide, and store operations can be chained. The effect chaining has on performance can be significant. In the case of 128-element vectors of 64-bit floating point elements, it would take 39 μ s to load one element; add to a second, and multiply to a third, (already in vector accumulators); then store the result in a different register, if done sequentially. If these operations were chained, however, the time required would be 13 μ s.

Vector processor design using high speed Schottky and low power dissipation CMOS ICs enabled Convex to build a hardware system that is much faster than any supermini in handling floating point operations. The C-1 cannot match the performance of the multimillion dollar supercomputers, but it does not require ECL or gallium arsenide technology and sophisticated freon cooling systems either. It fits in a standard 19-in. rack, is air cooled, and needs no special electrical power considerations.

As one of five subsystems making up the supercomputer's CPU, the vector processing system makes a key contribution to the system's performance. Working in conjunction with the optimizing and vectorizing Convex Fortran 77 compiler, the C-1 hardware, and especially the vector processing system, enables the system to run most existing Fortran programs faster than any scalar machine.

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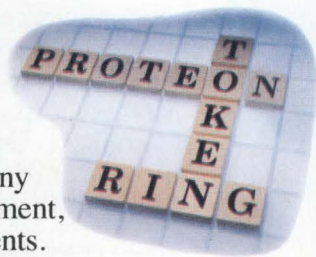
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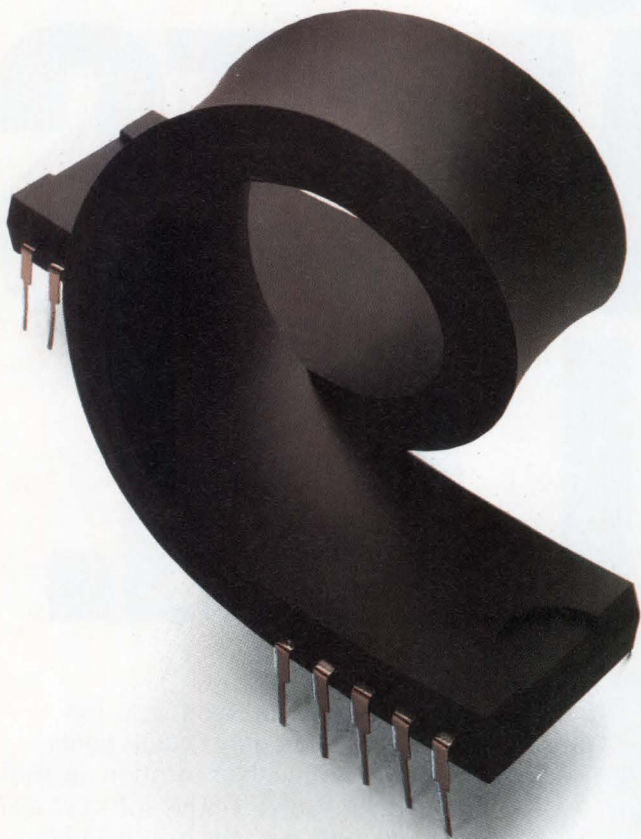
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STANDALONE UNIT SATISFIES STORAGE AND BACKUP NEEDS

Designers need more intelligent and flexible memory systems. Such units could take advantage of technological improvements in disk drives and have only a minor impact on existing hardware and software.

by **Kenneth J. Hallam**

Changes have occurred in the operating environment with systems becoming more involved in realtime processing, graphics, transaction processing, or networking. All of these applications require more storage with faster access. They also take considerable time from the CPU to manage and multiplex the multi-user requests and therefore leave less time for storage needs.

Incorporating new storage technology into existing systems often requires changes in both system software and hardware. Even minor adjustments can call for major changes in software I/O drivers or operating systems. Similarly, the existing hardware may not be able to handle the speed of a faster data transfer rate.

Surveying the issues

Increased storage on the average system, plus growth in data density and transmission rates, can increase substantially the likelihood of data transfer errors, correctable or otherwise. This requires additional software for error recovery. The most com-

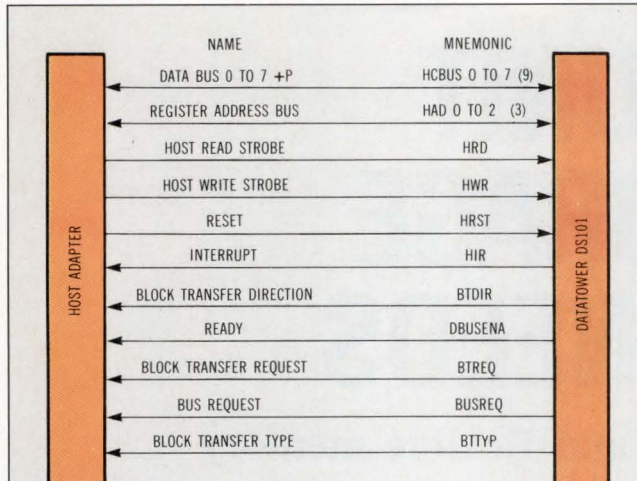
mon error recovery technique is to retry the failed operation. Other methods include repositioning the moving head actuator, changing the timing of the read circuitry, or using an error correction code. Unfortunately, most of these methods require CPU participation. Since many recovery operations involve mechanical motion, the time demands on the CPU can be detrimental to the user, even to the extent of halting all other activity.

Many Winchester users wrestle with the problem of factory defect listings. All of these drives have some permanent defect locations identified during factory testing, which are provided on a printed list and are written on a specified area of the disk. In most system applications, this information is entered by hand, if it is used at all.

Backup is another critical issue on most systems. Small multi-user multitasking environments usually operate with Winchester disk storage of less than 30 Mbytes. Backup is usually performed by floppy disks. This operation is tedious and inefficient, and as the data base grows, the backup operation becomes more onerous. A reasonable backup procedure could be developed by adding a tape drive, a suitable controller, and the appropriate software. While the backup operation is in progress, however, no other tasks can be performed: the multi-user, multitasking environment becomes a single-user batch operation.

Since the Winchester drives are not removable, some alternate media that can be removed and placed in a location remote from the CPU are necessary for disaster protection. The removable

Kenneth J. Hallam is systems product manager at Priam Corp (San Jose, Calif). Mr Hallam is responsible for marketing the Priam controller and subsystem products.



Interface signals between the DataTower storage system and a host adapter board consist of an 8-bit bidirectional bus plus parity, a 3-bit unidirectional register-address bus, 8 unidirectional control lines, and a reset line.

Winchester disk is often touted as the answer to the backup problem. It has yet to be demonstrated, however, as a reliable and cost-effective solution. Most of the new removable Winchester drives have not been on the market very long, and the media cost is still high.

Alternate solutions

An alternate solution for smaller systems is the streamer tape cartridge drive. These drives are less expensive than the half-inch reel-to-reel drives (used on most larger systems) and the QIC-02 and QIC-24 standards offer some relief from the series of competing interfaces and formats. Both reel-to-reel and cartridge streamers, however, suffer the same handicap in backup applications: they tie up system resources.

The Priam DataTower storage system helps solve some of these problems by offering an integrated storage and backup solution, with the device interfaces hidden from the system. At the heart of storage system is the DeleGate model DS101, an intelligent peripheral control system. It provides a high degree of data integrity by incorporating features such as transparent defect mapping and automatic error detection and correction. The DS101 can access data in physical and logical addressing modes. In addition, its device-to-device copy operation performs without using the host system bus and allows concurrent access to disk storage. The DS101 also provides isolation for the CPU hardware and software from device characteristics. Consequently, as device technology evolves, new devices may be added without major impact on the system environment.

The interface at the I/O plug of the DataTower is a generic microprocessor-oriented bus, with a full handshake on all transfers. It uses a 37-pin sub-miniature D connector with 21 signal conductors, 11 ground returns, and 5 reserved conductors. The command structure uses five basic commands for most system I/O activity: Read, Write, Format, Copy, and Resume. The command repertoire is quite extensive, providing a variety of options and diagnostic activities.

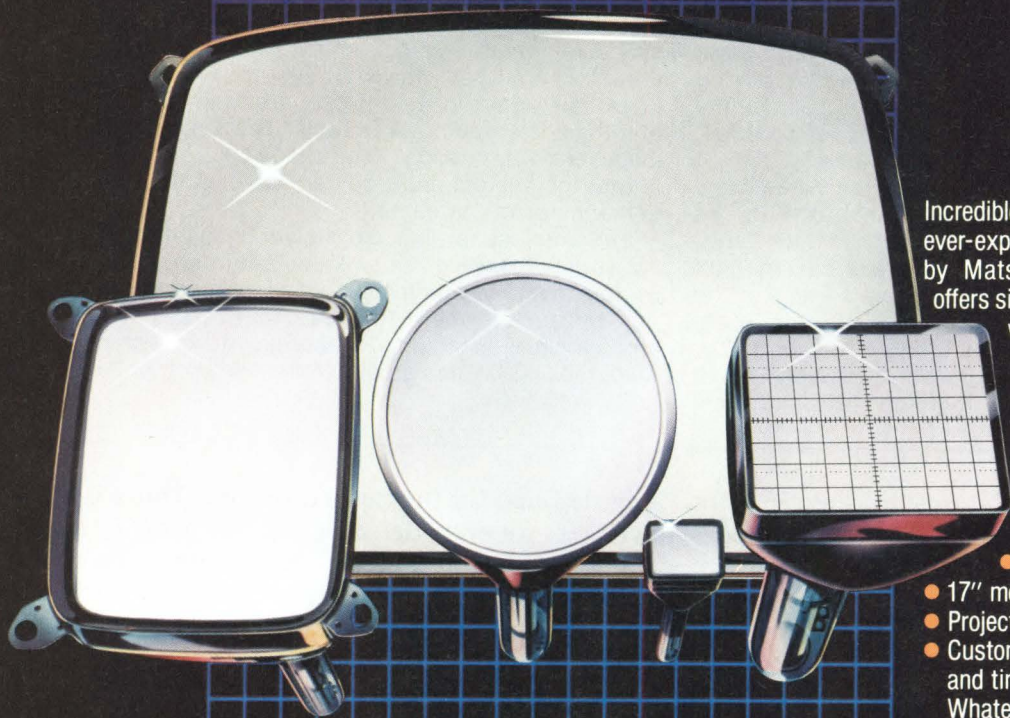
Using transparent defect mapping and automatic error detection/correction, the peripheral control system provides a high degree of data integrity.

The host system communicates with the DataTower across an 8-bit bidirectional bus through eight addressable registers located in the DS101 board. These registers, collectively known as the register file, are addressed via a 3-bit unidirectional register address bus that originates in the host system. They are loaded with command information by the host and read for status information upon command completion. The DS101 offers two basic types of commands: register-based and packet-based.

Register-based commands are the basic form of command structure, and are used for all I/O devices. The host system addresses the registers each in turn, loading them with the command parameter information. The command register, register 0, is loaded last. When loading, this register acts as an interrupt to the microprocessor on the DS101 and command execution begins. Upon command completion, the

Register File General Format		
Command Initiation	Register Number	Command Completion
Command	0	Interface status
Block output	1	Block input
Parameter 0	2	Result 0
Parameter 1	3	Result 1
Parameter 2	4	Result 2
Parameter 3	5	Result 3
Parameter 4	6	Result 4
Parameter 5	7	Result 5

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Past imperfect

In the late 1950s, the data processing industry began to use random-access magnetic storage devices, such as drums and disks, all of which were nonremovable. Magnetic tape was used as the backup or archival storage media. Access speed improved with the use of multiple heads and the introduction of voice coil actuators for the moving head assemblies. Along with advances in recording technology and manufacturing techniques for the high precision heads and media came removable disk packs. These disk packs effectively replaced tape as the primary storage element outboard of the CPU. They provide an acceptable backup solution, although not as cost effective as tape.

Fixed-disk technology broke into the marketplace with Winchester technology in the mid-1970s. As the technology moved to higher bit and track densities, the low mass read/write heads became still smaller and had to fly closer to the surface of the media. Contamination became the overriding concern in disk drive manufacturing.

Difficulties in holding the incredibly small mechanical tolerances required for removable

media led to the use of fixed media in a sealed or tightly controlled enclosure. Although they are non-removable, Winchester drives have enjoyed wide market acceptance due to their high density, high performance, and excellent reliability.

Tape serves as the primary backup medium for most large systems, but tape densities have not improved by the same order-of-magnitude that disk densities have. A low cost alternative to the high speed, refrigerator-sized, traditional reel-to-reel tape units has emerged, however. The streaming tape drive takes data in a continuous stream without starting and stopping. As a result, the drive can be made relatively cheaply. The penalty paid, however, is that the system must be dedicated to the data demands of the streamer.

Streamer tapes also are slower than the disk drives they back up. This places a burden on the system memory, which must act as a speed matching buffer between the disk and tape. The emergence of an industry-supported interface standard, the QIC-02, has greatly increased their popularity, however.

register file will contain status information for that command. Register 1 is used to transfer blocks of data in both directions. The data transferred through register 1 may be parameter or status information for a packet-based operation, or user data recorded or read from the disk. DMA or programmed I/O sequences handle transfers in and out of register 1.

The optional packet-based command passes more parameter information. It is initiated with the register command transfer packet. Packet commands are used in two instances: to transfer extended parameters needed to use the extended features available with the Format command or to initiate the device-to-device Copy command. In addition to the register file status, an extra 36 bytes of packet status may be read upon completion of a packet-based command.

Formatting considerations

Many formatting variations are available: with or without defect mapping, with or without several levels of interleaving, and with or without ontrack sector sparing. These options are selected through a register-based Format command or, for the more advanced/optimized formats, a packet-based Format command. Sectors from 256 bytes to 2 Kbytes may be used with the DS101.

The optional features of DataTower's Format command make it unique. Two basic formatting operation modes are possible. The first is traditional disk formatting: defective areas are flagged and an alternate cylinder area of the disk holds the informa-

tion destined for the flagged sectors. This requires two seeks for every defective sector, one to the alternate cylinder and one back to the user area. This formatting method makes use of the factory-supplied defect information.

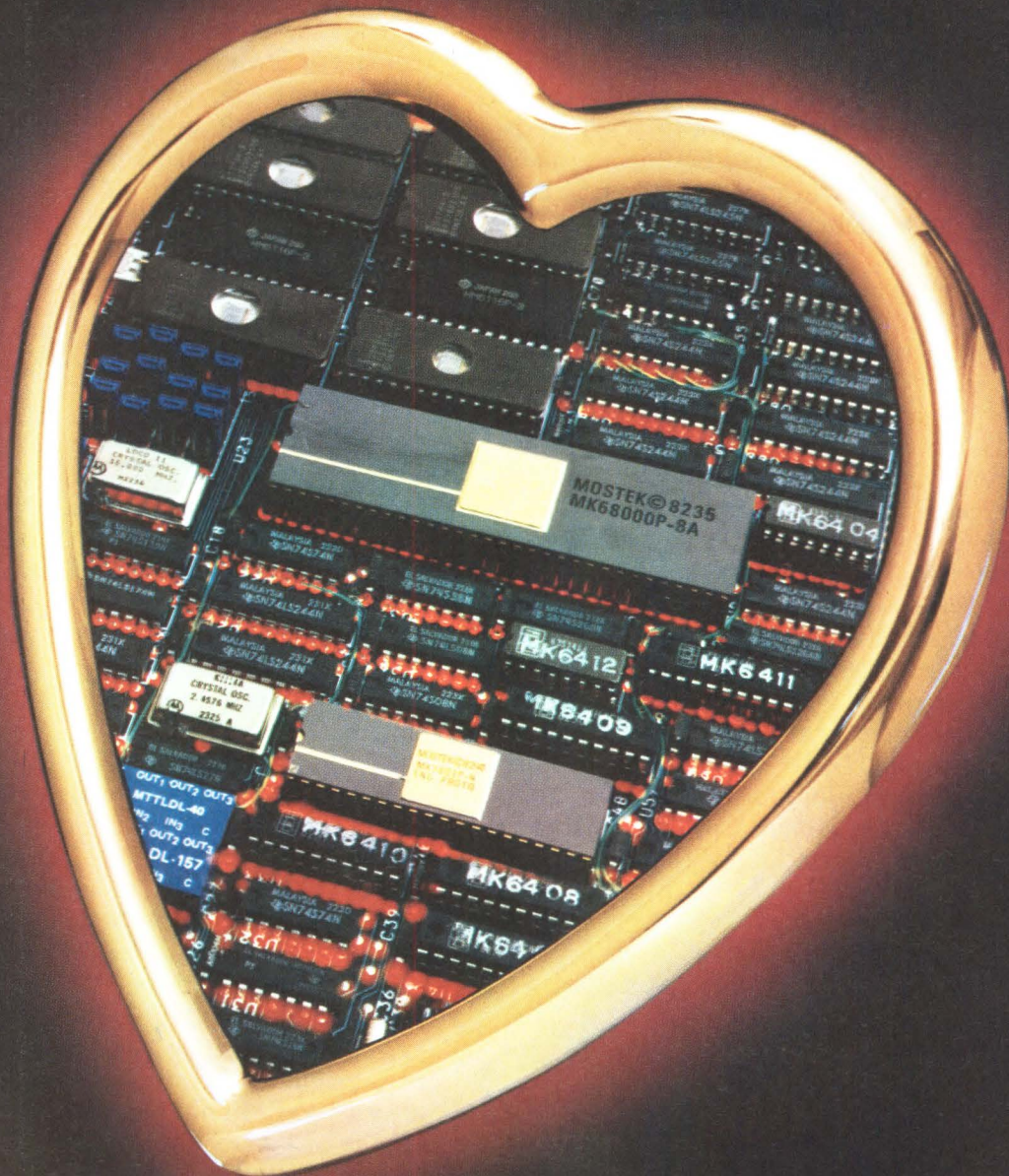
The second formatting mode is supported by the packet-based command structure. Its primary advantage is performance. The packet may specify spare sectors ontrack to avoid the extra seeks when encountering a bad sector. DataTower can reserve one sector per track as a spare. If a track has more than one defect, or the defect is more than one sector in length, the nearest neighbor spare sector is found and assigned as the alternate. If all tracks at that cylinder location have had their spare sectors assigned as alternates, then a one track seek is initiated to search for more alternates.

While reserving a single sector per track as a spare is not an efficient use of the media surface area, it provides better system performance than the traditional spare cylinder method. The area penalty for the ontrack spare sector method is about 1.6 percent. This is a small price to pay in view of the 70-ms (average) time savings from the elimination of the two seeks needed for the alternate cylinder method.

Defect mapping

Two types of media defects should be distinguished: defects identified at manufacturing test and defects discovered during use of the drive. Formatting with either the packet-based or the register-based command generates a complete defect map structure

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i pi Industrial Programming Inc.

CIRCLE 96

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on the formatted media. This feature, called dynamic defect reallocation, makes the drive appear defect-free to the CPU.

The DataTower establishes defect mapping during formatting by use of the prerecorded defect information placed on the drive at the factory. The factory defect information is recorded in terms of the number of bytes the defect is offset in absolute count from the index. A short record at the beginning of every track holds this information. The DS101 reads this information and maps it with the sector format chosen by the user. It will flag and assign alternate sectors for all defects automatically during formatting. This automatic process avoids the task of manually entering all known defects. Some applications ignore the factory defects and flag defective areas as they are discovered in system operation.

The DS101 creates a defect directory in the alternate cylinder area during the format operation. The defect directory is created on the first sector of the first flawless track of the alternate cylinder area. The defect directory map is a linked list of 128-byte records. Byte locations 1 and 2 of each record contain the address of the next record, bytes 1 and 2 have an address value of zero if there is no following record.

Even totally defect-free media do not stay that way forever. The DataTower will continue to monitor all read/write operations for media defects after the Format operation is complete. Sectors with hard failures found after formatting will be assigned alter-

nate locations, and the defect directory will be updated through dynamic defect reallocation.

When an alternate sector is assigned after formatting, a copy of the data at the old location is transferred to the alternate sector. Sometimes the original data has an error correction code syndrome that can detect an error, but cannot correct it. In this case, an absolute image is transferred to the new sector so that system-level error recovery procedures can start. A pointer exists in the defect directory that identifies the original sector location for diagnostic purposes.

DataTower continually monitors read/write operations for defects.

A bad sector can also be manually flagged after formatting. The register-based commands Specify Bad Sector or Specify Bad Track may be used. When these commands are issued, the bad sector or sectors are flagged, alternate sector(s) are located, and the defect directory is updated showing the alternate(s) location. To improve system performance when alternate sectors are encountered, the packet-based command should be used to format the disk. The packet command enables the user to specify ontrack sector sparing plus automatic defect mapping.

The error recovery operations of the DataTower stress data integrity. An ECC event is first handled by attempting up to four rereads of the sector in error. These rereads are done to obtain two identical ECC syndromes before correcting the data. Recognizing the limits of the 32-bit computer-generated code and the possibility that a disk drive's phase-locked oscillator may lock up out of phase, it might be possible to perform an ECC and transfer bad information without recognizing it as bad. Obtaining the two matching ECC syndromes reduces this remote possibility to almost nil.

Data on the move

Copy Data is a packet-based command used to transfer data between peripheral devices, typically between the streamer tape and the disk drive on DataTower. To begin the operation, the host first sends a Transfer Packet command, followed by Copy Data Packet. This packet contains the parameters used to control the Copy Data operation.

The Copy Data packet contains 16 bytes for each Copy Data step. The command may contain multiple steps for copies that gather or scatter data. A key aspect of this command is that it does not use the host processor, the host memory, or the host I/O bus once the command has been initiated. The host

HARD DISK FORMAT	
BYTE	7 6 5 4 3 2 1 0
0	02 HEX
1	CH NO. UNIT NO.
2	FBD /// MEDIA TYPE = 0
3	FILL BYTE
4	SECTOR
5	SIZE
6	DMD /// NO. SPARE SECTORS
7	NO. OF ALTERNATE CYLINDERS
8	CYLINDER INTERLEAVE FACTOR
9	HEAD INTERLEAVE FACTOR
10	SECTOR INTERLEAVE FACTOR
11	SECTOR INTERLEAVE TABLE LENGTH
12	SECTOR INTERLEAVE TABLE
N	(OPTIONAL)

The Format packet requires a minimum of 11 bytes of parameter information. More packet bytes are possible if the user elects to provide an optional sector interleave table.

may still access the disk drive during copy operations for normal read or write access. A second Copy command cannot be issued until the first Copy is complete.

The DataTower achieves an overlap of normal Read/Write commands and the Copy command using a three-port static RAM buffer in the DS101. Buffer size is 16 Kbytes, with approximately 10 Kbytes reserved by the Copy command to serve the streaming tape drive. The buffer is filled from the disk drive first, before the streamer tape is started, on a copy-to-tape operation. The Copy command can have multiple parameter packets that specify different disk locations for the data reads and writes.

The Copy command does not restrict access, so it is possible to alter data with a Write command in an area of the disk involved in the copy. File management is the responsibility of the user, however, as the DataTower recognizes addresses and data, not files.

The addresses of the source and destination devices are not restricted to some combination of disk or tape, nor must the addresses be different. A Copy command may be used to move data from one disk drive to another, or even to a different location on the same drive. This feature is useful in managing fragmented files, and in copying a single file with many extents. Tape-to-tape copies are possible, but not recommended, due to the poor performance of the buffer under this condition.

Both the Copy command and the packet-based Format command have an extensive table of status information in addition to the usual register file status information. The packet status can be read 36 bytes at a time on command. Detailed information about the transfer, including the number and status of records transferred from both source and destination devices, is available to the processor.

These features can make a significant contribution to overall system throughput when compared to the more traditional methods of software-intensive error recovery and backup procedures. The software changes required can be phased in gradually, since all the features can be defeated by setting option bits or parameter values as desired. Both physical and logical addressing are supported, and the automatic mapping of factory defects can be used with either scheme.

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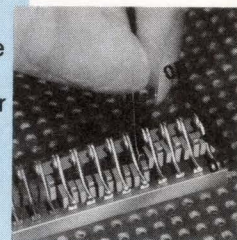
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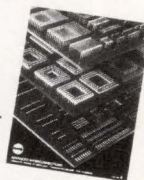
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COMPUTER DESIGN/April 1985

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CIRCLE 99

Software CAD system provides realtime assembler

The Case-I software CAD system supports interactive, realtime assembly programming. In addition to interactive programming, the Case-I system supports a relational data base for automatically generating documents associated with the program. The assembly language uses a structured set of mnemonics commonly supported by microprocessor instruction sets. Processors currently supported are the Z-80, 8085, 65402, and 8751.

This programming environment presents users with a screen format that divides into columns for address and data, label, instruction, modifier, and comments. The assembler handles all the code as it is entered. Incomplete code (eg, a jump instruction without a destination) is flagged and the user is prompted to supply code that is more complete. The system also marks discontinuous code segments. Documents generated by the Case-I

system include a specification, a listing, and a flowgram document. The specification provides definition details relevant to the code—such as name, programmer, and statistics about the program. The listing can be printed either as a normal assembly listing with addresses, opcodes, labels and comments, or as a 256-line memory page map to support the development and maintenance process. The flowgram is a computer-generated flowchart showing linear sequences, loops, and branches, with symbols that depict operations, decisions, and subroutines.

Assembly processes and documentation support are held together by the Case-I's relational data base. The base can maintain document data for a 32-Kbyte program in a data file of 512 Kbytes. The data base can also be used to create executable machine code for the microprocessors that it supports.

A Case-I system includes a 240 char/s printer, two 1-Mbyte 8-in. floppy disks, 0.5 Mbytes of RAM and a high speed DMA disk controller. It is based on a Z-80 single board computer with two RS-232-C ports. Case-I is priced at \$11,000. **Pro-Log Corp**, 2411 Garden Road, Monterey, CA 93940.

Circle 261

—T.R.W.



Instrument family runs under PC control

An estimated half million PCs appeared in engineering offices and labs in 1984 as a result of the groundswell of interest in the personal computer as an engineering tool. Recognizing this vast base, last year IBM began to market a third-party developed IEEE-488 (GPIB) controller board for the PC. Now, the concept of PC controllers for test equipment has gained the endorsement of Hewlett-Packard, originator of the GPIB.

With the introduction of the PC Instrument System, HP has chosen a unique tack. By eliminating individual

front-panel controls and displays—since the screen of the PC can be pressed into this role—HP has been able to introduce a line of basic test instruments, priced between \$500 and \$1500, that includes a 50-MHz dual-channel oscilloscope, a 4½-digit multimeter, and a full-feature function generator.

By means of a single controller board that mounts internally within the PC, up to eight PC Instruments run through a fast and direct control scheme in which they are “closely-coupled” to the PC bus. (The PC In-

struments do not run under GPIB control.) Since only the controller board for the HP system is internally mounted, the instruments themselves are individually packaged in separate modules that can be stacked. This frees the internal expansion slots within the PC for other jobs.

Designed to run under the control of the HP 150 or IBM PC/XT/AT and compatible computers, the PC Instruments are programmed in simple MS-DOS Basic statements. Soft-key functions may be added for the operator inputs and, in the case of the

HP 150, touch-screen functions can be integrated into the program. Instrument readings can be "windowed" onto the PC screen and their results can be data-logged at required intervals. In addition, data results are stored in files that are compatible with Lotus 1-2-3, which can be invoked from the test program to analyze data or to calculate and display graphs or plots.

GPIB instruments may be added to the PC Instrument system by using two available software packages. These HP-IB I/O Libraries are available for the Touchscreen PC or for IBM and compatible PCs. Again, programming is accomplished in MS-DOS Basic.

Currently available PC Instruments include the 61016A digitizing oscilloscope, with 50-MHz bandwidth, dual channels, and delayed trigger; the 61014A function generator providing sine, square, triangle, ramp, and pulse outputs at 0.5 Hz to 5 MHz, with burst mode; a universal counter



that provides frequency, period, time interval, unit counter, and frequency measurements at 5 readings per second; a 61010A digital I/O unit, which provides 16 digital inputs and 16 outputs plus two-wire handshake; and the 61001A power pack for support of up to eight instruments. Price is \$400 each for the interface boards that

handle the PC/XT/AT, HP 150, and GPIB linkage. Application software (for data logging, graphing, and other control function routines) costs \$400. **Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 262

—B.F.

Development system enables speedy migration to C

A language development system seeks to unbatch resources and eliminate compilation bottlenecks encountered by designers working with C. Known as Smart-C, this interactive software system is composed of three parts: a syntax-directed editor, a symbolic interpreter, and a parser.

The system closely couples editor and interpreter functions during program development. The C code can be interpreted as it is created so program logic can be checked before the compilation stage. Smart-C, which is produced by AGS Computers Inc, uses windows to display source code and values for variables and expressions. This further eases program debugging. Values and breakpoints can be displayed in one window while a section of the source code is interpreted in another window.

Gavin Villapiano, director of the AGS Advanced Products Group, highlights the editor when discussing

this system. "This is a syntax-directed editor," he says, "It automatically checks syntax. The system interpreter then allows you to quickly mock-up a program and ferret out runtime bugs." Villapiano notes that the compilation stage is historically a bottleneck for programmers working under deadline pressure. With the union of editing and symbolic interpretation in this system, he says, compilation time is dramatically cut.

The editor produces source code that is free from syntactical error. Because it automatically checks syntax, it encourages structured programming. The Smart-C editor works from a C language syntax data base and can intelligently manipulate string and character sets. Programmers are able to outline a program by displaying language skeletons that can be moved, transformed, or deleted, as development progresses. The symbolic interpreter, invoked by the editor at

any stage of program development, saves system resources. Syntax and logic testing is not needed after compilation. The interpreter presents a visual representation of the program, displaying values of variables and expressions.

Developed to handle problems of maintenance programming, the parser module formats existing C programs for use by the editor and interpreter. The parser serves to standardize C naming conventions.

As a whole, the aim of the Smart-C package is to go beyond syntactical correctness and streamline the overall Unix development process. Smart-C runs on micro, mini, and supermini-computers that support a C compiler and a Unix-like operating system. **AGS Computers, Inc.**, 1139 Spruce Dr, Mountainside, NJ 07092.

Circle 263

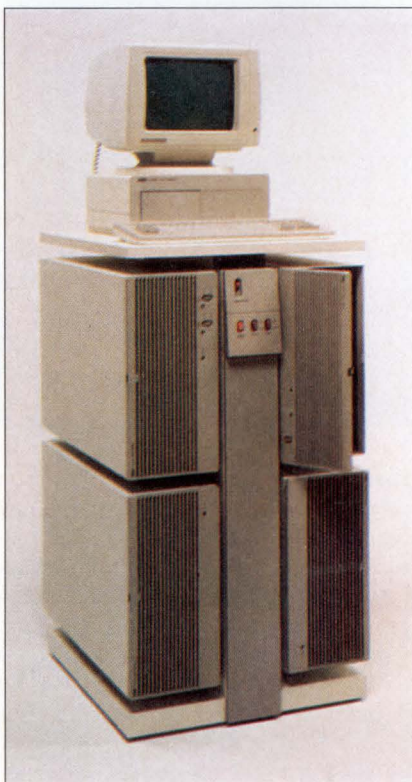
—J.V.

Compact communication processor built around a 32-bit chip

In its first implementation of the NCR32 microprocessor, NCR Comten has produced a powerful communication processor that can operate in a standard office environment. By using the 32-bit NCR chip, as well as proprietary semicustom and custom chips, Comten can package the processor in a 33- x 62- x 23-in. (83.8- x 157.5- x 58.4-cm) footprint, while providing application switching, routing, polling, automated dialing, error recovery, and multiplexing for up to 32 data lines.

Modular design allows 5620 users to choose the configuration that meets current processing power requirements, as well as allowing for easy future expansion. The modular components include a CPU, a channel interface unit for host connection, a communication subsystem supporting up to two communication base cabinets (each capable of handling up to 16 communication lines), a fixed disk drive to facilitate rapid load-and-restart, plus an optional system console for network control.

When used as a nodal processor in a pure SNA network environment, the 5620 links via standard SNA trunk protocols. For mixed SNA and



non-SNA environments, the 5620 attaches to the network through Comten's Communications Network System procedures.

Any combination of IBM or NCR hosts is supported by the channel interface unit. The system handles asynchronous, bisynchronous, and SDLC protocols. Individual line speeds up to 64 kbits/s are supported with automatic baud rate detect (ABRD) capability up to 19.2 kbits/s. ABRD determines the speed and code set of asynchronous terminals at the connection.

Main storage in the CPU ranges from 1 to 4 Mbytes. A channel interface adapter, which allows IBM compatibility, also has an NCR32 chip that is microprogrammed for the channel adapter function. The NCR channel interface adapter is 68000-based while the communication subsystem includes two character processor types: one for multiplexing from one to eight lines for 50 bits/s through 19.2 kbits/s and a higher speed processor for line 1 that runs from 19.2 to 64 kbits/s. Available in the last quarter of 1985, the 5620 will sell for \$22,000. **NCR Comten, Inc.**, 2700 Snelling Ave N, St Paul, MN 55113.

Circle 264

—N.M.

Communication boards adhere to OpenNET strategy

Two communication boards—the iSBC 552 COMMengine and the iSXM transport engine—connect microcomputer systems to Ethernet LANs. These boards plug directly into Multibus-based microcomputer and peripheral systems. Both products feature onboard memory and are based on the 80186 processor, the 82586 LAN coprocessor, and the 82501 Ethernet serial interface chip.

The iSXM 552 is a turnkey transport engine that includes a built-in diagnostics program and a version of Intel's iNA 960. The iNA 960 can be downloaded into the onboard memory while the iSBC 552 is an unbundled version of the iSXM board. Instead of providing transport layer

software, the iSBC allows users to load their own versions of network programs into the board's RAM. This allows flexibility in specialized applications. The OpenNET family of products consists of hardware and software covering the seven layers of the OSI model. Used in conjunction with the iSBC 186/51 COMMputer board, the COMMengine and the transport engine boards provide networking to any Multibus-based system, regardless of the operating system under which it runs.

In conjunction with the two boards, Intel Corp has also introduced two software packages—RMX Networking and Xenix Networking. These allow concurrent file-sharing

by systems using the iRMX operating system or Intel's version of Microsoft's Xenix operating system. This ability to provide transparent remote file access between the same or different operating systems allows applications to gain access to files anywhere in the network as if the files were stored locally. This in turn allows multi-user application software to run in a network environment without modification.

The 552 boards can be used with any operating system because they only require a high level interface to communicate with the host. But, while the iSBC 552 offers the hardware necessary for users to construct an Ethernet frontend processor for a

unique environment, the iSXM 552 provides full ISO transport services that run without additional configuration changes.

Intel derived the iSXM version of the iSBC 552 by populating the latter with 16 Kbytes of ROMs and 80 Kbytes of RAMs as well as supplying the iNA 961 software. The iSXM 552 is configured for Intel's 86/286-310

systems. The networking software products implement the file-access protocols used by Microsoft's Microsoft Networks and IBM's PC Network Program. These protocols were developed jointly by Intel, Microsoft, and IBM. RMX, Xenix, and DOS systems on the same network are compatible and can gain access to each other's files. Intel is making the

protocols available to the public and expects that other implementations will follow. The iSBC 552 COMM-engine costs \$1500, and the iSXM transport engine costs \$1800. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 265

—N.M.

State-of-the-art pattern generators enhance logic analysis system

Advanced pattern generators in the 91S16/91S32 series combine with the 9100 digital analysis system to produce a powerful test instrument. These pattern-generation modules reach operating speeds of up to 50 MHz, extending the performance of the 9100 logic analyzer in the realms of digital debugging and verification.

Teaming pattern generation with logic analysis enables functional testing of chips, boards, and systems. And test programs created during the system development cycle can adapt for use in manufacturing. The pattern generation modules can work as standalone stimulation sources, or link with DAS 9100 logic modules to form an integrated test system. The modules run at a 50-MHz rate, or 20-ns cycle time, bringing timing margin testing to logic analysis with accurate 1-ns edge placement of individual data and strobe channels.

Featuring 16 data channels of pattern generation along with two strobes and two clocks, the 91S16 modules output vectors upon execution of a user-written pattern generation program. This program can reach a length of 1024 instructions. Instruction types include if, jump, return, output, register, and enable/disable interrupts. External control inputs ease interaction between the unit under test, the pattern generator, and the DAS 9100 logic analysis modules.

The 91S32 outputs previously stored patterns in sequential order. It supports 32 data channels, four strobes, and four clocks. With the 91S32, up to 2048 bits per channel can be entered by the user or down-

loaded from a simulator or host computer. Six 91S32 modules can operate simultaneously, or five 91S32 modules can run under the control of a 91S16. This allows use of several, flexible pattern generation modes (eg, reloading memory on-the-fly). The 91S32 memory can divide into two pages each sized at 1 Kbit. One page can load while the other is executing.

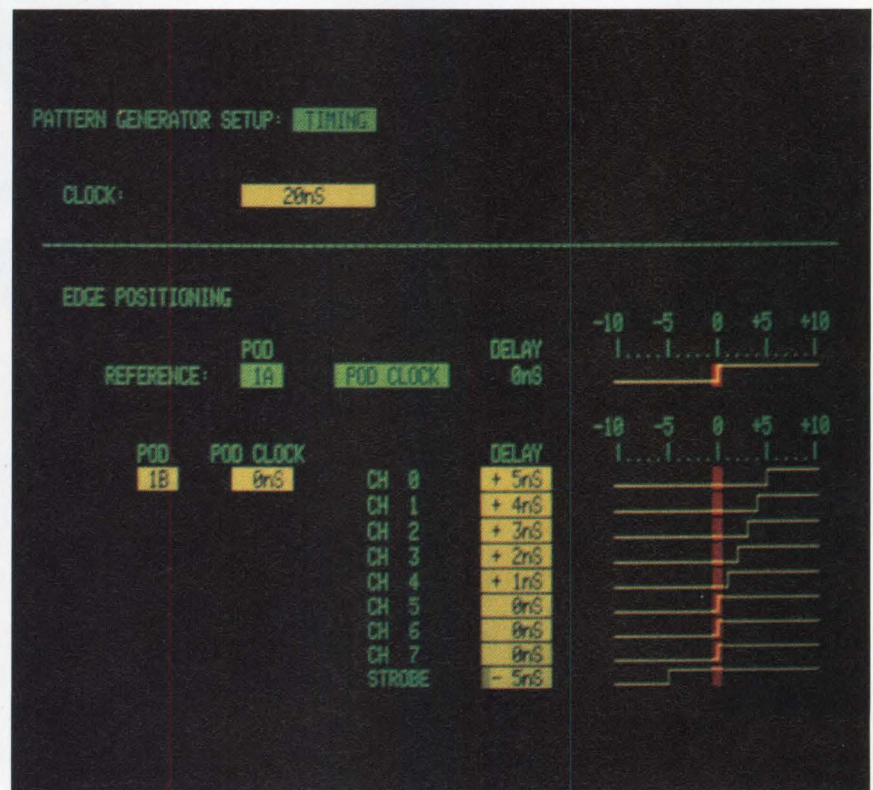
Data acquisition probes included with the pattern-generation modules have hybrid circuits within the probe tips that deliver accurate 50-MHz signal performance at the device pins.

A single probe can handle both TTL and ECL devices. Slew rate for TTL is 500 mV/ns while the slew rate for ECL is 150 mV/ns.

Users can save pattern programs on the DAS 9100's optional DC-100 tape drive. Tie-in options include RS-232 and GPIB porting. The 91S16 and 92S32 are priced at \$6900 and \$10,400, respectively. **Tektronix, Inc.**, PO Box 1700, Beaverton, OR 97075.

Circle 266

—J.V.



DIGI-DATA SERIES 2000

THE FAST STREAMER



At 125 ips, Digi-Data's Fast Streamer is 25% faster than others. Data is transferred at 200 Kbytes per second instead of the usual 160 Kbytes per second. That cuts down your back-up time per 2400' reel (including rewind) to about 6-1/2 minutes at 1600 BPI (46 Mbytes unformatted) or 10 minutes at 3200 BPI (yielding 92 Mbytes unformatted). And with 3600' tapes, unformatted capacity increases to 138 Mbytes (3200 BPI) and 69 Mbytes (1600 BPI).

Actual capacity of course varies, since long records utilize the tape more efficiently than short records.

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CIRCLE 100

Imaging board set adapts to Multibus configurations



The RTI-500M board set for the Multibus allows users to digitize and store video images in real time. Two boards comprise the set—the AS-501M and DS-501M. These join to an optional pipeline image processor. Fully compatible with Multibus and supporting a 24-bit addressing scheme, the board sets can support either 50 or 60 Hz operation. The DS-501M appears on Multibus as system memory with programmable windows into the image data. This board includes a “9th-bit plane” that enables graphics and cursor operation without affecting the 8-bit data image. The AS-501M will multiplex among four video sources under software control. **Recognition Technology, Inc.**, 335 Fiske St, Alco Park, Holliston, MA 01746. **Circle 267**

STD bus card is designed for low power applications

An STD bus system using the MSI-C888 card can directly access up to 128 Kbytes of memory, plus 512 inputs and 512 outputs. Incorporating an 80C88 CMOS microprocessor, the card's onboard memory includes 2 Kbytes of RAM with allowance for expansion to 4 Kbytes. Both maskable and nonmaskable interrupts are provided. The MSI-C888 can also be disabled for DMA to offboard memory and multiprocessor operations. Card typically requires 5-V at 60 mA at a 5-MHz clock rate. Unit price is \$350. **Microcomputer Systems, Inc.**, 1814 Ryder Dr, Baton Rouge, LA 70808. **Circle 268**

Computational throughput vaults using coprocessor subsystem

When used with Cromenco software languages, the Maximizer 12-MIPS coprocessor increases throughput of the company's computer systems. A 2900-series ECL bit-slice processor, running at a 48-MHz

master clock rate, lies at the heart of the subsystem. Maximizers have 16 Kbytes of high speed data memory (50-ns cycle time), 16 dual-port registers, and 4096 48-bit words of downloadable microcode instructions. A 60-ns multiplier chip, pipelined instruction path, and state-machine controlled DMA transfers are also featured. Microcode assembler software is also available. The Maximizer costs \$3495. **Cromenco, Inc.**, 280 Bernardo Ave, PO Box 7400, Mountain View, CA 94039. **Circle 269**

LAN connections derive from 32000-based gateway

The Advanced Systems Gateway combines host communication ability with modem sharing. It can connect different local area networks. The AS/Gateway is built around the 32000 microprocessor. The gateway is made up of two boards with the main board or bus master driven by a 32016 with 512 Kbytes of memory. It allows LAN-connected personal computer users to connect with other LANs. With an optional modem server, the gateway will allow personal computers on a LAN to share eight modems. The AS/Gateway will also handle both SNA connections and asynchronous services. Price is \$6000 plus \$125 per personal computer node. **National Advanced Systems**, 800 E Middlefield Rd, Mountain View, CA 94040. **Circle 270**

Adapter board expands options for PCs and compatible machines

Octacom is a flexible adapter board with multiple serial communication ports. It expands the operation of the PC, XT, AT, and PC compatibles. Octacom adds four to eight serial ports and can be installed in any full-length slot on the PC. This module contains separate 8250 UARTs that perform serial to parallel/parallel to serial conversion, data checking, parity generation, and baud rate generation. A PLA is used for addressing each UART on the Octacom module. The interrupt for each of the eight channels on Octacom can be programmed to send an interrupt to the CPU on any free interrupt level. A remote panel and shielded conductor ribbon cable setup is also available. A four-channel module costs \$295 and the eight-channel version is \$785. Octadrive software costs \$25. **Star Get Technologies**, PO Box 764, Cleveland, OH 44026. **Circle 271**

Dual-ported RAM module supports two bus structures

A memory module accessible from both the extended VMEbus and the VMXbus sports dual-ported RAM. Dubbed the DSSEDPRX, the unit is supplied with 128 Kbytes of CMOS static RAM. It can also be supplied with the DSSEDPRX-P daughterboard for capacity extended to 256 Kbytes. Jumper selectable VMEbus memory access times range from 150 to 300 ns, while VMXbus access times span the 180- to 330-ns realm. High speed logic delivers 35-ns memory access arbitration time between the VMEbus and the VMXbus. The basic DSSEDPRX costs \$1295. **Data-Sud Systems/U.S., Inc.**, 2219 S 48th St, Tempe, AZ 85282. **Circle 272**

Concurrent DOS implementation marks video display board

A PC-compatible display board centers around Motorola's 6845 and runs a form of Concurrent DOS. Known as the PC Video Board, it also works with GSX software. The board comes standard with 16 Kbytes of static RAM in CMOS, 24-bit memory addressing, and 16-bit addressing for I/O ports. It is aimed at creating color graphics in the IEEE 696/S-100 bus environment. In the color display mode, the graphic screen offers a choice of 160 x 200 pixels in 16 colors, 320 x 200 in four colors, or 640 x 200 in one color and black. Price is \$495. **CompuPro**, 3506 Breakwater Ct, Hayward, CA 94545. **Circle 273**

Multiprocessing engine off-loads VMEbus operations

CPU boards in the IV-1601 line are VME/VMXbus units that allow off-loading of all activity from the VMEbus, except for interprocessor communications and shared resource utilization. The VMXbus and large local RAM handle all other activity. The IV-1601 features a 68010 CPU running at 12.5 MHz, 512 Kbyte, or 1-Mbyte dual-ported SRAM, and an interrupter and interrupt handler. Options include a floating point processor and memory management. With the VMXbus functioning as an extension of the CPU board's local bus, up to six additional dual Eurocards can be interconnected by a flexible backplane that plugs onto the VMEbus P2 connector. Quantity 1 to 4 pricing is \$2750 for the 512-Kbyte model. **Ironics Inc.**, 742 Cascadilla St, Ithaca, NY 14850. **Circle 274**

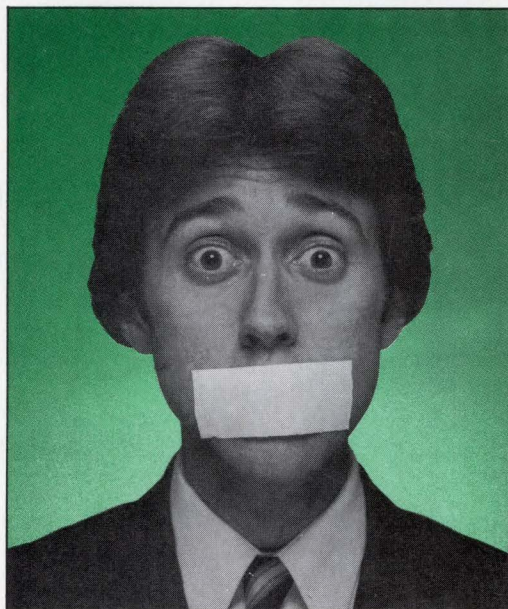
Zero-current tap switching marks power conditioner line

Central to the operation of a power conditioner line is zero-current tap switching technology. This approach increases system reliability by eliminating stress on the switching elements and by reducing the number of system components. Also fea-

tured in this three-phase Line 2 power conditioner series is Powerlogic control for fast performance. An internal micro-computer monitors the output voltage, determines necessary corrections, and initiates the response. Voltage flux is corrected in less than a cycle. These power conditioners provide common-mode

noise attenuation at a ratio of 10 million to 1 (140 dB) and normal-mode noise attenuation at a ratio of 1000 to 1 (60 dB). Units are available in 50 and 60 Hz models, with power ratings from 10 to 30 kVA. **Topaz, Inc.**, 3855 Ruffin Rd, San Diego, CA 92123. **Circle 275**

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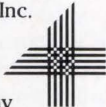
68000; and the RCA 1802 and 1805. Availability also includes OS-resident systems like MS-DOS, RSX/VMs, CP/M-80, and CP/M-86.

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Standby power system features line synchronization

The SPS-1000 provides a sine wave output with less than 5 percent total harmonic distortion, and is line synchronized to track the power line. This standby power system features a unique detection unit coupled with a solid state transfer switch for fast switching power protection. Features include built-in surge suppressor, overcurrent protection, voltage regulation, and emi/rfi filters. Capacity reaches 1000 VA. Units with frequencies of 50 Hz and high voltages of 220 and 240 V are available. **SAFT America, Inc.**, 107 Beaver Ct, Cockeysville, MD 21030. **Circle 276**

High density memory packaging expands RAM capabilities

A single inline memory module (SIMM) socket performs the connector functions for a high density memory packaging system while providing a means for expanding RAM capabilities. A SIMM socket accommodates two customer-supplied SIP modules, each containing nine surface-mounted memory chips. Total dynamic RAM capacity reaches 1152 Kbits. Zero insertion force contacts improve socket and module contact life, allow up to 25 mating cycles, and provide fast online assembly. Rated voltage is 250 V. **Molex Corp.**, 5224 Katrine Ave, Downers Grove, IL 60515. **Circle 277**

Coordinated protection highlights power distribution units

Power distribution units have add-on fuse protection, which provides proper branch circuit coordination. This Cyberex line has provisions for an electrostatically shielded isolation/stepdown transformer and transient suppression. An emergency power-off feature is noted. Standard ratings available are 30, 50, 75, 100 and 150 kVA with 120/208 V output from 480 or 208 V building services. **Cyberex Inc.**, 7171 Industrial Park Blvd, Mentor, OH 44060. **Circle 278**



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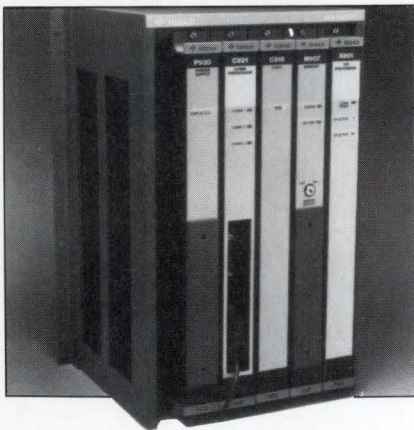
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High speed marks mid-sized controller unit



A high speed, full-function, programmable controller—the 984—sports increased logic-solving capacity in a mid-sized controller. The 984 features 16,000-word memory for logic and ASCII characters, 16-Kbyte CMOS RAM with battery backup and bipolar PROM, three integral Modbus ports, and a remote data access panel. It is software compatible with the 584 controller family. The CPU

module uses a 4-bit slice microprocessor configured in a 16-bit architecture. The CPU features a logic solver that works at 200 ns per instruction. Up to 2048 points can be configured with the controller. **Gould Inc, Programmable Control Div**, PO Box 3083, Andover, MA 01810.

Circle 279

Realtime industrial systems are built via microcomputer engine

Using four custom CMOS gate arrays to integrate key system functions, SBM-88 PC Engines combine PC compatibility with single-board system architecture. On the motherboard, these products directly integrate monochrome video and floppy disk controllers, an 8088 CPU, memory, serial ports, and I/O expansion bus and connectors. BIOS ROM supports MS-DOS, CP/M 86, Concurrent CP/M, and the PC/iRMX realtime operating system. Combining the SBM-88 with the iRMX 86 operating system and the 8087 math coprocessor (plus data acquisition peripheral boards) produces a system capable of many plant floor applications. A standard chassis, power supplies, and

enclosures are available for standalone or rackmounted configurations. The SBM-88 supports up to 256 Kbytes of RAM (expandable to 640 Kbytes). Standard interfaces include a floppy disk controller supporting up to four 5¼-in. drives, TTL-compatible video outputs, keyboard, and Centronics printer port, plus two RS-232 serial channels. In designer quantities, the units cost less than \$500. **Mostron Inc**, 560 Valley Way, Milpitas, CA 95035.

Circle 280

System translates images for control applications

The BLOB-1 measures and identifies binary image patterns and outputs, using parameters such as area, boundary, and centroid points. It converts visual images obtained via industrial computers and transmits them via an RS-232-C interface to a host. This system uses an algorithm based on Stanford University's Pattern Recognition Algorithm. **Intertek, Inc**, Naito Bldg, 728 Nishishinjuku, Shinjuku-ku, Tokyo, Japan 160.

Circle 281

SYSTEM ELEMENTS

Remote optical repeater compatible with IEEE 802.3 transceiver

A remote optical repeater, the CER-802 transmits 1000 m or more without speed degradation. Fiber optic benefits such as transmission security and resistance to electromagnetic interference are touted. The unit cuts transmission errors, and is compatible with IEEE 802.3 transceivers and Ethernet specifications. **Canoga Data Systems**, 21218 Vanowen St, Canoga Park, CA 91303.

Circle 282

Speech recognition keyboard uses vocabulary reaching 160 words

Plug-compatible with the IBM PC and XT, the KB 5152V speech recognition keyboard expands input options. Up to 160 words or phrases per vocabulary are available in this speaker-dependent peripheral. No software modifications are needed because commands are sent to the host just like key input. Input power measures 5 Vdc at 1 A typical. Nine

vocabulary subdivisions are available and discrete words/phrases can last for up to 1.25 s. **Key Tronic**, PO Box 14687, Spokane, WA 99214.

Circle 283

Analog delay devices need only a single TTL-level clock

With N-channel silicon gate technology in bucket-brigade configurations, general-purpose sampled analog devices are 8-pin miniDIP chips capable of delay times ranging from less than 300 μ s to over 4 s. The RD5106A (256 samples—capable of sub-300 μ s delay time) and the RD5108A (1024 samples—capable of 4-s plus delay time) have an onchip driver, as well as a clock controlled delay that requires only a single TTL-level clock. The devices will perform with less than one percent distortion and dynamic range of greater than 70 dB. Applications include voice and data scrambling, instrumentation, and sound effects. The 100-piece price of the RD5106A is \$5.25, with the

RD5108A being \$11. **EG&G Reticon**, 345 Potero Ave, Sunnyvale, CA 94086.

Circle 284

Monolithic CMOS dc-dc device is a flexible inverter/converter

Using monolithic CMOS technology, the Si7660 is a dc-dc converter/inverter. This low voltage device is intended for use as a voltage inverter but it can be enhanced with simple add-ons to provide voltage doubling, supply splitting, and simultaneous inversion and doubling. With the addition of two capacitors and a small signal diode, the Si7660 performs supply voltage conversion for an input range of 1.5 to 10 V, resulting in a complementary output of -1.5 to -10 V. The unit is available in two packages: the TO-99 "can" and an 8-pin plastic DIP. For 100-piece quantities, the cost of the TO-99 model is \$2.73 each and the DIP version is \$1.89 each. **Siliconix Inc**, 2201 Laurelwood Rd, Santa Clara, CA 95054.

Circle 285

Subdirectory scouting improves performance of MS-DOS machines

EasyPath Release 1.0 permits programs and commands to find files in subdirectories other than those being run. The hierarchical subdirectory structure of DOS can be employed without having to copy files back and forth. The product comes with specifications predefined for such major programs as Framework, Symphony, 1-2-3, dBase II, and WordStar. EasyPath can also locate files on any drive, including RAM disks. PC-DOS, or MS-DOS 2.00, or higher is needed. **Polygon Software Corp.**, 363 7th Ave, New York, NY 10001.

Circle 286

Knowledge engineering language drives AI system

The Insight system uses a knowledge engineering language called PRL, for Production Rule Language. This language is used to represent the If-Then-Else rules and the goal outlining that is used to define

knowledge. The system can employ both forward and backward chaining mechanisms for its reasoning processes. The Insight system runs on the IBM PC and compatibles and on the Rainbow. It requires a minimum of 128 Kbytes of RAM and one disk drive. Program cost is \$95. **Level 5 Research, Inc.**, 4980 S A1A Melbourne Beach, FL 32951.

Circle 287

Windowing interface eases application learning

A software product provides task windows for existing application packages. VisuALL Plus—which includes windows for Lotus 1-2-3, WordStar, and DOS—automatically converts computer codes and special rules of standard software packages and operating systems into easy-to-understand tasks that are displayed in window overlays. No program modification is needed. **Trillian Computer Corp.**, 405 Alberto Way, Los Gatos, CA 95030.

Circle 288

Software broadens horizons of interactive image processing

ImageAction enables users of PC, XT, and AT systems to perform image processing applications without programming experience. Used in concert with the PCVision Frame Grabber—a device that converts analog video signals to digital data—the software is mouse and menu driven and works on an “area of interest” principle. ImageAction can operate on whole images or subsections. Also available now, an enhanced Frame Grabber offers 8-bit digitization and pseudocolor capabilities. Besides the Frame Grabber, a typical hardware configuration for use with ImageAction includes a PC, XT or AT with 512 Kbytes of memory; disk drive; display screen; 8087 coprocessor; three-button optical mouse; a video camera (RS-170); and a 512- x 480-pixel resolution monitor. Single-use license for ImageAction software is \$995; the enhanced PCVision Frame Grabber starts at \$2995. **Image Technology, Inc.**, 600 W Cummings Pk, Woburn, MA 01801.

Circle 289

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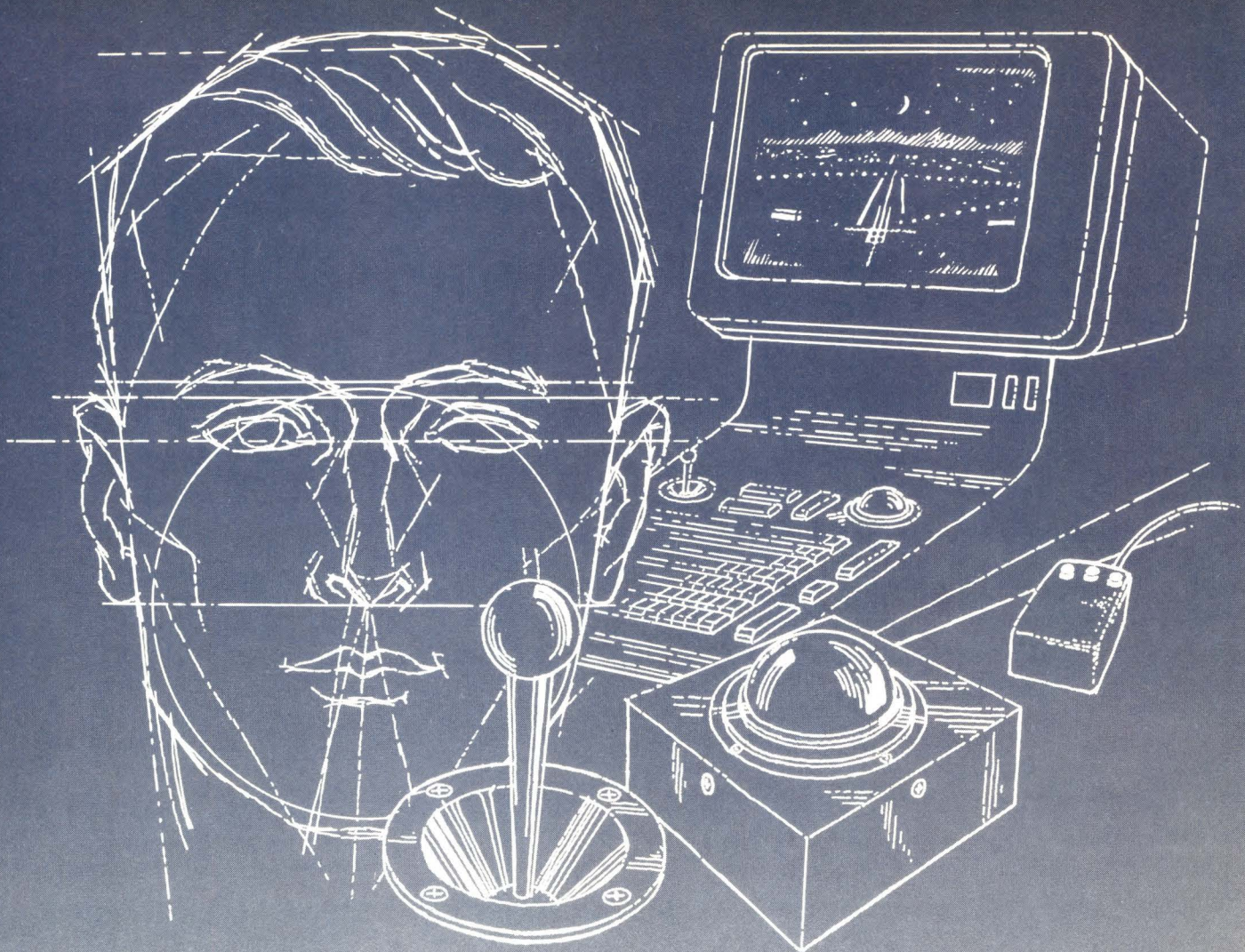
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Setup embellishes microcomputer graphics system quality

The Business Graphics System generates low cost, high quality slides, transparencies, and hard copy. The basic system consists of the Color Digital Imager IV film recorder and the Graphics Express software package. Interfacing with the PC or PC-compatible microcomputers, the Imager IV can produce high resolution 35mm slides and prints. It can simultaneously display up to 16 colors from a palette of 4000. Graphics Express is a software program that drives the film recorder and supports other output devices at full resolution. Options include a high resolution monitor and graphics tablet. A system sells for under \$11,000. **Bell & Howell**, 7100 McCormick Rd, Chicago, IL 60645.

Circle 290

Sonic digitizer handles 3-D objects for modeling analysis

The model GP-8-3D-P sonic digitizer allows users to input three-dimensional coordinate data using sonic technology. Objects (including ferrous substances) can be digitized. The GP-8-3D-P uses

sound to determine the distance between a digitized point and four microphone sensors that are mounted on a plane. The host computer then converts these distances into Cartesian X, Y, and Z coordinates. Point/trace mode and output format are host selectable. Formats include ASCII, binary RS-232-C, or parallel-packed binary. The unit costs \$7500. **Science Accessories Corp**, 970 Kings Highway W, Southport, CT 06490.

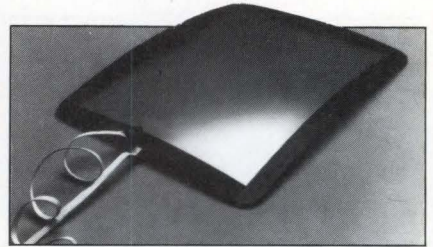
Circle 291

Plasma panels challenge the dominance of the CRT

Full-page dc-plasma display panels can show up to 2000 char (7 x 13 dot matrix) in an active area taking up 8.3 x 5.2 in. (21.1 x 13.2 cm). The panel's depth measures only 0.8 in. (2.0 cm) including driver modules. Minimal changes in the logic design are required for conversion from CRTs. Supply voltages required are 5 and 200 Vdc, 5-V floating. A smaller message board panel is also available. **Panasonic Industrial Co, Computer Components Div**, 1 Panasonic Way, Secaucus, NJ 07094.

Circle 292

Resistive membrane touch screens lower cost by dropping diodes



The recently developed E274 touch screen takes resistive membrane technology a step further. Evolving from its predecessor, the E270 touch screen, the E274 eliminates the need for diodes common to the membrane technique, by replacing diodes with a combination of a voltage dividing resistor network and special contact geometry to the screen's glass coating. Also notable are the screen's lower profile border, higher current draw (the E274 draws up to 140 mA for a drive voltage of 5 V), and use of a five-pin connector. **Elographics, Inc**, 105 Randolph Rd, Oak Ridge, TN 37830.

Circle 293

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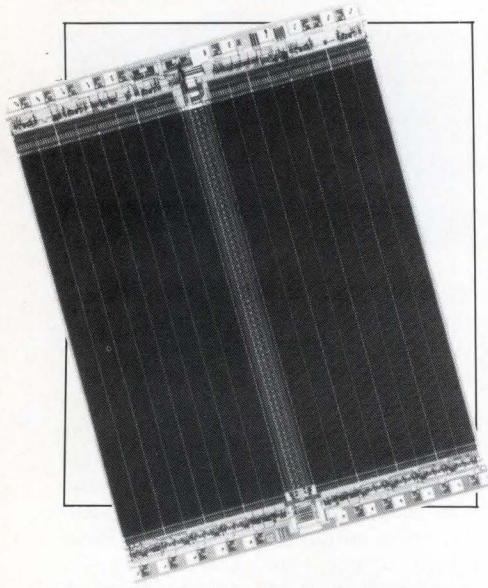
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Ultralow access times mark powerful CMOS SRAM devices



A CMOS 64-Kbit x 1 static RAM features access times as low as 45 ns and maximum active power consumption of 70 mA. Dubbed the F1600, this is a fully static asynchronous RAM that uses sub-2 μm

CMOS/NMOS technology. The device has three available speed versions: 45, 55, or 70 ns. All three versions sport low active power consumption levels of 40 mA (typical) and 70 mA (maximum). Standby power consumption (TTL levels) for the device is 5 mA (typical) and 20 mA maximum; full standby is 0.02 mA (typical) and 9 mA (maximum). The F1600 comes housed in a 22-pin dual inline side brazed ceramic package or leadless chip carrier. The commercial 70-ns version in a DIP package costs \$65 for 1000-piece quantities. **Fairchild Camera & Instrument Corp, Memory & High Speed Logic Div, PO Box 5000, Puyallup, WA 98373. Circle 294**

Semicustom chips designed to form linear mosaics

The FP300 series of linear mosaic arrays aims at simpler semicustom linear and combined linear/digital LSI. Using a macro cell concept, the chip boasts dramatic reduction in number of packages versus standard chip designs. The FB300 series of linear mosaic arrays is supported by the Linear CAD 1 package, which per-

forms schematic capture and Spice circuit simulation on the IBM PC. Pricing varies according to the complexity of the LSI design. **Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Circle 295**

Modem filter meets V.26/Bell 201, 2.4-kbit/s specs

A monolithic, switched-capacitor combo IC handles 2.4-kbits/s modem filter applications. Dubbed the RM5636A, this chip integrates four switched capacitor filters: a receiver bandpass filter that meets CCITT V.26/Bell 201 (2.4-kbit/s) modem specifications, a fixed compromise delay equalizer with a nominally flat amplitude response, and a 75/150-bit/s secondary channel filter (CCITT V.23/Bell 202). Also, a 3-kHz transmit low pass filter is used between the D-A and telephone lines. A model RM5637A is intended for use in 4.8-kbit/s modems. Filter features include 5- to 10-V power range, TTL/CMOS compatible inputs, and 22-pin package. **EG&G Reticon, 345 Potero Ave, Sunnyvale, CA 94086. Circle 296**

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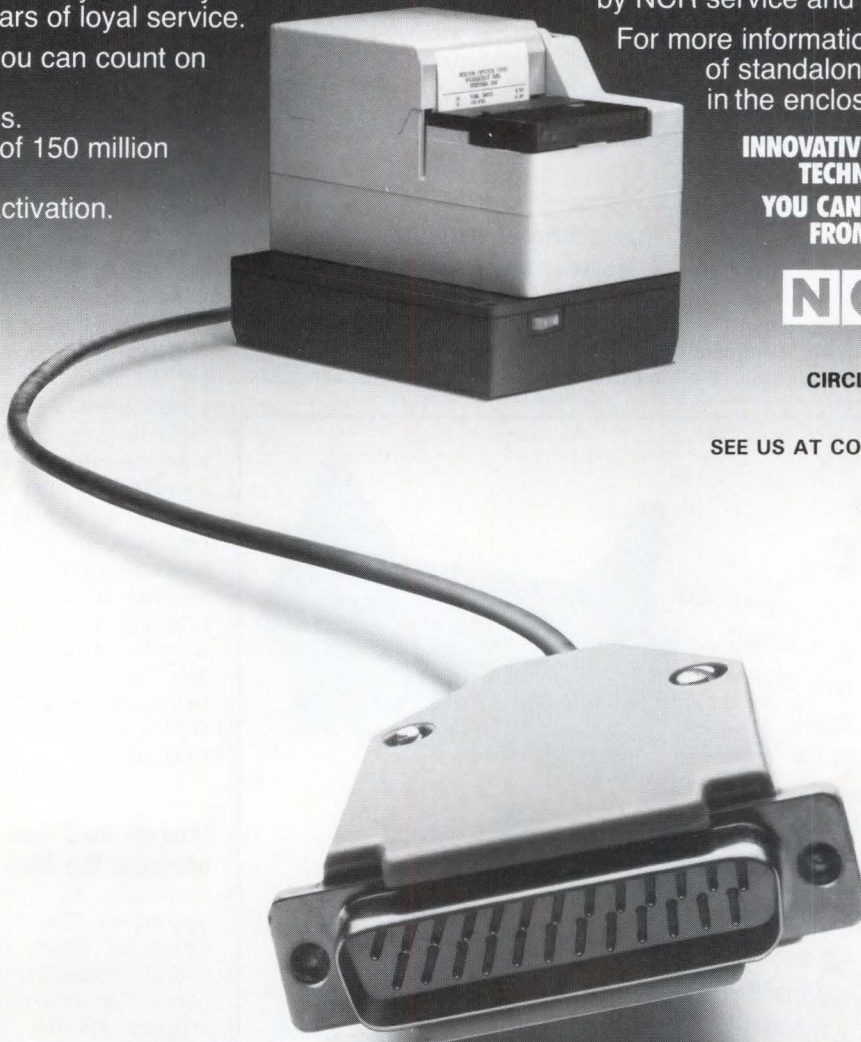
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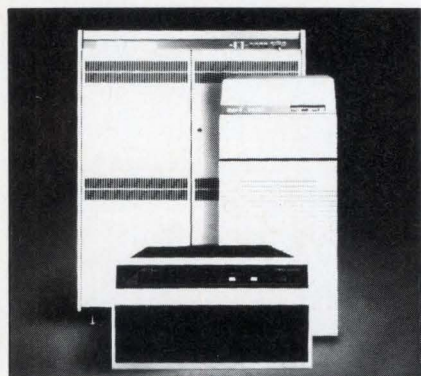
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Subsystem garners fast disk operation for the VAX



VAX series minicomputers gain fast disk operation via the DSS-1412 disk subsystem. This mass storage unit features a 1.2-Gbyte, 10-Mbyte/s disk drive interfaced to the Unibus using the DPS-2400 intelligent I/O subsystem. Unibus bandwidth limitations are circumvented with the DSS-1412. A 12-Mbyte/s interface to the disk and a 24-Mbyte/s internal disk are provided. Price for a complete DSS-1412 disk subsystem including one

disk, DPS-2400 I/O subsystem, and software is \$123,300. **Aptec Computer Systems, Inc.**, 10180 SW Nimbus Ave, Portland, OR 97223. **Circle 297**

Rugged bubble memory cartridges come in sizes up to 500 Kbytes

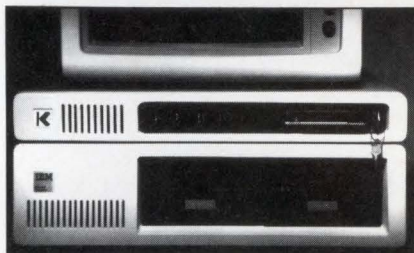
Innovative printed circuit board and packaging designs are behind a removable bubble memory cartridge that contains 0.5 Mbytes of memory. Other available cartridges include nonvolatile bubble memory versions with capacities of 128 Kbytes, 256 Kbytes, and 384 Kbytes. Cartridges are interchangeable. **Targa Electronics Systems, Inc.**, 3101B Hawthorne Rd, Ottawa, Ontario, Canada K1G 3H9. **Circle 298**

Tape controller performs 4 Mbyte/s bus transfers

The Tapemaster 1000, a controller for half-inch streaming and start/stop tape drives, uses a special data pipeline to transfer data across the Multibus at 4 Mbytes/s

with a 250-ns memory. It can transfer data to or from a drive at 1.5 Mbytes/s. A large onboard FIFO buffer of up to 4 Kbytes and true data throttling also distinguish this machine. Here, a preselected number of bus transfers will occur on each Tapemaster 1000 bus access, assuring Multibus data traffic control. Low quantity price for the Tapemaster 1000 controller is \$1654. **Ciprico**, 2405 Annapolis Ln, Plymouth, MN 55441. **Circle 299**

Compact unit provides mass storage for IBM PC/AT/XT



Integrating hard disk storage, a backup system and power directors for the IBM PC, AT and XT, the Masterflight system is packaged in a compact unit that fits between the computer and the monitor. The unit integrates five separate devices into a single box. They include a half-height 10-, 20- or 33-Mbyte hard disk; a half height 20-, 40- or 60-Mbyte streamer tape backup system; five power direction switches; a locking security key; and a surge protector. Each Masterflight system is configured to the user's specifications. The system is available immediately. Prices start at \$3795. **Kammerman Labs**, 8054 S W Nimbus, Beaverton, OR 97005. **Circle 300**

Internal hard disk upgrades the Mac

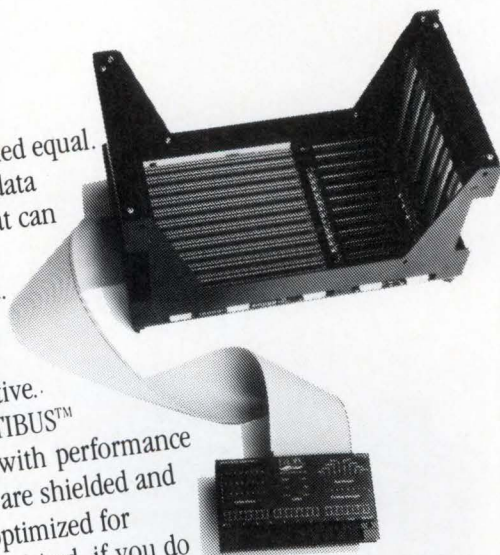
Combining an internal 10-Mbyte hard disk drive and memory expansion to 512 Kbytes of RAM, the HyperDrive enhances operation of the Macintosh computer. The machine's designers boast program transfers up to 20 times faster than the standard Mac. The HyperDrive's disk interface board directly connects to the Mac's main circuit, freeing the computer's serial ports for modem, printer, or AppleBus use. Thus, HyperDrive-equipped Macs can boot from either the hard disk or the machine's diskette. The cost of a HyperDrive is \$2195 (without RAM upgrade). **General Computer Co.**, 215 First St, Cambridge, MA 012142. **Circle 301**

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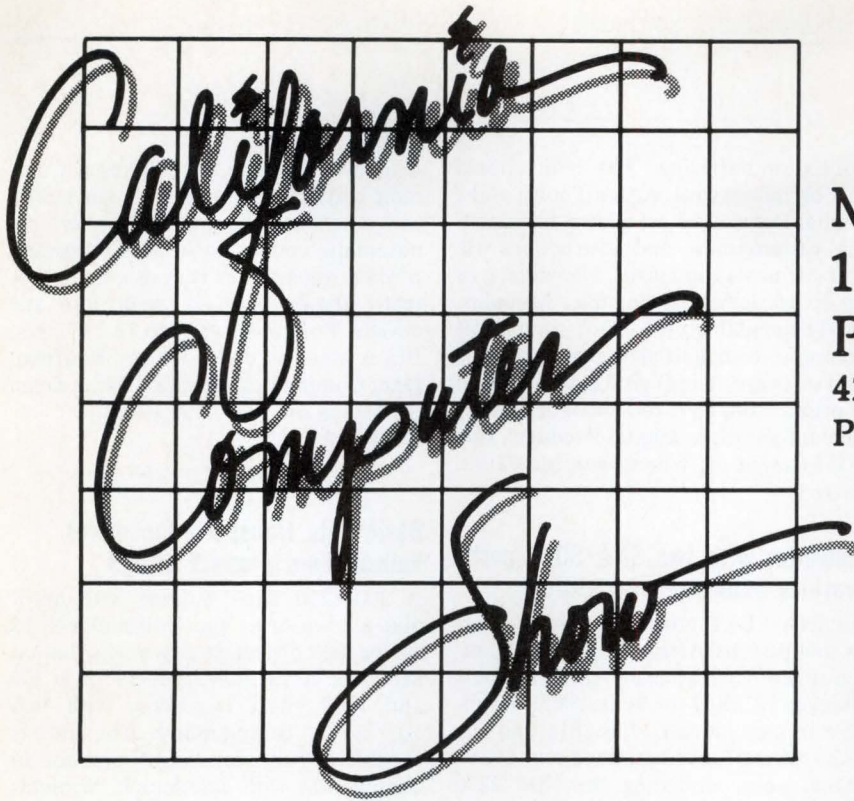
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Lower bit rates stimulate low cost networking capability

The 82588 controller brings 10-Mbit/s Ethernet chip set capabilities down to the 2-Mbit/s level. The 82588 reportedly supports the IEEE 802.3 standards now under development. The IBM Network and AT&T's StarLAN configuration loom as two important implementations of the chip. Housed in a 28-pin DIP, the device includes a programmable CSMA/CD controller, a 1- to 2-Mbit/s data encoder/decoder (supporting both NRZI and Manchester) and logic-based collision detection. The 82588 supports "buffer-chaining" memory management. The 82588 handles most functions associated with the physical and data-link layers of the Open System Interconnect model. Single-chip LAN controllers sell at \$45 each in lots of 1000. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 302**

LAN buffer links processor to master control computer

A bidirectional network buffer that links process control, shop or laboratory equipment, and a central management-analysis computer features up to 8 hours of data

collection buffering. The bidirectional link on this network buffer (known as the Digital DataCollector) allows downloading of programs and instructions via user-definable commands. Networking of up to 16 devices is possible. Modular, field-expandable RS-232-C-compatible components include all necessary cabling and software. The Digital DataCollector is priced from \$595 to \$8000, depending on configuration. **Digital Products, Inc**, 600 Pleasant St, Watertown, Ma 02172. **Circle 303**

Converter with two SNA/SDLC ports provides extensive diagnostics

An SNA/SDLC protocol converter family that permits users to add ports or configure protocols when an ASCII device is changed is called the Series 8800. Available in two models—the 8814 and the 8830—these converters have two SNA/SDLC ports emulating the IBM 3270 cluster controller. The 8814 has six ASCII ports but can expand to 12. The 8830 has eight ASCII ports and is expandable to 28. Software monitors the data stream on any connection and transmits the results to a selected port. A diagnostic program runs on command and "quick look"

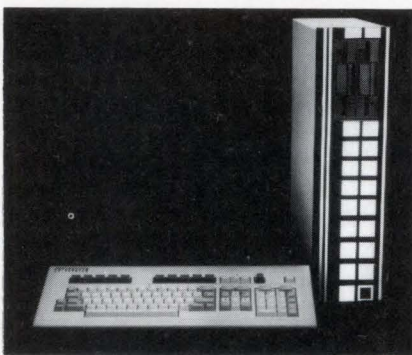
diagnostics are run at every reset. Common traffic control services (including assignment and requisition of passwords, automatic connect/disconnect, queuing of data when a port is in use, and automatic log-on/off) are built into the devices. Ports work at up to 19.2 Kbits/s. Prices start at under \$4000. **Kaufman Data Communications, Inc**, 145 E Dana St, Mountain View, CA 94041. **Circle 304**

Basic data transportation drives Volksmodem product design

A 300/1200 baud modem with auto-dial/auto-answer, the Volksmodem 12 can be used on standard two-wire dial-up networks. Asynchronous operation at 300 and 1200 bits/s is offered with Bell 103/212 A compatibility. The unit is capable of full unattended operation in conjunction with standalone terminals and computers with RS-232 interfaces. Power is provided by a 12-Vdc, 60-mA adapter. Casing measures 4.9 x 9.8 x 1.4 in. (12.5 x 25 x 3.75 cm). The unit is priced at \$299. **Anchor Automation, Inc**, 6913 Valjean Ave, Van Nuys, CA 91496. **Circle 305**

COMPUTERS

Supermicrocomputers center on a 68000 running at 10 MHz



Supermicros in the U-MAN 1000 series are 32-bit machines aimed at the single-user, mid-range market. Based on the 10-MHz 68000 processor, the systems have up to 1 Mbyte of RAM onboard, a 6809 I/O processor, dual 800-Kbyte floppies, and a 97-key keyboard. Besides two serial

ports, Centronics and general-purpose 16-bit parallel ports are offered. Presently, the CP/M68K and UCSD p-system are the operating systems offered supporting languages including CBasic, Pascal MT+, C, Forth, and Cambridge Lisp. **U-Microcomputers Ltd**, Winstanley Industrial Estate, Long Lane, Warrington, Cheshire, WA2 8PR England. **Circle 306**

Large memory capacity and dual-state architecture mark big systems

Systems in the Cyber 180 series are mid-range processors with four times the base memory of previous models. Expanded base memory capability of 16 Mbytes can be upped to 128 Mbytes of main memory. "Dual-state" architecture is featured. This setup provides the advantages of a virtual environment for users needing very large memories, while minimizing problems associated with virtual configu-

rations. I/O functions are isolated from CPU execution of user programs. Prices range from \$760,000 to \$1,575,000. **Control Data Corp**, PO Box 0, Minneapolis, MN 55440.

Circle 307

Multi-user series offers assorted setups for Unix systems

The Elite series of Unix-based multiuser systems is powered by 68010 and 68020 microprocessors. With the addition of an Ethernet controller, Elite models function in local area network configurations. The series features both VMEbus and Multi-bus architectures. The Elite 900 operates with a 16-MHz 68020; the 700 (which supports up to 21 users) with a 10- or 12-MHz 68010; the 500 with a 10- or 12-MHz 68010; and the 300 with a 10-MHz 68010. Prices begin at \$9995. **Brice Systems**, 737 Walker Rd, PO Box 558, Great Falls, VA 22066.

Circle 308

Single-board unit runs Forth and accommodates byte-wide memories

Forth development is speeded via the Forthcard, a single-board computer. It enables users to develop Forth and assembly language programs on an STD bus-compatible card. The unit uses the 65F11 Forth chip running at 1 or 2 MHz. It supports download and compilation of code from another computer. Sixteen I/O lines can be configured as parallel I/Os, interrupt inputs, serial I/Os (asynchronous, shift register, or multiprocessor communication), or as timer/counter I/O bits. The Forthcard can configure with an optional 5-V regulator or with most STD bus-compatible memory and I/O boards. Quantity pricing starts at \$299. **HiTech Equipment Corp**, 9560 Black Mountain Rd, San Diego, CA 92126. **Circle 309**

Supermicrocomputer boasts mainframe power

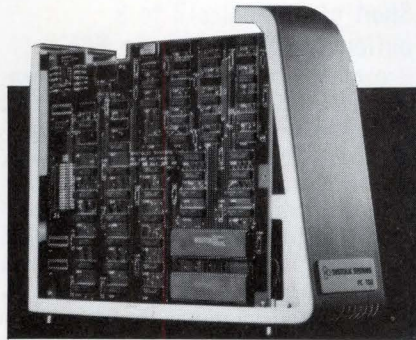
The 68/10 supermicrocomputer provides multitasking for up to 32 users. At the heart of the system resides a 68010 16/32-bit microprocessor that connects to a VMEbus and runs the Unix V operating system. The CPU links to a demand-paged MMU and a high speed 16-Kbyte cache memory that has a 90 percent average hit rate. Other features include a 32/64-bit IEEE floating point unit, a DMA controller, plus up to 8 Mbytes of memory. Using VLSI gate array technology, the 68/10 combines these elements to achieve 1-MIPS speeds with no wait states. The system provides two multiprotocol data links, a Centronics-compatible 8-bit parallel printer interface, and up to 32 RS-232-C serial ports. **Compuflex Inc**, 2601 E Chapman Ave, Fullerton, CA 92631. **Circle 310**

Unit features 20.8-Mbyte Winchester subsystem

Designated the Micro/11-73, this system contains a 20.8-Mbyte Winchester disk subsystem with RLV22 (RL02) software compatibility and a dual 8-in. floppy. A 1-Mbyte diskette subsystem is also featured. The system is supplied with a choice of dual size 256- or 512-Kbyte RAM modules or a quad-size 1 Mbyte RAM. All memory boards sport full byte parity. The 11-73 CPU contains 8 Kbytes of cache memory, floating point instruction set, memory management, and a line frequency clock. Two RS-232 serial ports are provided. One is used as the console

port. A basic system with 512-Kbyte RAM costs \$13,875 with quantity discounts available. **MDB Systems, Inc**, 1995 N Batavia St, Orange, CA 92267. **Circle 311**

Desktop array processor attaches to PC, mainframe speed reported

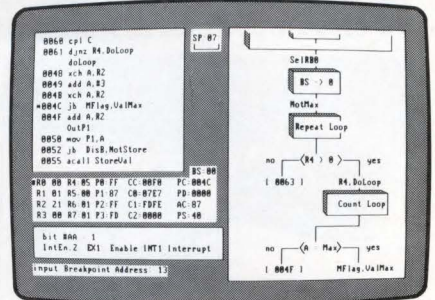


The PC-100 is billed as a desktop array processor that can attach to the IBM PC and other machines. With a 1-Mbyte/s DMA card, the PC-100 can perform a 100 x 100 matrix multiply in 20.6 s and a 1024-point vector norm in 0.02 s. The PC-100 software library includes linear algebra, nonlinear optimization, solution of differential equations, and signal processing program. Subroutines for scientific computing are also resident. Featured are IEEE standard arithmetic operation and 1-MFLOPS speed. The desktop array processor with DMA interface card and cable, and interface software, costs \$3589. **Systolic Systems, Inc**, 1630 Oakland Rd, San Jose, CA 95131. **Circle 312**

Multi-user, multitasking system boasts high Cobol throughput

The DPS 6/22 minicomputer is a multi-user system. Its central processor is augmented with a commercial instruction processor (CIP), which increases throughput of Cobol programs by executing instructions in firmware. A scientific instruction processor enhances Fortran, Basic, and Pascal performance and extends performance for Honeywell's InfoCalc electronic spreadsheet. Main memory capacity is 1.75 Mbytes, which can be doubled. Terminal and peripheral support is provided through a five-port workstation controller. All DPS 6/22 configurations include a hard-disk subsystem. With a 28-Mbyte fixed disk, a basic system costs \$12,995. **Honeywell Inc**, 200 Smith St, Waltham, MA 02154. **Circle 313**

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8051	✓	✓	✓
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8085		✓	✓
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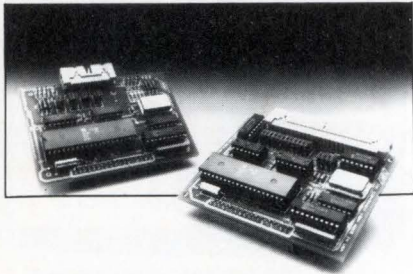


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CIRCLE 110

Dual serial multimodules extend I/O capacity of Multibus systems



Serial I/O capacity on the Multibus expands via the SERX-232 module. Here, two piggyback boards provide two added serial ports to any host Multibus board with an iSBX connector. Use of a Z8530 serial communications controller allows operation in asynchronous, byte-synchronous, and bit-synchronous modes. The unit supports X.25, SDLC/HDLC, and Bisync protocols. Modules support programmable data rates from 50 baud to 38.4 kbaud. **SBE, Inc.**, 2400 Bisso Ln, Concord, CA 94520. **Circle 314**

Bit-mapped compression board allows vector graphics on nonimpact printers

A board option to the Pixel 300 intelligent controller system, the BCB-300, reduces memory costs by requiring only one-half Mbyte of bit-mapped memory to output full-page graphics. This bit-mapped compression board allows complex vector graphics generation on nonimpact printers. The Pixel 300 controller system centers on the 68000 microprocessor. Based on the VMEbus, this unit has an open system architecture. The Pixel 300 board is offered for \$2000 per unit in quantities of 500 or more. **Electronic Machine Corp.**, 417 S Hill St, Los Angeles, CA 90049. **Circle 315**

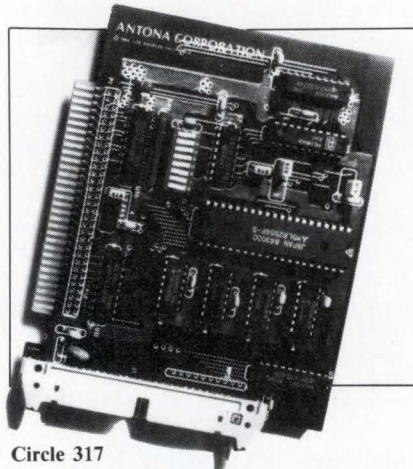
Board lets users concurrently run 3270 and PC-DOS applications

Designed to emulate 3278 and 3279 terminals, a micro-to-mainframe communication board has unique windowing features. Emulation allows a PC to access 3270 applications while concurrently running PC applications. Named the Power-Link, this interface board enables the user to view one host session containing information from a mainframe, one PC-DOS session from the personal computer, and two electronic note-pads. Users can select 10 screen profiles with one to four windows per screen. DMA board features

allow fast screen update, and quick data transfer. Multiple files may be transferred by creation of a batch file, then executed with a few keystrokes. Full international keyboard mapping comes standard. The board measures 5-in. long. **Tecmar, Inc.**, 6225 Cochran Rd, Solon, OH 44139. **Circle 316**

Short card handles 3 to 8 buffered I/O channels on PCs

Providing 3 to 8 buffered TTL I/O channels, the ANC-1055 occupies a short card slot in the IBM PC, XT, or AT. Programmable interrupt circuitry monitors four of the 245 channels to generate a user-selectable, software enabled interrupt. The programs can be done in Assembly language or MS-DOS Basic. The ANC-1055 card is directly pin compatible with the Opto 22, Crydom, and Gordos lines of modular relay boards making this card appropriate for industrial applications. Unit pricing is \$119. **Antona Corp.**, 2100 S Sawtelle Blvd, W Los Angeles, CA 90025.



Circle 317

Bidirectional data flow achieved in CMOS format

Designated the 54/74ACT646, a bidirectional 8-bit device in CMOS is pin compatible with existing bipolar interface circuits. The device can receive input signals and drive several interface devices. Two registers and two multiplexers are combined on this circuit. Data can be stored or transmitted via the registers, and the multiplexers, acting as switches, permit realtime data transfer or stored data transfer from one side to the other. This is a three-state noninverting device. Output drive current measures 12 mA. Operation of up to 25 MHz is achieved in the commercial temperature range. The plas-

tic model costs \$8.58 and the ceramic version costs \$9.92, each in quantities of 100. **Monolithic Memories, Inc.**, 2175 Mission College Blvd, Santa Clara, CA 95050. **Circle 318**

Digital controller for servo systems hooks up to Multibus

A Multibus-compatible digital controller handles brushless ac servomotor motion control. Commutation, velocity, and position servo-loops are precisely controlled in software. A 16-bit microcontroller is used to direct up to three motors, with a 1-ms update rate. Key features include three axes of control per card, multi-axis synchronization, and a 192-axis/host communication matrix. Continuous diagnostics are also reported. **Moog Inc., Electric Motion Controls Div.**, E Aurora, NY 14052. **Circle 319**

Advanced DMA controller boosts I/O throughput

Advanced DMA controllers in the 82258 series aim at applications requiring high speed I/O processing and throughput. In operation, the 82258 uses command and data chaining features to remove I/O processing functions from the central processor. Also touted is a transfer rate of 8 Mbytes/s (when the controller combines with iAPX 286 pipelined architecture). With speed selections of 6 and 8 MHz, the controller will be available in mid-1985, with the 6-MHz version priced at \$170 in quantities of 100. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 320**

Graphics processing board delivers high resolution on the Q-bus

A color display board—the QD512—sports LSI-11 Q-bus compatibility. It can operate as a 512- x 512- x 8-bit display or as the controller of a 4096- x 4096- x 8-bit system. It plugs directly into any quad Q-bus slot. Data loads into the unit by programmed I/O or by the QD512's DMA circuitry. QD512 resident data is continuously displayed on a standard monitor at a 10-MHz rate. Visible portion of the image covers 484 lines of 512 pixels each. Hardware zoom and roam functions allow rapid access to image details. Programs are called in Fortran. **Image Analytics Corp.**, PO Box 362, Hockessin, DE 19707. **Circle 321**

Large scale automatic testing offered in compact unit

Functional testers in the Compact Testers family run pin-modules at 4-MHz real time. Maximum pin count lists at 352 and IEEE analog capability is reported. Memory storage via a Winchester disk drive lists at 32 Mbytes, and a 10 Mbyte streaming tape drive is included. An optional high speed data link is offered, as is a CRT for programming without interrupting test processes. The basic Compact Tester comes packaged in a 6.6 ft² bay, with prices as low as \$110,000. **Computer Automation, Inc, Industrial Products Div, 2181 DuPont Dr, Irvine, CA 92713. Circle 322**

Programmers are optimized for logic to speed test/design process

Two logic programmers combine simple, menu-driven operating protocols with sub-2-s programming and testing. The portable units—the 60A and 60H—can each program more than 125 devices. The 60A is a multi-user tool for prototyping in the engineering lab. Used together with

a personal computer and logic design software, it can form a complete design and programming station. The 60H merges capabilities of the 60S with a software and hardware interface to an automatic device handler (not included). The programmers incorporate power-down-save storage of all programming parameters, and are compatible with the ABEL logic design language and the Programmable Logic Development System. The 60A sells for \$3425. The 60H sells for \$4425. **Data I/O Corp, 10525 Willows Rd NE, PO Box 97046, Redmond, WA 98073. Circle 323**

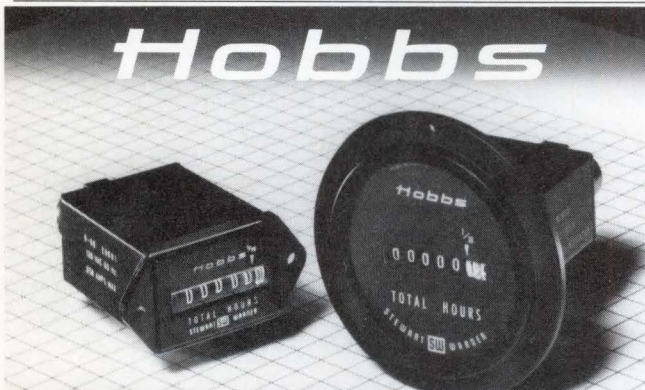
Emulator equipped with overlay memory runs on MicroVAX 1

True 32-bit universal microprocessor development derives from ZAX ICD-series in-circuit emulators linked to the DEC MicroVAX I. Development software for the ZAX/VAX combo includes C, Pascal, and PLM 86 support, manufacturer-compatible cross assemblers, and ZICE, which delivers full symbolic debugging capability, batch file control of the emulators, automatic journaling, and extensive help.

In-circuit emulators for 8086, 8088, 68000, 68010, Z80, 80186, and other families come with emulation overlay memory and breakpoint capabilities. With the emulators priced from \$4995 (for 8-bit) and \$7995 (for 16-bit), a typical three-user ZAX/VAX development system (including 8- and 16-bit emulators and terminals) is priced at \$56,000. **Zax Corp, 2572 White Rd, Irvine, CA 92714. Circle 324**

Desktop CAD system excels at drafting applications

A desktop computer aided design and drafting system—the Arttech 217 Workstation—is an engineering personal computer fully compatible with the Arttech 220 and 220GP stations. All three systems can be networked. The 217 is built around a 32-bit, 9000 computer. A 68010 utilizes 2 Mbytes of RAM. A system that includes the 217 workstation, a dual-disk drive, and Arplan software, costs \$29,900. **Skok Systems Inc, 222 Third St, Cambridge, MA 02142. Circle 325**



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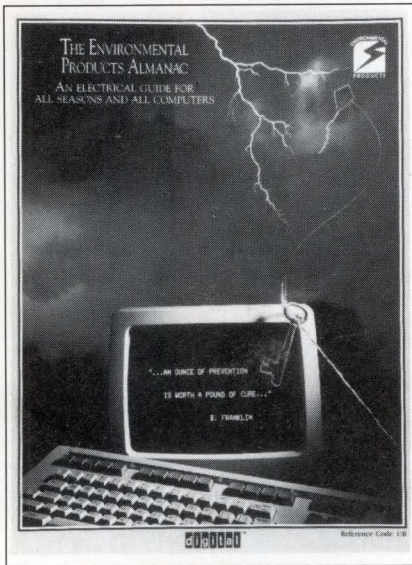
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Environmental protection



A booklet explains power related computer problems while presenting a line of products that include power distribution systems, constant voltage conditioners, transient voltage suppressors, and remote power switches. **Digital Equipment Corp**, Merrimack, NH.

Circle 410

Data on CMOS and NMOS

A special functions data manual compiles information on CMOS and NMOS products. Eleven chapters detail topics such as CMOS A-D and D-A converters, decoders and display drivers, and CMOS remote control functions. Data sheets provide complete specs for the individual circuits, including pin connections, block diagrams, testing and application information, and electrical elements. Pricing for the CMOS/NMOS manual is \$1.60 in quantities of 1 to 9. **Motorola**, Tempe, Ariz.

Circle 411

Surface mounting and device packaging

An updated brochure recommends products for surface mounting and device packaging. Adhesives and solder pastes are covered. **Electro-Science Laboratories, Inc**, Pennsauken, NJ.

Circle 412

ZIF sockets

Bulletin describes zero insertion force sockets and outlines the sockets' secure locking mechanism, easy insertion, and low profile. **Garry Electronics**, Langhorne, Pa.

Circle 413

Messenger workstations

A 16-page color brochure explains features and benefits of PDX Messenger workstation. Designed for networking, the Messenger communicates with CPUs via SNA, X.25, and Pixnet. The machine provides 3270 host access and PC functions. **Paradyne**, Largo, Fla.

Circle 414

Data product details

A short brochure details housings, logic boards, keyboards, plus auxiliary cards and software for a terminal and module line. **Falco Data Products, Inc**, Sunnyvale, Calif.

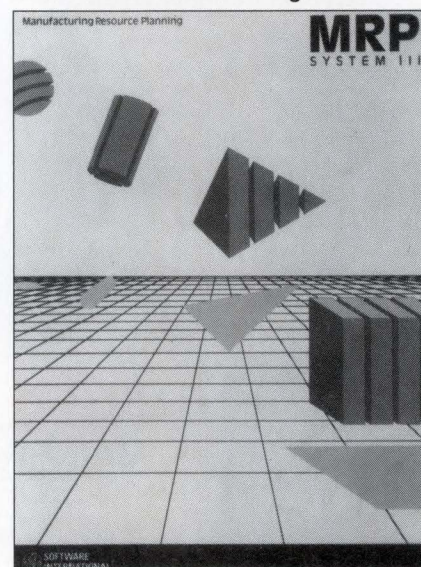
Circle 415

Structural software

A general-purpose structural software system capable of static, dynamic, and thermal analysis is the subject of a free brochure. Developed by the Georgia Institute of Technology, the system is known as GTSTRUDL. It provides a sophisticated structural data base system for frame structures. **Babcock & Wilcox**, Lynchburg, Va.

Circle 416

Mainframe manufacturing software



A modular, closed-loop manufacturing and resource planning software system for mainframes is described in a 16-page system brochure. The brochure details modules that plan materials required, schedule shop floor activities, and perform costing. **Software International Corp**, Andover, Mass.

Circle 417

Circuit board ATE

Item introduces L210 VLSI board test system, highlighting two possible test strategies: MultiMode, for commercial VLSI and modern bus architectures, and Performance Functional Testing, which is practical for boards with custom VLSI and advanced packaging. **Teradyne**, Boston, Mass.

Circle 418

Full test and instrumentation line

Test and instrumentation products and accessories from Wavetek are described in a 233-page catalog. In addition to full product descriptions, the book contains a selection guide that compares instrument features. **Wavetek**, San Diego, Calif.

Circle 419

Configurable graphics memory

Plotter Notes series for P 7550A-type products expands with a 16-page note. This application note defines configurable graphics memory, tells when and how to allocate memory, and advises you on the best use of each buffer. **Hewlett-Packard Co**, Palo Alto, Calif.

Circle 420

Integrated software for networking

Software developments covering systems for automated component sequencing, testing, insertion, and SMT assembly are depicted in a 12-page brochure. These integrated software tools can operate a single circuit assembly system, a network, or an automated factory. **Universal Instruments Corp**, Binghamton, NY.

Circle 421

Fiber optics for CAD

A fiber optic system designed specifically to remotely handle Computervision's Instaview color and monochrome CAD/CAM workstations is highlighted in a brochure that discusses the advantages of fiber optics. **Artel Communications Corp**, Worcester, Mass.

Circle 422

Printer choices

This 16-page brochure helps those selecting printers. Specific applications and their requirements are studied for a broad range of printers including panel and label miniprinters, as well as slip/document and column roll types. **Printer Products**, Boston, Mass.

Circle 423

MARKET FORECASTS

CRT displays

Unit sales of CRT monitors will progress at a 17-percent annual clip through 1990, according to Venture Development Corp, vaulting from just over 8 million units shipped in 1983 to 25 million in 1990. In *The CRT Video Display Monitor Industry through 1990*, the research firm anticipates only limited displacement of the traditional CRT by emerging flat-panel screens. CRTs, the firm feels, will remain functionally superior and less expensive. The report also notes that color monitors will show sustained increases in share of both end-user and OEM shipments, primarily due to expanding demand for graphics capabilities. The study sells for \$7500. **Venture Development Corp**, 1 Washington St, Wellesley, MA 02181. **Circle 469**

Hybrid circuits in Europe

Frost & Sullivan, Inc predicts that growth in the hybrid circuit market in Europe will proceed at a 35-percent average annual rate through 1989. New techniques in hybrid technology should drive the market to a \$3.9 billion level by the end of the decade. (Hybrid technology is a method of assembling electronic circuits using a substrate with interconnecting tracks onto which components such as semiconductor chips can be attached.) Hybrids are gaining in importance, the 272-page analysis states, because the resistor tracks connecting components can be trimmed to required tolerances. This garners an important advantage compared to other assembly techniques. Surface-mount techniques should affect hybrids heavily, the study notes. With anticipated growth rates averaging 119 percent annually through 1989, surface mounting will eventually outstrip the two traditional hybrid techniques—thin-film and thick-film. From a 1984 base of \$41 million, surface mounting will expand to nearly \$2.3 billion by 1989, gaining a 57 percent market share. Surface-mount development will also increase use of automated production techniques. Thick-film circuits, which comprise the bulk of the market at present (89 percent in 1984), will remain dominant until the end of the forecast period, when that sector's 40 percent share will be eclipsed by surface mounting. The thin-film sector will shrink, Frost & Sullivan believes, from 6 percent of the overall market, to 3 percent. The price of the report is \$1750. **Frost & Sullivan, Inc**, 106 Fulton St, New York, NY 10038. **Circle 470**

Printers

The printer market has become a personal computer-driven market, according to Datek Information Services. The *Printout Annual* reports that 1984 sales were high, but profits were minimal. The low end dot-matrix and full-formed character serial printer segments have exhibited the best record. Last year, these two technologies accounted for 66 percent of all printer sales in the U.S. Within the serial dot-matrix printer category, 83 percent of all shipments were machines running at 180 char/s or less. Japanese suppliers have gained a large segment of the low end market, forcing domestic vendors to counter with higher performance printers as well as sourcing of low end Japanese machines. This trend is likely to continue, Datek says. The 102-page *Printout Annual* is available for \$25. **Datek Information Services, Inc**, PO Box 68, Newtonville, MA 02160. **Circle 471**

Business software protection

For every authorized publication of business software, there is a pirated copy in circulation. This, according to Future Computing, Inc, is a major fact of life in the present software market. Basing its estimate on 45,000 questionnaire responses, Future Computing sets 50 percent as a conservative estimate of the extent of software piracy in the personal

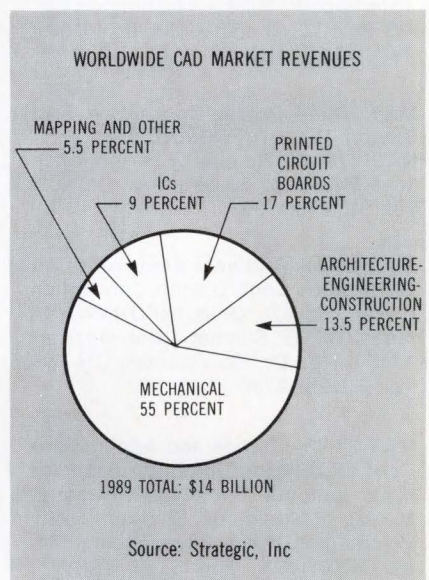
computer marketplace. Survey results are available in two reports: *Office Personal Computer Software Markets* and *Office Personal Computers: the Customers*. The surveys focus on twelve top business software packages for personal computers. Some of the products analyzed had a copy-protection feature designed to thwart unauthorized duplication, while others did not. Research indicates that copy-protected software is unlawfully used at almost the same rate as unprotected software. According to Future Computing, piracy cost the business software industry \$1.3 billion in lost revenues between 1981 and 1984. **Future Computing**, 8111 LBJ Freeway, Dallas, TX 75251. **Circle 472**

Disk drives

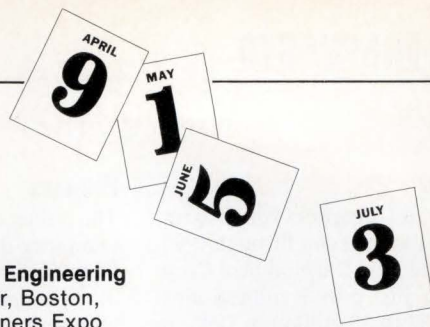
The market for 5¼-in. "quad-density" (double-sided, double-density, 96-track/in.) disk drives will surge as business users demand increased capacity, according to International Data Corp. The group maintains that business users account for at least 80 percent of today's storage market, and that their use of database management and graphics software mandates future disk drive storage needs. IDC predicts that half-height disks will be attractive as an interim product while OEMs await greater acceptance of sub-5¼-in. disks. **International Data Corp**, 5 Speen St, Framingham, MA 01701. **Circle 473**

IBM and mechanical CAD

With its new thrust into industrial automation, IBM will exert a greater force on all CAD/CAM markets, according to Strategic, Inc. The research group feels that the mechanical design sector should account for 55 percent of the \$14 billion in revenues it foresees for worldwide CAD markets in 1989. In the last four years, IBM has experienced a mercurial rise in the CAD market share. During this period, IBM managed to double its CAD share to 25 percent and become market leader, according to Strategic. In a recent study entitled *IBM's Industrial Automation Strategy*, the large market for computer integrated manufacturing (CIM), is considered. The report also looks at CIM's importance in CAD market strategies. This report views IBM's plans in the industrial automation sector, and identifies and analyzes the market impact. **Strategic, Inc**, 10121 Miller Ave, PO Box 2150, Cupertino, CA 95015.



Circle 474



CONFERENCES

APR 29-MAY 2—Society for Information Display Symposium & Exhibit, Sheraton Twin Towers, Orlando, Fla. INFORMATION: Hildegard Hammond, 201 Varick St, New York, NY 10014. Tel: 212/620-3388

MAY 6-9—Comdex Spring, Georgia World Congress Center, Atlanta, Ga. INFORMATION: The Interface Group, Inc, 300 First St, Needham, MA 02194. Tel: 617/449-6600

MAY 13-17—Int'l Conf on Distributed Computing, The Fairmont Hotel, Denver, Colo. INFORMATION: Dr Earl Swartzlander, TRW, Defense Systems, 1 Space Park, Redondo Beach, CA 90278. Tel: 213/535-4177

MAY 14-16—Test & Measurement World Expo, San Jose Convention Center, San Jose, Calif. INFORMATION: Meg Bowen, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

MAY 20-22—Custom Integrated Circuits Conf, The Portland Hilton Hotel, Portland, Ore. INFORMATION: Dr Wesley N. Grant, Sperry Computer Systems, Sperry Park, PO Box 43525, MS Y11B1, St Paul, MN 55164. Tel: 612/456-4130

MAY 20-22—Electronic Components Conf, Capital Hilton Hotel, Washington, DC. INFORMATION: Tom Pilcher, 3029 E Washington St, PO Box 372, Indianapolis, IN 46206. Tel: 317/261-1592

MAY 20-24—Dayton Convention Center, Dayton, Ohio. INFORMATION: NAECON '85, Samuel J. Rosengarten, 1445 Devoe Dr, Beavercreek, OH 45385. Tel: 513/255-4709

MAY 20-24—National Aeronautics and Electronics Conf, Dayton Convention Center, Dayton, Ohio. INFORMATION: NAECON '85, Samuel J. Rosengarten, 1445 Devoe Dr, Beavercreek, OH 45385. Tel: 513/255-4709

MAY 21-22—Trends and Applications Conf on Utilizing Computer Graphics, IEEE Computer Society and National Bureau of Standards, Sheraton NW Washington Hotel, Silver Spring, Md. INFORMATION: Mark Skall, NBS, Technology Bldg, Room A265, Gaithersburg, MD 29899. Tel: 301/921-2431

JUNE 3-5—Eastern Design Engineering Show, Bayside Expo Center, Boston, Mass. INFORMATION: Cahners Expo Group, PO Box 3833, Stamford, CT 06905. Tel: 203/964-0000

JUNE 3-6—Robots 9, Cobo Hall, Detroit, Mich. INFORMATION: Public Relations Dept, Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

JUNE 9-13—Computer Vision and Pattern Recognition, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 17-19—Int'l Conf on Computer Architecture, Boston Park Plaza Hotel, Boston, Mass. INFORMATION: Computer Architecture, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 19-21—NEPCON East, Bayside Expo Center, Boston, Mass. INFORMATION: Cahners Expo Group, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

JUNE 20-22—Int'l Conf on Fault-Tolerant Computing, Hyatt Hotel, Ann Arbor, Mich. INFORMATION: Prof John F. Meyer, Dept of Electrical Engineering & Computer Science, Univ of Michigan, 1075 E Engineering Bldg, Ann Arbor, MI 48109. Tel: 313/763-0037

JUNE 23-26—Design Automation Conf, Caesars Palace, Las Vegas, Nev. INFORMATION: Hillel Ofek, 1080 Marsh Rd, Menlo Park, CA 94025. Tel: 415/324-0700

JUNE 25-27—Computer Graphics West, Los Angeles, Calif. INFORMATION: Nat'l Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

JUNE 27-28—Workshop on Robotics and Expert Systems, Johnson Space Center, NASA, Houston, Tex. INFORMATION: Instrument Society of America, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

JULY 15-18—National Computer Conf, McCormick Pl, Chicago, Ill. INFORMATION: Helen Mugnier, AFIPS, 1899 Preston White Dr, Reston, VA 22091. Tel: 703/620-8926

JULY 22-26—SIGGRAPH, Moscone Center, San Francisco, Calif. INFORMATION: SIGGRAPH Conf Services Office, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

SHORT COURSES

MAY 20-22—Commercial Artificial Intelligence: Myths & Realities, Century Plaza Hotel, Los Angeles, Calif. INFORMATION: Gartner Group, Inc, PO Box 10212, Stamford, CT 06904. Tel: 203/964-0096

MAY-JULY—Knowledge Acquisition for Expert Systems, Palo Alto, Calif; Washington, DC; Cambridge, Mass. INFORMATION: Expert-Knowledge Systems, Inc, 6813 Old Chesterbrook Rd, McLean, VA 22102. Tel: 703/734-6966

MAY-JULY—Various Data Communications Courses, various cities. INFORMATION: Systems Technology Forum, 9000 Fern Park Dr, Burke, VA 22015. Tel: 703/425-9441

MAY-NOV—CAD 2001: The Countdown, Dallas, Tex; Boston, Mass; London, England; San Francisco, Calif. INFORMATION: CAD Seminars, Inc, 150 E Riverside, Suite 400, Austin, TX 78704. Tel: 512/445-7342

JUNE 3-4—Artificial Intelligence in Electronic Engineering & Manufacturing, Boston, Mass. INFORMATION: IPAC, PO Box 1869, Los Gatos, CA 95031. Tel: 408/354-0700

JUNE 3-12—Knowledge-Based Machine Vision, Southeastern Massachusetts Univ, N Dartmouth, Mass. INFORMATION: Prof C H Chen, Electrical & Computer Engineering Dept, SMU, N Dartmouth, MA 02747. Tel: 617/999-8475

JUNE 13-14—Optical Storage of Information, Univ of Wisconsin, Madison, Wis. INFORMATION: Univ of Wisconsin-Extension, Dept of Engineering & Applied Science, 432 N Lake St, Madison, WI 53706. Tel: 608/262-2061

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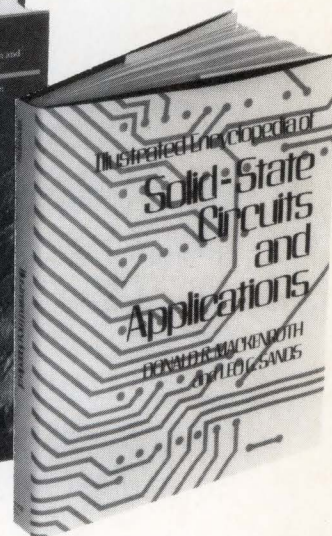
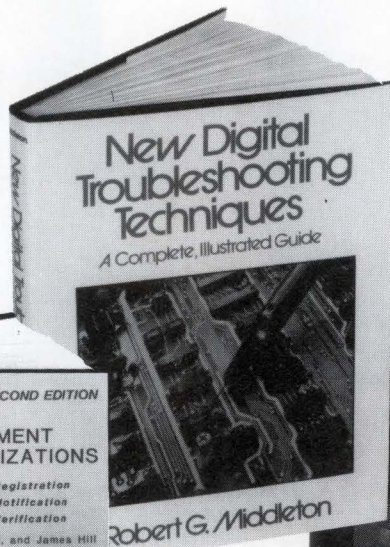
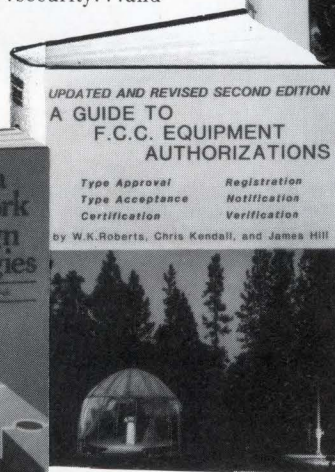
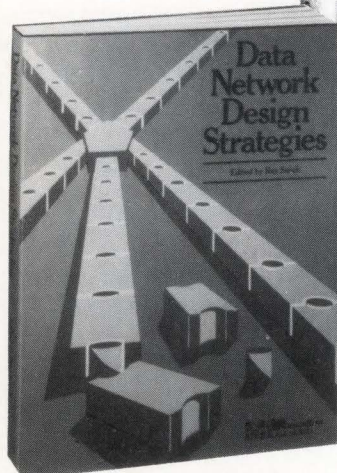
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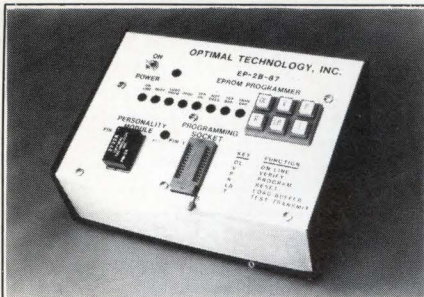
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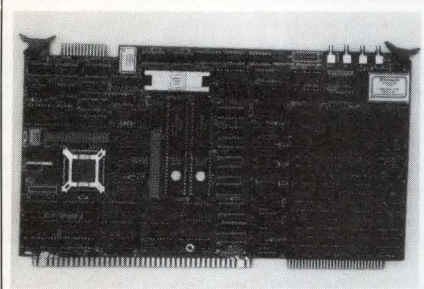
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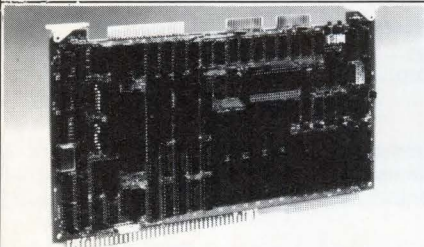
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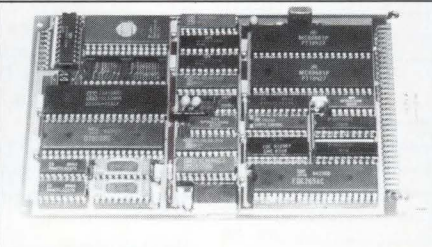


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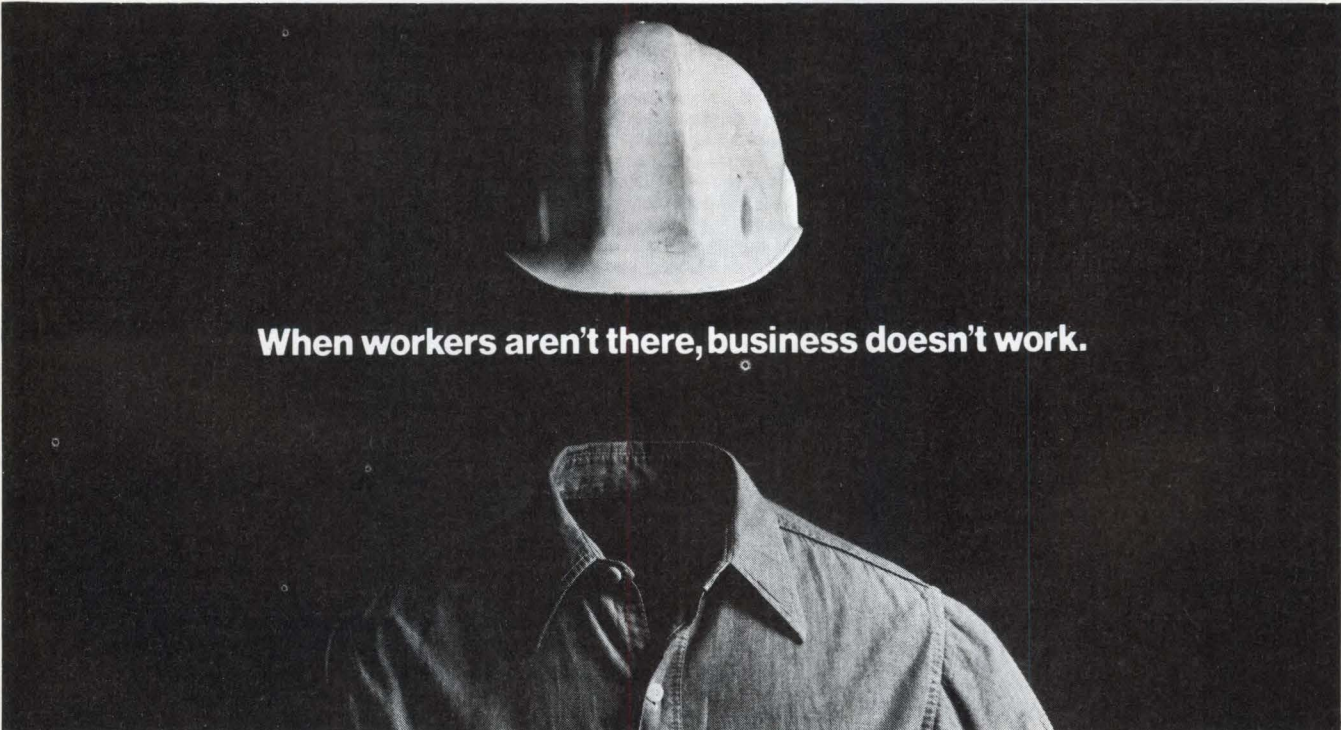
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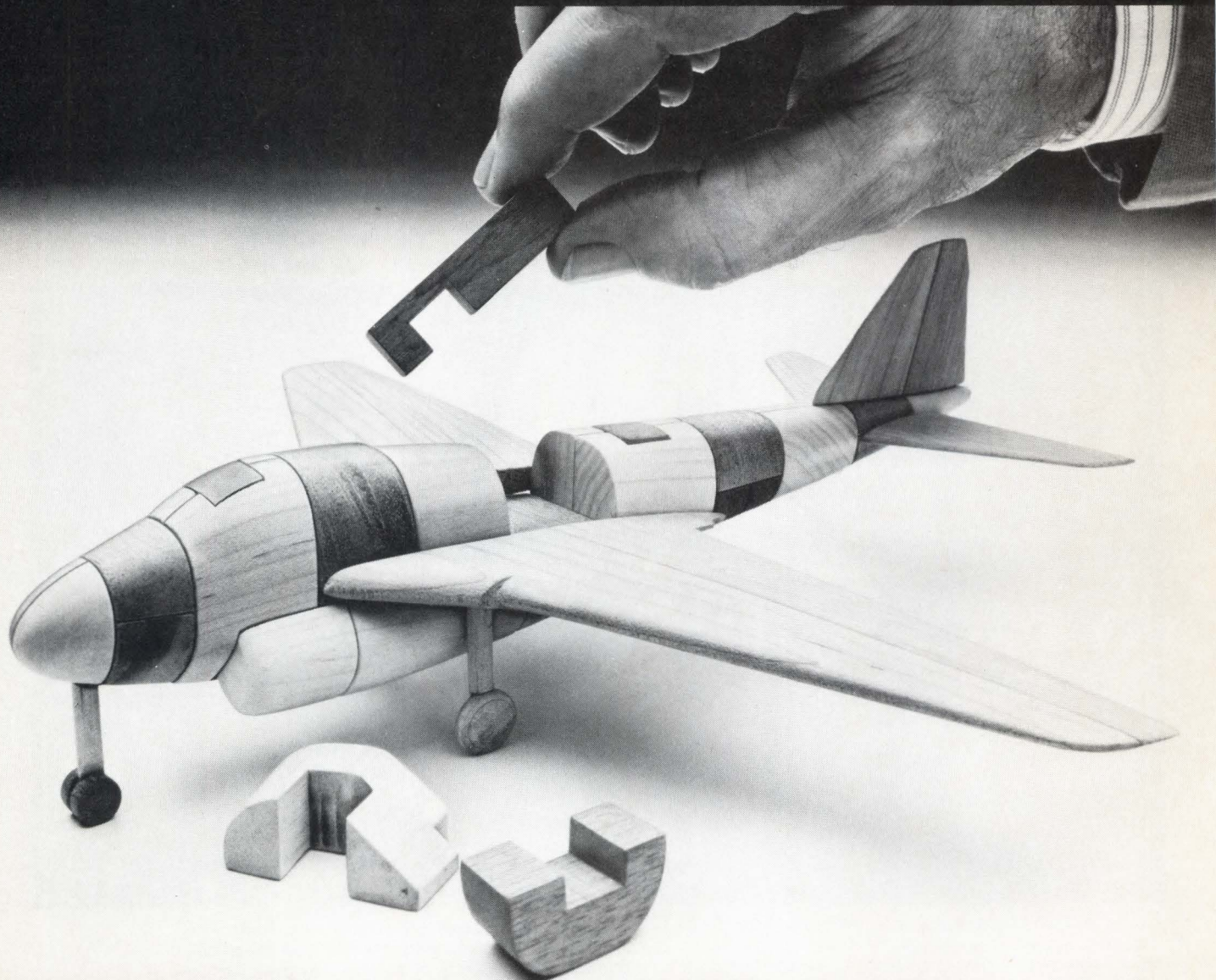
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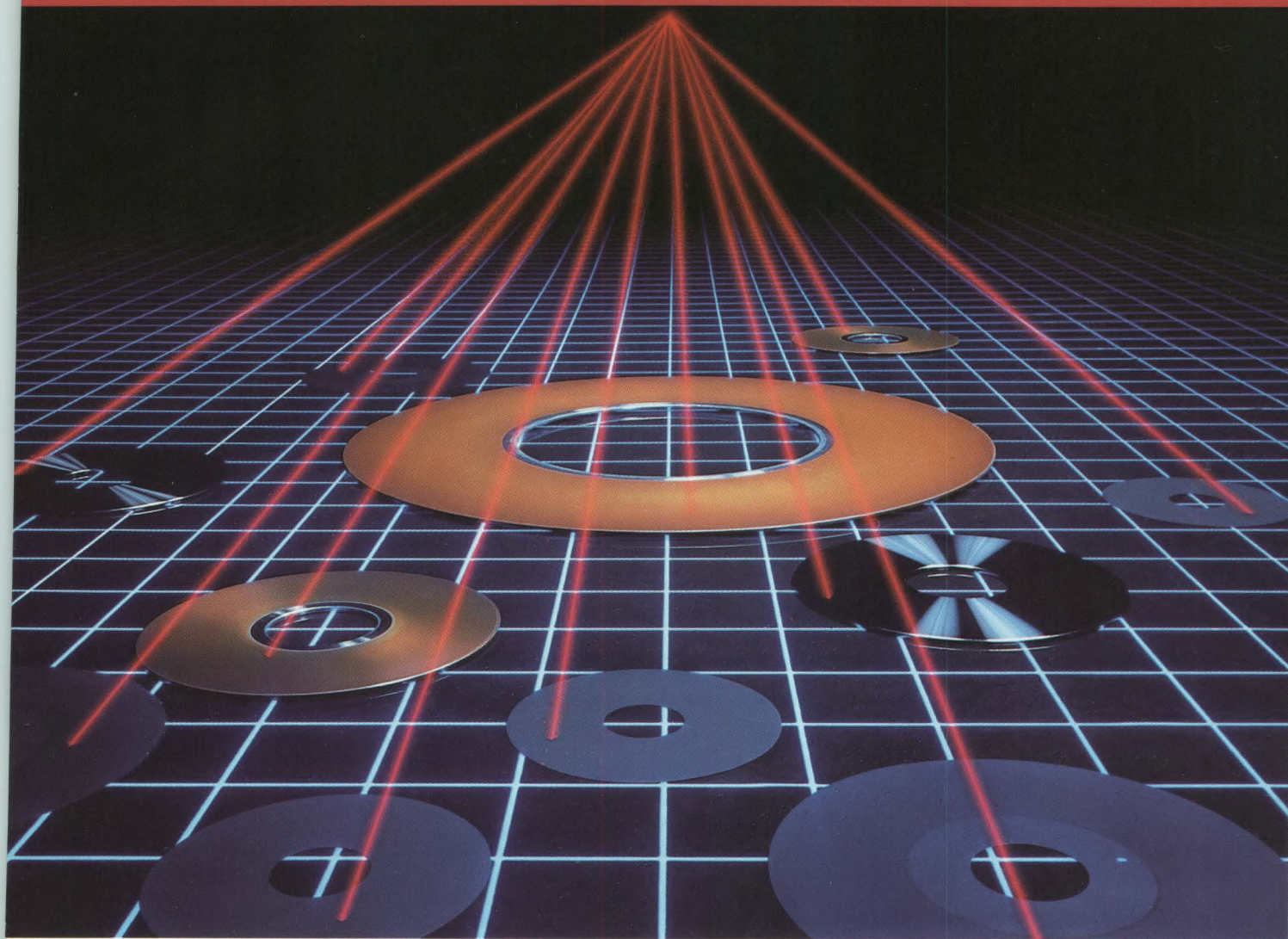
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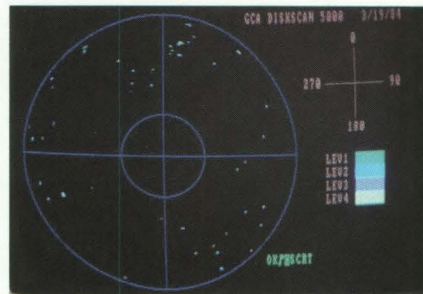
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