A PennWell Publication

# COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

## SPECIAL REPORT ON MICROSYSTEMS

## SYSTEM DESIGN WITH 32-BIT MICROPROCESSORS

## PROTOCOL ANALYZERS SIMPLIFY NETWORK DESIGN

## SPEECH RECOGNITION ENTERS THE REAL WORLD

## REMOVABLE WINCHESTERS TRIM SIZE

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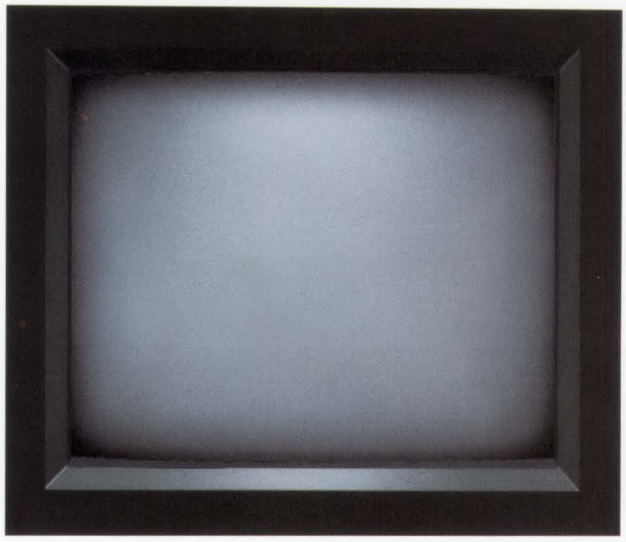

Which is to say, nonexistent. Some manufacturers make graphics software packages for mainframes. Others for minis. Still others make it for micros. But no one made high-level graphics software that ran on all three.

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CIRCLE 1

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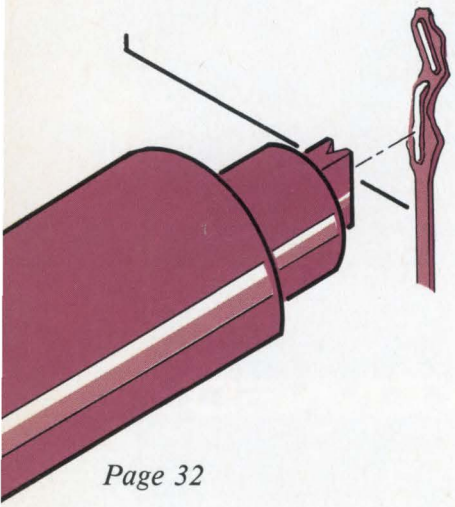
CIRCLE 2

COMPUTER DESIGN®

## System technology



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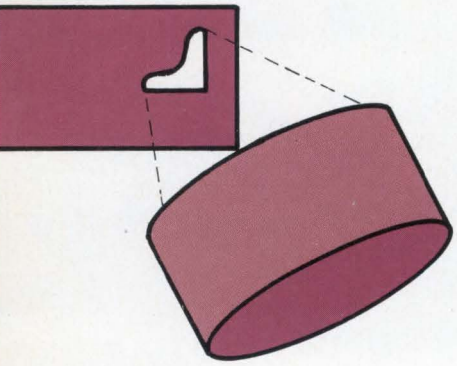
## System design



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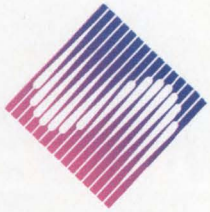
## SIGGRAPH '84



Vol 23, No. 7
June 15, 1984

# Special report on microprocessors/microcomputers—Part II



*This month's cover was created and designed by Mark Lindquist, Joe Pasquale, and Anezka Sebek. Parts of the design for this cover and the June I cover were based on material supplied by Pyramid Technology.*

# NCC product preview



# Departments



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(Top row L to R: Super Slave 128, HDC-1001, Super Slave 64, Bottom row L to R: Super Quad, Super 186, Super Six)

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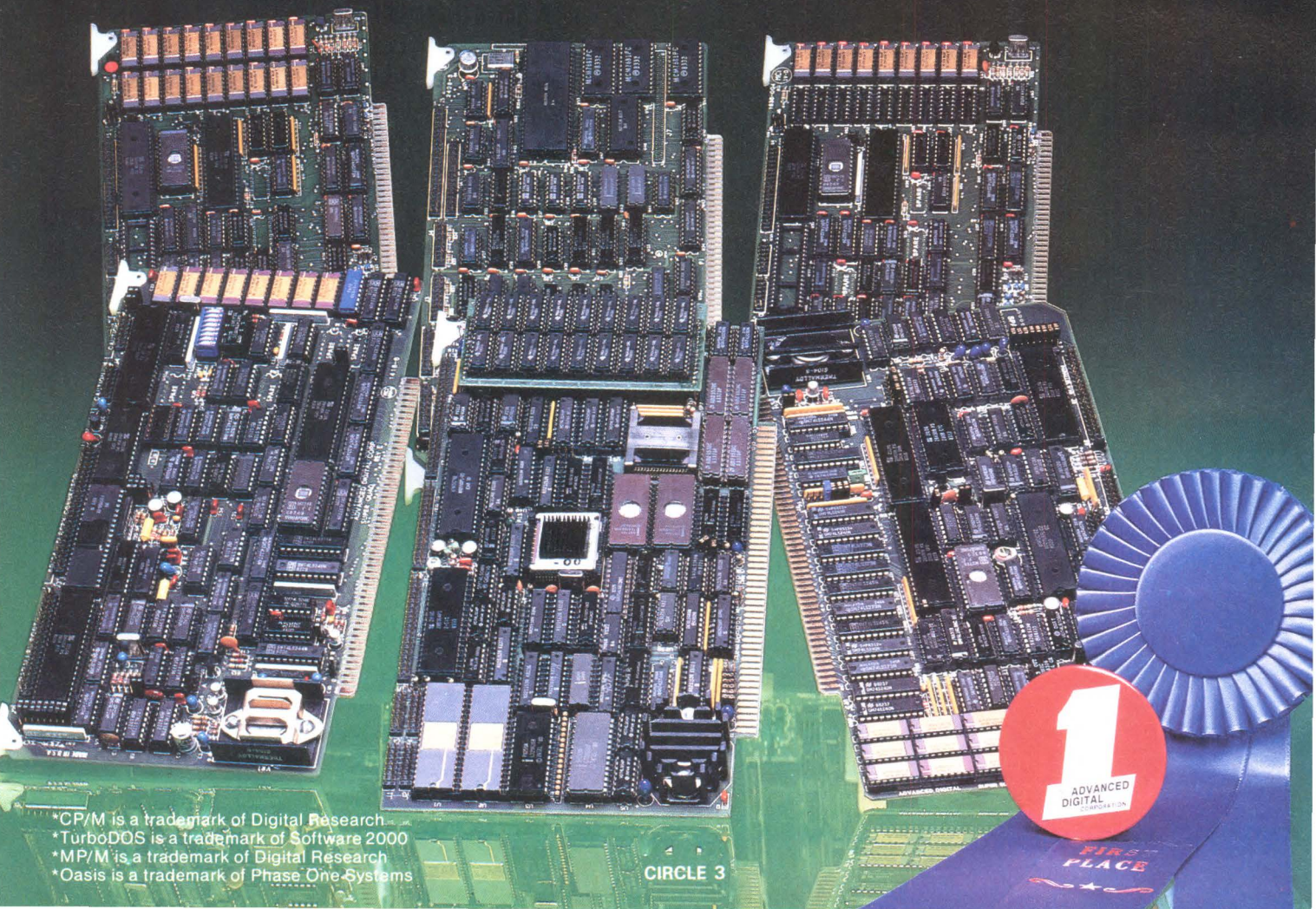


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CIRCLE 3

# UP FRONT

## DisplayWriter-to-PC connection is no bargain

Just-introduced, the IBM board-and-cable kit that allows the IBM-PC (and compatibles) to communicate with the IBM DisplayWriter dedicated word processor is raising some eyebrows. Until now, DisplayWriters could communicate only with 5520 Administrative systems and System 38s. But now, Big Blue says, for a mere $495 per connection board, a DisplayComm bisync program at another $375, and $299 for DisplayWrite2 software to emulate the DisplayWriter's commands for editing and formatting—an $1169 total just to hook up—design managers can integrate their DisplayWriter with a PC to run DBMSs, spreadsheets, integrated packages, computer aided design programs and more. A DisplayWriter costs about 2½ times the price of a fully equipped PC. Since a PC costs little more than $1169, and since (for most applications), a DisplayWriter cannot easily compete with current PC word-processing packages (which go for $200 to $500 or less), the hook-up is not feasible for many users. IBM has not said it is phasing out the DisplayWriter, but its more functional PC is a competitor for a high percentage of the dedicated word-processing customer base.—*H.H.*

## Technology marriage results in second product

A technology exchange pact forged three years ago by Intel Corp (Santa Clara, Calif) and Harris Corp (Melbourne, Fla) has borne its second fruit with the introduction of Harris Semiconductor's 80C88 CMOS 8/16-bit microprocessor. Coming one year after the debut of the 80C86 (a 16-bit CMOS microprocessor), the 80C88 displays full software compatibility with the earlier chip, as well as compatibility at the microcode level with NMOS 8086 and 8088 devices, according to Harris. The new CPU has a 16-bit internal architecture linking with memories and peripherals via an 8-bit bus. I/O is TTL/CMOS-compatible. Static CMOS circuit design results in a maximum standby current of 500 $\mu$A while maximum operation current is 10 mA/MHz. This marks an 85 percent reduction in power dissipation over NMOS systems. Reduced size and battery-operated systems appear among the likely targets for this microprocessor—*J.V.*

## New supercomputer architecture features tens of billions of bytes

A Massive Memory Machine (MMM) is the latest innovation for a supercomputer architecture to handle memory-bound computations. According to proposers Hector Garcia-Molina and Richard J. Lipton of Princeton University (Princeton, NJ) and Jacobo Valdes of Imagen Corp (Mountain View, Calif), the machine would have a primary physical memory of tens of billions of bytes. With orders of magnitude above what is normally available in memory, the MMM would be ideal for applications where computations are simply memory bound. There, a classic von Neumann machine (even with a relatively slow 1 to 10 MIPS processor) could outperform developmental supercomputers and, as a bonus, be easier to program. Program development would be enhanced, the trio claims, because new programs written for the MMM would trade available memory space for running time. Of course, there are design problems—but a novel hardware and bus architecture now under study could lead to reduced memory access times, controllable costs, and minimal memory errors. Extensions to the machine would determine the best I/O mechanisms, virtual storage, programming language, and special processors. Among the applications: database machines, VLSI design, and artificial intelligence.—*H.H.*

## UP FRONT

### IBM lays cable for future token-passing LAN

To transmit data between remotely located electronic equipment within a building, a cable distribution network must be installed. Now IBM Information Systems Group (Rye Brook, NY) offers its own cabling system for its large base of office electronic equipment. Unlike Xerox's Ethernet, however, which requires a coaxial cable, IBM's cabling system uses data-grade twisted-pair wires that connect wall sockets to wiring closets. This makes for fairly easy connection for data and voice transmissions to both computers and PBXs. Computers are connected via patches at the wiring closets. This starwired system has twisted-pair cables fanning out from each of the closets that can hold up to 64 cables. Equipment is plugged into the network via special wall outlets. Both data and voice connectors can be installed, thus making a natural connection to PBXs. The cabling system is the backbone of IBM's token-passing protocol scheme for data transmission on a local area network, slated to be fully operational by 1986.—*N.M.*

### Will microprocessor cooperation agreement affect the NuBus?

Intel-backed Multibus II and Motorola/Signetics/Mostek-backed VMEbus devotees are already hinting (and NuBus advocates are saying no) that future versions of the Texas Instruments' NuBus will not be fully independent of National Semiconductor's Series NS32000 microprocessors. National and TI have joined forces (*Computer Design*, June 1, 1984, p 5) to make a name for themselves in the 32-bit microprocessor marketplace. For multiprocessing environments, NuBus has hurt its two competitors because it is said to be the most microprocessor-independent of the new breed of 32-bit buses. Whether or not TI will feel obliged to come up with a 32-bit bus specifically designed for the NS32000 remains to be seen. Unlike Multibus II and VMEbus, NuBus is a single, general purpose bus that uses reads and writes only to handle its data bits. It is too early to say if there is a better way for the NS32000—*H.H.*

### Lower dislocations add promise for GaAs ICs

Japan's Sumitomo Electric Industries, Ltd, has announced developments of a large dislocation-free liquid encapsulated chochralski (LEC) gallium arsenide (GaAs) crystal. Present GaAs dislocation rates typically measure 2000 to 10,000/cm$^2$. This vastly curtails their widespread use. The firm claims dislocations ranging from 0 to 200/cm$^2$, and foresees defect-free GaAs ICs sporting 100,000 devices/chip, as well as the possibility of accelerated GaAs production. Targeted for supercomputers and optoelectronic communications, the dislocation-free LEC GaAs FETs are expected in large quantities next year.—*J.V.*

### 'Tis the year of the single-user 32-bit workstation

Thirty-two seems to be the minimum bit number that allows a single user to work at a station and derive computational results equal to those of mainframe processing. Indeed, 1984 may well be the year of the 32-bit thoroughbred. In evidence at the National Computer Graphics Association Conference were 32-bit workstations from such companies as Ridge Computers (Santa Clara, Calif), Paragon Technology (Pleasant Hill, Calif), Perq Systems Corp (Pittsburgh, Penn), and Saber Technology Corp (San Jose, Calif). Most have communication options that allow single-user stations to share resources with other workstations and large computers in a manner similar to the Apollo and Sun Microsystems networks (see *Computer Design*, June 15, 1984, p 97).—*N.M.*

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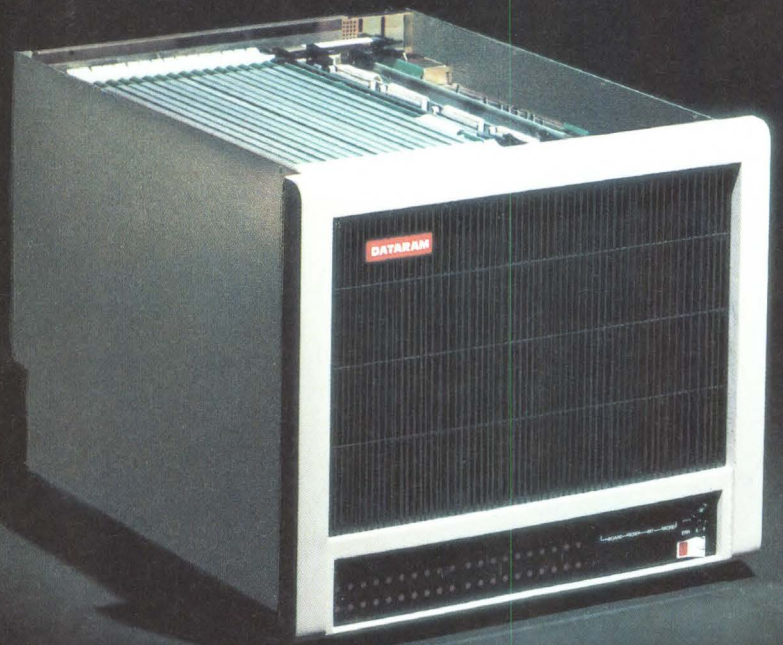


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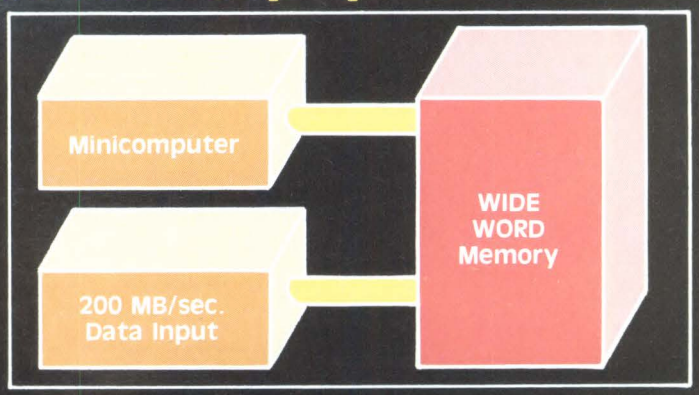


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CIRCLE 4

## UP FRONT

### Spreadsheets can aid computer designer in design as well as finance

VisiCalc, Perfect Calc, SuperCalc and some three dozen other microcomputer spreadsheets are often used by design managers for project monitoring and control, and "what-if" analyses. But design engineers are missing a bet if they do not use them as an aid in such chores as sinusoidal steady-state analysis, time-domain analysis, sensitivity calculations, and logic design. Recent work at the University of Arizona (Tucson, Ariz) by electrical engineering guru Lawrence P. Huelsman has shown that the ubiquitous spreadsheet—its paper form has been around since medieval Italy—is ideal for checking how the response of a design to an input will change as the design parameters change (the "what-if" function). Not only can output data be generated, but graphs can be plotted. Inexpensive spreadsheets offer self-prompting as well as organized structure design formats that need be set up only once. What is more, most spreadsheet analysis programs directly implement Boolean logic operations so that a variety of digital systems can be simulated. According to Huelsman, some spreadsheets like SuperCalc Version 1.4 even allow feedback circuits. Those that do not can be modified. It is even possible to simulate integrated circuits and their wiring.—*H.H.*

### Fall Joint Computer Conference to rise again

Bearing a familiar name, a new annual technical conference and computer equipment exhibition, entitled the Fall Joint Computer Conference (FJCC), has just been announced. It is the result of a joint agreement between the IEEE Computer Society and the Association of Computing Machinery (ACM). The first conference is planned for November 1986, with the site as yet to be determined. The two societies have a combined worldwide membership of over 125,000 computer professionals. Two representatives from each society will be appointed to serve as the FJCC steering committee. A joint news conference to be held during the July NCC meeting in Las Vegas will provide more detailed information about the new FJCC.—*J.H.*

### Unix-compatible operating system supports 11 users on IBM XT

Taking part in the trend to design microcomputer operating environments rather than operating systems (see *Computer Design*, July 1984), Network Consulting, Inc (NCI) (Burnaby, British Columbia) has come up with a realtime version of the Mark Williams Co (Chicago, Ill) Coherent operating system for the IBM XT. Unix Version 7-compatible (165 commands rewritten in assembler for faster execution), with System V memory routines, NCI Coherent supports an 8-line serial port card that, with the addition of two regular IBM serial lines, services up to 11 users. In short, NCI Coherent offers multi-user capability with Unix compatibility. Unlike Unix or its look-alikes, the license for the rewritten kernel operating system includes multi-users. This application-oriented operating system allows the XT to serve as a data multiplexer, protocol converter, network interface to IEEE 802 or 488 networks, database machine, or control processor. The latter functions are made even easier since the realtime operating system can run on intelligent peripheral boards; can be burned into PROM; and supports 11 different hard disks. With an eye to the needs of software developers and system integrators, the operating system also supports an IEEE-format math library, extra programming commands, screen editor, source code control system, lexical analyzer, compiler-compiler, Pro-Log interpreter for artificial intelligence applications, and the running of MS-DOS programs.—*H.H.*

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## The new Telex 9250 tape subsystem

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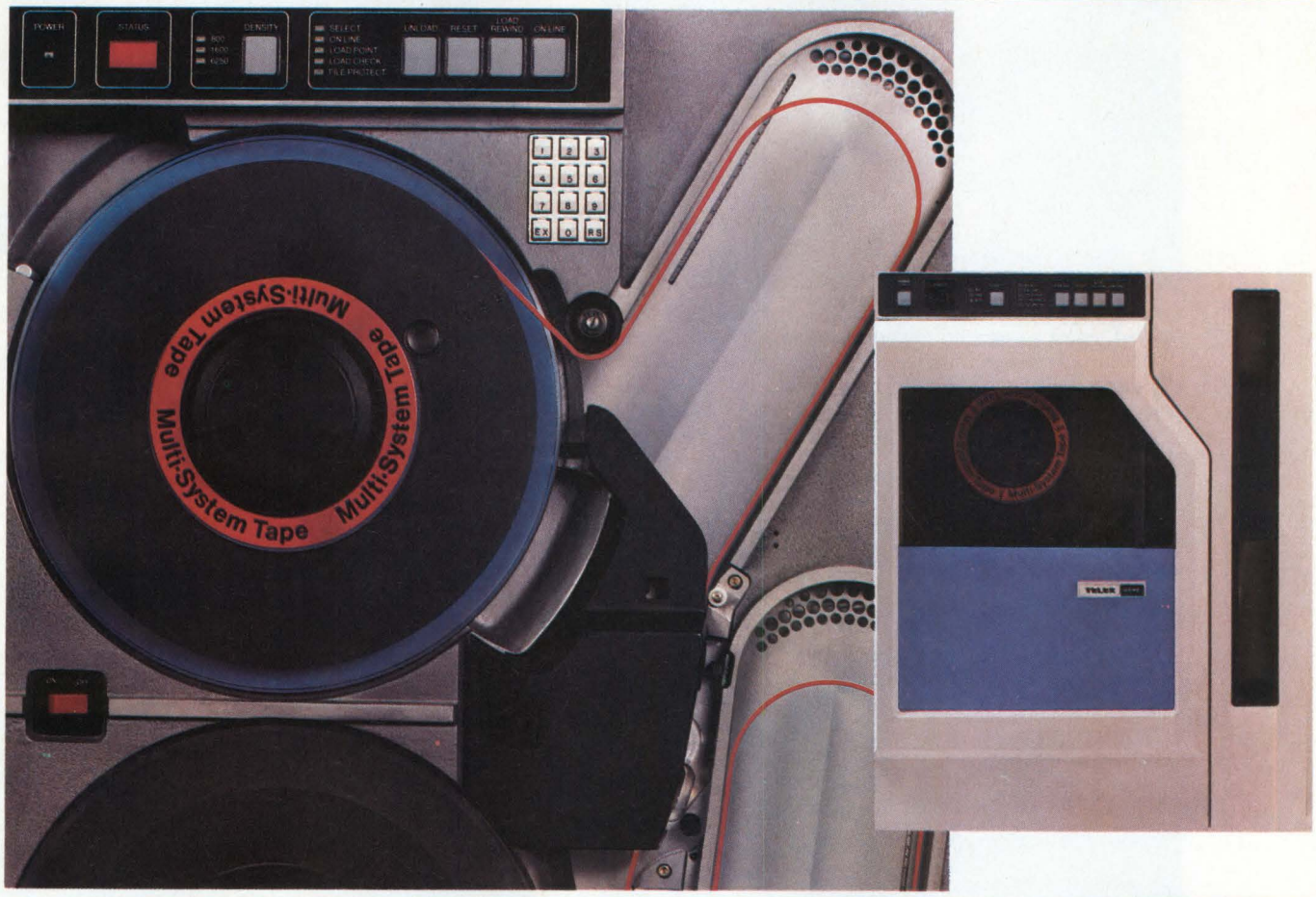


It took Telex to introduce a GCR subsystem with all the performance, all the reliability of larger subsystems — and make it affordable for minicomputer and mid-range mainframe manufacturers.

The Telex 9250 GCR tape drive is the first 50 ips unit to appreciably lower the cost of GCR without sacrificing performance. Advanced LSI gate array technology and vacuum column design offer advantages like low cost, low power and low noise (before offered only on old tension arm systems) — plus all the performance that only vacuum column technology can deliver, including . . .

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- Low maintenance

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CIRCLE 5

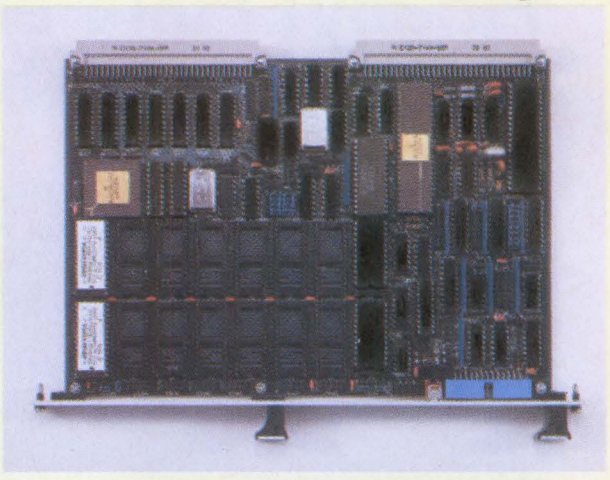
# Motorola's 68000 MPUs – the common systems from some of the industry's

**Callan Data Systems uses the 68010 because "it's the fastest, most advanced microprocessor available."**

"Motorola has established the 68000 product line as the **de facto** standard for the new generation of UNIX™ based super micro workstations and computer systems. Implementation of the chip on Callan's UNISTAR super micros is a perfect example.

"In the 16/32-bit UNIX-based microprocessor race, the 10 MHz virtual memory 68010 microprocessor, the heart of our UNISTAR 300 super micro, is the fastest, most advanced microprocessor available. It will remain one step ahead of the rest in the 16/32-bit UNIX microprocessor race."

Bill Pohlman, Vice President of Engineering, Callan Data Systems

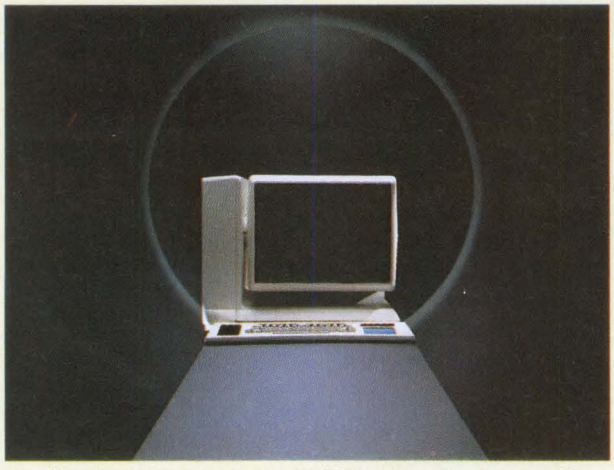


**Omnibyte uses the 68000 in the single-board computer market for its proven reliability and quality.**

"The single-board computer market that Omnibyte serves requires not only high performance, but also quality and proven reliability. For these reasons, Omnibyte chose the Motorola M68000 Family.

"The OB68K/VME1 incorporates the fast 12.5 MHz 68000R12. Its small-size, pin-grid array package allows room for more features on this sophisticated board-level computer."

Peter A. Czuchra, Marketing Manager, Omnibyte Corporation



**Apollo Computer uses the MC68010 as the heart of its DOMAIN DN300 to deliver mainframe-like CAD/CAE functions in a desktop unit.**

"Apollo's DOMAIN (Distributed Operating Multi-Access Interactive Network) is a high-performance local area network of dedicated computers operating in a distributed environment.

"The MC68010 microprocessor allows each Apollo DOMAIN to directly support virtual memory management in a network-wide demand paging environment. The performance and memory requirements of distributed CAD/CAE applications could only be satisfied with a design that incorporates microprocessors from the M68000 Family of devices.

Edward J. Zander, Vice President Marketing, Apollo Computer

**The Sun Workstation® uses the MC68010 to achieve superminicomputer performance.**

"The MC68010 is key to the architecture of our multi-purpose technical workstations. We designed a special no-wait-state memory to take full advantage of the speed of the 68010.

"The 68010's symetric instruction set and virtual-memory capability are the foundations of a cost-effective implementation of UNIX. And UNIX is key to Sun's commitment to industry standards in hardware and software."

Lloyd Fugate, Vice President of Marketing, Sun Microsystems, Inc.™

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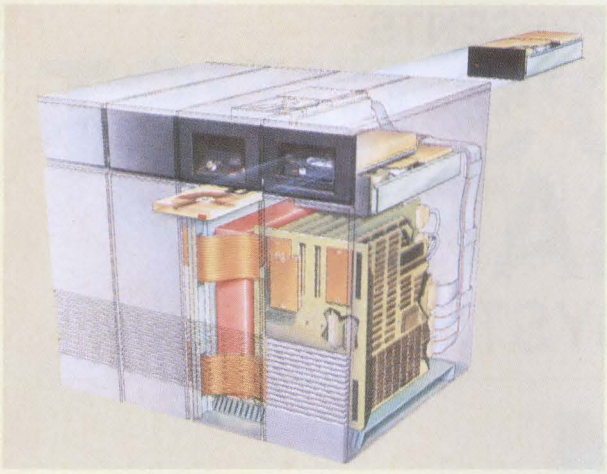
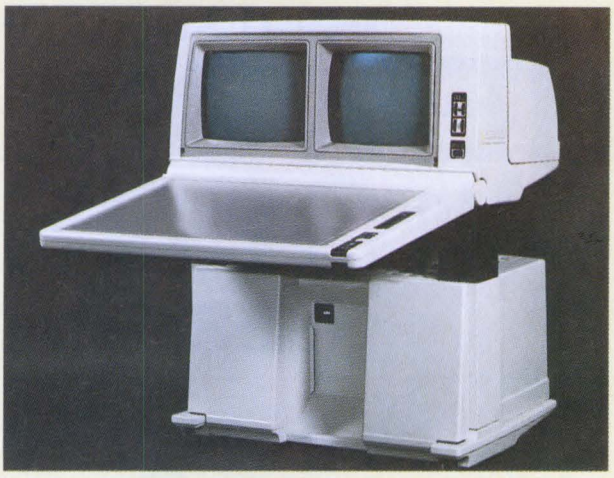


**Convergent Technologies uses the 68010 as the heart of its MegaFrame system.**

"The Motorola 68010, with its virtual memory, allowed us to build features typically found in mainframes and super-minis — features like demand page virtual memory — into our MegaFrame. So our MegaFrame is not a super-micro, it is a mini-computer, because of the 68010.

"Also, the 68010's linear address space is a real benefit for UNIX. We use up to 16 68010s in each system, all running on UNIX, all part of the 68000 architecture."

Steven Blank, Marketing Manager, Convergent Technologies

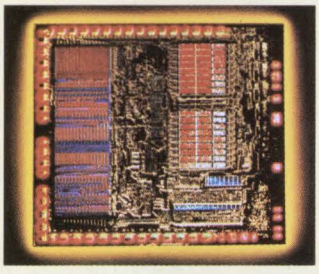


**Intergraph uses the 68000 for improved screen response and more workstations per host.**

"Creation of a screen image . . . is conducted up to three times faster than on a VAX-11/780.

"The MC68000 works with several Intergraph-designed processors to generate and manipulate graphic images locally . . . at the workstation. Offloaded of these burdens, the host computer is able to support many more workstations, such as executing database updates, running third party software and performing other background support tasks."

Bruce E. Imsand, Executive Technical Manager, Intergraph Corp.



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CIRCLE 7

# THE MARKET FOR COMPUTER GRAPHICS

Recently, a magazine aimed at advertising and marketing people asked me to write an article on the "vertical market for computer graphics." My initial impulse was to tell the magazine's editor that I was the wrong person for the job. The assignment seemed much more appropriate for someone from our sister publication, *Computer Graphics World*. After all, I thought, that magazine concentrates exclusively on computer graphics, while *Computer Design* covers the design of all types of computer systems. In the jargon of the publishing business, we have a "horizontal" audience, while they have a "vertical" one.

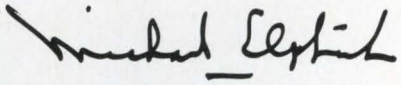
However, after doing some research and thinking things over, I realized that you, our readers, are really the key people in the computer graphics market. Several factors led me to that conclusion. Firstly, of course, graphics has become so pervasive that all types of computer systems (even inexpensive personal computers) offer graphics capability wherever it can be effective. Secondly, the largest application area for high resolution graphics is computer aided design and engineering—an area in which you are involved both as system designers and users. Thirdly, computer graphics is still in its infancy, and software standards are still being hammered out. Therefore, software has to be designed or specified by knowledgeable system engineers—the sort of people who read *Computer Design*. Last, but not least, high resolution graphics systems are expensive. So, their purchase must be authorized by management level people whose technical judgment can be trusted—in other words, by people like you.

Because you need to know how other engineers are coping and what's on the horizon, we devoted our May Special Report to a discussion of existing and proposed graphics standards. And, because you most likely have a dual involvement with workstations (both as designers and users), we used them as application examples in this issue's special report on designing with advanced microcomputers. Why then was I surprised to learn the importance of your role in the computer graphics market?

The answer to this question is simple. Because I am an editor and an engineer—not an advertiser or a salesman—I tend to think of technologies rather than markets. Of course, a technology (such as computer graphics) may also be an important market. But my viewpoint is different from that of our advertisers. I think of our readers as creative designers and problem solvers with specific information needs, not as potential customers in a market.

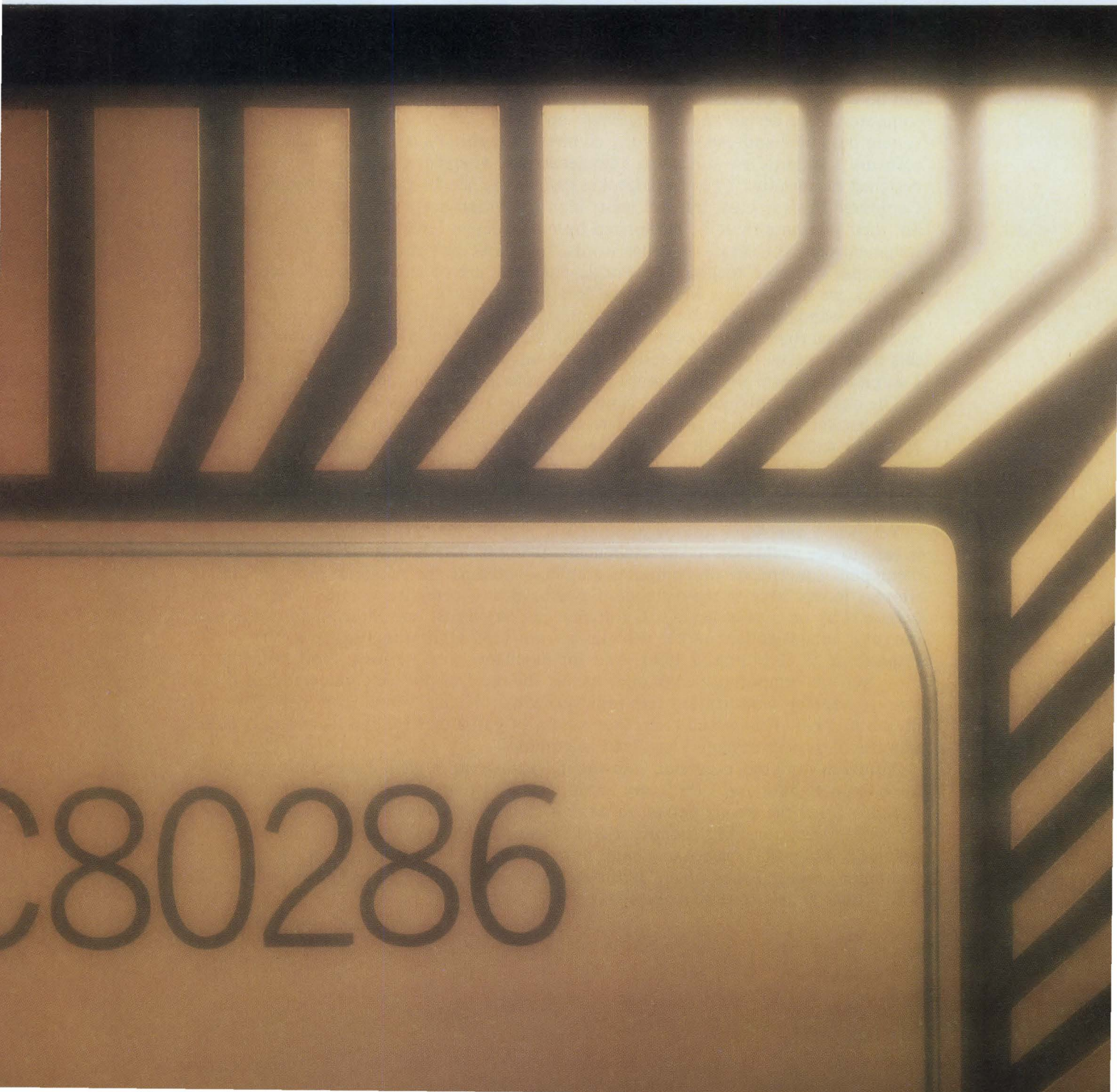
Yet, when one starts to look at computer graphics from a marketing viewpoint, it is easy to get caught up in the excitement. It is easy to see why so many startup companies concentrate on computer graphics—because the potential prize for the winners looms large in the distance. For all types of computer graphics workstations (which is by no means the entire graphics market), Frost and Sullivan forecasts that the total annual dollar market will climb from $335 million in 1983 to a very respectable $2.82 billion in 1990. And for intelligent workstations, those with the most built-in computing power and, hence, the most engineering value added, the market research organization sees rapid growth from just $65 million in 1983 to $1.03 billion in 1990. This would seem to ensure a bright future for the increasingly large number of system designers involved in graphics.

Although my brief excursion into the marketing realm gave me new insights into the computer business, I think my initial impulse was probably a sound warning. Perhaps I was the wrong person to write a marketing article—not because I work for the wrong magazine, but because it could give me the wrong perspective on the industry. After all, if too many engineers start to get excited about the markets for computer graphics, they might decide to become entrepreneurs and sales people. Then who would be left to design the systems?



Michael Elphick
Editor in Chief

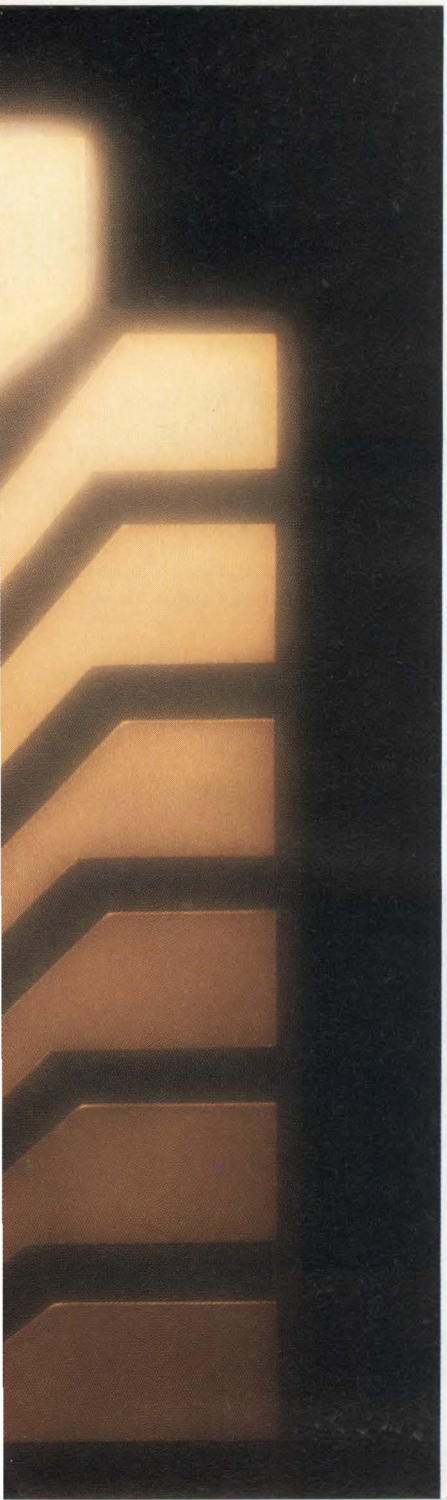
# MICROSOFT STRIKES GOLD.



This is what paydirt looks like when it's turned into silicon.

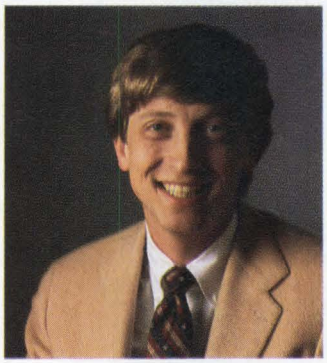
Intel's iAPX 80286 microprocessor.

Together, Microsoft and Intel used this gem to create another: the XENIX* 286 Operating System. The most powerful implementation of UNIX* on the market today for any microprocessor. And the most reliable, functional, commercial enhancement of the UNIX operating system ever created.



The XENIX 286 Operating System includes UNIX enhancements available from both AT&T™ and U.C. Berkeley. But Microsoft has also added loads of other commercial enhancements to make your life richer, in more ways than one. For instance, there are record and file locks, semaphores to help manage multiuser/multitasking data, and automatic disk recovery for better reliability.

Which makes XENIX 286 an ideal Operating System for applications software development. Over one hundred and fifty customized business software packages have been developed for XENIX, making it one of the most useable multiuser Operating Systems available today.



*Bill Gates, Chairman of Microsoft Corp.*

For Microsoft, the unique advantages of Intel's 80286 microprocessor were most appealing. As Bill Gates, chairman of Microsoft, said, "On-chip memory management and protection offered by the 286 ensures code compatability and makes it easy to port XENIX between different OEM systems."

In addition, its ability to run in fast 8086 mode makes the 286 the only processor that can support both XENIX 286 and MS-DOS without additional hardware. "With this ability, users get the best of both worlds in one piece of hardware," said Gates.

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CIRCLE 8

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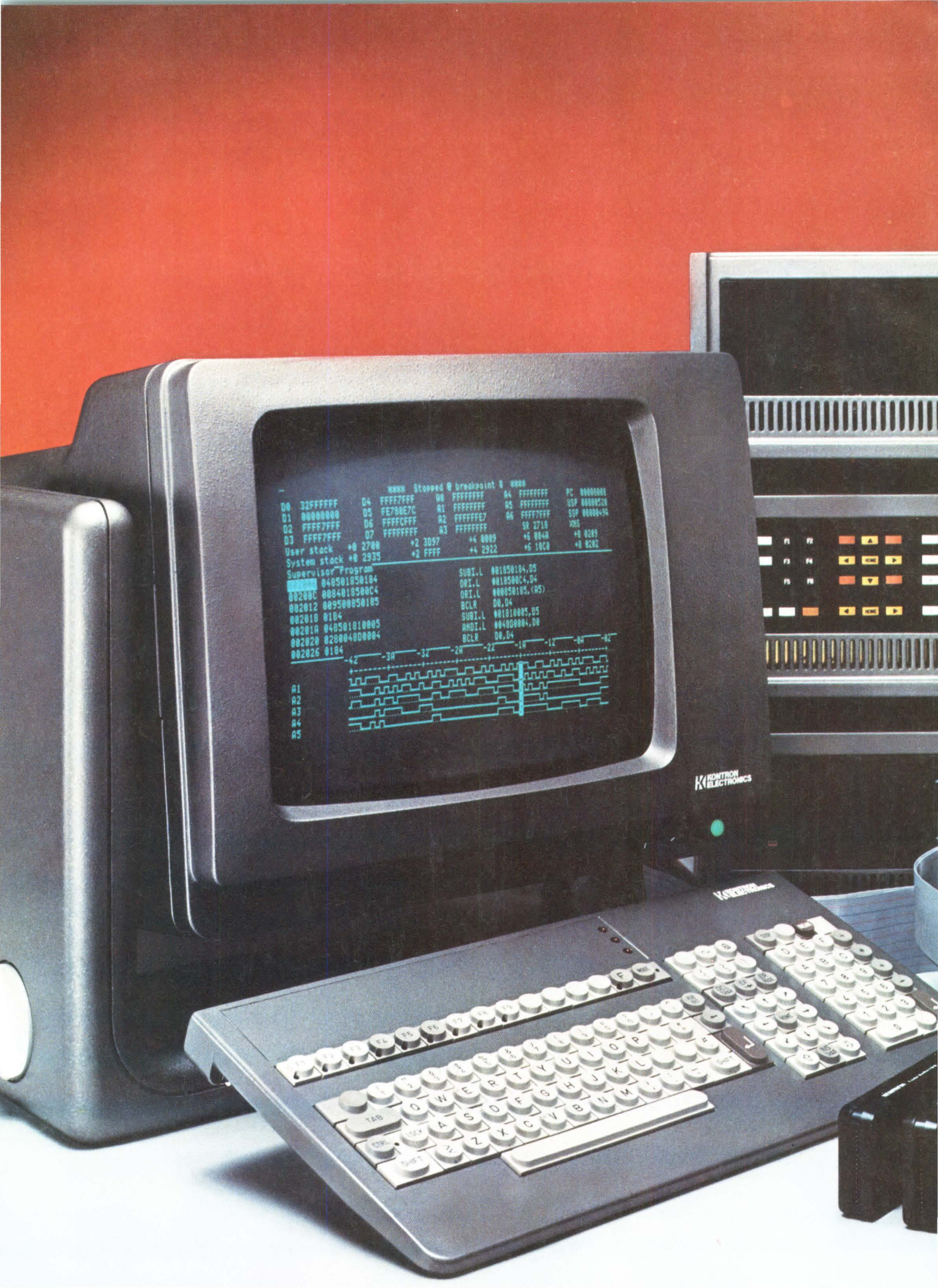
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**CIRCLE 13**

# Protocol analyzers take on functions to deal with network complexities

Communication networks, essential to virtually every computer installation, have recently assumed critical proportions. When AT&T relinquished its stranglehold on the communication business, it also gave up supporting individual installations. This has forced network operators to take on the task of network maintenance—an uncomfortable role for many. Accustomed to "one-stop shopping," operators must now, instead of simply calling the phone company, diagnose network disorders, as well as define the equipment at fault.

Add to these problems those created by the ever more complex networks, the proliferation of protocols and interfaces, and the shrinking store of skilled diagnostic personnel. The network environment is populated with a variety of vendors whose gear must communicate. While valiant attempts at standardization are underway, the available equipment still uses a confusing array of protocols that must be supported until those efforts yield fruit.

On top of all this, economic pressures are being brought to bear by the increasing costs of having a network go down. In crisis situations, losses due to outages can run to $1000 per minute. This demands that operator setup time and diagnostic time be kept to an absolute minimum. The result, when all of these factors are considered, is a tremendous need for sophisticated network diagnostic tools that can be quickly and effectively used, even in the hands of relatively unskilled personnel.

**Combining power with simple operation, the Simon 5 protocol simulator/monitor serves as a central console instrument or portable field unit. Diagnostics range from standard bit and block times to response time measurements on SNA cluster controllers.**

### Tools for troubleshooting

Equipment designed with these criteria in mind is emerging. Characteristically, it supplies sufficient intelligence and degree of programmability to reduce the skill level necessary to troubleshoot complicated networks. Operating at high speeds to match the trend toward higher speed networks, intelligent instruments also provide large amounts of data storage. This facilitates the isolation of problems by allowing repeated analysis of exactly the same data stream.

Specialized units such as response time analyzers, spectrum analyzers, and data line monitors, as well as network analyzers all serve in this complex arena. Each handles a single important element of the overall network function. Combining functions into a single intelligent piece of test equipment, protocol analyzers simplify the task of dealing with network complexity, whether charged with network maintenance or with aiding in the development of network software.

Designed for today's fast transmission speeds, the model 800 from Digilog Inc's Network Control Division (1370 Welsh Rd, Montgomeryville, PA 18936) looks to sophisticated software to handle bit-oriented multilevel protocols. In combination with smart hardware, this approach allows the relatively unskilled person to handle monitor and test functions, and provides seasoned operators with the tools to work more effectively.

Need for the sophisticated features displayed by this unit, and others of its type, stems from changes that have taken place within the communication field over the last several years. While data line monitors dating from the sixties established a window into the network, they were limited

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**Protocol analyzers**

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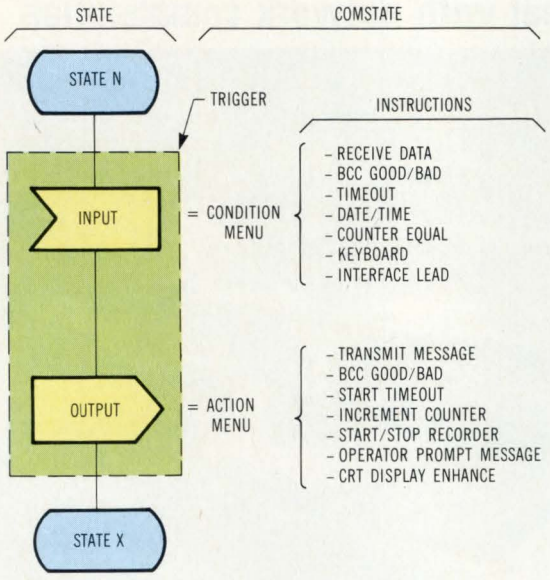


**Applying state definition techniques to data communication protocols results in an understandable method for documenting the protocol process. The Comstate technique uses input, output, or transition between states as a trigger to provide a high level programming approach to the problems of protocol diagnosis and emulation.**

to simple protocols and relatively slow transmission speeds. As line speeds increased, however, protocols also changed from easy-to-memorize character patterns to difficult to understand, bit-oriented multilevel protocols.

These challenges are met by designing intelligence into the diagnostic units. Thus, they can give the operator specific information detailing what went wrong with the protocol (whether character or bit oriented), as well as designate which device within the network created the problem.

Operating capabilities of Digilog's family of protocol analyzers encompass automatic setup, interchangeable electrically erasable PROM packs, and menu-guided operation, provided by the low end model 200 at transmission speeds to 19.2 kbits/s. Midrange units graphically display network interface timing at up to 72 kbits/s. On the high end, the model 800 can simulate high level protocols, memorize line performance, and display online statistics for lines operating at up to 256 kbits/s. The 10-Mbyte hard disk drive in this unit stores both programs and data off the line. Online statistics are displayed in color on its 10½-in. CRT.

**Simplifying protocol definition**

The programming process plays an important part in getting a tester to function in a specific communication environment. Recognizing the difficulty that programmers face in protocol definition, Atlantic Research Corp's Teleproducts Division (7401 Boston Blvd, Springfield, VA 22153) has provided tools to simplify that task. Based on a programming technique that facilitates protocol definition, the company's protocol analyzers enable programming to be done by less than high level programmers.

The technique applies state diagrams to protocol definition to provide an easily understandable means of documenting the protocol process and uses the concept of triggers as a high level programming approach. Defined as a protocol sequence—look for condition (input), take action (output), and/or transition to another state—triggers allow an operator to easily develop a test from a state diagram. Instead of trying to remember lengthy lists of instructions and their abbreviations, a user merely selects a desired input from a trigger condition menu and a desired output from a trigger action menu.

Embedded in the technique, as implemented in Atlantic Research's Interview Comstate protocol analyzers, are test development features that address and substantially eliminate unknowns. One is a display that summarizes details of up to eight triggers in a single state. Another display lists all states by name with a count of the number of triggers in each state. Using these displays it is easy to verify that the test parallels the state diagram definition of the protocol.

The technique provides, in every trigger, a descriptive prompt message that can print a record of the event. This allows the documentation required for network certification testing to be generated. The printout supplies a sequential record of each trigger occurrence and each state transition during test execution. The same state/prompt trace can also be displayed on the unit's CRT.

In addition, the Comstate II allows the use of up to 128 triggers in any state test, and up to 16 triggers in a single state. Testing requirements of X.25 networks are handled using mnemonic descriptions of receive and transmit frames and packets. This facility allows breakout of types, causes, and other extensions, while providing access to every bit. In SNA and BSC applications, the instrument can be used for host or network emulation, thus supplying diagnostic monitor tracing.

A portable unit that subscribes to the same general thesis, the Chameleon, from Tekelec Inc (2932 Wilshire Blvd, Santa Monica, CA 90403), uses a menu structure in conjunction with a simple programming language to

guide users through test setup. This is complemented with a help level that displays a detailed explanation of any term or feature.

Provision of multiple triggers allows data to be captured to the 16-Kbyte buffer or direct to the disk, which provides storage for 700 Kbytes of data. Analysis allows selective display of user-defined data from a prerecorded file. Selected data is displayed in full intensity, while all other data is visible in half intensity. Split-screen display enables both sides of a link to be studied simultaneously.

The multiprocessor architecture handles physical and link level on one processor programmed to handle HDLC, SDLC, Bisync, or transparent Bisync link access protocols. The second processor supports simulation packages that take care of higher level protocol procedures and data generation. A simulation trace in each package supplies simultaneous display of transmitted and received data. Trace packages provide display of a full interpretation of SNA and X.25 protocols. Traffic may be viewed live from the line or stored to disk for later analysis.

**Programming with soft keys**

Focusing on the shortage of skilled diagnosticians, the Simon 5 from Dynatech Data Systems (7644 Dynatech Ct, Springfield, VA 22153) builds on the menu approach used in the earlier DynaTest 1600. It adds soft keys, a help key, and removable hard disk to form a powerful, yet easy to use, protocol simulator/monitor. Each of four operating modes is accessed by pressing a single mode key. Standard menu selections include trapping, event counting, transmission testing, and bit-error rate testing. Once the format is chosen, the remaining parameters are automatically selected.

Menu mode pinpoints problems such as parity and block check errors, faulty addressing, and link initialization failures. Prestored menu tests accessed under protocol mode—monitor, event count, and BERT—are complete with operating parameters.

Programs to simulate and test virtually any protocol are built by simply selecting instructions on the soft key line of the display. Scroll mode searches captured data for specified pattern, event, or error. Data can be displayed in English or hexadecimal, compared to the interface status, checked for errors, or printed via the hardcopy port.

Programs are stored in up to 4 Kbytes of nonvolatile memory. These stored programs can interact either with data coming off the line or with data stored on the removable cartridge hard disk drive. Data rates range from 50 to 19.2 kbits/s internal. External clock rates can be 64 kbits/s full duplex. At this rate, 2 Mbytes of data and interface status can be stored on the disk. The internal buffer handles up to 8 Kbytes.

Packed in a portable 14-lb unit, the 4951A, developed by Hewlett Packard's Colorado Telecommunications Division (5070 Centennial Blvd, Colorado Springs, CO 80933), provides X.25 capability for testing sophisticated networks. Simulation capability allows detailed measurements to be made at physical interface, link level, and network levels. Success by relatively unskilled operators is assured by software driven keys.

These six software driven keys access the unit's troubleshooting capability, controlling the performance of network component simulation, data transmission monitoring, and bit-error rate tests. A single key—auto-configure—automatically determines line protocol, data code, speed, parity, and error checking. When combined with the other soft keys, the result is quick performance of complex tasks. Full benefit of the soft keys is realized in monitor and simulate menus. Here, the keys lead the operator through the measurements by presenting relevant choices at each decision point.

All data, timing, and lead status information is stored in the unit's 32 Kbytes of nonvolatile memory. An additional segment of memory provides storage for test setups and monitor and simulate programs. Data analysis, thus, can occur either in realtime or in post processing mode.

Whether designed for central site or remote use, instruments of this genre provide the tools necessary for network maintenance. Taking full advantage of the intelligent hardware and high level programmability, the units handle the complex protocols and diverse interfaces prevalent within today's networks. The high level of functionality available within a single instrument allows operators to not only detect problems within a network but to isolate faults to the piece of equipment responsible for them. Thus, the maintenance task is simplified not only by the level of function provided, but by the operator aids supplied through software.

*—Peg Killmon, Senior Editor*

**SYSTEM TECHNOLOGY**

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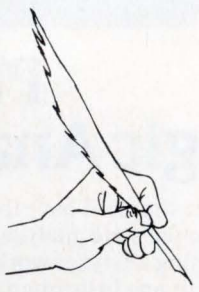


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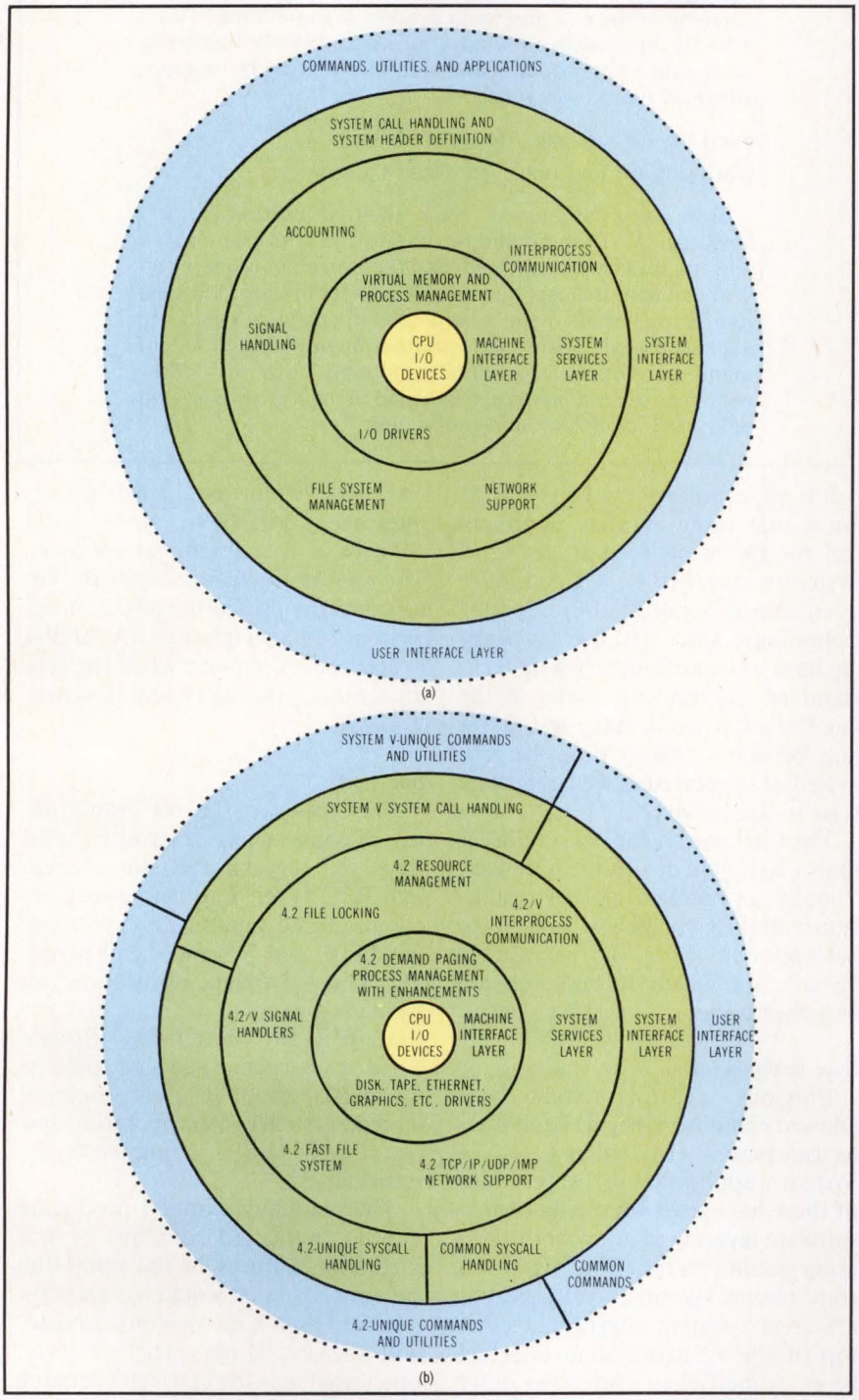
CIRCLE 14

# Dual-port operating system attacks Unix compatibility problems




**The classic Unix operating system is divided into layers that handle various machine, system, and user functions. Layers are isolated and communicate with calling conventions so software changes may be implemented modularly, and another system interface layer can be added on top of an existing one (a). With OSx, the system interface layer is split or segmented (b). Another system interface layer is not added.**

Both the University of California at Berkeley's 4.2 BSD Unix version and the AT&T Bell Labs' System V Unix have attributes that make them ideal for superminicomputer applications. But, they also have basic incompatibilities that limit how easily and efficiently application programs may be transported from one of these Unix environments to another.

Pyramid Technology Corp (1295 Charleston Rd, Mountain View, CA 94043) attempts to solve this incompatibility problem with its OSx operating system. This system was designed to be a compatible dual-port version of 4.2 BSD and System V Unix versions, without being just another Unix, according to Ross A. Bott, operating systems project manager for the company.

Bott claims that with OSx, one Unix environment, furnished by one of the ports and complete unto itself, can take advantage of the other environment. What is more, he adds, the OSx environment is ported on a 128-user, reduced instruction set, a 32-bit CPU, and 4 Gbytes of virtual memory address space. All this enables series 90x superminis to provide a gateway between networks using the two Unix environments.

OSx is also useful to the Unix community for other reasons. For one, as Bott said at January's Uniforum meeting in Washington, DC, OSx allows superminicomputer programmers to successfully develop programs in the 4.2 BSD environment, even if these programs will be run in the System V environment. The reverse is also true. According to Bott, superminicomputer programmers prefer the 4.2 BSD environment because its virtual memory support and file access mechanisms are superior to what is currently available in System V. It also has superior I/O performance and networking support. However, Bott admits that the upcoming enhancements in System V may possibly eliminate these differences.

*(continued on page 26)*

**Dual-port operating system**

*(continued from page 25)*

### Getting in and out

A program developer or another user determines the initial universe in the OSx operating system at log-in time. This is done by an entry in an /etc/u__ universe file maintained for each user. An alternate universe is obtained by entering either of two commands:

warp att (or just att)—to enter System V

warp ucb (or just ucb)—to enter 4.2 BSD

Both warp commands fork a shell within the alternate universe. A ^ D command returns to the original universe, and the universe command lists the universe in operation.

In addition, the user has the advantages of both Unix environments. For example, a command in one universe can be accessed while operating in another by prefixing that command with the prefix att or ucb. Inputs or outputs of different universe commands can be piped to each other with both wild card expansion and redirection.

It is important for the Unix user to know that some industry observers feel the battle between 4.2 BSD and System V may well be decided more by marketing clout than by superior technology. AT&T Bell Labs is pushing hard to make System V a *de facto* standard. In contrast, many of the key Berkeley people have left and it may be that 4.2 BSD will not be promoted or supported as well as System V or its successors.

The final reason for OSx's utility is that it is designed with the necessary "hooks" or pointers in place to allow future Berkeley or Bell versions to be incorporated. Thus, OSx can always be compatible with the latest version of either popular operating system.

**New design needed**

Previous operating systems have allowed computer designers and users to transparently run either 4.2 BSD or System V application software. Many of these have used what is known as software layering to allow both operating systems to function. However, conventional layering, such as putting a System V system interface layer on top of the 4.2 BSD system interface layer, is inefficient and slows down application program execution because of the additional software translation involved.

A 4.2 BSD operating system that wants to handle both 4.2 BSD and System V must make most of its software changes in the 4.2 BSD system interface level, with some lesser changes at the system service level. The former are drastic, while the latter concern new feature addition (eg, System V's semaphores). A similar procedure is followed when the fundamental operating system is System V based.

**Dual-port**

The OSx solves the overhead problem of conventional layering by splitting or segmenting the system interface layer into three parts—common call handling, 4.2 BSD call handling, and System V call handling. Thus, software connection can be made directly to the innards of the OSx. This approach helps alleviate performance penalty (which could be up to 50 percent in a conventional layered system) when operating system input data or commands are reformatted.

The company avoided producing another nonstandard Unix by not including features in the operating system kernel that would have accommodated both Unix versions. Instead, with the OSx design, program developers need only log in which operating system they prefer. Then, commands, libraries, header files, and system calls appear as expected. To do this, the OSx always pulls in the appropriate directory or command from the

*(continued on page 29)*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CIRCLE 16

### Dual-port operating system

*(continued from page 26)*

operating system that the user has specified. Only one version of functions that are identical in both systems is maintained.

Since the presently available version of 4.2 BSD has larger file blocking sizes, more efficient access algorithms and flexibile file names, in addition to the features mentioned earlier, it was chosen as the heart of the OSx. However, as OSx Product Manager David Gewirtz said, although the current 4.2 BSD is more suitable for running large superminis, if System V enhancements prove superior, it will be incorporated as the OSx heart.

### Inside story

The two separate 4.2 BSD and System V universes exist in the same file structure and share a common kernel. And, as mentioned, the directory structure for command binaries, libraries, and header files look exactly the way users of each universe expect. Moreover, there is compatibility with the shell files and other programs that make assumptions about where certain files are in directories.

These "two universe" features and capabilities are possible because the OSx operating system can implement conditional symbolic links. These links are similar to 4.2 BSD's normal symbolic links except that the directory or file to which the symbolic name points is dependent upon which universe is in use. Also, conditional symbolic links work as fast as the more conventional symbolic links and have little overhead penalty.

Conditional symbolic links allow separate underlying library and header directories that may be accessed at will. To do this, for each directory that needs to maintain different files or contents in each universe, a dual symbolic directory is established which contains the conditional symbolic links to each.

The Unix ls command is a good example of conditional symbolic link usage. This command's function is to list the files in a directory (/bin). The actual listing on the user's terminal differs in format depending on the universe in use. A specific format is expected when the file /bin/ls is executed. In the OSx, /bin/ls executes /.ucbbin/ls in the 4.2 BSD universe and /.attbin/ls in the System V universe. All this is user transparent and the conditional symbolic link amounts to a pointer to the specific command that corresponds to the current working universe.

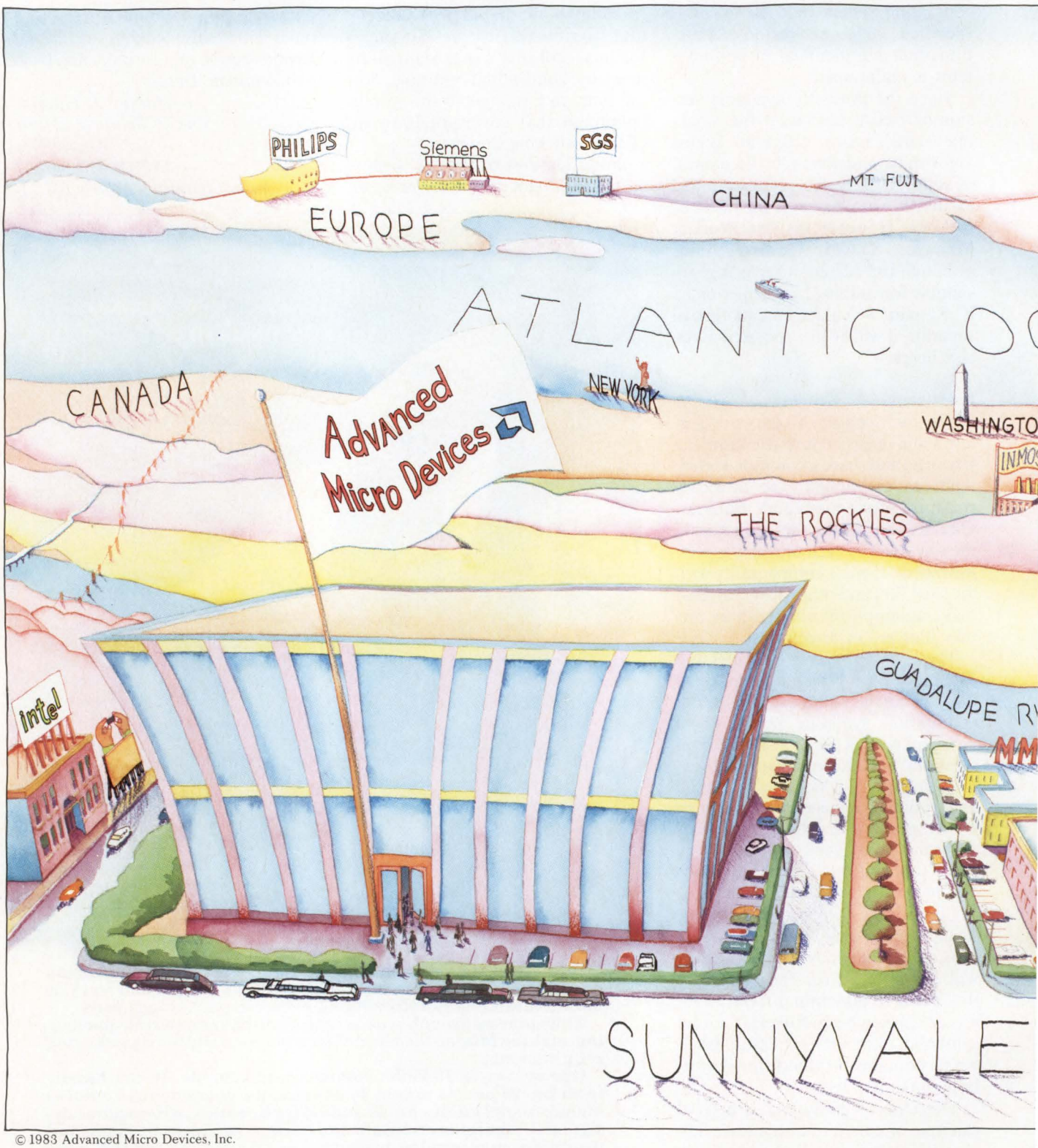
Other features of the OSx such as software development interfaces, signal processing, terminal drivers, and pipes will be discussed in the Special Report section of a forthcoming issue of *Computer Design*.

*—Harvey J. Hindin,*
*Special Features Editor*

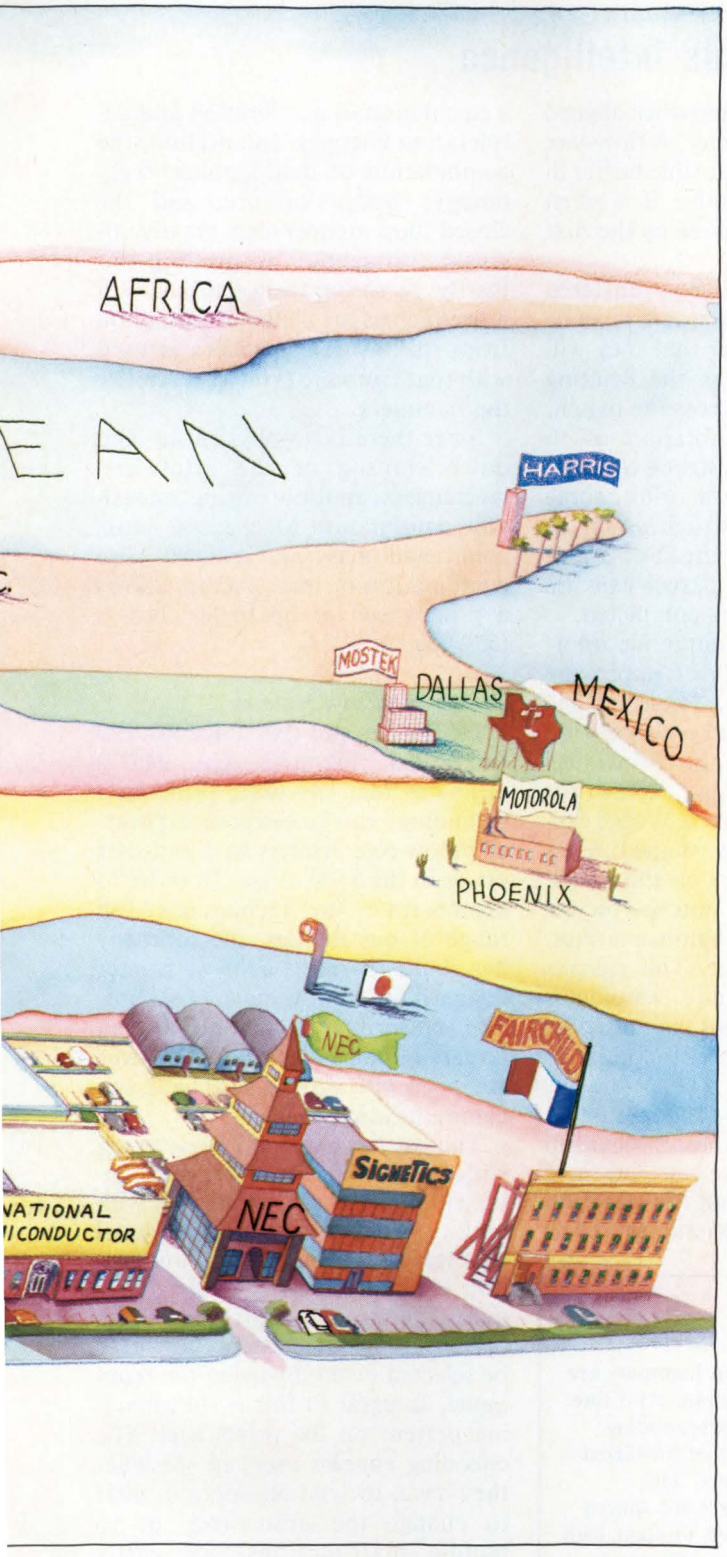
**SYSTEM TECHNOLOGY**

*(continued on page 32)*

# MEMORIES.



# A WORLD PERSPECTIVE.

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CIRCLE 19

# Printwheel technology ups speed, adds intelligence

A recent daisy wheel printing technology greatly reduces parts count, yet preserves the ability to print a 200-char extended character set on a single printwheel without shifting the carriage. In addition, the technology packages the plastic printwheel in a snap-in cartridge. This cartridge is encoded to let the printing system recognize the currently inserted printwheel.

### Opting for a dual-hammer technique

Extended character set (ECS) printing without physical shifting is done by using a dual-hammer technique. One hammer is used to print characters on the printwheel's outer circumference, while the second hammer strikes only those in the inner circumference. The hammers themselves are aligned with the print line, but the characters have a unique arrangement.

For example, the unshifted version of each character is located nine spokes ahead of its shifted counterpart on the wheel. When a given spoke is in the vertical position, the shifted character (in the inner ring) is aligned with the first hammer. At the same time, its unshifted (eg, italic, or alternate font) counterpart is aligned with the second hammer on the print line, but ahead of the first hammer's position on the paper.

The characters on the outer ring are tilted with respect to the line of the spoke. This ensures that they are upright on the print line when aligned with the second hammer. A firmware algorithm examines the line buffer in the printer to determine if a given character is to be printed by the first or second hammer.

Since the entire line is buffered before it is printed, characters can be arranged in the order that they will actually be struck as the printing mechanism moves across the platen. They do so with notation as to whether they will be struck by hammer one or two. As a result, some characters may be struck as far as nine print positions ahead of a previous character. But, all such gaps are filled in as the line is completed.

The printing technique incorporates several methods of improving speed and accuracy. These include position encoders and a closed-loop stepper motor for the printwheel mechanism, and wedge capture for the hammers and spokes. Wedge capture uses small wedge-shaped pieces behind the characters on the wheel, with corresponding notches on the hammers. When the hammer strikes, it captures the wedge. This ensures exact positioning and eliminates minute position variations caused by the settling of the wheel's motion, or by vibration.

The use of a closed-loop stepper motor for the printwheel mechanism allows a more precise calculation of wheel position (from information provided by the encoders), as well as a calculation of acceleration and deceleration energies. In addition, the combination of dual-hammer technology, wedge capture, and the closed-loop stepper can greatly increase throughput by printing on-the-fly. As the printwheel mechanism moves across the platen, information from its position encoders is used with that from the printwheel to fire the hammers.

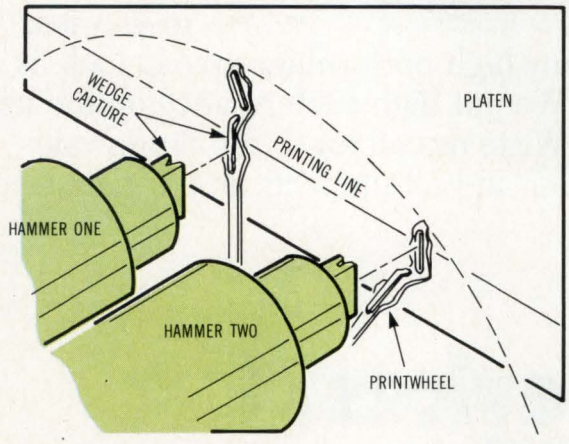
Since there is no physical up and down shifting of the printwheel mechanism, motion can be smooth and continuous. Mechanical parts count and mass are reduced. The combination of these factors allows a print speed of up to 80 chars/s (55 typical).

### Incorporating new features

Diablo Systems (901 Page Rd, PO Box 5030, Fremont, CA 94537) estimates that the basic printwheel technology can be easily incorporated in low cost printers with end-user prices in the $500 range. In order to demonstrate the technique's full range of possibilities, the company has built it into a new printer designed for networking applications. The 80IF printer is intended to run largely unattended and is thus equipped with various automatic and communication features.

The 80IF has a dual-bin sheet feeder with an envelope feeder, and a long-life ribbon. It can be equipped with multiple buffers or a 64-k optional spooler. Moreover, its communication capabilities let a remote user query the printer's status and select options to the same extent they could be selected onsite by using the front panel. Integral to this is the encoding present on the printwheel. The encoding enables users to see what they have, to send an operator alert to change the printwheel, or to handle malfunctions not easily resolved from a remote site.

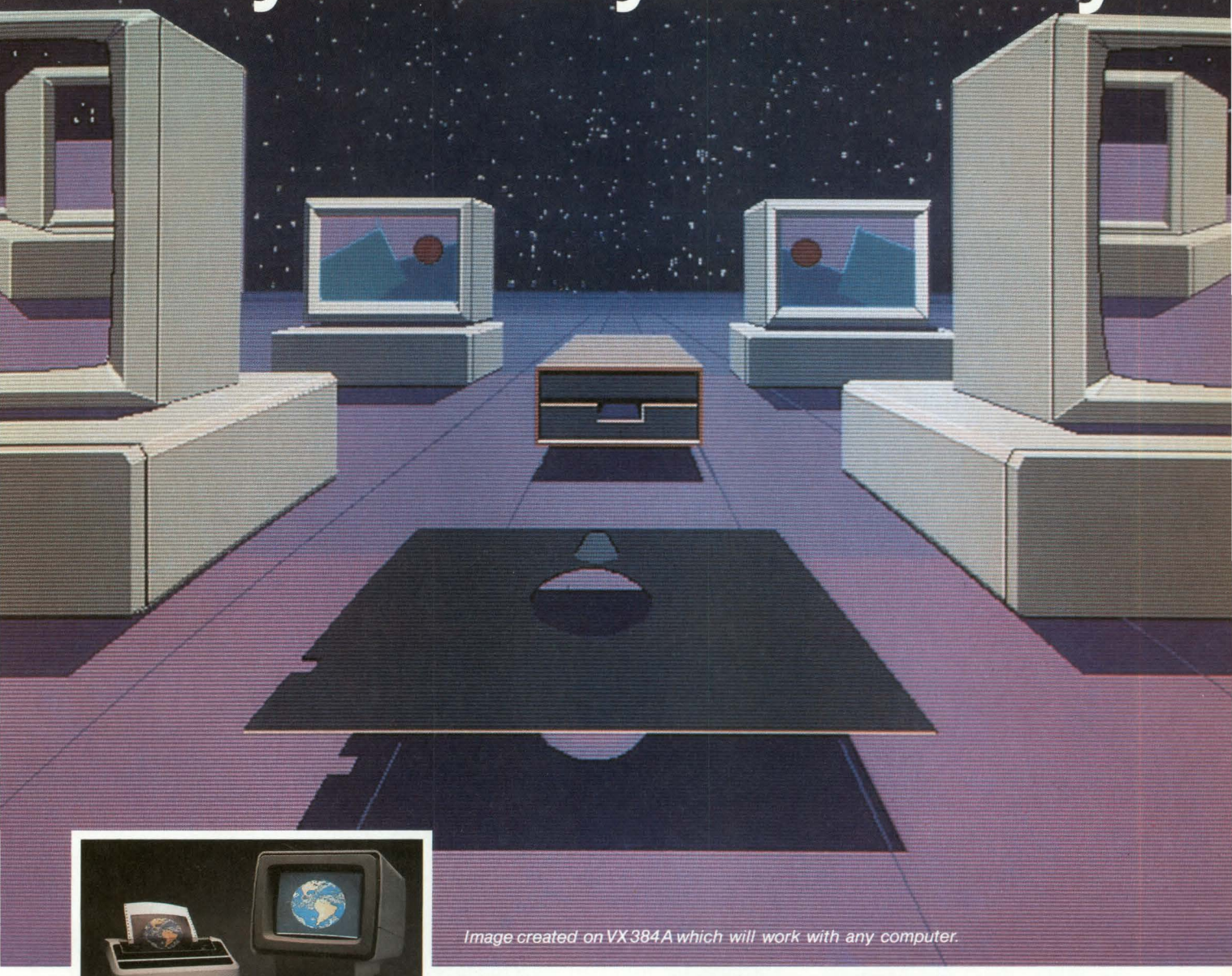
*—Tom Williams,*
*West Coast Managing Editor*




**The twin hammers are on the same print line with corresponding shifted and unshifted characters. The characters are spaced and tilted to align with the proper hammer. Notches in the hammers capture and align each character as it is struck.**

SYSTEM TECHNOLOGY
*(continued on page 34)*

# Vectrix has the graphics system for your next system. Already.





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**CIRCLE 20**

# The VMEbus to get larger slice of 16/32-bit board pie

Early in a project's life cycle, computer system integrators and designers must choose a bus and incorporate it into their workstations and computers. This bus of choice must, of course, be well suited to the realtime/interactive, commercial, and technical marketplaces these workstations and computers serve. Also, the microcomputer and peripheral board designers need to know the bus or buses for which they should design their boards.

Until now, there has been a lack of detailed projections about how the various buses will fare over the next few years. Also lacking have been analyses of who the major board manufacturers are, as well as their individual strengths and weaknesses.

**Microcomputer/Peripheral Board Market Growth**

| | 1983 | 1984 | 1985 | 1986 |
|---|---|---|---|---|
| Total board market | $350 million | $400 million | $490 million | $600 million |
| VMEbus sales | $30 million | $65 million | $150 million | $200 million |
| VMEbus market sales | 8.5 percent | 16 percent | 30 percent | 33 percent |
| Multibus market share | 60 percent | 50 percent | 40 percent | 30 percent |
| DEC Q-bus, BI market share | 30 percent | 30 percent | 30 percent | 30 percent |

### A new report

Those interested in this subject will be happy to hear that Zebu Corp (663 S Bernardo, Suite 222, Sunnyvale, CA 94087) has published proprietary investigations and a report about what the 16/32-bit board market will do in the next three years. Combining this report with additional statistical information from Dataquest, Inc (San Jose, Calif) and Ironoak, Inc (La Jolla, Calif) provides a first-class picture of what is going on with 16/32-bit board/buses and how new chip and bus technology affects them.

According to Zebu's president, microcomputer consultant Richard Main, the total board market will grow from $400 million this year to $490 million next year and $600 million in 1986. Main also says that the VMEbus's 16-percent share of this year's market will more than double, reaching 33 percent by 1986. Since Digital Equipment Corp's buses will stay at a 30-percent share in the same time period, it is Intel's Multibus and the planned Multibus II that will lose almost half of their market share. This reflects a drop from a dominant 50 percent this year to 30 percent in 1986 (see *Computer Design*, Feb 1984, p 27 for a bus update).

Main claims that market share trading and VMEbus growth is due to the appeal of the bus's Eurocard construction, as well as the scarcity of board and bus design, and production resources in general. He adds that the growing importance of standards is another factor leading to the growth of buses in general, and of the VMEbus in particular. For instance, asynchronous VMEbus is already an IEEE standard and synchronous Multibus II is being considered by the IEEE 896.2 synchronous bus committee.

The Texas Instruments just-introduced 16/32-bit NuBus is included in the 10-percent "miscellaneous" market share Zebu reports for 1986. The NuBus is the basis of TI's Nu Machine workstation and computer. It is also used by LISP Machine, Inc for its artificial intelligence-oriented Lambda machines that allow both Lisp and Unix in a workstation/computer environment. These machines include both the single-user Lambda machine, which has been on the market, and the full-function, two-user Lambda 2x2, which will debut on July 1 (see *Computer Design*, May 1984, p 5).

Both TI and LISP Machine have designed NuBus-based boards for their computers. Moreover, TI has designed a NuBus-to-Multibus converter board, enabling Nu Machine users to use any of the Multibus boards on the market. But, the NuBus has no other announced manufacturers using it, even though it has already been proposed as the basis for a synchronous bus standard to the IEEE 896.2 committee.

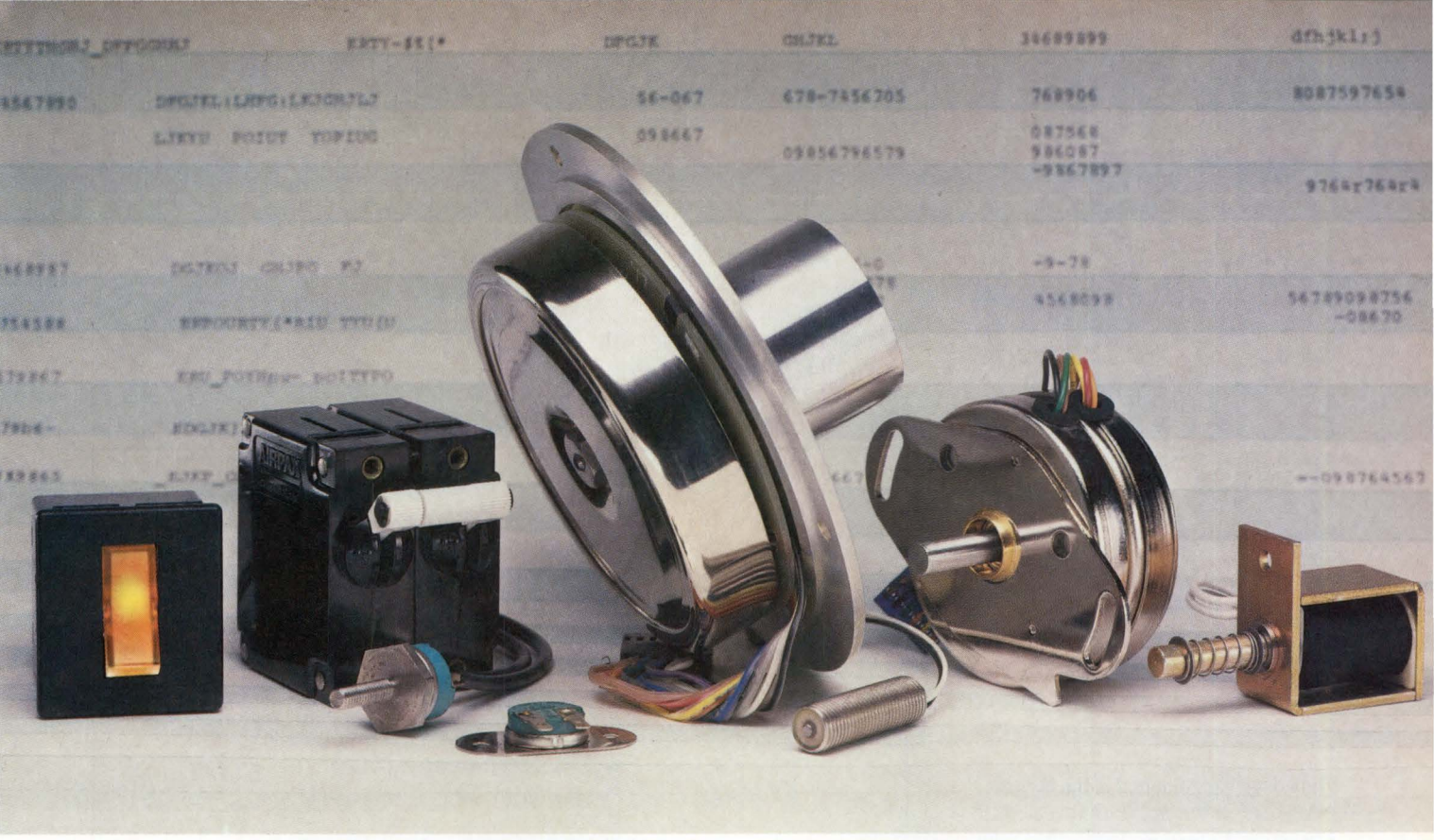
### Choosing between buses

The technical reasons for choosing between buses can be complex and, ultimately, only of interest to the experts. Intel (backing the Multibus duo) and the Motorola, Mostek, Signetics trio (backing VMEbus) have provided potential users with a variety of technical specifications, technical articles, and proprietary literature. The information stuffed into these can be compared and contrasted endlessly.

Ultimately, the judgements are subjective. Some users, for example, will not touch an asynchronous bus (VMEbus), while others will not deal with a synchronous bus (Multibus II). Many users are also arguing the merits of a multiplexed versus a non-multiplexed bus.

System designers, integrators, and board designers are more concerned with bus support and service, application software availability and variety, and vendor strategic alliances. Thus, DEC's Q-bus, Unibus, and BI buses will maintain their 30 percent market share because the firm is known for its support, service, and variety of application software. Its VAX architecture is a much-emulated computer hardware standard.

*(continued on page 36)*



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CIRCLE 21

**Predicting board market growth**

*(continued from page 34)*

**1984 VMEbus Market Leaders and Shares**

| Cost (in millions) | Manufacturers |
|---|---|
| $15 - $20 | Force Computers (mostly EEC) |
| $12 - $15 | Motorola Microsystems |
| $6 - $7 | Data-Sud (mostly France) |
| $4 - $5 | Philips Elcoma (strong internal use) |
| $1 - $3 | Astraea Computer (Signetics OEM) |
| $3 - $4 | UTC Mostek [Sys Tech (mainly EEC)] |
| $2 - $3 | Astraea Computer (Signetics OEM) |
| $2 - $3 | Xycom (one-quarter to one-half internal use in industry systems, Data-Sud OEM) |
| $1 - $2 | Signetics Microsystems (Astraea, Sigen OEM) |
| $1 - $2 | Plessey Microsystems (Force OEM and Licensee) |
| $1 - $2 | Mizar, Inc (mostly 100-mm boards) |
| $0.5 - $1.5 | Ironics Inc |
| Under $1 | Compcontrol BV, Wormald Data Systems, Micro-Sys (DEC-TEC), Sigen Corp, Graphics Strategies, Omnibyte Corp (mainly Multibus manufacturer), Sky Computers, miscellaneous (40+ companies U.S.A. and EEC) |

Estimated $65- to $85-million market in 1984 worldwide (boards only)

Intel's Multibus family also has its points. More vendors have been building boards to Multibus than VME and there is a wide variety of installed software. Likewise, there is the IBM PC connection. Intel's 8088 16-bit microprocessor can hook up to Multibus, and in turn, to the IBM name.

Several factors work in the VME's favor. First, it is associated with the 68000 (recognized as a superior machine to the 8088) through the Motorola connection. This processor is at the heart of most of the 16- and 32-bit workstations running the AT&T Bell Labs' Unix operating system. Unix is popular in today's multi-user, multitasking environment and it may even become popular for the single-user, multitasking environment that IBM's new Unix is bringing to the IBM-XT.

Second, strategic alliances behind the VMEbus need to be considered. For example, Motorola, Signetics, and Mostek are all producing chips to work with the bus (both on a primary- and secondary-source basis). And, Plessey in England, Philips in Holland (owner of Signetics), and Thompson CSF in France all favor the VMEbus.

**Not a good reason**

Motorola seems to have mixed feelings about the VMEbus being associated with the 68000. On the one hand, it enjoys the perceived benefits of the 68000 family and a tie to a specific bus. On the other hand, Motorola says that its VMEbus is processor independent and can work with Intel, National, Zilog, or AT&T Technologies microprocessors. Yet, Intel is fond of saying that Motorola's VMEbus is "only" 68000-oriented.

Of course, proponents of the VMEbus say that the Multibus is oriented toward Intel's 8080/8086 family. Intel disagrees, and points out vendors who supply other microprocessors with the Multibus. Motorola does likewise for the VME. Actually, smart engineers can make most any processor work with most any bus. It is just a matter of how expensive the microprocessor cycle overhead is and whether or not that matters. Ultimately, like everything else, it is a

*(continued on page 38)*

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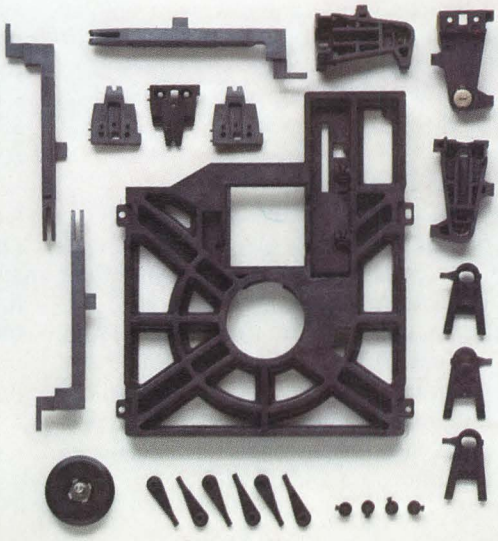

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CIRCLE 23

**Predicting board market growth**

*(continued from page 36)*

**1984 Multibus Market Leaders**

| Cost (in millions) | Manufacturers |
|---|---|
| $150 - $200 | Intel OMO |
| $30 - $36 | National Semiconductor |
| $8 - $10 | Central Data Corp |
| $7 - $8 | Xylogics |
| $6 - $7 | Advanced Micro Devices |
| $5 - $7 | Monolithic Systems |
| $4 - $6* | Zendex Corp, Interphase |
| $3 - $4 | Forward Technology |
| $2 - $3** | Omnibyte |
| $2 - $3 | Heurikon, Metacomp |
| $1 - $2 | Microbar |
| Under $2 | Bubble-Tec, Codata, Comark, Diversified Tech, Matrox, Pacific Micro, Plessey Microsystems, Chrislin, Micro Mem, Datacube |
| Under $1 | Eti Micro, Relms, Aim Tech, Burr-Brown |

The above figures do not include chassis, protocard, connector, power supply or other hardware items. Figures also do not reflect private and captive sales except Intel OMO sales are one-third to Intel ISO. *Includes NEC into Zendex. **Does not include VMEbus or other systems.

matter of preference. And, choosing the supplier of a particular board comes down to the supplier's perceived strengths and weaknesses. Here, Zebu's list is helpful. For example, it labels certain board manufacturers as famous for poor management and production, or says that they are strictly "me-too" operations showing no product innovation.

Designers trying to decide who to do board business with, whether they buy a VME-based or Multibus-based board, want to know who will be around in a year or two to support their products. One way to tell is to see who is doing well compared to other companies in the market.

**Who's doing what?**

Tabular material taken from Zebu's study shows the Zebu-estimated 1984 market leaders and their shares for both the VME and Multibus markets. In the second table, Munich, West Germany-based Force Computers leads the pack with more than $20 million in business. The firm has just opened a California office in Santa Clara and concluded a second-source agreement with Plessey Microsystems of Pearl River, NY. Motorola Microsystems in Phoenix, Ariz is second with a $65-million board market. Data-Sud of Montpellier, France accounts for third place with $7 million, and some seven other firms boast of over $1 million each.

Intel's Hillsboro, Ore operation dominates the Multibus market with a minimum of $150 million to earn in 1984 (one-third internal sales). National Semiconductor of Sunnyvale, Calif is a "poor" second with only a minimum of $30 million to gain this year. Central Data Corp of Champaign, Ill comes in third with an $8-million minimum and has a variety of competitors at its revenue heels.

As is the case with the VMEbus, a variety of other firms take care of the rest of the Multibus market. Some are giants in their own right and safe to deal with even if their particular bus market share is low. Others are not well known, or even unknown outside of their customer base.

*—Harvey J. Hindin,*
*Special Features Editor*

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## HP 4955A—increase your capability with top performance features.

With the HP 4955A you can bring your products to market faster, and with a greater level of reliability than ever before. Our datacomm-enhanced BASIC lets you program sophisticated test routines and perform high-level protocol analysis. Exercise your hardware and software as it's being developed, not after it's installed. Monitor, simulate, and trigger from 50 bps to 72 kbps. You can easily identify protocol problems at the physical interface, frame, and packet levels using the HP 4955A's multiple display formats. Plus, our intelligent 256K byte buffer memory increases real data storage by eliminating line idles without sacrificing timing information.

## HP 4951A—"instant" productivity.

The HP 4951A features advanced one-button autoconfiguration which easily does the setup work for you and gets you monitoring data quickly on-line. Like the HP 4955A, it gives you 63 simultaneously active triggers for extensive testing. In post-processing mode, you can do detailed repetitive analysis for hard-to-track errors. You can trap on characters, error conditions and lead transitions. To isolate problems down to the network component level, BERT mode lets you measure bit errors, block errors, errored seconds, and percent error-free seconds. You can simulate a CPU, modem, terminal, or group of terminals for complete interactive testing. The HP 4951A accommodates most popular protocols, data codes, and speeds (to 19.2 kbps).

For more information on the HP 4951A and HP 4955A protocol analyzers, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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3801401

CIRCLE 25

# In 64K DRAMs, INMOS high performance and flexible ...including 8K x 8.


Look to INMOS for a wide selection of 64K DRAMs. We offer access times from 100ns. By-1, by-4, and by-8 organizations. Plus features that boost performance and simplify design. This is the family that lets you avoid compromises by giving you the performance and organization you want...at costs you can afford.

**8K x 8 — The cost and space saver.** This newest member of the INMOS 64K DRAM family, available in a plastic package, offers access times of 120 and 150ns. The by-8 organization is a natural for microprocessor designs and other applications that require word width rather than memory depth...in process controllers, intelligent terminals, and buffer memories for example. And its pin 1 refresh makes it a very attractive alternative to 8K x 8 static RAMs. Because it combines low power and low cost with minimal support circuitry.

**16K x 4 — The performance chip.** With 100, 120, and 150ns access times, this organization makes a lot of sense in high-performance systems, such as high-resolution graphics, where high data rates are required. Packaged in plastic DIPs, the IMS2620 also gives you the right combination of cost, organization, and speed for microprocessor systems, terminals, and even arcade and home games. If you're upgrading from 16K x 1 chips, it provides a factor of four reduction in chip count. And its "$\overline{CAS}$ before $\overline{RAS}$" refresh assist function minimizes required support circuitry for cost and space savings.

**64K x 1 — The big-system choice.** This DRAM also gives you a choice of 100, 120, and 150ns access times. What's more, it includes "Nibble Mode," which allows effective cycle times below 85ns. Available in a variety of packages, including plastic DIPs, ceramic DIPs, and chip carriers, it's ideal for systems requiring lots of memory depth.

**Check the chart.** You'll find the industry's broadest family of 64K DRAMs...and the right device for your requirements. Then call an INMOS distributor for all the details.

| Organization | Access Time (ns) | Cycle Time (ns) | Part No. |
|---|---|---|---|
| 8K x 8 | 120 | 190 | IMS2630-12 |
| | 150 | 240 | IMS2630-15 |
| 16K x 4 | 100 | 160 | IMS2620-10 |
| | 120 | 190 | IMS2620-12 |
| | 150 | 240 | IMS2620-15 |
| 64K x 1 | 100 | 160 | IMS2600-10 |
| | 120 | 190 | IMS2600-12 |
| | 150 | 230 | IMS2600-15 |

**INMOS Distributors:** Anthem Electronics, Arrow Electronics, Falcon Electronics, Future Electronics, Lionex Corp., RAE

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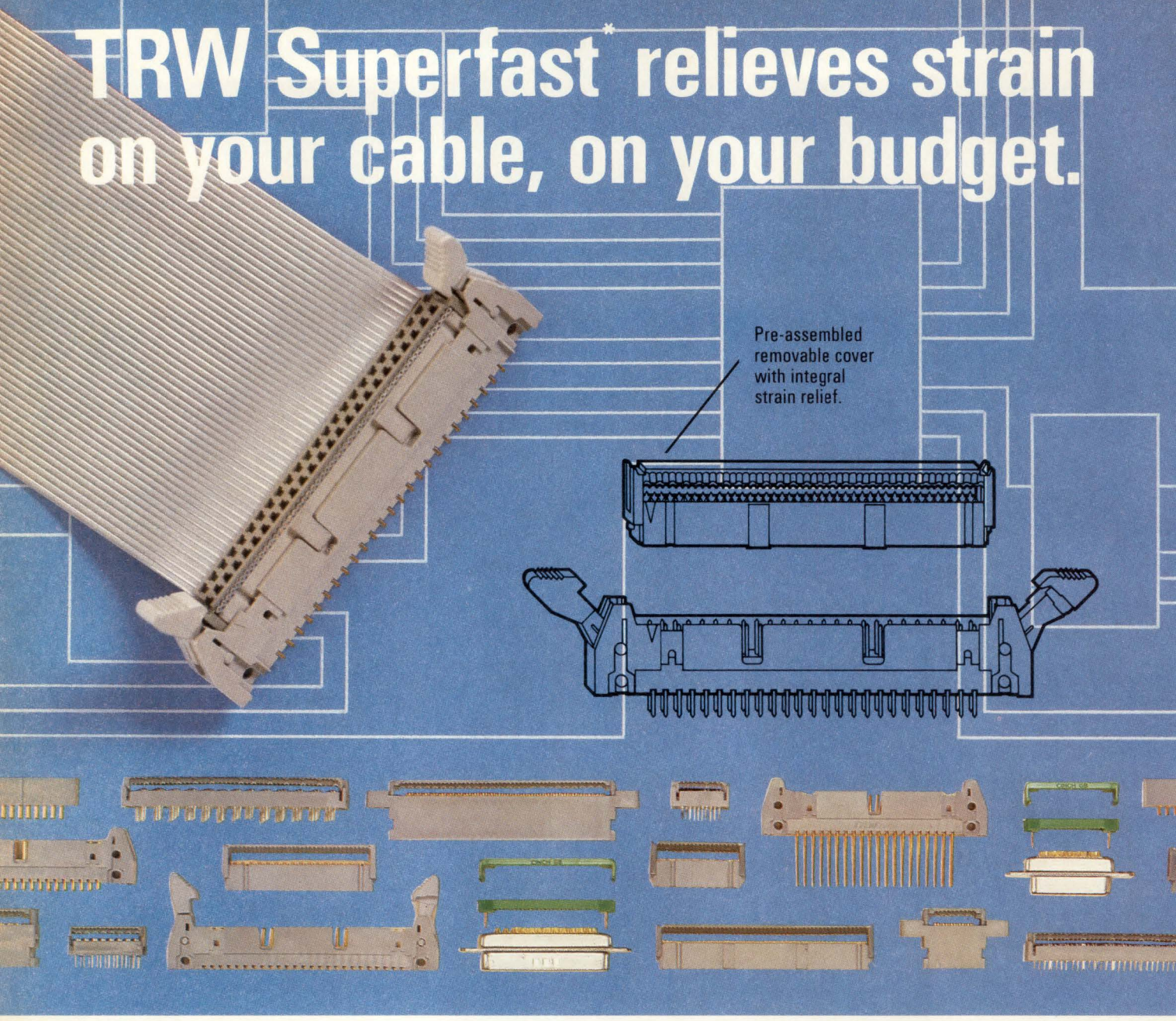
CIRCLE 26

# means organizations

# TRW Superfast* relieves strain on your cable, on your budget.




## Specify TRW Superfast Flat Cable Connectors

This is the flat cable mass termination interconnect system that's designed to relieve strain in every way.

The cover/strain relief is pre-assembled as an intergral part of the connector. So you're assured of effective cable strain relief without extra parts to buy or assemble. And one, simple, snap-action operation puts it in position.

TRW Superfast connectors are just as easy on your budget. Low prices to begin with. More density because of the lower profile of the overall package height. And the Superfast design requires less cable, less labor and reduces space requirements when used in a daisy chain mode. Superfast even meets MIL-SPEC requirements.

All this is part of the Value Engineering that TRW built into every Superfast Flat Cable Connector. It also includes features like an exclusive one-step insulation displacement contact system with a unique contact design for high reliability connections.

And you can get all the connector sizes and types you need in the Superfast system. More important, you can get fast, off-the-shelf delivery from the TRW Connector distributor network—the best in the business—to prevent strain on *your* commitments.

For more information on the Superfast Flat Cable Connector System, contact your TRW Electronic Components Group sales office, or see your local TRW Connector Distributor. Or write: Connector Division, TRW Electronic Components Group, 1501 Morse Avenue, Elk Grove Village, Illinois 60007. Phone 312.981.6000.

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TRW

**Connector Division**
TRW Electronic Components Group



**CIRCLE 27**

# SIGGRAPH '84

## Conference on Computer Graphics and Interactive Techniques

**Minneapolis Auditorium and Convention Hall**
**Minneapolis, Minnesota**
**July 23 to 27, 1984**

Just a few short years ago, computer graphics was essentially a stepchild of digital technology, without a status of its own. (Remember when monochrome line representations were state-of-the-art?) Today, computer graphics exerts an especially strong influence on all other phases of digital technology. Not only has computer graphics matured to full-spectrum color, representation capabilities have more than kept pace. System designers must now remain fully aware of computer graphics technology—where it is today and, even more important, where it will be tomorrow.

**Courtesy: Henderson and Agnis Kaugars, Geometric Productions (Geopro), Berkeley, Calif.**

SIGGRAPH '84, the Eleventh Annual Conference on Computer Graphics and Interactive Techniques, is representative of the growth and maturity of the industry. As in previous years, the 1984 conference is based on the need to share information with those who can put it to use.

This year, SIGGRAPH is divided into five basic segments: technical program, courses, design arts show, electronic theater, and vendor exhibitions. Although these segments vary in importance depending on the individual attendee's interests, each serves a legitimate purpose in the overall conference.

The technical program is divided almost equally into paper presentation and panel sessions (see pp 47 to 52). In all, 10 paper presentation sessions will cover such diverse subjects as modeling, hardware, visible surface algorithms, ray tracing, interactive systems, shading and texturing, and graphics standards. Emphasis will be on technology of the future rather than what has come out of the past. Most papers will stress broad technology instead of specific applications.

The panel sessions will present more general coverage of technology, as well as concepts for the future. For example, one panel will deal with Japanese computer integrated manufacturing (CIM). Chaired by a staff member of the University of Tokyo, this panel of speakers from Japanese companies will cover the current status of CIM, including computer aided design (CAD), computer aided engineering (CAE), computer aided manufacturing (CAM), and computer aided testing (CAT), as well as flexible manufacturing systems (FMS).

A related panel will describe the extensive research being done on computer graphics in Japanese universities. Other panels will discuss the influence of super computer systems on computer graphics, storage and retrieval of integrated graphics and text, graphics standards, microcomputer graphics, and development of semiconductor hardware.

This year a wide range of courses will cover four basic divisions: general, visual synthesis, CAD/CAM/CAE, and applications (see map on p 52). The general group includes such subjects as color perception, raster graphics, computer interfaces, and the Graphical Kernel System (GKS) graphics standard. In the visual synthesis group are animation, image synthesis, bitmap graphics, and mathematics.

The CAD/CAM/CAE group includes such diverse subjects as robotics, solid modeling, freeform curves and surfaces, and VLSI. Within the graphics applications segment are interdisciplinary issues, distributed graphics systems, and scientific/engineering considerations.

Indicative of what can be expected at the design arts show are the illustrations

*(continued on page 45)*


# New Qantex 7065.
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No matter how heavy the traffic, our new Qantex 7065 multimode printer will keep your documents flowing smoothly. At a very affordable price.

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CIRCLE 28

*(continued from page 43)*
reproduced with this discussion of SIGGRAPH '84 Approximately 35 architectural, industrial, and visual communication design projects will be exhibited. Each project will be an example of significant applications of computer technology. (After this conference, the exhibit will travel to cities in North America, Europe, and Japan.) The design arts show will be presented at the Minneapolis College of Art and Design from 9 am to 5 pm from Sunday, July 22 through Saturday, July 28.

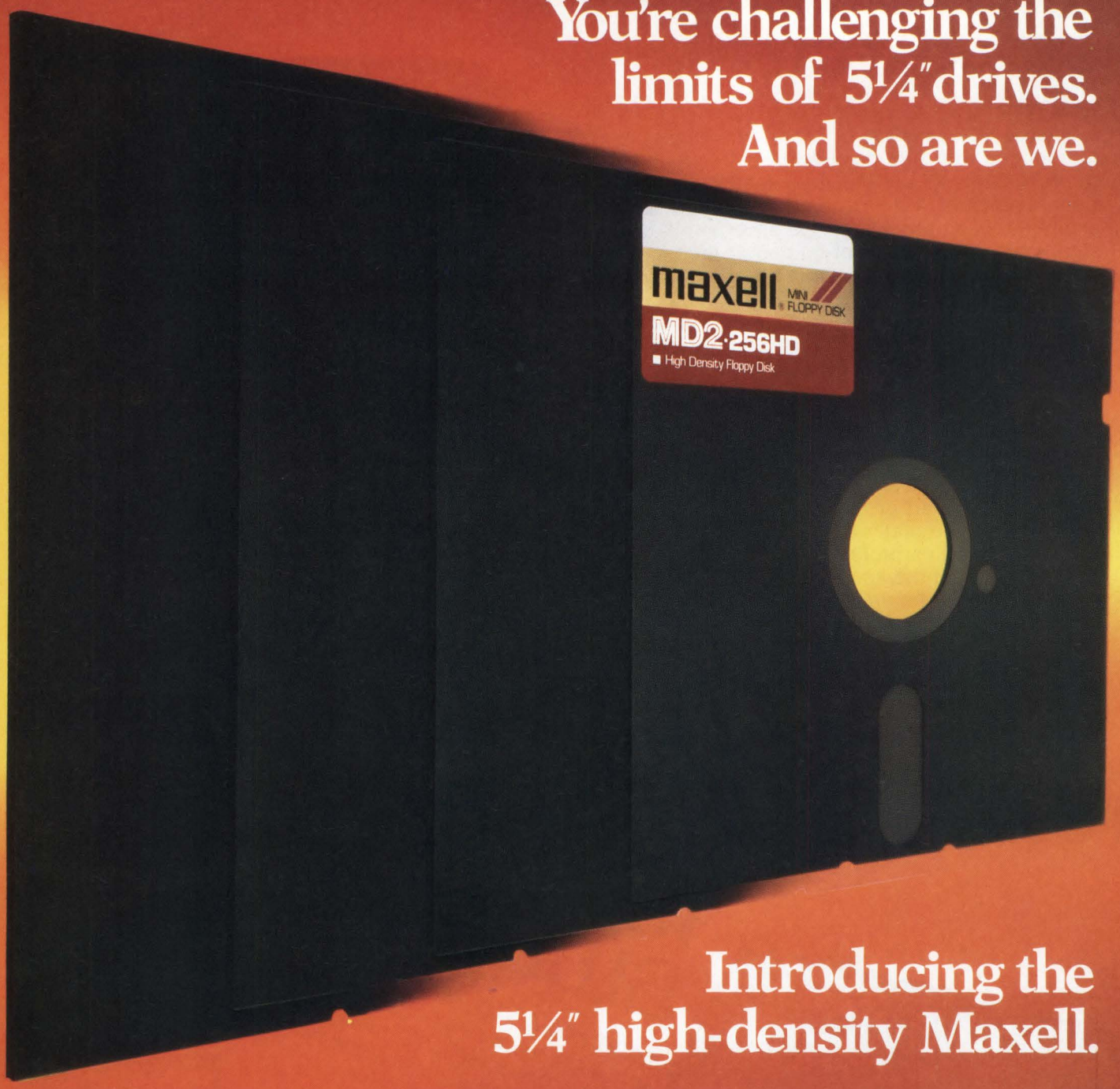
Unlike many of the "movie" theaters regularly provided at conferences, which allow attendees to nap a bit without seemingly violating their companies' trust, SIGGRAPH's electronic theater will be a basic part of the conference. According to the preview literature, experienced computer graphics professionals will select four hours of state-of-the-art computer-generated film and video presentations from a long list of submissions. Final staging and sequencing will be completed by a committee of audio and visual artists and experts. The theater will be divided into two evening events, on Tuesday and Wednesday, in the auditorium arena.

Portions of the vendor exhibition will include representatives from most of the graphics-related industries. For example, there will be CAD/CAM/CAE, image processing, display systems, hardcopy devices, input devices, software, workstations, and other OEM products. And of course, within this group will be related publications and magazines—including *Computer Design,* whose covers are an example of how computer graphics has developed. (Compare *Computer Design* covers from its first use of computer graphics in December 1980 through this latest issue.)—*S.F.S.*

SIGGRAPH '84 is sponsored by the Association for Computing Machinery's Special Interest Group on Computer Graphics in cooperation with other groups, including the IEEE Committee on Computer Graphics. For further information, contact the SIGGRAPH '84 Conference Office, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

*(continued on page 47)*

# You're challenging the limits of 5¼" drives. And so are we.

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CIRCLE 30

(continued from page 45)

## Technical Program Excerpts*

All paper presentation sessions will be held in the Minneapolis Auditorium and Convention Hall arena. Panel sessions will be held in the Nicollet and Greenway Ballrooms of the Hyatt Regency Hotel.

### Wednesday, July 25

**10:45 am to 12:15 pm**

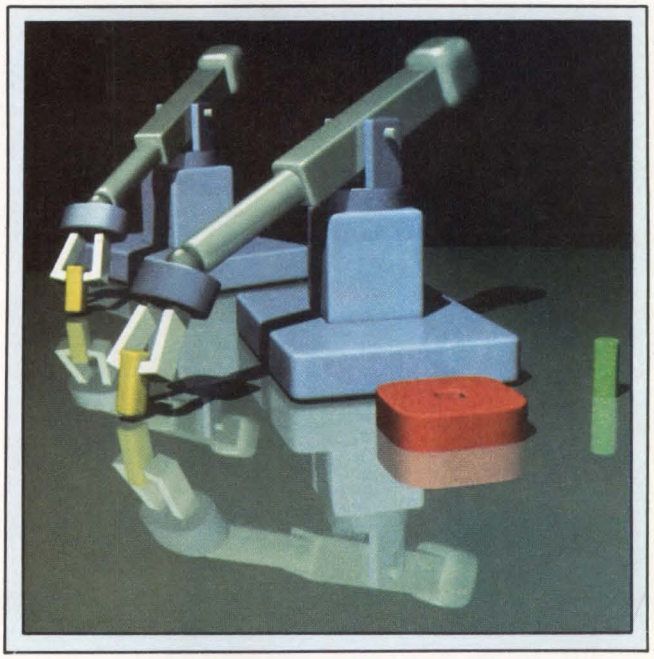
**Papers: Modeling I**

Chair: Dick Gordon, Univ of Manitoba

"Plants, Fractals, and Formal Languages"
Alvy Ray Smith, Lucasfilm Ltd

"Simulation of Natural Scenes Using Textured Quadric Surfaces"
Geoffrey Y. Gardner, Grumman Aerospace Corp

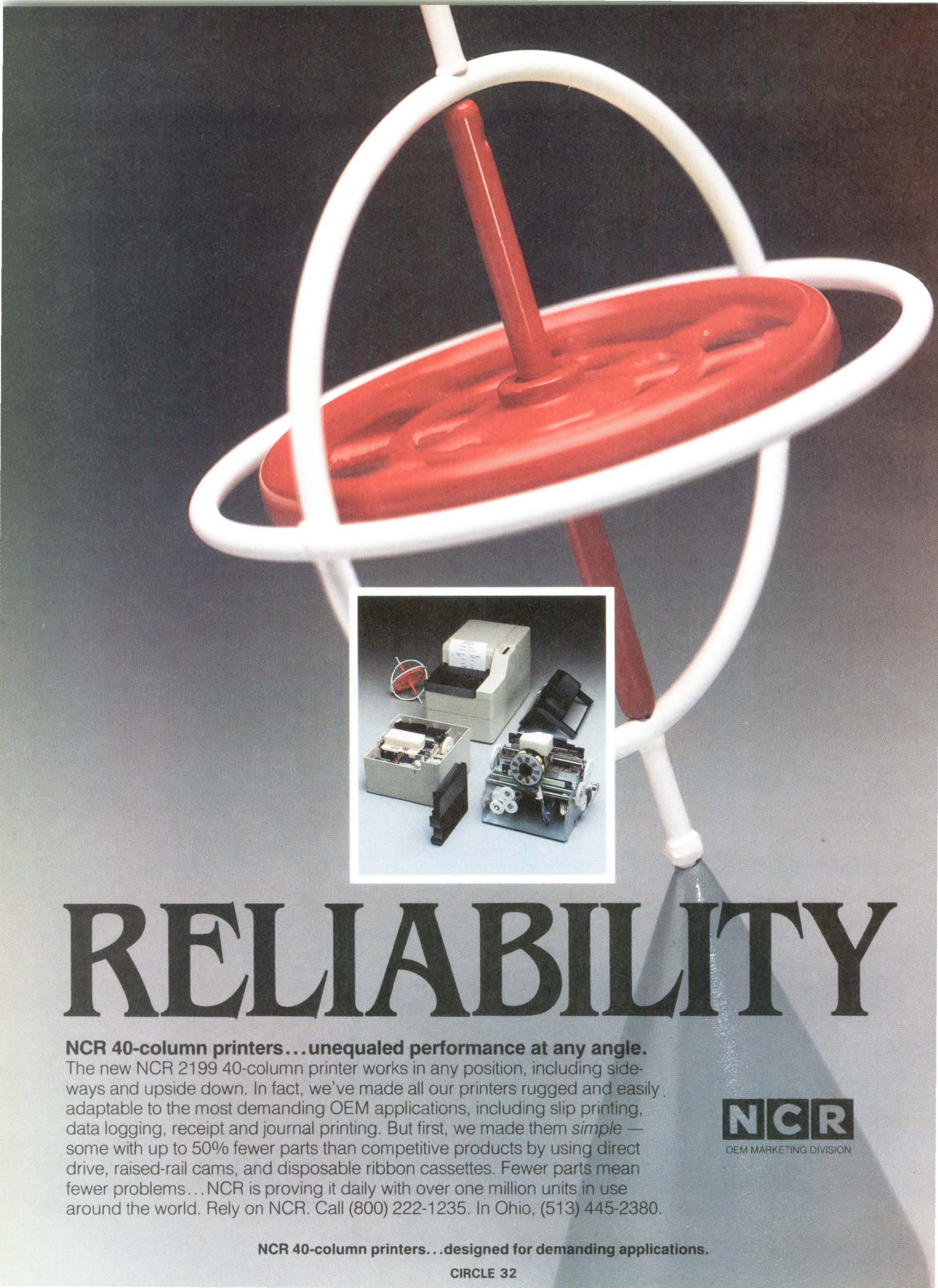
"Global and Local Deformations of Solid Primitives"
Alan H. Barr, Raster Technologies Inc



**Courtesy: Raster Technologies, North Billerica, Mass.**

* Based on information available at press time. Subject to change.

(continued on page 49)

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CIRCLE 32

(continued from page 47)

### Panel: Computer-Integrated Manufacturing in Japan

Chair: Tosiyasu L. Kunii, The Univ of Tokyo

**1:00 to 3:00 pm**

### Papers: Modeling II

Chair: Thomas W. Sederberg, Brigham Young Univ

"Interpolating Splines with Local Tension, Continuity, and Bias Control"
Doris H.U. Kochanek, National Film Board of Canada

"Efficient Octree Conversion by Connectivity Labeling"
Markku Tamminen, Helsinki Univ of Technology

"Automatic Synthesis of Graphical Object Descriptions"
Mark Friedell, Harvard Univ

### Panel: Computing in the Fast Lane: Super-systems for Computer Graphics

Chair: Richard Weinberg, Fifth Generation Graphics, Inc

Panelists: Michael Cosman, Evans and Sutherland Computer Corp; Joseph M. Cychosz, Control Data Corp; Gary Demos, Digital Productions; Kouichi Omura, Osaka Univ, and Rodney Stock, Lucasfilm Ltd

(continued on page 50)

**Courtesy: Susan Van Baerie and Douglas Kingsbury, Ohio State University, Columbus, Ohio.**

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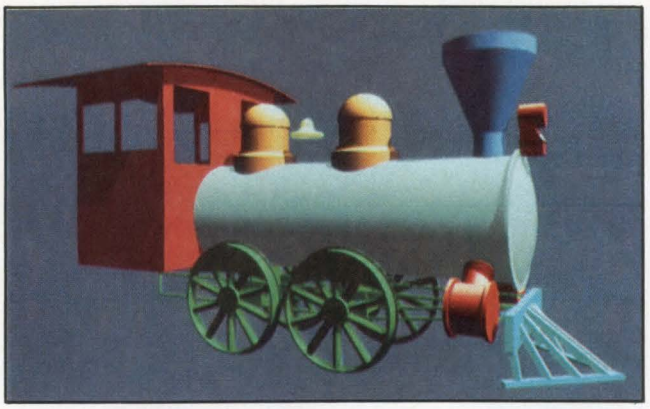


**Courtesy: CADLAB, Purdue University, Lafayette, Ind.**

**3:15 to 5:45 pm**

### Panel: A Retrospective: Six Perennial Issues in Computer Graphics

Chair: Robert M. Dunn, RM Dunn & Associates, Inc

Panelists: Edwin Catmull, Lucasfilm Ltd; David Evans, Evans & Sutherland Computer Corp; James Foley, The George Washington Univ; Robin Forrest, Univ of East Anglia; Alan C. Kay, Atari Inc; Stephen R. Levine, Electronic Graphics Associates; Carl Machover, Machover Associates Corp; and Robert Sproull, Carnegie-Mellon Univ

## Thursday, July 26

**9:00 to 10:30 am**

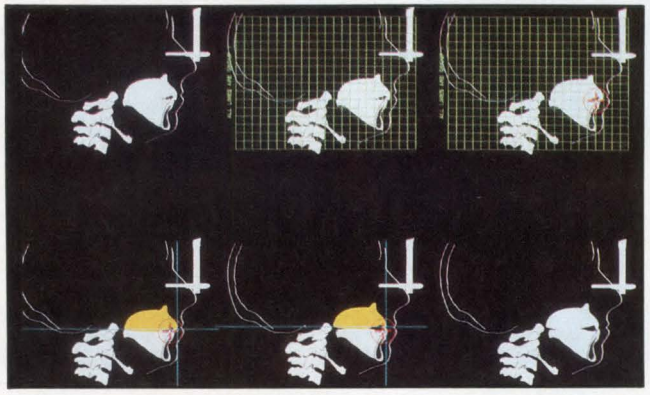
### Papers: Hardware

Chair: Ian Hirschsohn, Superset Inc

"A Parallel Processor System for Three-dimensional Color Graphics"
Haruo Niimi, Kyoto Univ

"Chap—a SMID Graphics Processor"
Adam Levinthal, Lucasfilm Ltd

"A Hardware Stochastic Interpolator for Raster Displays"
Timothy S. Piper, CAE Electronics Ltd



**Courtesy: Robert A. Sternberg, Arctan Graphic Arts, Inc, Rochester, NY.**

### Panel: International Technology Transfer

Chair: Carl Machover, Machover Associates Corp

**10:45 am to 12:15 pm**

### Papers: Visible Surface Algorithms

Chair: Bruce Brown, The Quail Group

"Invisibility Coherence for Faster Scan-line Hidden Surface Algorithms"
Gary A. Crocker, General Electric Co

"The A-buffer, An Antialiased Hidden Surface Method"
Loren Carpenter, Lucasfilm Ltd

"An Analytic Visible Surface Algorithm for Independent Pixel Processing"
Edwin Catmull, Lucasfilm Ltd

**2:00 to 3:30 pm**

### Papers: Ray Tracing I

Chair: Gary Rogers, Superset Inc

"Beam Tracing Polygonal Objects"
Paul S. Heckbert, New York Inst of Technology

"Ray Tracing with Cones"
John Amanatides, Univ of Toronto

"Distributed Ray Tracing"
Rob Cook, Lucasfilm Ltd

### Panel: Trends in Semiconductor Hardware for Graphics Systems

Chair: Henry Fuchs, Univ of North Carolina

**3:45 to 5:15 pm**

### Papers: Ray Tracing II

Chair: Edwin Catmull, Lucasfilm Ltd

"A Parallel Algorithm and Architecture for Realistic Image Synthesis"
Mark Dippe, Berkeley Computer Graphics Laboratory

"Ray Tracing of Steiner Patches"
Thomas W. Sederberg, Brigham Young Univ

"Ray Tracing Volume Densities"
James T. Kajiya, California Inst of Technology

### Panel: Microcomputer Graphics

Chair: Howard Pearlmutter, Softweaver

## Friday, July 27

**8:30 to 10:00 am**

### Papers: Interactive Systems

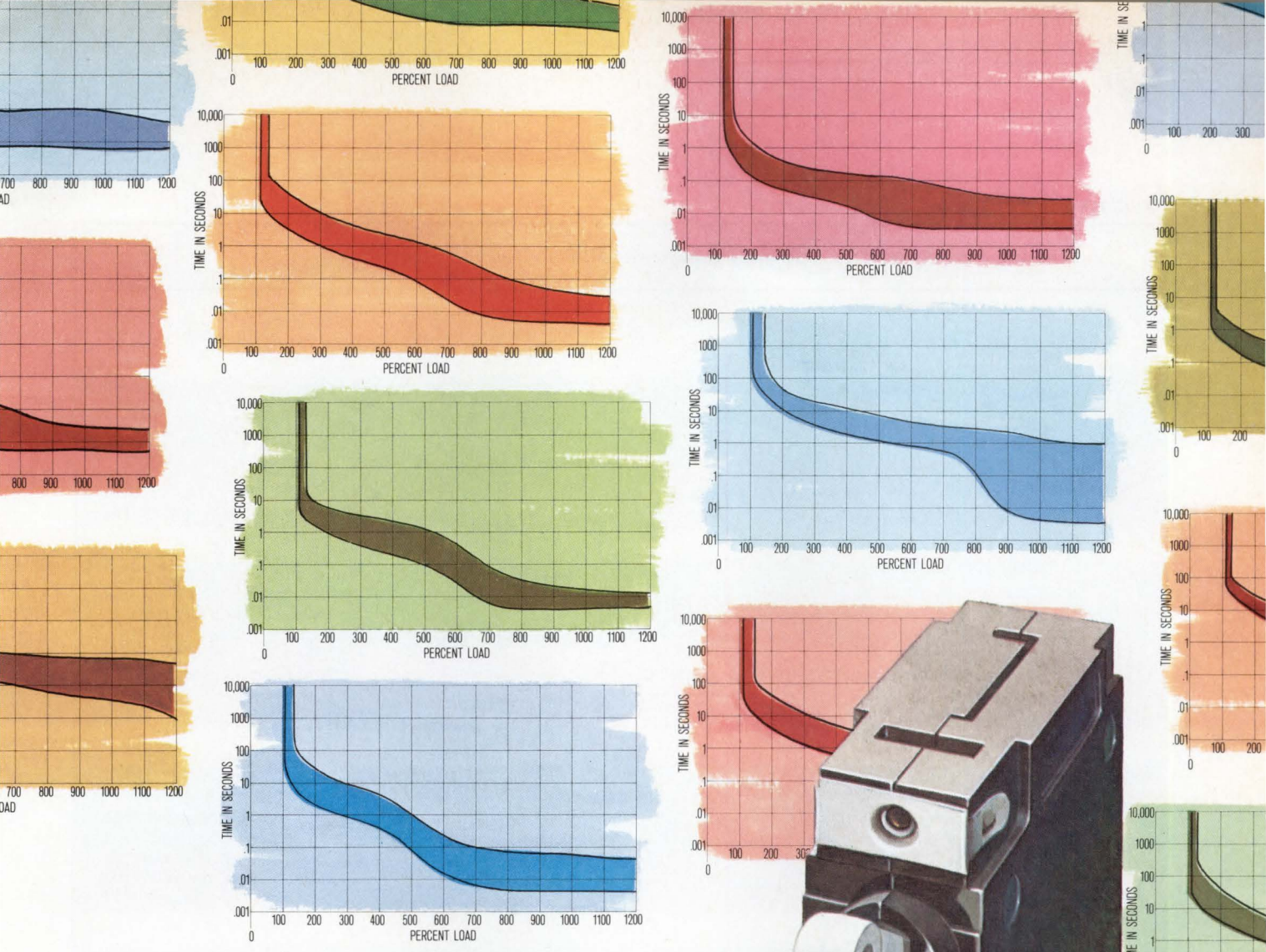
Chair: John Brewer, Louisiana State Univ

"A System for Algorithm Animation"
Marc H. Brown, Brown Univ

"Priority Windows: A Device Independent, Vector Oriented Approach"
Richard J. Littlefield, Battelle Northwest

"Manipulating Simulated Objects with Realworld Gestures Using a Forch and Position Sensitive Screen"
Margaret R. Minsky, Atari Cambridge Research Laboratory

(continued on page 52)

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CIRCLE 34

7688

(continued from page 50)

**Summary of Key SIGGRAPH '84 Courses**

| | General courses | Monday July 23 | Tuesday July 24 | Course site |
|---|---|---|---|---|
| 1 | Introduction to computer graphics | x | x | Auditorium and Convention Hall |
| 2 | Color perception | x | | Hyatt Regency |
| 3 | Introduction to raster graphics | x | | Hotel Leamington |
| 4 | Psychology of user-computer interfaces | | x | Amfac Hotel |
| 5 | How to design user-computer interfaces | x | | Amfac Hotel |
| 6 | Device-independent computer graphics using the standard: GKS | x | x | Auditorium and Convention Hall |
| | Visual synthesis | | | |
| 8 | Introduction to computer animation | x | x | Amfac Hotel |
| 9 | Advanced computer graphics animation | | x | Auditorium and Convention Hall |
| 10 | Introduction to TV, video, film, printing | | x | College of Art and Design |
| 11 | State-of-the-art in image synthesis | x | | Heritage Hall, Public Library |
| 12 | Advanced image synthesis | | x | Heritage Hall, Public Library |
| 13 | Technologies of highly interactive computer graphics | x | | Auditorium and Convention Hall |
| 14 | Bitmap graphics | | x | Hotel Leamington |
| 15 | The mathematics of computer graphics | x | x | Cricket Theatre |
| | CAD/CAM/CAE | | | |
| 16 | Graphics applications in robotics | x | | Holiday Inn |
| 17 | CAD systems | | x | Holiday Inn |
| 18 | Introduction to solid modeling | x | | Auditorium and Convention Hall |
| 19 | Advanced topics in solid modeling | | x | Auditorium and Convention Hall |
| 20 | Freeform curves and surfaces I | x | | Auditorium and Convention Hall |
| 21 | Freeform curves and surfaces II | | x | Auditorium and Convention Hall |
| 22 | VLSI and computer graphics | x | | College of Art and Design |
| | Graphics applications | | | |
| 26 | Distributed graphics systems: workstations, microcomputers, and mainframes | | x | Holiday Inn |
| 27 | Building scientific and engineering graphics applications | | x | Hyatt Regency |

**10:15 to 11:45 am**

## Papers: Shading and Texturing

Chair: Maureen Stone, Xerox Palo Alto Research Center

"Summed-area Tables for Texture Mapping"
Franklin C. Crow, Xerox Palo Alto Research Center

"Modeling the Interaction of Light Between Diffuse Surfaces"
Cindy M. Goral, Cornell Univ

"Shade Trees"
Rob Cook, Lucasfilm Ltd

## Panel: Role and Reality in Graphics Standards

Chair: James R. Warner, Precision Visuals

**1:15 to 2:45 pm**

## Session: Algorithms for Painting and Matting

Chair: Larry McCleary, Naval Oceans Systems Center

"A Family of New Algorithms for Soft Filling"
Kenneth P. Fishkin, Univ of California-Berkeley

"Texture Synthesis for Digital Painting"
John-Peter Lewis, Massachusetts Inst of Technology

"Compositing Digital Images"
Tom Duff, Lucasfilm Ltd

## Panel: The Storage and Retrieval of Integrated Graphics and Text

Chair: R.A. Earnshaw, Univ of Leeds

Panelists: William R. McMunn, Gerber Systems Technology; and S. Pollitt, Huddersfield Polytechnic

**3:00 to 4:30 pm**

## Session: Graphics Standards

Chair: Jose Encarnacao, FG Graphisch—Interaktive Systeme

"A Programmer's Interface to Graphic Dynamics"
Joshua U. Turner, IBM Corp

"Imaging with GKS"
Cliff Stoll, Space Telescope Science Inst

"NOVA*GKS, An Implementation of the Graphical Kernel System"
Clinton N. Waggoner, Nova Graphics International Corp

## Panel: Computer Graphics Research in Japanese Universities

Chair: Laurin Herr, Pacific Interface □

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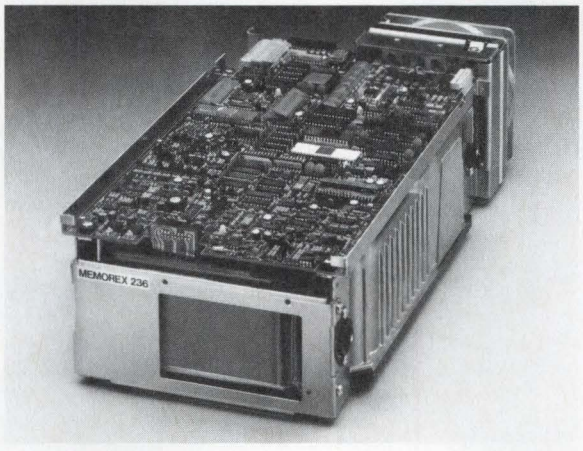


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**CIRCLE 35**

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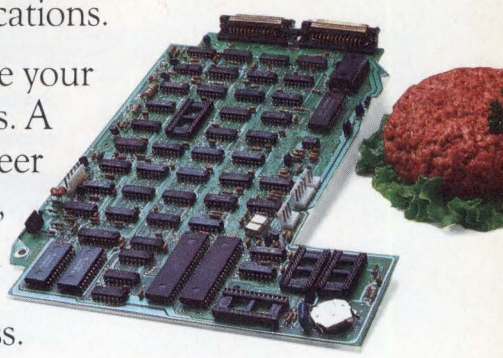

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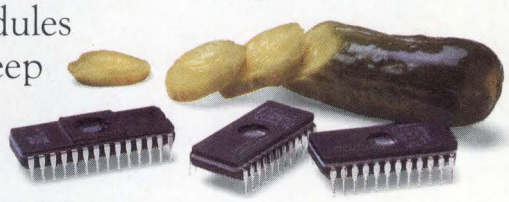

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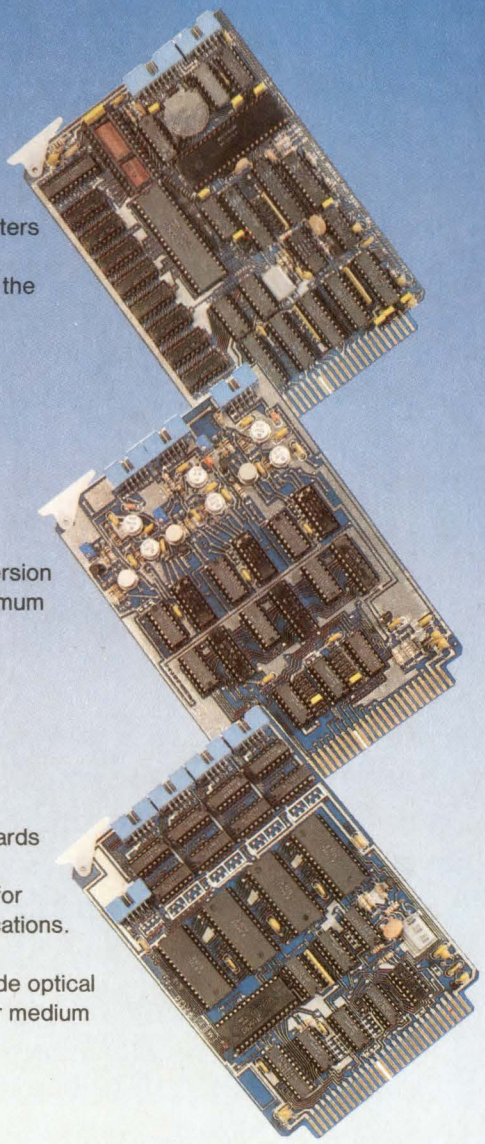

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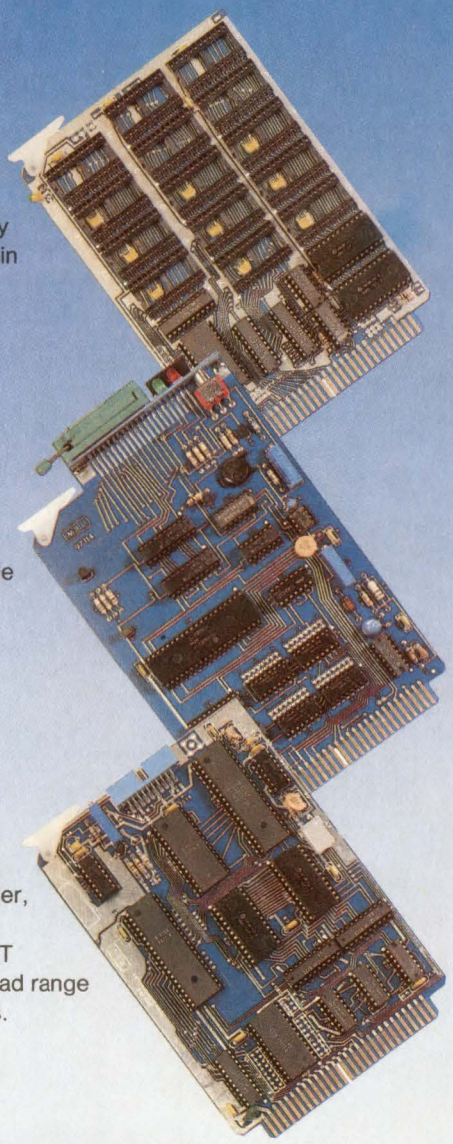

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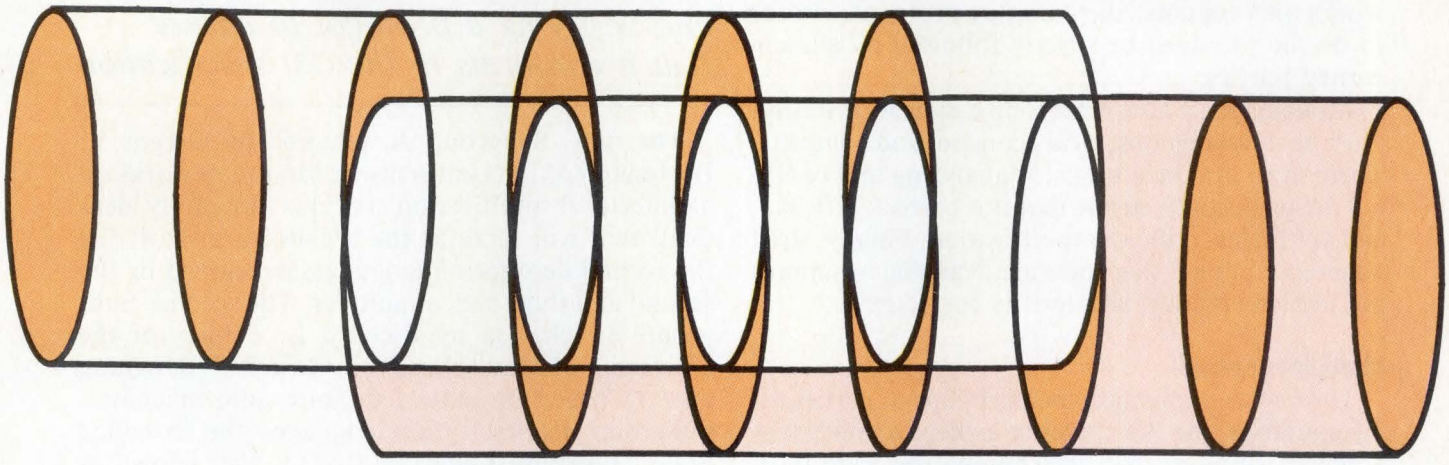
# FORMAL PROTOCOL SPECIFICATION READY TO MAKE ITS MARK

**Specification, implementation, validation, and test procedures are under development worldwide to help computer communication gurus define international and national protocols.**



**by Harvey J. Hindin,
Special Features Editor**

Software protocols implementing the upper layers of the International Standards Organization's seven-layer model for computer communications are evolving rapidly. In fact, final versions of such protocols are expected in the next two years. However, these as well as other protocols from standards-making bodies, such as the Europe-based International Consultative Committee for Telephone and Telegraph and the U.S.-based National Bureau of Standards, present some fundamental implementation problems to the computer community.

For example, take the manufacturer, system integrator, computer designer, or end user who wants to incorporate these protocols into real products. Each has no easy way of knowing if the software a source claims is an implementation of a particular protocol is actually accurate or compatible with other implementations. This is a serious problem. The success of the worldwide effort to develop upper-level software protocols largely depends on the ability to properly specify, verify, and test the protocols and their implementations.

Recognizing this problem, diverse standards-making bodies, research organizations, universities, and industrial firms have pressed for formal protocol description and test techniques. The results of their efforts have been years in coming. But, next February a machine-readable, formal description of the transport (layer 4) and session (layer 5) layers of the International Standards Organization's (ISO) reference model for Open System Interconnection (OSI) should be presented to that organization's Technical Committee 97/Subcommittee 16/Working Group 1 (TC97/SC16/WG1). These documents will ultimately form the "law" that determines whether or not a piece of software aimed at proper session

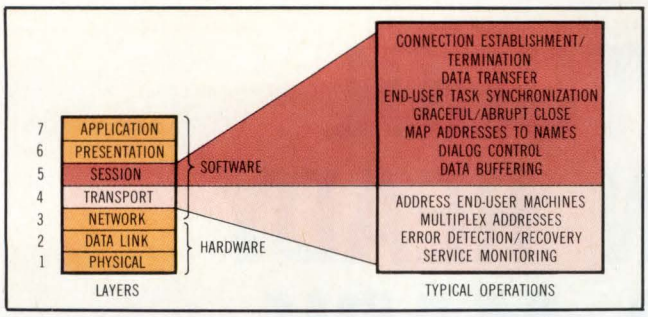



**Fig 1 Ultimately, there will be formal specifications for all seven hardware and software layers of the International Standards Organization's reference model for computer communications. The transport and session software layers are already draft international standards, and highly developed. They will be the first to be formally specified.**

or transport layer communication will really do the defined job. As might be expected, ISO will not stop at formal transport and session specification but will eventually specify all seven layers (Fig 1).

Protocol accuracy hinges on more than just bug-free software, however. If the ISO/OSI model is to succeed in allowing the economical, worldwide exchange of data between different computer networks and systems, the complex protocols chosen to do the job must be strictly followed by all concerned parties.

Attaining strict adherence is no easy feat. Protocols must be unambiguous, clear, concise, and complete. There must also be a basis for analyzing and verifying the protocol to ensure that it is correct, efficient, and conforms to the OSI specification. Finally, strict adherence implies that tools are available to support the implementation and test its correctness.

## Multiple sources

Through the voluntary memberships of participating countries, the ISO strives to achieve a universally accepted standard for determining the validity of ISO protocol implementations. But, as mentioned, there are complementary, cooperative efforts going on at the Consultative Committee for Telephone and Telegraph (CCITT) and the National Bureau of Standards (NBS). And, mirroring the industry's interest in this effort, researchers are making contributions, for example, at Sytek, Inc (Mountain View, Calif) and IBM (Raleigh, NC). The latter has an almost complete formal description of its ubiquitous systems network architecture (SNA).

Work is also proceeding apace at England's National Physical Laboratory, France's Paris-based Agence de l'Infomatique, Australia's Commonwealth Scientific and Industrial Research Organization in Canberra, Canada's University of Montreal, and Holland's Twente University of Technology in Enschede. These are but a few of the major players in the effort to define effective computer communication protocols that can be implemented globally without special training, and without the need to consult experts.

Another goal is to ensure availability of a wide variety of computer aided tools to assist practitioners in documenting, validating, implementing, analyzing, and testing protocols in general, and the ISO/OSI protocols in particular. Of note, however, is that the work is part of a larger effort to develop techniques that ensure the correctness of all types of software programs. This, in turn, is prompted by the need to produce bug-free, verifiable, testable software as one remedy to soaring computer system software costs.

The work of ISO's TC97/SC16/WG1 committee on formal description techniques (FDTs) is, perhaps, the most important ongoing effort because its work will directly lead to the important February 1985 presentation. The committee has been doing its often tedious, often abstract, but highly important job since it got together for the first time in Chicago in January 1980. Today, for efficiency, and since there are a variety of issues to address, the FDT group comprises three subgroups.

*There must be a basis for analyzing and verifying a protocol to ensure that it conforms to the OSI specification*

The first, Subgroup A, (chaired by Gregor V. Bochmann of the University of Montreal) works on architectural specification concepts (hopefully identical) that will serve as the architectural basis for the formal description languages developed by the second and third subcommittees. The second, Subgroup B, (chaired by Richard L. Tenney of the University of Massachusetts in Boston) is designing an FDT based on extended finite-state machines. Subgroup B's description language—the Extended State Transition Language (ESTL), also known as Estelle, has features similar to the specification and description language (SDL) or X.250, under development at CCITT. The third subcommittee (chaired by Chris A. Vissers of the Twente University of Technology) is working on an FDT based on what is known as temporal ordering of interaction primitives (Fig 2). It has forged a temporal ordering specification (TOS) language.

The three subgroups were formed because the committee members realized early on that the issues concerned with specifying an FDT were so highly mathematical and abstract in nature that subgroup specialization was needed to do the job. Worse, since the formal specification of protocols was a relatively new field, there was a wide diversity of opinion as to which FDT techniques were suitable for the different ISO layers. For example, there are many different techniques possible within the concepts of the extended finite-state machine and the temporal ordering of interaction primitives. What is suitable for one layer is not necessarily suitable for another.

Each subgroup is charged with constructing a common proposal that will complement, rather than compete with, the proposals of the other subgroups.

### What's going on

The complexity of protocol issues makes it difficult to understand what is going on with one FDT, let alone comprehend what is happening elsewhere. Thus, by design, all the subcommittees are generating tutorial documents for each FDT they produce. The goal of the documents is simple: people familiar with ISO/OSI standards should be able to read and understand them.

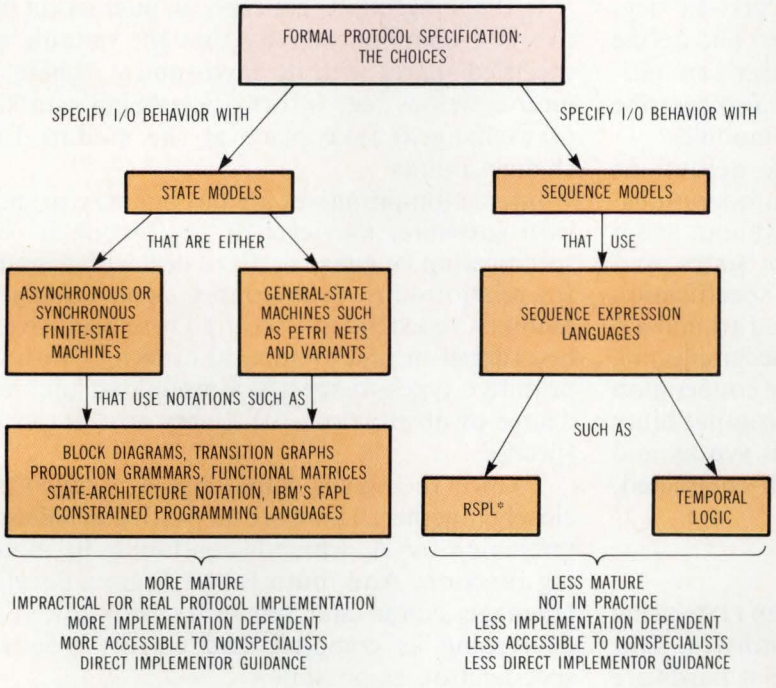
The rather elaborate documents produced are available to all concerned parties. But, from a practical point of view, it is significant that the subcommittees have come up with paper demonstrations of the FDTs they have developed. Members have concentrated on the transport layer of the ISO model for these examples because it is the best developed. In addition, it is a very real protocol with deep complexities. Thus, an implementation of it is far more than a mere exercise. As Richard desJardins, vice president of Computer Technology Associates (Englewood, Colo) and chairman of ISO Subcommittee 97/16 puts it, protocols need to be both powerful and simple for many people to use. But, they cannot be so simple that they hide the hard parts of an implementation.

Having nonexperts understanding their work is a major issue for the FDT subgroups. Ideally, an FDT and its associated language should be no more difficult to learn than a new programming language. Learning it should take about a month. Once this is done, as Carl Sunshine (principal engineer at Sytek) notes, the seat-of-the-pants techniques for hand coding (which many industrial firms use to implement narrative protocol descriptions) will end.

As mentioned previously, Subgroup A is striving to develop an architectural specification concept that forms the basis for the description languages developed by Subgroups B and C. It is also charged with ensuring that the results can be combined into a single specification.

To do its job, Subgroup A has defined a variety of useful protocol description concepts for formal specification. Chief among these are the module and the channel (Fig 3). A module is a specification unit whose behavior is defined by the language of Subgroup B or C. A module can also be defined in terms of a refinement—a structure of interconnected submodules. In turn, each of these must be specified. Modules or submodules interact with each other through channels whose specifications define which module interactions are possible when that channel is used.

Most of Subgroup A's architecture specification work is done. But, work on ensuring that the various B and C FDTs complement each other is still in progress, since it had to await the development of the languages by these committees. Subgroup A's remaining work consists of a liaison with B and C

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*RELIABLE SOFTWARE PRODUCTIVITY LANGUAGE

**Fig 2 There are almost as many formal description techniques as there are programming languages—if not more. Although overlaps exist, the conceptual approaches to protocol specification may be loosely classified as state or sequence models; each with advantages and disadvantages.**

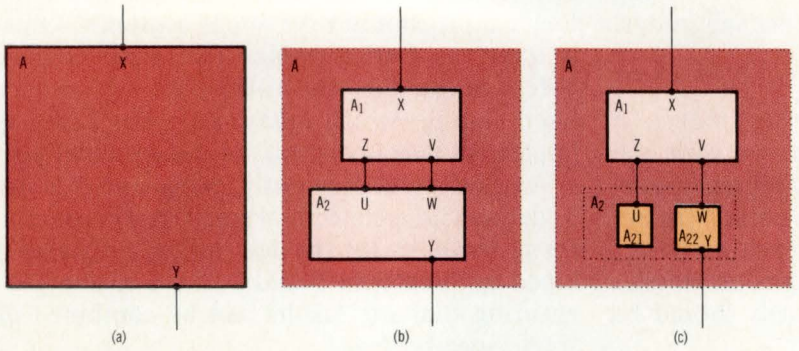


**Fig 3 The ISO/TC97/SC16/WG1 Subgroup A's architectural specifications for formal description languages include modules (units of specification) and channels. Modules (a) are defined interconnected submodules (b) or further refinements (c). All interact through channels.**

SOURCE: CHRIS A. VISSERS, TWENTE UNIVERSITY OF TECHNOLOGY ENSCHEDE, HOLLAND
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to check for, and eliminate, differences in the interpretation of architectural concepts.

For Subgroup B's work on FDTs, the name of the game is extended finite-state machines. These automatons provide the underlying model for determining how a protocol software module or submodule behaves.

A programming language is needed to specify the transitions occurring between the states of a finite-state machine when it represents the protocol actions. So, Subgroup A developed a special language uniquely suited to this chore. It is based on ISO's Pascal, with some committee-derived extensions.

Using this language, the specification of a state transition comprises the channel-type and module definitions, and the system's structure. The channel-type definitions name the two channel "players" (eg, the sender and receiver of a file transfer) and define the channel interactions and what player can initiate them. The channel-type definitions also describe the various connections between the modules.

As might be expected, the module definitions explain the actual transitions and their operations. Each transition is specified with the conditions under which it may be applied, the resultant states, and more. Finally, a system structure specification describes how modules are instantiated to make a system. The syntax and semantics for accomplishing these chores must be developed with the cooperation of Subgroups A, B, and C to ensure compatibility between different FDTs. Much of this syntax and semantics development work has been completed, although some work remains.

### Temporal ordering

Subgroup C has the task of setting up FDTs using temporal ordering of interaction primitives. This concept is somewhat equivalent to what hardware engineers know as the "black box" idea. With a black box representation of hardware, the box contents are of no concern. Only the terminal or I/O characteristics are of interest.

Similarly, with temporal ordering of interaction primitives, defining the behavior of a software module that is to be specified only necessitates concern for the module's interaction with its environment. Its software "insides" are of no importance. Thus, the specification interacts with the module implementation minimally, if at all. All that is done is to specify all possible sequences of information I/Os that may be encountered at the module's I/O channels. With this approach it is relatively easy, for example, to handle I/O time delays.

*Module definitions explain the actual transitions and their operations.*

In the Subgroup C concept, an interaction primitive is a common activity that the module being specified shares with its environment. These common activities (eg, information being established or exchanged) take place at the module I/O or channel points.

Interaction primitives are but one way to specify, with software, the level of abstraction a formal specification language needs to deal with a module's I/O relationships. (Subgroup C is also using what amounts to extended Pascal.) These primitives can be ordered in time (temporal ordering) with other primitive types to specify a module at the desired degree of abstraction—be it very abstract or quite specific.

To meet their goals, Subgroups A, B, and C work closely together. There are no particular milestones remaining for A, which is continuing its monitoring function. And, both B and C are still refining language syntax and semantics with the goal of developing as complete and correct a language specification as possible.

There is, of course, other work. For example, a translator is being designed to convert Subgroup B's language to Subgroup C's language. And, there is the question of how far the language work should

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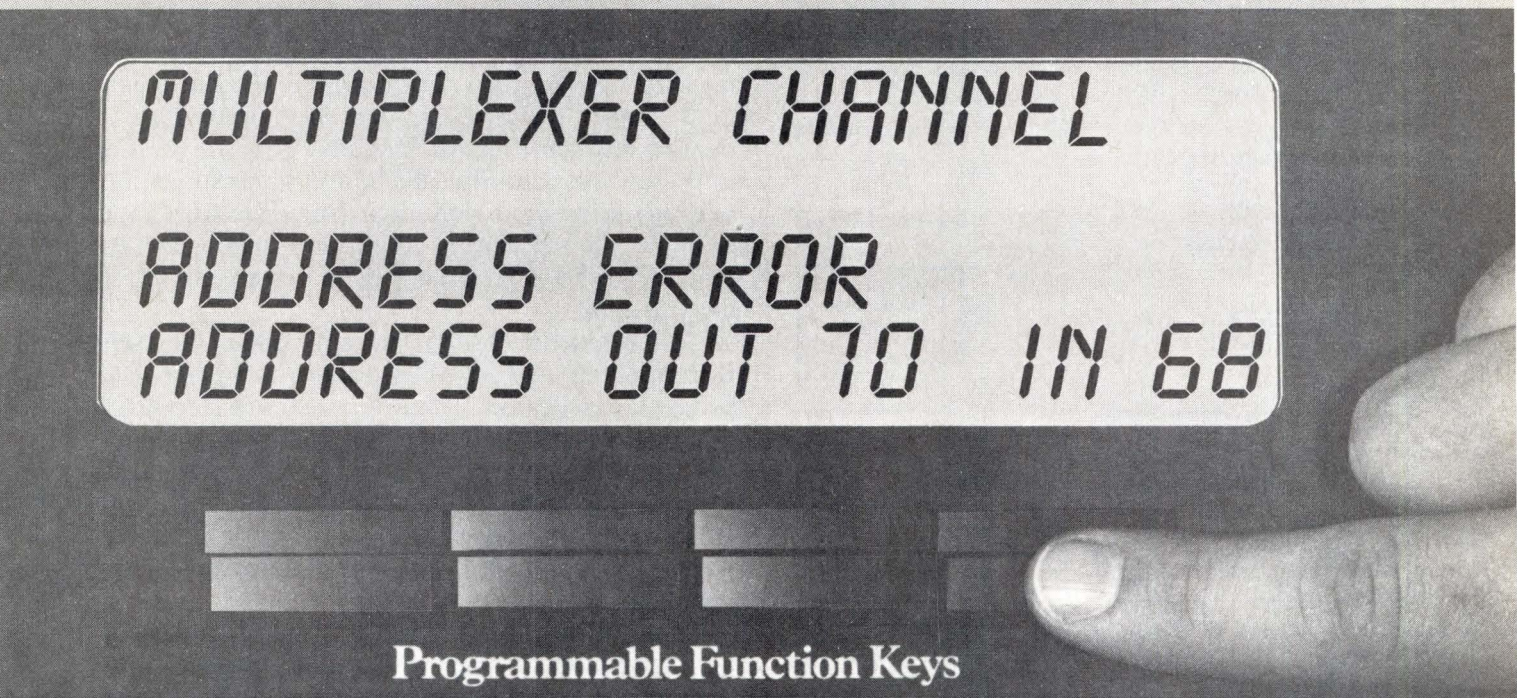


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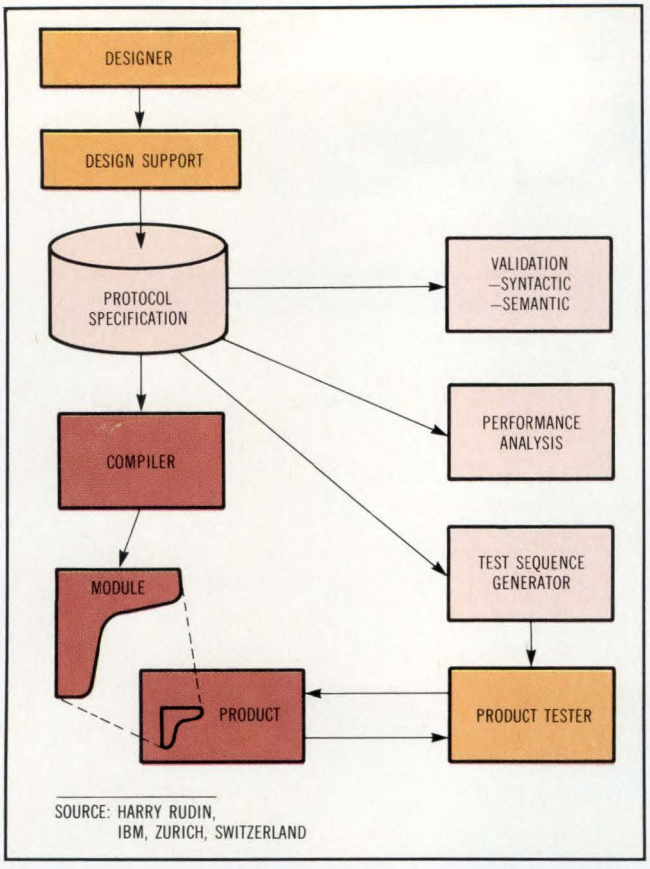


**Fig 4 The need to design, debug, and implement protocols in reliable software leads to a protocol engineering system. The protocol design is expressed in a formal, machine-executable specification. The system then derives design and analysis tools directly from the specification.**

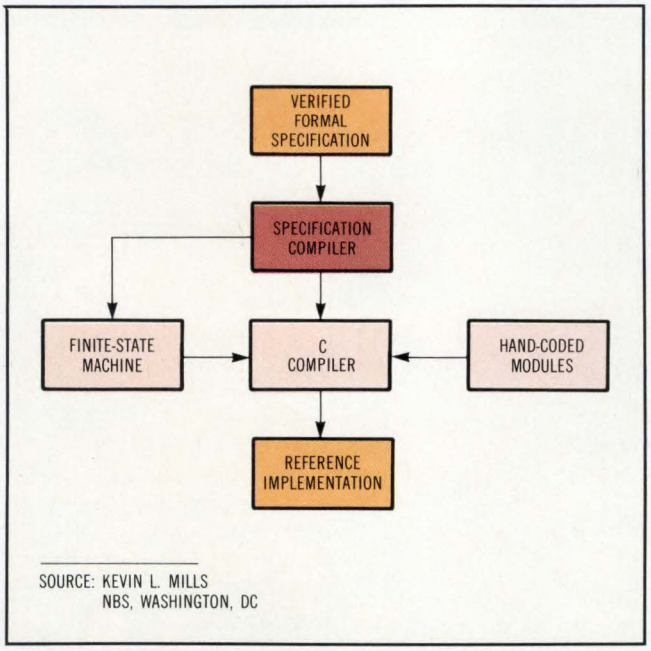


**Fig 5 In one typical implementation of the NBS class 4 transport protocol, automatically generated code comprises 4500 lines of C language; hand-coded modules for machine-specified functionality contain 5700 lines. Thus, about 40 percent of the implementation is generated without hand coding.**

go. To some committee members, the languages themselves should be made an ISO standard. Other members hesitate and say that only a language-descriptive document should be issued, and that it is the language-specified protocol only that must be a standard.

### Across the Atlantic

While all this ISO-based work occurs, other standards-making organizations are busy developing their own projects. For example, the European CCITT and the U.S.-based NBS are pursuing their own formal specification languages. However, it is important to note that all these organizations are working toward a common language with, for example, the NBS formal description language set to migrate to the ISO language (which is a superset of it) with time.

Unlike ISO, the CCITT has not concerned itself with applying its formal description language to a protocol description. CCITT is content to stop after defining its SDL language. Originally a graphics description language, for some people, SDL lacks some of the flexibility found in the ESTL language. According to various sources, it is even less flexible when it is compared with the Subgroup C TOS language.

On the other hand, it is well-established, and based on the finite-state machines familiar to generations of engineers. Much effort is going on to design similar facilities in SDL and ESTL so that the same functions are available from both. As presently designed, there is functionality in SDL that is unavailable in ESTL and vice versa. A key debate issue involves which enhancements to add to either language.

The CCITT formal specification experts and the ISO experts have decided to hold common meetings in order to accelerate their agreement (as much as possible) on one formal specification language. For example, they will hold common sessions at a Copenhagen, Denmark meeting this month. Regardless of these efforts, SDL will probably have a protocol specification life of its own because it is so well established. It is already a CCITT recommendation and these, historically, have a long life.

It is important that the CCITT and ISO formal description techniques be as close as possible. While ISO issues international specifications for seven layers of computer communications to "network the world," the CCITT also has an important task. It is charged with choosing the protocols for gateways to connect international telephone and data communication networks. Thus, for example, if the Canadian packet-switching network wants to communicate with the French network, it must first concur with the CCITT protocol methods.

CCITT's work should be viewed as complementary to the ISO work. Both organizations have the desire

to come up with, if not the identical specification language, then languages that are very similar or easily converted from one to another.

It can be fairly said that CCITT wanted to complete the job at hand and thus modified an established and well-known language it already had. On the other hand, ISO felt that the latest practical language technology was needed to do the job. ISO's ESTL specification language approach can be thought of as a middle ground between the well-established CCITT language design and the yet-to-come-mature TOS language and FDT from ISO's Subgroup C.

### Developing a specification compiler

For its part, NBS realized early the importance of a specification language for protocols. From the beginning of the computer communication protocol work, NBS has been working with its consulting firm; Bolt, Beranek and Newman of Boston, Mass in the NBS's Institute for Computer Science and Technology (ICST). Some years ago, BBN developed an extensions-to-Pascal-based specification language for NBS. These extensions provide for the augmented-with-variables definition of a finite-state machine. This language is the predecessor of the ISO ESTL language, and, while it is a functional subset, it is syntactically different.

However, NBS, like similar organizations in Canada, England, Australia, France, Germany, and Holland has done more than develop a specification language. It has developed a specification compiler that uses this language as its input and produces C code as the output. The NBS specification technique—this is how it is known since there is no name for it—has already been applied to the layer 3 component of the X.25 protocol, class 2 and class 4 of the ISO transport protocol, and early, partial specifications of the ISO session protocol.

NBS has even gone further. It is developing a suite of validation tools, performance analysis measures, and test sequences. All of these can guarantee that a formal protocol specification need not stand alone and can be used in conjunction with practical tools for the real-world tasks of the implementor (Fig 4). All the NBS tools arise from, and are based on, the formal protocol description.

NBS's full transport specification is a combination of English prose and the formal language specification. Sections of this document are literally the input to the specification compiler (Fig 5). The document itself was produced with a Unix text composition tool called Nroff. Nroff uses inserted software pseudo-ops to differentiate between the prose sections and the formal sections of the specification document. Thus, the formal sections are not composed in any way. The same pseudo-ops are used by the specification compiler (after the specification document is produced by a parallel enhanced-with-pseudo-ops Nroff operation that can turn text composition on and off) to enter document contents directly as compiler input.

For class 4 transport, the NBS compiler generates about 40 percent of the implementation code automatically, leaving out the machine-dependent parts. Thus, for example, primitives defined in the formal specification have to be hand coded, multiplexing must be taken care of by the implementor, and the connection to a particular computer's operating system must also be hand coded. In short, once the automatically generated code is supplemented with the necessary hand-coded material, the result is a protocol implementation ready for testing.

As might be expected, NBS is not the only organization with this compiler approach. For example, among major private companies, IBM has made a major push in this area with its SNA (see Panel, "Making protocols as formal as possible").

At NBS, the formal protocol specification is used for two other chores. It is also used to derive,

### Making protocols as formal as possible

Within IBM, automated implementation has been used to generate various systems network architecture implementations that take into account different machine architectures and system environments. Since a network architecture such as SNA can appear in varied device microcode, communication software, and test tools—to name a few examples of its use—it is important that all implementations be correct and consistent.

To set up its formal version of SNA, IBM uses its own language known as the Format and Protocol Language (FAPL). The formal SNA specification is written in FAPL. The specification input to a compiler is much like that used in the NBS design. FAPL, related to IBM's PL-I language, is a high level procedural language that can accommodate both the concurrency and the finite-state machines demanded by computer communication protocols. In this sense, it is similar in spirit to the Extended State Transition Language (ESTL). Originated in 1978, FAPL does not address the temporal ordering concept.

Of key importance is that IBM felt it would be too expensive to develop FAPL compilers for all significant machine architectures. Thus, the FAPL compiler output usually comes in an intermediate language for which a compiler already exists.

FAPL work is an ongoing process and, with time, more parts of SNA are brought under its wing. In fact, the work has gone so far that is has been incorporated in an IBM-shipped product. A formal SNA specification will also be useful when gateways between SNA and ISO-based networks are built to accommodate all SNA and ISO layers.

The potential for an error-free, order-of-magnitude, faster implementation of gateway software will be hard to resist. Formal methods cut the protocol implementation costs. For example, according to Codex Corp's (Mansfield, Mass) John D. Day who is one of the "fathers" of the ISO protocol work, the time for a typical OSI transport layer implementation is now 6 weeks. Considering that it used to be 10 to 15 months, this is quite an improvement.

## The NCC transport demo: a formal affair

At next month's National Computer Conference in Las Vegas, Nev, there will be a demonstration of the real-world capabilities of the National Bureau of Standards class 4 transport protocol working on local networks. At this conference, the NBS formal specification language will play a major role. This multivendor demonstration will use the NBS-generated formal specification-based transport document as its ground rules. In addition, the vendors will use the NBS-generated suite of test tools.

These test tools will ensure proper operation of both the carrier sense multiple-access/collision detection (CSMA/CD) network implementation (the IEEE 802.3 standard) of the transport protocol, and the IEEE 802.4 token-bus network implementation. Toward this end, NBS has hosted preliminary testing (at its so-called neutral site) of the 802.3 implementation while General Motors has hosted the 802.4 version's neutral site. Moreover, before testing at GM, every vendor has tested its transport protocol at NBS using either Telenet or 802.3.

Coordinated by NBS, GM, and Boeing Computer Services Co, the 14-vendor demonstration includes 9 vendors showing a business-geared network: Advanced Computer Communications, Boeing Computer Services, Charles River Data Systems, Digital Equipment Corp, Hewlett-Packard, Honeywell Information Systems, ICL, Intel, and NCR. Seven firms are running the industrial demonstration: Allen Bradley, Concord Data Systems, DEC, Gould Modicon, Hewlett-Packard, IBM, and Motorola.

The business demonstration will show NCC attendees that it is possible to transfer multiple file types (eg, ASCII) on a token-bus local network from an IBM Series/1 computer and IBM PC combination to a "foreign" machine/terminal combination. Running an ISO file transfer protocol with the aid of the ISO class 4 transport protocol will accomplish this.

Other business and factory capability demonstrations will use a CSMA/CD local network, other file types, and programmable industrial controllers. For the participating vendors and their audience, it is a graphic demonstration of how powerful the ISO protocols can be in allowing disparate computer equipment to communicate. It is also a sure sign that the days of the single-vendor computer environment are gone.

through semi-automated processes, suites of implementation tests. Clearly, testing any given implementation is necessary for confidence that the compiler is functioning well.

Moreover, the formal specification is also the input to a protocol verification process. In this case, verification means that the formal specification is examined to look for (among other problems) deadlocks, livelocks, completeness, boundedness (an action is taken for every protocol message that is exchanged), and that protocol completion ends off in a known machine state.

As mentioned, NBS's formal description language is a subset of the ISO ESTL language (see Panel, "The NCC transport demo: a formal affair"). NBS is in the process of building a compiler for the Subgroup B language. It is also designing the same suite of tools for verification, compilation and test generation for the Subgroup B language as it has for its current language.

The bottom line of all this, says Jerry Linn, manager of the high level network protocol program at NBS's ICST, is that class 4 and class 2 transport is the only protocol that NBS will distribute using the NBS formal description language. NBS will soon adopt ESTL and is currently developing a class 4 transport specification with it. NBS is also heavily involved with the previously mentioned ISO effort to have formal descriptions of ISO transport and session protocols ready by the end of this year for presentation at next February's Paris ISO meeting. There will also be formal NBS contributions to ESTL-based specifications for other ISO protocols, such as file transfer and Internet.



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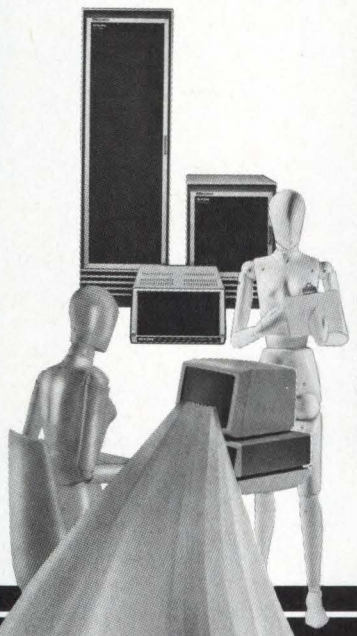

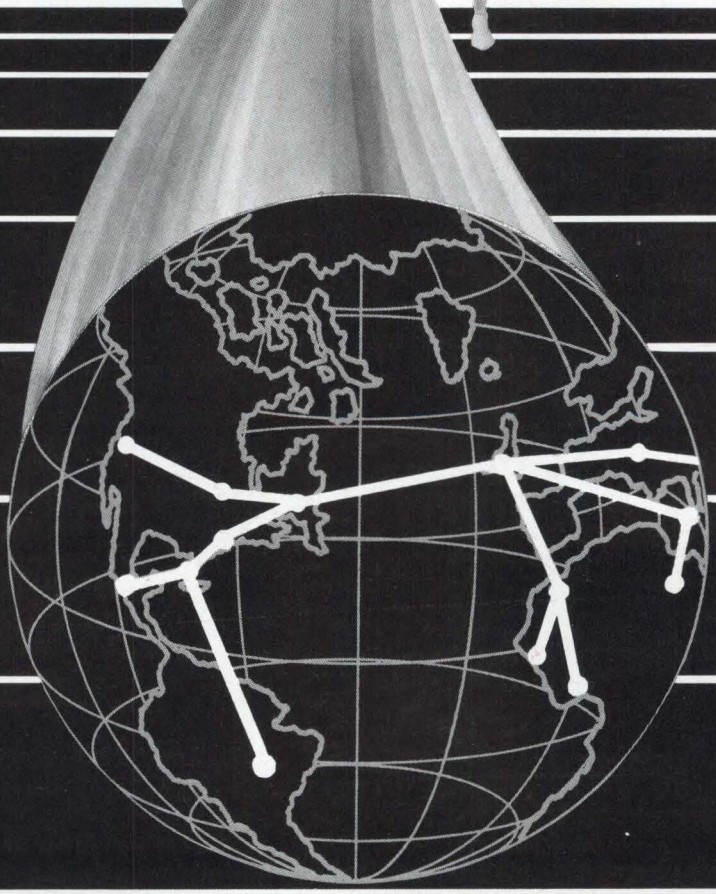

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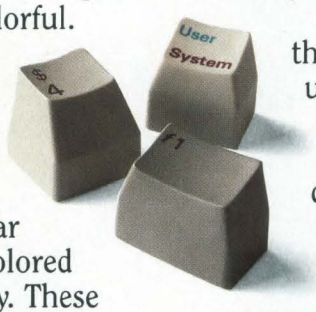


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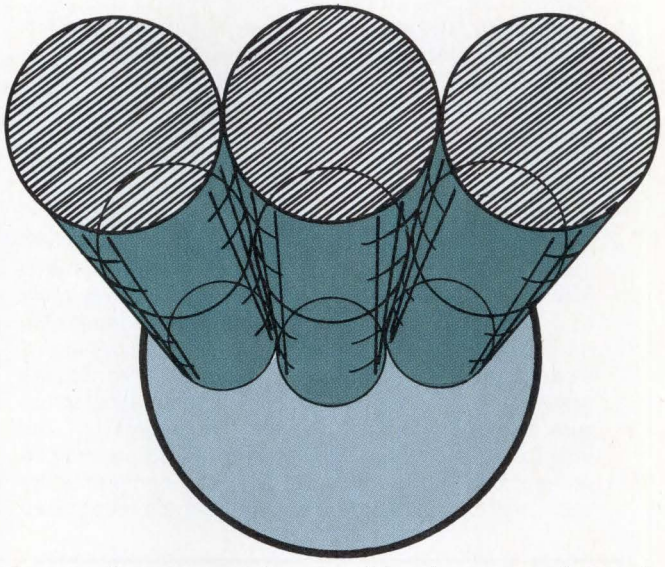
# PRACTICAL AND CONTINUOUS SPEECH RECOGNITION

**A continuous speech recognition system that accepts sentences of any length permits cost-effective voice-data entry in demanding real-world environments.**

**by Steve Ross and Jeff MacAllister**



Despite the recent attention paid to speech recognition, the microphone poses no serious threat to the computer keyboard. Indeed, most commercial speech-recognition systems are little more than toys rather than serious alternatives to data entry. However, there is a system available that can provide cost-effective, voice-data entry in real-world environments.

This continuous speech-recognition system, the Verbex Model 3000, can accept naturally spoken sentences of any length. This capability enables the Model 3000 to overcome the drawbacks of isolated-word systems or those of connected-speech systems, which require users to speak in a staccato rhythm or limit utterances to a few words.

Many of the system's design elements stem from the results of the Department of Defense's Advanced Research Project Agency (ARPA) Speech Understanding Research (SUR) project. This study was conducted in the 1970s with the goal of demonstrating continuous-speech recognition in an experimental environment. Continuous-speech recognition is difficult because a word's pronunciation varies dramatically depending on its context in a sentence, and because word boundaries are poorly defined in continuous-speech signals.

*Steven Ross is senior software engineer/project leader at Verbex, Two Oak Park, Bedford, MA 01730, where he is responsible for product algorithm development. He holds a BS in electrical engineering and computer science from the Massachusetts Institute of Technology and an MS in computer science, also from MIT.*

*Jeff MacAllister is principal systems engineer at Verbex, where he is responsible for new product development. He holds a BS in electrical engineering from MIT.*

### Some systems require unnatural speech

To overcome these problems, isolated-word systems require sustained pauses between words. This approach, which provides obvious word boundaries and encourages consistent pronunciation, simplifies the recognition process. However, it also places an unnatural constraint on the speaker that ultimately limits throughput.

Although the SUR project achieved significant developments in the continuous-speech-recognition field, the systems developed for the program demanded immense amounts of computation and ran many times slower than real time on mainframe

computers. Picking up where the SUR program left off, Verbex developed a speech-recognition algorithm that can run in real time on low cost hardware configurations.

To interpret continuous speech, the Model 3000 employs a grammar to specify all meaningful, legal utterances that might be spoken (see Panel, "Grammar in speech recognition"). Through a deferred decision-making approach, the system can recognize each grammar as a unit (see Fig 1). This technique contrasts with some isolated-word approaches that use a branching structure of subvocabularies to specify a recognition sequence. To determine successive subvocabularies, systems using such approaches must recognize each word as it is spoken. Moreover, an early mistake can force the system to take a wrong path through the network of all possible utterances.

To avoid such pitfalls, the Verbex algorithm continually examines multiple parallel hypotheses by simultaneously comparing input data with the grammar-defined set of all legal utterances. It discards hypotheses only after obtaining sufficient evidence against their validity, and it defers reporting recognition until a complete legal sequence is spoken.

The algorithm's grammatical constraints operate in both word-sequence directions—that is, from left to right and from right to left, so that each word provides clues about the words spoken before it and after it. The system knows the syntactic context of

## Grammar in speech recognition

A simple example of a typical grammar illustrates the power of continuous speech recognition. In this example, an inspector verbally reports defects as they are encountered. In the case of PC board inspection, for example, the inspector verbally inputs a defect followed by its location. Defects consist of defect-type specifications followed by the actual problem encountered. Locations are specified by their proximity to a part that is described by one of four letters, followed by one or more digits. The grammar, as expressed in Verbex grammar notation, a variant of BNF, is shown in the Table.

In the notation, alternatives are listed on adjacent lines, and concatenated words are listed left to right. Names preceded by a period indicate that they refer to compound grammatical structures that must also be defined. If there is no period at the beginning of a name, the name refers to a vocabulary word. Square brackets indicate that the enclosed grammatical structure is optional. The plus sign indicates that the immediately preceding grammatical structure may be repeated one or more times. This notation permits the specification of any grammar that can be recognized by a finite-state automation. Fig 1 shows a finite-state graph representation of the grammar as noted above.

Sample legal utterances include "die wrong above R 6 7," "die metallization near A 8," "capacitor missing Z 1 2 3 4." But, even though all the words in the vocabulary are known by the system, the utterances "U missing above diffusion" and "substrate damaged above 2 below 3" are unsuitable because of the constraints that the grammar places on the allowed utterances. For example, only four words may appear as the first word in the utterance, and the one said determines which words may appear as the second word in the utterance.

The reverse is also true. Knowing the second word in the utterance helps to constrain what the first word might have been. If the second word is "missing," the first word must have been either "die" or "capacitor." The deferred decision-making approach enables the Model 3000 to make use of these constraints in both directions. Also, similar words such as "Z" and "3," might be difficult to distinguish, but "Z" can never follow another letter or digit, while "3" can never be the beginning of a part location.

### Grammar Notation

| | | | |
|---|---|---|---|
| .inspect | : : = | .defect | .location |
| .defect | : : = | substrate | .subdefect |
| | | die | .diedefect |
| | | capacitor | .capdefect |
| | | header | .hdrdefect |
| .subdefect | : : = | cracked | |
| | | chipped | |
| | | metallization | |
| | | contamination | |
| | | bonding | |
| .diedefect | : : = | wrong | |
| | | missing | |
| | | damaged | |
| | | metallization | |
| | | confusion | |
| .capdefect | : : = | wrong | |
| | | missing | |
| | | defective | |
| .hdrdefect | : : = | plating | |
| | | clearance | |
| | | grounding | |

| | | | |
|---|---|---|---|
| .location | : : = | [.preposition] | .partlocation |
| .preposition | : : = | above | |
| | | below | |
| | | near | |
| | | left-of | |
| | | right-of | |
| .partlocation | : : = | .letter .digit$^{+}$ | |
| .letter | : : = | U | |
| | | Z | |
| | | R | |
| | | A | |
| .digit | : : = | 1 | |
| | | 2 | |
| | | 3 | |
| | | 4 | |
| | | 5 | |
| | | 6 | |
| | | 7 | |
| | | 8 | |
| | | 9 | |
| | | 0 | |

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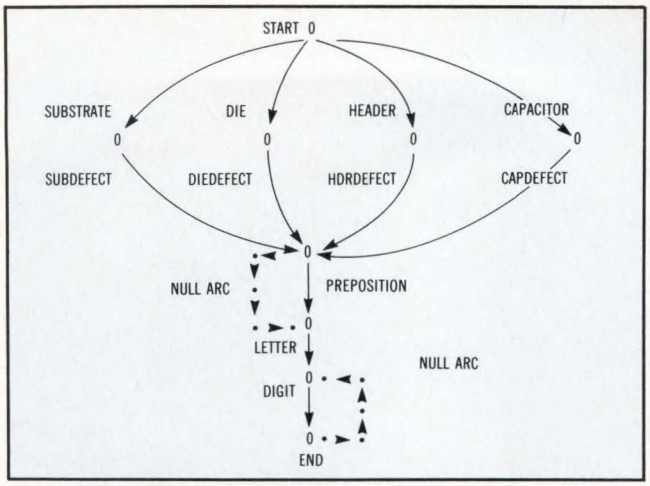


**Fig 1 This finite-state graph representation of a grammar for an inspection process illustrates that only four words can appear as the first word in an utterance.**

the utterance, so it can eliminate many unmeaningful interpretations of speech and nonspeech inputs, such as speaker interjections and background noise. This improves accuracy.

To further improve accuracy, word models stored in the system allow it to accommodate the variations in the users' pronunciation and cadence. A two-phase process builds the word models. In the first phase, enrollment, the user speaks each vocabulary word a few times in isolation, allowing the system to characterize the word's baseline pronunciation. In the training phase, the user speaks a representative subset of the legal utterances that make up the application grammar. This allows the word models to be refined to match the pronunciation of realistic, continuous speech. The enrollment and training phases require about 1 min/word.

Because the Model 3000 is speaker dependent, the system need only contain one pronunciation model for each word for the current user, thus reducing memory requirements. Although the underlying word-model structure is Markovian, some of the Markov word-model constraints have been relaxed. This step has reduced computational requirements by a factor of five without significantly affecting recognition accuracy.

## Hardware selection

Adept at pattern-matching operations requiring a fast multiplier and rapid access to large amounts of memory, the system's single-board speech processors use 2901 chips. This enables flexible construction of fast, pipelined computer systems with large memory spaces. The Model 3000's star architecture (Fig 2) includes from two to four such processors and can handle from 120 to 360 words. Each processor contains 1/4 Mbyte of data memory as well as program memory storing 4000 microcode instructions, each with 64 bits. Horizontally microprogrammed, each speech processor executes 5 million instructions per second (MIPS).

In the star architecture, the speech processors surround an 8086-based control processor that coordinates the speech processors, merges their results, controls data exchange between various system elements, and communicates with a host computer. The control processor is equipped with a 1/2 Mbyte of RAM into which a portion of the speech-processor memory is mapped. The processor maintains, loads, edits, and stores grammatical and vocabulary information for each application, as well as enrollment and training results for each user. The system uses an IEEE 796 bus for interfacing with a variety of standard and specialized modules, including the speech-processor boards.

Other system features include an audio I/O board, a 1-Mbyte floppy disk, and three RS-232-C interfaces for connection to a user's host computer or other terminals. Options include a second 1-Mbyte floppy disk, a 10-Mbyte Winchester disk, a printer, and additional speech processors for larger vocabularies.

The system's parallel-processor architecture allows it to rapidly accomplish the computation that the continuous-speech-recognition algorithm requires. In essence, during recognition the system attempts to find the legal sequence of words that most closely corresponds to the observed spoken utterance. The system must first extract the features of incoming speech and match these features against stored word models. Then, it must perform a global dynamic programming search to find the minimum-cost path through the network of possible utterances contained in the application grammar.

When a user speaks into a directional microphone headset, the analog speech waveform goes to the audio processor. There it is amplified, filtered, and digitized at a sampling rate of 16 kHz by a 12-bit

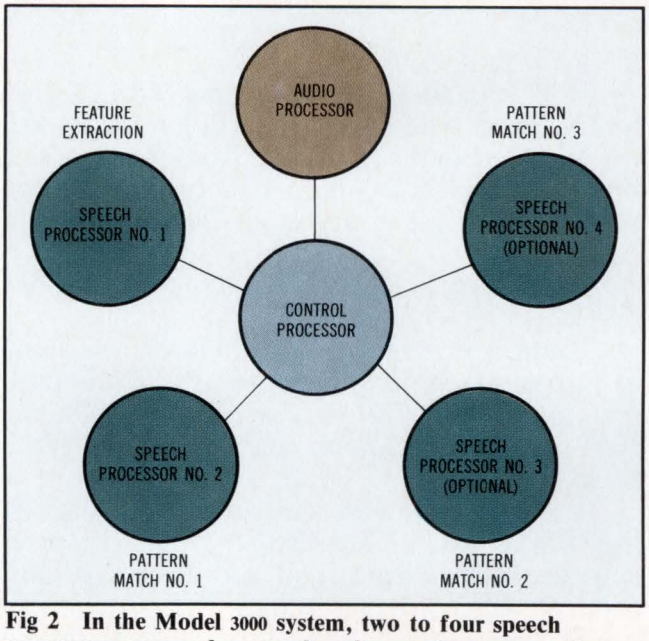


**Fig 2 In the Model 3000 system, two to four speech processors surround an 8086-based control processor. One speech processor handles feature extraction; the others are responsible for pattern matching.**

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A-D converter. A first in, first out (FIFO) buffer transfers the digitized waveform to the 8086 control processor at 10-ms intervals.

The control processor passes the waveform to the first speech processor, which is dedicated to feature extraction. This speech processor first performs a spectral analysis of the incoming signal. Then, a principal-component transformation translates the results of the spectral analysis into a set of features. These features emphasize the information-bearing components of the waveform.

Earlier Verbex systems utilized auto-correlation in addition to pure spectral analysis (without principal-component reduction) to identify 96 features in each 10-ms interval. For the Model 3000, after testing recognition accuracy with 32, 24, 16, and 8 principal component features, the designers found that a 16-feature template was sufficient for 99 percent word-level accuracy in operational conditions. Reducing the number of parameters by a factor of six results in significantly less memory requirements and speeds up template loading and matching processes. The parameterized 10-ms frame is returned to the control processor, which stores it until the remaining speech processors need it for pattern matching.

Responsibility for pattern matching is shared among the remaining one to three 2901 speech processors. Pattern matching consists of template matching and a dynamic programming search to identify the word sequence that best corresponds to the parameterized frames of a spoken utterance. In template matching, the system attempts to match the parameterized signal against the stored components of each word model. Developing a low cost template-matching alogorithm helps save on computation requirements. Moreover, a streamlined template-matching process is used, in which templates are only matched if they are part of a valid hypothesis about what utterance might have been spoken.

### Keeping a hold on vocabulary

Each speech processor contains a portion of the system's total vocabulary and possesses a copy of the entire active grammar. The standard resident vocabulary is 120 words and is stored in the processors' RAM. By increasing the number of bit-slice processors, vocabulary can be tripled in size to 360 words. At any one time, the utterance the system is attempting to recognize is defined by the active grammar, which refers to a subset of the resident vocabulary. For most applications, the vocabulary usually contains from 60 to 180 words, depending on computation complexity and grammar configuration.

During pattern matching, a dynamic programming search finds the word sequence that provides the best overall match to the input features. The dynamic-programming graph search is performed over a network that consists of the finite state grammar (ie, a representation in network form of all possible legal utterances) with the word-model

### Algorithm software development

Continuous speech recognition is a complex process, and the success of any system depends on the sophistication and efficiency of the recognition-algorithm software. To tackle the problem of developing software that could perform the large amounts of parallel computation required in continuous speech systems, Verbex has developed two simulators as well as a special language.

The first simulator, implemented in the C language on a DEC VAX 11/780, serves to verify the design of the algorithm software, although it does not operate in real time. Concurrent with the hardware development, the second simulator emulates the hardware. This allows verification of the microcode derived from the first simulator.

Although the highly parallel characteristics of the speech processor's horizontal microcode would enable the recognition algorithm to run extremely fast, programming exclusively at the microcode level would be time consuming and expensive. To speed the software development, a machine-dependent, high level language (MDHL) is designed, which offers the accessibility and transparency of a high level language without sacrificing too many of the microcode's advantages.

The MDHL serves primarily to program uncritical operations not involving frequent time-consuming loops during the speech-recognition process. It thus allows programmers to focus on manually optimizing the 10 to 20 percent of the microcode executed most often. By abstracting those horizontal-microcode elements that least concern the programmer, the MDHL reduces programming time by a factor of 10; each MDHL line services about three microcode lines. The MDHL provides control and data-structure primitives that enhance program readability, and it eases translation of the algorithm from C.

The MDHL optimally allocates registers based on the entire program structure, an important task because the speech processor has only 16 registers, while programmers have to deal with more than 200 variables. With the MDHL's register allocation, programmers could use symbolic register names, and the MDHL would automatically handle allocation and parameter passing among subroutines, thus eliminating the save/restore overhead normally associated with subrouting invocation. Potential register conflicts could be flagged so that programmers could decide which variables to store in memory.

This development process enables most software development to take place independently of hardware development. MDHL, which resembles C, eases speech-processor programming since the portion of the algorithm software residing in the control processor is able to be transferred directly (in C, with a small amount of assembly-language optimization for the sake of speed) from the simulator to the control processor. Furthermore, after hardware integration, verification tests could be performed on the VAX simulator and the hardware. This helps to distinguish between hardware and software problems.

networks spliced in. Incremental costs in time for the search are determined by template matching, as described above. The global nature of the system's dynamic programming search ensures that it takes full advantage of the syntactic constraints provided by the grammar. Therefore, detection of a particular word in the utterance helps to constrain, and thus helps to successfully recognize the sets of words that might have been said both before and after the recognized word.

### End-of-utterance detection

Since each speech processor performs dynamic programming over nonoverlapping portions of the grammar, control over reporting a recognized utterance resides in the control processor rather than in an independent speech processor. After every 10-ms frame of pattern matching, the control processor merges the grammar states of all the speech processors to keep them synchronized. Each speech processor reports to the control processor what it considers to be the most probable state of the utterance, which the control processor then records in a traceback network. The control processor reports back to the speech processors on the merged results of every frame. This prevents the speech processors from diverging in their hypotheses and ensures consistency during dynamic programming.

*During pattern matching, a dynamic programming search finds the word sequence that provides the best overall match to the input features.*

The control processor continues to add to its traceback network characterization of the history of the matching process over time. Using "partial traceback" techniques helps reduce the size of the traceback memory so that it is proportional to the length of a word, rather than to the length of an utterance, thus reducing memory requirements by a factor of five or more. The control processor recognizes that it has come to the end of an utterance when it detects that a complete, legal utterance has been spoken. It then traverses backwards in history through the traceback network to reconstruct the interpreted utterance.

This grammar-based approach to end-of-utterance detection differs significantly from other speech-recognition systems. These systems detect the end of a word or an utterance by listening for a sustained drop in the amplitude of the speech signal. Because the Model 3000 does not report a recognition, it does not stop listening until it has found a legal utterance. Thus, it reduces the chance of extraneous triggerings from background noise or irrelevant speech and in many cases, allows users to pause between words without jeopardizing the recognition. For a seven-digit grammar representing, for example, a phone number, the system will not detect end-of-utterance until it has heard all seven digits, even if the speaker pauses in the middle of the string.

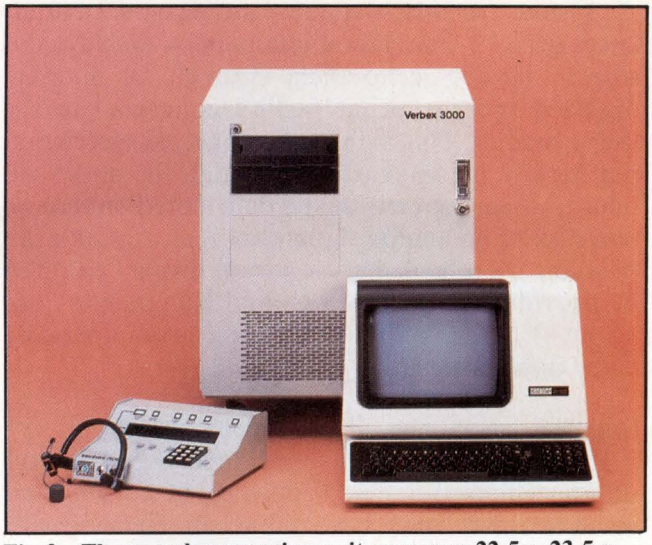


**Fig 3 The speech-processing unit measures 22.5 x 23.5 x 26.5 in. The user workstation features a microphone headset the user employs to input verbal data and commands.**

The system's highly hierarchical control software is based on the RMX-86 operating system, which was selected for its multitasking capabilities. The control software was written in C (see Panel, "Algorithm software development"), and consists of a system monitor, an application interface, and customer-specific, data-entry application software.

The application interface software is designed as a comprehensive set of speech functions that enables customer-specific voice-data-entry applications to be written easily, typically in a page or two of Pascal. The Model 3000 speech application development system (SPADS) allows users to write such applications. Users can transfer their applications to a standard Model 3000 system on floppy disk or use them directly on the SPADS system. All software is supplied, including that used for self-diagnostics, communications, enrollment and training, generic test application, as well as algorithm and system software.

Extensive human factors engineering is involved in the design of the system's external configuration (Fig 3). Because of speech processing unit is mounted on wheels and measures only 22.5 x 23.5 x 26.5 in., users can conveniently place it in or out of the work area. The user workstation includes a lightweight wired or wireless directional microphone headset through which the user inputs verbal data and commands. The workstation also contains audio processing electronics to amplify the speech waveform.

For data entry applications, immediate verification of the recognition accuracy is highly desirable. For immediate verification of recognition accuracy,

the system can either visually echo recognized utterances on a 32-character alphanumeric display console or audibly echo them through an optional digitized speech output facility connected to the user's headset. This high quality digitized speech output facility is implemented through the audio I/O board, which converts digital data stored on the system disk to an analog signal that recreates natural, pleasant speech. A remote visual display can also be provided, as well as a Digital Equipment Corp VT-102 CRT terminal for developing customized data entry applications.

### Practical advantages of continuous speech

Constrained grammars, grammar-based end-of-utterance detection, and sophisticated word models result in a data-entry system that can reject virtually all superfluous noise or interjected words. These features contributed to the high accuracy achieved in field tests. There are, however, subtler advantages provided by continuous-speech recognition. Most data-entry applications are based on visual inspection of materials or documents and can also involve physical handling of certain materials. Entering data verbally frees up eyes and hands and permits mobility, thus maximizing the efficiency of data entry. When workers enter data in their natural voices, without staccato-like rhythms or artificial pauses, they do not need to concentrate on the data-entry method. Instead, they can concentrate on the task at hand. Data is therefore captured at the source, without intermediate transfer steps, helping to reduce data-entry errors and increase throughput.

The system can increase the speed and accuracy of shipping and inventory transactions while it eliminates error-prone, record-keeping steps. It can enhance and accelerate inspection and quality control tasks, helping to reduce repairs and to improve product reliability and worker productivity. As a man/machine interface with computer aided design/computer aided manufacturing systems, the unit allows designers to focus on their work without spending time mastering a keyboard or other input controls, particularly when high amounts of symbol, label, or other data entry are required.

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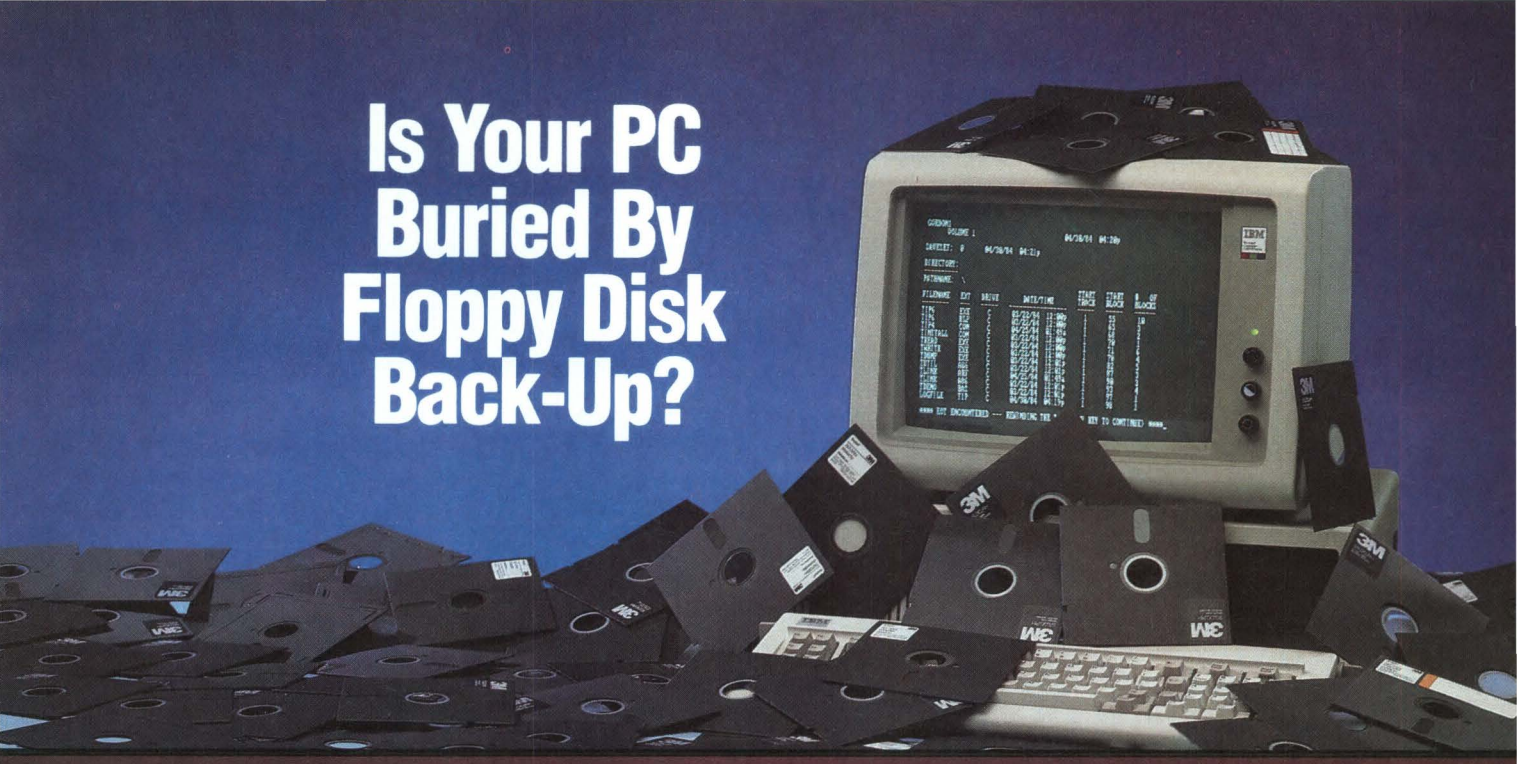
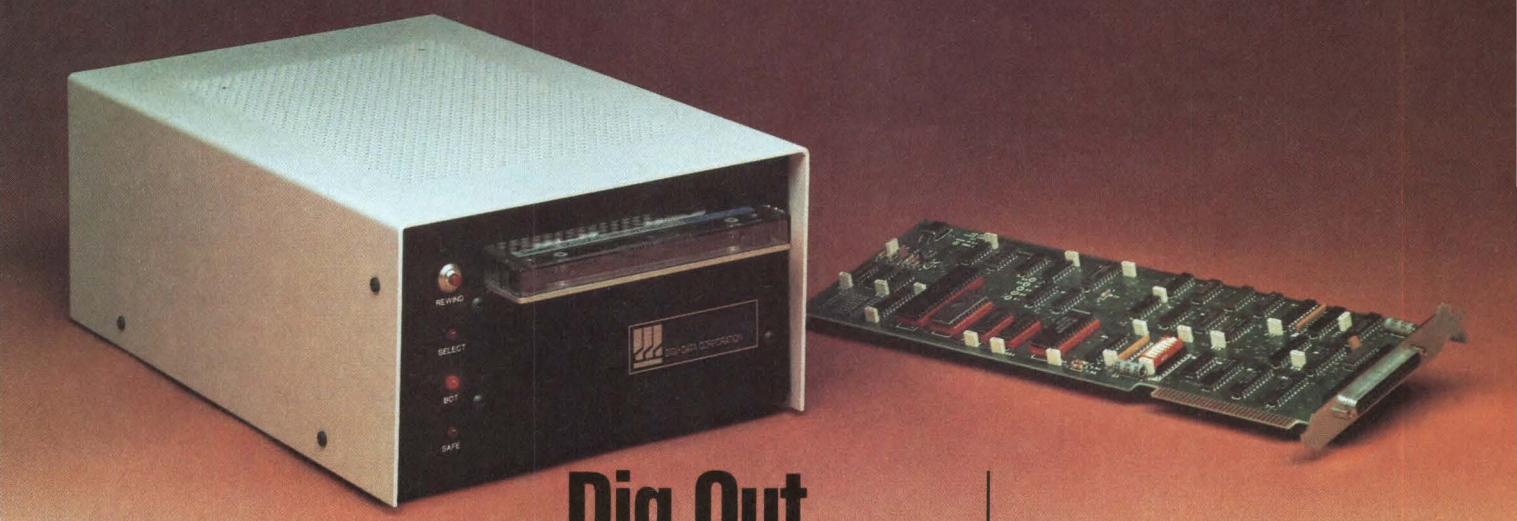
*High 704* *Average 705* *Low 706*

# Is Your PC Buried By Floppy Disk Back-Up?



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CIRCLE 46

# The Hitachi CMOS 6300 Family— 8-Bit, Single-Chip Microcomputers

## The Real Performance Leader

The 63B01 offers you a powerful CPU and high-speed operation for systems requiring complex and fast data processing. Here's how it compares with the 80C51.

## Benchmark Study

| | Execution Time (μs) | | Code Efficiency | |
|---|---|---|---|---|
| | 63B01 | 8051/ 80C51 | 63B01 | 8051/ 80C51 |
| XTAL (MHz) | 8 | 12 | 8 | 12 |
| Instruction Cycle Time (μs) | 0.5 | 1 | 0.5 | 1 |
| **TASK** | | | | |
| Binary Multiply | 39 | 42 | 37 | 43 |
| Bit Manipulation | 6.5 | 6 | 8 | 8 |
| Logical Operations (AND/OR) | 7 | 3 | 11 | 6 |
| Nibble Comparison | 11 | 12 | 29 | 29 |
| Interrupt Processing | 11.5 | 21 | 1 | 19 |
| **TOTALS** | **75** | **84** | **86** | **105** |

Execution time for the 6301 ranges from 0.5 μs (2 MHz) to 1 μs (1 MHz) depending on the model, at a wide range of operation: Vcc = 3V to 6V. And an error-detecting function prevents illegal op-code and illegal addresses.

Other enhancements of the 6300 Family include upward source and object code compatibility with the HD6800 and bus compatibility with the MC6800 Family.

## All the Support You Need

Hitachi's comprehensive development support includes evaluation kits, emulators, prototyping devices, and cross-software packages running under CP/M on personal computers and under ISIS-II on Intel development systems.

The 63P01 offers piggyback flexibility, which lets you "fine tune" programming before committing to a final ROM code. All this development support is available now for you to start your design.

## Enviable Track Record

The 6301 has been in mass production for more than two years. Five million units are now the brains behind hand-held terminals, briefcase computers, printers, digital switches, phones, modems, and automotive spark control computers.

## Available in Quantity

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Stop-Start Serial Communication Interface
16-Bit Timer
8 x 8 Multiply Instruction
Low Power Consumption Mode (60mW)
Sleep Mode (10mW), Standby Mode (10μW)
Instruction Cycle Time: 0.5μs
40-Pin Package

| Part No. | Architecture |
|---|---|
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| HD6303 | External ROM |
| HD63P01 | Piggyback EPROM |

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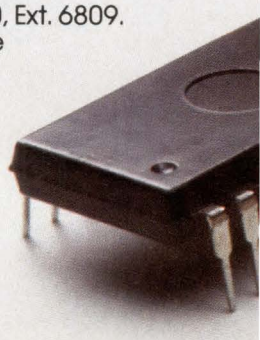

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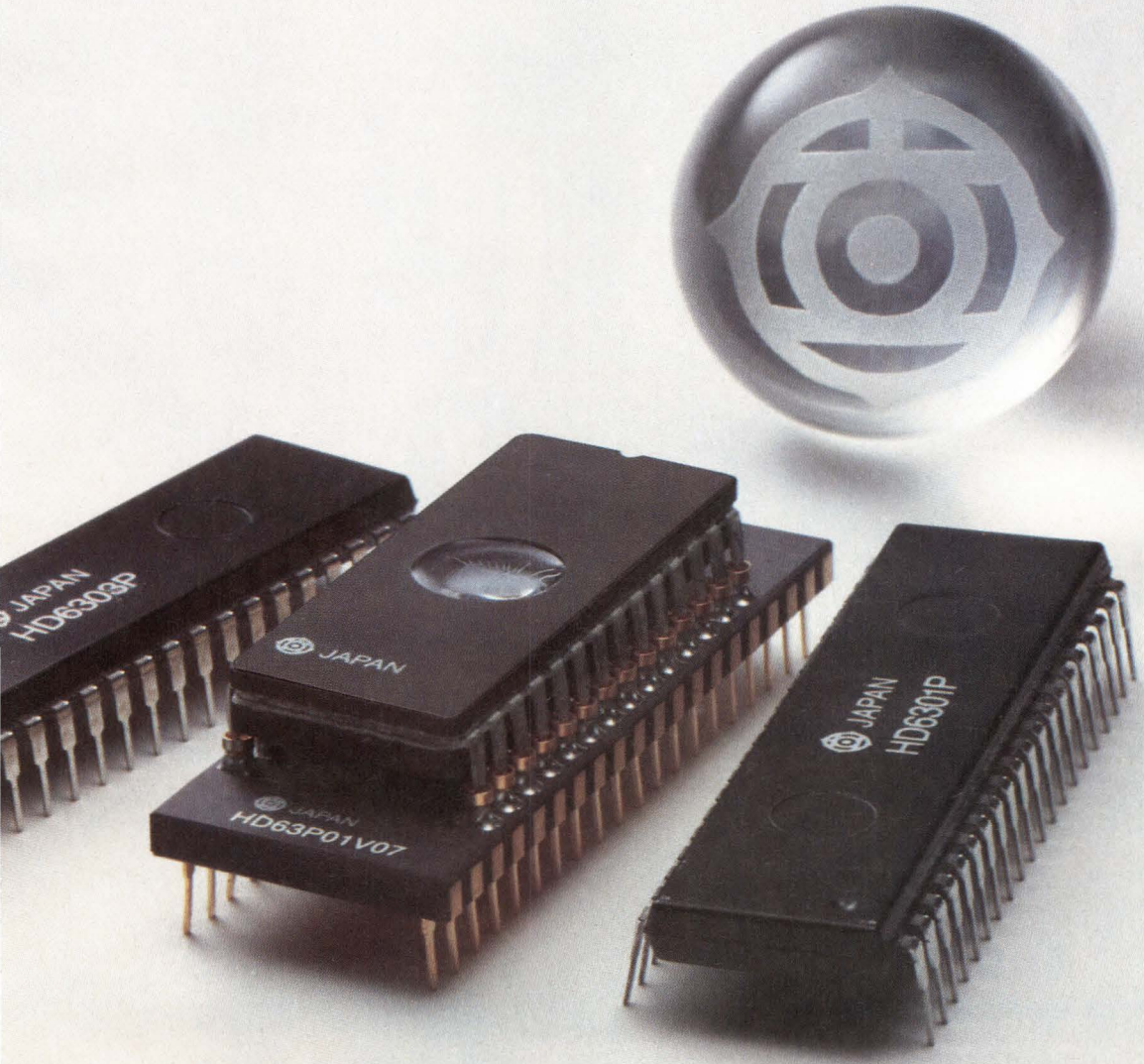


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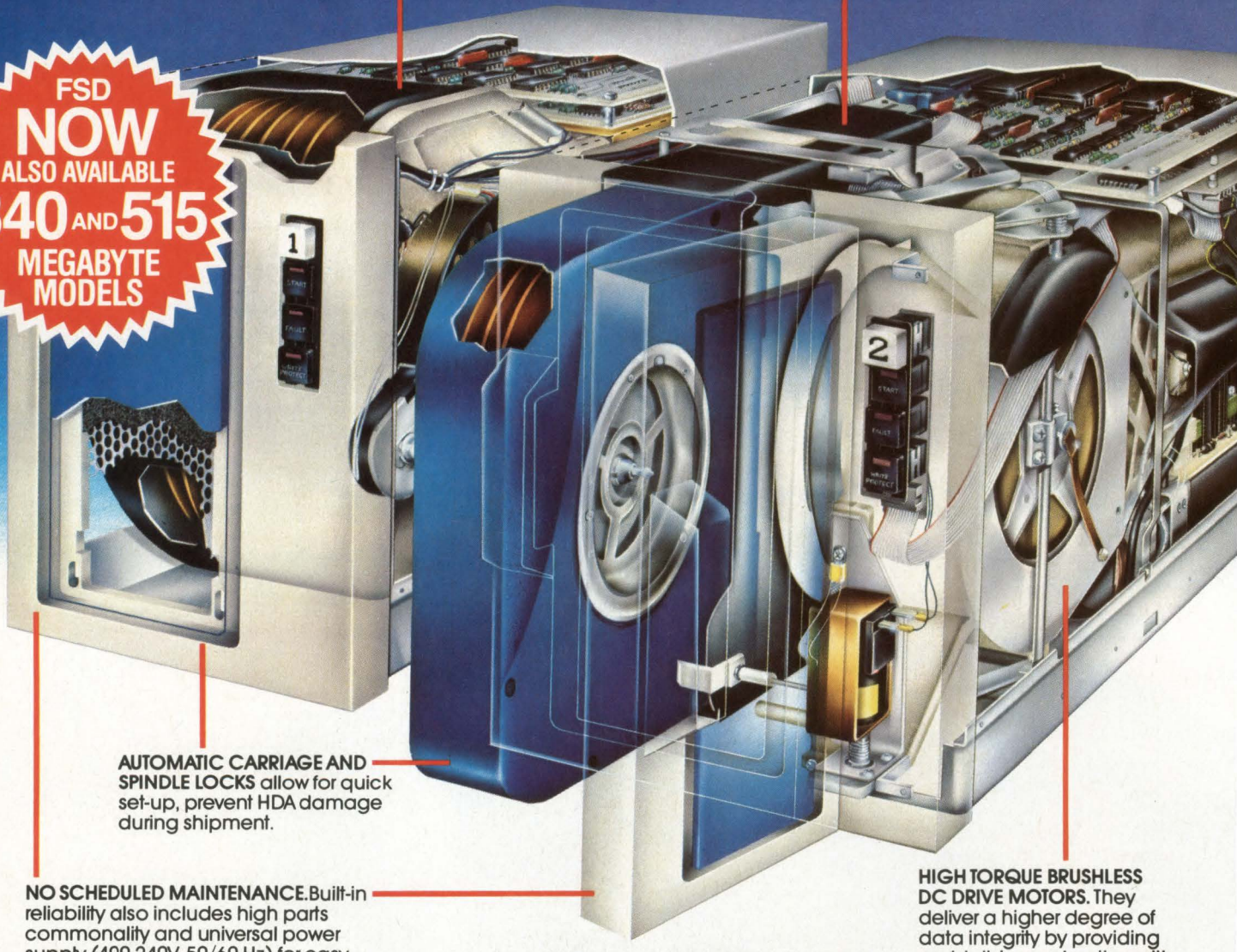


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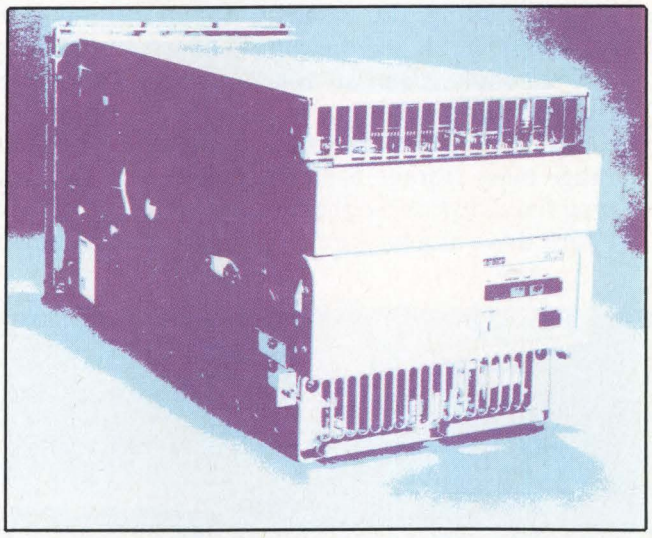
CIRCLE 48

# REMOVABLE DISK DRIVE PROVIDES HIGH END MUSCLE

**To keep ahead of the competition, designers set their sights on a compact Winchester drive with a removable cartridge, borrowing heavily from the world of larger, fixed-platter memories.**

**by Carl J. Blatchley, Shyam C. Parikh, Fernando A. Zayas, and Jack Cole**



In response to the shrinking size and decreased cost of computers, disk drive makers are under pressure to design smaller, yet higher capacity systems. Furthermore, where rapid advancements in circuit integration have significant impact on reducing a computer's size, the factors surrounding a disk drive's overall package are also linked to a broader range of considerations. Among these are the performance characteristics of mechanical systems and magnetic materials.

This demand for a smaller drive with better performance, as well as the competitive spur to hold down prices, has led one group of storage system designers to develop a drive that draws on a multitude of innovations and features not usually associated with midrange performance Winchester disk drives. The resultant design is a fixed/removable unit that has significant advantages over others in its class, and requires less space than a comparable unit.

The design goals for the recently announced RC25 fixed/removable disk drive subsystem are to achieve both a higher storage capacity-to-volume ratio and a smaller footprint in comparison to the drives it would replace in midrange computer systems. The Table compares the RC25 with three recent removable-disk midrange drives. As shown, the newer drive is smaller and more lightweight than these drives, and it is compared to other currently available drives as well. Even where space and weight considerations are relatively unimportant, the improvement in data capacity—to 26 Mbytes per platter—is substantial.

The total space occupied by the drive is minimized by integrating the platter mechanics, drive electronics, controller, and power supply into a single subsystem

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*Shyam C. Parikh is senior engineering manager at DEC. He holds an MSEE from City College of New York.*

*Fernando A. Zayas is principal engineer at DEC. Mr Zayas holds a BS in computer science from the Georgia Institute of Technology.*

*Jack Cole was a consulting engineer with DEC when this article was written. He is now an independent consultant. He holds a BSEE from Michigan State University.*

**Comparison of RC25 with Three Removable-Disk Midrange Drives**

| Drive model | Type | Total data capacity | Areal density | Volume | Footprint | Weight |
|---|---|---|---|---|---|---|
| RC25 | integral | 52 Mbytes | 12.3 Mbytes/in.$^2$ | 1.2 ft$^3$ | 1.4 ft$^2$ | 50 lb |
| RC25 | rack | 104 Mbytes | 12.0 Mbytes/in.$^2$ | 2.6 ft$^3$ | 2.9 ft$^2$ | 120 lb |
| RL02 | rack | 10.4 Mbytes | 0.9 Mbytes/in.$^2$ | 2.9 ft$^3$ | 3.3 ft$^2$ | 75 lb |
| RK0M | floor | 28 Mbytes | 1.55 Mbytes/in.$^2$ | 15.4 ft$^3$ | 4.2 ft$^2$ | 326 lb |
| RM02 | floor | 67 Mbytes | 2.3 Mbytes/in.$^2$ | 15.2 ft$^3$ | 4.7 ft$^2$ | 430 lb |

package. At the same time, it is necessary to maintain an 8-in. platter in order to offer high reliability, superior performance, and a storage capacity adequate for the needs of midrange computer systems. The drive's design thus requires that every aspect be evaluated for the best trade-offs of performance and size, including the strategy for positioning the read/write head, and the choices of servomechanism, power supply, clean-air system, heads, control electronics, and packaging.

In recent years, the basic configuration for midrange mass storage has consisted of a Winchester-type fixed disk and either a removable disk drive or a tape drive as a backup or software loading device. Although a fixed drive with tape backup remains the most common mass-storage arrangement, the tape cartridge occupies more space and is slower and less convenient than an equivalent disk drive.

## Putting performance first

Opting for the higher removable disk performance, the RC25 uses a removable, front-loading cartridge on a single spindle with the fixed platter. The fixed/removable disk drive subsystem is currently packaged as an integral part of the VAX-11/725 system (Fig 1). The 8-in. fixed disk and 8-in. removable-cartridge disk each have 26 Mbytes of formatted data storage, giving the system a 1:1

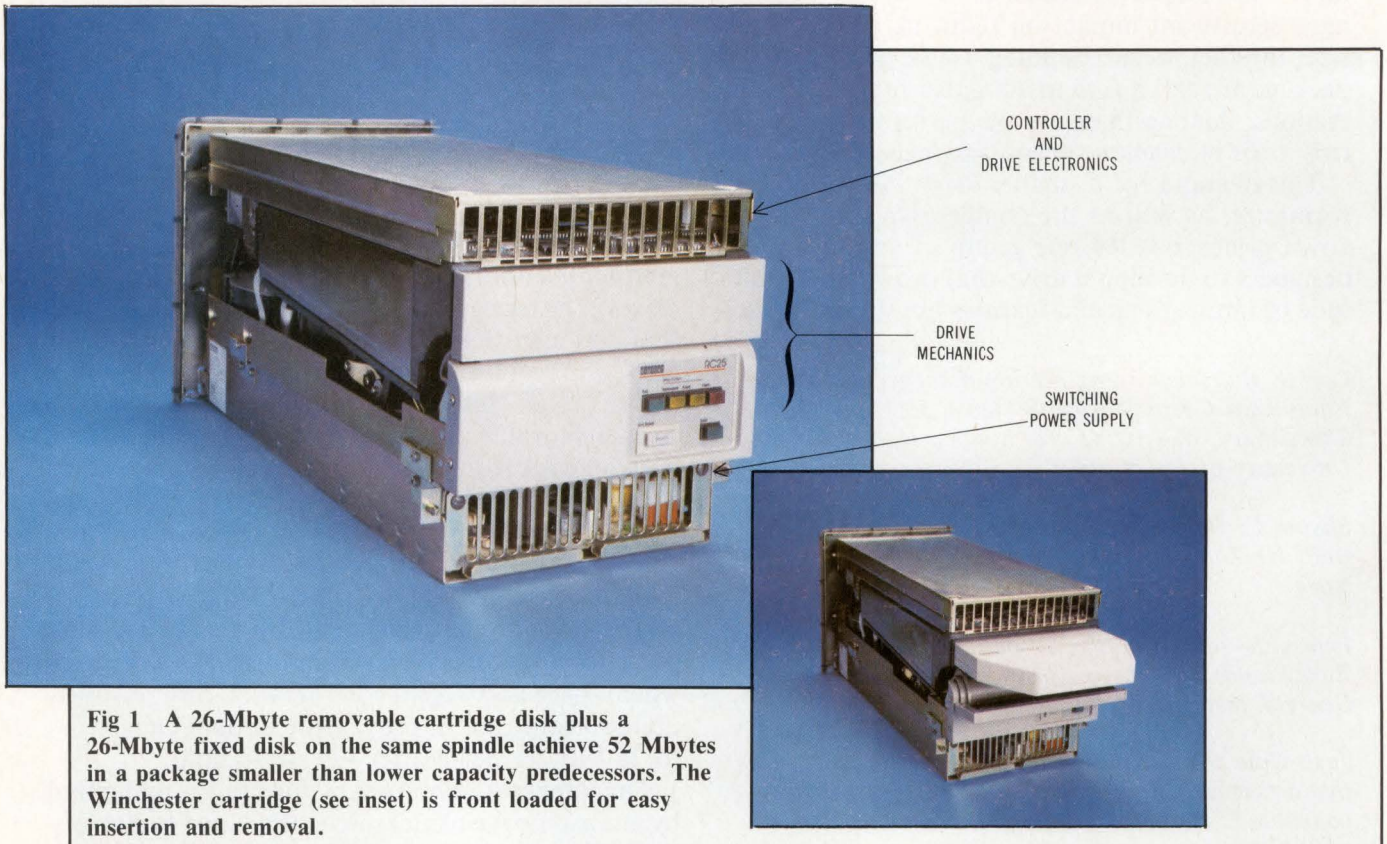


**Fig 1 A 26-Mbyte removable cartridge disk plus a 26-Mbyte fixed disk on the same spindle achieve 52 Mbytes in a package smaller than lower capacity predecessors. The Winchester cartridge (see inset) is front loaded for easy insertion and removal.**

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backup ratio. The minimum configuration of a single-spindle fixed/removable master disk drive is expandable to a slave disk drive via the master disk drive's integral controller. The slave disk drive has no controller module and is cabled to that of the master. Otherwise, the master and slave drives are the same.

To pack the most storage capacity into the least space, track density is pushed to 1000 tracks/in. According to the designers, this is higher than any other removable disk drive. Instead of a linear read/write head-positioner, the drive has a rotary positioner (Fig 2), which requires less space and power, and weighs less than typical linear positioning systems. In addition, mounting the shaft on a high stiffness, aircraft-type bearing treated with a special lubricant gives it the needed accuracy.

For noise immunity, the servosystem's tachometer, which provides velocity feedback as the heads move from track to track, is a double-coil magnetic type. This design rejects extraneous electromagnetic fields, yet still measures the velocity of the heads precisely. The tachometer's high bandwidth aids in settling the heads into place and desensitizes the servosystem to external vibration and mechanical shock. Counterbalancing the positioner arms also minimizes the effect of vibration and shock.

Servo information is embedded between the disk's data carrying sectors at the factory, thus alleviating the need for the head alignment often associated with dedicated servo-driven, head-positioning systems. This embedded information occupies less space than with dedicated systems and yields a higher data capacity. In addition, an adaptive runout correction scheme eliminates the effects of nonconcentric tracks with respect to the axis of rotation, thus helping the servosystem to follow the drive's narrow data tracks.

### Advantages of a switching power supply

An important step toward reducing the drive's overall package size is to power it with a switching, rather than with a linear, power supply. The switching power supply's advantages over the linear type—approximately 80-percent efficiency compared to 50 percent and substantially smaller, lighter, and less expensive power transformer and filter capacitors—produce a unit that mounts on a single hex-sized module measuring 8.5 x 15.6 in. A comparable linear power supply would require twice the space and add to the drive's cost and weight. On the other hand, it is necessary to provide special filtering, shielding, and grounding to suppress the noise spikes that accompany the switching supply. These spikes are a curse to the analog sections of the drive's read, write, and servo control circuits.

The drive's clean-air system features another innovative design. Despite the removable nature of the disk cartridge, the air inside it, as well as in the fixed disk space, is maintained at a better than class

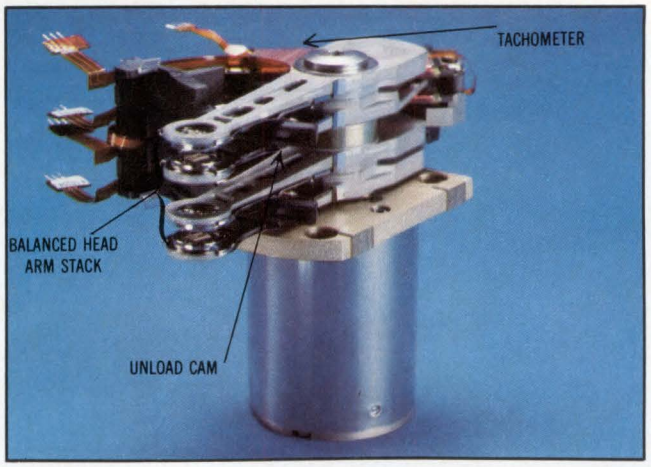


**Fig 2 The drive's rotary-type head positioning mechanism requires less space, consumes less power, and weighs less than its linear motion counterparts. A high stiffness, aircraft-type bearing adds to positioning accuracy, while the counterbalanced positioner arm resists shock and vibration.**

100 rating (100 particles of 0.5 $\mu$m or larger per cubic foot). This level is possible due to the drive's positive-pressure airflow system. A single centrifugal fan mounted on the bottom of the spindle motor moves interior air through a recirculating filter. To overcome any leakage, this fan brings in exterior air through a second filter that is 99.98 percent efficient. Moreover, the drive's clean-air system is independent of the electronic's cooling-air system. Yet, to save space and minimize acoustical noise, one dual-inlet centrifugal fan cools both the electronics and the power supply.

To prevent contaminants carried in the ambient air from entering the removable disk cartridge, a locked head actuator door on the cartridge automatically opens, but only when the cartridge is inserted. Likewise, the spring-loaded sliding door over the disk hub functions in a similar manner. This door also helps keep particles from interfering with the proper seating of the removable disk hub over the drive spindle.

The drive also overcomes one of the traditional disadvantages of loadable Winchester disks: the 2 min needed for the startup sequence. This time usually consists of spinning the disk up to speed, purging the filtration system, stopping the disk, loading the heads on the stationary disk, and spinning the disk up to speed again. Instead, a special head flexure design in the RC25 controls the head attitude precisely enough to permit the heads to load onto the disk while it is rotating. This reduces the startup sequence time required for spinning the disk up to speed, purging the system, and loading the heads to less than a minute.

Many of the drive's advanced features are located in its controller. In addition to performing the usual control functions, the disk-resident controller is microprogrammed to perform many functions usually not found in the drive itself. This makes the drive's electronics both simpler and less expensive. The advantage is especially great in two-drive (eg,

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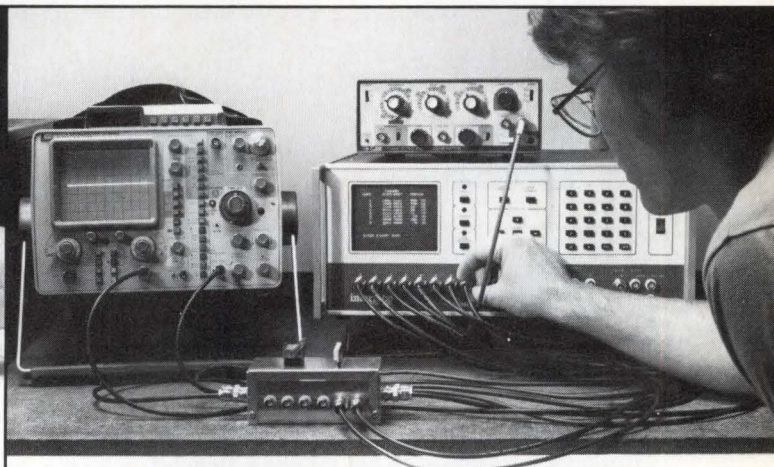

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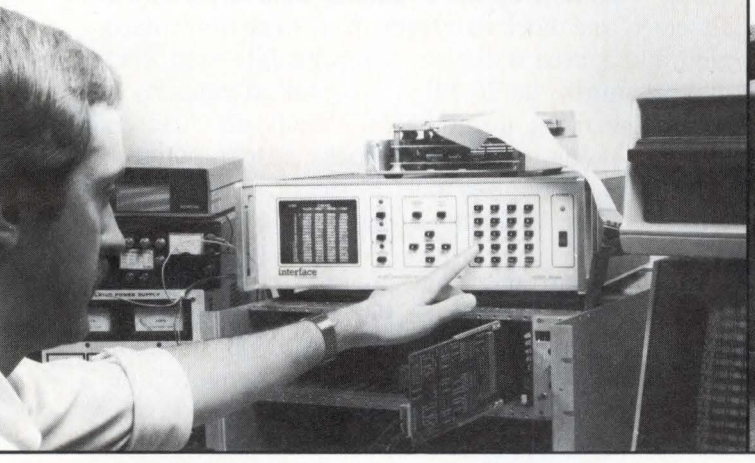
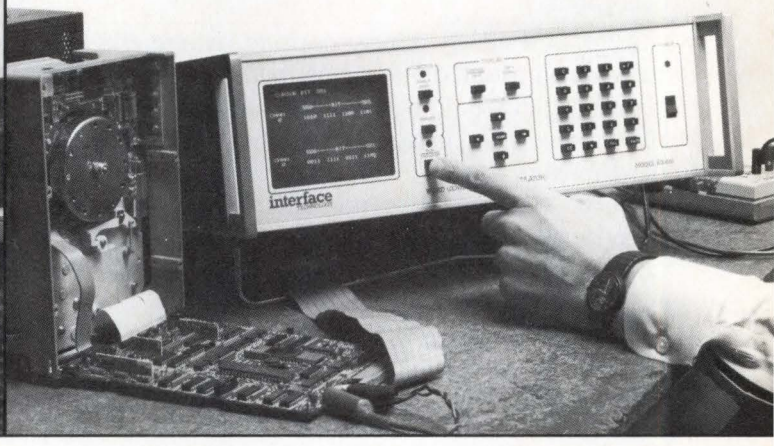


**DWGs eliminate building dedicated circuitry.**

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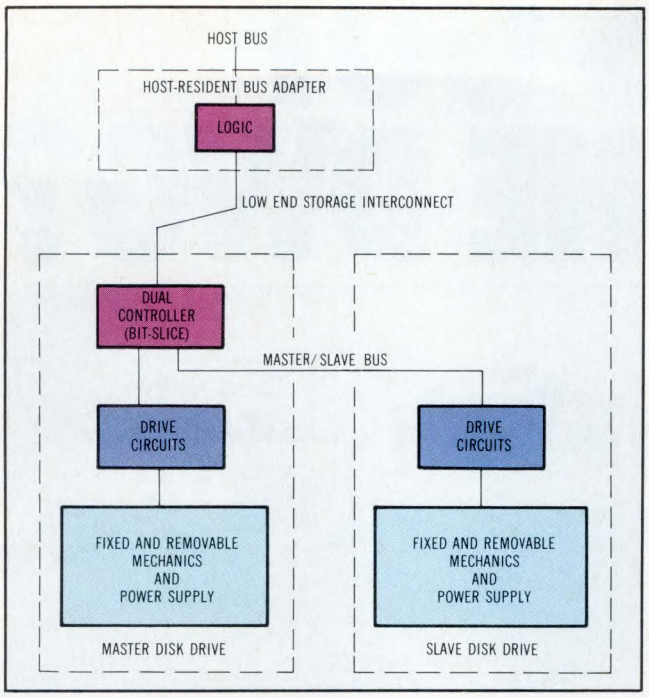


**Fig 3 The drive-resident controller is microprogrammed to perform various functions not normally found within the drive itself. This causes the subsystem electronics to be simpler and less expensive. In addition, a slave unit that does not contain its own controller can operate under the command of a master, thus simplifying a two-drive configuration.**

master and slave) configurations, where the extra microprogrammed functions in the dual controller replace what would be duplicate hardware in the separate drive circuits (Fig 3). Much of what would be off-the-shelf IC hardware in the controller is also replaced by three custom LSI chips: a serializer/deserializer that auto-correlates sync words and handles serial data flow, a Reed Solomon error correction code (ECC) generator, and an encoder/decoder that supports high density storage by converting 2-bit data groups into 3-bit groups for writing data, and reverses the conversion for reading data.

The dual-sequencer controller splits the two asynchronous processes of a disk drive: the exchange of data with the drive, and the exchange of data with the host. One sequencer performs disk I/O using memory internal to the controller for holding the data. The other sequencer performs I/O operations with the host and keeps the disk I/O sequencer fed with data. This split lets the drive be used with hosts of different speeds and loads while still optimizing transfer rates.

Many of the traditional host functions are handled by the controller. It accepts multiple requests from the host and internally queues them to the correct drive, and also handles all necessary retries and error corrections. Errors are presented to the host in the form of error-log packets that contain detailed information about the error, including the context in which it occurs. These features reduce the burden on the host and aid in the diagnosis of problems.

Since the controller queues up multiple commands for a drive, it can perform an elevator-type seek optimization. In master/slave configurations, the controller even overlaps its seeks between the two drives. The result, under heavy loads, is that the apparent average seek time of 35 ms actually drops to less than 20 ms. For realtime applications where timely completion of particular requests is more important than total system throughput, the drive lets selected requests bypass the optimization routine.

## Blocking out defects

The controller's dual-sequencer, bit-slice microprocessor offers a number of firmware attributes that contribute both to high areal density and good data integrity. One of these attributes is its bad-block retirement algorithm. Most data errors in a high density disk drive are caused by disk defects. The error rates can be improved by orders of magnitude by simply not using those areas of the disk containing defects. Much like the spare rows or columns of high density RAMs and ROMs, the disk contains spare areas called replacement blocks. The data that would normally be written in sectors with defects is instead written in defect-free replacement blocks.

The replacement-block area of the disk occupies about 3 percent of the available data area, and is allocated one block to a track. Yet, since the replacement block area is distinct from the data area, each disk maintains its 26-Mbyte formatted capacity in spite of varying numbers of defects on different disks. Locating replacement blocks close to potential defect areas minimizes their impact on performance. However, the majority of replacement blocks go unused.

In addition to the replacement-block backup for media defects, the drive's 170-bit ECC can correct up to 8 bytes located anywhere in a 512-byte sector. The actual corrections are performed in microcode. Moreover, the ECC is generated and checked by its custom LSI circuit.

As an added protection against failure in the controller's ALU, the data path, or the ECC chip itself, a checksum is computed on every sector as it is brought in from the host. This checksum stays with the sector as it travels inside the controller and goes out to the disk. When the data is later fetched from the disk by the controller, this checksum is recomputed and evaluated as the data is delivered to the host.

Quadruple redundant headers on each sector also provide an additional margin of immunity to disk defects and noise. The microcode checks that an acceptable number of copies match before it performs a read or write on that sector.

The ECC and redundant headers work in concert with the bad-block retirement strategy. The circuits and microcode analyze each soft error, whether it is in the data area or the header area, and determine if the error has the characteristics of a media defect

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or random noise. If the error does not have the effects of random noise, the data is read again. If the error persists, the sector is replaced. This mechanism allows blocks to be replaced automatically in the unlikely event that a defect develops after the drive leaves the factory.

However, certain kinds of data errors inherently cannot be corrected by an ECC. One example is an error in the sync mark that precedes the data, in which case the entire sector is read incorrectly. Some earlier designs would create this kind of error in the event of a single-bit error in the preamble, or if the sync bit itself was read incorrectly.

Because the drive uses a sync word instead of a sync bit, however, it is able to perform a bit-by-bit auto-correlation over the incoming serial data stream. This determines where the sync mark is and where the first word of the data begins. Since an auto-correlator is difficult and expensive to build, it is incorporated in the drive's custom LSI serializer/deserializer chip.

### Avoiding the impossible

Phase-lock loop failure is another source of uncorrectable errors, since it garbles an entire data block. Here again, custom LSI performs the best available algorithms without paying a penalty for size. In this case, the circuit detects that an error exists in the preamble and disables spurious attempts at correction that could prevent the loop from locking onto valid data.

In addition to its extensive data checking and error correction schemes, the drive automatically performs three types of diagnostics during power up. One test, for example, checks the controller logic (and can be invoked on command as well). A head-load test checks the digital, analog, and mechanical functions of the drive. Moreover, a port initialization test checks the quality of data transfers between the drive and host.

A user can run diagnostics on demand to verify the disk drive's seek and read/write error rates and to check for noise in the servo system. Since these diagnostics are contained in the drive, a host computer is not required. The user both initiates these diagnostics and learns their results through the front panel of each drive. For example, the controller continuously monitors each drive's error rates and reports unacceptable error rates to the user. The user can then take corrective action before the drive begins producing unrecoverable errors.

A fault light goes on when the drive makes an error that cannot be corrected by retries or other error recovery mechanisms. When the light flashes, the user presses the fault switch. The front panel then displays a fault code that identifies the field replaceable unit that has failed and provides the information to the host for such functions as remote diagnosis and error logging. The user again presses the fault switch, and the controller attempts to clear the fault and return to normal operation.

Additional drive-resident diagnostics can be run for quick verification when a field replaceable unit has been installed or when the system, rather than the disk drive, is believed to be the source of the fault. When a host computer is present, additional diagnostic capability exists. These host-resident diagnostics verify operation of the adapter card and its ability to perform DMA operations and interrupts.

In most drive subsystems, the controller connects directly to the host processor's bus. In the RC25's drive, however, a bus adapter connects to the host bus, allowing the drive to connect to a variety of host computers without changing controller hardware, controller microcode, or even any jumpers. Each adapter is a quad-size module (8.5 x 10.4 in.) for the Unibus and dual-size module (8.5 x 5.2 in.) for the Q-bus. The microprocessor-based controller itself fits on one hex module located inside the master drive's enclosure.



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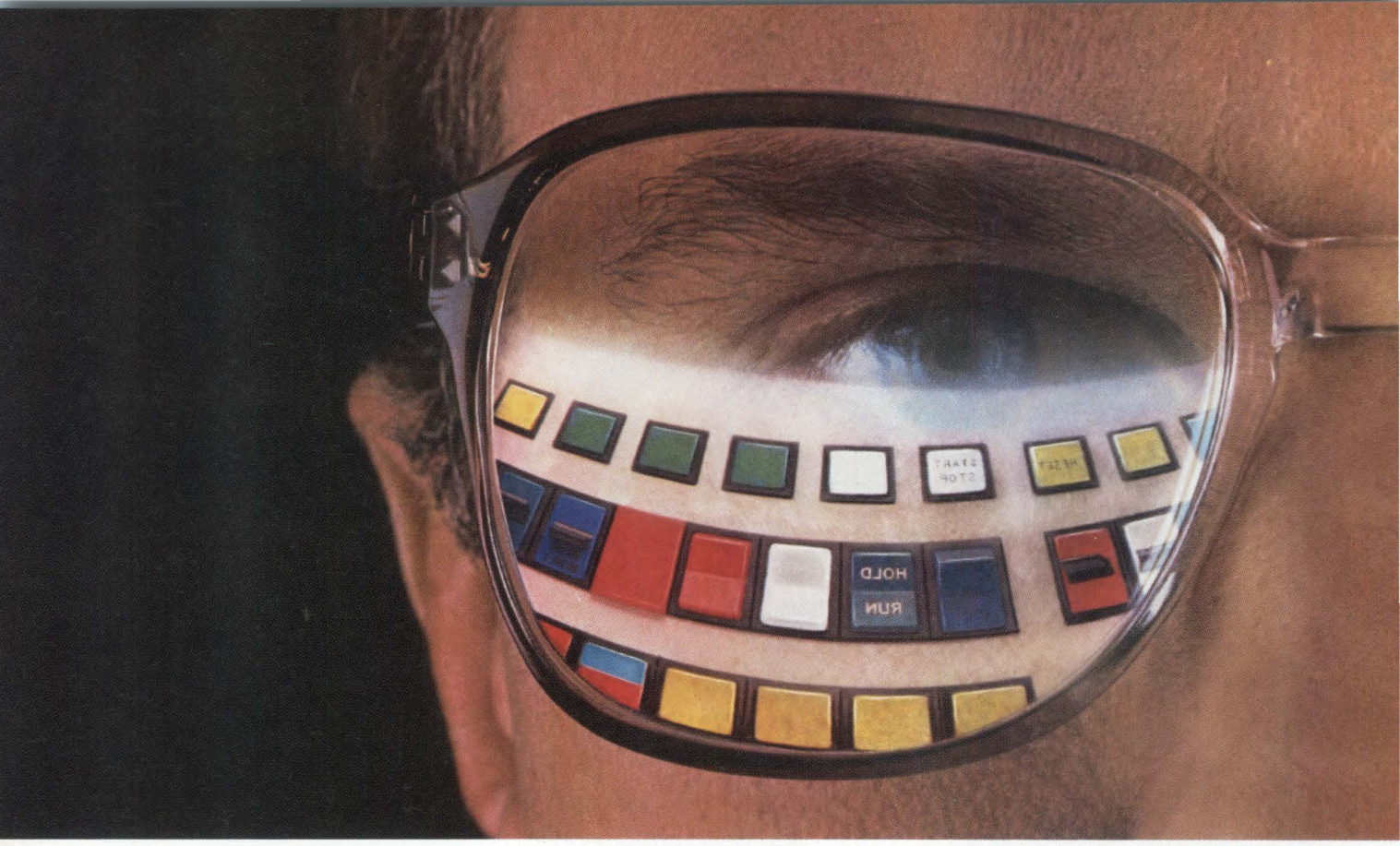



# We design our through your

With the first glance, your customer begins to form an impression of your product. And the manual controls you use play a major role in this important first impression—as well as long-run operator satisfaction.

That's why we take great care to build human factors into the design of our manual products. By designing our manual controls from your customer's point of view, we can help make your product look better, feel better, work better and, finally, sell better.

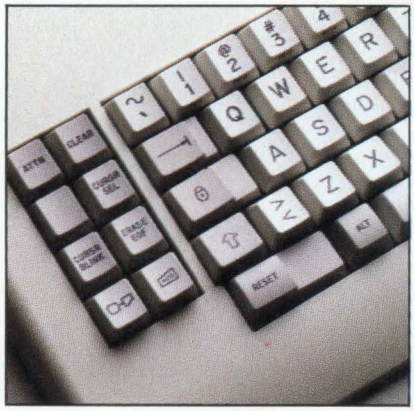
Not only do you get well designed manual controls from MICRO SWITCH, you get lots of them. Our continuing development program has led to a variety of new products to fit specialized requirements. And with the broadest selection of product options in the industry to choose from, you get the flexibility and freedom to design your products to meet your customer's needs.

**New looks for new needs.**

Our Programmable Display Pushbutton is an excellent example of our ability to respond to emerging needs in the marketplace with new products having unique human factors features. It is a user-friendly pushbutton that provides two-way communication between the system and the operator. Our Programmable Display Pushbutton offers the state-of-the-art ability to display an infinite number of legends when programmed through a computer. This multi-function capability means that one switch can replace dozens, reducing panel space and viewing area to simplify the operator's tasks and reduce the possibility of error.

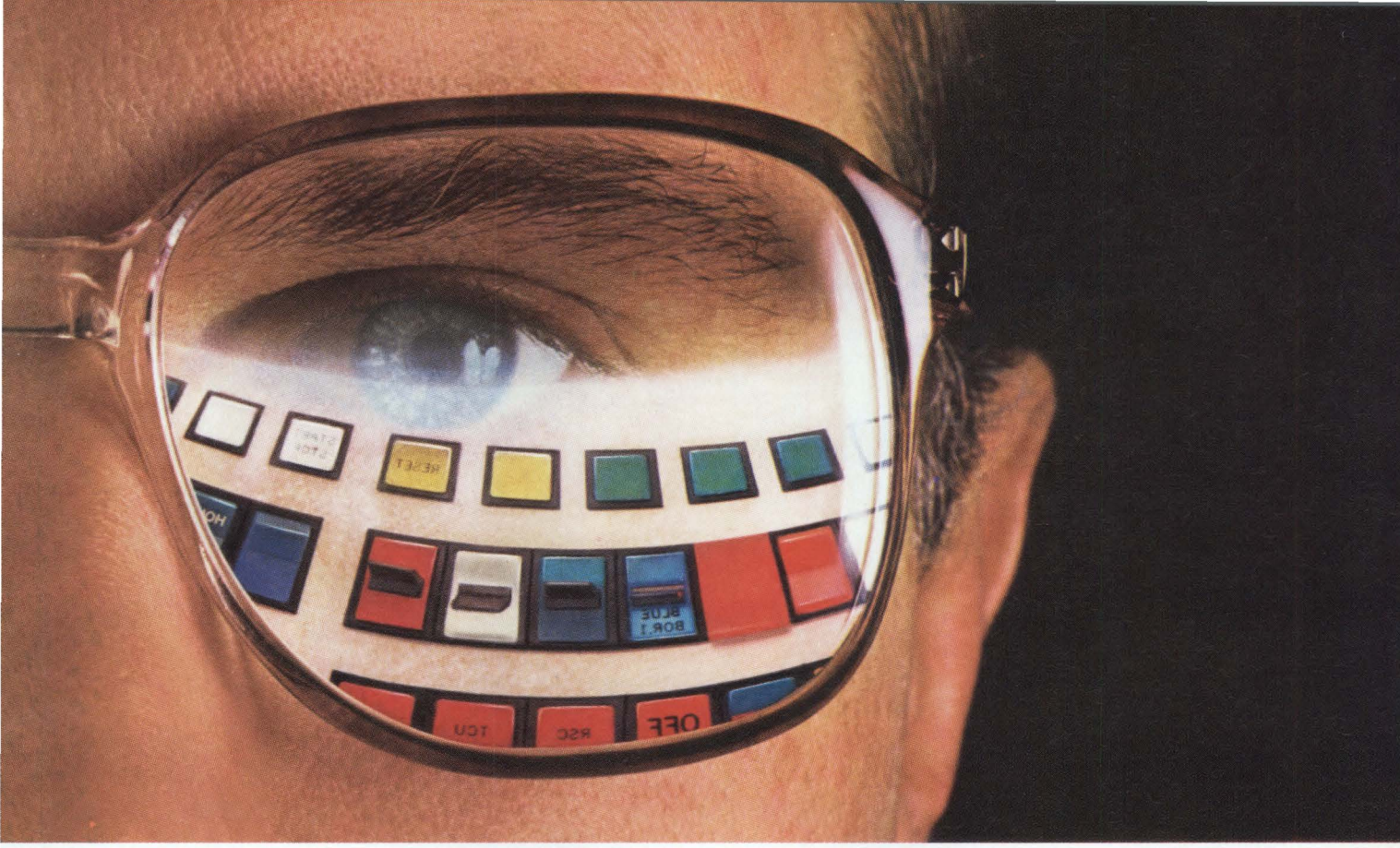
**Even the best can get better.**

We're always working to improve our manual products to meet your changing needs. For example, based on years of experience in building quality keyboards, we were able to combine quiet operation and excellent tactile feedback in our new Silent-Tactile keyboards. These low profile keyboards look good and feel good. They retain their consistent positive feedback month after month, year after year. Their silent operation helps make work environments more pleasant. Because in a room full of CRTs, it's what you don't hear that counts.



**Take your pick from a variety of quality controls.**

Constant efforts over the years have resulted in a broad line of human factors-designed manual products. Our touch panels, for example, combine high quality graphics with reliable switch operation. We take special care with such details as embossing for positive finger positioning, snap discs for tactile feedback and high quality color and graphics.

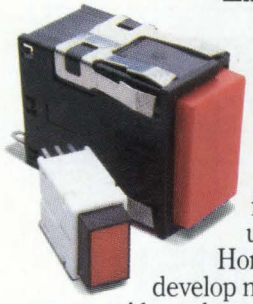


# manual controls customer's eyes.

The Advanced Manual Line and Miniature Manual Line display the same painstaking concern for detail and quality. They're designed to be visually pleasing—with clean lines, vivid colors, bright, even illumination, attractive shapes and sizes. And their appearance is coordinated, both within and among product groups. So you can build harmony into your design.

Having this wide selection of controls to choose from means you can specify the best combination of performance and price—always with superior human factors features.


**Experience you can count on.**



For over 40 years we've been building manual products to help solve all kinds of control problems. For years we've been conducting and publishing the results of original human factors research. No other controls manufacturer does. And we work with Honeywell's industrial design experts to develop new products and materials.

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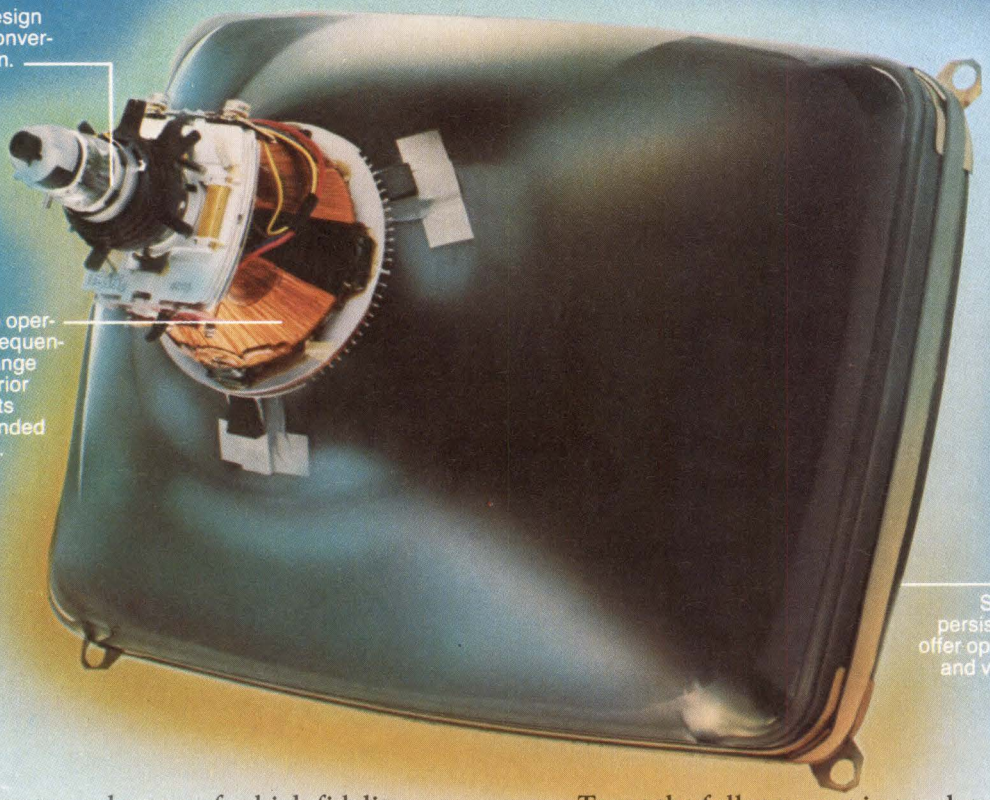
CIRCLE 54

# The other side of our CRT story.




From the front, you know us for high-fidelity color reproduction.

But behind those pretty pictures is an equally important part of our story—superior technology. You see, Mitsubishi Electronics pioneered high-resolution CRTs. We've continued to advance the state-of-the-art with design refinements. And, in the process, we've earned a reputation for innovation and leadership.

When you get technical, you won't find a better, more reliable CRT. Or a broader product range. Our unsurpassed selection covers all sizes and performance criteria for applications including CAD/CAM, computer graphics, imaging, process control, MIS and more. Check the chart for a brief overview. And note that we're very cost competitive, even when compared to less capable CRTs.

Of course, our story wouldn't be complete without mentioning our large network of knowledgeable sales representatives. There's a Mitsubishi Electronics professional near you for fast response to your needs. One call is all it takes for pricing and delivery information, as well as technical and applications assistance.

To get the full story, get in touch today. We'll send complete technical information and the location of your nearest representative. Just contact: Mitsubishi Electronics America, Inc., Industrial Electronics Division, 991 Knox Street, Torrance, CA 90502. Telephone (213) 515-3993.

| CRT RESOLUTION RANGE AND SIZE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Series | | US | UA | ST | SA | AT | MT | AM |
| Availability Dot trio pitch (mm) | 10″ (9V) | | | | | 0.31 | | |
| | 12″ (11V) | | | | | 0.31 | 0.37 | 0.47 |
| | 14″ (13V) | | 0.2 | 0.31 | 0.25 | 0.31 | 0.4 | 0.4 |
| | 16″ (15V) | | | 0.31 | | 0.31 | | |
| | 20″ (19V) | 0.25 | 0.25 | 0.31 | | 0.31 | 0.44 | 0.56 |
| | 26″ (25V) | | | 0.37 | | | | |
| Screen Structure | | Dot | Dot | Dot | Dot | Dot | Dot | Stripe |

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CIRCLE 55

# Special report on microprocessors/microcomputers—Part II

**When you're designing a first-rate computer system, it doesn't make sense to compromise with a second-rate monitor.**

Consider PGS instead. We make three no-compromise monitors, all fully compatible with the IBM-PC, to match your requirements and your budget.

**High resolution** PGS set the price/performance standard for high resolution RGB color monitors with the HX-12: .31mm dot pitch, 690 dots horizontal resolution, and precise color convergence for a crisp, sharp image.

**Super resolution** And, when your specifications call for super resolution, there's our no-compromise SR-12: an RGB monitor with a horizontal scan rate of 27.5 KHz which supports 690x480 resolution in non-interlaced mode.

**Monochrome** For price/performance in a monochrome monitor, we've set the standard with the MAX-12: our amber monitor with dynamic focusing circuitry which ensures sharpness not only in the center but also in the edges and corners.

**The monitor to meet your needs**

All three PGS monitors are engineered for no-compromise performance to offer you a cleaner, sharper image than any other monitor in the same price class. The HX-12 and the SR-12 both feature uncompromising color convergence for crisp whites without color bleed. The MAX-12 offers impressive clarity in an amber phosphor monitor that runs off a standard monochrome card—no special card is required.

At PGS, our no-compromise approach includes all the details, too, from non-glare screen to a shielded cable—standard features on all PGS monitors, color or monochrome.

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Compare your specifications to ours, listed below. Then call us at 800-221-1490 and we'll send you a fully detailed spec sheet plus everything else you need to know about all three no-compromise PGS monitors.

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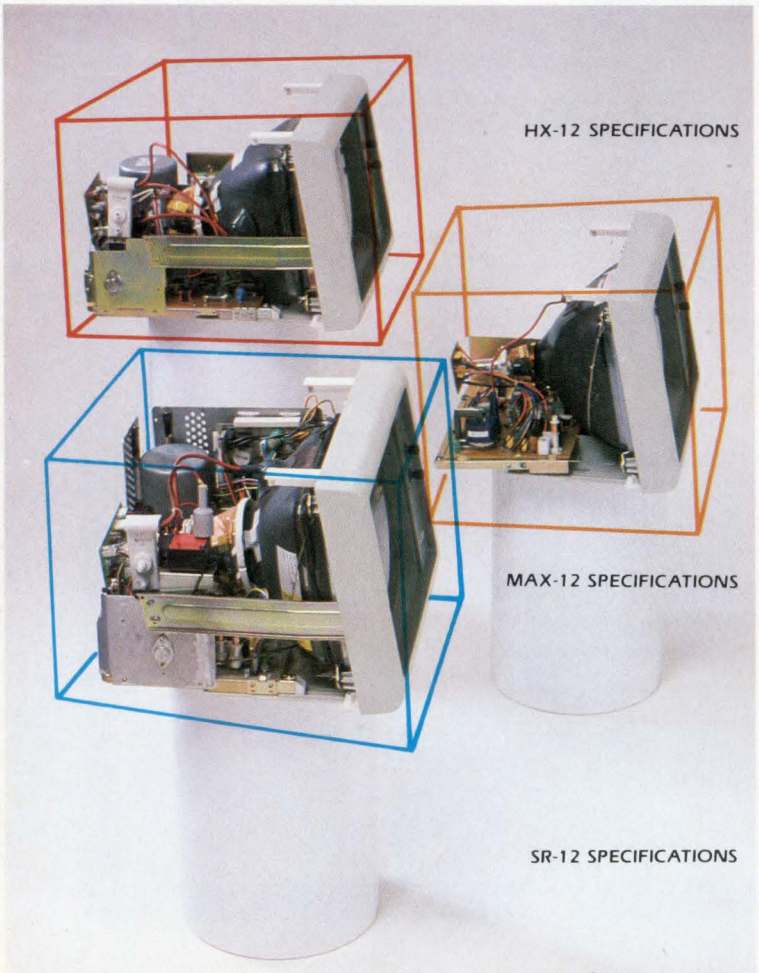
# PGS delivers 3 no-compromise ways to improve your image



HX-12 SPECIFICATIONS

| | |
|---|---|
| CRT | 12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22) |
| Input Signals | R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels |
| Video Bandwidth | 15 MHz |
| Scan Frequencies | Horizontal: 15.75 KHz Vertical: 60 Hz |
| Display Size | 215mm x 160mm |
| Resolution | Horizontal: 690 dots<br>Vertical: 240 lines (non-interlaced)<br>480 lines (interlaced) |
| Misconvergence | Center: .6mm max Corner: 1.1mm max |
| Display Colors | 16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels) |
| Characters | 2000 characters (80 characters x 25 rows—8x8 dots) |
| Input Connector | 9 Pin (DB9)—cable supplied to plug directly to IBM PC |

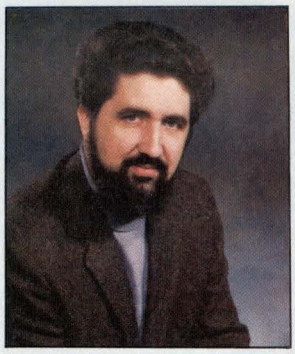
MAX-12 SPECIFICATIONS

| | |
|---|---|
| CRT | 12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor) |
| Input Signals | Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels |
| Video bandwidth | 18 MHz |
| Scan frequencies | Horizontal: 18.432 KHz Vertical: 50 Hz |
| Display size | 204mm x 135mm |
| Resolution | Horizontal: 900 dots Vertical: 350 lines |
| Input Connector | 9 Pin (DB9)—cable supplied to plug directly to IBM PC |

SR-12 SPECIFICATIONS

| | |
|---|---|
| CRT | 12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface |
| Input Signals | R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels |
| Video bandwidth | 25 MHz |
| Scan frequencies | Horizontal: 31.5 KHz Vertical: 60 Hz |
| Display size | 215mm x 160mm |
| Resolution | Horizontal: 690 dots<br>Vertical: 480 lines (non-interlaced) |
| Misconvergence | Center: .5mm max Corner: 1.0mm max |
| Display colors | 16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels) |
| Characters | 2000 characters (80 characters x 25 rows) |
| Input Connector | 9 Pin (DB9)—cable supplied |

CIRCLE 56



## SPECIAL REPORT ON

# MICROPROCESSORS/ MICROCOMPUTERS—Part II

The onslaught of 32-bit microprocessor power on the engineering community is causing a lot of excitement as well as pain. System designers are being asked to design a new generation of computer-based products embedded with a micro technology that is as powerful as its predecessor mainframe technology. Yet, these new 32-bit machines lack the coordinated hardware and software support to ensure their success.

A machine that can manipulate data 32 bits at a time, while also addressing 32-bit words, is the dream of most digital design engineers. But, engineers must consider all aspects of designing with the 32-bit tools before using them in high speed data crunching operations. As the June 1 companion issue points out, 32-bit microprocessors are upon us. And, while only two are currently available, designers are addressing all the necessary elements now to yield efficient designs later.

Such concerns as the choice bus architecture, proper memory management techniques, software adaptability, and maximum I/O throughput are all part of the system designer's game plan. An efficient design will incorporate the right kinds of elements in an optimum configuration for the intended application. The following special report section considers the required elements for optimizing 32-bit micro power.

With National Semiconductor's NS32032 as the only mainstream chip available (excluding the micro-programmable NCR/32), it is no wonder that it is the workhorse for several board and system designs. Thus, the staff-written portion of the report concentrates heavily on a workstation example where the chip's power is being used to the fullest, and where it works well with other 16- and 8-bit microprocessors. This 32-bit unit is making the professional workstation both a design project and a design tool for the system engineer. One of the contributed articles discusses the practicality of this double-duty.

Three articles that follow offer insight into the salient features of the Multibus II, the NuBus, and the VMEbus. Written by engineers who were instrumental in formulating the 32-bit bus specifications, these articles are geared for designers looking to obtain the most from open-system bus architectures.

Rounding out the section is a discussion of a transportable native-code package that suits 8-, 16-, and 32-bit microprocessors of the same family. The article delves into some of the necessary software manipulations that engineers face every time a new processor is introduced into the market.

Nicolas Mokhoff
Senior Editor

# ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 8031 AND 8051 ALTERNATIVES.

**Rockwell's R6500 single-chip family—including the R6501Q "Super Microprocessor" —offers available solutions to long lead times.**

In as little as six weeks, Rockwell International can deliver alternatives to the 8051/31, 8048/49 or 8041 families of single-chip products. Our field applications engineers are ready to answer conversion questions and Rockwell's development aids can provide an MDS II cross-assembler and in-circuit emulation hardware to aid in your redesign process.

| Models | R6501Q | R6500/11 | R6500/12 | R6500/1 | R6500/41 |
|---|---|---|---|---|---|
| ROM (x8) | — | 3072 | 3072 | 2048 | 1536 |
| RAM (x8) | 192 | 192 | 192 | 64 | 64 |
| I/0 Lines | 32 | 32 | 56 | 32 | 23 |
| Serial Comm. | UART | UART | UART | — | — |
| Counters | 2 x 16 | 2 x 16 | 2 x 16 | 1 x 16 | 1 x 16 |
| Expansion Bus | 65K | 16K | 16K | — | 4K |
| Interrupts<br>External<br>Internal<br>Host | 6<br>4<br>— | 6<br>4<br>— | 6<br>4<br>— | 3<br>1<br>— | 4<br>1<br>2 |
| Standby RAM (mW) | 12 | 12 | 12 | 35 | — |
| Package | 64-pin QUIP | 40-pin DIP | 64-pin QUIP | 40-pin DIP | 40-pin DIP |
| Replaces | 8031 | 8051 | | 8048/49 | 8041 |

Our R6501Q microprocessor provides an alternative to the 8031. This "super microprocessor" device extends the R6500 family with four new bit manipulation instructions, and offers 192 bytes of RAM, two 16-bit counters, a serial (UART) port, 32 I/O lines, plus a full 65K address bus.

In addition, the R6500/11 or R6500/12 microcomputers can end your search for an 8051 alternative. The R6500/11 has all the features of the R6501Q, plus 3K of ROM, 32 I/O lines—or 56 I/O lines with the R6500/12—and address expansion to 16K is available.

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And if you're waiting for an 8041 to off-load tasks from your central CPU, look at the R6500/41. It has 1.5K ROM, 64 bytes of RAM, a 16-bit counter, multiplexed address expansion to an additional 4K and a host bus that talks 8050/Z80 or 6500/6800.

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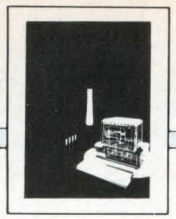
CIRCLE 57





# THIRTY-TWO BIT MICROS POWER WORKSTATIONS

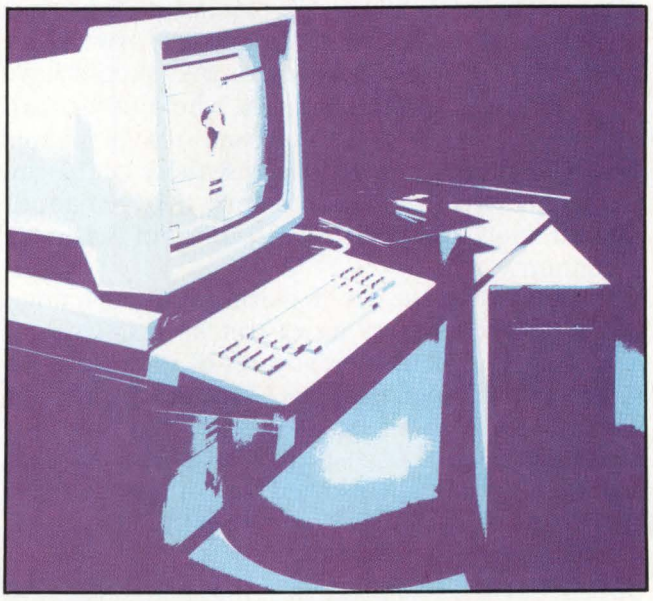
**New "star" processors require strong supporting casts and clever designs to be effective engines in engineering workstations.**

**by Nicolas Mokhoff, Senior Editor**

With system engineers just beginning to reap the benefits of their 16-bit microprocessor-based designs, and 32-bit chips about to be integrated into new designs, a complacent observer might conclude that there will soon be an IBM/370 mainframe-equivalent computer on every professional's desk. Yet, behind this "ethereal" work environment is a more realistic prognosis. The mainframe-per-desk dream will only materialize when all components of this powerful workstation perform as members of one orchestra in a symphony of information processing and communication.

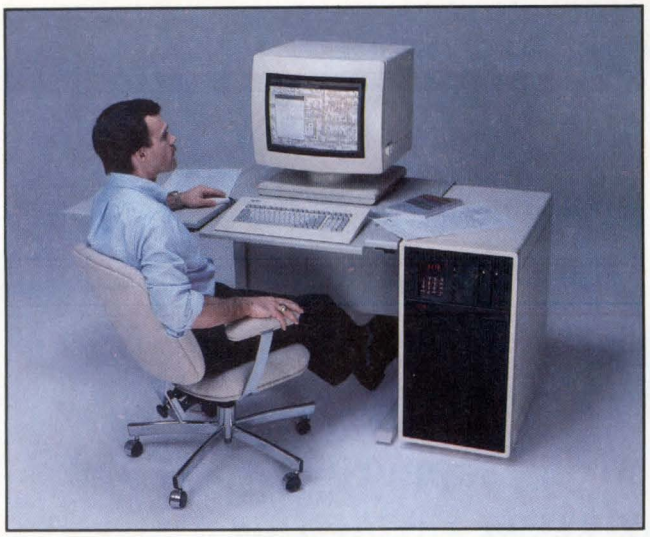
To make successful "data music" together, 16- and 32-bit microprocessors must perform in concert within a system architecture. No matter what outstanding features a sophisticated microprocessor possesses, the chip by itself contributes little to the workstation's overall performance. It must also be incorporated on an efficient bus architecture and surrounded with proper hardware and software support.

Moreover, high performance workstations usually embody more than one "star" microprocessor. In an efficient multitask, multiprocess workstation, various 8-, 16-, and 32-bit separate processors are used for such data-intensive functions as graphics, high speed I/O, diagnostics, and communications. Thus, this multiprocessing capability must be accommodated within the designer's system specification—a tricky task, to say the least.



The current frenetic pace in defining 32-bit microprocessor bus specifications lends credence to the notion that design engineers need more than glorified VLSI chips to make their systems really work. Thus, both chip manufacturers and users have strongly identified their marketing strategies and applications with one of four open-system bus schemes, such as Multibus II, VMEbus, NuBus, and Futurebus, or with some kind of proprietary bus. These proprietary 32-bit bus schemes are closely related to a particular hardware configuration and are therefore limited in appeal to the entire design community.

One such "closed" open-system bus scheme is in the works at Digital Equipment Corp (Maynard,



**Syte Technology's first workstation, the model 300, displays the kind of power now available to the design engineer. It is designed for engineering-oriented applications including software development, computer aided engineering, and project management. The multiple microprocessor hardware lets users make fast floating point calculations on a DEC VAX-11/750 supermini. The system allows multiple operating systems to run concurrently on one mode; simultaneously on multiple computers on the network.**

Mass). The company is developing a 32-bit bus architecture for a whole family of new 32-bit machines. If history is a guide, DEC should have wide success in promulgating a whole new board industry on the par of its Q-bus and Q-22 compatible board business. However, because those boards are intimately tied to DEC computers, they remain of interest only to that particular segment of the design community.

For the rest of the design world, choosing among available open-system buses can be a harrowing experience. Of course, advocates of the respective schemes will defend their bus to the death based on worthy technical merits. However, they will also readily admit that such factors as marketing, and compatibility with an installed base of products that sport their choice bus's 8- and 16-bit predecessors, are critical in the selection process.

The bus standardization issue is, in itself, a moving target. It is best, therefore, to let the actual standards documents supply the sufficient information on the individual buses (see reference section, "Obtaining bus specifications," on p 112). In light of recent developments, it is perhaps more beneficial to concentrate on several arbitrary hardware and software choices from manufacturers of sophisticated workstations. In all cases, the companies choose a processor, system architecture, software environment, and communication capability to produce a single-user networked workstation that suits a particular set of specifications for a well-targeted market. Among the workstations highlighted are those from Syte Information Technology (San Diego, Calif), Sun Microsystems (Mountain View, Calif), Apollo Computer, Inc (Chelmsford, Mass), Tektronix (Wilsonville, Ore), Hewlett-Packard (Palo Alto, Calif), Jupiter Systems, Inc (Berkeley, Calif), and Saber Technology Corp (San Jose, Calif). This analysis offers a general perspective on both the components and the thinking process needed to optimize the new 32-bit micros.

In the case of Syte Information Technology, company principals went out of their way to endorse the National Semiconductor (Santa Clara, Calif) NS32032 when that chip was introduced. The microprocessor became the CPU for the company's first product—the model 300 workstation. Aside from the publicity benefits for both companies, the endorsement also yielded some interesting insights into the technical evaluations done by Syte engineers. According to Syte system architect, Michael Fischer, "For the first time, a single chip [NS32032] incorporates many features that were previously associated with mainframe machines."

### An efficient chip architecture

Two key features of the NS32032 are the symmetry of its instruction set and the ability to efficiently run programs written in high level languages. The instruction set's orthogonality allows all instruction types to operate on all addressing modes and data types. This makes it relatively easy to construct efficient programs in either assembly language or high level languages. And, because special cases need not be used to any great extent, portability is extended and programs are easier to debug and modify. Moreover, the features allowing efficient execution of high level language programs become even more important. This is because virtually all of the software for modern processors (including applications, compilers, and operating systems) is now written in high level languages.

Part of this high level language support is provided by a module-linkage facility. This facility permits independently compiled modules to call each other through a mechanism that does not require a linking loader. The benefits here are easy use and easy distribution of utility and support software. According to Fischer, the NS32032's module-linkage facility protects proprietary code because source code need not be distributed. The modules are encapsulated and independent. They can thus be efficiently shared using the common-linkage mechanism, regardless of the source language in which the module was written.

Another important feature for high level language support is the chip's set of addressing modes. The available modes include stack-frame support, with a hardware-frame pointer register; static-data area support, with a hardware pointer register; and dual-displacement indirect addressing modes with both a pre- and post-index for accessing pointers in a stack frame or in the static area. Other modes featured are external addressing for referencing external

variables located in other areas; external addressing for referencing external variables in other modules; and scaled-index mode, which makes array indexing much simpler, according to Fischer.

The many instructions in the NS32032 instruction set are uniquely oriented toward efficient, high level language support. These instructions include interactive array subscript calculations, array-index bounds checking, a multiway branch, and independent division operations for producing quotient and remainder. (Most machines take the time to produce both quotient and remainder in all cases, even though only one is usually needed.) In addition, there are string operations that generalize to bytes, words, and double words; and bit-field operations that enable accessing of variable-length, bit-addressed fields anywhere in memory without byte boundary and alignment restrictions. There is also a rich set of floating point operations to extend the integer operations in a consistent manner.

Moreover, the chip's memory management architecture is patterned after the memory management system used on a number of successful large scale machines, including the IBM 370 series and DEC VAX. Memory management support instructions are tightly integrated with the CPU instruction set. Various tightly coupled CPU functions on peripheral chips can be implemented in a "custom slave." Instructions exist for this slave, and the NS32032 hardware user can supply the slave circuitry.

### The four principles of tight coupling

The chip's tightly coupled architecture provides a firm basis for Syte's closely coupled system architecture in the 300 workstations, as well as in the company's overall network of model 300 workstations—the series 3000. The Syte architecture serves as the foundation of a product family that the company plans to develop throughout the decade. This architecture's principles define the structure of the hardware, software, and user interface. These principles can be generically applied to the majority of workstation architectures. Moreover, these principles are incorporated in four main objectives: a single-level, network-wide, and demand-paged address space; a single, uniform interface between all system resources; a configuration that supports a wider range of performance levels; and a technology-independent system that is economically feasible.

The first objective, a network-wide address space, allows any user (or object) to gain direct access using a common mechanism (or any other object or resource) on the Syte network. Bruce Hamilton, the company's vice president of engineering, says that a global address space of 64 bits is sufficient to accommodate the substantial increases in memory and bulk storage that any technology advances might provide during this decade. Thus, to accommodate the large address space in the network, demand paging is used within the address space itself. There, it supports virtual memory spaces to create an independent address space for each process running anywhere in the network. Demand paging permits a program, or a combination of programs larger than the physical memory, to be run on any node in the network. Initially, each process's virtual address space will be 24 bits or 16 Mbytes. Larger process address spaces up to 32 bits will be supported when the technology is economical, according to Hamilton. Demand paging is now a key feature in other manufacturer workstations as well.

*The NS32032 chip incorporates many features previously associated with mainframe machines.*

The second objective, a single, uniform interface between all system resources, is provided by an operating system kernel called the global environment manager (GEM). Files, directories, buffers, processes, windows, and devices are all treated as objects by the GEM. Different object types are arranged in a hierarchy and messages are interpreted by the object to which they are sent. The sender of a message need only know which object to send the message to, and what is to be done with it—nothing about how it will be done.

The GEM creates all objects with a unique identifier to permit unambiguous communication between all objects in a network. An object only interprets its own messages and manages its internal data structures. The capabilities of any object can be extended or modified without altering any code associated with other objects.

The ability to configure a system to support a wide range of performance levels is the company's third objective and is achieved by optimizing the performance of a single node (a standalone workstation). Thus, the Syte architecture provides many performance levels: closely coupled, multiprocessor configurations for high performance; loosely coupled configurations for distributed processing; and multiuser configurations for a low cost per station advantage. The configuration quality is enhanced by using standard interfaces for external connections. These include RS-232, Multibus (IEEE 796), iSBX (IEEE P959), Ethernet (IEEE 802.3), Small Computer System Interface (American National Standards Institute-X3T9.2), and QIC-02/QIC-24. Finally, the fourth objective—technology independence—is met by having all system software written in a high level language, using proprietary high bandwidth internal buses, and adhering to industry standard external interfaces.

The Syte network consists of nodes connected by an Ethernet local area network (LAN). The GEM operating system runs in a supervisory mode on each

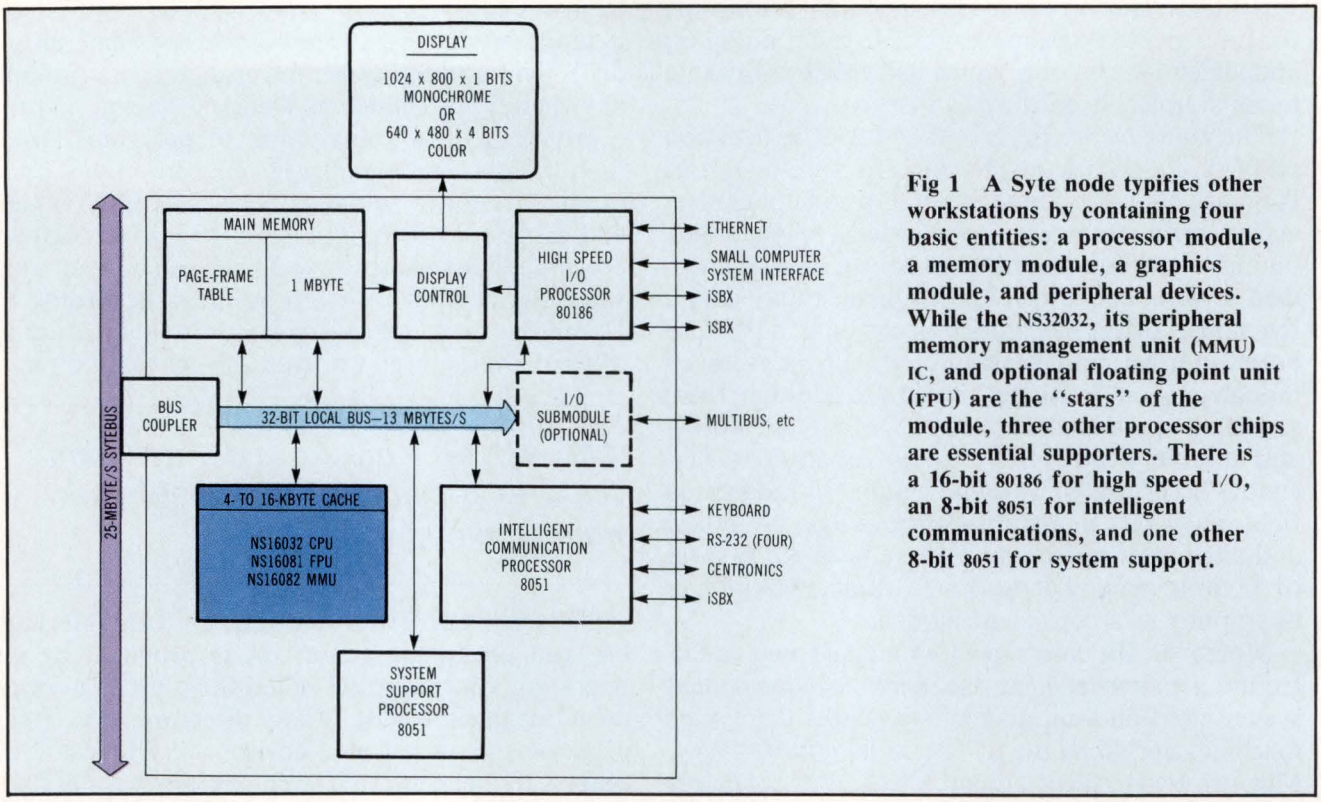



**Fig 1 A Syte node typifies other workstations by containing four basic entities: a processor module, a memory module, a graphics module, and peripheral devices. While the NS32032, its peripheral memory management unit (MMU) IC, and optional floating point unit (FPU) are the "stars" of the module, three other processor chips are essential supporters. There is a 16-bit 80186 for high speed I/O, an 8-bit 8051 for intelligent communications, and one other 8-bit 8051 for system support.**

node to make the total resources of the network available to all users. A processor module in each node is connected to the network through its high speed I/O subsystem via Intel (Santa Clara, Calif) 80186 and 8051 interface chips (Fig 1).

A node is the basic physical entity in the network. It consists of one or more of the following: a processor module, a memory module, a graphics module, and peripheral devices (eg, Winchester disks, quarter-inch streaming tape, a floppy disk, and a line printer). Each module contains cooperating systems that perform the functionally distributed tasks. The modules communicate via a 25-Mbyte/s Sytebus. A node can contain up to four copies of each type of module; up to eight modules in any combination.

### Bit slicing into a graphics processor

Thirty-two bit microprocessors are still not powerful and flexible enough to accommodate high resolution graphics requirements. Thus, the graphics module is designed with a high speed, microprogrammed, bipolar graphics processor (AMD 29116) and 1 Mbyte of display memory. Its high resolution display output can drive one to eight 1000- x 800-pixel monochrome monitors, one 1000- x 8-pixel color monitor, or two 1000- x 800-pixel x 4-plane color monitors. The graphics processor performs display-list interpretation, vector-generation raster operations, and full chip-and-pick support. A Syte node can contain up to four graphics modules.

As with other modules, the company's graphics module has a closely coupled architecture. In conventional systems, interactive graphics display generators usually attach to their host computers as peripherals. This type of loosely coupled configuration requires that all graphics information be transferred between the host and the display generator by programmed I/O or DMA transfers. This not only incurs the I/O handling overhead of the host operating system, but also imposes a bottleneck on the flow of information between the application program and the display generator. As a result, the loose coupling reduces performance by increasing the amount of data transferred, and requires software and/or firmware whose only function is to support the transfer process.

Syte's high performance distributed workstations are bound by a more tightly coupled display subsystem organization. Typically, this tighter coupling eliminates the interface circuitry by placing the display generator directly on the workstation's I/O bus. This saves the cost of the interface, but does not address either excess data transfers or the additional software required to support the transfer.

The architecture of the system's graphics facilities reduces the data transferred and the support software required. The product line has two implementations that solve these problems. One is oriented for high performance at intermediate cost; the second for intermediate performance at low cost. Both of these graphics options are closely coupled to the rest of the system, and are supported in a transparent manner to the application software. This is done by using the same objects, messages, and external data structures.

The first implementation uses an optional onboard display subsystem on the processor module. This subsystem generates a high resolution monochrome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(1000 x 800) or medium resolution (640 x 480 x 4) color display directly from the onboard main memory. A separate memory port is used to fetch display data from memory without involving the local bus, which connects to other subsystems. The sole interface is shared by main memory, which all of the processing subsystems already use. Cost is minimized because not even interboard busing is required for the display generator.

The second implementation is the graphics module, which attaches to the 25-Mbyte/s Sytebus. The close coupling between the graphics module and the processing subsystems on other modules is achieved by using the common physical address space of the Sytebus. The coupling operates in both directions. Image memory on the graphics module is directly addressable as system memory. Moreover, the graphics processor can directly address any offboard memory to access display data structures, font descriptions, etc. The display list can be managed by the same memory management routines as the rest of the system, and without the need to maintain two parallel data structures.

Because Syte is a relatively new startup company, its engineers could design the tightly coupled display subsystem from the start to fit within the overall system architecture. But, working for an established organization such as Tektronix, which has the constraints of an established product architecture, calls for different tactics. Such is the case for Tektronix engineers in Wilsonville, Ore concerning their design of the 4115B graphics terminal.

### Popping the bottleneck cork

The design goal of the 4115B is to increase the performance level of the 4113 graphics terminal from the normally adequate 2-s response time to "instantaneous" response. This requirement is due to user exposure to powerful single-unit systems, which allow functions to be performed locally and thus require realtime response.

The 4113's bottleneck appeared because the central processor (the 8086) was severely overloaded and the vector-generator hardware was idle most of the time. To remedy this, Tektronix engineers opt for the bit-slice route instead of using a fast 32-bit micro. The vector-generator hardware is replaced with a microprogrammable bit-slice "picture processor." This allows the lower level graphics-processing functions to be off-loaded from the 8086. Along with the bit-slice processor, the picture processor contains several hardware accelerators for speed-critical tasks. The entire "update" is constructed to fit onto two standard-sized cards.

The 4115B picture processor is an instruction-set processor that executes programs (display lists) built by code running on the 8086. The initial specification of the display-list format was done by software engineers who wrote the original 8086 code, and by the micro coders who would implement the instruction set. While the specification evolved along with the implementation, task partitioning between the 8086 and the picture processor did not change drastically after the first specification.

As in the 4113 and the 4115B, the 8086 comprises the multitasking operating system, host communication, peripheral management, and display-list management functions. The code in the 4115B, however, differs significantly from that of the 4113 in several key areas. For example, many data paths are 32 bits wide in order to support the 32-bit coordinate space. Also, new algorithms and data structures allow faster, more space-efficient creation of many small graphics segments. New code is also used to drive the hardware dialogue overlay and cursor overlay (not present in the 4113). Moreover, an additional 8087 numeric coprocessor is used for the wide arithmetic operations needed to generate graphics-image transforms for the picture processor.

*One 32-bit workstation uses an "ideal" combination to produce one of the industry's fastest and highest resolution displays.*

The picture processor executes commands from a display list that is resident in system memory. It transforms graphics primitives, described in a 32-bit integer coordinate space, into 1280- x 1024-pixel screen-coordinate space, and clips the results to rectangular view ports on the screen. It scan-converts the transformed primitives and writes pixels into the frame buffer. Using information from the display list, the picture processor also controls the appearance parameters (eg, primitive attributes such as line style, filled or hollow areas, and background transparency of dot-matrix characters).

Since the picture processor is an independently executing processor, it must gain access to the system bus and perform data transfers to and from system memory and I/O devices. In the 4115B, the details of these low level operations are hidden from the microcode. Two hardware state machines (both resident in a single registered programmable array logic IC) implement the bus-acquisition and data-transfer protocols.

A single microinstruction activates the machines. The microcode can then continue executing until it needs the results of a bus read, or until it tries to start another bus operation. At that time, a hardware "wait" mechanism temporarily halts the picture processor until the original cycle is completed. Thus, microcode does not have to test any status flags to see if a transfer is completed before starting another transfer.

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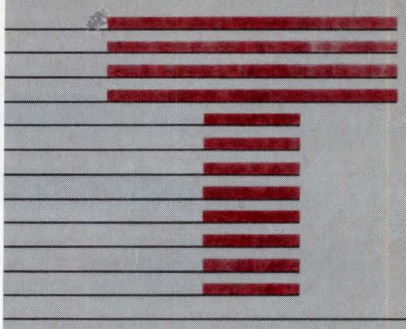

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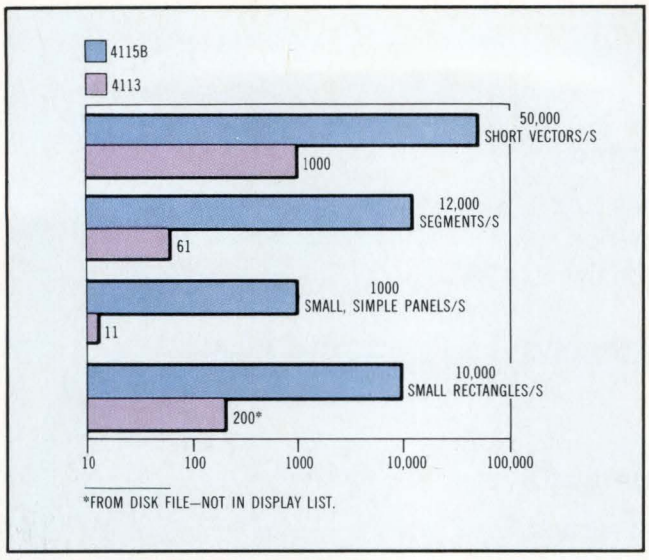



**Fig 2 When Tektronix engineers enhanced the 4113 graphics terminal with a picture processor and added special microcode to the 8086 processor, the result was the 4115B terminal featuring a 32-bit coordinate space. When comparing the system performance of the two terminals in terms of the amount of elements that can be drawn per second, the 4115B excels considerably.**

To assist in the transformation of points from 32-bit terminal-coordinate space, the picture processor also features low cost, serial/parallel multiplier hardware. Like the bus-transfer circuitry, this hardware is activated by, and can operate in parallel with, microcode. Moreover, to achieve the desired processing speed, up to 48- x 48-bit multiplications are performed using multiple passes and partial-product accumulation in microcode.

Testing a design's value requires a quantitative metric against which system performance is measured. For the design of the 4115B, senior engineer Douglas Doornink and his design team at the Tektronix Information Display Division establish performance metrics according to the product's target areas. The metrics measure the per-second drawing speed of vectors, segments, and simple panels. All vectors and panels have two-dimensional transforms applied to them as they are drawn.

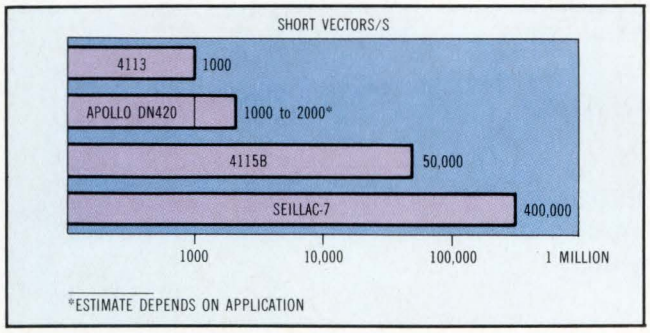



**Fig 3 The performance of the 4115B can be compared to the performance of other architectures by using just the speed at which short vectors are drawn as the metric. For the relatively limited amount of upgrading done on the 4113 terminal, the 4115B fares well above the Apollo DN420. However, it does not approach the speed of a Seillac-7, where the operations are performed through a pipeline architecture.**

From analyzing sample pictures from typical applications, the team determines that the average vector length is about 10 pixels on a 1280 x 1024 display. Pictures in this category have an average number of vectors equal to 30,000. Pictures with longer pixels have typically fewer vectors. In the worst case, an application may have only one vector per segment; in the best case, all vectors would be in one segment. According to Doornink, because the picture processor incurs significant overhead for each segment, both cases require benchmarking.

Another important picture type is that using simple panels. A simple panel is defined as a panel having fewer than 16 edges. One implementation of a simple panel is in a solids model, where a mesh description is used and the image is generated with many quadrilaterals. For these image types, the quadrilaterals have an area of about 100 pixels. There are other applications such as VLSI computer aided design, in which the panels to be filled are even simpler and can be rendered by rectangles. Because of this, another benchmark for the rectangle fill performance is needed, again using rectangles within an area of 100 pixels.

The performance gains from adding a microcoded picture processor are dramatic, as shown in Fig 2. Some performance comparisons to four other architecture types are also included. Overall, the 4115B fares well compared to the more conservative approaches (Fig 3).

## "Ideal" combination makes a fast display

For its part, Saber Technology Corp develops its 32-bit workstation using an "ideal" combination of the NS32032, the Unix operating system, and a proprietary circuit technology called QSEL. The result is one of the industry's fastest and highest resolution displays—a 19-in. video monitor with a 60-Hz noninterlaced refresh rate that can address bit-mapped graphics with a full gray-scale resolution of 1664 x 1248 pixels.

To complement its high resolution monitor, a graphics subsystem is designed to support the 2-million pixel image for ultrahigh resolution. And, to meet the needs of three-dimensional design and solids modeling, the graphics subsystem architecture is based on a proprietary high bandwidth bus structure (Fig 4).

The system provides true bit-mapped graphics and allows control of any pixel placement and movement. The graphics subsystem can take data (eg, a design) directly from mass storage by bypassing the CPU, and bring it to the video display very quickly under DMA control. The image memory unit is comprised of image planes designed to the 2-million pixel density of the display. The basic subsystem can contain up to eight image planes.

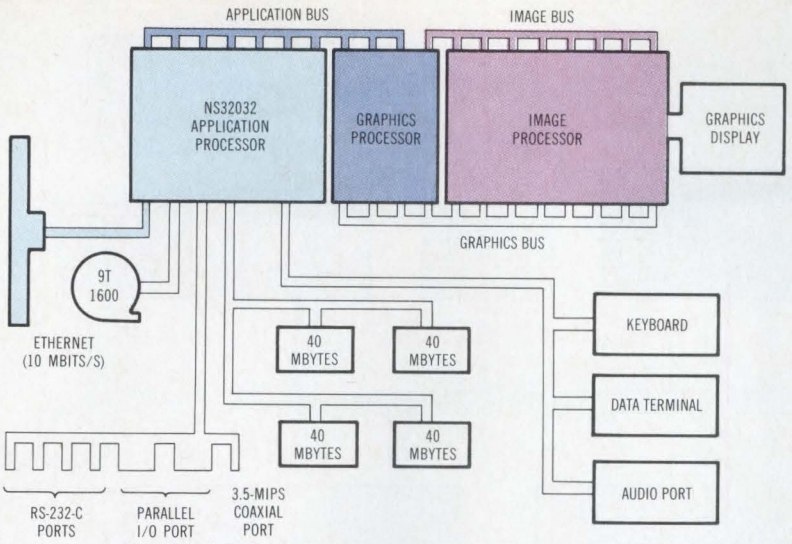



**Fig 4 An example of 32-bit microprocessor power combined with innovative circuitry for display on a high resolution screen (1664 x 1248 pixels with a full gray scale) is Saber Technology's Interactive Graphics Computer System (IGCS). An NS32032 running at a 10 MHz controls the graphics subsystem, which uses a proprietary 20-Mbyte/s bus and QSEL circuit technology as a fast graphics buffer. The Berkeley Unix operating system, Ethernet, and IBM coaxial connections ensure that the workstation is a standalone unit and an integral part of a computer aided engineering network.**

Expansion is available for a total of 24 image planes. The image subsystem supports a unique ultrahigh speed display interface providing 180-MHz video with 24-bit color resolution. Each primary color has an effective 8-bit conversion at the very high video data rate. The rate results in a pixel time of less than 6 ns.

The NS32032 used in Saber's workstation runs at 10 MHz and processes at approximately 1.2 million instructions per second (MIPS). The system also has a high performance floating point coprocessor. Saber has designed its own memory access (DMA) system. The DMA has a 20-Mbyte/s transfer rate and 8 variable-burst length, dynamically relocatable channels. All DMA devices are first in, first out (FIFO) buffered.

Saber's system, dubbed the Interactive Graphics Computer System (IGCS), has two independent disk controllers, each on a separate DMA channel with its own disk subsystem. One is allocated to the Unix operating system, the other is used for applications. Each disk subsystem can support four drives.

Meanwhile, Apollo Computer adds a 32-bit workstation as another node for its proprietary Domain network. The company dubs the Domain as a distributed processing system designed for both general-purpose and interactive graphics applications.

In essence, the network is a collection of powerful personal workstations and "server" computers interconnected by a high speed LAN. Both workstations and server computers can run very large and complex applications. The personal workstation is provided with a high resolution, bit-mapped display. Therefore, each user can display the output of programs written in Fortran, C, or Pascal. A Domain server processor can act as a file or peripheral server, as well as a gateway to other networks. All workstations and server processors share a common

**The Apollo DN320 workstation distinguishes itself by incorporating a standard hardware floating point processor. The processor is implemented in bit-slice technology. This allows structuring of both 32- and 64-bit floating point data formats that adhere to the IEEE standard. As another node in the Domain network, the DN320 offers each user 1.5 Mbytes of main memory, 16 Mbytes of virtual address space and a 1024- x 800-pixel display. A 68010 is used as the central processor.**

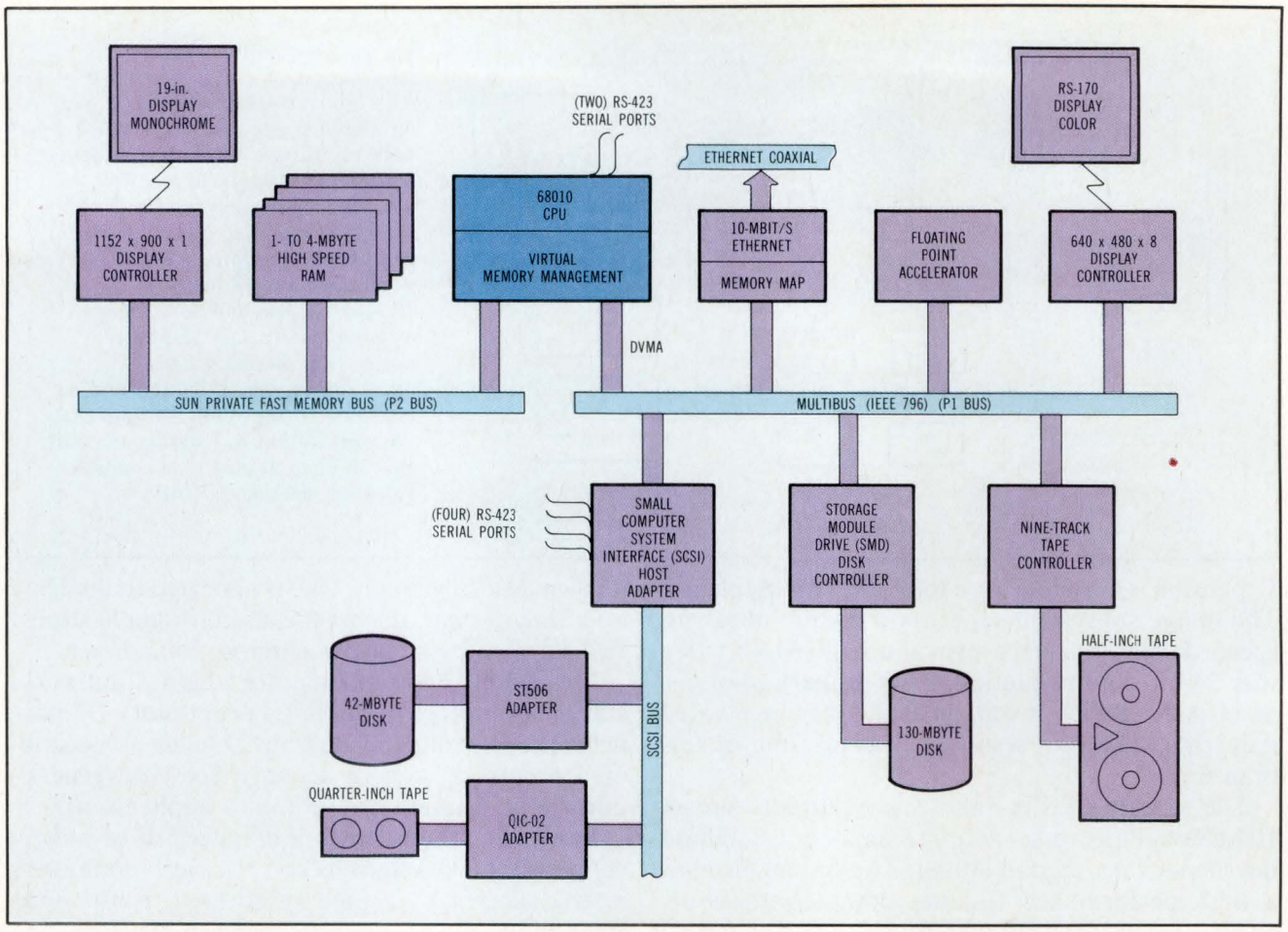



**Fig 5 Adherence to an open-system architecture and to industry bus standards is a design requirement for the Sun-2. Using the IEEE 796 Multibus specifications for the card cage and backplane, the unit divides its tasks between the two respective connectors. P1 is used for I/O access to a wide variety of peripherals, while P2 provides access for high speed data transfers to both main memory and display memory.**

network-wide virtual memory system that allows groups of users to share programs, files, and peripherals.

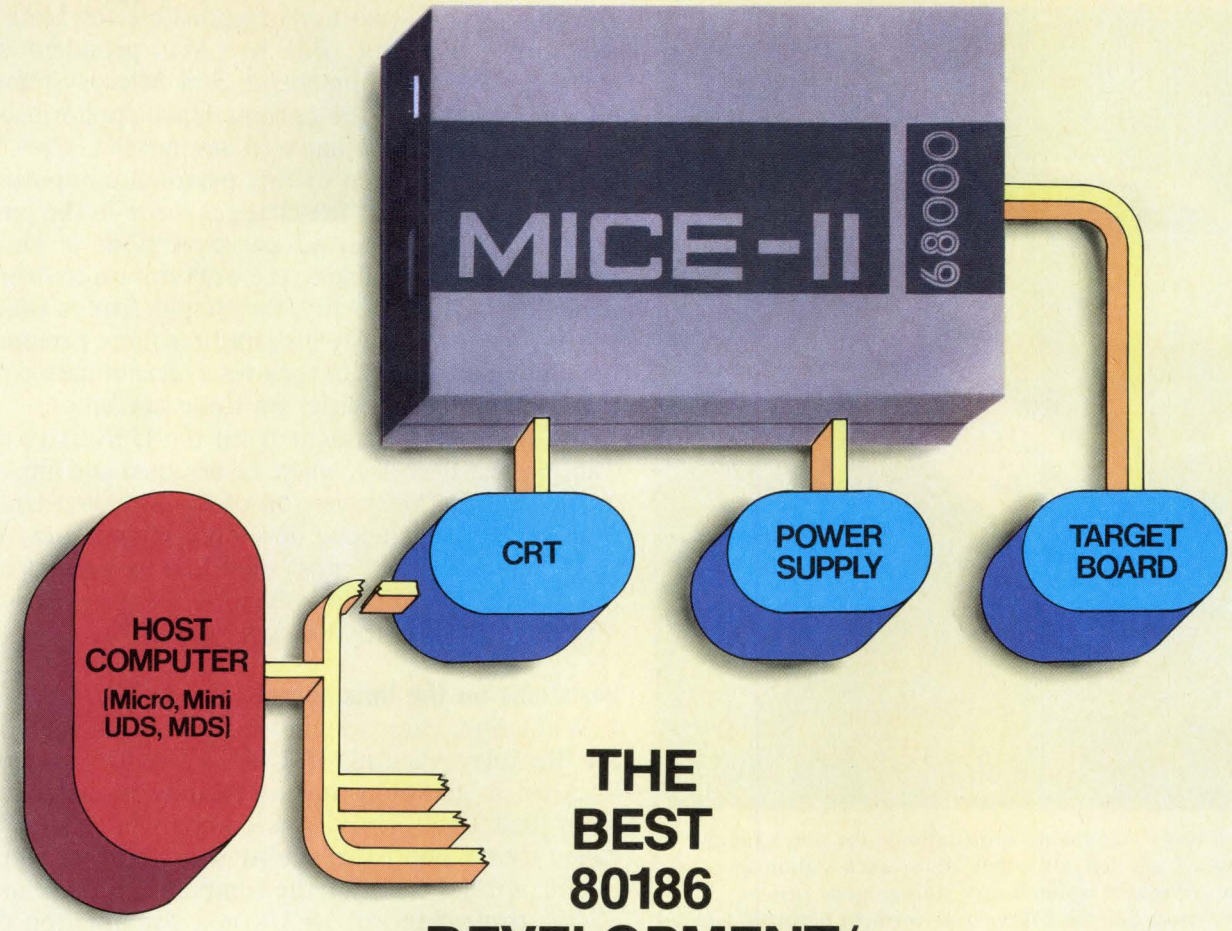
Like the networks from Syte and Sun Microsystems, the Domain station consists of three main parts: a powerful processor with a large virtual address space, a high speed cache, and a high resolution, bit-mapped graphics display subsystem. Moreover, the workstation supports a full 256-Mbyte virtual address space. Thus, applications that exist on mainframes or superminicomputers can be converted to the Domain system with minimal effort, according to Dave Nelson, Apollo's vice president of research and development. The structure of virtual memory is based on objects that are 32-bit, byte-addressable virtual address spaces and accessible from anywhere in the network.

## It's all part of the domain

To explain the advantages of object-based systems, Nelson comments, "In conventional timesharing systems, separate mechanisms are frequently used to implement similar system functions." For example, Nelson points out that programs may be managed by a paging system, whereas data files are accessed and handled through a file system. Thus, two distinct system mechanisms exist to handle similar system entities. In contrast, he notes, a Domain-type system deals exclusively with objects without regard to their physical location on the network or their specific functions. According to Nelson, the object abstraction simplifies the overall system design by casing all system entities into a common framework and by managing them with a common set of mechanisms.

The DN320, for example, can execute up to 24 concurrent processes with 16 Mbytes of virtual address space per process on the terminal's multiwindow display. Standard within the DN320 is a floating point unit implemented in microcoded bit-slice technology.

Sun Microsystems' workstations sport similar features. Based on the 68010 and, when available, on the 68020 32-bit architecture, the Sun-2 can also use up to 16 Mbytes of virtual address space per process. As a fairly new startup company, its engineers go to excruciating extremes to make sure their design adheres to popular standards (Fig 5). This will allow future Suns within the same family to communicate, and thus stay transparent to technology innovations.

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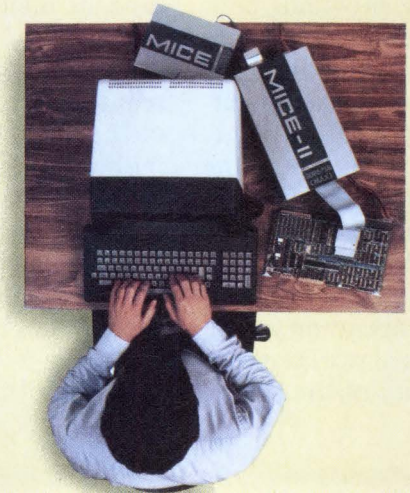


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**As with other standalone workstations, the Sun-2 family runs on a Unix derivative that allows each station to operate without a separate disk storage unit. Instead, diskless nodes use the Ethernet network to perform demand paging as well as routine file I/O. The 68010-based workstation is designed for easy upgrading to true 32-bit computing power when the 32-bit (both address and data) 68020 chips become available.**

Currently, Sun-2 workstations operate the 68010 processor with a 10-MHz clock. At this high clock rate, most microprocessor systems are limited by the speed of their main memory because the CPU must incur one or more wait states on every access to memory. These states are essentially wasted clock cycles. While some designs attempt to relieve this problem by introducing expensive high speed cache memory access, Sun engineers use a custom memory management unit (MMU) that allows the processor to access all of main memory without wait states. In effect, this turns all of main memory into cache.

The MMU implements two-level address translation for virtual memory operations, providing both segment and page addressing. The MMU hardware supports multiprocessing by having separate read, write, and execute commands for both the operating system and the user on every memory page. Optimizations for the company's Unix operating system include referenced and modified bits for each page of memory to facilitate efficient demand-paging algorithms, and hardware support for eight separate contexts to facilitate rapid process switching.

Unix is emerging as the standard operating system for this new generation of professional workstations. This is largely due to the popularity of the PDP-11 and the VAX-11—two units responsible for Unix's widespread use. But, Bill Joy, vice president of research and development at Sun Microsystems, adds a warning to the current Unix euphoria by saying, "It would be naive to assume that Unix is unqualifiedly suitable to this personal computing environment, or that the changes made in the past few years to the most advanced versions of Unix were directly applicable to the workstation environment." According to Joy, the change from a time-sharing environment to a shared-resource personal computing environment requires a reexamination of the Unix system facilities on these machines.

Joy joined Sun straight from the University of California at Berkeley, where he designed and implemented the Berkeley version of Unix, called Unix 4.1 BSD. He later helped develop Unix 4.2 BSD. As such, he may be the most qualified to expand on the virtues and limitations of Unix (see Panel, "Massaging Unix for the workstation").

### Variations on the Unix theme

While Sun Microsystems has placed its stake in the Berkeley version of Unix 4.2 BSD, Hewlett-Packard is gambling on an enhanced version of AT&T Bell Lab's Unix. The company's version is called HP-UX and is for the HP 9000 series 500 computers, a series based on the company's proprietary 32-bit, three-chip set. HP-UX is a combination of AT&T Bell Lab's Unix, portions of the University of California at Berkeley's Unix implementation, and Hewlett-Packard software enhancements. Because Unix is easy to implement on a variety of processors and computer architectures, Hewlett-Packard engineers see it as the ideal choice. Moreover, it is compatible to the distinct architecture of current HP 9000 products: the 68000-based series 200 and the company's 32-bit based series 500 computers. HP-UX is also planned for future products.

Obviously, HP-UX facilitates easy importation of Unix-derived programs onto Hewlett-Packard equipment, and offers users a consistent, powerful program development environment. Complementary extensions address the company's own manufacturer's productivity network (MPN). It reflects the company's view of how computer systems can be used in manufacturing organizations to improve productivity.

Rather than implementing every function of system III Unix, Hewlett-Packard software engineers include features that are important for either porting standard software or for their absolute program development value. With these guidelines, a compatibility hierarchy is used in which kernel services have the highest priority. Library subroutines have the second choice, and commands have the third choice. As a result of this approach, HP-UX includes all System III kernel intrinsics and all libraries except for a handful of graphics subroutines. More than

## "Massaging" Unix for the workstation

Unix is available today on all major 16-bit and soon-to-be-available 32-bit microprocessors, all vying for use in high performance workstations. It is the dominant system on the Motorola 68000 family. And, with the forthcoming high performance 32-bit chips, Unix will be available on a mature architecture where an individual workstation will pack more performance than the large time-shared DEC VAX-11/780. This turn of events will put new demands on Unix, because it needs to change to meet single-user system needs, rather than spend its efforts trying to apportion an overloaded time-sharing system.

Bill Joy, vice president of research and development at Sun Microsytems, places his bets on a new version of the Berkeley 4.2 BSD as the predominant version for the 32-bit based workstations. "The standard versions of Unix in use today, Version 7, Xenix [from Microsoft], and System III from Western Electric are all similar in facilities," says Joy, "but all of these systems lack true interprocess communication primitives." He notes that while the pipe facility allows related processes to communicate in a one-directional, byte-stream fashion, the standard Unix versions lack facilities for unrelated processes to communicate, and for communication over a local network.

**Debugging support**

Joy contends that standard Unix also has very poor support for debugging. The only available debugger program does not support source-level debugging, but requires the inspection of assembly language and low level program details in operation. In addition, the standard Unix has little support for the smart terminals, which have become widely available and quite inexpensive. One must recall that Unix was written when the predominant terminals were hardcopy or refresh terminals. Programs only adequately supported terminals with cursor addressing and other features.

As the principal developer of 4.2 BSD, Joy says that this version addresses the various usage problems on smart workstations, expecially when these are tied in a network. Joy explains, "The 4.2 BSD system includes a number of enhancements to the earlier standard systems. First and foremost of these enhancements is full support for local networking and interprocess communications." According to Joy, this support provides full access to local network protocols, and allows unrelated processes to conveniently communicate. The system includes abstract models of both datagram and socket-oriented communication, and allows processes to perform I/O operations without blocking. The processes can thus multiplex input from and output to different streams.

In addition, the standard 4.2 BSD system includes a full implementation of the Defense Advanced Research Project Agency's (DARPA) transmission communication protocol and Internet interface protocols. Other protocol implementations are underway for the system. These include support for standard protocols, such as X.25. The 4.2 BSD system has a source language debugger (dbx) that replaces the previous assembly language expressions, the setting of breakpoints and conditional breakpoints, and other features commonly found in other commercial systems.

The 4.2 BSD system includes a terminal data base, first developed for the Berkeley version of Unix Version 7. This data base allows programs to be written independent of the terminal type being used. Joy says that this approach is quite successful, and descriptions of several hundred different terminal types are available. This allows Unix to support the wide range of CRT terminals found in the market today. The 4.2 BSD also includes support for virtual memory management, an essential requirement for supporting the large applications typical of the VAX/Unix environment. This virtual memory support also lets Unix support substantial Lisp applications. It can also off-load applications from the popular PDP-10 engine, for which the PDP-10 address space has proved to be insufficiently large.

**Improvements still necessary**

With all these enhancements, however, 4.2 BSD leaves room for improvement for use on workstations, according to Joy. Among the improvements Joy would like to see for the single-user environment are better access to files as server machines; a better memory management facility to accommodate the required number of individual jobs on each station; improved paging algorithms that will not degrade performance; and optimized process scheduling.

Porting to a new processor is one way to improve upon 4.2 BSD. That, however, is not an easy task. Porting requires modification of the Unix source code so that it works on another type of computer system.

According to Jeffrey Schriebman, president of Unisoft Systems (Berkeley, Calif), the most rigorous aspect of the task is porting the kernel. This is because the kernel interacts with the computer hardware more than any other part of the operating system. Anywhere from 20 to 30 percent of the 15,000 lines of kernel source code need to be changed to make Unix operational on a new CPU.

Approximately 10 to 20 percent of the kernel involves interaction with the memory management unit (MMU). This includes process creation, resource allocation, and process swapping. When a new MMU is used for an existing CPU type, this code must be redone.

Another 10 percent of the kernel code involves the device drivers. This code generally needs to be changed even for a minimal-effort port. The remaining portion (approximately 70 to 80 percent) of the Unix kernel code should pass through the porting process unchanged. This makes most of the source code the same for a VAX, a Bell 3B20, or a Motorola 68000.

While porting the Unix kernel is the most demanding part of the porting task and requires the most experience, it is only part of the job, according to Schriebman. Porting the 300,000 lines of utility software as well as the innumerable application packages presents several subtle difficulties. Also, if the target machine uses a new CPU, the source code must be checked for machine dependence.

While the popularity of Unix is increasing dramatically, so is the proliferation of different Unix versions and implementations. "Porter" engineers are thus faced with as many benefits as limitations when writing compatible software between machines.

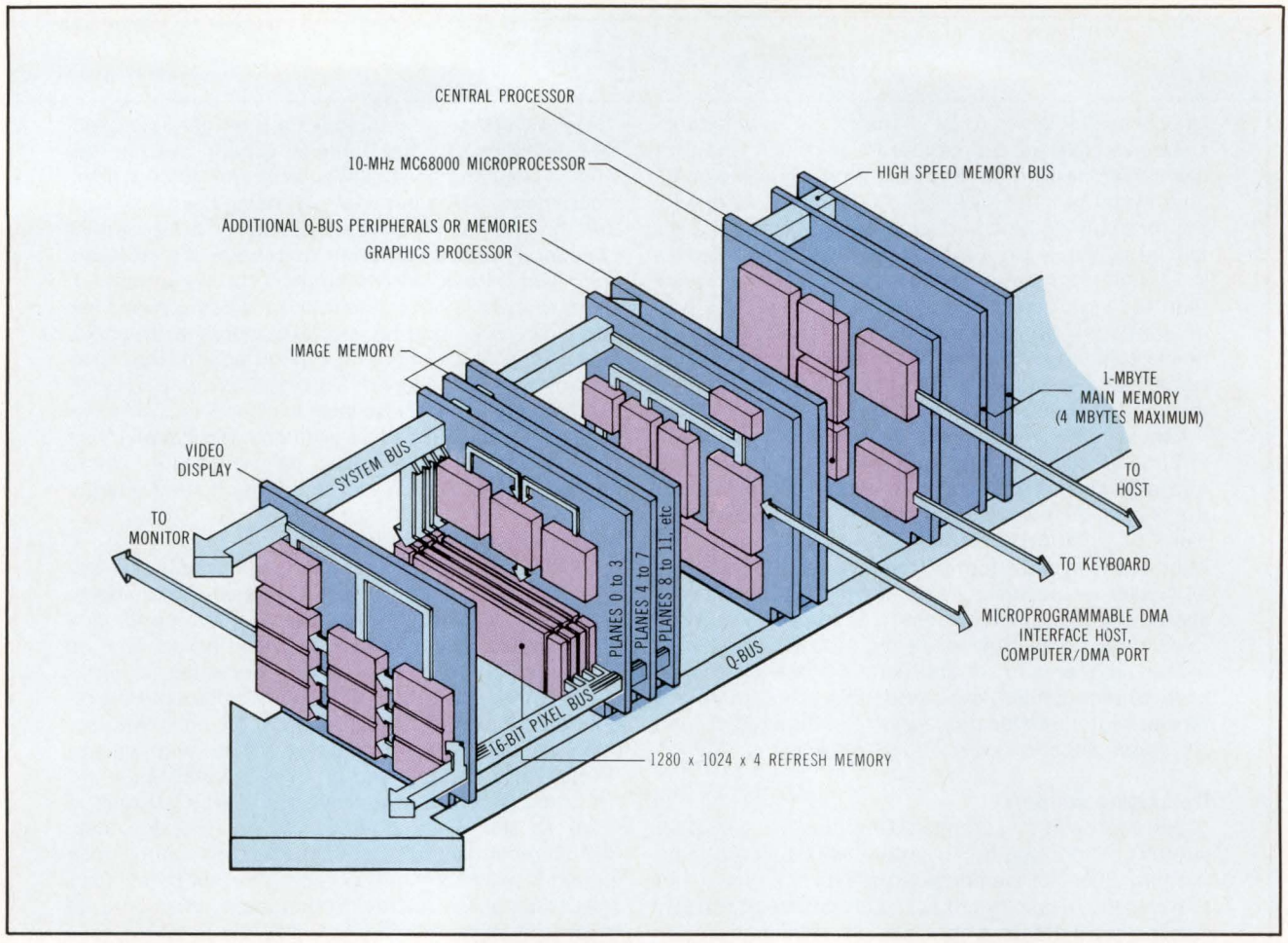


**Fig 6 An example of a high resolution workstation designed on the Q-bus is the Jupiter 12. Sporting a 32-bit 68010 processor, the unit also runs the Unix operating system and connects to an Ethernet. Among the standard graphics capabilities incorporated in the single workstation through the power of a 32-bit microprocessor are anti-aliasing vectors, solids, and text. Display-list management with three-dimensional transformations into multiple windows is also available.**

125 of the most useful System III commands and a small, but important number of Berkeley 4.2 BSD commands are also offered.

To satisfy customer base enhancements, programming languages, graphics, database management, device and instrumentation I/O, local area networking, and friendly user interfacing are being standardized. These extensions, which appear as additional kernel intrinsics, libraries, and commands, will bridge the gap between the company's HP-UX and non-HP-UX computers.

## A matter of compatibility

According to Michael Hetrick, project manager at Hewlett-Packard's Loveland, Colo facility, perhaps the most critical issue in establishing the future course for HP-UX is its degree of compatibility with AT&T Bell Lab's Unix and the Berkeley version. Says Hetrick, "While 4.2 BSD Unix is currently the superior version, Bell is developing improved versions that could eventually surpass 4.2 BSD in capability and reliability." Also, four microprocessor manufacturers are in the process of validating System V, AT&T Bell Lab's latest Unix version, on its microprocessor products. The four companies are Motorola (Phoenix, Ariz), Zilog (Campbell, Calif), National Semiconductor, and Intel (see *Computer Design*, Aug 1983, p 113). System V could become the most affordable Unix and the Unix of choice for portable application programs.

In light of these factors, Hewlett-Packard engineers choose the Bell System III version as the base standard. The compatibility hierarchy will determine which portions of System V and its successors are HP-UX candidates.

Hetrick projects extensions beyond the Bell versions if these fail to meet company requirements in a timely fashion. However, he says he prefers to adopt an existing Unix-based implementation before embarking on an original design project. The potentially rich source of enhancements will most certainly come from the University of California at Berkeley 4.2 BSD version, whose features such as the C shell, mailer, and selected kernel intrinsics are expected additions.

Hetrick also says that Microsoft's (Bellevue, Wash) Xenix, with its large intalled base and a potentially well-developed source of Unix application

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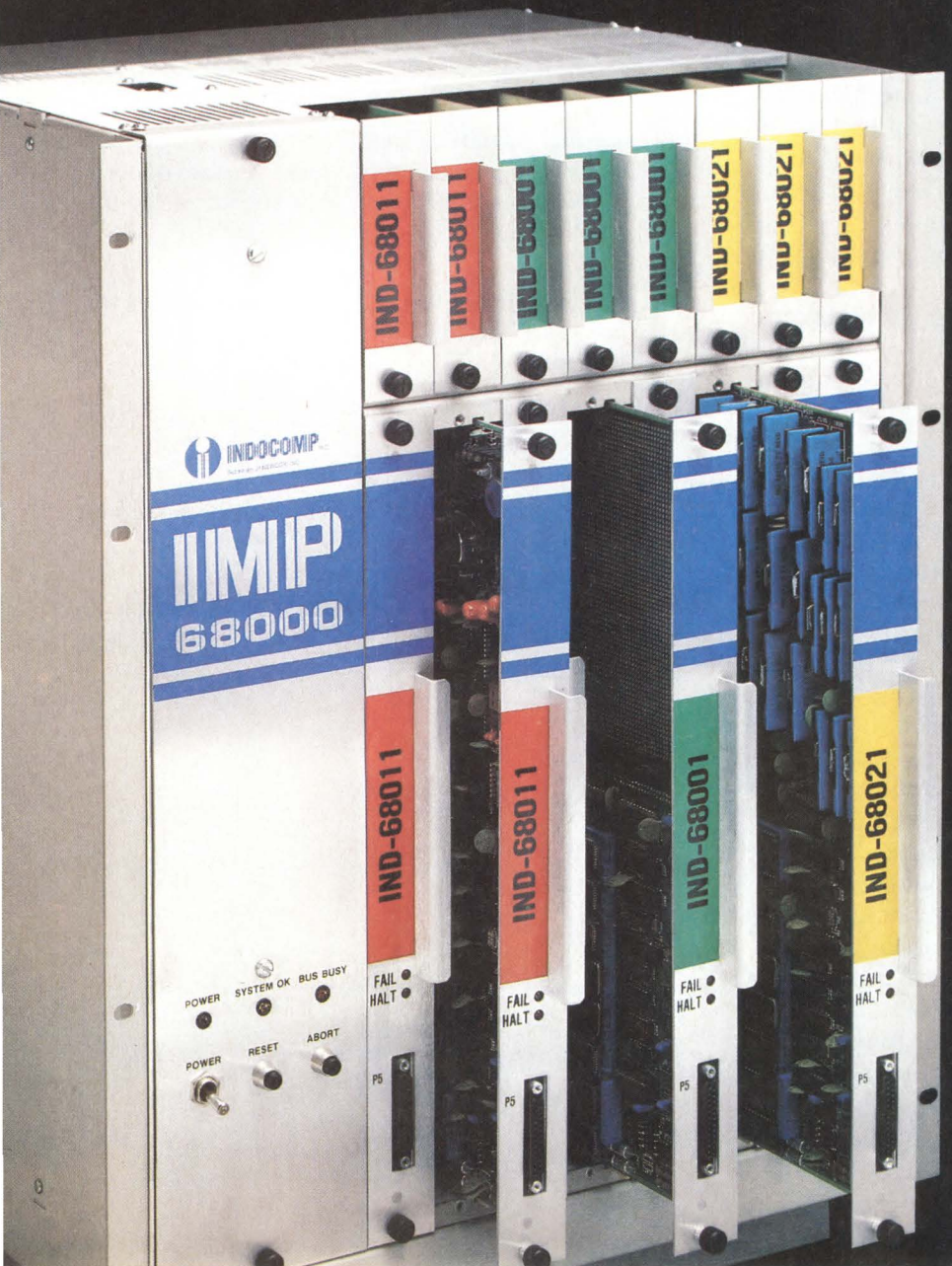


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CIRCLE 61

programs, might also influence the HP-UX operating system. This is because both Xenix and HP-UX are being selectively enhanced with Bell System V and Berkeley features to the same System III definition. Thus, conformance between the Xenix and HP-UX is likely.

*Although Unix is emerging as the standard, its system facilities must be reevaluated in light of changes in the workstation environment.*

In support of low cost computer systems, Hewlett-Packard engineers are also examining methods of subsetting HP-UX without sacrificing compatibility or an easy growth to the higher performance systems. Code-compaction and reduction techniques for both the operating system kernel and the disk-resident commands are being considered. Under investigation is a high performance distributed HP-UX operating system that allows individual workstations to rely totally on shared-network peripherals. Thus, the cost per system is dramatically reduced, but local processing power is maintained. HP-UX will also be modified to support several European languages and the 16-bit Kanji character set. Thus, localized application program solutions will be possible.

Jupiter Systems Inc's vice president and director of technical support, Peter Harris, places his confidence in the Berkeley Unix 4.2 in more direct terms by stating, "If you were marooned on a desert island and only had one operating system to run on your workstation, it would have to be the Berkeley version." Harris was under different design constraints when developing the Jupiter 12 color raster graphics workstation. Based on a 68010, and using the Q-bus as the central data distribution channel, the workstation had to have a graphics resolution of 1280 x 1024 pixels at a 60-Hz refresh rate. The graphics also had to be accessible by many users (Fig 6).

According to Harris, "It is quite common for a team of programmers, all ostensibly working on graphics programs, to be able to share a graphics display. They all have their own alphanumeric terminal, of course, but everybody shares the single graphics screen display." In a development environment, says Harris, a large percentage of clock time will be spent on the text editor or compiling and linking. These cycles typically run from a minimum of 1 min for a small change, to all day for a major new software module. When it comes time to look at the graphics screen, adds Harris, it will only take 1 or 2 s (at worst case 1 min if things are done slowly) to actually draw the picture—the result of all the programming.

This kind of situation calls for high performance, high resolution single-user workstations. To achieve high speed and access to every individual pixel, Jupiter engineers use a high speed 16-bit ALU for coordinate transformation, and assign statements to each pixel instead of using function calls. Also, a 32-bit microprocessor provides at least 21 bits of logical addressing for 1280 x 1024 pixels, while an image memory port window is mapped to the main memory bus. The result is a station, with from 4 to 32 memory planes, that allows the user to choose between a color lookup table system with a 16.7-million color palette, or two different RGB options with up to 8 bits per color and 8 bits of overlay.

Thus, workstations currently entering the market are ready to serve high performance applications from the office desk environment. While 32-bit microprocessors play a key role in making workstations powerful entities, much remains to be done on the periphery to make these micro "stars" award-winning performers. It still remains to be seen who has the best supporting cast.

### Obtaining bus specifications

Readers interested in obtaining the latest versions of open-system 32-bit bus specifications should contact the following individuals:

Multibus II:
John Beaston, Intel Corp, 5220 NE Elan Young Pkwy, Hillsboro, OR 97123.

NuBus:
George White, Texas Instruments, 17881 Cartwright Rd, Irvine, CA 92714.

VMEbus:
Wayne Fischer, Force Computers Inc, 2041 Mission College Blvd, Santa Clara, CA 95054.

IEEE Futurebus:
Paul Borrill, University College London, Mullard Space Science Lab, Holmbury St Mary, Dorking RH5 6NT England.

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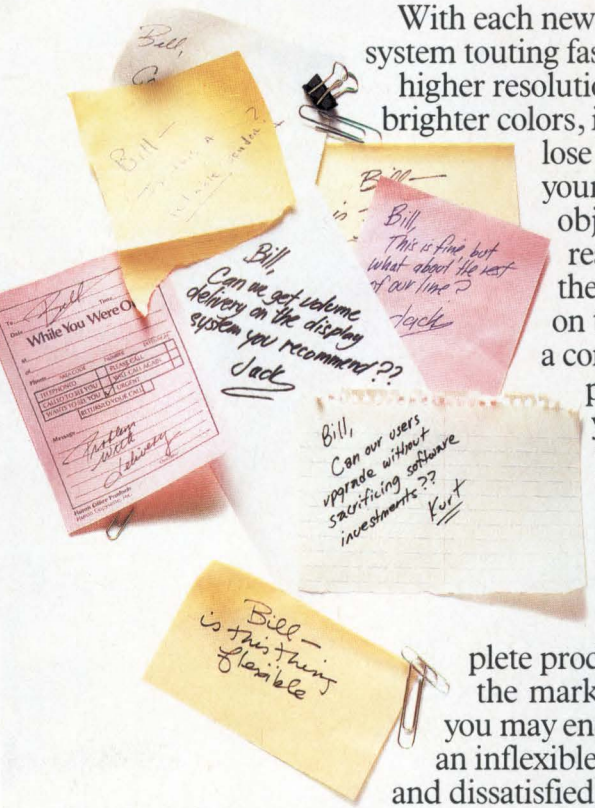


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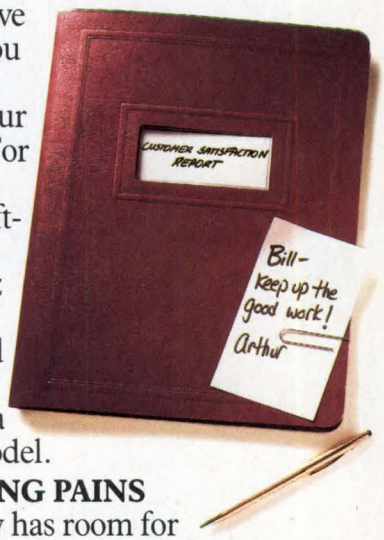


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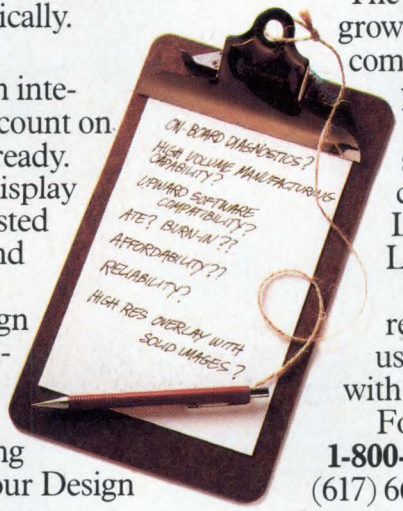


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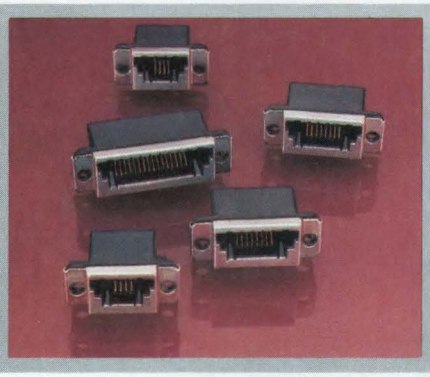

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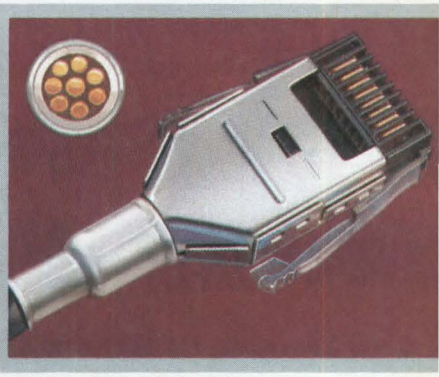

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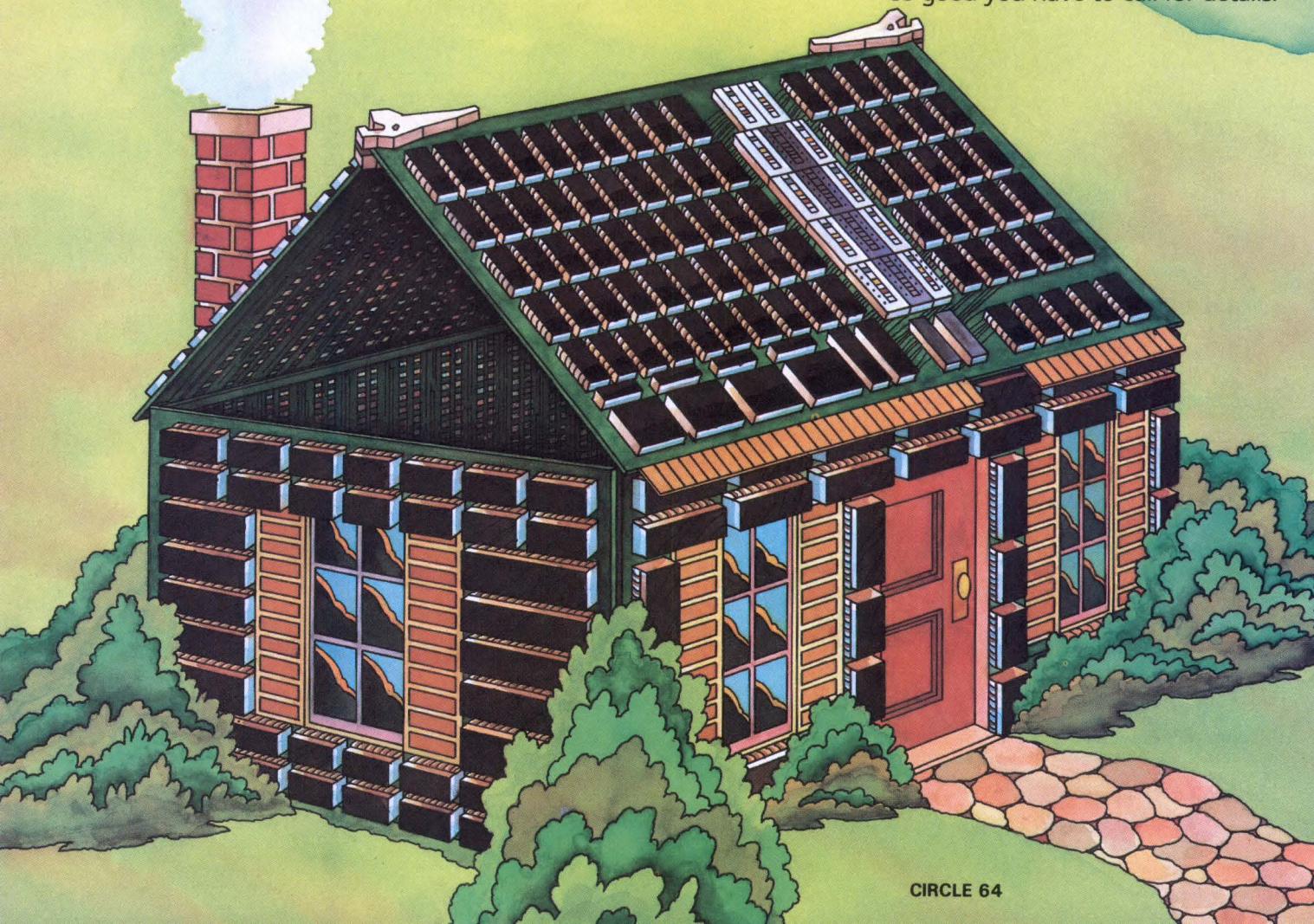

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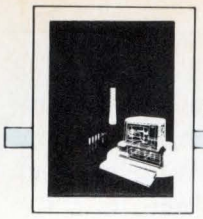




# MESSAGE PASSING SUPPORTS MULTIPLE PROCESSOR DESIGN

## Enhancing message-passing capabilities on Multibus II allows efficient data transmission among multiple processors.

**by Stephen J. Packer and Narjala Bhasker**

As microcomputer systems have evolved into complex multiple processor designs, they have been very difficult to build. This is because there has been no adequate solution to the problem of interprocessor cooperation. Until recently, the system programmer has been forced to provide software algorithms that are either very complex and slow, or are not extensible to more than two processors. Now, however, the message passing facility of Multibus II provides a hardware solution for interprocessor communication. At the same time, it gives the system programmer a standard software interface well suited for creating a distributed microcomputer-based operating system. Moreover, a special message space provision allows users to name modules with a message address rather than taking up memory address space.

*Stephen J. Packer is manager of Multibus II serial architecture at Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123, where he is responsible for Multibus II message passing design and implementation. He holds a BS and an MS in electrical engineering from the University of Washington.*

*Narjala Bhasker is a software engineer at Intel Corp, Hillsboro, OR, where he is responsible for message passing on the Multibus II serial system bus. He holds a BS in electronic engineering from the Indian Institute of Technology, Madras, India and an MS in computer science from Syracuse University.*

Early microcomputers based on a single microprocessor depended on various support chips for such functions as I/O and memory access. The integration level of these support functions required more than one PC board for use with reasonably sized systems. The Multibus I system architecture allowed separate boards supporting various microcomputer functions to be interconnected. To minimize the cost of the support circuitry needed to interface the local bus to the external bus, the local bus architecture of the chosen processor was extended. Thus, Multibus I supported the memory, I/O address space, and bit transfer width of 8- and 16-bit microprocessors.

The bus I/O space was used to access various I/O devices such as the serial universal asynchronous receiver/transmitter (UART). Even complex I/O boards for disk and tape controllers used the I/O space for control. It soon became apparent, however, that a single processor could not handle the I/O functions required for appropriate performance.

### Dividing the system into specialized functions

Intelligent I/O controllers, devised to off-load many complex I/O functions, leave more of the processor bandwidth for the application. This partitioning of the system into specialized functions, usually requiring an entire board, is quite natural. Using shared memory for data exchange between the

application processor and the special purpose, functionally partitioned modules is also natural.

In today's microcomputer systems, the system bus that interconnects functional modules is used almost exclusively for data movement between modules rather than for program execution. This data is encapsulated in control structures and is considered an interprocessor message. Memory-mapped control structures of interprocessor messages have variations as numerous as the programmers who program them. Only in those cases where hardware interfaces exist has any controlling standard emerged. The

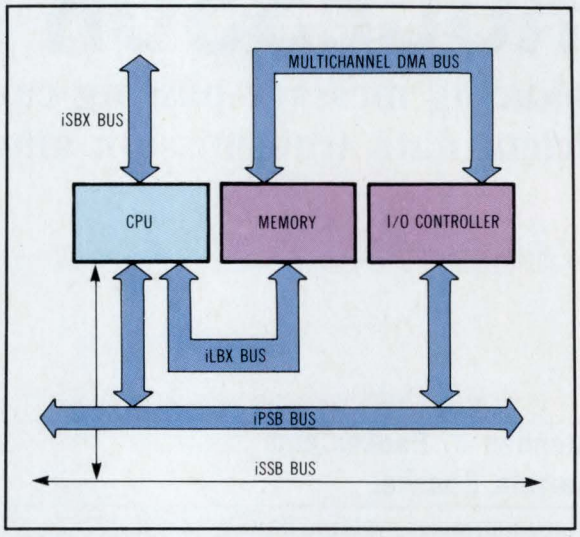
## Extending Multibus I into Multibus II

To provide computational power for increasingly complex applications, microcomputer systems have evolved from basic single-processor systems to more intricate multiple processor systems that distribute the total processing load among various hardware modules. Intel's Multibus I system architecture developed a multiple bus structure approach for these complex multiple processor systems. Using a design strategy known as functional partitioning, the Multibus I architecture provided a specialized bus for specific critical functions, thus preserving the bandwidth of the system bus for interprocessor communication and data movement.

The Multibus II system architecture refines this approach and extends its range (see Table). By providing a traditional microprocessor bus for the access of memory and I/O address space via the parallel system bus (the iPSB), Multibus II continues the evolutionary path established by Multibus I. It also prepares the way for future 32-bit microcomputers by providing 32-bit data and address paths to memory. The bus clock frequency of 10 MHz provides a maximum 40-Mbyte/s transfer rate that anticipates performance requirements for future microprocessors.

Like Multibus I, Multibus II permits multiple bus masters capable of requesting and arbitrating for access to the bus. The Multibus II arbitration policy is more involved and allows complex algorithms as well as avoiding access starvation for all modules. In addition, Multibus II provides the centralization of bus functions in a single module. This reduces the cost of multiboard systems, since all boards need not carry the overhead of providing bus-level functions such as clock and timeout.

For designs using large amounts of RAM and executing from this memory with minimal delays (see Figure), the Multibus II specification provides a local bus extension (iLBX II). Multiple iLBX II execution buses can exist in a single Multibus II system that isolates the processors' execution environments from one another and leaves the system bus for data movement between environments.




The serial system bus (iSSB) is offered as the lowest cost method of interconnecting functional modules in a system. The processor interface is identical to the message-passing facility in the parallel system bus except for initialization and error management.

### Multibus II Specifications in Brief

**Parallel system bus (iPSB)**

- 32-bit address and data path width
- 16-bit I/O address and data width
- synchronous operation with clock rate of 10 MHz
- 40-Mbyte/s transfer rate (sequential-transfer)
- up to 20 agents
- support of 8-, 16- and 32-bit processors
- 8-, 16-, 24-, 32-bit transfers
- no starvation arbitration policy
- central system functions; clock, timeout, power fail
- transfer parity, DIN connectors, distributed ground pins
- interconnect address space (512 eight-bit, one interrupt line registers) for system-level diagnostics and configuration
- 256 interrupt sources
- message passing

**Local bus extension (iLBX II)**

- 32-bit memory and 26-bit address path width
- 16-bit I/O address and data width
- synchronous operation with a clock rate of 12 MHz
- 48-Mbyte/s transfer rate (sequential-transfer)
- up to 6 agents (one master and one secondary master)
- pipelining (overlap of address and data cycles
- support of 8-, 16- and 32-bit processors
- 8-, 16-, 32-bit transfers
- optional transfer parity, DIN connectors
- one interrupt line

**Serial system bus (iSSB)**

- bus clock rate of 2 MHz
- up to 32 nodes on a maximum of 10 m of cable
- up to 20 nodes on one backplane CSMA/CD access method
- deterministic collision resolution
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**System bus extension (iSBX)**

- low cost I/O extension to CPU board

**Multichannel DMA bus**

- 16-bit address and data path width
- asynchronous operation with clock rate of 2 MHz
- 8-, and 16-bit transfers
- up to 16 nodes on cable of up to 15

purpose of these standard interfaces has been to provide a software-compatible hardware upgrade to earlier products. Hardware available for message passing in an efficient and easy-to-use manner frees the system programmer for more important tasks. Any solution to the interprocessor communication problem comprises one of two options: a pass-by-reference interface, or a pass-by-value interface.

The pass-by-reference approach to interprocessor communication passes pointers between modules without copying the actual data. This requires a shared memory resource accessible by the cooperating processors (Fig 1). In tightly coupled systems having the same types of processors with shared memory and I/O, the pass-by-reference architecture is very effective.

With this method, however, there are often very serious impediments to microcomputer design. First, the hardware architecture of shared processors must be compatible, if not exactly the same, particularly if the processors are sharing executable code. This hinders the development of hybrid systems for processors with radically different internal structures.

*A pass-by-reference architecture is very effective in tightly coupled systems with the same processor types.*

For example, mixing 8-, 16-, and 32-bit processors with memory is extremely difficult if there are byte-alignment differences among the selected processors. Also, a processor with a wider data path than the accessed memory may be restricted to specific instructions that make only byte-data references. All too often, the software algorithms must be context sensitive to allow processor-independent implementations.

Achieving low cost and high performance execution requires that memory arrays be used on processor boards. For memory-mapped messages, this onboard memory must be dual-ported and accessible from the onboard CPU and the offboard modules via the Multibus interface. This forces the two processors to view the memory by different address ranges (Fig 2). The different addresses by which the processors know the same physical memory location are called aliases. Such "aliasing" results in a loss of performance since one of the processors must recalculate all the pointers to reach the same addresses.

More importantly, the software algorithms for managing shared data structures are not extensible to more than two processors without hardware help. When two-processor algorithms are used in a system with three or more processors, a shared data structure is needed for each communicating pair. Performance suffers in a server module because it must search a list of data structures for each requester. But, the most serious difficulty is configuring such a system when modules are optionally added or deleted.

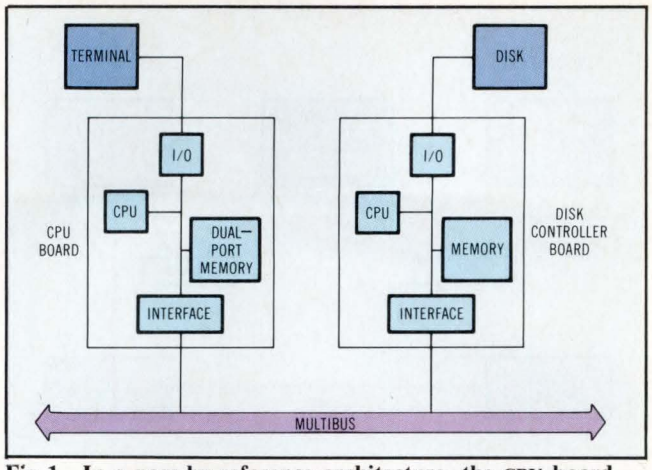


**Fig 1 In a pass-by-reference architecture, the CPU board contains a microprocessor such as the Intel 80286, and supports logic, I/O devices, a dual-port RAM array, and a parallel system bus (iPSB) interface logic. The disk controller board has a processor such as the 80188, a parallel I/O interface, and sufficient RAM for sector caching. The disk controller communicates via messages contained in data structures in the dual-port RAM of the CPU board.**

Almost all memory-mapped, message-passing schemes assume a single-application processor and a dedicated slave processor. In future systems, the functional modules must become servers that will accommodate multiple application processors. In addition, the user must be able to add and remove application modules without disrupting the system. Finally, a pass-by-reference implementation does not lend itself to memory protected systems (like Microsoft's Xenix operating system) that are not object oriented. A failing processor or faulty software can easily compromise a system using shared memory.

## Defining the pass-by-value interface

Another choice for a message-passing design is the pass-by-value strategy that copies data, rather than exchanging it, via pointers. This method is usually selected when protection criteria are more important

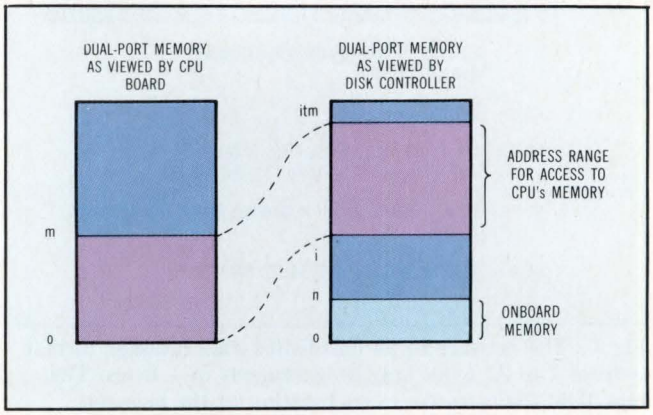


**Fig 2 In the pass-by-reference scheme, the disk controller software views the CPU's memory in different address ranges. Aliasing complicates the software and severely reduces performance.**

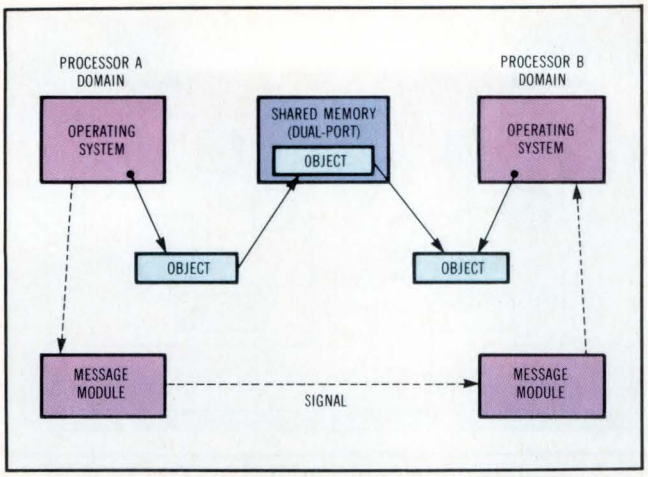


**Fig 3 The operating system of processor A in the pass-by-value approach transfers a memory object to the operating system of processor B. It invokes a message-passing module that copies the object from private memory to a shared memory area. As processor B is interrupted, it calls out its message-passing module and copies the data to a private memory area.**

than maximum system performance. Given the functional partitions of a distributed microcomputer system, a pass-by-value implementation requires a double copy of the data (Fig 3). The data is copied from application space to some internal system space, where it can be accessed by the second processor. After the first processor interrupts the second, the second can move the data to the memory space of the receiving application.

This process of double-copying the data places a considerable strain on the system's performance and yields a lower level of performance—the most serious disadvantage of the pass-by-value method. Nonetheless, a pass-by-value implementation is easier than a pass-by-reference method because differences in the hardware (eg, memory data width) are confined to the interface software. New modules are easier to develop since internal data structures need not be known to other modules. Finally, existing operating systems such as Xenix can be used without rewriting their internal structures.

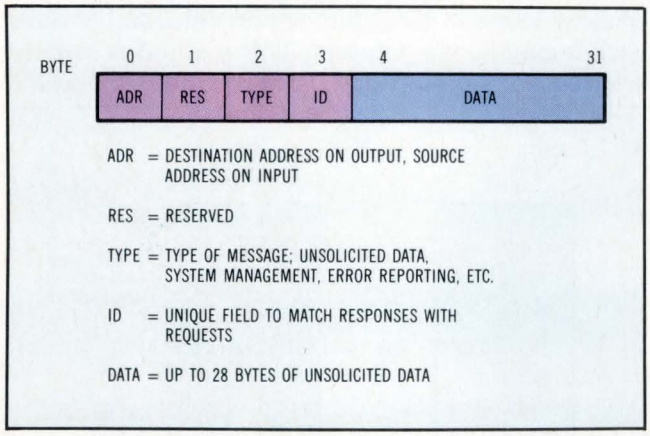


**Fig 4 The message in an unsolicited data message format is from 4 to 32 bytes long in increments of 4 bytes. The type field indicates the exact function of the message, which may be an interrupt (with no data); a data message; or a local control message between the processor and the message device. The last category is not transmitted on the bus and hence is not specified in Multibus II.**

An obvious choice for the system programmer is some high performance version of the pass-by-value method. Getting high performance, however, requires an architectural hardware change to augment the software algorithm. A distributed operating system and a distributed application have similar requirements for messages exchanged between modules. This is because both use independent processes that must communicate with other processes.

The messages received by the process providing a service to another process are unsolicited (ie, the receiver cannot predict when a message will occur). These unsolicited messages are used to negotiate the movement of varying and potentially large amounts of data. This partitioning of the kinds of messages expected in a system can be used to define a new model for message passing.

A special Multibus II message space provides a means of naming modules by a message address rather than by using a memory address. This message address space is much smaller than the address space of the supported processors, and the message-passing facility is independent of the physical medium implementation interconnecting the functional modules. This permits a software design that can support a wide range of systems—from those that use the low cost serial bus to the high performance parallel bus. This design will also eventually support the interconnection of single-chip functional modules.

Unsolicited messages can either be requests for service or a reply to a request for service (Fig 4). Thus, messages become the fundamental basis for requester/server implementations of distributed processes. The most important requirement for unsolicited messages is high efficiency and low latency for the movement between functional modules (ie, the cost of sending the message must be a fraction of the task switching time for the operating system). In addition, any delays must be short. Commands can therefore be thought of as processor interrupts with data.

Unsolicited messages generated in a system are usually quite short—usually less than 32 bytes. Nonetheless, they carry the needed control information for such diverse functions as global object management and I/O control. Within a single system, the total system capacity needed to generate unsolicited messages is self-limiting. This is due to a limit on the number of requests that can be sent before a reply is required to continue processing.

These two attributes make unsolicited messages ideally suited for a hardware first in, first out (FIFO) buffer (Fig 5). Messages bounded in size and number can be placed in the output FIFO of the sending module, and then removed by the receiving module. The FIFO implementation has two advantages. First,


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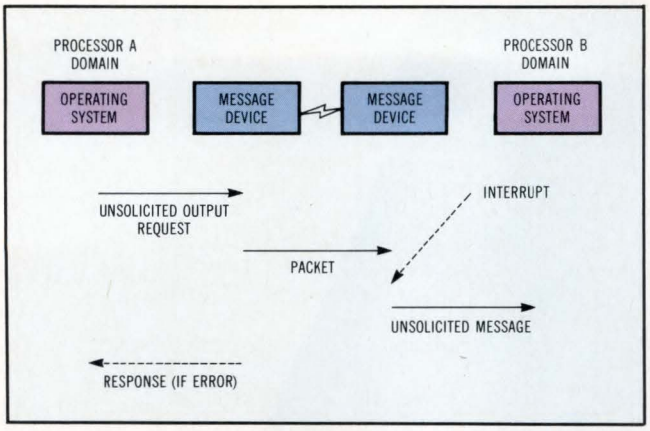


**Fig 5 An unsolicited output message is moved into the message module first in, first out (FIFO). This is very efficient for processors with a string move instruction. The message devices cooperate to move a packet containing the unsolicitied output message to the receiving module FIFO. The receiving operating system can remove the message from the FIFO on interrupt with a string move or a byte-by-byte read of an I/O port.**

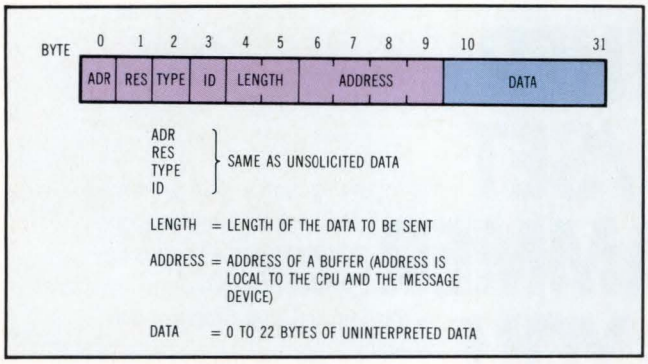


**Fig 6 In a solicited output message format, two additional fields appear in the solicited message, indicating the address and the length of the data to be sent. Only the length field is actually transmitted on the bus because the address is local to the processor and its message device.**

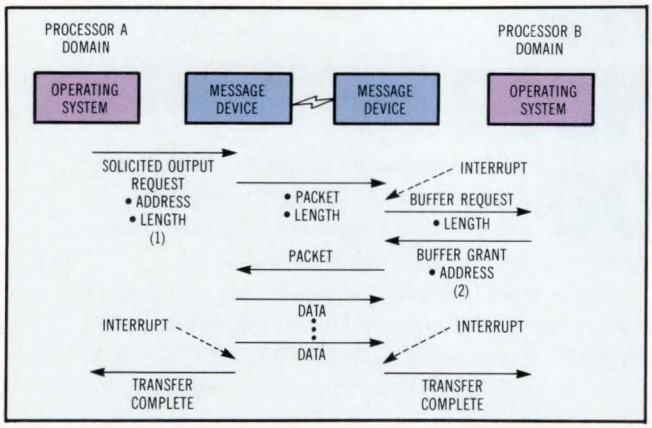


**Fig 7 The data address in the solicited message procedure is retained in the sending message device and the length forwarded to the receiving device. On interrupt, the receiving operating system receives the buffer request and replies with a buffer grant message. The message devices move the data, up to 64 Kbytes, without further processor action. On completion, both sender and receiver get a transfer complete message.**

it is easy to buffer messages that arrive with a random distribution, processed at a fixed rate. It is also easy to implement a "FIFO full" recovery strategy for those rare cases where messages are generated in excess of the chosen FIFO's capacity. Thus, overall system performance can be determined by the performance of the FIFO mechanism, not by the efficiency of the "FIFO full" recovery.

Second, movement of the message to the FIFO immediately frees the memory containing the message. This is a significant advantage to the operating system since a subsequent interrupt and context switch is not necessary in order to release the buffer at a later time.

When placed in FIFO, unsolicited messages are delivered to the operating system. This expectation is based on the high reliability of a computer bus where errors are very rare, and extraordinary recovery procedures can be tolerated. Thus, the inability to deliver a message is immediatly reported to the sender, and the recovery action determined by the appropriate software.

## Processing solicited messages

Eventually, the exchange of unsolicited messages results in the need to move a large amount of data. The bulk data movement can be accomplished by many unsolicited messages, but the cost of processing interrupts in the receiving module would bog down the system. Furthermore, such interrupts would no longer arrive randomly and in the limited number originally assumed.

An acceptable alternative is a DMA facility between functional partitions in which each end independently authorizes transfers. This facility must not compromise the low latency required by unsolicited messages. The solicited message facility of Multibus II provides this feature.

Solicited messages are initiated with a special message placed in the FIFO. The solicited message contains specific fields that define the origin and length of a buffer in the sending system's local memory (Fig 6). The length field is sent to the receiving module FIFO, where it appears as a request to allocate a buffer of specific length.

After allocating the buffer, the receiving module sends a message through its output FIFO, carrying the address of its buffer. The data movement then takes place without any further involvement of the processor in the modules. Upon completion of the data transfer, messages are generated and placed in both the sender's and receiver's input FIFO which signals the completion and return status. At this point, ownership of the buffers returns to the modules (Fig 7).

There are several advantages to this method. First, the assignment of buffers is completely under the control of the functional modules that own them. Thus, this facility is compatible with the memory

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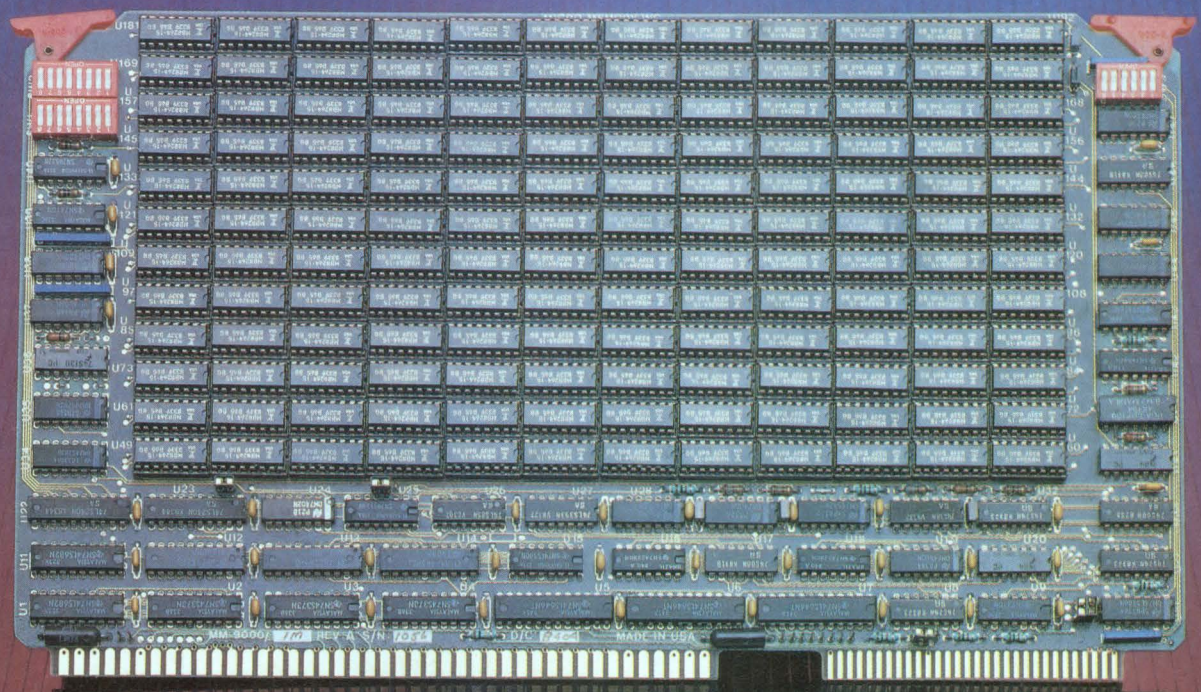

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protection features of the operating system. All pointers are used only in their natural address range. Second, the actual data movement can be controlled to optimize the bandwidth of the various buses in the system. This increases overall system performance. The data can be retrieved or stored from the module's memory at the rate of the internal bus on the module.

*Pass-by-value message-passing is usually chosen when protection criteria are more important than maximum system performance.*

Since the data transfer can be done at the full bandwidth of the interconnect bus, running all three buses at the speed of the slowest bus is not necessary. The module's CPU is not involved in this transfer except for potentially delayed access to its local memory bus during actual transfer.

The data is made into packets to suit the physical medium or to meet realtime needs for low latency access to the interconnect bus. The packets are transferred on the module interconnect bus at the optimum speed, whether serial or parallel, while unused bus bandwidth remains available to other communicating modules.

The design of the Multibus II message-passing facility can be implemented in a single VLSI device. The architecture offers a very simple device that is used only to support interrupts (unsolicited messages with no data). A more complex device is needed to support unsolicited messages with data and solicited messages. This device requires a FIFO controller, a DMA controller, a small amount of RAM for packet buffering, and a logic control unit. The serial system bus device is a derivative of the parallel message device with the replacement of the 32-bit bus interface with a serial interface unit.

While Multibus II-compatible boards do not require custom VLSI, boards designed by Intel will support the message-passing facility of Multibus II when the VLSI devices are fully tested and qualified. These VLSI devices will be available to ensure the rapid acceptance of the Multibus II specification.

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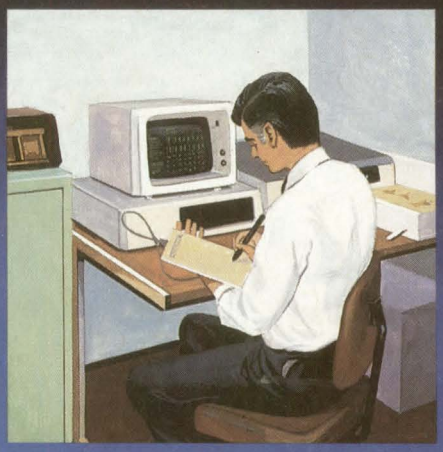

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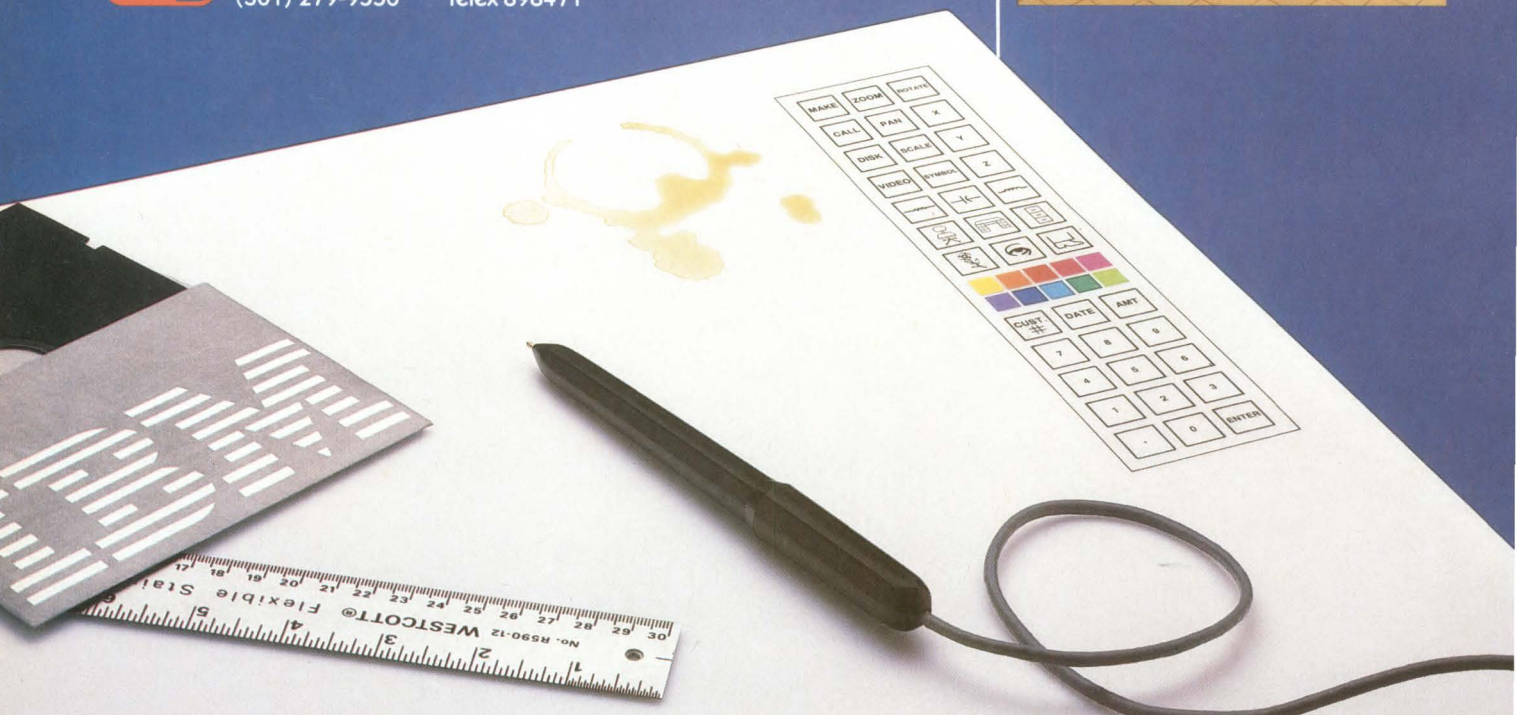
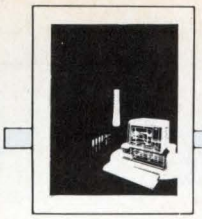






# BUS STRUCTURE EASES MULTIPROCESSOR INTEGRATION

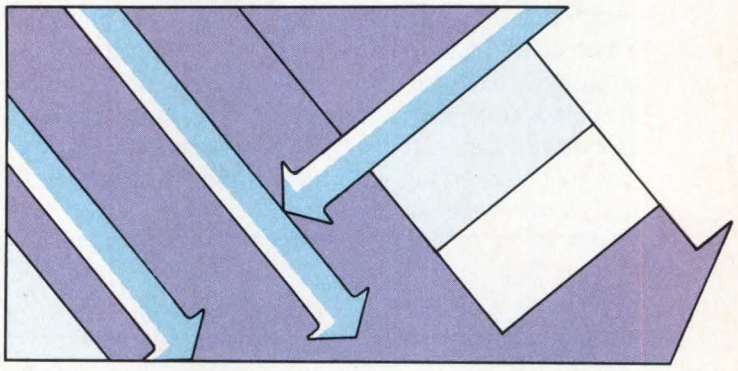
## Use of a 32-bit NuBus in memory-mapped I/O and interrupt operations aids system configuration.

**by George P. White**

Where system integrators once needed to carefully account for processor cycles, the availability of low cost, high performance microprocessors is fostering a new approach to system design. Now, auxiliary processors handle cycle-hungry support functions such as graphics or numerical processing, thus freeing the CPU to direct its power directly to the user's application. Yet, because conventional architectures wrap system resources such as memory and I/O hardware tightly around a CPU core, traditional architectures still do not provide a sufficiently flexible framework for exploiting the cost and performance advantages of multiprocessor designs.

Originally developed at the Massachusetts Institute of Technology specifically for multiprocessor architectures, Texas Instruments' 32-bit NuBus provides system integrators with system architecture independence, high bandwidth, easy system configuration, a simple protocol, and small pin count. In fact, because the NuBus maintains a simple protocol for all bus operations, 49 signal lines are sufficient to handle all transactions for up to 16 different devices in the 4-Gbyte address space of the buses.

*George P. White is manager of Nu Machine development at Texas Instruments, 17881 Cartwright Rd, Irvine, CA 92714. He holds a BS in electrical engineering from the Massachusetts Institute of Technology.*



The NuBus accomplishes this feat by supporting only read/write transactions. Unlike conventional bus structures, which require separate signals for memory access, interrupts, and I/O operations, the NuBus includes all these operations under its umbrella of read/write transactions. I/O and interrupt operations are mapped into the address space and handled just as accesses to system memory.

Furthermore, by laying system resources within this 4-Gbyte memory address space, the NuBus decouples the logical function of system resources from the physical implementation of system hardware. Instead of altering hardware switches and jumpers, engineers can reconfigure systems simply by changing variables in the NuBus address space. Consequently, without disturbing the logical architecture, system integrators are free to modify a system's physical framework to achieve the required balance between system cost and performance.

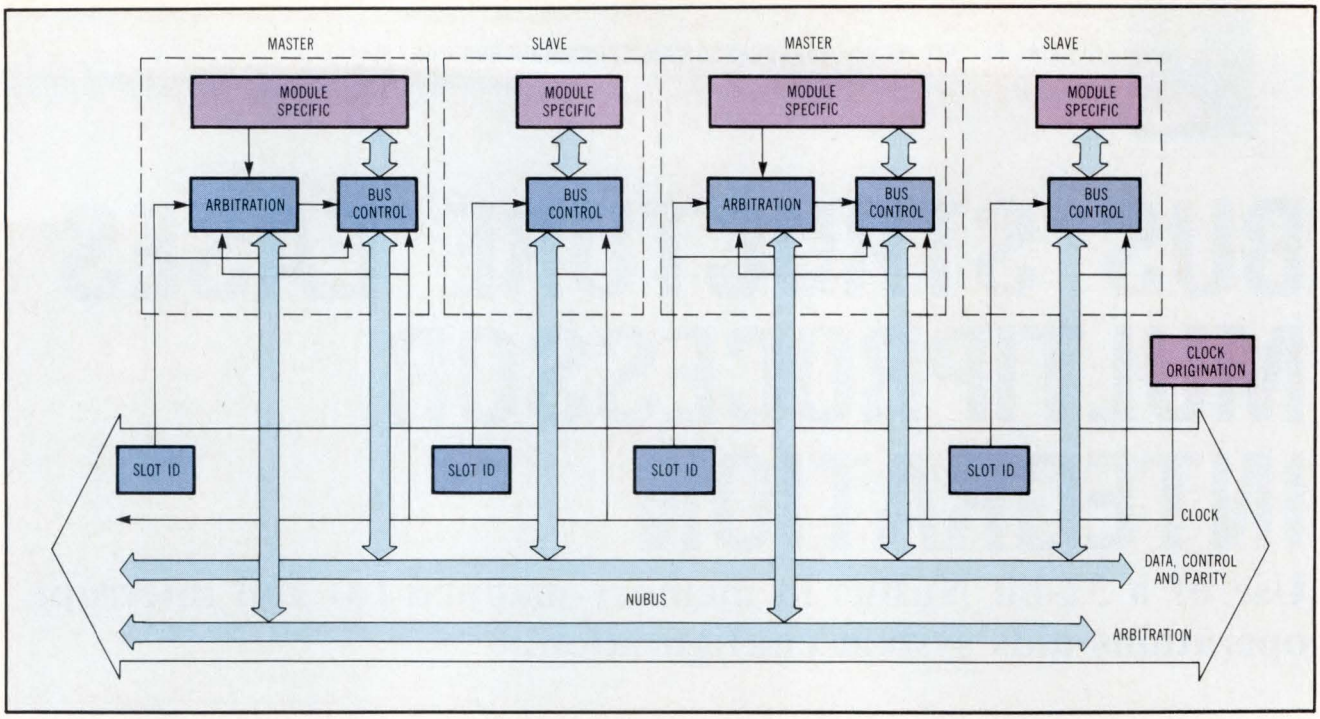



**Fig 1 Identified by a unique value wired into the backplane, each module capable of participating in the arbitration mechanism is free to serve as either bus master or slave in the NuBus. A 10-MHz system clock synchronizes this 32-bit multiplexed bus to provide up to a 37.5-Mbyte/s transfer rate in block mode.**

Accommodating I/O and interrupt operations within this framework provides good mapping between bus operations and the structures in memory, which can be manipulated by high level programming languages. By uniformly dealing with all resources in the address space, even a high level language such as Fortran can affect I/O and interrupt operations just by transferring a 32-bit number to some specified memory location.

**TABLE 1**
**NuBus Bus Definitions**

| Classification | Signal | No. of Pins |
|---|---|---|
| Utility | $\overline{\text{RESET}}$ | 1 |
| | $\overline{\text{CLK}}$ | 1 |
| Control | $\overline{\text{START}}$ | 1 |
| | $\overline{\text{ACK}}$ | 1 |
| | TM0 | 1 |
| | TM1 | 1 |
| Addressdata | $\overline{\text{AD}}$<31..0> | 32 |
| Arbitration | $\overline{\text{ARB}}$<3..0> | 4 |
| | $\overline{\text{RQST}}$ | 1 |
| Parity | $\overline{\text{SP}}$ | 1 |
| | $\overline{\text{SPV}}$ | 1 |
| Slot ID | $\overline{\text{ID}}$<3..0> | 4 |
| | Total signals | =49 |
| Powerground | +5 | 11 |
| | −5 | 8 |
| | +12 | 2 |
| | −12 | 2 |
| | $\overline{\text{GND}}$ | 23 |
| Reserved | $\overline{\text{RSVD}}$ | 1 |
| | Total pin count | =96 |

Furthermore, uniform memory of the NuBus model aids device access to memory at a lower level. The small address space supported in earlier bus structures (eg, Multibus) could force programmers to deal differently with memory, depending on the source of the memory reference. For example, a CPU would access its onboard local memory with one set of addresses, while references to the same memory originating from other boards would need to incorporate an offset into that set of memory. With its single memory map, the NuBus permits any device to access any memory—even that local to a particular board—with a consistent set of addresses.

## Simple structure

Driven by a central system clock, the NuBus is a synchronized bus that provides designers with a framework free from the specific control structure of a particular microprocessor. In fact, the NuBus specification imposes few constraints on system design—any module that can arbitrate for the NuBus can potentially serve as bus master (Fig 1).

No particular slot position is defined as the bus master. Instead, each slot has an identification hardwired into the backplane. Consequently, boards can be differentiated without the need for jumpers or switches. Besides the signals shown in Fig 1, the only other signals required by the NuBus are reset and power (Table 1). Although adopting a triple-height Eurocard form, the NuBus specifies use of only a single 96-pin connector and uses only 49 of those for signals—relegating the rest as extra power and ground lines.

To the system integrator, this low pin count benefits both present and future designs. Having fewer interconnection pins in current designs translates into more mechanically reliable systems. On the other hand, future systems can easily migrate to designs using VLSI bus interface chips, which demand low pin count for low cost designs.

With its 10-MHz cycle, the NuBus supports a 37.5-Mbyte/s block transfer rate across 32 multiplexed address and data lines. Although optimized for 32-bit transfers, the NuBus also supports unjustified 8-bit byte and 16-bit half-word transactions. In contrast, a justified bus like Multibus II always places 16-bit data in the least significant 16 lines, even if the address specifies data in a more significant position in a word.

A justified bus structure permits designers to attach 8- or 16-bit interfaces to a common set of lines, but at the cost of a more complex bus structure. Moreover, the NuBus's unjustified structure results in a simpler organization at the small cost of a few more transceivers.

## Bus transactions

Each 100-ns NuBus cycle ensures that signals settle along the NuBus before receivers latch in the values (Fig 2). With the rising edge of the cycle, drivers assert (low) or deassert (high) signals on NuBus lines. After signals settle during the 75-ns (unasserted) portion of the bus cycle, receivers sample the signals on the falling edge of the clock signal. The 25-ns (asserted) portion of the signal helps avoid skew in bus signals.

All basic NuBus signals require a clock cycle. In addition, various NuBus signals combine to form higher level transactions, like those for read/write operations. In fact, the NuBus permits these transactions to be a variable number of clock cycles long. Consequently, although it is a synchronous bus controlled by a central system clock, the NuBus provides the adaptability of an asynchronous bus without losing the design simplicity of a synchronous bus.

All NuBus transactions involve a dialogue between a device requesting service (master) and a device providing service (slave). Unlike traditional systems where a bus slave is a device incapable of independent action, the NuBus master/slave concept simply describes the temporary relationship between two NuBus modules during a particular bus transaction. In fact, provided that it can arbitrate for the NuBus, any module can serve equally well as slave or master in the NuBus protocol.

In the NuBus, a transaction commences with a START signal from a bus master and terminates with an acknowledge (ACK) signal from a slave. In parallel with toggling the START signal, the master notifies the slave of the type of transaction by manipulating transfer mode (TM) and the lower 2 bits of the AD lines. Thus, with these four control signals,

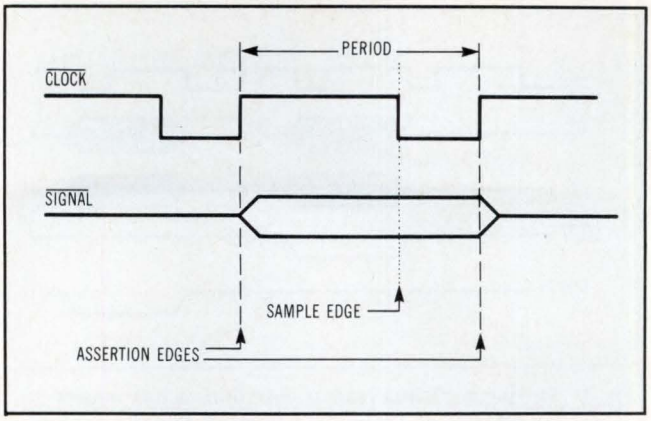



**Fig 2 Each NuBus clock cycle lasts 100 ns. During the rising edge, devices place signals on the NuBus. After allowing 75 ns for these signals to settle, receivers latch in data during the falling edge of the clock signal. A 25-ns sample period helps avoid bus skew problems.**

the master can initiate read/write transactions involving bytes, half-words, or words (Table 2).

Transactions across the multiplexed NuBus include separate phases for address and data. For example, in the initial phase of a read transaction, a bus master such as a CPU sets the address lines, asserts the TM control signals to indicate the type of transaction, and toggles the START line (Fig 3). When it has prepared its response, the slave replies in the latter phase of the transaction by placing the data on the AD lines, indicting the status of its response on the TM lines, and asserting ACK.

On the other hand, in a write operation, the bus master first places the address on the AD lines and toggles the TM and START control lines. In the next cycle, the bus master places the data to be written on the AD lines and waits. After it has latched the data, the addressed slave acknowledges and indicates the status of the completed transaction by setting the TM lines.

**TABLE 2**
**Read/Write Transactions**

| $\overline{TM1}$ | $\overline{TM0}$ | $\overline{AD1}$ | $\overline{AD0}$ | Type of Cycle |
|---|---|---|---|---|
| low | low | low | low | write byte 3 |
| low | low | low | high | write byte 2 |
| low | low | high | low | write byte 1 |
| low | low | high | high | write byte 0 |
| low | high | low | low | write half-word 1 |
| low | high | low | high | write, block |
| low | high | high | low | write half-word 0 |
| low | high | high | high | write word |
| high | low | low | low | read byte 3 |
| high | low | low | high | read byte 2 |
| high | low | high | low | read byte 1 |
| high | low | high | high | read byte 0 |
| high | high | low | low | read half-word 1 |
| high | high | low | high | read, block |
| high | high | high | low | read half-word 0 |
| high | high | high | high | read word |

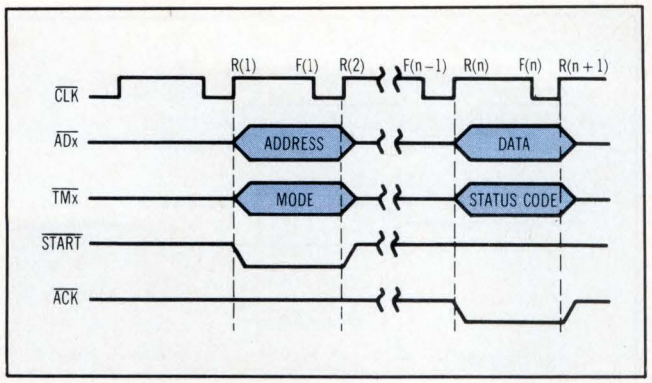



**Fig 3 During a NuBus read transaction, a bus master places the address of the desired data on the bus, identifies the transfer mode (TM), and toggles the START line. When the addressed slave is ready to respond, it places the data on the address/data lines, indicates the status, and toggles the acknowledge (ACK) line.**

Just as the AD lines double for address and data, the TM lines indicate transaction type during the address phase and the status of the result during the data phase. Of the four possible result codes, two results—bus transfer complete and error—correspond to positive and negative ACK codes commonly found in bus architectures.

Similarly, the third result code—bus timeout errors—is a signal used to guard against transactions targeted for nonexistent memory locations. For example, a NuBus master might initiate a transaction into the area of memory occupied by a certain module and receive a bus timeout code (from a separate logic). This indicates that the required module has been functionally removed from the NuBus.

The fourth result code—try-again-later—is a unique signal that should find a major role in multiprocessor systems. Logically indicating a result falling between error and success, the try-again-later code indicates that the master should simply defer the transaction to a later time, rather than jump into extensive exception-handling routines. This signal can find extensive applications in situations where a device serves more than one master. In dual-ported memory, for example, when a master finds an access blocked because of contention with another device using the memory, the master can sit on the bus—preventing its use by other potential bus masters—or release the bus and try again later. The NuBus try-again-later signal provides a mechanism to implement the latter, more efficient method.

Besides potentially improving bus throughput in multiprocessor systems, the try-again-later signal fills a critical need in avoiding deadlock in these systems. For example, in the Nu Machine, a separate 8088-based module acts as a converter between the NuBus and the Multibus (see Panel, "The key role of the diagnostic unit"). But, the use of such a converter can easily result in deadlock if the converter tries to access the NuBus at the same time that a NuBus module tries to access the converter. When this happens, both the converter and the NuBus master may find themselves deadlocked waiting for access to the other. The converter, however, relieves the potential deadlock by simply transmitting a try-again-later signal to the NuBus master and completing its own operation.

In addition to its role in boosting bus efficiency and mediating deadlock possibilities, the try-again-later signal can be used as a prefetch signal to slow devices. Moreover, in a bus converter to some slow bus, (rather than holding up a high speed bus like the NuBus), a converter can transmit a try-again-later signal to free the high speed bus and simultaneously access the information from the slower bus. In this way, the converter has the desired data available immediately upon the original requester's return.

## Block transfers

Besides simple read/write transactions, the NuBus also supports block-mode transfers. Although some bus protocols such as Multibus II permit block-mode transfers of any length, the NuBus supports transfers only of smaller blocks—2, 4, 8, and 16 words. More compact block transfers of this sort

### The key role of the diagnostic unit

Designed specifically for multiprocessor architectures, the NuBus already stars as central performer in Texas Instruments' Nu Machine. Equipped with a 68000-based CPU, the Nu Machine is designed to be independent of any particular CPU. Although such a processor-independent architecture provides system integrators with a flexible framework for crafting their own systems, it also demands an alternate approach for ensuring basic system operation in the absence of any particular CPU.

Filling this maintenance role as well as illustrating the use of the NuBus in a simple multi-CPU design, is the Nu Machine's system diagnostic unit (SDU). This unit is a separate 8088-based module with onboard memory, serial I/O for console communications, and maintenance and diagnostic test stored in onboard ROM. When the system is powered up, the SDU tests the NuBus through a series of bus transfers, identifies all boards in the system, initiates self-test routines associated with each board in the system, and signals the operator.

In addition to this maintenance work, the SDU becomes another potential master on the NuBus, acting as a converter between the NuBus and Multibus, once the system's integrity is ensured. In normal operation, the NuBus and Multibus system can operate independently. The Multibus appears as a 1-Mbyte window within the SDU's address space.

When a NuBus master addresses a memory location falling in this Multibus window, hardware-mapping logic converts the NuBus access into a Multibus reference without intervention of the 8088 CPU at bus speeds. On the other side of the window, the converter monitors each Multibus cycle for references to addresses which are mapped to NuBus. When a conversion is required, the SDU uses a Multi-to-NuBus page map to construct references to the NuBus address space.

**TABLE 3**

**Block Length and Destination Address**

| $\overline{AD5}$ | $\overline{AD4}$ | $\overline{AD3}$ | $\overline{AD2}$ | Block Size Words | Block Starting Address |
|---|---|---|---|---|---|
| don't care | don't care | don't care | high | 2 | (AD31 to AD3) 000 |
| don't care | don't care | high | low | 4 | (AD31 to AD4) 0000 |
| don't care | high | low | low | 8 | (AD31 to AD5) 00000 |
| high | low | low | low | 16 | (AD31 to AD6) 000000 |

conform more closely to the fundamental concept that a bus is a data-transfer highway freely available to any potential bus master. Furthermore, transferring arbitrarily long blocks requires a mechanism to suspend, or preempt, the transfer. This results in a more complex structure.

In addition, unlike other protocols, the master warns the slave that it is going to transfer a block and supplies the transfer length at the beginning of the operation. Supplying this information at the beginning opens the possibility for higher performance response. For example, if it is supplied with the size of the transfer beforehand, a slave has the opportunity to speed the transfer by prefetching the requested data from its storage.

By setting address bits AD2 to AD5, the bus master indicates the length of the block in the first phase of the transaction, as well as the destination address of the block (Table 3). In subsequent phases of the transaction, the bus master transmits (in block write) or receives (in block read) successive words from memory until the requested amount of words has been transmitted or an error occurs.

As each word within a block transfer is read or written, the slave uses TM0 as an intermediate ACK. The slave sends the ACK only after the final word in the block transfer has been transmitted.

## One for all

Unlike other bus architectures, read and write serves for all operations on the NuBus, including I/O and interrupts, because I/O and interrupts are mapped into the NuBus's 4-Gbyte address space. In fact, all devices occupy a reserved portion of the NuBus address space specified by each slot's ID (Fig 4). Thus, the device that occupies slot 0 may occupy addresses between F0000000 to F0FFFFFF.

Originally popularized by Digital Equipment Corp's PDP-11, memory-mapped I/O operations write to memory addresses instead of using special I/O instructions or wires. Instead of a memory cell, the specified location contains a universal asynchronous receiver/transmitter command register. As a result, high level languages gain the ability to deal with I/O directly. Furthermore, the same memory management schemes that translate memory references and isolate system memory from application programs, now apply to I/O. Consequently, application programs can safely draw on a subset of system resources directly without concern that users might intrude on sensitive areas.

In the NuBus, a similar situation applies to interrupts. To initiate an interrupt in conventional systems, a device asserts a special line that runs to the CPU. When the CPU acknowledges the interrupt, the device replies with some identifying code that the CPU uses to enter an interrupt software routine. These conventional systems need only deal with the problem of detecting the source of an interrupt.

On the other hand, a multi-CPU system not only needs to specify the source of an interrupt, but must also be able to post an interrupt to a specific device. Thus, the NuBus maps interrupts into its address space so that devices can direct interrupt requests to specific devices.

Memory-mapped interrupts become particularly important in systems that can support multiple bus masters. Where a conventional approach would require a separate wire for each potential bus master, the NuBus approach provides a more flexible, less hardware-dependent approach.

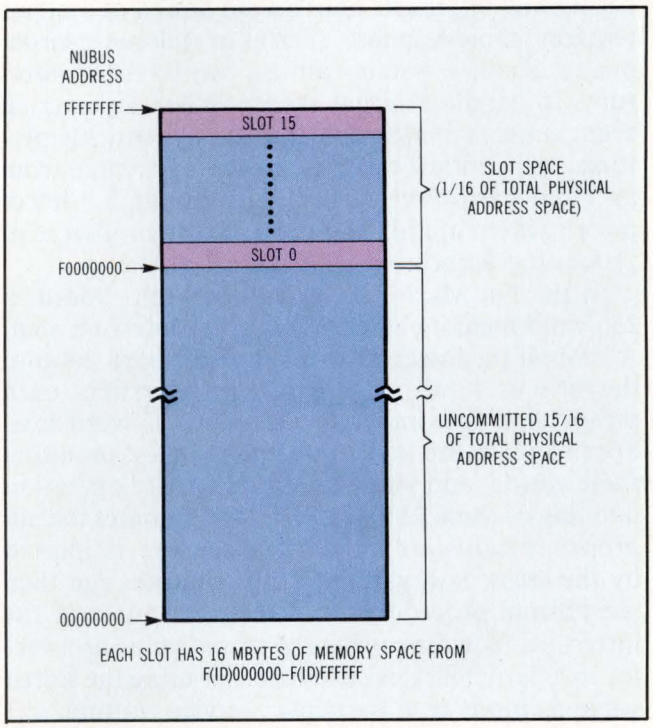



**Fig 4 The NuBus associates each of its 16 slots with a reserved portion of its 4-Gbyte address space. Each slot spans an address range from F(ID) 000000 to F(ID) FFFFFF. Thus, slot 0 fills addresses from F0000000 to F0FFFFFF.**

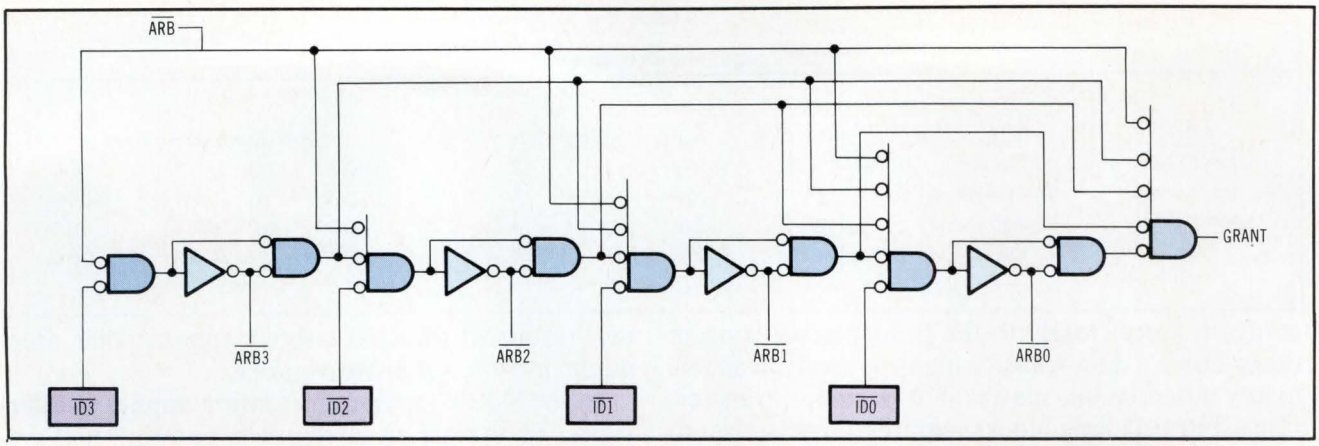



**Fig 5 Simple combinatorial logic is sufficient to implement the NuBus arbitration (ARB) logic. The $\overline{ARB}x$ lines are common to all modules, while the $\overline{ID}x$ inputs are unique to each card. The $\overline{ARB}$ signal is asserted if the module is requesting the bus, while the grant signal indicates whether the $\overline{ARB}x$ lines match the slot's $\overline{ID}x$ lines.**

Furthermore, as separate system resources evolve into more powerful devices, memory-mapped interrupts provide a graceful migration path. For example, devices such as disk controllers are gaining more independence from the CPU. After transferring a block of data between memory and disk, a smart controller on the NuBus can write its status word to a special location, interrupting the CPU for further action. The NuBus offers system integrators a simple mechanism to take advantage of such powerful techniques.

Using the NuBus's interrupt structures, programmers can easily implement advanced features like coroutines, in which a high level language issues an interrupt to another process. Similarly, software-configured interrupts like this aid design of systems requiring rapid response, such as in realtime environments. Here, a system can use two levels of interrupts to handle external events. When an external event causes an interrupt, the CPU can quickly perform some critical task (eg, removing a value from an input hardware register), and dispatch a lower priority interrupt to itself to handle any subsequent processing associated with the external event.

In the Nu Machine's 68000-based CPU board, a 256-word memory block serves as the interrupt area. Although the lower 32 words are not used because the 68000 uses only seven hardware interrupts, each priority level falls into a corresponding 32-word area. Special hardware logic on the CPU board monitors these words, and when it detects a write operation into any of these 32 words, the logic initiates the appropriate hardware interrupt procedure supported by the 68000. Software-interrupt routines can then use normal procedures to detect the source of the interrupt, including using the stored value as a vector to a particular device handler, or using the stored value as input to a particular service routine.

In addition to providing a consistent approach for handling I/O and interrupts, the memory-mapped approach adopted by the NuBus permits system integrators to rely on software to configure systems. In the Nu Machine, each hardware module uses a special set of memory locations within its reserved memory to specify configuration information. Thus, during a software configuration phase, an operating system can simply access these locations to obtain necessary system information. If a module is not present, the bus timeout that results during the NuBus transaction tells the operating system that the corresponding device is unavailable and should not be included in the system definition.

## Critical arbitration

In any bus-oriented system with more than one potential master, the concept of arbitration is crucial. Multiprocessor systems such as the Nu Machine rely on bus arbitration mechanisms ensuring that each processor is allowed access to the bus regardless of its defined priority. The NuBus, optimized for multiprocessor architectures, provides a fair arbiration mechanism that guarantees access to any module requesting bus access.

The NuBus traces its arbitration lineage through a long history of bus protocols extending back to the S-100 bus. In the daisy chain arbitration technique, a signal propagates serially through all boards in the backplane. If it decides that it wants to assume control of the bus, a board simply does not propagate the signal.

Unfortunately, this approach does not provide a fair distribution of bus cycles. Boards closer to the daisy chain origin stand a better chance of acquiring the signal and of starving lower priority boards of bus access. Furthermore, this approach requires that all slots on the backplane be filled or bypassed with jumper cables. This is often at the cost of mechanical difficulties as jumpers fall off or users connect incorrect pins.

In the analogous software situation, scheduling algorithms can avoid starvation of lower priority tasks caught in a mix of higher priority processes. However, arbitration demands strict mechanisms integrated into the basic structure of the bus itself. The

mechanism cannot provide exceptions. During multiprocessor system design, an engineer cannot prejudice the architecture with the idea that a certain potential master should be allowed more bus cycles than others.

For example, when compared with a disk controller, an Ethernet communication module might be considered a lower priority device and assigned a correspondingly lower hardware priority. However, the data transmitted through this communication module may assume major importance in the system. Consequently, a system integrator must be certain to disassociate hardware priority on the bus from importance. Conventional daisy chained systems force designers to associate hardware priority with importance. The NuBus, however, maintains a strict approach to fairness in arbitration. No single module can be weighted to enjoy more bus activity at the expense of others.

To do this, the NuBus adopts a parallel scheme. Bus arbitration begins when one or more potential bus masters assert the bus request (RQST) line, and each attempts to place its unique ID on four open-collector lines on the bus—the arbitration (ARB) lines. Each slot is given a unique identification by a 4-bit ID code hardwired into the etch of the backplane.

In placing ID codes on the ARB bus, the boards use a strategy common to other bus architectures that ensures that only the highest ID stays on the bus. If a board sees a bit that is of a higher order than its own bits as it puts its code on the bus, the board lifts its signal. For example, if the board with ID4 attempts to place its ID on the ARB lines (assert ARB2) and finds that ARB3 is already asserted—indicating that a higher ID is already on the ARB lines—it simply removes its signal.

Implemented with simple combinational logic (Fig 5), this technique dictates that only the highest ID remains on the ARB lines at the end of the two bus cycle arbitration contests. Because this arbitration contest occurs over separate lines in parallel with read/write transactions, this mechanism does not cut into bus throughput. In fact, because typical NuBus transactions require at least two bus cycle, a new bus master will be ready to initiate its own transactions when the previous bus master has completed its turn on the NuBus.

### Determining fair arbitration

Although this arbitration scheme does seem to involve a priority aspect, fairness counteracts it. If three boards request the NuBus simultaneously, the highest numbered board wins. However, fairness ensures that the lower numbered pair of boards will gain access before that particular higher numbered winner gains the bus again.

Fairness in the NuBus is a simple protocol—once the RQST line is asserted, no other boards are allowed to request the bus. For example, if three boards want the bus at the same time, they will all assert the RQST line at the same time. The highest numbered board will win out, but the other two boards will still be asserting the RQST line. After the last board of the three uses the bus, the RQST line will become deasserted. This then starts another arbitration contest.

In addition to serving as the medium for bus request and achieving arbitration fairness, this single RQST line also mediates bus locking in the NuBus. Bus locking is typically used for indivisible test and set instructions used to implement semaphores for interprocess communication. In bus locking, once a device wins the bus, it simply continues to assert RQST and maintain its ID on the ARB lines. During the next arbitration, the same board will always win because, by the definition of fairness, its ID will always be the highest numbered in the current arbitration round. The NuBus needs no extra wire, mechanism, or state to accommodate bus locking. This mechanism is enfolded within the larger concept of fairness.

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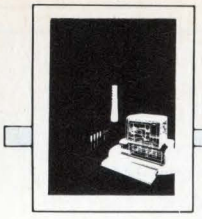



# VERSATILE BUS SUITS REALTIME PROCESSOR APPLICATIONS

## Industrial applications are well suited for VMEbus configurations with 32-bit CPU and PDOS operating systems.

**by Wayne Fischer and Paul Roper**

Each year, more designers are using existing buses and backplanes instead of reinventing the wheel for each new project. The engineering time, prototyping, testing, evaluation, startup production cost, and field support required for each new bus are now at the point where not even large companies such as Motorola (Phoenix, Ariz) and Intel (Hillsboro, Ore) are willing to take on the task by themselves. Once a bus is introduced to the market, it needs large manufacturer and user bases in order to survive and be successful. Therefore, the current market trend is for several major semiconductor and/or equipment manufacturers to codevelop new high performance buses and then cointroduce them to the market with a show of multiple-source support. The VMEbus makes its mark with such a beginning.

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The VMEbus has recently become the most talked about and designed-in 8/16/32-bit high performance bus on the market in both the U.S. and Europe. Besides providing a high performance backplane, the VMEbus, which in itself has become a worldwide standard in packaging of computer-based systems, uses the popular and standard Eurocard and associated mechanics. Even though the MC68000 is the most often implemented microprocessor on the VMEbus, the bus is specified to be processor independent. Microprocessors such as the Z80, Z8000, 16032, and 80186 have also been designed onto the VMEbus.

Even Intel endorsed the VMEbus manufacturers and users by counteracting with its Multibus II specifications in November 1983. Multibus II extends Multibus I and provides a solution for 32-bit operations. It uses essentially the same mechanics as the VMEbus, except for the card depth (220 mm versus 160 mm). The overall performance of Multibus II is also very much the same as that of the VMEbus. The major difference between them is that Multibus II is synchronous and uses multiplexed data transfers, whereas VMEbus is asynchronous and uses nonmultiplexed data transfers.

### Developing critical mass

In late 1983, VMEbus achieved what might be termed "critical mass." Earlier, in October 1981, the joint introduction of the VMEbus to the industrial press in Munich set a precedent with a completely detailed specification that was developed prior to product design. This is in contrast to the earlier microprocessor days when products were developed initially to reflect a list of pinouts, as in

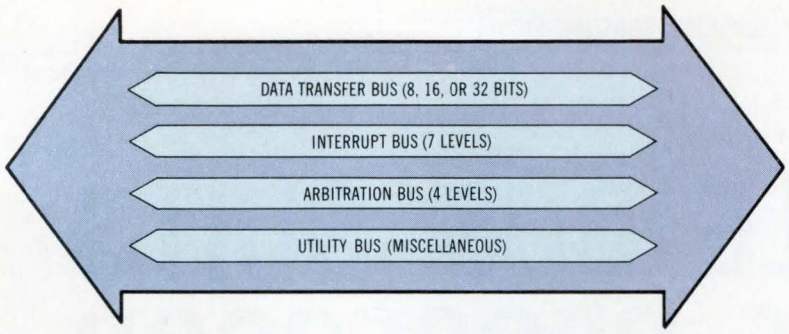


**Fig 1 The VMEbus can be functionally divided into four sub-buses: data, interrupt, arbitration, and utility, with each one specified separately in the VMEbus specification.**

the case of the S-100 bus. Earlier bus designs such as the S-100, Multibus, and others, evolved with technology and time. Incomplete bus specifications caused incompatibility among various manufacturer board designs. In addition, these early bus specifications either did not allow for expansion of new processor developments or they were too specific to a particular vendor's products such as Multibus I. As a result, the original S-100 pinout list was developed into a complete IEEE standard—IEEE 696. Although Multibus I was much better defined and controlled, design engineers were still required to clarify the specification. They then modified it to accommodate a 16-bit data path, and a 24-bit address path. IEEE 796 (Multibus I) is just now being printed by the IEEE, some 9 years after Intel originally introduced it in 1975.

VMEbus's development had a much shorter maturation period. The relatively quick acceptance and adoption of VMEbus by the industrial market place enticed the IEEE Microprocessor Standards Committee (MSC) to approach the VMEbus Manufacturers Group, consisting of Motorola, Mostek (Carrollton, Tex), and Signetics (Sunnyvale, Calif) in late 1982, to solicit a proposal for presentation to the IEEE MSC to standardize the VMEbus. The proposal presented at the March 1983 IEEE MSC meeting was overwhelmingly approved and a VMEbus Standard Project Committee began its work. Five months later, in September 1983, the IEEE Standards Board gave final approval to the VMEbus Standard Committee by assigning P1014 as the IEEE standard reference number during the standard development. Eventually, when the standard is fully approved, this will be known as the IEEE standard—IEEE 1014. The VMEbus standard should be approved by late 1984.

## Dividing VMEbus architecture

VMEbus can be functionally divided into four sub-buses; data transfer, arbitration, interrupt, and utilities (see Fig 1). First of all, data can be transferred across the backplane at 8, 16, or 32 bits at a time, on a cycle basis. The address path width can be of 3 different sizes: 16, 24, 32 bits. This allows the coexistence of 8-, 16-, and 32-bit microprocessors in one VMEbus-based system. Also, memory and I/O can be 8, 16, or 32 bits in width. Thus, it is possible for an 8-bit microprocessor to transfer data to and from a 32-bit memory, and for a 32-bit microprocessor to transfer data to and from an 8-bit memory or I/O device. Fig 2 shows the VMEbus signals used with a master and slave for data transfers.

All transfers through the VMEbus are performed asynchronously. This allows the designer to make the appropriate trade-offs between system cost and system performance when designing both master and slave boards. The master setup time, the slave response time, the master termination time, and the slave termination time can be as fast or as slow as the designer chooses. (See Fig 3 for a typical byte read cycle.)

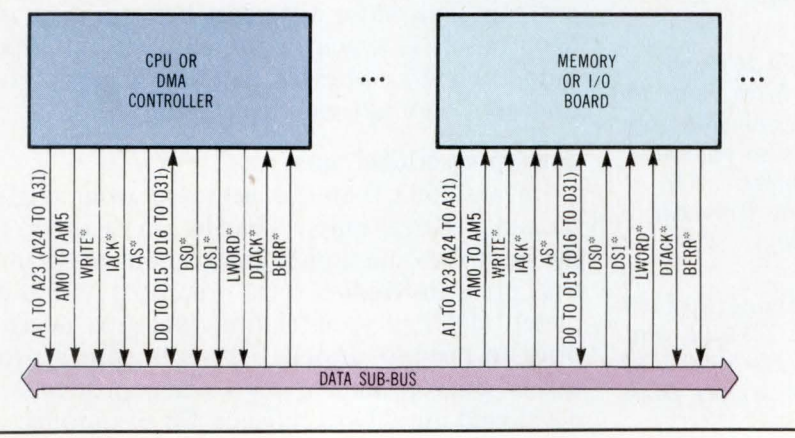


**Fig 2 Accommodating up to 20 boards, the VMEbus has boards that can function as master, slave, or master and slave.**

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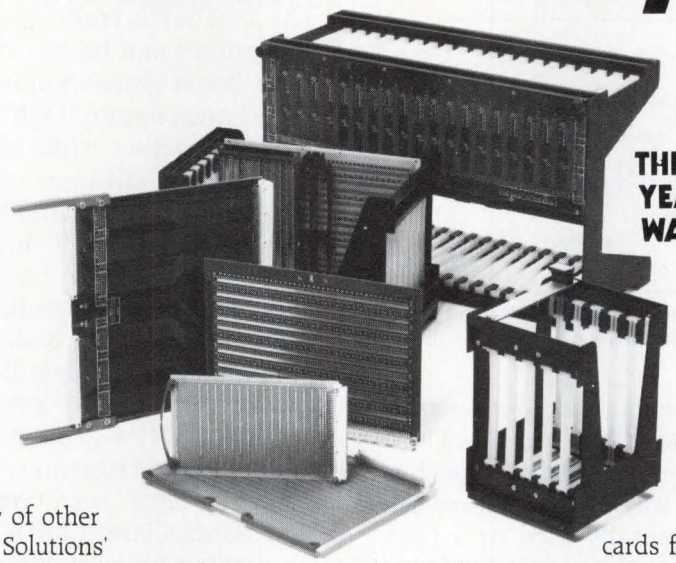

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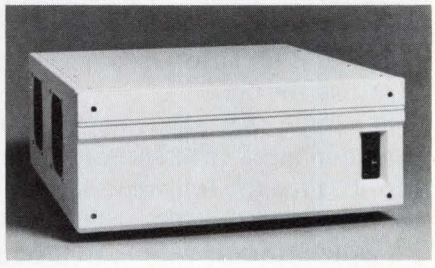

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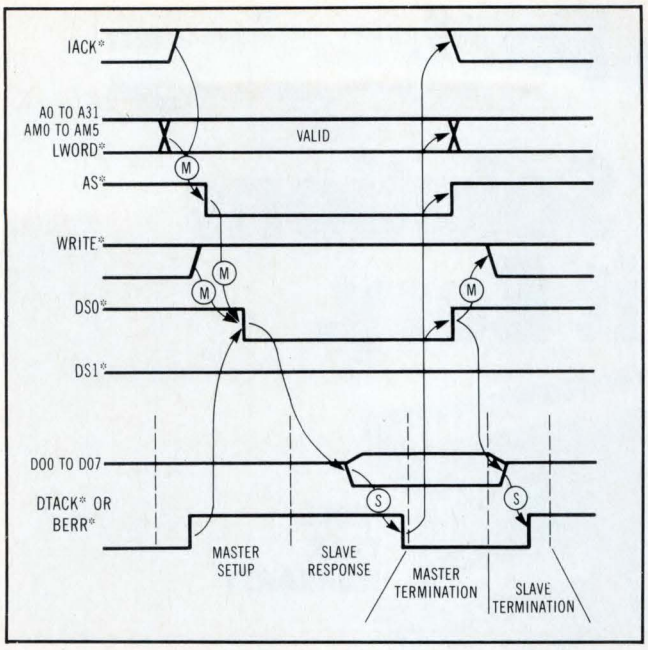


**Fig 3 Each data transfer across VMEbus can be divided into four parts, with each being as slow or as fast as the system designer requires.**

The flexible arbitration scheme uses four separate bus request lines for requesting bus control. Thus, VMEbus board designers can design the bus requester circuit one of two ways. The release when done (RWD) requester is generally used by a DMA controller that uses the bus for short periods of time and then exits the bus. The release on request (ROR) requester is usually implemented on CPU boards where the processor keeps tight control of the bus and gives it up only when another master processor must use the bus.

The logic that arbitrates the bus can be implemented in three different ways: a priority arbiter sets priorities for the four request levels from highest to lowest; a round-robin arbiter lets each level be at the same priority, with each level taking its turn at using the bus; and a single-level arbiter monitors just one level for bus requests. Within each level there can be any number of sublevel requesters (with associated masters). VMEbus uses a daisy chain for granting bus control, where the requester closest to slot one has the highest priority for that level. This scheme allows any number of bus requesters to be used in a system.

Seven lines are dedicated for hardware interrupt generation. There can be from one to seven interrupt handlers in the system at any one time, and an interrupt handler can take care of from one, to all seven, of the interrupt lines. Each interrupt response cycle, contains any amount of interrupts. During the interrupt response cycle, an 8-bit status identification or vector number is passed from the interrupter to the interrupt handler. Within a VMEbus-based system, there can be up to 7 times 256 different status IDs or vector numbers. (See Fig 4 for the bus interrupt block diagram.)

The utility bus provides a 16-MHz clock source, a system reset line, an ac fail line, a system fail line, a 5-V source, a 12-V source, a −12-V source, and an optional 5-V standby source. The ac fail line gives a minimum of 4 ms warning that dc power is about to go out of the specified operating limits. The system fail line lets a system master or monitor know that one of the modules plugged into the VMEbus has detected a failure.

## Mixing and matching boards

The VMEbus is truly versatile because any number of boards can be mixed and matched within a VMEbus-based system. For instance, due to VMEbus's asynchronous nature, high and lower speed boards can work together while processor, memory, and I/O boards of different data and address path widths can also coexist. The Eurocard mechanics allows for mixing of single-height boards with double-height boards, and mounting in various mechanical configurations. As such, VMEbus boards, designed and built to the VMEbus specification, can coexist regardless of speed, data and address path width, or other features.

This flexibility also allows greater ease in porting various operating systems to boards having different processors. Thus, such companies as Force Computers (Santa Clara, Calif), Motorola, Mostek, and other VMEbus manufacturers have ported (or are in the process of porting) Unix V to their VMEbus-based systems. Due to Motorola's effort in doing the initial port to the 68000, companies such as Unisoft (Berkeley, Calif) and Santa Cruz Operation, Inc (SCO, Santa Cruz, Calif) can easily do a custom port of Unix V to almost any computer system.

With all its popularity and user acceptance, Unix is still not the answer for all people to all things. The two main criticisms of Unix are its bulky size and its lack of realtime responsiveness, particularly to interrupts. Because of its memory requirements for execution and disk storage, Unix cannot be practically considered as a ROM-able and realtime operating system.

This leads to the second major operating system type—the realtime operating system. This system is

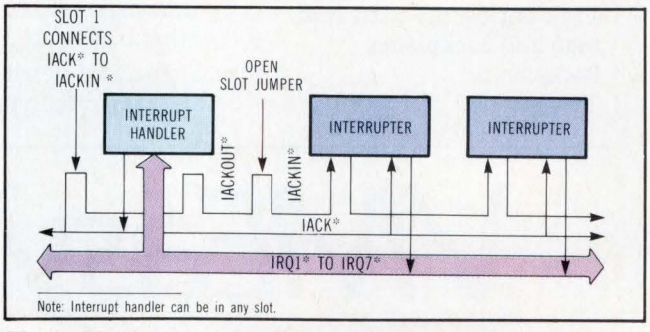


**Fig 4 The interrupt handler can be in any slot, and can handle from one to all seven of the interrupt levels on the VMEbus. Each level can have as many interrupters as necessary.**

**Benchmark Comparisons between PDOS 2.6c and VERSAdos 4.2**

| Benchmark | PDOS 2.6c on VME Force System (in seconds) | VERSAdos 4.2 on Exormac System (in seconds) | Execution Speed PDOS vs VERSAdos + |
|---|---|---|---|
| 10 million rotates | 51.43 (12)* | 54.39 (12)* | – |
| 100,000 task swaps | 21.98 (6) | 48.60 (16) | 2.1 x |
| 100,000 read time of day | 36.85 (6) | 50.89 (20) | 1.3 x |
| 100,000 set system event bit | 26.39 (8) | – | – |
| 100,000 test system event bit | 14.34 (8) | – | – |
| 100,000 resource allocations | 56.87 (10) | 102.15 (60) | 1.7 x |
| 100,000 send and receive 64 bytes | 130.89 (14) | 236.34 (74) | 1.7 x |
| 1 million task synchronization | 115.87 (50) | 2491.64 | 20.3 x |
| 100,000 lock and unlock file | 87.34 (16) | – | – |
| 100,000 10-byte record rereads | 105.44 (22) | 648.70 (82) | 5.8 x |

*Program size in bytes.
+Adjusted by .95 for differences in memory speeds.

Note: Both machines insert wait states and thus first benchmark should be used to adjust timing comparisons for hardware differences.

especially suited to industrial applications. The two major choices for a 68000-based system are Motorola's VERSAdos and Eyring Research Institute's (Provo, Utah) PDOS. While VERSAdos can be considered a high performance operating system because of its relatively large size and diverse functional features, it is somewhat slower in its realtime responsiveness. Eyring's PDOS realtime operating system has a more versatile approach. As the Table shows, it has relatively fast response time for interrupt handling, task switching, message passing, and task initiation. In addition, because of its smaller size, integrating application software to the PDOS operating system is easier than to VERSAdos. In fact, functionally identical PDOS library routines are 48 percent the code size of the VERSAdos equivalents.

## The realtime alternative for VMEbus systems

Initially developed for the Texas Instruments 9900 microprocessor, PDOS is a powerful multitasking, multi-user, realtime operating system. In 1982, its overall system features were enhanced and at the same time, it was transported to Motorola's 68000 processor. The modular approach and hardware independence features of PDOS allowed its port to the Force systems to be completed in only a few days.

PDOS is written in assembly language for fast, efficient execution. Its size, accuracy, and power make it well suited for process control, system development, educational and scientific environments, factory automation, and industrial applications. As development systems can be very expensive, PDOS's small size and low disk dependence cut costs by allowing most applications to be developed and implemented on the target system.

The PDOS kernel is the multitasking, realtime nucleus of the operating system. The main responsibilities of the kernel are task scheduling, synchronization, and memory allocation. Other functions include system clock maintenance, character I/O, and even processing. The additional modules comprising the PDOS system are the user configurable and hardware dependent Basic I/O System (BIOS) and universal asynchronous receiver/transmitter (UART) modules, file manager, debugger, monitor, and floating point package. Each is a separate module that can be selectively added to the final product.

Tasks are the components comprising a realtime application. Each task is an independent program that shares the processor with other tasks in the system. User tasks interface to the PDOS kernel and file manager through the one word 68000 line-A instruction. The highest priority task that is ready always executes. Tasks on the same priority level are scheduled on a round-robin basis.

Pending some external event, a task may suspend its execution, allowing lower priority tasks to execute. This event can be a hardware interrupt, a delayed software counter, or a signal from another task. The context switch time from the occurrence of the event to the time that the suspended task is executing again is less than 150 ms in an 8-MHz, no wait-state basis.

Intertask communication and synchronization in PDOS involves mailboxes, message buffers, and single-bit events. Queued message buffers move 64-byte messages with ease in mapped and non-mapped systems. Tasks can be suspended on multiple events, allowing system timeouts along with the external event. Mailboxes are designed for direct task communications.

The PDOS file management module serves to support sequential, random, read only, and shared access to named files on a secondary storage device. These low overhead file primitives use a linked, random access file structure and a logical sector bit map

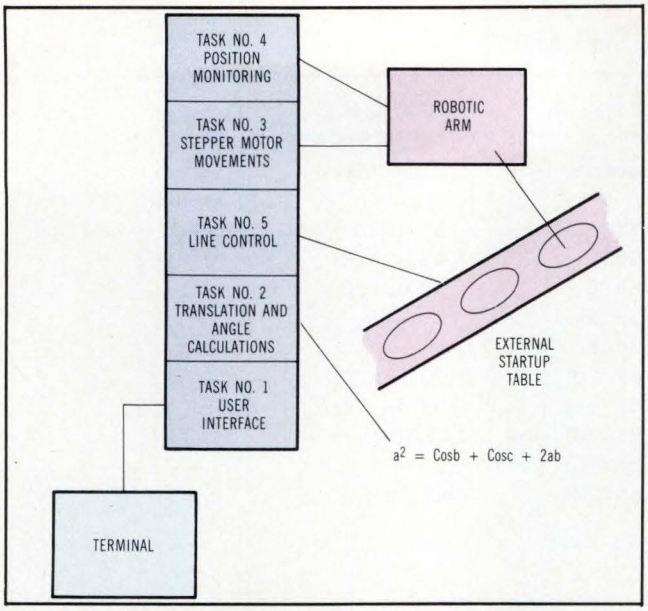


**Fig 5 A robotic application can require many tasks executing at different priority levels. To achieve a total solution, each task must function and communicate properly.**

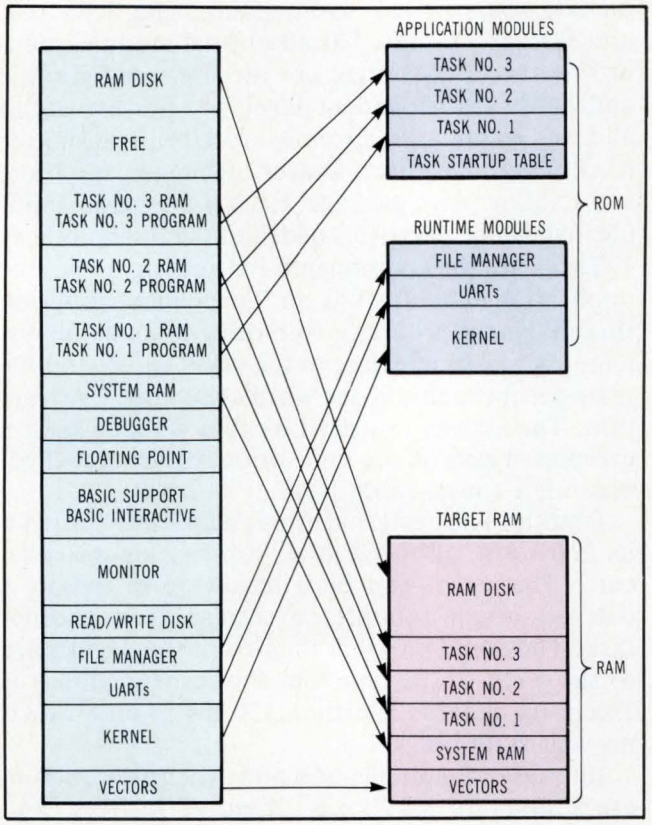


**Fig 6 A final debugged application is configured to an EPROM target solution. This method eliminates the need for unnecessary and costly development hardware and software.**

for allocation of secondary storage. In addition, up to 32 files can be opened simultaneously and no file compaction is ever required.

PDOS modules are position independent and may reside anywhere in memory without reassembly. The file system is not disk intensive and is thus suitable for all storage device types. One of the more popular configurations of PDOS uses RAM as a disk device. This is often battery backed up and well suited for hostile environments.

In standalone applications, a simple external start-up table is all that is required to link user programs to the PDOS kernel residing in EPROM. The PDOS kernel, BIOS, and UART modules, file manager, and floating point package require less than 12 K of EPROM. Other EPROM-able modules include a fast, industrially oriented Basic interpreter, assembly debugger, and command line processor. (See Fig 5 for a typical development cycle for a robotic arm.)

PDOS is provided on a floppy disk-based, development/target system that has been interfaced to a moderately dumb robotic arm. An assembly language program is developed to output the stepper pulses at regular 3 ms intervals to the robotic arm. (PDOS tasks operate equally well in supervisor or user modes.) This assembly program is linked into a high level language driver task, which executes on a high priority and suspends on an event waiting for commands through the message buffers.

A more sophisticated program is developed to transform Cartesian coordinate commands into wrist, elbow, and shoulder movements. These commands are "mailed" to the robot driver task and the synchronization event is set. This awakens the driver task, which then retrieves the commands, outputs the movements, resets the event, and continues to repeat the process. During the 3-ms interval, the driver task again suspends, allowing other tasks to continue executing. This enables concurrent processing of the next command.

Other tasks can also be added to monitor the arm position and record various results on a RAM disk. This can be done with a possible user interface task to adjust control parameters on-the-fly. Since the target is for a hostile, standalone environment, the resulting system can reside in EPROM. Any PDOS system modules not used need not be included. The result is an efficient and cost-effective product that can be easily reproduced (Fig 6).

It was for these features that Force Computers teamed up with Eyring Research Institute to port PDOS to the company CPU and I/O boards. A major trend has begun this year in most industries toward automating processors with higher performance microprocessors, based on standard buses, such as VMEbus, and standard operating systems, such as PDOS. Not only does PDOS run very efficiently and fast on VMEbus, but VMEbus also uses the robust capability of PDOS to its fullest extent.

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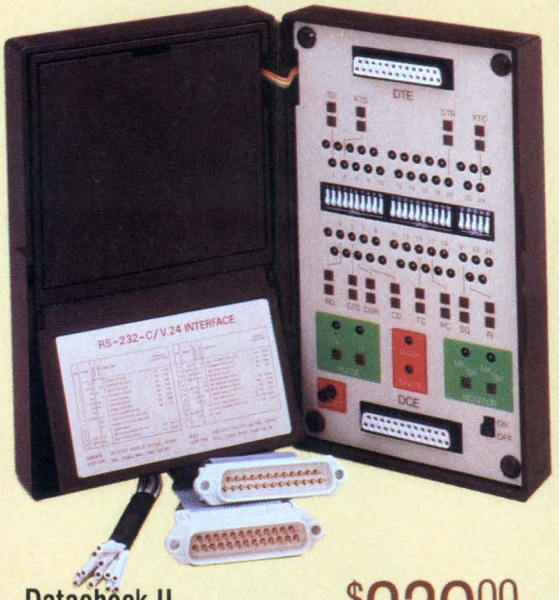


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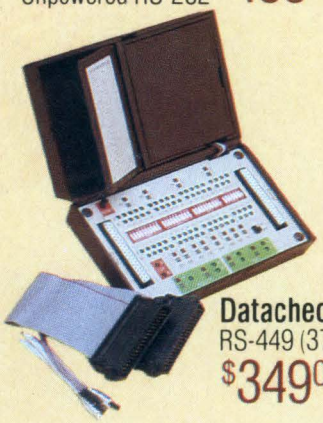

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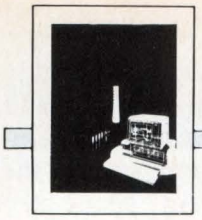
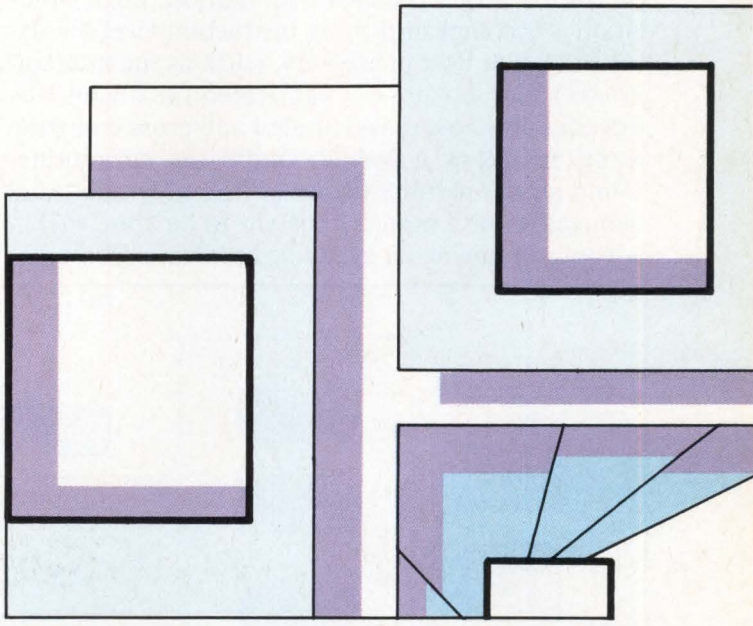




# PORTABLE NATIVE-CODE PACKAGE SUITS 8- TO 32-BIT MICROS

**Transporting native code to newly introduced microprocessors saves development time and redundant software writing.**

**by Thorn Smith**



Programmers usually have to rewrite assemblers and debuggers for each new microprocessor introduction. Rewriting processor-independent (or application) code from one host machine to another can generally be accomplished using high level languages. However, processor-dependent code requires a monumental rewrite. Processor-dependent software (eg, an assembler, a disassembler, or a debugger) can be rewritten from one machine to another, but the recompiled code is still basically targeted for the original machine.

For example, an assembler can be transported to a host machine based on a different processor, but it cannot be retargeted for its new host. The assembler is actually a cross assembler. In such a case, it would be ideal to separate the assembler's target-independent code (eg, the pseudo-op preprocessor and symbol utilities) and write only a simple micro assembler to perform the actual target-dependent assembly. Incorporating this micro assembler and its associated disassembler in the system allows both to be shared by a debugger and compiler. Thus, only a small amount of code has to be written and linked with the processor-independent code to generate a complete software package.

One implementation of this solution uses a portable native-code package and its associated programs, written in the C programming language (Fig 1). With this package, only a few host- and target-dependent subroutines need to be written in order to generate complete native-code software that includes an assembler, disassembler, emulator, debugger, and test code. Only two major sets of routines must be written—host-dependent routines and target processor-dependent routines.

*Thorn Smith is a programmer at Zilog, Inc, 2448 Brenning Dr, San Jose, CA 95111. He specializes in system debugging.*

The native-code package is divided into four modules. Host-dependent subroutines are part of the environment (ENV) module. These subroutines are designed for the machine on which the native code programs run. The ENV module contains the host operating system/kernel and host processor information to compensate for host processor byte swapping. It also has links to simple memory and I/O access routines. Currently, the Zilog native-code package offers ENV modules for several operating systems: VAX/Unix, VAX/VMS, S8000/Zeus, and CP/M. Modules for board-level environments are also available.

*With the native-code package, only two major sets of routines must be written: host-dependent routines and target processor-dependent routines.*

Host-dependent subroutines (see Table 1) must be written in C. These subroutines include run and single-step. They are called by the debugger to execute context switching on the host machine or, if the target processor differs from the host processor, to perform a target processor simulation. Such simulation is accomplished by an instruction-level simulator (ILS). For host processors, (such as the Z800 and Z80,000) that are not yet fabricated on silicon, the opcodes are cross disassembled and cross emulated using an ILS as a pseudo single-step subroutine. Using an ILS permits the cross assembly and cross debugging for a target processor to be done well in advance of having an available hardware prototype. Once the chip sees life, the emulator can quickly change to a context switch-and-trap operation and be put onchip. The user need not relearn the operator interface because the onchip monitor uses the same code, but with a different single-step subroutine.

The second module houses target-dependent subroutines. This micro assembler and disassembler (MAD) module contains subroutines designed for the machine that the native code targets. The MAD module holds target processor information for a procedure such as target processor byte swapping. It also contains target processor information for the processor frame structure, register mnemonics table, frame offsets, as well as MAD subroutines. The native-code package supports Z8, 8080, Z80, Z800, Z8000, and Z80,000 CPU target moculdes. Here, the Z800 will be considered in particular.

Since processors tend to divide into families in which MAD code is generally redundant, programming the MAD module is simplified. The Z80/Z800, Z8000/Z80,000, and Z8 MAD module families differ internally, but must have the same calling arguments. Furthermore, disassemblers must return the same, fixed-opcode string formats. Target-dependent subroutines that must be written as defined in C are as follows: assemble a string into memory, disassemble memory into a string, and get the byte length of an opcode.

A third module, which is transparent to the package, contains a library of subroutines that are used as a runtime library extension. This UTILS module contains routines that manipulate a common symbol table, decode numeric expressions, and resolve radix conventions and string utilities.

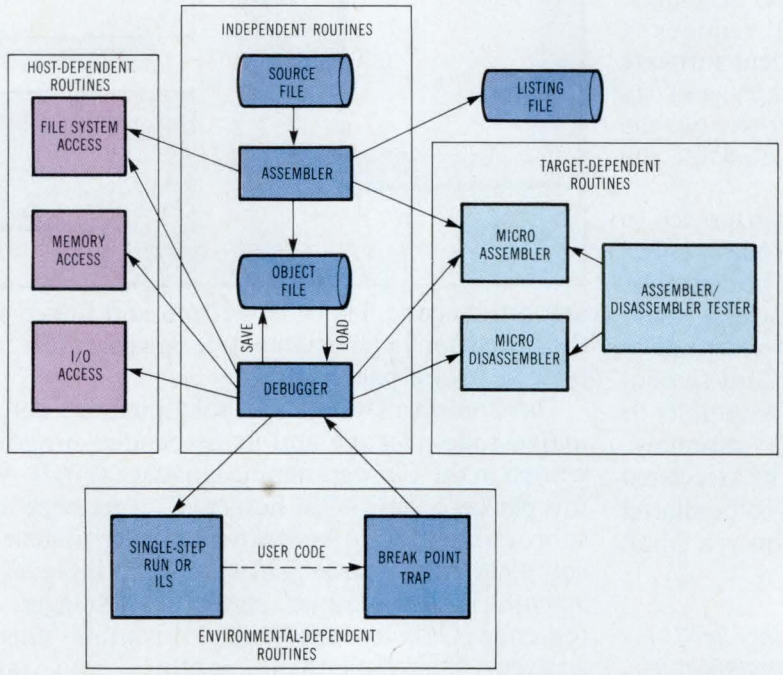



**Fig 1 A portable native-code software package consists of four highly interactive modules. These modules separate host-dependent from host-independent routines, reducing the amount of code that needs to be rewritten for each new microprocessor/microcomputer. The instruction-level simulator (ILS) allows emulation of instructions for chips that are not yet on silicon but whose specifications are available. Thus, both development time and cost are minimized.**

**TABLE 1**

**Host-dependent Subroutines Written by User of Native-Code Package**

```
selseg (address)                        Select a memory segment or high address
byte= ldbyte (address)                  Load a byte from memory
stbyte (address,byte)                   Store a byte into memory
word= ldword (address)                  Load a word from memory
stword (address,word)                   Store a word into memory
byte= pibyte (ioport)                   Read a byte from a port
pobyte (ioport,byte)                    Write a byte to a port
word= piword (ioport)                   Read a word from a port, or special I/O read
poword (ioport,word)                    Write a word to a port, or special I/O read
sbkpt (address)                         Set a breakpoint into code memory
          --------------------
cbkpt (address)                         Clear a breakpoint from code memory


run (frame)     Load processor state and go
sstep (frame)   Load processor state and perform 1 operation
bkpt (frame)    Called by the running/stepping program to reenter debugger
```

In addition to host, target, and utility routines, some system routines (such as open files, read files, and write files, as well as terminal I/O) are also available. If the host system lacks a Unix runtime library, the following Unix routines can be written and linked-in: open a file for read/write, close a file, read a line from a device, format and output to a device, and format and encode to a buffer.

To complete the native-code package, the host and target modules are simply compiled into object modules. These modules are, in turn, linked with a set of other modules containing host- and target-independent code. Finally, three object modules ready for execution are produced: ASM, a cross assembler that generates object code for the debugger from the target source area; DBG, a cross debugger that loads and executes or emulates the object code; and MADTEST, a program that tests the instruction set by comparing the assembler to the disassembler.

Target-dependent MAD subroutines represent the most complicated and important routines for the Z8, Z80/Z800, and Z8000/Z80,000 processor families. These target-independent routines must be coded and have an identical external call-and-return convention in order to interface with the debugger. MAD routines are primarily table driven, consisting of the main, opcode, and operand tables.

The main table holds at least the binary opcodes, an index into the opcode table, and an index into the operand table for the various operand combinations. Indexes are used instead of direct pointers in the main table because they usually number less than the 255 combinations of opcodes and operands, and consequently use less table space as bytes. Opcode length is computed using a formula composed of the opcode and the operand types.

The operand table contains the string of the operand and a back pointer to its start index in the main table. This back pointer is used solely for assembler speed optimization purposes, since the opcode is always determined first. Then, the operand combinations are scanned in the main table starting with the back pointer as an index and ranging to the back pointer of the next opcode. The operand table holds the

**TABLE 2**

**Opcode Entries for Z8 Main Table**

```
000h,   IM+00,   0,       0       ; .word   IM
012h,   R1+10,   R1+14,   0,      ; adc     r,r
013h,   R1+10,   I1+14,   0,      ; adc     r,Ir
014h,   R2+20,   R2+10,   0,      ; adc     R,R
015h,   R2+20    I2+10,   0,      ; adc     R,IR
016h,   R2+10    IM+20,   0,      ; adc     R,IM
017h,   I2+10    IM+20,   0,      ; adc     IR,IM
002h,   R1+10    R1+14,   0,      ; add     r,r
```

string of the operand—if there is one—as well as data on the transformation, type, and binary placement of any numeric field within the operand. Except for the operand string, data is discrete for the MAD module and is encoded differently for each processor. For example, the Z80,000 directs this data to subindex a fourth table which contains operand groups.

### Shortcuts to implementation

Both calls to the assembler and disassembler return an index of the main table opcode record. If the index is a zero, either the binary cannot be disassembled or the assembler cannot assemble the line. Main record zero defaults to a byte or word opcode, depending on whether the target processor is an 8- or 16-bit machine.

The Z8's main table (Table 2) is the simplest among the processors considered here. The binary is clean enough to write a MAD module without even using a table technique. However, a table is more appropriate for adding data columns in order to generate an emulator. The Z8 main table maintains byte 1 as the single byte for the opcode string index, byte 2 as the opcode binary, and the last 3 words for the operand descriptors. The operand descriptors are 16-bit numbers with the highest bits representing a class, and lower bits signifying byte and bit offsets of the binary mask location.

Implementing the Z80/Z800 MAD can be difficult if one is unaware of the shortcuts. First, all Z800 opcodes can be expressed in terms of one of nine prefix sequences plus a single byte (ie, 12 bits). Second, the prefix code determines the binary template and the location of subfields. Finally, the numeric subfields within the binary have only a few simple templates if they are offset after the prefix sequence rather than from the start of the instruction. The Z80/Z800 main table incorporates these premises as shown in Table 3.

The first byte of the Z80/Z800 main table is a special byte used only by the single step Z800 simulator (the ILS), which contains information used for updating the flag bits on a single step for that opcode. The second byte is a code (0-8) that indicates the opcode prefix sequence. The Z80/Z800 microprocessors have nine possible prefix codes placed before the opcode byte that also determine the template and opcode length. These opcode prefix codes, are, in hexadecimal:

0) (null) No prefix code
1) CB
2) DD
3) ED
4) FD
5) DD,CB
6) DD,ED
7) FD,CB
8) FD,ED

Byte 3 of the Z80/Z800 main table is the opcode byte itself. Bytes 4 and 5 are the operand indexes; these indexes reference a record in the operand table. The operand table record then contains a string of the operand, and operand type, and an offset control byte. The operand string contains a string of the operand, including a special tilde character (~) to represent a numeric encode to the disassembler, or to decode a subnumeric field in the operand substring to the assembler parser. The operand record control byte is split into two 4-bit nibbles. The high nibble describes the type of number and, acordingly, the formula to use for encoding or decoding the number from the opcode's binary to the tilde character in the operand string. The operation of the Z80/Z800 micro assembler main table is illustrated in Fig 2.

Z8000/Z80,000 MAD routines are less complicated (while larger) than those of the Z80/Z800, but the opcode templates are clean enough to use operand

**TABLE 3**

**Premises Incorporated in Z80 Main Table**

```
BY+0,     0,     0,  000h,  1,   50,    0,   ; ..5.3...  byte   ~
   0,     0,     0,  08ah,  2,  141,    6,   ; **5*3V0*  adc    a,  (hl)
   0,     0,    DD,  089h,  2,  141,    7,   ; **5*3V0*  adc    a,  (hl+ix)
   0,     0,    DD,  08ah,  2,  141,    8,   ; **5*3V0*  adc    a,  (hl+iy)
   0,  WD+2,    FD,  08bh,  2,  141,   44,   ; **5*3V0*  adc    a,  (hl+~)
   0,     0,    DD,  08bh,  2,  141,   10,   ; **5*3V0*  adc    a,  (ix+iy)
   0,  WD+2,    FD,  089h,  2,  141,   45,   ; **5*3V0*  adc    a,  (ix+~)
   0,  WD+2,    FD,  08ah,  2,  141,   46,   ; **5*3V0*  adc    a,  (iy+~)
   0,  D3+2,    FD,  088h,  2,  141,   47,   ; **5*3V0*  adc    a,  (pc+ )
   0,  WD+2,    DD,  088h,  2,  141,   48,   ; **5*3V0*  adc    a,  (sp+~)
   0,  WD+2,    DD,  08fh,  2,  141,   49,   ; **5*3V0*  adc    a,  (~)
```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grouping. Control codes can be expressed directly without indexing as shown in Table 4. The first byte of this table is the byte length of the Z80,000 instruction. Bytes 2 to 7 serve as the binary opcode template without prefix codes. Bytes 8 to 12 are the operand types and offsets. Unlike the Z800 operand string indexes, the Z8000 has 16-bit numbers that express classes and byte and bit offsets directly. Thus, an operand table can be ignored. There are over 30 operand types for the Z8000 and Z80,000.

The debugger of this portable-code software package is a program that can be linked with any MAD target subroutine module to produce a custom debugger. Only one source of the debugger is needed for its dozen or so environments and targets. The debugger features a unique local single-step instruction, signified as a carot (^). This command allows users to execute any permissible instruction by assembling the opcode into a local space and single-stepping it directly without altering the user's code area. Another feature of this debugger is its symbolic capability.

As a consequence of the symbolic capability, a default hexadecimal radix cannot be supported since

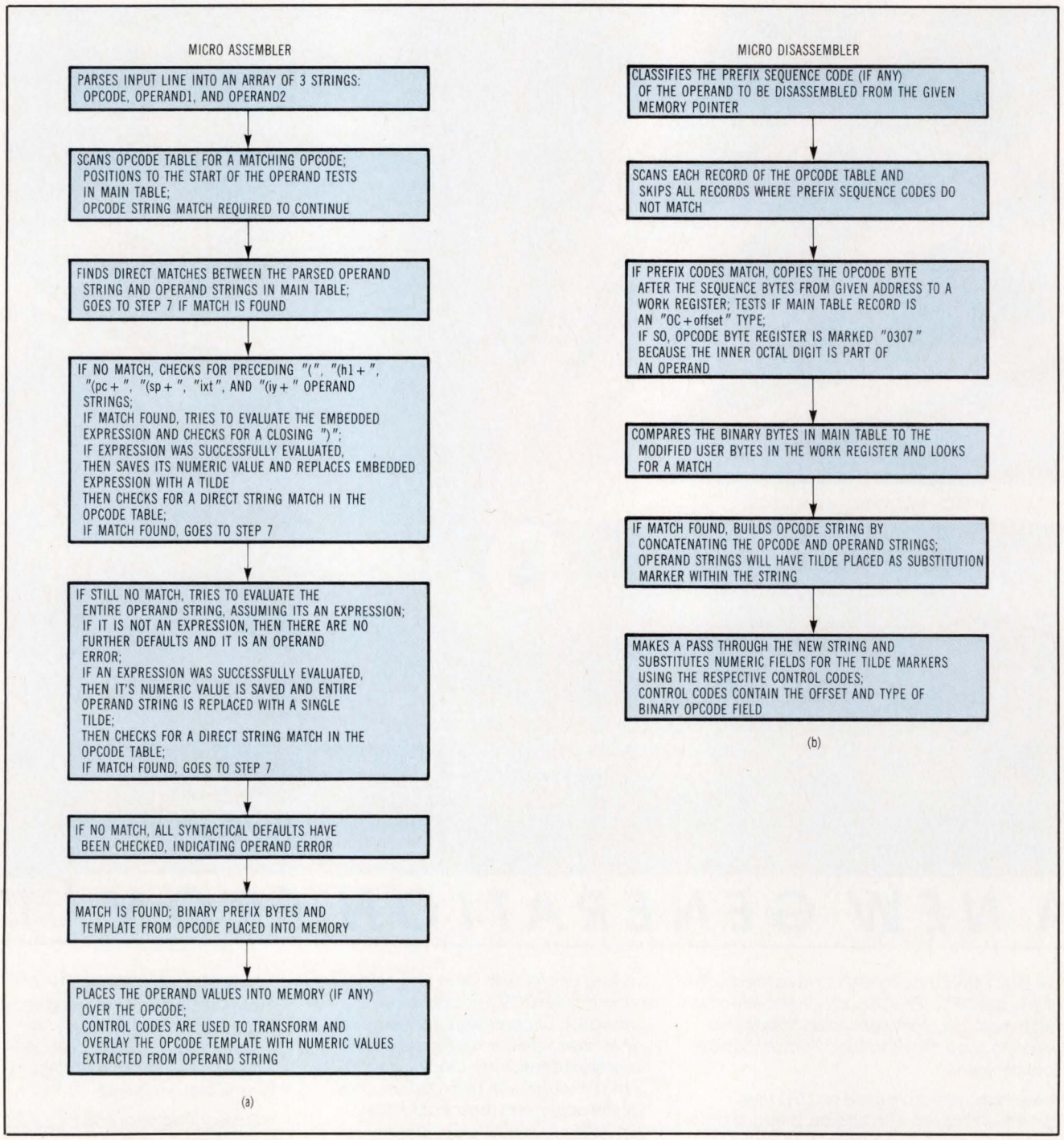


**Fig 2 The Z80/Z800 micro assembler operation occurs in an eight-step sequence (a). Micro disassembler operation begins with prefix sequence code classification (b). Use of prefixes speeds execution.**

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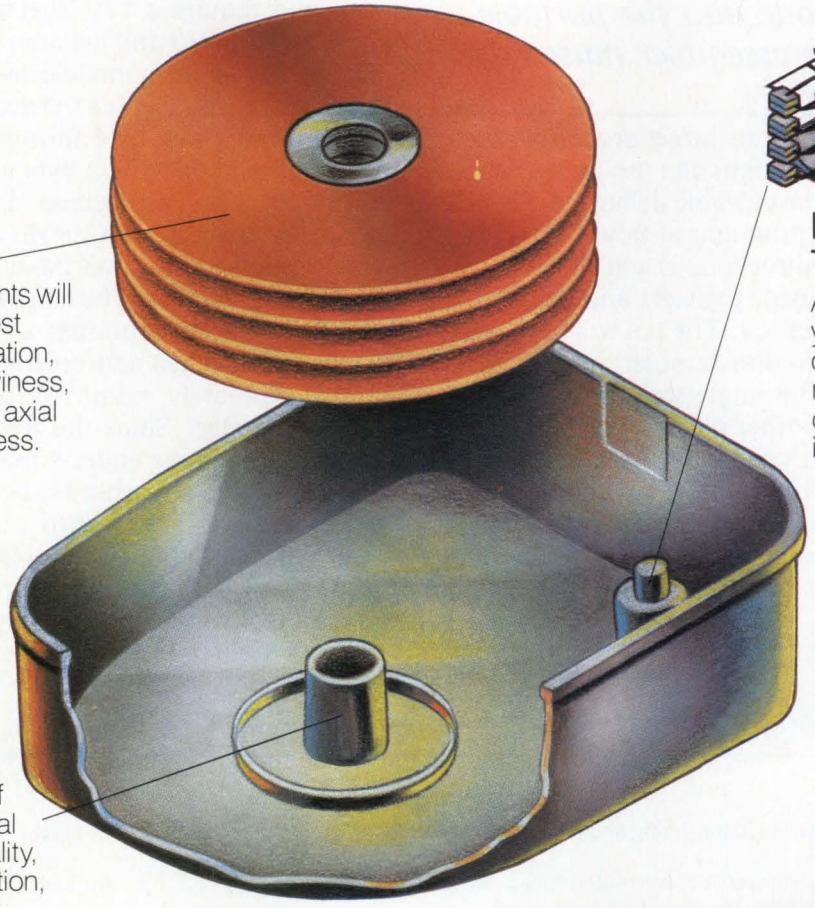

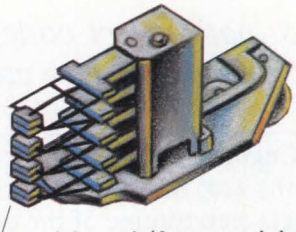

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numbers may conflict with symbols. Therefore, the default radix is decimal, with hex numbers preceded by zeros. The portable debugger command set, regardless of target processor, is shown in Table 5. (Further commands have been added to the set subsequent to the writing of this article.)

To load object code into the portable debugger, a cross assembler must exist. In Zilog's package, a processor-independent portable assembler (ASM) deals with multiple passes and preprocesses a standard set of pseudo-ops. If an instruction is not a pseudo-op or comment, ASM calls the MAD subroutines to do the actual assembly. The portable assembler will produce Intel hexadecimal, Tektronix hexadecimal, or the IEEE microprocessor universal format for object modules (MUFOM).

*To load object code into the portable debugger, a cross assembler must exist.*

Engineers who incorporate target processors such as the Z800 into future designs can use an ILS as the single-step routine of the portable debugger. The ILS facility executes target programs at slower than real-time rates (around 60 instructions/s) and allows access to the simulated processor registers and to the full range of simulated memory. The ILS works in conjunction with the micro disassembler, and is called at one point only as the single-step routine of the portable debugger. In other native-code debuggers for processors now in production, the single-step routine actually does a context switch-and-trap return to execute an instruction. But, users of this ILS are given the illusion that they are actually running under the target processor while debugging object code.

When the ILS is called as a single-step, its only argument is a pointer to the processor state frame containing all of the necessary Z800 registers. The ILS calls the MAD to disassemble and parse the opcode from memory at the given program counter. In the process, the disassembler needs to extract the numeric values and types of the operand fields in order to encode the instruction to a string. This data is also available to the ILS as the necessary information to emulate the opcode. The ILS primarily switches on the opcode index of the disassembled instruction and subswitches on the operand types or values. After the operation is performed, the flags are controlled by the flag control code given in the MAD table.

Certain hardware-intensive components, such as onboard DMA or serial I/O chips, cannot be simulated at the instruction operation level by the ILS and would require a TTL-level simulator for their emulation. The I/O and memory access subroutines are in the environment module and are also simulated as part of the ILS. The ILS I/O accesses to port 1 will read or write a raw byte through the host kernel; port 2 will read or write a byte as two hexadecimal characters; port 3 as decimal characters; and port 4 as octal characters. Certain I/O ports for the memory management unit (MMU) control are intercepted by the address. The handshaking occurs with the memory access routines to simulate the processor's MMU. When address translation is enabled, the ILS ultimately needs to access a 16-Mbyte addressing space. Since the host machine cannot simulate such a large address space, higher physical addresses beyond an arbitrary boundary (usually 16 Kbytes) are overflowed onto a disk file.

This portable native-code package uses a common utility library. These routines process symbols and expressions for the entire package. The expression

**TABLE 4**

**Micro Assembler and Disassembler Routines for Z8000/Z80,000**

```
2,  000h,000h,000h,000h,000h,000h, X2+00,     0,    0,     0,     0, ;.word #W
2,  0b5h,000h,000h,000h,000h,000h, RR+14,RR+10,     0,     0,     0, ;adc r3,r2
2,  0b4h,000h,000h,000h,000h,000h, RB+14,RB+10,     0,     0,     0, ;adcb rh3,rh2
4,  07ah,002h,0b5h,000h,000h,000h, RL+34,RB+30,     0,     0,     0, ;adcl rr6,rh6
2,  081h,000h,000h,000h,000h,000h, RR+14,RR+10,     0,     0,     0, ;add r3,r2
2,  001h,000h,000h,000h,000h,000h, RR+14,II+10,     0,     0,     0, ;add r3,@r2
4,  001h,000h,000h,000h,000h,000h, RR+14,X2+20,     0,     0,     0, ;add r3,#W
4,  041h,000h,000h,000h,000h,000h, RR+14,AA+20,PR+10,     0,     0, ;add r3,W(r2)
4,  041h,000h,000h,000h,000h,000h, RR+14,AA+20,     0,     0,     0, ;add r3,W
```

**TABLE 5**

**Portable Debugger Command Set**

| COMMAND / OPERATORS | SYMBOL | DESCRIPTION |
|---|---|---|
| $ [symbol=] #expr | $ | Symbolic assignment/calculator |
| @ #addr, instruction | | Instruction single patch |
| ^ instruction | | Single step instruction locally |
| a [#addr] | $a | Assemble source code |
| b [#addr] [,#addr] ... | | Set/display breakpoint(s) |
| c [#addr] [,#addr] ... | | Clear (all) breakpoint(s) |
| dX [ #from ] [,#to] \|\| [ ,#count]] | $d | Dump memory |
| fX #from,#to,#data | | Fill memory |
| g [ #addr] | | Jump/Go to user code (execute) |
| i filename | | Inload (overlay) a file |
| l [#from [,#to ] \|\| [,,#count]] | $l | List (disassemble) |
| m #from,#to,#count | | Move memory |
| p #port [,#data] | | Port read [write] data |
| q quit | | Quit |
| sX [ #addr] [,#data] ... | $s | Set memory |
| t [#count] | | Single step w/display |
| u [#count] | | Single step wo/display |
| x [reg #data] [,reg #data] ... | | Set/Display register(s) |
| y [flags] | | Flip flag status bit(s) (szhpnc) |

'#' (numeric) fields can be any symbolic expression.

The command suffix 'X' is blank for byte 'W' for word.

evaluator subroutine, when given a symbol table and a string pointer, will parse and interpret the string as a symbolic expression. Miscellaneous add-symbol and search-for-symbol routines are also present. These subroutines are used in all places where a numeric field can be expressed so that native-code routines are fully symbolic everywhere.

The object code's emit subroutine for the assembler and the load subroutine for the debugger are also grouped together in a module and can be substituted for different object-code formats. Currently, Intel hexadecimal format, modified Intel format, Tektronix hexadecimal format, binary image, and the IEEE's proposed MUFOM object-code formats can be selected.

Easy additions of host and target processor bases are allowed by the portable native-code package. Improvements to the basic assembler and debugger are processed globally across all of the new implementations. When features (eg, a pseudo-op to the assembler or macros to the portable debugger) are added, these changes are carried across all of the package's products automatically. This package can grow both horizontally in terms of processor targets and hosts, and also vertically in terms of enhancements across all products due to the global nature of the package's code.

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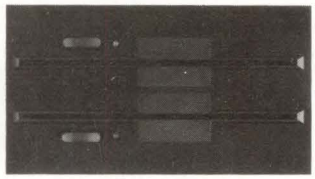

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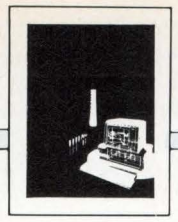




# USING PERSONAL WORKSTATIONS FOR SOFTWARE DEVELOPMENT

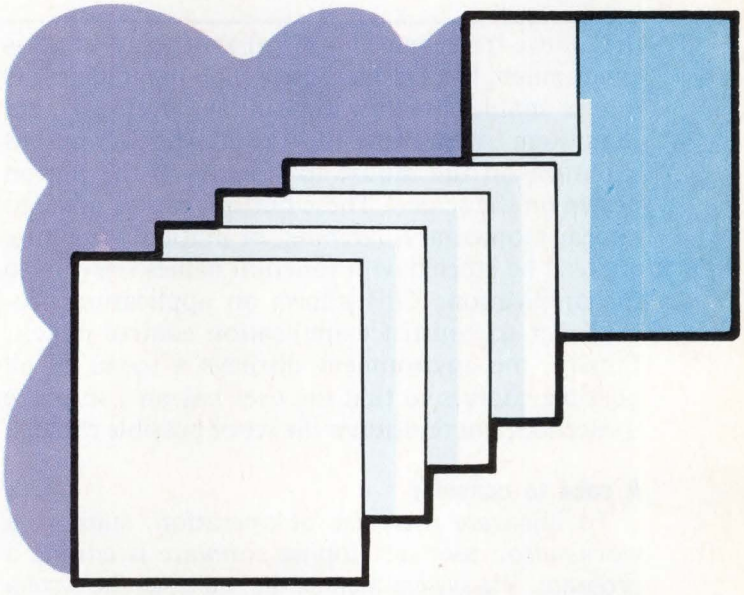
## A 32-bit microprocessor provides the basis for system tools that improve software development productivity.

**by Anthony R. West**

Although engineering talent is growing, the demand for it is growing even faster. This trend pressures the computer industry to focus on building better computer tools in order to improve engineering productivity. And, while the increase in algorithm complexity and the need for sophisticated graphics and user interfaces requires more CPU cycles per user, 32-bit microprocessors (eg, the Motorola 68010) permit this power to be economically packaged in a single-user system.

The SunStation is an example of such a general-purpose, professional workstation—it offers substantial 32-bit CPU power, virtual memory, bit-mapped raster graphics, and the ability to communicate with other systems via local networks (Fig 1). The capabilities of such workstations offer substantial advantages to software engineers.

Professional workstations are powerful networked single-user systems. Software engineers interact with professional workstations via a bit-mapped graphics display screen, on which the system maintains a multiwindow user interface (Fig 2). With this system, users have the ability to create windows (ie, independent virtual terminals) on the screen until the number of interaction streams matches the degree of parallelism required by the problem-solving approach. These windows may overlap on the screen. Users are also given a mouse pointing device, which controls the cursor position on the screen. This mouse can be used to invoke actions on the object at the cursor location. As the cursor is moved on the screen, rapid context switching is handled by demand-paged virtual memory operating systems. This environment has several advantages over traditional tools.



The first advantage is that no saving of interaction state is required. The user can switch from one stream of interaction to another by simply moving

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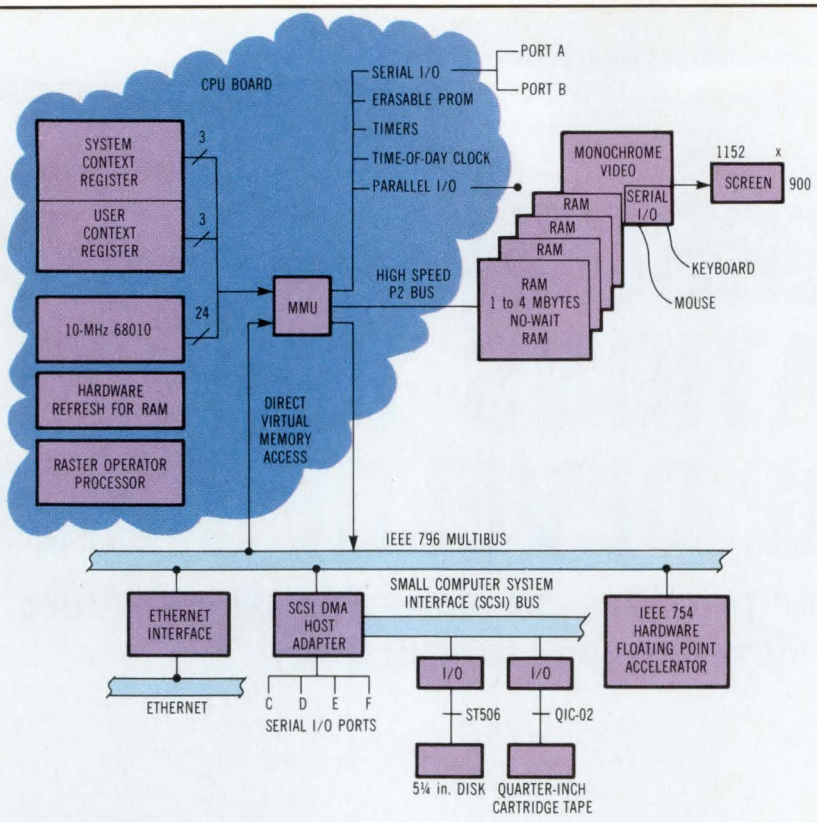



**Fig 1 In the Sun-2 model 120 workstation, virtual addresses emitted by the 10-MHz 68010 are expanded by one of two 3-bit context registers before being mapped into a real address by the proprietary, two-stage memory management unit (MMU). The address can be mapped to onboard devices, to main memory via the high speed P2 bus, or onto the IEEE 796 Multibus via the P1 connector, depending on how the tags in the MMU are set. The monochrome frame buffer appears as 128 Kbytes of contiguous main memory, and the 68010 uses the raster operation processor on the CPU board to perform bit-map transformations in the frame buffer.**

the mouse from one window to another. Also, this environment has familiar interaction paradigms: the mouse enables the user to point at "buttons" that the system can draw on the screen. The user pushes a button on the mouse to "depress" the button drawn on the screen. These buttons can be made to appear momentary, latching, or mutually resetting and can be labeled with function names relevant to the application. This allows an application programmer to construct application control panels. Finally, the environment displays a menu of all possible choices so that the user has only to make a selection, not remember the set of possible choices.

## A case to consider

To illustrate this ease of operation, suppose a workstation user developing software is editing a program. Via system menus, the user asks the system to create multiple windows on the screen. In one window, the source code of the program being developed is edited with a text editor. In another window is the control panel for the compiler, or buttons for invoking the compiler on the program being edited. A third window contains the debugger control panel, and, finally, the fourth window shows the output of the application running under the debugger's control.

After the program is edited in the source editor window, the user tries the results by pushing the SAVE button and moving the mouse/cursor to the compiler control panel. Next, the user pushes the COMPILE button (a latching button that appears to pop out again when the compilation is completed), and then the TEST button on the debugger panel. This enables the user to set breakpoints by pointing with the mouse to source lines in the source window wherever execution stops are desired. The application runs, and, when a breakpoint is encountered, the programmer can point to variable names in the source program, then push the PRINT button in the debugger panel to display the value of those variables.

Notice that in the above scenario the editor, compiler, and debugger are permanently loaded. Thus, the system needs virtual memory to hold all the code. The user need only put the desired tools on the screen once before being able to travel around the development loop, without having to deal with loading programs. User-interface context switching is very efficient. Furthermore, a programmer new to the system can quickly learn how to use it for software development because the control panels are designed specifically to support the normal, default development mode. Sensibly labeled buttons let the user quickly determine how to use the control panel to get the job done. However, more complex, involved options are not precluded.

Multi-user timesharing systems hold a definite place in the computing environment. One of the major advantages of a time-sharing system is that all the users share a common file system. Thus, no special work is required to make sure that one person's code is made accessible to another—it all resides on the same disks. With a personal workstation, however, code is developed in a distributed

fashion and is stored on various storage devices scattered throughout the facility.

In order for the programmers to share their work with others, their workstations have to be able to communicate with other workstations, and with specialized server machines dedicated to providing network resources to the entire community. SunStations, for example, provide the ability to transfer files between workstations through SunServers and larger time-sharing systems, such as Digital Equipment Corp's VAX machines. Also, Sun users can employ the Ethernet to log into remote machines as if they were using a terminal directly attached to those machines.

### Opening the window

The advantage of these networking tools for leveraging the software engineer's productivity really comes out when combined with the window system. Consider Fig 3, where the user is editing the source of a program module in one window. Suddenly, the user remembers that the program is missing the definition of a system data structure.

The code defining the data structure is part of the operating system, written by someone else, and is kept on a file server dedicated to another project. Using the system menus, the user opens another window on the screen, and logs into the file server where the operating system source is stored [Fig 3(a)]. The user types the command to cause the file server to list the source module containing the data structure, and the system code appears in the new window, having been transmitted across the Ethernet [Fig 3(b)]. The user then selects the particular part of the module to be copied into the program, moves the mouse over the source editor window, and pushes the MENU button to bring up the menu in order to paste selected text into the current window [Fig 3(c)]. The user has pushed the PASTE button and the window system has typed the selected code into the program.

Insight into these issues has led Sun engineers to exclusively use SunStations to perform system development rather than via cross-development off larger machines. These engineers have used the company's distributed environment for the past two years (Fig 4). Apart from the advantages listed above, Sun's use of workstations offers a number of additional benefits that are crucial to the strength of the company's software today.

By using the workstations for software development, engineers gradually added features to improve their usability for software development. Examples of this include a graphical performance monitor, which runs concurrently in a window with other system activities (Fig 5). The monitor displays a strip-chart log of a number of crucial system parameters (eg, CPU utilization, free memory, network activity, and page faults). Before the monitor, Sun engineers had no convenient way of making this system information understandable to the average programmer.

Another benefit of using one's own workstation comes from pride of ownership. Since system developers tend to be finicky about the quality of the tools they use, forcing them to use the systems they were developing motivated them to fix the bugs. This, in turn, led Sun implementors to form performance expectations for their software development

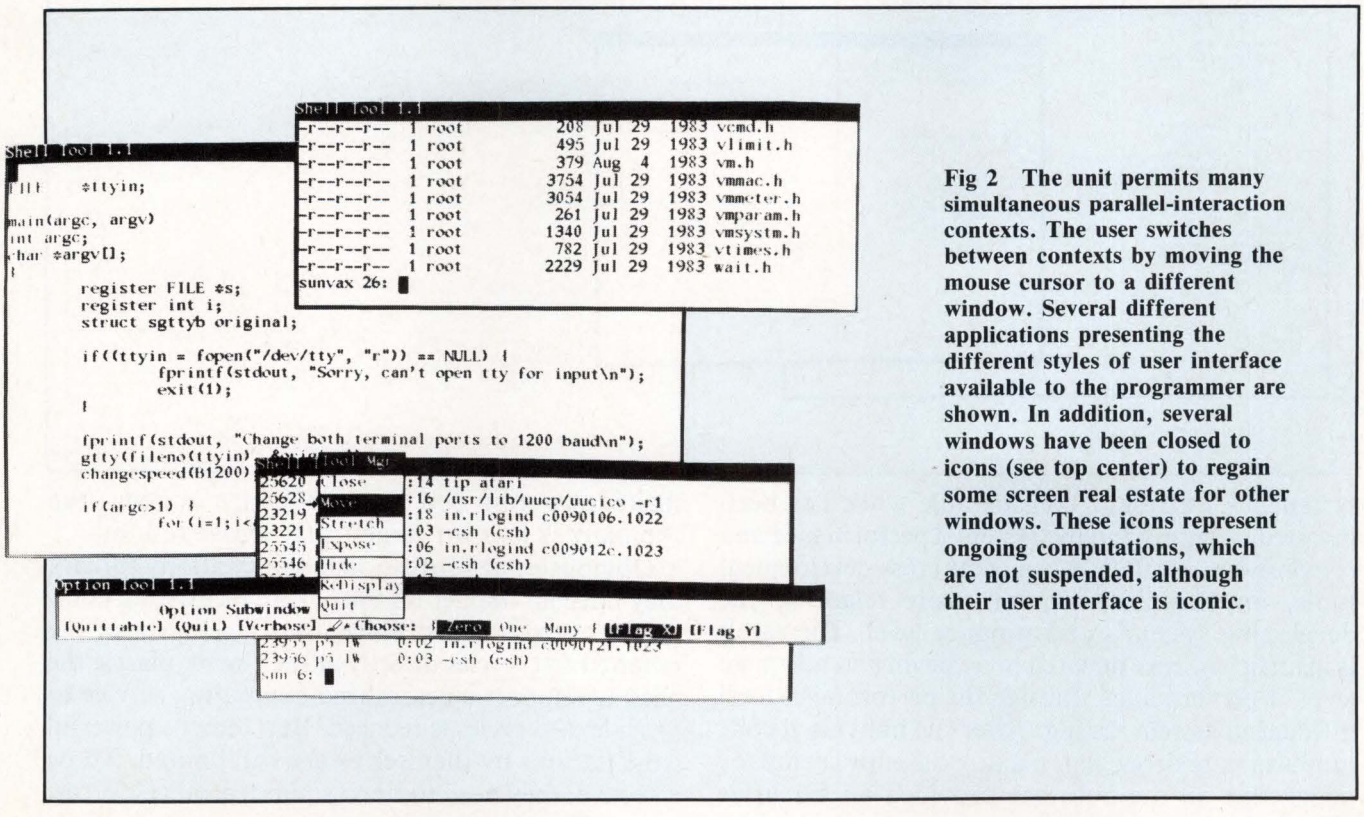



**Fig 2 The unit permits many simultaneous parallel-interaction contexts. The user switches between contexts by moving the mouse cursor to a different window. Several different applications presenting the different styles of user interface available to the programmer are shown. In addition, several windows have been closed to icons (see top center) to regain some screen real estate for other windows. These icons represent ongoing computations, which are not suspended, although their user interface is iconic.**

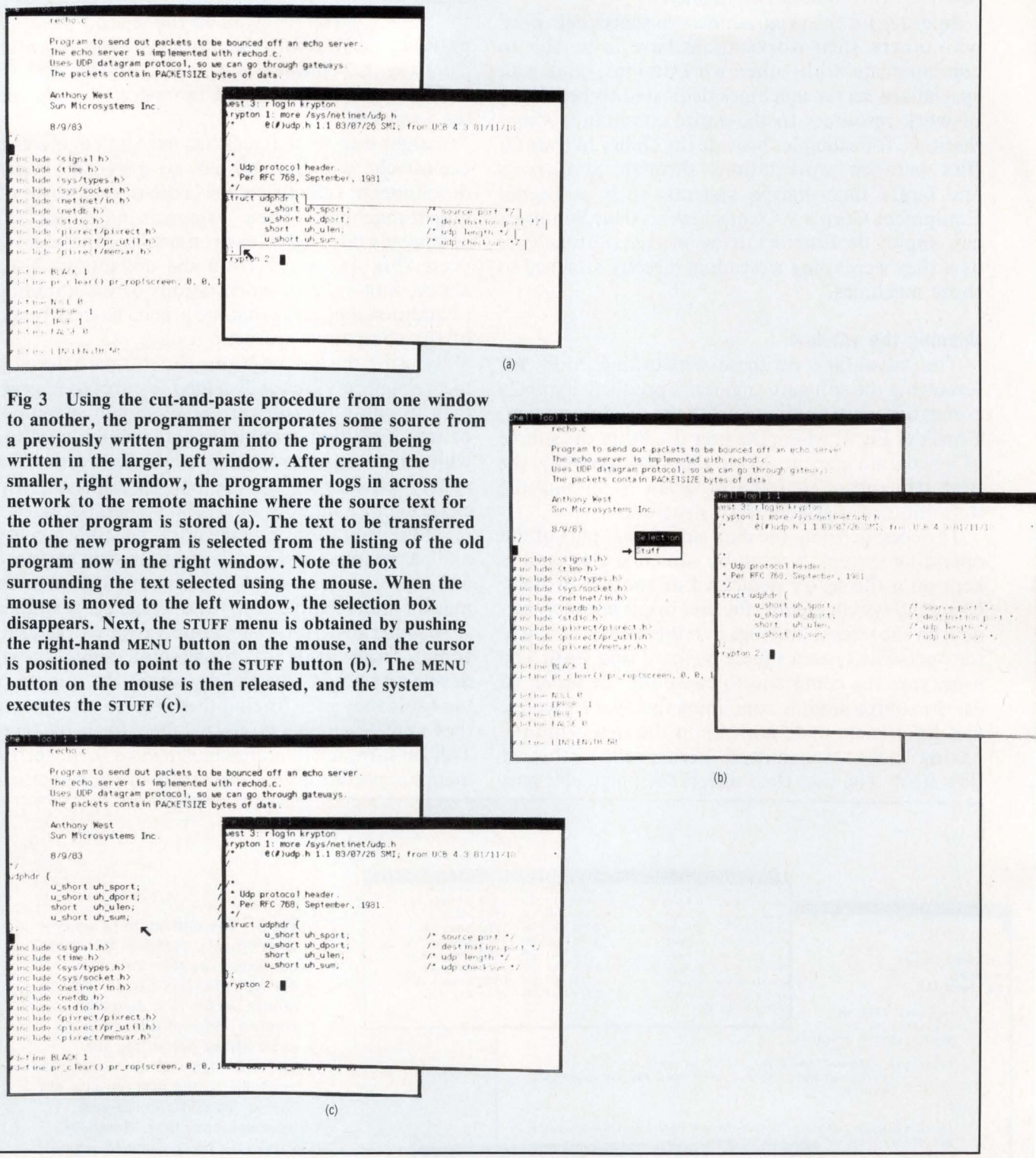



**Fig 3 Using the cut-and-paste procedure from one window to another, the programmer incorporates some source from a previously written program into the program being written in the larger, left window. After creating the smaller, right window, the programmer logs in across the network to the remote machine where the source text for the other program is stored (a). The text to be transferred into the new program is selected from the listing of the old program now in the right window. Note the box surrounding the text selected using the mouse. When the mouse is moved to the left window, the selection box disappears. Next, the STUFF menu is obtained by pushing the right-hand MENU button on the mouse, and the cursor is positioned to point to the STUFF button (b). The MENU button on the mouse is then released, and the system executes the STUFF (c).**

systems. As a result, considerable work has been invested in improving the system's performance and responsiveness. Often, when using cross-development tools, implementors cannot easily relate to the developing system's performance level. The result is insufficient care devoted to achieving an adequate level of performance. Raising the performance level influenced system testing. After the individual code modules were debugged, making the entire company dependent on the outcome provided an extensive shakedown test bed for the entire system—the company is its own largest pre-release test site.

Obviously, as professional workstations spread, they have an impact on the nature of existing computing environments. Since users have most of the required CPU cycles directly at their work places, the need to support a centralized computing service to provide CPU cycles is reduced. But, today's powerful workstations by themselves are still limited. To be effective, they need to tie to some central resources.

Naturally, a transition from time-sharing to workstations does not happen overnight—most large engineering organizations have just started to evaluate workstations as productivity tools. It will take some time for this technology to really take hold of the computing base.

*Workstations are part of distributed information environments and the driving force behind new engineering environments.*

Furthermore, there are applications and users for which time-sharing is the best or most cost-effective solution. This is true for support personnel, whose use of the computer is mostly for text processing and gaining access to other, more conventional productivity tools such as electronic mail. Clearly, this type of user needs access to the same type of network environment as the workstation user, because support personnel (eg, secretaries) work closely with their professional staff, and it is important for them to access the same files, mail, and tools. It is for this reason that SunStations are designed to be capable of configuration as multi-user time-sharing systems with conventional ASCII display terminals. In this way, the support staff can share the engineers' information tools.

The workstation, then, is a component in a distributed information environment, which also contains time-sharing systems, management information systems, and systems optimized for providing specialized services. One of these specialized services is number crunching. Workstations are powerful, but a certain class of computing applications will always require raw CPU power that is best found in large mainframes (eg, simulations, scientific problem solving, and image processing). A requirement to complement the workstation's capabilities with access to large, powerful systems for specific applications tasks will always exist. Such systems can be thought of as processing servers, and are accessed via the local network. Notice that interactive time-sharing is specifically excluded from this class of application—the type of interaction between workstations and processing servers is much more like the older concept of remote job entry and batch computing.

In addition, workstations need access to specialized file servers or central repositories of information. In fact, disk storage capacity is still best bought in large chunks. Large drives are more reliable, offer higher performance, and can be located in secure, environmentally stable rooms. This simplifies administration and archiving, tasks users usually do not want to be concerned with. This work is best made the responsibility of a dedicated, specialist team, who can keep the information in one place up to date, archived, and secure. Such a team can be found in a computer center.

## File server functions

Specialized file servers found in larger systems provide a central point where the information generated by various workers comes together. Finding things is simplified, and simple operating procedures

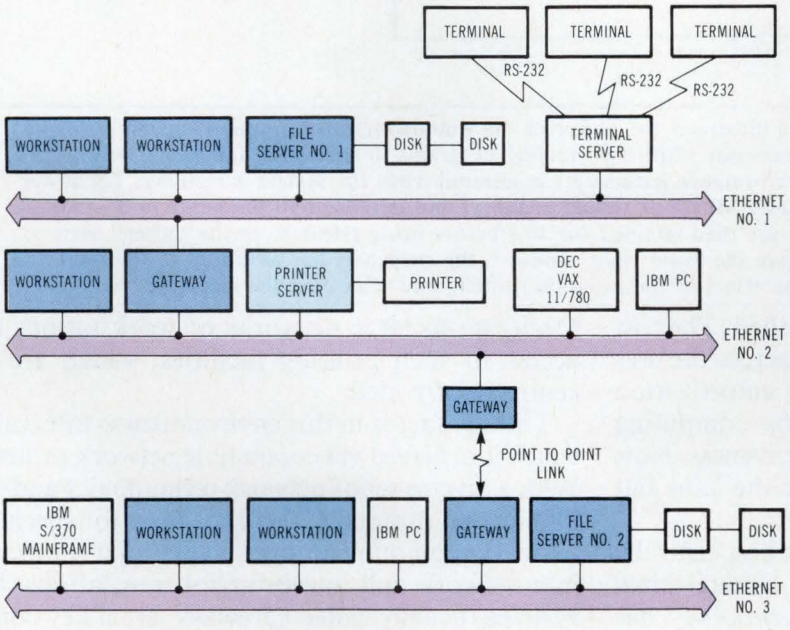



**Fig 4 Workstations are intended to be one component in a distributed information environment. The key to being able to glue the components of an information environment together into an integrated whole is compatible, industry-standard network protocols. Gateways enable one type of transmission technology to be interfaced to another (eg, point-to-point links). Terminal servers enable terminals to be connected to the network, rather than to a specific host. Thus, they can be used with any host in the internetwork.**

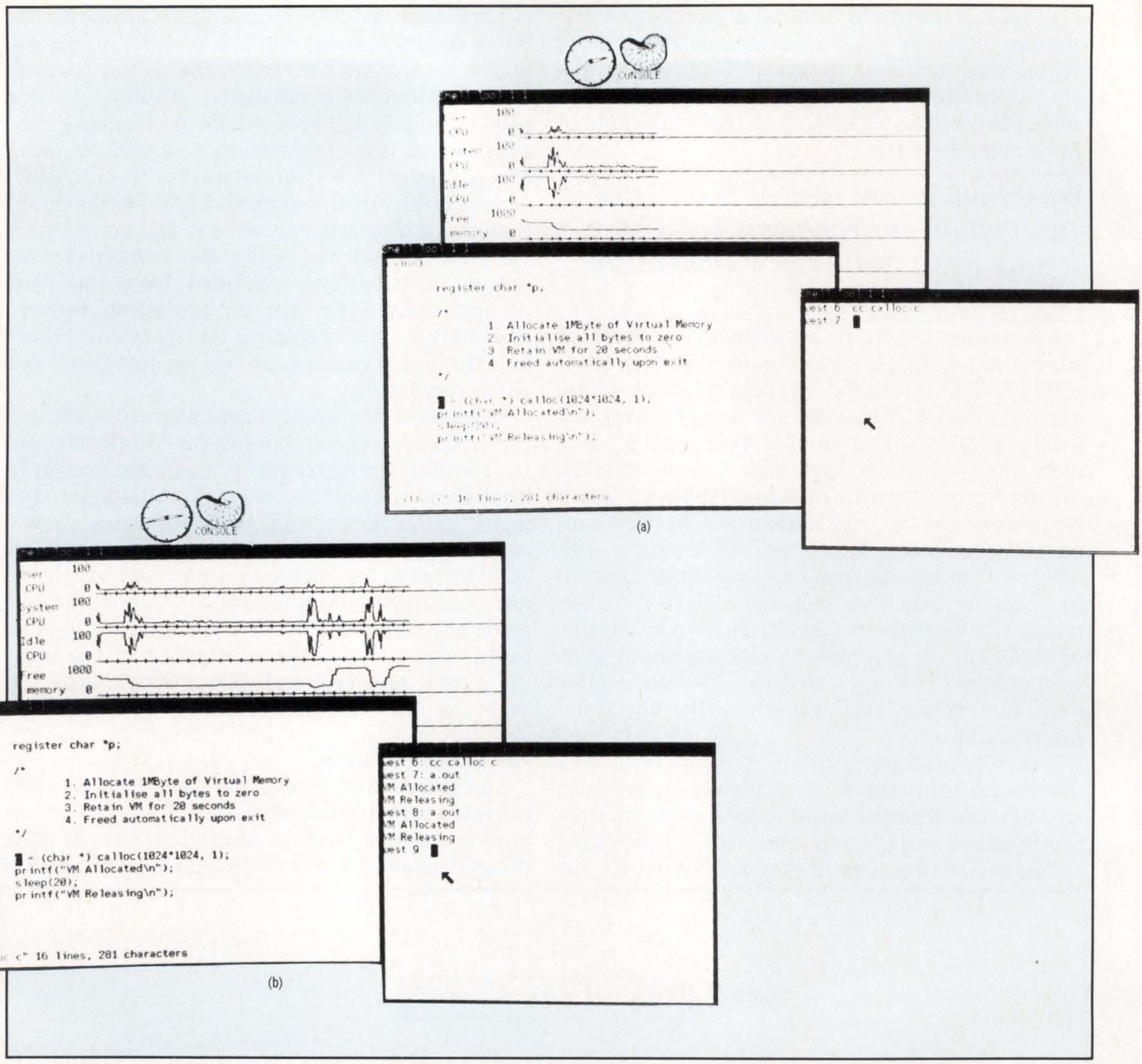



**Fig 5 This before (a) and after (b) example illustrates the power of the window-oriented graphics capability for presenting information about the system's behavior while it is running programs to software engineers. The top window shows a stripchart log of system performance parameters monitored while the system is running. The lower left window shows a program which allocates 1 Mbyte of virtual memory, and initializes all the pages to 0—faulting them into real memory to do so. The pages are then retained for 20 s before being released. In the "after" view, the allocation program has been run twice (see the lower right window), the stripchart has advanced to the right and the free memory line dips twice, showing the effect of the program running and allocating the memory.**

for system development can be established. The cost of these servers can also be amortized across the user community. This is not new—the amortization technique has been used for years by computing centers to analyze their own cost effectiveness. Now however, it is not CPU cycles that are the issue but other services, such as file storage.

Three other types of servers that are best centrally located are printing, communication, and terminal servers. New, nonimpact printing technology has become available. High performance laser printers, for example, enable the printing of graphics information or proof-printing of typeset documents. Moderate to large networks of workstations need access to such printing facilities, which are best centrally provided.

The key factor in this environment is integration, which is achieved via compatible network protocols. With a diverse set of network technologies and communication protocols, there is a need for specialized network communication servers that implement internetwork and interprotocol translations. Such systems, usually called gateways, are a key component in the system environment.

Finally, as the set of services and machines connected to a local network grows, it becomes more

attractive to connect conventional RS-232 terminals to the network, rather than to any specific computer. This way, not only can the amount of point-to-point wiring within establishments be reduced, but the set of services that the terminal can access is greatly expanded. Connection of terminals to a network is the responsibility of a small, specialized communication server that provides terminal users with remote log-in capability and protects them from having to know about network topology, addresses, or protocols. An example of such a machine is an X.25 Packet-Assembler/Disassembler (PAD).

### Strategies for migration

Workstations force a new style of computing into our professional environments. Yet, it is imperative to analyze how an organization can respond to this pressure in a planned, evolutionary way, since the alternative—revolution—disrupts the productivity that it is trying to improve.

A first step in this process could be the installation of a local network, which functions as the data communication vehicle between all components in the computing environment. The cable installation itself is relatively simple, and the connection of the various machines in the network can be gradual. Eventually, network interfaces for all the popular networks and host computers can be incorporated and necessary software can be written.

Sun Microsystems' experience has been to build up its internal network to the point that now its employees have changed their working habits because of the new types of tools available to them. The availability of widespread electronic mail and high quality printers are two main factors causing people to change their working habits—people like to use these tools.

Hence, workstations, although they are but one component of the distributed information environment, can be the driving force for a company to provide a new environment for their engineers. Because the engineers constitute an influential power group within the organization and are usually the first group to receive the workstations, any migration plan will rely heavily on their recommendation to use leading-edge professional standalone workstations.

*Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.*

*High 725* *Average 726* *Low 727*

# EMULEX IMPROVES AND TAPE BACKUP BY

Emulex sets the pace with three great storage subsystems for the full range of DEC QBus and Unibus systems. Whether you need Winchester disk, cartridge disk, ¼" streaming tape, or a combination unit, you'll be a step ahead with Emulex.

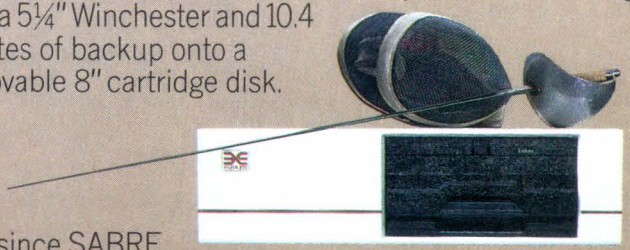
## INTRODUCING VAULT.™

Emulex rises above the competition with the Vault.™ This 70-MByte tape subsystem is built around the CDC Sentinel ¼" cartridge tape streamer and uses Emulex's own TC05 (QBus) or TC15 (Unibus) tape coupler to interface with your system. The Vault is totally software transparent to standard TS11 software. So this compact tape unit looks just like a big ½" TS11 subsystem to your operating system and diagnostics.

Vault comes complete with power supply in a single compact cabinet. It's the perfect backup unit for smaller QBus systems such as the MICRO/PDP-11 and MICRO/VAX.

## PRESENTING SABRE.™

SABRE™ is a sharp solution for LSI users who need more storage and backup. It packs 31.2 MBytes of main storage onto a 5¼" Winchester and 10.4 MBytes of backup onto a removable 8" cartridge disk.



And since SABRE is an exact RL02 emulation, all existing operating and diagnostic software can be used as is.

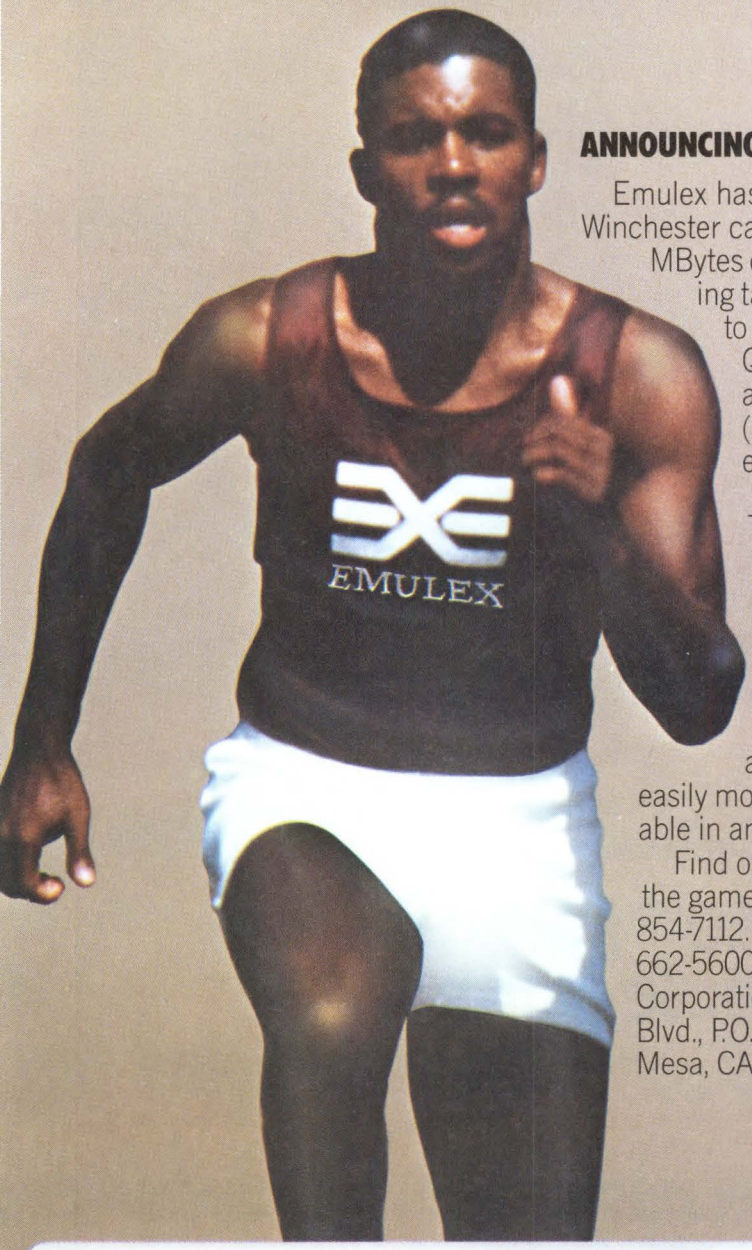
SABRE is 5¼" high and slips into any 19" RETMA enclosure. A desktop version is also available. Both come complete with power supply, host adapter and connecting cables.

SABRE needs only one-eighth the space and one-quarter the power of four RL02s. And it eliminates the need for a separate system bootstrap, bus terminator and clock control board.


*DEC, QBus, Unibus, TS11, MICRO/PDP-11, MICRO/VAX, LSI and RL02 are trademarks of Digital Equipment Corporation. CDC and Sentinel are trademarks of Control Data Corporation.

GSA Contract #: GS00K84015S575

# DEC DISK STORAGE LEAPS AND BOUNDS.




**ANNOUNCING MEDLEY.™**

Emulex has another winning combination with the Medley™ Winchester cartridge tape subsystem. It gives you either 35 or 110 MBytes of formatted storage and up to 70 MBytes of streaming tape backup. The Medley is fully software transparent to the operating system and diagnostic software of QBus and Unibus CPUs. And it uses the powerful and versatile Small Computer System Interface (SCSI) which keeps your options open for peripheral expansion.

Medley is interfaced to the system with a TC05/TC15 tape coupler and a UC02 (QBus) or UC12 (Unibus) host adapter. By using the Mass Storage Control Protocol (MSCP), the UC02 and UC12 allow the operating system to utilize the precise characteristics of the Winchester disk drive without patches or modifications to the operating system.

For convenience, Medley's disk drive, tape drive and power supply all fit into an attractive cabinet that easily mounts in a standard 19" rack. The Medley is also available in an attractive desktop version.

Find out how Emulex subsystems can keep you ahead of the game. Call toll-free (800) 854-7112. In California (714) 662-5600. Or write Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

EMULEX

**The genuine alternative.**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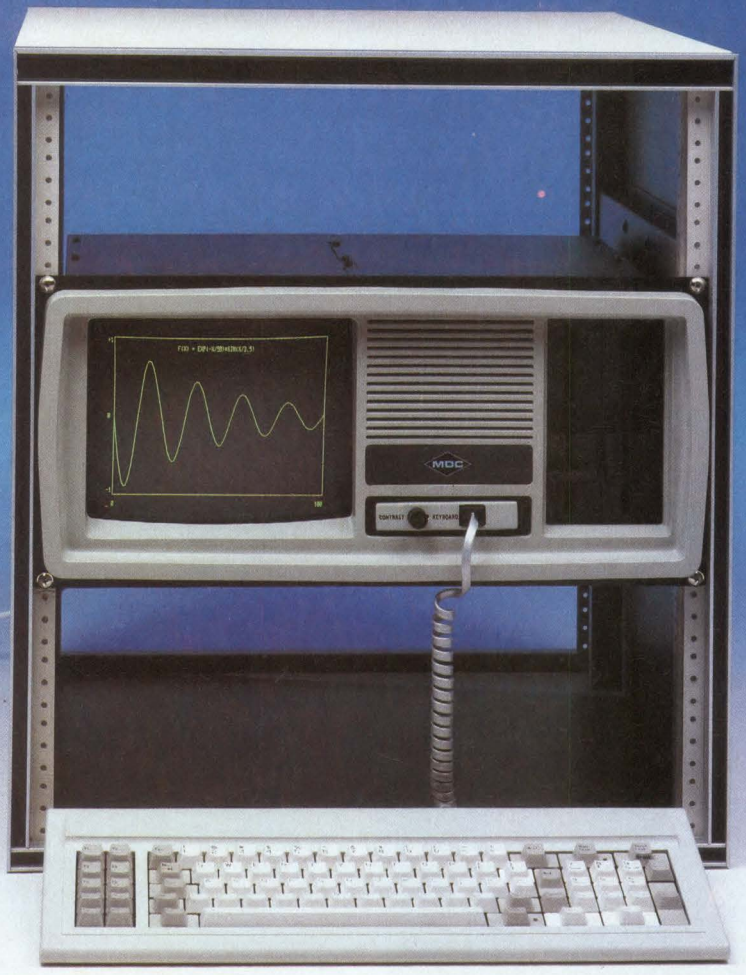
CIRCLE 80

# You won't find this PC in an office.



**Compatibility:**
IBM® PC

**RAM on main board:**
256 KB standard
512 KB optional

**Storage:**
Two 320 KB floppies
Optional 10 MB Winchester
RAM-disk built in

**Ports:**
1 parallel, 1 serial

**Expandability:**
4 available slots
110 W power supply

**Display:**
High-contrast, non-glare
16x13 character font
640x325 graphics built in

**Software:**
MS™-DOS, GW-BASIC™, assembler

## The MDC RM-1600™ Rackmount IBM PC-Compatible Computer

At last, an IBM PC-compatible computer for industrial and scientific use. The RM-1600 makes available thousands of IBM PC-compatible software and add-on hardware products. It also offers the modularity of a rackmount housing.

And the RM-1600 provides four available expansion slots and a high capacity 110 W power supply that let you really mix and match all those add-ons.

For additional storage and speed, an optional 10 MB Winchester replaces a diskette drive. Or for speed enhancement alone, try the built-in RAM disk, using the 512 KB on-board RAM capacity. In numerical applications, you can add an 8087 co-processor for greater speed.

So whether the application is laboratory instrumentation, test and measurement, R&D, numerical control, process control, or OEM systems, the RM-1600 lets you contruct your equipment as you want it.

MDC has been building process control equipment for over 13 years. We first created the RM-1600 for our own use, and now offer our advantage to you. Take the advantage; give us a call and arrange for a closer look.



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CIRCLE 81

# NCC PRODUCT PREVIEW

The National Computer Conference—or NCC as all "in" people refer to it—is traditionally the event chosen by the majority of computer industry companies to introduce or exhibit their latest and most important products. This year is certainly no exception. Several hundred companies will use the Las Vegas exhibit floors to display the finest in micro and minicomputers, data communication equipment, interface devices and boards, memory chips and systems, power supplies, test equipment, and peripherals of all kinds.

As in past years, *Computer Design* editors contacted exhibitors of record, requesting descriptions and information on their "new" products—that is, those that have not been previously exhibited or announced. Publishing deadlines, being what they are, precluded obtaining information on every important new product. Also, many companies prefer to announce their newest products at the conference itself.

However, the following pages contain a thorough coverage of known new products, plus short descriptions of established but important exhibited items. Of course, a key criterion in choosing which to include in this Product Preview was the product's potential interest and value to *Computer Design* readers. If not inclusive, the listings are certainly representative of what attendees should expect to see on the exhibit floor. As for startling breakthroughs in the technology, NCC '84 attendees will be the first to learn of them—simply by being in Las Vegas at the right time.

**Booth numbers that begin with A, B, C, or D will be located in designated areas of the Las Vegas Convention Center. Booth numbers beginning with an H can be found in the Las Vegas Hilton.**

## COMPUTERS

### Low cost workstation handles simultaneous voice/data

The ES.1 voice/data workstation integrates a telephone, a 9-in. CRT data terminal, an internal 300-baud, full-duplex modem, a detachable keyboard, and support software in an affordable desktop package. Simultaneous voice/data communications are completed with two telephone lines, allowing users access to data bases while speaking on the telephone. Its telephone directory operates by single-keystroke dialing. The station can also redial the previous 15 telephone numbers automatically. In addition to generating and sending electronic messages, users can maintain a personal calendar/reminder file. The data terminal displays 25 rows of 80 chars on the CRT. The typewriter-style, full-travel keyboard includes 10 function keys. The control panel has a standard touch-tone telephone keypad, with 13 programmable function keys and 8 dynamic soft keys for menu selections. The standard ES.1 comes with two modular RJ11C telephone plugs and costs less than $1000. **Zaisan, Inc,** 13910 Champion Forest Dr, Houston, TX 77069.

**Booth H546** **Circle 260**

### Five personal computers are IBM compatible

The Z-100 PC systems are software and expansion-board compatible with the IBM PC. Series features three desktop and two portable systems, an IBM expansion bus, and a detachable keyboard. Desktops are available in three 5¼-in. floppy disk drive configurations: single drive ($2699), dual drive ($3099), and dual drive with floppy and 10.6-Mbyte Winchester hard disk drive ($4799). Portable systems have 9-in. amber monitors and are available in single-floppy disk drive ($2799) and dual-floppy disk drive ($3199). Basic design features include an Intel 8088 processor, a BIOS system in ROM, and an MS-DOS operating system. Standard features include 128-Kbyte RAM, which expands to 640 Kbytes, two RS-232-C serial ports, one Centronics compatible parallel port, RGB color output, built-in menu-driven diagnostic software, three scrolling modes, and high speed text and graphics display. Units are available immediately. **Zenith Data Systems,** 1000 Milwaukee Ave, Glenview, IL 60025.

**Booth A2042** **Circle 261**

# COMPUTERS

## Portable computer features dual-processor expandability

User-friendly EXECUPORT XL series portable computers feature an 8-bit Z80 processor, or a 16-bit, 80186 processor. CP/M, MS-DOS, and CP/M-86 operating systems are supported. A 22-key keyboard provides 44 user-defined functions with all keys programmable from the operating system. The Z80 processor-based EXECUPORT XL has an 80-Kbyte memory, a 9- x 5-in. phosphor screen, and a 5¼-in. dual double-sided, double-density floppy disk drive. The EXECUPORT XL+ (80186-based) adds a 16-bit coprocessor and 128-Kbyte memory. Options include 300/1200-baud 212A-type intelligent modem, telephone handset, 200-char/s printer, and hard disk. The self-contained EXECUPORT XL is priced at $2695; the XL+ is $3495. **Computer Transceiver Systems, Inc,** E 66 Midland Ave, Paramus, NJ 07653.

**Booth C3594** **Circle 262**

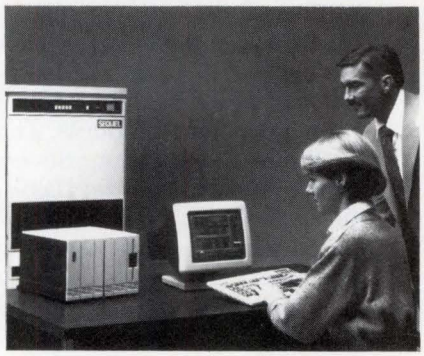
## Workstation incorporates half-height hard disk option and modem

A half-height hard disk option for the 16-bit Mad-1 computer provides 10 Mbytes of formatted data storage in its Winchester drive. This 1.63 in. high, 5¼-in. drive stores up to 12.7 Mbytes of unformatted data. The hard disk replaces one of the 360-Kbyte floppy disks that are standard with Mad-1. Users can choose between a two floppy, 128-Kbyte RAM system, and a system with one floppy and one hard disk. In addition, Winchester drive RAM increases to 256 Kbytes. The Mad-1 desktop computer uses an 80186 microprocessor for twice the processing speed of the IBM PC. A typical Mad-1 workstation costs $6295 and is IBM PC compatible. Also available for Mad-1 is a Bell 103/212A-type 300/1200-bit/s modem. The modem option gives the computer synchronous or asynchronous Bell-compatible data communication capability. Speed selection is automatic, and an FCC registered telephone line interface is included. Under software control, the modem can perform a number of functions automatically. These functions include calling or being called by another computer, transferring data, and performing error checking. The modem, which is installed on the Mad-1 video board, does not use an expansion slot. Mad-1's modem option is under $500. **Mad Computer, Inc,** 3350 Scott Blvd, Bldg 13, Santa Clara, CA 95051.

**Booth C4474** **Circle 263**

## Intelligent workstation runs 10 simultaneous tasks

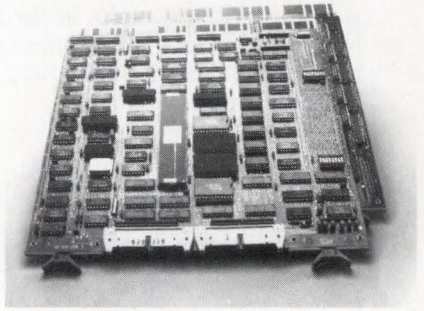
The modularly designed Microdata 1000 intelligent workstation combines a full range of automation features, taps into data bases, and has a system manager that lets it perform 10 different applications simultaneously. The workstation uses MicroReality, a new version of Microdata's Reality operating system with built-in relational data base. Users can search for and retrieve virtually any information without complicated commands or specialized programs. When linked to a central computer, the workstation automatically retrieves data needed to answer queries. Microdata 1000 retains up to 1 million chars of information in its own memory, and can file up to 80 million chars on hard disk. Available software includes word processing, electronic spreadsheet and calculations, electronic mail, business graphics, project management, and task scheduling. Embedded in the operating system is a Context Manager that divides the workstation's memory into 10 separate computer systems. Each partition can load and run a program,



and maintain separate data in the computer's memory. Users need not turn off one application and close out its files before running another application. The basic Microdata 1000 package includes 12-in. monochrome display, separate keyboard, and expandable CPU housing. Expansion options include floppy disk drives, Winchesters, streaming tape systems, and a color controller for use with a 15-in. color display system. The workstation connects to a variety of printers and plotters. Single-station Microdata 1000 systems start at $8075. **Microdata Corp,** 17481 Red Hill Ave, Irvine, CA 92714.

**Booth C3566** **Circle 264**

## System increases Q-bus storage capacity



The system 58 line of Q-bus minicomputers features a 40-Mbyte Winchester. Standards include 5¼-in. Winchester, 1 Mbyte 8-in. floppy, DEC LSI-11 processor, 256- to 4096-Kbyte memory, 22-bit Q-bus backplane, and integrated DEC or Unix operating system. Systems are packaged in desktop or rackmountable enclosures. **Cambridge Digital Systems,** PO Box 568, 65 Bent St, Cambridge, MA 02139.

**Booth C4214** **Circle 265**

# COMPUTERS

## Briefcase-sized computer has multiple windows

The IS-II briefcase-sized computer, Consultant, is designed as a portable desktop unit. It has multiwindowing capability and integrated software. Six function keys provide data handling, calculation, word processing, communications, and help. The computer supports custom software and ROMs. Weighing 4 lb, 6 oz, and measuring $11\frac{13}{16}$ x $8\frac{7}{16}$ x $1\frac{7}{16}$ in., IS-II has an 8 x 40, bit-mapped LCD with angle adjustment, 32-Kbyte, nonvolatile RAM, 64-Kbyte ROM, and 128-Kbyte tape storage. CMOS technology permits operation on internal, rechargeable, NiCad batteries that provide up to 8 hrs/charge. Future options include thermal printer, numeric keypad with 16 additional function keys, and 3½ in. floppy disk drive. IS-II is available immediately and costs $995; IS-IIB with built-in modem will be available in September for $1095. **Sord Computer of America, Inc,** 645 Fifth Ave, New York, NY 10022.

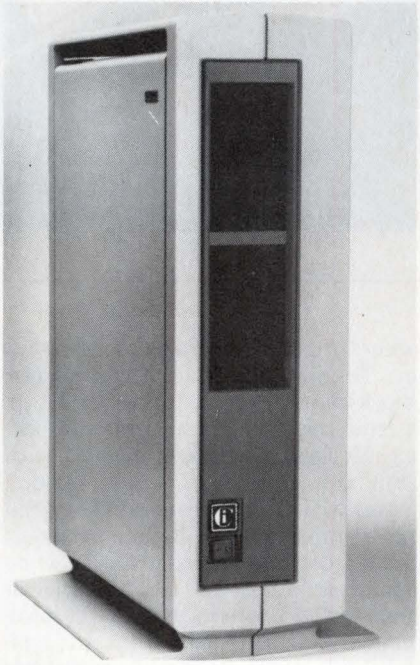
**Booth C4356** **Circle 266**

## Family of 32-bit systems optimized for multi-users

The 6000 series family of 32-bit systems uses a Motorola 68010 microprocessor and is optimized for multi-user, multitasking environments. The series employs an open architecture, designed in accordance with industry standards. The systems run under a Unix-derived operating system, based on and compatible with Unix System V from AT&T Bell Labs. Communication software includes 2780/3780 bisynch (BSC) and 3770 SNA remote job entry, 3270 BSC and SNA interactive communication. The 6300 system has processor boards, disk drives, and a power supply in a 23 x 22½ x 10 in. enclosure. It features a 2-Mbyte main memory, removable media storage, and fixed mass storage of up to 37 Mbytes. The 6600 features a realtime, message-based, operating system with distributed implementation in system processing. Each 6600 measures 29 x 28 x 16 in. **Four-Phase Systems,** 10500 N DeAnza Blvd, Cupertino, CA 95014.

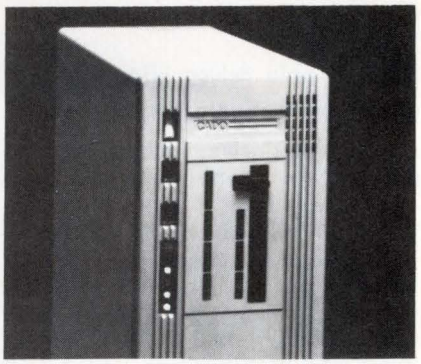
**Booth B3238** **Circle 267**

## Micro offers DEC compatibility and upward expansion



Based on the DEC Micro/PDP-11, the CI-Micro-11, is a 40-Mbyte computer system that provides upward expandability and a variety of configurations. Available CPUs are LSI-11/23+ or LSI-11/73. Compatible Winchesters have 10- to 40-Mbyte capacity. Emulation on the Winchester is RL02, RL01, and RD51. Each system comes with dual-floppy backup. Floppies are available in RX50 (800 Kbytes) or RX02 (2 Mbytes). The Micro-11 operates under existing, unmodified system software and diagnostics. The emulations permit software-transparent operation under RSTS-E, RSX11M, RSX11M+, RT-11, and Unix operating systems. Each Micro-11 comes with floormount or rackmount hardware. A standard configuration comes with LSI-11/23+ CPU, 256 Kbytes, a 4 x 8 blackplane, and 800-Kbyte dual floppy. All are enclosed in a rackmountable chassis for a cost of $6850, single quantity. **Chrislin Industries, Inc,** 31352 Via Colinas 101, Westlake Village, CA 91362.

**Booth D3530** **Circle 268**



## Low cost computer system supports 16 terminals

The TIGER ATS 16 modular, low cost computer system supports up to 16 terminals, printers, peripherals, or communication devices. The 2 cubic ft system is built around an Intel 80186 microprocessor, together with 512-Kbyte RAM, 10-Mbyte micro Winchester storage, 1.2 Mbyte diskette storage, and a serial I/O card with RS-423-C connectors for four devices. Basic system price is $12,895. **CADO Systems Corp,** 2055 W 190th St, PO Box 3759, Torrance, CA 90510.

**Booth C3856** **Circle 269**

## Microcomputer system based on 16032 CPU

The IEEE 696 compatible multi-user system 816/G is built around National Semiconductor's 6-MHz NS16032 CPU, with an NS16202 ICU and an NS16082 MMU. It also features 512 Kbytes of 16-bit static memory (expandable to 16 Mbytes), 12 serial ports, a Centronics printer port, and a parallel port. The system provides 1.2 Mbytes of floppy disk storage and 40 Mbytes of hard disk storage. Software includes Unix version 4.2, as well as C and Fortran programming languages. Volume shipments of the system 816/G are scheduled for late 1984. List price is $19,995. **CompuPro, a Godbout Co,** 3506 Breakwater Ct, Hayward, CA 94545.

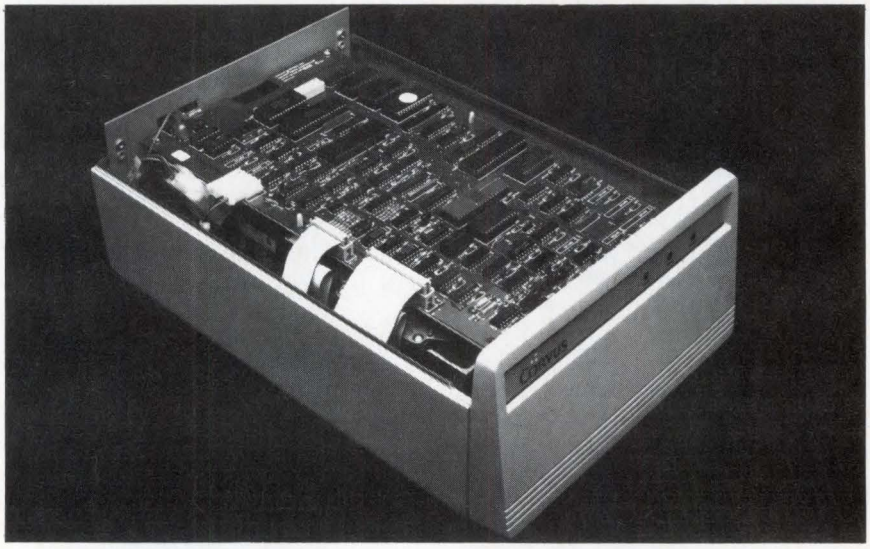

**Booth A2166** **Circle 270**

# MEMORY SYSTEMS

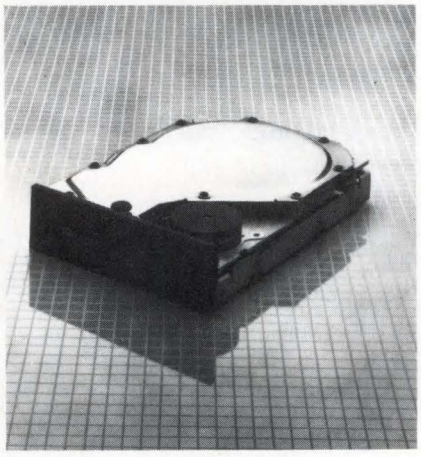
## Network-only drives eliminate disk server for increased throughput

Low cost disk drives with built-in local area network interface eliminate dedicated disk server in network applications. The OmniDrive 5¼-in. Winchester mass storage systems increase capacity, while cutting up to $1000 in costs. Drives are compatible with Apple II, Corvus Concept, DEC RAINBOW 100, and IBM PC and XT computers. Only 5 x 10 x 14.25 in., transfer rate is 687.5 Kbytes/s. Available in 5.5-, 11.1-, 16.6-, and 45.1-Mbyte formatted storage capacities, suggested retail prices are $1995, $2495, $3195, and $4995, respectively. **Corvus Systems, Inc,** 2100 Corvus Dr, San Jose, CA 95124.

**Booth D3010** **Circle 271**



## Low cost half-height Winchesters store 26 Mbytes



As part of the CM3000 series, the 3426, 5¼-in. Winchester contains a proprietary hybrid circuit to minimize parts count and conserve board real estate. The drive uses two disks and four heads, and features a 690-track/in. density. By employing a simplified crystal controlled spindle drive and an embedded track zero concept, the required electronics occupy only one PC board instead of the two needed in other drives. The drive has a time-tested swing arm actuator design powered by a stepping motor with closed-loop stepper control. This—together with an onboard microprocessor and high output, high resolution manganese-zinc heads—results in reliable recording densities. The average access time is 85 ms with track to track access at 18 ms. Average latency is 8.3 ms. The mechanism is protected against shock and vibration while in transit by a dedicated head parking zone and locking. Mechanically interchangeable with standard half-height 5¼-in. floppy drives, the drive will operate from the same power supply. Maximum current drain from the 5-V logic supply while operating is 1 A, and 0.9 A is typical; from the 12-V motor supply, 3 A is maximum during startup, and 1.3 A is typical, 1.6 A is maximum while operating. Packed in the industry standard half-height case, the drive measures 1.625 x 5.75 x 8.0 in. (41.3 x 146 x 203 mm) and weighs 3 lb. **Computer Memories Inc,** 9216 Eton Ave, Chatsworth, CA 91311.

**Booth A1614** **Circle 272**

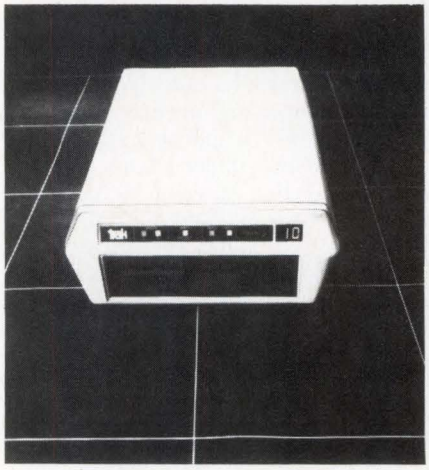
## Intelligent floppy disk drives cover all areas

Two floppy disk drives have been added to Atari computer systems' intelligent disk drive series. The double-sided, double-density AT-D4 drive has a 352-Kbyte storage capacity in addition to a built-in parallel printer port and 2-K print buffer, read/write and single/double density indicators, and a digital track counter. The AT-D4 companion unit, the AT-S2 extended auxiliary drive, has a 700-Kbyte storage capacity, a double-density drive, a printer interface and 2-K print buffer, and a RAM disk. Drive operation is monitored through a LED display. **Trak Microcomputer Corp,** 1511 Ogden Ave, Downers Grove, IL 60515.

## High performance DEC compatible systems offered

The MSV11-Q 1-Mbyte memory module is contained on a single, quad-height board. It is plug-compatible with the DEC LSI-11 Q-bus and is fully supported by DEC operating systems. They can be configured with up to 4 Mbytes of main memory. MSV11-Q is priced at $3950. Also shown will be DHV11 asynch DMA multiplexer with 64 line expansion capabilities, the BA 800/L large system chassis, and the STV11 streaming tape controller. **General Robotics Corp,** 57 N Main St, Hartford, WI 53027.

**Booth C3942** **Circle 273**



**Booth A2063** **Circle 274**

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CIRCLE 82

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# MEMORY SYSTEMS

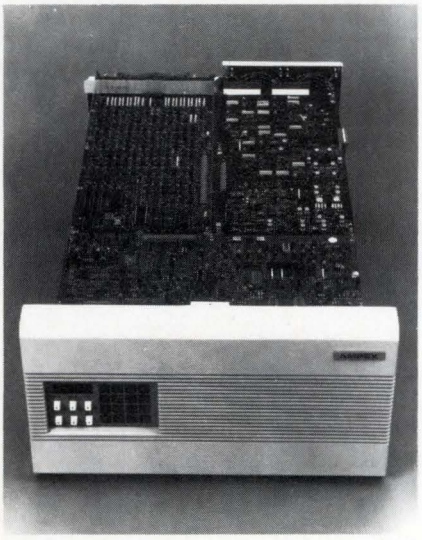
## Tape cleaner/evaluator uses microprocessor for control

Series 3000 permits preprogrammed error limits, tape lengths, leader lengths, and stripping lengths for simple, one-button maintenance. All tape reels have IBM-type, quill release, self-seating hubs. Tape speed is 200 in./s in forward/clean/test mode, 450 in./s in reverse/rewind mode; total cycle time for a 2400-ft reel is less than 3.5 min. The series 3000 measures 18 x 33⅜ x 19 in. and weighs 140 lb. Power requirements are 115 Vac at 60 Hz; 230 Vac at 50 Hz; and 475 W. **Computer-Link Corp,** 40 Ray Ave, Burlington, MA 01803.

**Booth A1232** **Circle 275**

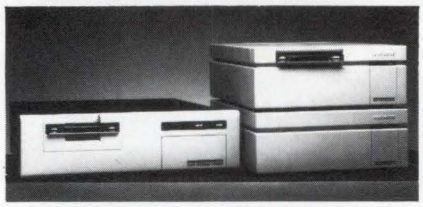
## Winchester disk drive family offers 825-Mbyte storage

The 14-in. rackmountable Centaurus offers 330, 660, or 825 Mbytes of unformatted capacity, with an average access time of less than 25 ms. A linear voice-coil actuator in a closed-loop dedicated servo system is used. Features include a direct-drive dc spindle motor, built-in tester, universal ac power supply, automatic spindle/carriage locks, and SMD interface with dual-port capabilities. Conventional ferrite heads and oxide media support densities of 960 tracks/in. and 12.5 kbits/in. Centaurus model 825 is $8250. Deliveries begin in September 1984. **Ampex Corp,** 401 Broadway, Redwood City, CA 94063.



**Booth A1034** **Circle 276**

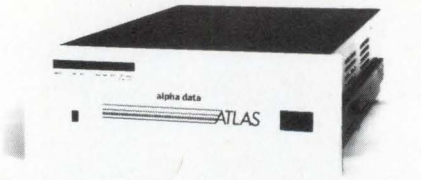
## High capacity Winchesters range from 40 to 140 Mbytes



High capacity 5¼-in. Winchester and quarter-inch tape subsystems are available for DEC PDP-11/23, 11/73, and MICRO/PDP-11. MicroVAX systems are available in rackmount or tabletop form. The 5¼-in. Winchester provides fast access time, while the quarter-inch tape offers up to 20-Mbyte cost-effective backup. Available in a variety of configurations, prices start at $5695 for a 40-Mbyte module. **Data Systems Design,** 2241 Lundy Ave, San Jose, CA 95131.

**Booth H518** **Circle 277**

## Winchester disk drive combines moving heads and fast access




Winchester-style, 128-Mbyte ATLAS disk drive has distinct advantages over other Winchesters. Based on combined disk head seek and settle times, the disk has an 8-ms average access time, and an average latency time of 18 ms. Its 1-Mbyte cylinder size increases data throughput, processing 50 to 60 access commands in 72 ms. An integral spindle/brushless dc motor offers high efficiency and 3600 rpm at 50 and 60 Hz. Mounted on a head lifter, the retractable heads never touch disk surfaces. Disks are in a sealed chamber, and use an ANSI/SMD interface. Rackmounted, the ATLAS is 19 x 7 in. The next-generation ATLAS disk drive with 100-Mbyte storage capacity in 7 in. form will be announced at NCC. **Alpha Data Inc,** 20750 Marilla St, Chatsworth, CA 91311.

**Booth A1146** **Circle 278**

## Magnetic tape subsystems use intelligent controller for SCSI bus

Three subsystem models—TD1012, 1050, and 1750—provide 800 to 1600 bits/in. on half-inch, nine-track tape. Features include full hardware and software compatibility with any host unit or other peripheral supporting the SCSI standard bus. They can control up to four, ½-in. tape transports with support for standard and optional tape commands. Over 40 Mbytes of data can be stored on a single 2400-ft reel of 1.5-mil tape and all subsystems use 7-, 8½-, and 10½-in. standard reel size. Variable data block sizes are programmable in both read/write modes up to a maximum 32-Kbyte buffer size. A software tape-to-tape copy feature is also available. The 1012 model supports 9 tracks, 1600 bits/in. in the start/stop mode. Operating at 12.5 in./s, data transfer rate is 20 kbytes/s. In streaming mode at 100 in./s, it transfers at 160 kbytes/s. The 1050 version supports 7- or 9-track 800 bits/in. (NRZI) and 1600 bits/in. (PE) in start/stop mode. At 45 in./s, data transfer rate is 72 kbytes/s. The 1750 model supports 9-track dual density 800 bits/in. (NRZI) and 1600 bits/in. (PE) in start/stop mode. Operating at 75 in./s, data transfer rate is 120 kbytes/s. In 100s, prices range from $4550 to $5950 each. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.

**Booth B3838** **Circle 279**

## Removable/hard disk subsystem designed for Intel products

The VRC model 8520 8-in. fixed-removable hard disk drive is designed for Intel System 310. It operates under iRMX 86 or Xenix software. The subsystem stores 10 Mbytes on a removable cartridge and 10 Mbytes on a fixed disk. It mounts in a CPU card cage, and operates over a 0 to 50 °C temperature range. **Vermont Research Corp,** Precision Park, North Springfield, VT 05150.

**Booth D3326** **Circle 280**


# WE'VE BEEN DELIVERING 3½" WINCHESTER DISK DRIVES FOR OVER A YEAR.

Rodime has been setting a new standard in Winchester disk drive storage for more than a year. Its 3½" drive with 5 and 10 megabytes of formatted storage has become the industry leader for sub 4" Winchester disk drives. Rodime has now delivered tens of thousands!

### The proven compact drive and proven quantity supplier

With thousands of its 3½" Winchester drives in operation today Rodime has further demonstrated its reputation for reliability, a major design consideration for our 3½" drive, and quality. It has a rugged design with high resistance to shock, an important consideration for portability and for vibration prone environments. Using advanced large-scale integration, the entire electronics for the drive are on a single compact board and there are no adjustments or select-on-test components.

### New design horizons

The compact size of Rodime's drive suddenly puts large-scale storage into areas never considered before. The 350 series is one-fourth the volume of a 5¼" Winchester drive. And the 250 series, which includes

mounting brackets and a face plate, fits into the same space as a half-height 5¼" Winchester offering even fur[illegible]r shock and vibration isolation. Now system designers have a new level of flexibility. One area that has received attention is use with portable computers. Several major portable computer manufacturers have already incorporated Rodime 3½" Winchester disk drives into their products. There are other equally exciting areas such as desk top computer systems, intelligent terminals, point-of-sale terminals, industrial controllers, telecommunications systems, navigation and guidance systems, and portable instrumentation. In fact, the list of potential uses is only limited by the imagination of the system designer.

### A tradition of excellence

In a few short years, Rodime has established itself as a major force within the Winchester disk drive industry. Rodime is one of the few manufacturers that are delivering 5¼" Winchester drives with a broad range of capabilities up to 54 megabytes. And is the only manufacturer delivering high-performance 3½" Winchester drives in production quantities.

For the compact 3½" Winchester disk or other 5¼" Winchester requirements, look to Rodime. Rodime delivers.

RODIME

**Western Sales Office:** (714) 770-3085 • **Central Sales Office:** (512) 453-5135
**Distributors:** San Jose, CA (408) 946-8000 • Tustin, CA (714) 730-8000 • San Diego, CA (619) 279-5200, 453-9005
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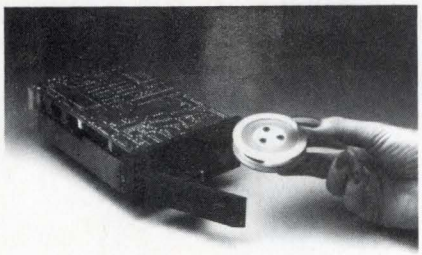
Addison, TX (214) 387-4949 • Austin, TX (512) 835-0220 • Sugarland, TX (713) 240-2255



CIRCLE 83

# MEMORY SYSTEMS

## Tape drives have 5- to 40-Mbyte capacities

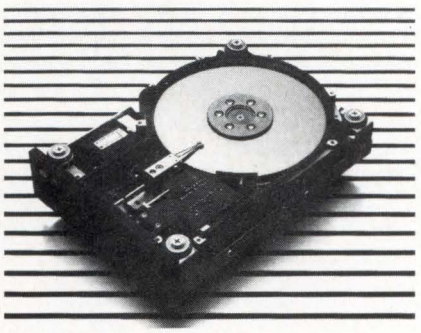


The ID 1010, 10-Mbyte family of tape drives has formatted capacities of 5, 10, 20, and 40 Mbytes. All drives use single-reel, self-threading, and fixing-head technology. Using standard quarter-inch tape, the single reels are upward compatible with 5- to 20-Mbyte models. The 5-, 10-, and 20-Mbyte models use SA450/SA300 floppy interface; the 40-Mbyte version uses SA850. **Interdyne Co,** 157 Topaz St, Milpitas, CA 95035.

**Booth C3436** **Circle 281**

## Half-height Winchester meets demand for compact storage

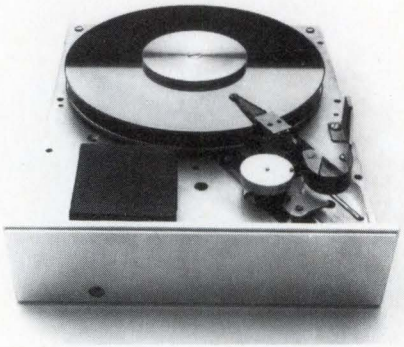
The HH-725 20-Mbyte drive provides high reliability for use with all microcomputers. The drive uses plated media for full 25.5 Mbytes of unformatted storage. Features include a single PC board and thermally isolated stepper motor. Functions include self-test during power-up, self-diagnostics, write fault detection, servo-position control, and interface control designations. The HH-725 has a recording density of 9680 bits/in., and a track density of 648 tracks/in. Also displayed will be the HH-312 10-Mbyte, half-height Winchester drive. **Microscience International,** 575 E Middlefield Rd, Mountain View, CA 94043.



**Booth C4366** **Circle 282**

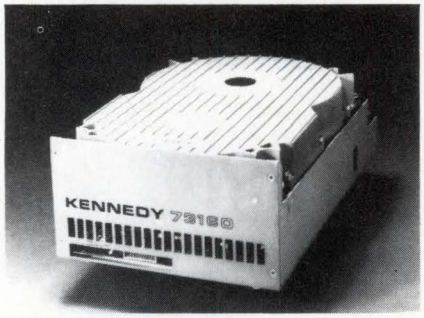
## Half-height Winchesters hold 12.76 Mbytes on two platters

Half-height, model CG912 5¼-in. Winchester disk drives use 306 cylinders to maintain total compatibility with IBM-PC DOS 2.0/2.1 software. The drives feature head spring suspension, multisource iron oxide recording media, and actuator lock. Drive electronics are on one PC board. Power of less than 12 W is needed. Stepper-motor driven head actuator has 85-ms average access time. **Cogito Systems,** 2355 Zanker Rd, San Jose, CA 95131.



**Booth C3242** **Circle 283**

## Winchester 8-in. drive employs minicomposite heads




Composite heads and high performance rotary actuator give the model 73160 an unformatted capacity of 165.9 Mbytes and an average access time of 20 ms. With four magnets instead of two, mass is reduced while access time is increased using less power. Composite heads provide improved read/write resolution with a narrower field, thus reducing fringing, and increasing data and track density. Disks have 9980 bits/in. on inner cylinder, 823 tracks/surface, and 800 tracks/in. The unit's data transfer rate is 9.67 MHz. The drive measures 4.62 x 8.55 x 14.25 in., and weighs 25 lb. Price is $4695; 90-day ARO delivery. **Kennedy Co,** 1600 Shamrock Ave, Monrovia, CA 91016.

**Booth A1344** **Circle 284**

## Tape drive operates in 1600/6250-bit/in. formats

An optional STC 2920 tape drive is integrated into the Bell & Howell tape subsystem that includes tape transport, formatter/controller, power supply, and resident microdiagnostics. Also shown will be the 6600 COM printer system that produces wet or dry, online, cut fiche in less than 60 s. The high speed, self-contained unit utilizes a DEC PDP-11 minicomputer and powerful software package. **Bell & Howell, COM Division,** 16691 Hale Ave, Irvine, CA 92714.

**Booth H412** **Circle 285**

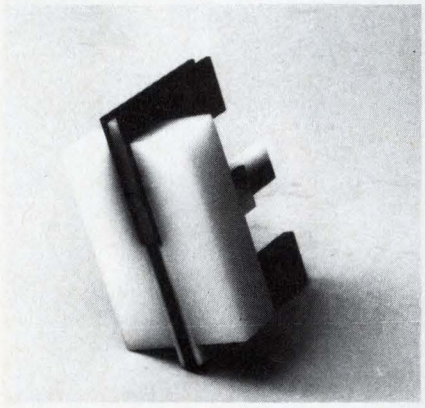
## Streaming-tape drives employ quarter-inch magentic tape

Two 500-Mbyte streaming tape drives have a half-inch magnetic recording tape cartridge. Model MT-2210 occupies 8.75 in. in a 19-in. rack; model MT-2220 has an 8.5- x 10.2-in. panel footprint. Drives read/write data on 300-Mbyte tapes. They can operate in a 200- or 50-in./s streaming mode with a data transfer rate of 240-kbytes/s, restoring 500 Mbytes in only 36 min. A two-track read/write head stepped 12 times creates a 24-track serpentine format with a 9600-bit/in. packing density. Self and offline testing diagnostic routines reside in the firmware. The MT-2210 is priced at $5500; the MT-2220 at $5750. Deliveries are scheduled for late 1984. **MegaTape Corp,** 1041 Hamilton Rd, Duarte, CA 91010.

**Booth C4362** **Circle 286**

# MEMORY SYSTEMS

## Glass-bonded subassemblies are epoxy free

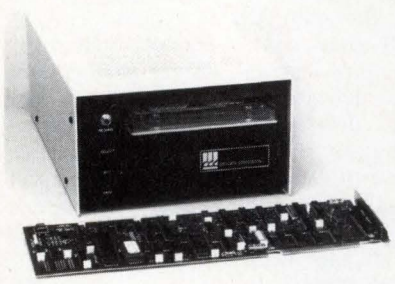


Two 96-track/in., glass-bonded subassemblies are designed for floppy disk applications. Glass bonding eliminates core shift, and minimizes head and media wear. The hot pressed, manganese-zinc subassemblies are available in single- or double-sided tunnel erase. Standard track formats or custom formats are available. **Ferroxcube,** 5083 Kings Hwy, Saugerties, NY 12477.

**Booth B3627** **Circle 287**

## Single PC-compatible cartridge replaces 51 floppies

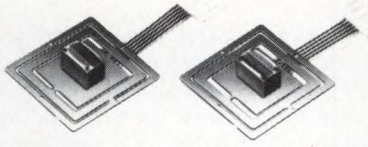
Providing 16.5 Mbytes of disk backup in one cartridge, the model 70 PC transfers data at 0.7 Mbytes/min. This allows users to back up a 10-Mbyte PC/XT in 15 min. Data storage is in a file-oriented architecture that permits backup of only the changed disk portion. The cartridge tape subsystem is fully compatible with the IBM PC, as well as most PC compatibles, like Compaq, Columbia, and Eagle. Included with the unit is a Z80-based controller for the PC, driver software, and cables. The 70 PC is a 6400-bit/in., 4-track, quarter-inch tape drive that uses ANSI standard 4- x 6-in. tape cartridges. Housed in a desktop enclosure, the unit weighs less than 20 lb. Price is under $1400 in 100s. **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, MD 20794.



**Booth C4126** **Circle 288**

## Smooth floppy disk drive heads minimize damage risk

Models F723 and F724 are made with a manganese-zinc compound that minimizes disk damage. These floppy disk drive heads are available with dual-sided gimballed configuration and carriage assemblies. DC resistance is 35 Ω nominal read/write, 3 Ω nominal erase. They ave a 458-kHz minimum resonance frequency. The E2SMR direct drive motor



for 5¼-in. floppy disk drive applications, meauring 91 x 11.8 mm, and weighing 360 g, is also shown. It has a rated voltage of 12V ±10 percent, and a rated speed of 300 rpm. Models F883 and F884 floppy disk drive heads have a dc resisance of 50 Ω maximum read/write; erase of 5 Ω maximum. **Sankyo Seiki Co Ltd,** 20911 Western Ave, Torrance, CA 90501.

**Booth A2242** **Circle 289**

## Half-height removable Winchesters available in quantity

The 6.38-Mbyte SQ306RD cartridge disk drive features 3.9 in. graphite sputtered thin-film media housed in a standard 5¼-in., half-height footprint. Also displayed will be the 25.5-Mbyte SQ325F, and the 38.2-Mbyte SQ338F. **SyQuest Technology,** 47923 Warm Springs Blvd, Fremont, CA 94539.

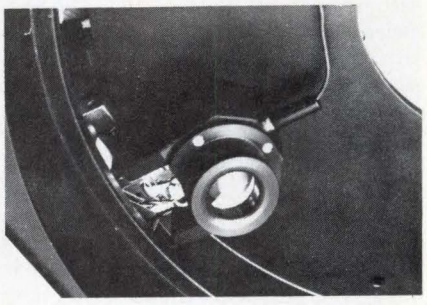
**Booth H910** **Circle 290**

## Floppy disk system provides high speed and large capacity

Portable microprocessor controlled 5¼-in. floppy disk system is easily interfaced with RS-232, RS-422, or 20-mA interface. Typical applications include program loading, peripheral storage, data logging, computer storage and backup, and data transfer between other RS-232 systems. The large capacity (2 Mbyte), high speed (200 kbaud) system is available with custom protocols. The system is 6.5 x 5 x 9.5 in. and runs on 110 V, or 220 V optional. The system sells for $700 in 100s. **Analog & Digital Peripherals, Inc,** 815 Diana Dr, Troy, OH 45373.

**Booth A1846** **Circle 291**

## Head inspector examines while installed



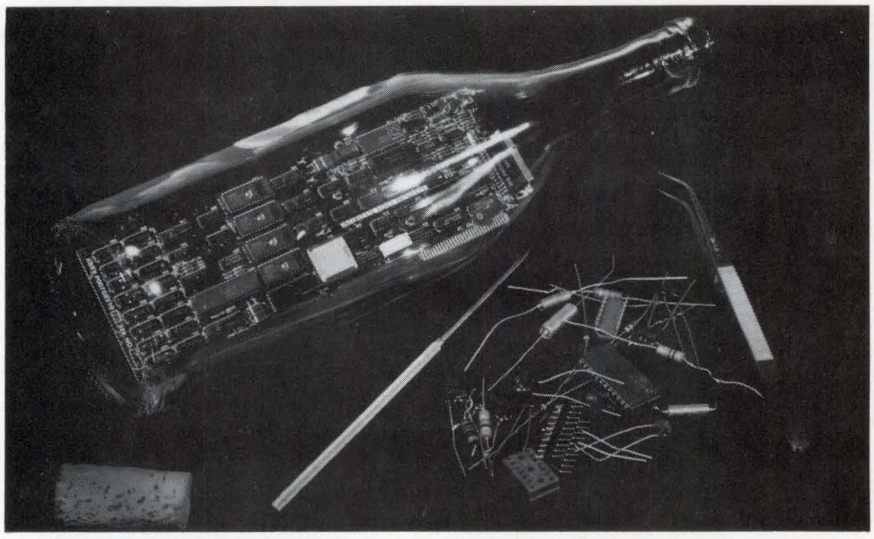
Disk head inspector unit examines disk heads for removable media disk drives while still installed. CPX also carries media, spares, subassemblies, alignment packs, absolute filters, and disk drive heads. Locator task force service helps find scarce parts. **CPX,** 19821 Nordhoff St, Northridge, CA 91324.

**Booth C4298** **Circle 292**

# INTERFACE

## Speech recognition board operates in keyboard/PC modes

A plug-in, printed circuit speech recognition board designed for the IBM PC and XT computers contains all processing, memory, and I/O interfaces needed to convert spoken word to digital code. A 16-bit Intel 80186 microprocessor, 128-Kbyte DRAM, and 32-Kbyte EPROM allow the board to execute speech recognition algorithms not previously available. A menu-based utility program provides such features as subroutines written in Basic, and help display. Keyboard mode simulates keystrokes; spoken utterances appear to the CPU as though entered by keyboard. In addition, any IBM PC compatible software can be used. The board holds up to 240 isolated words or phrases with an 80-ms minimum word length. It has an audio input bandwidth of 200 to 7000 Hz, with



a 10 kΩ input impedance. Power requirements are 5 V at 1A, 12 V at 80 mA, and −12 V at 150 mA. **Interstate Voice Products,** 1849 W Sequoia Ave, Orange, CA 92668.

**Booth 3628** **Circle 293**

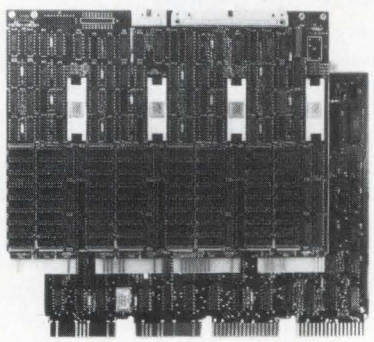
## High performance peripheral controllers feature gate array designs

Supporting IEEE 796 Multibus-based systems, the 420 series provides fast memory transfers and improved error correction. The controllers allow simultaneous operation of a QIC-02 interface tape drive and either ST506/412 or ESDI disk drives. A modular design puts all Multibus and tape control functions on a common motherboard and implements interface circuitry on a flush-mounting daughterboard. Gate array devices permit 2.5-Mbyte/s DMA transfers and ECC logic to implement a 32-bit ECC algorithm to correct up to 11 bits. The proprietary DMA controller's bandwidth is in excess of the combined transfer rates of the data drive (100 Kbytes/s) and the disk drive (625 Kbytes/s to 1.2 Mbytes/s). A speed match between high speed disk data path and the system bus takes place with a 4-Kbyte FIFO buffer. The tape drive uses a 512-Kbyte buffer. These buffers eliminate late data conditions for disks and tape. As a result, there is no loss of disk revolutions or stopping tape during periods of heavy bus activity. An I/O parameter block results in a high degree of programming flexibility via channel control and improved system response. Commands are issued from the operating system by creating a block in memory and pointing the controller board at the block. When the controller finishes executing a command, it sets a completion status and controller ready bit in the status register. Detected errors generate an error code, which is returned in the block for examination by the operating system. The peripheral controllers are priced at $995. **Xylogics, Inc,** 144 Middlesex Tpke, Burlington, MA 01803.

**Booth H835** **Circle 294**

## Graphics controller handles high resolution monitors

The GC-20 graphics controller is designed for use with monitors on DEC LSI-11 minicomputers. The controller consists of a GI-20 graphics interface board and RM-20 refresh memory board. It generates a 1024 x 1024 interlaced image, with 4 bits per pixel, and emulates Tektronix 4010, 4014, and 4065 terminals.



The GI-20 uses an onboard 68000 microprocessor, supported by 128-Kbyte RAM and 128-Kbyte EPROM. A rear edge cable provides interface to the RM-20 board. The RM-20 contains four 7200 VLSI graphics controllers; each drive one of four 1024 x 1024 planes. The GC-20 controller costs $5900 in single quantities. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512.

**Booth A1314** **Circle 295**

## Fixed-disk controller combines ESDI and SCSI

The S2410 supports up to four ESDI disk drives with the option of 5- or 10-Mbit/s NRZ data rates. The SCSI bus connection is designed for systems requiring multiple hosts and disconnected operating efficiencies. The host interface is the small computer Xebec interface (SCXI), a subset of ANSI SCSI with a maximum host transfer rate of 1.5 Mbytes/s. It has all the standard SCSI features plus extensions, controller-to-controller copy for tape backup, device-independent host drivers, and bus parity checking. The disk drive interface supports removable hard sectored drives, sector pulse drives for maximum capacity and data reliability, and programmable block sizes. **Xebec**, 432 Lakeside Dr, Sunnyvale, CA 94086.

**Booth A2134** **Circle 296**

# INTERFACE

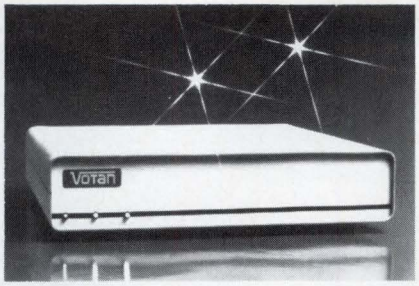
## Standalone emulators offer high price/performance ratio

In-circuit emulator, ICD 178 68000, emulates the Motorola 68000, 68008, and 68010 in one unit. It contains 128-Kbyte emulation memory, 4-K deep x 48-bits wide realtime trace buffer, 3 hardware and 8 software breakpoints, and an external breakpoint probe for TTL signals. Optional software package turns an IBM PC into a complete development system for the 68000. The unit is 4.2 x 8.2 x 11.8 in., and weighs less than 10 lb. The price is $7995, and delivery begins in June. The ICD-278 Z80H full-function standalone debugger will also be shown. This 7-lb unit is priced at $4995, and is 3.2 x 8.2 x 11.8 in. The ICD 178 8048 in-circuit emulator for the Intel 8048 family features 4-Kbyte emulation memory, and a built-in PROM programmer for the 8748 and 8749. It has the same weight, dimensions, and price as the ICD-278. **ZAX Corp,** 2572 White Rd, Irvine, CA 92714.

**Booth H844** **Circle 297**

## Terminal gives voice I/O to ASCII devices

The VTR 6000 voice terminal provides complete voice I/O functions at reduced cost. Offering voice recognition, speech generation, and telephone management capabilities, the terminal connects to any computer supporting an RS-232 serial port and X-on/X-off protocol. Continuous speaker-dependent recognition (CSDR) allows an individual to speak in normal conversational flow. Speech recognition operates over standard telephone lines. Phone interface capabilities include auto-answer, autodial, and encode/decode. The standalone VTR 6000, consisting of a chassis, power supply, microphone, and speaker, is available immediately and costs $3950. The VSP 1000 voice processor board offers voice I/O on a single, low cost board and features CSDR. The board contains all hardware required to service a voice channel with custom LSI chips performing proprietary pattern matching functions. VSP 1000 conforms to IEEE 796 specifications. The VSP 1000 is available immediately and costs $2500. The VPC 2000 voice card for speech command and control of PC




programs will also be shown. This lists for $2450 and is also available immediately. **Votan,** 4487 Technology Dr, Fremont, CA 94538.

**Booth C3772** **Circle 298**

## Interface handles IEEE 488 compatibility

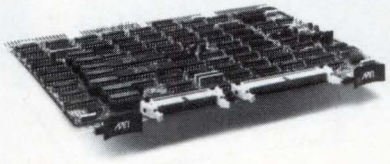
The Candy Apple IEEE 488 interface implements the Intel 8291A and 8292 integrated circuit set, which provides computers with an Applebus interface that has talker, listener, and controller capabilities. An independent power supply is provided. The system is useful for such applications as laboratory, test and measurement, and process control, or any application with an IEEE 488 interface. **Tecmar, Inc,** 6225 Cochran Rd, Solon OH 44139.

**Booth C3694** **Circle 299**

## Streaming tape controllers offer versatility

A Q-bus streaming tape controller, the MSV05, uses low cost quarter-inch cartridge tape drives. This single-board, dual-height unit emulates DEC's TSV05 subsystem. Features include 45-Mbyte backup capability, ability to interface with QIC-02 cartridge tape, block mode DMA, and 16-Kbyte buffer. Model MX22, an 8-in. and 5¼-in. floppy disk controller, emulates two RX02 subsystems and interfaces with up to four floppy disk drives simultaneously. Designed exclusively for Unibus-based computers, the controller has internal diagnostics and an integral LED. A versatile Q-bus floppy disk controller rounds out the offerings. MXV24 is a dual-size, RX02-compatible controller with 22-bit addressing, built-in diagnostics, and formatting capability. **Micro Technology, Inc,** 1620 Miraloma Ave, Placentia, CA 92670.

**Booth C4260** **Circle 300**



## Disk tape controllers back a variety of computers

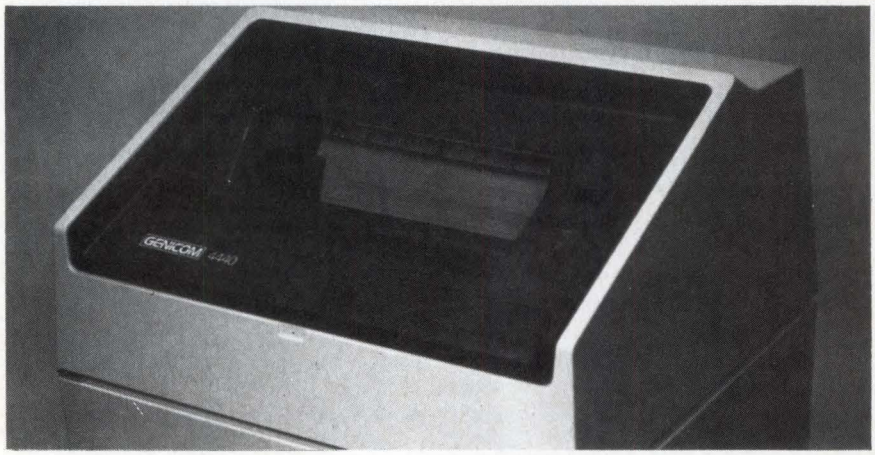
SPECTRA 27 multifunctional disk/tape controller supports Data General's MV minicomputer series and is compatible with its FCC hardened chassis. SPECTRA 27 emulates DG's 6060 and 6160 series disk and 6021 tape subsystems. SPECTRA 17 is a single function, disk-only version of the SPECTRA 27. SPECTRA 126 is a multifunctional disk/tape controller for Texas Instrument's 990, 600, and 800 computer users. It emulates TI's CD1400 and DS80/300 disk and 979 tape subsystems. SPECTRA 116 is a single-function, disk-only version of the 126. SPECTRA 121 is a Unibus-compatible, multifunctional disk/tape controller for DEC PDP-11 and VAX computers. It emulates DEC's RM02/5, RM80, and RP06/7 disk subsystems. The 111 is a single-function, disk-only version of the 121. **Spectra Logic Corp,** 1227 Innsbruck Dr, Sunnyvale, CA 94086.

**Booth A2122** **Circle 302**

**Booth numbers that begin with A, B, C, or D will be located in designated areas of the Las Vegas Convention Center. Booth numbers beginning with an H can be found in the Las Vegas Hilton.**

# PERIPHERALS

## Printers operate in three different modes




Two high speed shuttle matrix models from the Genicom 4000 series operate at speeds from 300 to 600 lines/min. The models incorporate three printing modes: draft, NLQ, and graphics/plotting. Features include serial and parallel interfaces, character expansion printing, automatic bold and underline, automatic superscripts and subscripts, and nine bar codes. Also shown will be products for the 3000 matrix printer series. **Genicom,** 1 General Electric Way, Waynesboro, VA 22980.

**Booth C3308** **Circle 303**

## Keyboard combines low cost, choice of keycaps

Next generation keyboard combines low cost, full travel, quality, and reliability. Two different keycaps plus tactile or linear feel are available. Also shown will be a wireless keyboard. It may be used in wireless, simplex mode, and buffers up to 16 keystrokes. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60087.

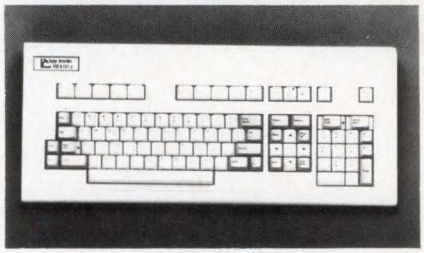
**Booth A2100** **Circle 304**

## Printer with extended interface is 3274/76-compatible

An extended communication interface capability for a 300-line/min printer system provides model 1 or 2 emulation with Type A coaxial connection. The Innovator 202 supports transparent mode compatibility, processor interrupt transmission, local or remote configuration, BSC or SNA data streams, SNA control string capability, and built-in diagnostics. One of five logical, and one of two physical buffer sizes are user definable. A micro-based, single-board computer system controls the printer. Price is $7395, with 30-day delivery from stock. **Innovative Electronics, Inc,** 4714 NW 165th St, Miami, FL 33014.

**Booth A1333** **Circle 306**

## Plug-compatible keyboard for IBM's PCjr



Professional-grade, plug-compatible keyboard for IBM's PCjr provides operator comfort and keyboard durability. The portable keyboard has a low profile design, typewriter key location, LED indicators, connector cable, a separate numeric cursor, and function key areas. **Key Tronic Corp,** Department E6, PO Box 14687, Spokane, WA 99214.

**Booth 4206** **Circle 307**

## Line printer offers variety of character sets

Linewriter 800 third-generation band-line printer has an 800-line/min speed. Linear free flight print hammers and low band speed provide quality correspondence printing. LSI and VLSI technology, a 600,000-line cassette ribbon, and operator replaceable print boards reduce maintenance costs and increase reliability. Sixty-five different print boards in 48-, 64-, 96-, and 128-char sets are available. **Centronics Data Computer Corp,** 1 Wall St, Hudson, NH 03051.

**Booth C3830** **Circle 305**

## Monochrome monitor designed for high resolution display

High resolution monochrome monitor has 100-MHz video amplifier with less than 4-ns rise and fall times. Geometry and linearity specifications are ±1 percent for graphics display. Optional external brightness and contrast controls, and 30- to 70-kHz horizontal scan rate are available. Price for single-bit ECL video input and ac power supply is $1225. **Video Monitors, Inc,** 3833 N White Ave, Eau Claire, WI 54701.

**Booth A1915** **Circle 308**

# PERIPHERALS

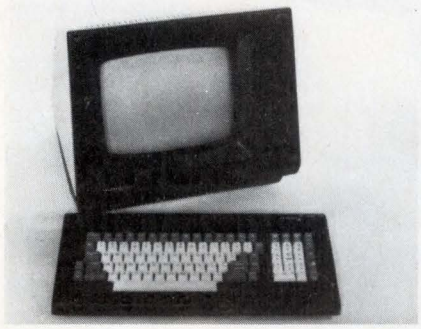
## Low noise daisy wheel printer runs at high speed

Low cost, high speed daisy wheel printer 6300 has 96 chars and operates at 40 chars/s with a 60 dBA noise level. A 16-in. platen and multistrike ribbon round out special features. Operating on a Centronics parallel or RS-232-C serial interface, power consumption is 70 W. A 3-Kbyte buffer memory is expandable to 15 Kbytes. The printer measures 600 x 400 x 125 mm, and weighs 14 kg. **Juki America,** 299 Market St, Saddle Brook, NJ 07662.

**Booth A2644** **Circle 309**

## Multifunctional terminal offers Honeywell, DEC compatibility

Multifunctional 7-HNY terminal offers Honeywell VIP7300 and DEC VT102 compatibility. It contains two bidirectional RS-232 ports, as well as line drawing and mosaic character sets. Setup parameters are entered from the keyboard. It has 12 preprogrammed function keys, and a 512-char, nonvolatile memory. An extended ANSI code set allows communication with a single terminal. Available in 9-, 12-, and 15-in. CRT sizes, and white, green, or amber phosphor. List price for the 12-in. CRT is $1695, with 45-day delivery. **Teleray,** Box 24064, Minneapolis, MN 55424.



**Booth A1858** **Circle 310**

## Personal computer keyboard meets ergonomic standards

The FC2500 personal computer keyboard provides 83-key layout for a detachable, serial interface keyboard. Standard features include 30-mm height requirements, LED key stations, 5 Vdc operation, selectable baud rates, and output format. Keyboard is emi/rfi shielded by an injection molded noryl enclosure. A standard 6-conductor modular phone connector with 6-ft, 26-gauge coiled cable is used. Optional features include 12-Vdc operation for

long cable requirements, repeat disable, audible feedback, and quiet tactile feel. Also shown will be the Cyclops touchscreen device, and Beetle cursor director. **ITW Cortron, division of Illinois Tool Works, Inc,** 400 W Grand Ave, Elmhurst, IL 60126.

**Booth A1442** **Circle 311**

## Printers added to nonimpact page printer family

The Lasergrafix 1200 and 800 model I, are two intelligent nonimpact page printers. The 1200 prints at 12 pages/min, has resolution of 90,000 dots/in.$^2$, and a full bit-mapped memory. The 800 prints 8 pages/min and is priced at $9995; the 1200 is $24,995. A low end Lasergrafix 800 model II is an 8-page/min word processing printer with limited graphics, selling for between $5000 and $6000. The Lasergrafix 2400 is a higher speed printer, able to process 24 pages/min, handle up to 11- x 17-in. paper, with a full bit-mapped page memory. This unit sells for about $35,000. **Quality Micro Systems, Inc,** PO Box 81250, Mobile, AL 36689.

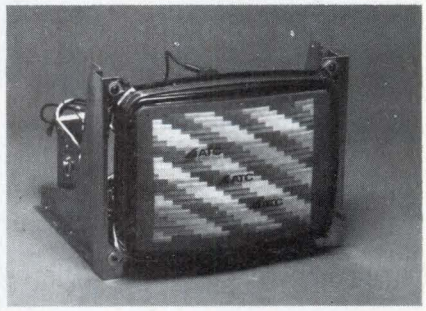
**Booth C4150** **Circle 312**

## Printer peripherals are plug-compatible with micros

The MVP 150B dot-matrix line printer is designed specifically for plug compatibility with the IBM PC. It can be used as either a shared resource printer or system printer. Features support such applications as graphics and word processing at speeds from 80 to 200 lines/min. Price is $3745 with 30-day ARO. The 4160 printer/plotter will also be available. Its print hammer dot is one-half the size (0.010 in.) of standard dots; dot density is 160 horizontal x 168 vertical dots/in. Bar-code labels have high resolution, and meet MIL-STD-1189 requirements. Suggested price is $5380; 30-day ARO. **Printronix, Inc,** 17500 Cartwright Rd, Irvine, CA 92713.

**Booth 4166** **Circle 313**

## High-resolution terminal displays 16 colors



Model 14DD981 color terminal has a 14-in. CRT with a 90-degree reflection angle. The noninterlaced resolution of 720 dots x 396 lines, has a usable display of 210 x 280 mm. The terminal provides a 25-MHz video bandwidth, 24.5-kV high voltage, and 15.75-kHz horizontal scanning frequency. AC power input is 120 V ±10 percent at 60 Hz, or 240 V ±10 percent at 50 Hz. It weighs 27.5 lb, and provides 16 display colors. **Audiotronics,** 7428 Bellaire Ave, N Hollywood, CA 91605.

**Booth A1434** **Circle 314**

# PERIPHERALS

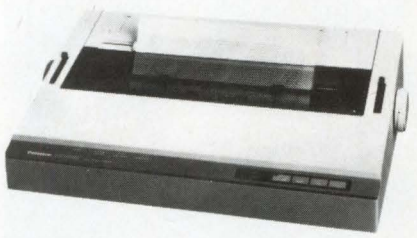
## Letter quality printer uses electrophotographic method

Elpho 20 nonimpact, electrophotographic page printer provides letter quality at a 20-page/min print speed. Designed as a shared printer, simultaneous copying is accommodated. With a printer resolution of 300 x 300 dots/in., print matrix is 30 x 50. Up to ten 140-char sets are resident. Self-test and remote diagnostics, and two-page buffer are featured. Printer supports Data Products byte parallel, Centronics byte parallel, and RS-232-C interfaces. **Philips Peripherals,** 385 Oyster Point Blvd, S San Francisco, CA 94080.

**Booth D4226** **Circle 315**



## Daisy wheel printer provides word processing functions

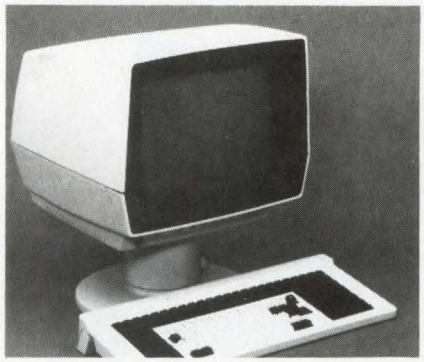


A Diablo-compatible, bidirectional printer has a full 96-char wheel. The serial-impact KX-P3151 prints at 22 chars/s in 12 pitch, or 21 chars/s in 10 pitch. This logic-seeking printer also accommodates such word processing functions as bold and shadow lettering, backspace, margins, tabs, and underline. Such features as standard friction feed, optional tractor and cutsheet feeds, as well as multistrike fabric ribbon, LED lights, and reset alarm are provided. The KX-P3151 will be available in late 1984. However, Panasonic will show three 9-pin, dot-matrix printers, and three computer display systems. **Panasonic Industrial Co,** One Panasonic Way, Seacaucus, NJ 07094.

**Booth C3588** **Circle 316**

## Intelligent terminal configured for Univac emulation

Model 8188-7 VIT intelligent terminal is designed for user-selectable emulation of Univac UTS-400, U100/200, and IBM 3275/3271/3277. Included is TTY emulation. An alternate operating system interface is available for CP/M-80. The VIT utilizes a 68000 microprocessor, 128- to 1024-Kbyte RAM, two RS-232 host interfaces, and one printer interface. **Megadata Corp,** 35 Orville Dr, Bohemia, NY 11716.



**Booth C4036** **Circle 317**

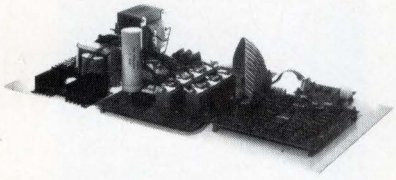
# PACKAGING & POWER

## Portable UPS protects small electronics from power problems

Plug-in 750 VA mini-UPS regulates voltage to ± 3 percent of nominal. Input frequency fluctuations of up to ± 10 percent of nominal (60 Hz) are tightly regulated at the output to ± 0.5 percent Hz. It offers an auto inverter restart and an alarm circuit for signaling battery operation. This assures that the inverter will resume normal operation after shutdown due to discharged battery as soon as ac input power is restored. Price is $1619. **Sola Electric,** 1717 Busse Rd, Elk Grove Village, IL 60007.

**Booth A1604** **Circle 318**


## Control system handles UPS conditioning



Master Control Module (MCM) II solid state controls for rotary UPS conditioners feature bidirectional bypass without interruption of critical load, as well as digital metering readout capabilities. The MCM II has no moving parts. **Atlas Energy Systems,** 9457 Rush St, South El Monte, CA 91733.

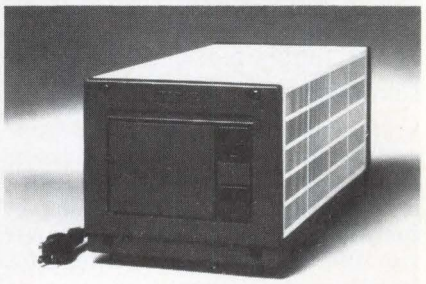
**Booth B3910** **Circle 319**

## Increased inverter efficiency furnished in UPS series

Uninterruptible B series power systems include a 50-kVA model with greater than 83-percent efficiency at 25 percent of load and over 87-percent efficiency at 100 percent of load. The B series UPSs provide protection from 1 to 50 kVA and will be available in 1-, 3-, 5-, 10,- and 25-kVA single-phase, and 25-, 37.5-, and 50-kVA three-phase models, with 50-Hz versions for foreign markets. Models UPS 103-3B and UPS 153-3B supply output power at 10 and 15 kVA respectively. They operate along with an external auxiliary battery that furnishes energy to the UPS inverter during ac input power failure. In turn, the inverter furnishes uninterrupted and conditioned power to the critical load. Smaller series models feature an inverter synchronization frequency window of ±60 Hz, slow slew rate frequency (1 Hz/s typical), and automatic forward transfer on the bypass switch after overload induced reverse transfer occurs. The 1-, 3-, and 5-kVA units also feature a transistorized pulse width modulated static inverter. On the 103-3B and 153-3B models, the inverter converts dc to the desired, well-regulated transient-free 120/208-Vac three-phase output, with optional 480-Vac available. Recovery time to normal operation after transient is 34 ms to less than ±2 percent of average steady state conditions. Audible noise for the 103-3B and 153-3B measures less than 70 dB(A weighted) at 6 ft. Heat loss is 8,900 Btu/hr for the 10-Vac model; 12,800 Btu/hr for the 15-Vac version. In addition, the SPR 201 and SPR 401 compact UPS models for microcomputers measure 6 x 11 x 12 in. and weigh 32 lb. The 201 output is rated at 200 VA, while the 350 is set at 350 VA. Output frequency accuracy for these units is marked at 60 Hz, ±005 percent. **Elgar Corp,** 8225 Mercury Ct, San Diego, CA 92111.


**Booth A1500** **Circle 320**

## Power conditioner controls voltage with microcomputer



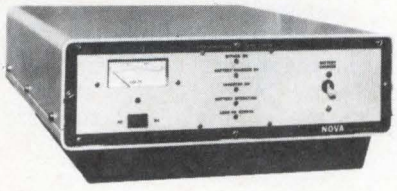
Power conditioner with Powerlogic, microcomputer-controlled voltage regulation has 4 to −8 percent output voltage regulation band for all line and load conditions. An input circuit breaker opens if output voltage exceeds 12 percent of rated nominal. At operating frequencies of 47 to 53 Hz for 50-Hz models, and 57 to 63 Hz for 60-Hz models, operating temperature is 0 to 40°C. Conditioner has a 90 percent minimum efficiency rate, and 2 percent maximum harmonic distortion rate. **Topaz**, 9150 Topaz Way, San Diego, CA 92123.

**Booth A1000** **Circle 321**

# PACKAGING & POWER

## High frequency switching means reduced weight for 1-kVA UPS

MinTaur 1-kVA rated uninterruptible power system packs batteries and one-quarter cycle solid state transfer switch in a 99-lb module. Designed for operations that include microcomputers, process control, and CAD/CAM, this UPS handles up to 10 times overload through automatic operation of the static transfer switch. I/O voltage specs are 120, 220, and 240 Vac. Standby time is 9 min at rated load and 0.8 power factor. The Integra 5-kVA UPS requires no special battery room, ventilation, or special wiring. I/O voltage measures 120 Vac, with 208 and 220 Vac available, and voltage regulation is set at ±1 percent. MinTaur model 11-1K60-Y11 is now available at $3700. The Integra system is priced at $12,975. **Nova Electric Mfg Co,** 263 Hillside Ave, Nutley, NJ 07110.



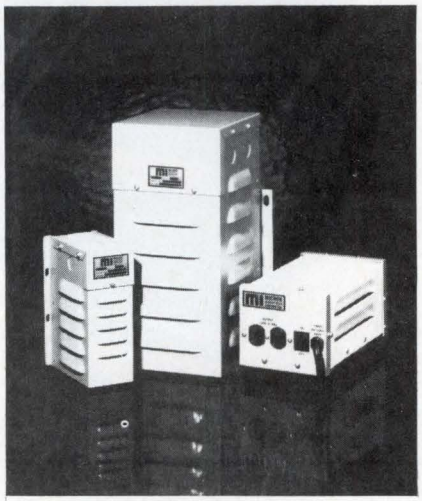

**Booth A1231** **Circle 322**

## Power supply provides continuous sine wave output

Uninterruptible power supplies provide uninterrupted sine wave output at power disruption, thus preventing overheating of transformers or overstressing of computers. Ratings of 200 and 500 VA are offered. Series also attenuates transverse and common-mode noise, as well as maintaining voltage within ±3 percent of nominal. LED indicators show battery condition and current operating mode. Alarm activates at power outage. Series will be available in late 1984. **The Superior Electric Co,** 383 Middle St, Bristol, CT 06010.


**Booth B4101** **Circle 323**

## Constant voltage regulators protect sensitive equipment



Power conditioning regulators provide dependable protection against ac power fluctuations for sophisticated electronic equipment. They also correct and maintain power quality at required levels. Coils are located outside the core, permitting 2-yr warranty. The considerably lighter-weight regulators (up to 45 percent) require no maintenance. Regulators can be custom designed to meet a variety of needs. **Micron Industries Corp,** 1830 N 32nd Ave, Stone Park, IL 60165.

**Booth B4007** **Circle 324**

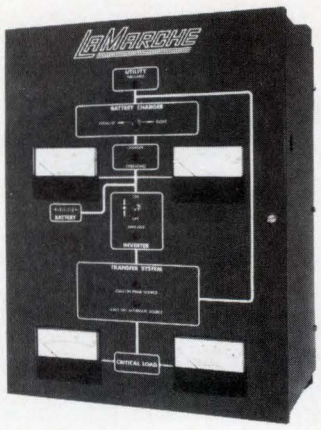
## Monitoring system geared toward various mainframes

The Environmental Data Acquisition and Control System (EDACS)—the microprocessor controller of the 4000 series—is a powerful environmental monitoring system for small or large computers. It provides the series 4000 with a way to collect data on all aspects of the computer room environment. Users select functions appropriate to computer operation, then program these functions into EDACS. Additional programming is possible with the system's microprocessor-based, interactive capabilities. The system uses high speed CMOS components, with full battery backup power. User-friendly interface has 320-char LCD, and 16-key user keyboard for interactive communication. Optional 40-char data logger line printer, and full mainframe and remote diagnostics communication capabilities are available. Series 4000 product line is priced from $7000 to $30,000, depending on configuration. **Computer Power Systems, Inc,** 18150 S Figueroa St, Carson, CA 90749.

**Booth C4282** **Circle 325**

## Uninterruptible power systems offer variety

Ranging in size from 500 to 20,000 VA, these UPSs offer 24-, 48-, and 120-Vdc operation. Both ferroresonant and new sine weighted pulse width modulation models are available, with or without static switches. **LaMarche Manufacturing Co,** 106 Bradock Dr, Des Plaines, IL 60018.




**Booth B3420** **Circle 326**

## Total power protection provided by UPS

Uninterruptible power systems are designed as cost-effective systems for total power protection applications. Typical UPS is 20 to 50 percent smaller than conventional UPS designs, and has static bypass transfer switches for uninterrupted forward or reverse transfer. UPS modules are available in standard ratings from 2 to 600 kVA. **Emergency Power Engineering, Inc,** 3580 Cadillac Ave, Costa Mesa, CA 92626.

**Booth B4228** **Circle 327**

# PACKAGING & POWER

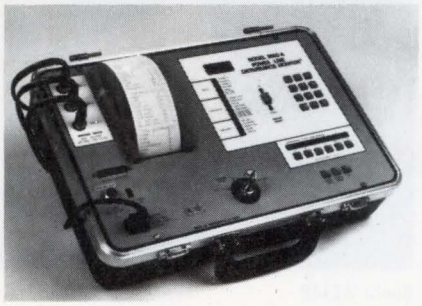
## Modular power system makes mini hookup easy

Using modular construction, the series 1000 UPS allows self-installation for terminal cluster, microcomputer, and minicomputer applications. This compact system measures 40 x 17 x 21 in., includes 5-min battery, and weighs 370 lb. Series 1000 offers 90 percent efficiency, −20 percent input voltage tolerance, 2-percent output regulation, and sealed maintenance-free batteries. Power rating is 3 kVA. System is priced at under $6000. **Exide Electronics,** PO Box 58189, Raleigh, NC 27658.

**Booth B3938** **Circle 328**

## Power line disturbance monitor with self-diagnostics

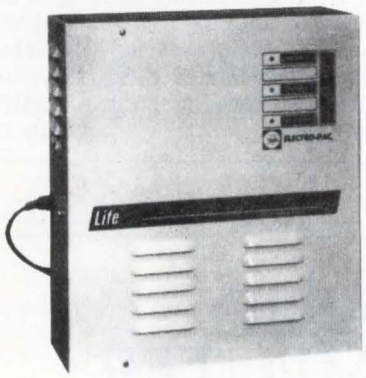
As an upgrade of the model 3600 unit, the 3600A measures disturbances of brief duration that deviate from the operating thresholds of sensitive electronics. This portable unit features a self-test program that checks the microprocessor, time-of-day clock, RAMs, EPROMs, printer, power supply, and other circuits. The unit then prints out an internally generated test pattern on a top to bottom readable tape. An uninterruptible power system provides battery ride-through and allows the monitor to operate during complete blackouts for as long as 2 hrs. It includes a selectable baud rate RS-232 port that allows use in remote, unmanned locations on a long-term basis. **Liebert Corp, Programmed Power Division,** 995 Benicia Ave, Sunnyvale, CA 94086.



**Booth A1722** **Circle 329**

# PACKAGING & POWER

## An ac power device supplies clean, reliable power

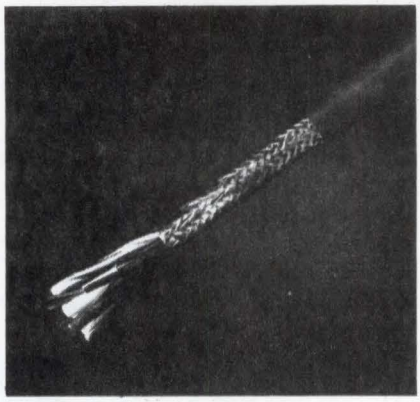



An uninterruptible ac power supply is now available with 1-kVA power output. This unique design provides voltage regulation and line filtering, plus an inverter for power outages. Maintenance-free battery handles full system power for 5 to 10 min. An external battery may be used if needed. **Instrumentation and Control Systems, Inc,** 520 Interstate Rd, Addison, IL 60101.

**Booth A1306** **Circle 330**

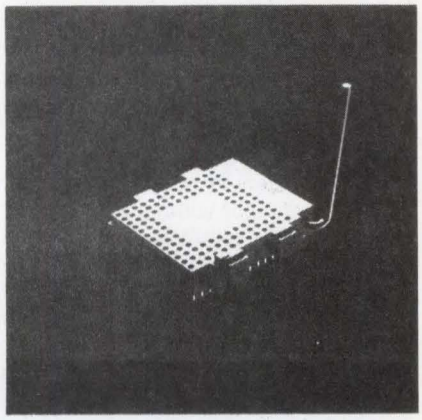
## Multipair data cables allow extended distance transmission

Series 8162 data cables combine low capacitance and high shield effectiveness. The series has 24 AWG stranded conductors that allow extended distance data transmission in EIA RS-232 and RS-422 applications. Each pair is shielded to avoid crosstalk and improve signal integrity between pairs. **Belden Electronic Wire and Cable,** 2000 S Batavia Ave, Geneva, IL 60134.



**Booth C4511** **Circle 331**

## Pin grid array socket allows insertion without force

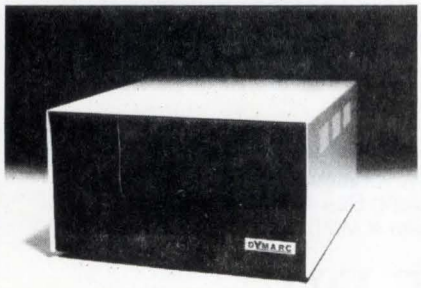


This pin grid array socket has lever-actuated cam, allowing insertion and extraction of substrate without applying force to pins. Pin diameters of 0.020 to 0.016 in., and pin lengths of 0.125 to 0.210 in. can be mounted. Socket has an initial contact resistance of 15 MΩ (max), and final contact resistance of 25 MΩ, **AMP Inc,** PO Box 3608, Harrisburg, PA 17105.

**Booth H328** **Circle 332**

## Uninterruptible power supply weighs only 32 lb

The model 1350 uninterruptible power supply provides instant back-up electric power for computers. Weighing only 32 lb, and compact enough to fit in 0.5 $ft^3$ space, the 1350 is priced at $750 with maintenance-free battery. System provides 120 V at 350 VA, has a 12-ms transfer time, and a single phase 60-Hz supply. **Dymarc Industries,** 21 Governor's Ct, Baltimore, MD 21043.




**Booth C4145** **Circle 333**

## Compact, stationary batteries for use in UPS applications

Compact series of JCW stationary bateries is designed for 10- to 30-kVA, 15-min reserve time uninterruptible power systems. A 10-kVA, 60-cell battery string fits in an 8-in., two-tiered battery rack. Batteries range from 0.18 to 0.54 kW per cell. Transparent plastic containers, an dead-top, flame-retardant covers are standard. The lead-alloy terminals ensure tight connection to other units in the string. **C&D Power Systems,** 3043 Walton Rd, Plymouth Meeting, PA 19462.

**Booth A1917** **Circle 334**

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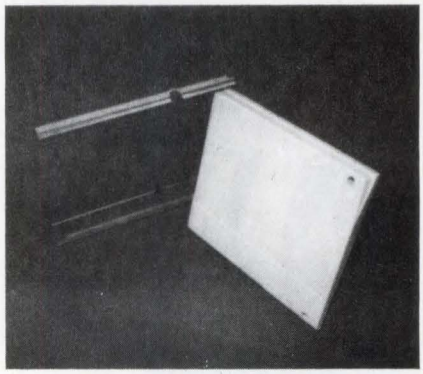
## One-sided shielding requires no painting

Color housings can be shielded with FCM-CS, electroless plating on plastic that shields against electromagnetic interference, and protects only certain parts of a plastic housing. Single-sided shielding can be applied to all plastic products. **FCM Plastics,** 2555 Oak Industries Dr NE, Grand Rapids, MI 49505.



**Booth A2110** **Circle 335**

# SOFTWARE

## Software implements database and management systems

Two systems are available for IBM mainframes and DEC VAX. Clio is a multimodel data base implemented on IBM mainframes under OS, DOS, and VM, as well as on DEC VAX systems. It requires a minimum storage allocation of 64 Kbytes for batch execution. A host language interface provides easy access to Clio data bases from other high level programs. SPITAB is a unique table management tool for IBM mainframes. It runs on standalone under VSAM, or as an interface to IMS or DL/1 data base. **United Software Systems and Services Corp,** 1801 Avenue of the Stars, Suite 300, Los Angeles, CA 90067.

**Booth D4214** **Circle 336**

## Software system transports IBM system/36 programs to PC-XT

The Baby/36 consists of several components including RPG II compiler, operation control language processor, and screen-format generator. In addition to allowing system/36 software to run on the PC/XT, the package can also be used as a standalone development system. Utilities include source entry, sort, data exchange, and data file. **California Software Products, Inc,** 525 N Cabrillo Park Dr, Santa Ana, CA 92701.

**Booth H822** **Circle 337**

## Systems software package provides fast CRT terminal switching

VIRTUE software package provides fast and easy switching of a CRT terminal between computers in an IBM virtual machine environment. Single-stroke function key on the CRT terminal makes the switch. Auto-hold and auto-clear monitor ongoing activity, and an audible alarm signals when a console screen has been altered, requires data entry, or has a full buffer. Lease price is $4000; monthly license plan is available. Also shown will be the Westi/CICS interface program. This program allows users to access online application programs that have been written in command level Cobol for IBM's CICS. And, the Disk Space Manager Version 7 supports multiple CPUs in VM or a real shared DASD environment. **Westinghouse Electric Corp, Advanced Systems Technology,** 777 Penn Center Blvd, Pittsburgh, PA 15235.

**Booth C3872** **Circle 338**

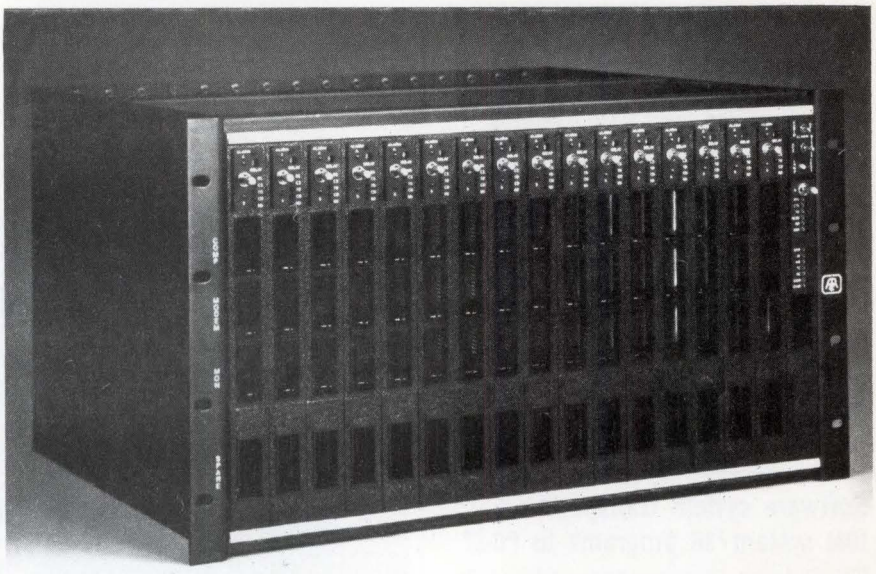
## Database system mixes applications with performance

Unify, a Unix-based relational database system, combines fourth-generation application development facilities with high performance. Applications can be developed without programming, thus increasing productivity. Functions include interactive data entry, ad hoc queries, report writer, database updates, and database load/unload. Ease of use results from the underlying relational data model, full-screen, and menu-oriented user interface. All Unify tools are menu driven; the menu command line can be used as a command interpreter. **Uniq Digital Technologies,** 28 S Water St, Batavia, IL 60510.

**Booth B4010** **Circle 339**

# DATA COMMUNICATIONS

## Network test systems cover datacomm areas



The NTS all-circuit Alarm System offers full-time circuit fault alarming. Local or remote CRT provides user-selectable alarm parameters for each circuit. The NTS Trouble Ticket and Management Report System have a large data base to store, coordinate, analyze, and present alarm conditions. Critical data can easily be obtained on specific circuits. NTS Distributed Remote Site System allows interconnection of up to 16 NTS equipment sites. Any site can access and test any other site through the master site. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

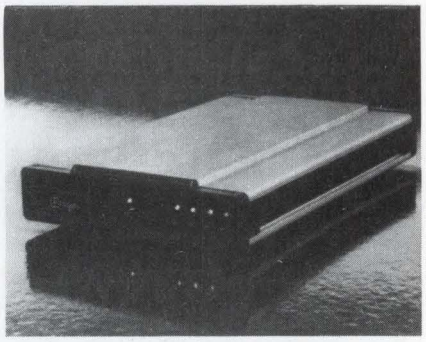
**Booth B4138** **Circle 340**

## Distributed processing system allows file access

Any 8-bit IBC computer can be connected to any other 8-bit IBC computer through the distributed oasis processing system (DOPS). Thus, the user can access other systems' files on a system level. DOPS utility requires only a 20-Kbyte memory. Network communication interface consists of memory, plus a serial port from each computer with serial interface operating at speeds to 38.4-kbaud for high speed data transfer. Also shown will be 8- and 16-bit Oasis, Middi Cadet, and high performance Middi Cadet systems. **Integrated Business Computers,** 21621 Nordhoff St, Chatsworth, CA 91311.

**Booth D4128** **Circle 341**

## Modem performs as data comm system



The Smartmodem 300 directly connects to RS-232-C compatible computers or terminals and can be program controlled in any language by ASCII character strings. Device capabilities include auto-dial and auto-answer. The 300-baud unit, is priced at $289 and comes with a power pack and modular telephone cable. Intended for use with the IBM PC and Smartmodem 300, 1200, and 1200B models, Smartcom II communication software allows automatic log-on to remote systems. Information that is often rekeyed can be stored in macros, while special keys that stop and start incoming data capture permit selective storing and printing. The program requires an 80-col monitor, one disk drive, 96 Kbytes of RAM, an asynchronous communication card, and DOS 2.0, 1.10, or 1.00. Estimated price is $149. Smartcom II packages for the DEC Rainbow 100, Xerox 820-II, and Kaypro II are available, as is a Hayes Terminal Program for Apple's II Plus, IIe, or III computers. **Hayes Microcomputer Products, Inc,** 5923 Peachtree Industrial Blvd, Norcross, GA 30092.

**Booth H802** **Circle 342**

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CIRCLE 87

# SYSTEM ELEMENTS

## Two-axis joystick has only 3/8-in. diameter

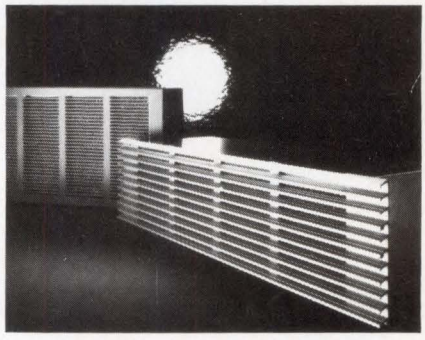
Model 462 subminiature, force-operated joystick requires less than one half inch of back panel space. The two-axis stick gives 1.1-V full-scale output in both X and Y with a 200-Ω source impedance when 500 V are applied. Model 621 Trackball, low profile unit fits into tight locations without sacrificing quality. Features include a 1½-in. diameter ball in a 3- x 3-in. case. Unit requires a single 5-Vdc supply. **Measurement Systems, Inc,** 121 Water St, Norwalk, CT 06854.
**Booth B3906** **Circle 343**



## Precision pin tractors have replaceable belt and tooling

Two 6- and 8-pin super precision, long life pin tractors can position the pin to ±0.0005 repeatably. OEM packages are available for bidirectional forms feeding with double-lid tractor operations. A single-lid bidirectional form system eliminates 30 to 40 in.-oz of form torque. Also available will be a 7-pin, high speed printhead to integrate into printers. **Precision Handling Devices, Inc,** 63 S Main St, Assonet, MA 02702.
**Booth A1820** **Circle 344**

## Variable speed blowers feature quiet operation



The line of BDS5 and BDS8 blowers achieves maximum SCFM air delivery with quiet operation. Offered as complete panel-mounted assemblies, BDS5 and BDS8 include built-in variable speed controls, motor overload, prewired selection of 3- or 6-ft cords, and a reusable filter. An optional air deflector is available. **AMCO Engineering Co,** 3801 N Rose St, Schiller Park, IL 60176.
**Booth B3916** **Circle 345**

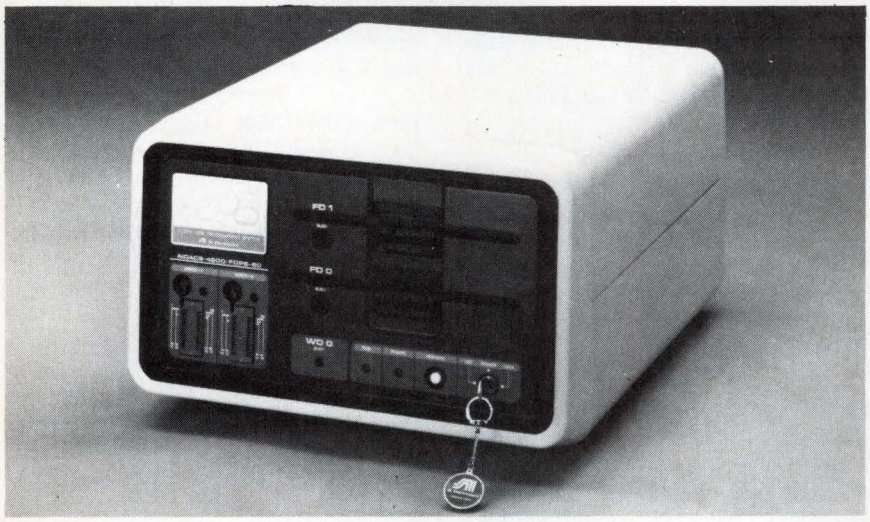
## Data streamer heads designed for disk backup

Cassette data streamer heads for Winchester disk backup are designed for use in .15-in. data cassettes. Heads contain 2-channel, 4-track read/write with full track erase mechanical format. Head contour is designed for tape speeds up to 90 in./s, and ensures head to media contact and forward to reverse amplitude variations of 20 percent maximum. Total capacity on 450 ft. of .15-in. tape is 20 Mbytes unformatted. **Nortronics Company, Inc,** 8101 Tenth Ave N, Minneapolis, MN 55427.
**Booth C3414** **Circle 346**

# NCC PRODUCT PREVIEW

## TEST & DEVELOPMENT

### Support systems aid 16-bit micro development



To support 16-bit microprocessor systems, the FDPS-60 series main host unit and associated in-circuit emulator ICE86/88 series products are available to developers of software, hardware, firmware, and integrated systems. The FDPS-60 comes standard with dual-floppy drives; model FDPS-60W comes with an added 5¼-in. Winchester drive. The host system uses a multiprocessor 5-MHz structure with 8086, 8087, and 8089 chips. DRAM is 512 Kbytes; ROM is 16 Kbytes. Six serial I/O ports (RS-232-C) are available, along with a Centronics-compatible parallel I/O port used as printer interface. The ICE86/88 is a standalone in-circuit emulator with emulation pod for 8086 or 8088. It can be used alone with a CRT terminal and independently or jointly with a host computer such as the FDPS-60. Entire memory space is 1 Mbyte; 64 Kbytes is for I/O. Up to 10-MHz realtime emulation is provided. Delivery of both products is one month ARO. **Ai Electronics Corp,** 2-28-16 Shimomaruko, Ota-ku, Tokyo 146, Japan.

**Booth B4527** **Circle 347**

### Test equipment provides increased speeds

Analog test equipment (ATS) gives an increase in testing speeds of 8 to 10 times over digital testing techniques. Flow map information can be written on the disk drive after testing. Test parameters are user-selectable; test sequences are pre-selected and pre-programmed. **Applied Circuit Technology,** 2931 La Jolla St, Anaheim, CA 92806.

**Booth H204** **Circle 348**

### System runs automatic final tests on Winchesters

The Model DX525AT/S computer-based, automatic test system performs a comprehensive final test on up to 32 Winchester disk drives, while logging and analyzing results. The system runs a series of tests on ST506-type drives simultaneously, independently, and asynchronously. Included in the system are a central console with IBM PC/XT, floppy disk and printer, and up to four test bays of eight testers each. Entry of variable information is through a hex keypad terminal at each bay of testers. System console is 55 x 35 x 34 in., each test bay is 20 x 30½ x 57¼ in. Power may be 115 Vac or 230 Vac. System is $43,050 for a console and one test bay. Delivery is 60-day ARO. **Applied Memory Technology,** 2822 Walnut Ave, Tustin, CA 92680.

**Booth C4089** **Circle 349**

# NCC PRODUCT PREVIEW

**ANN ARBOR TERMINALS, INC,** Ann Arbor, Mich—Ergonomic enclosures and serial keyboards are added to the ANSI standard graphics terminal family. Members include the Genie, Genie + Plus, Ambassador, and Guru.
**Booth A1826**

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**APPLIED MAGNETICS CORP,** Goleta Calif—Line of magnetic heads for tape drives, rigid disk drives, and floppy disk drives will be presented.
**Booth A1322**

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**APPLIX, INC,** Southboro, Mass—Next-generation integrated office software system combines advantages of PC software with the sophisticated communication capabilities of traditional office automation systems.
**Booth C3464**

---

**CIPHER DATA PRODUCTS, INC,** San Diego, Calif—The high performance group code recording M990 tape drive uses cache technology. This unit, which is the first in the GCR CacheTape product line, features error free interface with outboard defect management and 180-Mbyte storage capacity.
**Booth C4118**

---

**COMPUTER COMMUNICATIONS, INC,** Torrance, Calif—Group 8000 communication cluster products include the 8274 C remote cluster controller, 8178 display station, and 8287 printer station. Also displayed, the CC-8 enhanced emulation processor is a plug-compatible replacement for IBM 270X/370X frontend processors, as well as 3704/3705 controllers that operate in emulation mode.
**Booth H118**

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**DATA SPECIALTIES, INC,** Northbrook, Ill—Zebra demand printer produces bar code product IDs and alphanumerics on shipping labels, tickets, or tags. It uses RS-232-C serial interface and communicates in ASCII code.
**Booth B3528**

---

**DIGI-DATA CORP,** Jessup, Md—Model 70 PC offers high performance data storage and retrieval, as well as Winchester hard disk backup for the IBM PC. Series 6400 and 8300 quarter-inch cartridge tape drives are available in both unidirectional and serpentine head versions. Series 2000 half-inch streaming tape drives are offered in 100- and 125-in./s version for 1600 bits/in.
**Booth C4126**

**DISTRIBUTED LOGIC CORP,** Garden Grove, Calif—Product line consists of disk and tape controllers that interface a variety of Digital Equipment Corp operating systems. Line includes model DQ342 quarter-inch magnetic tape coupler, as well as DQ619 5¼-in. and DQ419 8-in. floppy disk controllers.
**Booth C4221**

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**DRANETZ TECHNOLOGIES, INC,** Edison, NJ—Modem cartridge addition allows telephone line access for the series 626 remote monitor unit. This instrument measures power line disturbances in a wide range of applications.
**Booth A1404**

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**FCM PLASTICS, DIV OF PLASTIC TECHNOLOGIES INC,** Grand Rapids, Mich—FCM-CS electroless plating provides effective shielding. It protects the environment from EM radiation while allowing use of mold-in-color parts.
**Booth A2110**

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**FUJI PHOTO FILM U.S.A., INC,** New York, NY—Double-sided, double-density 8-in. floppy disk performance is achieved in new 1.6-Mbit, 5¼-in. model.
**Booth B3315**

---

**GAVILAN COMPUTER CORP,** Calif—Mobile computer holds built-in 3½-in. disk drive and comes in 8- and 16-line LCD versions.
**Booth D3932**

---

**GIMIX, INC,** Chicago, Ill—A 15-user C language development system, the 6809 CPU III, performs high speed DMA transfers using memory attributes and illegal instruction trapping to protect users from program crashes. Intelligent serial I/O boards reduce system overhead and allow 19.2-kbaud terminal operation. The C compiler runs OS-9, a multitasking, multi-user, Unix-like system.
**Booth B4016**

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**HOUSTON INSTRUMENTS,** Austin, Tex—New DMP-51 plotter combines 22 in./s high speed, 4 G acceleration, and 0.025-mm (.001-in.) resolution. Plotter is compatible with DM/PL software programs; produces C- or D-size drawings.
**Booth A1334**

---

**IBEX COMPUTER CORP,** Chatsworth, Calif—Compact and intelligent, the PCT-1000 is an IBM-format compatible, 9-track streaming tape drive. The unit provides up to 138-Mbyte backup for Winchester hard disks, read/write access to archival data banks, and intercomputer data exchange.
**Booth A2126**

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**IOMEGA,** Ogden, Utah—Alpha-10, Beta-5, Bernoulli box—high performance cartridge disk drives featured.
**Booth A1714**

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**ISOREG CORP,** Littleton, Mass—Single-phase Isoguard UPS provides stable power within ±2 percent of correct voltage when power line voltage deviates ±10 percent from normal. Units range from 300 VA to 10 kVA.
**Booth B4015**

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**KMW SYSTEMS CORP,** Austin, Tex—Coaxial interface adapter allows attachment of devices to all IBM 3270-type controllers; VP-10 controller, which features 200,000 vector capacity, connects mainframes to low cost raster output devices.
**Booth C3630**

---

**LIEBERT CORP,** Columbus, Ohio—A computer room installable UPS system, the Programmed Power Center, is available for 50- to 200-kVA loads. The system offers low weight, compact design, and quiet operation.
**Booth A1722**

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**LORTEC POWER SYSTEMS,** North Ridgefield, Ohio—UPS provides reliability (more than 140,000 hr MTBF) while using delta magnetic regulation technique for 3-phase power generation.
**Booth A1009**

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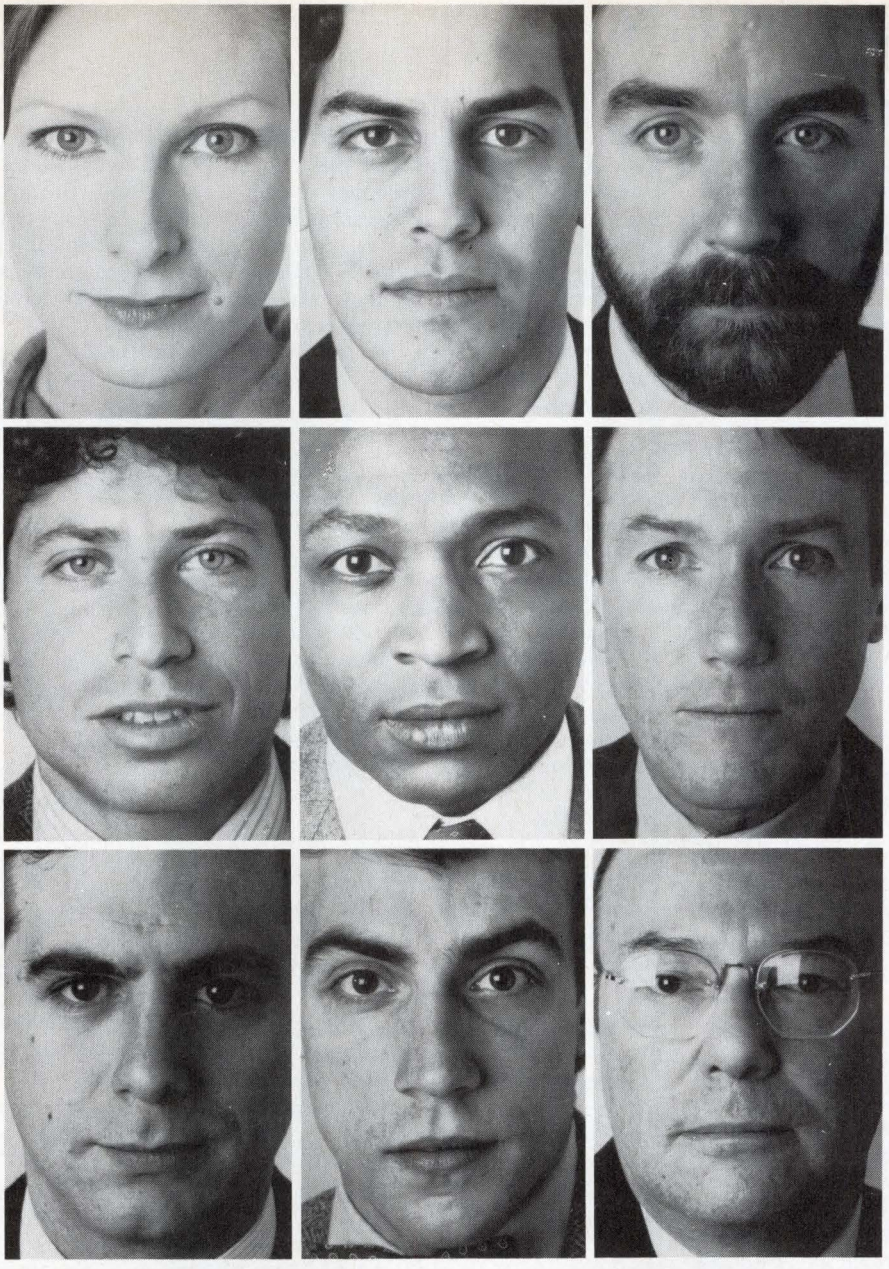
**MAXTOR CORP,** San Jose, Calif—The XT-1000, XT-2000, and XT-4000 5¼-in. disk drive families use Whitney-type head sliders and flexures to allow high density recording with greater stability and margins. Space saving miniature surface-mounted circuit components allow a single MAXPAK PC board for improved reliability.
**Booth D3038**



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CIRCLE 90

**MEMTEC**, Salem, NH—Companion models 410, 420, and 440 miniature reel-to-reel tape drives back up Winchesters, offering 10-, 20-, and 40-Mbyte capacity, respectively. Integral tape guide design eliminates belts, rollers, capstans, and cams. Models fit the same half-height form factor as 5¼-in. Winchesters and minifloppy drives.
**Booth A1428**

---

**MICOM SYSTEMS, INC**, Chatsworth, Calif—Micro7400 protocol converter provides a communication path permitting up to 12 asynchronous terminals to access IBM mainframes. To the host, the Micro7400 appears as an IBM 3274 Model 51C cluster controller communicating in either the bisync or SNA/SDLC protocol.
**Booth C3118**

---

**MICRO SWITCH, DIV OF HONEYWELL**, Freeport, Ill—The programmable display pushbutton (PDP) projects images through 560 LEDs on a 1.5-in.$^2$ dot matrix. This I/O device simplifies control panel functions in aerospace, process control, industrial, and other applications.
**Booth C3598**

---

**MICRO-TERM, INC**, Fenton, Mo—TWIST terminal displays data in both 60-col x 24-line "landscape" and 80-col x 72-line "full page" formats. Dual-format is achieved via CRT screen that rotates 90 degrees. Characters automatically reorient in less than a second. The terminal's native mode is ANSI 3.64.
**Booth C3946**

---

**MOSTEK CORP**, Carrollton, Tex—New 16-bit single-chip MK68200 microcomputer configures as an embedded standalone controller in single-chip mode or as an intelligent peripheral controller in expanded bus mode. The MK68200 provides full-duplex USART with data rates up to 1.5 Mbits/s.
**Booth A2066**

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**NICOLET COMPUTER GRAPHICS DIV, NICOLET ZETA CORP**, Martinez, Calif—Zeta 822 plotter provides 0.025 mm (0.001 in.) resolution graphics for both continuous feed and cut sheet media; plotter attains high throughput using eight pens on one microcomputer-controlled carriage.
**Booth A1836**

**OAK SWITCH SYSTEMS, INC**, Crystal Lake, Ill—Low profile full-travel membrane (FTM) keyboard uses new rocker mechanism design that reduces operator fatigue. FTM keyboard can be placed in enclosure and still meet the 30-mm DIN standard. Operating voltage ranges from 1 to 30 Vdc and operating currents span from 50$\mu$A to 20 mA per single switch, resistive load.
**Booth A2057**

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**ONYX SYSTEMS**, San Jose, Calif—Series 186 16-bit microcomputer system is based on iAPX 80186 CPU. It offers 256 Kbytes of dynamic parity RAM (expandable to 768 Kbytes), and supports up to six simultaneous users. Onyx implementation of Concurrent DOS and PC Mode are among the operating systems available. Cobol, Basic and C languages are supported. Ergonomically designed terminal sports 14-in. nonglare screen and 104 sculptured keys arranged on three key pads.
**Booth D3238**

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**PERKIN-ELMER**, Oceanport, NJ—System V available for full line of superminis and workstations.
**Booth A1122**

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**PERTEC PERIPHERALS CORP**, Chatsworth, Calif—Vindicator FS1000 half-inch streaming tape drive incorporates firm's microformatter interface standard, which is plug-compatible with widely available controllers. An 8-in. fixed disk drive will also be displayed.
**Booth C4398**

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**QUANTUM CORP**, Milpitas, Calif—Both 5¼- and 8-in. Winchester disk drives available.
**Booth H734**

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**QWINT SYSTEMS**, Northbrook, Ill—Teleprinter includes 80-col, dot-matrix typing unit, full ASCII keyboard, standard RS-232 serial interface, and optional built-in modem. Intended for peripheral and telecommunication applications; signal speeds offered range from 110 to 1200 baud.
**Booth B4432**

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**RENEX CORP**, Springfield, Va—Twinax connected protocol converter links ASCII devices to System 34, 36, and 38.
**Booth B4027**

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**SEITZ TEK**, Torrington, Conn—Combining a sheet feeder and bidirectional tractor drive in one mechanical unit, the ST-150 paper feeder features antibacklash drive for accurate print registration and holds up to 150 sheets in sizes up to 14 x 14 in.
**Booth B4038**

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**SGS SEMICONDUCTOR CO**, Phoenix, Ariz—Samson 32/16-bit virtual memory computer system is marked by dual-port memory, Multibus compatibility and uses SGS's port of Unix System III with Berkeley enhancements. Virtual memory processor provides 16-Mbyte addressing range. Distributed microprocessors are featured with DMA for all I/O, disk, and magnetic tape controllers.
**Booth D4522**

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**SIDEREAL CORP**, Portland, Ore—The Micronet Desktop store-and-forward message switch accommodates up to 24 ports. This modular system is available unbundled or as a hardware/software package. The Micronet 85 multi-user system features an icon-based user interface with six global commands for simple operation.
**Booth H318**

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**SOLA ELECTRIC, A UNIT OF GENERAL SIGNAL CO**, Elk Grove Village, Ill—Power protectors, including a new SPS and two UPS, will be presented. New UPS offerings include a 1-kVA model available as a 120 V, 60-Hz model and a 220/240 V, 50-Hz model.
**Booth A1604**

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**SYQUEST TECHNOLOGY**, Fremont, Calif—Removable 5-Mbyte formatted, and fixed 10-, 20-, and 30-Mbyte formatted Winchesters feature 3.9-in. graphite coated thin-film metallic alloy disks and use 5¼-in. controller interfaces without modification.
**Booth H910**

# NCC PRODUCT PREVIEW

**TELPAR, INC,** Addison, Tex—A data communication tester, the DCT-100, provides industry standard RS-232-C breakout panel with the ability to print the received or transmitted data stream on an integral, 20-col thermal printer.
**Booth C3418**

---

**3M,** St Paul, Minn—Micrapoint II computer-assisted micrographic retrieval system capacity has been expanded through the addition of a rigid disk module. Containing a 70-Mbyte unformatted disk with a net record storage capacity of 40 Mbytes, the module houses a quarter-inch streaming tape cartridge for backup.
**Booth C3542**

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**TRI-DATA,** Mountain View, Calif—Netway 274 cluster controller connects various incompatible workstations, peripherals, and hosts. Each controller supports up to 16 workstations connecting up to 5 multipoint and 16 point-to-point host connections. The 274 supports IBM 3270 BSC and SNA/SDLC, Burroughs Poll/Select, and asynchronous start-stop protocols.
**Booth D3203**

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**UVP, Inc,** San Gabriel, Calif—Memorase EPROM erasers include the C-25, C-50, C-91, and C-90. Also available, the 4-W desktop DE-4 can erase 8 EPROMs within a 15 min span
**Booth B3727**

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**VERMONT RESEARCH CORP,** North Springfield, Vt—Removable hard disk subsystem aims at Multibus configurations. Based around the 10-Mbyte model 8520, 8-in. fixed/removable hard disk drive, the subsystem is designed for Intel System 310 and operates under iRMX 86 or Xenix software.
**Booth D3326**

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**VERTEX PERIPHERALS,** San Jose, Calif—Line of 5¼-in. Winchester disk drives will be demonstrated. These models feature capacities of 30, 51, 72, and 100 Mbytes.
**Booth D3635**

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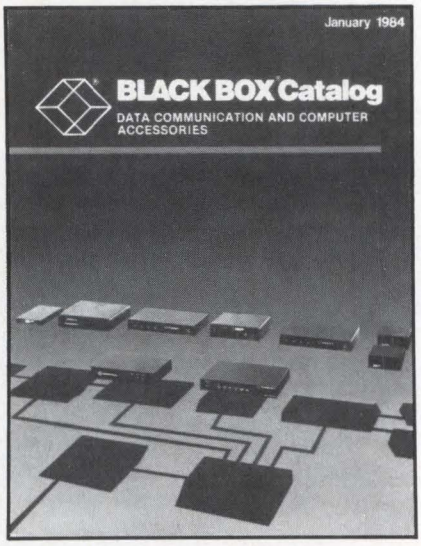
**WINTEK CORP,** Lafayette, Ind—This SMARTWORK printed circuit board editor runs on the IBM PC without special hardware. Single- and double-sided boards up to 10 x 16 in. can be designed.
**Booth A1828**

**ZETACO,** Eden Prairie, Minn—A fully emulating, single-board disk controller, the BMX-1, supports up to four SMD disk drives on Data General's burst multiplexer channel. Onboard switches are eliminated by EEPROMs that allow drives to be configured from the console.
**Booth D3306**

**July Preview**
*Watch for a special article on computer graphics*

### Data communication equipment




Reference book features over 300 products designed for data communication and computer operation; complete description includes photos, diagrams, text, and prices. **Black Box Corp,** Pittsburgh, Pa.

**Circle 410**

### Video boards

Controller boards and video systems catalog is divided into sections covering Multibus, Q-bus, Unibus, STD bus, S-100 bus, and Exorciser bus applications; complete specs, schematics, and photos, along with application notes, are included. **Matrox Electronic Systems Ltd,** Quebec, Canada.

**Circle 411**

### Semiconductor devices

D-A and A-D converters, precision op amps, precision voltage references, analog switches and MUXes, and dual transistors are profiled in 352-page catalog; transistor application notes detail over 25 circuits. **Micro Power Systems, Inc,** Santa Clara, Calif.

**Circle 412**

### Development seminars

Catalog of professional development seminars to help improve performance and productivity covers topics in data communication, CAD/CAM, software engineering, and others; books and videocassettes are also available. **Institute for Advanced Technology, Control Data Corp,** Rockville, Md.

**Circle 413**

### Electronic components

A 64-page, full-color magazine prints articles on the company's electronic components and applications; titles deal with speech/transmission ICs, computer controlled teletext, and fast coprocessors. **Philips Elcoma,** Eindhoven, The Netherlands.

**Circle 414**

### Digital process instruments

Product catalog features over 100 digital process instruments marketed through worldwide distributors; included are automatic process controllers with dual limits, counter process controllers, and flat packs. **International Microtronic Corp,** Tempe, Ariz.

**Circle 415**

### Magentic tape systems

Full-color brochure provides a quick-reference guide to magnetic tape systems and controllers compatible with specific HPIB and GPIB systems; reference chart, performance ranges, and applications are included. **Dylon Data Corp,** San Diego, Calif.

**Circle 416**

### Thick-film materials

Catalog describes such thick-film materials as cermet conductors, resistors and dielectrics, and surface mounting materials; key properties and typical applications are summarized. **Electro-Science Laboratories, Inc,** Pennsauken, NJ.

**Circle 417**

### Scalar network analyzer

Brochure describes family of 10 automated network analyzer systems covering the 10-MHz to 40-GHz range; optical units offer accuracy equivalent to 60-dB directivity, and automatically locate transmission line faults. **Wilton Co,** Mountain View, Calif.

**Circle 418**

### Connectors and accessories

Catalog provides complete data on Cinch connector products, including mechanical, electrical, and environmental specs; comprehensive index cross-lists distribution part with factory part to simplify ordering. **TRW Electronic Components Group, Connector Div,** Elk Grove Village, Ill.

**Circle 419**

### Single-chip data books

Complete technical data for over 100 members of the single-chip microcomputer and 8-bit microprocessor/peripheral families is compiled in shelf reference with master index; a memory selector guide lists all parts available as of late last year. **Motorola Inc, MOS Microprocessor Div,** Austin, Tex.

**Circle 420**

### Optoelectronics catalog

Broad line of LED lamps, along with numeric, alphanumeric, and dot-matrix displays, is detailed in full-color catalog; data includes features, drawings, specs, and selection guides. **International Devices, Inc,** Santa Ana, Calif.

**Circle 421**

### Converting dc-dc

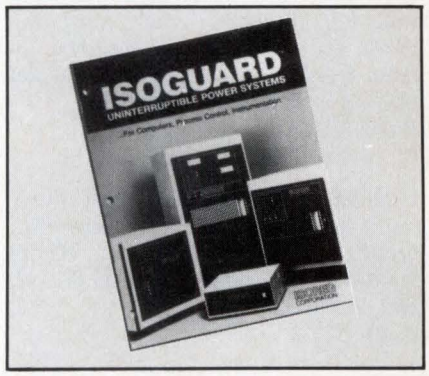
Petit potted power packs that convert computer power to low noise amplifier power are described in data sheet; units are designed for use on plug-in computer peripheral cards and feature over 500-V isolation between input and output. **Calex Mfg Co, Inc,** Pleasant Hill, Calif.

**Circle 422**

### Test equipment

Illustrated buyer's guide cites a range of testers and analyzers, outlining features, specs, and prices. **Sencore,** Sioux Falls, SD. **Circle 423**

### Uninterruptible power systems




Technical literature details Isoguard uninterruptible power systems and summarizes the differences between static and rotary types; spec chart compiles power rating, maximum current, input and output voltages, and battery resume information. **Isoreg Corp,** Littleton, Mass.

**Circle 424**

# CALENDAR


## CONFERENCES

**AUG 2-6—Autofact Japan Conf and Expo** (held conjointly with **Mechatronics**), Osaka, Japan INFORMATION: Leslie Hossack, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0023

**AUG 12-15—Computers in Engineering Conf and Exhibit,** Las Vegas Hilton, Las Vegas, Nev. INFORMATION: Mary Benedict, American Society of Mechanical Engineers, 345 E 47th St, Suite 13M, New York, NY 10017. Tel: 212/705-7100

**AUG 19-24—Technical Symposium on Optics and Electro-Optics and Instrument Display,** Town & Country Hotel, San Diego, Calif. INFORMATION: Rich Donnelly, Information Services, SPIE, PO Box 10, Bellingham, WA 98225. Tel: 206/676-3290

**AUG 21-24—Conf on Parallel Processing,** Hilton Shanty Creek, Bellaire, Mich. INFORMATION: Tse-yun Feng, 1604 Stormy Ct, Xenia, OH 45385. Tel: 614/422-1408

**AUG 30-SEPT 1—Conf on Solid State Devices and Materials,** Kobe, Hyogo, Japan. INFORMATION: Susumu Namba, Osaka Univ, Faculty of Engineering Science, Toyonaka, Osaka, Japan 560.

**SEPT 5-8—Conf on Digital Signal Processing,** Florence, Italy. INFORMATION: A. G. Constantinides, Dept of Electrical Engineering, Imperial College of Science & Technology, Exhibition Rd, London SW7 2BT, England. Tel: 01/5895111

**SEPT 11-13—Midcon Electronics Exhibition and Convention,** Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**SEPT 11-13—Mini/Micro-Southwest Computer Conf and Exhibition,** Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**SEPT 11-13—Voice Input/Output System Applications Conf,** Marriott Crystal Gateway Hotel, Arlington, Va. INFORMATION: Robert Burgess, Public Information Office, Lockheed Missiles & Space Co, Inc, Sunnyvale, CA 94086. Tel: 408/742-6688

**SEPT 16-20—Compcon Fall,** Hyatt Regency Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**SEPT 17-21—FOC/LAN (Fiber Optic Communications and Local Area Networks) Exposition,** MGM Grand Hotel, Las Vegas, Nev. INFORMATION: Michael O'Bryant, Information Gatekeepers, Inc, 138 Brighton Ave, Suite 212, Boston, MA 02134. Tel: 617/787-1776

**SEPT 19-21—Connector and Interconnection Technology Symposium,** Disneyland Hotel, Anaheim, Calif. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

**SEPT 26-28—Eurocon: Computers in Communications & Control,** Brighton, England. INFORMATION: Brian Atkinson, IEE, Savoy Place, London, WC2R OBL England.

**OCT 1-4—AUTOFACT 6 Conf & Exhibit,** Anaheim Convention Center, Anaheim, Calif. INFORMATION: Soc of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

**OCT 2-4—Northcon Electronics Conf & Exhibit,** Seattle Center Flag Pavilion, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**OCT 2-4—Mini/Micro Northwest Conf & Exhibit,** Seattle Center Flag Pavilion, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**OCT 8-10—9th Conf on Local Area Networks,** Minneapolis, Minn. INFORMATION: Harvey A. Freeman, Architectural Technology Corp, PO Box 24344, Minneapolis, MN 55424.

**OCT 8-10—ACM Annual Conf: The Fifth-Generation Challenge,** San Francisco Hilton Hotel, San Francisco, Calif. INFORMATION: Karen Duncan, Chairman, ACM '84, 15 Parsons Way, Los Altos, CA 94022.

**OCT 10-12—Design Automation Workshop,** East Lansing, Mich. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**OCT 10-12—LOCALNET '84,** Sheraton Harbor Island Hotel, San Diego, Calif. INFORMATION: Online Conferences, Inc, Suite 1190, 2 Penn Plaza, New York, NY 10121. Tel: 212/279-8890

**OCT 15-17—The Future of Optical Memories,** Loew's Summit Hotel, New York, NY. INFORMATION: Joanna Spilman, Technology Opportunity Conference, PO Box 14817, San Francisco, CA 94114. Tel: 415/626-1133

**OCT 15-18—Conf on Ada Applications & Environments,** Sheraton Midway Hotel, St. Paul, Minn. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**OCT 16-19—Int'l Test Conf (Cherry Hill '84),** Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**OCT 22-26—Annual Industrial Electronics Conf (IECON '84), on Industrial Applications of Microelectronics,** Keio Plaza Intercontinental Hotel, Tokyo, Japan. INFORMATION: Frank A. Jur, Bechtel Corp, 45 Fremont St, MS 45/17A26, San Francisco, CA 94109. Tel: 415/768-3023

**OCT 30-NOV 1—Wescon Electronics Exh and Conf,** Anaheim Convention Center, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 772-2965

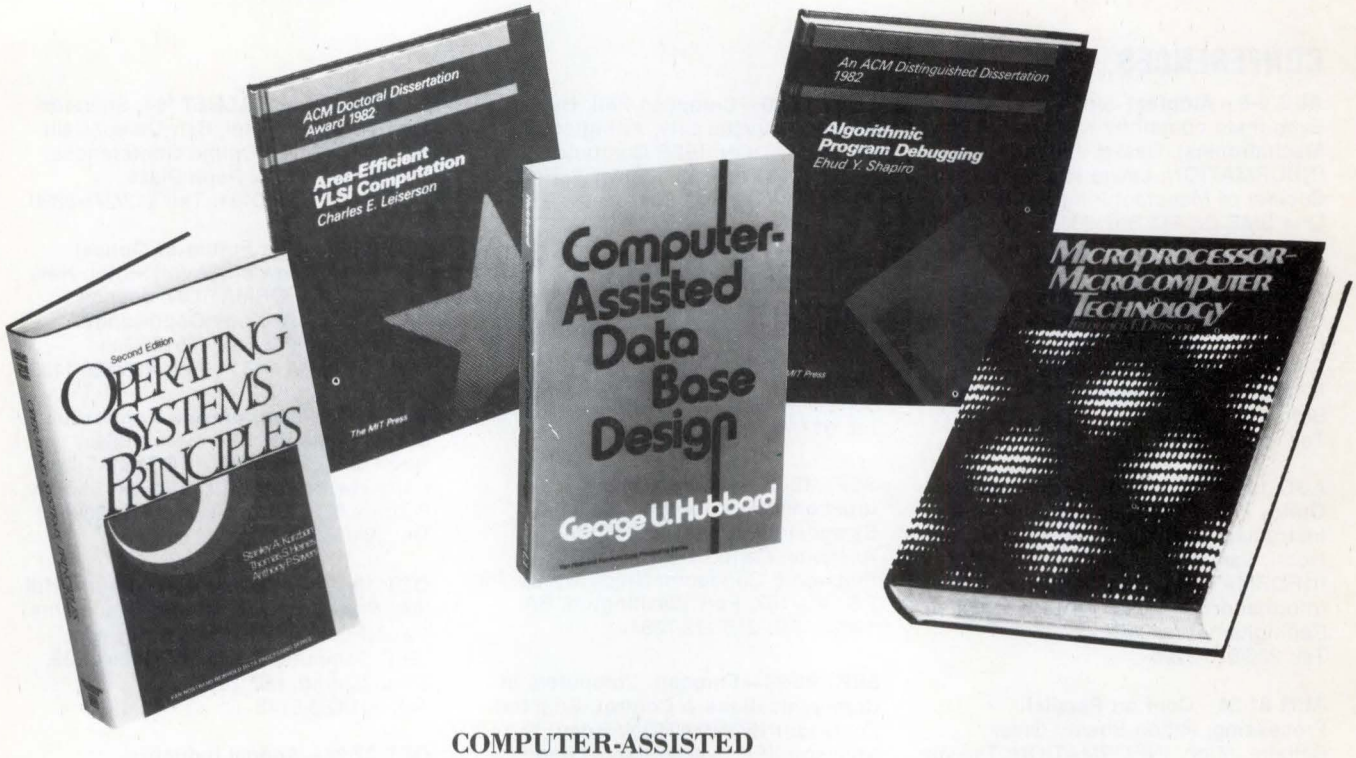
## SHORT COURSES

**Networks & Systems, Software, Digital Processing, Microprocessors, and Man/Machine Systems,** various dates and locations. INFORMATION: Eric R. Garen, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. Tel: 213/417-8888

**Personal Computers, Basic, and Lotus 1-2-3,** various dates, BU campus. INFORMATION: Joan Merrick, Boston Univ Metropolitan College, 755 Commonwealth Ave, Boston, MA 02215. Tel: 617/738-5020

**Robotics, Data Communications, Personal Computers,** various dates, Univ of Michigan campus. INFORMATION: Viola E. Miller, The Univ of Michigan, College of Engineering Summer Conf, Chrysler Center, Ann Arbor, MI 48109. Tel: 313/764-8490

# Designer's Bookcase

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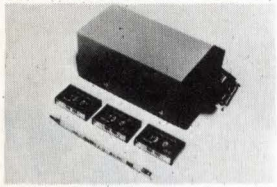

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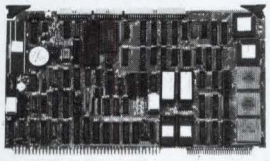

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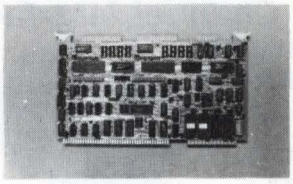

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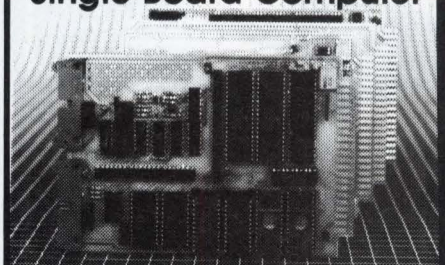

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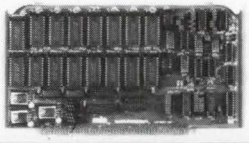

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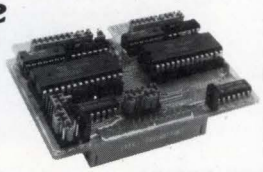

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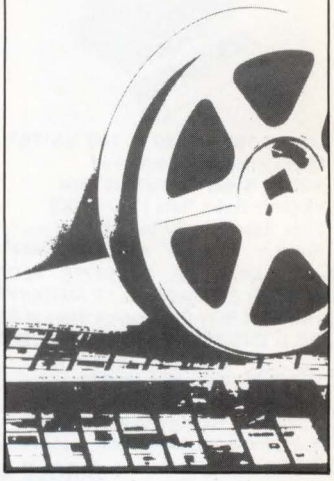
# This Publication is available in Microform.



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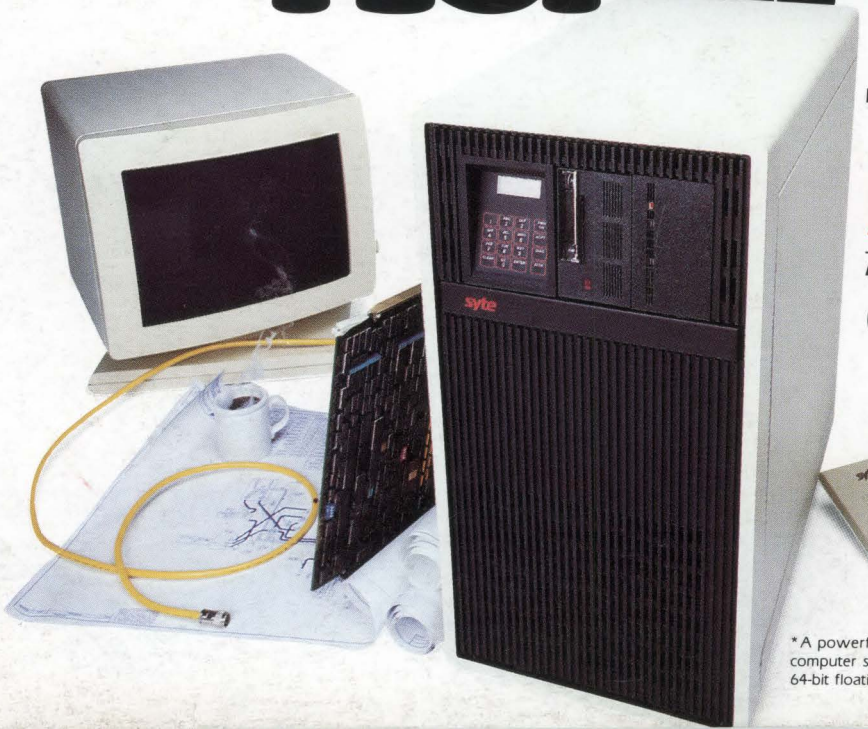


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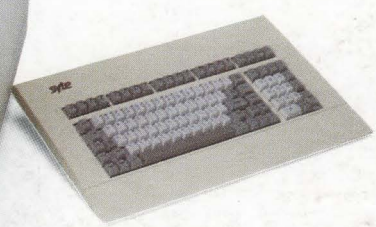


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