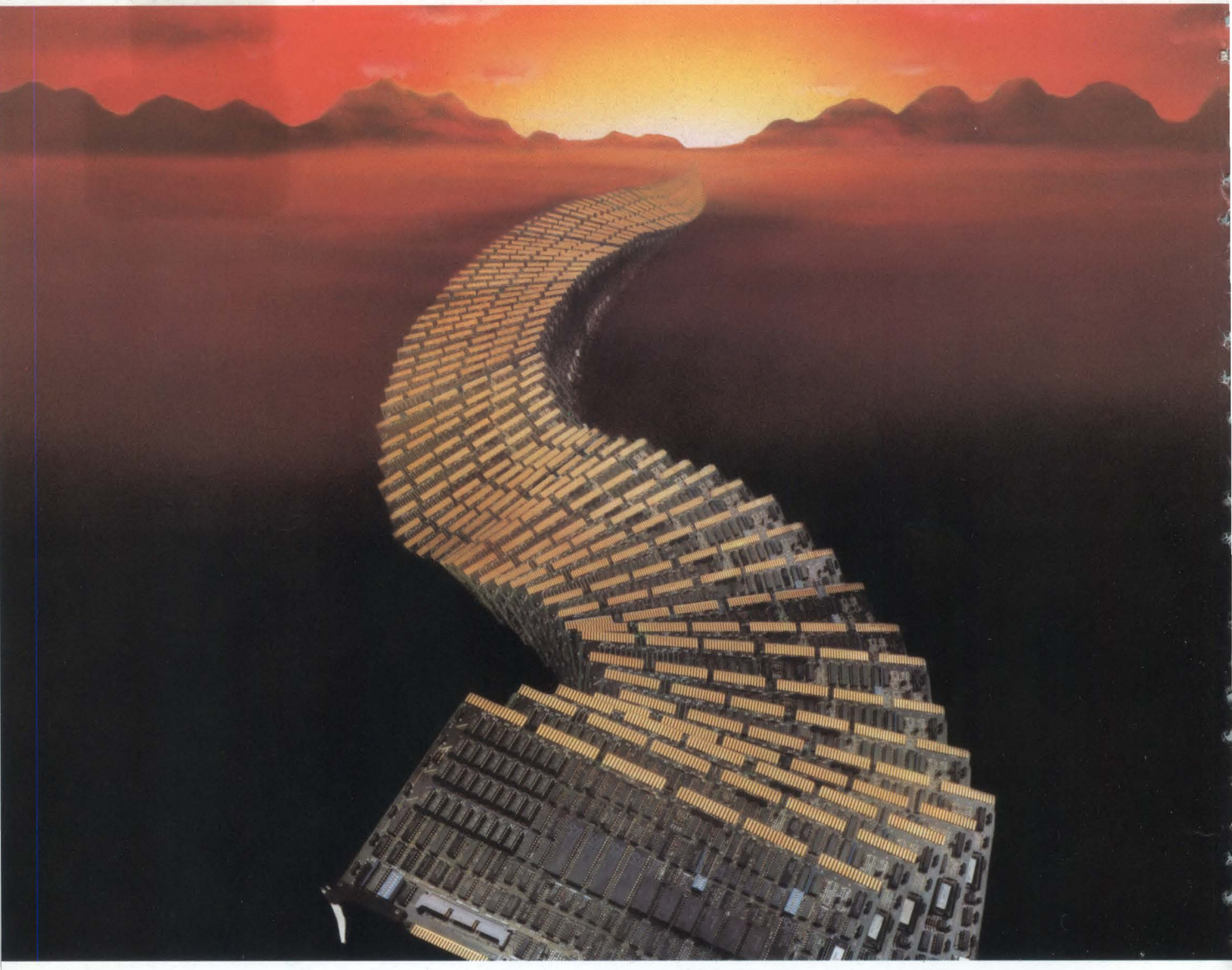
A PennWell Publication

APRIL 5, 1983

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

From out of the West... Leadership in disk controllers



Long recognized as the dominant independent tape controller company serving the minicomputer industry, Western Peripherals has extended this leadership to disk controllers.

The industry measures leadership *by the numbers.* Western Peripherals has the largest installed base of independent peripheral controllers operating in the field today. Products include disk and tape controllers for DEC, Data General and Perkin-Elmer computers. They include controllers for Winchester and removable disk drives, streaming, start-stop and cartridge tape drives. No other supplier has as broad a line.

Western Peripherals makes *the numbers count.* Leadership in performance and reliability. All Western Peripherals controllers have multiple drive support capabiiity and are software transparent to the host computer. All feature extensive self-testing, as well as the industry's highest reliability — *over 45,000 hours actual (measured) MTBF.*

And leadership in product availability, delivery, service and support. Western Peripherals controllers are available either separately or as a complete, fully tested subsystem. They are supported by a full year factory warranty and a national field service organization. In most cases availability is 30 days ARO.

Find out how much our leadership can mean to you.

western peripherals
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Model 6455 Cartridge Tape System

Loaded with Features — Loaded with Benefits.

Kennedy products have always provided innovative new features. And these features have always provided added benefits and convenience for the user. For instance, our Model 6455 offers these features and benefits:

Feature: Start/Stop Operation

Benefit: Drive can emulate a ½" tape drive by providing the ability to perform selective file back-ups, file-restructuring, journaling and software updates.

The drive is effectively a ½" Tape Drive in a smaller package.

Feature: Hard Read Error Spec. of 1 in 10" bits.

Benefit: Best data reliability of any tape cartridge drive. Gives the user confidence in the integrity of the back-up medium.

Feature: On-board Diagnostics

Benefit: Drive can be tested off-line with no test equipment required. Use of S.A. also lowers the MTTR.

Feature: Cartridge Jam Protection

Benefit: Protects the cartridge from damage if cartridge jams. This is accomplished by sensing a current surge and then disabling the motor. Thus insuring that the cartridge will not be damaged.

Feature: High Density Recording

Benefit: Storage capacity of 23 MB on a single cartridge.

By now you can see what we're driving at. Model 6455 is full of unique features and benefits for you. For the complete story, write or call us today.

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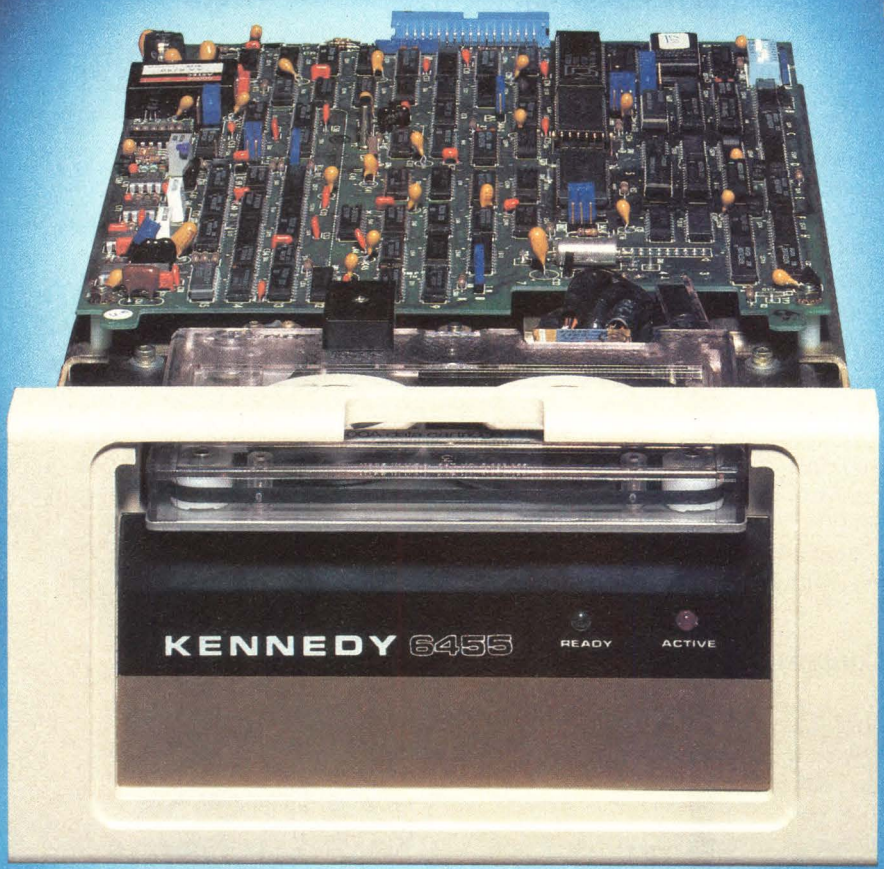

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CIRCLE 2

How You can Cut the Cost of Custom Memory Down to Size.

First, Compare Making Your Own to Buying From Us.

When you make your own, costs can vary. You gamble on finding and keeping experienced memory design engineers. Internal priorities can delay delivery. And your materials come from several sources.

When you buy from us, the price we quote, upfront, is the price you pay. Plus, you get the benefit of more than 10 billion bytes of experience in building memory products with an average of 250,000 hours MTBF. And you get a single product, on time, with a full warranty.

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I'd like more information on your Custom Memory Program.

☐ **Convince Me.**

Enclosed are my immediate Custom Memory Requirements. Please send me a quote.

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Please send me your literature on G.E. Intersil Systems Standard Memory Products.

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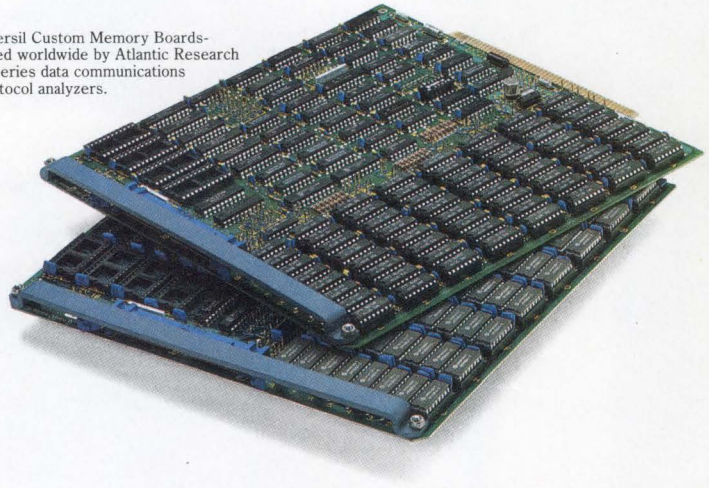

Intersil Custom Memory Boards-Used worldwide by Atlantic Research in series data communications protocol analyzers.

Intersil Systems

Microsystems Division

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CIRCLE 3

UP FRONT

TI microcomputer family to use Seeq EEROM technology

Texas Instruments' TMS7000 family will be the first microcomputer to use Seeq's EEROM technology. Under an agreement between TI and Seeq Technology, Inc, Seeq will develop versions of the 8-bit, single-chip TMS7000 microcomputers using Seeq's 2K x 8, 5-V only, nonvolatile electrically erasable read only memory in place of TI's standard ROM. The resulting EEROM TMS7000 and future versions will be available to TI beginning in 1984.

Functionally and electrically interchangeable with the TI TMS7020, the Seeq 72720 adaptive microcomputer will contain an added program instruction permitting it to program and alter its own nonvolatile program memory. Other features will include twice the amount of internal RAM (256 bytes instead of 128). Additional registers and control logic prevent external access to the internal program memory. The device will have a 13-ms byte write/byte erase.

HP commits to PBXs in future office networks

Agreements between Hewlett-Packard Co and ROLM Corp, Northern Telecom, and Intecom, Inc covering testing and certifications of HP 3000 business computers and HP terminals for interconnection through PBX products, in effect, are committing the computer manufacturer to PBXs for its office networks. HP foresees no conflict between the use of PBXs and the use of LANs based on the IEEE 802 CSMA/CD standard, such as for the HP 9000 32-bit desktop computer.

HP views the PBX as complementary, handling large numbers of terminals and low to medium speed workstations. Further, the twisted-pair distribution method used in PBXs and their ability to handle voice traffic make them well suited for office applications.

Another contender for the sub 4″ floppy disk market

Competing in the 3¼″, 3½″, and 4″ floppy disk market, particularly for the personal computer business, is Maxell Corp of America's 3″ version—the most compact of all. The 3″ disk has a memory capacity of 500k bytes of information on both sides, the same as the compatible, 5¼″ double-density minifloppy disk.

Support for the small disk format, jointly developed by Hitachi, Hitachi-Maxell Ltd, and Matsushita Electric Industrial Co, is provided by 17 American and Japanese companies. As rotation speed, data transfer rate, recording capacity/track, and other specifications are the same as those for the 5¼″ disk, 3″ drives can be substituted.

Agreement on streaming quarter-inch cartridge tape drives

QIC-24, a proposed recording format standard for quarter-inch streamers that permits recorded media interchange, has been agreed to by six manufacturers: Archive Corp, Cipher Data Products, Inc, Data Electronics, Inc, Qantex Div of North Atlantic Industries, Inc, Tandberg Data A/S, and Wangtek. ADES, Apollo Magnetics Corp, Kennedy, Nortronics Co, and Systech Corp were observers; committee members Irwin Magnetics, Inc and Sankyo Sieki Manufacturing Co were not present for the agreement.

UP FRONT

Pretriggers

More than nine times the storage capacity previously available on the IBM Personal Computer is now provided on the XT version. Each XT system has 128K bytes of RAM, 40K bytes of ROM, a dual-sided 5¼" diskette drive (368k bytes), and a 10M-byte fixed disk drive (also 5¼"). RAM is expandable to 640K bytes; other diskette drives can be added.

Two low cost, fully portable logic analyzers that provide 16 or 32 parallel channels of data acquisition at up to 50 or 20 MHz, respectively, have been added to the Tektronix Design Automation Div line. A joint design of Sony and Tektronix, both the 318 and 338 offer state and timing with optional serial state and character analysis.

An integrated voice and data terminal that permits access to computerized information resources and electronic mail systems via video screen and keyboard has been introduced by Northern Telecom. The SL-1 Displayphone is intended for use with the SL-1 digital business communication system.

Serial I/O protocols and electrical interfaces of the MPA-2000 communications controller from Metacomp, Inc can be altered for varying applications. Any of four full-duplex DMA channels supports SNA/SDLC, HDLC, or X.25 protocols, and RS-232 or -422/423 interfaces.

Programmers can switch from editing to computing program modules on the SoloSystems single-user/multitasking workstation. Two MC68000 microprocessors handle CPU and display control functions.

Development and application tools for robotic systems, including manipulator arms, controllers, and software, are being offered in a joint venture of Machine Intelligence Corp and Yaskawa Electric Co. Machine vision can also be added.

Low cost color terminals and an ink jet color raster copier are among graphics products being introduced by Tektronix. A high end terminal features 1280 x 1024 fixed resolution and a 32-bit coordinate space.

Bit-mapped graphics can be added to color and monochrome displays via two controller chips, the SCN2674 and SCB2675, introduced by Signetics.

Both artificial intelligence and CAD, as well as other applications requiring large scale problem-solving applications, are targets for a Lisp based computer system introduced by Symbolics. Compared to similar superminicomputers, the dedicated single-user model 3600 is said to offer significant price/performance advantages, and can deal with massive intelligence programs that previously could only be handled on mainframes. Based on the Lisp language, its software environment also extends the size of a problem that a designer can solve.

Trace record acquisition at up to 20 MHz can be accomplished synchronously or asynchronously with a 32-channel logic analyzer/emulator from Advanced Digital Technology. The model 4009A supports all Motorola 6809/E microprocessor versions and combines features of both a logic analyzer and an in-circuit emulator.

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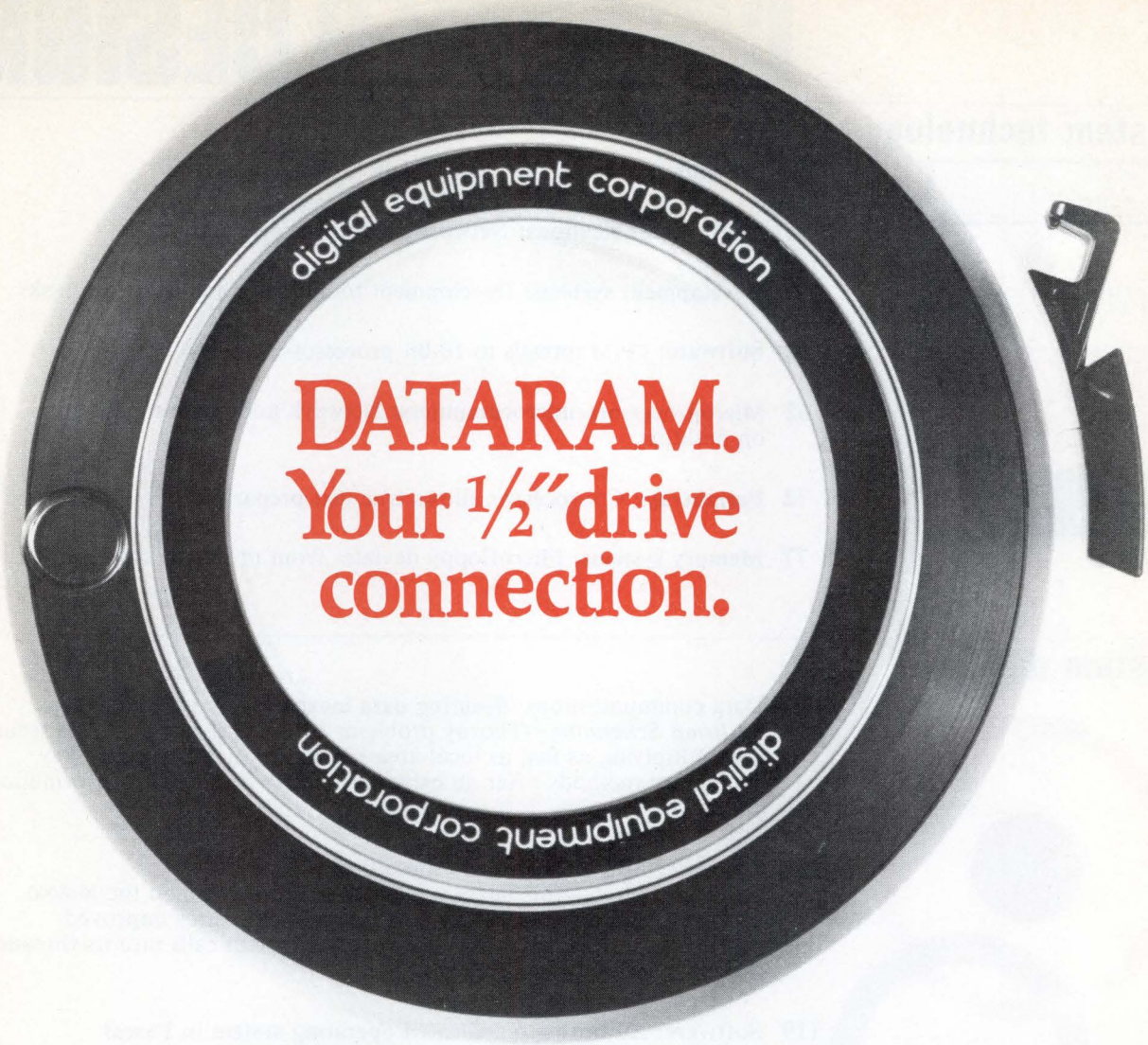
BPA
ABP



It's easy to interface your ½" drive to a DEC computer. When you have connections.

Dataram provides tape drive connections to your host LSI-11, PDP-11, or VAX computer, with a family of couplers/controllers that operate in NRZI, PE, or GCR modes. Dataram's couplers/controllers operate with ½" tape drives from all major manufacturers. As slow as 25 ips — or as fast as 125 ips. 200 BPI to 6250 BPI. With TM11 and TS11 emulations.

Start-stop or streaming. Efficient streaming is supported by a unique RSX-11M utility, FASTSAVE-11M, which provides optional backup and save capability for Dataram's streamer coupler. A full one-year warranty is standard.

For more information about ½" drive connections, call (609) 799-0071. We'll help you make the connection you need!

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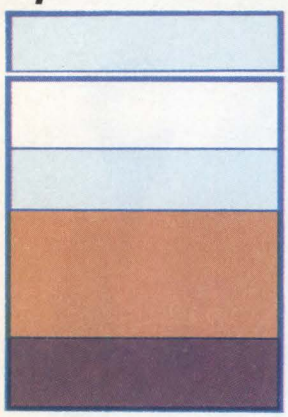
DATARAM

CIRCLE 4

COMPUTER DESIGN®

System technology



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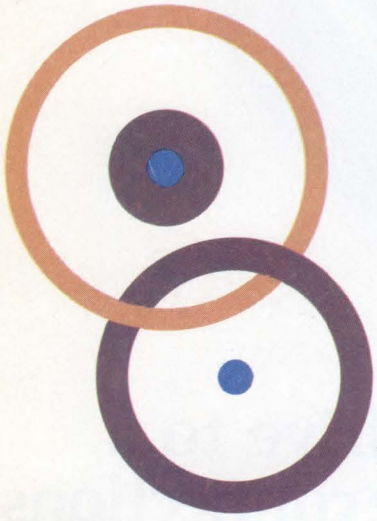
System design



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SID '83

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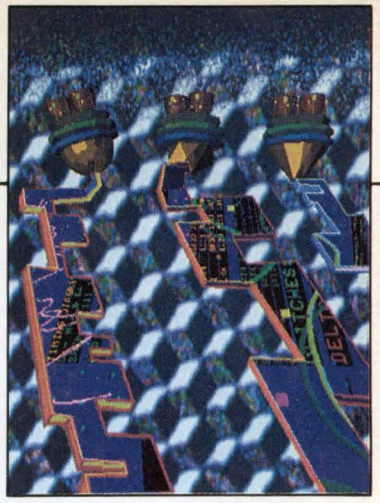

This month's cover, entitled "Timing Diagram," was created by Mark Lindquist and Joe Pasquale.

Special report on systems development and testing

System components

Departments

Designers' preference survey*

*Appearing in Domestic issues only

Editorial reviewers for parts of this issue:

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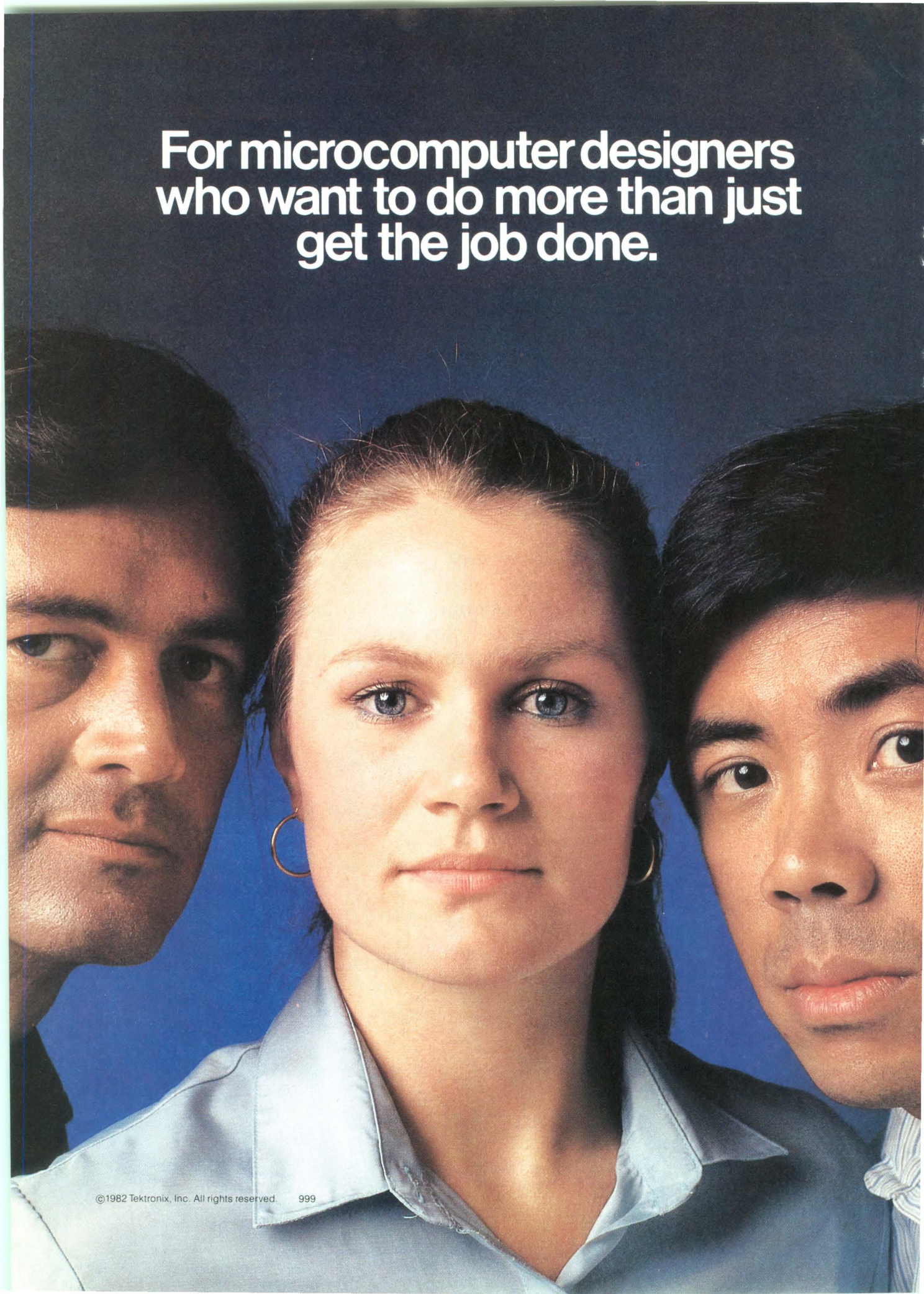
For microcomputer designers who want to do more than just get the job done.
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Tek dedicates the 8500 Series.

Every new generation of processors means skyrocketing code requirements and debugging problems. Today, just getting the job done is a formidable challenge.

But now, Tek's new 8500 Series gives you the best software development and integration tools for better and faster microcomputer designs in all three major design environments: Single-user, Multi-user and Host.

The 8500 Series gives you 16-bit and 8-bit Real-Time Emulation.

16-bit designs can require awesome debugging. But the 8500 Series, with fully transparent Real-Time Emulation, makes absolutely no demands upon your prototype's memory space or interrupt structure. Nor does it impose wait states or stretched clock pulses during program execution.

You no longer have to design around restrictions imposed by your development system.

For real-time debugging, the Trigger Trace Analyzer.

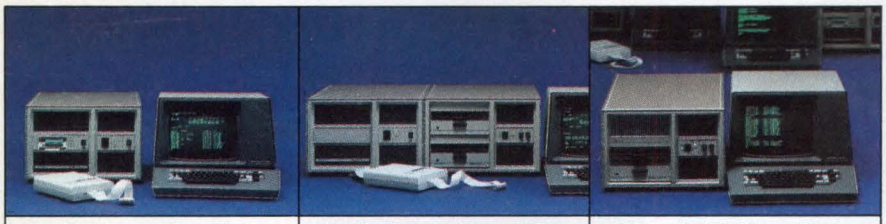
The 8500 Series offers the Trigger Trace Analyzer, a powerful real-time logic analysis option for the 8540 or 8550, which selectively acquires the data you specify so you quickly locate those hard-to-find bugs.

A full set of software development tools and more.

The 8500 Series provides all the standard tools: assemblers, editors, compilers, linkers, loaders and a library generator. It also gives you GUIDE (a friendly interface), a well-organized file system, as well as intelligent command files so you can quickly develop your software.

Complete support for all microprocessor design environments.

The 8540 interfaces with your mainframe computer to extend its software development capability to cover hardware and software integration.



8540 Integration Unit.	8550 Single-User MDL	8560 Multi-User MDL
Develop software on host computer.	Single users develop software with 8500 Series tools running under 8550's DOS/50, with an advanced hierarchical filing system and a friendly user interface.	Multiple users develop software with 8500 Series tools running under 8560's TNIX, a derivation of Bell Laboratories' UNIX** Operating System.
Interface transparently to host computer via ASCII, RS-232 communications ports to debug software with 8540's real-time emulation, with full support for both 8-bit and 16-bit chips.	Debug 8-bit or 16-bit software real-time emulation, using 8550 system resources for I/O simulation.	Debug 8-bit or 16-bit software through high-speed interface with 8540 Integration Unit, which can use 8560 system resources for I/O simulation.
Real-time debugging with Trigger Trace Analyzer. Up to ¼ Mbyte emulation memory.	Real-time debugging with Trigger Trace Analyzer. Up to ¼ Mbyte emulation memory.	Real-Time debugging with 8540's Trigger Trace Analyzer.

The 8500 Series chip support:

16-bit	8-bit		
Z8001	6809	1802	8022
Z8002	6800	6500/1	8041A
8086	6808	8088	3870
68000	6802	8048	3872
TMS9900	Z80A	8039	3874
SBP9900	8080A	8039-A	3876
	8085A	8035	F-8
	8049	8021	

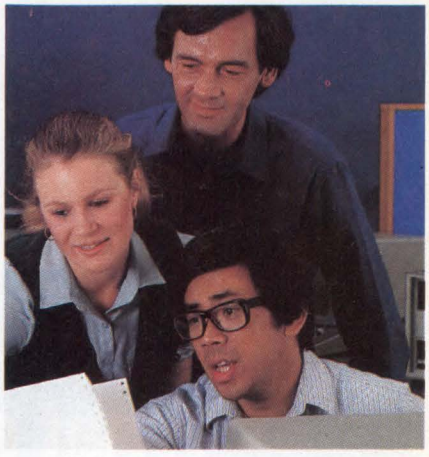
The 8550 offers a complete set of microcomputer design tools in a single desk-top package.

The 8560 is a "team-oriented" multi-user development system. It supports any combination of up to eight software or hardware workstations through an operating system called TNIX*.

Full transportability for planned growth.

Besides getting the job done in the three design environments, the 8500 Series offers migration paths between them.

This built-in hardware and software compatibility maximizes return on capital invested, and minimizes reorientation as people move from one environment to another.



For more information on purchasing or renting the 8500 Series, contact your local Tektronix sales engineer. We'll show you how our products help you get the job done.

And a lot more.

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ACCESS combined with an IBM Personal Computer and a hard disk gives you additional development systems for less than a third the price of Series-III systems. Imagine: a complete development system for just $8,000! Compare this to $28,900 for a hard-disk Series-III system.

ACCESS combined with your Intel software and the IBM PC provides a complete development package. ACCESS provides you with a Series-III operating system simulator (UDI), support for Intel's iSBC-957 debugger, and a data link program for transferring files between the IBM and Intel systems. ACCESS and the IBM PC with a hard disk are also faster than a Series-III with a hard disk.

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CIRCLE 7

PUBLISHER'S PERSPECTIVE

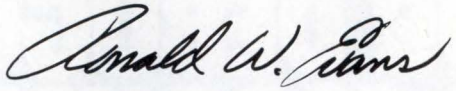
Now is the time

This month, our editors are addressing another important technological market—that of systems development and testing. While reviewing these Special Report articles, the issue of future directions in system design comes up. Will tomorrow's engineers be as creative, enthusiastic, and stimulated as today's? The answer to this question lies not in the intensity of the technological fires but rather in who has the fuel to stoke them.

This country is witnessing the erosion of two important American fundamentals—scientific education and professional opportunity. Today's students are being deprived of the high quality education afforded to the industry leaders and entrepreneurs who have placed the United States at the top of the technological ladder. These students are faced with shortages of qualified teachers, educational funding, and equipment.

Even for those who do make it through the educational obstacle course, our industry is offering fewer ground floor opportunities. Subsidized foreign competition, governmental policies, and increasing regulation are softening financier and venture capital support for emerging technology. Tomorrow's entrepreneurs will be dealing with risk factors beyond their control, unless we act now.

Our industry, and we as individuals, must become more active in supporting higher quality education. At the same time, our industry must come out from behind its veil of naiveté and become involved in geopolitics—otherwise, in 10 years our editors will be discussing what could have been.



Ronald W. Evans
Publisher

MAY PREVIEW

Special Report on Mass Storage Technology
Mass storage is not limited to large systems that hold hundreds of megabytes or even gigabytes of data. The almost insatiable demand for storage capacity is being increasingly met by much smaller systems that provide less than a megabyte. A staff-written article in the May Special Report, therefore, focuses on the smaller storage equipment currently available or being introduced: sub-4″ floppy disk drives.

Other major articles on mass storage include: managing several host CPUs with a shared server . . . Streaming tape drive backup for Winchester drives . . .

National Computer Conference Products
An issue within an issue, descriptions of significant new products that will be shown at NCC '83 will be an important part of May's *Computer Design*.

Gould Millennium

The 9516S Microsystem Integration Station.

If your microprocessor software has been developed on a VAX™ or PDP-11,™ only one emulator lets you download your executable code for total standalone debugging.

The Gould Millennium 9516S Microsystem Integration Station.

It's DEC-compatible so there's no need for software conversion.

Because it's standalone, you leave your host free for other projects, including continual code development.

The fact is, with an RS-232-C interface, you can use the 9516S with *any* host computer or development system.

Multi-Ice™ supports four microprocessors at once.

For debugging multi-processor systems quickly, the 9516S Multi-Ice™ lets you control and monitor any combination of four 8- or 16-bit microprocessors.

Simultaneously. In parallel. And in real-time.

Which means instant hardware communications between microprocessors. Synchronization of program execution. And interleaved display of independent trace buffers.

You can perform logic trace analysis. High speed memory emulation. Complex and super breakpoints.

Built-in procedural language interpreter.

The 9516S procedural language interpreter is a very powerful yet flexible tool derived from the high-level "C" programming language. It offers you a debug environment much like your own high-level programming environment, giving you the option of bypassing assembly language.

During debug and sytems integration, it lets you manipulate and display data, access system resources, and control those resources.

In short, the procedural language interpreter will dramatically increase your effectiveness and productivity.

You can interrogate and make decisions based on real-time information from the 9516S hardware resources. Including software program analysis. Automatic test set-up and execution. Simulation of target hardware. And post-processing analysis.

No more "wait states."

Only the 9516S offers real-time universal emulation *all the time.*

It offers bus cycles as short as 160 ns. Dual bus structures (expandable to 32 bits) provide real-time control and monitoring of independent measurement and debugging tools. Without stopping emulation.

You can set up all your conditions, run at full speed, then check the recording to see what happened.

With the 9516S you can specify up to 8 complex and 4 super breakpoints. Use 80 channel and 1,024 word-deep

FOR DEBUGGING THE µP CODE YOU DEVELOP ON YOUR VAX OR PDP-11, ONE EMULATOR STANDS ALONE.

Clearly the Best.

trace memory for exceptionally qualified logic trace. Or gather information in real-time and display it—while the target system continues to be emulated.

Menu simplifies debugging efforts.

The 9516S is ideal for the experienced *and* occasional user.

Its menu-driven interface lets you start debugging immediately, without having to learn a command language.

You can mix the easy-to-follow menu interface commands with the command language statements to set up specific tasks.

Eight soft keys help you move through the menu and provide fast selection of field options. And when you need help, you can access an on-line user manual for quick reference.

Uncompromising dedication to high performance.

At Gould Millennium, we believe in making every instrument the best for the job it's designed to do.

The standalone capability, procedural language interpreter, multi-processor control and human interface characteristics of our 9516S are evidence of that commitment to excellence.

For detailed application notes or demonstration, write Gould, Inc., Instruments Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279, Gould Biomation and Gould Millennium Products.

For fastest response, call toll-free:
Nationwide (800) 538-9320;
In California (800) 662-9231 or
(408) 988-6800.

The Gould Millennium 9516S Microsystem Integration Station supports *any* combination of 8086, 8088, 68000,* Z8001, Z8002, 68B09/E, 8085A and Z80A microprocessors. It includes a 1 megabyte thinline double-density, double-sided floppy disk drive. Its RS-232-C port lets you interface with any minicomputer for fast, effective software development.

*Introduction in the first quarter of 1983.

CIRCLE 8

COMPUTER DESIGN

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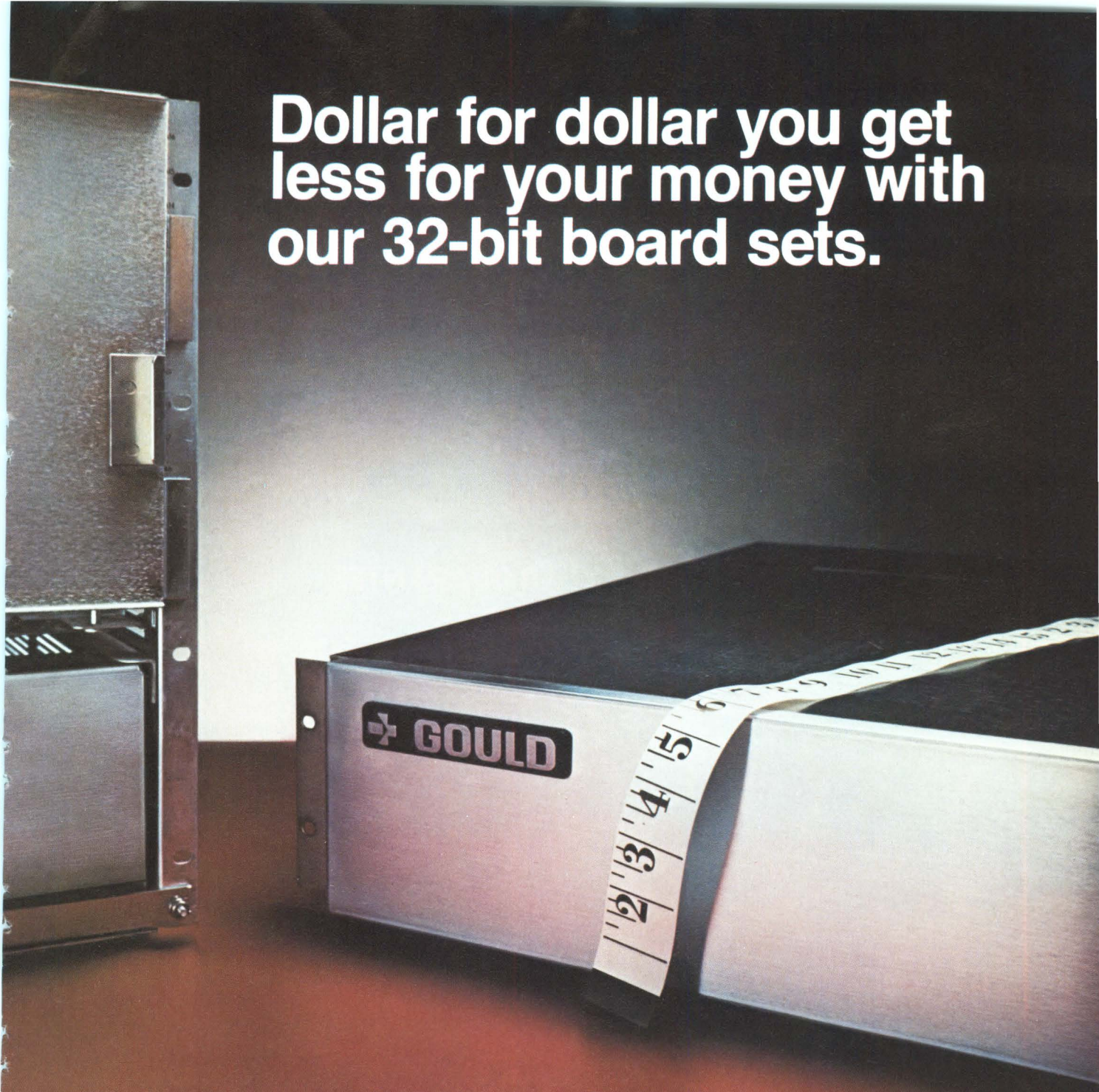

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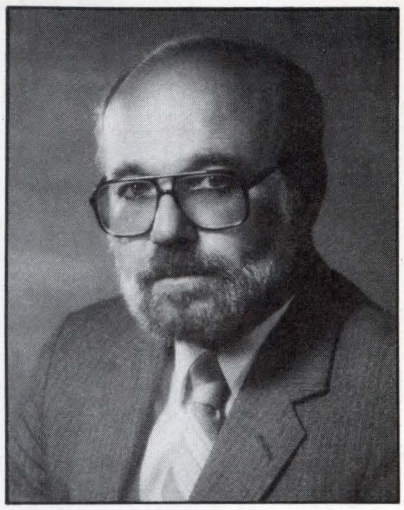
CIRCLE 12

A CARTEL BY ANY OTHER NAME . . .



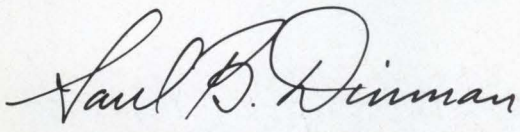
According to Webster, a cartel is two or more businesses that join forces in order to limit output, fix prices, and divide available markets amongst themselves. Loosely, its purpose is to do some kind of market rigging. Cartels have been around for a long time. The Europeans and the Japanese were practicing the fine art of forming cartels while we were still learning how to survive as a nation.

Recently, we have witnessed a new high—in fact, a form of technical renaissance—in intercorporate cooperation for the purpose of furthering the state of the art. As technology advances at an increasing pace, there is a greater need for standards of all kinds. Standards committees and independent associations have served as forums for thrashing out differences in "specsmanship." But lately, we have had little patience with committees that have either taken too long to establish standards, or have come up with standards that are too convoluted. In the latter case, the joke about how "a camel is a horse designed by a committee" often holds true. Other times, we have totally disregarded committees and have been guilty of simply accepting or endorsing the standards set by the clear-cut market leader at the time.

Today, a 2-year delay in defining a bus standard, a local area networking standard, or a software interface for graphics is unacceptable. This slack time can keep hundreds of technical companies from furthering both the state of the art and their own economic well-being. As a result, we have witnessed the beginning of an era of cooperative standards efforts between major companies. By enlisting the backing and pledges of many companies to support a common standard, they all can get on with the business of developing markets that everyone knows lie in waiting.

Like it or not, we have also added a new dimension to the concept of a cartel. A group of companies can conceivably "rig a market" by defining an alternative to another group's set of standards, if they have enough economic clout. If we are going to play in the ball game of cartels, we must realize that we are playing an international game, where some of the other players are whole governments whose main interests do not include furthering any art.

Currently, we are the technology leaders. But, as the game moves into the cartel arena, the results do not necessarily depend upon technological leadership, they depend upon economic muscle. Maybe the economic might of an IBM or ITT is roughly equivalent to that of a small nation, but what kind of combine—cartel, if you will—does it take to equal the economic clout of a Japan or a Common Market? Our government is going to have to adopt a different outlook on the matter; we should at least be allowed to play the game using the same rules as the competition.



Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—September
"Ethernet and the PBX—A Beneficial Partnership"
Vern Coleman, Advanced Micro Devices

This article will now compete with other monthly winning articles for the 1982 editorial excellence award.

WITH THESE RELIABLE LITTLE OR

In today's everybody-wants-a-piece-of-it desktop market, manufacturers are sending more and more systems into the office.

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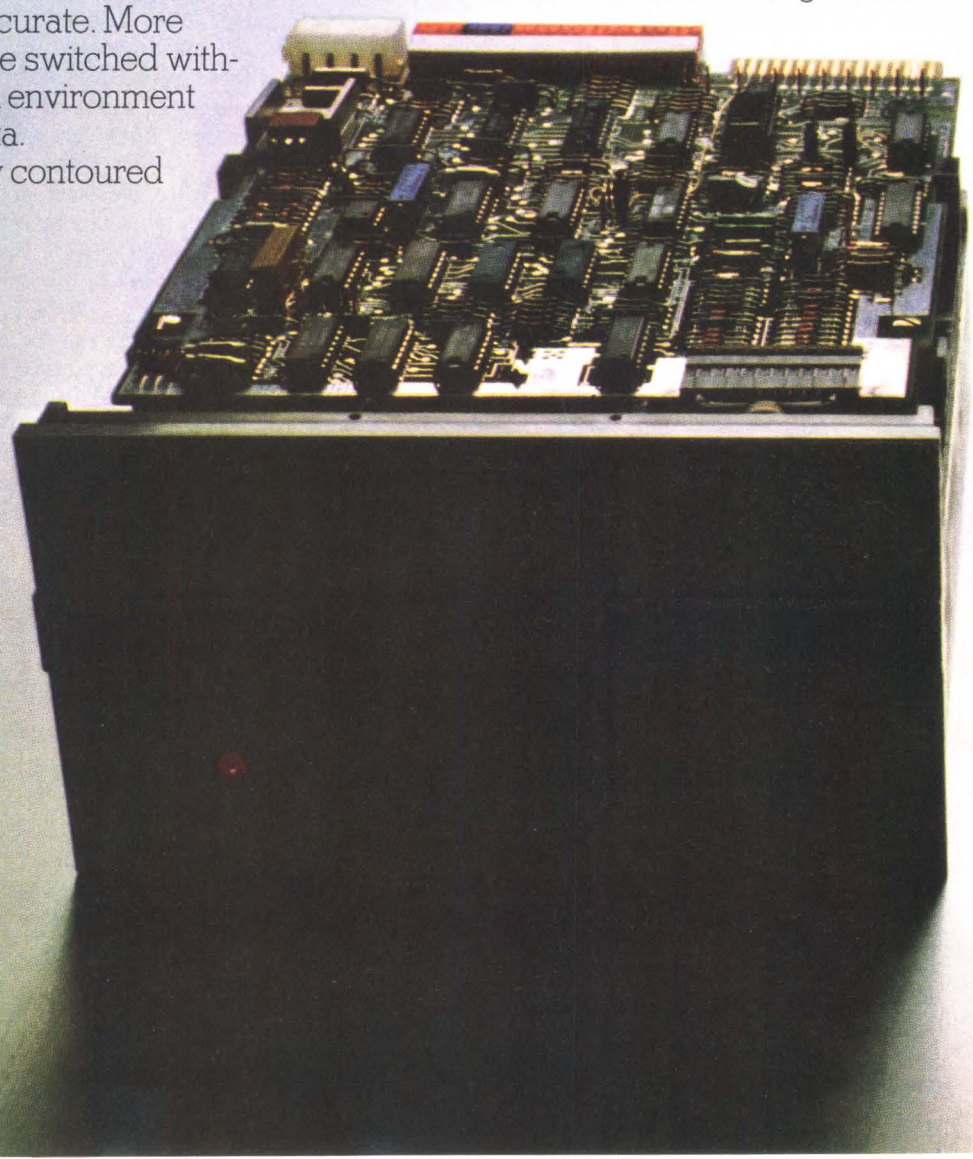

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CIRCLE 13

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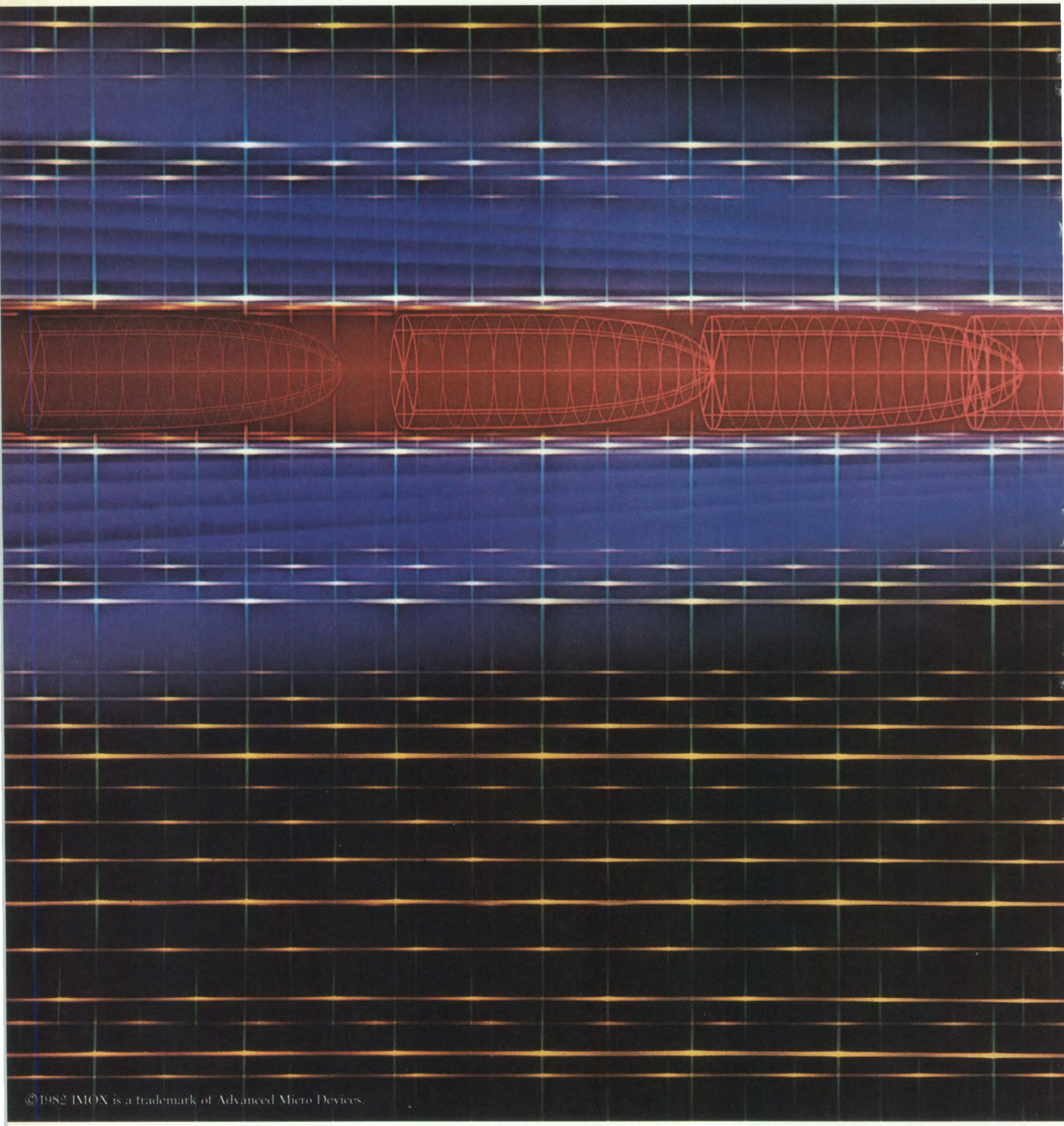

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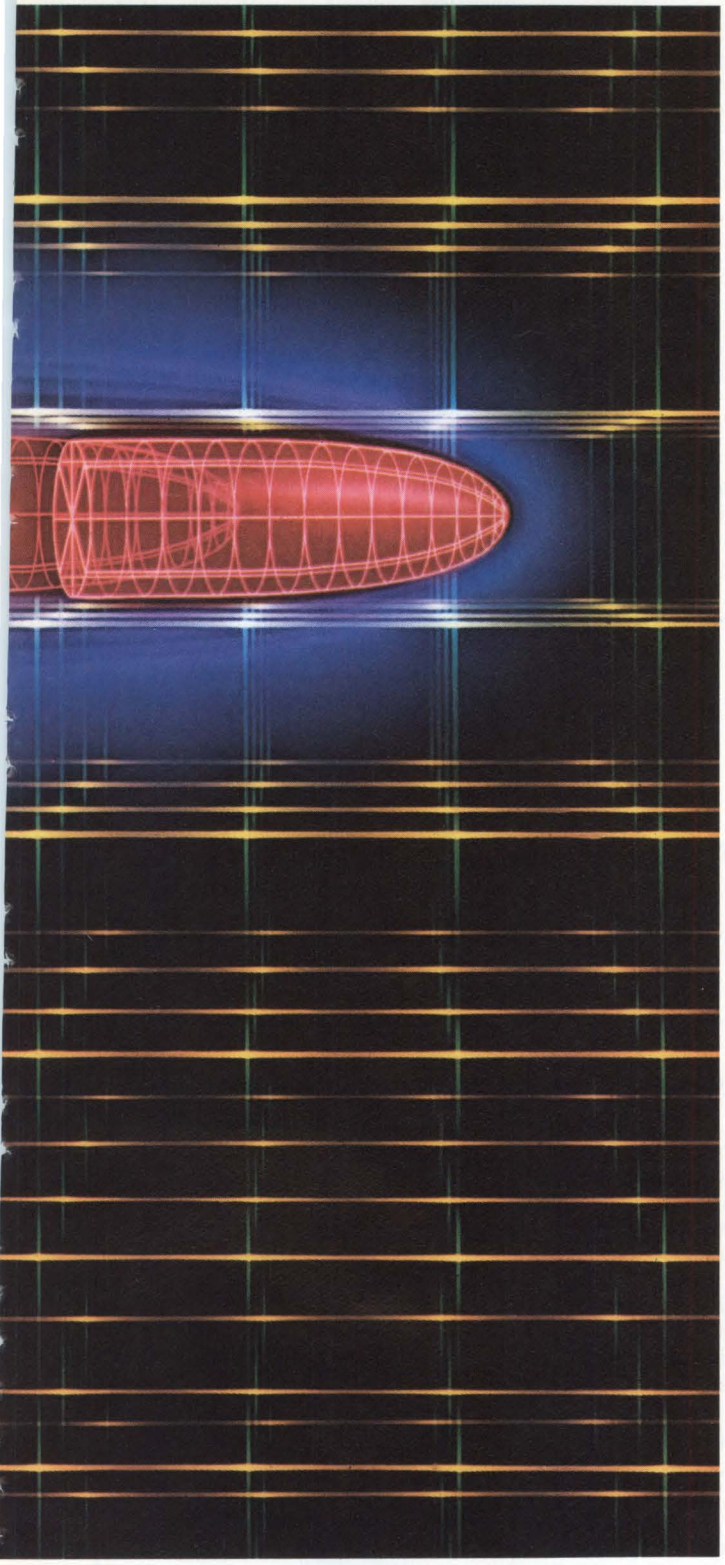

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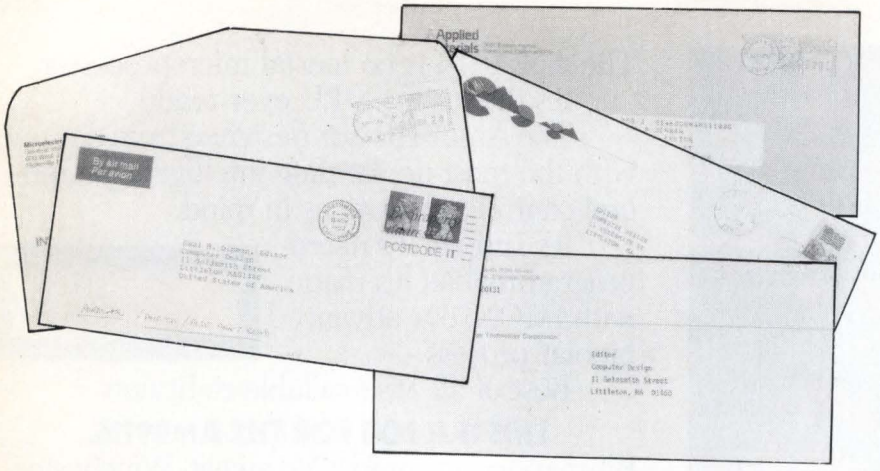


Larger holes merit looking into

Before the industry spins off into the new drive geometry (see "Winchester 5¼" Drive Packs 140M Bytes on Eight Disks," Jan 1983, p 170), it seems that an analysis of the disk center hole dimension would be both instructive and, in the long run, fiscally prudent. With the arrival of this new geometry, there is clearly a trade-off whereby low value real estate (disk area near the center) may be reasonably exchanged for highly desirable motor volume. If the placement of the motor inside the spindle allows only one additional disk, the benefit seems very clear.

As a designer of fractional horsepower (FHP) and sub-FHP electric servo and disk drive electric motors, I would like to ask disk drive and disk manufacturers two questions: first, has anyone in the disk memory systems industry performed such an analysis? If so, will disk manufacturers offer a design with a larger center hole at a price the industry can justify?

Increasing the hole size from 40 to 50 mm offers motor manufacturers a performance improvement based on maintaining the same motor geometry that is approximately proportional to $(50/40)^2 = 1.56$. This will result in higher efficiency, less power dissipation, a smaller driver and, consequently, lower temperature rise. Further benefits are higher acceleration, reduced head flying speed, and lower instantaneous speed variation due to the motor manufacturers' option to design motors with less torque ripple over the entire frequency spectrum of interest. Magnetic shielding to reduce stray fields is also essential, and the increased radius would allow for extra shielding if required.

Thus, for a 56% increase in motor volume, the loss of disk area corresponding to the increased hole size works out to just under 8%. With the arrival of still higher density recording, I feel it is worth taking a hard look at our options before we become locked into the 40-mm hole size for all future generation 5¼" Winchester disks.

Peter M. Bartlett
Indiana General Motor Products
1168 Barranca Dr
El Paso, TX 79935

Required reading—with two exceptions

Both "Borrowing rf Techniques for Digital Design" by David Montgomery (May 1982, p 207) and "Understanding the High Speed Digital Logic Signal" by Malcolm Davidson (Nov 1982, p 79) should be essential reading for young engineers concerned with high speed logic. Unfortunately, Mr Davidson's otherwise excellent article has two misconceptions. First, it is often not practical to correctly match the transmission line. Second, his high reliability system contains a number of potentially serious single-point failures.

For example, mismatch occurs in the design of high speed backplane buses, such as the P896. In this case, the backplane can be considered as a transmission line. However, the characteristic impedance varies considerably with the number of connectors and cards installed. Consequently, reflections are inevitable, even with approximately terminated lines. The waveform seen at any connection point will therefore be dependent on the physical position of both the transmitter and receiver, and also on the number and position of other cards installed at the time. Many problems can be overcome by careful design of the data transmission protocol, and by using extra strobe and acknowledge lines.

The high reliability example is the simplest form of "m" out of "n" modular redundancy. It is true that increasing logic does not necessarily increase reliability. However, such systems must be built so that no single hardware or software failure will prevent correct operation. Triplicating the transmission lines minimizes the failures concerned with the line; it does nothing to overcome failures due to the extra logic. Many problems can be overcome by careful

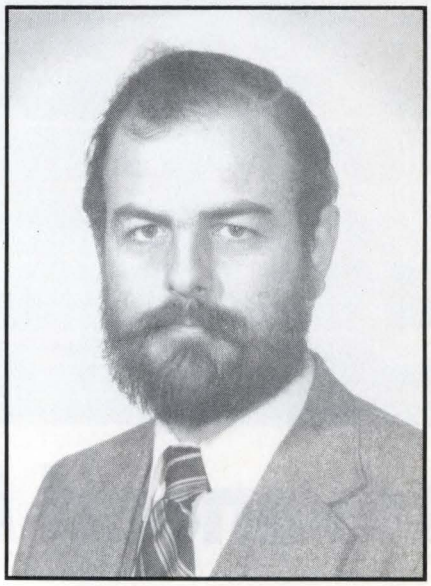
(continued on page 24)

Computer Design adds new Field Editor

Sam Bassett has joined *Computer Design* as a Field Editor. Sam's background includes a wide range of experience. Previously, he was a senior editor at *InfoWorld* magazine, a technical writer with the Paul Pease and DWT Associates agencies, and a free-lance writer for various computer and electronics companies in Silicon Valley.

Sam holds a BA and an MA from Hawthorne/Paideia University in Petaluma, Calif. He has a knowledge of RPG, Cobol, Fortran, and PL/1 languages, and has taught himself Pascal and Forth.

Sam is working out of *Computer Design*'s Sunnyvale, Calif offices. He is specializing in microprocessors, microcomputers, and memory systems. In addition, he is responsible for West Coast coverage of software, data communications, and computers.



UDS serves up 9600 bps

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CIRCLE 15

(continued from page 22)

attention to error detection and correction codes and protocols, without having to add large amounts of extra logic.

R. D. Edwards
Silhill House
2235/7 Coventry Rd
Sheldon, Birmingham B26, 3NW,
England

Brits 1 . . . Yanks 0

I would like to respond first on a technical note and second on a philosophical one. I agree that it is difficult to "match" the line or, more accurately, to define Z_o over the entire length of an interconnect. If a backplane design is to be carried out, then the short, open circuit stubs that exist due to cards being plugged in can be thought of as additional capacitance. This Z_o now becomes equal to

$$\sqrt{\frac{L}{C + C_a}}$$

where C_a is the additional capacity due to boards. This backplane must only be terminated at each end and never in the middle.

Mr Edwards' points concerning reliability are appropriate; however, they reiterate the importance of careful design. There are always reasonable and unreasonable designs that satisfy system requirements. The competent designer will usually adopt a "reasonable" design based upon the correct fundamentals.

On a more philosophical note, it is ironic that the only response has been from England. The United States spends billions of dollars each year developing complex digital systems, often used as part of the nation's so-called defense. Based on the minimal response this series of articles has garnered, it is apparent that the system designers do not possess the appropriate theoretical expertise.

The digital electronics industry is producing small microcomputer systems that are offline, relatively simple data processing devices. They are controlled exclusively by software types (computer scientists) and the programming is being used to control inefficient hardware. The fundamentals are being gradually lost and, because this industry is market driven, the repercussions of this loss will be felt when it is too late.

Universities and colleges must be required to play an important role in reversing this trend of increasing ignorance for today's technology to be used efficiently in tomorrow's products.

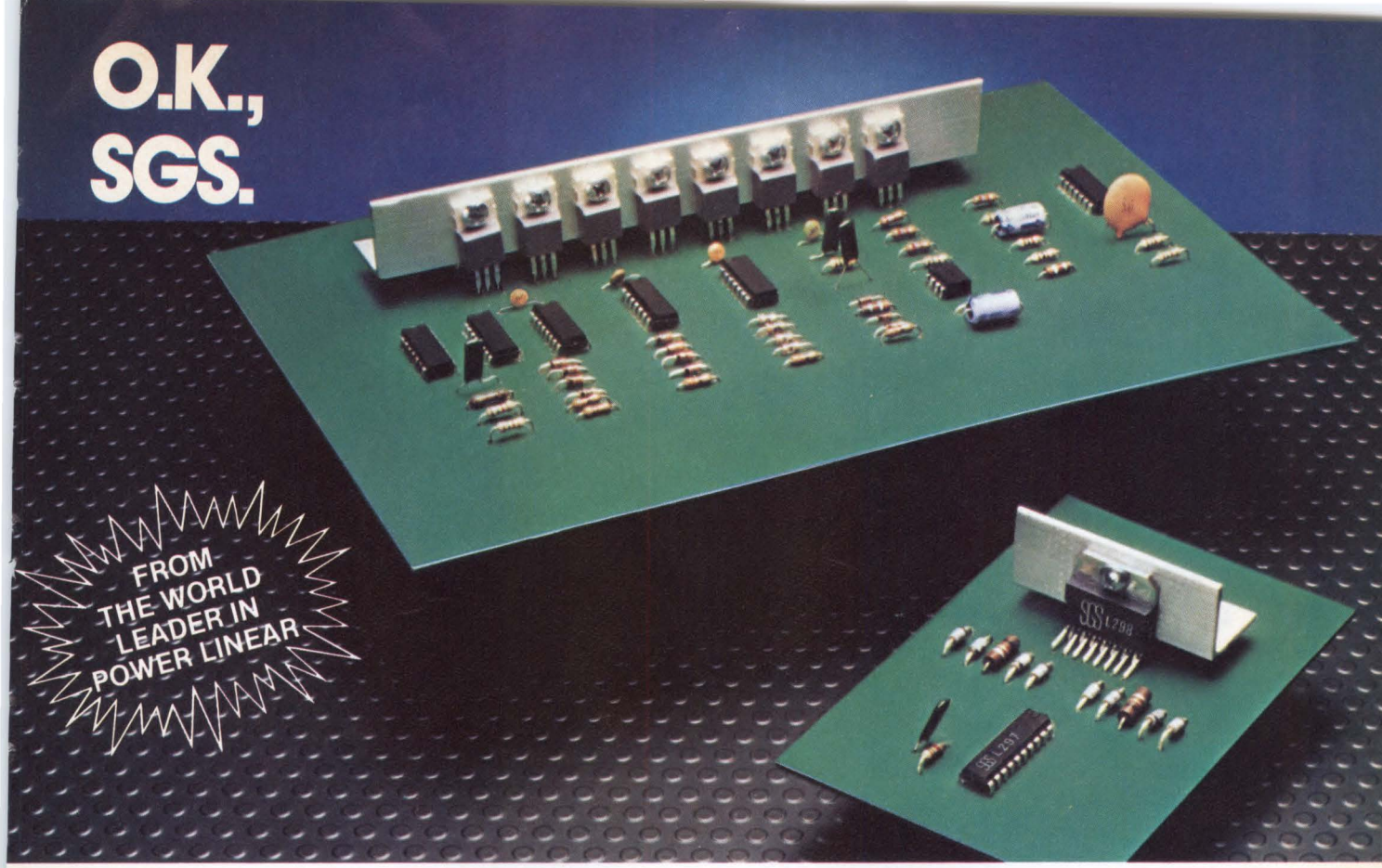
Malcolm F. Davidson
Heaviside Industries Ltd
PO Box 2742
Westport, CT 06880

A dream made possible

Thank you very much for the Hall of Fame piece in your Dec 1982 issue (p 85). I am sincerely honored to have been chosen as a member of the Computer Industry Hall of Fame. It is truly an accomplishment I would never have dreamed possible!

Gary A. Kildall
Digital Research
160 Central Ave
Pacific Grove, CA 93950

O.K., SGS.



Tell me how to drive bipolar stepper motors in less space, at half the cost.

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The L297 needs only clock and direction input signals to generate the four phases required to drive the motor. The L297 features full or half-step modes, with 2 steps per clock pulse possible in the full step mode. The device accepts input commands for clockwise or counter-clockwise operation. In addition, a home signal is generated to detect when the motor is in the home position.

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Cut Constant Current Drive Costs in Half
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L293 Dual H Driver
The L293 power amplifier can be used in place of the L298 for lower current, lower power motor drive applications.

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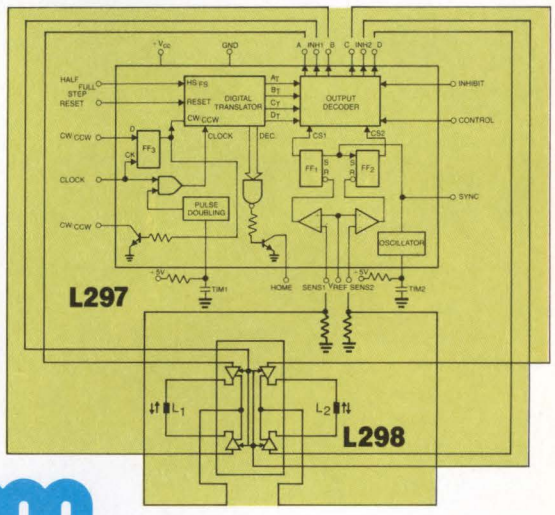
Block Diagram and Typical Application



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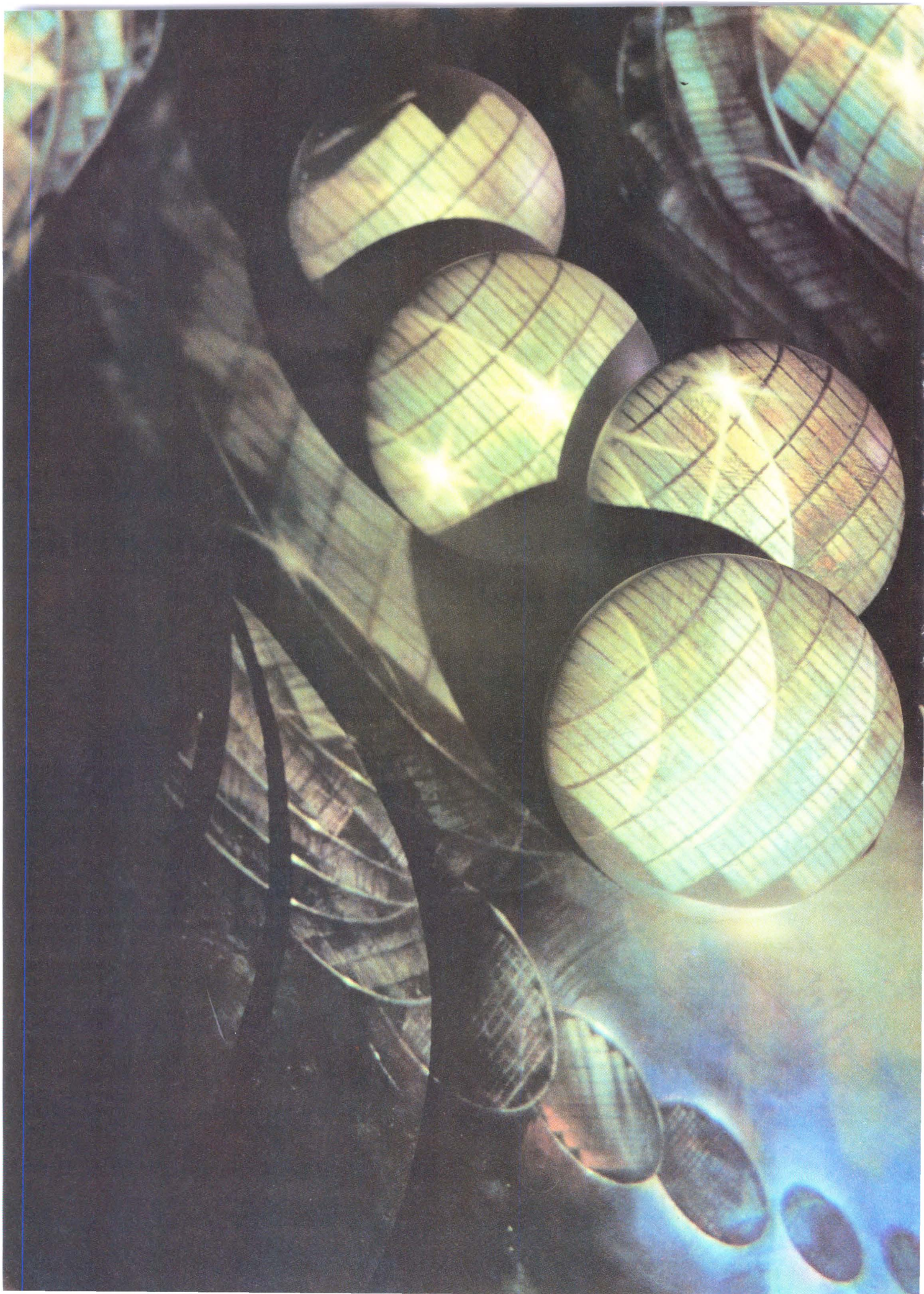
CIRCLE 17



New 64K DRAM...

"Nibble Mode" gives effective cycle time under 85ns

Here's another first in VLSI from INMOS. It's a 64K x 1 DRAM with a feature called "Nibble Mode". By providing the on-chip equivalent of 4-way interleaving, the IMS2600 allows high-speed serial read/write access to 2 bits, 3 bits or a nibble, allowing effective cycle times below 85 ns.

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	Access Time	Cycle Time	"Nibble Mode" Cycle Time
IMS2600-10	100ns	160ns	55ns
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But that's not all. The part operates at cycle times down to 160ns and dissipates only 303mW max at 350ns cycle time (standby power is only 22mW). In addition, this advanced 64K DRAM offers "$\overline{CAS}$ before $\overline{RAS}$," a refresh-assist function that frees pin 1 for future 256K use.

The IMS 2600 is a direct plug-in replacement for other 64K DRAMs in existing designs. And it's the 64K standard for new designs. Available now, the IMS2600 is packaged in a 16-pin, 300-mil DIP with the industry standard pinout.

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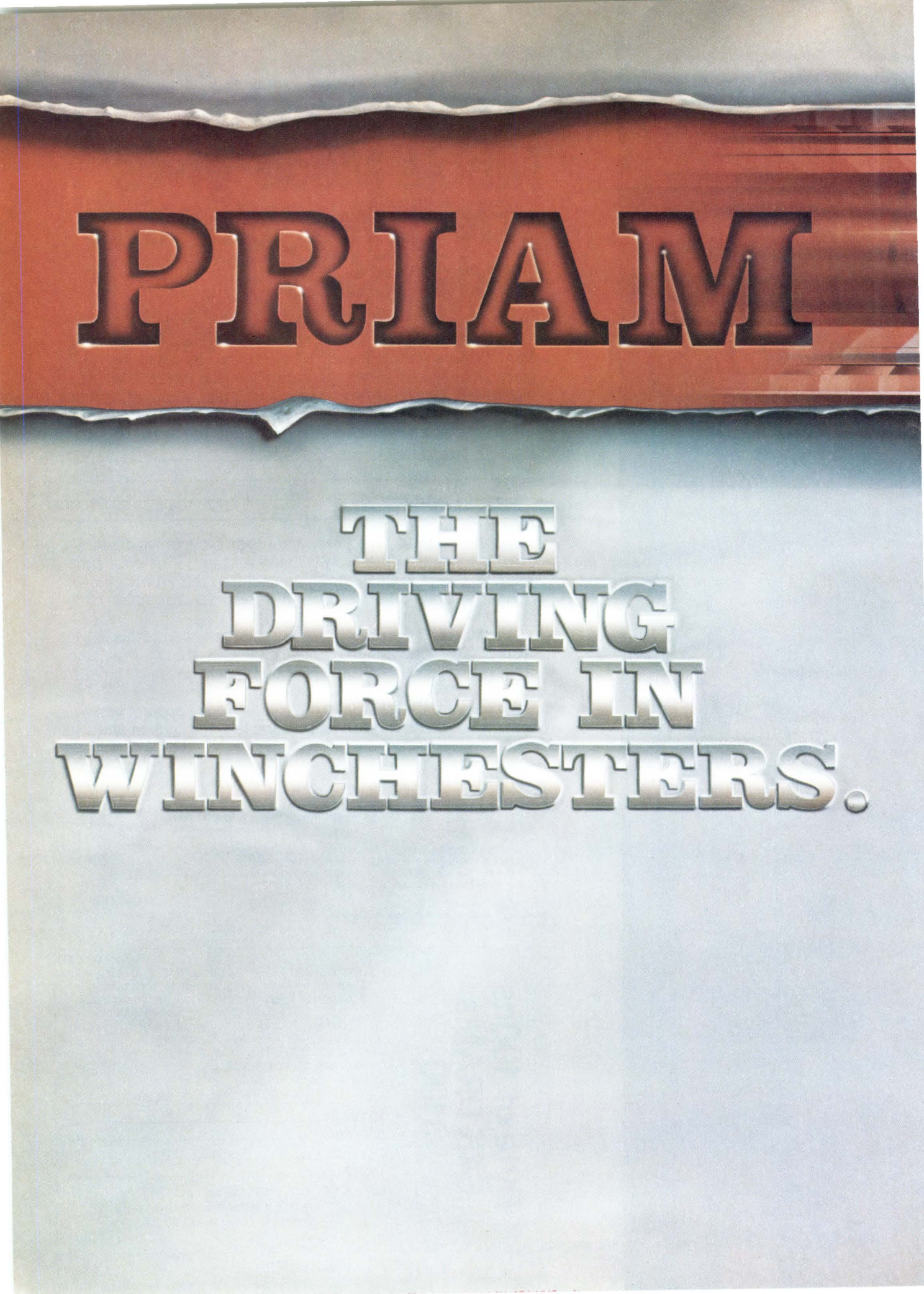
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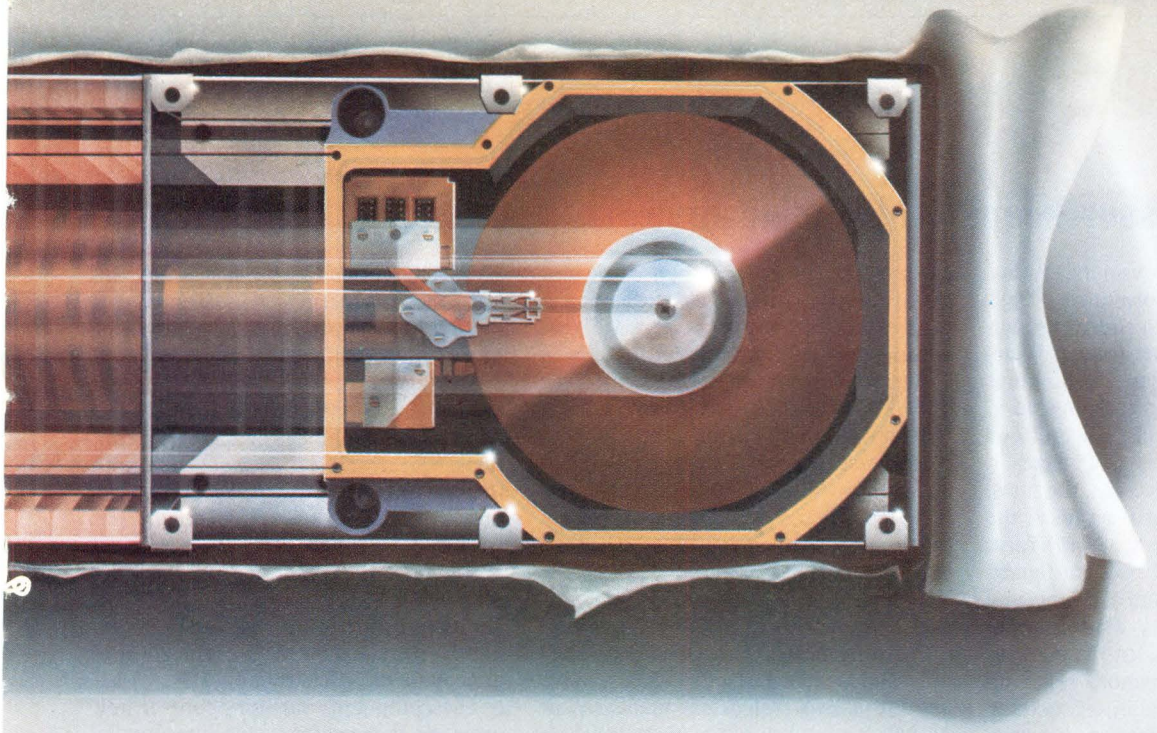

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PRIAM Time. We've paid our dues by delivering thousands of Winchester disc drives. We've proven our technical superiority and high reliability in the field. We're the force to be reckoned with on the high-performance Winchester scene.

A growing family of winners. From the beginning in 1978, PRIAM has been the driving force in high-end Winchester technology. We've proven our technology in the 14-inch Winchester market with our 34, 68 and 158 Mbyte units. Our 8-inch drives have capacities of 35, 70 and 105 Mbytes in a floppy-sized package. And, we're adding a 50 Mbyte 5¼-inch drive to our growing family.

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Size	Model	Capacity (MB)	Access Time
14″	3350	34	45 ms
	6650	68	45 ms
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SMART Interfaces. PRIAM gives you the finest in interfacing flexibility. Our intelligent interfaces can control up to four drives in any mix, plus tape or floppy backup. They're your fastest and easiest route to putting a Winchester database in your system. Or, if you have an SMD or ANSI controller, our drives can be supplied with a matching interface.

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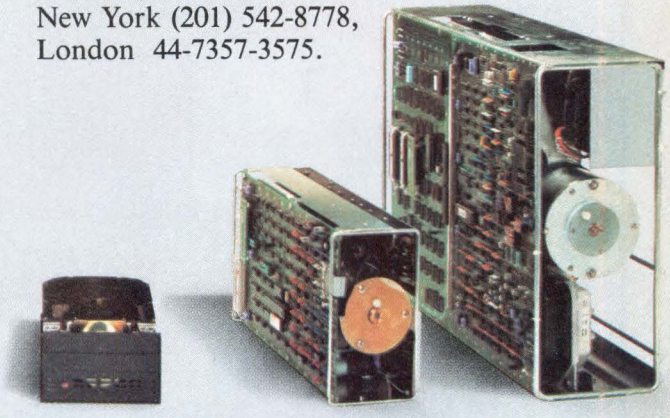

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CIRCLE 19

Bipolar processor keeps 16-bit mini alive

Overlapping its 32-bit cousin the MV/4000 in price and performance, Data General's 16-bit S/280 can churn through instructions at 900k-Whetstones/s. Garnered from a microprogrammed bipolar bit-slice CPU and onboard cache memory, this performance level puts the unit one up on most 32-bit minis and makes it twice as fast as its predecessor, the S/140.

The minimum 3-board set uses the standard 15″ x 15″ (38 x 38 cm) form factor resulting in a compact configuration. Both CPU and system cache occupy a single board. Memory control unit/input/output unit (MCU/IOU) resides on a second board, and memory takes up the third. A bidirectional interprocessor bus provides communication between CPU and MCU/IOU. Separate memory address and memory data buses allow the MCU/IOU to access memory independent of the CPU. When CPU, 2M memory, and floating point and burst multiplexer channel (BMC) options are installed, there are still 10 slots left.

Based on a 16-bit arithmetic logic unit (ALU) consisting of cascaded 4-bit microprocessor slices, the CPU uses third generation bipolar technology to gain a 150-ns cycle time. Running under the direction of microprograms taken from the 288K-bit control store, the CPU processes machine level instructions in a 3-stage pipeline. Simultaneously performing fetch, decode, and execute operations on sequential instructions improves CPU performance.

Microinstructions residing in 55-ns PROMs are coded in a 72-bit horizontal microword, which is divided into multiple independent control fields. This division allows concurrent management of hardware resources. Assembly language level performance is improved by reducing the number of microcycles to execute a line of code.

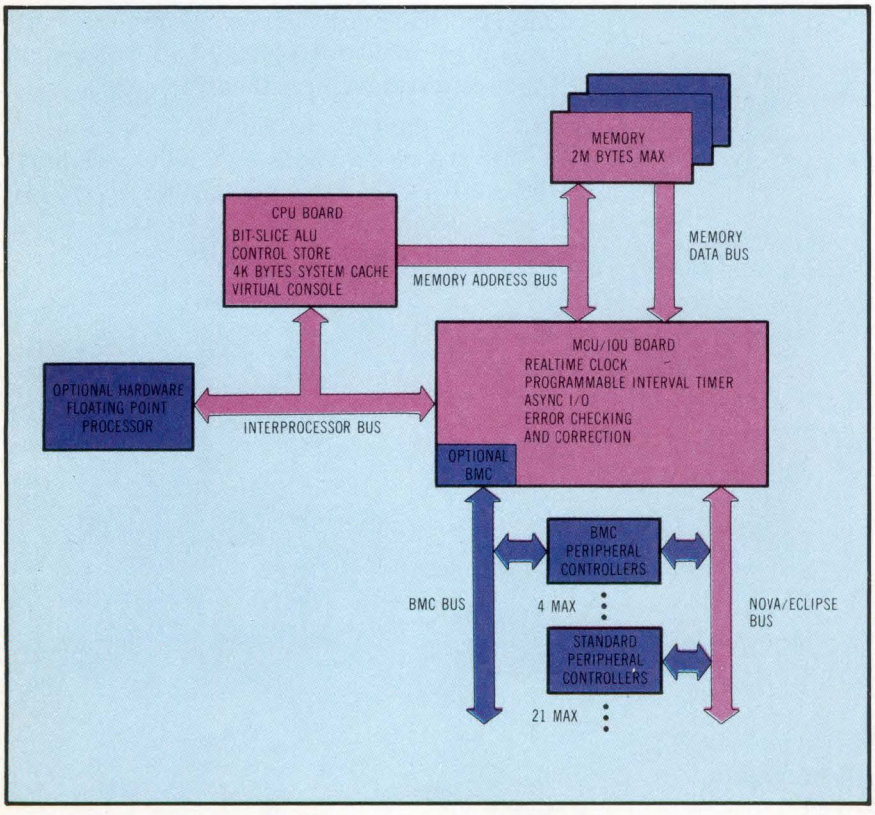
Accelerating overall performance by improving memory access and reducing CPU to I/O contention, the system cache lies between the CPU and main memory. Fabricated in 55-ns bipolar RAM, this local memory permits the effective CPU cycle time to approach that of the cache RAMs rather than that of main memory.

Storing recently used instructions and data, the 4K-byte cache is divided into two sets of 256 blocks. Each block contains four 16-bit words associated with the contents of a 4-word block in main memory. The two independent sets within the cache yield a hit rate of approximately 95%. This results in an effective memory access time of 193 ns and permits programs that run predominantly from cache to execute at rates greater than 3M instructions/s.

The computer's memory control unit provides the primary CPU interface to memory. Memory modules formed of 16K- or 64K-bit 150-ns dynamic MOS RAMs are 2-way interleaved on every board. Modules come in 512K-, 1024K-, or 2048K-byte increments. Error correction and detection are carried out continuously when memory locations are either refreshed by the memory control unit or accessed by a specific CPU operation. This prevents single-bit errors from accumulating and many multibit errors from occurring.

The I/O control function serves as primary interface to CPU accumulators and main memory. It also incorporates realtime clock, programmable interval timer, and asynchronous port. A data channel I/O bus provides direct memory access through the I/O control unit at a bandwidth of 2.2M bytes/s input and 1.7M bytes/s output. The BMC option supplies a wideband I/O path independent of the standard data channel. This channel permits bursts of data to be transferred into memory at 13.3M bytes/s and out of memory at 9.7M bytes/s.

Performance levels of the S/280 provide the power necessary to handle time-critical online applications, including scientific computation and industrial automation and process control. Prices range from $30,000 for a CPU with 512K-byte memory to $72,535 for a package containing CPU with 2M-byte memory, floating point unit, 73M-byte Winchester disk, 1600-bpi streaming tape drive, and operating system and language support. The hardware floating point unit sells for $6000 and the burst multiplexer option for $1500. **Data General Corp**, 4400 Computer Drive, Westboro, MA 01580.
Circle 240



Based on a bipolar bit-slice processor, the 16-bit S/280 combines microprogrammed CPU with 4K-byte cache memory to supply performance in online applications. Optional floating point processor lifts ratings to the 900k-Whetstone/s level.

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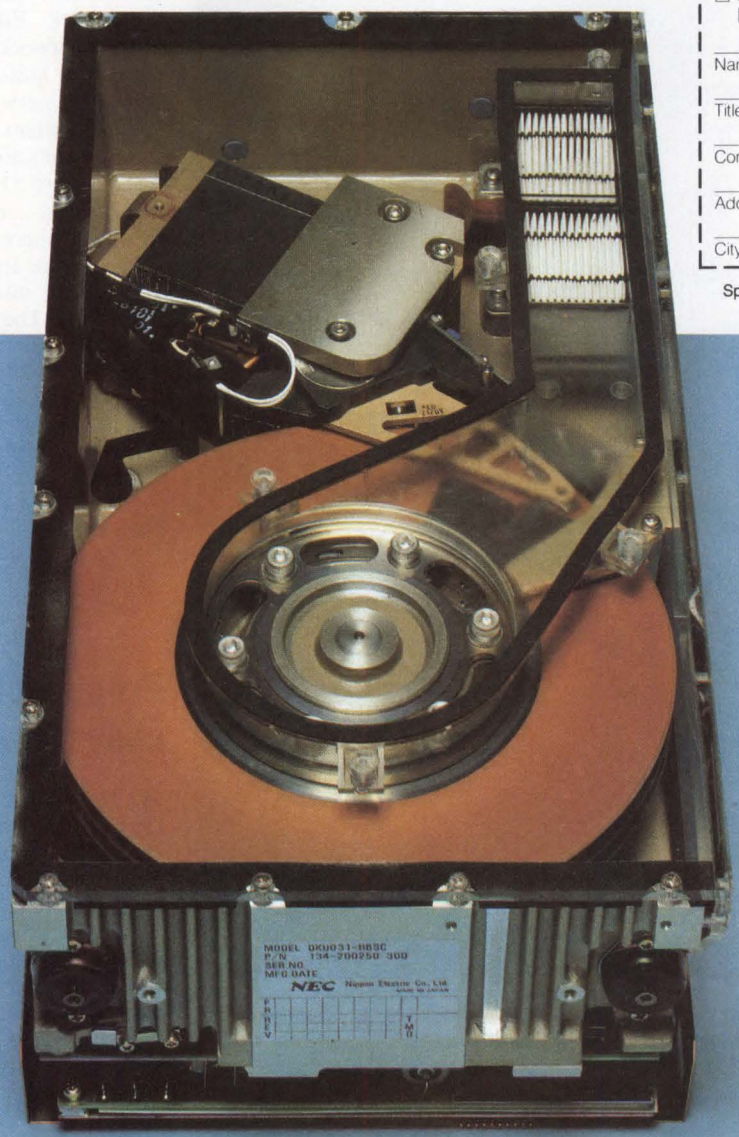

CIRCLE 20

Network combines voice and data

All communication—whether voice or data, at high or low speed—is performed on the LANmark network. By integrating local area networking with a communication switch, InteCom Inc provides the advantages of both while eliminating the need for separate installations. The 512M-bps network is currently available for Ethernet applications.

Integration is accomplished through use of the company's integrated business exchange IBX S/40. Star architecture permits the IBX to perform LAN functions internally. Simultaneous voice and data are provided to each user from 8192 ports without degrading performance standards. Terminals can be up to 2000′ apart for twisted pair wires or up to 25,000′ apart with fiber optics.

Both format conversion and protocol translation are performed by the IBX through packet switching techniques. The architecture is based on a nonblocking switching matrix and redundant 32-bit computers called the master control unit (MCU). The MCU contains 4M bytes of directly addressable memory and 67M bytes of disk resident memory, and handles as many as 64 switching networks. Each pair of these networks routes circuit and packet transmissions to different destinations.

Coordinating functions are provided for up to 32 distributed interface multiplexers (MUXes), the next layer in the architecture. The MUXes support the 8192 data ports and link up to 12,000 electronic telephones called integrated terminal equipment (ITE).

Single-data option boards within each ITE provide direct RS-232-C or RS-449 interface with data terminals, eliminating the need for modems and integrating voice and data. Because the ITEs also connect the IBX directly to Ethernet devices or to an Ethernet network, conventional Ethernet coax and transceivers are not used.

LANmark Ethernet can extend an existing network, both in distance and in number of attached devices; replace the Ethernet network; or interconnect existing systems. Among other Ethernet enhancements are expansion of bandwidth from 10M to 512M bps, full- instead of half-duplex, and packet and circuit switching where none existed before.

In a future application, LANmark will also replace IBM 3270 coax with twisted pair wiring. The 3270 workstations will be plugged into specially equipped ITEs, then to the IBX, and finally to the 3274 cluster controller. Workstations, therefore, will have access to many separate cluster controllers rather than to the present single controller. **InteCom Inc,** 601 InteCom Dr, Allen, TX 75002.
Circle 241

InteCom's LANmark network, based on use of the company's star architecture IBX S/40 integrated business exchange, provides simultaneous voice and data transmission through each of 8192 ports. Interconnection of the 512M-bps Ethernet compatible system is via 2-pair telephone wire.

Processor family eases communications

The Netway family of interface processors from Tri-Data allows the user or OEM to configure arbitrary networks without regard to the equipment manufacturer or the communications protocol used.

Netway Processors provide a variety of hardware interfaces to make electrical connection between various brands of equipment. Software protocol conversion allows them to talk to one another, and firmware handles network management.

(continued on page 34)

This Lundy has an all-pervasive breath-takingly beautiful 4097th color. It's called high resolution.

Lundy's T5484 Color Raster Graphics Terminals have the highest color resolution available. Think of that resolution as a Super Hue—a 4097th color—that mixes with all other 4096 colors to make each as sharp as you've ever seen.

Our 5480 Series of color raster terminals and workstations aren't the only ones with 4096 colors. But the colors have never looked so good. Because resolution has never been higher.

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The 1536 × 1024 pixels set a new standard for displayable resolution. Raster staircasing is significantly reduced without the complexity of anti-aliasing.

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You shouldn't be forced to ditch programs in place when you buy a new terminal. For that reason, standard with all 5000 Series models is a Tektronix 4010 or 4014 Emulator with mixed-mode software switch for enhancing existing programs with color-native protocol.

Lundy's 5484 color raster design workstation.

Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software development program to provide the most comprehensive application packages.

Lundy will help you see more in graphics.

When you look at our 5480 Series, take a close look at Lundy, too. We're a company that's as good as its products.

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A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

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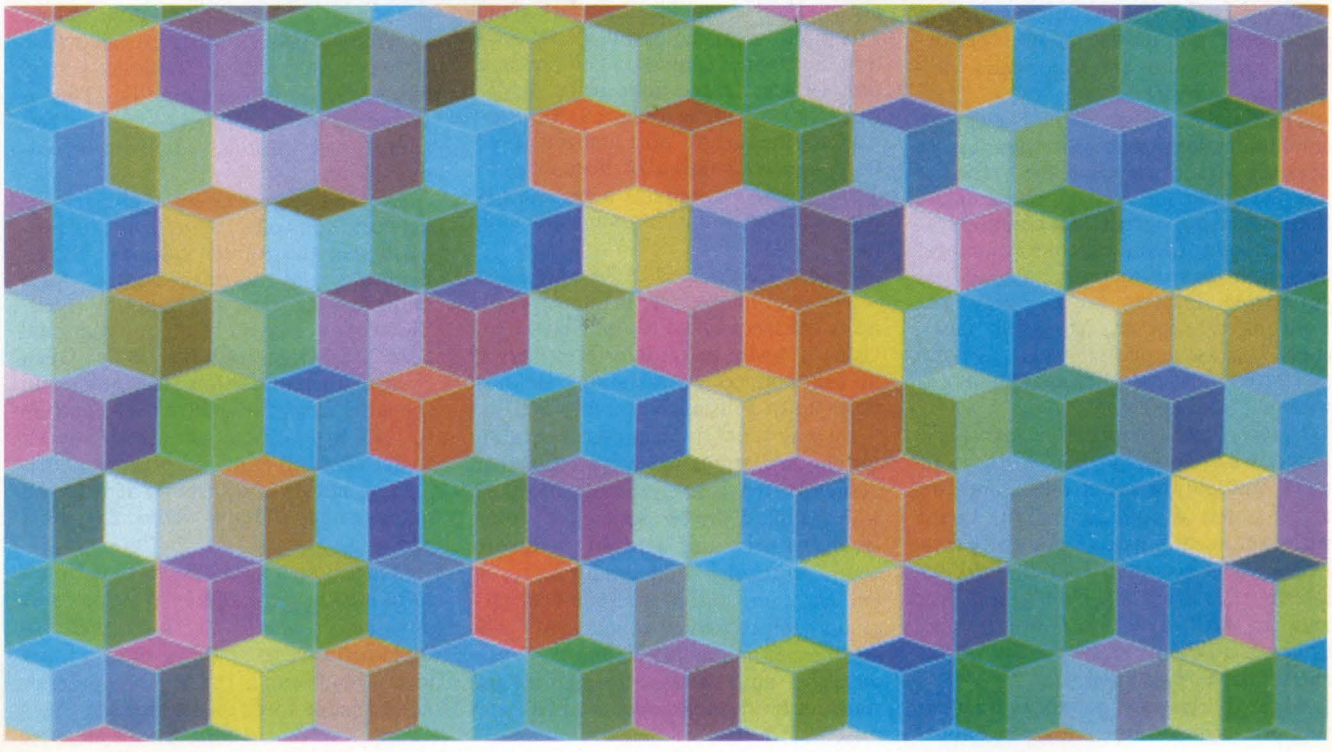
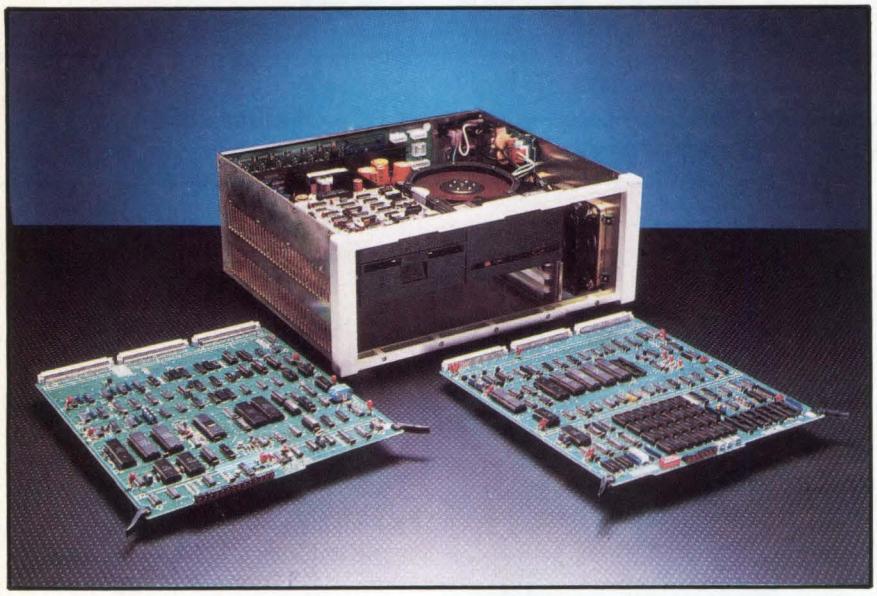
The Lundy 5688 displays 256 high resolution colors at a time. User downloadable character fonts; programmable character sizes.



CIRCLE 21

Interface processors
(continued from page 32)



Shown here is Tri-Data's Netway 200 communications processor with communication board (left), and processor memory board (right). Card cage at rear is presented with high density 5″ floppy disk drive and 10M-byte ST506 compatible hard disk installed.

Any mechanism that facilitates communications between hosts, servers, and terminals is a valuable addition to a system integrator's toolkit. Tri-Data has developed such a mechanism in its Netway processors. The family of processors is based on the company's proprietary operating system, Netway Communications Operating System, implemented on distributed multiple Z80 microprocessors with appropriate connector and networking hardware.

The family consists of the Netway 200 communications processor, Netway 100 device interface processor, the Netway 50 interface, and the Netway communications operating system. The communications processor handles remote and local network management. Protocols supported include BSC3; Burroughs Poll/Select; ICL C01, C03 (full XBM); start/stop ASCII; IBM 3270 SDLC; IBM 3270 SNA/SDLC; IBM IPARS (SABRE); and X.25 with X.3, X.28, and X.29.

Netway 200 comprises a processor board with a Z80 CPU, 256K bytes of RAM, multiple DMA controllers, and two RS-232 ports; a communications board with four RS-232 ports, a floppy disk controller, a Centronics parallel printer interface, and a 100K-byte/s SASI bus; and an 800K-byte 5¼″ floppy disk drive. A 10M- or 15M-byte 5¼″ Winchester drive is optional.

RS-232 ports can be configured to support asynchronous, bisynchronous, or bit oriented synchronous transmissions under software control. The SASI bus is used as a high speed communications channel, linking up to eight Netway 200s and/or external Winchester drives into a local network.

The Netway 100 device interface processor connects a workstation or host port to the Netway local network via an RJ11 tap to a twisted pair cable. In addition, it provides emulation and presentation services to the node being served. One Netway 100 is required for every workstation or host port unless its functions are workstation or host resident. The Netway 100 contains a Z80 and 64K bytes of RAM, and it communicates at up to 19.2k bps.

Basically a shielded cable with a plug at one end, the Netway 50 interface connects the Netway 100 to the Netway 200. Using a 4-wire RS-422 interface, Netway 50 can connect workstations or host ports up to a distance of 2 mi.

Netway communications operating system consists of an operating system kernel written in Z80 assembly language, with standard driver modules for interfacing with various hardware and software protocols. Full multitasking is implemented, so that multiple host protocols can be handled concurrently. The system also maintains a library of user messages and stores information and statistics on network operation for later review.

Dynamic network reconfiguration (rerouting messages around bottlenecks) is available on the system, as is password protection, and automatic log-on to value added networks and data bases via symbolic addressing.

Availability is quoted as early in the second quarter of 1983 in small volumes (5 to 15), with volume shipments to follow. The price of a Netway 200 configured for IBM 3270 Bisynch protocol will be $11,040 for a single unit, or $7680 in OEM quantities. **Tri-Data**, 505 E Middlefield Rd, Mountain View, CA 94043.
Circle 242

Ethernet compatible frontend processor

Exos/101 from Excelan, Inc is an Ethernet compatible frontend processor built on a single Multibus board. The 16-bit processor includes an 8-MHz 8088 CPU, EPROM firmware, and up to 128K bytes of RAM. It implements Ethernet Version 1.0 and is compatible with Version 2.0.

Excelan chose to support Ethernet because its bandwidth of up to 10M bps allows significant quantities of information to be transferred quickly, and matches the output rate of some of the fastest large Winchester disk drives. Ethernet's packet structure allows a large central file server to service several remote stations concurrently. This is accomplished by interleaving packets addressed to various stations in its output stream.

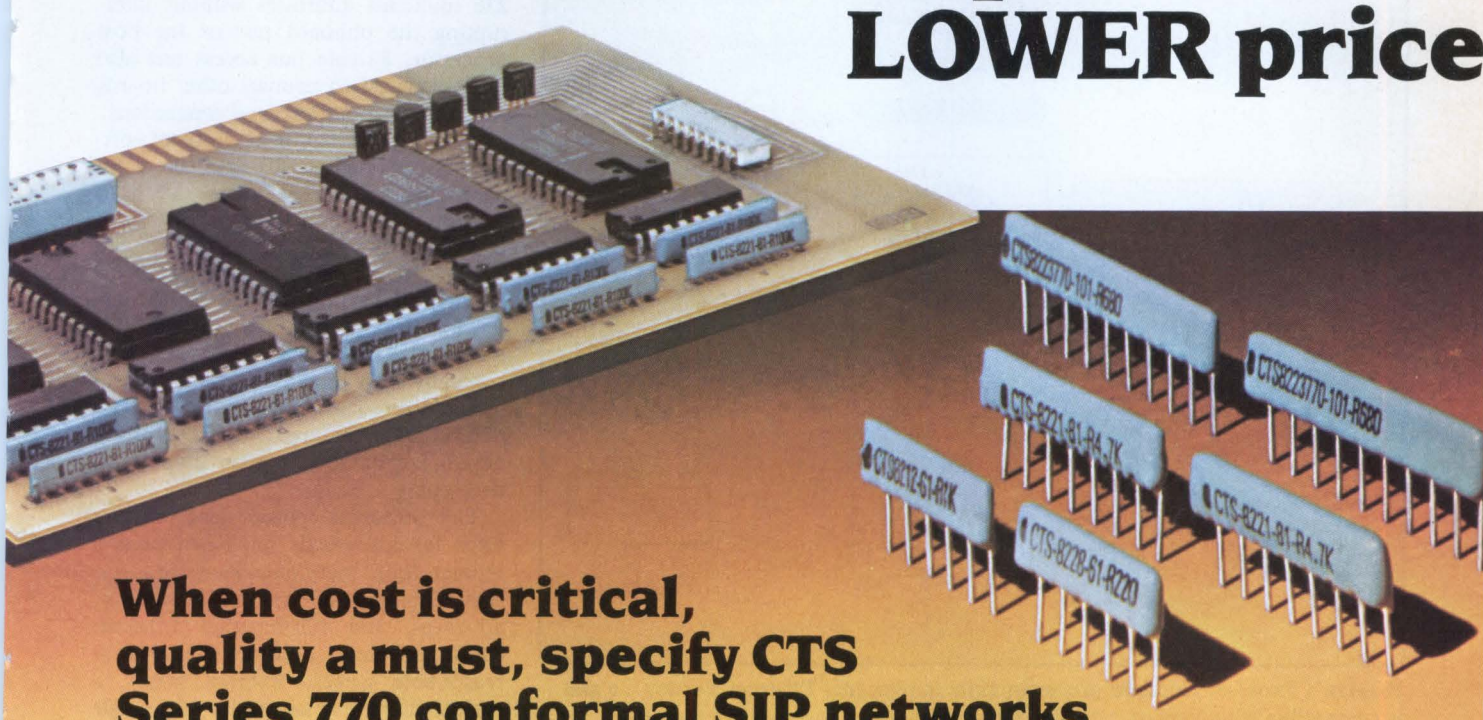
Exos/101 can act as either an Ethernet network controller or a frontend processor. In the former case, the NX/101 firmware and network control logic implement physical and data link levels, the two lower layers of the International Standards Organization's (ISO's) Open System Interconnection (OSI) model. In the latter case, the onboard 8088 and up to 128K bytes of RAM allow the Exos/101 to act as a full frontend processor, offloading network, transport, and session management details from the host processor.

When designing a system based on a local area network, a key question to be answered is whether the high level protocol software (that above Ethernet link level) should run in the host computer or be offloaded to its own processor.

(continued on page 36)

NEW CTS conformal SIP networks offer...

LOW board profile (.195") LOWER price



When cost is critical, quality a must, specify CTS Series 770 conformal SIP networks

CTS, acknowledged leader in resistor networks, now offers a line of conformal SIP's with an on-board height no greater than a DIP package (.195"). CTS experience in resistor network technology is now available in a new conformal network featuring a low selling price. Priced lower than molded or ceramic networks, CTS conformally coated SIP networks are finding more and more applications.

Series 770 networks are designed for high volume, cost-sensitive applications such as electronic games, personal computers, telecommunications gear and automotive devices. They are winning acceptance from OEM's who demand CTS reliability at a reasonable price.

Available in 2 to 12 pin sizes, these SIP networks can be supplied for large volume custom requirements or in many standard resistance values for fast off-the-shelf delivery.

Contact your CTS Distributor for off-the-shelf delivery or write for complete specifications to: CTS Corporation, 406 Parr Road, Berne, Indiana 46711. Phone: (219) 589-8220.

CIRCLE 22

CTS Series 771 Standard height (.350") SIP Networks also available

When higher power handling is a consideration, the Series 771 conformal SIP is the answer. They offer the same well-known CTS reliability and are available in 4 to 20 pin sizes.

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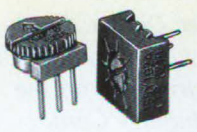

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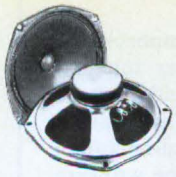

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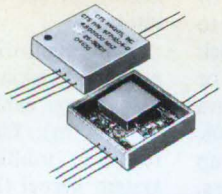

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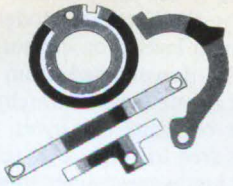
CIRCLE 25



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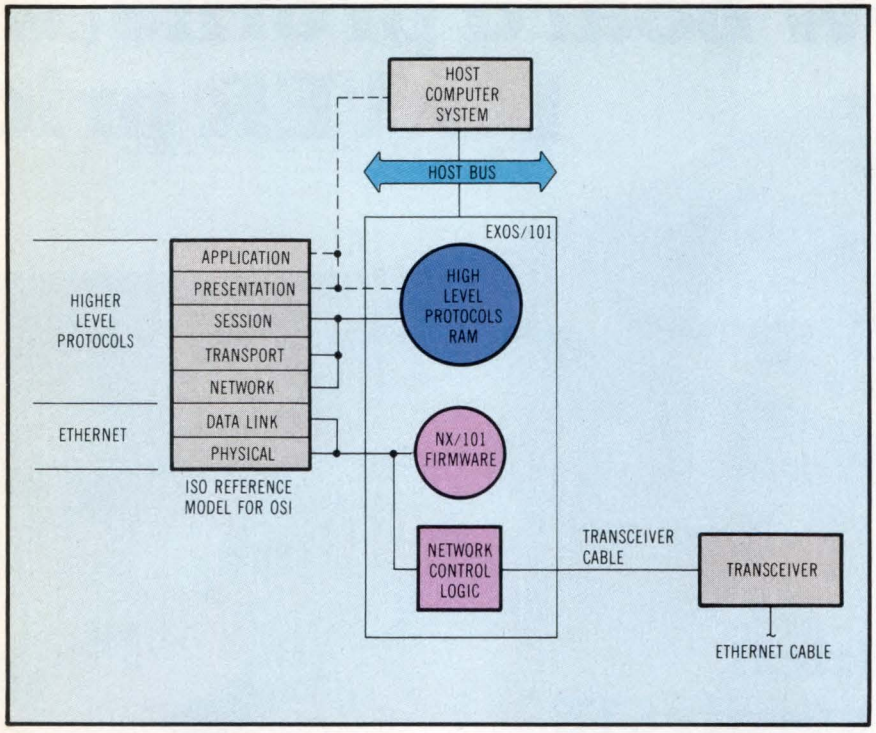
CIRCLE 26

Frontend processor

(continued from page 34)



Excelan's Exos/101 frontend processor fully implements Ethernet Version 1.0 and is compatible with Version 2.0. The 8088 processor and memory are almost exclusively available for the execution of high level protocol software, thereby offloading this task from the host processor and simplifying LAN integration into the host environment.

High level protocol software consumes large amounts of host computer time and memory if executed there. Communication protocols are interrupt intensive and require much context switching. Since most operating systems are not optimized for performing these functions, they must be modified to do so efficiently. Modifying an existing operating system is no trivial programming task and becomes prohibitive when changes must be made in the protocol, or when the operating system is updated.

As the cost of microprocessors and memory moves down the semiconductor learning curve, it becomes more practical to offload communication control to an intelligent peripheral. Communication then becomes a matter of a simple operating system call, and the host resources can be devoted to important applications, such as computation and serving user requests.

The 16-bit 8088 CPU and 64K bytes of RAM in the Exos/101 Model 1 allow it to run high level protocol software, which can be downloaded from the host or from the network. Scratchpad and data areas consume 4K bytes, leaving 60K bytes free for high level software or up to 32 hardware-chained message buffers. The Model 2 has an additional 64K bytes of RAM, which can be used for software.

With a high level interface established between the host and the network, both the network and the protocols can change without impacting existing application programs. Likewise, operating system changes will not affect the way a node looks to the network, and file or message service can go on as usual.

Each Exos/101 has 8K bytes of PROM firmware, which acts as a network executive. Called NX/101, this firmware manages the Ethernet interface and maintains network management statistics such as number of error-free transmissions and receptions, CRC errors, collisions, timeouts, packet fragments received, alignment errors, and buffer overflows. In addition, this firmware manages the Multibus interface, generating all necessary control and data signals for the standard Ethernet interface. These signals are transmitted via the shielded cable from the edge connector on the top of the board to the interface.

Full diagnostics include loopback and a time division reflectometer function that locates cable faults to within about 35′ (11 m). Firmware also provides a realtime, multitasking, mini-operating system kernel that defines the software environment for high level protocol development and execution.

Via hardware, the Exos/101 can recognize and respond to packets sent to up to 256 multicast addresses without interrupting the onboard 8088 or the host processor. Private bus access has also been provided to connect other boards supporting various link level connections.

Although no high level protocol software is provided at this time, the company has announced its intention to develop and support standard ISO protocols. Moreover, it plans to market and support *de facto* standard protocols from third parties, such as the Transmission Control Protocol/Internet Protocol and Xerox's Network System. The company also intends to support proprietary protocols for specific applications that individual customers have developed or are in the process of developing.

The Ethernet component of the Exos/101 is presently implemented as a bipolar finite state machine, using discrete components. As VLSI technology advances, and full-function Ethernet controller chips become available at reasonable prices, Excelan plans to replace discrete components with single chips, reducing real estate and power requirements without altering the interface or capabilities of the processor.

Excelan has also announced its intention to adapt the Exos/101 concept to non-Multibus environments, and to license the resulting customized hardware for OEM manufacturing. The company will also offer to redesign OEM supplied hardware to incorporate the appropriate VLSI Ethernet technology when it becomes available.

The Exos/101 Model 1 is priced at $1560 each, and $810 in OEM quantities of 500. The Model 2 is priced at $1795/$930. Both models are quoted as available for immediate delivery. **Excelan, Inc**, 2180 Fortune Dr, San Jose, CA 95131.

Circle 243

The World's Most Elegant Microprocessor Family is Here. Now.

NS16000

Elegance is everything.

No more band-aids to stretch an architecture.

The NS16000 features a totally new, totally practical architecture—not simply an enhancement of an existing one. With supporting National and third-party software, the NS16000 microprocessor family becomes the first to offer system designers the opportunity to adopt the migration path and performance of a full 32-bit architecture that will endure to the end of the century. That's elegance.

No more programming in novel ways for obscure reasons.

Only the NS16000 microprocessor family's architecture is deliberately based on high level languages, intentionally designed to support their use. The architecture's structure and behavior correspond directly to the objects and operations of HLLs—enabling symmetric use of general-purpose registers, memory locations, expanded addressing modes, data types, and sophisticated instructions. The disadvantages of writing programs in HLLs for microprocessor-based systems have now been elegantly relegated to computer history.

No more dead-end segmentation.

The NS16000 is the first commercial microprocessor to solve the problems of large memory management by using both uniform addressing and Demand Paged Virtual Memory. With this memory strategy —equivalent to that used in the VAX™-11 and all present IBM mainframe computers—each programmer, each program, each task, can simultaneously and independently access a uniform addressing space of 16 megabytes, without reservation or special exception. That's elegance.

Think about it.

The New Criterion in Software Productivity:

The NS16000 Microprocessor Family.

The pure migration path and the virtuoso performance inherent in the NS16000 microprocessor family are just the beginning.

The NS16032 CPU, now available, has a 16-bit-wide data path to memory and 32-bit architecture. Other CPUs in the family will feature 8- and 32-bit-wide data paths, but the 32-bit implementation in each ensures that the software you write today will work *without modification* tomorrow, when you upgrade from one CPU to the next.

Evaluating performance: a 32-bit integer multiply on the NS16032 CPU takes only 8.3μs at 10MHz.

The architecture of the NS16000 family is based on the roots of all the most powerful high level languages—to fully support the use of HLLs.

Programmers have long asked for a microprocessor designed with the software in mind. The regularity of the architecture for which code is being generated significantly affects its quality: the more regular the architecture, the simpler it is to produce lean, fast code. And, of course, designers and programmers write programs more quickly in high level languages.

The CPUs in the NS16000 family provide a high degree of regularity in the arrangement and use of their 32-bit registers. Data can be read or written 1, 8, 16, or 32 bits at a time, as a sophisticated program requires. Transfers from one register to another are not restricted: no special conditions inhibit a programmer's creativity.

The virtuosity of the NS16000 instruction set is clear. It includes over 100 basic instruction types, chosen on the basis of the use and frequency of specific instructions in various applications. Special-case instructions, which compilers cannot use, have been avoided.

The instruction set is also symmetrical: instructions can be used with any addressing mode, any operand length (byte, word, and double-word), and can use any general-purpose register. Instructions are *genuine* two-operand instructions as well.

These factors, combined with the regularity of the NS16000's architecture, mean that programs require significantly less code—greater code density, in fact, then the VAX-11. The simplicity by which it now becomes possible to implement a compiler, for example, is matched only by the increased speed of its execution.

The NS16000 family provides the largest number of different addressing modes ever included in a microprocessor.

Elegant programming demands that instructions be as powerful as possible, and that the range of addresses be as large as possible. So to be effective, a powerful instruction set must be accompanied by a powerful set of modes of referring to data in registers and memory.

The NS16000 architecture supports not only the standard addressing modes common to most processors (*register, immediate, absolute,* and *register relative,* for example), it also introduces HLL-oriented modes unique to microprocessors:

1. Top-of-stack (a simple, very powerful mode used to evaluate arithmetic expression in HLL);
2. Scaled Indexing (used to access elements in byte, word, double-word, or quad-word arrays);
3. Memory Relative (used for manipulating fields in a record); and,
4. External (used to access data in separately compiled modules.

Moreover, there are no restrictions on the use of these addressing modes—an instruction that operates on data of a particular kind can use any of the addressing modes that refer to that data.

With an architecture that supports uniform addressing, the NS16000's Demand Paged Virtual Memory strategy makes a gigantic memory possible at a minimum cost.

The NS16082 Memory Management Unit (MMU), provides dynamic address translation, virtual memory management, memory protection, and both hardware and software debugging support. Customers now sampling this MMU are impressed with its raw power.

The NS16082 breaks the logical address space into 32,768 pages, each with a fixed size of 512 bytes. Which specific 512-byte pages of a program or data are actually in *real* memory is a function of the most recent demands of the program itself.

This Demand Paged Virtual Memory operates automatically, and gives an applications programmer complete freedom from any consideration of memory size or allocation strategy. Since the operating system places part of the user's programs and data in peripheral storage and brings them into real memory only as needed, the user may regard the combination of real and peripheral storage as a single, large memory, and can write large programs without worrying about the physical memory limitations of the system.

The power of Demand Paged Virtual Memory allows any number of separate and independent programs or tasks to execute cooperatively and efficiently in a substantially smaller (real) memory configuration than needed by a microprocessor using a *segmented* memory management scheme.

And, because it does not limit data base growth, Demand Paged Virtual Memory provides for continuing future data expansion.

Floating point is just one of the nine data types that the NS16000 architecture directly supports.

The NS16081 Floating Point Unit (FPU) offers very high-speed floating-point operations for both single- and double-precision operands. A 32-bit floating-point multiply, for instance, takes place in 4.8 μs at 10MHz.

Designing the NS16081 into a system will allow programmers to treat floating-point numbers as any other data types, and any of the addressing modes may be used to reference them. Customers now sampling this FPU are amazed at its performance.

The optional use of the FPU and MMU Slave processors—integral parts of the NS16000's architecture—gives the systems designer the ability to determine a price/performance trade-off while preserving all the initial software investment.

Evaluation tools are available now.

The DB16000 evaluation board is a complete microcomputer system. It carries the NS16032 CPU, the NS16201 Timing Control Unit, sockets for the MMU, FPU, and ICU (Interrupt Control Unit), 32K bytes of on-board RAM, a wide range of both standard and optional I/O interface devices, and a monitor program in PROM. To allow interfacing with a variety of computer systems, a complete pin-out of CPU addresses and functions for data and control are also included. Two BLX connectors enable functional enhancements.

A component evaluation kit (the NS160KIT) is also available, with complete documentation for each part.

The first products in a line of development tools—the NSX-16,™ with a PASCAL compiler, and the ISE/16™—are available now.

The NSX-16 software development package allows quick and easy compiling or assembly of NS16000 programs on the VAX-11, using the VMS™ operating system. The package includes a PASCAL compiler, assembler, linker, librarian, symbolic debugger, and other utilities. Once compiled, programs can be down-loaded through a serial data link to the DB16000 for execution. (A NSX-16 hosted on RSX™-11M, and a C cross-compiler for VAX will be available by mid-year. Before the end of this year, a full NS16032-based development system, with a UNIX® operating system and a choice of either a C or PASCAL compiler, will also be available.)

The ISE/16 In-System Emulator—the first in a series—is available to ease integration of user software with NS16000 hardware. It runs with the NSX-16 software development package, and allows real-time emulation of the NS16032 CPU, the NS16201 Timing Control Unit, and the NS16082 Memory Management Unit.

The availability of third-party software for the NS16000 family is growing day by day.

Suppliers are now working on operating systems (UNIX, for example), language compilers (such as PASCAL, C, and COBOL), and software for program development (among them, on CP/M®).

Training classes are in progress now.

Courses lasting from two to five days—held either at the Microprocessor Systems Division Training Center, or on-site—cover "The NS16000 Architecture," "NSX-16 Software Development Support on Starplex II™ or VAX," and "ISE/16."

Now you have every reason to explore elegant applications using the NS16000 microprocessor family—from personal computers, to graphics systems, to process control.

NS16000

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See it.

The NS16000 microprocessor family will be on exhibition at Electro '83 (look for booth number 4312), and NCC (look for booth number D-2022).

Read about it.

Introduction to the NS16000 Architecture

CIRCLE 27

National Semiconductor

MICROCOMPUTER SYSTEM DIVISION

Varied design approaches provide gateways

Attempting to link the asynchronous ASCII world of personal computers to the synchronous world of IBM SNA and public X.25 wide area networks has spawned a variety of product offerings. These range from terminal/cluster controller emulations to local area networks tied to wide area networks with gateway processors. Which product is adaptable to a system is dependent upon the particular application requirements and hardware already in place. There truly is no single product that meets all application needs.

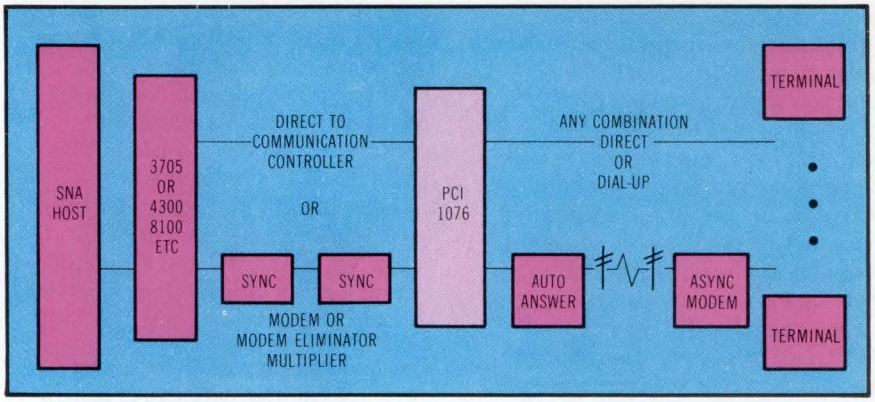
Perhaps the most straightforward approach is to have personal computers such as the Tandy Model II or Apple II emulate the characteristics of popular ASCII terminals. Protocol converters such as the PCI 1076 from Protocol Computers, Inc can link asynchronous terminals to the synchronous protocols of IBM's proprietary SNA/SDLC networks. Public networks can be linked using the X.25/HDLC protocol. In such cases, the personal computer loses control of the keyboard and CRT screen to the convertor. Within system firmware, keyboard and CRT control information is translated from ASCII format to commands understood by synchronous terminals such as the IBM 3278. Information is also translated from synchronous host computer to asynchronous terminals in much the same manner.

Besides providing 3278 terminal emulation, convertors such as the PCI 1076 also tackle the functions of an IBM 3276 cluster controller. Since the controller contains the intelligence and memory in a typical SNA clustered configuration, the 1076 buffers data packets for as many as seven personal computers. It also provides error detection and retransmission between the host and cluster.

Printers, also under the control of the convertor, direct hardcopy output directly to it rather than the screen. In addition, the IBM PC software package allows for downloading files from the host for local use.

Uploading files from the personal computer to the host is not supported since there are no host application programs available that deal with locally processed data. Files from an IBM host routed to the personal computer are stored in either printer format or a continuous data stream. The 7887+ software package for the IBM PC is priced at $200, with the price of a single-port PCI 1076 quoted at $3100.

Another approach is possible with Computer Development, Inc's ETC 100 communication controller. The ETC 100 supports communication between personal computers, between IBM SNA networks, and between public X.25 networks. This local area network is configured as a star. Similar to Protocol Computer's approach of a master/slave relationship between personal computers and converter, the ETC 100 also handles keyboard and screen handling chores. In addition, it emulates IBM 2780/3780 devices in either SDLC synchronous or BSC bisynchronous formats. File handling software is provided in machine language formats for a variety of personal computers as well. Not only does this provide file downloading between host and personal computers, but it also permits files to be transferred between personal computers.



IBM PCs are linked to IBM hosts via Protocol Computer's PCI 1076. The 1076 emulates 3278 synchronous terminals, 3287 printers, and 3276 cluster controllers in a traditional IBM SNA/SDLC configuration.

How the ETC 100 differs from Protocol's approach is in the manner that terminal characteristics are handled. Rather than have personal computers emulate ASCII terminals, the controller maintains a device table listing the actual screen and keyboard characteristics of the IBM PC, Zenith Z89/Z100, Televideo 802, NEC Advanced Personal Computer, Eagle II, and XEROX 820. Functions such as cursor and carriage control can be translated between personal computers as well as translated for synchronous terminal emulation.

Different personal computers can communicate with each other and remote hosts via the controller. Files, passed transparently through the controller, are reformatted by file servers residing within each personal computer. Pascal versions of the file transfer program are available on diskettes for those processors not already supported with machine language versions. Likewise, terminal characteristics are supported for personal computers not already contained in the ETC 100. A user merely enters a series of commands into the controller's system monitor program. These commands describe such functions as control characters and data transfer formats. Thus, designers are free to support any personal computer they choose at anytime they choose. The fear of incompatibility is thus eliminated.

Each ETC 100 contains, in 8K bytes of firmware, the necessary information to convert 110- to 56k-bps asynchronous communications to synchronous SDLC/HDLC data link protocol and SNA/X.25 network and transport protocols. The system monitors download the necessary control data into 16K bytes (expandable to 64K bytes) of system RAM. Data formatting and control transfer for terminal communications is also handled this way.

Up to four personal computers are supported with individual serial I/O ports. A single-token local area network controller arbitrates interprocessor requests for an optional auto-dial modem or printer (either serial or parallel). Besides serving printers and modems, either one or both parallel ports can service synchronous SNA or X.25 communications and bisynchronous SNA transfers.

Using the onboard 6809 microprocessor for character translation, a gateway between SNA and X.25 networks can also be established. Protocol Computer's 1076 handles SNA/X.25 gateways as well, with separate SNA and X.25 converters.

(continued on page 44)

VISUAL brings ergonomic excellence and high resolution to low cost graphics terminals.

The VISUAL 500 and VISUAL 550 are ergonomically advanced terminals that emulate the Tektronix® 4010/4014 but cost only about half as much. And they have 768 x 585 resolution for sharp text and graphic display on a large 14″ screen.

Ergonomic features include a lightweight plastic housing that can easily be swiveled and tilted for maximum operator comfort. A detached keyboard, sculptured keys and non-glare screen are only a few of the many other human engineering advantages characteristic of VISUAL terminals.

Both the VISUAL 500 and VISUAL 550 are compatible with standard software including PLOT 10,™ DISSPLA®, TELL-A-GRAF,® SAS/GRAPH, DI3000/GRAFMAKER, INFOgraf, SPSS,® TEMPLATE,™ GSS-PLOT,® and GSS-CORE.®

Advanced graphics features include: Resident Vector draw, point plot, circle and arc draw, rectangle draw, multiple linestyles and patterns with rectangle pattern fill. Raster scan technology provides fast data update and develops a bright display image. An Auxiliary Port supports printer/plotters and data tablets.

Powerful alphanumeric operation is also provided, displaying 80 characters by 33 lines with separate display memories for alpha and graphics modes. The VISUAL 500 provides selectable emulations of the DEC VT52,® Data General D200, Lear Siegler ADM-3A, and Hazeltine 1500 terminals. The VISUAL 550 is DEC VT-100 protocol-compatible as well as a character or block mode terminal which complies to the ANSI X3.64 standard.

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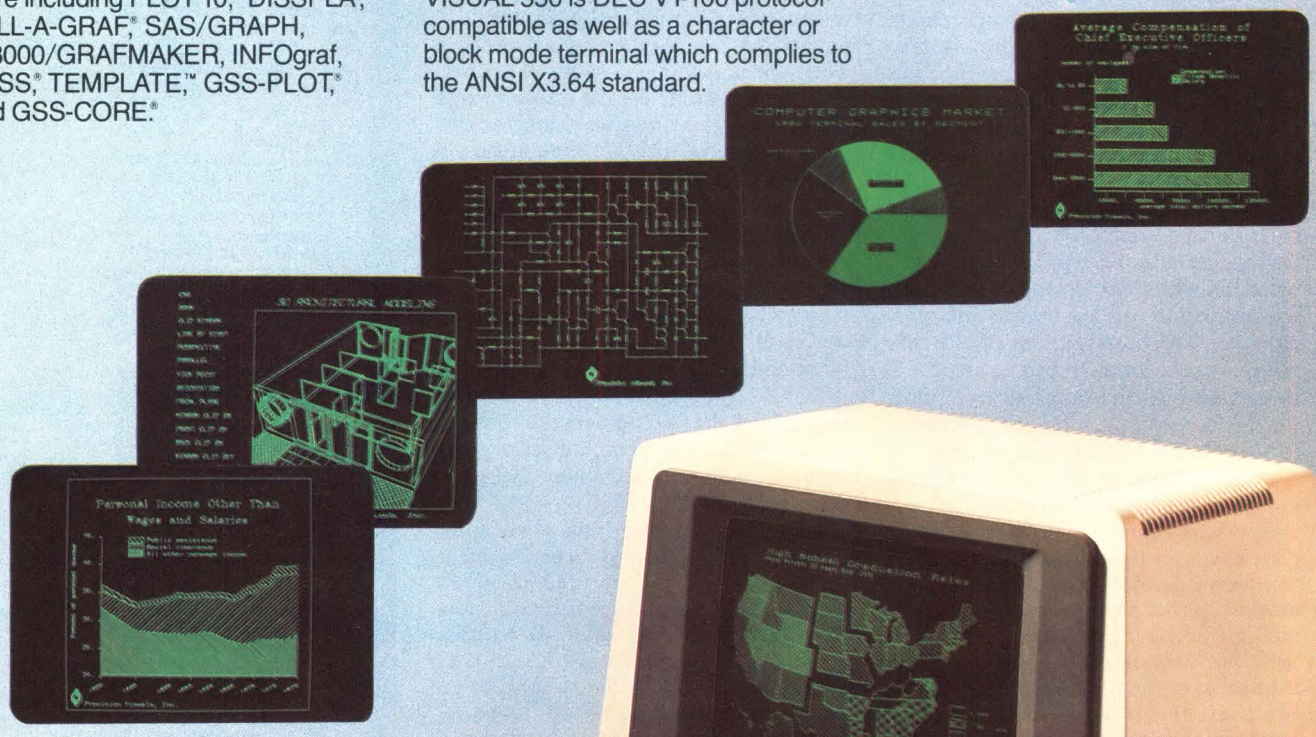
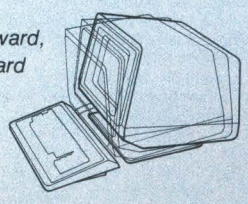
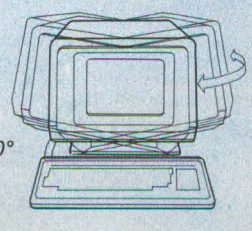




Tilt: 10° forward, 15° backward



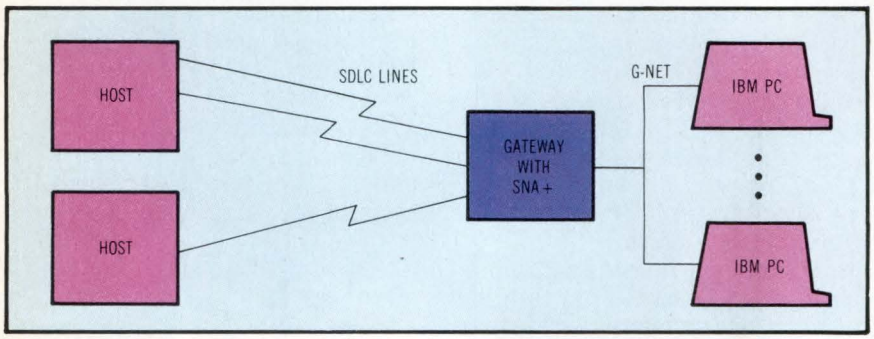
Swivel: 270°

VISUAL 500/550

CIRCLE 28

Providing gateways

(continued from page 42)



Using the SNA + software package and a network interface module, each IBM PC on the G-Net broadband network sends data packets. These packets are suitable for translation on the Gateway Communications gateway processor that handles 3270 terminal emulation and 3274 cluster control functions.

Error detection and retransmission is also provided for both local and remote asynchronous communications. A proprietary frame protocol ensures that messages are received without interruption. It also causes retransmission from the last good byte sent. The proprietary frame protocol can be embedded into SNA/X.25 transmissions for an added measure of security when ETC 100 controllers are at either end. Normal error detection with these protocols will cause retransmission of the entire message. However, SNA hosts without ETC 100 cannot detect the frame protocol since it is embedded into the data packet. Prices for the ETC 100 controller and associated software are available upon request.

Local area networks with baseband buses are linked to SNA and X.25 networks with gateway processors from Gateway Communications, Inc. The company developed an Ethernet-like network with a proprietary carrier sense/multiple access scheme to support up to 255 workstations at 1.4M-bps data transmission speeds. According to the company, this is closer to the synchronous 3270 terminal environment than the maximum 19.2k bps used for asynchronous terminals. The IBM PC is the only personal computer now supported on G-Net. A network interface module containing a Z80B microprocessor and 64K bytes of RAM prepares data packets for transmission on G-Net with appropriate supervisory commands.

The SNA+ software package on the gateway processor allows the personal computer to concurrently establish two SNA display stations and one printer session on the same or different hosts. The user can switch between the two display sessions, with all host display information kept up to date regardless of which session is being displayed. Automatic log on assigns the user to an active host when the SNA boot program is called. The user need only use the screen menus to continue a secondary session. Actual 3270 keystroke/display emulation is handled in the gateway processor, since only data packets are sent between the user and host.

The gateway processor itself consists of a Z80A processor with 64K RAM. A communication executive controls and downloads the necessary device controllers (the system can be configured with 5¼" floppy disk drives and Winchester disk drives), port service routines for up to 16 serial communication ports (RS-232-C or RS-422), and 8 high speed circuits operating at 56k bps.

Additional processor boards are automatically reconfigured when added. These processors are dedicated to handling additional local network capacity or committed as gateways to wide area networks such as SNA and X.25. The executive can download application packages to handle 3270 BSC, 3270 SNA, 3270 DSP, and X.3 ASYNCH. Gateway processors can also serve as host pads for communications between SNA hosts and X.25 public networks.

Prices for the gateway processor and G-Net interface modules are quoted at $1560 and $595, respectively. SNA+ pricing is available upon request. **Computer Development, Inc**, 6700 SW 105th, Suite 200, Beaverton, OR 97005, **Gateway Communications, Inc**, 139 E Alton Ave, Santa Ana, CA 92707, and **Protocol Computers, Inc**, 6150 Canoga Ave #100, Woodland Hills, CA 91367.

Circle 244 **Circle 245** **Circle 246**

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CIRCLE 29

The black facts about c

Fact 1.
Software development is expensive.

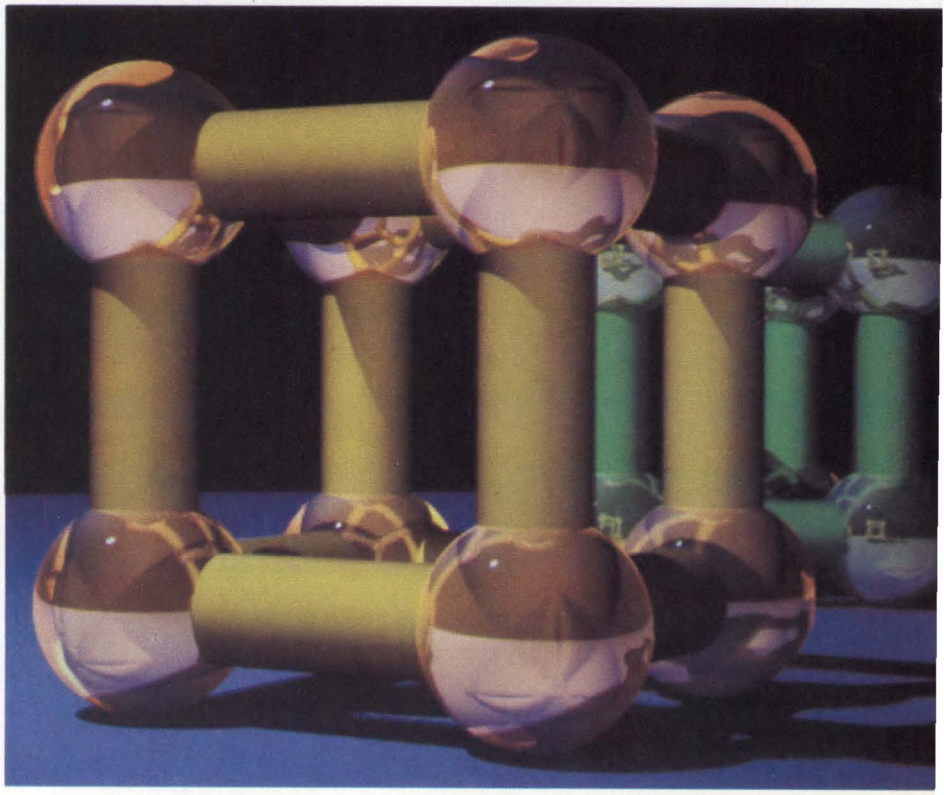
Raster Technologies' Model One graphics systems feature software tools that speed application development. Like an integrated local debugger. Command stream translator. Local command execution. A complete HELP facility. And truly easy to use macro programming. These unmatched software tools save you time and money.

Fact 2.
Software redevelopment is even more expensive.

With Raster Technologies' fully compatible Model One family, you can take advantage of the latest hardware without any software rewrites. This means an easy upgrade to a more powerful product while still using the same graphic commands, program development tools and host library. So the application developed for the best hardware today can run on the best hardware tomorrow. Without modification.

Fact 3.
Performance is a lot more than good specs.

Graphics performance goes beyond pixel and vector timing specs. It is the ability to display a complex picture without having to wait. Provide instantaneous interaction between an application program and its user. And efficiently communicate with a host computer. The kind of total graphics performance you should measure before you buy.



and white olor graphics.

Fact 4. Graphics applications demand flexibility.

The Model One family from Raster Technologies offers maximum flexibility at the lowest cost. Because it lets the user select the combinations of display resolution, color and refresh rates that are right for that particular application. Factors that are different for every application.

Fact 5. Graphics technology is moving fast.

Raster Technologies is dedicated to one business: graphics. All our development efforts focus on advancing graphics technologies. With the latest microcircuitry. The newest and fastest microprocessors. The most advanced display list architectures. And the most innovative pipelined multiple processor designs. All to advance graphics capabilities compatibly. And keep today's customers with us tomorrow.

Fact 6. You should benchmark the Model One.

All three Model One graphics systems – the Model One/25, Model One/40 and Model One/60 – offer the best software development tools. Total compatibility to eliminate software redevelopment problems. Total systems performance. Maximum flexibility. And a dedication to the graphics business.

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Development tool eases complex design tasks

Anticipating the need to support multiple-microcomputer systems, the Rockwell Design Center (RDC) allows users to develop and debug programs simultaneously on four separate processors. The RDC can operate as a standalone development system, or as a satellite terminal to an Intel Isis-II system. In the latter case, the designer can use the familiar host operating system, editor, and mass storage facilities, while using the RDC to download and debug code for multiple-microcomputer systems.

The company notes that multiple-microcomputer systems fit well into dedicated realtime control applications where the traditional approach for software design is to split control functions into speed-dependent categories. Using single microcomputers, the designer must combine interrupt techniques with different sections of the realtime program. Control functions operating at different speeds can be interleaved to operate at their required speeds while still remaining within the microcomputer's capabilities.

Using single-chip microcomputers complicates program design and debugging since processors must jump from one section of code to another. Changes in one section of the program affect the functional timing of others. Development times are difficult to predict, and associated costs tend to escalate.

Multiple microcomputers overcome this liability by dedicating a single microcomputer to each realtime task. Smaller programs, assigned to separate processors, are less costly to design and easier to debug. They minimize the complex timing relationships involved with a monolithic control program. With this approach, different realtime control functions are processed in parallel to reduce the complex interleaving of different sections of code. This results in faster responses for individual functions, affecting overall system throughput.

Conventional development systems work well at integrating hardware and software in single-computer systems, but are not useful for multiple-computer applications. Development tools are typically dedicated to one processor, making it difficult to view other system segments. Consequently, if hardware/software integration problems do appear, it is hard to determine which processor is faulty.

The RDC supports multiprocessor systems with six buses. Four of the buses are dedicated to the target processor systems. The fifth allows I/O functions to be developed using standard board modules, and the sixth acts as the master controller for overall system integration by supervising the activities of the other buses. Such resources as 5¼" floppy disk drives, an optional PROM programmer, a 12" (30-cm) CRT display, a parallel printer port, and 64K bytes of dual-ported memory used for downloading code and actual program execution are provided.

This independent allocation of memory allows software to be debugged while application programs (such as editors and assemblers) are also executing.

(continued on page 50)

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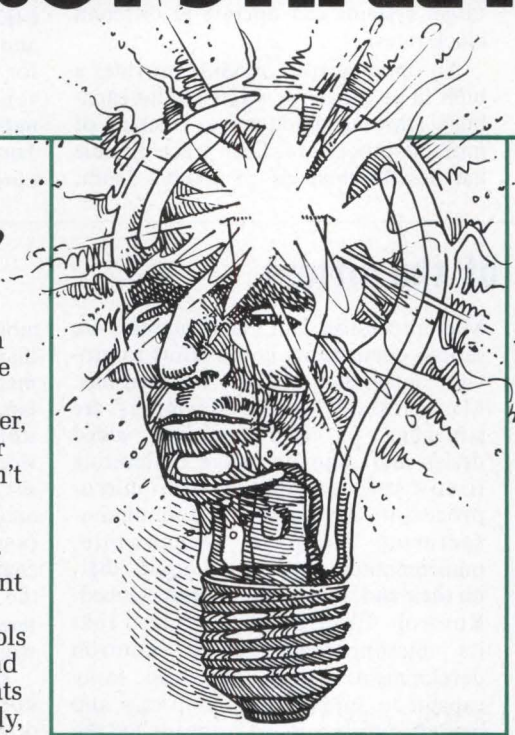

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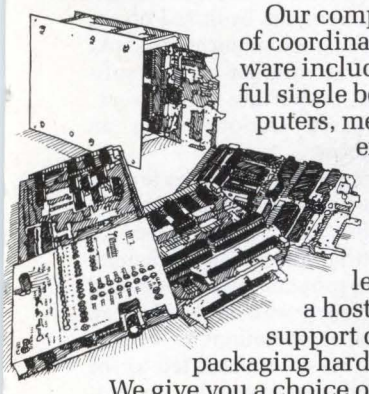

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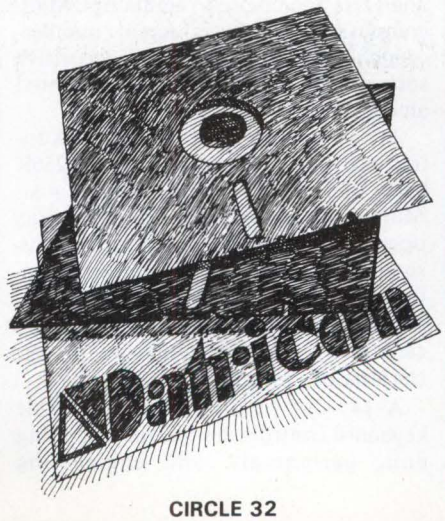

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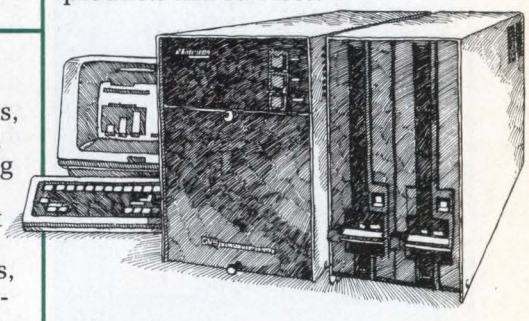

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* OS-9, trademark of Microware

CIRCLE 32

Development tool

(continued from page 48)

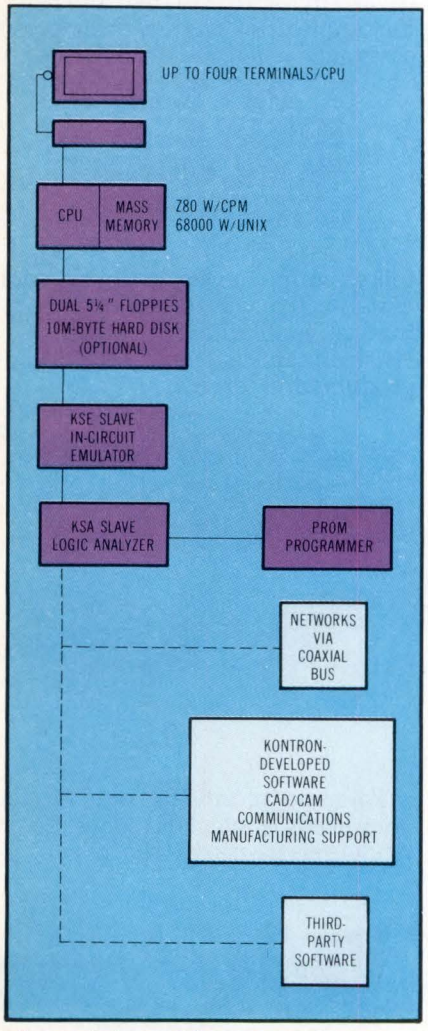
A single-board computer on the system bus acts as a host for software development before programs are downloaded into target personality modules. These modules currently support the company's 6502 based microcomputers. Dual processors (the system CPU and the target processor) allow the user to maintain control even while the target processor is executing a program. Five internal breakpoints, with synchronous outputs, can be used with an external logic analyzer. In conjunction with a user-defined break signal, breakpoint conditions in one processor can trigger a series of events in another processor, providing a basic level of interprocessor communications. More elaborate schemes are left to the designer.

Each personality module provides extensive debugging facilities including illegal opcode detection and memory allocation for I/O operations and ROM emulation. Since target processors need not be the same type, each of the four target systems can operate at different clock rates.

An optional trace module provides a built-in bus analyzer with stimulus capability allowing simultaneous tracking of multiple processors. Each trace module handles 32 channels of 200-bit depth, with four trigger condition levels. To monitor complex timing relationships, trigger conditions between trace modules can be linked to follow program execution in separate processors.

The Rockwell Design Center comes with CRT display and keyboard, two double-density/dual-sided 5¼" disk drives, Forth based operating system, 64K bytes of memory, and both serial and parallel ports. Prices start at $10,950 for the basic system and $1950 for personality modules. **Rockwell International, Electronic Devices Div**, 4311 Jamboree Rd, Newport Beach, CA 92660.
Circle 247

Mini vs micro, survival of the fittest



The modular architecture of the KDS development system allows for flexible configuration of processors, peripherals, and instrumentation modules. Expansion with networks and CAD/CAE software is also possible.

Microprocessors and minicomputers are serious competitors in the effort to provide integrated design workstations. Microprocessor system supporters are struggling to meld computer aided design and computer aided engineering (CAD/CAE) capabilities with microprocessor development and manufacturing support. Meanwhile, minicomputer supporters argue that, on their end, that goal has been reached. Kontrol Electronics believes that its microprocessor based Kontron development system (KDS) can easily expand to support both CAD/CAE and manufacturing support software. On the other hand, First Systems notes that their minicomputers already run such software. In fact, they also serve as a development system with cross-assemblers and target processing.

The key question is, which class of processor is the most effective vehicle for hardware and software integration? Microprocessors allow the distribution of intelligence to end users, and the sharing of instruments like logic analyzers and in-circuit emulators. Minicomputers provide powerful number-crunching capabilities and extensive software tools that are also shared among users.

At the heart of its workstation, Kontron has a Z80 microprocessor with 256K bytes of memory running under CP/M. Moreover, an upgrade to the UNIX operating system will be available this summer that will have a 68000 based central processing unit with 1M byte of memory. In this configuration, the Z80 card acts as the I/O controller for the UNIX based system.

A 14" CRT terminal with detachable keyboard controls the central processing unit, peripherals, and engineering modules. Peripherals include two floppy disk drives, each with 616k bytes of formatted storage, an optional 10M-byte hard disk drive, and a network controller allowing the linkage of several workstations. Engineering modules consist of the Kontron logic analyzer (KLA) and Kontron slave in-circuit emulator (KSE). Because all peripherals and engineering modules can be placed off the bench, the engineer needs only the terminal and target hardware on his workbench.

Through its modular architecture, the KDS can be configured to meet a designer's specific needs. It can also operate as a linked network, sharing peripherals and data bases. Workstations can be fully configured with terminals and local mass storage and engineering modules. A modified terminal with a Z80 processor, instrument modules, and I/O supported by network software can also be used. Up to eight distributed stations can be linked on the 800M-bps KOBUS communications link. MP/M and CP/net are the current software packages supporting the network, with UNIX based stations using an Ethernet protocol.

Although engineering modules are not under network control, the company notes that files can be transferred to workstations that have in-circuit emulators and PROM programmers. Command sequences included with these files can cause the desired operations to be executed and the results transmitted to the sending station. Consequently, the cost per workstation can be reduced by sharing expensive resources such as hard disks and instrument modules. Meanwhile, each workstation has sufficient memory and processor capability to

(continued on page 52)

Retro-Graphics™ and TeleVideo. Lear Siegler. Datamedia. ADDS. And TI.

Now with GEN.II,™ choose a monochrome, gray-scale, or color-formatted terminal to deliver our Tek 4010/4027 compatible graphics.

For a variety of text terminals, the world of cost-efficient graphmaking is now made possible by Digital Engineering's GEN.II Retro-Graphics terminal enhancement — a "snap-in" PC card assembly that provides Tektronix®-based graphics software compatibility.

Once installed, GEN.II will perform monochrome imaging on the TeleVideo® 950, 925, 920, 912, and 910, Lear Siegler ADM 3A, 3A+, and 5, and ADDS VIEWPOINT and VIEWPOINT/3A PLUS; gray scale on TI's Model 940; and color on the Datamedia™ ColorScan™ 10, 30, 60, 70, and 10H.

But best of all a Retro-Graphics enhancement costs only a fraction of what you're paying now for an equivalent graphics terminal: about $1200-1900, depending on the GEN.II model you order.

Introducing GEN.II Retro-Graphics. For superior bit-mapped technical plots and MIS charts.

Our second-generation enhancements provide emulation of the Tektronix 4010 graphics terminal *and* simulation of the Tek™ 4027 color graphics terminal. In standard resolutions on all GEN.II models. And in medium resolution — 640 by 480 pixels — on Color Retro-Graphics™ for the ColorScan 10H.

Because GEN.II products are based on industry-standard Tek protocol, operation is both powerful and familiar to most programmers. Raster-scan images are generated quickly on GEN.II because up to 48 Kb's of graphics intelligence is "resident." This also means costly host-terminal data transmissions are held to a minimum.

English-like commands simplify graphics operation and programming. For example, entering from the keyboard or computer the following command string

!PIE, 200, 90, 120

will cause the upgraded terminal to draw a pie chart sector with a radius of 200 and fill in the area between 90 and 120 degrees. The filled area can be a color in the case of Color Retro-Graphics, an intensity level in the case of gray-scale GEN.II, or a dithered shade in the case of our one-color products.

In addition, GEN.II enables the programmer to draw *polygons* and *vectors. Define* and *shape text characters.* And *recall stored graphs* with similar high-level command strings. And you get all this without the loss of existing terminal features.

GEN.II software compatibility protects your hardware investment.

Since our products are compatible with Tek's 4027 and 4010, GEN.II's performance on utility and applications programs, both present and future, is ensured. Currently, more than 20,000 Retro-Graphics enhancements are successfully being used with DISSPLA® and TELLAGRAF®, PLOT 10™, Template™, DI-3000™, and ILS® graphics programs.

Comprehensive support at every level.

Good ideas mean little if you cannot build on them. Optional interfaces let you hook up a variety of input/output devices of your choice. These include a light pen and digitizers, impact and non-impact serial printers, and video devices. There's solid documentation at every level. And fast, accurate backup by our own customer service and worldwide distribution network.

Digital Engineering's GEN.II Retro-Graphics and your choice of terminal — for economy and compatibility in a sophisticated graphics workstation.

Call us today for full details, demonstration, and the name of your local Retro-Graphics distributor — your "one source" for graphics.

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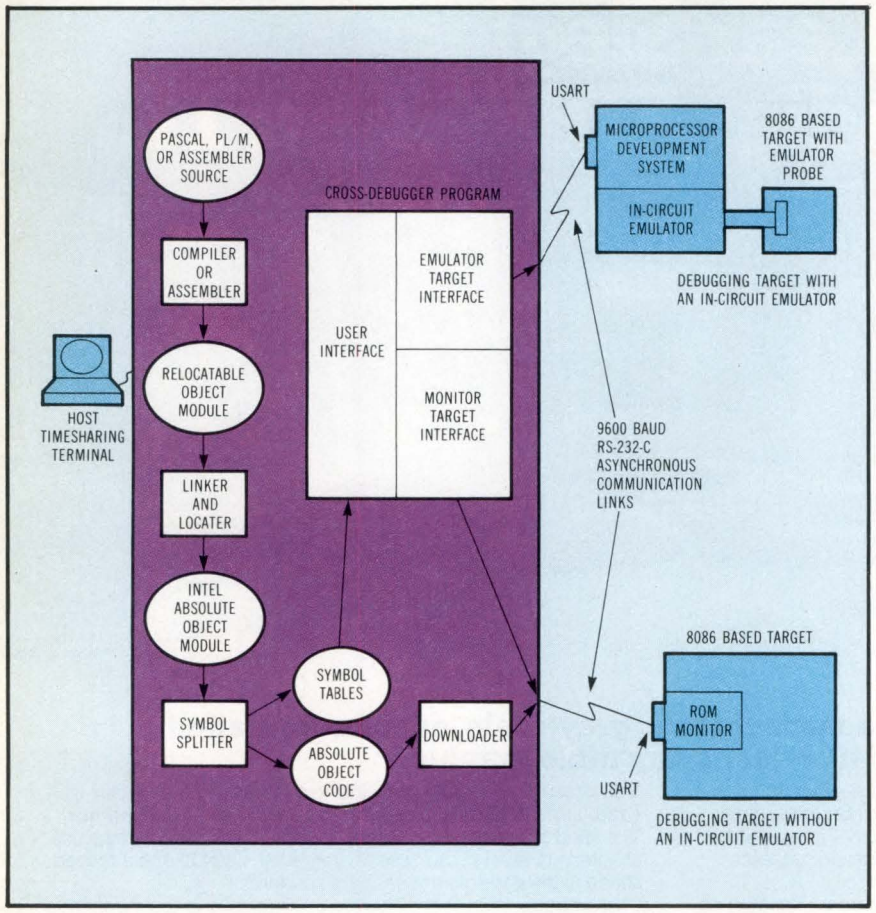
CIRCLE 33

Mini vs micro

(continued from page 50)



Users can do the bulk of their software development chores on a minicomputer with cross-development tools. They can also load debugged code directly into target systems for full-speed execution, or into an in-circuit emulator for hardware diagnosis.

develop code using the provided assemblers, compilers, editors, and linkers.

Users can develop software in either Pascal, which allows programs to be target independent, or assembly level code. Once software has been debugged, Pascal statements are translated into object code for a specified microprocessor with a target compiler. Changing microprocessors requires initiating another target compiler, not a rewrite of the original program.

Designers can edit the assembly source code generated by the compiler, or link in assembly programs from a user-defined library. Thus, Pascal's structure and documentation features can be combined with assembly language speed.

Once code has been debugged and compiled, it is loaded into emulator or target memory for sequential execution. While executing, the designer can use the emulator to trigger the logic circuitry's timing sequence or the microprocessor's breakpoints. The logic analyzer can use interrupts forced by the emulator under terminal commands to determine timing relationships.

Coupling the logic analyzer and emulator modules to a common probe in the microprocessor socket allows the designer to move from module to module without changing operating systems or command routines. The terminal provides a common user interface. Fully debugged code can be burned into ROM, with the PROM programmer, and the prototype circuit board operated at its specified speed. The logic analyzer can detect signal faults too narrowly spaced to be detected by a state analyzer.

The price for the KDS begins at $12,500 for the terminal and CPU chassis, 256K bytes of RAM, and two floppy disk drives. KSE modules start at $5700 with personality modules for popular 8- and 16-bit microprocessors priced as low as $2200. KLAS offer 32, 48, and 64

(continued on page 54)

The Alps Advantage in micro-printers:

"Simply amazing, yet amazingly simple!" That's the usual reaction to our new Series DPG printer-plotters. We think you'll agree they're a good example of the innovative technology that's such an important part of The Alps Advantage. Totally unique and different from any other printer on the market today, they offer an exclusive combination of design and performance features:

Ball point pen writing, for alpha-numerics and graphics. Exclusive ink technology developed by Alps makes possible the use of specially engineered, tiny ball point pens that actually *write*, in 1 or 4-colors, with a simultaneous plotter action in the X and Y-axes. Virtually unlimited capability for character size variations, special symbols, images, even 3-D graphics.

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2¼" or 4½" plain paper. All DPG mechanisms use standard commercially available plain paper: 2¼" for Models DPG 11 or 13 (1 or 4-color); 4½" for Models DPG 21 or 23 (1 or 4-color).

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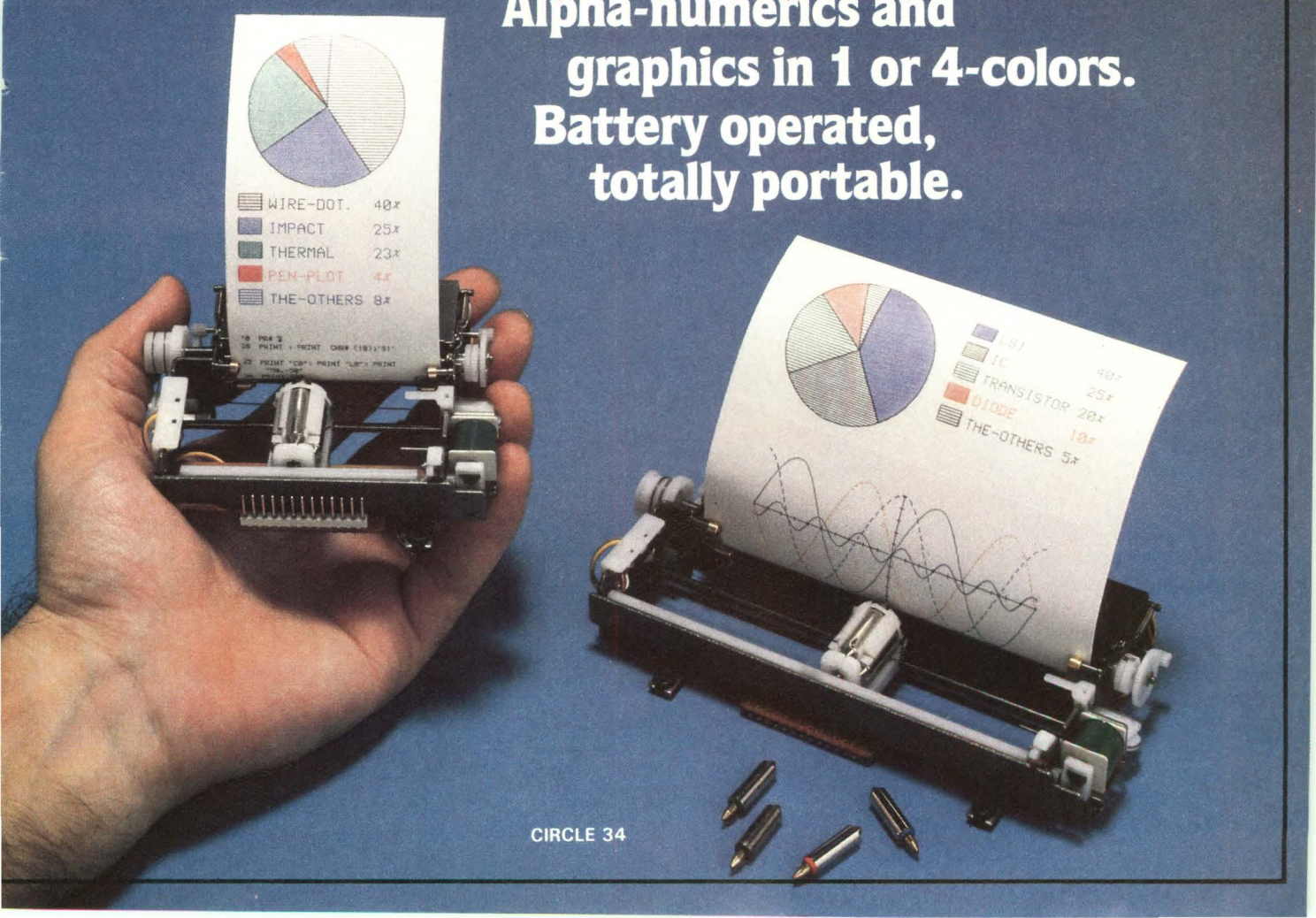


CIRCLE 34

Mini vs micro

(continued from page 52)

channels at prices beginning at $10,000. A PCB routing package is planned for the spring, to be followed by such software packages as list of materials, and engineering change orders.

Such software is already running on minicomputers and mainframe computers, with cross-development tools prevalent on this class of processors. However, in the most dominant techniques—simulation and target processing—the emphasis is on the cross compiler or cross assembler. Usually little assistance is provided for debugging microprocessor code in the host computer, and little interaction when the code is downloaded for target processing.

A cross debugger, available from First Systems, keeps both diagnostic facilities and all symbol tables on the host. The cross debugger can be used with an in-circuit emulator, or the target system, with a small monitor program installed.

Without the aid of an in-circuit emulator, the user causes the transfer of code from the host to target RAM. In a typical session, the user instructs the host cross debugger to insert a breakpoint in target memory at a specified line in the program. A GO command starts the target processor executing at full speed until the breakpoint is reached.

At this time, the monitor program in the target asserts control and uses a serial communication link to inform the host that a break has occurred. A user then has a variety of options: examine or set symbolic variables, registers, or absolute memory locations; remove or insert additional breakpoints; and display a procedure call trace-back. Target execution is then resumed until the next breakpoint is reached.

Together with the company's cross assemblers and cross compilers, the cross debugger supports program development for the Intel 8086. Programs for the iAPX/186 are on the way. Languages supported include the company's Pascal-86 (with Intel's Pascal-86 supported soon) and Intel's PL/M-86 and 8086 assembler. Users can examine the value of full expressions using the syntax of the program being debugged. They can also interact with I/O statements of the target program. Such features as automatic transfer of application data and test files between the target system and host will soon be added.

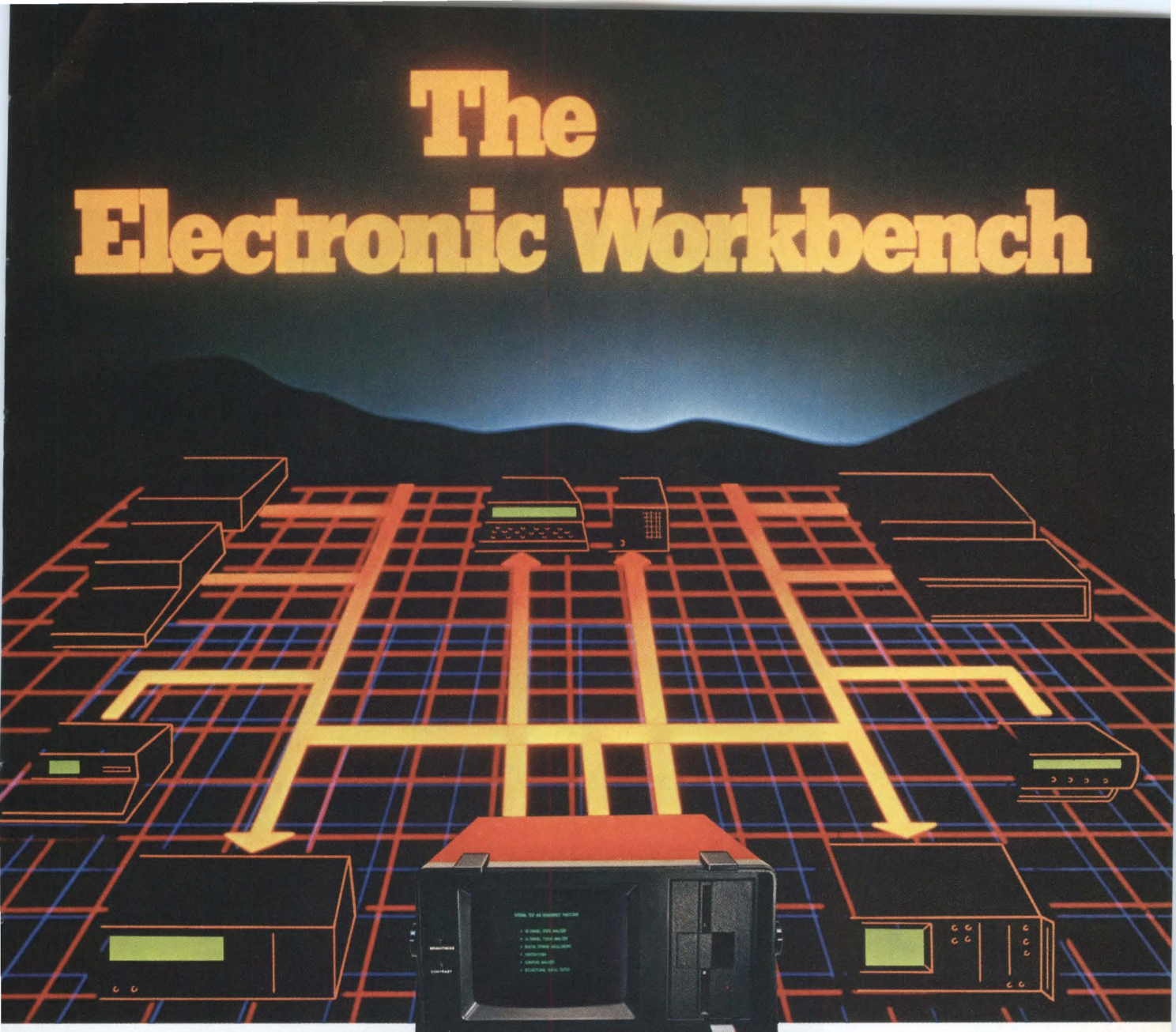
In-circuit emulators can be shared among users via a serial communication link between the host and emulator. An in-circuit emulator would debug ROM code, accumulate traces of recent bus events, and break complex events, such as store operations, into locations within a memory range. With the 100 breakpoints that it provides, the cross debugger can be used to overcome typical large-program limitations of 2 to 4 breakpoints.

Cross debuggers, assemblers, and compilers are available for the DEC VAX-11 family as well as for IBM 370 compatible mainframe computers. Prices range from $6000 to $10,000 with specific prices available upon request. **Kontron Electronics**, 5730 Buckingham Pkwy, Culver City, CA 90230, and **First Systems Corp**, 865 Manhattan Beach Blvd, Manhattan Beach, CA 90266.

Circle 248

Circle 249

The Electronic Workbench



Now, a Logic Analysis System that puts a bench-full of instruments at your fingertips.

The NPC-764. It just makes good sense. When performing logic analysis and other measurement functions, you shouldn't have to face different sets of knobs, switches and dials. That's why we've developed the NPC-764, the Electronic Workbench. Now your analysis tasks are all done the same way—with a familiar ASCII keyboard and easy-to-use, self-prompting menus. Simple keystrokes are all it takes to run tests and record data on disk. And all logic analysis and other internal functions are ROM-based and ready to go on power up. No messy setups. No relearning of multiple instruments.

The NPC-764 includes a 48-channel State Analyzer and a 16-channel, high-speed Timing Analyzer. And, as optional plug-ins, a single-channel Digital Storage Oscilloscope, a 5-function Counter-Timer/Signature Analyzer, and bidirectional Serial Tester.

But the NPC-764 is more than just a multiple-function instrument. It also incorporates a GPIB controller and RS-232 MASTER/SLAVE capability. Standard. A common set of commands lets you control the internal analyzers and any GPIB- or RS-232-compatible devices you include in your setup—pattern generators, emulators, spectrum analyzers, PROM programmers . . .

And that's not all. The NPC-764 is a full desk-top computer, with floppy disk storage and a CP/M® operating system. Use it for general-purpose computational tasks or the execution of commercially available CP/M programs.

The NPC-764, with all its internal measurement functions, requires less than *half* the investment of the equivalent instruments purchased separately. And the ASCII keyboard and menus are so user friendly it sets a new standard for the industry.

Not quite ready for all this capability? Start with our basic NPC-748. It provides exactly the same measurement functions, but 16 fewer state channels and no floppy disk drive. Upgrade easily to the NPC-764 at any time.

There's a whole lot more we'd like to tell you about the Electronic Workbench. For additional information, applications assistance or a personal demonstration, just give us a call: **(800)-NICOLET, (415) 490-8300** (Calif); TWX: **910-381-7030**. Nicolet Paratronics Corporation, 201 Fourier Avenue, Fremont, CA 94539.

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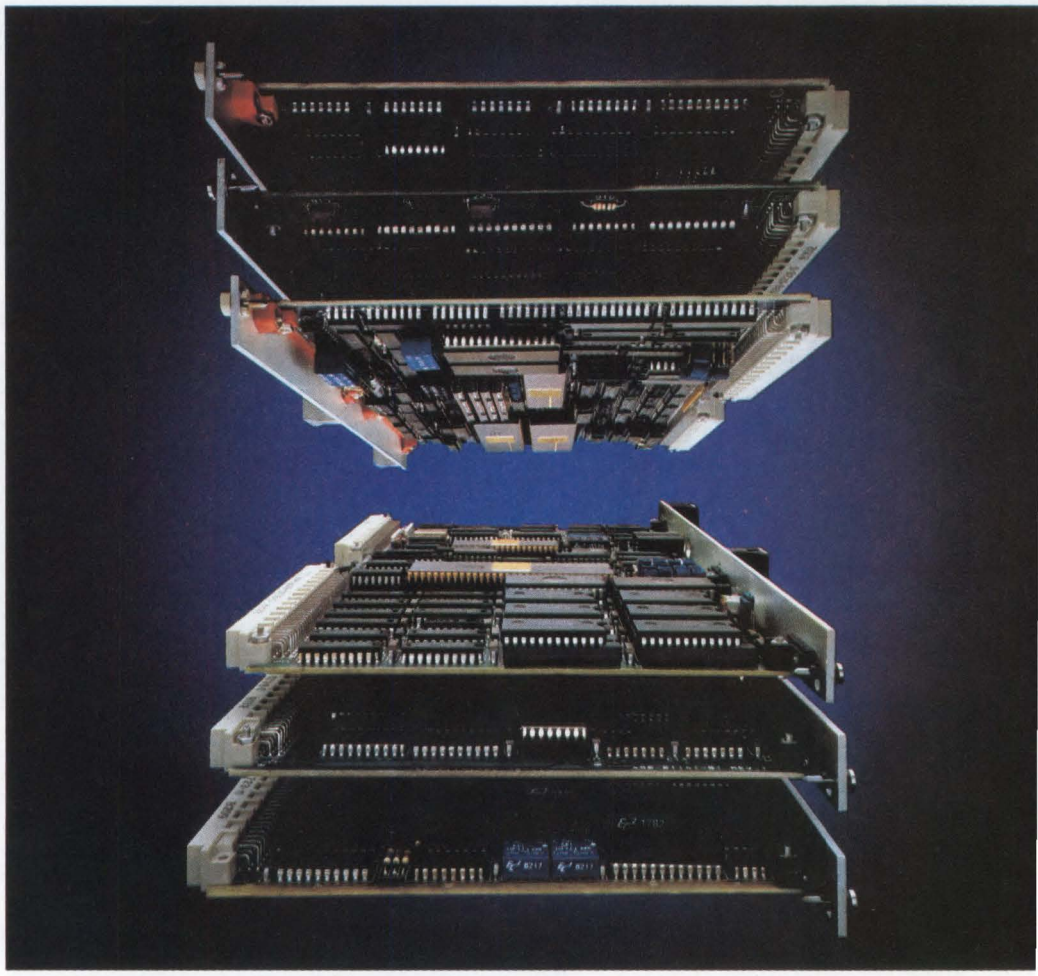
CIRCLE 36

SPRING



BOARDS

Get ready to make a quantum leap past your competition. Because with our ix new 68000 VMEbus boards and UNIX™ operating system, that's exactly what ou'll be able to do. What's more, our new board-level solutions are just the first wave of the multi-user system solutions you'll be able to get from Mostek. So now, here's no reason not to be launching into the future with the Mostek MK68000.

What makes us so confident? First of all, consider the VMEbus, a very compact board structure with truly high-performance timing parameters. And nherent expansion to 32-bit address and data.

Second, look at the boards: VME-SBC: At the heart of it, an 8 MHz MK68000 with upgradeability to 10 or 12 MHz, SIO, BYTEWYDE™ memory and a firmware monitor. VME-SASI: A SASI™ controller with DMA. VME-FLP: A double-sided, double-density floppy disk controller with DMA and sector buffer. VME-SIO: Four-channel (RS-422/RS-232). VME-DRAM: ¼ MB DRAM with byte parity, plus full 32-bit VME interface. VME-MMCPU: Memory-managed CPU with on-board 128K bytes DRAM and full multiprocessor capability.

Third, there's our VME BASELINE System to get you started. It includes three boards (SBC, DRAM, SIO) and a power supply in a 10-slot card cage.

Finally, coming later this year will be UNIX, the high-performance, program-development operating system that opens the door to Pascal and C, as well as our Assembler/Linker software and RADIUS™ development station.

Together, it all adds up to the most powerful and versatile way yet to hit the ground running with a 68000 system solution. To find out more, contact Mostek Corp., 1215 W. Crosby Rd., MS2205, Carrollton, Texas 75006. (214) 466-6000. In Europe, Mostek International (32) 2.762.18.80. In Japan, Mostek Japan KK (81) 3.404.7261. In the Far East, Mostek Asia Ltd. (852) 5.296.866.

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UNITED TECHNOLOGIES MOSTEK

CIRCLE 37

FINALLY, MULTIBUS STORAGE SYSTEMS DESIGNED WITH THE MOST IMPORTANT FEATURE YOU CAN BUY.

FORESIGHT.

The Multibus® market is very quietly growing like crazy.

The 16-bit processors are taking off. The applications are getting more complex. And the users are becoming more and more sophisticated.

If you're one of them, it's probably as clear to you as it is to us that you're going to need high performance disk systems designed to accommodate your future growth.

Rather than make you wait until the last minute, here they are.

Presenting the 770 Multibus Storage Systems from Data Systems Design.

The DSD 770 Multibus storage systems offer you the kind of flexibility and performance you'll need, not only now, to get your product to market quickly, but also later, to keep pace with your growing needs.

The systems come in four basic configurations: An 8" 10 Mb or 40 Mb Winchester with either a ¼" streaming tape for back-up, or a 1 Mb floppy for low cost software distribution. All competitively priced.

And they all fit nicely into a 19" rack because each system is only 5¼" high.

But the real magic comes courtesy of our new multi-function Multibus controller/interface.

Multiple choice on one Multibus board.

Our new controller/interface contains a Winchester disk interface that will handle two drives of up to 40 Mb each. An interface for ¼" streaming tape. And a floppy drive interface that can control two 1 Mb floppy drives.

Plus data separation.

32-bit ECC for high reliability.

Automatic self-test. Self diagnostics.

Full compatibility with IEEE 796 standards.

Intel® iSBC® 215 and iSBX™ 218 emulation.

24-bit addressing.

A high speed internal bus and pipelined architecture with a dual port buffer to move data at non-interleaved speeds. And a read/write sequencer to go with it that's capable of running faster than any 8" Winchester drive likely to come along for a long time.

But here's the kicker. All this takes up just one slot in your Multibus backplane because it all comes on just one board.

And for those of you with unique packaging requirements, our controller/interface board is also available by itself, for 8" or 5¼" disk drives.

Hindsight will prove you right.

We don't expect you to buy systems with an eye to the future without looking into service and support.

But this is one area we were unable to improve upon. Because we decided we should offer the same kind of efficient service and intelligent support that's made us a leading storage system supplier in the DEC®-compatible market.

That kind of service includes our exclusive on-board HyperDiagnostics™. Remote diagnostic assistance. Rapid Module Exchange™. And the most comprehensive, yet inexpensive extended service program in the business: HyperService™, now with guaranteed twenty-four hour or less module swap.

All backed by support which, according to our customers, is second to none.

It pays to plan ahead.

Given the opportunity all this presents, you're probably going to want to know more about the 770's. And the new Multibus controller/ interface that goes with them.

We can supply you with a comprehensive twelve-page data sheet, that tells you everything you need to know about both, and it's yours for the asking.

So call us today.

Better yet, call us yesterday.

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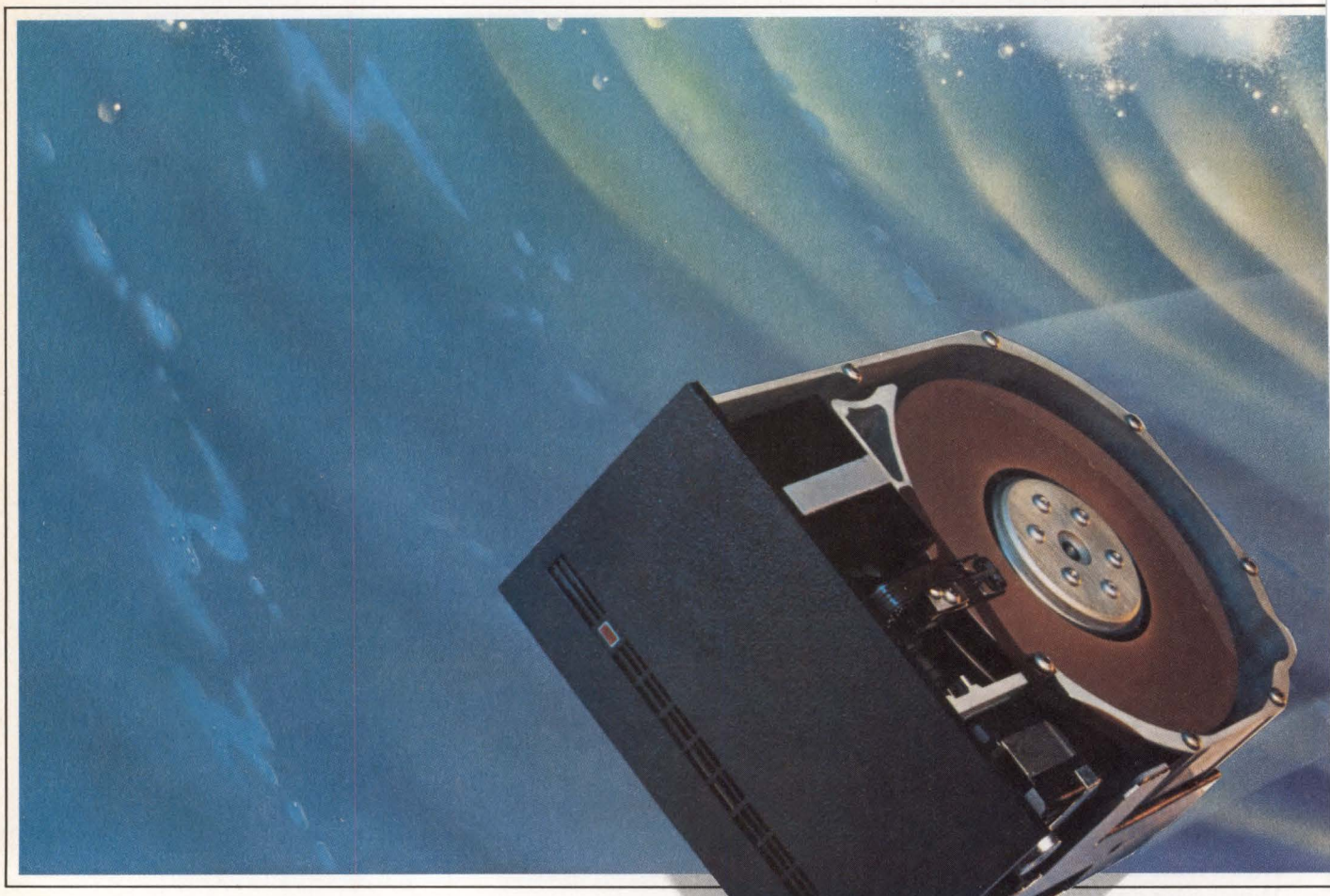
The Seagat



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The ST400 Series offers the right capacities. 6.38, 12.76 or 19.14 megabytes (unformatted). All use the same industry-standard ST506 controller and matching mini-floppy form factor for easy upgrade.

The right features.

All use manganese-zinc heads, advanced stepper motor, metal band actuator, open loop head positioner, and patented air flow spindle pump. An onboard microcomputer provides buffered seek and fast step algorithm for an average seek of 85 milliseconds, including settling time.

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Seagate backs the ST400 family with a full one year warranty, our industry-leading "105% Seagate Guarantee," and the world's biggest support team devoted entirely to 5¼" Winchesters.

Meeting special needs.

Looking for faster, more reliable removable storage? Go with our new ST706

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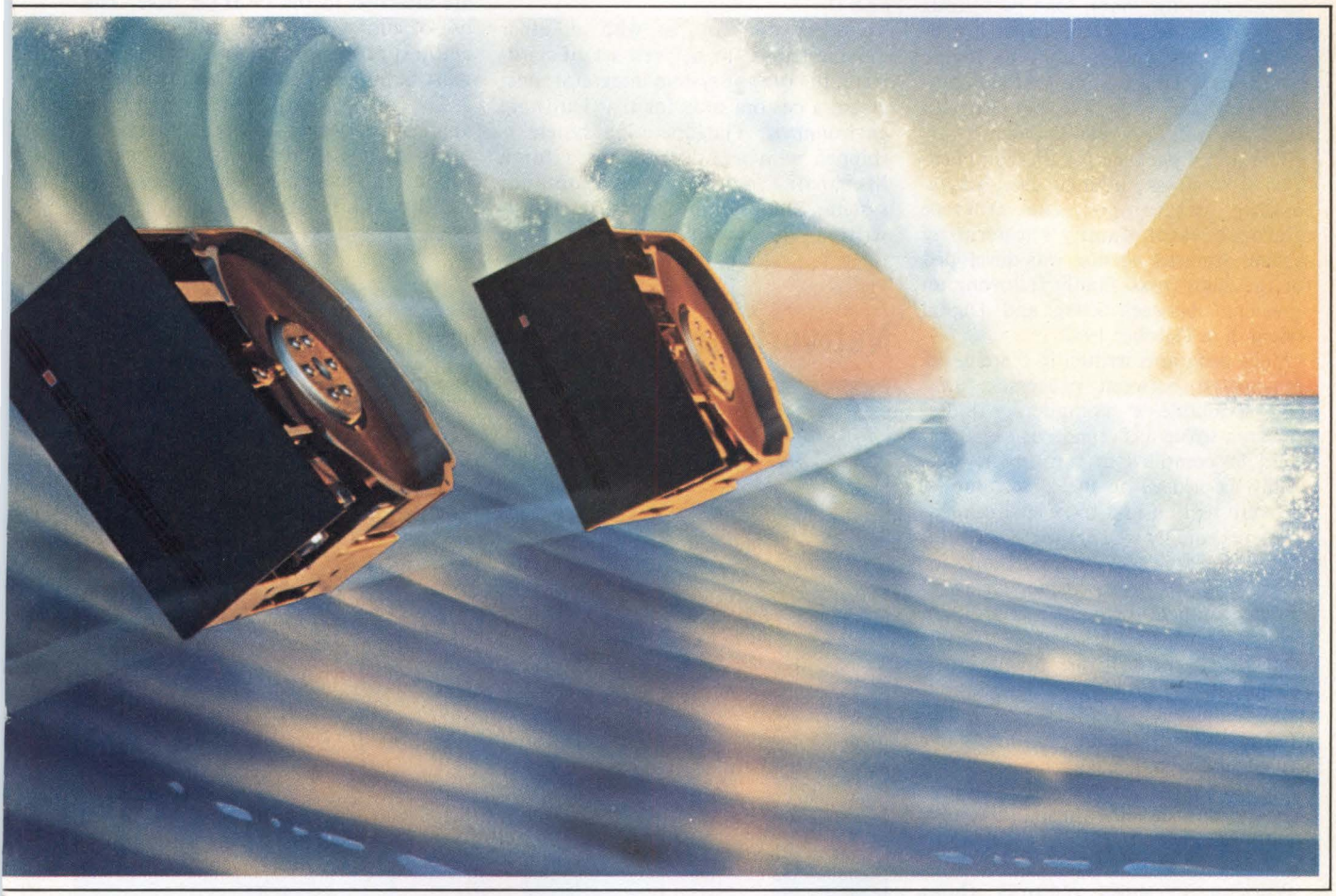

removable cartridge drive. Need a more compact drive? Pack more data in less room with our new ST206 half-high Winchester. Both new drives store 6.38 megabytes (unformatted) with reliable bit and track densities.

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Selection. High volume delivery. Quality. Competitive pricing. So go with the tide. Call Seagate.

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	ST406	ST412	ST419
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"Turning the tide in disc technology"

CIRCLE 39

CP/M spreads to 16-bit processors and beyond

Using the C programming language as a vehicle, Digital Research, creator of the CP/M operating system, is opening up new avenues for CP/M. One path leads CP/M to a wide range of 16-bit microprocessors, and another allows software authors to write programs that are compatible not only with CP/M, but also with Bell Labs' UNIX operating system.

The initial package for these applications is CP/M-68K, a single-user, single-tasking version of the MC68000 microprocessor family's operating system. Another version was developed for the Zilog Z8000 family following an agreement between Zilog and Digital Research in October 1982.

Since programs written in C are easily transported between processors that have available C compilers, Digital Research wrote a C version of CP/M that could be compiled to run on the 68000 family as well as on the Z8000. Since C software written in a UNIX environment now runs equally well in the CP/M world, Digital Research sees an opportunity for synergy. First, UNIX provides an excellent environment for multi-user program development with a great array of tools available to the software professional. Second, CP/M provides a less intimidating environment for the end user while still supplying many useful utilities and occupying much less memory. Thus, sophisticated software development projects can now be undertaken in the UNIX environment with the results easily transported to the CP/M world.

Version CP/M-68K requires about 24K bytes of memory, depending on the basic I/O system (BIOS) size. This BIOS is the only part of the operating system that needs modification to adapt to a given hardware environment. CP/M-68K, however, can manage up to 16M bytes and handle a maximum disk capacity of over 8G bytes.

To simplify CP/M software conversion, the CP/M-68K file system is compatible with all other CP/M and MP/M file systems, including CP/M-86. Digital Research says that high level language programs can be recompiled with little or no modification, while assembly language programs, obviously, must be recoded.

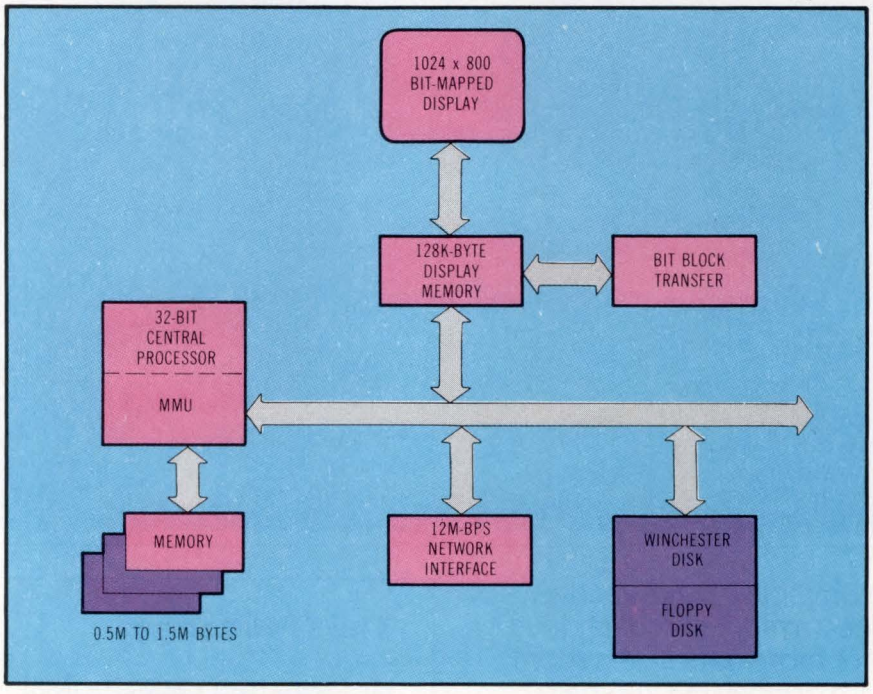
The CP/M-68K package includes a C compiler and runtime library compatible with UNIX Version 7. Also included in the package are a 68000 assembler, a linker for both relocatable and absolute load modules, and a utility to convert CP/M-68K load modules to Motorola S-Record form. In addition, a version of CP/M-68K cross-development tools is available to run under UNIX on a DEC PDP-11 or under VMS or UNIX on a DEC VAX-11.

To adapt CP/M-68K, as with all other CP/M versions, to a given set of hardware, the OEM or system integrator must create a custom BIOS for that hardware environment. The operating system is shipped with a BIOS configured for a Motorola EXORmacs development system, along with one working BIOS written in assembly language and another written in C. Further customization is possible through use of resident system extension (RSX) modules, which are attached to the CP/M-68K base. The use of coprocessor chips, such as math and text processors, is not restricted but must be supported by the application.

The emergence of CP/M in C and UNIX applications leaves open the possibility of its use in virtually any processor that supports a C compiler. **Digital Research**, PO Box 579, Pacific Grove, CA 93950.
Circle 250

MICROPROCESSORS/MICROCOMPUTERS

Network node puts supermini on desktop



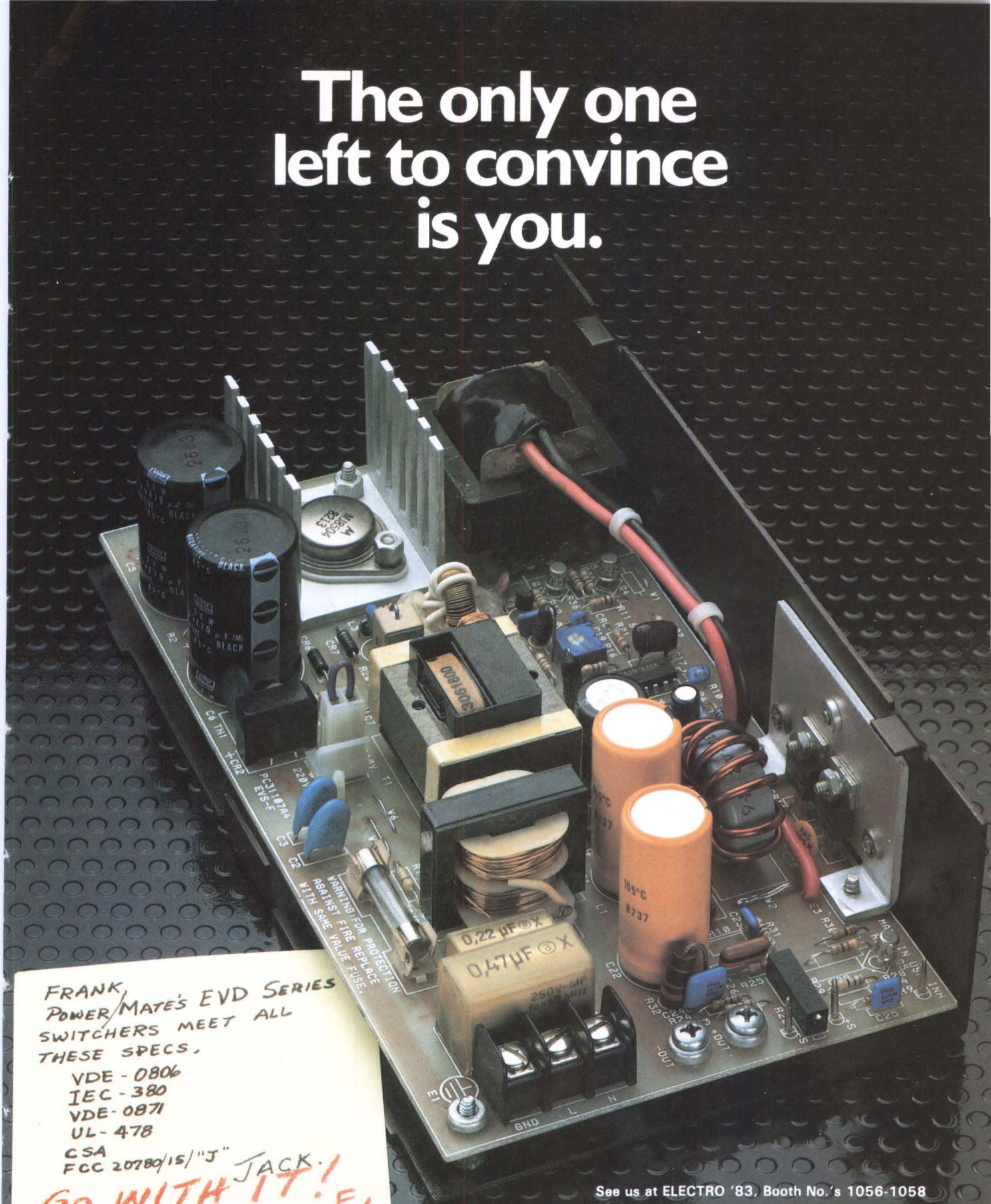
Based on the MC68010 microprocessor, DN300 delivers a 16M-byte virtual memory address space with 1.5M-byte main memory. Also included in a desktop package are high performance graphics and access to a 12M-bps network.

Eliminating the dependency on mainframe access, Domain network nodes make technical professionals independent by putting them in control of their own time. Apollo's DN300 computational node supports this concept by replacing mid-range superminis with a desktop unit. Operating alone or as part of a 12M-bps local area network, the unit costs 20% to 30% less than competitive units. Resources such as mass storage, communication gateways, and printers can be shared across the network as though they were locally connected.

To achieve standalone power, the DN300 uses the Motorola MC68010 microprocessor and DMA controller. This virtual memory processor, combined with memory management unit (MMU), is claimed to deliver the power of a VAX-11/750. The dedicated VLSI processor supports up to 15 concurrent user processes. Each process gains a virtual address space of 16M bytes from the integral MMU. This MMU dynamically maps 24-bit virtual addresses into a 22-bit physical memory address space

(continued on page 64)

The only one left to convince is you.



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CIRCLE 40

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Network node

(continued from page 62)

and maintains protection and usage statistics for each 1024-byte page of data.

The station is built around two printed circuit boards that contain the CPU with 0.5M-byte main memory, memory management hardware, display controller with 128K bytes of dedicated display memory, and network interface. The network interface provides a 12M-bps baseband data rate, made possible by self-synchronizing hardware bit stuffing techniques, ring topology, and token passing arbitration. Two separate RS-232-C ports provide independent, software selectable transmission rates from 50 to 19.2k baud.

The integral display provides a horizontally oriented 17″ (43 cm) screen with 1024- x 800-pixel resolution. The 15 concurrent virtual memory processes can be viewed using the screen in a multiwindow mode; highest resolution is obtained by using the entire bit-mapped raster scan display. A dedicated 128K-byte dual-port display memory performs interlaced refresh at 80 kHz.

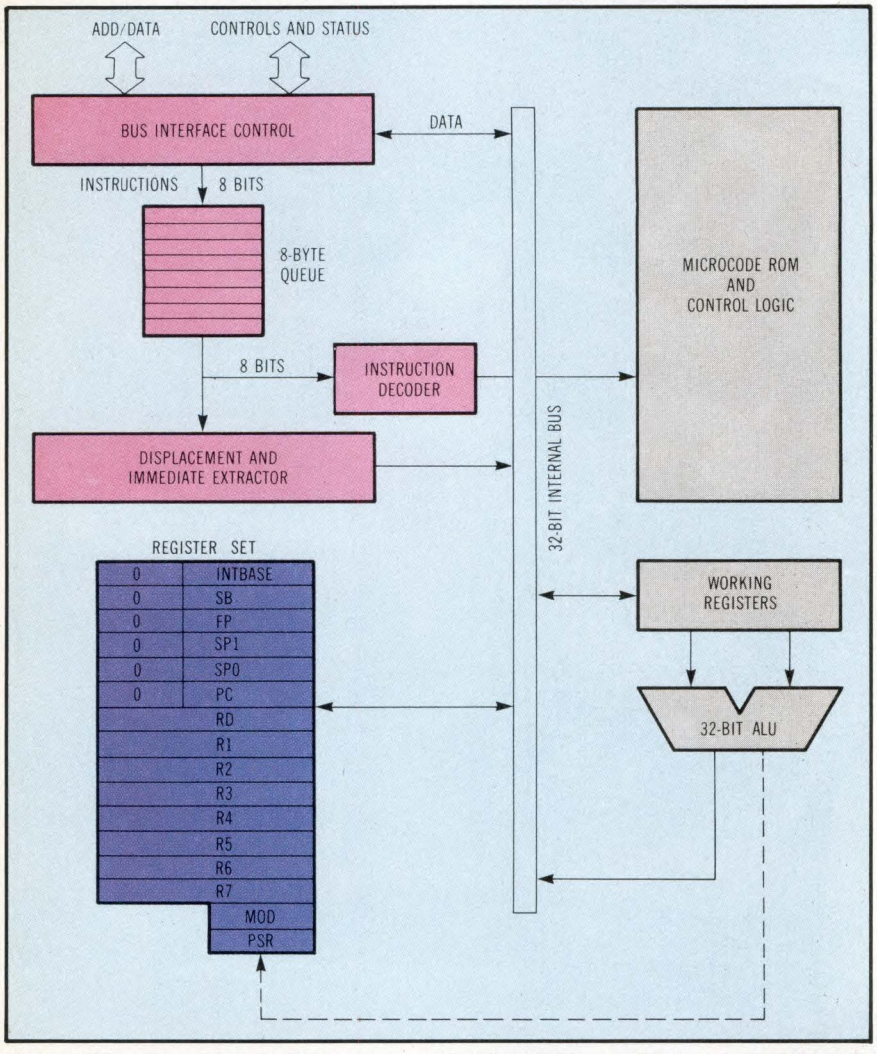
Local Winchester and floppy disk drives can be directly connected to the station. An 8″ Winchester supplies 34M-byte capacity and a 1M-byte/s DMA transfer rate. The 1.2M-byte double-sided, double-density 8″ floppy provides a 500k-byte/s DMA transfer rate.

Standard software for the DN300 includes the Aegis operating system which provides network-wide virtual memory. Optional are FORTRAN 77, Pascal, C, and the SIGGRAPH Core graphics library. In addition, AUX provides a software environment based on UNIX System III; D3M is a distributed data management system; and DOMAIN X.25 supports the X.25 packet switching communication protocol.

Prices for the node range from $10,449 to $27,900 depending on the amount of main memory and mass storage. **Apollo Computer Inc,** 15 Elizabeth Dr, Chelmsford, MA 01824.

Circle 251

32-bit architecture for 8-bit systems



National Semiconductor's 8-bit NS16008 maintains 32-bit architecture in its internal data paths, ALU, and general registers, along with a 24-bit address that gives a 16M-byte linear addressing range. The instruction set facilitates high level language programming.

An 8-bit CPU with many of the performance features of a 16-bit device is National Semiconductor's claim for the NS16008, the latest member of the NS16000 microprocessor family. The device has an 8-bit data bus, multiplexed with the low eight lines of its 24-bit address bus, while maintaining a full 32-bit architecture in its internal data paths, ALU, and general registers.

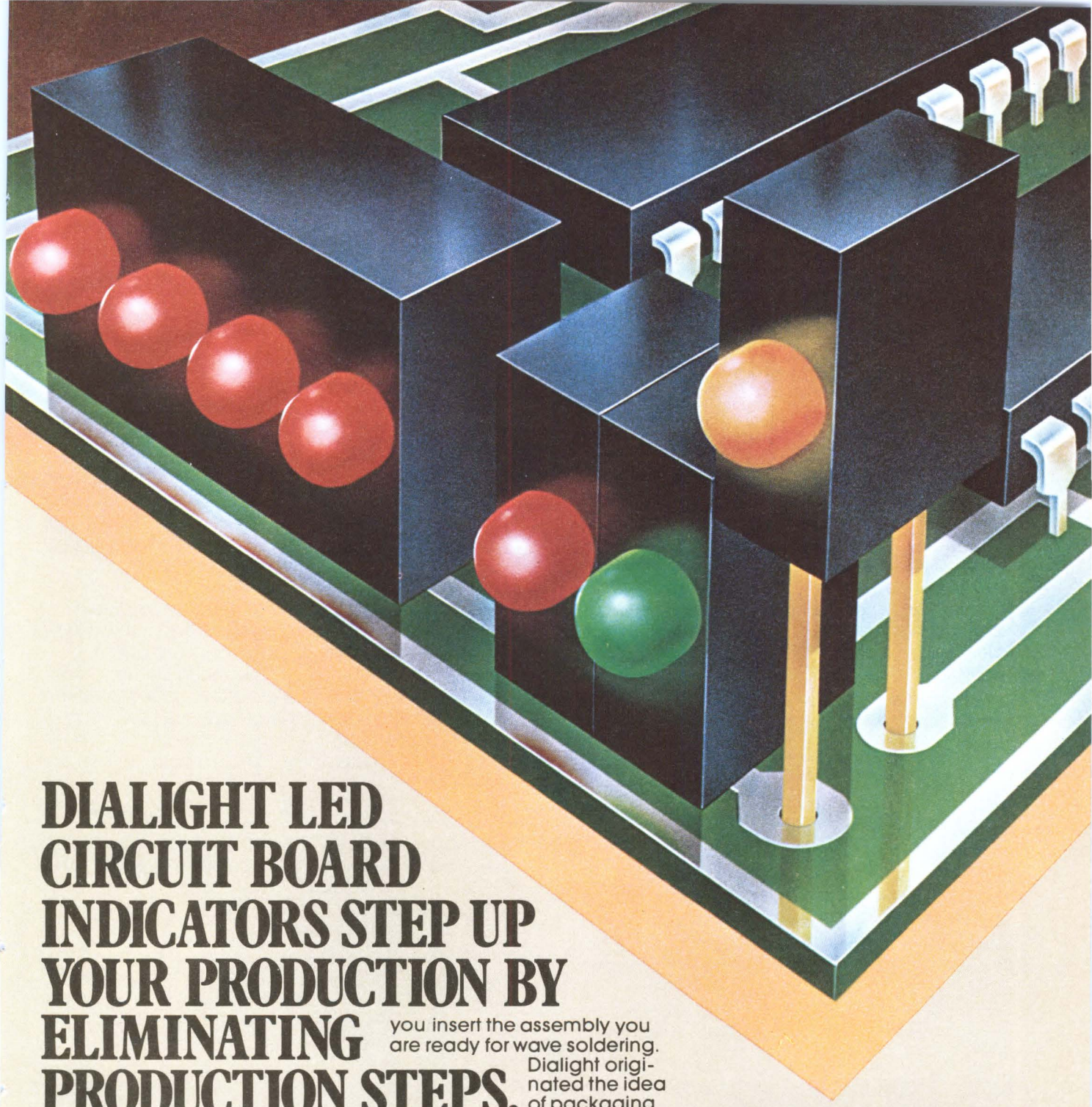
In building new systems, designers are often faced with difficult choices in deciding whether to use an 8- or a 16-bit microprocessor. An 8-bit device results in lower overall systems costs by limiting chip counts. On the other hand, 16-bit CPUs have wide addressing ranges and more flexible, powerful instruction sets.

The NS16008 is offered in a 48-pin DIP. Pins AD0 through AD7 are multiplexed to act as either an 8-bit bidirectional data bus, or as the low-order 8 bits of the address bus. Together with pins A8 through A22, they also make up a 24-bit address bus, which provides the NS16008 with a 16M-byte linear addressing range.

Most previous 8-bit CPUs provided only 16-bit address buses and were limited to a 64K-byte address space. The NS16008 avoids this 64K limitation and the time and circuitry necessary to implement bank switching—the traditional way 8-bit devices have overcome it.

Internally, the NS16008 has a complete 32-bit architecture (Figure). A with other members of the NS16000 family, the register set consists of six 24-bit special-purpose registers and eight 32-bit general purpose registers. The general registers can hold byte, word, or double-word data or addresses and can also hold quad-word (64-bit) data when used as even/odd pairs.

(continued on page 67)



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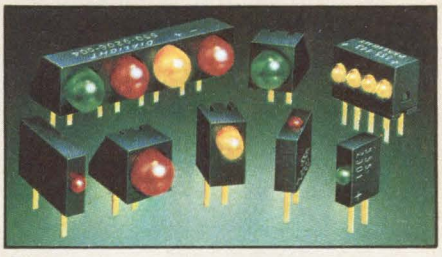

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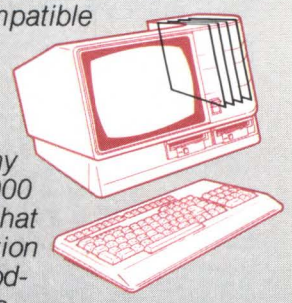

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32-bit architecture

(continued from page 64)

The dedicated registers provide three address registers: INTBASE, which points to the beginning of a program or routine; static base (SB), which points to the frame pointer (FP), which can be used to point to local variables for a currently executing subroutine. Two stack pointers (SP0, SP1) and a program counter are also included in the special-purpose registers.

The NS16000 family provides a number of instruction set features designed to ease high level language implementation. Memory relative addressing allows any general purpose register's contents to be used as an offset from a fixed address. This permits a routine or control to pass data to any other routine located within an 8M-byte memory area.

A CASE instruction allows multiway branching, depending on a general purpose register's contents (up to 2^{32} possibilities). Bit-manipulation instructions handle Boolean operations and control of peripherals via parallel ports, and string instructions allow search, movement, and translation operations to continue until (or while) any given character class is found.

The NS16008 also eases the assembly language programmer's job by the symmetry and orthagonality of its instruction set. Any data type can be used in any instruction, with any addressing mode, and with any source or destination. Thus, the instruction set is easier to remember, requires less research in manuals to determine restrictions, and generates less code. High level language compilers are therefore easier to write, smaller, and faster.

Single-address machines, such as most 8-bit CPUs, require that arithmetic and Boolean operations be carried out on a specific register's contents, thereby requiring a great deal of data movement both from and to the accumulator. The NS16008 provides general 2-address capability, allowing addition, subtraction, multiplication, division, and other operations to be carried out while both operands are in memory, again saving both time and memory.

While the NS16008 has many of the characteristics of a 16-bit CPU, it is not a 16-bit device and is not suited specifically for 16-bit applications. Applications that need efficient virtual memory support, or high throughput, like CAD/CAM, require other microprocessors such as the NS16032 (and its CMOS version, the NS160C32) or the NS32032.

The NS16008 is best suited to applications that deal with byte-wide (8-bit) data such as CRT terminals, word processors, and dedicated controllers. Documentation, training, software products, and developmental support are available from the company.

Sampling of 6-MHz parts will begin soon, with production quantities available in the third quarter of 1983. Price is quoted as $100 in quantities from 1 to 24. The 10-MHz parts will be sampled in September 1983, with production scheduled for late 1983 or the first quarter of 1984. **National Semiconductor**, 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 252**

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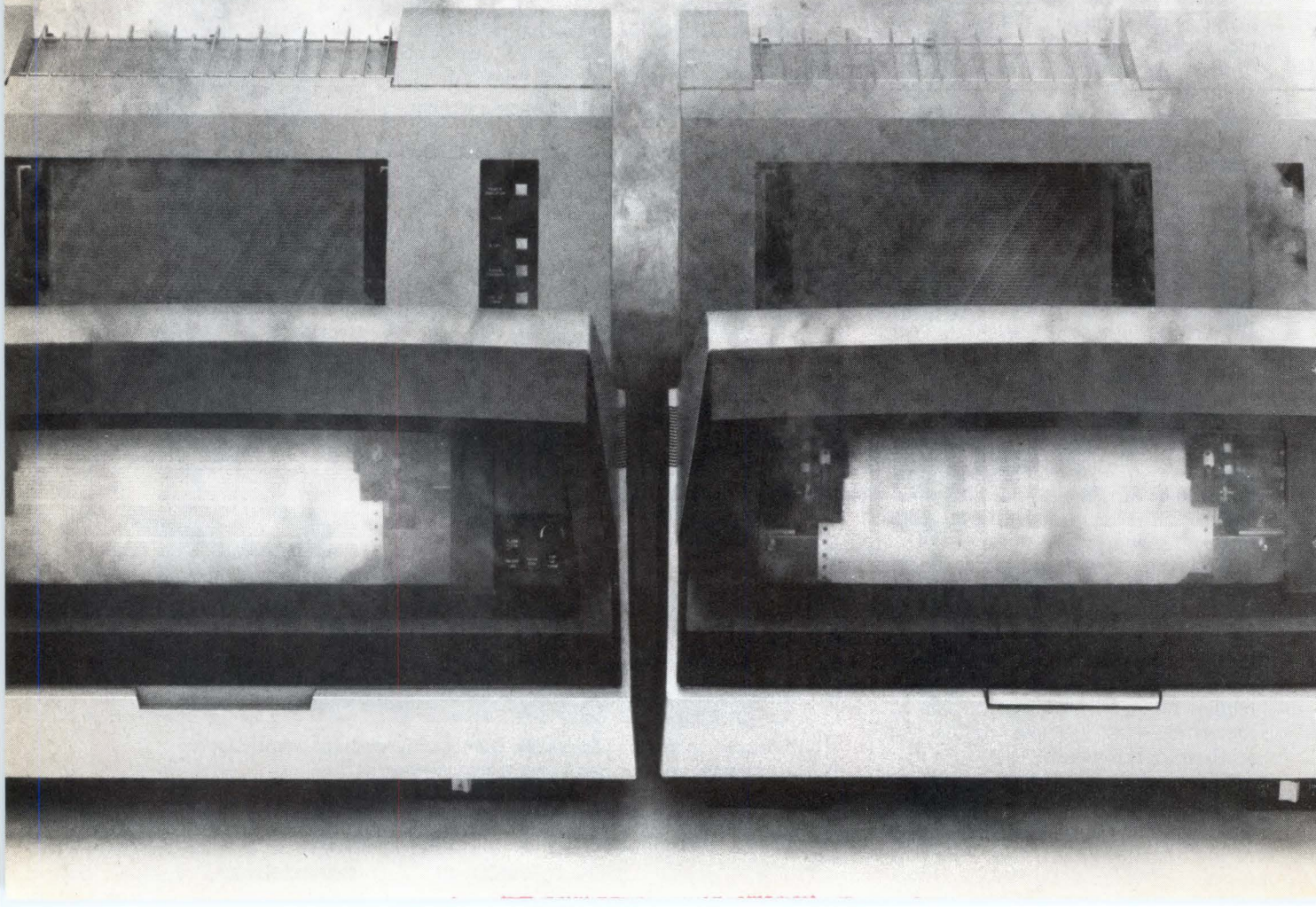

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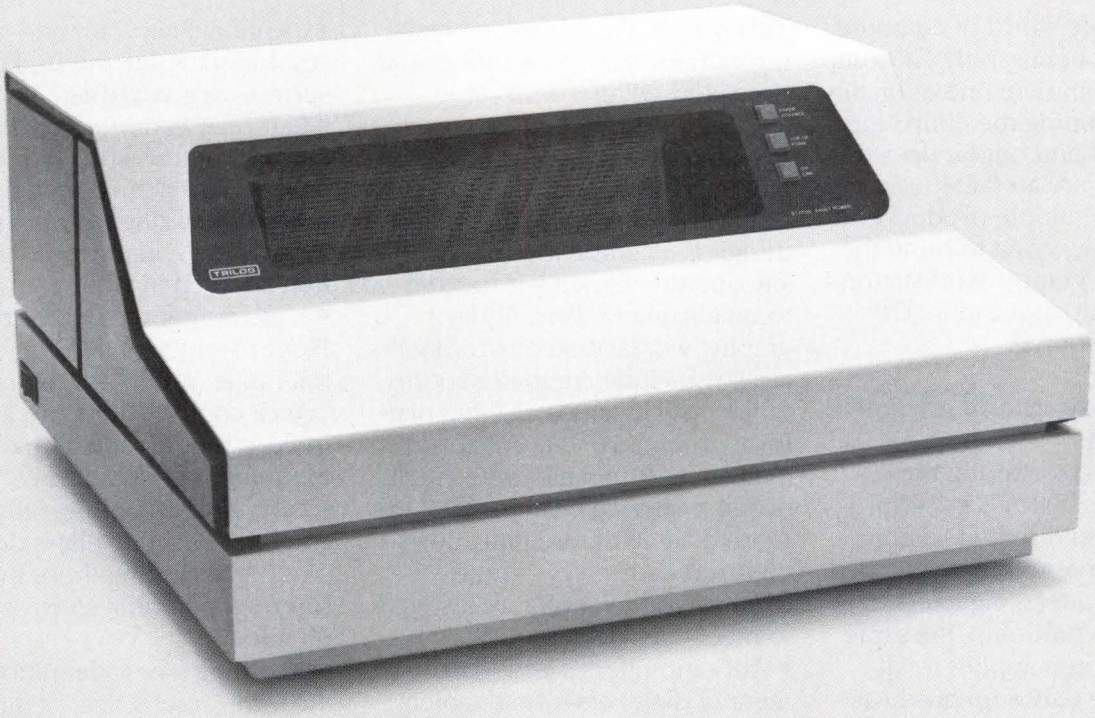

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The CalComp Computer Graphics Glossary

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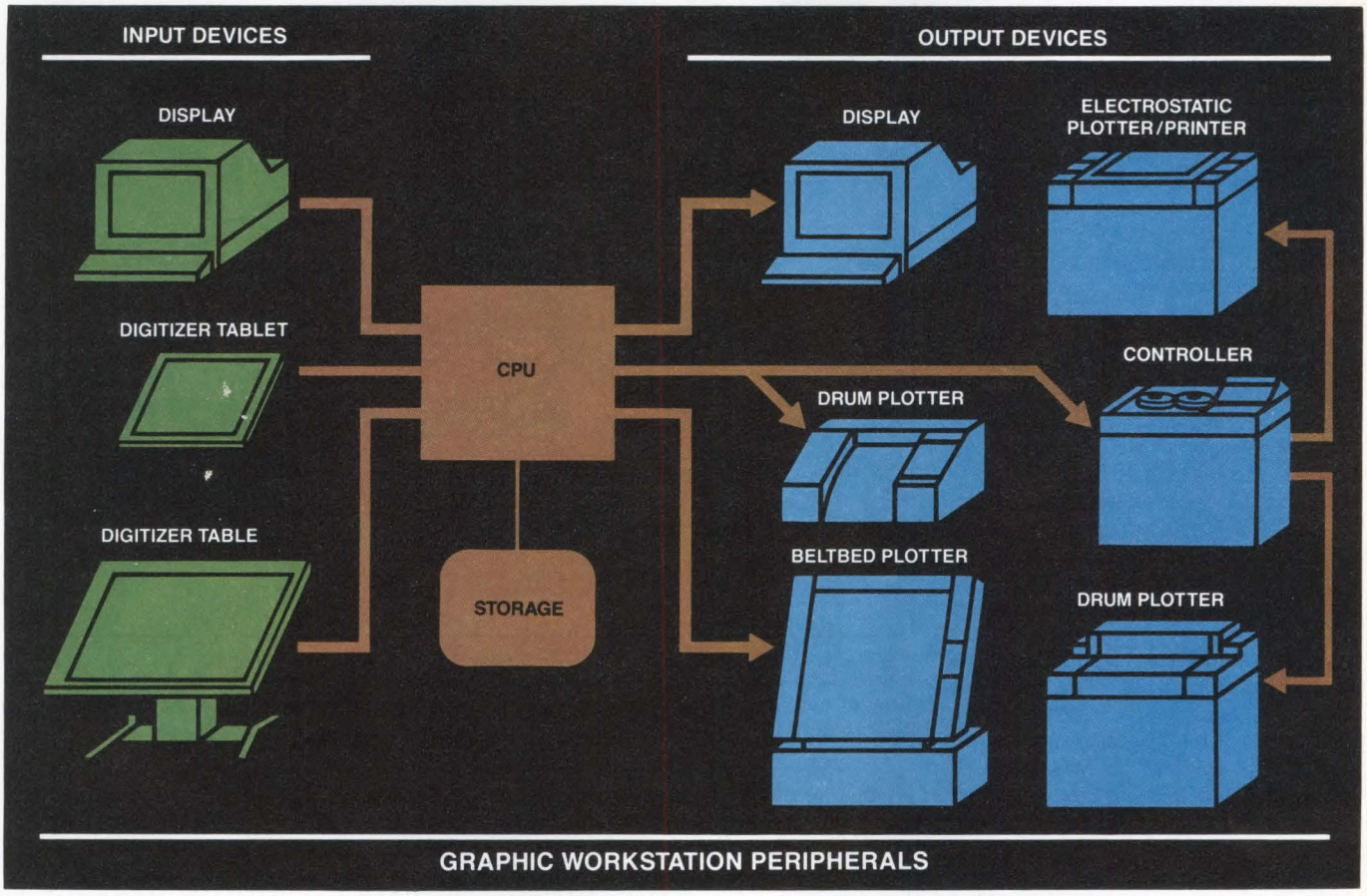

Displays:
Resolution - 640 x 512, 1024 x 768, 1024 x 1024
Models - Color or Monochrome
CPU - Dual Motorola MC68000

Digitizers:
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Tables - 24″ x 36″ to 44″ x 60″

Drum Plotters:
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Speeds - 4.5, 10, 30 Inches/Second

Flatbed Plotter:
Plotting Area - 48″ x 82″
Speed - 30 Inches/Second

Beltbed Plotters:
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CIRCLE 46

Coprocessor allows true text preparation

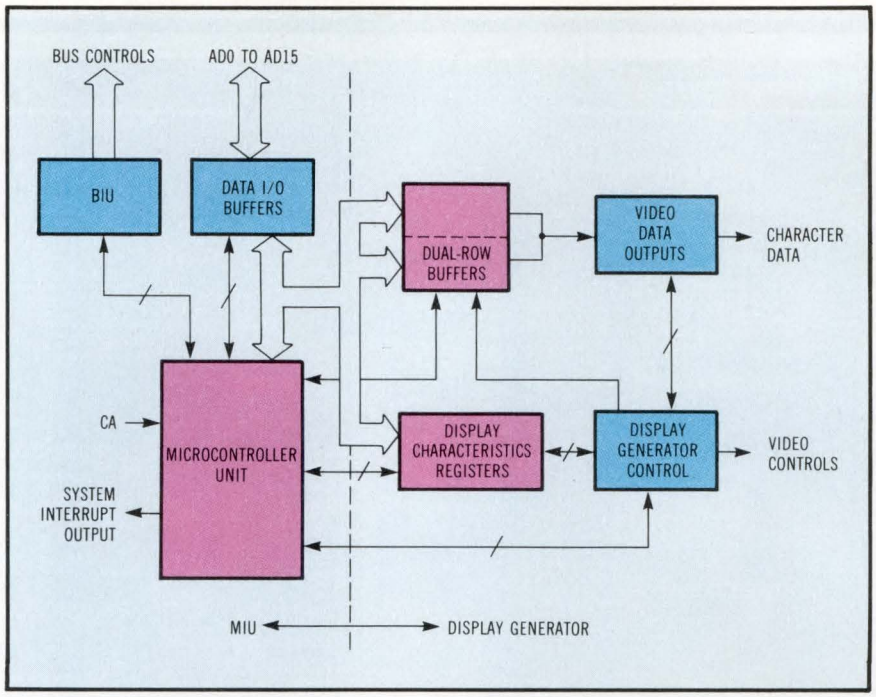
A text coprocessor chip from Intel Corp uses DMA and linked list processing to display publication quality text onscreen. In addition to displaying proportional spacing with simultaneous superscripts and subscripts, the 82730 maintains linked lists of text blocks for extremely rapid manipulation and formatting of text files.

Thus, one broad application area in word processing opens up—the designer can program the text display coprocessor to match the capabilities of a known printer in the system for true text preparation.

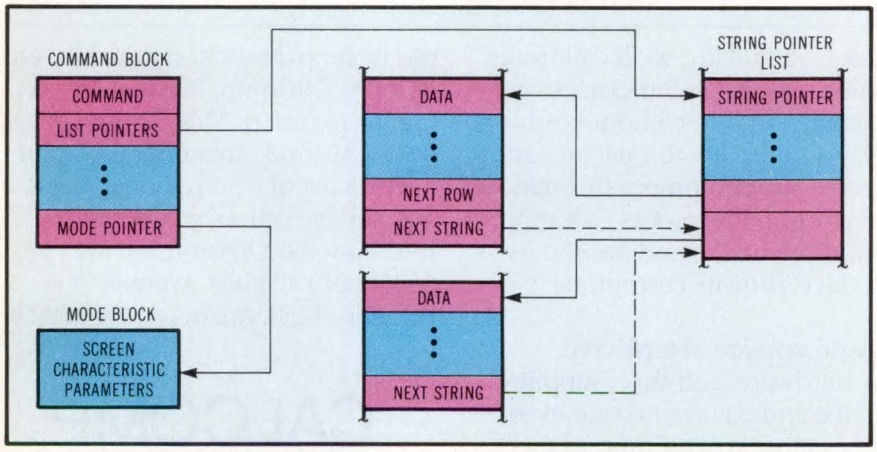
The programmable nature of the 82730 allows for dynamic loading of soft ports, multiple windows, and user programmable field and character attributes. The CPU, however, is relieved of the need to attend to display control through the use of message blocks; it merely issues a channel attention (CA) command to start the 82730 working. A command block set up by the CPU contains commands and pointers to other message blocks, such as mode block containing screen characteristic parameters, and also lists pointers that keep track of the sequence of text blocks.

After the text coprocessor has set itself up by reading the parameters, it uses its DMA capability to take in the text data stream indicated by the string list pointer. In addition to the mode and string list pointers in the command block, the 82730 can process high level commands embedded in the text stream, such as TAB, SUPERSCRIPT/SUBSCRIPT, SKIP, and REPEAT.

The string pointer list is particularly important in speeding up text block manipulation. Instead of forcing the coprocessor to shift data around to keep all text blocks in memory contiguous, the 82730 maintains a list of pointers to the text block locations in memory. When it has processed all the commands in a memory control block, the 82730 signals the CPU that it is ready to start another block. In the meantime, the CPU may have prepared an entirely new block for the 82730 to work on, or may have sent the processor back to the original block, depending on the CPU's requirements.



Shown here is a block diagram of the 82730. Dual-row buffers maintain a steady flow of character data to be displayed. Display generation determines how to display data by reading the display characteristics registers.



With 82730 display access and control, the CPU activates the coprocessor to read a command block. This block may contain pointers to mode blocks (display parameters) or to string pointers that maintain the proper sequence of text blocks in memory.

The 82730 is divided into two main sections: the memory interface unit (MIU), which handles communications between the 82730, the CPU, and the memory; and the display generator (DG), which controls the screen.

The MIU is further divided into two sections—a bus interface unit (BIU), and a microcontroller unit (MCU) that contains microinstruction store for display parameters and attributes.

Thus, the MCU fetches data from memory and stores them either in row buffers (for data to be displayed), or in display characteristics registers that store the display parameters (eg, screen size and blink rate). The MCU and DG communicate asynchronously—the MCU fetches one row of up to 200 characters while the DG displays the other row. The buffers are swapped at the end of each display operation, so there is no wait between rows being displayed. Since the contents of the display characteristics registers are read in from a memory control block and determined by the DG parameters, the user can invoke parameters for the whole screen with a single high level command to reference a given memory block.

Control of screen resolution and other parameters has also been put into the user's hands by separating the video

(continued on page 77)

Name one microsystem with

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- 1 MIPS performance
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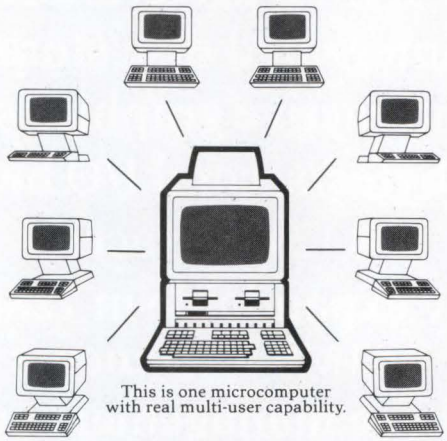

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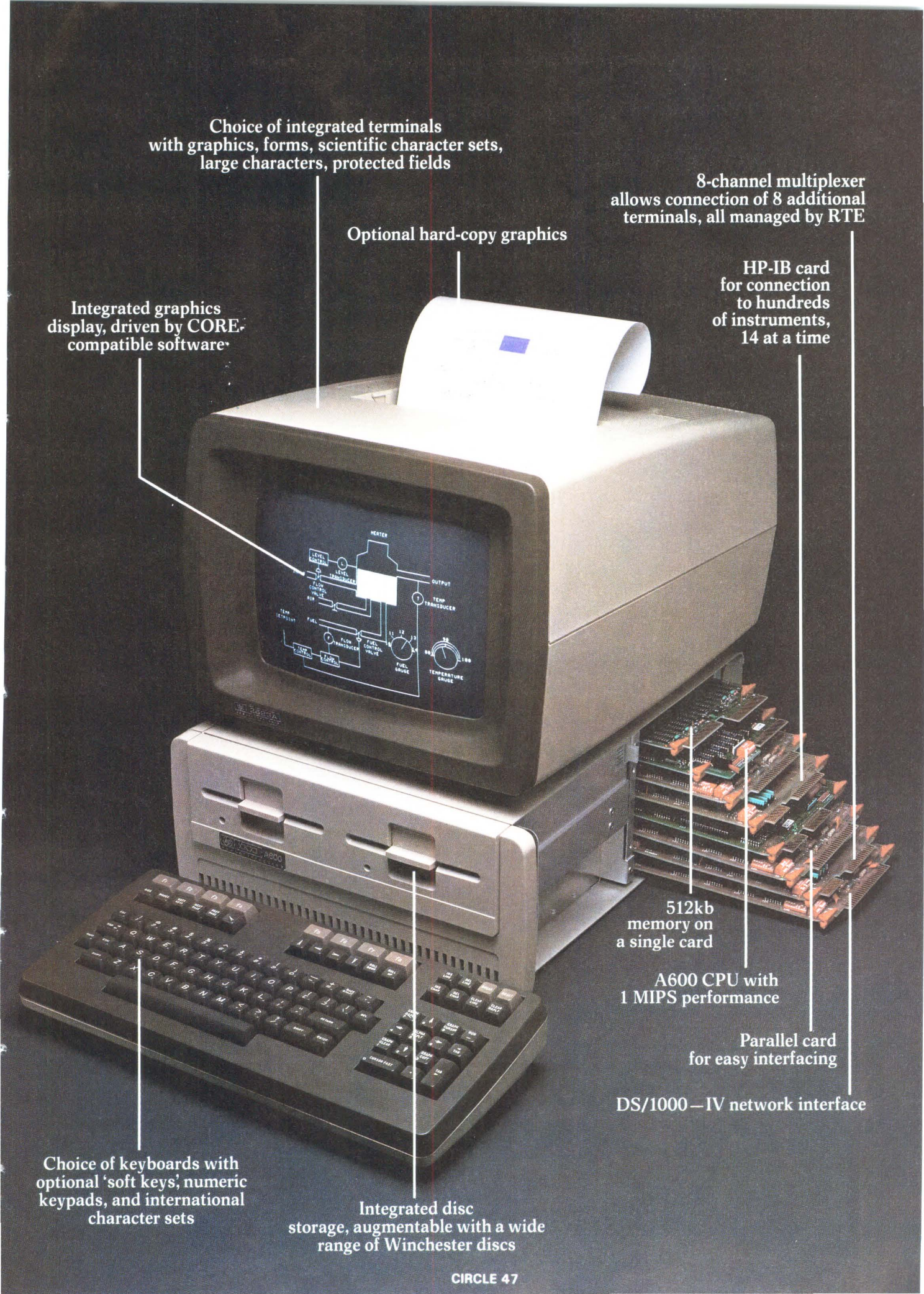
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Working Within the Systems

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CIRCLE 48

Coprocessor chip

(continued from page 72)

interface clock from the bus interface clock. The video interface clock consists of two clocks: the reference clock (RCLK) and the character clock (CCLK). The RCLK controls the raster timing, thus determining scan rate and lines, while the CCLK controls the rate at which character and attribute information is shifted out of the chip. Thus, characters of varying resolution, size, and position can be defined, and proportional spacing can be controlled. **Intel Corp**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 253

MEMORY SYSTEMS

Microfloppy deviates from proposed standard

Presenting designers with yet another alternative, Tabor has announced its entry into the microfloppy market, as promised. Unlike its competitors, the TC500 Drivette uses a 3¼" flexible disk that is packaged in the soft vinyl jacket used in larger versions.

A single-sided drive with 500k-byte capacity, the drive contains a standard 5¼" interface to make it plug to plug compatible with existing 5¼" drives. In addition, by recording at a 140-tpi density, it provides data compatibility with single-sided 96-tpi 5¼" drives since both contain 80 tracks of data.

To make the device particularly attractive in portable instruments, recorders, and computers, the design has eliminated unnecessary weight. Reduced complexity results from incorporating multifunction parts, minimizing fasteners through the use of self-piloting and snap together parts, and basing the unit on a rugged 1-piece die-cast chassis. This produces a drive one-fourth the size, one-half the weight, and with only 60% of the power requirements of a 5¼" floppy drive.

The unit holds 500k bytes of unformatted data, recorded using MFM techniques at a 9250-bpi density on the inner track. Formatted capacity is 328k bytes. Rotating the disk at 300 ±1% rpm, the direct drive spindle motor eliminates belt drive and associated problems. Speed is accurate and stable. Start time is 400 ms maximum. The stepping motor lead screw carriage incorporates a no-backlash feature that provides accurate recording on 80 tracks at a 140-tpi density. Track to track access time is specified at 10 ms minimum with an average access time of 282 ms. Average latency is given as 100 ms.

According to company president Michael F. Hanley, the flexible jacket was chosen over the hard shell used by other vendors because it lends itself to available manufacturing techniques. Accordingly, media prices should drop to $1 per disk by 1984; the hard shell diskettes are projected to have a 40% higher manufacturing cost because of their mechanical complexity.

Evaluation units are currently being shipped, with full production on the way. Price per unit is $315. **Tabor Corp**, Lyberty Way, Westford, MA 01886.

Circle 254

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CIRCLE 50

NCC '83

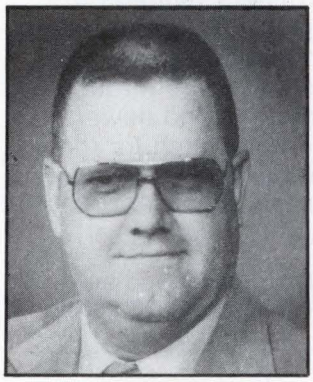
National Computer Conference

Anaheim Convention Center, Anaheim, California
May 16 to 19, 1983

John P. Imlay
Keynote Speaker

Take representative parts: computers, communications, and people; mix thoroughly for four days, and what do you have? The National Computer Conference, which returns to Anaheim, California May 16 to 19. Together with the equipment exhibition and Professional Development Seminars, NCC '83's Technical Program will give attendees the chance to stay on top of their own field and catch up with what's been happening in other sectors of this multifaceted computer industry.

As in previous years, the Technical Program is organized along interest tracks that will help conference-goers pinpoint their areas of greatest concern. This year's tracks are set up as follows: software engineering, management and education, database and distributed systems, human and social issues, office automation, decision support systems, hardware, telecommunications and computer applications, and personal computers. Sessions most likely to attract *Computer Design* readers are listed on the following pages.



Donald B. Medley
Conference Chair

Allen N. Smith
Program Chair

High performance Winchester technology will head this year's hardware sessions. Though well-established in large computers, its entry into small business systems, word processors, and personal computers is keeping Winchester technology in the news. High performance disk drive development trends that cover a wide range of potential applications will be identified.

Meanwhile, high performance computing in itself remains the consuming passion of many *Computer Design* readers. A panel will present state of the art vendor offerings, application requirements, how one facility develops and provides available resources, and the new directions university research may take in the area of scientific simulation.

Up-and-coming multiprocessor computer designs are also likely to draw attention, particularly from designers of fault-tolerant systems. The advent of inexpensive VLSI components is making multiprocessor architecture feasible in a growing breadth of applications.

Beyond that, separate sessions will be devoted to microcomputer design and array processor development. Microcomputer design topics will emphasize evolving Multibus standards, dynamic RAM architectures for graphics applications, and a unique approach to microprocessor memory. Array processor panelists will evaluate the impact of hardware and software advances and look to a plethora of powerful new array processors being used in applications like signal processing, image processing, simulation, CAD, testing, and dynamic analysis and control.

Day by day, the partnership between telecommunications and computer applications becomes stronger. Work on the reference model for open systems interconnection (OSI) continues

(continued on page 80)

NCC '83

(continued from page 79)

at full tilt toward settling ground rules for developing protocols that interconnect heterogeneous systems. When this goal is realized, designers will be able to integrate advanced technologies into systems they just dreamed about 10 years ago.

One session will review the latest draft of OSI's 7-layer protocol, network layer service, and the role intelligent peripherals can play in system architecture. Other sessions will assess strides in computer communication network techniques for routing, flow and congestion control, and network configuration management. Ongoing development is zeroing in on improved performance, algorithm efficiency, and distributed operation support.

At the session on fifth-generation computers, the human element will assume a bigger slice of the computer pie as speakers cull their experience from ongoing technology based projects. Japan has thrown down the gauntlet for leadership in advanced computer technology by the 1990s with its government funded Fifth-Generation Computer Project. U.S. government and industry leaders will describe their strategies for meeting this challenge through parallel work on supercomputers and powerful logic-inference machines. Then watch for the software engineering meeting titled "Artificial Intelligence: Blue Sky or Tools of the Future?"

For registration information, contact NCC '83 Registration, Dept 1040, Washington, DC 20044. Tel: 703/558-3680.

Technical Program Excerpts*

Session M1-1: Communicating with Data Bases in English

Mon 1:30 to 3 pm, Salon G

Leader: M. Evens, Illinois Institute of Technology

M1-1/1 "Knowledgeable Contexts for User Interaction"
B. H. Thompson, F. B. Thompson, and T-P. Ho, California Institute of Technology

M1-1/2 "An English Language Processing System Which 'Learns' about New Domains"
B. W. Ballard and J. C. Lusth, Duke University

Panelists: L. Harris, Artificial Intelligence Corp; and B. J. Grosz, SRI

Session M1-3: Current Database Machines

Mon 1:30 to 3 pm, Salon A

Leader: M. Plesset, Aerospace Corp

M1-3/1 "Application of the Massively Parallel Processor to Database Management Systems"
E. Davis, North Carolina State University

Panelists: S. Fuld, Amperif Corp; E. I. Lowenthal, Intel Corp; and R. Epstein, Britton-Lee, Inc

Session M1-4: Office Automation: State of the Art and Key Issues

Mon 1:30 to 3 pm, Salon E

Leader: A. Wohl, Advanced Office Concepts

Session M1-5: High Performance Winchester Trends

Mon 1:30 to 3 pm, Salon 1

Leader: T. Williams, *Computer Design* magazine

M1-5/1 "Winchesters for Multi-User/Multitask Applications"
L. Jacob, PRIAM

Panelists: R. Brechtlein, Century Data Systems; J. Ramos, Evatek; D. Weir, IBIS; and T. Scooros, PRIAM

Session M1-6: Protocols for Computer Communications

Mon 1:30 to 3 pm, Salon F

Leader: H. V. Bertine, Bell Labs

M1-6/1 "A Standard Session Protocol for Open Systems Interconnection"
C. E. Young, Bell Labs

M1-6/2 "The Role of Intelligent Peripheral Interfaces in Systems Architecture"
I. D. Allen, Sperry Univac

M1-6/3 "Progress on the Network Layer of the OSI Reference Model"
P. F. Linington, Rutherford Appleton Lab

Session M1-7: Microcomputer Software Protection

Mon 1:30 to 3 pm, Salon 3

Leader: W. Green, Wayne Green, Inc

Panelists: B. Godbout, Godbout Electronics; G. Morrow, Morrow Designs; G. Kildall, Digital Research; P. Hipson, Alternative Micro Systems; and D. Myers, Jones Futurex

Session M2-1: Artificial Intelligence: Blue Sky or Tools of the Future?

Mon 3:30 to 5:30 pm, Salon 1

Leader: R. Maxion, Xerox Corp

Panelists: J. Mostow, USC/Information Sciences Institute; E. Rich, University of Texas, Austin; J. S. Brown, Xerox PARC; and J. McDermott, Carnegie-Mellon University

(continued on page 82)

*Technical Program sessions are subject to last-minute changes.

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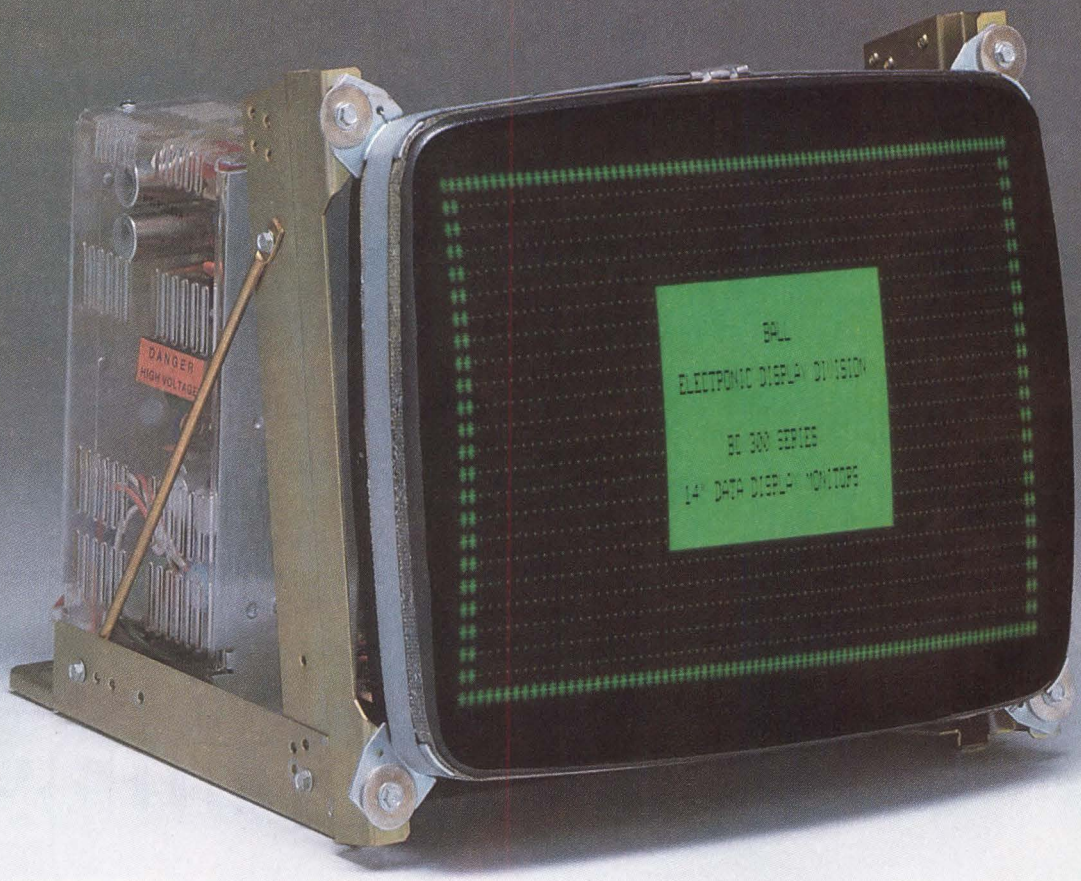

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CIRCLE 51

NCC '83

(continued from page 80)

Session M2-3: Research Database Machines

Mon 3:30 to 5:30 pm, Salon J

Leader: P. Hawthorn, Lawrence Berkeley Lab

M2-3/1 "A Reconfigurable VLSI Architecture for a Database Processor"
K. Oflazer, Carnegie-Mellon University

M2-3/2 "Implementing Set Theoretic Relational Query Functions Using Highly Parallel Index Processing Hardware"
S. Pramanik, Michigan State University

M2-3/3 "Cost-Effective Ways of Improving Database Computer Performance"
D. K. Hsiao, Naval Postgraduate School

Panelists: M. Missikoff, Instituto di Analisi dei Sistemi

Session M2-6: Advances in Computer Communication Networks

Mon 3:30 to 5:30 pm, Salon 3

Leader: E. F. Wunderlich, American Bell, Inc

M2-6/1 "Three Heuristics for Improving Centralized Routing in Large Long-Haul Communication Networks"
I. M. Pesic and D. W. Lewis, University of Santa Clara

M2-6/2 "A New Probabilistic Routing Algorithm for Packet Switched Computer Networks"
C-Y. Chin and K. Hwang, Purdue University

M2-6/3 "Optical Wireless Modem for Office Communication"
T. Minami, H. Morikawa, and O. Takahashi, Fujitsu Labs Ltd

M2-6/4 "A High Throughput Interconnection Structure"
J. A. Hernandez and R. Joly, Ecole Nationale Superieure des Télécommunications; and E. Horlait and G. Pujolle, Université Pierre et Marie Curie

Session T1-1: Writing Less Code: An Approachable Ideal

Tues 8:30 to 10 am, Salon A

Leader: N. L. Bloom, American Management Systems, Inc

T1-1/1 "Writing Less Code—An Approachable Ideal"
N. L. Bloom, American Management Systems, Inc

T1-1/2 "Foundation Software: A Significantly Improved Approach to the Development of Large Application Systems"
G. A. Curtis, American Management Systems, Inc

T1-1/3 "A Case Adaptable Applications Software"
M. Woodward, Associates Financial Services; and P. F. Digimmarino, American Management Systems, Inc

Session T1-3: Fifth Generation Computers

Tues 8:30 to 10 am, Salon E

Leader: F. F. Kuo, SRI International

Panelists: R. E. Kahn, DoD—DARPA; E. Feigenbaum, Stanford University; and D. H. Brandin, SRI International

Session T1-5: DSS Design Methodologies—1

Tues 8:30 to 10 am, Salon G

Leader: D. T. Lee, University of Hartford

T1-5/1 "A New Look at Existence Dependency in Data Bases"
T. C. Chiang, Bell Labs

T1-5/2 "Issues in the Design of Relational Model Management Systems"
R. W. Blanning, Vanderbilt University

Panelist: D. Wszolet, Information Builders

Session T1-6: High Performance Computing

Tues 8:30 to 10 am, Salon J

Leader: D. Theis, Aerospace Corp

T1-6/1 "Universities and the Future of Computing Technology for Scientific Simulation"
K. G. Wilson, Cornell University

Panelists: S. Chen, Cray Research, Inc; J. Swanson, Swanson Analysis Systems, Inc; G. Michael, Lawrence Livermore Labs

Session T1-7: Voice Processing

Tues 8:30 to 10 am, Salon 3

Leader: J. L. Flanagan, Bell Labs

T1-7/1 "The Technology of Digital Speech: Compression, Editing, Storage"
R. E. Crochiere and J. L. Flanagan, Bell Labs

T1-7/2 "Statistical Modeling for Automatic Speech Recognition"
R. L. Mercer, T. J. Watson Research Center

T1-7/3 "Implications of VLSI Technology for Speech Processing"
R. W. Broderson, University of California, Berkeley

Session T2-1: Software Management for the '80s

Tues 10:30 am to 12 noon, Salon A

Leader: S. M. Jacobs, TRW

Panelists: G. L. Barksdale, Jr, Ford Aerospace & Communications; R. Loesh, Jet Propulsion Lab; D. Reifer, Reifer Consultants, Inc; R. Valleni, TRW; and J. D. Wick, Xerox Corp

Session T2-3: Relational Database Management

Tues 10:30 am to 12 noon, Salon E

Leader: P. Shaw, IBM Corp

T2-3/1 "Local Query Translation and Optimization in a Distributed System"
A. Hevner, University of Maryland

T2-3/2 "Progress Toward Database Management Standards"
D. R. Deutsch, General Electric Information Services Co

(continued on page 84)

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T2-3/3 "Command Usage in a Relational Database System"
J. D. Joyce and D. D. Warn, General Motors Research Labs

Session T2-4: DSS Design Methodologies—2

Tues 10:30 am to 12 noon, Salon G

Leader: D. T. Lee, University of Hartford

T2-4/1 "The DSS Development System"
R. H. Bonczek and A. B. Whinston, Purdue University; N. Ghiaseddin, University of Notre Dame; and C. W. Holsapple, University of Illinois

T2-4/2 "Applications of Fuzzy Languages and Pictorial Data Bases to Decision Support Systems Design"
E. T. Lee, Memphis State University

Panelist: S. Kimbrough, Massachusetts Institute of Technology

Session T2-5: Microcomputer Design Topics

Tues 10:30 am to 12 noon, Salon J

Leader: S. Cooper, Intel Corp

T2-5/1 "Dynamic RAM Architectures for Graphics Applications"
D. Finke, Intel Corp

T2-5/2 "The iRAM—An Innovative Approach to Microprocessor Memory Solutions"
J. J. Fallin, Intel Corp

T2-5/3 "Multibus Continues to Evolve to Meet the Challenges"
S. Cooper, Intel Corp

T2-5/4 "Analysis of the M6809 Instruction Set"
J. Boney, Motorola, Inc

Session T2-6: Human Voice Communications with Computers

Tues 10:30 am to 12 noon, Salon F

Leader: J. M. Nye, Marketing Consultants International

Panelists: R. Rabin, Verbex/Exxon Communications Systems; M. H. Hitchcock, Interstate Electronics Corp; C. Berney, Centigram Corp; and J. M. Nye, Marketing Consultants International

Session T3-1: Reducing Program Development Risks with Reusable Code

Tues 1:30 to 3 pm, Salon G

Leader: L. Martin, Raytheon Computer Services

Panelists: J. A. Manara, Security Pacific National Bank; J. E. Kunkler, Xerox Corp; J. Corkery, Raytheon Computer Services; and R. Lanergan, Raytheon Missile Systems Div

Session T3-7: Distributed Processing

Tues 1:30 to 3 pm, Salon F

Leader: D. Kutnick, The Yankee Group

Panelists: D. Kutnick and P. Burstyn, The Yankee Group; and P. Dorn, Dorn Computer Consultants

Session T4-1: Software Engineering Techniques and Approaches

Tues 3:30 to 5:30 pm, Salon 1

Leader: A. Pyster, TRW/DSG

T4-1/1 "Stepwise Structuring: A Style of Life for Flexible Software"
E. Sandewall, S. Hagglund, C. Gustafsson, and L. Jonesjo, Linkoping University

T4-1/2 "HITS: A Symbolic Testing and Debugging System for Multilingual Microcomputer Software"
T. Chuso et al, Hitachi, Ltd

T4-1/3 "A Global Checkpointing Model for Error Recovery"
K. Kant, Northwestern University

T4-1/4 "Development Tools for Bus Controller Software"
M. I. Thomas, Tecsi-Software

Session T4-3: Microcomputer Database Management Systems

Tues 3:30 to 5:30 pm, Salon A

Leader: E. Ivie, Brigham Young University

Panelists: K. F. Barley, DataWise; G. Everest, University of Minnesota; D. J. Rodman, David J. Rodman Assocs; J. C. Norman, Condor Cord; and J. C. Collier, MicroPro

Session T4-4: Electronic Mail

Tues 3:30 to 5:30 pm, Salon 3

Leader: W. Ulrich, Walter Ulrich Co

T4-4/1 "Current Issues in Electronic Mail Heralding a New Era"
W. Ulrich, Walter Ulrich Co

T4-4/2 "The Integration of Multimedia Communications"
B. P. Donohue, ITT, American Bell, Inc

T4-4/3 "Voicemail"
P. F. Finnigan, Voicemail International, Inc

T4-4/4 "Electronic Mail: Evolving from Intracompany to Intercompany"
H. P. Burstyn, The Yankee Group

Session T4-5: Dynamic and Reconfigurable Architectures for Realtime Parallel Systems: Software Problems

Tues 3:30 to 5:30 pm, Salon J

Leader: C. Davis, Ballistic Missile Defense Advanced Technology Center

T4-5/1 "Reconfigurable Fault-Tolerant Multicomputer Network"
C. Davis, Ballistic Missile Defense Advanced Technology Center; S. P. Kartashev, University of Nebraska; and S. I. Kartashev, Dynamic Computer Architecture, Inc

(continued on page 86)

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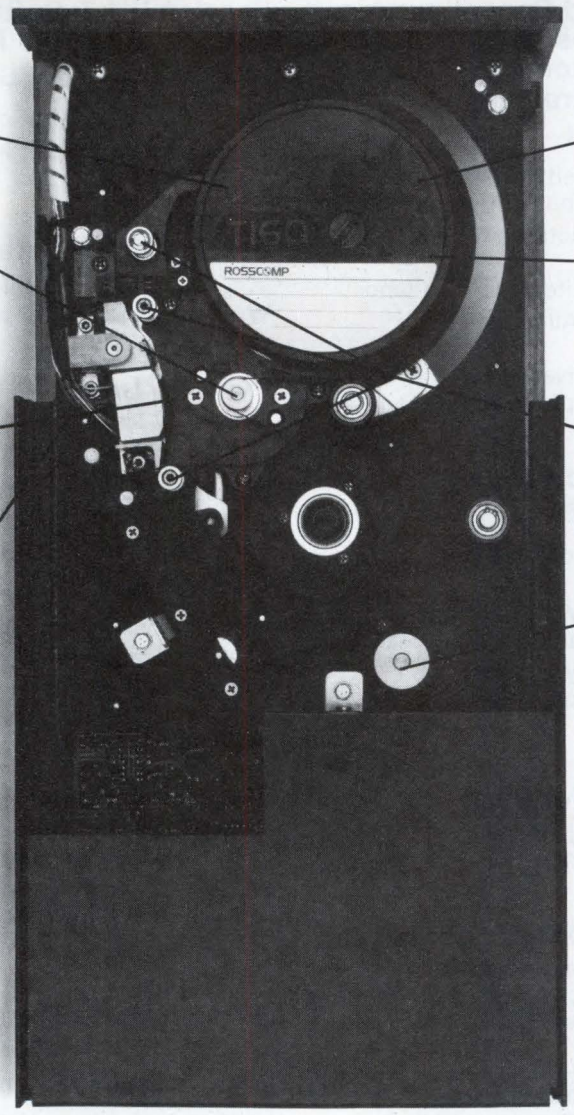

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(continued from page 84)

Session T4-5: Dynamic and Reconfigurable Architectures for Realtime Parallel Systems *(continued)*: Hardware Structures

Tues 3:30 to 5:30 pm, Salon J

Leaders: S. P. Kartashev, University of Nebraska; and S. I. Kartashev, Dynamic Computer Architecture, Inc

T4-5/1 "Reconfigurable Architectures for VLSI Processing Arrays"
M. Sami and R. Stefanelli, Politecnico di Milano

T4-5/2 "Conflict-Free Memory Allocation for Associative Data Files"
S. P. Kartashev, University of Nebraska; and S. I. Kartashev, Dynamic Computer Architecture, Inc

Session T4-6: Network Security

Tues 3:30 to 5:30 pm, Salon F

Leader: J. M. Nye, Marketing Consultants International, Inc

T4-6/1 "Network Security and Vulnerability"
J. M. Nye, Marketing Consultants International, Inc

Panelists: L. Adleman, University of Southern California; D. R. Whitson, Datotek, Inc; and R. O'Connor, Motorola, Inc

Session W1-1: Directions for Software Engineering: Now and in the Future

Wed 8:30 to 10 am, Salon A

Leader: W. E. Riddle, Software Design & Analysis, Inc

Panelists: R. Balzer, USC Information Sciences Institute; L. Belady, IBM Corp; J. Munson, System Development Corp; and J. Musa, Bell Labs

Session W1-5: Super Micros: Commodity Computer, Commodity Software

Wed 8:30 to 10 am, Salon F

Leader: J. Stidd, Molecular Computing

Panelists: P. Alker, Convergent Technology; M. Florio, Onyx; and J. Stidd, Molecular Computing

Session W1-6: Special Applications of Technology

Wed 8:30 to 10 am, Salon J

Leader: L. Cameron, Atlantic Richfield Co

W1-6/1 "The Laboratory Automation System in the Electrical Communications Laboratory"
N. Terashima, Nippon Telegraph & Telephone Public Corp

W1-6/2 "Applications of Digital Optical Disks in Library Preservation and Reference"
W. R. Nugent, Library of Congress

Panelist: J. Cornwell, Walt Disney Productions, Inc

Session W1-7: Software Transportability in the Personal Computer World

Wed 8:30 to 10 am, Salon 3

Leader: P. O'Grady, Micro Focus

Panelists: P. O'Grady, Micro Focus; T. McCalmont, Cromemco, Inc; and T. Rollander, Digital Research

Session W2-1: Software Technology for Adaptable Reliable Systems

Wed 10:30 am to 12 noon, Salon J

Leader: L. E. Druffel, U. S. Department of Defense

Panelists: S. Redwine, The MITRE Corp; and E. Kruesi, General Electric Co

Session W2-2: Software Maintenance—Application System Perspective

Wed 10:30 am to 12 noon, Salon G

Leader: N. Chapin, Infosci, Inc

W2-2/1 "Improving Software Maintenance Attitudes"
P. C. Tinnirello, A. M. Best Co

W2-2/2 "A Methodology for Minimizing Maintenance Costs"
J. Connell and L. Brice, Los Alamos National Lab

W2-2/3 "Quality Assurance and Maintenance Applications Systems"
B. J. Taute, Time, Inc

W2-2/4 "Human Investment Techniques for Effective Software Maintenance"
N. L. Marselos, Western Electric Co

Session W2-3: Measuring the Impact of Information Techniques

Wed 10:30 am to 12 noon, Salon 3

Leader: J. M. Nilles, University of Southern California

Panelists: D. Mankin, Rand Corp; A. M. Mohrman, University of Southern California; and G. Talbot, TRW, Inc

Session W2-5: Videotex Systems

Wed 10:30 am to 12 noon, Salon A

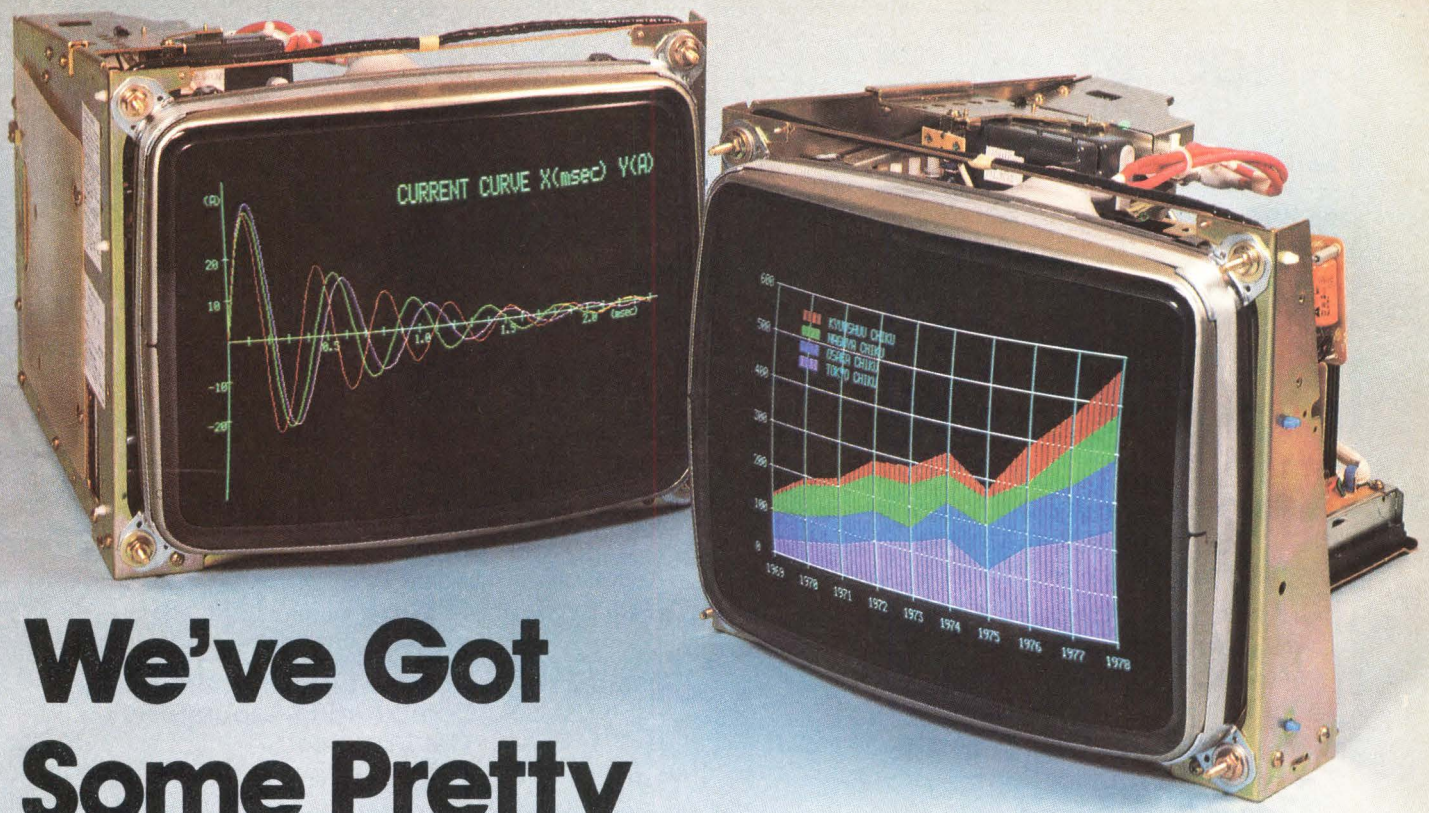
Leader: G. H. Arlen, Arlen Communications, Inc

W2-5/1 "Tales from the Trial Trail: Videotex Progress in the United States"
G. H. Arlen, Arlen Communications, Inc

W2-5/2 "Videotex and Teletext in the Business/Consumer Marketplace"
L. T. Pfister, Time Video Information Services

Panelists: S. Berkman, Time Video; M. Hayes, DEC; J. Holly, Times Mirror Videotex

(continued on page 88)



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CIRCLE 54

(continued from page 86)

Session W2-6: Network Services Planning

Wed 10:30 am to 12 noon, Salon E

Leader: J. King, DMW Group, Inc

W2-6/1 "Planning High Speed Digital Services in the Bell System"
G. Handler, American Telephone & Telegraph

Panelists: H. Jamison, Tymshare; and D. Russell, Satellite Business Systems

Session W2-7: The Next 5 Years in Microcomputers

Wed 10:30 am to 12 noon, Salon F

Leader: P. Nesdore, Auerbach Publishers

Panelists: P. Nesdore, Auerbach Publishers; J. Pornelle, Author; and A. Osborne, Osborne Computers

Session W3-1: Experience in Ada Applications

Wed 1:30 to 3 pm, Salon A

Leader: G. Booch, Consultant

Panelists: S. Fox, Computer Corporation of America; K. Krishnaswimy, Ford Aerospace Corp; and J. Hutchison, GE Research and Development Center

Session W3-2: Control of the Maintenance Function

Wed 1:30 to 3 pm, Salon 3

Leader: N. Zvegintzov, Zvegintzov Assocs

W3-2/1 "Structured Software Maintenance"
G. R. E. Schneider, Naval Weapons Center

W3-2/2 "Application Maintenance: One Shop's Experience and Organization"
R. E. Marsh, Dow Corning Corp

W3-2/3 "Organizational Issues of Effective Maintenance Management"
G. L. Richardson, Texaco, Inc; and C. W. Butler, University of Arkansas

Panelist: R. Martin, National Bureau of Standards

Session W3-6: Howard Aiken and the Harvard Computation Laboratory: The Machines

Wed 1:30 to 3 pm, Salon G

Leader: I. B. Cohen, Harvard University

Panelists: G. Hopper, U.S. Navy; R. M. Bloch, R. M. Bloch Assocs; J. A. Harr, Bell Telephone Labs; and P. F. Strong, Harvard University

Session W4-1: Future Visions: Ada Environments of the 1990s

Wed 3:30 to 5:30 pm, Salon A

Leader: H. Hart, TRW

W4-1/1 "Implementation of an Ada Runtime Environment"
H. Fischer, Litton Data Systems; and E. H. Sibley, Alpha Omega Group, Inc

W4-1/2 "Future Ada Environments"
S. H. Saib, General Research Corp

Panelists: F. Belz, TRW; T. Standish, University of California, Irvine; and H. Hunke, Commission of the European Communities

Session W4-3: Applications in Distributed Database Management

Wed 3:30 to 5:30 pm, Salon F

Leader: C. Mohan, IBM Corp

W4-3/1 "A Distributed Database Design for a Communications Network Control System"
S. L. Kota, S. C. Lo, and M. H. Aronson, Ford Aerospace & Communications Corp

W4-3/2 "Empact: A Distributed Database Application"
A. Norman and M. Anderton, Tandem Computers Inc

W4-3/3 "Dynamic Replication, An Overview"
T. P. Daniell, R. C. Harding, Jr, and S. H. Nauckhoff, IBM Corp

Panelist: C. Mohan, IBM Corp

(continued on page 90)

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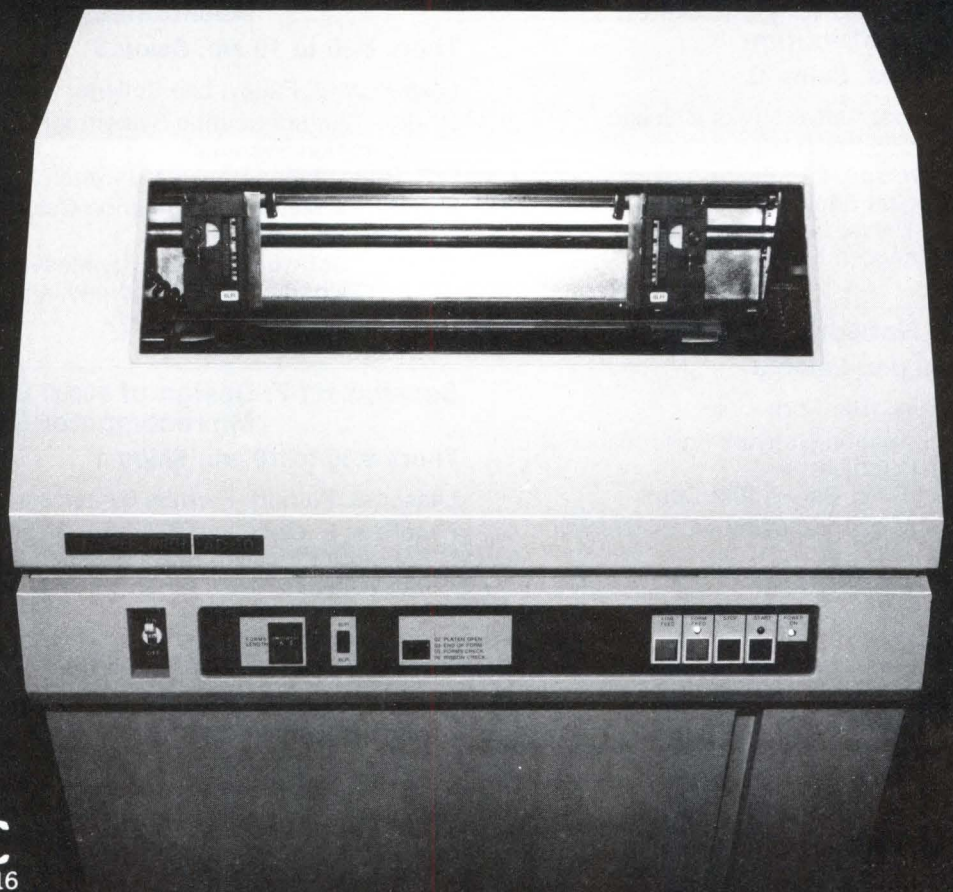

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CIRCLE 56

Session W4-5: Howard Aiken and the Harvard Computation Laboratory: The Laboratory and Aiken's Contribution

Wed 3:30 to 5:30 pm, Salon G

Leader: R. Ashenhurst, University of Chicago

Panelists: F. P. Brooks, Jr, University of North Carolina; K. E. Iverson, I. P. Sharp Assoc; M. V. Wilkes, Digital Equipment Corp; A. G. Oettinger, Harvard University; and W. L. Semon, Syracuse University

Session W4-6: Network Management

Wed 3:30 to 5:30 pm, Salon 3

Leader: K. Maruyana, IBM Corp

W4-6/1 "IBM Information Network Performance and Availability Measurement"
R. C. Soucy and R. M. Bailey, IBM Corp

W4-6/2 "Designing and Managing an SNA Network for Growth"
S. M. Schiffman, IBM Corp

W4-6/3 "Backup and Recovery in the IBM Information Network"
K. Bhadra and S. M. Schiffman, IBM Corp

W4-6/4 "Logical Problem Determination in an SNA Network"
R. A. Weingarten and E. E. Iacobucci, IBM Corp

Session H1-1: Software Engineering by the Year 2000

Thurs 8:30 to 10 am, Salon E

Leader: J. A. Rader, Hughes Aircraft Co

Panelists: B. Boehm, TRW; L. Belady, IBM Corp; T. Gilb, Consultant; and L. Druffel, U.S. Department of Defense

Session H1-4: Beyond Productivity: The Future of Office Automation

Thurs 8:30 to 10 am, Salon F

Leader: N. D. Meyer, N. Dean Meyer and Assocs, Inc

Panelists: N. D. Meyer, N. Dean Meyer and Assocs, Inc; E. Sokol, Organizational Research Group; and D. C. Engelbart, Tymshare, Inc

Session H1-5: New Developments in Array Processors

Thurs 8:30 to 10 am, Salon G

Leader: W. J. Karplus, University of California, Los Angeles

Panelists: G. Bekey and D. Cohen, University of Southern California; R. Borgioli, CSP, Inc; R. Tracy, Floating Point Systems, Inc; and W. J. Karplus, University of California, Los Angeles

Session H1-6: Creative Ideas for Systems Development and Measurement

Thurs 8:30 to 10 am, Salon 3

Leader: W. E. Farley, Lee College

H1-6/1 "An Information System for Developing Information Systems"
B. Blum, Johns Hopkins University Hospital

H1-6/2 "A Metric of Estimation Quality"
T. DeMarco, Yourdon, Inc

H1-6/3 "Software Productivity Measurement"
J. S. Collofello, S. N. Woodfield, and N. E. Gibbs, Arizona State University

Session H1-7: Design of 68000 Based Microcomputer Systems

Thurs 8:30 to 10 am, Salon 1

Leader: S. Puthuff, Fortune Systems

Panelists: E. Lupin and R. Mellen, Cromemco; S. Puthuff, Fortune Systems; and T. Gunter, Motorola, Inc

Session H2-6: Multiprocessor Computer Designs

Thurs 10:30 am to 12 noon, Salon 1

Leader: B. Patterson, Intel Corp

H2-6/1 "Intel iAPX 432—VLSI Building Blocks for a Fault-Tolerant Computer"
B. Patterson, Intel Corp

H2-6/2 "Performance Evaluation of the MP/C"
B. W. Arden and R. Ginosar, Princeton University

H2-6/3 "A Multiprocessor with Replicated Shared Memory"
S. L. Lillevik and J. L. Easterday, Oregon State University

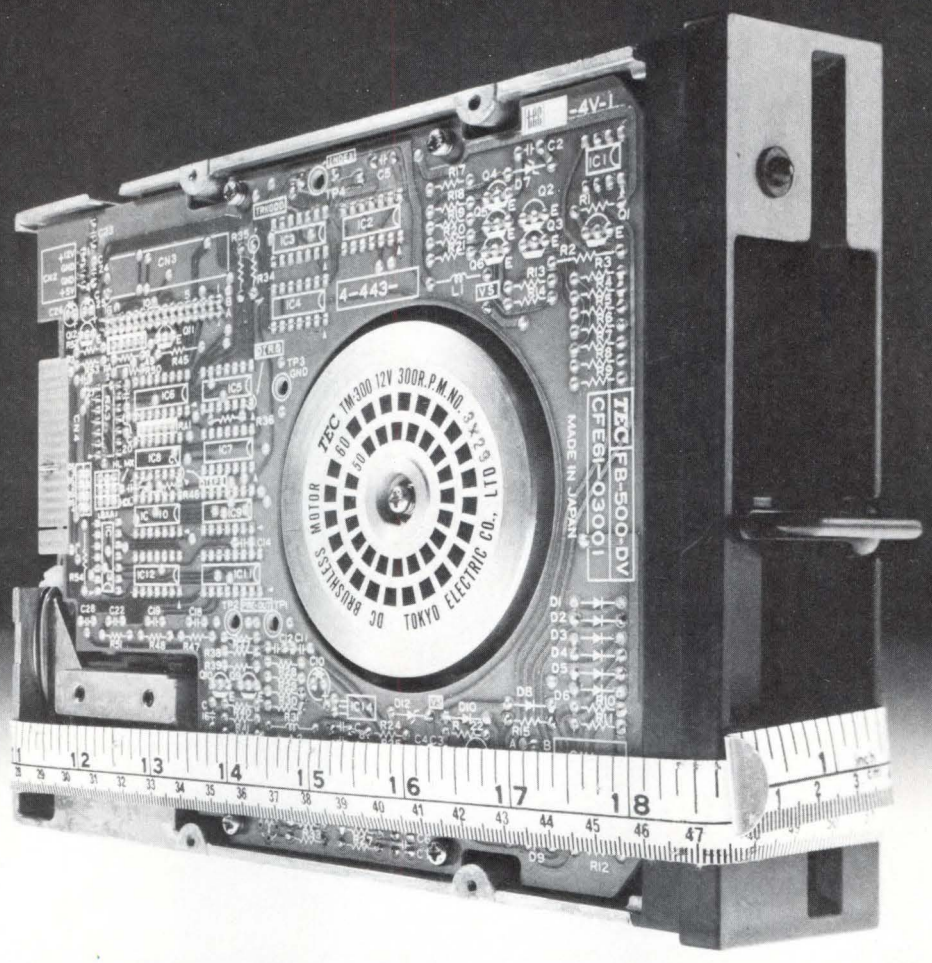
Session H2-7: CAD/CAM

Thurs 10:30 am to 12 noon, Salon G

Leader: D. M. Herstad, Arthur Andersen & Co

Panelists: N. P. Jeffries, Center for Manufacturing Technology; J. H. Keller, Rocketdyne; and N. Schweitzer, Computervision □

HALF-SIZE 5¼ INCH FLOPPY DRIVES FROM NSA



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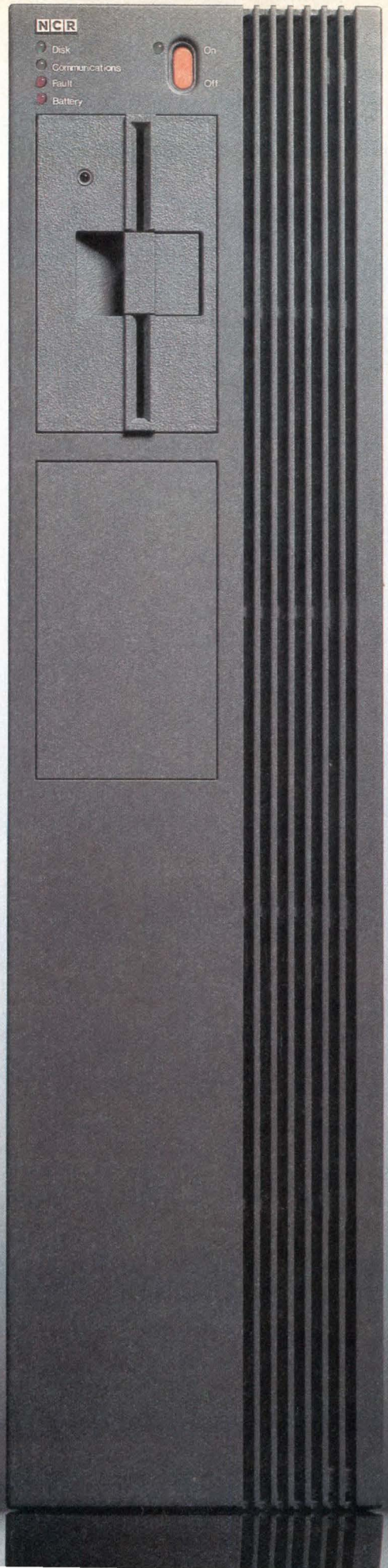
CIRCLE 57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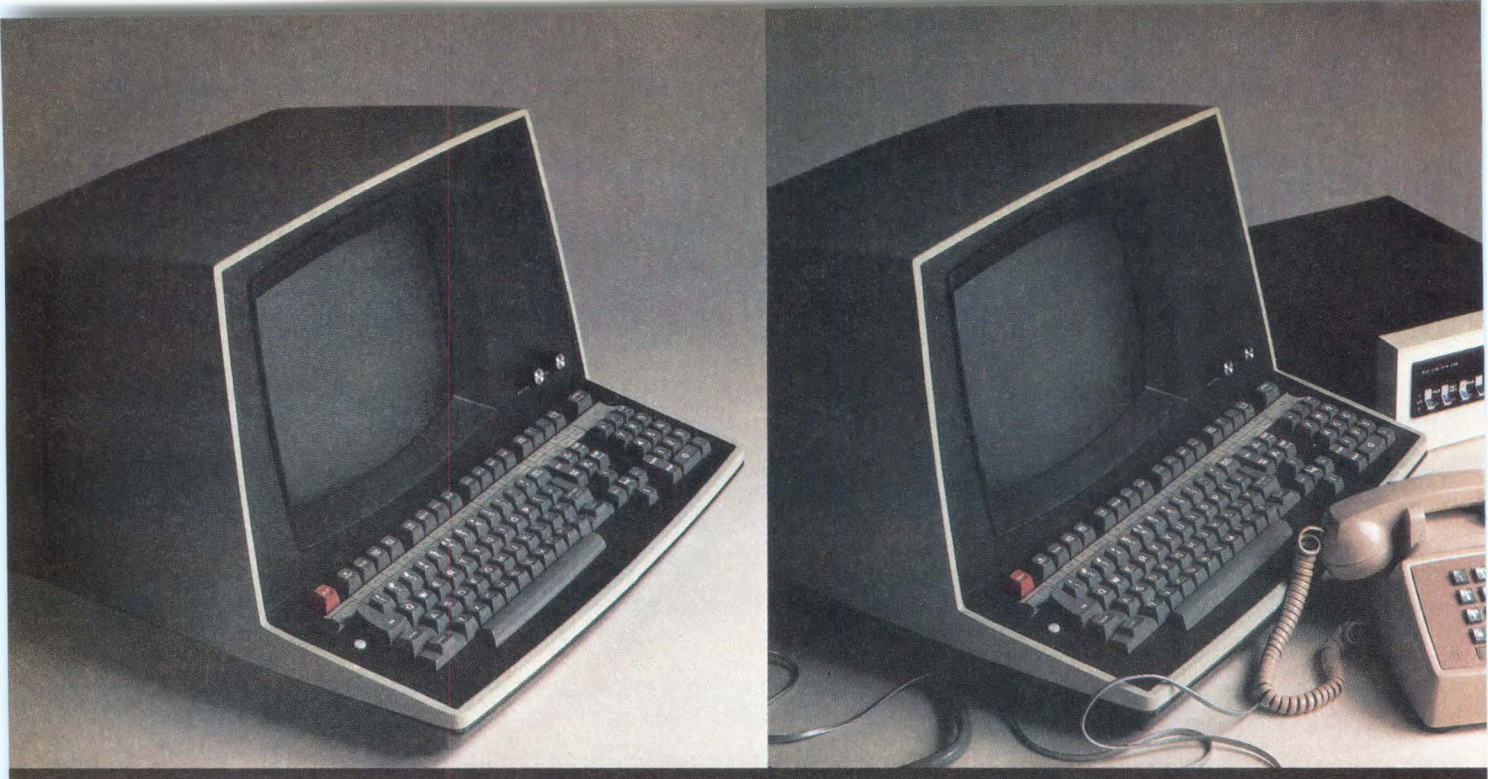

MODEMS SHOULD BE HEARD AND NOT SEEN.

As you can't see, the terminal on the left has a low-cost Rockwell R24DC modem built in. It's connected directly to the U.S. dial-up network with nothing more than a standard telephone jack. No acoustic coupler. No phone. No tangled wires.

It's easy to connect the R24DC modem inside your terminal. It's LSI-based, with the entire 2400 bps modem and data access arrangement on a single 5"x 7.85" plug-in card. With power requirements of ±12V and +5V, it consumes only 3 watts.

Rockwell's R24DC integral modems are FCC-registered and both Bell- and CCITT-compatible. And they're widely used in point-of-sale terminals, and for cleaning up PBXs, data concentrators and data communications devices.

To get the inside story on Rockwell modems, call the Electronic Devices Division, Rockwell International at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, California 92660.

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CIRCLE 59

SID '83

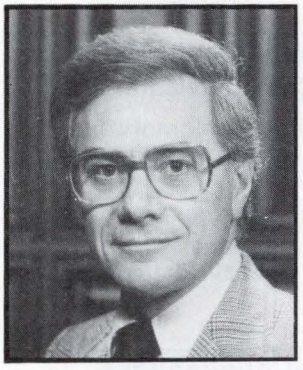
Society for Information Display International Seminar and Symposium

Marriott Hotel, Philadelphia, Pennsylvania
May 10 to 12, 1983

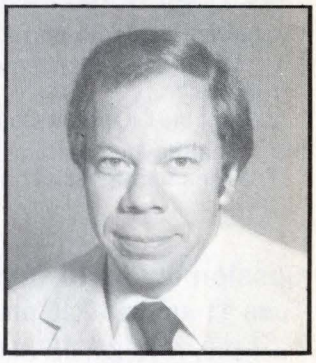
Bart Donohue III
Keynote Speaker

There's a lot more to display technology than meets the eye, and that's what the Society for Information Display's symposium this May 10 to 12 is all about. Authorities from the United States, Japan, Finland, the Netherlands, Austria, Germany, England, France, and Switzerland will get together at the Marriott Hotel in Philadelphia to take stock of global progress in information display technology and survey an international exhibition of components, accessories, operational equipment, and complete systems.

Pivotal technical advances in fabricating, characterizing, and measuring display devices, panels, and subsystems will be explored over the course of a 2-day tutorial seminar, to be held on the days before and after the conference. Seminar Chair Peter Pleshko, manager of plasma display technology development and manufacturing at IBM's Kingston, New York facility, reports that on Monday May 9, fabrication and characterization will tender equal weight as participants benchmark the three major flat panel technologies: plasma, liquid crystal, and ac electroluminescence. Friday's meetings will be split into two groups. One will cover the historical evolution of the three types of display technology, while the other will deal with image quality perception and measurement.



Andras Lakatos
General Chair



James Price
Program Chair

Keynote speaker Bart Donohue III, executive director of research and development at American Bell, will assess how technical advances in information processing, communication, and storage tie into information management and communications. Donohue's talk, "The Technological Explosion and the Emerging Business Opportunities," will mark the opening of SID's Technical Program during Session 3 on Tuesday at 10:15 am.

Of course, the main conference attraction will be its distinguished Technical Program, which will run the gamut from contrast enhancement filters and ink-jet printers to the latest in simulator displays, optical storage, and thermal recording media. Besides that, three evening "rump" sessions will pitch ideas about portable computer displays, the need for color displays, and the display marketplace in 1990.

Recognizing that displays are a crucial concern in portable and handheld computers, panelists in the first evening session will review system requirements and viable display technologies for the upcoming breed of mobile computers. In addition, now that color has penetrated computer graphics technology, the second evening session will evaluate how color is being used in a variety of technical fields. Panelists will rate how well shadow mask CRTs, beam penetration CRTs, and monochrome displays match user needs. Finally, the third evening panel will earmark market trends, then paint a display scenario for the opening of the last decade in this century. Topics ranging from large screen home displays to teleconferencing and wearable electronics are expected to come up.

For registration information, contact Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

(continued on page 96)

SID '83

(continued from page 95)

Technical Program Excerpts*

Session 4: Electroluminescent Displays
Tues 11 am to 12:15 pm, Commonwealth H

Cochairs: M. R. Johnson, Texas Instruments, Inc; and E. Schlam, U.S. Army ERADCOM

4/1 "Failure Phenomena in ac TFEL Panels"
L. Tannas, Jr, Aerojet ElectroSystems Co

4/2 "Delamination Mechanism in ac TFEL Panels"
K. Okamoto, M. Wakitani, S. Sato, S. Miura, S. Andoh, and S. Umeda, Fujitsu Labs, Ltd

4/3 "Deep Traps and Mechanism of Device Aging in ZnS:Mn ac Thin Film EL Devices"
K. W. Yang, Tektronix, Inc; and S. J. T. Owen, Oregon State Univ

Session 5: Contrast Enhancement Filters
Tues 11 am to 12:15 pm, Commonwealth J

Cochairs: C. Infante and A. Silzars, Tektronix, Inc

5/1 "Contrast Enhancement and Halo Suppression for CRTs"
J. Rancourt, Optical Coating Lab, Inc

5/2 "Multilayer Coatings for CRT Panels"
T. Jones and S. Saulsbury, Optical Coating Lab, Inc

Session 6: Liquid Crystal Applications
Tues 11 am to 12:15 pm, Commonwealth K-L

Cochairs: A. R. Kmetz, Bell Labs; and J. H. Becker, Exxon Enterprises

6/1 "An LC/CRT Field-Sequential Color Display"
R. Vatne, P. Johnson, and P. Bos, Tektronix, Inc

6/2 "A π-Cell Optical Switch"
P. Bos, P. Johnson, and K. R. Koehler-Beran, Tektronix, Inc

6/3 "Gray-Scale Imaging on a Multiplexed LCD"
Y. Suzuki, M. Sekiya, K. Arai, and A. Ohkoshi, Sony Corp

Session 7: Large Screen Displays
Tues 2 to 5 pm, Commonwealth H

Cochairs: L. T. Todd, Jr, Projectron, Inc; and R. Tsai, Singer Librascope

7/1 "A 64M-Pel Liquid Crystal Projection Display"
A. G. Dewey, S. F. Anderson, G. Cheroff, J. S. Feng, J. Gordon, C. Handen, J. W. Johnson, J. Leff, R. T. Lynch, C. Marinelli, R. W. Schmiedeskamp, and H. M. Sierra, IBM General Products Div

7/2 "Video Projection Systems and Optics"
B. H. Welham, U.S. Precision Lens, Inc

7/3 "Liquid Crystal Message Center Display"
J. R. Burns and G. W. Taylor, Princeton Research Assocs, Inc

7/4 "A 70-ft^2 Message Board Using TFEL Devices"
J. Duncker, Lohja Corp

7/5 "Three-Color, 8′ x 8′ Display Using a Laser-Addressed Liquid Crystal Light Valve"
S. Kubota, S. Sugama, S. Naemura, and N. Nishida, Nippon Electric Co, Ltd

7/6 "A Fiber-Optic Magnifying Display Panel"
W. E. Glenn, NY Institute of Technology

Session 8: Optical Storage and Thermal Recording Media
Tues 2 to 5 pm, Commonwealth J

Cochairs: R. C. Durbeck, IBM Corp; and J. Mir, Eastman Kodak Co

8/1 "Video Disk Technology—Present and Future"
K. I. Hagemark, 3M Co

8/2 "Archival Te-Alloy Optical Recording Films"
L. Vriens, B. Jacobs, D. Broer, and W. de Poorter, Philips Research Labs

8/3 "CS_2-Te Thin Films for Optical Disks"
N. Funkaoshi, Y. Asano, and H. Yamazaki, NTT Tokai

8/4 "Thermal Ink Transfer Printer with Ink Layer Reformation Mechanism"
S. Nakaya, K. Tanoshima, I. Nose, and T. Takeda, OKI Electric Industry Co

8/5 "Passive Thermal Display"
S. Nakaya, K. Tanoshima, I. Nose, and T. Araki, OKI Electric Industry Co

Session 9: Color CRTs
Tues 2 to 5 pm, Commonwealth K-L

Cochairs: I. M. Wilson, Zenith Radio Corp; and I. F. Chang, IBM Research Center

9/1 "Resolution of Data Display Tubes"
P. G. J. Barton, Philips Research Labs

9/2 "Horizontal MTF Analysis for Color CRTs"
A. Kojima, Sony Corp

9/3 "The Effects of Asymmetric Optics on Spot Size and Deflection Defocusing in Picture Tubes"
D. J. Bechis, RCA Labs; and H. Y. Chen, RCA Picture Tube Div

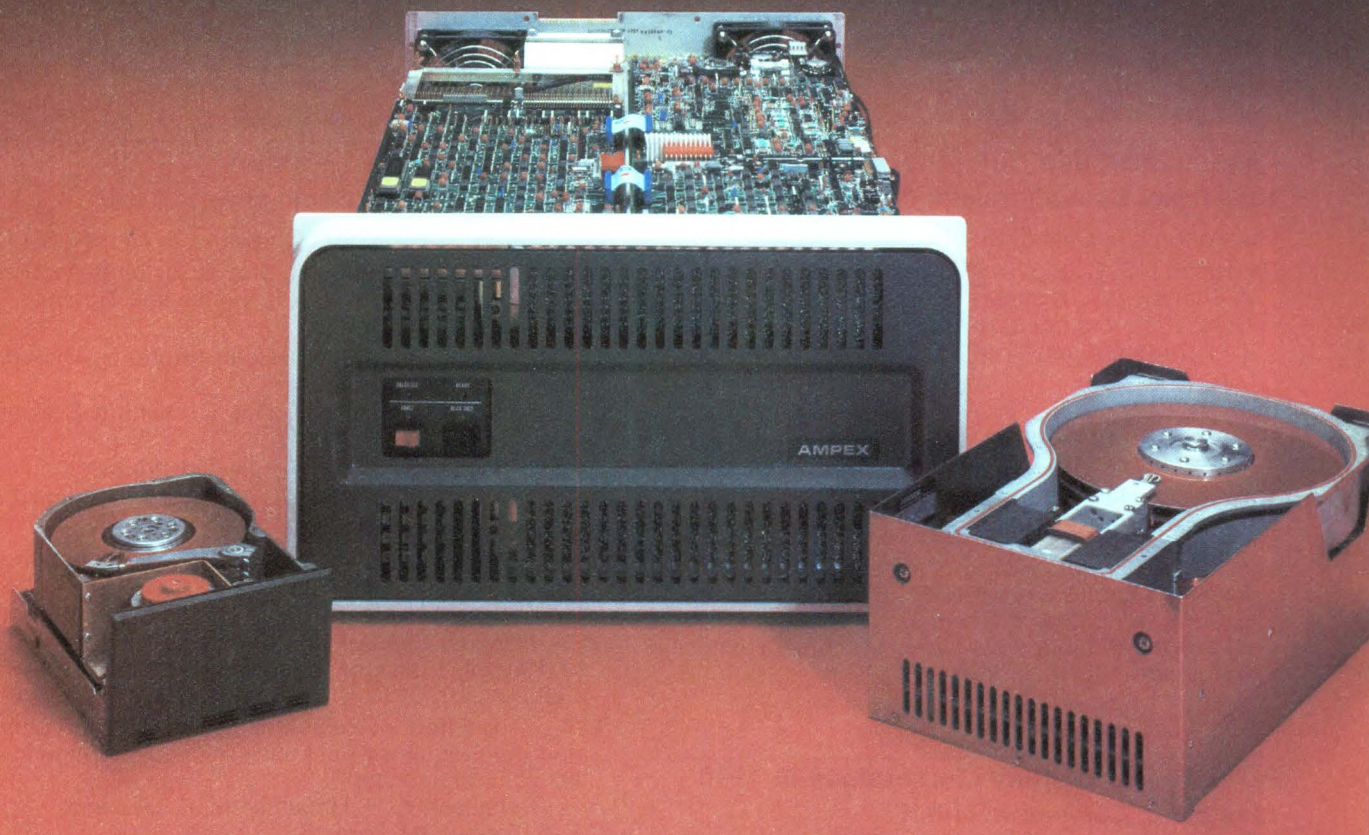
9/4 "Expanded Field Lens Design for Inline Color Picture Tubes"
R. C. Alig, RCA Labs; and R. H. Hughes, RCA Picture Tube Div

9/5 "A High Brightness Shadow Mask Color CRT for Cockpit Displays"
R. C. Robinder, D. J. Bates, P. J. Green, G. D. Lewen, and D. R. Roth, Tektronix, Inc

(continued on page 98)

*Technical Program sessions are subject to last-minute changes.

WE'VE GOT IT ALL



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CIRCLE 60

SID '83

(continued from page 96)

Panel 1: Portable Computers and Displays
Tues 8 pm, Commonwealth H

Moderator: I. F. Chang, IBM Research Center

Panelists: I. F. Chang, IBM Research Center; J. Ellenby, Grid Systems Corp; S. T. Mayer, Atari Corp; P. R. Van Loan, Hewlett-Packard Co; and J. D. Vurich, Axlon Corp

Panel 2: The Need for Color in Displays
Tues 8 pm, Commonwealth J

Moderator: J. A. Mays, Systems Research Lab, Inc

Panelists: R. Barbin, RCA; R. Carpenter, USAF Human Research Lab; R. Carter, Naval Biodynamics Lab; L. Silverstein, Boeing Commercial Airplane Co; H. Snyder, Virginia Polytechnic Institute; and G. Spencer, Raytheon Corp

Panel 3: The Display Marketplace in 1990
Tues 8 pm, Commonwealth K

Moderator: A. Silzars, Tektronix, Inc

Panelists: M. Alam, A. D. Little; J. Costellano, Electronic Display World; E. Yamazaki, Hitachi Mobara Works; W. Hughes, RCA Picture Tube Div; C. Slupek, Chrysler Corp; and C. Trish, Gnostics, Inc

Session 10: System Applications and Image Processing
Wed 9 to 11:50 am, Commonwealth H-J

Cochairs: D. D. Pinsky, Interstate Electronics Corp; and J. Brindle, Naval Air Development Center

10/1 "Radar Image Generation Using a Laser and Fluorescent Pigment Screen"
H. Yamada, M. Ishida, M. Ito, and K. Miyaji, Shibaura Institute of Technology

10/2 "A Modular Large Screen Display System"
J. M. Kaster, Research Institute for Anthropotechnik

10/3 "A Realtime Raster Graphic Display System Utilizing Two Frame Buffers"
E. Piller, Technical Institute of Vienna

10/4 "Representation Protocol for Videotex Systems"
A. W. Mansky, General Instrument Corp, Jerrold Div

10/5 "Computer-Generated Pictures of Protein Structures"
A. M. Lesk, Medical Research Council Laboratory of Molecular Biology; and K. D. Hardman, Harvard Univ

10/6 "Multifunction Keyboard Using Programmable LED Matrix Keys"
R. J. Spiger, Boeing Aerospace Co

Session 11: Ink-Jet Printers
Wed 9 to 11:50 am, Commonwealth K-L

Cochairs: H. L. Funk, IBM Corp; and T. Werner, 3M Co

11/1 "Ink-Jet Printing Using Drop Collision Deflection"
T. Tsuzuki, M. Suga, H. Naganuma, and T. Itano, Nippon Electric Co, Ltd

11/2 "High Resolution Full-Color Printer by Microdot Ink-Jet Printing Method"
T. Yamada, Y. Matsuda, T. Doi, E. Yoshino, S. Sagae, and Y. A. Ono, Hitachi Ltd

11/3 "High Resolution Color Ink-Jet Printer"
J. Maeda, K. Fukushima, A. Akao, and E. Shimizu, Sanyo Electric Co, Ltd

11/4 "The Influence of Ink/Media Interactions on Copy Quality in Ink-Jet Printing"
C. W. Jaeger, H. Le, and D. Titterington, Tektronix, Inc

11/5 "Droplet Ejection of DOD Ink-Jet Printer"
M. Kutami, T. Mizuno, T. Satoh, and T. Matsuda, Fujitsu Labs, Ltd

11/6 "The Effect of Pulse Shape on the Drop Volume and the Frequency Response of Drop-on-Demand Ink-Jet Transducers"
H. Gerhauser, K. H. Hirschmann, F. Lee, and F. E. Talke, IBM Corp

Session 12: CRT Technology
Wed 2:15 to 5 pm, Commonwealth H-J

Cochairs: A. Martin, Thomson-CSF; and J. Mays, System Research Labs

12/1 "An Oscilloscope CRT with Meshless Scan Expansion"
B. Janko and N. Franzen, Tektronix, Inc

12/2 "A Quadrupole Scan Expansion Lens System"
N. Frazen, Tektronix, Inc

12/3 "Garnet Phosphor for Heads-Up Display"
B. R. Critchley and J. Lunt, Thorn EMI Brimar, Ltd

12/4 "A 230-MHz Bandwidth High Resolution Monitor"
C. Infante, D. Denham, and B. McKibben, Tektronix, Inc

12/5 "A 7-GHz CRT for Realtime Digital Oscilloscopy"
C. Loty, Electronic Lab of Applied Physics

Session 13: Gas Discharge Displays
Wed 2:15 to 5 pm, Commonwealth K-L

Cochairs: P. Ngo, American Bell; and P. Pleshko, IBM Corp

13/1 "A 2000-Character Self-Scan Memory Plasma Display"
G. Holz, D. Miller, and J. Ogle, Burroughs OEM Corp

(continued on page 100)

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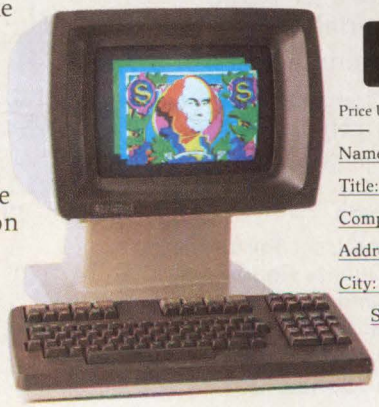

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CIRCLE 61

SID '83

(continued from page 98)

13/2 "Two Equal Brightness On-States in ac Plasma Panels Driven by Conventional Sustain Waveforms"
L. F. Weber and C. N. Steiner, Univ of Illinois, Computer Based Education Research Lab; and M. J. Marentic, Interstate Electronics Corp

13/3 "A Gas Discharge Display"
M. DeJule, A. Sobel, and J. Markin, Lucitron, Inc

13/4 "The Flatscreen Display Construction and Circuitry"
D. Glaser, M. DeJule, C. J. Whelchel, C. S. Stone, A. Sobel, and J. Markin, Lucitron, Inc

Session 14: Active Matrix Addressing

Thurs 9 am to 12:15 pm, Commonwealth H-J

Cochairs: D. E. Castleberry, General Electric Co; and T. C. Maloney, Panelvision Corp

14/1 "A Self-Aligned a-Si TFT Matrix Circuit for LCDs"
K. Asama, T. Kodama, S. Kawai, Y. Nasu, and S. Yanagisawa, Fujitsu Labs, Ltd

14/2 "A 220- x 240-Pixel a-Si TFT Transmission Matrix LCD"
K. Suzuki, T. Aoki, M. Ikeda, Y. Okada, Y. Zohta, and K. Ide, Toshiba Electron Devices and Device Engineering Lab

14/3 "A Liquid Crystal Matrix Display Using Te-TFTs"
M. Matsuura, Y. Takafuji, K. Nonomura, F. Funada, and T. Wada, Sharp Corp, Central Research Labs

14/4 "A 480- x 480-Element Dichroic Dye MOS LCD"
K. Kasahara, K. Sakai, Y. Komatsubara, A. Saito, K. Ide, S. Matsumoto, and H. Hori, Toshiba Electron Device Engineering Lab, Research and Development Center

14/5 "Electrical Properties of CdSe TFTs Prepared by Photolithography"
M. J. Lee, C. P. Jidge, and S. W. Wright, Imperial College Thin Film Lab

14/6 "High Voltage Polycrystalline Si TFT for Addressing EL Devices"
T. Unagami and B. Tsujiyama, NTT Ibaraki Electrical Communication Lab

14/7 "A 240- x 240-Element LC Video Display Addressed by Poly-Si TFTs"
S. Morozumi, K. Oguchi, S. Yazawa, T. Kodaira, H. Ohshima, and T. Mano, Suwa Seikosha Co, Ltd

Session 15: Human Factors in Video Display Terminals

Thurs 9 am to 12:15 pm, Commonwealth K-L

Cochairs: D. Hanson, Boeing Commercial Airplane Co; and H. Snyder, Virginia Polytechnic Institute

15/1 "Effects of VDTs on Telephone Directory Assistance Representatives"
S. J. Starr, Bell Telephone Labs

15/2 "Touch Entry Devices and User Performance Part I: Quantifying Display Quality Requirements"
R. J. Beaton, J. H. Schulze, and H. L. Snyder, Virginia Polytechnic Institute

15/3 "Touch Entry Devices and User Performance Part II: Relationship between Optical Quality and User Performance"
J. H. Schultz, R. J. Beaton, and H. L. Snyder, Virginia Polytechnic Institute

15/4 "CRT Symbol Subtense Requirements"
S. P. Roger and J. C. Gutmann, Anacapa Sciences, Inc

15/5 "Brightness and Color Contrast of Information Displays"
G. Murch, M. Cranford, and P. McManus, Tektronix, Inc

15/6 "Color Contrast Effects on Visual Performance"
T. M. Lippert, W. W. Farley, D. L. Post, and H. L. Snyder, Virginia Polytechnic Institute

Session 16: LCD Technology

Thurs 2 to 5 pm, Commonwealth H-J

Cochairs: P. R. Van Loan and F. Kahn, Hewlett-Packard Labs

16/1 "Black LC Guest-Host Systems for Indoor and Outdoor Applications"
B. S. Scheuble, G. Weber, L. Pohl, and R. E. Jubb, E. Merck

16/2 "A 240- x 320-Element MOS Addressed High Resolution LCD"
S. E. Shields, B. G. Fletcher, and W. P. Bleha, Hughes Aircraft Co

16/3 "Integration of Drive ICs onto LCDs"
P. Streit, Videlec, Ltd

16/4 "Design of Reliable Large Area TN LCDs for Automotive Applications"
F. Matsukawa, H. Arai, and H. Yamane, Mitsubishi Electric Corp; and Y. Inoue, Optrex Corp

Session 17: Simulator Displays

Thurs 2 to 5 pm, Commonwealth K-L

Cochairs: R. Hennessy, National Research Council; and S. Black, Evans and Sutherland

17/1 "Simulator Evaluation of Color in Pictorial Flight Display"
T. C. Way, Boeing Military Airplane Co; R. E. Edwards, Boeing Computer Services Co; and J. M. Reising, Air Force Flight Dynamics Lab

17/2 "Visual Scene Manipulations for Simulation Training"
G. Lintern, B. Nelson, and K. Thomley, Canyon Research Group, Inc

17/3 "Reducing Apparent Popping in Area-of-Interest Displays"
K. Berbaum, Canyon Research Group, Inc; and J. Allen, Naval Training Equipment Center

17/4 "Evaluation Techniques for 3-D Displays"
J. O. Merritt, Perceptronics, Inc

17/5 "New Technology Applied to Old Ideas in VTOL Displays"
S. N. Roscoe, New Mexico State Univ

17/6 "The Command Flight Path Display"
S. M. Filarsky, Naval Air Development Center; and G. W. Hoover, Systems Assocs, Inc □

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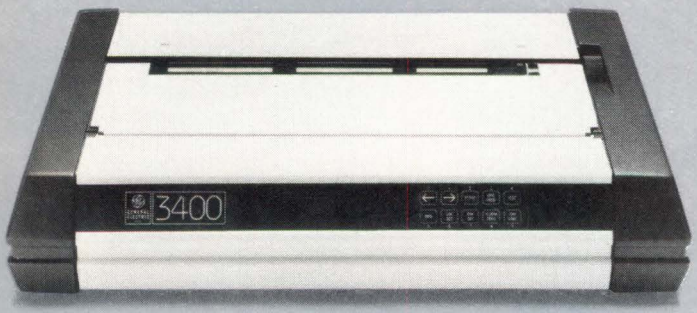
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SECURING DATA INEXPENSIVELY VIA PUBLIC KEYS

Thorny problems of user privacy and data security are multiplying as fast as local area networks. Luckily, public key encryption methods offer an extremely secure medium for information exchange.

by Brian Schanning

Increasing quantities of valuable and sensitive data are being digitally stored and distributed within insecure computer systems. This has created a need for effective protection from unauthorized access. But, to be practical, that protection must also be inexpensive. Data encryption, the traditional solution for classified military communications, is one possible answer.

Conventional cryptographic protection in a communications link involves scrambling the data at the transmitter. Usually, the scrambling algorithm is controlled by a key, such as a many-digit variable entered by the equipment operator. An identical key must be present in the receiving equipment to unscramble the data. These keys, kept secret from everyone outside the communications system, must have as much protection as the data they guard.

The usual method for distributing cryptographic keys is to physically carry them to the transmitting and receiving sites, an awkward and expensive process for even the simplest networks. This approach proves totally inadequate for local area networks (LANs) with inherently large connectivity and access to public and private long-haul systems.

Fortunately, the public key cryptographic concept, first proposed by Stanford University researchers Diffie and Hellman [1] and pioneered by Rivest, Shamir, and Adleman at MIT,[2] may supply a sorely needed solution to the problems of key distribution and protection.

Brian Schanning is the leader of the computer network analysis group at The MITRE Corp, Burlington Rd, Bedford, MA 01730. Mr Schanning has a BSEE from the University of Notre Dame and an MSEE from Stanford University.

Public key systems employ two distinct keys for each user—an encrypting key and decrypting key. The former is available to all members of the network; the latter, a secret code number selected by each individual user, need never be disclosed to anyone (including personnel at other communication sites). The 2-key approach allows any sender to encipher messages through the universally known encrypting key of the intended recipient. However, only the intended recipient can decipher the message, since only he knows the decrypting key. In short, the public key approach allows the secure exchange of messages without prior secret exchange of keys.

For any public key system to succeed, however, prolonged knowledge of the public encrypting key must never compromise the secret decrypting key. By exploiting the complexity of certain classic mathematical problems, this may be achievable. For example, efficiently factoring very large numbers into their component primes is an exercise that has bedeviled leading mathematicians for centuries. Despite the advent of powerful modern computing resources, factoring a general 200-digit composite number, which is the product of two 100-digit primes, can still take over 100 years.[2] The persistent difficulty of this and similar problems has been suggested as the basis on which to effectively prevent computation of the secret deciphering key, despite unrestricted knowledge of the encrypting key. Encrypting algorithms, based on this process, are gaining popularity.

Finding the public key distribution algorithm

First proposed by Diffie and Hellman,[1] the discrete exponential public key distribution (PKD) algorithm is particularly amenable to microprocessor software implementation. Remarkably simple in operation, this PKD system depends on some useful properties associated with the exponential function $F(a,x) = a^x$.

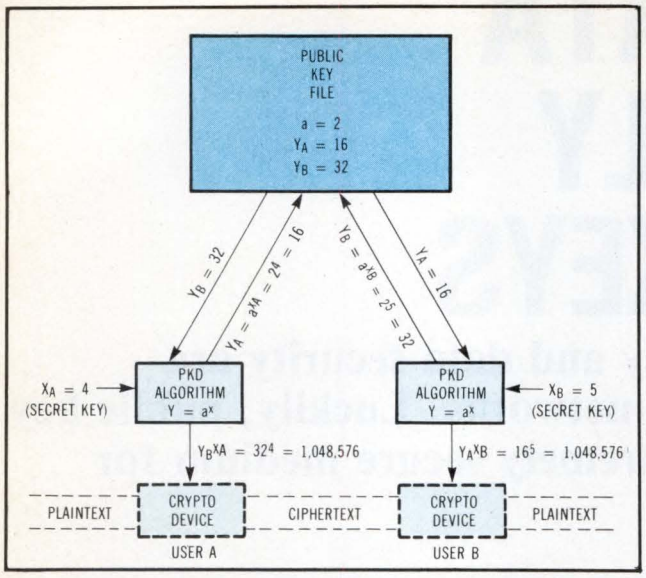

Fig 1 Diffie-Hellman public key model. Users A and B each select a random number (X_A, X_B) to serve as a secret key. This number is then used to calculate a public key. The end result is user A calculating $(a^{X}B)^{X}A$ and user B calculating $(a^{X}A)^{X}B$. These quantities are equal and can be used by A and B as keys for a conventional 1-key system.

First of all, exponentials can be evaluated very efficiently, even with an 8-bit microprocessor. While at first glance it appears that calculating a^x requires $x-1$ multiplications, it is more sensible to use the repeated multiplication and squaring procedure described by Knuth.[3] For example, calculating 27^{23} could be accomplished by multiplying 27 by itself 22 times. A more rational approach would be to produce 27^2, 27^4, 27^8, 27^{16}, (4 successive squaring operations) and then combine 27, 27^2, 27^4, 27^{16} (3 more multiplications) to produce 27^{23}. The total number of multiplications (7) is considerably less than the brute force approach (22), and, in fact, the general algorithm requires no more than $2 \log_2 x$ multiplications to compute a^x.

The second useful property of the exponential operation is its commutativity. Mathematically, this simply means that the order in which the exponentiation is done is immaterial. If

$F_x(a) = a^x$, and $F_y(a) = a^y$,

then

$F_x[F_y(a)] = F_y[F_x(a)]$

or

$(a^y)^x = (a^x)^y$.

For example,

$(2^4)^5 = (16)^5 = 1{,}048{,}576$

and

$(2^5)^4 = (32)^4 = 1{,}048{,}576$.

With these two properties in mind, Diffie and Hellman proposed that their PKD system operate in the following manner. (See Fig 1.) Each user independently chooses a large (100-digit) random number as a secret key. For instance, user A chooses X_A; user B separately chooses X_B. Each is kept as a secret key and only known to its respective creators. Each secret key X_i is used to calculate a public key, Y_i, by raising another number "a" to the X_i power. (The number a is a publicly known parameter that everyone agrees to use as a common base, or "medium of exchange.") Users exchange the Y_is. Thus, A knows Y_B, and B knows Y_A. Each user then raises the other's public key to his own secret key power. Therefore, user A calculates $Y_B{}^{X}A$ and user B calculates $Y_A{}^{X}B$. Substituting for the Y_i, it is evident that A has calculated $(a^{X}B)^{X}A$ and B has calculated $(a^{X}A)^{X}B$.

Actually, the system just described is impractical since raising 100-digit numbers to 100-digit powers could result in a 10^{102} digit number. Consequently, all calculations must be performed in a finite field. Diffie and Hellman originally proposed using a field with p elements, where p is a 100-digit prime number. In such a system all results are reduced by taking the modulo remainder when divided by p. Thus, in a field with 7 elements [GF(7)] 2 x 4 mod 7 = 8 mod 7 = 1. Exponentiation in such a field takes $2 \log_2 p$ multiplications and divisions. The commutative property still holds in such a field. The previous example now becomes $(2^4)^5$ mod 7 = (16 mod 7)^5 mod 7 = 2^5 mod 7 = 32 mod 7 = 4 and $(2^5)^4$ mod 7 = (32 mod 7)^4 mod 7 = 4^4 mod 7 = 256 mod 7 = 4.

While the discrete exponent implemented in GF(p) will certainly work, a more efficient approach is to use another type of finite field, an extension field $GF(p^n)$. Instead of performing integer arithmetic modulo p, polynomials of degree $n-1$ [with coefficients in GF(p)] are manipulated modulo, an nth-degree irreducible (ie, prime) polynomial. When p = 2, these manipulations actually end up being shifts and "exclusive OR" operations on n-bit words, which ordinary microprocessors can perform very efficiently. PKD computations in $GF(2^{127})$, using an irreducible polynomial $X^{127} + X + 1$, formed the basis of MITRE's PKD experiments. Exponentiation in $GF(2^{127})$ with an 8-bit Z80A takes about 4 to 6 s; 2 to 4 s on a 16-bit LSI-11/23. GF(p) calculations of a similar size can take 10 to 30 s on a PDP-11/45.

The security of all this, however, depends on a third property: the difficulty of computing the inverse function. If $F(a,x) = y = a^x$, the inverse function is known as a logarithm: $F^{-1}(a,y) = x = \log_a y$. If this is easily done, a third party can find out the secret keys of any user and thus compute K_{ij} for any user-pair i, j. The problem of calculating logarithms for large numbers has received much attention lately; the best known procedure[4] appears to be computationally infeasible when number size exceeds about 400 bits (120 digits). While there is no guarantee that this is the best method possible, the simplicity of the underlying problem statement makes it conceivable that some lower bound may eventually be established. Until this occurs, the discrete exponential PKD system will remain an intriguing, but unsanctioned approach to supporting key distribution for conventional 1-key systems.

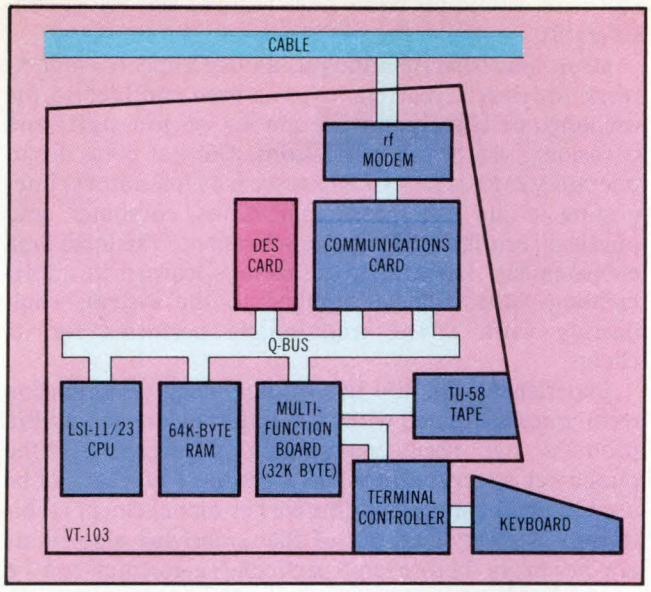

Fig 2 The MEMO workstation is based on the DEC VT-103. Addition of modem, communications controller, and DES card results in a secure data transmission and reception medium.

A practical application of public keys

In June of 1978, a small research team, funded under MITRE's Independent Research & Development Program, was assembled to explore public key concepts. Following a theoretical review and tradeoff analysis of proposed public key systems, the PKD system previously discussed was selected for microprocessor implementation and use with the National Bureau of Standard's data encryption standard (DES)[5] algorithm. This 64-bit block cipher requires a 56-bit key and is available in chip form from a variety of manufacturers. MITRE's approach was to employ the 2-key concept to accomplish the secure distribution of a single key for use with a commercially available and federally approved 1-key data encryption algorithm. By late 1979, this public key/DES hybrid cryptosystem was being demonstrated on the MITRENET broadband 1M-bps carrier sense multiple access (CSMA) LAN.

Following this initial success, problems that might arise in a practical application of these techniques were studied. The newly emerging technology of electronic mail, which requires privacy and authentication, a highly interconnected network for its many potential users, and data protection (both in transit and in storage), seemed an ideal testbed. The result: the MITRE encrypted mail office (MEMO) system.

MEMO enables a user to compose, mail, retrieve, and locally store sensitive correspondence, all under the protection of public key and DES. As initially configured, the system consists of three office workstation terminals connected to MITRE's LAN. Correspondence can be locally composed and encrypted, then sent to a network mailbox. Each recipient scans an in-box and selectively retrieves messages for viewing. Messages can also be saved locally on encrypted tape cartridges. A printer and public key distribution center (PKDC) are also part of the network.

The office workstation, the user's primary MEMO interface, is a Digital Equipment Corp VT-103 terminal. Basically, the VT-103 is a modified VT-100 terminal with internal LSI-11 backplane and card cage. The VT-103, when combined with a radio frequency (rf) modem and a Z80 based CSMA communications card (built to a MITRE design), is the standard MITRENET terminal. A number of host computers, accessible by such terminals, include an IBM 3031 (running MVS/TSO), IBM 4341 (VM/CMS), PDP-11/45 (RSX-11M), four PDP-11/70s (RSTS/E or PWB/UNIX) and a VAX-11/780 (PWB/UNIX). Currently, MITRENET supports 150 such terminals.

Normally, all MITRENET terminals send and receive data in the clear on a single 50.5-MHz carrier. MEMO, on the other hand, is an experimental subnetwork, sending and receiving electronic messages via encrypted data packets.

To accomplish this, the MITRENET terminal was augmented with the DEC KDF11-SE processor option consisting of three dual-width boards: the LSI-11/23 central processing unit (CPU), a 64K-byte random access memory (RAM) board, and a 32K-byte multifunction board. A MITRE designed dual-width DES encryption board is also included. The MEMO VT-103 was purchased with the TU-58 cartridge tape driven option. Fig 2 summarizes the configuration of this MEMO office workstation.

Another major element of the system is the mailbox. In order to conserve funds, a workstation was converted to mailbox duty by adding a CDC 9427H cartridge disk drive and Xylogics dual-width Q-bus controller interface board.

Other support elements in MEMO consist of the PKDC and printer. Each is connected to the MITRENET cable via standalone bus interface units with integral S-100 backplane, Z80A microprocessor, rf modem, and communications card. An S-100 DES card, appropriate RAM, and/or interface cards complete their configuration.

Software to enable security

Software for the office workstation and the mailbox was programmed in MACRO-11 using a PDP-11/45 development facility. Four separate RSX-11 tasks were designed: NETWRK, LOGIN, CRYPTO, and APPL. The first three tasks were common to both the workstation and the mailbox, and the fourth task was tailored to the application of a particular element. Mailbox tasks ran under RSX-11M. For the office workstation, RSX-11S, a memory resident subset of the RSX-11M system, was used. The ability to develop and transport the software between the development PDP-11/45 (running RSX-11M) and the target LSI-11/23s (running RSX-11M or 11S) proved to be a great convenience.

The PKDC and printer software were implemented in Z80 assembler code. Development and testing were done in RAM on an S-100 based CROMEMCO System 3 microcomputer. All code was then "burned" into erasable programmable read only memory and transported to the target machines.

Unfortunately, no Q-bus compatible DES devices are commercially available. Fig 3 depicts the architecture of the board that was designed. It consists of a Western

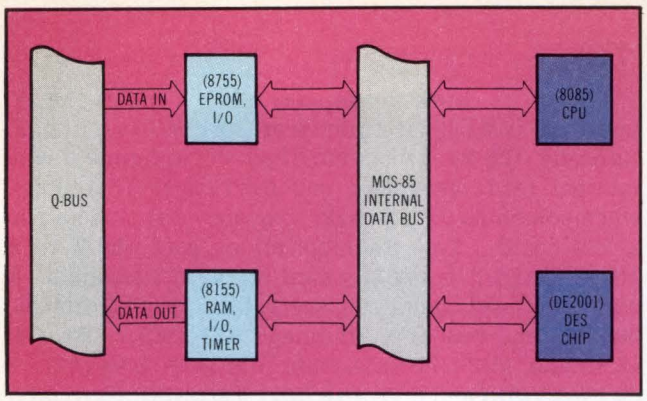

Fig 3 Data encryption standard board features a 1M-bps encryption chip and an 8085 microprocessor for control. Eight DES keys are available.

Digital DES chip (1M-bps maximum encryption rate) controlled by an Intel 8085 microprocessor. The 8085 was programmed to accept up to eight separate DES keys and operate in the electronic code book, cipher feedback or cipher block chaining modes.[6] The design was similar to the original S-100 based DES board design used in the PKDC and printer. In fact, the Q-bus prototype was developed by first connecting an MDB Q-bus foundation board with our S-100 DES board and bypassing the S-100 bus logic.

From MEMO system definition to integration testing, the entire project took approximately 18 months and involved 3.5 man-years of effort. Approximately 77.8k bytes of PDP-11 and Z80 assembler code were developed. The use of a high order language such as Pascal, especially for the office workstation application software, would probably have reduced this effort considerably.

MEMO has been operating as an experimental subnetwork for over a year. Its use has been confined to the exchange of correspondence among project staff, and occasional visitor demonstrations. Current plans are to operate MEMO as part of a LAN security laboratory, integrating it into other communications, computer, and physical security techniques applicable to the local area environment. Hopefully, the lessons learned in implementing MEMO will be applied to the systems engineering work MITRE traditionally performs for its clients.

Experience with the use of public key distribution techniques combined with conventional data encryption products has been encouraging. Conceptually, the public key approach provides a flexible tool that can be used to build a more distributive key management architecture. Security analyses of the underlying algorithms are necessary before any particular algorithm can be recommended for widespread use. The National Bureau of Standards is currently soliciting a proposed public key cryptographic algorithm standard.[7] In the interim, future data network designers should give increasing attention to the problems of data security. Networks initially designed with a communication security capability in mind will inevitably prove more competitive than networks requiring expensive retrofits or replacements. Network designers should begin to consider security in future product plans. When customers awaken to the very real security risks currently being taken, nothing but the best will be acceptable.

References

1. W. Diffie and M. E. Hellman, "New Directions in Cryptography," *IEEE Transactions on Information Theory*, vol IT-22, no 6, Nov 1976, pp 644-654.
2. R. L. Rivest, A. Shamir, and L. Adleman, "A Method for Obtaining Digital Signatures and Public-Key Cryptosystems," *Communications of the ACM*, vol 21, no 2, Feb 1978, pp 120-126.
3. D. E. Knuth, *The Art of Computer Programming, Volume 2: Seminumerical Algorithms*, Addison-Wesley, Reading, Mass, 1981.
4. L. Adleman, "A Subexponential Algorithm for the Discrete Logarithm Problem with Applications to Cryptography," *20th Annual Symposium on Foundations of Computer Science*, Oct 1979, pp 55-60.
5. "Data Encryption Standard" (*FIPS PUB 46*), National Bureau of Standards, Jan 15, 1977.
6. "DES Modes of Operation" (*FIPS PUB 81*), National Bureau of Standards, Dec 2, 1980.
7. "Solicitation for Public Key Cryptographic Algorithms," National Bureau of Standards, *Federal Register*, vol 47, no 126, June 30, 1982, p 28,445.

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ADAPTING FORTH TO A MULTI-USER WORLD

This latest version of Forth for use on the M68000 processor addresses 16.7M bytes of memory, features improved arithmetic performance, and incorporates system calls into its threaded lexicon.

by Bruce Sweet

Design engineers have good reason to consider Forth for new microprocessor based equipment. Forth's threaded code offers rapid execution speed and low memory overhead—critical advantages in many applications. Further, since there is now a multitasking version of Forth available, the opportunity exists to forge extremely high performance applications in the Forth language.

Forth is particularly powerful when running under a multitasking operating system. This was Forth's original configuration, which was developed to use with minicomputers. It is loaded into random access memory (RAM) from the system disk, but instead of taking over the machine, this version runs concurrently with the operating system. It often uses some of the operating system features to enhance its own power.

In a system using an advanced 16-bit microprocessor such as Motorola's M68000, valuable processing power is wasted if the entire central processing unit and its resources are dedicated to just one task. Since applications usually grow larger and more sophisticated with time, Forth, running under an external operating system, offers increased power and flexibility for such applications.

Hemenway/Forth is aimed at demanding realtime applications in laboratory, industrial automation, data aquisition, and process control markets. Termed a nonstandard superset of Forth-79, this 16-bit version of Forth incorporates two unusual and particularly noteworthy design characteristics. First, it incorporates an internal user-transparent 32-bit architecture. Second, it runs concurrently with MSP/68000, Hemenway's realtime, multitasking operating system.

Because of these design innovations, this 16-bit version of Forth provides the user with exceptional power. For example, users can access the complete 16.7M-byte address space of the M68000 microprocessor. In addition, enhanced arithmetic operations are provided, including 32 times 32-bit multiply/divide and modulo instructions in software. Additional 16- and 32-bit arithmetic operations are performed in hardware for high throughput.

Users can extend the Hemenway/Forth word set to include all of the MSP/68000 operating system call routines, thus greatly improving programming efficiency. Shared memory and intertask communication abilities allow users to combine application-specific routines written in Hemenway/Forth with routines written in other languages, including assembler.

Finally, the MSP/68000 operating system, using the random file input/output (I/O) system calls, handles Hemenway/Forth's mass storage operations. The language package incorporates four 1024-byte block buffers. These reduce the number of disk I/O operations, thus increasing throughput. Both hard and floppy disks can be accommodated.

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The challenges

Forth's inventor, Charles Moore, originally defined Forth to be based on a 16-bit internal structure capable of addressing 64K bytes. Therefore, adapting the language to the 68000 poses three major software engineering challenges. The 68000 addresses 16.7M bytes, due to its 24-bit addressing architecture. This is much larger than the Forth-79 standard requires, but it

represents a significant performance enhancement. The first challenge is taking advantage of this feature.

The 68000's instruction set includes powerful addressing modes that are perfect for Forth's address interpreter. However, they are based on 32 bits. The second challenge is incorporating the modes into the language. Finally, with all the 68000's power and capability, the third challenge is to implement Forth so that the user can most effectively harness the machine's assets.

In responding to the first challenge, address space, the Hemenway/Forth design team adapted the language to a 32-bit architecture. This enabled it to use the 68000's extended addressing ability. Although current 68000s use only the first 24 bits for their addressing range, it was decided that the Forth design would incorporate all 32 bits of addressing for future versions of the 68000. This immediately made the language nonstandard according to the Forth-79 specification. But, it also allowed the design team to use all of the processor's addressing modes and its full address space.

These decisions created a 32-bit wide Forth cell, rather than a standard 16-bit cell. Then, the return and data stacks, as well as the address interpreter, were based on this new 32-bit cell. These changes made the 68000 look more like the ideal Forth machine.

A closer look at the Forth address interpreter and the 68000 instruction set shows the reasoning behind this approach. In the standard implementation of Forth, the address interpreter fetches a 16-bit word from memory and uses it to point to an address. But the 68000 uses sign extension in 16-bit fetches to fill the high order word in its 32-bit address registers. For example, a MOVE.W $7FFF,A1 instruction loads a $00007FFF into register A1, while a MOVE.W $8000,A1 loads $FFFF8000. Consequently, in a system with more than 64K bytes of memory, a 16-bit indirect fetch will not fetch the contents of the next word above $7FFF in the 68000's zero page.

Unless this problem is avoided, what should be one instruction becomes three. Specifically, to execute MOVEA.W (A1)+,A2, one must perform CLR.L D1, then MOVE.W (A1)+,D1, and finally, MOVEA.L D1,A2. Further, this extra code must be included within the Forth address interpreter, the most frequently executed section of the language. Thus, execution speed suffers considerably.

Fortunately, because the design team chose a 32-bit implementation of the language, they were able to meet the second challenge and exploit the power and variety of the 68000's addressing modes. For example, an efficient solution to the problem of an indirect word fetch with paged memory combines three instructions into one. By using the MOVEA.L (A1)+,A2 instruction, the following address interpreter code is produced

```
NEXT MOVEA.L (A1)+,A2     ; Get next instruction, increment
     MOVEA.L (A2)+,A3     ; Get parameter address, increment
     JMP(A3)              ; Jump indirect to code address
```

This solution takes advantage of the fact that the 68000 allows user-defined stacks, and that any of the 68000's address registers can be used as a stack pointer. Specifically, the MOVE.L Rn, –(An) and MOVE.L (An)+,Rn instructions are used to push and pop the Forth data and return stacks, respectively.

In addition to extending the Forth address range, this approach provides several advantages. For example, it allows the machine to deal directly with integers as large as $7FFFFFFF. By contrast, in a standard 16-bit stack implementation, double-number words must be used to handle 32-bit integers. Such words must pop the stack twice: first acquiring the high order cell, and then the low order cell. While some 16-bit Forth versions use extended instruction sets to handle double-precision numbers, Hemenway/Forth handles them intrinsically and transparently.

The final challenge posed by implementing Forth on a 68000 based system—how to give the user the maximum benefits of the hardware/software combination—proved most interesting. As mentioned, 8-bit versions of Forth typically run as standalone systems. However, most of the 68000's power is lost when the computer is dedicated to just one application. If the language runs on an interrupt driven, multitasking operating system instead, Forth and other programs can execute concurrently in a realtime environment.

It involved several steps to modify the language to run under such an operating system. The initial transformation was straightforward. Two Forth primitives, KEY and EMIT, were changed. Previously, these primitives performed single-character I/O through asynchronous communications interface adapter hardware drivers. Now, they are calls to the operating system's console drivers.

The operating system's random access file method was used to give Forth mass storage ability. Specifically, each random record on the MSP disk was built to be 1024 bytes—the size of a Forth BLOCK. A Forth block buffer handles loading, editing, and general access to data stored on disk; a simple virtual memory system manipulates the data flow between the disk and this buffer.

To implement virtual memory, Hemenway/Forth uses four block buffers and a least-used buffer protocol. This provides faster direct memory access for data in RAM than more frequent disk I/O operations. The two Forth words, BLOCK and SAVE-BUFFERS, handle the reading and writing of Forth blocks. Within these words, instead of having sector read/write routines, I/O is vectored to the MSP operating system's random record read/write calls. Because the I/O is now bound to the system, Forth is portable to any hardware configuration on which the operating system is running, including those incorporating Winchester disk drives.

Adding new words adds power

Both Hemenway/Forth and the MSP/68000 operating system can be extended. Users themselves can expand the Forth word set. For example, a Forth word can be created to take advantage of the system primitives that deal with multitasking operations and user-added hardware devices. Sharing memory and disk directories between Forth applications and other programs involving various languages or processes is also possible. Additionally, users can take advantage of the different serial and parallel drivers provided within the operating system.

A specific example puts the power of this feature into perspective, while also highlighting how user-written extensions can be implemented. Suppose that access to

TABLE 1

Constructing a New Forth Primitive

Instruction		Mnemonic			Comment
00000A64	00000007			DC.B 7,'GETTIME'	
00000A6C	00000A38	R		DC.L ENDDUP	
00000A70	00000A74	R		DC.L GETTCD	
			GETTCD	@GETTIM	GETTIM SYSTEM CALL
00000A78	2B02			MOVE.L D2,-(A5)	PUSH DAY OF YR/YR
00000A7A	2B01			MOVE.L D1,-(A5)	PUSH HR:MIN:SEC
00000A7C	6000 12A4			BRA NEXT	JUMP ADDRESS INTERPRETER
00000A80	00000A80	R	ENDGTIM	EQU *	
			*		
			*		

the operating system's realtime clock is required to set and display time from within Forth. To do this, one must first generate two new Forth primitives to get and set the system clock. These primitives are called GETTIME and SETTIME, respectively.

GETTIME is an example of how simple most new primitives can be with the MSP/68000's system calls. Constructing a primitive can involve as few as three lines of code. As seen in Table 1, @GETTIM is the system call GETTIM. This call returns the time of day in register D1.L and the Julian date in D2.L. In both cases, the data are binary coded decimal (BCD) bytes. Each register uses only the three lowest order bytes. Thus, if the current time is 2:45:10 168/82, D1.L contains XX024510 and D2.L is filled with XX016882.

The next two instructions simply push the contents of the D1 and D2 registers on the data stack, pointed to by A5. The final instruction in the routine, the fourth line of code, jumps to the address interpreter routine NEXT.

After creating the GETTIME and SETTIME primitives, the user must know how to use them. SETTIME accepts five parameters on the data stack. Thus, to set the time to 10:30:00 168/82 data are entered in the format 10 30 0 168 82 SETTIME.

To display the time, the user must write some Forth code to convert the two BCD parameters into a readable display on the cathode ray tube (CRT). See the Figure. The first algorithm used gets the time, then converts the two BCD parameters to binary, and finally displays the time in the format hr:min:sec day of year/year.

In line 4 of the program listed in the Figure, the new Forth word BCDCON uses the word U/MOD. The U/MOD is an unsigned 32-bit divide operation that first expects a

```
>4 LIST
  0 : . NUM <# #S #>TYPE ;
  1 : . 2NUM .NUM .NUM ;
  2 : . TIM .2NUM 58 EMIT .2NUM 58 EMIT .2NUM
  3    DROP SPACE .2NUM .NUM 47 EMIT .2NUM ;
  4 :  BCDCON 6 0 DO 16 U/MOD LOOP DROP ;
  5 :  TIME GETTIME SWAP BCDCON 7 ROLL BCDCON . TIM ;
  .
  .
  .
 15
  OK
```

The screen listing is the Forth code to display time (copyright of Hemenway Corp, 1982).

16-bit unsigned divisor, and then a 32-bit unsigned dividend, to be placed on the stack. When invoked, it leaves the unsigned quotient and remainder on the stack. BCDCON's operation exploits the fact that dividing by 16 is the same as shifting right 4 bits, leaving the BCD digit as the remainder on the stack. Thus, this word basically shifts each BCD digit on the stack as a 32-bit binary number. Then, it drops the leftover high order byte from the data stack.

Line 0 defines the word .NUM. Using the three Forth words <# #S #>, it converts a binary number on the stack into an American Standard Code for Information Interchange (ASCII) string (in this case, only one character per stack entry) and leaves a count and pointer to this string on the stack. Completing this definition, the word TYPE uses the count and pointer as parameters and displays the string on the console. In keeping with Forth's hierarchical structure of programming, line 2 defines .2NUM, which prints two numbers on the console.

Line 5 of the code defines TIME. When invoked, this Forth word displays the time and date in the previously described format. The sequence of operations is GETTIME leaves the two BCD parameters on the data stack, with the time of day on top followed by the Julian date. SWAP then interchanges these parameters. BCDCON converts the top parameter to six binary numbers. Next, 7 ROLL gets the Julian date parameter, which is now the seventh value on the stack, and moves it to the top. BCDCON again converts this parameter to 6 more binary values on the stack, increasing the total to 12 parameters. Finally, the new word .TIM (line 2) takes these parameters and formats them on the display.

To understand how .TIM works, the user must know that the word EMIT prints an ASCII value from the stack. According to the ASCII decimal conversion chart, 58 corresponds to a colon, while 47 converts into a slash. Therefore, .TIM prints the hours, a colon, the minutes, a colon, and the seconds. It then drops the high order 0 byte from the day of the year, prints a space and the day of the year, and ends by printing a slash followed by the year.

In addition to the programming efficiency described in the preceding example, Hemenway/Forth on the 68000 also provides high benchmark performance. Though benchmarks can be, and often are, tailored to supply the results manufacturers want, a good benchmark test will provide insight into processing power. Consider, for example, the Sieve of Eratosthenes algorithm. (See Jim

Forth fundamentals

Forth is a threaded, interpretive language that is written using reverse Polish notation (RPN). It stresses simplicity and enables rapid program development and execution.

Key to the language is the Forth word. In fact, the entire language is composed of primitive and secondary words. A Forth primitive forms the building block for all other words. An example is the address interpreter word, NEXT. Secondary Forth words consist of threads of addresses pointing to either primitive or other secondary words. Eventually, all threads point at an executable primitive.

There is a close correlation between Forth and most assembly languages. For example, the Forth interpretive pointer (IP) corresponds to the assembler program counter (PC). Essentially, the IP points to the PC and executable code.

Forth is infinitely extendable—all secondary words are made up of previously defined words. Words are stored in the Forth dictionary, a linked list of system and user-defined words. This dictionary can be subdivided into application-specific vocabularies, such as the Forth text editor.

The most common method for defining new Forth words is the colon (:) definition. The syntax to define a new word in Forth is : NEWNAME {BODY} ; where NEWNAME is the name of the new word and {BODY} is the word making up the body of the new definition. The semicolon (;) serves as the terminator.

When the Forth text interpreter encounters the colon, it invokes the Forth compiler. Here lies a distinction that sets this language apart from others: Forth is both interpreted and compiled. To see how this is achieved, take a close look at the defining word (:) in the Figure.

Forth's dictionary contains vocabularies that are linked lists of Forth words. Contained in these lists are two pointers, CONTEXT and CURRENT. CONTEXT points at the vocabulary to be searched in a dictionary lookup; CURRENT, at the vocabulary to which the word is to be linked. Upon execution of : , CONTEXT is set the same as CURRENT. The threaded code of : next contains the word CREATE, which scans ahead and parses the name of the new definition into a length-significant character format, to be stored in the CURRENT vocabulary (referred to as the header). CREATE also establishes the links in the CURRENT vocabulary. Subsequently, : changes the Forth system from its interpretive mode to a compiling mode by setting a variable called STATE to a nonzero value. Now the system is ready to compile the body of the new word into the dictionary.

When compiling, Forth gets the next word and searches through the dictionary's CONTEXT vocabulary. Finding the word, it checks to see if the word is IMMEDIATE. An IMMEDIATE word has a bit set in its header to indicate immediacy; if the bit is set, the word is to be executed and not compiled. The ; at the end of a definition is an example of an immediate word. (If the word is not IMMEDIATE, the code address is added to the threaded code making up the new definition.)

When the compiler encounters the ; in the NEWNAME example, the definition is terminated by a word called EXIT (a primitive of ;) and the STATE variable is cleared. This returns Forth to the interpretive mode.

Forth's ability to define new words gives it immense power. For example, an entire program can be executed just by entering the word that defines it.

Programs are developed and subsequently saved in a Forth SCREEN. A SCREEN is a 1024-byte block of memory that is displayed on a CRT console in a 16-line by 64-character format. SCREENS can be built by loading a Forth text editor from a previously defined screen. Internally, a SCREEN is interpreted the same as if the data had come from the console input buffer.

A structured language, Forth includes WHILE, REPEAT, and DO loops. These, however, must be defined in RPN. Moreover, in Forth, all looping mechanisms must be compiled. When TENLOOP is compiled, the limit and index are stored as literals in the new dictionary entry. At runtime they will be pushed on the data stack as parameters for the DO. The DO instruction subsequently pushes these parameters onto the return stack and executes the code up to the word LOOP. Then, LOOP performs a checking operation to see if the index is less than the limit. If it is, Forth increments the index and performs another iteration; if the index is at the limit, execution resumes until the end of the definition.

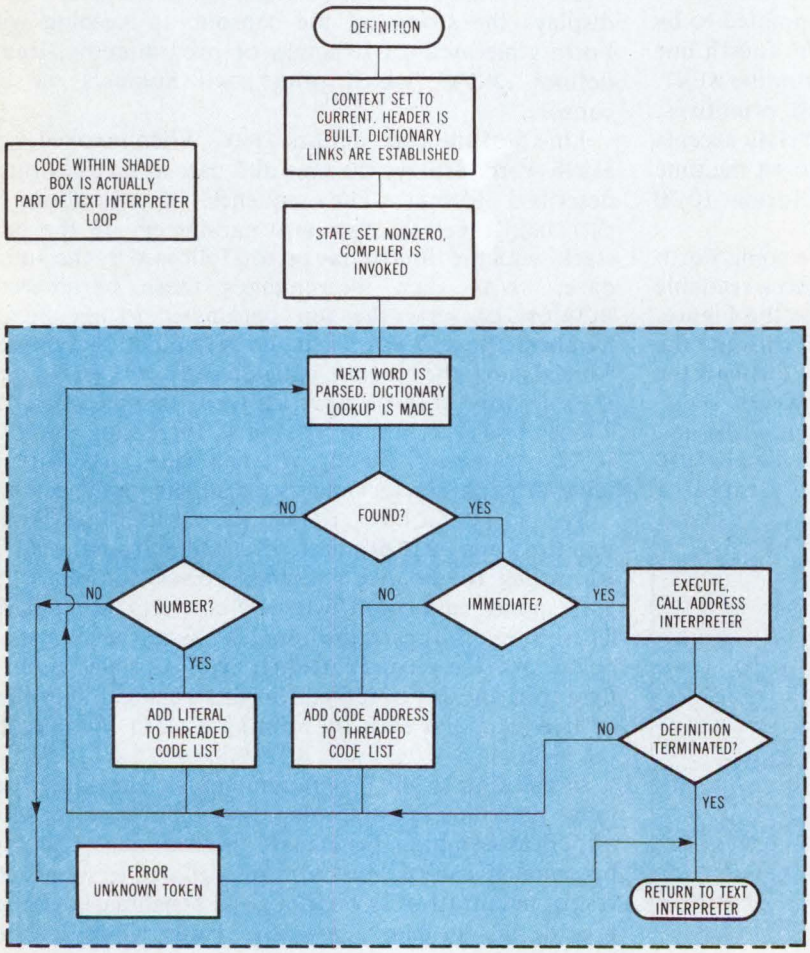

TABLE 2

Sieve of Eratosthenes Benchmark Comparisons

The contenders	Execute time for 10 iterations (seconds)
68000 based alternatives	
Hemenway/Forth (8 MHz)	27.0
Assembly (8 MHz)	1.12
Motorola Pascal (4 MHz)	14.0
MT Microsystems Pascal (4 MHz)	9.0
RSI Pascal (4 MHz)	10.2
Forth versions	
Hemenway/Forth (68000, 8 MHz)	27.0
Decus Forth (PDP-11/70)	11.8
Polyforth (Texas Instruments 990/10)	60.2
JKL Forth MDS (8080, 2 MHz)	440.0
Fig-Forth (Z80, 4 MHz)	85.0
Forth (6502, 1 MHz)	265.0

Gilbreath's "A High-Level Language Benchmark," *Byte*, Sept 1981, pp 180-198.) This algorithm, which computes all prime numbers from 3 to 8190, avoids division and uses the knowledge that certain numbers (eg, even numbers and multiples of primes) cannot be prime. It executes quickly and accesses a considerable amount of memory.

Using a Microbar Model DBC68K-80 microcomputer board operating at 8 MHz with no wait states, and running the Forth program shown in listing 9 of the referenced article, Hemenway/Forth executed 10 iterations of the Sieve of Eratosthenes algorithm in 27 s.

Comparative execution times for other types of M68000 code and other versions of Forth are supplied in Table 2. With the exception of high horsepower PDP-11/70 applications, Forth running on Motorola's M68000 outpaces its competitors.

Such speed, flexibility, and power are key reasons why this implementation of Forth is worthy of consideration. No longer relegated solely to industrial control applications, modern Forth is proving to be an efficient development language. Its extendability and common sense structure are giving Forth an enthusiastic and vocal following. Forth's debut on 16-bit, multitasking systems should further enhance its fortunes.

Bibliography

L. Brodie, *Starting Forth*, Prentice Hall, Inc, Englewood Cliffs, NJ, 1981. "The Forth Language," *Byte*, Aug, 1980, special issue.

H. Katzan, Jr, *Invitation to Forth*, Pertrocelli Books, Inc, New York, NY, 1981.

R. G. Loeliger, *Threaded Interpretive Languages*, Byte Books, Peterborough, NH, 1981.

R. N. Ting, *Systems Guide to Fig-Forth*, Offete Enterprises, Inc, San Mateo, Calif, 1981.

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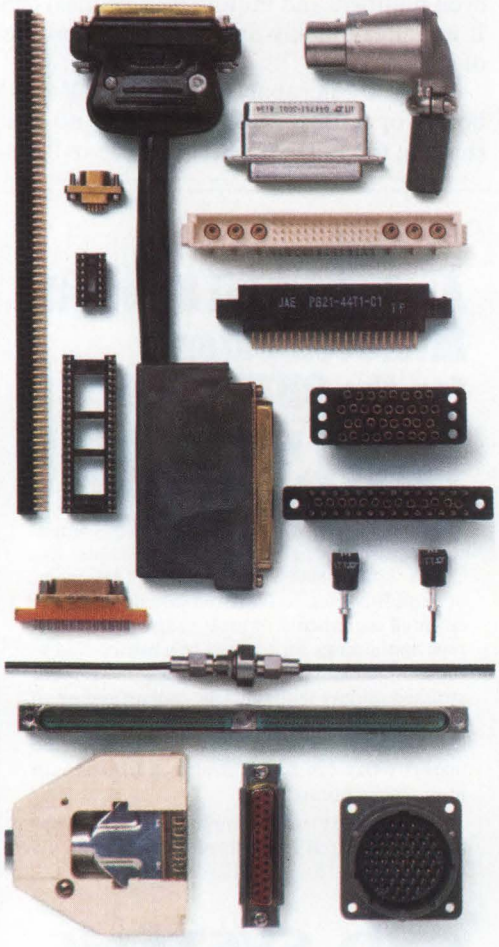
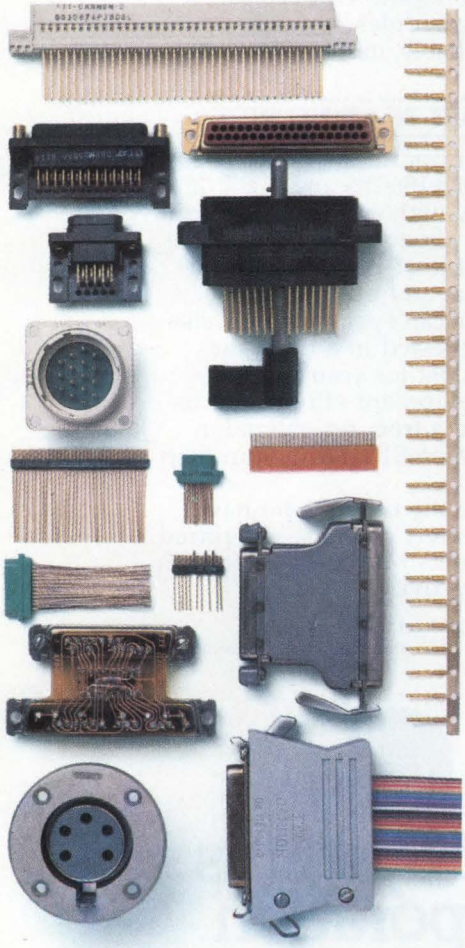


connection.



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CIRCLE 70

AUTHORING A DEDICATED OPERATING SYSTEM IN PASCAL

Designers: Create compact, customized operating system kernels for concurrent realtime applications.

by Christopher DeMers

Traditional operating systems are general purpose in nature. They must function over a wide variety of applications and this very universality makes them less than ideal for dedicated applications.

To design an operating system for dedicated microcomputer applications, a distinction must be made between software development and runtime environments. The development environment resembles the general purpose operating system environment in that it must service people and have efficient tools for software development (eg, editors, compilers, assemblers, linkers, and debugger utilities). It differs from the general purpose system in that a development environment is used to develop object code for another microcomputer.

The function of the runtime execution environment is to react to the actions of surrounding equipment quickly enough to exercise control. While the development environment is flexible, human oriented, and relatively slow in responding, the runtime environment is rigid, machine oriented, and extremely fast in responding. Because the attributes of these two environments conflict, it is unrealistic to expect that the same operating system can serve both functions efficiently. The Table, "Dedicated and General Purpose Application Distinctions," summarizes these differences.

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Taking parts of the development system and building a truncated operating system is the traditional way of fitting general purpose operating systems to dedicated applications. Because it is difficult to separate the functions of a general purpose operating system (Fig 1), the resultant software product often has a general purpose flavor. Furthermore, since operating system components are not divided into read/write and read only categories, read only memory, programmable read only memory, and electrically programmable read only memory (ROM, PROM, and EPROM) cannot be used in the target system.

Rapid growth of the microprocessor/microcomputer market compelled Digital Equipment Corp to design a total system for the development of dedicated applications. The resultant software system is actually two distinct operating systems—one for development (RT-11), the other for the target application. Specifically designed for a dedicated environment, the application system contains only those services needed by the application (Fig 2). This dedicated operating system is automatically built by developing the application in a higher level language.

MicroPower/Pascal, the software system, represents a synthesis of system implementation language, development environment, and runtime environment. It is a realtime, multitasking modular operating system designed for dedicated microcomputer applications. Operating system access and application programming take place in an extended version of standard Pascal.

The language

Pascal is used as both the application language and the system implementation language. Traditionally, assembly language has been used as a system implementation language to perform hardware-specific functions.

Dedicated and General Purpose Application Distinctions

Dedicated	General purpose
Minimal memory (RAM/ROM)	Large memory (all RAM)
Software resides in ROM or is loaded from device at power-up	Software resides in mass storage
Wide range of environments (disk-killers, dust/heat)	Computer room, clean environment
Operating system exactly tailored to fit each application	Operating system is tailored to satisfy a wide range of needs
Many hardware interfaces are application specific (custom)	Most hardware interfaces are general purpose and known to the operating system
Much code is hardware specific, requiring MACRO or other system implementation language	Most code is written in machine independent, general purpose languages (FORTRAN, COBOL, BASIC)
Target machine is customized for application (debug on target)	Host machine is the target (debug on host)

But MicroPower/Pascal provides the necessary facilities in a high level language. It is standard Jensen and Wirth Pascal, currently tracking the International Standards Organization standard, with extensions to permit concurrent realtime applications and hardware interfacing.

Pascal was chosen because it is a widely used, structured programming language and offers most of the required features. Standard Pascal is block structured, which encourages the grouping of statements into logical components, thus increasing code modularity. It is strongly typed, meaning that all variables must be defined and cannot deviate in definition throughout the program.

Another powerful feature of Pascal is data structure. With Pascal, the programmer extends the language to include whatever combinations of data types the application requires. Consequently, unlike simple data, data structures (eg, integers, real numbers, and characters) can be combined in one structure called a record.

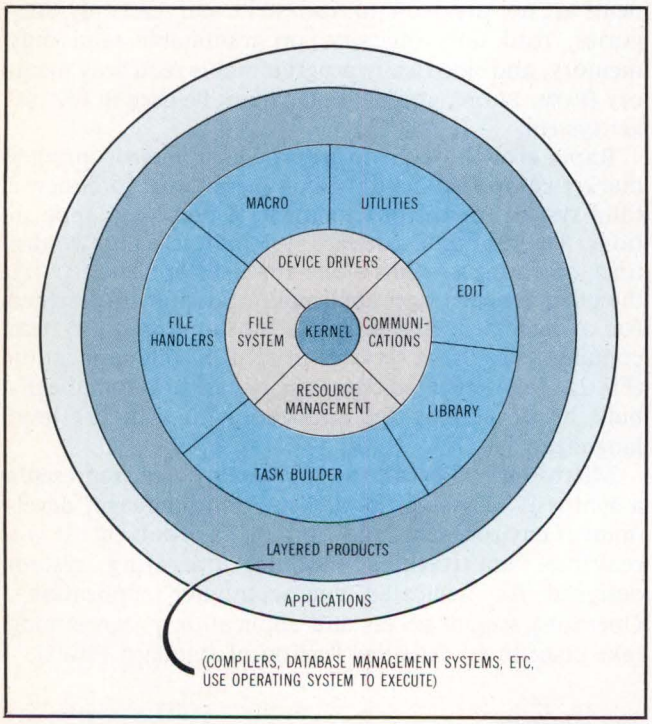

Fig 1 Shown is a breakdown of traditional operating system components and structure. Such monolithic code is not easily broken into subsets or excerpted. Thus, using it for dedicated applications often proves impossible.

Finally, Pascal code is easily maintained. The constructs provide partial documentation and strongly typed variables keep the code consistent. Code written by programmers is quite readable, though not exactly self-documenting, and it requires fewer comments.

Standard Pascal does not have input/output capabilities, nor can it perform many of the other functions required for dedicated application programming, such as bit manipulation, concurrency, and/or realtime response. Consequently, extensions must be added to the language to take advantage of the operating system's (the kernel's) features.

Pascal compilers usually require the application code to be written in a single source program. MicroPower/Pascal has separate module compilations that allow the application to be divided into separate programs. Each programmer writes and debugs modules. During integration of the modules, only the linkages (data transfers) need to be tested. Modular construction encourages libraries of commonly used routines to be built for use across different applications, thus freeing programmers for more original work. Separate module compilation increases productivity and efficiency by allowing a programming team to work on the same application.

Extending the language

A number of extensions to MicroPower/Pascal improve efficiency in the runtime environment: concurrency, interrupt handling, exception handling, and data type extension. Concurrency (multitasking) is essential in many dedicated realtime applications since executing code segments can cause significant events to be missed. Typically, operating systems have some method of supporting concurrency, but most application languages do not. FORTRAN, for instance, does not allow two or more subroutines to run simultaneously. If multitasking is required, it has to be done by the operating system working around the higher level language, rather than in concert with it.

MicroPower/Pascal, on the other hand, allows the designer to treat each independent program segment, called a process, as if it is executing concurrently with the others. Because the processor can only run one instruction stream at a time, each process will, in fact, run at different times. The programmer must divide the application into processes and determine their priorities. The MicroPower kernel scheduler switches between the

processes according to their relative importance (priority). If the processes are identical (ie, the application is managing several identical devices), they can share an instruction sequence but have separate data areas. In this way, MicroPower/Pascal supports reentrant code so that the application is not burdened with extra copies of the code.

Multitasking requires interprocess communication and synchronization. This is accomplished by the use of semaphores and messages implemented by the MicroPower kernel and defined in extended Pascal. Semaphores are the basic mechanisms for synchronizing processes. There are several types of these data structures: binary and counting semaphores control access to shared resources; message semaphores (packet queues) provide interprocess communication (mailboxes); and ring buffers are used for data transfer from one process to another.

Interrupt handling routines are usually written in assembly language since higher level languages do not support them. Device handlers can be written in MicroPower/Pascal, however, allowing the programmer to do the entire application in a higher level language. This is possible because extensions to the language permit access to individual bits. Interrupt routines in MACRO-11 (the PDP-11 assembler) still have slightly more efficient code than Pascal and may be used in time-critical situations. But the small increment gained in execution time will not, in most cases, be worth the loss of programming efficiency.

In many dedicated applications, error conditions can stop the system from running. Designers try to anticipate all such errors and write software routines to handle each type. Unfortunately, because there are so many error conditions that can arise while executing an application, it is impossible to anticipate all of them. Some are hardware detected, such as a parity error or a divide by zero. Other errors, such as reading a floating point number into an integer variable, are detected by the vendor's software. Still others are application-specific cases detected by the application software.

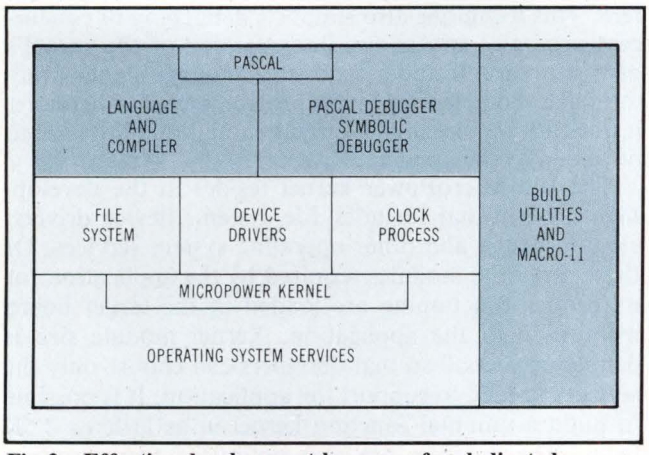

Fig 2 Effective development language for dedicated applications must exhibit modularity if efficient operating systems are to be constructed. Shaded components reside in the host system and aid the development process. Unshaded components minister to the needs of the target system and its application.

Given the multitude of errors possible, it is not surprising that designers occasionally overlook some and thus develop unreliable code.

MicroPower/Pascal simplifies the problem by recognizing most errors and creating a single error reporting mechanism. A single exception handling routine, written in Pascal, can deal with all errors—hardware or software detected, vendor or user defined. However, if different parts of an application require that particular error conditions be handled differently, each can have its own exception handler.

This error detection concept is important in applications that cannot leave parts of the system (eg, valves, motors, and switches) in random states. Because the software can monitor and trap these exception conditions, orderly shutdown of the system is ensured.

Finally, standard Pascal offers strong data typing and can extend the language to support additional data types. MicroPower/Pascal takes full advantage of this and adds data type extensions to enable the designer to describe the entire realtime application. Such extensions include, but are not limited to, UNSIGNED integers, READ ONLY and WRITE ONLY variables, and the attributes AT, PACKED, STATIC, GLOBAL, EXTERNAL, and VOLATILE.

The AT attribute allows the programmer to fix a variable's position at a particular memory location. For example, the location of a device register could be defined in Pascal without using assembly language.

Using the Pascal RECORD construct, each bit or group of bits can be logically assigned to a variable. This eliminates the time-consuming task of calculating AND/OR masks to access the bits. It is even possible to define and access the same memory location with more than one name by making multiple assignments to that location (see Fig 3).

The PACKED attribute is applied to records, sets, and arrays. It induces the compiler to produce efficient code for that particular data structure and therefore conserves memory. Although this attribute is described in the Jensen and Wirth standard, it is often omitted from Pascal compilers because it is difficult to implement. This particular implementation, however, not only saves memory but also allows the designer to describe the required size and position boundaries of the field. In order to access a memory location that has each of its bits defined (as in a control and status register), it is essential that the data access be in packed format.

An integer is normally read as 15 bits plus a sign bit. An UNSIGNED integer permits those cases where all 16 bits should be read as data (eg, a 16-channel parallel interface). UNSIGNED integers also allow description of integers between 0 and 65,535, permitting a program to compare virtual address pointers and to perform address arithmetic calculations.

READ ONLY and WRITE ONLY are used to describe hardware registers with these attributes. If the program tries to change variables so assigned (eg, writing to a READ ONLY register) the compiler will generate an error message at compile time. Such attributes are assigned because of hardware restrictions and/or programming convention and clarity. Following a convention of READ ONLY for a device status register isolates the programmer

```
CONST
        input = FALSE;
        output = TRUE;

TYPE
        open_close  = (open,close);
        start_stop  = (start,stop);
        on_off      = (on,off);

VAR
      output_csr: [AT(%O'164164'),VOLATILE] PACKED RECORD
                  direction: [POS(8)] BOOLEAN;
                  END;

      outputs:  [AT(%O'164166'),VOLATILE,]PACKED RECORD
                oil_pump:          [POS(0)]  start_stop;
                water_pump:        [POS(1)]  start_stop;
                oil_valve:         [POS(4)]  open_close;
                water_valve:       [POS(5)]  open_close;
                oil_drain:         [POS(6)]  open_close;
                water_drain:       [POS(7)]  open_close;
                oil_heater:        [POS(8)]  start_stop;
                water_heater:      [POS(9)]  start_stop;
                mixer:             [POS(11)] start_stop;
                oil_heater_light:  [POS(12)] on_off;
                water_heater_light:[POS(13)] on_off; ;
                END;

(* Enable parallel interface for output *)
output_csr := output;
(* start water pump, water heater and turn on water heater light *)
WITH outputs DO BEGIN
  water_pump := start;
  water_heater := start;
  water_heater_light := on;
END;
```

Fig 3 This program shows how MicroPower/Pascal interfaces to a parallel device that controls various pieces of machinery. Devices are turned on or off with a specific bit in the parallel interface. Parallel device control and status registers reside at an address defined by the AT attribute.

from the device's actual hardware characteristics. This allows error to be found before the program is placed in the target, as well as simplifies debugging.

STATIC variables are assigned fixed memory locations and exist for the duration of the application. This allows programs to enter and exit subroutines without variables being allocated, deallocated, and reallocated again when the subroutine is reentered.

GLOBAL and EXTERNAL attributes refer to links between independently compiled program modules. An EXTERNAL symbol in one module references information globally defined in another module. Conversely, the programmer uses the GLOBAL attribute to indicate to the linking utilities the information that must be shared with other modules.

The VOLATILE attribute is not found in most Pascal compilers, as it is only used with optimizing compilers. Optimizing compilers minimize memory references by putting variables stored in memory into central processing unit (CPU) general purpose registers for fast access. The VOLATILE attribute tells the compiler not to do this. All references to this particular variable must do a memory read and must not store data either in a register or on the stack. This attribute can be used for writing the interface to a device so that the software will retrieve the most current status of the device rather than the old or changed status in the register.

The operating system

Programming dedicated applications requires two environments—development and runtime. In the case of MicroPower/Pascal, the development system consists of PDP-11 or LSI-11, with a minimum of 128K bytes of memory. Most important, the development system must run under the RT-11XM operating system. Soon, MicroPower/Pascal will be supported under the RSX-11M and VAX/VMS operating systems.

The target system, any LSI-11 bus microcomputer, runs under MicroPower—a modular, multitasking kernel. Because it is modular, only those modules required by the application become part of the target operating system. But MicroPower is not a traditional operating system. Instead of being predefined in system generation, it is created when the application code is written. Services needed for the system to run are combined with the application code during the linking phase on the RT-11-based development system. This creates a MicroPower/Pascal memory image to be placed in the target system's memory.

A realtime application designer can build many diversified applications with the same tools. Build utilities help the designer customize each application. Included with the build utilities are the MACRO-11 assembler, the Pascal compiler, and a Pascal symbolic debugger.

Unless requested, the symbolic debugger does not provide information in hexadecimal or octal form, or in machine readable code. Instead, information is provided to the programmer in Pascal and described in the source program. The debugger resides in the host and communicates to a small service module (approximately 800 words) in the target system. All debugging is done in random access memory (RAM). Programs can be committed to ROM after debugging is complete. Although this may require an additional RAM board, it allows the designer to examine and alter data as well as to track the realtime execution of the application in the target system. This technique also supports debugging of concurrent processes and allows interrogation of the kernel's data structure. It understands the language's data structures and those defined by the programmer. Furthermore, it does not require any in-circuit emulation hardware to be added to the system.

The full MicroPower kernel resides in the development system and includes file system, device drivers, clock process, and other operating system services. Of these, only the modules required by the application for its proper functioning are loaded in the target board memory with the application. Kernel module size is deliberately small so that designers can choose only the services needed to support the application. It is possible to build a minimal function kernel in as little as 2.5K bytes. The modules are also optimized for execution speed. This satisfies two crucial realtime application requirements—small memory and speed.

In addition, the kernel manages the interleaving of multiple processes, allowing each process to be written as if it had exclusive use of its own CPU. Such multitasking

allows the separate description of different aspects of the application to reduce programming complexity. The designer need only establish priorities and define interprocess communication. The MicroPower kernel scheduler manages execution of each process.

Both the kernel and the application code can be put into ROM. Code not modified during execution can reside in PROM instead of RAM. Using PROM decreases the amount of RAM needed for the application to just the changeable portions (variables). This has several advantages in dedicated applications. First, code can run immediately upon power-up without memory loading or initialization. Second, the code in PROM is naturally shareable (reentrant) since it is not self-modifying. Finally, the requirement for mass storage is eliminated, although the kernel will support such devices when required. Of course, if the designer wants to use RAM instead of PROM, he retains that option.

Efficiency

A skilled assembly language programmer can produce efficient code. Thus, despite its many features, MicroPower/Pascal would be inadequate if it did not also produce efficient code. To do this, the compiler must generate a correct machine language program from Pascal and then optimize it.

Like most compilers, this one performs local optimization (accomplished by looking at a small sequence of instructions). Unlike most compilers, it does the more difficult tasks of global optimization, common subexpression elimination, jump/branch resolution, and cross jumping or branch tail elimination. The result is a machine language program only slightly less optimized than that produced by a skilled assembly language programmer. Unlike the painstaking work of a human programmer, however, the compiler optimizes code at 400 lines/min. Combining that with Pascal programming's increased speed offers a great improvement in productivity over MACRO-11 coding. In fact, assembly language can be eliminated altogether, since the compiler can directly generate object code without an intermediate MACRO-11 step. The user still has the option of generating a MACRO-11 listing, if needed, just as the option of writing any part of the code in MACRO-11 is retained.

In summary, MicroPower/Pascal uses a structured high level language to build and control a dedicated operating system kernel. That kernel does not exist in its final form until the application code is written on the development system. Build utilities automatically choose the services needed to support the application. Software is debugged in Pascal while running in the target microcomputer. Finally, object code is optimized to produce code nearly as efficient as that of a skilled assembly language programmer. Thus, this extended version of Pascal allows designers to quickly and efficiently program realtime, concurrent tasks for their dedicated applications.

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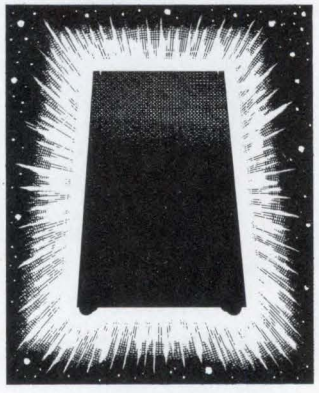

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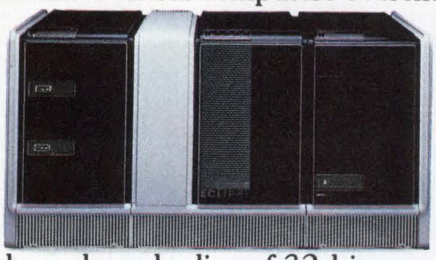

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CIRCLE 72

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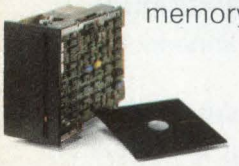

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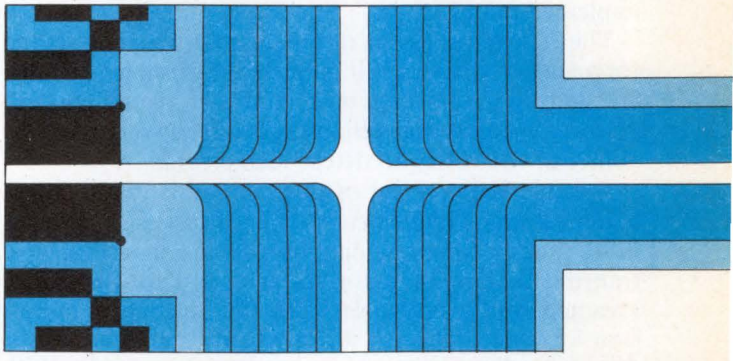
CIRCLE 73

PARALLEL DATA COMPRESSION FOR FAULT TOLERANCE

When computers operating in software implemented fault-tolerant systems exchange the results of their intermediate error calculations, CRC or checksum based data compression is a must.

by James F. Nebus



Presently, all commercially available fault-tolerant systems use one of two major fault recovery approaches: "hot standby" or majority voting. Majority voting systems can be further classified in hardware and software categories.

The fault-tolerant computers belonging to the software voting group are known as software implemented fault-tolerant (SIFT) systems. In the hardware voting scheme, redundant processors are tightly coupled—they often have continuously synchronized clocks and voting on each bus transfer cycle. In contrast, SIFT computers are loosely coupled—they are usually synchronized only at software checkpoints and vote only on inputs and outputs that are external to the computer.

One advantage of SIFT systems is that their hardware bases may be multiple non-fault-tolerant systems interconnected with some additional support circuitry. This makes it convenient to upgrade a non-fault-tolerant system to a fault-tolerant one without obsoleting hardware or applications software. A disadvantage of SIFT systems is the performance degradation associated with software voting. This voting usually consists of exchanging and comparing input/output (I/O) data among the redundant processors. Performance degradation is not a severe problem in existing SIFT computers,[1] as these computers operate in a process control environment. In this application, the I/O data to be sent and compared usually consist of only a few data words. However, in a general purpose, data processing environment, the quantity of data being exchanged and compared is great.

From an application viewpoint, the amount of I/O data may be as much as several kilobytes for printing a file or painting a cathode ray tube screen. Even small I/O data buffers that write a disk sector or transmit a data link control (DLC) message consist of 256 bytes. This type of I/O operation causes substantial performance degradation in a SIFT system. Therefore, data compression techniques should be used to condense the I/O data to a code that is a fraction of the original buffer length. This code can then be exchanged and voted among the processors.

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TABLE 1

Error Detection Probability Formulas with Single Precision Checksum

Condition	Probability of Error Detection
$i < z - \log_2 s$	1
$i = z - \log_2 s$	$1 - 2^{-s}$
$i = z - (\log_2 s) + 1$	$1 - 2^{-s}(1 + sCs/2)$
$i > z - (\log_2 s) + 1$	$1 - 2^{-(z-i)} + 2^{-s}$

Where i = bit position, column (i = 0 is least significant bit)
z = no of checksum bits
s = no of words in data block
C = combinatorial operator, that is

$$sCs/2 = \binom{s}{s/2} = \frac{s!}{s/2!\,(s - s/2)!}$$

The SIFT class of fault-tolerant systems detects faults by employing separate, but redundant, computers that exchange and compare intermediate results under software control. If all processors agree on these results, it is assumed the system is functioning correctly. When the intermediate results are in the form of large data buffers, data compression techniques can be used to reduce these large buffers to a manageable size that can be exchanged and compared. Two methods of parallel data compression, checksums and cyclic redundancy check (CRC) codes, differ in their fault coverage and ease of implementation.

The first requirement of a data compression method for a SIFT system is that it indicate the existence of a discrepancy in the I/O data buffers of each redundant processor. Overall system reliability is directly related to the ability of the voting to detect such errors.

Another requirement of this method is that the data compression be implemented in hardware, since it takes more time to compress data in software than it does to transmit the original data buffer over a 10M-bps local area network. It is also desirable that the data compression logic be connected directly to the data bus and be driven by direct memory access (DMA) methods. With these methods, the time to perform the data compression is limited by the memory's cycle time. For input from external devices, the data compression logic is activated by the presence of an I/O address or DMA channel acknowledge associated with that input device. In this way, data compression can be performed parallel to the placing of input data in memory, thereby eliminating input operations overhead.

How to compress the data

The two simplest methods of data compression are checksums and CRC codes. Today, these techniques are used primarily for error detection. Checksums are often used to verify the contents of programmable read only memories and are usually calculated by software. CRC codes are used primarily for encoding serial data such as DLC messages and disk sectors. The two most prevalent CRC codes are CRC-16 and the International Consultative Committee's CCITT-16.

A checksum is the binary addition of the words in the data block to be compressed. An error in any column of the data block results in either the associated checksum bit column or the carry to the next bit position being in error. For the most significant bit position, the carry bit is lost. As a result, it is more difficult to detect a change in the data block in this column than in the least significant bit position.

In general, the ability to detect an error varies for each column in a checksum. The least significant column provides the most error detection, and the most significant column provides the least. Another disadvantage of checksum data compression is that the checksum calculated is independent of the data values' order in the I/O buffer. This is due to the commutative property of checksum addition.

A single precision checksum is one in which the checksum width is equal to the word width of the data block to be compressed. Table 1 lists the formulas for calculating the error detection probability in each column of a single precision checksum.[2] An extended precision checksum's width is greater than the word width of the data block to be compressed. Let d be the difference between the checksum width and the data block word width. Also, let S be the number of words in the data block to be compressed. If $S < 2^d$, the extended precision checksum will be able to detect an error in any bit position of the data block. In this case, the carry-out of the most significant bit position is always 0, so no information is lost.

Consider the practical example of a 512- x 16-bit I/O buffer to be compressed with a checksum code. Table 2 shows the probability of two such data buffers, differing in particular bit position, to be compressed to the same checksum code. Note that any changes in D_0 through D_7 will be detected, whereas any changes in D_{15} have only a 50% chance of being detected. Assuming that all columns are equally as likely to be in error, the net probability of detecting an error is 0.935. A 26-bit, extended precision checksum would ensure that all errors would be detected for a 512-word data block.

A binary adder of the checksum's width is necessary to implement the checksum logic. A 16-bit checksum

TABLE 2

Positional Checksum Error Probability for 512- x 16-bit Data Block

Column	Error Detection Probability
D_0 to D_6	1
D_7	~1
D_8	0.96
D_9	0.99
D_{10}	0.98
D_{11}	0.96
D_{12}	0.94
D_{13}	0.87
D_{14}	0.75
D_{15}	0.50

Net Error Detection Probability = 0.935

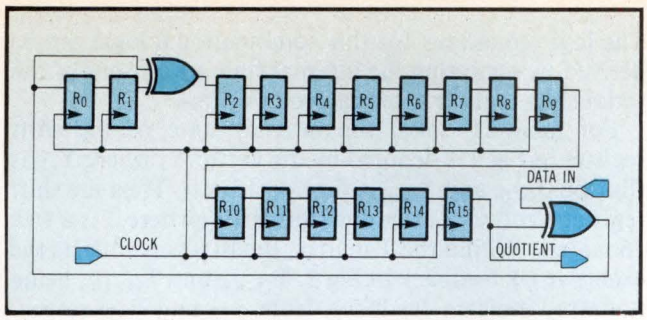

Fig 1 Serial CRC code generator circuit using exclusive OR feedback. Shift registers contain the remainder of modulo-2 division performed on data polynomials. The remainder serves as CRC code used for compression.

register with tristate outputs could be constructed with four 74LS83s, two 74LS273s, and two 74LS244s—a total of eight integrated circuits.

CRC codes and their uses

As mentioned earlier, CRC codes are used primarily for serial data. Data compression using CRC codes is performed by treating the serial data as a polynomial's coefficients. The first bit in an n-bit long serial data stream is the coefficient for X^{n-1}, while the last bit is the coefficient for X^0. For example, the input data 110201021 Hex can be represented as $X^{32} + X^{28} + X^{21} + X^{12} + X^5 + 1$. This input data polynomial is used as the dividend in a modulo-2 division process. Choosing the divisor CRC polynomial as $X^{16} + X^2 + 1$ results in the quotient $X^{16} + X^{12} + X^5 + X^2 + 1$, or 11025 Hex; the remainder is $X^{14} + X^7 + X^4$, or 4090 Hex. By definition, the remainder is the CRC code, and the quotient is discarded.

With serial input data, CRC codes are easily generated using shift registers with exclusive OR feedback as shown in Fig 1. The shift register is initialized to 0. As the serial dividend is shifted into the register the quotient is shifted out, while the remainder is the shift register's internal state after the last shift. The remainder of $X^{14} + X^7 + X^4$ previously mentioned would be represented in Fig 1's circuit by flipflops 14, 7, and 4 being 1, and all others being 0. An alternate divider circuit for the divisor $X^{16} + X^2 + 1$ is shown in Fig 2.[3] The quotient this circuit produces is the same; however, the register's contents after the division is not the remainder as it is in Fig 1.

After the division, the polynomial value for Fig 2's register is $X^{14} + X^7 + X^4 + 1$, or 4091 Hex. Nevertheless, this CRC generator has the same error detecting capabilities as that of Fig 1. If all error patterns are equally likely in a data block of k bits, then the probability that an r-bit-wide CRC code will detect an error is

$$1 - \frac{2^{k-r} - 1}{2^k - 1}$$

As k goes to infinity, this probability approaches $1 - 2^{-r}$. For a 16-bit CRC register, the probability of detecting an error is 0.999985. This figure is somewhat misleading as all error patterns are generally not equally likely, but rather depend on the digital system's implementation. Several types of errors are more likely than others, however, in a bus oriented microcomputer.

The most elementary type of error is the single-bit error. This fault manifests itself in the SIFT voting scheme as a bit change among I/O data blocks. A single-bit error would most likely be caused by an intermittent fault. If the intermittent error occurs in a control signal to a device connected to a parallel bus, it might result in a multibit error among the parallel bits over the bus. This type of error could manifest itself as all, or some subset, of the bits in a single word of the data block in error. Crosstalk among bus signals is another fault that causes a multibit error in which all bits in error occur in the same data word.

Another type of multibit error likely in bus oriented systems is one in which the bits in error are in the same columns, or bit positions. This type of error could result from a faulty bus driver or improper bus loading or timing. If all the bits in a certain bit position are in error, the fault will probably be a hard one. An intermittent fault may cause a few bits in the same bit position to err. Of course, many faults will cause the system to go haywire. These catastrophic failures can be minimized with the use of memory protection, bus parity, and error correction code memories.

A watchdog timer is one method of recovering from the remaining failures in a SIFT system. This timer is initialized with a value that is greater than the longest time between synchronization or voting among processors. It is reloaded with this value every time a processor communicates with the others. If a processor's watchdog timer expires, it resets that processor. The processor then goes through a warm startup before attempting to synchronize with the other processors. Each processor has the other processors' watchdog timer output signals as its inputs.

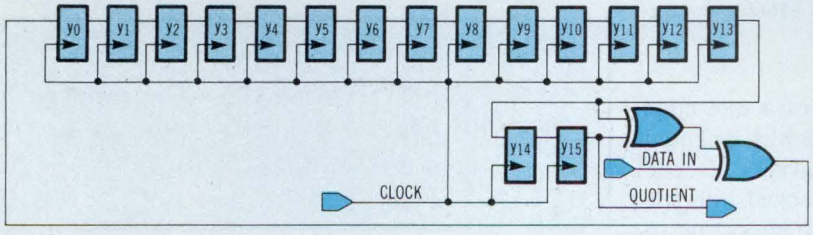

Fig 2 Alternate serial CRC code circuit. CRC results are similar and error detection ability is the same as that of the original CRC circuit, though a slightly different operation is used.

CRC fault coverage

How effective CRC codes are in detecting hardware dependent, noncatastrophic faults can be determined. As mentioned, the probability of detecting a data change between two data blocks is $1 - 2^{-r}$, assuming that all changes are equally likely. Note that this formula does not take the divisor polynomial into account, but only the polynomial's degree or the shift register's length. Called the generator polynomial, this divisor polynomial is reflected in the number and placement of shift register feedback taps, which are included in the exclusive OR function. This generator polynomial, P(X), determines the probability at which certain types of errors are detected, assuming that all error patterns are not equally probable.

It is convenient to view the generator polynomial's role in the data compression process as analogous to the hashing function's role in constructing a symbol table. A good hashing function maps similar symbols into different locations in the symbol table. Likewise, a good generator polynomial maps data blocks with different bit positions that are likely to change, as a result of a fault, into different CRC codes.

Some important theorems relate the generator polynomial to the error detecting properties of CRC codes.[4]

Theorem 1 states that a generator polynomial with two or more nonzero coefficients detects all single-bit errors. The circuits in Figs 1 and 2 provide a different CRC code for each of two data blocks that differ by a single bit, as they are both based on $P(X) = X^{16} + X^2 + 1$.

Theorem 2 states that if P(X) is of degree r and the coefficient of X^0 is 1, then all (r, r) faults are detected using P(X). An (r, r) fault is one in which the erroneous bits are within r consecutive bit positions. At most, r bits can be in error. This theorem addresses the case of a word in the data block that is in error. The polynomial $X^{16} + X^2 + 1$ has a nonzero coefficient for X^0; therefore, it detects all (16, 16) faults.

Theorem 3 states that if each of the irreducible factors of P(X) appears an integral multiple of b times, then as the number of input data bits goes to infinity, the probability of detecting a multibit error in a certain bit position or column is

$$1 - \frac{1}{2^{r/b}}$$

The polynomial $X^{16} + X^2 + 1$, P(X), can be reduced to $P(X) = P_1(X)^2 \cdot P_2(X)^2$, where $P_1(X) = X^6 + X^5 + X^3 + X^2 + 1$ and $P_2(X) = X^2 + X + 1$. Both $P_1(X)$ and $P_2(X)$ are irreducible, prime polynomials. Therefore, the probability of detecting a multibit error in a certain bit position or column is $1 - 2^{-16/2} = 0.996$.

Parallel CRC generator applications

Figs 1 and 2 represent implementations of a CRC code generator for serial data. In a parallel bus oriented microcomputer, it is more applicable to have a CRC code generator in which a word of data is clocked into the CRC generator for each bus cycle. It is also important to have parallel combinational logic calculate the next internal state of the CRC register, rather than try to synchronize a shift register clock to each data transfer. The logic equations for this combinational logic can be derived by analyzing the internal state transitions of the serial shift register after each clock pulse.

For analysis' sake, the internal state of the shift register in Fig 2 is denoted by the vector Y, where $Y_{(1)}$ is flipflop 0, y_0, and $Y_{(16)}$ is flipflop 15, y_{15}. Then the shift register's contents after one shift is TY, where T is a 16 x 16 matrix. Within the T matrix, the first row reflects the exclusive OR feedback in Fig 2. $T_{(1, 14)}$ and $T_{(1, 16)}$, being nonzero, indicate feedback from y_{13} and y_{15}, respectively. The remaining rows in T are the identity matrix, which mathematically represents the shift operation of the shift register. $T_{(2, 1)}$ is the upper left element, and $T_{(16, 15)}$ is the lower right element along the diagonal in this identity submatrix.

In forming a CRC code, the shift register is initialized to zero, $Y_0 = 0$. Define Y_n to be the shift register's state after n shifts. Label the n serial input data bits as D_0, first bit, through D_{n-1}, last bit. After the first bit is clocked into the shift register, $Y_1 = D_0x$ where x is an elementary vector. After the second bit, D_1, is shifted into the register, $Y_2 = D_0Tx \oplus D_1x$. When the third bit is clocked into the register, $Y_3 = D_0T^2x \oplus D_1Tx \oplus D_2x$.

Boolean matrix algebraic rules governing this calculation are fairly straightforward. Boolean matrix multiplication rules are exactly like those for real matrices with one exception: the multiplication and addition operators are replaced by the AND and exclusive OR operators in the Boolean case. For example, consider that T is a p x q Boolean matrix, X is a q x r Boolean matrix, and Y is the product of T and X (Y = TX). Then y is a p x r matrix in which the element y_{ij} in the ith row and jth column is the exclusive OR of the ith row vector of T ANDed with the jth column vector of X. More specifically,

$$y_{ij} = \oplus \sum_{k=1}^{q} t_{ik}x_{kj}$$

In general, the internal state of the shift register after n shifts is

$$Y_n = \oplus \sum_{k=0}^{n-1} D_{n-1-k}T^kx$$

Apply this result to develop the state transition logic equations for the parallel CRC generator. First, the input data must be relabeled to apply to the 16-bit parallel implementation. Instead of the input data stream of $D_0\,D_1\,D_2 \ldots D_{n-2}\,D_{n-1}$ as in the serial case, the input data for the parallel case can be labeled as $D_0\,D_1\,D_2 \ldots D_{14}\,D_{15}\,D_0\,D_1 \ldots D_{14}\,D_{15}\,D_0 \ldots D_{15}$. The words in

$$Y_{n+16} = D_0T^{15}x \oplus D_1T^{14}x \oplus D_2T^{13}x \oplus D_3T^{12}x \oplus D_4T^{11}x \oplus D_5T^{10}x \oplus D_6T^9x \oplus D_7T^8x \oplus D_8T^7x \oplus D_9T^6x \oplus D_{10}T^5x \oplus D_{11}T^4x \oplus D_{12}T^3x \oplus D_{13}T^2x \oplus D_{14}Tx \oplus D_{15}x \oplus T^{16}Y_n$$

Fig 3 Expansion of next state polynomial. The equation provides information on the next state in terms of present register conditions.

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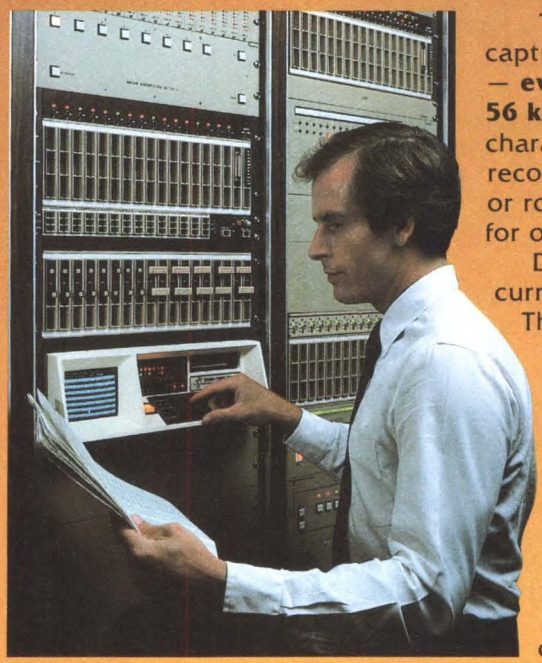

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the data block can be thought of as concatenated to form a serial bit stream with a length 16 times the number of words in the data block. From the preceding formula, the shift register's contents can be expressed as follows when used as a function of their internal state 16 shifts prior to their present state

$$Y_{n+16} = \left[\oplus \sum_{k=0}^{15} D_{15-k} T^k x \right] \oplus \left[T^{16} Y_n \right]$$

For the parallel input case, this formula gives the next state, Y_{n+16}, in terms of the present input data, D_0 to D_{15}, and the present state, Y_n. Fig 3 expands the formula just expressed. Fig 4 lists the state transition equations for each bit position in the parallel CRC polynomial generator. In this figure, Y_i represents the next state and y_i designates the present state of bit position i in the 16-bit parallel CRC generator register.

Parallel CRCs with PALs

The logic required to generate the exclusive OR of multiple signals, as in the state transition equations, lends itself to implementation with a programmable array logic (PAL). The AND-OR logic array of the PAL can be programmed to perform the exclusive OR function. The exclusive OR of n signals can be generated with 2^{n-1}, n input AND gates feeding a 2^{n-1} input OR gate. For example,

$$A \oplus B \oplus C \oplus D = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D}$$

Fig 5 shows the circuit for the parallel CRC generator using PAL family devices.[5] Each PAL implements part of the state transition equations listed in Fig 4. Parallel data are clocked into the register on the rising edge of each data strobe. In order to select only those bus cycles to be included in the CRC calculation, this data strobe must be qualified by an I/O address or DMA channel acknowledge. This circuit assumes that the data are valid 90 ns prior to the data strobe edge, and the CRC

$$\begin{aligned}
Y_{15} &= D_0 \oplus y_{13} \oplus y_{15} \\
Y_{14} &= D_1 \oplus y_{12} \oplus y_{14} \\
Y_{13} &= D_2 \oplus y_{11} \oplus y_{13} \\
Y_{12} &= D_3 \oplus y_{10} \oplus y_{12} \\
Y_{11} &= D_4 \oplus y_9 \oplus y_{11} \\
Y_{10} &= D_5 \oplus y_8 \oplus y_{10} \\
Y_9 &= D_6 \oplus y_7 \oplus y_9 \\
Y_8 &= D_7 \oplus y_6 \oplus y_8 \\
Y_7 &= D_8 \oplus y_5 \oplus y_7 \\
Y_6 &= D_9 \oplus y_4 \oplus y_6 \\
Y_5 &= D_{10} \oplus y_3 \oplus y_5 \\
Y_4 &= D_{11} \oplus y_2 \oplus y_4 \\
Y_3 &= D_{12} \oplus y_1 \oplus y_3 \\
Y_2 &= D_{13} \oplus y_0 \oplus y_2 \\
Y_1 &= D_0 \oplus D_{14} \oplus y_1 \oplus y_{13} \oplus y_{15} \\
Y_0 &= D_1 \oplus D_{15} \oplus y_0 \oplus y_{12} \oplus y_{14}
\end{aligned}$$

Fig 4 State transition equations derived from Fig 3. These equations provide information on individual bit positions within the CRC generator. PLAs are the most practical hardware implementation of these equations.

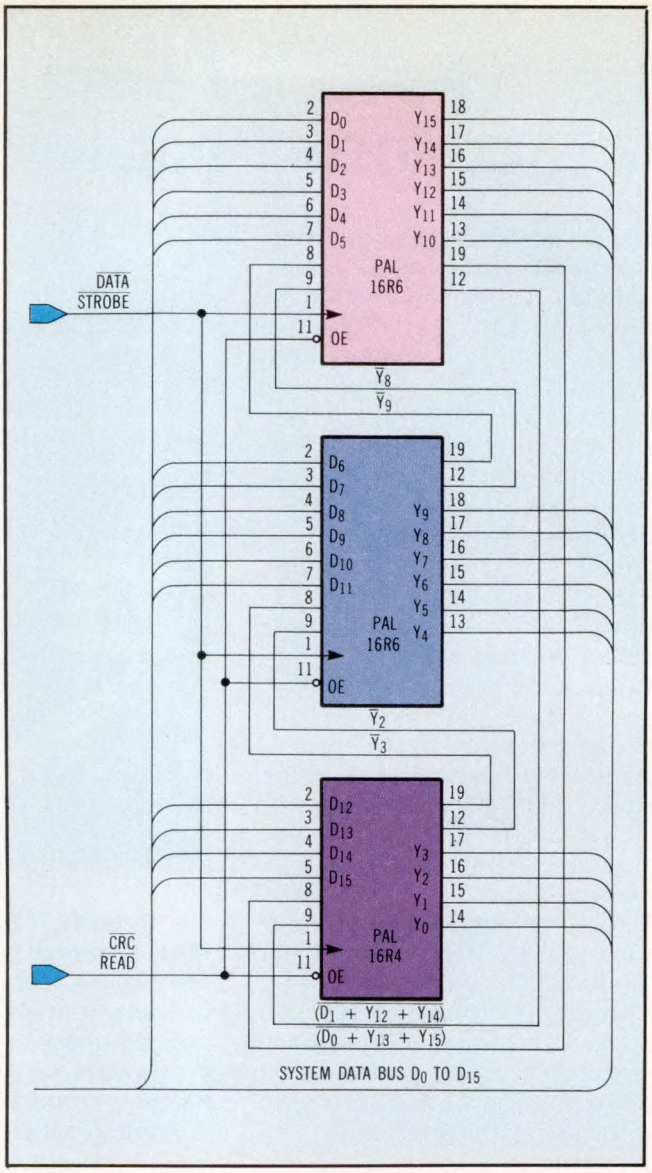
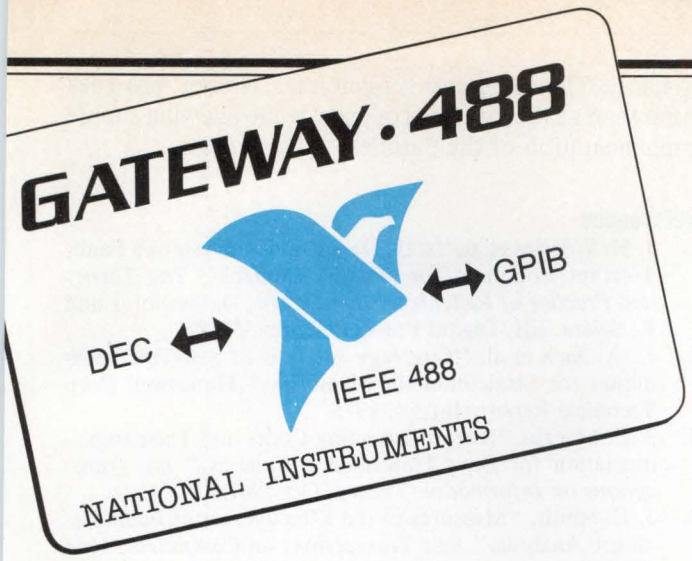


Fig 5 Parallel CRC generator circuit built using PLA devices. Each chip is responsible for part of the transition equations and requires external timing and control.

register is cleared prior to each data block calculation. Note that the value sent to the data bus is the inversion of the CRC register contents.

Fig 6 illustrates the operation of the parallel CRC generator of Fig 5. Values in Fig 6 are the same as those used in the previous serial CRC generator example. The three words of input data are 0001, 1020, and 1021 Hex. Assuming that the CRC register is initialized to zero, the intermediate results after each data strobe assertion are as shown in Fig 6. After the third data strobe, the parallel CRC register's contents agree with Fig 2's shift register after 48 clock cycles.

Of course, the parallel CRC generator can be used in non-fault-tolerant systems to provide error detection wherever high data integrity is required. It can also be used as a bus monitor to enhance the capability of diagnostics.[6] In this mode, the diagnostics invoke a set procedure within the system. The bus cycles resulting from this procedure can be accumulated in the CRC generator and then compared with a result known to be correct.



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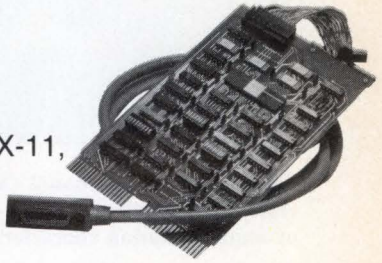

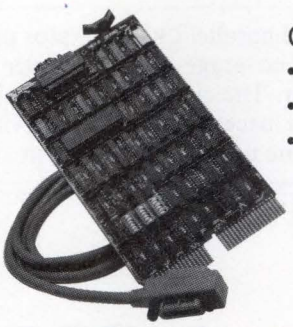

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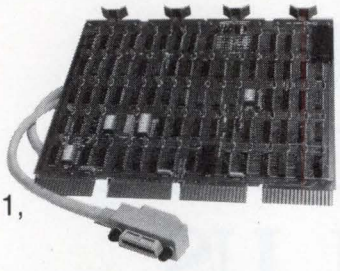

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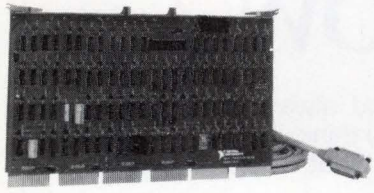

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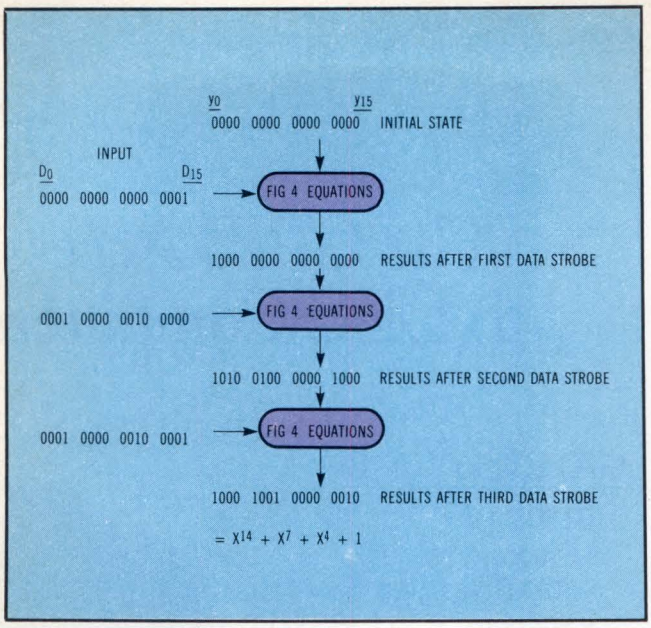

Fig 6 Parallel PLA based CRC generator operational steps. Data input at left yields the intermediate results shown. Ease of implementation characterizes the parallel approach.

For data compression, the parallel CRC generator provides more effective error coverage and is simpler to implement than a checksum. The circuit presented provides the hardware support necessary to help alleviate performance degradation due to software voting in SIFT systems. The generator polynomial chosen provides more than adequate error coverage while allowing simple implementation of the parallel CRC generator.

References

1. J. H. Wensley et al, "SIFT: Design and Analysis of a Fault-Tolerant Computer for Aircraft Control," *The Theory and Practice of Reliable System Design*, D. Siewiorek and R. Swarz, eds, Digital Press, 1982, pp 559-584.
2. L. A. Jack et al, "Coverage Analysis of Self-Test Techniques for Semiconductor Memories," Honeywell Corp Technical Report MR12399, 1975.
3. J. E. Meggitt, "Error Correcting Codes and Their Implementation for Data Transmission Systems," *IRE Transactions on Information Theory*, Oct 1961.
4. J. E. Smith, "Measures of the Effectiveness of Fault Signature Analysis," *IEEE Transactions on Computers*, June 1980.
5. J. Birkner and V. Coli, *PAL Handbook*, Monolithic Memories, 1982.
6. D. Bhavsar and R. Heckelman, "Self-Testing by Polynomial Division," *Proceedings of the IEEE Test Conference*, 1981.

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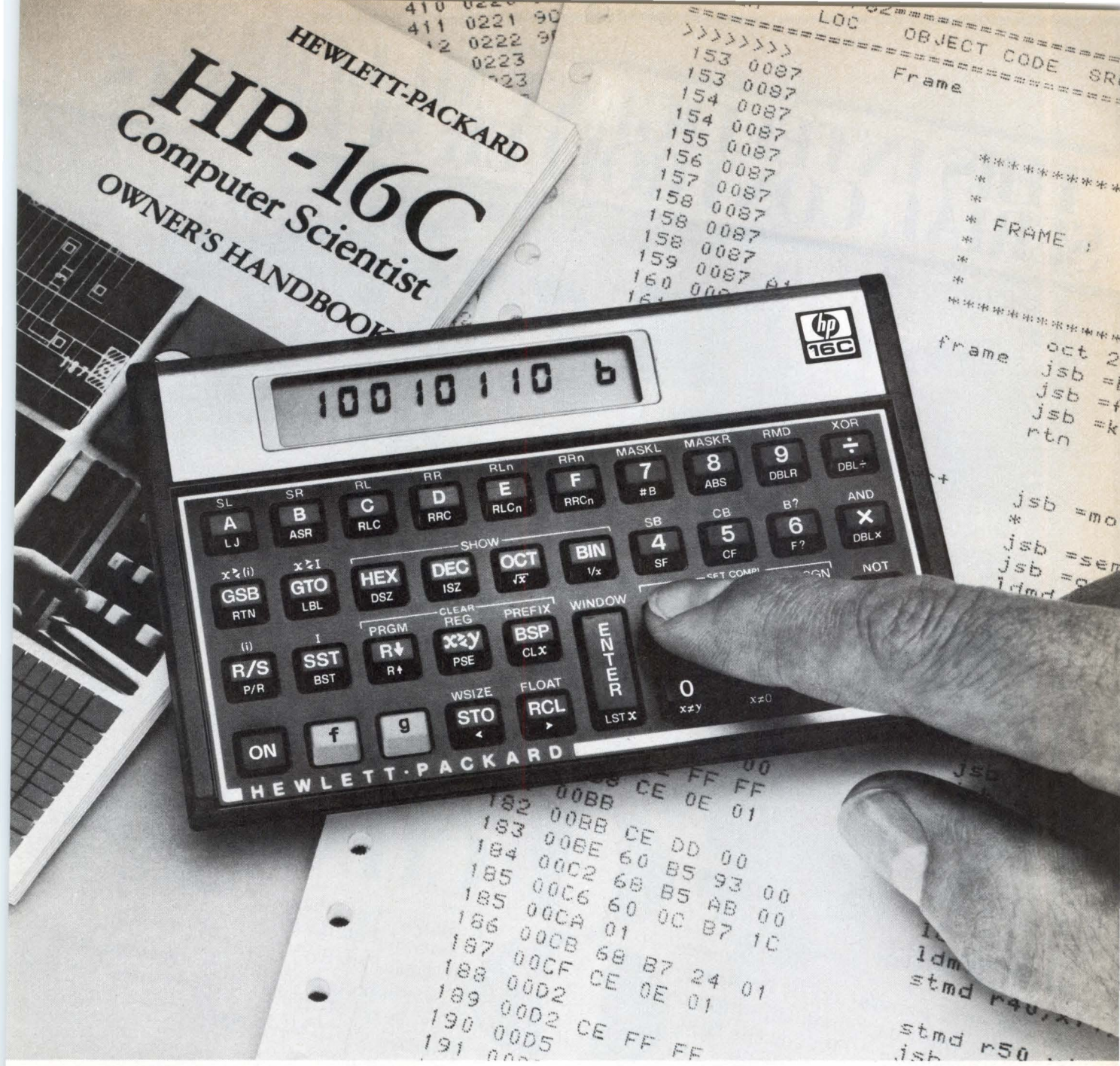

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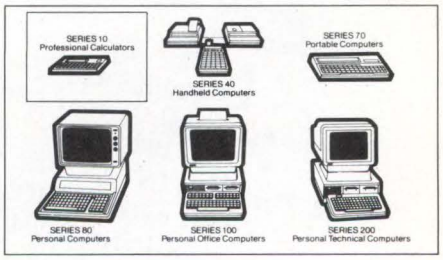

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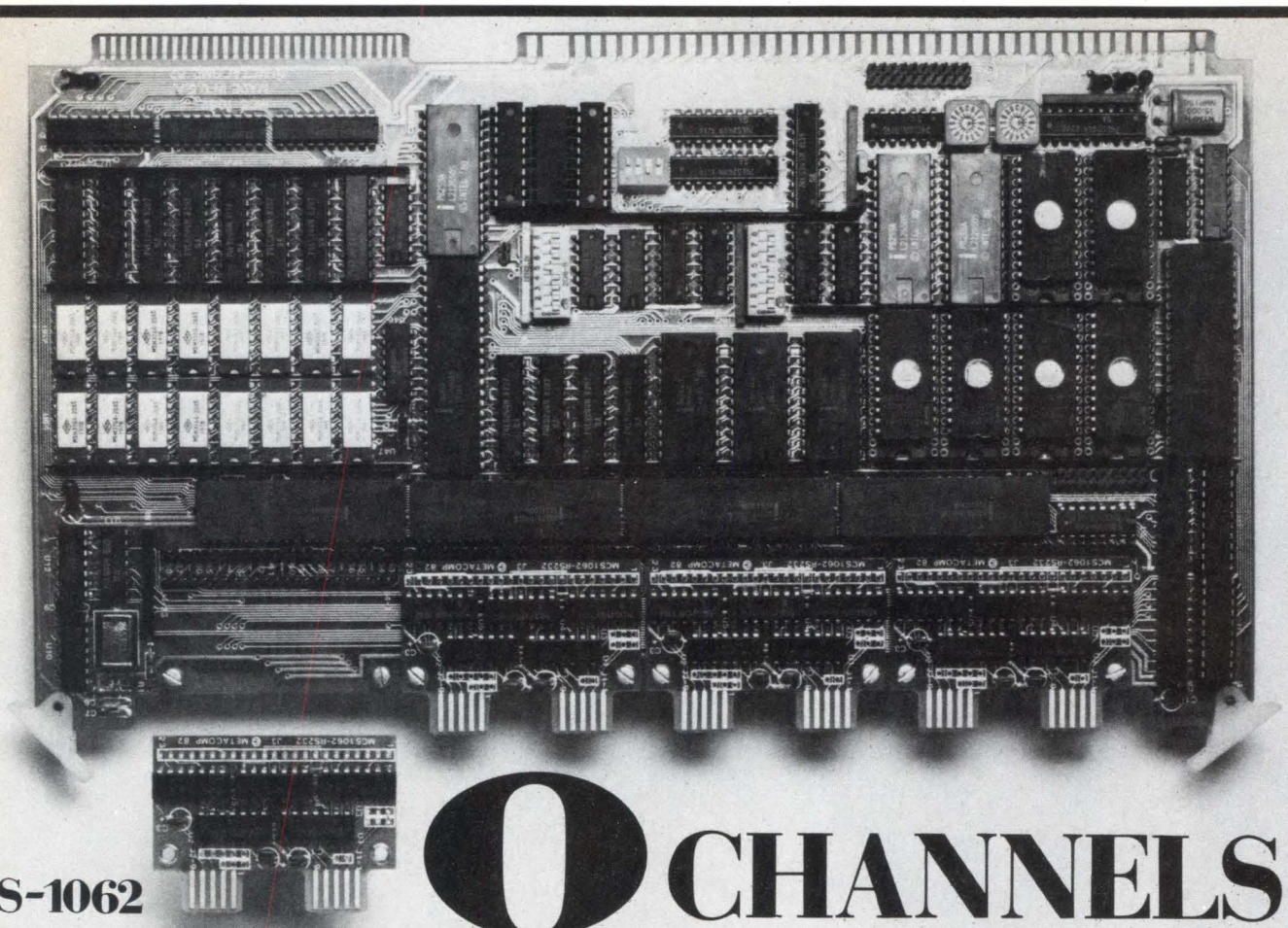

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BIT ORIENTED DATA LINK CONTROLS—PART II

The advent of VLSI chip sets serving specific data communication protocols like X.25 is resulting in more reliable and less expensive computer communication.

by Alan J. Weissberger

This is the second in a series of two articles on high data link controls.
(See Computer Design, *March, pp 195-206 for Part I.)*

Exception conditions occur as the result of busy situations, transmission errors, station malfunctions, and other operational problems. Fortunately, high level data link control attempts to recover from these situations before notifying the Network layer.

A busy condition occurs when a station temporarily cannot receive or continues to receive information (I) or unnumbered information (UI) frames due to internal constraints such as buffering limitations or processing bottlenecks. The busy condition is indicated by the transmission of an RNR frame containing the receive sequence number N(R) of the next expected I frame. Traffic pending transmission at the busy station can be transmitted prior to or following the RNR. The continued existence of a busy condition must be reported by retransmission of RNR at each poll/final (P/F) frame exchange.

When the internal constraint is eliminated, the busy condition is cleared at the station that transmitted the RNR. Clearing of the busy condition is reported to the remote station by transmission of any one of a variety of frames. A busy condition is also cleared when a primary station transmits an I frame with the P bit set to 1, or when a secondary/combined station transmits an I frame with the F bit set to 1. See Fig 1(a) for an example of busy condition establishment and clearing.

A frame received in error is simply discarded by the receiver without any further action. If the frame is an I frame, the error will either manifest itself later in the form of a send sequence number N(S) sequence error, be detected by means of timeout recovery or checkpoint P/F bit recovery.

N(S) sequence error and REJ recovery

An N(S) sequence exception occurs in the receiving station when an I frame that is received error free contains an N(S) sequence number that is not equal to the receive variable (R) at the receiving station. The receiving station does not acknowledge the frame causing the sequence error, or any I frames that may follow, until an I frame with the correct N(S) number is received. Unless sequence reject (SREJ) is to be used to recover from a given sequence error, the information field of all I frames received whose N(S) does not equal the receive variable (R) will be discarded.

The REJ command/response initiates a sequence error recovery earlier than is possible with checkpoint recovery. The REJ reports the sequence error and calls for retransmission of I frames starting with N(R) − 1. Fig 1(b) illustrates the use of REJ recovery. If a retransmitted I frame is again received in error, then the REJ recovery cannot be repeated due to possible ambiguities. The error situation must be resolved by either checkpoint or timeout recovery.

It is possible to receive a REJ that acknowledges all outstanding I frames; ie, the N(R) of the REJ frame equals the send variable S. This can occur if station A

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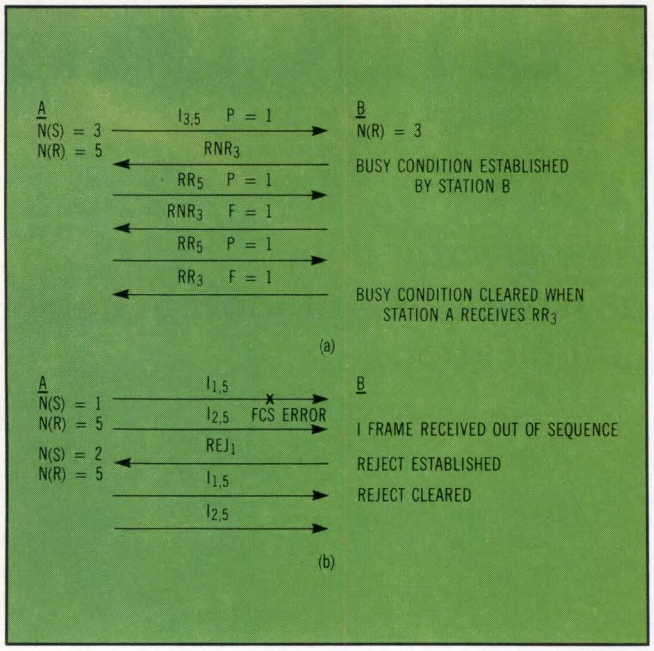

Fig 1 HDLC recovery from exception conditions can often be accomplished without notification of the Network layer. Busy condition exception (a) results in an RNR frame being sent and eventually cleared by a frame with P bit set to 1. Sequence error recovery (b) demands retransmission of the correct I frame. If the incorrect frame is sent, other recovery means must be attempted.

sends an RR, RNR, or I frame to acknowledge a received I frame and the frame sent was discarded due to a frame check sequence error. If station B had no I frames to send, a response timer would expire and the same I frame could be sent with P = 1 [this is particularly true in X.25 link access procedure (LAP) where there are no S commands]. In this event, station B (receiving REJ) should terminate timer recovery and proceed without retransmitting I frames.

A single I frame or the last I frame in a sequence of I frames cannot be recovered by REJ since no frames are received out of sequence. Also, a frame with the P bit set to 1 may be lost. To recover from such situations, high level data link control (HDLC) provides a timeout function. Use of the timeout differs in normal response mode (NRM) and asynchronous balanced mode (ABM) or asynchronous response mode (ARM).

In NRM, only the primary station has a timeout function. The timer is started upon transmission of a command with the P bit set to 1. It is restarted when an error-free frame with the F bit set to 0 is received, and stopped when an error-free frame with the F bit set to 1 is received. Upon expiration of the timer, it is recommended that the primary station query status with a supervisory frame.

In ABM or ARM, each station has a timeout function. The timer is started (provided it is not running already) every time an I frame or a frame with the P bit set to 1 is sent. It is restarted when a frame is received that acknowledges a not yet acknowledged I frame. The timer is stopped when no unacknowledged I frame is outstanding.

Checkpoint recovery is based on a checkpoint P/F bit cycle starting with the transmission of a frame with a P bit set to 1 by the primary/combined station and ending either with the receipt of a frame with an F bit set to 1 or when the response timer expires. For a secondary station, a checkpoint cycle begins with the transmission of a frame with the F bit set to 1 and ends with the receipt of a frame with a P bit set to 1.

If a primary station receives a frame with the F bit set to 1 during a checkpoint cycle, in NRM, it initiates retransmission of unacknowledged I frames. Sequence numbers will be less than or equal to the N(S) number of the last I frame transmitted.

In ABM, checkpoint retransmission is only initiated based on frames received with the F bit set to 1, to avoid possible interference with other recovery possibilities. HDLC ABM does not specify under which conditions the P bit has to be set. One strategy is to set the P bit only when it is necessary to query the status of the other station—for example, after the response timer has expired.

There are certain exception conditions that cannot be recovered by HDLC. The Network layer must be notified of these conditions and recovery should be attempted by the Network layer or operator intervention.

Retry or retransmission attempts are counted by the data link control (DLC) station, but after some planned number "n," correct station action is reported as unrecoverable at the data link layer. Those actions that should be retried include attempts to obtain acknowledgment of a set mode command such as SNRM or DISC, resume communications with a busy station, achieve initial online status at a secondary station, or initiate active communications at a secondary station. Other procedural errors requiring higher layer recovery include analysis and recovery from a rejected command specified in the information field of a frame reject (FRMR) response frame, recovery from wrong station identification specified in the information field of an XID response frame, dealing with I frames with information field length exceeding maximum length system specified parameter, and handling an incorrect or null information field in a TEST response when a TEST command with information field has previously been sent.

Role of LSI/VLSI

Large scale integration/very large scale integration (LSI/VLSI) circuits have greatly simplified HDLC hardware design, and standardized DLC input/output (I/O) driver firmware. In addition to the basic character assembly/disassembly functions of universal asynchronous receivers/transmitters and universal synchronous/asynchronous receivers/transmitters, modern chips support the HDLC type of bit oriented framing. Features such as flag/abort generation and detection, zero insertion/deletion, cyclic redundancy check/International Consultative Committee for Telephone and Telegraph (CRC)/(CCITT) V.41 generation/checking, and secondary and global address selected reception provide this support. By incorporating HDLC framing chips in terminals and computers, HDLC, synchronous data link control (SDLC), and X.25 hardware have become increasingly cost-effective.

Table 1 traces the history of LSI datacomm circuits. The trend has been to amalgamate many of the hardware functions necessary for one or two binary serial interface(s). Only in 1982/3 is there true intelligence, in the form of onchip firmware, incorporated into VLSI data communication chips.

Presently, there are three categories of HDLC type chips: bit oriented framing, multiprotocol framing, and X.25 link level. Bit oriented framing chips (Intel 8273, Motorola 6854, Western Digital 1933) transmit and receive HDLC frames with single-octet or extended address and control fields. Some chips also feature residual character handling, short frame rejection, IBM SDLC loop mode, nonreturn to zero inverted (NRZI) encoding/decoding, and a digital phase locked loop for receive clock recovery.

Residual character handling provides the means to send and receive characters that do not match the programmed character length. For example, if an integral number of octets are required in a frame, using 6- or 7-bit characters, the information field will have to be padded if the number of bytes (n) is not a multiple of 8. This requires transmission and reception of a residual (short-bit) character. Residual character detection can also determine if received frames are octet aligned. If not, recovery at a higher layer may be required. The CCITT X.25 packet layer is currently being revised to handle a nonoctet aligned information field.

Short frame rejection is the ability to disregard received frames that have not completed their address and control fields. With a 16-bit CRC and single-octet address and control fields, the minimum frame length is 32 bits. There is a 40-bit minimum frame length with extended control; with extended address and control, it is 40 bits plus 8(m − 1), where m is the number of address octets. Most HDLC chips merely discard frames less than 32 bits, but some, like Signetics' 68562 and Rockwell's 68561 multiprotocol chips, perform rejection of all short frames.

IBM SDLC loop mode support includes repeating received data onto transmit data and the ability to change the GO AHEAD (01111111) bit pattern into an opening flag, which is then followed by the frame to be transmitted. NRZI coding complements the line state whenever a binary 0 is encountered in the data stream. HDLC zero insertion guarantees a 0 after, at most, five 1s. In turn, this ensures a line transition within 6-bit times. These line transitions make it possible to use a digital phase locked loop for clock recovery. Without guaranteed transitions in the data, a phased locked loop would drift, and bit synchronization would be lost. In addition, the phased locked loop permits HDLC equipment to be directly interconnected, or asynchronous modems to be used.

Multiprotocol framing chips handle byte oriented and sometimes asynchronous formatted data, as well as bit oriented framing. The Signetics 2652, SMC 5025, Fairchild 3846/6856, and TI 9903 support one synchronous serial receive and transmit channel. The Rockwell 68561 can handle one synchronous or asynchronous channel while the Zilog Z80-SIO, Z-SCC/SCC, NEC 7201, Intel 8274, and Signetics 68562 support two asynchronous/synchronous serial communication channels. The Z-SCC/SCC is the most advanced chip in this category. In addition to the features previously described, it includes a bit rate generator; digital phase locked loop; choice of nonreturn to zero, NRZI, frequency modulator FM0, FM1, or Manchester encoding/decoding; IBM SDLC mode; local loopback; and automatic echoplex operation. Table 2 highlights the features of the more advanced dual-channel multiprotocol chips.

TABLE 1

LSI Datacomm Circuit Evolution

Chronology	Device
1971	UART
	Bit rate generator
1974	USART
1977	Bit oriented receiver/transmitter
	Multiprotocol receiver/transmitter
	USART and BRG
1978	Dual-channel multiprotocol receiver/transmitter
	DES encryption
	Manchester encoder/decoder
1980	Polynomial generator/checker
1981	Advanced dual-channel multiprotocol receiver/transmitter
	32-bit CRC generator/checker
	IBM 3270 coax A receiver/transmitter
1982	X.25 link level controller
	Token bus LAN controller
1983	SDLC/X.25 link level controller
	Ethernet LAN controller
	Token ring LAN chip set

Multiprotocol chips permit a data communication system to support both character controlled and bit oriented DLCs within the same equipment. For example, a multiplexer or concentrator might service asynchronous or character controlled DLCs on its low speed terminal lines and bit oriented DLCs on it backbone (long haul) lines. Thus, economies of scale may be realized by using a single integrated circuit in different products. The advantages include volume purchasing, single part qualification, simplified incoming inspection, and reduced inventories.

Prevention of hardware obsolescence is another important advantage of a multiprotocol chip. When a new DLC procedure is supported, the same printed circuit board can be used and the DLC chip reprogrammed. This has enabled equipment designed for binary synchronous communication to later support SDLC and X.25 equipment.

A multiprotocol chip can also accommodate an X.21 circuit switched interface. CCITT X.21 requires a character controlled DLC during call establishment and a mutually agreed upon DLC (usually HDLC) during information transfer phase. This is facilitated by changing the chip's protocol from character controlled to bit oriented once the call establishment phase is complete.

The link control type of HDLC chip incorporates firmware as well as hardware functions. In addition to line framing and formatting, the procedural elements that

control link operation are implemented in microcode within these chips. Examples of link control functions include link setup, reset, and disconnect; acknowledging commands and I frames; setting and clearing of busy conditions; timeout controls; and retransmission of unacknowledged commands and out of sequence I frames. Link control chips contain a direct memory access (DMA) controller that is used to access control blocks, setup parameters, and buffer tables located in an external random access memory that is shared with the host microprocessor. A memory management scheme and an interrupt control procedure facilitate interprocessor communications.

Western Digital 2501 and 2511 link controllers support X.25 LAP and link access procedure balanced (LAPB), respectively. The Fairchild F16425, although not yet available, promises to support SDLC as well as X.25 LAPB in a single chip. In both cases, the host microprocessor, relieved of all DLC responsibilities, reduces software/firmware development time and cost, and improves system throughput through parallel processing. For example, X.25 packet level code could be executed on the microprocessor concurrently with X.25 link level processing within the link control chip.

Recently, link control chips for local area networks (LANs) have been announced. These include the Western Digital 2840 and SMC 9026 token bus controllers, the Intel 82526, AMD-MOSTEK 7990, SEEQ 8001, Fujitsu Ungermann-Bass LAN-1 and 2, and Rockwell 68802 Ethernet controllers. Texas Instruments' token ring chip set for the IBM LAN is also included. These chips do not implement HDLC. Instead, they contain microcode for media access control, which is a sublayer of the Open Systems Interconnection (OSI) Data Link layer as defined by the IEEE

TABLE 2

Dual-Channel Serial Communication Controller Features

Parameter	Zilog Z80-SIO	NEC 7201/ Intel 8274	Zilog 8030	Zilog 8530	Signetics
Introduction date	1977	1981	1981	1981	1983
Max data rate	800k	800k	1M	1M	1M
Package pins	40	40	40	40	4048
Address and data muxed	No	No	Yes	No	No
Register addressing	Pointer	Pointer	Direct	Pointer	Direct
Interrupt vector compatibility	Z80	8086/8088 8080/8085	Z8000	8086/8088 8080/8085/Z80	68000 8086
Internal interrupt priorities	Fixed	1-bit	Fixed	Fixed	Fixed
DMA request/ acknowledge pins	2/0	4/1	4/0	4/0	4/4
DMA implementation	Z80-DMA	Extended daisy chain logic plus 8237	Z8016	8237/Z80-DMA	8237/68450
Counter/timers	None	None	Two	Two	Two
Bit rate generators (BRG)	None	None	Two	Two	Four
Crystal or transistor-transistor logic inputs to BRG	None	None	Two	Two	One
Local loopback	No	No	Yes	—	Yes
Auto echo	No	No	Sync/async	—	Sync/async
TDRD coding options besides NRZ	None	None	NRZI, biphase (FM) Manchester encoded data	—	NRZI, biphase (FM) Manchester encoded data
Digital phase locked loop	No	No	Yes	—	Yes
SDLC loop mode	No	No	Yes	—	Yes
Bit oriented procedures					
Secondary address comparison	Yes	Yes	Yes	Yes	Yes
All parties address recognition	Yes	Yes	Yes	Yes	Yes
Partial SA byte comparison	No	No	Yes	Yes	Yes
Underrun line fill options besides FCS-flag	None	None	Abort	Abort	Abort Abort-flags

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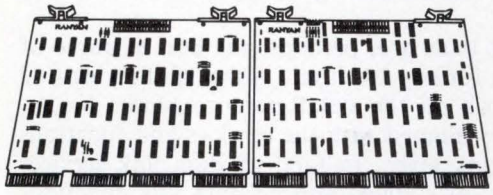
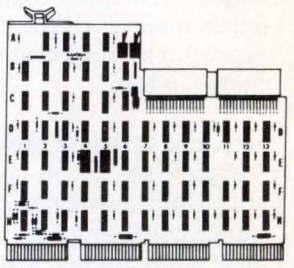


Peripheral Processor Link PPL-1



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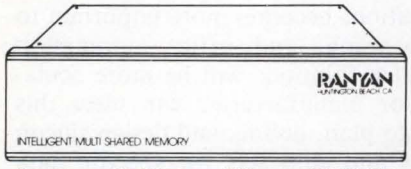

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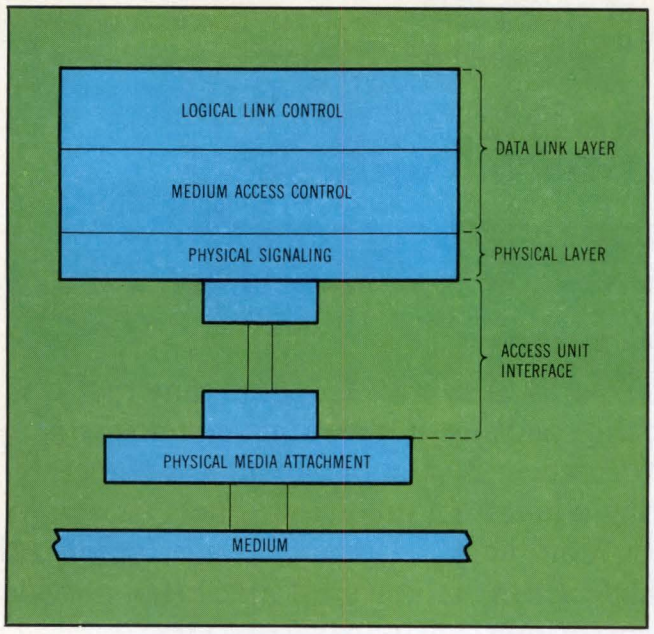


Fig 2 Link control interrelationships, shown in the reference model for OSI/IEEE 802 LAN plan, are served by the new generation of VLSI chips. These result in microcoded protocols and transparent layer interfaces.

802 LAN standards committee. Logical link control, the upper sublayer of the data link layer, is the host microprocessor's responsibility. This interrelationship is shown in Fig 2.

Future of VLSI data communication controllers

Software on silicon controller chips, such as the X.25, SDLC, and LAN chips just discussed, contain I/O firmware as well as hardware functions. The advantages of these chips are many and extend to both the equipment manufacturer and the end user. Software development efforts and associated costs are reduced by the new chips. Because the product design cycle is shorter, new products get to the market faster. Also, increased functional density of VLSI and exhaustive testing (by many customers) of the onchip software improve reliability. The modular structure and predefined software interface facilitate the incremental addition of processing power without needing reentrant or redundant code in the microprocessor. Furthermore, adding processing power will not degrade system throughput nearly as much as if the code were resident in the host microprocessor. Finally, complex protocols such as X.25, SDLC, Ethernet, or token passing are transparent to the system integrator and the end user. This decreases the amount of training required.

To complement software on silicon chips, standardized higher layer protocols could be marketed as solid state software. These protocols, implemented as programs in read only memory, can be executed by a host microprocessor. Examples include the CCITT X.25 packet procedures and IBM Systems Network Architecture path control, transmission control, and data flow control. The European Computer Manufacturers Association (ECMA), National Bureau of Standards, and International Standards Organization (ISO) transport and session protocols; and the file transfer, remote job entry, and virtual terminal protocols being developed by the American National Standards Institute and ISO are other examples of potential solid state software routines.

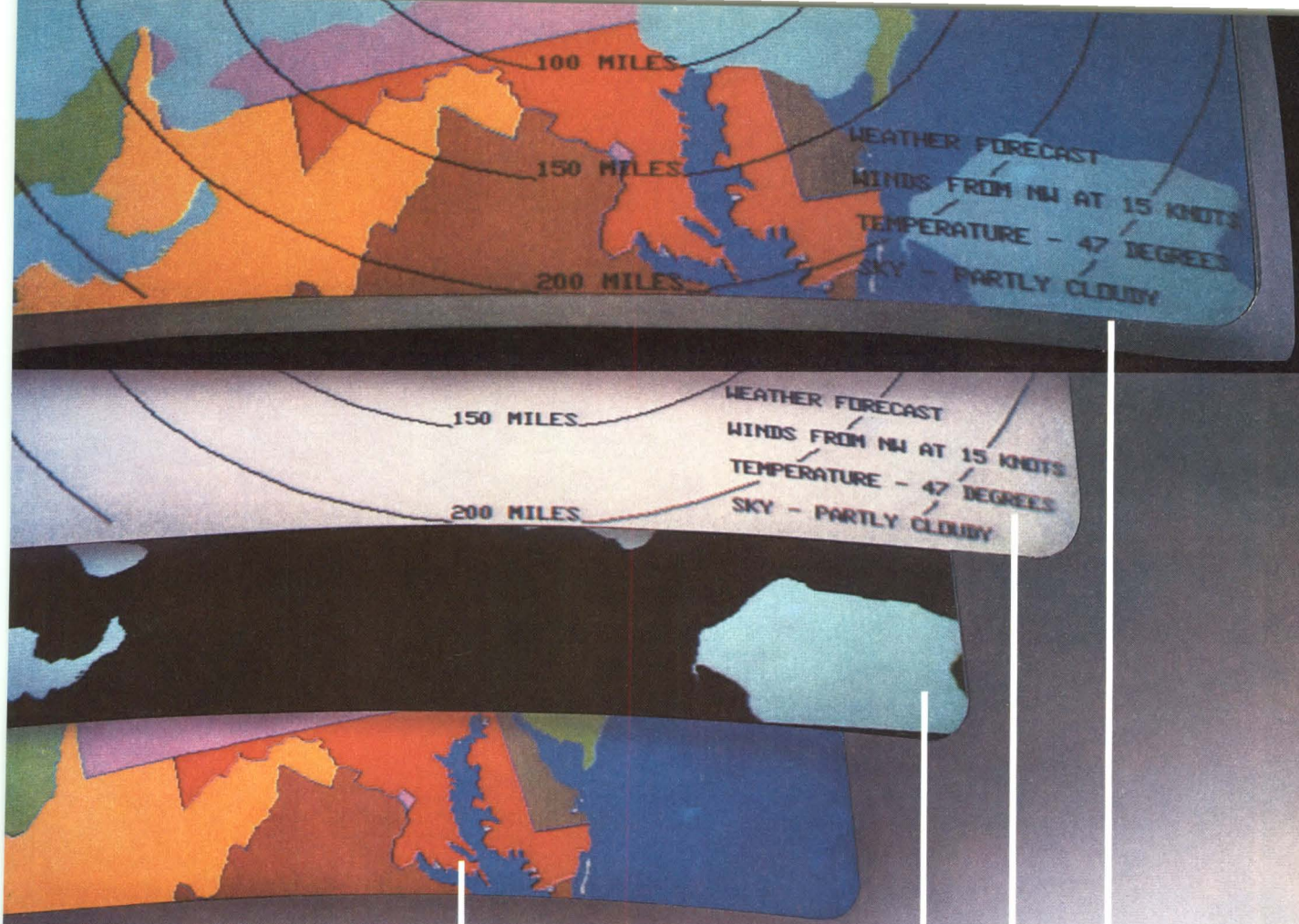
An appropriate shared memory interface to a link level controller chip would be standardized by the chip vendor. This interface would incorporate control blocks for initialization parameters; data link and higher layer status; retry counts; and setup, disconnect, and reset commands. Memory management and DMA control would be handled by the software on silicon chip while the microprocessor executed the solid state software.

Chip sets, put together by VLSI manufacturers, would make implementation of an X.25 terminal or LAN office product much simpler, more cost-effective, and more reliable (see Fig 3). These chip sets would also facilitate mixed vendor communications over a common transport medium—the ultimate goal of the ISO/OSI Reference Model.

Bit oriented DLCs are, perhaps, the best example of peer protocols for any OSI layer. Although they existed before the work on the OSI/Reference Model began, they are closely aligned with the services and functions in the Data Link layer. In fact, all data link services (except quality of service) and all data link functions (except data circuit chaining) are accommodated in contemporary bit oriented DLCs. Also, LSI and VLSI chips have simplified implementation of bit oriented DLCs in equipment designed for local area and wide area networks.

This is a clear example of what can be done within the context of OSI. Hopefully, the same degree of functionality for the high layer peer protocols now being developed by ISO, ECMA, and CCITT will be forthcoming. If these higher layer protocols find support within the end-user community, a huge market for packaged VLSI solutions will emerge.

As data communications becomes more important to computer, data processing, and office automation users, the need for VLSI solutions will be more acute. Today, microprocessor manufacturers can meet this challenge by starting to plan, define, and design silicon software components and chip sets for specific data communication applications.



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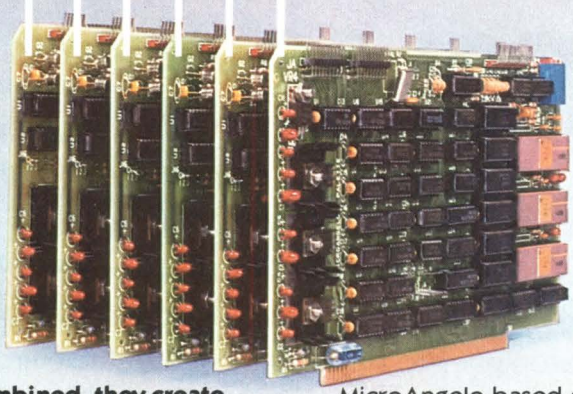

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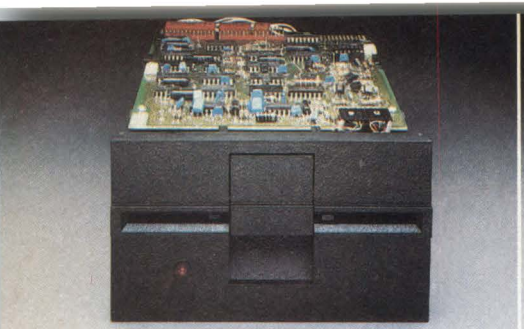

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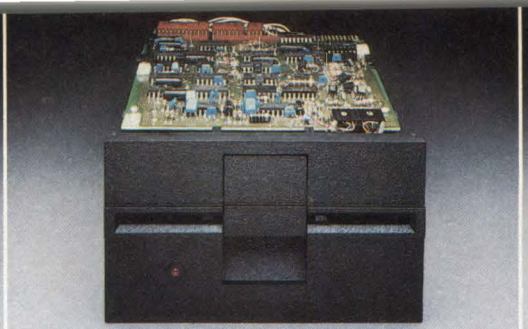

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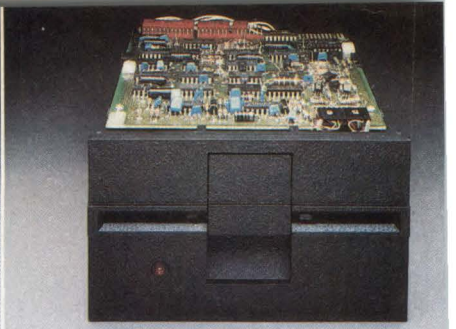

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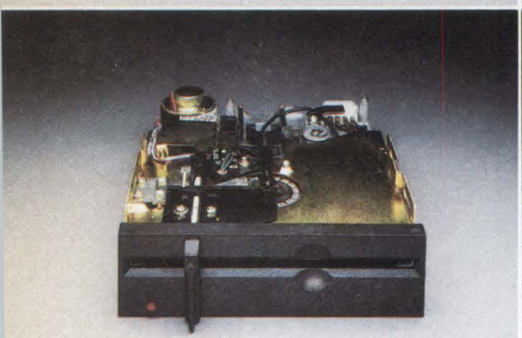

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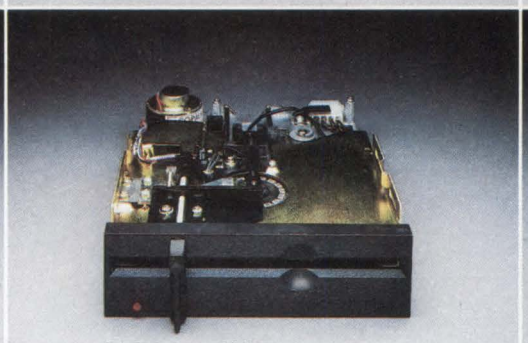

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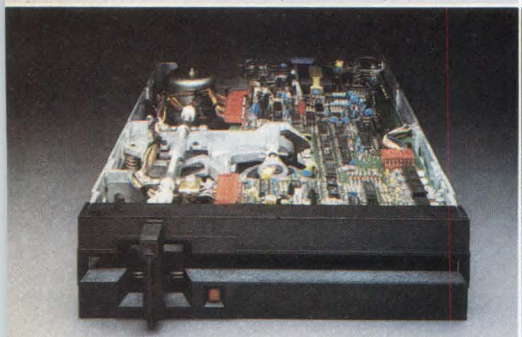

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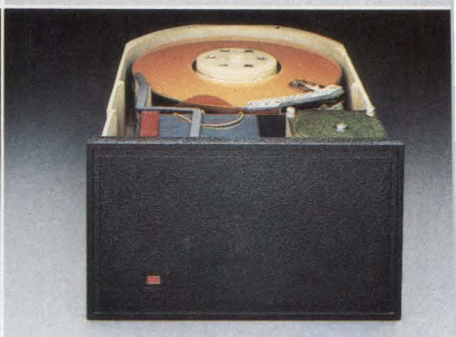

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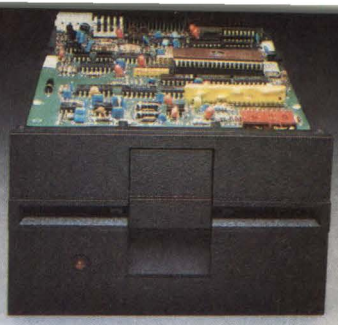

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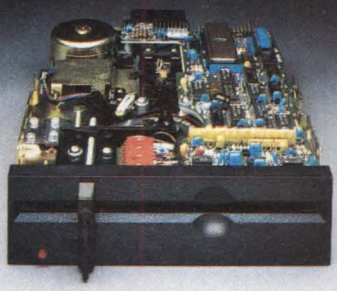

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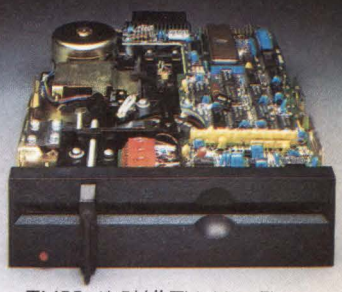

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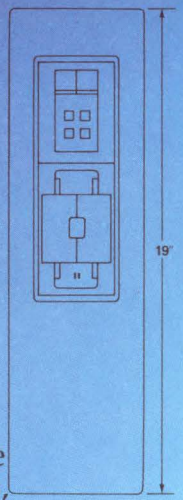

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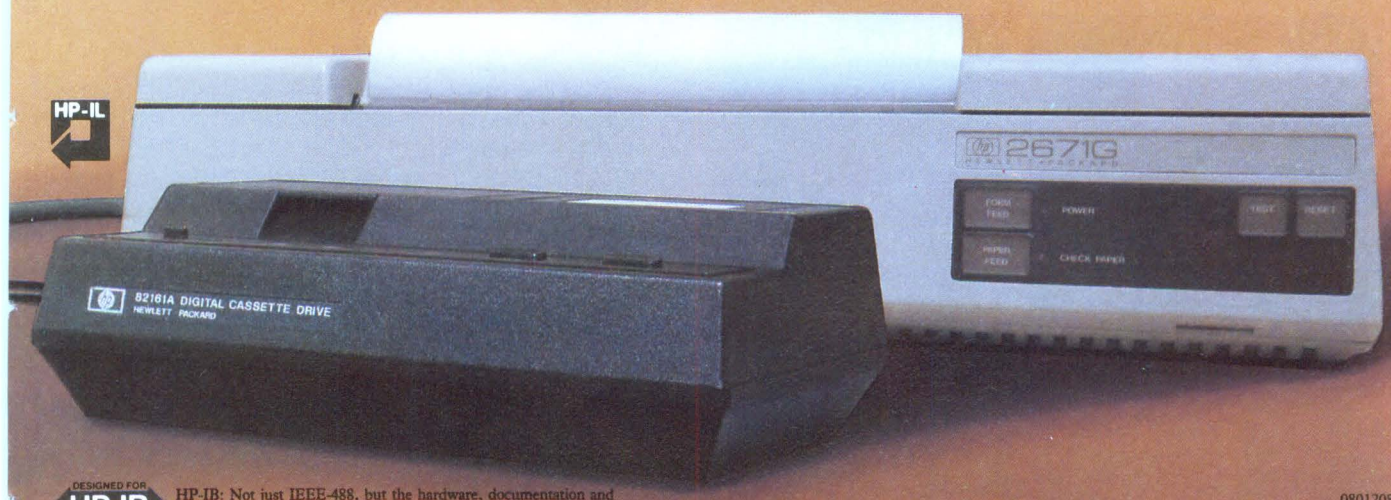
CIRCLE 82



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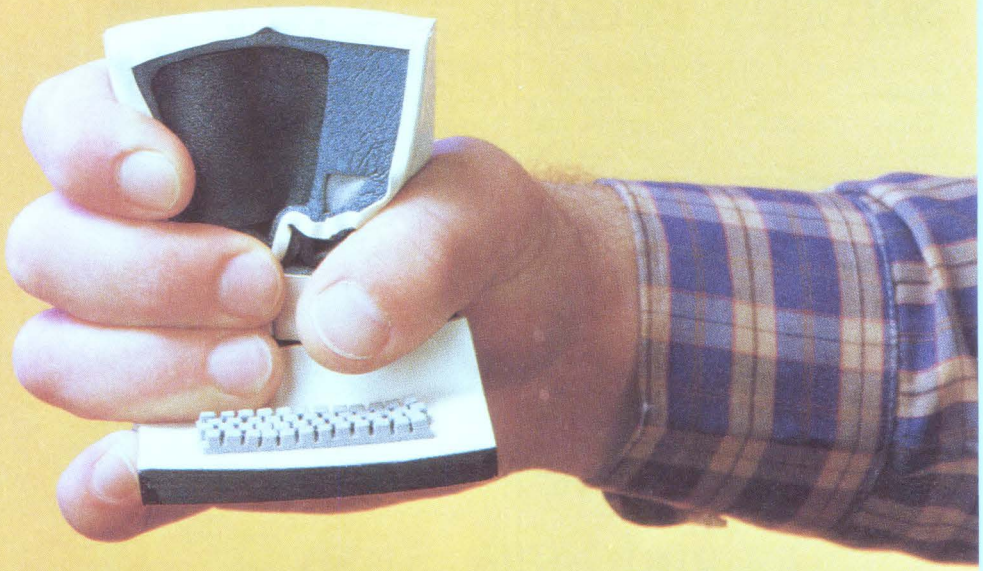

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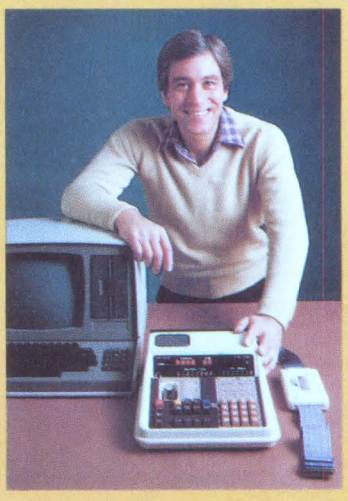

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CIRCLE 83

SPECIAL REPORT ON

SYSTEMS DEVELOPMENT AND TESTING

As a result of the ever-increasing use and complexity of microprocessors, the functional density of most digital equipment is at a point where development and testing at the logic gate level play a minor role in system design. Design efforts today require joint hardware and software teams working in terms of higher level languages and functions.

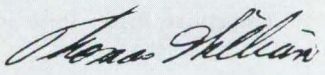
This hardware/software nature puts a two-fold burden on team members and their instrumentation. First, hardware designers need specialized instrumentation such as logic analyzers, waveform digitizers, and traditional-type instruments that still allow the hardware technician to find, isolate, and examine a suspected fault in detail. Software designers have similar needs. High level languages on development systems must still allow the programmer easy access to generated code.

Second, and most difficult, hardware and software designers must communicate with each other beyond the integration stage. Thus, it is insufficient for hardware instrumentation and software to be mutually exclusive. Rather, software must be correlated with hardware at a high level.

While communication among all levels of test and development is vital, managing information—that most precious commodity—is becoming paramount. Communication and information management needs feed one another. Moreover, software development systems and hardware instrumentation are becoming linked in LANs to share resources. Therefore, smooth flow, organization, and version control are essential for coordinating design team efforts.

Logic analyzers represent an active instrumentation area. Issues affecting the newer logic analyzers' design, and the incorporated features, distill issues impacting overall digital design. Based on microprocessors themselves, logic analyzers are being applied to microprocessor based systems. They have both the need and the capability to look at and correlate events in hardware and software. The complexity of their applications demands that logic analyzers be easy to set up and use, and that they enable users to rapidly find and interpret necessary data. Because they stand between lower level hardware instrumentation and higher level software, they can bear a great part of the communications and compatibility burden.

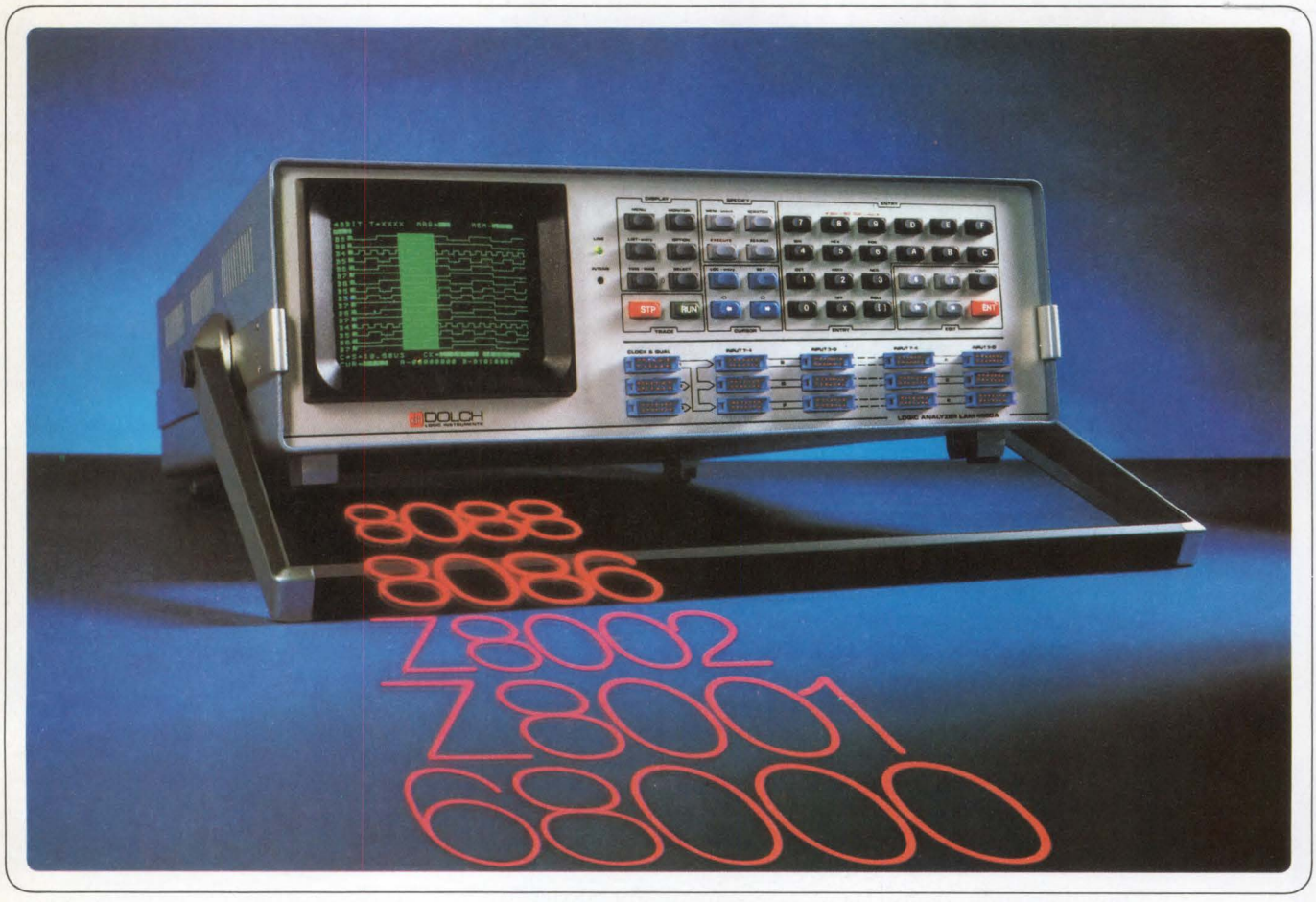
Communication functionality and compatibility impact two vital measures of productivity—design time and cost. The modern development and test operation will combine hardware and software tools. Incorporated in this will be standalone capabilities suited to team members' individual functions, as well as instruments such as development systems with integrated logic analyzers, and large multi-user systems for high level software development.



Thomas Williams
West Coast Managing Editor

Dolch.

advanced logic analysis



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Friendly, yet powerful, personality

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Plus Some Powerful Pluses

300 MHz Sampling: Besides having 48 channels, for state or timing analysis, you can overlay 16 more at 300 MHz. The 3.3 ns resolution lets you spot short glitches and resolve critical timing sequences.

Advanced Triggering: Multi-level, multi-function triggering gets you to your data — and analysis — quickly.

Area Tracing: You can limit data tracing to specific areas of interest in your system's memory — there's no need to record unwanted data.

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For more reasons why the 4850A is ideal for 16 bit (and 8 bit!) microprocessors see a demonstration. Call (800) 538-7506; in California, (408) 998-5730. Or write: 230 Devcon Drive, San Jose, CA 95112.

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LOGIC INSTRUMENTS

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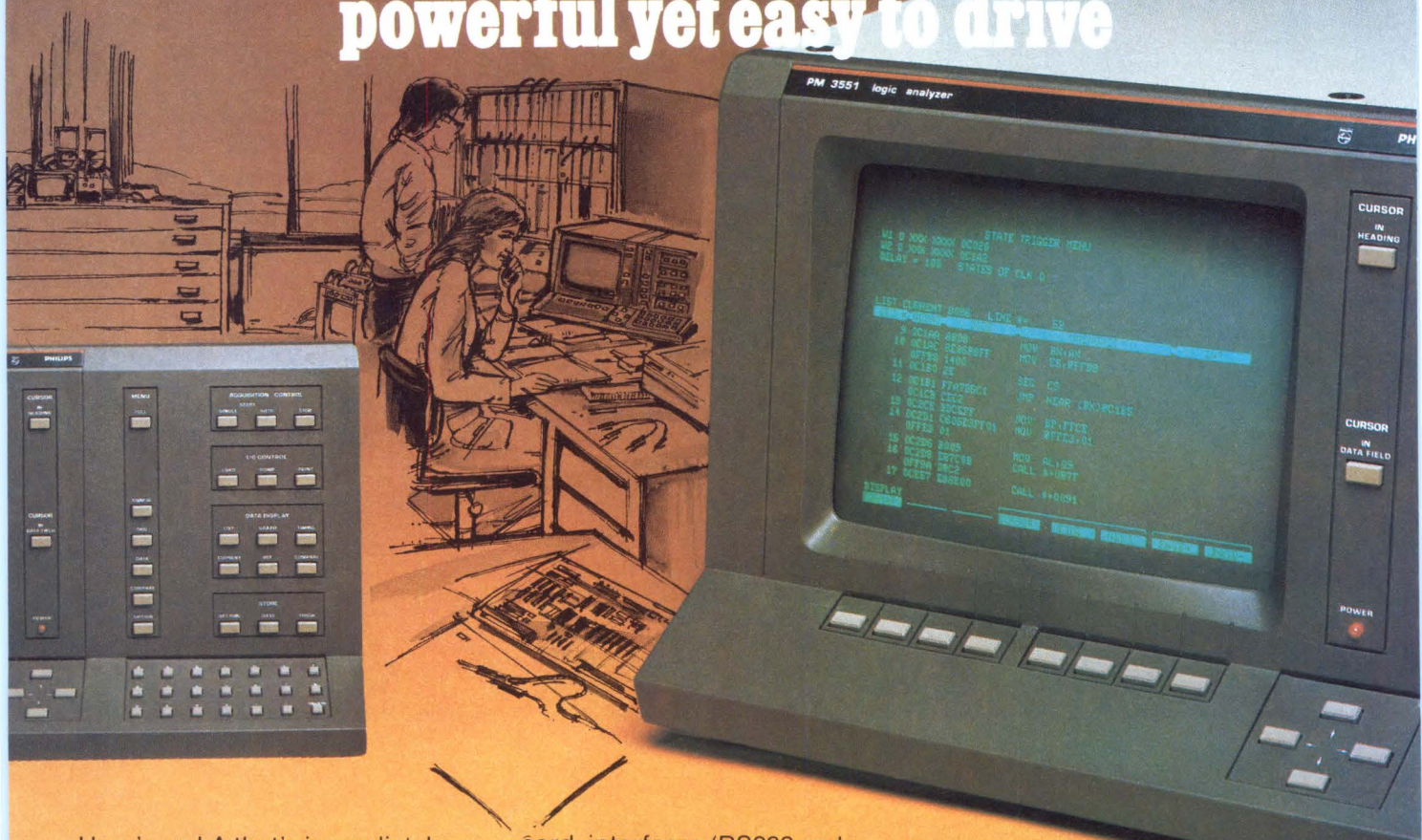

Here's an LA that's immediately understandable... the PM 3551 from Philips. Cursor prompting and soft-key entry give you intelligence at your fingertips. You can exploit the power of more than 250 functions the very first time you switch on, because all functions are clearly labelled above the softkeys. You can therefore setup in seconds, without reference to the manual.

Expandable operation. You can start, for example, with a 35-channel model which will comfortably handle 8- and 16-bit multiplexed processors. As and when you need to handle minis and 16-bit non-multiplexed processors you can make a simple expansion to 59 channels. Other performance options include a 300 MHz timing card, interfaces (RS232 and IEEE 488) plus disassemblers.

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CIRCLE 86

LOGIC ANALYZERS RISE TO THE CHALLENGE OF MICROPROCESSORS

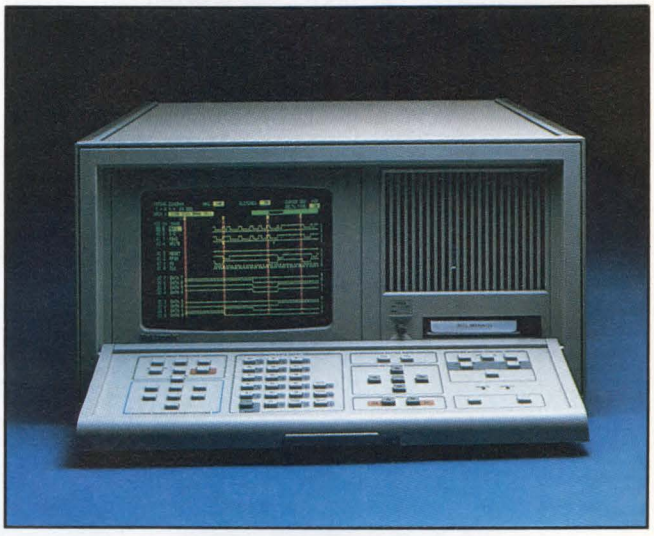
In the total picture of cost and efficiency for a design operation, the advanced logic analyzer assumes vital importance by aiding both hardware and software development.

by Tom Williams,
West Coast Managing Editor

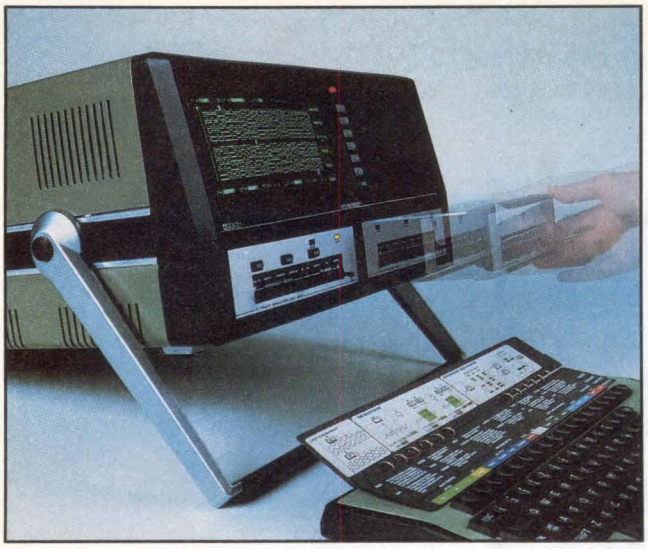
Tracking the ever increasing complexity of microprocessor based digital circuits, the logic analyzer is evolving toward a versatile, cost-effective, and relatively easy to use instrument that will fit efficiently into the overall design and engineering operation. While logic analyzers do not perform analysis, they store data produced by logic circuits that the human operator must manipulate and interpret. Thus, a logic analyzer's effectiveness as an analysis tool can be measured by its effectiveness in capturing data of interest, and then processing and manipulating that data to be presented in a variety of meaningful ways. The analyzer's effectiveness can also be measured by how easily the operator can set up and use the instrument.

Additionally, logic analyzers are finding their place in the overall design process of advanced hardware/software systems, most of which incorporate microprocessors. This role imposes the need for flexibility and modularity on the instruments. It also requires that they communicate and work smoothly with other instruments, as well as with computers that can be used to oversee the design and debugging operation. Since today's logic analyzers are microprocessor based, they possess the microprocessor's adaptability. The ability to work in concert with development systems and other instruments will be vital in the total design effort.

Digital design task requirements have forced the logic analyzer to have standalone, single user capability, and a price considerably below that of a full-blown microprocessor development system. At the same time, however, the logic analyzer must have some of the characteristics usually associated with the development system, such as access to the processor and mnemonics capability. The logic analyzer must allow the user to look from his level of analysis of hardware and software, and see what is happening at a higher level in software.



The DAS 9120 series color logic analyzer from Tektronix. The first logic analyzer to utilize color in the display to highlight information, the 9120 includes a tape cassette to store setup parameters, and multiple clocks to capture synchronous and asynchronous data.



The Dolch Atlas 9600 system can accept 2 plug-in preprocessors in its mainframe and control 12 others, be they logic analyzer, trace, emulation, or word generation modules. The flip chart on the keyboard relates soft key definition to the various modules.

With the increasing feature density of designs, both hardware and software design are reaching past the integration phase—where the twain have traditionally met—and are borrowing information from each other for use in their own tasks. Thus, the hardware end wants to know how to most efficiently implement the functions called for by software, and the software end wants to know what effects its microprocessor programs are having on the logic circuits they control.

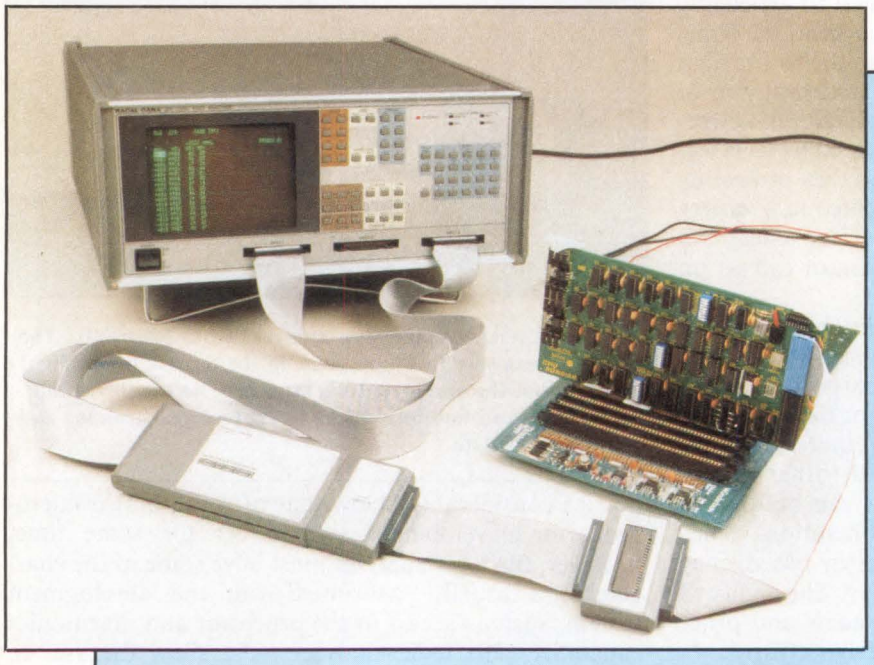
In the days of 4- and 8-bit processors, it made sense to write and debug programs in assembly language on a development system that used in-circuit emulation in the debugging stage. A logic analyzer was then used—perhaps with a link to the microprocessor—to test and debug the hardware. Today's 16-bit microprocessors are simply too complex for that. Often, a software design team writes programs on a multi-user minicomputer in a high level language such as Pascal. They are then cross-compiled into the processor's native code and downloaded to a development system for emulation, debug, and integration.

As a standalone instrument, the logic analyzer must fit into this process. In a development lab, one or two workstations may be full-blown development systems with logic analyzers integrated into them, but the expense of such systems makes it impractical for every design team member to have one. The logic analyzer must fit between the development system and lower level hardware instrumentation (eg, oscilloscopes, digital multimeters, and waveform digitizers).

Capturing data

A logic analyzer's first task is to efficiently acquire and store the data of interest for the specific problem the user is trying to solve. Gone are the days of "faster, wider, and deeper" when the instrument was merely expected to quickly grab as much data as it could from as many channels as possible. The size of today's programs makes selectivity a key feature of a logic analysis tool.

Since most advanced microprocessors run at less than 20 MHz, a sampling rate five or ten times that is usually adequate. Some analyzers do provide special high speed channels for asynchronous clocking such as the K500-D from Gould, Inc's Instrument Div (Santa Clara, Calif), which has eight channels that clock at 500 MHz, and the DAS 9100 from Tektronix, Inc (Beaverton, Ore), which has two 660-MHz channels. Similarly, memory depth is generally sufficient at 1024 bits per channel, but some analyzers, such as the KLA series from Kontron Electronics Inc (Redwood City, Calif), provide an expansion option up to 2048 bits per channel. All modern analyzers prefer to rely on selectivity rather than raw memory depth.



The Series 200 logic analyzer from Racal-Dana. The microprocessor pod allows the analyzer to handle 8-bit processors. A family adapter then reads the specific pins of the chip, which are interpreted and disassembled by ROMs in the instrument.

The Kontron Logic Analyzer/ Slave Emulator (LASER) has combined the KLA 64 logic analyzer with a development system and emulation. The front panel keyboard on the analyzer folds down to reveal up to 1.2M bytes of floppy disk storage.

The need for input flexibility is a well recognized, expanding area. In addition to 48 data inputs, the K101-D from Gould's Instrument Div features 12 external clock inputs: 6 are sample edge-sensitive clocks and 6 are level-sensitive latch enable clocks. Latch enable clocks can be used in a DEMUX input mode to gather and correlate data that occur at different times, and then to display the data as a single 24-bit word. This word is obtained from an 8-bit multiplexed bus, using only 16 probes, and contains 16 bits of low and high order address information, plus 8 bits of data.

Gould's newest member of the K100-D line, the K105-D, can be set up with 32 or 64 main (20-MHz) state and timing sample inputs, 8 or 16 high speed (100-MHz) inputs, and up to 8 external clock inputs that can be combined into 4 Boolean expressions. As well as defining specific word patterns and system operation segments for recording and analysis, these inputs can be linked with the microprocessor disassemblers to analyze memoric flow, and with high speed events elsewhere in the target system.

Triggering is a selection method that has developed an increasing number of variations. The ability to trace a given event or trigger word is a natural development of triggering capability. To conserve memory, and not waste time on nonevents, a number of instruments trigger on signal transitions only. This gives a compact recording of state conditions, showing only those program lines or addresses where something occurred. In the timing analysis mode, however, analyzers like the Kontron KLA series and the PM 3551 from Philips Test & Measuring Instruments, Inc (Mahwah, NJ) do count the clock cycles so that they can accurately reconstruct timing waveforms by inserting clock cycles on the display.

Once trigger capability has been established, however, it is desirable to trigger on a large number of possible conditions including a sequence of events, the occurrence of a given address or input/output (I/O) port, a break in a defined sequence of events, a given set of clock conditions, or even higher level software symptoms. Logic analyzer manufacturers are racing to incorporate what they deem to be the most useful combinations of triggering features.

Sequences of events, or trigger levels, are usually available to define relatively complex qualifications for initiating data acquisition. The Philips PM 3551 includes a "trigger on sequence break" feature that allows the user to define a loop such that the analyzer will trigger when the program does not successfully complete the loop. In a technique that combines triggering and tracing, the same instrument allows selective data acquisition. Each successive occurrence of the trigger will cause capture of a number of following samples. This allows rapid overview of branch addresses, for example, and where they lead in the program flow.

In addition to capturing data initiated by a given trigger event, it is often desirable to examine what happened immediately prior to that event, especially if the trigger is an error condition under investigation. The Series 200 analyzers from Racal-Dana (Irvine, Calif) include a pretrigger feature that shows the data preceding the trigger event as up to 50 negative line numbers. This allows the operator to readily see where in the program flow the error occurred and what conditions may have caused it.

Gould, Inc's K500-D logic analyzer can use three events to control the measurement window. The arm event, controlled from the front panel, allows the analyzer to look for an enable event. This, in turn, allows the instrument to seek the trigger event. The trigger event defines the end of memory and thus determines how many words are recorded prior to the trigger. The enable event, even though it may not be recorded, can be used as a reference (ie, it had to have happened prior to the trigger event).

The Philips PM 355. The soft keys in a row along the bottom of the screen are defined by a label at the bottom of the display to guide the user through setup and measurement procedures.

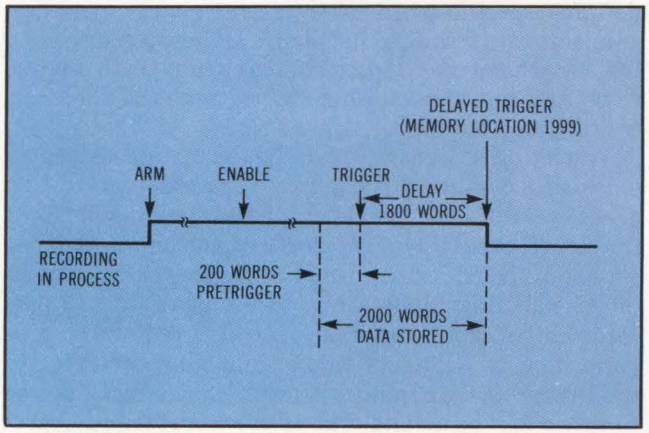
Along with multiplexed buses and prefetching (things that tend to confuse the true nature of timing relationships), the advent of systems using multiple microprocessors that communicate asynchronously adds another duty to the logic analyzer—time correlation. Such relationships require multiple clocks to handle data and addresses, and some use a clock qualifier to strobe into memory only the data associated with a given event, such as an I/O operation.

Microprocessor adapter modules and personality probes do much of the bus demultiplexing and microprocessor disassembly. The probes allow the analyzer to display the processor's mnemonics, along with data from the system under test. Several manufacturers, such as Dolch Logic Instruments (San Jose, Calif) and Gould's Instruments Div, provide disassembly in the probes themselves. In such an arrangement, the personality probe for a specific microprocessor connects to the processor socket and then to the logic analyzer's channel lines. A variation of this, the Racal-Dana product line, supplies a standard 8-bit probe and adapters for various microprocessor families. Information is taken into the instrument in the form of ones and zeros, and disassembly is done by disassembler programs plugged into read only memory (ROM) sockets in the logic analyzer. One advantage of this approach is that the user can easily switch between mnemonic display of processor instructions and binary, hexadecimal, and other formats.

The Tektronix DAS 9100 system takes a mainframe approach to microprocessor interfacing. Its PMA 100 personality module adapter connects the specifics of a processor to the DAS' data acquisition, triggering, and Define Mnemonics facilities. To use the DAS with a new microprocessor, the user plugs the new personality module into the PMA 100 and loads a tape with that processor's characteristics, via the tape drive, in the 9100 mainframe.

Also from Tektronix, the 1240 logic analyzer incorporates a dual timebase that allows concurrent, synchronized data acquisition from two separate timebases. The trigger can be defined using information from both timebases, and data are displayed in a time correlated manner. Similarly, the DAS 9100 system features an "arms" mode that allows simultaneous acquisition of synchronous and asynchronous data, then correlates them for display in either timing or state mode.

Capturing glitches is another important area in data acquisition. Approximately 5-ns signal transitions are generally regarded as glitches. They are displayed as small spikes in timing displays or noted with some symbol in the state display. One danger with this is that a pattern of glitches might be mistaken for a trigger word. The Gould K500-D, for example, has a trigger



In the K500-D from Gould, Inc, three sequential events are required to complete a recording. The trigger controls memory contents, while the enable allows the instrument to seek the trigger. The arm both begins recording and acts as the precursor to the enable event. Combination of enable and trigger events allows nested triggering. Here, the trigger delay is 1800 words.

filter that requires a glitch to exist for more than three clock cycles before a pattern in that time frame may be considered as valid data. As a corollary, many analyzers can be programmed to trigger on a glitch or a pattern of glitches since these are often significant sources of malfunction. To avoid problems associated with asynchronous data sampling, the Dolch 4850 instrument allows definition of timing tolerances via a skew window of ±9 clock samples. Thus, the user can set up timing conditions or windows, in which another transition could occur.

One of the newer features being incorporated in logic analyzers is pattern generation to stimulate the logic circuits under investigation. Recognizing that stimulation patterns are often needed (other than microprocessor outputs), the Racal-Dana 202 and the Tektronix DAS 9100 include word generation modules. The DAS 9100 module contains 16 output channels plus 2 programmable strobes, while the Racal-Dana 202/205 can convert 16 of its logic analyzer inputs into word generator outputs.

Tracing modes are useful in monitoring a set of inputs, an I/O port, or an address. Racal-Dana has a post-trace capability that lets the instrument capture up to 16 states of data after the trigger condition. Thus, a trace word and its results can be observed repeatedly. Similarly, Dolch's LAM 4850 has a trigger trace monitor in which a realtime word recognition counter keeps track of the trigger sequence. An occurrence count of various sequences, providing statistical information on portions of the program, is thus made possible. This trigger trace monitor feature is indicative of the type of performance analysis capabilities that are beginning to appear in advanced logic analyzers.

Interpretation and presentation

Considering logic analyzers as a class of instruments, the issues of data processing and ergonomics—ease of setup and use—tend to blend together. Once data are acquired and determined to be of the most interest, this data must be presented for analysis in a meaningful form (ie, readily readable in terms of the functions of the system under test). One of the fundamental requirements is to format data in the commonly accepted modes: binary, hexadecimal, octal, and decimal. Almost all current logic analyzers provide a timing display. Also, it is becoming ever more important to display mnemonics.

Mnemonic capability is not only important for following a microprocessor program, but it is also useful in easily identifying groups of signals or program sections. In the case of proprietary or bit-slice processors, the system designer must first determine the names of processor instructions. The 1630 logic analyzer from Hewlett-Packard (Palo Alto, Calif), for instance, allows the user to define up to 5-character labels to identify each channel in terms of its connection to the target system. In addition, the 1630's microprocessor-specific preprocessor performs inverse assembly to display instructions as they appear in the original source code.

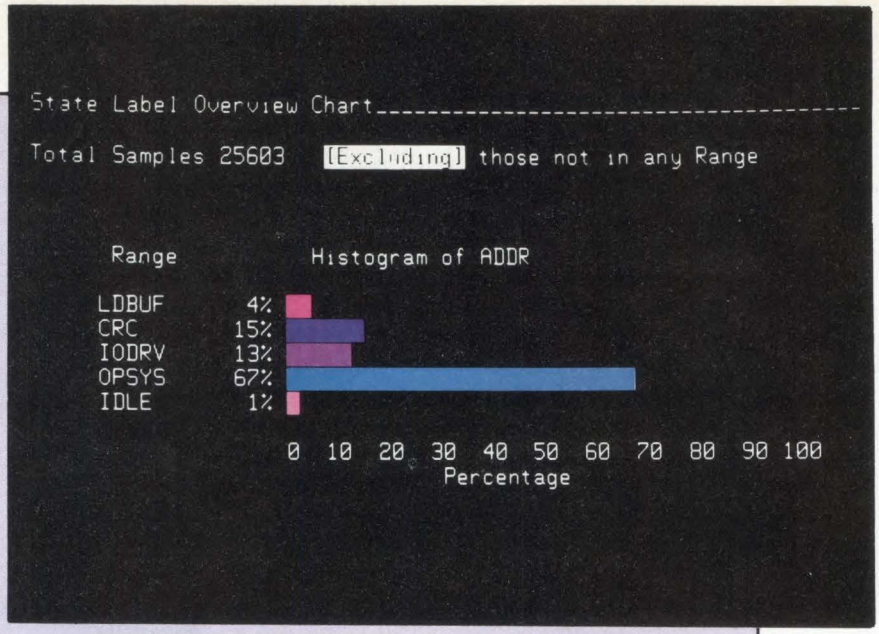
With the DAS 9100's Define Mnemonics feature, the user can define his own language by labeling data words up to 10 characters long. Data words are matched to an assigned mnemonic and displayed in the state table. Code can be quickly verified by first assigning mnemonics to events that are expected to occur, and then checking the state table. Up to 256 mnemonics can be stored and assigned to a single group of 256, or spread over 16 different groups of 16 each. Groups can be turned on and off as desired for selective examination of system operation.

Hewlett-Packard's 1630A/D logic analyzer gives designers a single instrument for both hardware and software test, debug, and analysis. The timing analysis mode (shown) opens a versatile window for observing bus, control line, and status signals.

Once data have been selectively captured and labeled, there is still quite a bit of information in the instrument's memory to deal with. The user needs a convenient method to find what he is looking for. Scrolling and paging through memory are obvious methods, but so are SEARCH and FIND commands. Racal-Dana's 200 series provides all four options and an auto-add feature to capture data. In this mode, it will capture the first 250 words the first time the program is run. The next time it will wait through the first 250 before capturing the next 250, and so on. Thus, the same trigger word can be used to capture different occurrences even though the program starts running from the beginning every time.

Windowing is a particularly useful feature in the timing analysis mode, as an address list is not handily displayed. A number of instruments provide a small graphic line representing the total memory space, with an indicator showing how much of memory is presently being displayed and where that window is located in the total memory space. When the display resolution is increased, the total amount of memory space presented on the screen decreases, and vice versa.

For timing measurements, it is necessary to have a visual picture of the timing relationships (represented by waveforms on the screen) and an exact measurement of timing down to the actual clock resolution of the instrument. Users can measure relative time between events (eg, a trigger cursor and one or more reference cursors) by positioning cursors, which cross all the waveforms,



An example of performance analysis on the Hewlett-Packard 1630. Label histograms display activity as a function of address space to quickly identify the distribution of program activity among software modules.

over the timing display. In addition, with analyzers from Philips, Tektronix, Gould, Hewlett-Packard, and others, this measurement can then be displayed as a delta time number on the screen.

Color in logic analyzers made its first appearance with the Color DAS 9129 from Tektronix. To make items of interest easier to find in a long state table listing, for instance, the 9129 highlights the trigger position in red. Glitches in the timing display appear as small green spikes on yellow waveforms and cursors appear as red lines. Setup and other reference information are displayed in green characters or green reverse video.

In addition to testing and debugging hardware and software, logic analyzers are being used in the software optimization process. By using performance analysis features, the user can see software bottlenecks and pinpoint areas that affect overall system performance. Hewlett-Packard's 1630, for example, uses nonintrusive methods to perform time interval distribution measurements and provide a histogram of time taken between two user-specified events. Displaying the average execution time of a module of code, along with the minimum and maximum times, is one option. In another approach, the user can take advantage of the ability to assign labels to various address ranges and perform label distribution measurements to display histograms of address space use.

Putting theory into practice

If the instrument does not lend itself to straightforward setup and configuration, however, all data acquisition and display features will only lead to frustration. Efforts in designing ergonomic setup procedures focus on defining the setup in terms of the functions of the target system. Since setup can be an involved process, a number of analyzers provide a means of storing setup parameters, along with a certain amount of test data.

Use of menus is, by far, the most common way to ease the tedium of configuring the instrument. The new instruments made by Hewlett-Packard, Gould, Tektronix, Kontron, and others can detect what plug-in modules and options are attached to them and display their power-up configurations to the user. The user's first task, then, is usually to group and label the available channels to suit the specific situation.

Most logic analyzers—at least those not integrated into development system workstations—avoid using a full ASCII keyboard. Even those that do have a keyboard, such as the Dolch Atlas, provide a number of programmable soft keys to lead the user through the configuration menus and perform many of the functions used during measurement operations.

In addition to the six soft keys next to the screen, the Dolch Atlas system has another row of programmable keys ("flip keys") along the top of its ASCII keyboard. The ROM-based operating software in each of the Atlas plug-in modules determines the functions of the flip keys. The name "flip key" is applied because each module comes with a page that can be added to a flip chart situated above the row of keys. The user simply flips to the page corresponding to the module in use and reads the key functions for that module.

Programmable soft keys are also used in Philips and Tektronix machines. In addition, Tektronix, in its 1240 logic analyzer, has introduced a touch-sensitive screen on which the user can see valid options highlighted in reverse video and make menu choices by touching them. To select numeric values, such as a signal level, the user turns a scoll knob on the front panel until the desired value appears.

Both Kontron and Racal-Dana narrow some of the menu options the user must choose from by incorporating process operator prompts into the menu. At each stage of the setup, these prompts present the user with only the pertinent questions. Hewlett-Packard's 1630, for example, helps in establishing measurement conditions by displaying options in bracketed fields, like transistor-transistor logic (TTL), and emitter-coupled logic (ECL).

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CIRCLE 87

The panorama

Logic analyzers, though microprocessor based, have become computers in their own right, and as such need their own peripherals. Besides a keyboard and display, some kind of mass storage device is obviously needed. The Kontron KLA series has gone the farthest in this direction by incorporating one or two 5¼" floppy disk drives behind the fold-down keyboard. The disks are used to store not only setup parameters and test data, but also to hold all the operating system software for the logic analyzer itself. This makes instrument upgrades and modifications mostly a matter of programming.

Tektronix and Hewlett-Packard have opted for mini-cassette tape drives, while Racal-Dana selected nonvolatile memory chips, electrically erasable programmable read only memories, to store setup data. Moreover, they also store patterns produced by the analyzer's word generator option to be used in stimulating the target system.

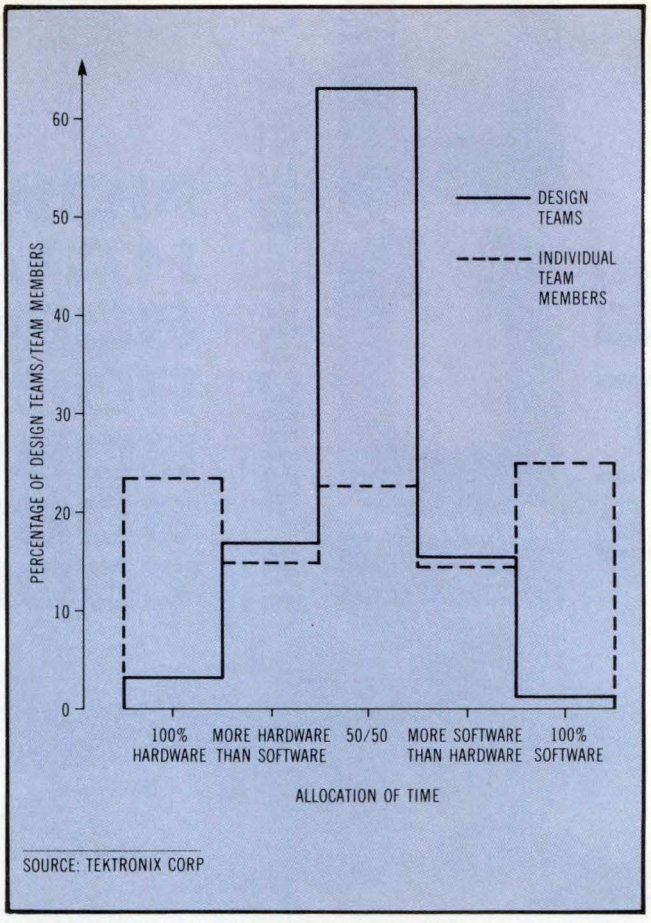
The logic analyzer's computer nature includes another attribute—communications capability—that will make it even more versatile as a standalone instrument within the overall design effort. The ability to store and share data via local area networks and to work closely with software development efforts is at hand, but the need remains for logic analyzers to be standalone instruments within this picture.

In July 1982, Tektronix surveyed 458 engineers (see the Tektronix histogram). This revealed that over 60% of the design teams found their efforts evenly divided between hardware and software (solid line). When individual activities (broken line) were examined, however, 24% of those surveyed said they spent 100% of their time on hardware, while 25% spent 100% of their time on software. When overlaps were considered, 39% of the engineers spent more time on hardware, and another 39% spent more time on software. This study reveals a specialization that still must be served by specialized tools, while an integrated tool also fits into the total picture.

As logic analyzers develop more computer-like characteristics, it is reasonable to expect them to fit smoothly into the software development realm. As opposed to the specialized computer (ie, the logic analyzer), the full computer can marry in-circuit emulation to logic analysis. Such integrated workstations are already making their appearance in the form of the Hewlett-Packard 64000 Logic Development System, the Dolch Atlas system, the Kontron Logic Analyzer/Slave Emulator, and the Gould 9516 Microsystem Integration Station.

Recognizing the need for communication between software emulation and hardware analysis, Hewlett-Packard supports a broad range of configurations in the 64000 system. But also recognizing that such a system cannot be justified for every member of a design team, the company is fully behind cost-effective standalone analyzers such as the 1630. In some instances, corporate mergers have been reflected in integrated products aimed at that part of the design team's efforts devoted equally to hardware and software.

Kontron's Logic Analyzer/Slave Emulator marries emulation and analysis by incorporating Kontron's KLA analyzer with the FutureData (Culver City, Calif) development system. Software development and debugging in high level languages is thus possible. Moreover, the long sought-after ability to correlate events in hardware with what is happening in high level software is now closer to reality. Gould's 9516 incorporates a dual bus architecture with a 160-ns emulation bus and a Multibus control bus. In addition, a 32-bit expansion bus is provided for future 32-bit microprocessors.



Results from a 1982 engineering survey done by Tektronix, Inc. The graph shows the distribution of time between hardware and software design teams and individual team members.

The Dolch Atlas system takes the effort toward integrating instrumentation functions in the design process even further. One CP/M based control computer can handle up to 14 plug-in instrumentation frontend processor modules. The system's logic analyzer modules are essentially plug-in versions of Dolch's standalone logic analyzers. However, the Atlas system supports trace and emulation modules and word generation. Signature analysis modules are said to be coming soon. One of the more forward-looking aspects of the Atlas system is its orientation toward local area networking, which allows communication between computers and other instruments. It also provides a means to download the results of large scale software development projects into an instrumentation environment, where integration and debugging can be done with easy communication between all levels of complexity.

As indispensable as these emerging emulation/analysis workstations will be for the design team, they will not replace the standalone logic analyzer (because

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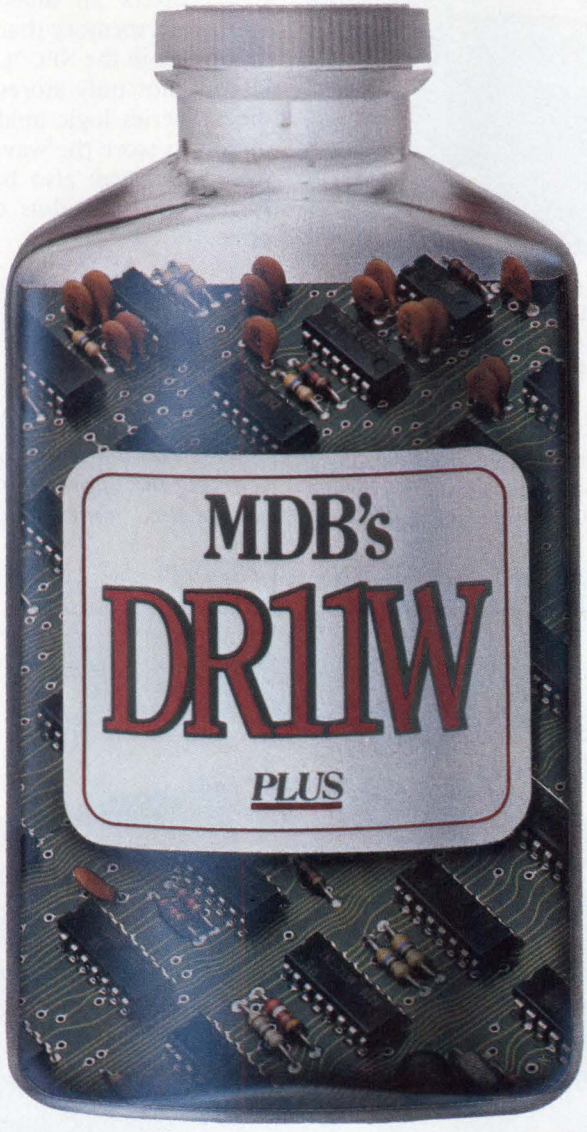

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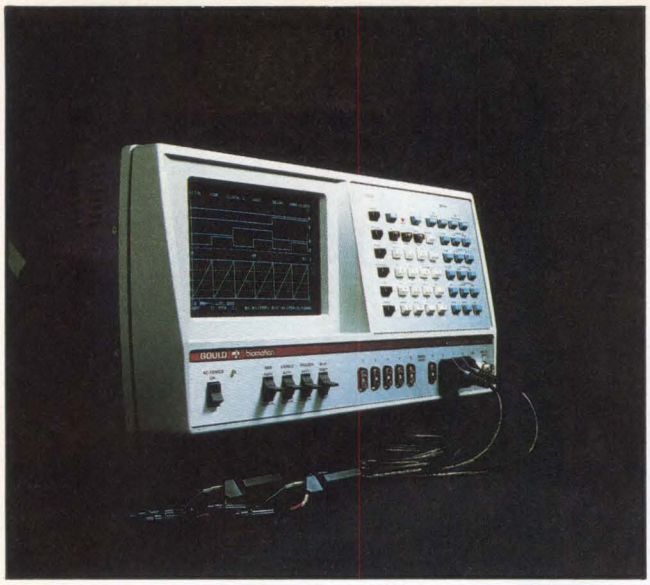

Gould, Inc's K500-D logic analyzer features a 2000-word memory and eight high speed inputs that clock at 500 MHz. In addition to time and data domain analysis, the K500-D has an input for an analog waveform digitizer.

of cost) nor the high level minicomputer in the software development phase (because the complexity of today's software tasks requires multiple programmers sharing files, dividing duties, and working in high level languages).

On the other side of the coin, one that is not often brought into the glamorous light of computer systems, is the need for the logic analyzer to communicate with lower level hardware instrumentation. When glitches occur, it is desirable to see exactly what kind of waveform has produced that glitch (which usually only appears as a spike or some other symbol on the logic analyzer's display) and to look at that waveform in its analog form.

One of the most significant of these is the digital oscilloscope, or waveform analyzer. The NPC-764 logic analyzer from Nicolet Paratronics Corp (San Jose, Calif) offers an analog waveform analyzer with a 1000-word memory that can be triggered by trigger conditions set in the NPC-764. Gould, Inc's 4500 digital oscilloscope not only stores waveforms when triggered by the KD series logic analyzers, but it has a floppy disk option to store the waveform data. Theoretically, such stored data can also be submitted to a computer for further analysis, thus completing the instrumentation cycle.

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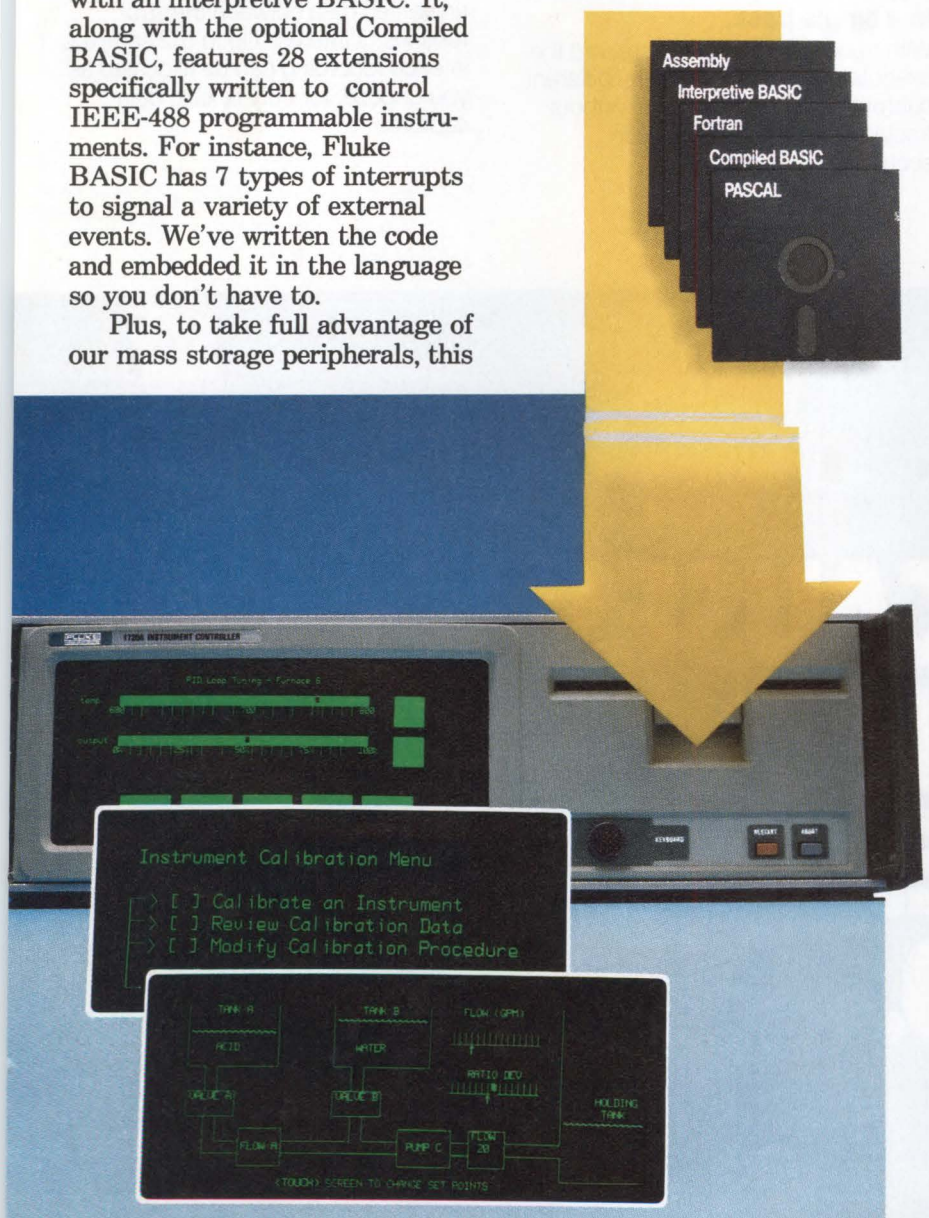

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Circle 93 for Technical Data

16 trace control levels store widely-separated segments of program flow.
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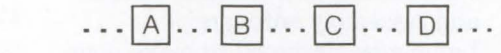
For example, in a numerically controlled mill, A is a port-reading subroutine for measuring a motor's position during the calibration cycle. B is the arithmetic subroutine that calculates the required calibration change. C outputs the new motor position, and D displays and prints the adjustment. The time between each subroutine is substantial but the data is irrelevant.



With trace control, you can record from the entry point of each routine to its exit point, without losing the initial information or wading through the unwanted data between the subroutines of interest. Up to 512 samples in each recording can be allocated as you choose, for truly flexible data capture.

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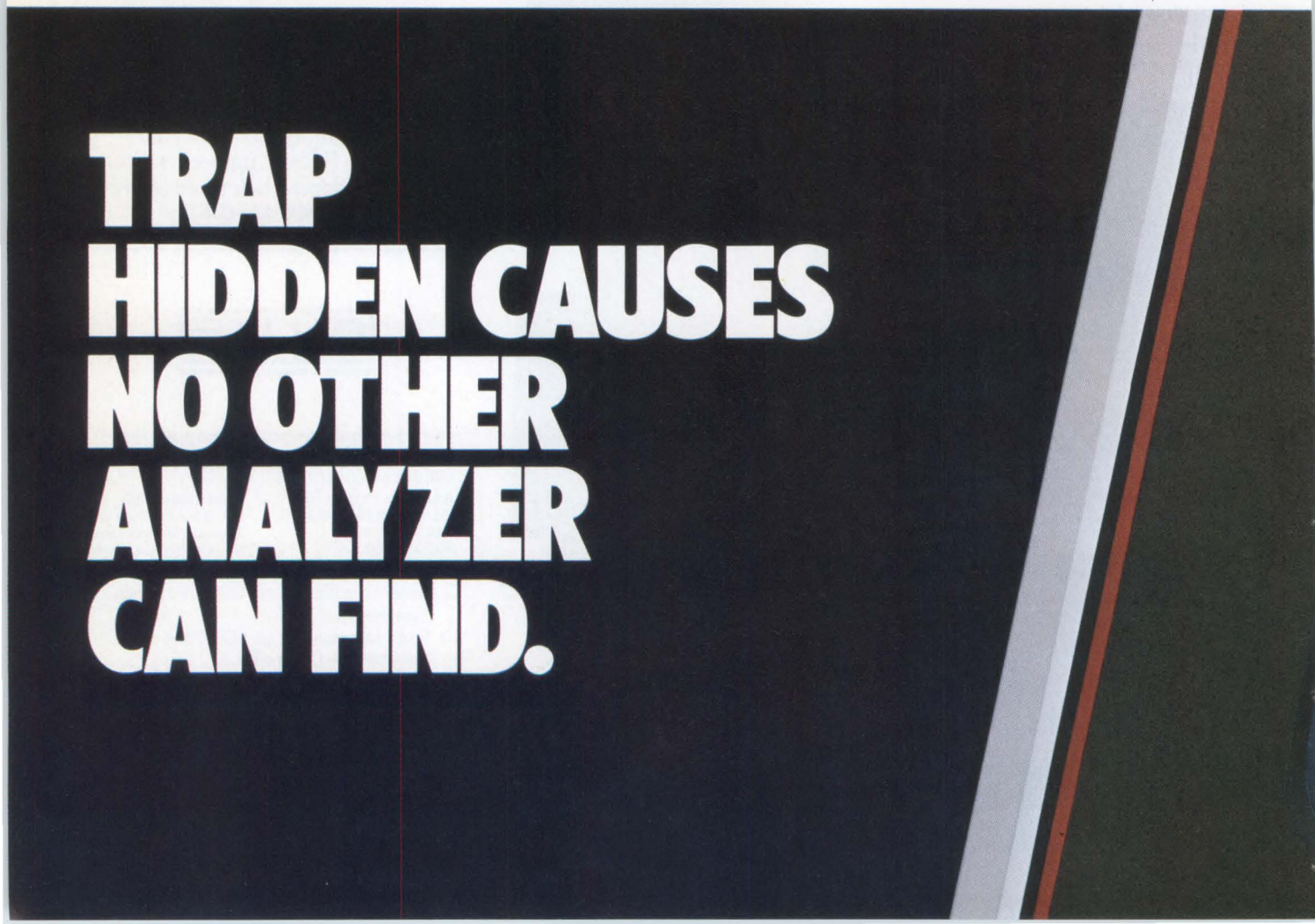

Find unknown execution errors in real time.

The K101-D or K102-D continuously monitors system execution, in real time, and displays a trace level status message. When a problem occurs, you can often identify the faulty sequence area immediately, just by reading the trace level status.

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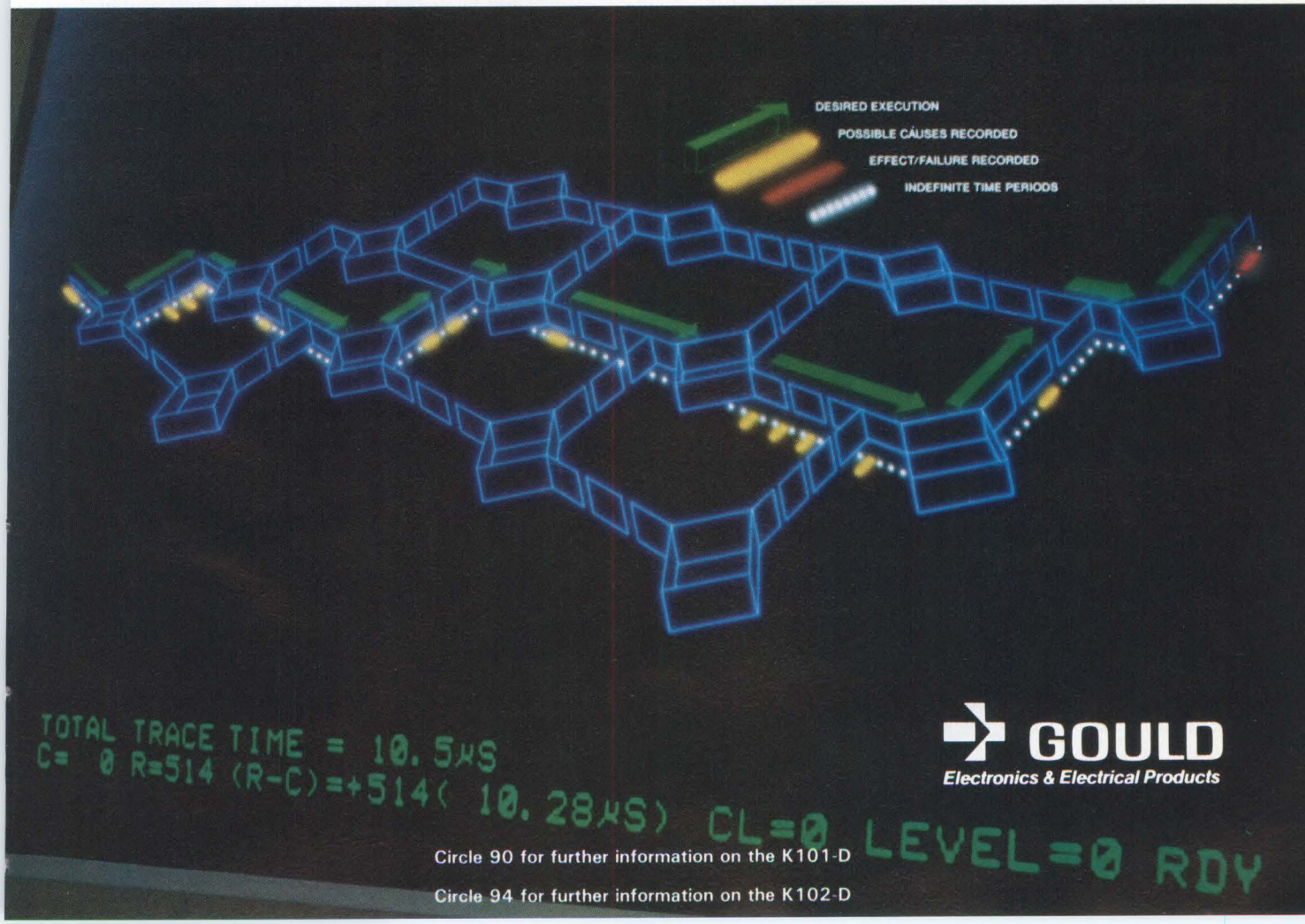

Circle 90 for further information on the K101-D

Circle 94 for further information on the K102-D

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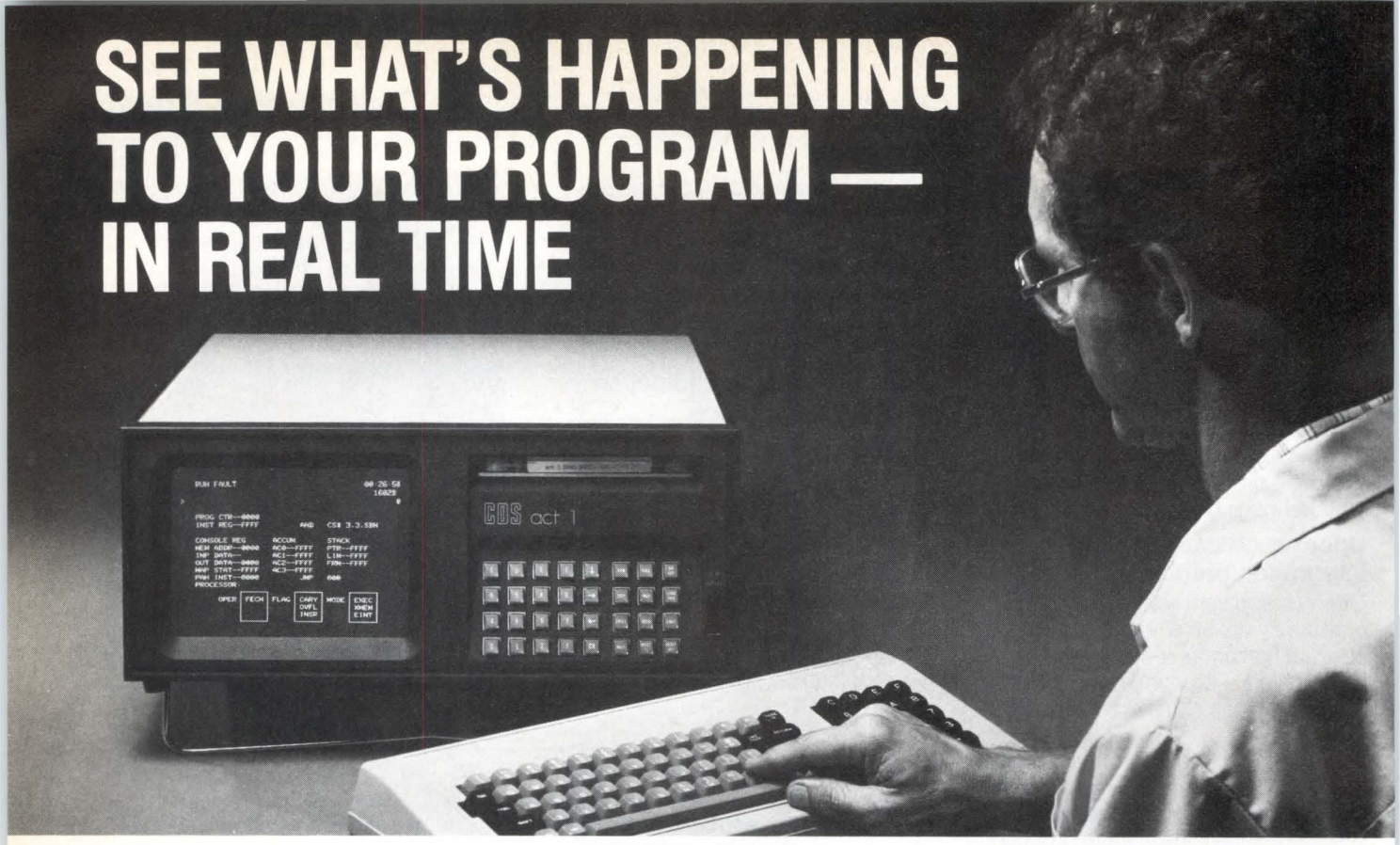

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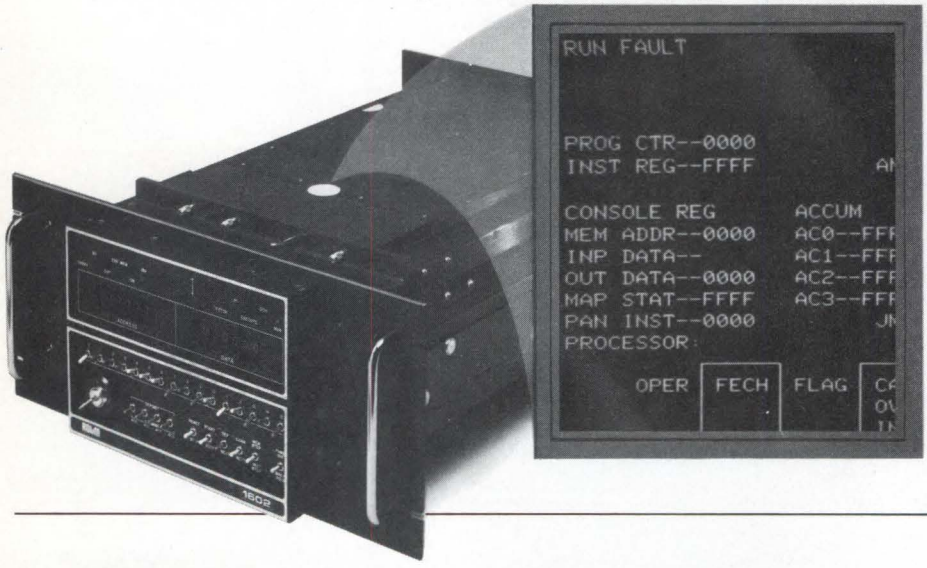

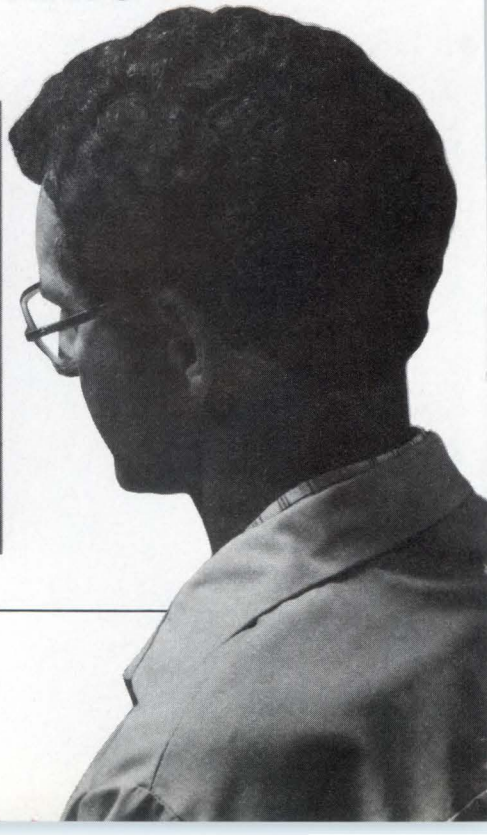

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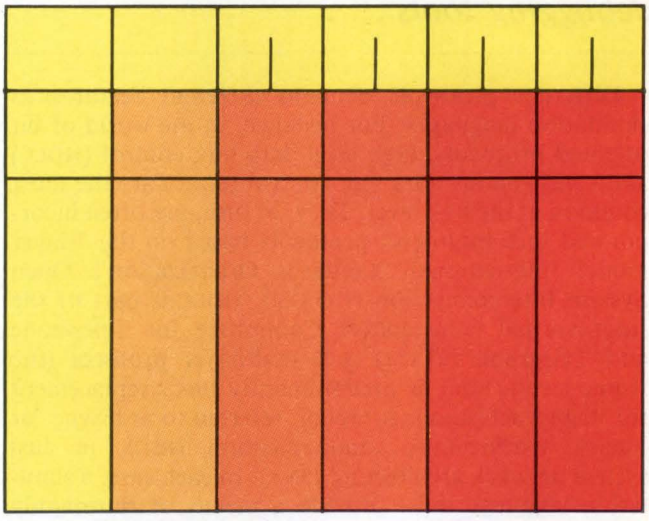
CIRCLE 95

SIMULATION TESTING ZIPS DATACOMM PRODUCTS TO MARKET

Protocol simulation languages avoid prolonged beta testing as they approximate real-world error conditions in the privacy of the designer's own lab.

by Adrian Warren, Michael Leigh, and Philip Black

As the demand for greater communication ability in small, inexpensive computer systems continues to grow, communication innovations rely more and more on software. Unfortunately, a noticeable time lag exists between the introduction of innovative hardware and the software capable of fully using it. The cost of creating completely new application software is rising, resulting in increased pressure on software design teams to quickly complete an expanding list of research and development tasks. The areas suffering most are regression testing and live environment (beta) testing stages. Avoidable errors that are expensive, embarrassing, and time-consuming to correct often go undetected until picked up by a disgruntled customer.



A protocol simulation language, however, can create the live environment needed in a data communication project to develop and test systems effectively. Simulation provides a major advantage over a real customer/real environment test, ie, by introducing abnormal operating conditions, of any specific type, at will. With such a language, beta testing time is saved because full error recovery capabilities can be designed, installed, and tested in advance; money is saved because fewer after-the-fact design changes are necessary.

Protocol simulation languages are merely vehicles for constructing and simulating protocols accurately, quickly, and cheaply. They can be driven by any host

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Michael Leigh is Tekelec Inc's marketing manager. He is a computer marketing specialist, having represented data communication companies in Europe and the United States. Born and educated in London, he has a degree in marketing from the Communications Advertising and Marketing Education Foundation. Mr Leigh also holds a graduate level degree from the London College of Distributive Trades.

Philip Black, president of Tekelec Inc, has pioneered several communication network projects and is involved in the preparation of ANSI Standard X3535/125 (data communication performance parameters) and the U.S. CCITT workshop on the integrated services digital network (ISDN).

machine, but they are generally of more value when used in conjunction with a data communication protocol analyzer/simulator. Protocol simulation languages can be used from the initial design phase, through the various stages of creation and testing, to the product's field site maintenance. Greatly varying levels of knowledge are inherent in the job functions associated with these project stages.

Since BASIC is widely understood and relatively easy to learn, it is an appropriate choice as the *lingua franca* of protocol simulation languages. BASIC provides a ready user interface since the user does not have to know where or how cyclic redundancy checks (CRCs) or block check counts are generated to test and to transmit a specific frame of information. This approach allows the running of menu-driven test programs by nontechnical staff. In addition, test results can be easily gathered, analyzed and distributed, which speeds feedback to research and development (R&D) engineers and makes it more meaningful because errors are easily documented and specific bug ridden modules quickly identified.

Simulation languages provide . . . a comprehensive kit of development and debugging tools . . .

Different protocols demand different features in simulation languages. For instance, in the world of bit oriented protocols, high level data link control (HDLC) and synchronous data link control (SDLC) are the most common at the link level. They, in turn, are often incorporated into multilevel protocols based on the 7-layer model International Standards Organization's Open System Interconnection (ISO OSI). HDLC is part of the International Consultative Committee for Telephone and Telegraph (CCITT) X.25 multilayer protocol (the frame level). SDLC is predominantly IBM's replacement for its bisynchronous protocol, referred to as bisync, or binary synchronous communication (BSC), in IBM system network architecture (SNA). In each case, a simulation language must provide a means of thoroughly testing each protocol.

Protocol simulation languages provide original equipment manufacturers (OEMs) with a comprehensive kit of development and debugging tools. For the first time, a battery of negative, "what-if-something-goes-wrong" tests can be carried out before product completion and subsequent beta site testing. By making use of simulation techniques, it is possible to build full-error recovery into a new system, regardless of whether the error is in the hardware, in the software, or is operator induced. This recovery ability is not attained easily by other means. Even the equipment that a product will eventually run in conjunction with only provides a source of positive testing; little in the way of negative testing is possible. The dangers of this situation are illustrated in the following hypothetical situation.

A firm manufactures plug-compatible IBM look-alike 3276 cluster controllers. Even though the firm has access to a real IBM 3705 frontend processor with all the hardware and software necessary to drive it, the manufacturers are still unable to find out what happens when the system receives an invalid SNA/SDLC command because the 3705 is incapable of generating erroneous commands. Compounding the problem is the fact that documentation in this area is often incomplete.

Using simulation in the design process

Simulation techniques can be used effectively by OEMs in many facets of data communication applications, including system, hardware, and software design and testing, and quality assurance (QA) and customer support test procedure design. The major criterion for deciding whether or not to use simulation is the project's use of communication protocols. Simulation is needed when two or more intelligent devices communicate—with or without packet or circuit switching. Link protocols that can be simulated include SNA/SDLC; X.25 levels 2 (HDLC), 3, and above; BSC 3270; and many more.

The steps involved in taking a project from concept to completion include these broadly defined modules: identifying the application; creating specs (including selection of protocol to be used); selecting hardware/software parameters; translating the specs into logic diagrams and software tasks; allocating tasks to the various hardware/software teams; testing the modules prior to integration; integration/integration testing; regression testing; QA testing; and beta site testing/ongoing customer support. Each creative use of specialized simulation software can help designers achieve goals faster, more comprehensively, and sometimes with significantly less capital outlay in the last five modules.

Prior to integration, each of the modules, in the absence of simulation, must be tested in isolation. Specialized interface routines must be written to accomplish this. Delays during the integration stage of the project may be encountered by several design teams trying to use limited test resources. Additional software must be written to drive the various modules once the interface routines are completed. Apart from these drawbacks that waste time and money, problems arise when the team that writes the application software under test also writes the test procedure software. Undiscovered errors can be unknowingly mirrored and introduced into the test software.

When a protocol simulation language is used, flow control testing that avoids unnecessary, repetitive programming is easily achieved. A specific module's functions can be isolated and examined in normal operation as well as in forced-error states that have been set up. Tests are created in an easy to write, flexible format that uses proven language syntax and standard industry mnemonics.

Another important advantage of simulation testing at the module stage is that each group can test its modules as soon as the code is finished. This freedom to systematically complete one task, thoroughly test it, and then proceed immediately to the next is invaluable. During the course of an entire project, this process saves many engineering hours.

Integration testing, of course, is a must. Once a system is integrated, it becomes much more difficult to

TABLE 1

Basic Command Extensions of FRAMEM

Command	Syntax	Usage
MLIST	MLIST	Display user defined frame control mnemonics
DELETE	DELETE "name"	Remove "name" from the frame control mnemonic table
DEFINE	DEFINE "name" = x	Add "name" to frame control mnemonic table, x = value of frame control
DEFSUB	DEFSUB "name" = x	Define a subroutine to be called when "name" frame is received; x = line number of subroutine
DISPF	DISPF	Display the last frame received or transmitted
REC	REC	Receive a frame from the line if one is available
TRAN	TRAN	Transmit a frame
TPRINT	TPRINT	Print a trace of received and transmitted frames
CLEAR	CLEAR	Clear trace buffer
SET	SET xxx = 1 SET xxx = 0	Set interface signal xxx to logical 0 or 1
TEST	TEST xxx = 1 TEST xxx = 0	Test if interface signal xxx is at specified level (logic 0 or 1)

find and test error conditions due to the possibility of subtle inter-module communication errors. Creating an established test procedure for each stage of integration is important because if the need to rewrite one or more modules arises, the whole integration process has to be repeated. This stage of testing must be designed in conjunction with the initial system design.

Once each module has been fully tested for optimum performance, the integrated system can be isolated by function, or groups of functions, and tested as a complete system. If bugs occur, the events causing errors can be recorded on disk and reintroduced once modifications have been made. This is the essence of continuous regression testing.

Although by no means guaranteed, a flawless design is more likely if simulation is used from the start.

Regression and QA test plans are important in the initial planning stage. These tests must be performed to ensure that each cell of the various state matrices that is subsequently modified can be easily retested. New or modified modules must not cause further errors. It is therefore essential that the test plan be flexible enough to allow additional test procedures without requiring extensive revisions to existing tests. Using simulation software, it is easy to adapt a set of integration tests from modulo 8 to modulo 128. It is just as simple to change from standard 8-bit HDLC addressing to expanded 16-bit addressing or to take a set of tests designed to measure the performance of an HDLC device and adapt these tests to fit an SDLC device, as can be seen in the case study that follows. Through the use of simulation software, the integration testing stage can be repeated as often as necessary, using consistent benchmark programs.

Many problems that occur when the QA test team starts testing a new product stem from the fact that test team members often do not have the same programming background as the R&D engineers. Frequently, the QA team has to rely on test procedures written by a programming team—that is, by necessity, the same team that programmed the new equipment in the first place. This may cause tunnel vision test flaws. Delay and test errors result because of insufficient communication or the inability to translate requirements from one group to another.

QA engineers need no longer rely on the programming department because of the creation of a high level language, founded on BASIC, that has been extended for protocol simulation. With even a relatively low level of programming knowledge, QA engineers can develop a comprehensive range of tests in order to check out all facets of the new project. QA testing can be performed quickly and consistently, and protocol violations can be introduced for response testing.

Beta site testing—a polite expression for a company that volunteers to be a guinea pig in return for new technology and expanded customer support—is an important aspect of any new product development. This field test can last a few weeks to a year or more, depending on the product's complexity, and can uncover flaws that have not materialized during lab development. These bugs are often evident only in abnormal conditions that occur in a real-life environment.

Although by no means guaranteed, a flawless design is more likely if simulation is used from the start. Not only can a complete barrage of creative negative testing be completed and the necessary modifications made sooner, but individual tests can be revised quickly while other benchmark measurements remain consistent. Because the regression/reintegration test stages are completed faster and more thoroughly, a highly reliable product goes to beta testing sooner, and beta testing may, in turn, be completed sooner.

A case study

FRAMEM, Tekelec's FRAMe level EMulation software, is an extension of the BASIC programming language (Table 1). (For all practical purposes, emulation and simulation should be considered the same.) While FRAMEM was designed specifically for use on the link

TABLE 2

FRAMEM Variable Examples

Code	Comments
TIM0	Count down in 10-ms intervals
TIM1	Count up in 10-ms intervals
TIM2	Count down in seconds
TIM3	Count up in seconds
RXADDR	Address field
RXFCTL	Frame control field with poll/final bit and N_s, N_r removed if necessary
RXP/F	Poll/final bit (either 0 or 1)
RXN(S)	N_s if received
RXN(R)	N_r if received
RXV(S)	V_s of rejecting station
RXV(R)	V_r of rejecting station
RXRFCTL	Rejected frame control byte
RXDIAG	Diagnostic byte
RXFRLEN	Length of frame received
TXADDR	Address field
TXFCTL	Frame control field
TXP/F	Poll/final bit
TXN(S)	N_s
TXN(R)	N_r
TXV(S)	V_s
TXV(R)	V_r
TXRFCTL	Rejected frame control field
TXDIAG	Diagnostic byte

level, higher language levels may be included in the data stream, even though they will remain transparent to FRAMEM.

The hardware on which FRAMEM runs is a protocol simulator called the Chameleon. When coupled with the Chameleon, FRAMEM allows a user to customize an HDLC/SDLC type of link control protocol. As a result, a user can emulate a specific device, such as a 3276 cluster controller, or test a specific device by supplying either valid or invalid prompts/replies. FRAMEM also allows a user to certify that a compatible device does indeed adhere to the protocol that it is using.

FRAMEM was designed to allow for specific manufacturers' deviations from standard protocols. To this end, FRAMEM employs a set of special variables (Table 2) that are used to hold frame information (such as sequence numbers, frame control fields, and poll/final bit); some special transmission, reception, and pin level interrogation and setting commands; plus a set of commands used for timing control. In addition, a BASIC language approach minimizes the time that a user spends becoming familiar with program syntax and structure.

After a simulation language has been mastered, users can perform many tests specific to their projects. The following two scenarios are common to many projects, while the third situation in this series illustrates how easy it is to change simulation programs to suit new criteria.

In the first scenario, FRAMEM programs the Chameleon to perform like a 3705 IBM-type frontend processor. The purpose of this test is to ensure that a 3274 controller, in normal response mode, will respond correctly—by transmitting a frame reject (FRMR)—to the following illegal commands: reception of an unimplemented command; invalid N_r; buffer overrun, that is, when an I-frame has an I-field greater than 256 bytes. Table 3 lists the FRAMEM program and comment lines required for the negative testing of a 3274 controller.

In the second scenario, FRAMEM is used to program the Chameleon to perform like either side of an X.25 link. This example illustrates how a link is established, how eight I-frames are transmitted with the correct sequence numbers, and how the link is disconnected. Table 4 lists the code and comments pertinent to an X.25 simulation.

The flexibility of protocol languages is further demonstrated by showing how easy it is to make changes in the coding of the second scenario, just described. If a new line of code, such as 3 EXTEND, is added at the start of the test, the 8-bit address field is automatically changed to the expanded 16-bit HDLC mode address field. If another line, 5 MOD 128, is added, the number of frames sent/received (N_s and N_r) values are automatically changed from modulo 8 to modulo 128. Either or both of these changes could be implemented. If lines 20, 70, and 230 were changed so that 20 TXFCTL = SNARM; 70 IF RXFCTL = NSA GOTO 90; and 230 IF RXFCTL ÷ NSA GOTO 1000, then the scenario will have been changed from an HDLC to an SDLC protocol with a great savings in time and energy for QA test engineers.

With regard to the X.25 simulation of the second scenario, it is possible to use an automatic simulation software package that requires no user programming. One reason this is possible is that the CCITT X.25 protocol can be defined within fixed parameters in levels 2 and 3. An exception is level 1, the physical interface, which offers the choice of X.21 or X.21 bis. The latter is more commonly known as the American National Standards Institute (ANSI) RS-232-C. The physical link option therefore calls for two alternatives, both available "off the shelf," that have few differences. RS-232-C is by far the most common in the United States; however, the 15-pin X.21 plug is the most commonly used in Europe and may be seen in the United States on many of the new public branch exchange offerings.

It is possible to use an automatic simulation software package that requires no user programming.

Level 2 uses the European Computer Manufacturers Association subset of transparent Bisync or HDLC link level control. Although link access procedure (LAP) and LAP balanced (LAPB) (two different acceptable link access protocol methods) are documented and differentiated by their mnemonics and flow control, both have the same fixed-bit parameters. The flags, the control field, and the address field are always 8 bits (extended mode HDLC is not included in the X.25 spec but does apply to X.75 and allows for 16-bit addressing), and the frame-check sequence is always 16 bits. Although the information field can be any length, this has no bearing

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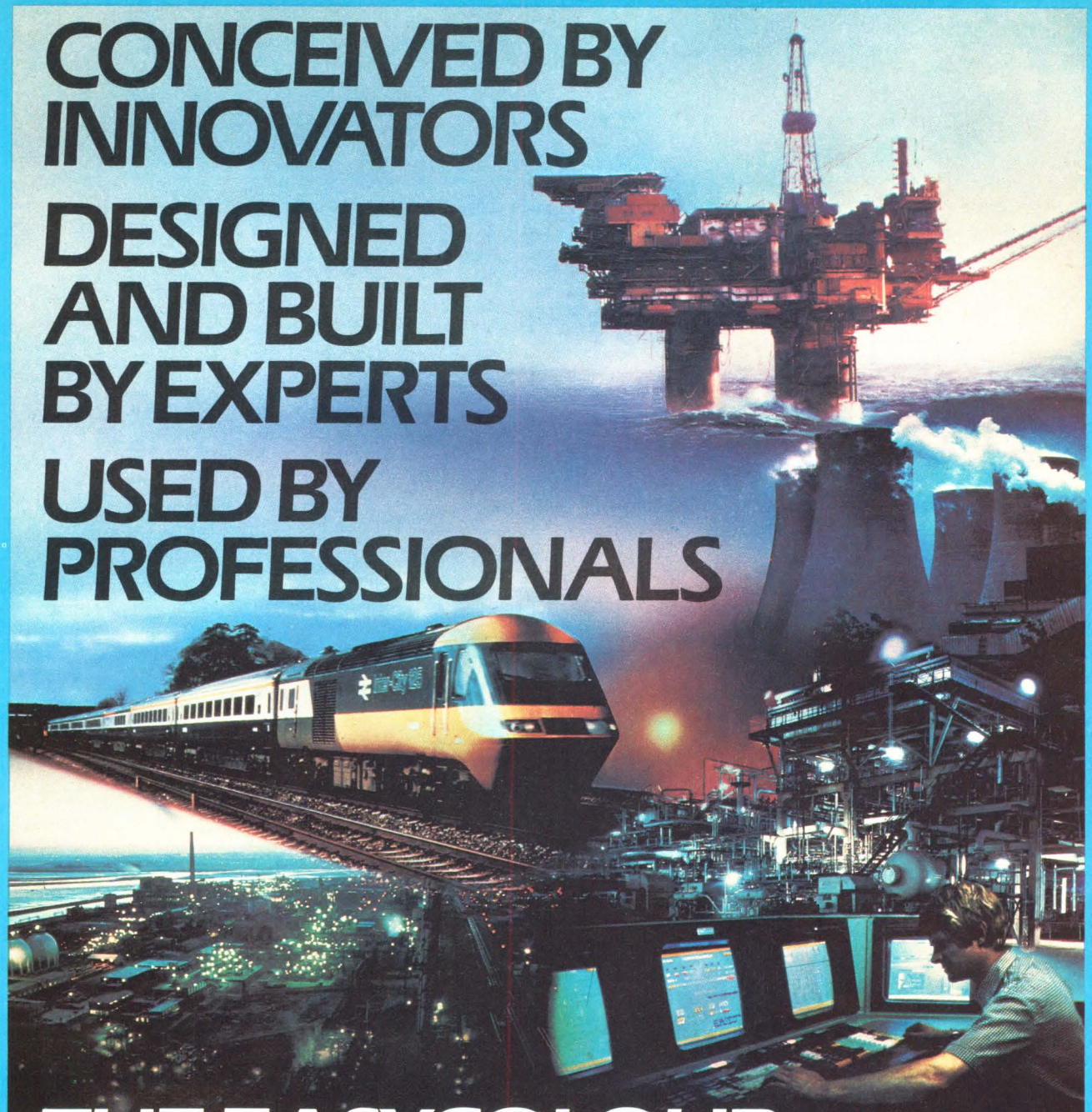

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TABLE 3

3274 Simulation Code and Comments

Code	Comments
10 CLEAR	Clears the trace memory
20 TXADDR = &CO	Sets the address field to CO Hex
30 TXP/F = 1	Sets the poll bit to on
40 GOSUB 400	Executes a subroutine that sets the controller in normal response mode and waits for an NSA response
50 TXFCTL = &FF	Sets the frame control field to FF Hex
60 GOSUB 300	Executes a subroutine that transmits a frame and waits for a response
70 IF RXFCTL # FRMR GOTO 250	Checks that an FRMR was received and if not will go to the end of the test
80 GOSUB 400	Executes a subroutine that will set the controller in normal response mode
90 TXFCTL = IFRAME	Sets the frame control field to an I-frame
100 TXN(S) = 0	Sets N_s to 0
110 TXN(R) = 2	Sets N_r to 2
120 TXIFIELD = ASC > ABCDEFGHIJKLMNOPQRSTUVWXYZ	Defines an I-field equal to the ASCII equivalent to the alphabet from A to Z
130 GOSUB 300	Executes a subroutine that transmits the frame and waits for a response
140 IF RXFCTL # FRMR GOTO 250	Checks that an FRMR was received and if not will go to the end of the test
150 GOSUB 400	Executes a subroutine that will set the controller in normal response mode
160 TXIFIELD = HEX >	Clears the I-field
170 FOR A = 1 to 300	Is a loop that creates an I-field 300 bytes long
180 TXIFIELD + ASC > A	Is a loop that creates an I-field 300 bytes long
190 NEXT A	Is a loop that creates an I-field 300 bytes long
193 TXN(R) = 0	Sets N_r to 0
194 TXFCTL = IFRAME	Sets the frame control field to an I-frame
200 GOSUB 300	Executes a subroutine that transmits the frame and waits for a response
210 IF RXFCTL # FRMR GOTO 250	Checks that an FRMR was received and if not will go to the end of the test
220 PRINT	Prints a blank line on the terminal
230 PRINT "TEST PASSED"	Prints a message to say that the controller passed the test
240 GOTO 270	Transfers control to line 270
250 PRINT	Prints a blank line on the terminal
260 PRINT "TEST FAILED"	Prints a message to say that the controller failed the test
270 TPRINT	Prints a trace of the traffic
280 STOP	Terminates the program
300 TRAN	Transmits a frame
310 REC	Checks if a frame has been received
320 IF RXFRLEN = 0 GOTO 310	Checks the variable RXFRLEN, which indicates the length of a frame received, and if it is 0—ie, no frame received—will loop until a frame is received
330 IF RXP/F # 1 GOTO 300	Checks that the final bit is set in the frame received and if not will transfer control to line 300
340 RETURN	Is the end of the subroutine
400 TXFCTL = SNRM	Sets the frame control field to an SNRM
410 TRAN	Transmits the frame
420 REC	Checks if a frame is received
425 IF RXFRLEN = 0 GOTO 410	Checks the variable RXFRLEN, which indicates the length of a frame received, and if it is 0—ie, no frame received—will loop until frame is received
430 IF RXP/F # 1 GOTO 410	Checks that the final bit is set in the frame received and if not will transfer control to line 410
440 IF RXFCTL # NSA GOTO 400	Checks that the frame received is an NSA and if not transfers control to line 400
450 RETURN	Is the end of the subroutine

TABLE 4

Code and Comments for X.25 Simulation

Code	Comments
10 TXADDR = 03	Sets the address field to 3
20 TXFCTL = SABM	Sets the control field to an SABM
30 TXP/F = 0	Sets the poll bit to 0
40 TRAN	Transmits the frame
50 REC	Checks if there has been a frame received
60 IF RXFRLEN = 0 GOTO 50	Checks the variable RXFRLEN and if 0 (ie, no frame has been received) loops to line 50
70 IF RXFCTL # UA GOTO 40	Checks that a UA response has been received and if not loops back to line 40
100 TXFCTL=IFRAME	Sets the control field to an I-frame
110 TXIFIELD-HEX>0123456789ABCDEF	Defines the I-field in Hex
120 FOR TXN(S) = 0 to 7	Is the start of a loop that will increment TXN(S) from 0 to 7
130 TRAN	Transmits the frame
140 REC	Checks if there has been a frame received
150 IF RXFRLEN = 0 GOTO 140	Checks the variable RXFRLEN and if 0 loops back to line 140
160 IF RXFCTL # RR GOTO 1000	Checks that an RR frame was received as a response and if not transfers control to the error routine at line 1000
170 IF RXN(R) # TXN(S)+1 GOTO 1000	Checks that the correct value of N_r was received and if not transfers control to the error routine at line 1000
180 NEXT TXN(S)	Is the end of the loop
190 TXFCTL=DISC	Sets the control field to a DISC
200 TRAN	Transmits the frame
210 REC	Checks if a frame has been received
220 IF RXFRLEN = 0 GOTO 210	Checks the variable RXFRLEN and if zero (ie, no frame received) loops back to line 210
230 IF RXFCTL # UA GOTO 1000	Checks that a UA response was received and if not transfers control to the error routine at line 1000
240 PRINT "TEST O.K."	Prints a message that the test was correct
250 STOP	Terminates the program
1000 PRINT "TEST FAILED"	Prints the message that the test failed
1010 STOP	Terminates the program

on the structure of the actual protocol. Within the control field, N_s and N_r and the poll/final bit all remain in constant position.

Similarly, level 3 (the packet level) retains a constant format in terms of its address and control fields. Also, the general format identifier (GFI) logical channel group (LCG) and logical channel number (LCN) and the packet-type identifier remain constant. Fig 1 shows the X.25 frame and packet level structures.

The simulation software for X.25 applications is an exact mirror image of the frame/packet structure depicted in Fig 1. A terminal manufacturer can set this software up in a host computer to function exactly like an X.25 network. A network equipment manufacturer can make the software function like a number of simultaneous subscribers sending correctly structured traffic. A modem manufacturer can simulate both sides of the link and choose whether to give or receive the clock. This choice refers to the data terminal equipment/data circuit terminating equipment (DTE/DCE) relationship in an X.25 network. A DTE receives the clock, while the DCE provides the clock.

In this true simulation, the software performs exactly as the real equipment would—providing that the host computer drives it correctly. Flow control at the frame and packet levels, errors and error recovery, data generation and reception, as well as all protocol timers and counters, are all handled automatically. No programming is necessary unless deviation from the standard protocol is designed in order to test error recovery procedures thoroughly. If an operator wants to alter the protocol, the amount of programming required is proportional to the amount of deviation. Standard X.25 mnemonics are used to address the specific parameter or series of parameters. Prepackaged GTE Telenet type certification procedures with which to test the equipment's compatibility are available.

Finished simulation scenarios in the SNA/SDLC world are created by the user from a simulation language. (Strictly speaking, this language is actually an emulation.) The reason that automatic simulation is not possible in SNA/SDLC is that many user-defined variables are available. Although the flag, address field, and control fields are always 1 byte long, the transmission

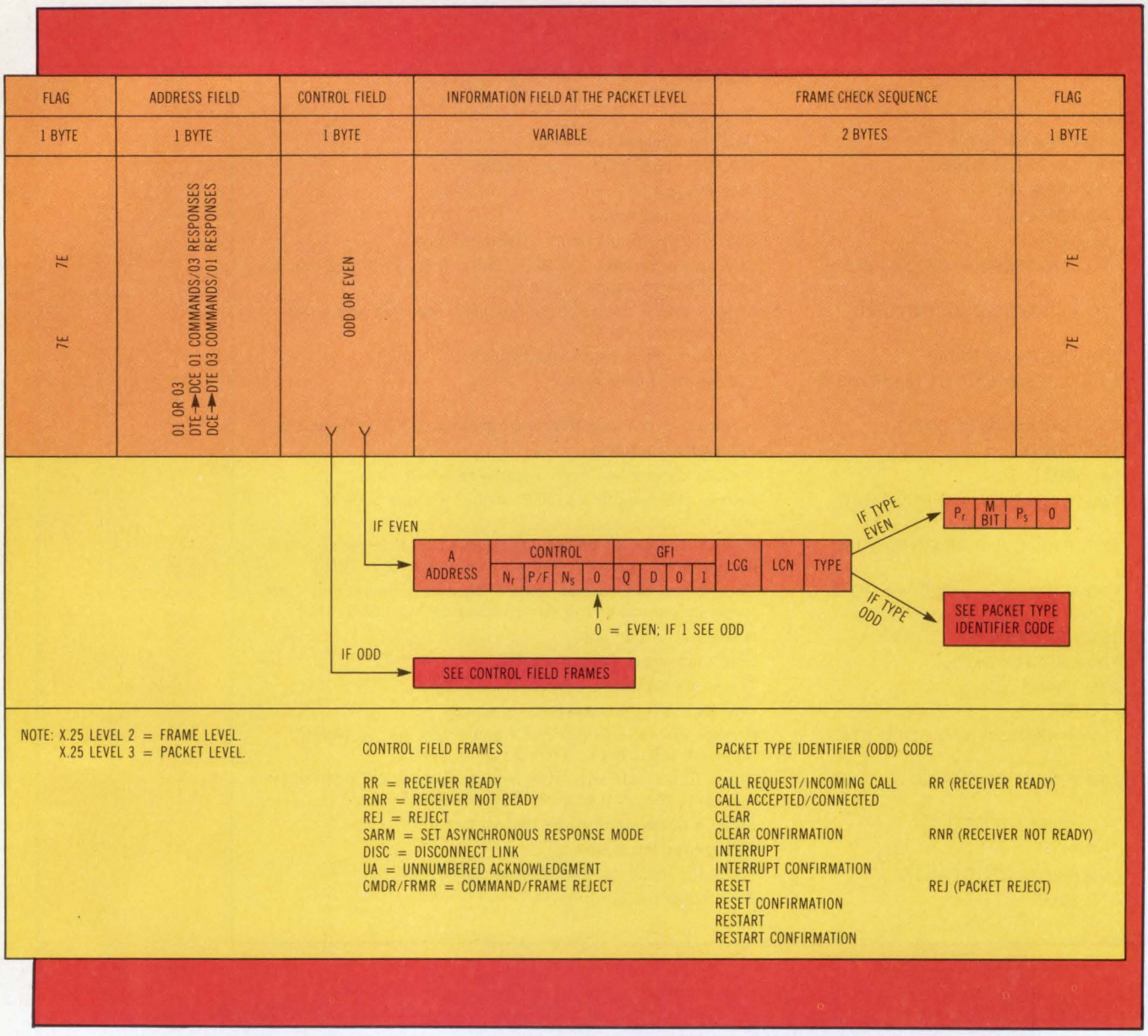

Fig 1 X.25 frame and packet level structures. By introducing various negative fault states into the frame structure through a simulation language, data terminal equipment manufacturers can see how their designs perform in the real world.

header (TH) can be from 2 to 10 bytes long. Similarly, although the request response header (RH) is always 3 bytes long, the function management header (FMH) and the request-response unit (RU) are both nonspecified variables. The frame sequence illustrated in Fig 2 is completed by a 2-byte frame check sequence (FCS) and a 1-byte flag.

The number of other SNA protocol variables is almost infinite. Even narrowing the scope of the discussion to just the 3270 model range—which includes only half-duplex, flipflop, send/receive protocols—leaves enough valid options to fill a large manual.

A protocol simulation language for the IBM world provides an invaluable tool with which to define respective values for the myriad options available to the user. Once defined, these options need not concern the user again unless a change in those values is specifically desired. Only the routines under investigation require attention; the rest of the protocol structures will run automatically within the user-defined framework. Tremendous time-saving and consistency result. The ability to isolate error generation sources quickly should not be discounted, either.

By using a specific Bisync simulation package, the user can fully support the protocol. Check counts, acknowledgments (ACKs), and negative acknowledgments (NAKs) can be handled manually or automatically. All control codes are available in mnemonic form for both Extended Binary Coded Decimal Interchange Code (EBCDIC) and ASCII. Multiple data blocks can be created and transmitted under program control. Point to point and multipoint environments are supported in normal and transparent text modes.

Hardware implications of simulation software

Simulation software is usually part of an integral hardware/software system, which is not to say that the software cannot be configured to run on an alternative

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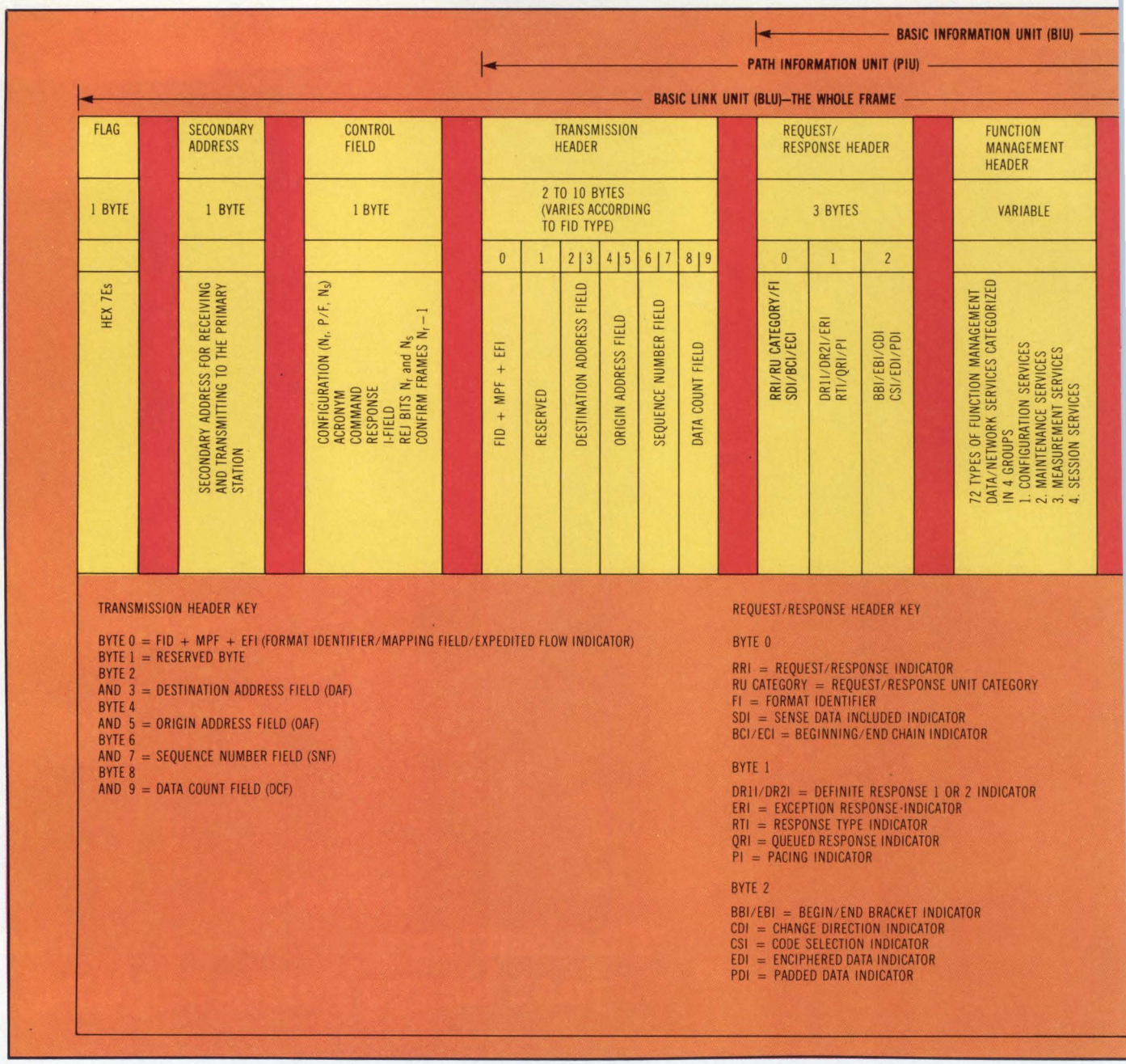
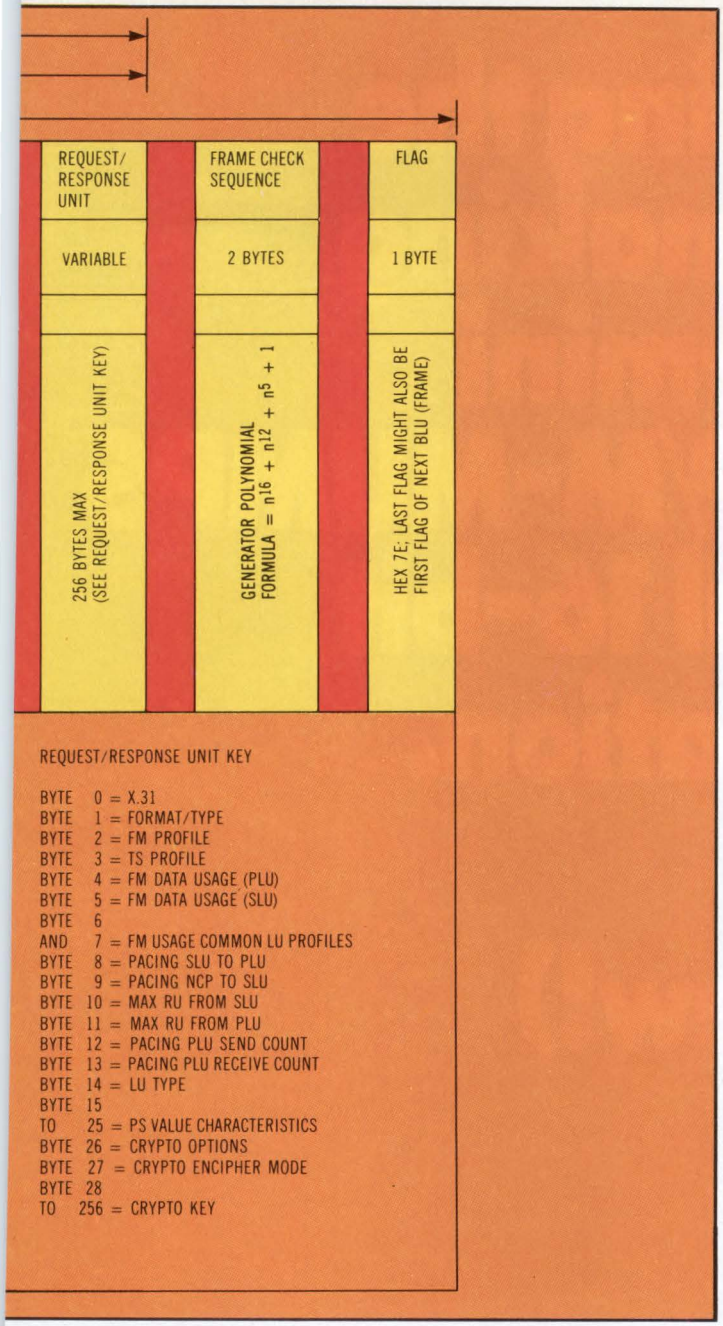


Fig 2 SNA/SDLC **frame structure. Simulation of such complex frames demands simulation software that is flexible, powerful, and predictable. If any of these criteria are not met, simulation accuracy is in question.**

host. However, the hardware has usually been developed with a high level communication capability built in. The hardware usually has a split-screen display to show traffic on both sides of the link. It should have multiprocessor architecture with specific protocol handling components to allow such things as automatic CRC calculation for a number of protocols. If simulation software is run on an alternative device, some of the advanced features of the software will most likely be lost due to the lack of hardware communication features. It is also possible to lose compound triggering analysis functions and introduce error conditions unknowingly. In addition, new application packages and software upgrades will not be easily adaptable.

Therefore, if the project is large, the cost of software-specific simulation hardware is justified. A price of $20,000 for a fully equipped high speed (128k-bps) machine, complete with different language packages for low level/high level work, is about the norm. A machine with low speed simulation ability may cost $14,000 plus software. Costs should be weighed against the enormous time/expense savings and increased reliability that simulation provides. Remember that some simulation hardware is expandable and adaptable to other projects, such as Teletex or local area network development. This adaptability allows the amortization of cost over several projects.

The buyer should make sure that the hardware vendor whom he selects has a strong background in communication protocols and network communication. Further, by asking the right questions of vendors, designers often find that an existing protocol is already



equipped to do the job for which a hybrid protocol was originally chosen. In the competitive communication marketplace, every little bit helps. Obviously, in communication simulation, subtle shades of gray color the designer's decision making. One thing exquisitely clear, however, is the value of a powerful simulation language to both developers and users of modern network hardware.

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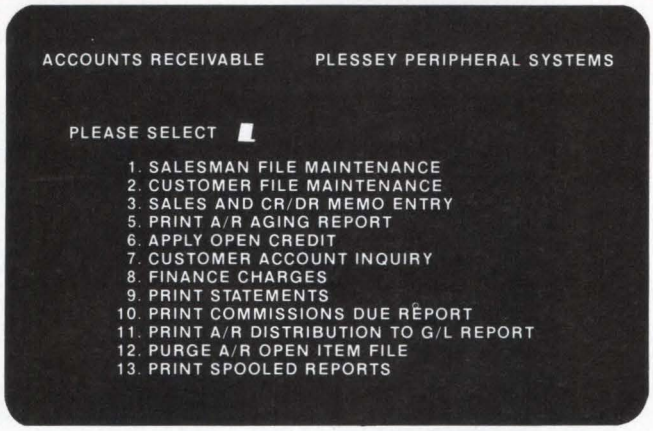

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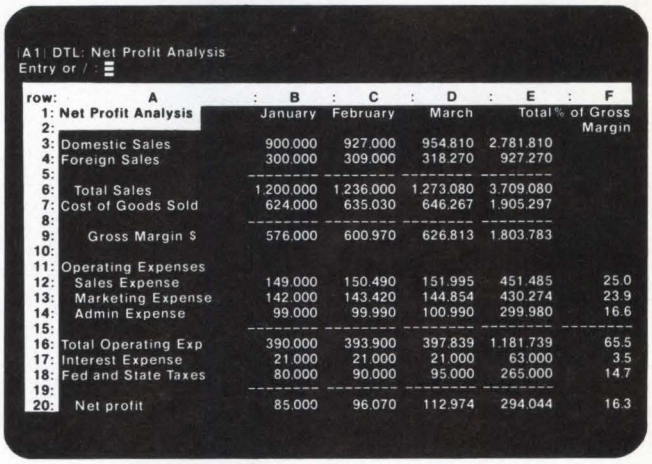
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1:	Net Profit Analysis	January	February	March	Total	% of Gross Margin
2:						
3:	Domestic Sales	900.000	927.000	954.810	2.781.810	
4:	Foreign Sales	300.000	309.000	318.270	927.270	
5:						
6:	Total Sales	1.200.000	1.236.000	1.273.080	3.709.080	
7:	Cost of Goods Sold	624.000	635.030	646.267	1.905.297	
8:						
9:	Gross Margin $	576.000	600.970	626.813	1.803.783	
10:						
11:	Operating Expenses					
12:	Sales Expense	149.000	150.490	151.995	451.485	25.0
13:	Marketing Expense	142.000	143.420	144.854	430.274	23.9
14:	Admin Expense	99.000	99.990	100.990	299.980	16.6
15:						
16:	Total Operating Exp	390.000	393.900	397.839	1.181.739	65.5
17:	Interest Expense	21.000	21.000	21.000	63.000	3.5
18:	Fed and State Taxes	80.000	90.000	95.000	265.000	14.7
19:						
20:	Net profit	85.000	96.070	112.974	294.044	16.3

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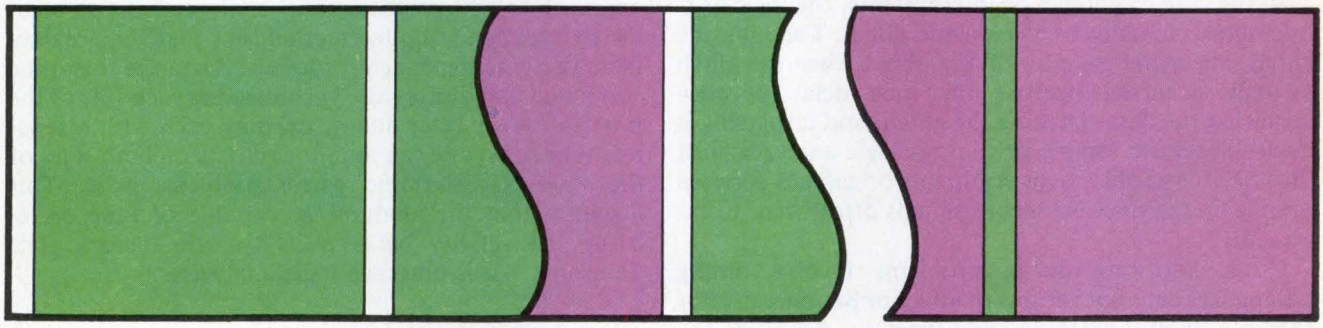
CIRCLE 101

TIME AFTER TIME, LOGIC ANALYZERS GET THE JOB DONE

Dual timebase logic analyzers enable designers to debug as never before—providing, of course, that the right triggers are pulled.



by Sandra Jumonville

Most logic analyzers to date have been designed as data acquisition rather than data analysis tools. To make debugging easier, modern logic analyzers offer faster acquisition speeds, more channels, larger memory, and a better human interface. Unfortunately, while laudable, this is far from what is needed to solve today's complex design problems. Pattern generation, for instance, can also be a very useful tool to provide the engineer with more control and modeling of both the design and debug of the system.

Software is an increasingly important part of the design effort. Luckily, the modern logic analyzer is finally addressing software debug issues by offering mnemonic disassembly of processors, extensive data qualification, and sophisticated triggering that facilitates tracking program flow. Most recently, the logic analyzer has joined with the development system to offer support of both design and debug exercises. However, neither system hardware nor software functions are autonomous. The system integration process brings together these two design phases. Solving the complex problems that appear during system integration consumes enormous amounts of design time.

If the logic analyzer really "analyzed" during the system integration process, then the integration phase would be far less time-consuming. It is in this area that the logic analyzer can be improved.

Hardware debug demands bandwidth

Regardless of which technology is chosen, there are two generic problems related to hardware design: parametric and functional. Parametric problems deal with specification tolerance such as threshold sensitivity, operational temperature, transient rise and fall times, and setup and hold times. Functional problems deal with performance and include faulty components, high

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frequency noise, ground planes, circuit loading, propagation delays, and component operational characteristics that differ from vendor specifications. The intricacy of hardware problems is a direct function of the types of components chosen. Often, the hardest problems to isolate are combinations of parametric and functional flaws.

A typical hardware design problem might arise from combining standard transistor-transistor logic (TTL) components and 100k series emitter-coupled logic (ECL). Vendors specify minimum and maximum operating voltages for both parts' families, yet in reality, such parts do not always operate at specified limits. The hardware engineer is concerned with sensitivity to different threshold voltages, but he must also take into account operating temperatures and resultant speed differences.

To aid the design effort, a logic analyzer needs sufficient resolution to monitor ECL-type components. It must also provide auto update of the display for monitoring realtime activity. This allows threshold sensitivity checks to be performed on multiple components. Since ECL parts are specified in nanoseconds, a designer will not be able to detect high speed timing errors or high frequency race conditions if the logic analyzer is a 50-MHz type.

In the case of glitches or intermittents, the logic analyzer must actually trigger on the glitch. Latching the glitch into memory tells nothing about when the glitch actually occurred because the time delay between acquiring the data, latching the glitch, and displaying it could be several sample periods. A logic analyzer must thus be able to observe intermittents or glitches between sample clocks since erroneous signals often occur unexpectedly.

Other hardware debug problems involve timing parameters between various modules or peripherals. For example, typical machine cycle times for Schottky TTL parts are around 40 ns. This is slow compared with the machine cycle time of the microcode in a mainframe central processing unit (CPU), which is approximately 8 ns. But stepper motors for line printers can be as slow as one revolution per second. Accommodating this range of timing problems need not require a specialized test equipment array. One good logic analyzer can do it all.

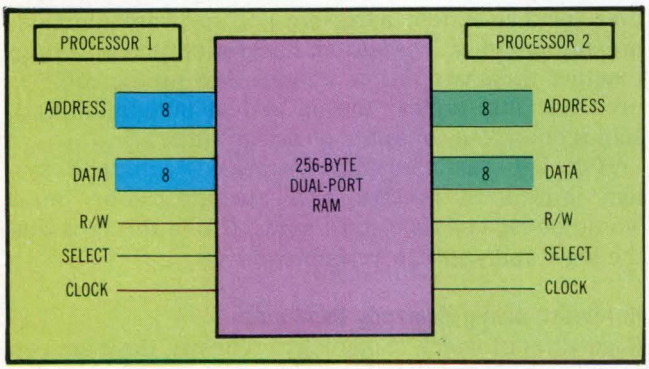

Fig 1 Dual-port RAM is a source of logic timing problems. These are most expeditiously unraveled by a dual timebase analyzer. By observing each side of the RAM independently and time correlating the results, premature read/write cycles can be exposed.

A logic analyzer needs sufficient resolution to monitor ECL-type components.

The dual-port random access memory (RAM), when used as an interprocessor communication device, is a good example of a timing problem source. (See Fig 1.) If data contents are incorrect, it can be assumed that the RAM was being read too soon by one of the processors.

It would be tedious to isolate the problem if a traditional logic analyzer were used because one would have to logically OR the two processor clocks, then AND them with the OR of the two select lines. One would have to be assured that the clock edges were far enough apart (within the sampling resolution of the logic analyzer) to sample them correctly. If "select" is high on one processor and the other clock gets an edge, then the data acquired are invalid. In any case, getting the right data to analyze can prove difficult. Most crucial is the timing of the two ports. Since this clocking scheme does not guarantee when events actually occur, it is not very useful for timing analysis.

Using a dual timebase logic analyzer is a better approach to this problem. This analyzer has two completely separate sampling mechanisms that acquire data from two interdependent processes. Data are then time correlated and displayed. By connecting each side of the RAM to the analyzer and associating each with a separate time base, one can monitor activity on both sides of the RAM to determine where problems exist. This demands that the analyzer be capable of time correlating the activity between its two time bases. The Tektronix 1240 is one such logic analyzer.

Software debug

Lack of prototype hardware often hampers software debugging. In this case, the same computer is used for both writing and debugging the code. A major problem is that not all the support tools (eg, emulators) are available for the processors being used. To run software, for the most part, integrated development systems and large host computers are and will continue to be used.

Standalone logic analyzers do have some of the features required to debug code, such as data qualification, sophisticated triggering, and range recognition. But most logic analyzers do not have enough memory to accommodate several routines, symbolic debug, and general purpose fetch prediction. Logic analyzers must ultimately address these issues to be useful for software design.

Software debug problems usually result from inefficient coding, overwriting of the stack, misplaced pointers, improper use of program variables, and unpredictable software interaction with the hardware. A classic example of a software problem is depicted in Fig 2. Here, a typical processor stack is divided into frames. The frame pointer points to the subroutine return address currently being executed. The stack pointer points to the location that contains the subroutine variables. If the stack is pushed, the last

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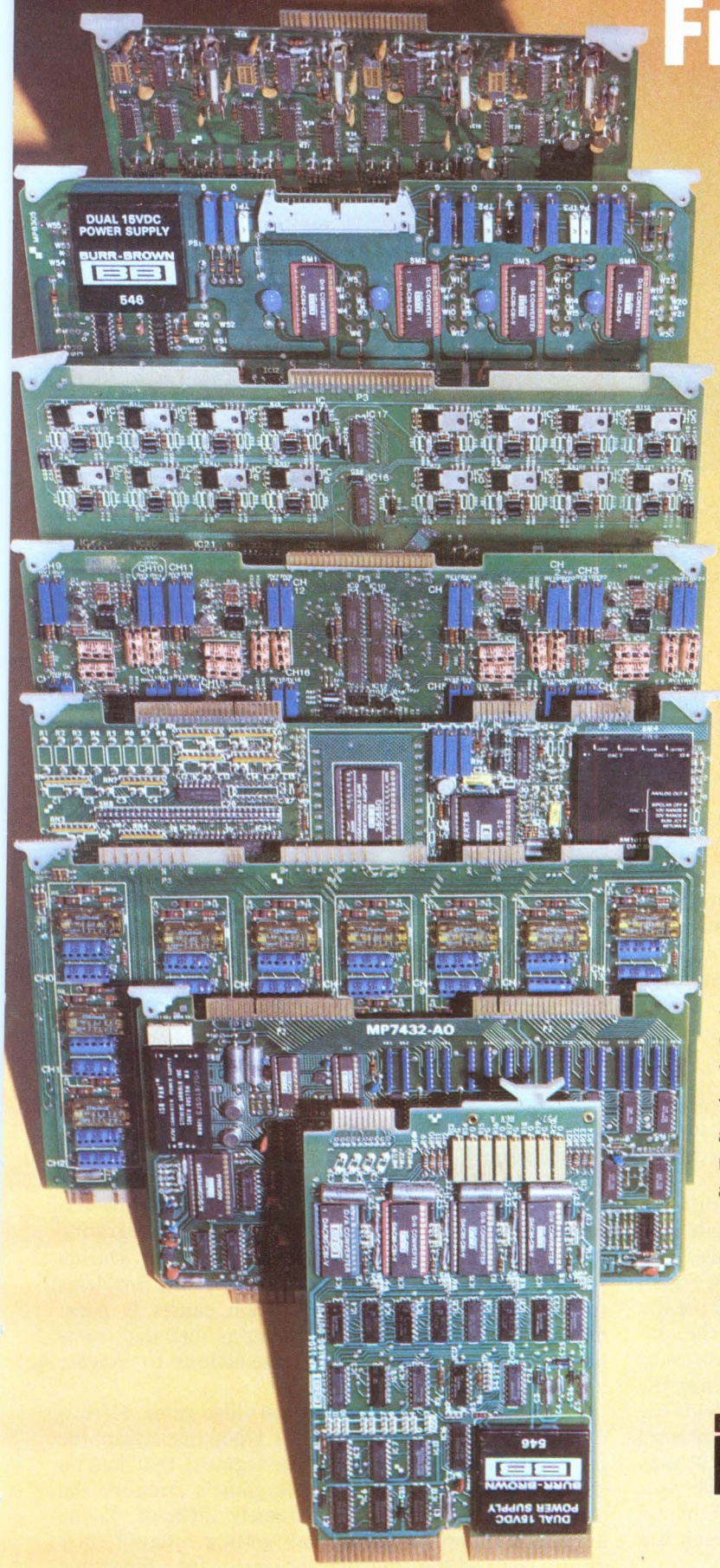

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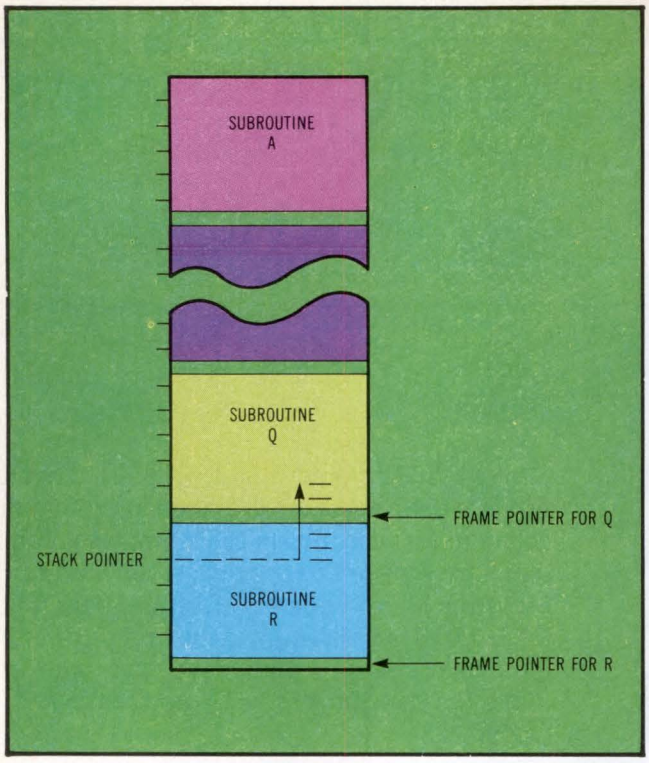

Fig 2 Software debugging often centers around the stack. Here subroutine A calls Q which, in turn, calls R. If Q pushes the stack too often, the stack pointer will be overwritten and the return address lost. By observing the pointer status during subroutine execution, the logic analyzer can aid in detecting overwrite.

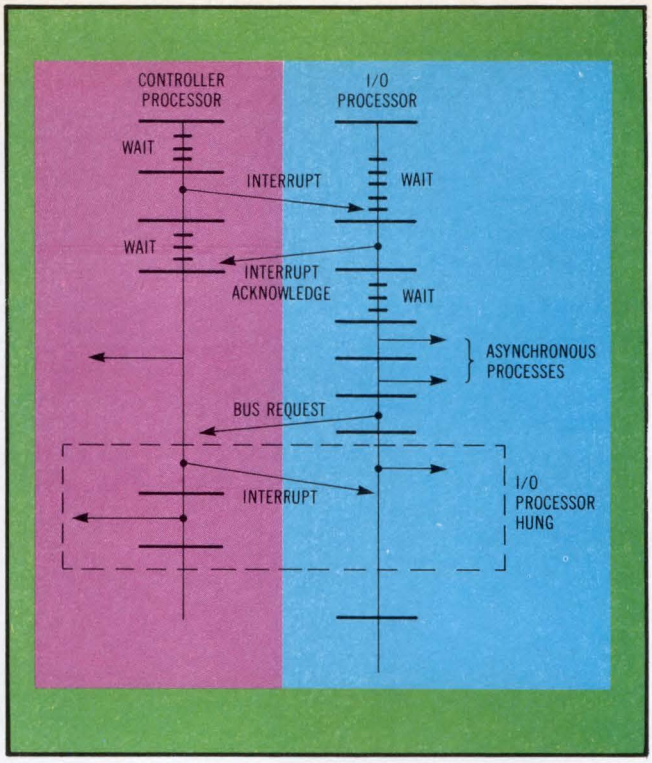

Fig 3 Interrupt cycle problems between processors can be easily detected with a dual timebase analyzer. By tracking address, data, and control lines of both processors via independent triggering (Ping-Pong), interprocessor timing subtleties become obvious. Processor efficiency, or lack of it, is also painfully clear.

location that had subroutine variables in it is overwritten (a normal procedure). However, if the stack is popped too many times when a subroutine is executing, the stack pointer will be located above the frame pointer. Then, the subroutine cannot return to the main program because the return address has been overwritten.

In the stack of Fig 2, subroutine A calls subroutine Q which, in turn, calls subroutine R. During the execution of Q, the stack is popped too many times. Q calls R, which executes and returns to Q when it is finished. However, Q cannot return to A because the return address was lost when the stack was popped. Using a logic analyzer, debugging this problem can be accomplished by waiting for a call to the particular subroutine in question. Then, the analyzer can be triggered on a write instruction to the frame pointer location.

Another typical software problem, yet more difficult to solve, is the monitoring of a simple read/write process such as an interrupt cycle between a controller processor and an input/output processor (IOP). (See Fig 3.) The controller processor asserts an interrupt and the IOP responds with an interrupt acknowledge. While the controller processor has the bus, the IOP continues processing on its asynchronous bus while continuously polling the central bus to see if there are more data available. If the IOP requests a bus grant and then continues to process before the CPU returns the handshake, the IOP may erroneously conclude that it has control of the bus. Obviously, it does not. The CPU can interrupt again and the IOP will never know what happened. The result is a hung processor.

A dual timebase logic analyzer provides the best debugging solution for this situation. With such an analyzer, all the address, data, and control lines for both processors can be monitored. By creating a trigger condition that follows both processes and tracks back and forth between time bases ("Ping-Pong triggering"), data can be acquired and observed in a time-correlated manner. Some very interesting graphics can be generated using performance analysis on this data. Performance analysis provides statistical information on the amount of time each device spends processing or stuck in wait states.

System integration

In any project, system integration consumes the majority of time. Designs are becoming so complex that they must be subdivided into functional blocks. While this simplifies debugging individual modules, integrating those functional blocks becomes more difficult. During system integration, when the most difficult problems surface, quickly identifying problem causes is paramount. Is the code not performing as intended, or is hardware timing off, causing instructions to execute improperly?

As an example, consider a typical video game. Here, a CPU drives a video controller chip. Upon inspection, the game display might reveal a line segment that has no data. Determining where in the game's circuitry the problem originates can be extremely difficult. Is the horizontal ramp to the display getting intermittently destroyed? Did the controller processor send the wrong

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Figure 1
Logic Cell Usage

Function	Cells
Independent Inverter	⅓
Two-input NAND or NOR	⅔
Three-input NAND or NOR	1
Two independent Inverters	1
Three parallel Inverters	1
Two-to-one MUX	1
Two-input NAND plus Inverter	1
Four-input plus two-input NAND	2
XOR	2
Transparent Latch with clear	2
Shift Register bit with clear	2
Analog Comparator	3
Four-to-one MUX	3
Static Shift Register bit with clear	4
D-type Flip-Flop with set or clear	4
JK-type Flip-Flop	6
Three-to-eight Binary Decoder	10
Sixteen-to-one MUX	16
Four-bit Adder with carry out	28
Static FIFO, m wide and n deep	(2m + 9)n
Four-bit synchronous, cascadable, up/down, binary Counter with parallel load and asynchronous clear	38

INTERFACE CONSIDERATIONS

On the G70250 you may have any number of interface signals up to a maximum of 40, including power and ground. Just one power pin and one ground pin are usually needed. At 5.0 Volts, the typical quiescent supply current for the G70250 with outputs unloaded is only 10 microamperes. Active circuit power dissipation will depend on the particular logic implemented and on the operating conditions used. With representative logic running at 20MHz, supply current will be about five milliamperes.

As many as 36 of the chip interface signals can be outputs, each of which can drive up to 10 'LSTTL loads. Contained within each interface cell is all the circuitry needed to handle input protection, level shifting, output fan up, output drive, bare drain configurations and tri-state buffers. Interface buffer transistors can also be used to make good analog switches. Interface pads are undedicated and each may be power or ground or output or input or bidirectional.

LOGIC SPEEDS

The curves in Figure Two show the worst-case speeds for an inverter and a two-input NAND gate. For typical layouts and logic configurations, including wiring between nodes, a gate sees a fanout load of three. Critical logic paths can be enhanced by decreasing the wiring and logic loading and by careful use of extra cell transistors to improve internal gate drive without adding logic levels. Supply voltages up to ten Volts may be used and will significantly increase logic speed. The propagation delay values in Figure Two are characterized for these conditions:

- Input transitions of two ns
- Average of both transition directions
- Measured at 50% points of the waveforms
- Ambient temperature of +70°C
- Power supply of 4.75 Volts
- Worst-case processing parameters

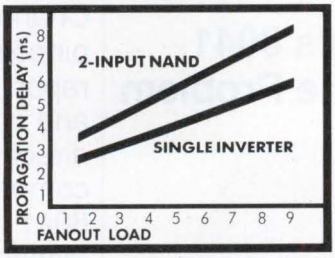

Figure 2
Propagation Delay vs. Loads

INTERFACE SPEEDS

Figure Three shows the worst-case propagation delays and transition times of a single output buffer. Even loaded with 10 'LSTTL loads plus 50 pF, the buffers are quite fast. For heavier DC or capacitive loads where speeds are important, driver transistors may be connected in parallel on the chip.

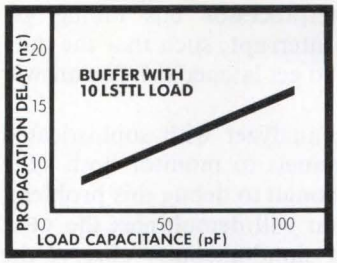

Figure 3
Propagation Delay vs. Capacitive Load

PACKAGES

Many packages are available to accommodate your interface signal needs. The G70250 chip will fit in standard narrow dual in-line packages like those of 20 pins and less. DIPs up to 40 pins may be appropriate in your application. For situations where space is at a premium, a small Leadless Chip Carrier or Pin Grid package might be chosen. We will work with you to define the package best suited to your needs.

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DEVELOPMENT INTERFACE

There are many ways you can interface with us to accomplish the development of your particular logic solution. We have implemented more than 650 arrays since we started in 1974 and our experience indicates that it is usually best for us to do all the development engineering with your original logic drawing and test vectors as the starting point. We normally take full responsibility for the complete chip development from your specifications. If you give us:

- the final functional logic drawing in your format
- test vectors and a timing diagram
- operating environment and package specifications;

Then in three to five weeks we will give you:

- the package pin assignments
- the converted physical logic drawing
- critical path simulation results
- the layout verification net list

Two to three weeks later, we will send you 50 packaged and tested parts for your approval. We are then ready for your production order.

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At International Microcircuits we use several computer tools and programs during development and at each step we always keep experienced designers in the loop. Compared to so-called fully automatic layout, this gives us some key advantages:

- Better control over chip performance
- Higher gate utilization
- Smaller chips
- Lower production prices

This approach is only viable with the independent layout verification provided by our software tools. Our present hardware setup includes an Applicon 860 graphics system supporting several design terminals, a sophisticated CAE workstation for schematic capture and simulation, plus a VAX II/750 system running a variety of software for layout, checking, simulation and verification.

DEVELOPMENT PRICING

For a full development cycle on the G70250, where we undertake responsibility for the chip circuitry and performance and layout, the total non-recurring charges are $18,500 for commercial products. This figure includes test program development and prototype parts as well as all chip development engineering, computer time, tooling and fabrication. We will be glad to provide a detailed development quote for your particular application and for other chip sizes.

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Production prices depend on several factors, including packaging, order volume, screening specifications, operating environment and speed requirements. Each chip is unique and has only one customer. Thus, for your individual part, the experience curve that associates declining production costs with rising accumulated volumes is driven by your orders alone. We price accordingly with steps that provide ongoing price decreases with accumulated total volume over time.

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CIRCLE 103

It is technically impossible for one individual to be an expert in all areas of design.

information? Did the interprocessor bus timing get delayed in response to an interrupt, such that the data were not held long enough to get latched in? The answer could be any of these.

A single timebase logic analyzer with sophisticated triggering and enough channels to monitor both state and timing signals is not enough to debug this problem. An analyzer is required that will demultiplex the CPU; monitor handshaking; and simultaneously observe the vertical, horizontal, synchronous, and pixel data. A dual timebase logic analyzer can accomplish these diverse tasks with ease.

Why is logic analysis the best tool?

Projects today are so complex that it is technically impossible for one individual to be an expert in all areas of design. Design must therefore be divided into hardware and software tasks, then subdivided into functional blocks, making total design a team effort. This process demands high-tech tools as well as talents. It is not cost-effective to have many separate tools for each engineer. A logic analyzer is the one tool that meets the high performance criteria and can be used for most tasks by all of the design team members.

Good logic analyzers with an adaptable human interface and the sophistication to solve complex problems can be extended to areas such as manufacturing and service. Since test technicians must often perform the same tests as engineers, the mass storage of logic analyzer setups and reference memory are extremely helpful. The same options are of value to service teams. In addition, the added ability to communicate remotely can greatly facilitate their roles. Finally, in addition to the technical features outlined, good logic analyzers must be portable for those times when the technical mountain will not come to the engineering Muhammed.

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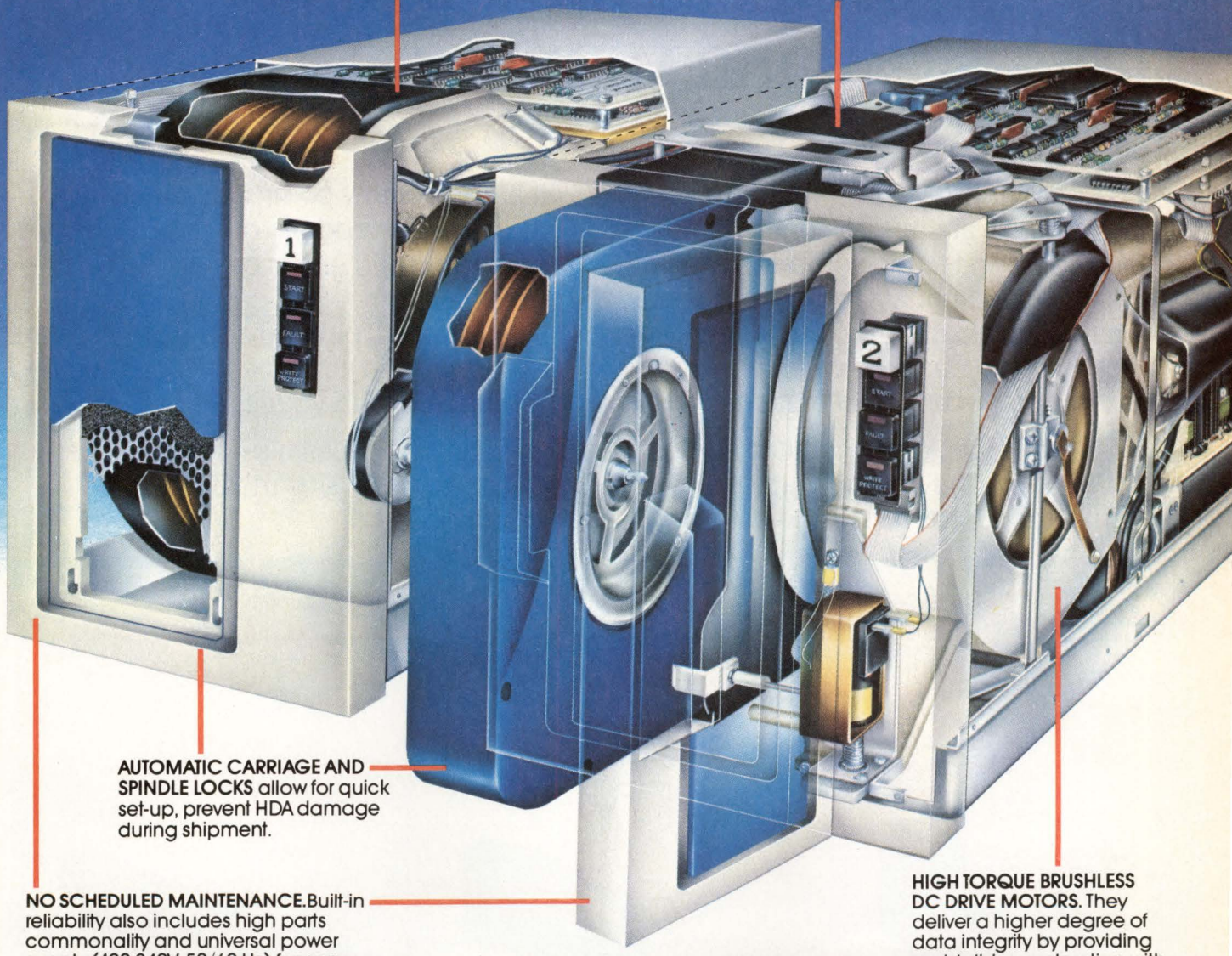

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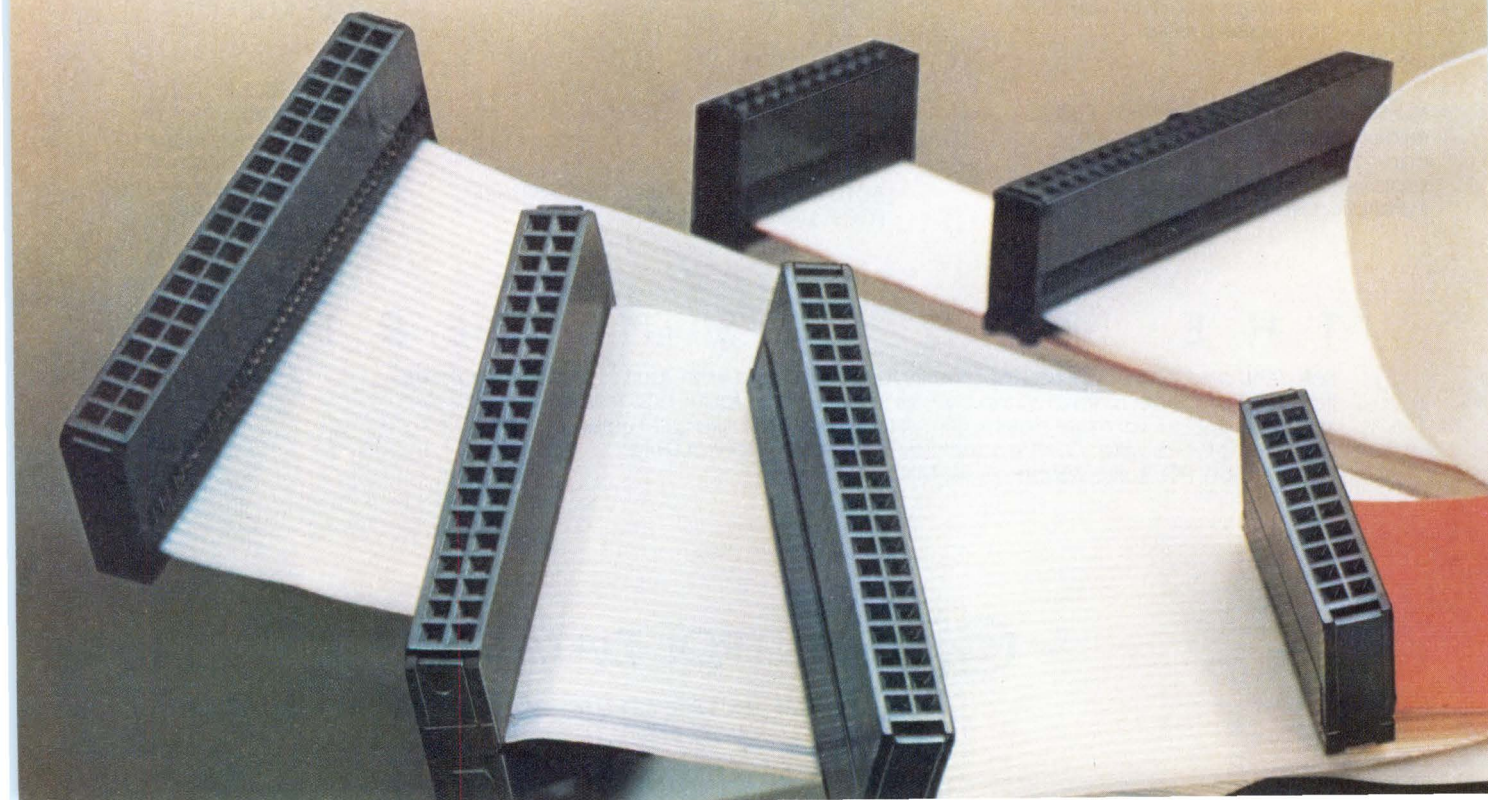

AMP Facts

Typical Mechanical/Electrical/ Environmental Properties

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Mating Force	8 oz. max./contact
Unmating Force	1½ oz. min./contact
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Vibration	15 G's, 10-2000 Hz
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Contact Resistance	25 milliohms max.
Insulation Resistance	5000 megohms min.
Dielectric Withstanding Voltage	500 volts RMS (sea level)

Environmental

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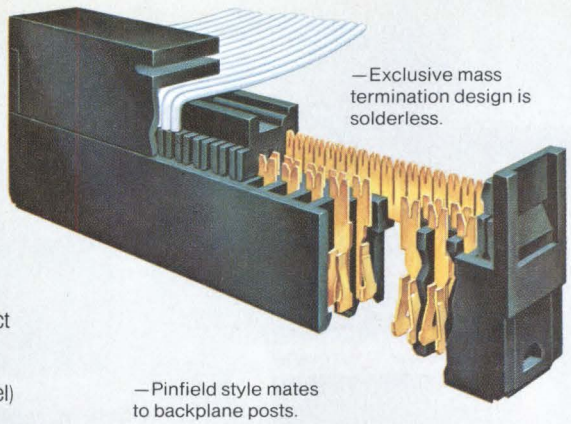
Thermal Shock	5 cycles: —65°C to 105°C
Moisture Resistance	10 days, 25°C to 65°C, 80-98% R.H.
Salt Spray	5% solution, 48 hours
Industrial Gas	10% SO_2, 24 hours



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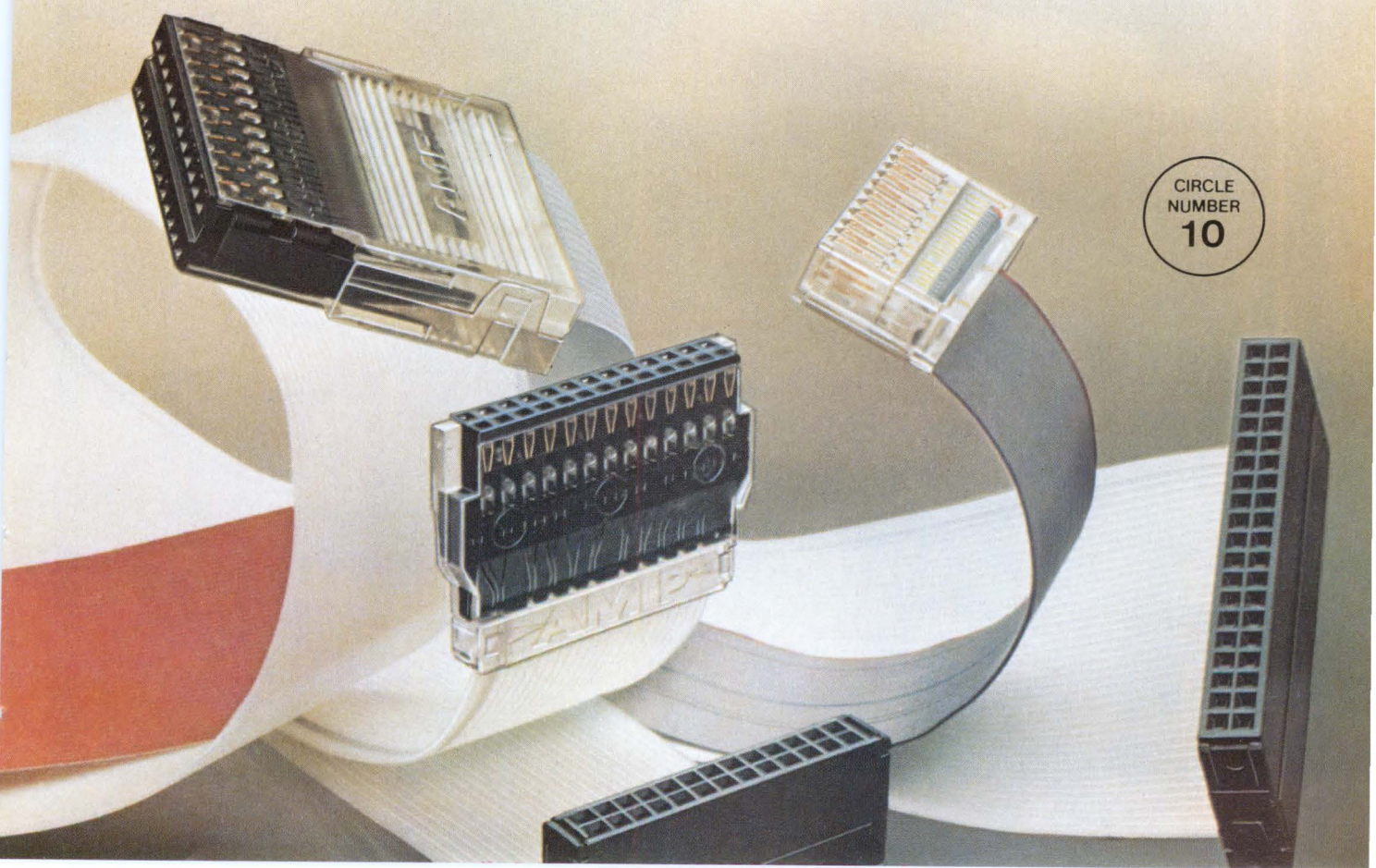

CIRCLE NUMBER 10


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CIRCLE 107

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CIRCLE 108

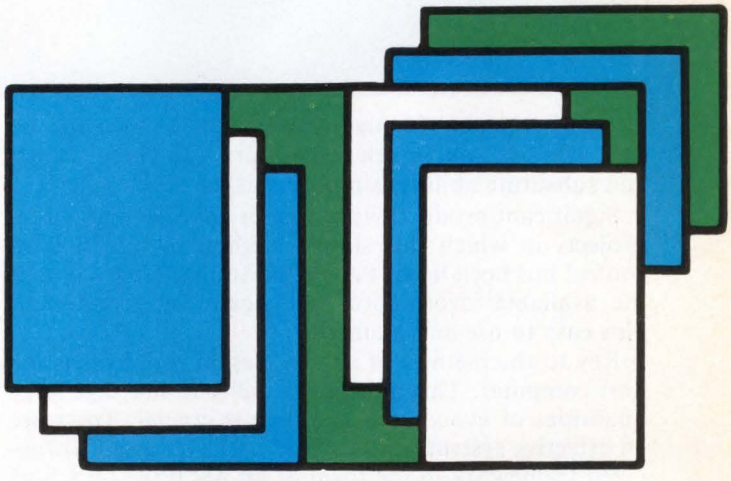
AN INFORMATION MANAGEMENT TOOL FOR SYSTEM DESIGNERS

There is no reason why computer based information system designers must be the last to incorporate productivity enhancers into their professional lives. The system described proves just that.

by Joseph F. Blazewicz

In the earliest stages of microcomputer based system design, the designer is encumbered with reams of information. End-user requirements, system variables, hardware alternatives, speed, memory criteria, costs, and schedules are all factors to be reckoned with early in the system design. The system designer's first job is to organize this information, then communicate it as needed to all engineers and managers involved in the project.

A system design tool, built around a core of information common to most facets of microprocessor based designs, easily facilitates this process. If the information core is faithfully maintained as an American National Standard Code for Information Interchange (ASCII) data file, a series of data flow diagrams and reports can be readily generated. Further, this development aid is a project organization tool used and created predominantly by the system designer. It guides software designers in the first 30% to 40% of a project's lifetime. After this, depending on further technical developments, the data files and flow diagrams can be frozen or updated. The data file can be continually sorted and recombined to provide reports needed by project personnel. In the system described, such a file based development aid is implemented with a single command to the computer, giving the designer access to any of five reports from the information core file.



These reports consist of a project status report, a file sorted list, a memory type sorted list, the executive task sequencing requirements, and a runtime estimate report. The ease with which these reports are created ensures that accurate information is instantly available. In addition, telephone modem connections to local terminals supply customers and subcontractors with the same information.

After the developing data file has reached maturity, program design language (PDL) tools using the data file mnemonics structure the next stage of project development.

Joseph F. Blazewicz is a senior microprocessor system designer at General Electric's Simulation and Control Systems Dept, 1800 Volusia Ave, Daytona Beach, FL 32015. He is currently involved in applying microprocessors to robotic vision and energy control systems. Mr Blazewicz has a BSEE from the New Jersey Institute of Technology and an MSE from the University of Pennsylvania.

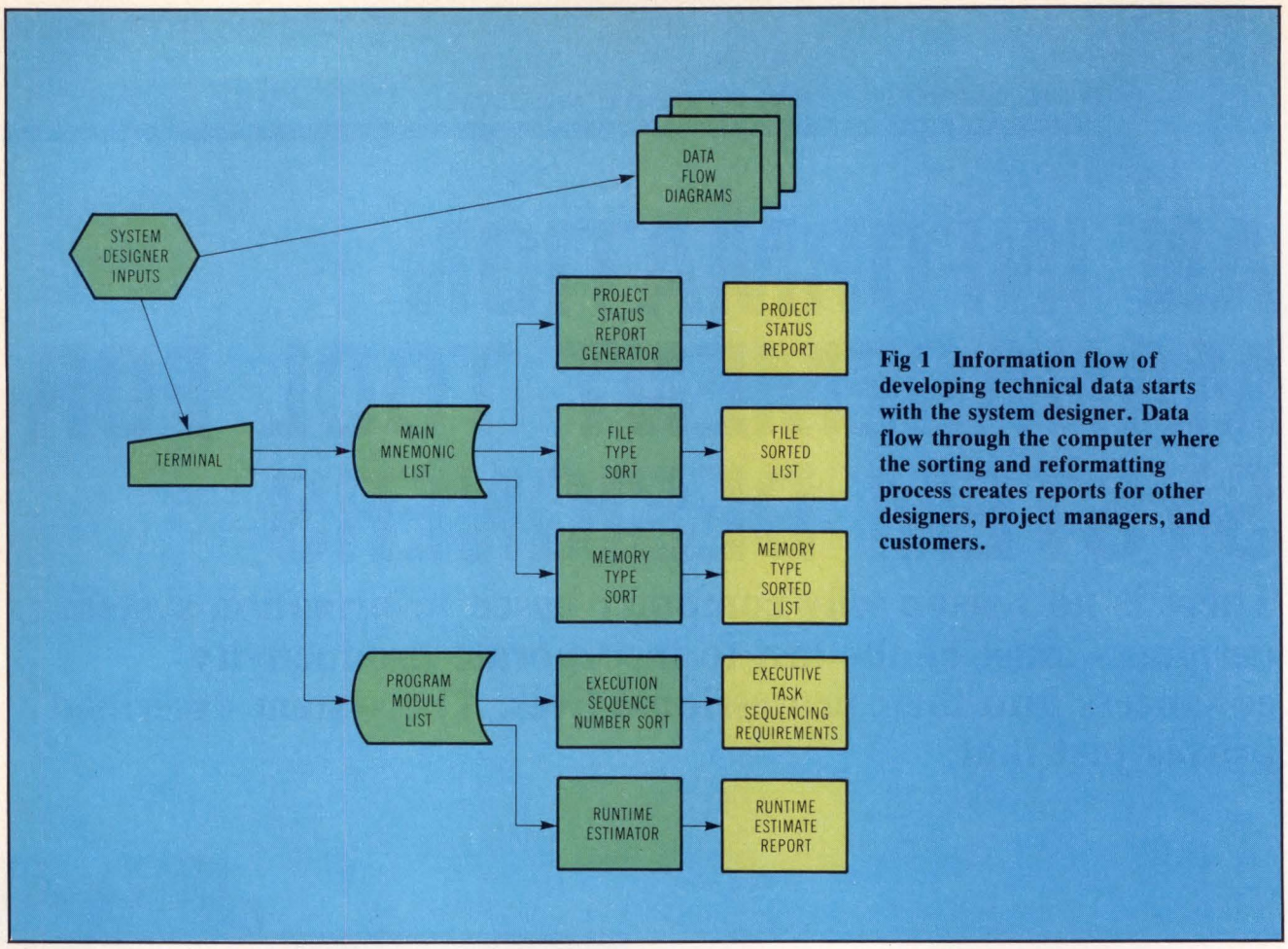


Fig 1 Information flow of developing technical data starts with the system designer. Data flow through the computer where the sorting and reformatting process creates reports for other designers, project managers, and customers.

PDL development frequently leads to revision of the core data file, and screen text editors with global search and substitute abilities simplify further development.

Significant productivity increases have been noted on projects in which this simple method of information control has been used. Project personnel often say that the available information is logically interconnected, plus easy to use and maintain.

Key to the method of solving design problems is the host computer. This machine's ability to massage large quantities of evolving design data is crucial. To create an effective system, the designer needs a logically organized framework in the form of an ASCII file on a host computer. As additional information develops, this framework fills with data, and the file's overall structure iteratively changes to accommodate new developments. A data flow diagram is developed and maintained parallel to the core file development. This diagram gives visibility to the development process and is a convenient key to point to groups of framework entries in the core file.

An overview of the methodology is shown in Fig 1. Within the host computer, the system designer uses a text editor to construct tabular listings that define the framework in which developing project information is stored. Two 132-character tabular listings—the main mnemonic list and the program module list—form the heart of the system.

Experience with the system has shown that the listings develop most rapidly when certain stipulations are met. First, the system designer must have a cathode ray tube terminal located at his or her work area. Next, the text editor (screen type) must permit rapid, simple global searches, preferably using special function keys. Finally, the host computer must provide many conveniently located terminals for project personnel to use. This last stipulation, the provision of many terminals, often spawns arguments from cost-conscious purchasing directors. A convincing argument can be made for the purchase of terminals, however, if hidden project costs are exposed.

With enough terminals, that unwelcome task . . . the meeting, is not required as often . . .

There are many sources of hidden costs. One is the need for frequent printouts of developing data in the absence of terminals. With a sufficient number of terminals, printouts are practically eliminated. Another hidden cost is the time spent shuffling through printouts and doing visual searches. Screen text editors save large amounts of time in small increments. Further, with terminals, the files are always at the latest stage of development, so other employees can access the files as needed. More money is wasted using central, marked-up documents that require employees to constantly recheck for the latest information. With enough terminals, that unwelcome task of all project managers, the meeting, is not required as often since 2-way verbal communication is minimized.

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CIRCLE 109

From theory to reality

The system discussed here uses a VAX 11/780 computer, which services other nondesign projects within the facility. In addition, a DEC EDT screen type editor is used because it requires minimal operator training. Almost like a word processor, this editor provides powerful file merging and global editing commands that are easily grasped by nonprogrammers and can also be taught to employees unfamiliar with computer programming. DEC VT100 terminals or similar units are sufficient for the purposes of file maintenance.

Data flow diagrams of the microbased design are drawn parallel to the developing files and provide project workers the visibility they need in the developing design. The five report types shown in Fig 1 are created automatically by the system. These reports are created by using a resident VAX sorter program that sorts tabular lists via simple 1-line commands. The file sorted list, memory type sorted list, and executive task sequencing requirements reports are each created with a single command to the VAX sorter program. Project status and runtime estimate reports are created by simple FORTRAN routines. These routines extract information from the tabular main mnemonic list and program module lists and calculate sum totals of parts of the lists.

The data flow diagrams . . . are a roadmap to the evolving system.

Data flow diagrams of the developing project are valuable in providing project development visibility. The worth of these diagrams is evident during design reviews, customer subcontract communications, assignment of development tasks, and training of new developers and users. During design reviews, action items can be keyed to the diagrams' serialized blocks.

The data flow diagrams, similar to hierarchical input/process/output (HIPO) diagrams, are a roadmap to the evolving system and can be developed and maintained by employees with either hardware or software backgrounds. The diagrams fall into two categories: major data flow paths and multiple use modules.

Fig 2, an example of a major data flow path, is typical of 10 to 40 pages of diagrams that can develop from

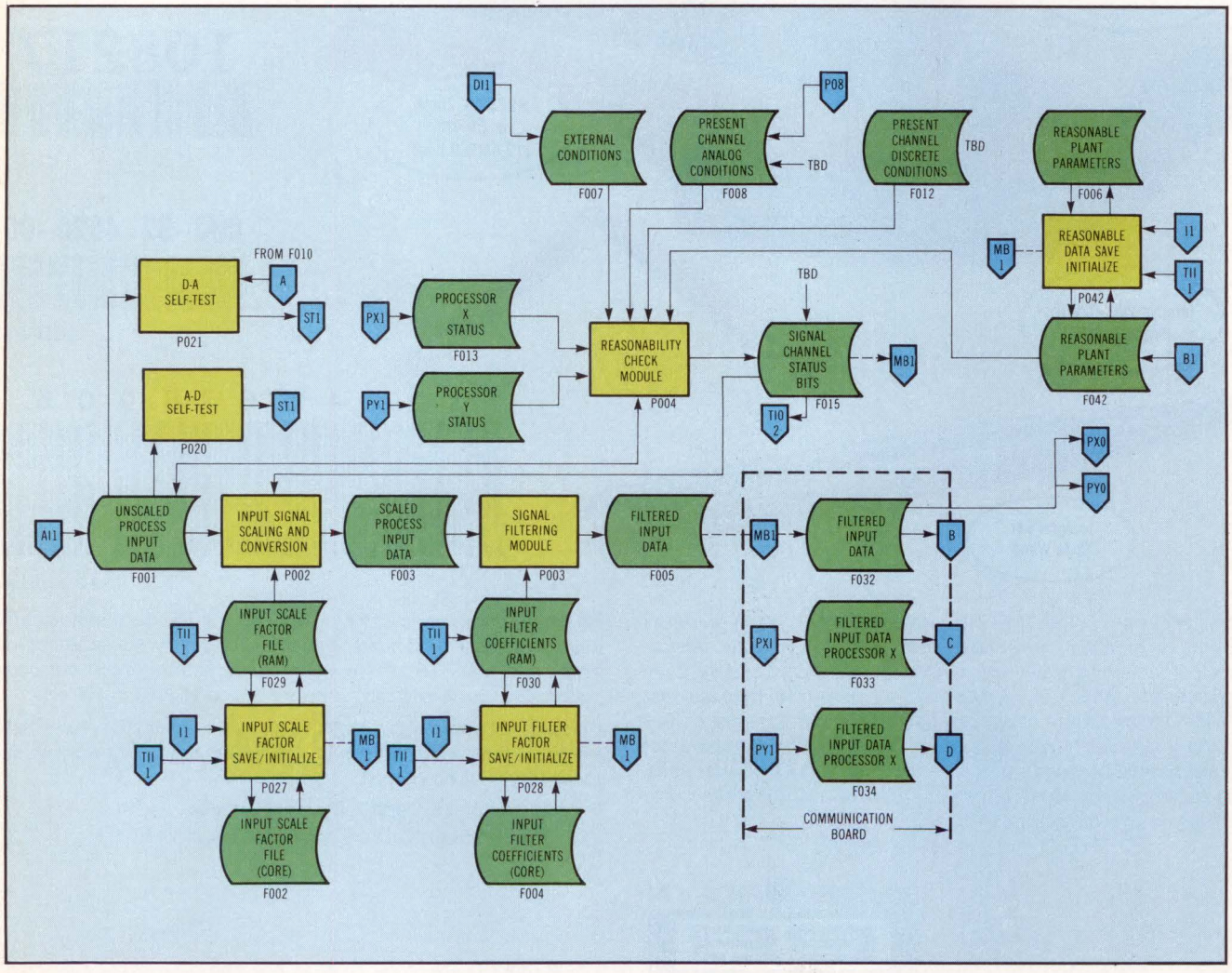
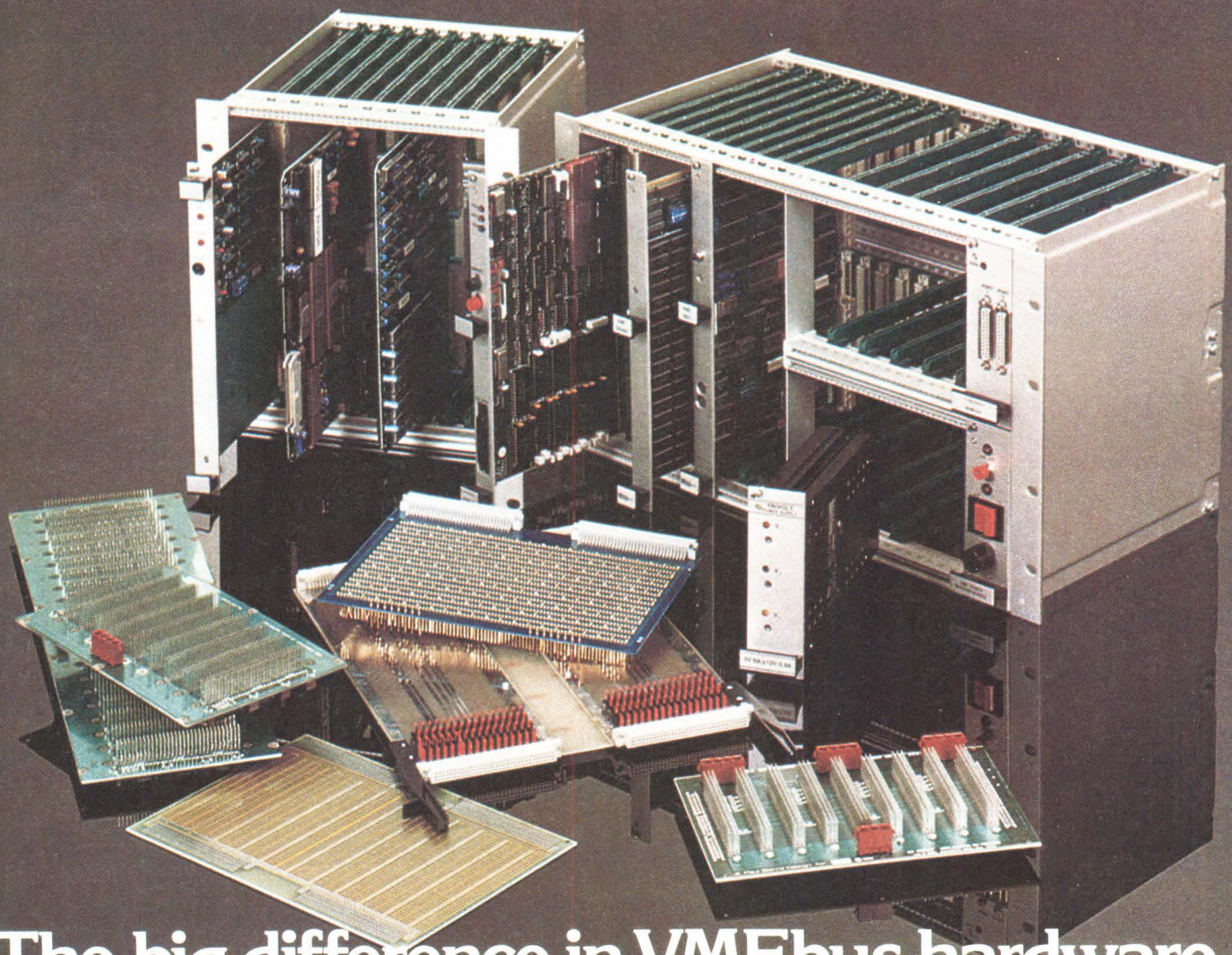


Fig 2 System data flow diagram provides visibility to the total system task and modularizes the effort to permit assigning development tasks. Note that interprocessor communications of specific files can be seen. Ten to 40 pages of such diagrams can develop on a medium-sized microcomputer application project.



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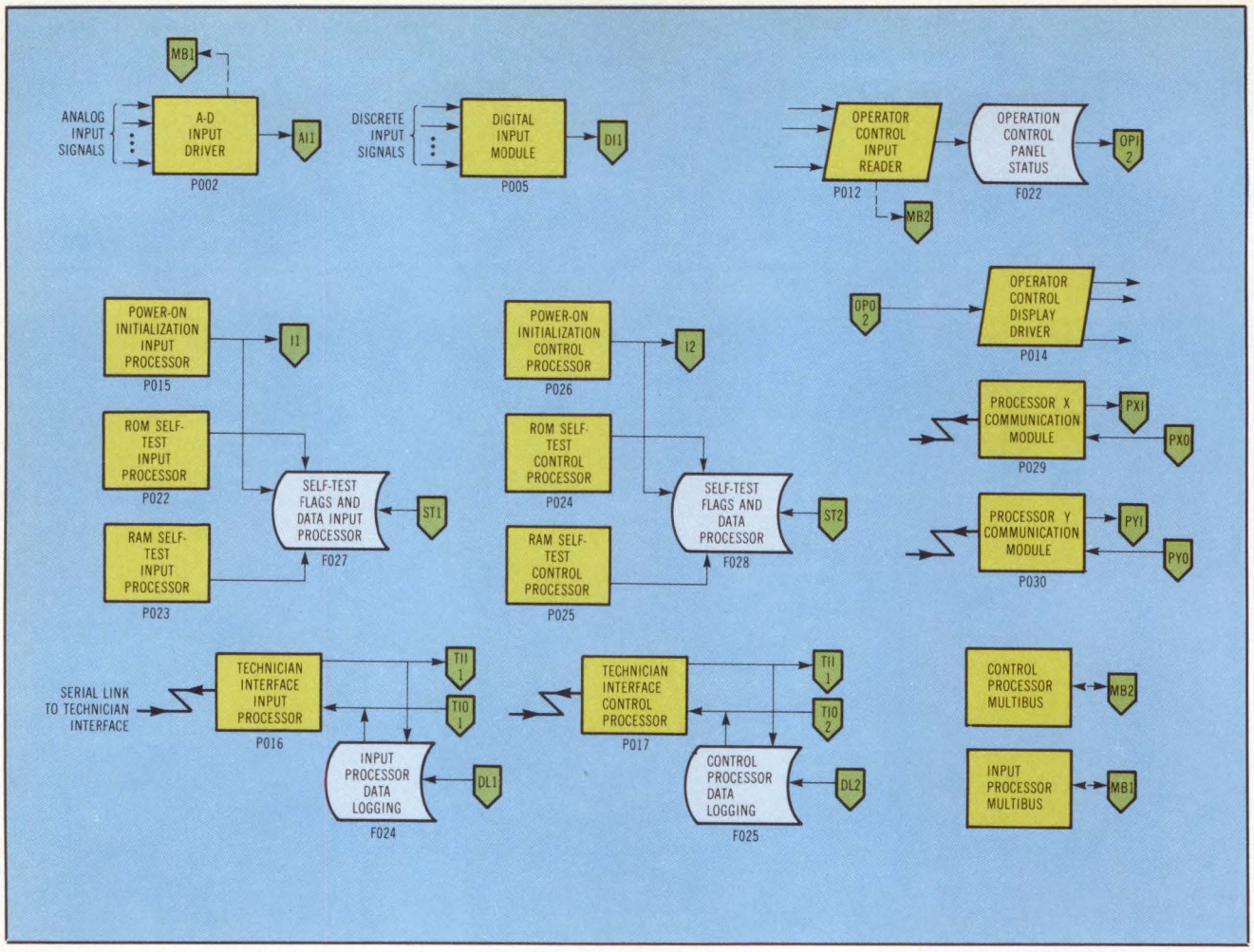

Fig 3 Recurring module notations simplify the system data flow diagram. Program modules or files that are accessed frequently by many parts of the system can be grouped together. Self-test result files, A-D input drivers and files, and bus communication link drivers are typical modules.

application efforts on a small- to medium-sized microprocessor. Most of the diagram is made using three symbols. The square boxes represent program modules that operate on data modules. The curved boxes represent data modules, and the offpage connectors (pentagons) represent connections to data paths on other sheets of the diagram. The solid and dashed lines between the modules indicate the direction of information flow between them.

If good data entry habits are established early, the information system is easy to maintain.

Program and data code that perform utility functions such as data conversion, hardware and software control, self-test routines, operator panel interface, bus communication, and data logging can be written as multi-user modules.

Both hardware and software data paths and connections are shown in Fig 2. Program modules that use common data buses and serial links are shown by off-page connectors and dashed lines. The MB1 and MB2 off-page connectors in Fig 3 are defined as data paths that require use of a Multibus portion of this particular design. Simple sums of columns in the data files, created later, are used to obtain bus loading analysis information to ensure that bus data transfer rates are not exceeded.

All program and data modules are arbitrarily serialized with PXXX and FXXX numbers as shown. These serial numbers are used in the data files to define specific details of these modules' contents.

F001 in Fig 2 is a data module that contains unscaled process input data. The information's source is the analog to digital (A-D) input driver module P002 in Fig 3. The Multibus is used for this data transfer. In Fig 2, the information in F001 is used by program module P021 for the digital to analog (D-A) self-test, and also for P020 (A-D self-test) and P002 (input signal scaling and conversion). Program module P002 uses the information in F001 and the input scale factor data in file F029. Files F029 and F030 are random access memory (RAM) files preliminarily loaded from core files F002 and F004 by program modules P027 and P028, respectively. The I1 off-page connector to Fig 3 shows that P027 and P028 are controlled by program module P015 as one of the microprocessor's power-on initialization operations.

As the design matures, several of the program modules are likely to require further refinements. For

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TABLE 1

Controller Variable/File/Module List

Computer Mnemonic	Math Symbol	Variable Description	Memory Type	Applicable Notes	File Storage Number	Bytes of Storage	Engineering Units
ADFLGi		A-D self-test flag i		004	F027		
ADRFLi		A-D converter bias reference		004	F001	2	
ADRFHi		A-D converter gain reference		004	F001	2	
AFILF1	AQQ1	Filter coefficient A steam flow	01		F004	4	
AFILF1	AQQ1	Filter coefficient A steam flow	02		F030	4	
AFILF2	AQQ2	Filter coefficient B steam flow	01		F004	4	
AFILF2	AQQ2	Filter coefficient B steam flow	02		F030	4	
AFILF3	AQQ3	Filter coefficient D steam flow	01		F004	4	
AFILF3	AQQ3	Filter coefficient D steam flow	02		F030	4	
AFILP1	AWE1	Filter coefficient A pressure	01		F004	4	0.321896

example, data module P004 (the reasonability check module) in Fig 3 needed a page of data flow diagram information to define data flow and interaction within itself. On first iterations of the design, data modules are assumed to be separate groups of memory. Further design developments and memory storage monitoring needs from the project status report and the file sorted list might dictate that files such as F001, F003, and F005 require overlaying of the same RAM area to keep the memory or design cost reasonable.

Diagrams assign development tasks. For example, software developers can be assigned specific program modules to develop with conventional programming flowcharts or PDL. These developments in turn are labeled with the serial number as a shorthand notation for indexing the developing documentation.

The computer mnemonic list

In parallel with the developing data flow diagrams of Figs 2 and 3, the main computer mnemonic list shown in Fig 1 is being developed as an ASCII data file. Table 1 is typical of a partially completed mnemonic list, sorted alphabetically by the name of the mnemonic to be used in the final assembly or higher level code. The eight columns represent typical design interests: mnemonic name, math symbol for equations, variable description, arbitrarily numbered memory type, applicable notes in a note file kept on the computer, data module serial numbers from the data flow diagrams of Figs 2 and 3, number of storage bytes for each mnemonic, and the mnemonic's engineering units range.

This file is created and maintained by a screen text editor. A small- to medium-sized design may require 10 to 20 pages of this file including 500 to 1000 variables. This file represents the basic framework into which developing information is deposited; software developers and users will employ it later for system maintenance.

As development continues, the list grows rapidly and the discipline required to maintain it is rewarded when the list is sorted and summarized by various support programs. Scanning the list for open entries in the various columns gives a preliminary indication of project design status. For example, with a single 1-line command to a system sorter routine, the file sorted list mentioned in Fig 1 is obtained. The result is that the main mnemonic list is sorted by file storage number (data module number), and within this number sort, each of the mnemonics is sorted alphabetically. As a result of this sort, all identical file storage numbers in the file storage number column of Table 1 are grouped together, and all computer mnemonics within the same grouping of a file number in the computer mnemonic column are alphabetically sorted. This sorted list now becomes a report that defines the contents of each of the file blocks or data modules shown in Figs 2 and 3.

Manually scanning this file sorted list and totaling the number of bytes in each file provides file size information. The system as implemented includes an automatic scan via a simple 27-line FORTRAN routine to supply this system sizing information.

Sorting Table 1 by memory type provides another useful report as a memory type sorted list. Typical memory types used on a controller project appear in Table 2. Sorting Table 1 by the applicable notes column produces a listing with all variables affected by specific notes grouped together. Notes are any information that must be keyed to specific variables. For example, the maximum rate of change of an input variable can be listed in a note at the end of the list.

TABLE 2

Project Memory Requirements Sorted According to Type

Memory Type No	Processor	Memory Description
01	Input	Core
02	Input	RAM
03	Input	ROM
04	Communications	RAM
05	Communications	ROM
06	Control	RAM
07	Control	ROM
08	Control	Battery backed up

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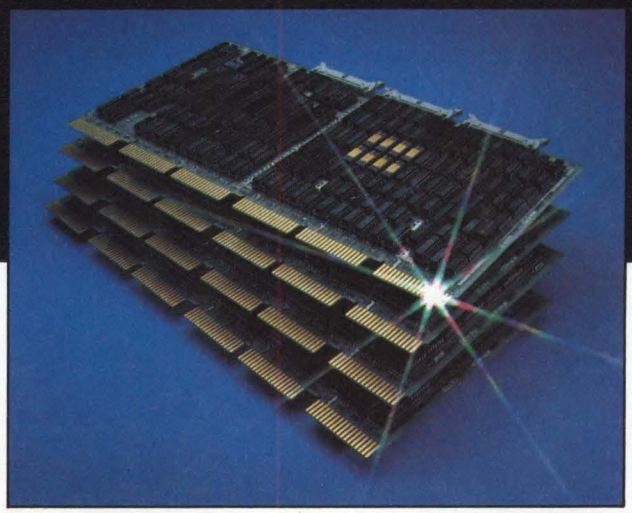

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CIRCLE 112

TABLE 3

Program Module List

Module Number	Program Module Name	Memory Type	Executive Task Number	Estimated Time (ms)	Actual Time (ms)	Storage Bytes	Module Folder	Buses Involved	Bus Loading Percentage
P001	A-D input selector	03	021	0.0001		00053	I0279	02	1.2
P002	Input signal select, convert, and scale	03		1.2000	1.563	01240	I1002	02	5.3
P003	Signal filtering module	03	023	11.8	14.7	00720	I2456		
P004	Reasonability check module			21.0	8.43		I2365	02	88.2
P004	Reasonability check module							01	12.3
P005	Process control discrete input module		035			00098			

Information concerning the program modules in Figs 2 and 3 is included in a computer file as shown in Table 3. The 10 columns of this program module list include a program module number, name, memory type in which the module is stored, executive task number assignment, and other, more specific information. In fact, all columns may not be applicable to each program module.

Sorting this list by executive task number provides a sequence of events list of module execution. Scanning that list for execution times allows the system designer to efficiently estimate the length of critical time paths in the design. Sorting the list by memory type allows a scan to be made that obtains memory storage requirements imposed by the program modules on the system's various memory types. This information is automatically included in a project status report and is useful to the hardware and software designers involved.

Finally, a global data module list is maintained that is used as a list of data modules within Figs 2 and 3. This list is primarily an index to the data flow diagrams and, when used with Table 1, gives the software designer the title of the module within which specific variables are stored.

After the basic lists and data flow diagram have matured, detailed design of the program modules can begin. This usually starts with a preliminary requirements text for each program module. A PDL processor is useful in these early stages to organize the developing text. Table 4 is an example of a PDL table of contents that is automatically created from Table 3's computer file.

TABLE 4

PDL Table of Contents

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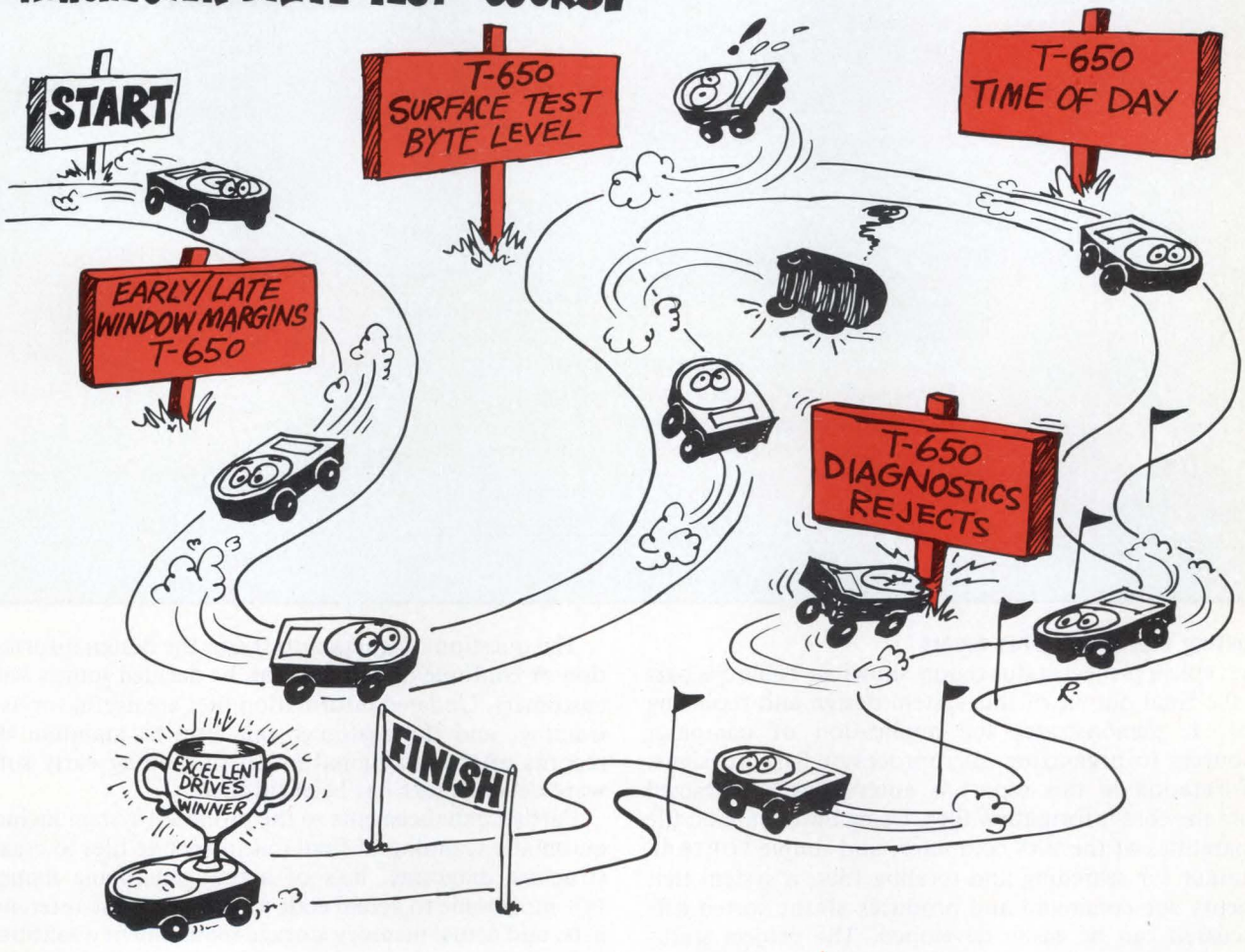

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CIRCLE 113

TABLE 5

Automated Project Status Report

System Variable Quantities

Total no of system variables 672
No of variables assigned to files.....249 (37%)
No of variables assigned to memory types.....185 (28%)
No of variables assigned to engineering units 48 (7%)

Assigned Data and Program Storage Requirements by Memory Type

Memory Type	Processor	Memory Description	Data Storage (No of bytes)	Program Storage (No of bytes)	Total No of bytes
01	Input	Core	280	782	1062
02	Input	RAM	2413		2413
03	Input	ROM		6320	6320
04	Communications	RAM	1220		1220
05	Communications	ROM		2137	2137
06	Control	ROM	470		470
07	Control	ROM	39	3140	3179
08	Control	Battery RAM	320		320

Program Module Quantities

Total no of program modules 183
No of program modules assigned to memory types 19 (10%)
No of program modules with estimated time.....12 (7%)
No of program modules with measured time.....6 (3%)
No of program modules with storage requirements 54 (30%)

Bus Time Loading Information

Bus No	Percentage Load
01	1
02	6

Creating a project status report

The typical project status report shown in Table 5 is part of the final output of this system design and reporting tool. It demonstrates the application of computer resources to organizing microprocessor based designs. Information in this report is automatically extracted from the core information files. Using the command file capabilities of the VAX computer, and simple FORTRAN routines for searching and totaling files, a system that accepts one command and produces all the sorted lists discussed can be easily developed. The project status report can then be created using simple FORTRAN subroutines. Thus, all sorted files and reports are accessible to all project employees, and the ease of creating data speeds up the design process.

A framework within which design information can be gathered and efficiently organized is crucial to the success of any microprocessor based project. The method discussed improves design productivity in the formative stages of a project. And, if good data entry habits are established early, the information system is easy to maintain. Advantages of the system are that it allows easy assignment of development tasks and that it helps maintain continuity even with changes in personnel. The automatically created status reports are produced at no charge and keep designers, managers, customers, and users aware of developments. Further, the system can be assembled in small, no-risk pieces and then continually expanded. Even if development stops at the core data file and data flow diagram stages, significant advantages are gained without implementation risk.

The question of whether to freeze the design information or continue updating it can be decided jointly with customers. Updated information files are useful for user training, and the customer can elect to maintain the records after the original intent of guiding early software development has been fulfilled.

Further enhancements to the proposed system include automatic scanning of final machine code files to create structure diagrams, lists of actual mnemonic names, PDL mnemonic to actual code mnemonic cross-reference lists, and actual memory storage requirement quantities. Regardless of the sophistication of the information management system, the value designers gain by employing the fruits of their labor is obvious. A computer based design information system can improve productivity as well as communication.

Acknowledgments

The author wishes to thank Don Wolfe and Robert Partlow for their efforts in making this report possible.

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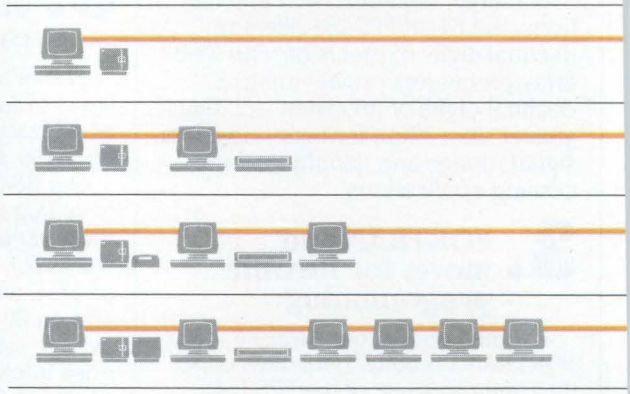

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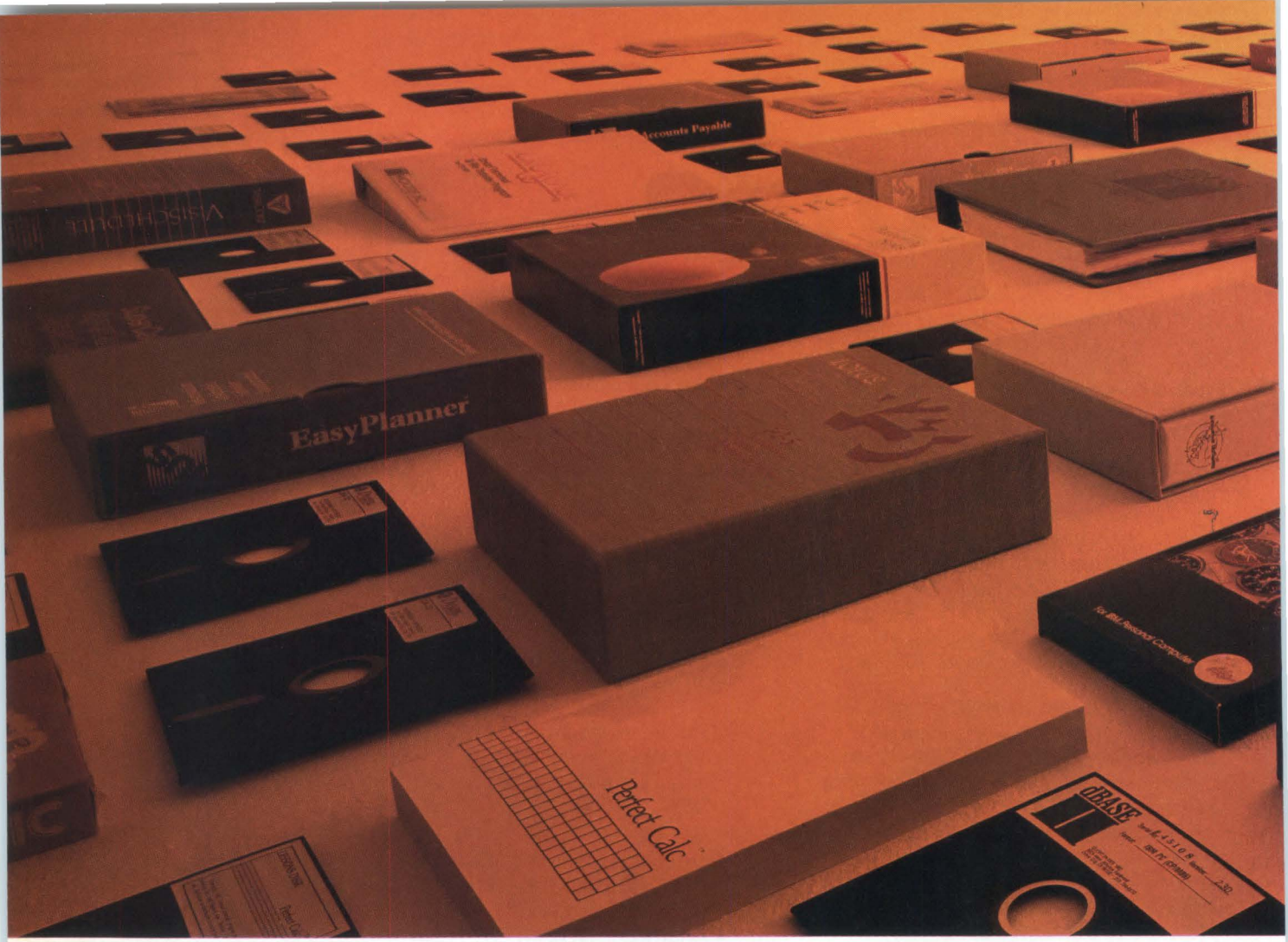

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Growing with the demands for more professional personal computers, Texas Instruments has taken several steps away from the game machines with its entry of the TI Professional Computer. This expandable system combines internal diskette and Winchester drives, enhanced communications, ergonomically precise keyboard, internal modem, and high resolution displays. In addition, voice management and English language command capabilities—usually available only on large mainframes in artificial intelligence labs—will be introduced for the computer this year.

The compact system unit houses an 8088 16-bit CPU and 64K-byte RAM that is optionally expandable to 256K in 64K-byte increments. The computer's 8K-byte system ROM is expandable to 16K. A 320K-byte built-in diskette drive is standard; an optional 5M- or 10M-byte Winchester drive, or a second 320K diskette, can be installed internally by users. Also featured as part of the main unit are diskette controller, 5-slot expansion bus, keyboard interface, parallel printer port, power supply, speaker, and monochrome or color CRT controller with 4K-byte video display memory.

High resolution data are presented on a 12″ (30-cm) green phosphor monochrome display or on the optional 13″ (33-cm) color display. Both CRTs use a 25-line x 80-col format and 720 x 300 pixels with the graphics controller option. Applications programs, even with extensive graphics, can operate with either display unit without modification. No reprogramming is required when changing displays.

Communications options provide a variety of protocols needed for smooth interaction with other computers and data bases. Both TTY and 3780 emulators are available for the computer in network environments. Standalone 3270 SNA, clustered 3270 BSC/SNA, 3101 emulation, and communications to TI's Business Systems minicomputers will be supported as part of the third-quarter 1983 enhancements. Either a 300- or 300/1200-bps internal direct connect modem, with auto-dial/answer capabilities, provides communications to other peripherals or data bases over ordinary telephone lines.

The low profile 97-key keyboard contains a 57-key typewriter layout, 18-key numeric keypad, 5 cursor control keys, and 12 special function keys. Upper- and lowercase characters and a selection of international character sets are available. The standard 256-character set is expandable to 512 for scientific and business use.

Omni impact printer model 850, as a companion to the system, prints at 150 cps and provides a variety of fonts, compressed print, and enhanced print options. The 850 also features raster graphics ability, which can be used to directly print graphics from the computer's display.

By supporting MS-DOS, CP/M-86, Concurrent CP/M-86, and UCSD p-System operating systems, the computer is compatible with BASIC, Pascal, FORTRAN, and COBOL. More than 100 third-party software applications, including a range of accounting, financial modeling, database access and management, graphics, and word processing packages are available. In addition, the computer has access to the large data base of programs written for CP/M-80 using a softcard supplied by Xedex Corp. Advanced integrated applications are already under development by third parties for introduction during 1983.

Also planned for this year is the natural language user interface. Derived from TI's research in artificial intelligence, the interface combines common English words and phrases into computer commands. Users construct sentences from word groups shown in a set of windows displayed on screen. Selected items from each window appear at the bottom of the video screen as standard English sentences describing the functions to be performed. The computer can also recognize and respond to voice commands through the voice management system. Combining speech processing, voice recognition, and telephone management functions in a single integrated internal unit, the 32-bit signal processing microcomputer based system recognizes an unlimited number of spoken words or phrases.

TI is also planning to increase user memory and add other I/O devices by year end. The computer is currently selling for $2595 for basic equipment. **Texas Instruments Corp, Data Systems Group,** PO Box 402430, H-651, Dallas, TX 75240.

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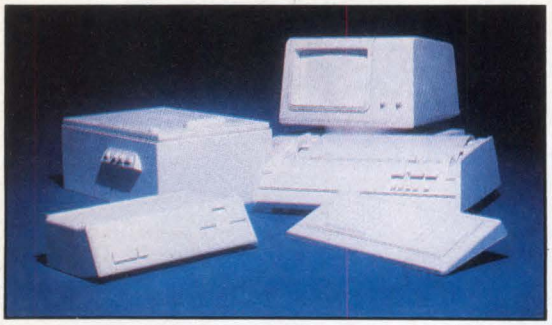
Flame retardant resins tailored to application designs



To meet UL flame retardant requirements for computer and business equipment enclosures, General Electric has provided four new resins tailored to increase design choices of materials without mandating overspecification. The new resins are derived from NORYL® N190 resin, a modified polyphenylene oxide-based thermoplastic. Introduced in 1964, N190 has become a commonly selected material for equipment housings. It does not corrode tooling as does flame retardant acrylonitrile-butadiene styrene (FRABS) material and thereby eliminates the cost of mold cleaning.

The resins provide low specific gravities (1.06 to 1.09, ASTM method D792) and thin-wall capacities down to 0.6″ (1.5 cm) without sacrificing the UL listings. An ultraviolet grade resin also affords color stability under office lighting. Each resin combines high impact strength, rigidity, low gloss finish, broad processing window, and no corrosive plate-out during molding. The resins meet flammability requirements of UL STD 478 for computer room equipment and UL STD 114 for office and business equipment. All materials covered under these standards must also pass a mold stress relief test, during which the part is exposed to a 10 °C temp greater than the operating temp, or 70 °C for seven hours. The enclosure must not soften, warp, or distort. In addition, a 5 ft/lb falling-ball impact test must be satisfied.

As a replacement for the higher priced FRABS, CRT-200 resin is UL listed at 94 V-1/V5, UL STD 478. The resin also satisfies UL enclosure requirements for stationary business equipment and provides a heat deflection temp (93 °C at 264 psi, ASTM method D648) and impact strength that is superior to FRABS. Price in truckload quantity is $1.37/lb or 5.4 cents/in^3.

PC-180 resin, for personal/portable computers, is UL V.2 listed. Low specific gravity (1.09), greater tensile and impact strengths than FRABS, and a $1.20/lb or 4.7 cents/in^3 cost are featured.

Low voltage machines that are not intended for computer room use and that operate at under 42 Vdc or 30 Vac can be designed with HB-235 resin. The material meets the less stringent UL HB flammability specs. Heat deflection temp is 235 °F (113 °C), which makes the resin comparable to both ABS and ABS/polycarbonate blends. The resin is $1.29/lb or 4.9 cents/in^3.

UV-180 resin can solve the problem of ultraviolet light degradation of equipment under fluorescent lights. It is $1.49/lb or 5.9 cents/in^3.

With the exception of the UV stabilized grade, all resins being introduced are priced below NORYL N190 or comparable materials; the UV grade has a $0.02/lb premium. **General Electric Co, NORYL Products Div,** One Noryl Ave, Selkirk, NY 12358.
Circle 262

Computer puts printer, modem, CRT, and keyboard in one package

Access portable computer system integrates more peripherals into a single compact unit than other comparable systems, while keeping its retail price at $2495. Power packed system performance is derived from five high speed microprocessors. Included as standard features are a printer, internal communications modem, CRT monitor, two double-density 5¼″ disk drives, keyboard, 64K user memory, operating system and software package, multiple I/O ports, storage compartment for 10 diskettes, and leather carrying case.

The full 64K RAM easily handles most software programs. Access is CP/M 2.2 compatible and comes with "Perfect Software," an integrated package with virtual memory programs that accommodate documents larger than the system's memory. Up to seven files can be simultaneously worked on, or any two files displayed on a split screen. Four programs equip users with word processing, spreadsheet, spelling correction, and database management capabilities. M BASIC from Microsoft and C BASIC from Digital Research are also included.

The built-in bidirectional printer delivers hard copy at 80 cps in four type sizes, including a condensed font with up to 132 chars/line output. In addition to the full 96 ASCII character set, the impact dot matrix printer provides full graphics capabilities and software driven type styles.

Communications links use an internal modem either through the direct connect modular phone jack for online operation, or through the acoustical coupler for telecommunications from any standard telephone. Transmitted data are simultaneously printed. The modem is adjustable from 0 to 300 baud, and includes manual originate and answer, auto-dialing, and directory support operating modes.

Detachable from the main unit, the low profile typewriter style keyboard has 15 function keys, cursor controls, and numeric pad. The amber 7″ (18-cm) CRT displays 80 characters on 24 lines and a 25th status line. Selectable attributes include inverse, blink, blank, underline, double underline, and half and full intensities.

Peripherals are easily interfaced to the Centronics compatible or bidirectional parallel port, to the two RS-223-C serial ports with software selectable baud rates to 9600, or to the fully implemented IEEE 488 port. An onboard controller/interface for standard 8″ floppy drives is included, along with a composite video jack for access to an additional monitor. The two 5¼″ single-sided, double-density drives provide 184k bytes of storage per diskette. Optional are double-sided, double-density drives yielding 736k bytes of diskette storage.

An internal UPS gives up to one hour of portable system operation, and can be recharged from any standard household outlet at 12-V battery. The computer operates from 110 or 220 V. **Access Matrix Corp,** 2159 Bering Dr, San Jose, CA 95131. **Circle 263**

Low cost, high performance PCB CAD system

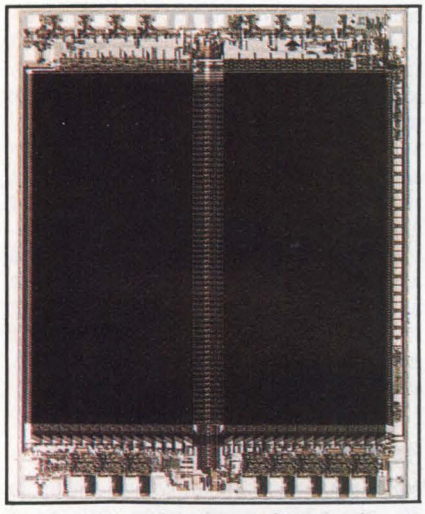
Performance equivalent to or better than that of most high performance minicomputer and mainframe based systems, but at lower cost, is promised for Cadnetix' CDX 5000 and 5001 microcomputer based CAD systems. The more sophisticated model 5000, a standalone workstation with 32-bit internal architecture, up to 3.5M bytes of RAM, 19″ (48-cm) color display, 40M-byte 5¼″ Winchester disk drive, and 1M-byte mini-floppy disk drive is priced at $74,500, including all software. However, the model 5001, with only 0.5M bytes of RAM and a 20M-byte Winchester starts at $59,500. This system is without advanced features such as automatic component placement and automatic trace routing. Both include a detachable low profile keyboard that meets ergonomic standards and a mouse input device. In addition to the components shown in the photo, a floor based card cage contains such peripherals as the disk drives, power supply, and capability cards.

Software packages provide an interactive schematic generator supporting hierarchical design, automatic component placement optimization, and high speed automatic trace routing. Interactive editing of automatic component placement, trace routing for manual control of critical areas, continuity and design-rule checking, automatic generation of PCB artwork and NC tapes for production, and automatic generation of design documentation are also software elements. The present operating system is a UNIX lookalike, but a UNIX compatible OS is planned for later introduction.

The system incorporates design verification/design-rule checking for automatic, continuous checking as designs progress. An improved router technique provides faster trace routing than the technology used in other systems. The object oriented approach to the user interface results in almost immediate productivity gains, instead of the typical 6-month learning curve on some other systems. The "undo" key lets the user immediately correct mistakes and prevents accidental loss of data due to operator error. It can reverse single instructions or a queue of wrong instructions. A fast-response graphics system reduces designer's wait time.

Future systems will include optional Ethernet communications interfaces that will connect the workstation to 200M bytes of online storage. **Cadnetix Corp,** 5797 Central Ave, Boulder, CO 80301.
Circle 264

Latched EEROMs supply upward migration and 1-ms write time



A comprehensive 3-member family of EEROM chips pushes Seeq Technology's 1-year-old, 5-V memory devices to include an advanced set of expandable E^2 functions, a variety of memory densities, and a complete 5-V system with onchip latches and the fastest available write time. The 2-micron EEROMs include 16K-bit model 52B13, 32K-bit model 52B23, and 64K-bit model 52B33.

All are produced via dry plasma etch processing to compound density while cutting size. This scaled E^2 oxynitride technology employs wafer stepper lithography and plasma metal etching, giving the 52B33 a 64K-bit die area of less than 35k mil^2. Through these processes, the 52B33 chip can use a 4-transistor memory cell that measures 168 $micron^2$. A minimum drawn channel length of 3 microns, coupled with a 6-micron pitch for metal and diffusion, are combined to produce a cell that is 60% smaller than that used in Seeq's earlier EEROM model 5213.

Such reduced cell size and increased density over 64K-bit nonvolatile memories make the 52B family EEROMs a viable alternative to EPROMs. At a die size equivalent to typical 64K EPROMs, a price per bit crossover becomes a new competitive advantage.

To achieve bus independence, the EEROMs have integrated system latches that are four times as dense and 45% smaller than 16K EEROM 5213. The need for system level components such as address, data, output, and chip enable latches are eliminated by providing these functions as an integral part of the memory chip. At the falling edge of write enable, the signals are latched internally to free all system bus lines for other operations. Write enable is the only signal required to remain valid for 1 ms during programming. One-ms write and erase times are billed as industry firsts for EEROMs and are also claimed to be 10 times faster than speeds provided by comparable EEROMs and EPROMs. A 250-ns read access time guarantees compatibility with most high speed microprocessors.

In addition to byte-clear and byte-write operations, the entire EEROM array can be cleared in a single 5-V only operation. The 52B23 32K and 52B33 64K chips also feature 5-V chip erase. Other EEROMs typically use in excess of 12 V, which is not readily obtainable in TTL level systems. Each 52B EEROM operates on a 5-V TTL level in read, write, and erase modes. Each byte may be erased or written up to 10k times.

Silicon Signature, Seeq's data traceability feature approved by JEDEC, is stored in ROM in every die and contains onchip device and programming information. Seeq's DiTrace feature stores production flow data to the wafer level on bits outside the normal addressable array.

The 16K model 52B13 is available for $27.90/100 units. The 32K 52B23, at $71, and the 64K 52B33, at $185, are available in prototyping quantities. **Seeq Technology Inc,** 1849 Fortune Dr, San Jose, CA 95131. **Circle 265**

RS-232-C handheld telecomputer

Model TC 103 telecomputer system for hard-wired LAN installation in fixed or portable locations plugs directly into an RS-232-C port. System has a QWERTY-style full alphabetic keyboard, with control and shift functions to generate the full 128-char ASCII code set. User friendly help keys facilitate development of computer-initiated dialoguing software to reduce or eliminate operator training. A 16-char LCD display, variable scroll rate from 2 to 30 cps, and repeat key to allow review of the last 80 chars received are included. **IXO, Inc,** 6041 Bristol Pkwy, Culver City, CA 90230.
Circle 266

Bell compatible, 1200-bps modems

DF03 series Bell 212A/103J compatible 1200-bps modems for rack mounting connect directly to public or private telephone networks and public switched telephone networks. RS-232-C/RS-423-A interface circuits are used. The DF100 mounting rack ($850) with internal 120-Vac supply accommodates all DF series modem modules. It can accept a redundant power regulator option that assumes the power load should the primary regulator malfunction. Modems are $750 for a basic unit and $950 for an autocall version that originates dialing from unattended stations. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 267

Rapid poll modem

MP-96 9600-bps modem can be set up in 20 ms while maintaining full-speed operation for both outbound polls and inbound responses. This operating mode extends the economies of multipoint operation, avoiding protocol sensitivity, load unbalance, and split-speed limitations. Modem can also operate 1 or more drops at 7200 or 4800 bps. Unit resumes operation immediately after short line interruptions. **Paradyne Corp,** PO Box 1347, 8550 Ulmerton Rd, Largo, FL 33540.
Circle 268

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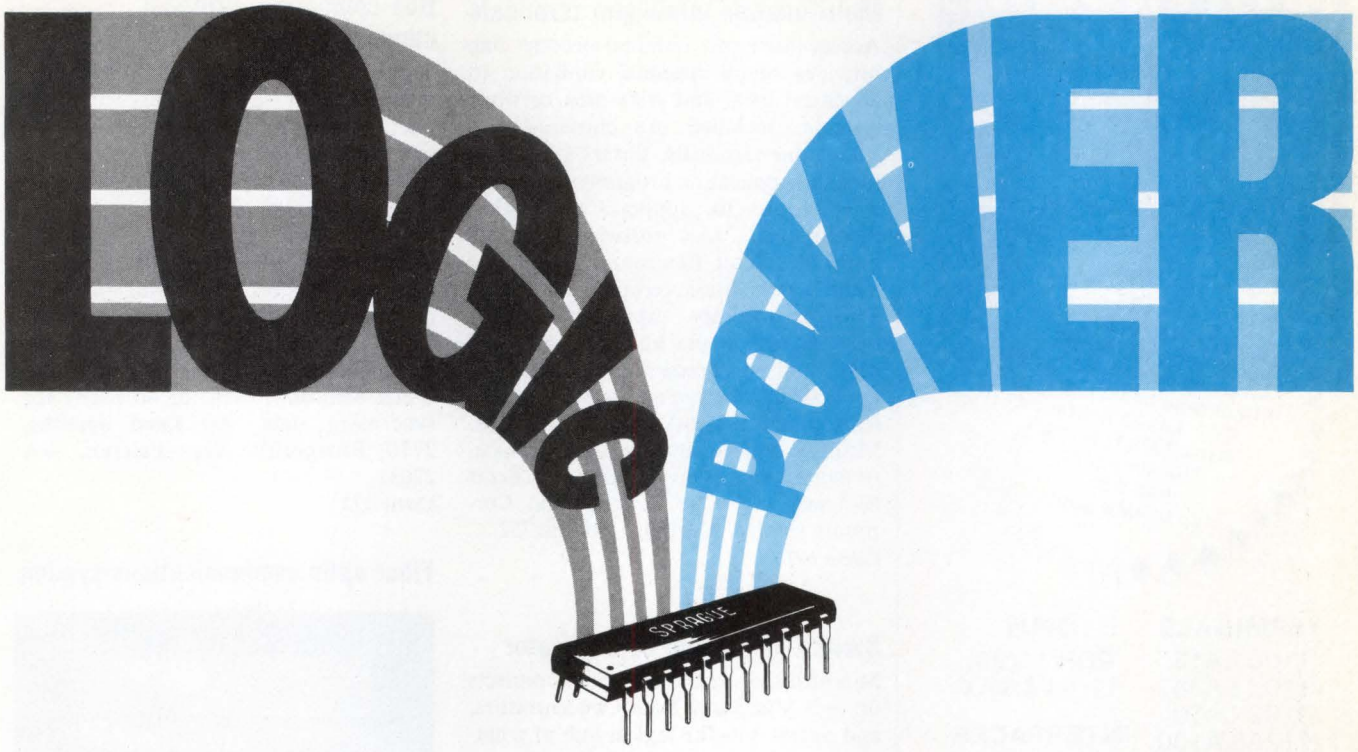

Sprague BiMOS ICs Simplify Interface Designs

Sprague BiMOS Latch/Drivers can be advantageously employed in a variety of sink and source drive applications: relays, solenoids, stepping motors, LED or incandescent displays, thermal print heads, vacuum fluorescent displays, and many more.

These IC's incorporate CMOS inputs, latches, and control circuitry to provide minimum loading and compatibility with CMOS, PMOS, NMOS, and TTL. The bipolar Darlington outputs are suitable for use with a wide variety of high-voltage or high-current loads. The bipolar/MOS combination provides extremely low-power with maximum interface capability.

Type	Description	V_{OUT}	V_{DD}	I_{OUT}	Engineering Bulletin No.
UCN-4401A	4-Bit Latch/Driver	50V	18V	500mA	26180
UCN-4801A	8-Bit Latch/Driver	50V	18V	500mA	
UCN-4805A	Latched Decoder/Driver	60V	18V	−40mA	26181
UCN-4806A	Latched Decoder/Driver	60V	18V	−40mA	
UCN-4810A	10-Bit Serial-input, Latched Driver	60V	18V	−40mA	26182
UCN-4815A	8-Bit Latch/Source Driver	60V	18V	−40mA	26183
UCN-4821A	8-Bit Serial-input, Latched Sink Driver	50V	15V	350mA	26185
UCN-4822A	8-Bit Serial-input, Latched Sink Driver	80V	15V	350mA	
UCN-4823A	8-Bit Serial-input, Latched Sink Driver	100V	15V	350mA	

For the engineering bulletins of interest to you, write to: Technical Literature Service, Sprague Electric Company, 555 Marshall St., North Adams, Mass. 01247.

For further information, write or call Paul Emerald, Semiconductor Division, Sprague Electric Company, 115 Northeast Cutoff, Worcester, Mass. 01606. Tel. 617/853-5000.

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CIRCLE 119

Multifunction intelligent terminals

Access intelligent terminal product line provides simple terminal emulation to advanced local and wide area network systems. Included are clustered and standalone terminals, library of emulators and application programs, and software tools to support application development. LAN software operates under the Scott Environment Management System. Basic terminal starts with 64K-byte memory, expandable to 1M byte. Based on the 8088, each terminal has 1 microprocessor to execute the application program and a second micro to support network communications. Memory options include dynamic RAM, UVPROM, and nonvolatile RAM. **Scott Systems, Inc,** One Metropolitan Corporate Center, Marlboro, MA 01752.
Circle 269

Switch selectable concentrator

Micro860 Concentrator Switch connects up to 8 Micro800/2 Data Concentrators, and operates as the logical hub of a network to allow any async channel on 1 concentrator to communicate with any other channel on that or any other concentrator. Add-on networking functions include switching, channel contention, queuing, and centralized management. Matrix, fixed destination, local, and class selection switching types are provided. Four-composite model is $2550; 8-composite version is $3250. **Micom Systems, Inc,** 20151 Nordhoff St, Chatsworth, CA 91311.
Circle 270

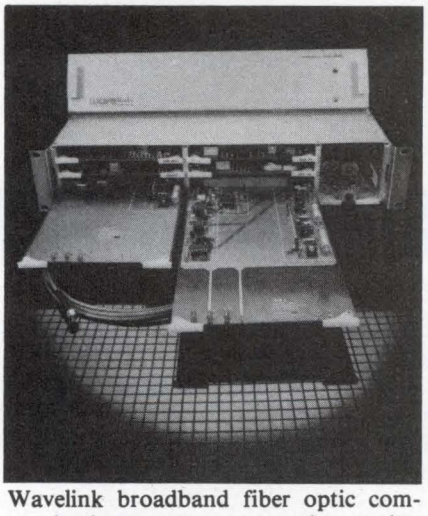
Combined multiplexer/statistical concentrator

Statcon series 11 brings software transparent remote statistical concentration to the company's CS11 line of multiplexers. Special microprogramming provides demultiplexing required to funnel remotely concentrated data into a single RS-232 computer port. Up to 64 local/remote lines can be connected to any DEC PDP-11 or VAX-11 system via a single backplane slot and without any modification of std software. Each remote link plugs into 1 local RS-232 port; remaining RS-232 ports can be allocated to local asynch line applications. Existing CS11 configurations can be converted to include Statcon 11 capability via PROM set change. **Emulex Corp,** 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.
Circle 271

Bus compatible protocol converters

Three bus compatible protocol converters for the LSI-11 Q-bus, Multibus, and S-100 bus feature 2 I/O ports, 8085 based microprocessors, and LED indicators and test switch under program control for diagnostics. The PCU-40 PCU-42/48, and PCU-52 have programmable controllers to serve a range of peripheral devices, connecting via RS-232 or Burroughs' direct connect (TDI) circuits. Options include baud rates from 50 to 19.8k bps and word lengths of 5 to 8 bits with odd, even, or no parity for sync/async data. **Air Land Systems,** 2710 Prosperity Ave, Fairfax, VA 22031.
Circle 272

Fiber optic communications system



Wavelink broadband fiber optic communications system transmits analog signals over 2 km using an LED source and FM transmission method. FM method operates with an ON/OFF action of the transmitting device to ensure system linearity. Unit is not susceptible to intermodulation distortion or diminished signal to noise ratio. An avalanche photodiode is incorporated for its photoelectric effect. Data option is built on a plug-in board that is fully interchangeable with audio boards. Serial asynch data is input via RS-232 interface. **The Grass Valley Group, Inc, a Tektronix Co,** PO Box 1114, Grass Valley, CA 95945.
Circle 273

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Model 70Q emulates DEC** TM11/TU10 magnetic tape subsystems, and is supported by RT-11V4, RSX-11MV4.0 and RSTS/EV7.0 operating systems without modification. The Q-bus controller occupies one quad-slot.

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CIRCLE 121

MULTIBUS

Q-BUS

RS-232

S-100

Three-way port sharing switches

Models 8351-D and 8352-D, RS-232 A, B, and C switches provide the capability to share 1 computer port among 3 peripherals. Model 8351-D ($160) switches 12 of the most required RS-232 interface signals and is sufficient for most port sharing applications. Model 8352-D ($180) switches all signals at the RS-232 interface and will satisfy any 3:1 sharing application. All desktop unit connections are made via 4 female 25-pin EIA connectors on the rear panel. The speed/code transparent switches require no power. **Electro Standards Laboratory, Inc**, PO Box 9144, Providence, RI 02940. **Circle 274**

Two DSU buffers and upgraded LADDs

The 832 and 835 digital service unit (DSU) buffers join Bell System dataphone digital service (DDS) links. DSU 832 interconnects DDS links operating with an RS-232 interface at data rates of 2.4k, 4.8k, or 9.6k bps. DSU 835 interconnects DDS links operating with a CCITT V.35 interface at 56k bps. The units are $1750 each. Added features to the family of local area data distributors (LADDs) provide MIL-188/114 interface capabilities for the 2200 and 2300 LADDs that now operate at rates to 2.5M bps. The 2300 LADDs can be interconnected to terminal equipment operating at 772k bps with a Bell T1 carrier operating at a line rate of 1.54M bps. The 2370 feature is available on all 2300 models operating with a V.35 interface at 1.54M bps. **Avanti Communications Corp**, Aquidneck Industrial Park, Newport, RI 02840.
Circle 275

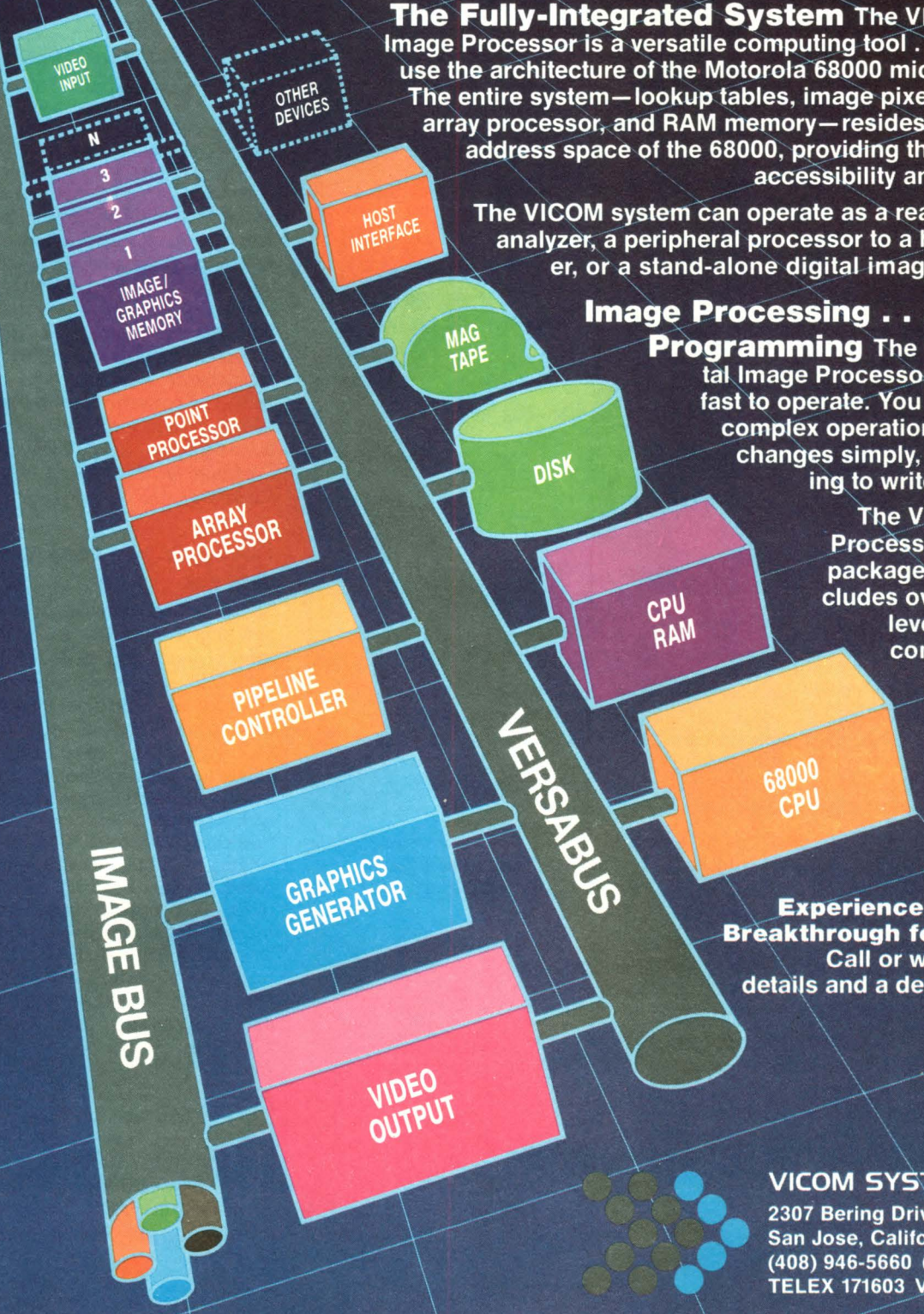
Multiprotocol converter

SNA/SDLC protocol converter SMRTE ONE (sync/async multiprotocol remote terminal emulator) allows use of both bit-oriented and char-oriented protocols, either separately or combined. Four serial ports and 1 RO printer parallel port are provided. Any serial port can be used as the main I/O while others are configured as required by attached hardware. The 24-char LCD calls up the main menu, which includes protocol desired, port location, baud rate, device selection, and diagnostic routines. All menu item selections can be set up from the front panel via push buttons. Unit price is $3995. **Modemsplus, Inc**, 217 E Trinity Pl, Decatur, GA 30030.
Circle 276

VICOM Digital Image Processor

The Architectural Breakthrough

The latest development in digital image processing is here! It's a major breakthrough in systems architecture from Vicom Systems, Inc. And it *combines* patented hardware and software features you've been waiting for to give you unequalled speed and flexibility in a variety of applications.



The Fully-Integrated System The VICOM Digital Image Processor is a versatile computing tool . . . the *first* to use the architecture of the Motorola 68000 microcomputer. The entire system—lookup tables, image pixels, registers, array processor, and RAM memory—resides in the direct address space of the 68000, providing the ultimate in accessibility and efficiency.

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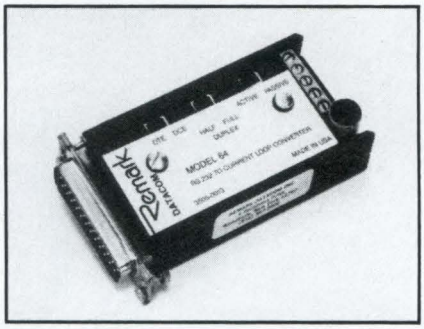
Compact 103J compatible modem

A Bell 103J compatible modem, the VS103P is mounted on a 24 in^2 PCB and features RS-232-C and TTL interfaces. Zero to 300-bps full-duplex operation with manual or automatic originate/answer capabilities are provided. The modem is FCC registered and TAP certified for direct connection to the switched network. Pulse or tone automatic dialer option stores up to 32 digits in memory. It is priced at $165 in lots of 100. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086. **Circle 277**

Universal programmable current loop converter



Model 64 allows any computer to interface with current loop peripherals or utilize their internal current loop interface circuitry to drive remotely located RS-232 based peripherals. Current loop interfaces can be half-duplex/passive loop, full-duplex/passive loop, half-duplex/active loop, and full-duplex/active loop. The RS-232 port is switch selectable to support DTE or DCE interface. The converter provides for 20- or 60-mA current loops and operates from dc to 9600 bps. **Remark Datacom Inc,** 4 Sycamore Dr, Woodbury, NY 11797. **Circle 278**

Fiber optic plug compatible data link

Series of fiber optic RS-232-C data links are plug compatible replacements for most 4- and 9-wire EIA RS-232-C extension cables. Extending cables beyond the 50' (15-m) limit of a std RS-232-C cable, the links provide emi/rfi resistance, data security, reduced error rate, and also eliminate ground loops. Full-duplex asynch data rates from dc to 56k bps with less than ±4-µs pulse-width distortion over −20 to 80 °C range on cable lengths to 3281' (1 km) are accommodated. Module HFM 5005 kit **($165)** contains fiber optic transmitter/receiver module and a cube power supply. DCE/DTE switch provides 1 module type for both DTE and DCE equipment. **Honeywell Inc, Optoelectronics Div,** 830 E Arapaho Rd, Richardson, TX 75081. **Circle 279**

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CIRCLE 125

Multibus compatible datacom boards

MZ-80 processor board uses a 6-MHz Z80B CPU and has 32K-byte RAM and 4K-byte ROM. The Multibus compatible board is $960 in OEM quantities. MZ-MMB multipurpose memory board ($515) adds 32K bytes of 150-ns static RAM. MZ-MSIO ($800) I/O board provides 4 independent RS-232 serial I/O channels. MZ-SIO8 board features 8 independent serial I/O channels and is available in RS-232 ($640) and current loop ($1040) versions. MZ-RMC 19″ (48-cm) rackmount chassis ($1400) holds up to 8 boards and has dual, low noise fans and 150-W switching power supply. **Thomas Engineering Co,** 1040 Oak Grove Rd, Concord, CA 94518.
Circle 280

Software emulates star microcomputer network

InfoShare communications package provides data exchange between remote microcomputers running either CP/M or MP/M and a central MP/M system. The remote micro can also be operated as an MP/M console in the same system. Security utility protects the host system from unauthorized entry. Protocol transfer of ASCII and binary files, simple ASCII file transfer between nonrelated terminal programs, communications with timeshare systems, and echo to printer are possible. ASCII commands can be passed to an auto-dial/answer modem. One-time system license charge is $250. **The Information People,** 443 Hudson Ave, Newark, OH 43055.
Circle 281

Smart modem links computers at 1200 bps

MDM-1200 intelligent modem/dialer incorporates an 8-bit microprocessor and communicates data over telephone lines at speeds to 1200 bps. The full-duplex, direct connect modem ($1495) has a single RS-232-C port that controls the microprocessor's functions before entering data mode and transferring data to/from the telephone after entering data mode. Unit can be connected to either a CRT terminal or directly to a computer system. Simultaneous transmission/reception of serial binary data is at either 0 and 300 bps or at the fixed rate of 1200 baud for bit synch/asynch formats. **Cromemco, Inc,** 280 Bernardo Ave, Mountain View, CA 94043. **Circle 282**

SOFTWARE

Pascal compiler for PDP-11 UNIX systems

Pascal-2 optimizing compiler for PDP-11 systems operating under UNIX features a multipass operation which generates compiled code that is 30% to 40% smaller and twice as fast as the company's Pascal-1 compiler. Support tools include debugger, execution profiler, and development utilities. Debugger allows logic errors to be interactively solved at the source program level. Profiler identifies execution bottlenecks. License fees for Pascal-2/UNIX begin at $3950. **Oregon Software,** 2340 SW Canyon Rd, Portland, OR 97201.
Circle 283

Floating point library

The 8051 FPAC/DPAC floating point libraries process floating point numbers in the proposed KCS IEEE single- and double-precision formats. They are delivered in optimized source assembly language form. In addition to std arithmetic operations and floating point conversion routines, the library includes functions to compute sine, cosine, tangent, arctangent, square root, common and natural logarithms, exponentiation, and floating point number to integer power. ASCII to floating point and floating point to ASCII conversions are also included. **U S Software,** 5470 NW Innisbrook Pl, Portland, OR 97229.
Circle 284

C compiler with CP/M and UNIX compatibility

A complete systems implementation of C gives application program compatibility with both CP/M and UNIX OS. The C compiler, designed for 16-bit 8086 and 8088 based machines, works with the company's 16-bit utilities, and includes a relocating linker and assembler as part of the package. The compiler also has built-in features of the UNIX error checking LINT program. **Digital Research,** PO Box 579, 160 Central Ave, Pacific Grove, CA 93950.
Circle 285

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C

Development software for TMS9900

System-99 enables any CP/M-80 microcomputer to serve as a software development station for TI's TMS9900 microprocessors. The software encompasses the TI 990/10 and 990/12 assembly languages with extensions to treat the TMS9940 processor. A macro assembler, interactive editor/assembler, text editor, and cross-reference generator are featured. System programs must be offloaded to the target processor for test as a direct transfer from memory via byte stream over a CPU port or via .COM or .HEX disk files. Individual diskette systems are $150. **Allen Ashley,** 395 Sierra Madre Villa, Pasadena, CA 91107.
Circle 286

Ada and Pascal under UNIX

An Ada compiler for the Concept/32 family of 32-bit computers provides for application software development under UNIX. Future validated versions of the compiler will accept the programs without modifications. The Pascal compiler, which also runs under UNIX, is compliant with international standards. Both compilers generate machine code via the C compiler for Concept/32 computers. Object programs execute directly at raw machine speeds. Ada, Pascal, and C subprograms can be mixed in a single program. Usage charges are $10,000 for Ada and $6000 for Pascal. **Gould Inc, S.E.L. Computer Systems Div,** 6901 W Sunrise Blvd, PO Box 9148, Ft Lauderdale, FL 33310.
Circle 287

Application program development for 68000 based systems

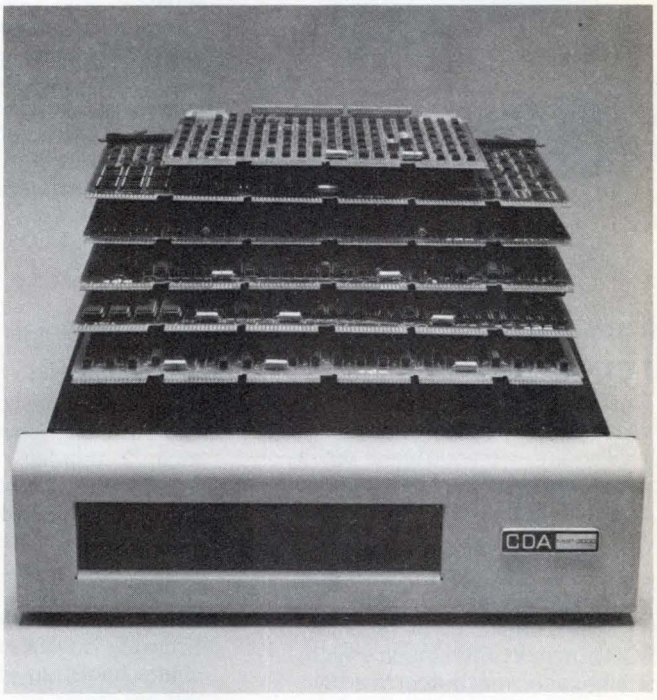
ASM-68000 structured macro cross assembler and the Link-68000 relocating linkage editor package can be used for 68000 based microcomputer applications development. ASM-68000 assembler translates assembly language source statements into relocatable object code for the Link-68000 linker. The code is then combined into an absolute load module for loading into the Mostek AIM-68000 in-circuit emulation module. This module works with the Radius remote access development system for use in a host computer environment. Package is $3000; a software license agreement is required. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 288

CP/M communications via HASP

Haste software package allows CP/M based microcomputers to communicate via the IBM HASP bisynchronous protocol. Incoming data can be directed to a disk file, console, printer/plotter, or any combination of these units. Screen-oriented text editor allows jobs of 17 lines or less to be entered and sent without leaving Haste. System requires 64K memory, CP/M-80, interrupts, and synchronous modem. Haste disk and manual is $500. **Florida State University, Computing Center,** Tallahassee, FL 32306.
Circle 289

Talk to the editors
Have you written to us lately? We're waiting to hear from you.

THE VERY PROGRAMMABLE
ARRAY PROCESSOR
FROM
CDA
COMPUTER DESIGN & APPLICATIONS, INC.



The MSP-3000 32-bit floating point array processor provides a level of programmability that other array processors don't. It includes a large Fortran callable library containing vector, matrix and signal processing functions. Additional mini-programming and microcoding levels simplify and speed easy development of special algorithms. Available programming tools include a symbolic assembly language, cross assembler, loaders and debuggers.

Complete systems, including 256 kilobytes of memory, array library and support software for the LSI-11,* PDP-11* or VAX* are under $25,000 in ten-unit quantities.

The DPG raster display controller attaches directly to the MSP-3000 internal bus. A high resolution display of up to 1024 x 1024 pixels is refreshed from the MSP-3000 data memory. The host bus need not be tied up to transfer processed data to the display.

Specifications

Speed: . . Five million floating point operations per second
Memory: 256KB, 512KB, 1MB, 1.5MB, 2MB
Display Format: . . . . . 128^2, 256^2, 512^2, 1024^2 x 1, 2, 4, 8, 16, 32, 48 bits/pixel
Options: . . . . . Parallel I/O; joystick; color or b/w monitor

CDA
COMPUTER DESIGN & APPLICATIONS INC.
411 WAVERLY OAKS ROAD
WALTHAM, MA 02154
617/647-1900

*LSI-11, PDP-11 and VAX are trademarks of Digital Equipment Corporation.

CIRCLE 129

In-circuit emulator forms development systems

"The Emmy" universal line of in-circuit emulators can be tied to existing computers or can be purchased as packaged systems, with a DEC Professional 325 small computer for single-user applications or a DEC PDP-11/23 for multi-user environments. Hardware includes a central 2-port RS-232 controller and pod for 8086/8088 and 8051 devices. Controller passes data from the terminal to Emmy software, which monitors and controls execution of microprocessor programs during debugging. Software includes OS, text editors, and microprocessor cross assemblers and cross simulators. Existing PDP-11 applications remain effective. Station with controller, 8086 pod software, and CRT terminal is $5200. **Digital Automation Corp,** 2 Fifer Ave, Corte Madera, CA 94925.

Circle 290

CP/M compatible STD bus microcomputer

ABL-1 general purpose, CP/M compatible STD bus 8-bit system has 64K-byte static RAM, 2 thin-line 8″ floppies (up to 3.2M-byte double-density storage capacity), a single-density controller that supports up to four 8″ double-sided floppy drives, and two RS-232-C ports. Both 4-MHz Z80A and 6.144-MHz 8085 CPUs are available. ABL-1 Auto-BIOS firmware is 2732A PROM resident and includes bootstrap routine and hardware self-test programs. The all metal ABL-1 ($6295) comes in a RETMA 19″ x 7″ (48- x 18-cm) rack with optional side panels for table mount. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 291

Realtime software analysis

The 91A24 data acquisition module for the DAS 9100 digital analysis system provides realtime analysis of software operation during software development and integration. Module has extended Define Mnemonics feature for microcomputer systems operational analysis. Data collection and disassembly of software flow functions can also be specified. Up to 4 modules/system permit a max of 96 channels of synchronous software acquisition with bus cycles down to 100 ns. For multiplexed address and data buses, the module accepts the address, then the data, at intervals down to 50 ns. Async acquisition is selectable in rates from 100 ns to 5 ms. Price is $5500. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

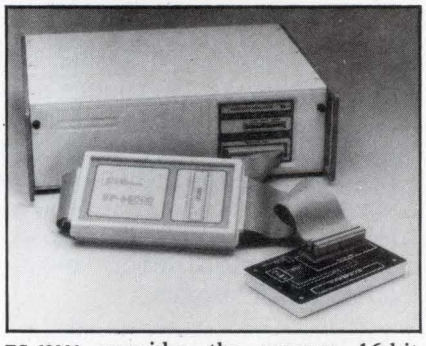
Circle 294

Automated custom IC design

ZyPAWS (ZyP automated workstation) for automated design of custom ICs based on standard cell libraries uses the 32-bit virtual memory Prime 2250 computer, which runs under the PRIMOS OS and supports up to 20 users. Model ZyPAWS is a frontend workstation for logic and circuit simulations, and test program generation. ZyPAWS II fully integrated workstation has color graphics capability for automatic cell placement and routing. ZySPICE enhanced circuit simulation program based on SPICE version 2.E includes small geometry transistor models. ZyPSIM proprietary event driven logic simulator yields silicon level timing predictions to guarantee delivery of ICs that correspond to the ZyPSIM output. ZyTEST proprietary software modules convert simulator output into Sentry series compatible automatic test programs. ZyPART proprietary programs automatically generate cell placement and routing directly from the ZyPSIM network file. **ZyMOS Corp,** 477 N Mathilda Ave, Sunnyvale, CA 94088.

Circle 292

Low cost emulation support for 68000



ES-68000 provides the MC68000 16-bit micro and 8080 Z80, and Z8000 families with in-circuit emulation, running the user's system in real time up to 10 MHz (12.5-MHz capability planned). Emulation debugging requires no space, uses no I/O ports, does not interfere with interrupts, and requires no modification to the system under test. Unit also features a 2046 step x 72 bit-wide trace history, breakpoint system, and optional 16-channel logic state analyzer. The emulator can stand alone or run from a remote computer. Price with options is $9950. **Applied Microsystems Corp,** 5020 148th Ave NE, PO Box 568, Redmond, WA 98052.

Circle 293

New Amdek 3" micro-floppydisk drive system!

AMDISK-III . . . the engineer's choice:

- New 3" hard plastic encased diskette.
- Up to 1 megabyte storage. (unformatted)
- Plug-in compatible with 5¼" drives.
- Compatible with - IBM-PC.

Specifications

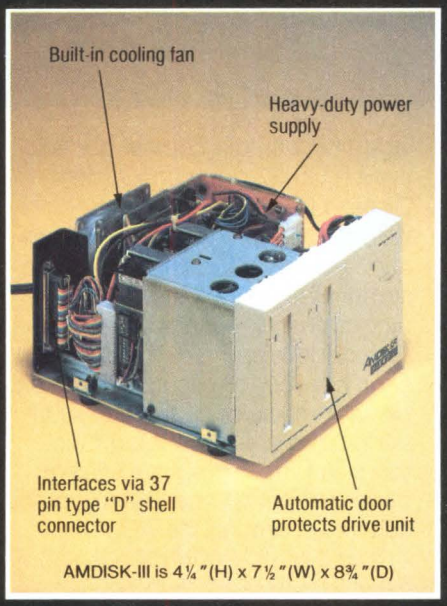
	Unit	Double Density
Capacity		
Unformatted Per Surface	Bytes	250K
Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	1
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10^{-9}
Hard Error		10^{-12}
Seek Error		10^{-6}
Media	3 inch Cartridge	
Drive Interface	Plug Compatible with 5.25 inch FDD	

External Interface

Connector: 37-pin "D" shell connector

Pin No.	Signal	Pin No.	Signal
1-5	Unused	13	Write data
6	Index	14	Write enable
7	Motor enable C	15	Track 00
8	Drive select D	16	Write protect
9	Drive select C	17	Read data
10	Motor enable D	18*	Select head 1
11	Direction	19	GND
12	Step pulse	20-37	GND

*drives are single head



AMDISK-III is 4¼"(H) x 7½"(W) x 8¾"(D)

Evaluation samples $480

Includes two-drive Amdisk unit with built-in power supply, 4 diskettes and application literature . . . Call (312) 364-1180.

The AMDISK-III Micro-floppydisk System is an engineering breakthrough in disk size, storage capacity, media protection and user convenience. Designed for microcomputers for many applications, the Amdek system is ruggedly constructed to provide years of trouble-free operation. Warranty is 90 days (parts & labor).

Put the new AMDISK-III to test . . . its recording format, data transfer rate and disk rotation speed are compatible with 5¼" floppydisk drives. Call, or write for evaluation samples at only $480.00 . . . or circle the reader service number for full technical details.

See us at NCC/83 Booth P7638

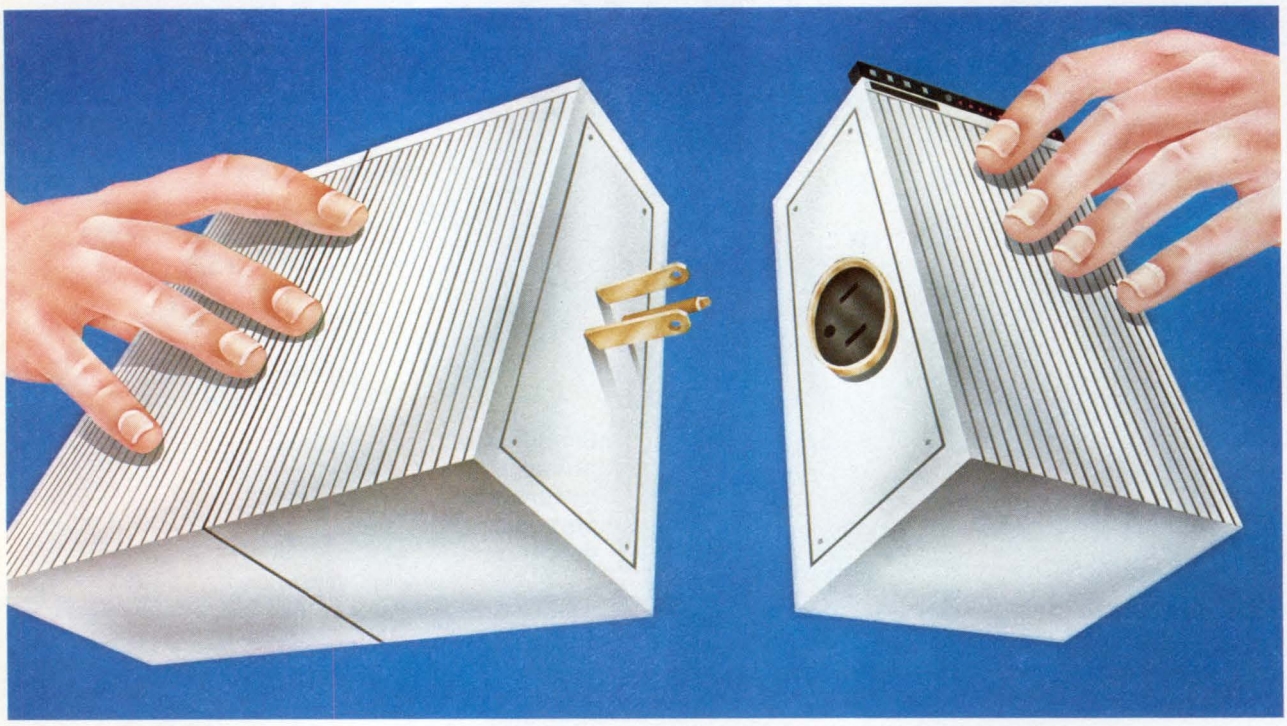
2201 Lively Blvd. • Elk Grove Village, IL 60007
(312) 364-1180 TLX: 25-4786

AMDEK CORP.

Amdek . . . your guide to innovative computing!

CIRCLE 131

At last, plug-in parallel processing in a 32-bit supermini system.



Perkin-Elmer announces the Model 3200 Multiple Processing System, an exciting new concept for demanding real-time applications.

Room to grow

The Model 3200MPS gives you extraordinary system expandibility. You can start with a host CPU and one auxiliary processing unit (APU). Then as your needs grow you can plug in more performance by adding as many as eight additional APUs.

Should you need even more horsepower, plug-in parallel processing lets you add exactly what you need as you need it—from a single APU to a whole fleet of multiple processing systems.

And no matter what the size of your configuration, a central point of control and management is provided by a single copy of our field-proven OS/32 operating system.

Design flexibility

With parallel-processing APUs you can take advantage of application segmentation and structured programming techniques to speed system development. You can segment your application into multiple task modules, with each APU performing a set of related functions. To further optimize system performance, you can easily re-allocate tasks among the APUs.

Your Model 3200MPS provides maximum flexibility for software development, reliability, and system maintenance. To incorporate new design changes or correct problem modules, simply work on the problem module while your system continues to operate. And the Model 3200MPS can be structured to permit continued system operation though one or multiple APUs may fail. When so structured, the APUs can receive immediate maintenance attention while the system continues to run or they can wait for routine scheduled maintenance.

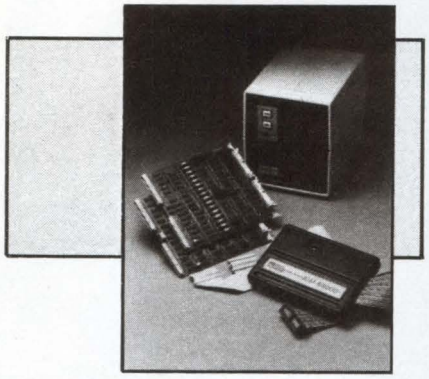
And our state-of-the-art universally optimizing FORTRAN VIIZ enables you to use modular programming techniques without sacrificing real-time efficiencies.

To find out more about how you can plug into all the advantages of plug-in parallel processing minis, mail the coupon or call today: The Perkin-Elmer Corporation, Two Crescent Place, Oceanport, NJ 07757.

Tel: 800-631-2154. In NJ, 201-870-4712.

PERKIN-ELMER

In-circuit emulator for MK68000 microprocessor



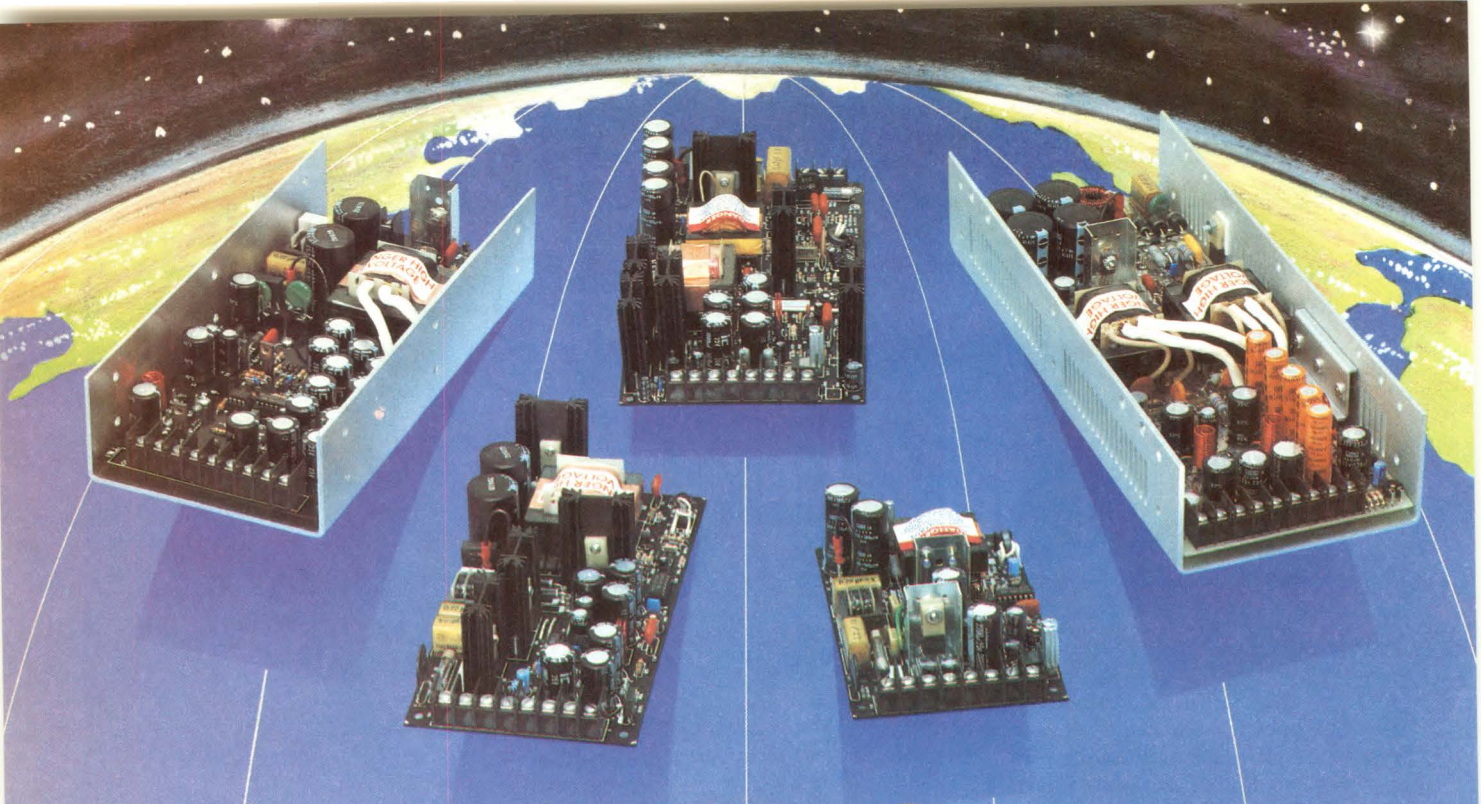
AIM-68000 in-circuit emulator for the MK68000 16-bit microprocessor works with Mostek's Radius and Matrix development systems. The 2-board set features realtime emulation at clock speeds to 10 MHz with no wait states, and allows operation in standalone mode for software debugging without the target system. Flexible breakpoints trigger from hardware, timer, or software. Single-step emulation with break on register contents using non-realtime emulation is also possible. The emulator features a non-realtime emulation register trace memory plus 16K words of emulation memory that can be mapped into eight 2K-word blocks addressable on any 2K-word boundary. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 295

Low cost 80286 software development

The DV286 80286 software development vehicle ($2495) works with CP/M-80 and CP/M-86 based development systems, or Intel development systems running the 8086 assembler. A MACRO286 (80286 instruction macro package) and execution vehicle (IEEE 796 compatible board with iAPX286 microprocessor and full virtual memory capability) must be installed. Software can be developed on the host and then loaded to the execution vehicle over an RS-232 port. PROM based DEBUG286 provides single-instruction execution, breakpoint setting, memory disassembly, and examine/modify of memory, I/O, and registers. **Microbar Systems, Inc**, 1120 San Antonio Rd, Palo Alto, CA 94303.

Circle 296



From Power-One
International Series Open-Frame Switchers
Designed for the World

POWER-ONE Quality - Now in Switchers

Following the successful lead of our International linear series, these all-new, high-quality switchers are designed specifically for products sold throughout the world...resulting in easier international marketing and bigger profits for you.

Multiple Outputs, With Worldwide Capabilities

Depending on the model, the new International Series offers up to 5 outputs to accommodate today's most popular applications...including small computers, terminals, peripherals, word processors, disk drives, Winchesters, and printers. At present, eleven models are available, ranging from 40 to 250 watts. Each has worldwide AC input capabilities which are field selectable.

Meets Domestic & International Safety Standards

Our new switchers are designed to meet VDE, UL, IEC, CSA, as well as most other regulatory agencies worldwide. We use VDE-approved components where required, in addition to the appropriate creepage, insulation, and clearance distances. The International switchers also meet the emissions limits of FCC Docket 20780 Class A, and VDE 0871/6.78 Class A. All of which adds up to easier system approval for products targeted for major international electronics markets.

Lightweight, Small Size, and Efficient

Incorporating the very latest state-of-the-art in switching technology, the new International Series switchers offer all the benefits of switching power supplies — high efficiency, low heat dissipation, light weight, small size and simple construction. Add these advantages to POWER-ONE's traditional quality and low cost, and there's no better buy in the world... *or for the world!*

SEND FOR OUR NEW BROCHURE!

MODEL	+5V	+12V	−12V	−5V	+24V	+12V	OUTPUT POWER	CASE SIZE (inches)	PRICE SINGLE QTY
SPL40-4000	5A	0.5A	0.5A	0.5A			40W cont.	2.00 x 3.92 x 6.30	$105
SPL53-4000	8A	2.5A/5A PK	0.6A	0.6A					
SPL53-4101	8A	1.2A	0.6A		1.5A/3A PK		80W cont.	2.10 x 4.25 x 8.25	$125
SPL53-4102	8A	1.2A	0.6A			2.5A/5A PK			
SPL65-5000	8A	1.2A	1.2A	0.5A	1.2A/1.5A PK		85W cont. 95W PK	2.10 x 5.00 x 9.00	$150
SPL130-4100	15A	4A/6A PK	1.5A			1.5A			
SPL130-4101	15A	1.5A	1.5A		2A/4A PK		130W cont. 150W PK	2.45 x 5.00 x 10.50	$198
SPL130-4102	15A	4A/6A PK	1.5A	1.5A					
SPL200-4100	35A	4A/8A PK	1.5A	1.5A					
SPL200-5100	35A	4A/8A PK	1.5A	1.5A		1.5A	200W cont. 250W PK	2.45 x 5.00 x 13.00	$270
SPL200-5200	35A	4A/8A PK	1.5A	1.5A	4A/6A PK				

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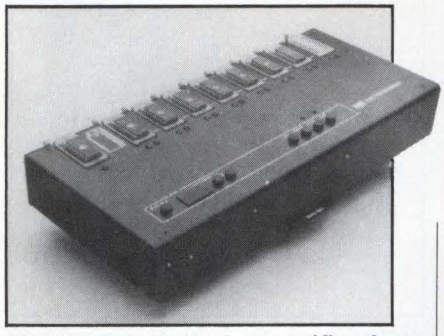
Outside California Call Toll Free 800/235-5943

CIRCLE 134

Eight gang EPROM/EEPROM programmer

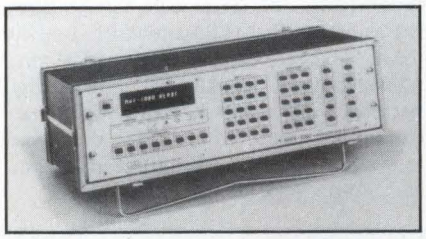


Model 8204 programs or verifies from 1 to 8 EPROMs or EEPROMs. As a free standing unit it performs blank tests, compare, and copy operations with a master. Two-way data transmission is provided for up/downline loading from a computer via RS-232-C serial interface. Virtually all EPROMs are programmable. If a fault is detected, power shutdown occurs automatically, the condition is displayed, and a fault alarm is audibly indicated. All functions are performed without personality modules or other accessory devices. Operating voltage is 110/220 Vac ±15%, 50/60 Hz. **Sherman Pirkle, Inc**, 3 Captain Parker Arms, Lexington, MA 02173.

Circle 297

TEST & MEASUREMENT

5¼" and 8" Winchester analyzers



MWX-1000 provides full and semi-automatic, and/or manual testing of ST506 and SA1000 interfaced drives. Test results are automatically logged through a serial printer port. In manual mode, all prime functions can be initiated from the keyboard, and presented on the alphanumeric display. Unit can also be keyboard programmed to provide any combination of std tests. Up to 16 drives can be multiplexed and exercised. Dual-microprocessor design with dedicated bipolar bit-slice microprocessor handles the I/O lines at a 200-ns cycle time. Price is $5995. **Wilson Laboratories, Inc**, 2237 N Batavia St, Orange, CA 92665.

Circle 298

Low cost 6502 microprocessor system analyzer

Interactive microprocessor in-circuit system analyzer for 6502 software development, the DA6502-A is $279 in single quantity. The portable analyzer allows the user to easily examine processor registers, read/modify memory locations, halt a program at a specific address, step-through a program, and stop a program at a location after a number of loops have been completed. The standalone, clip-on microprocessor analyzer has an 8-digit hex display. Microprocessor is keyboard accessed with 24 switches. Unit is approx 6.25" x 7.5" x 3.5" (15.88 x 19.1 x 8.9 cm). **DA-TECH Corp**, 92 Steamwhistle Dr, Ivyland, PA 18974.

Circle 299

Signature analyzer with HP-IL

HP 5006A signature analyzer ($995) provides full-option programmability on HP's interface loop (HP-IL). Fully programmable HP-IB (IEEE 488) option ($300) helps suit it to signature measurement for automated test stations. Composite signature function sums individual node signatures. The 25-MHz clock rate extends measurement capability to high performance digital circuits. CMOS logic and TTL thresholds are featured. Display and unstable light are latchable to catch intermittent faults and unstable signatures. Contact local **Hewlett-Packard** sales offices.

Circle 300

Benchtop analyzer tests linear/digital parts

LTS-2012 benchtop component test system evaluates linear, data conversion, and digital ICs and provides 16-bit overall system measurement accuracy, dual-floppy drives, integral alphanumeric keyboard and display, and BASIC and menu-style programming. Disk drives have 368K-byte storage. Std software for lot yield analysis, lot parametric distribution, and test datalog and library of turnkey test programs written to manufacturers' specs are available for all device families. Boards are available for DACs, ADCs, op amps/regulators, digital devices, and a user prototype board for custom device testing. Calibration board verifies internal 16-bit accuracy. Base price is $31,500. **Analog Devices Inc**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

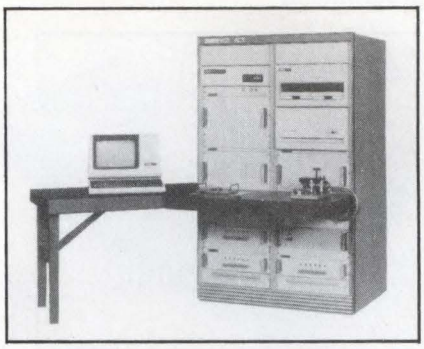
Circle 301

Low cost, modular logic analyzer

NPC-748 logic analysis system has 32 state channels and eliminates the integral floppy disk drive and its associated disk controller board. However, all items are self-contained modules that can be readily plugged back into the NPC-748 to upgrade it to an NPC-764 analysis system. All test/measurement features and accessories available for the NPC-764 are identical for the NPC-748. These include 16 channels of timing analysis, dedicated microprocessor probes, high speed analog waveform recording, bidirectional RS-232 analysis, and counter-timer/signature analysis. Functions can be used individually or internally linked. NPC-748 is $11,500; NPC-764 is $16,900. Upgrade kit is $6200. **Nicolet Paratronics Corp**, 201 Fourier Ave, Fremont, CA 94539.

Circle 302

Magnetic bubble memory tester

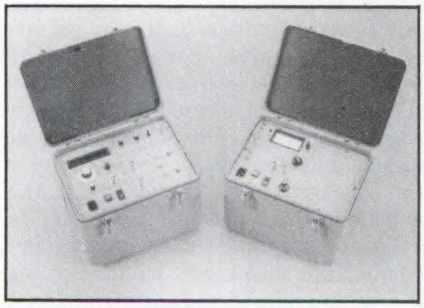


WJ-1455 magnetic bubble memory test system for virtually all magnetic bubble memories features expanded error logging capabilities and remote diagnostic functions. Characterization software package, graphics capability, automatic temp chamber control, and networking of test systems for centralized data collection/analysis are also featured. All previous magnetic bubble memory test software from the company will operate unmodified with WJ-1455. **Watkins-Johnson Co**, 2525 N First St, San Jose, CA 95131.

Circle 303

Bandwidth test set

Model 70 portable bandwidth tester measures end to end frequency domain bandwidth of a fiber optic cable system. The self-contained transmitter and receiver are available in 3 wavelength options: 850, 1300, and 850/1300 nm. Frequency range is 10 to 400 MHz. At 850 nm, with 50-micron core graded index fiber, the tester can handle fiber losses of 34 dB at full bandwidth, and 40 dB at 100 MHz bandwidth. At 1300 nm, allowable losses are 20 and 26 dB. Using peripheral equipment, frequency range can be extended to 1 GHz and allowable losses increased by 10 dB. **Siecor Corp**, 610 Siecor Park, Hickory, NC 28603.



Circle 304

ESPRIT III™

goes TVI-950 one better.

Our new Esprit III™ is a plug-to-plug replacement for the TeleVideo TVI-950. Same command set. Same keyboard layout. The same features. Even the same user-PROM capability.

But Esprit III goes TVI-950 one better. And that one important difference is price. Esprit III costs $300 less. In fact, it costs $100 less than TeleVideo's far less capable TVI-925.

Look at the numbers. TVI-950 performance for less than TVI-925 cost. You'll agree. Esprit III is the best one.

	Esprit III	TVI 925*	TVI 950*
Buffered mode	**Yes**	Yes	Yes
Programmable function keys	**Yes**	No	Yes
Line graphics	**Yes**	No	Yes
Page/line transmit	**Yes**	Yes	Yes
Smooth scrolling	**Yes**	No	Yes
Price	**$895**	$995	$1,195

*Trademarks of TeleVideo Systems, Inc.

Esprit Systems, Inc., Hazeltine Terminals Division, 500 Commack Road, Commack, NY 11725 (516) 462-5598

Esprit Systems, Inc.
Hazeltine Terminals Division

See us at NCC Booth W6288

CIRCLE 137

Enhancements for small computers

Optional binary synchronous communications adapter attaches the IBM PC to host systems or other IBM PCs via switched or leased line networks using BSC protocols. Installable in 1 of the 5 system expansion slots, it operates up to 9600 bps. An external modem must be connected between the adapter and telephone line. Price is $300. Binary synchronous 3270 emulation, version 1.0 software, when used with the BSC adapter, allows the IBM PC to act as a terminal that can communicate with a host system as if it were a BSC 3270 device. It requires 128K bytes of user memory. Price is $700. **IBM Corp, System Products Div**, PO Box 1328, Boca Raton, FL 33432.
Circle 305

Enhanced supermicrocomputers

Supermicro 64X and 32X multiprocessor microcomputers support 64 and 32 concurrent users. Model 64X has 136M-byte disk capacity that is expandable to 272M bytes. Model 32X has 60M-byte disk capacity expandable to 240M bytes. Both systems feature Z80B based file processor with 256K RAM and double bus transfer rates of 400k bytes/s. The X series application processors (Z80A 64K processing boards) are also available ($995). Basic Supermicro 64X with 136M-byte disk, 500K-byte floppy, and 32 application processor slots lists for $22,995. Supermicro 32X with 60M-byte disk, 500K-byte floppy, and 32 processor slots lists for $18,995. **Molecular Computers**, 251 River Oaks Pkwy, San Jose, CA 95134. **Circle 306**

CP/M processor card for DEC computers

Model 100 CP/M plug-in processor card for PDP-11 and LSI-11 computers contains a 6-MHz, Z80 processor, 64K-byte RAM, and computer interface to either the Unibus or Q-bus. When the CP/M OS is running, host computer serves as an I/O processor for the Z80. Diskettes in CP/M format may be read to and written from directly. Virtual CP/M disks can be to 33M bytes. Users can easily switch between RT-11 and CP/M. Card with CP/M software, license, and RT-11 control program is $1250. **Decmation**, 930 Tybalt Dr, San Jose, CA 95127. **Circle 307**

High end, 8-bit CMOS microprocessors

HD6301X series of CMOS 8-bit microprocessors in 1-, 1.5-, and 2-MHz versions ($28, $34, and $41) incorporate 4K-byte ROM and 192 bytes of RAM, which are both externally expandable to 64K bytes. Units provide synch/asynch serial communications interface circuitry, baud rate generator, and three 16-bit and one 8-bit timer/counters. Series is software compatible with the company's CMOS 8-bit HD6301V microprocessor, and upward compatible with NMOS HD6801S and HD68000. Features include 45 I/O lines, 8 output lines, memory interface, 88 instructions, error detection, and sleep/standby power save modes. **Hitachi America, Ltd**, 1800 Bering Dr, San Jose, CA 95112.
Circle 308

CMOS single-chip microcomputers

TMS70C00 and TMS70C20 microcomputers have typ power dissipation of 50 mW at 5 V and also feature a wakeup mode that dissipates 4 mW and a halt mode that typ requires 2 mW. TMS70C20, a CMOS version of the TMS7020 NMOS microcomputer, has 128 bytes RAM and 2K bytes onchip ROM. Features include 32 I/O lines, 1 internal and 2 external prioritized interrupts, an 8-bit timer with programmable 5-bit prescaler, 64K-byte address space, and a stack for control and data storage. The CMOS TMS70C00 ROM-less 8-bit micro is available for software development. Both devices are in 40-pin, 600-mil, plastic DIPs. **Texas Instruments, Semiconductor Group**, PO Box 401560, Dallas, TX 75240.
Circle 309

Floating point hardware for MC68000

SKYFFP for MC68000 microcomputers running on the Multibus or VME-bus is a single-card processor capable of 3-ms floating point add/subtract/multiply operations on 32-bit single-precision data, and 12-ms operations for 64-bit double-precision data. Square root, logarithmic, and trigonometric functions on IEEE std 32-bit single-precision and 64-bit double-precision floating point data can also be performed. Completely transparent to the user, processor requires no modification to existing FORTRAN, Pascal, or C programs. Runtime modules can replace existing software emulation subroutines. Price is under $1000 for OEM quantities. **Sky Computers, Inc**, Foot of John St, Lowell, MA 01852.
Circle 310

THE DAWN OF A NEW HORIZON

A State-of-the-Art Breakthrough Magnetic Amplifier Switcher Series

Rugged magnetic amplifier regulated switch-mode power supplies provide state-of-the-art efficiency plus power fail circuitry.

Elpac's 23 years of proven experience provides the **MASS-300** (300 Watts) - the first in a new family of multiple output, switch-mode power supplies.

Check these features:

- Typically 80% efficiency.
- State-of-the-art design employing high frequency, magnetic amplifier regulators for auxiliary outputs.
- High efficiency regulated auxiliary outputs result in saving storage energy in the input filter capacitors, therefore providing longer hold-up time.
- Power fail circuit monitors stored energy in the input filter.
- Power limited and thermally protected against excessive power conditions.

Now, check these specifications:

- **MASS-300** - The "Ultimate" of switching regulators at an affordable price of under $1.00 per watt in OEM quantities.
- Packaged in a convenient 1.6 watts per cubic inch (15.00" x 4.95" x 2.50") open or enclosed chassis.
- AC Input of 90-132/180-264 VAC at 47-440 Hz.
- DC Outputs: 5v, 25A (30A Peak); 12v, 4A (6A Peak); 12v, 4A (6A Peak); 24v, 4A (6A Peak).
- All outputs regulated.
- Full rated to 55°C with air flow.

Complies with Safety Specifications:
UL 478/1012*
CSA 22.2-154*
VDE804/5.72 (Class I)
*Recognition pending.

Elpac has a reputation where reliability comes first. We've done it again with **MASS-300**. Plus, a worldwide network of over 200 distributors providing fast, responsive delivery at an affordable price.

For detailed specifications on our new **MASS-300** or for a free catalog or applications assistance on our full line of power supplies and low power DC-DC converters, call or write today!

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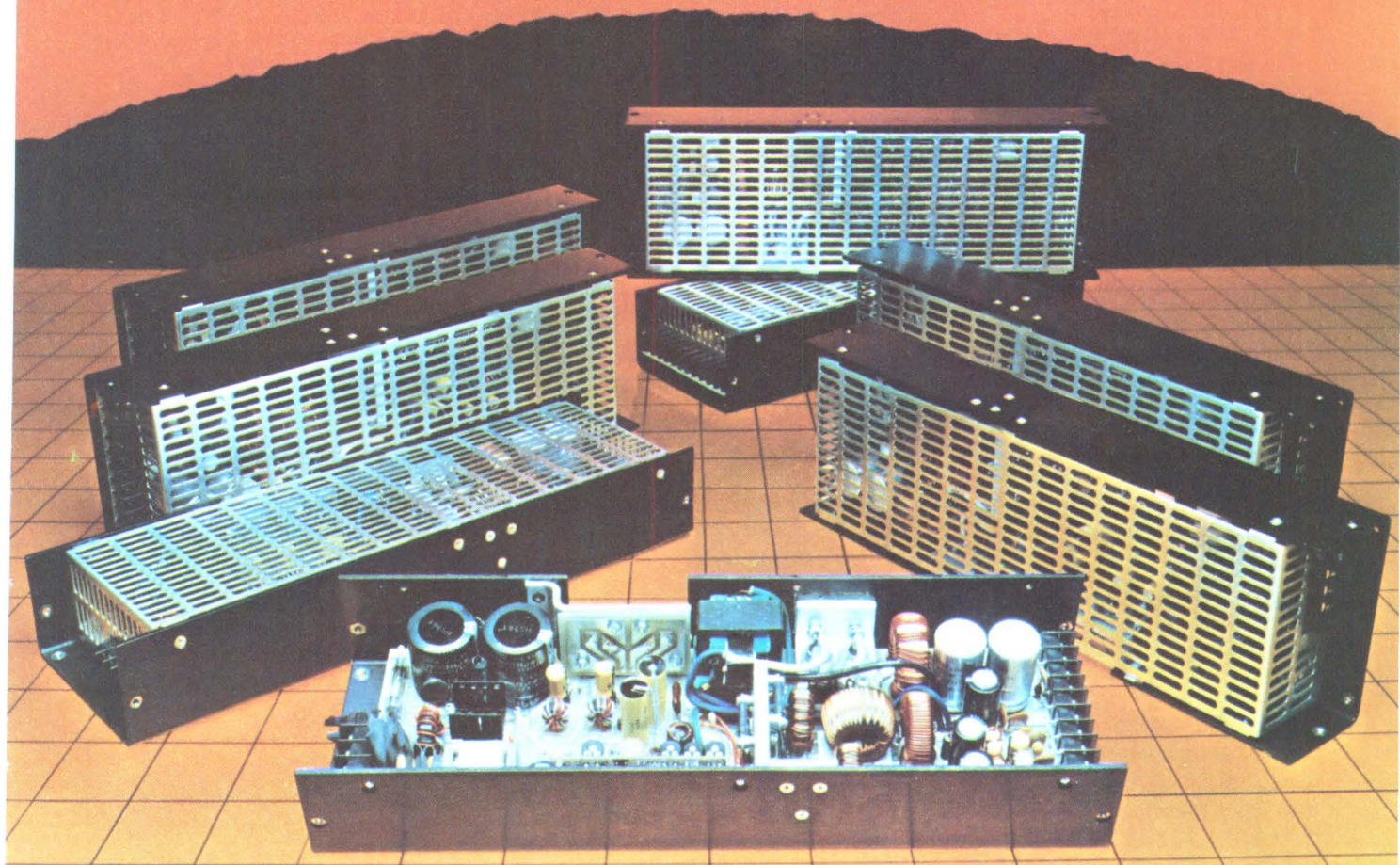
CIRCLE 139



MASS-300 SERIES

ANOTHER UGLY® Where Beauty is in the Performance

SYSTEM COMPONENTS/MICROPROCESSORS/MICROCOMPUTERS

User programmable, single-chip microcomputer

A user programmable version of the F3870 single-chip microcomputer, F38F70 is a complete 8-bit microcomputer on a single MOS IC with 2K-byte PROM replacing the 2K-byte ROM on the F3870. Programming is via a std PROM programmer and programming board. ROM code can be easily transferred to the F3870. The F38F70 ($29.70) executes the F8 system and F387X family instruction set of more than 70 commands and features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of TTL compatible I/O. **Fairchild Camera and Instrument Corp**, 3420 Central Expressway, Santa Clara, CA 95051.

Circle 311

Convection cooled single-board computer

DS1-4/6 single-board computer is packaged in an all-metal enclosure that measures 3.5″ x 7″ x 14″ (8.9 x 18 x 36 cm) and meets or exceeds all FCC Class A requirements for rfi shielding, as well as UL specs. Convection cooled enclosure acts as a heat sink. Unit requires no fan. The Z80 based microcomputer has 64K RAM, boot ROM, parallel printer and hard disk ports, up to 4 RS-232 ports, and disk controller. Controller interfaces with 5¼″ and 8″ drives in either single- or double-density formats. Series is available with either 4-MHz Z80A or 6-MHz Z80B microprocessor. In quantities of 500 or more, unit is $492.75. **Davidge Corp**, 1951 Colony St, Mountain View, CA 94043.

Circle 312

Expanded R6500 microprocessor family

R6501Q microprocessor contains separate address and data buses, 192 bytes of RAM, and can be used with external ROM or EPROM to implement a 2-chip system. Compatible with all R6500 family members, the micro uses an enhanced R6502 CPU with 4 new Boolean bit manipulation instructions—memory bit set, or reset and branch on bit set or bit reset. The 64-pin part provides 32 I/O pins via four 8-bit ports, two 16-bit programmable timers, a full-duplex serial port with programmable baud rates, and 10 interrupts. Sample quantity price is $28.20. **Rockwell International**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660. **Circle 313**

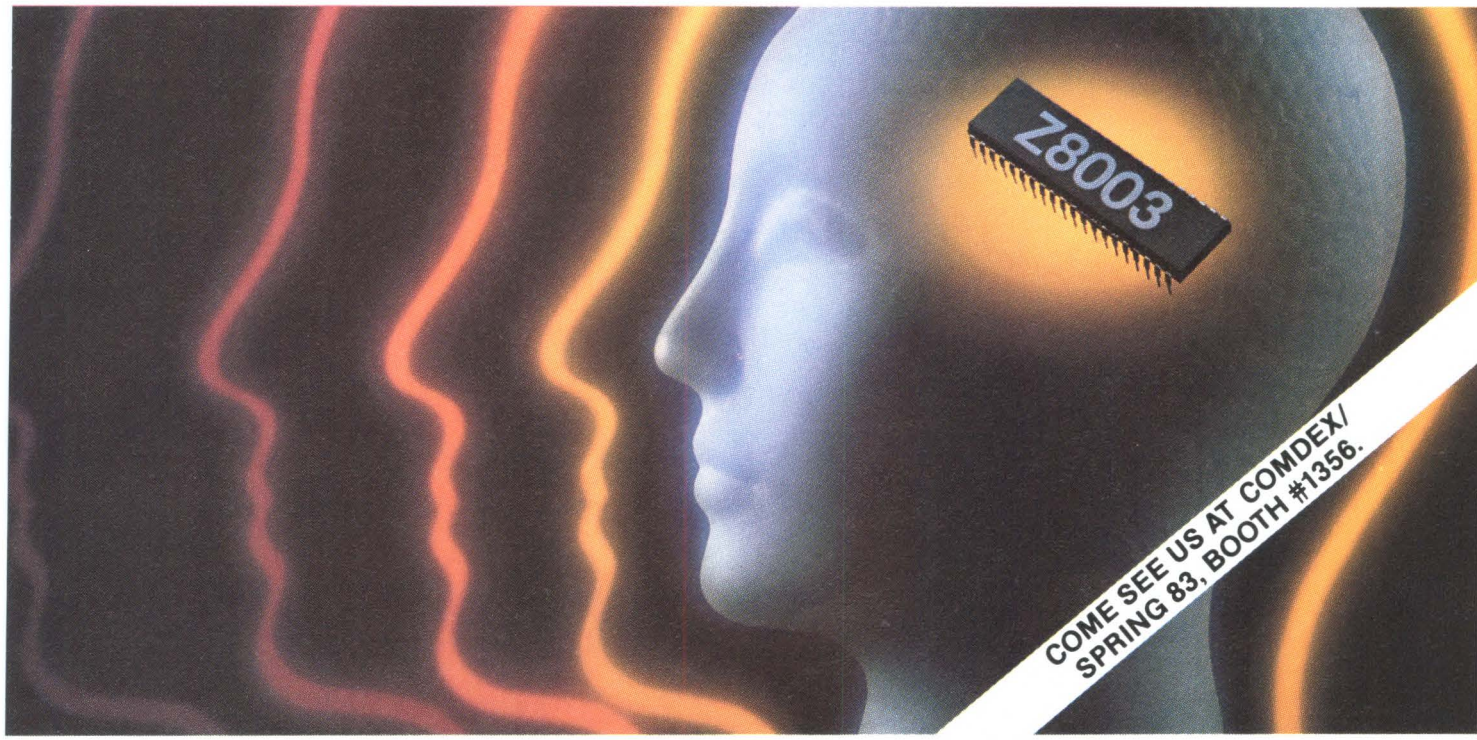
Fast data manipulation for text processing

The 82730 dedicated processor operates as a text coprocessor with Intel's line of 8- and 16-bit microprocessors. The chip performs concurrently with the system CPU to obtain its own data/instructions from memory and to execute them independently of, and in parallel to, the system CPU. Text can be displayed onscreen with proportional spacing, simultaneous super/subscript, dynamically reloadable fonts, and programmable field and char attributes. Enhanced editing and over 80 programmable options are provided. The processor can be paired with the 82720 graphics display controller chip for text processing with bit-mapped graphics. **Intel Corp**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 314

Like to write?
The editors invite you to write technical articles for Computer Design. For a free copy of the Author's Guide, circle **503** *on the Reader Inquiry Card.*

Now! Zilog adds virtual memory to the fastest 16-bit microprocessor you can buy.



Introducing Zilog's new generation of CPU's—the Z8003 with virtual memory. It lowers the cost of resident system memory, extends program-code portability and provides a convenient interface for large auxiliary storage. It's the ideal microprocessor for those big system applications.

The Z8003's virtual memory eliminates the need for program overlays, as well as the physical memory size constraints found in other chips. Programmers can design as if they had 16MB of physical memory. And users can run large programs more economically than previously possible with any other microprocessor.

A new Z8015 Paged Memory Management Unit (PMMU) adds dynamic memory relocation and protection capabilities to Z8003 systems. Each Z8015 handles sixty-four 2,048-byte pages of logical address space which map into 16 MB of physical memory.

The Z8015 contains additional features that assist the Z8003 in efficient implementation of virtual memory systems.

The Z8003 is the world's first 16-bit CPU with a 32-bit general-purpose register set. All arithmetic operations (including multiply and divide) are performed at remarkable speeds of up to 14 MHz. It brings you one step closer to Zilogs 32-bit CPU —a single chip which will have all the features of the Z8003 and Z8015.

To find out how the Z8003 virtual memory CPU and the Z8015 PMMU surpass what you're currently using, fill out the coupon and mail to: Zilog, Inc., Components Tech. Publishing, 1315 Dell Avenue, Campbell, CA 95008. Or call TOLL-FREE (800) 272-6560.

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Z8003/Z8015 CD 4/6/83

Zilog

Pioneering the Microworld.

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Draw Your Own Conclusions.

RESOLUTION
800 dot horizontal by 480 vertical high speed quality graphics.

TEKTRONIX 4014 EMULATION
Most all the Tektronix features are supported including: 4010 and 4014 Emulation, Plot 10 Compatible, 4096 by 4096 Addressable Plot Area, Variable Line Types, Point Plot, Vector Plot, Incremental Plot, and Write Through Mode.

SPECIAL FEATURES
Selanar Native Mode Command Structure, Area Fill, Circle, Arc and Box Commands.
Also variable scale factor for changing image size, relocatable origin, special write modes, swtichable video, and built in crosshair feature and more.

SINGLE BOARD DESIGN
The SG480 is a small single board design (4.5 by 5 inches) and simply plugs into the VT100 STP port. Only one small cable is required. The SG480 comes with a replacement CRT tube and attached yoke – simple installation without critical adjustments.

DEC TERMINALS SUPPORTED
VT 100, VT132
In addition Selanar has comparable products for the VT101 and VT102 plus other products for the VT100, VT103, VT105, and VT180.

HARDCOPY
Hardcopy is available for several printers, including DEC LA34 format. Options currently available are for C.Itoh, Epson, Data South, Texas Instruments, and Selanar's SG120 PLUS with DEC's LA120.

Call Selanar Today. Tomorrow's Already in the Works.
For more information about our revolutionary 480 VT100 Graphics Feature — or any of the Selanar graphics retrofit products — give us a call. Low cost graphics never looked so good.

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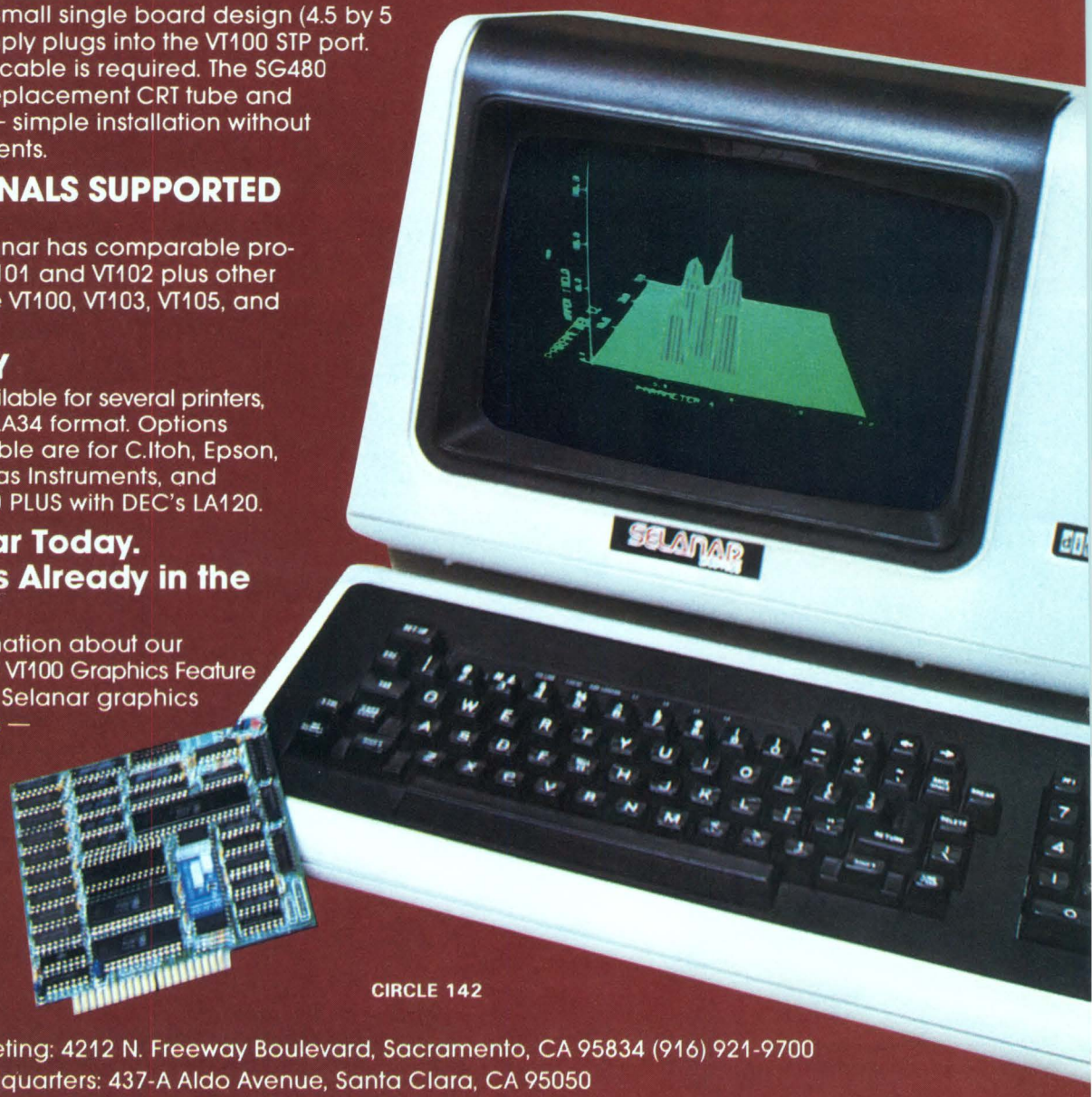
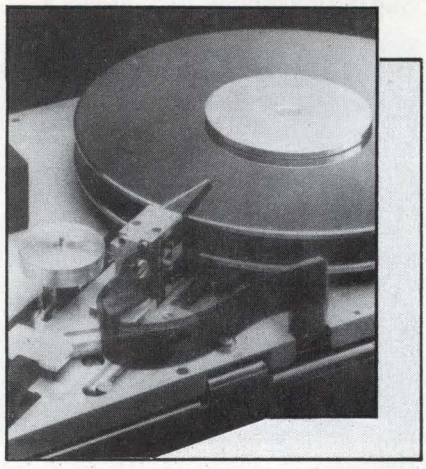
graphics enhancement



CIRCLE 142

Sales and Marketing: 4212 N. Freeway Boulevard, Sacramento, CA 95834 (916) 921-9700
Corporate Headquarters: 437-A Aldo Avenue, Santa Clara, CA 95050
European Headquarters: Selanar GmbH, Ahastrasse 5, 6100 Darmstadt, West Germany

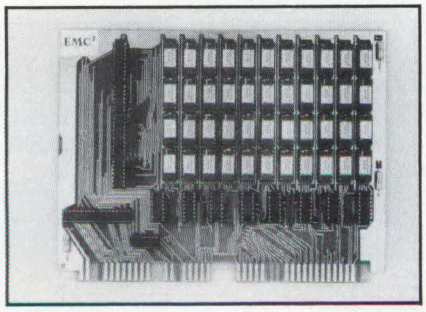
Half-height Winchester



Cogitator series I slimline Winchester disk drives include model 906, which stores 6.38M bytes on 1 platter, and model 912, which stores 12.76M bytes on 2 platters. Compatible with the ST506/412 std interface, both drives have average access time of less than 85 ms, including settling. Thin-film plated media are utilized and dynamic braking systems stop the disk within 4 s after head touches down. Mn/Zn composite R/W head is mounted on an IBM 3370 type suspension. Packages measure 1.625″ x 5.75″ x 8″ (4.128 x 14.61 x 20 cm) and are powered by std dc voltages. **Cogito Systems Corp**, 118 Charcot Ave, San Jose, CA 95131.
Circle 315

Wang compatible memory boards

The VM and VS series memory cards provide all main memory requirements for Wang VS-50, -80, -90, and -100 central processors. Memory capacity of VS-50 and -80 can be expanded with the VM-8 128K-byte and/or VM-12 256K-byte card. The larger VS-90 and -100 machines are expanded with either the 1M-byte VS-4A, 512K-byte VS-2A, or 256K-byte VS-1A cards. All cards are hardware/software compatible with the Wang host processor. They are interchangeable with the Wang memory boards, require no modifications, and are installable in less than 15 min. **EMC Corp**, 385 Elliot St, Newton, MA 02164.



Circle 316

LSI-11 add-in memory with calendar/clock

Compatible with LSI-11/2 and LSI-11/23 microcomputers, MM-1123C family of add-in memories provides up to 64K bytes of nonvolatile storage and an onboard calendar/clock. Family operates with 16-, 18-, and 22-bit address Q-bus backplane and is available in either rechargeable or nonrechargeable battery versions. Realtime calendar/clock also provides programmable periodic interrupt that is switch selectable on 16-byte boundaries of the I/O page. Board's battery status line can be jumpered to 1 of 256 locations in the I/O page for host computer monitoring of battery condition. The MM-1123CC/64 64K-byte rechargeable memory board is $875. **Micro Memory, Inc**, 9436 Irondale Ave, Chatsworth, CA 91311.
Circle 317

Nonvolatile 64k x 8 RAM module

NVR64 64k x 8 nonvolatile memory module measures 4″ x 2″ x 1″ (10 x 5 x 3 cm) and features 135-ns cycle time. With 10-year data retention, an unlimited number of R/W cycles, and 5-V operation, this internally buffered unit connects directly onto the microprocessor bus. Up to 8 units fit on an S-100 card, or 4 on a Eurocard. Up to 0.5M-byte memory can be added without significant system redesign. **Greenwich Instruments Ltd**, 22 Bardsley Ln, Greenwich, SE10 9RF, London, England.
Circle 318

256K-bit CMOS RAM module

HM-92560 low power 256K-bit CMOS RAM module is built using 16 synchronous HM-6516 2K x 8 CMOS RAMs. Devices are packaged in LCCs and mounted on a multilayer ceramic substrate. Module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data I/O buses and chip enables allow the user to format the module as either a 16K x 16 or 32K x 8 array. Ceramic substrate capacitors reduce noise and minimize need for additional external decoupling. Address access time is 170 ns, operating current is 30 mA/MHz max, and standby current is 500 μA guaranteed over industrial and military temp ranges. The 48-pin DIP has 0.1″ (0.3-cm) centers between pins. Prices range from $605 to $2332. **Harris Corp, Semiconductor Group**, PO Box 883, Melbourne, FL 32901.
Circle 319

Low cost, ½ " tape drive alternative

CacheTape 75 ½ " 75-ips tape drive provides file sort capabilities and tape processing. Online backup functions allow continuous primary processing without interruption, while the tape provides background file save/restore functions. The tape drive backs up 80M- to 300M-byte Winchesters. A 3200-bpi version provides 93M bytes of unformatted capacity on a std tape reel. It is fully software transparent with existing vacuum column and tension arm software. OEM quantity price is $2820. **Cipher Data Products, Inc,** 10225 Willow Creek Rd, PO Box 85170, San Diego, CA 92138. **Circle 320**

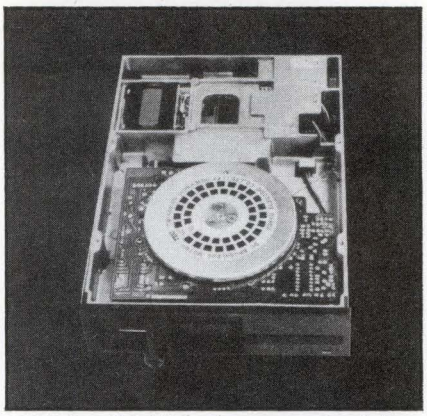
5¼ " Winchester drives removable, fixed, and dual media

Cardiff family of 5¼ " fixed and/or removable media Winchester drives are fully compatible with available microcomputers and controllers in size, power requirements, interface, and data transfer rate. Voice coil linear motor configuration makes possible high speed dynamic positioning of the R/W heads with no increase in drive depth over std 5¼ " floppies. Embedded servo information allows 3 times greater track densities than is possible with open-loop stepper positioning systems. Five models are available, ranging in unformatted capacities from 20M to 80M bytes. Formatted capacity is 15M bytes/disk. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.
Circle 321

Low cost SMD compatible 14 " Winchester

AMS 513 14 " 513M-byte Winchester disk drive is SMD interface compatible and combines a 32k-byte/track capacity with a 5-platter configuration that utilizes 19 data heads reading 10k bpi. Unit includes a basic drive, power supply, and desktop enclosure. Selectable dual access is optional. Sealed contamination controlled disk compartment, ventilated spindle, spin motor brake, carriage lock, and dedicated landing zones are featured. Drives are priced at $7900 for OEM 50 to 99 quantities. **Century Data Systems,** 1270 N Kraemer Blvd, PO Box 3056, Anaheim, CA 92803.
Circle 322

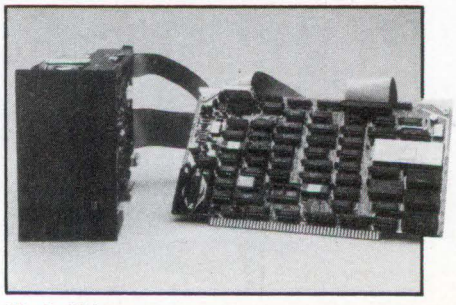
Super thin floppy disk drives



Half-size 5¼ " floppy FB500 series drives have an unformatted storage capacity range from 250K to 1K bytes. Track to track access for double-density 96-tpi model ($170) is 3 ms. Single-density 48-tpi model ($112) has track to track access of 6 ms. Dimensions are 41 x 146 x 209 mm. Shugart plug compatible interface is included. Stepping motors, direct drive brushless dc motors, and Mn-Zn Fe ceramic heads are used. **Nissei Sangyo America, Ltd,** 40 Washington St, Wellesley Hills, MA 02181.
Circle 323

5¼ " hard disk subsystem for S-100 computers

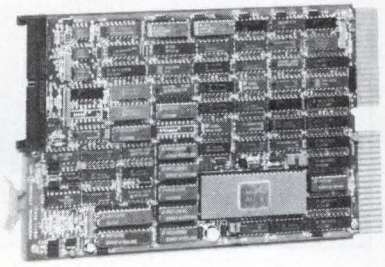
Built around the company's HDC-1001 error correcting hard disk controller board, a 5¼ " Winchester disk subsystem for S-100 microcomputers is available in 5M-, 10M-, 20M-, and 40M-byte configurations. Controller board has an onboard microprocessor and provides control for up to 4 drives and up to 8 R/W heads. Data separation is built in, and the subsystem provides up to 5M-byte/s data rates, 256 sector addressing range, CRC generation/verification on ID fields, unlimited sector interleave, auto-retry on all errors, and auto-restore and reseek on seek error. Subsystem comes with the controller board, connector cable, CP/M BIOS disk, and hard disk drives. **Advanced Digital Corp,** 12700 B Knott Ave, Garden Grove, CA 92641.



Circle 324

GET THE POWER YOUR Q-BUS SYSTEM WAS DESIGNED TO GIVE

It's Plug-In Simple with Remarkable DEC-Compatible Technology from Andromeda Systems



The WDC11 Triple Function Compatible Controller: Its Power is Amazing Versatility

Interfaces with 8- and 5¼-inch Winchester and floppy disk drives, and includes an intelligent bootstrap ROM. This LSI-11 compatible Controller emulates these standard DEC devices: RK-05, RL-01/2, RP-02, RX02.

That's only a **sampling** of the freedom of selection you have with the WDC11 Controller. It adds performance to your LSI-11 computer system. Easily and cost-effectively.

Winchester Add-On Subsystems: Their Power is Speed, Storage Capacity, Reliability, Compactness, and Low Cost

Get major throughput gains from your LSI-11 floppy-based system at a cost you can live with. Andromeda's popular MDS series, with a 5¼-inch Winchester drive, has a data transfer rate **over eight times** that of an RX02 floppy! Standard DEC emulations are available. Includes built-in bootstrap and formatting.

All Andromeda Winchester Subsystems will quickly and conveniently cover your mass storage needs for today and tomorrow.

Complete Turn-Key Computer Systems: Their Power is Big Overall Performance for Small Space and Cost

One totally integrated package includes computer and disk drives. For example, the 11/M1-W (pictured) holds a standard 5¼-inch Winchester disk drive, 2 x 5 card cage, control panel, and power supply.

Andromeda Turn-Key Computer Systems are easily expandable, and may be custom-configured to fit your processing requirements, space constraints and budget. Specify 8-inch disks if you wish, or dual drives, or floppies...or a combination.

Andromeda is the Q-Bus specialist. Our single objective is to develop fine products that unleash the power that is inherent in your DEC LSI-11 system.

Call or write today for more information. We'll be in touch.

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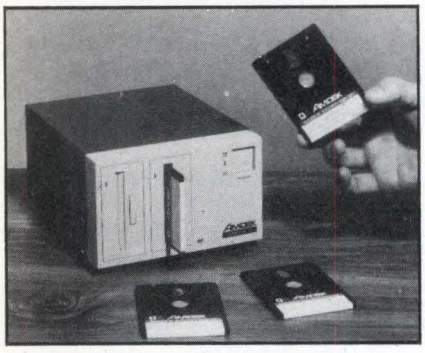
CIRCLE 145

3″ floppy drive evaluation samples

Micro-Floppydisk 3″ drive system and 4 Micro-Floppydisk cartridges can be evaluated by OEMs for $480. The dual-disk drive system provides 1M-byte unformatted storage, has built-in power supply, and accommodates two 3″ floppy disk cartridges. Recording format, data transfer rate, and disk rotation speed are compatible with 5¼″ std floppies. Recording capacity is 125k bytes single sided or 250k bytes double sided, with double-density (500k bytes) capability. Write protect mechanism ensures read only status for recorded data. **Amdek Corp,** 2201 Lively Blvd, Elk Grove Village, IL 60007.



Circle 325

1.4G-byte disk drive with 12M-byte/s transfer rate

Model 1400 1.4G-byte disk drive transfers at 12M bytes/s and is based on the company's proprietary thin-film media with modified ferrite heads. Density is greater than 15k bpi. Onboard microprocessor allows self-test diagnostics that operate automatically during power-up and continuously monitor the drive's operating condition. With an auxiliary embedded servo, drive provides dynamic track following adjustments while in warm-up mode. Initial shipments are scheduled for first quarter 1983. **IBIS Systems, Inc,** 1850 Evergreen Dr, Duarte, CA 91010.

Circle 326

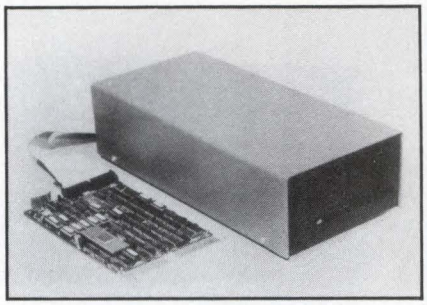
32K-byte CMOS RAM for STD bus

Multiwire mil spec high density circuit board combines area density of wire-wrap with minimal thickness of PCBs for discrete pin to pin insulated wire without the pin wrapping for termination. Using Multiwire, the 6″ x 4″ (15- x 10-cm) STD bus RAM card provides 32K bytes, onboard rechargeable battery backup, write protect switch, 4k boundary protect switches, and low power consumption. **Kennor Holdings Pty Ltd, Kennor Computing Div,** 38 McCoy St, Myaree, PO Box 94, Applecross, Western Australia, 6153.

Circle 327

Winchester upgrades floppy based Q-bus systems

Mini Disk System (MDS) family of Winchester mass storage subsystems provides storage capacities of 5M, 10M, 15M, and 20M bytes. Subsystems are fully compatible with LSI-11/2, -11/23, and -11/23-Plus processors. Package includes the WDC11 dual-width controller card, 6′ (2-m) cable, and drive chassis. Chassis can be used desktop or mounted behind the host system. Controller emulates RK05, RL01/02, and RP02 disks. Intelligent bootstrap for startup and RLV12 compatible 22-bit DMA are included. Prices range from $3995 to $5700. **Andromeda Systems, Inc,** 9000 Eton Ave, Canoga Park, CA 91304.



Circle 328

CMOS RAM module with battery backup for AIM/RM65 systems

Nonvolatile single-card memory module GE65-12K provides up to 12K of CMOS RAM with battery backup and is fully compatible with Rockwell AIM and RM65 microcomputer card systems. It is provided in a Eurocard version to plug into a Rockwell RM65 card cage or AIM buffer adapter. Capacities of 2K to 12K in 2K increments using 2K x 8 CMOS static RAM circuits are available. Card accepts 2716 type EPROMs. All address, data, and control lines are buffered. Max memory access time in std version is 200 ns; higher speed memories are available. With 2K memory, price is $235. **Golden Electronics Inc,** 2133 Yorktown, Ann Arbor, MI 48105.

Circle 329

WINCHESTER BACKUP/ DATA BASE MANAGEMENT!

Model 451 — serpentine write
Model 450 — standard write

Back-up your Winchester with the new Model 450 or 451 cartridge tape drive. With the capability of a full tape peripheral, the new Qantex drive can be used to perform file search, update records, and edit/reformat data.

Designed for disk backup as well as archival storage or data logging applications, the 450/451 packs 17.2 megabytes on a single data cartridge, with a packing density of 6400 bpi and 192,000 bits per second transfer rate.

Both models incorporate a rugged transport mechanism with a precision servo motor. Model 450 offers a standard, and Model 451 a serpentine recording head. Read-after-write dual gap and selective erase are standard features of both models.

The serpentine tape drive features a special read-after-write recording head that provides bi-directional tape operation avoiding time-consuming rewind time.

The new Model 450/451 is available now! Contact us today for complete details!

Qantex*

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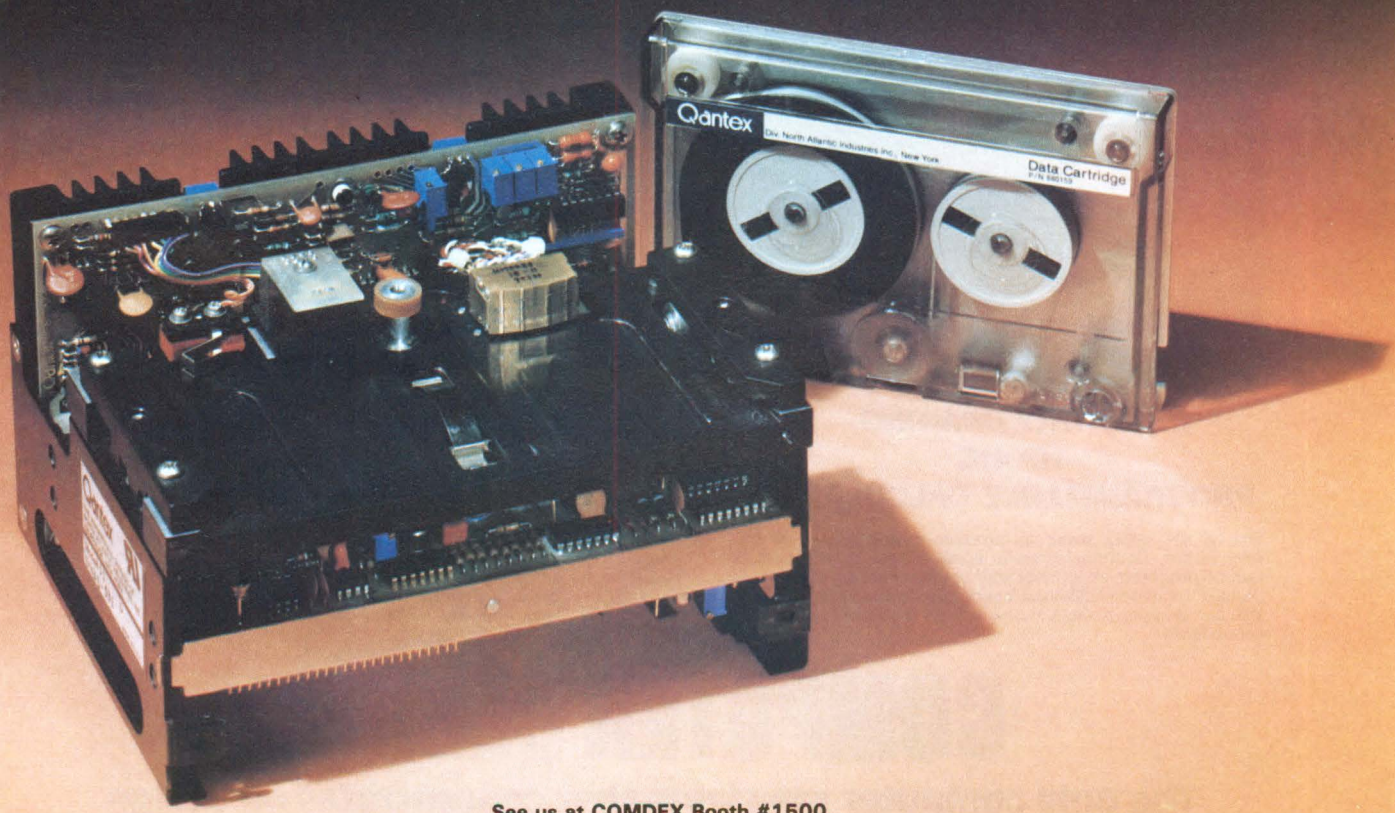

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CIRCLE 147

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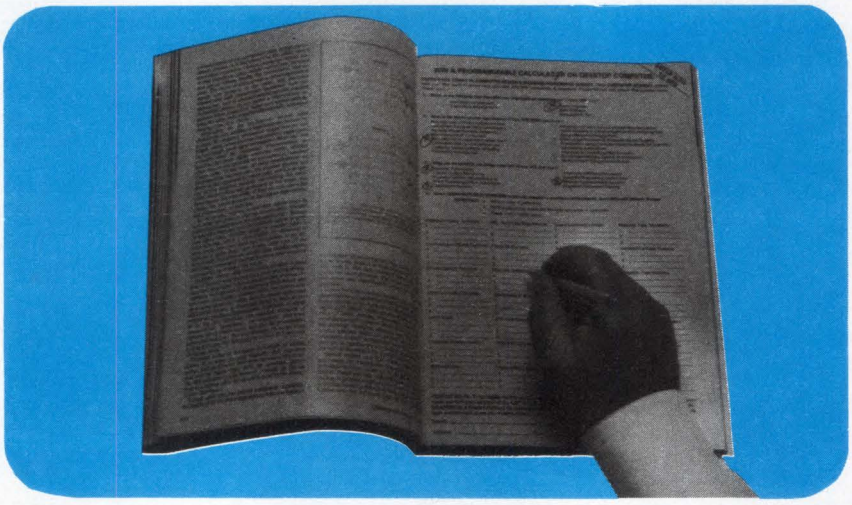
YOU MAY WIN A VALUABLE PRIZE IN THE PROCESS

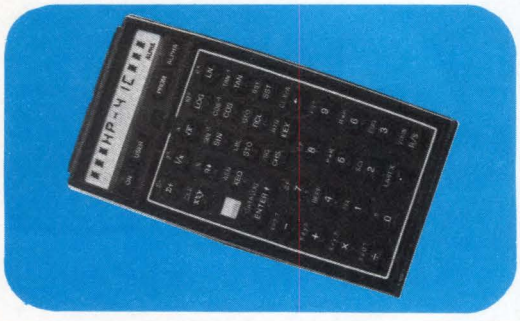


In every issue of *Computer Design* you'll find a bound-in survey questionnaire entitled "Designer Preference Survey." Your participation in these surveys is important. Your answers are significant. They tell our editors what's going on in the marketplace, what kinds of systems you are designing, how your product choices are shaping up, what products, subsystems, equipment and components you are using or would like to use.

The answers you supply can guide our editors in selecting the topics, features, and technical data that will be on target with the kinds of projects you are working on.

The questionnaires also alert manufacturers to your needs. The inputs you give us help them to develop products with the speeds, ranges, capacities, etc. that you require.

As an added incentive, each questionnaire returned gives you a chance to win a valuable prize. Drawings are made each month, with a grand prize drawing at year end.



MONTHLY DRAWING
HP 41C
PROGRAMMABLE CALCULATOR

The HP 41C offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total operations in function library. You can add peripherals and extension modules to expand capabilities.

ANNUAL DRAWING
HP 85
DESK TOP COMPUTER

This portable (20#) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56 K byte memory, CRT screen, and 150 built-in HP BASIC language commands. You can add peripherals and software packages to expand system capability. A $2800 value!

COMPUTER DESIGN

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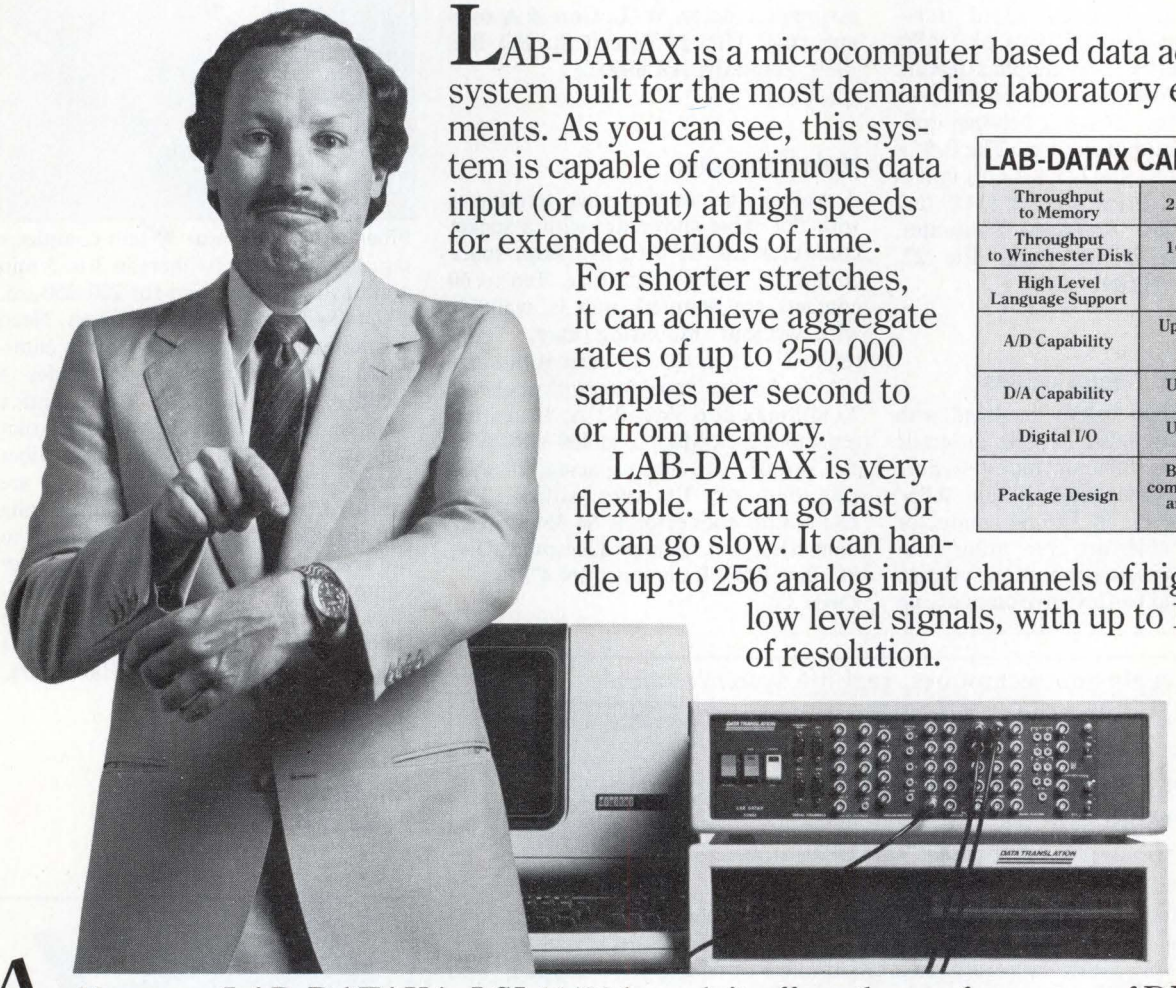
"Over 2 minutes at 100,000 A/D samples per second and LAB-DATAX hasn't missed a data point."

Fred Molinari, President



LAB-DATAX is a microcomputer based data acquisition system built for the most demanding laboratory environments. As you can see, this system is capable of continuous data input (or output) at high speeds for extended periods of time.

For shorter stretches, it can achieve aggregate rates of up to 250,000 samples per second to or from memory.

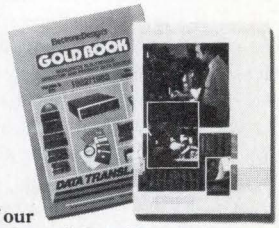
LAB-DATAX is very flexible. It can go fast or it can go slow. It can handle up to 256 analog input channels of high level or low level signals, with up to 16-bits of resolution.

LAB-DATAX CAPABILITIES	
Throughput to Memory	250 kHz at 12 bits
Throughput to Winchester Disk	100 kHz at 12 bits
High Level Language Support	BASIC and FORTRAN
A/D Capability	Up to 256 channels, 12-14-16 bits resolution
D/A Capability	Up to 32 channels at 12 bits
Digital I/O	Up to 64 channels input/output
Package Design	BNC connections, complete separation of analog and digital signals

And because LAB-DATAX is LSI-11/23 based, it offers the performance of DEC's hottest microprocessor. And it's compatible with the LSI-11 family of products. Including over 50 of our analog I/O peripherals and our DTLIB, CPLIB, RSXLIB, and DTBASIC software packages.

Naturally, LAB-DATAX comes with complete diagnostics, full documentation, and comprehensive warranty and service support.

This system was designed by the most innovative company in analog I/O. There's none to match it.



For a copy of our 336 page catalog call Data Translation. Or turn to Volume 111 of the Gold Book.

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951-646.
European Headquarters: Data Translation, Ltd., 430 Bath Rd., Slough, Berkshire SLI 6BB England (06286) 3412 Tlx 849-862.

Fiber optic wavelength multiplex/demultiplex couplers

WC4200 series of wavelength multiplex/demultiplex fiber optic couplers can transmit 2 channels over 1 optical fiber. Two low cost moderate speed transmitters can be used in place of 1 high speed transmitter. The couplers feature low insertion losses and high port to port isolation for low crosstalk between optical channels in duplex links. The 0.5″ x 0.5″ x 3.2″ (1.3- x 1.3- x 8.1-cm) unit is PC mountable. Prices start at $1450 in 2 to 8 quantities. **American Photonics, Inc**, Milltown Office Park, Rte 22, Brewster, NY 10509.
Circle 330

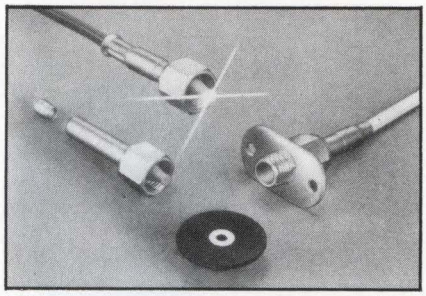
Insulated IDC ribbon cables

A line of ribbon cables insulated with Gore-Tex® Expanded PTFE (a dielectric material that is 70% air and 30% pure polytetrafluoroethylene) is on 0.05″ (0.13-cm) centers. In 2 to 64 conductor widths, the cables are compatible with all mass termination connection systems. They are suited to flex environments up to 50M cycles, airborne electronics, high temp cable routing, and where chemical immunity is needed. The cables provide low dielectric constant, low crosstalk, light weight, fast signal speed, and a low dissipation factor. **W. L. Gore & Associates, Inc**, 1505 N Fourth St, PO Box 1389, Flagstaff, AZ 86002.
Circle 331

Male connector

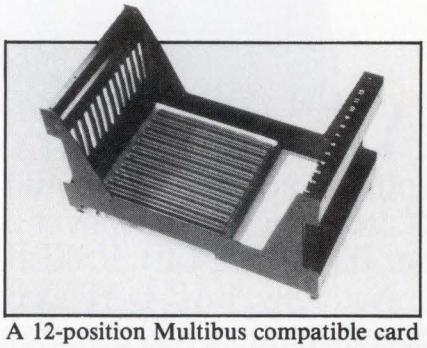
A male connector that mass terminates with flat cable and mates with a socket connector can be used as T-tap, splice connector, and I/O interface. Ten to 60 contacts are featured; unit is available with/without mounting ears. Temp range is −55 to 105 °C; current rating is 1 A dc; contact resistance with socket is 20 mΩ max at 6 Vdc, 0.3 A. Insulation resistance is 1k MΩ min at 500 Vdc. Wire size is 0.05″ (0.13-cm) spacing, 28 AWG stranded or 30 AWG solid. The 10-position connector is $4.36. **Cooper Industries, Inc, Belden Electronic Div**, PO Box 1980, Richmond, IN 47374.
Circle 332

Fiber optic connector uses no adhesive



Fiber optic connector system completes termination of glass fibers in 3 to 5 min and has unitized design for 200/250-μm, 100/140-μm, and 50/125-μm fibers. Need for adhesives to retain the fiber is eliminated. Preassembled plug includes a metal retaining assembly (MRA) and a resilient ferrule. Ferrule has insert that houses 3 metallic rods to form fiber clamp. Cable's strength members are captured between a jacket retention ring and the MRA when a crimp is applied to the rear of the plug assembly. Another crimp on the MRA barrel forms and activates the metal rods of the fiber clamp for a mechanically stable grasp on the stripped fiber. **AMP Inc**, Harrisburg, PA 17105.
Circle 333

Multibus card rack with noise immunity



A 12-position Multibus compatible card rack runs all signal lines between 2 parallel ground lines. A ground line runs directly under the signal on the other side of the backplane. Effects of crosstalk between critical signals and ringing are minimized. Backplane also features parallel priority, −5-V regulator, and reset switch options. PCB hold-down bars secure plugged-in cards and can be slid aside for easy card removal. Numbered card slots are on 0.6″ (1.5-cm) centers. Sideplate kit accommodates 19″ (48-cm) cabinet mounting and cooling fans. **Mupac Corp**, 10 Mupac Dr, Brockton, MA 02401. **Circle 334**

Put a little tape backup in your DEC microcomputer.

SMS' DSX-11 is a complete DEC microcomputer with 80Mb Winchester and ¼" cartridge tape backup. With over 20Mb per tape cartridge, Winchester backup has never been so easy. Emulating DEC's latest TS11 tape device, standard RT-11 and RSX-11M software makes disk backup, system boot, media interchange, archiving and software distribution a snap!

256Kb main memory (expandable 4Mb)

Expansion space for 15 dual height modules.

LSI-11/23 16 bit CPU with memory management.

4 Serial ports.

Advanced disk controller with ECC, flaw management, bootstrap, error retry and non-interleaved data transfer.

PDP-11* architecture compatible with RT-11, RSX-11M and UNIX** software.

7.8Mb, 35.6Mb or 71.2Mb Winchester disk.

Self test with LED display of system faults.

Start/stop tape supports file operations.

Compact 3M Cartridge.

APE CONTROLLER ONLY AVAILABLE FOR VOLUME REQUIREMENTS.

* Trademark of Digital Equipment Corporation. ** Trademark of Western Electric.

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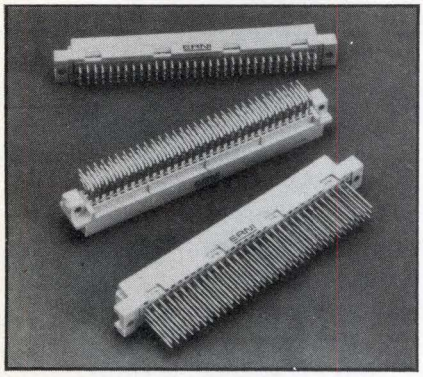
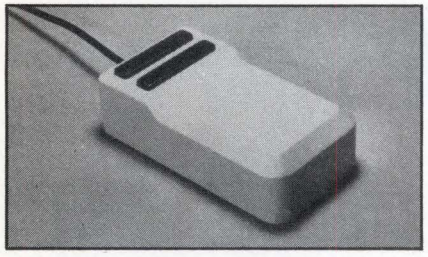
Polyester DIN connectors withstand 220 °C



Series STV-B (2-row) and STV-C (3-row) connectors, molded from polybutylenterephtalate (PBTP), meet DIN 41612 specs and withstand soldering up to 220 °C. The glass-filled polyester material combines electrical characteristics with high resistance to chemicals and solvents. Socket spring elements provide low, constant contact resistance and high contact pressure with low friction. Polarized bodies prevent accidental mismating and enclosed contact areas prevent damage to contacts. **ERNI Components Corp,** 1235 E Davis St, Arlington Heights, IL 60005.
Circle 335

PERIPHERALS

Smart optical mouse positioner



OptoMouse cursor controller encloses 2 rocker switches that roll on the X-Y axes of a flat surface, and communicates its movements to the computer and interface by a tail-like cord. Custom optical imaging system is incorporated for superior resolution. Unit requires only 5 V from the host system. Controlled by its own microprocessor, it is designed with min parts count and can emulate existing graphics protocols such as Tektronix Plot 10 and Summagraphics bit pad. Host interface is via RS-232-C serial port. **USI International,** 71 Park Ln, Brisbane, CA 94005.
Circle 336

Graphics terminal compatible with Template software

The G-1000 high resolution 16-bit microprocessor based raster graphics terminal is compatible with Megatek's Template software. The host-independent software package supports both batch and interactive applications and features a large subroutine library. Template allows writing of a software driver, which takes advantage of the terminal's hardware features to offload the host computer. Template exploits G-1000 features like textured lines, 4 char sizes, point/plot mode, scroll, user-defined initial cursor position for input, selective erase by vector/area, and alphanumeric overlay. **Genisco Computers Corp,** 3545 Cadillac Ave, Costa Mesa, CA 92626.
Circle 337

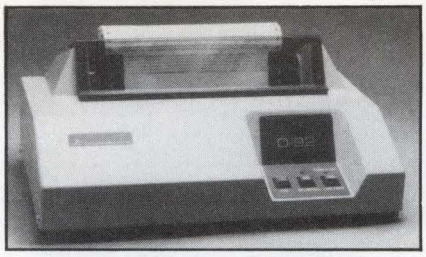
Tailless mouse

Without an attached cable, the Datawafer system mouse cursor can be moved, unhindered, above the 0.2″ (0.5-cm) position detector. Positioning information is transmitted any time the mouse is moved 3″ (8 cm) on or above the desk wafer surface. Cursor-positioning system contains a battery powered mouse, a wafer embedded with all passive position detecting elements, and optional electronic circuitry for signal conversion and interface with data processing equipment. **Display Interface Corp,** 525 Post Rd, Milford, CT 06460.
Circle 338

Color graphics CRT

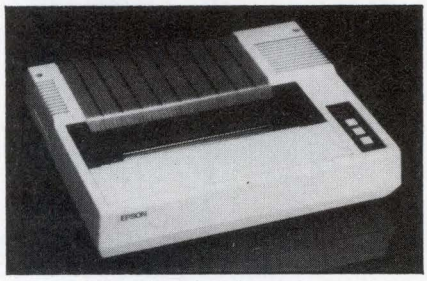
CD-2053D 20″ (51-cm) color CRT monitor uses self-convergence, inline technology, and a 0.31-mm dot pitch matrix. The TTL CRT produces red, green, blue, yellow, magenta, cyan, and white colors. Horizontal sweep frequency is 24.2 kHz; vertical sweep is 54 Hz. Recommended display density is 3040 chars in a 7 x 9 dot pattern. Text processing density is 38 lines of 80 chars. Built-in circuitry includes CRT block, RGB video amplifier, horizontal/vertical deflection circuits, high voltage supply, power supply with voltage regulator, high voltage limiting circuit, and autodegaussing circuit. Max power consumption is 150 W. **Nissei Sangyo America, Ltd,** 40 Washington St, Wellesley Hills, MA 02181.
Circle 339

Reduced price printer



Dual-mode printer D-92 is available for $399/unit, a 42.5% price decrease over the previous cost. Modular design enables specific upgrade selections by users. Dual-mode operation uses a 7 x 9 matrix font and an 11 x 9 matrix for near letter quality documents. Features include 100-cps bidirectional printing, short line seeking logic, friction paper feed, parallel interface, 800-char buffer, 6 char sizes with each printing mode, 100M-char reusable printhead, and a 5M-char continuous loop ribbon cartridge. Full ASCII char set prints both upper- and lowercase chars at 40, 48, 66, 80, 96, or 132 chars/line. Options include RS-232-C serial interface, adjustable tractor feed, dot addressable graphics, 9600-baud operation, 2K buffer, X-ON/X-OFF, control X/Y, and single-sheet feeder. **Data Impact Products, Inc,** 745 Atlantic Ave, Boston, MA 02111.
Circle 340

160-cps, 4-density printer



FX-80 bidirectional printer has 160-cps print speed and software selectable choice of elite (12-cpi) or pica (10-cpi) print spacing. Users can download special fonts into memory from the computer system. The 9 x 9 dot-matrix print has the same 1:1 graphics scale vertically as horizontally. Dot-addressable graphics capability and 2K-byte buffer are provided. Printer ($699) provides chars with full descenders and is downward compatible with the Epson MX printer series. Proportional spacing, pin- and friction-feeds, and std parallel communications interface (serial or IEEE 488 interfaces optional) and 4 printing densities are featured. **Epson America, Inc,** 3415 Kashiwa St, Torrance, CA 90505.
Circle 341

NEW... from DATARAM

MOTOROLA VERSAbus 1.0 MB ADD-IN

Not just more capacity; more capability

Motorola's 68000 is a winner, and using this popular microprocessor in a VERSAbus/VERSAboard configuration is a smart move. Dataram's new single-board 1.0 MB DR-680 can make it even smarter. Increased single-board memory capacity means lower power, less space, higher reliability, and lower cost...and the DR-680 provides a lot more!

More speed: Ability to perform match cycles reduces access/cycle times by allowing immediate reading of data registers when adjacent words/bytes are accessed.

Advanced error handling: The DR-680 provides an on-board control and status register (CSR) which allows program control of ECC functions and contains the diagnostic information required for error analysis. The CSR can be read or written via the VERSAbus. Additionally, the DR-680 greatly increases reliability by performing error "sniffing" and error "scrubbing" during refresh operations.

Availability: Best of all, the 1.0 MB DR-680 is available now. And it comes with Dataram's standard one-year warranty.

For more information, send in the adjacent coupon or, for faster response, call Dataram today at (609) 799-0071.

VERSAbus and VERSAboard are registered trademarks of Motorola, Inc.

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CIRCLE 178

Low cost optical mouse

Summa:Mouse combines a solid state optical system with microcomputer processing to eliminate slips/skips. User need not press down or rock the mouse during operation. Fully compatible with the company's MM series digitizers, the mouse also offers Bit Pad, MM series, and Tektronix PLOT 10 formatted protocols. The handheld unit has 3 push buttons for tactile feedback. Auto-baud feature sets serial transmission rate to that of its host, or presets to a 300- to 9600-baud range. RS-232 and TTL level outputs are available without external hardware. **Summagraphics Corp,** 35 Brentwood Ave, Fairfield, CT 06430.
Circle 342

Half-inch tape with extended gap start/stop performance

Vindicator ½″ streaming tape drive is an auto-loading, drawer mount transport with extended gap start/stop performance suitable for nonstreaming applications. Extended gap feature is front panel selectable from 0.6″ to 10″ (1.5 to 25 cm). Tape provides either 46M- or 92M-byte unformatted capacity. Auto-power restart and load online commands bring the drive back to ready state after a power failure. Data transfer rates are 40k bytes/s (25 ips, 1600 cpi) to 160k bytes/s (100 ips, 1600 cpi). Nominal access time in 100-ips mode is 240 ms read or write. Price is $2825; volume discounts are available. **Pertec Peripherals Corp,** 9600 Irondale Ave, Chatsworth, CA 91311.
Circle 343

Third generation APL terminal

Model 16-APL user definable multipage APL editing terminal is ANSI X3.64 compatible and features true char overstrike and instant replay. The 385 displayable chars include 96 APL, 128 ASCII, 64 mosaic, 32 line drawing, and 32 sub/superscripts, plus 33 special symbols and math notations. Its 4-page display memory can be expanded to 8 volatile/nonvolatile pages. Terminal displays a 24-line x 80-col page. Two fully buffered bidirectional RS-232 ports and 9″, 12″, and 15″ (23-, 30-, and 38-cm) CRTs are provided. **Research Inc, Teleray Div,** PO Box 24064, Minneapolis, MN 55425.
Circle 344

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Relief for terminal headaches.

Panasonic believes that terminal ergonomics should begin at the CRT screen. Fuzzy characters, excessive brightness, distracting glare and reflections can all lead to operator discomfort and "terminal headaches." That's why our newest monochrome and high resolution color CRTs are available with a team of innovations designed with "human factors" in mind: our new Super Dark high contrast screen and the famous Panasonic Direct Etch™ anti-reflection surface.

The Super Dark screen has been specially engineered for a high-contrast display that reduces operator fatigue caused by excessive brightness. The high contrast screen provides acceptable viewing at low brightness levels, so the CRT beam current is minimized and resolution is maximized. Characters are sharp, clear and easy to read. And the Super Dark screen helps reduce reflectance, while hiding normal long term screen burning too.

You can combine the Super Dark screen with our optional Direct Etch™ anti-reflection surface (available on most models), which effectively diffuses distracting ambient reflections without the drawbacks of bonded faceplates and plastic overlays. To minimize resolution loss, the screen glass is etched close to the phosphor; in tandem with the lower beam currents allowed by our Super Dark screen, resolution can actually be better than that of most conventional polished glass tubes. And operator comfort is much greater.

Super Dark Screen and Direct Etch™ are available on all popular-sized Panasonic data display tubes, including our affordable new high resolution in-line color CRTs. We're the CRT source to relieve everyone's terminal headaches. For prices and complete information, write Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, NJ 07094; or call (201) 348-5278.

Panasonic CRT screen ergonomics: Super Dark Screen and Direct Etch™.

Panasonic®
just slightly ahead of our time

CIRCLE 154

THE CENTRONICS PRINTSTATION 350.

THIS IS WHAT PRINTSTATION TECHNOLOGY IS ALL ABOUT.

Since its introduction in late 1981, the innovative Centronics technology behind the Printstation 350 Series has received OEM praise for its paper handling and reliability. With new Printstation family additions, we now offer new capabilities and higher speeds. Now, more than ever, the Printstation 350 family will provide OEMs with the flexibility to meet all their printing needs. Bar code printing. Large characters. Color. Graphics. More Multipass fonts. More speeds, from 50 cps (multipass) to over 400 cps (10 cpi). And more efficiency with an outstanding new breakthrough: a 1-, 2- or 3-bin automatic sheet and envelope feeder option.

Add these new capabilities to proven Printstation 350 innovations such as true multi-function paper-handling, and family design with 80% parts commonality—and you have the ideal OEM printer choice for all three information processing categories.

DATA PROCESSING.
Printstation 350 means exceptional throughput—approaching line printer speeds in DP applications such as: ▫ Program listings ▫ Business reports ▫ Data logging ▫ Spread sheets . . . using full 6-part, single sheet or fan-folded forms . . . and capable of operating at 100% duty cycle.

BUSINESS PROCESSING.
Whether in an office or on a loading dock, whatever a business needs, a Printstation 350 will print: ▫ Bar code tickets ▫ Mailing labels ▫ Insurance forms ▫ Purchase orders ▫ Sales charts & graphs ▫ Invoices . . . on business cut sheet, instant tear-off and sprocket-feed forms . . . with graphics . . . and without afterthought options.

WORD PROCESSING.
A Printstation 350 means complete job flexibility with a choice of fixed pitch or proportional fonts for: ▫ Business correspondence ▫ Office memos ▫ Proposals ▫ Personalized and form letters ▫ Envelope addressing.

And with our new automatic sheet/envelope feeder you can maximize operator productivity at an amazingly low cost.

Attractive and quiet enough for every office but right at home in a warehouse, teller station or shipping department. — That's Printstation 350. From Centronics—the first choice of OEMs worldwide. For a copy of our new Printstation 350 brochure, write Centronics Data Computer Corp., One Wall Street, Hudson, N.H. 03051.
Tel. (603)883-0111

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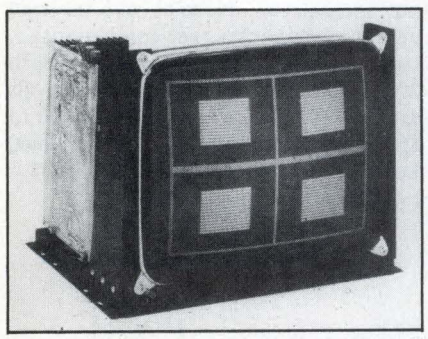
CENTRONICS® PRINTSTATIONS

CIRCLE 152

Tektronix compatible graphics added to VT100 terminals

DQ650 series GEN.II Retro-Graphics terminal enhancements for the entire VT100 family of video terminals are programmed with 32k bytes of local software. The enhancements provide bit-mapped imaging, Tektronix 4010 graphics terminal emulation, and monochromatic emulation of graphics functions on Tektronix's 4027 color graphics and 4014 graphics terminals. Pixel resolutions are 800 x 480 (DQ650M) and 800 x 240 (DQ650S). Prices range from $1230 to $1715. **Digital Engineering, Inc,** 630 Bercut Dr, Sacramento, CA 95814.
Circle 345

Monochrome graphics monitors

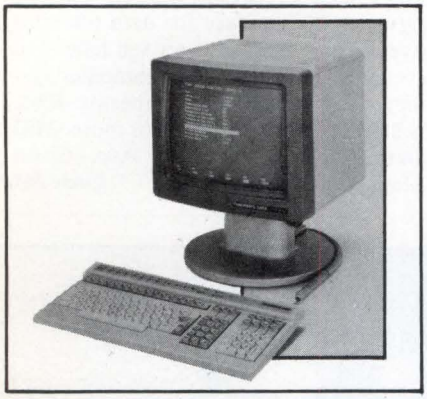


Family of high resolution monochrome CRT monitors provides up to 1100 lines at 60-Hz noninterlaced refresh rate and either 70- or 120-MHz video amplifiers. The 70-MHz amplifier accepts TTL, linear, or ECL levels; the 120-MHz amplifier interfaces to differential ECL. Vertical refresh rates to 90 Hz, interlaced or noninterlaced, and horizontal rates from 30 to 65 kHz are available. All monitors have stator yoke, regulated high voltage, and dual-axes dynamic focus. Units are available with any JEDEC phosphor, contrast enhanced faceplates, and antireflection coatings. Prices for the 70-MHz 15″, 17″, and 19″ (38- x 43- x 48-cm) monitors are $685, $767, and $799. **U.S. Pixel Corp,** 125 Irving St, Framingham, MA 01701.
Circle 346

Bar code scanning wand with memory

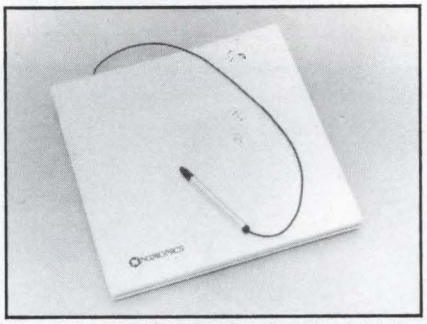
Datawand scanner reads, decodes, stores, and transmits bar coded data independent of data entry terminal. The handheld unit has 4K digits of low power CMOS memory for data storage. Scanner firmware is stored in onboard microprocessor memory. Rechargeable NiCad batteries are provided. When not in use, unit rests in a recharger module that also serves as an interface for data transfers over phone lines, into an MSI handheld computer, or into a host computer system via an RS-232-C type connector. Price is $199 in quantities of 100 or more. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626. **Circle 347**

Ergonomic terminal emulates VT100/52 family



Model TDV-2230 smart terminal emulates the DEC VT100/52 terminals and also provides as std features alternate char attributes, printer port, local echo, modem control support, host editing, local editing, and buffered line mode transmission. Four operational setup menus list control options for cursor/keyboard, screen/terminal, and communications modes. Selections can be made from the keyboard or the host computer and are stored in nonvolatile EAROM. Other menus store code sequences and control setup of tab rack. Base price is $1875. **Tandberg Data, Inc**, PO Box 99, Labriola Court, Armonk, NY 10504.
Circle 348

Digitizing pad



An electromagnetic 11″ x 11″ or 20″ x 20″ (28- x 28-cm or 51- x 51-cm) digitizing tablet features user specified output data in absolute measurement or in min increments of 0.001″ (0.25 cm). Metric or English measurements are switch selectable. Dual RS-232-C, bit parallel, or IEEE 488 interfaces can be output in either std serial or packed binary format. Pad operates in point, stream, incremental, or switch stream modes and measures up to 200 points/s. Firmware for self-diagnostics, matrix menuing, and host override are included. Button cursors, axis rotation, and scaling are optional. **Numonics Corp**, 418 Pierce St, Lansdale, PA 19446.
Circle 349

Panel mount thermal printer

PL20RM 20-col panel mount thermal printer comes with switch selectable TTL parallel or serial interfaces. Input power can be either ac or 12 Vdc. The 96 ASCII chars are std with 5- x 8-dot char matrix with descenders. A 39-char input buffer is furnished, and 120-line/min throughput is achieved. Normal and inverted print modes can be implemented. Underscore is via software control. Both 200′ (61-m) and 150′ (46-m) paper rolls are available. Prices range from $460 to $575, depending on quantity. **Telpar, Inc**, PO Box 796, Addison, TX 75001.
Circle 350

COMPUTERS

Single-board array processor

APB-3000 single-board Multibus version array processor computes number arrays using virtually any known algorithm. Standard routines include FFTs, power spectral density, correlation, digital filtering, and deconvolution. Full dual-port memory access to both program and data memory allows custom software algorithm development. Branches and break points can be set to facilitate debugging. Instruction execution time is 100 ns. Board is fully pipelined for max throughput. Host processor can access data in onboard memory cache at any time. **Marinco Inc**, 11760 Sorrento Valley Rd, San Diego, CA 92121.
Circle 351

On the perception of elegance.

Artist, engineer and scientist alike can't help but share a passionate appreciation for the forms of nature. Regard the exquisite symmetry of the nautilus shell. It is only one of nature's expressions of grace in shape and line. And it was achieved through a development program aimed entirely at function.

Around Honeywell, Underseas Systems Division scientists occasionally speak warmly of the elegance of algorithms encountered along the way to significant breakthroughs in software design. We *do* enjoy working with people who find pleasure in technical solutions embodying that special simplicity called elegance.

Right now we're searching for a few such software specialists with a BS/MS and background in structure design, field testing, or real time/time-control applications for test and diagnostic hardware. Experience with UYK-20, AYK-14, or CMS-2 would be most welcome.

Here's vigorous challenge, coupled with the opportunity to discover certain elegances of style among the Vikings, the North Stars, and other elements of good living unique to the Twin Cities area of Minnesota—the vigorous quality-of-life capital of the U.S.

For prompt, confidential consideration call George Bills collect at 612/931-6713. Or send resume to: George Bills, Engineering Manager, MN 11-102 0D, Underseas Systems Division, Honeywell, 600 Second Street N.E., Hopkins, MN 55343. Honeywell is an equal opportunity employer.

Honeywell

Making a world of difference.

CIRCLE 157

Computer to printer interface

Printer adapter interface ADA 1800 allows the Commodore Pet and CBM computers to output to parallel interface printers. Supporting 8 bits, the $129 adapter works with the Commodore disk and operates via BASIC commands. It is addressable and does not tie up the bus; address is switch selectable. A 4′ (1-m) cable with std 36-pin Centronics connector is provided. Switch selectable upper/lowercase, upper/lowercase reversed, uppercase only, and graphics are featured. Power is obtained from the printer or externally. **Connecticut micro-Computer Inc**, 36 Del Mar Dr, Brookfield, CT 06804.
Circle 352

Intelligent graphics controller

MLZ-VDC graphics controller has Z80A CPU, DMA controller, 132-byte FIFO on the Multibus for buffering command flow, and up to four 28-pin sockets allowing up to 32K EPROM/ROM and 16K RAM. It provides 24-bit addressing with complete master/slave or multimaster capabilities. Bus map defines board position. One Intel compatible iSBX expansion module connector, uPD7220 graphics display controller for graphics and char generation, and 512K bytes of onboard memory are included. Programmable lookup table displays 16 colors from a palette of 4096. Integral lightpen interface is available. **Heurikon Corp**, 3001 Latham Dr, Madison, WI 53713.
Circle 353

Floppy disk interface

Z2800 single-card floppy disk interface features a Z80A processor with 2K RAM and 4K ROM, and floppy disk and RS-232-C ports. Supplied firmware duplicates DEC TU-58 cassette drive protocol; jumper selectable executive program enables development of custom interface. Memory is expandable to 40K RAM/ROM. A second RS-232-C port with selectable baud rates and stop bits is available. Disk port accommodates single- or double-sided, single- or double-density floppy disks. IBM 3740 and IBM 40 formats are standard. Single-quantity price is $195. **Greco Systems**, 10020 Prospect Ave, Santee, CA 92071.
Circle 354

Intelligent controller for single-, multi-user systems

HD/CTC interfaces two ST506 compatible 5¼″ hard disk drives and a Streaker cartridge tape drive to an S-100 system. The intelligent controller has a Z80A (optional Z80B) CPU, 8K-byte RAM, and 16K-byte ROM to remove I/O control from the system CPU. Other hard disk and cartridge drive sizes can be accommodated with minor alterations to the onboard hardware/firmware. **Teletek Enterprises, Inc**, 9767F Business Park Dr, Sacramento, CA 95827.
Circle 355

Controller interfaces LSI-11s with 5¼″ Winchesters

DQ614 disk controller interfaces 1 or 2 5¼″ Winchesters with LSI-11, -11/2, -11/23, and -11/23 PLUS microcomputers. System operates directly from the Q-bus without additional boards and emulates up to 4 RL01 or RL02 disk drives, giving formatted capacities to 41.6M bytes. Occupying a single dual-wide slot in any LSI-11 backplane, the controller is totally transparent to RT-11, RSX-11, and RSTS operating systems. It operates with drives that incorporate an ST506 interface. A microprocessor based universal formatting system compensates for drives with varying number of heads, transfer rates, surfaces, and capacities. The controller will handle 5¼″ drives to 50M bytes. Price is $1695. **Distributed Logic Corp**, 12800 Garden Grove Blvd, Garden Grove, CA 92643.
Circle 356

Video I/O processor for Multibus

Video digitizer boards VAF-512 and QVAF-512 work with the firm's RGB-GRAPH and QRGB-GRAPH frame buffers, providing a complete Multibus or Q-bus 512- x 512- x 8-bit imaging system. VAF-512 board has a 800-s/pixel hardware vector generator and RAM based 16M color look-up table. Onboard 10-MHz A-D flash converter and contrast control circuit are provided. Frames can be software programmed as continuous or 1-shot "freeze frame." Alphanumeric or graphic overlays can be implemented via additional video controller boards. Prices start under $2150 for a 4-bit unit and $3150 for an 8-bit unit. **Matrox Electric Systems Ltd**, 5800 Andover Ave, T.M.R. Quebec, H4T 1H4, Canada.
Circle 357

STD-Z80 bus compatible universal systems interface

Designed to interface the STD-Z80 bus to peripherals via the SASI bus, MDX-SASI2 STD bus host adapter interchanges peripherals without affecting either the host microcomputer interface or host software. Featuring up to 4-MHz operation, the 5-V card ($249) has mode 2 interrupt capability and occupies 8 I/O port addresses. Block of 8 contiguous addresses can be any of 32 or 64 I/O addresses. Data bus is 8 bits bidirectional; address bus is 16 bits plus optional I/O expansion. Card has a fast DMA controller and provides for DMA daisy-chaining via an additional connector. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006. **Circle 358**

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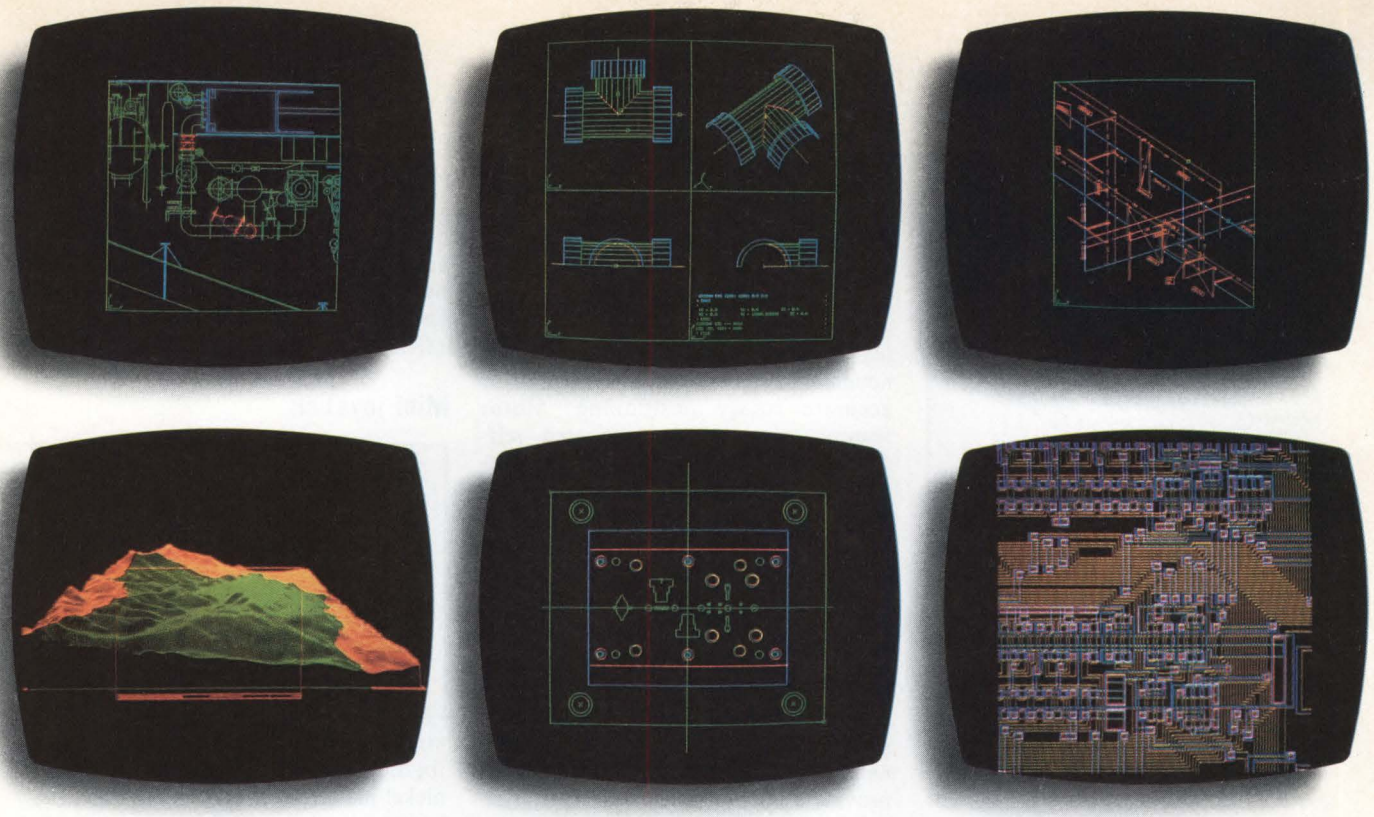

IT'S TIME TO TAKE YOUR PLOT 10 IDEAS OUT OF STORAGE.

Give your imagination the benefit of the latest graphics technology, with a D-SCAN dual-microprocessor GR-2412 raster terminal.

For example, the GR-2412's remarkably fast, remarkably accurate 4014 emulation makes it a snap to add color and selective erase to existing PLOT 10 routines.

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For immediate information on the GR-2412, contact Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051. Telephone (408) 727-0768.

Because ideas in storage don't get any better. Just older.

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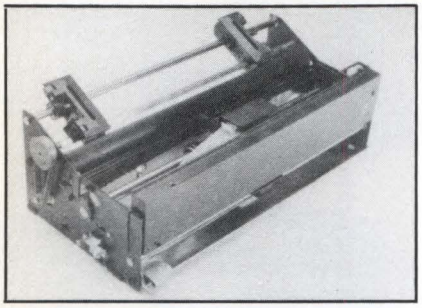
CIRCLE 159

Printer mechanism



Model 8-PMC matrix printer mechanism has all mechanical elements for an 80-col printer, including stepper motor for paper advance coupled to adjustable tractors for use with fanfold perforated paper. The 9-needle, free-flight matrix printhead is driven by a bidirectional motor with an encoder assembly on the rear extension of the shaft. Head travel speed is 25 ips; print rate is 250 cps (1200 Hz) at 10 cpi through 6-part forms. Reloadable ribbon is driven continuously from the reversing head drive motor. List price is $295. **Practical Automation, Inc**, Trapp Falls Rd, Shelton, CT 06484.
Circle 359

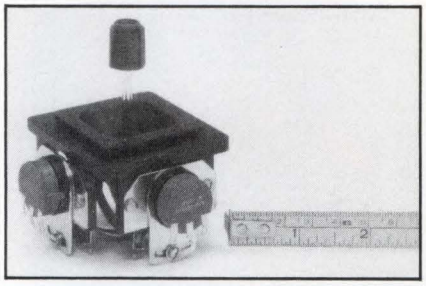
7.5° stepper motor with 26 oz-in holding torque

Series M-82801 stepper motors have a 26 oz-in holding torque and running torque starting at 16 oz-in. Step angle is 7.5° (48 steps/revolution) and step angle noncumulative tolerance is ±0.5° for accurate rotary positioning. Motor features permanently lubricated self-aligning bronze sleeve bearings. Self-aligning ball bearings are optional. Case size is 2.33″ x 1.4″ (5.92 x 3.6 cm). Price is less than $10 in 1k quantity. **Airpax Corp**, Cheshire, CT 06410.
Circle 360

SPDT/DPDT lighted switches

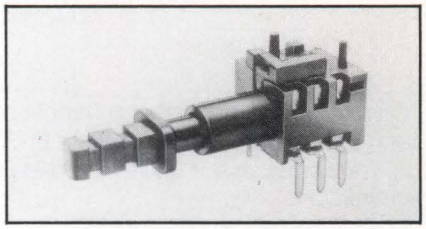
KB series of SPDT and DPDT, isolated lamp and LED circuit push-button switches come with momentary or alternate actions. Alternate action models provide a latch-down feature for physical determination of the switch mode. Colored and transparent round or square 0.457″ (1.161-cm) lens configurations are available. Lenses can be hot-stamped or labeled with clear legended film. Light sources include incandescent lamps and single- or dual-element LEDs. Dual LEDs have an IC voltage regulator chip and can be used in 6- to 28-V circuits without a ballast resistor. **NKK Switches of America, Inc**, 14415 N Scottsdale Rd, Scottsdale, AZ 85260.
Circle 361

Mini joystick



MJ series miniature proportional rate joystick has die-cast aluminum frame, nickel-plated steel bales and brackets, and anodized aluminum mounting bezel. Control features replaceable potentiometers for easy field repairs. Std pots are conductive plastic. Wire wound pots, special resistances, and shaft and body seals can be specified. Other options include Deadman switches, control shaft length, and Z axis. Cost is approx $57/unit in quantities of 500. **Bowmar Instrument Corp**, 8000 Bluffton Rd, Fort Wayne, IN 46809.
Circle 362

Miniature PC mount push-button switches



DPDT "Push Push Switch" for PC mounting features a selection of redundant contacts and precious metal switching surfaces. Low resistance contacts are self-cleaning. Switches provide an audible click tone and tactile feel during switching. **Switchcraft, Inc**, 5555 N Elston Ave, Chicago, IL 60630.
Circle 363

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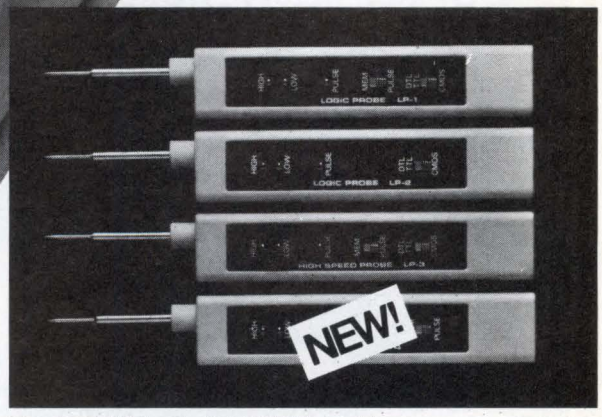

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CIRCLE 160

See us at ELECTRO, Booth #s 3139, 3141, 3143, 3145

1600-line/min thermal printhead

SM 20100 20-col thermal printhead prints up to 1600 char lines/min of a 5 x 7 matrix text. A square dot design and close coupling between adjacent energized dots form highly legible chars. The printheads can be ganged to obtain 40, 60, 80, or more cols. Intended for fixed head printers, the printheads can utilize a constant speed paper drive. An integral heat sink thermistor preheater and connector terminated cable make the unit ready to use. Prices range from $171.75 to $274.80. **Gulton Industries, Inc,** 212 Durham Ave, Metuchen, NJ 08840.
Circle 364

DIP PC mountable relay

G4D PC mountable DIP double-pole relay is provided as a std DPDT version, and high capacity DPDT and DPST-NO single silver contact types for midrange switching of 5-A loads. The CSA certified series includes UL TV-2 rated DPDT models that also offer nominal 800-mW power consumption and flux tight construction for flow soldering. Features include creepage distances of more than 0.12″ (0.30 cm) and extended operating life. Min load requirement is 100 mA at 5 Vdc. Coil voltage ratings range from 5 to 24 Vdc. **Omron Electronics, Inc,** 650 Woodfield, Schaumburg, IL 60195.
Circle 365

Combined transistor/resistors for built-in bias networks

DTA124(PNP)/DTC124(NPN) digital transistor contains a PNP or NPN transistor combined in a single package with 2 completely isolated thin-film bias resistors. The digital transistors implement bias networks and eliminate 2 external resistors in each interface circuit application. Because the built-in bias resistors are completely separated from each other and from the transistor, no interaction can occur between the devices. Bias levels can be set up in both positive and negative directions. Five different bias resistor combinations and 5 package styles are available. **ROHM Corp,** PO Box 19515, Irvine CA 92713.
Circle 366

Bicolor LEDs

Super-brite bicolor LEDs can be any combination of red, amber, and green; or high efficiency red, amber, yellow, and green. Cartridge packages come with std mounting hardware and either flying leads or std terminals. The LEDs are available with/without built-in resistors for selection of 2.4- to 28-V operation. The 2-terminal devices change color by reversing the polarity of the dc excitation voltage. If low voltage ac is used, a third color can be created. In 1k-piece quantity, price is $2.20 without resistors, $2.45 with resistors. **Data Display Products,** 303 N Oak St, Inglewood, CA 90302.
Circle 367

Microminiature relays

Series of PCB mountable relays allows 2 FBR 20 relays to be mounted in the space used by a single FBR 211 relay. Contact arrangement is SPDT. Contact ratings are 24 Vdc/1 A and 120 Vac/0.5 A. Max carrying current is 2 A. Std contacts are single gold overlay silver. Optional model uses bifurcated gold overlay silver-palladium alloy contacts. Drive voltages range from 1.5 to 24 Vdc with a rated power consumption of 0.3 W. Relays measure 9.8 x 7.4 x 9.8 mm and have a pin length of 4 mm. Prices are $0.99 each/1k lot. **Fujitsu America, Inc, Component Div,** 918 Sherwood Dr, Lake Bluff, IL 60044.
Circle 368

Sealed miniature code switches

"Roto-Dip" sealed and washable miniature code switches for direct mounting on PCBs provide either BCD or hex outputs. Gold-plated contacts and a 0.38″ (0.95-cm) cube package are featured. Both configurations are available in vertical and horizontal versions. Either screwdriver slot or extended shaft with mini-knobs for easy insertion can be specified. Each version can be further specified for shorting or non-shorting switching modes. **ELMA Switch Corp,** 1851 Reynolds Ave, Irvine, CA 92714.
Circle 369

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Our sleek 3½″ Micro Floppydisk system is every inch a Sony. So why would one of the world's most prestigious computer manufacturers decide to make it their standard?

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CIRCLE 161

PCB mountable LEDs

The 5350 series of indicators positions LEDs at right angles to the PCB and has a lead spacing of 0.1″ (0.3 cm). The 5370 series has LEDs positioned parallel to the PCB and a lead spacing of 0.2″ (0.5 cm). Indicators can be stacked adjacent to each other. Both series are available with red, green, or yellow LEDs; red LEDs can also be specified with built-in impedance for 5-Vdc operation. Units require no external current limiting resistors and are TTL compatible. Price is $0.56 each in 1k quantity. **Industrial Devices, Inc,** 7 Hudson Ave, Edgewater, NJ 07020.
Circle 370

Thick-film, thermal printheads

S200 series thick-film printheads provide 2-ms/line max thermal response, and recordings of 8 horizontal and 7.7 vertical dots/mm with models S216-8, S256-8, and S296-8. Models S215-12 and S258-12 have 12-dots/mm resolution. Recording widths range from 216 to 296 mm. An onchip high speed 32-bit shift register driver is provided. A 32-bit switching diode array is used with the heating elements and the shift register driver on a single substrate. A single 40-pin connector is used for all drive connections. **Mitsubishi Electronics America, Inc,** 991 Knox Ave, Torrance, CA 90502.
Circle 371

Wire lead 10- and 15-A power rocker switches

Wire lead versions of the C series miniature power rocker switch are available in 10- and 15-A models with SPDT/SPST switch functions. Black wire leads 6″ (15 cm) long are std. Molded construction has 4 integral legs for snap-in mounting. Switch body fits a std panel cut-out. Rocker and case material is UL 94V-2 rated 6/6 nylon. Insulation resistance is greater than 1k MΩ. Dielectric strength is 2500 V RMS at sea level. **C&K Components Inc,** 15 Riverdale Ave, Newton, MA 02158. **Circle 372**

CONTROL & AUTOMATION

High performance DMA controller

HD68450 64-pin DIP DMA controller has an advanced silicone mainframe channel I/O capability and 4 independent channels. Capable of a sustained throughput of 4M bytes/s, the controller also includes 32-bit architecture, vectored interrupts, bus exception handling, and 16M-byte HD68000 CPU address space. Hardware array and linked list chaining, bus matching between 16/32-bit memory accesses, 8-bit peripheral chips, and programmable bus bandwidth utilization are featured. Speed selections are 4, 6, and 8 MHz. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
Circle 373

Microcomputer analog expander board

MP8418-EXP microcomputer analog input expander for Multibus MP8418 analog I/O boards increases differential input capacities from 15 to 63 channels and single-ended input from 31 to 127 channels. Board features 12-bit resolution, overvoltage protection to 25 Vdc, and optional software programmable amplifier providing 11 binary weighted gains. Control signals and power are passed to the expander from the MP8418. Analog input signal is passed from the MP8418 to the expander. Multiplexer channel addresses are latched on the expander board. Price is $495. **Burr-Brown Research Corp,** Box 11400, Tucson, AZ 85734.
Circle 374

Temperature controller

Microprocessor based temperature controllers series 6000 have 2 digital displays, touch key operation, software linearized and stabilized thermocouple input with 3-mode PID heating, cooling controls, and dual alarms. Features include °F to °C conversion; alarms that can be energized for temp rise or fall and are selectable as process or deviation type; and program restart circuit that eliminates program lock-up due to transient voltage spikes or line brown out. Program automatically restarts within 20 ms after condition passes. The controllers are available in J or K type thermocouple calibrations. Prices start at $395. **Omega Engineering, Inc,** PO Box 4047, Stamford, CT 06907.
Circle 375

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Our $395 OEM unit price says it all. And then some. Because you can't find a better combination. Of price for you. And performance for your customers. The Freedom™ 50 is built for OEMs only. With features built-in that mean your customers reap benefits found in pricier VDTs. 9 cursor control keys. 5 separate function keys. Column and field tabs. A choice of 7 video attributes, assigned by character, that require no display space. A 24 x 80 display format. A 25th status line. 7 x 9 dot matrix within a 9 x 12 field. Baud rate to 19.2K. And more. There's the human touch, too. A 12-inch diagonal etched green phosphor screen. A detached keyboard. And 5 screen tilt positions. All help make work easier. And more productive. The Freedom 50 marks the new high in low cost VDTs. Only for OEMs. Only for $395 (*1K quantity). Only from Liberty, manufacturer of the standard Freedom™ 100. Call our San Francisco headquarters at (415) 751-7560.

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CIRCLE 169

1M-bit CMOS ROM

A 1M-bit CMOS ROM measuring approx 49 mm^2 utilizes a NAND cell design for its double-density capacity. The ROM is organized 128K words x 8 bits and uses 2-micron technology. Operating on a single 5-V supply with ±10% tolerance, the ROM has 3-ms max access time. Power dissipation is 60 mW max. It draws 12-mA max power when active and 10 μA in standby mode. A 52-pin flat pack and 40-pin DIP are available. Price is $70 each. **NEC Electronics U.S.A. Inc, Electronic Arrays Div,** 550 E Middlefield Rd, Mountain View, CA 94043.

Circle 376

Programmable, single-supply op amps

TLC251 and TLC271 op amps are fabricated with TI's Sigate LinCMOS technology that allows operation from a single power supply and provides highly stable input-offset voltages. Low power consumption, high input impedance, and low input bias and offset currents of std metal-gate CMOS op amps are maintained. Typ drift for both devices are 0.1 μV/month and 0.7 μV/°C at low bias. The op amps are available as an A version with 5-mV and B version with 2-mV tight end, guaranteed input-offset voltages. TLC251 operates from a supply range of 1 to 16 V; TLC271 operates from 4- to 16-V supplies. **Texas Instruments Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.

Circle 377

PSK modem filter complies with Bell 212A

XR-2120 PSK CMOS switched capacitor, 22-pin filter fulfills Bell 212A transmit/receive filtering requirements. The self-contained bandpass filter set requires external crystal and a single resistor. The CMOS IC contains autoswitching between answer/originate functions. Modem includes digitally programmable gain amplifier, input anti-aliasing filter, switched capacitor bandpass filters at 1200 and 2400 Hz that provide compromise line equalization, and RC active output filters. Unit is powered by either 6 or 12 Vdc, in either single- or split-supply configurations. Consumption is typ 0.2 W. Both 22-pin plastic ($29.02) and ceramic ($30.59) packages are available. **Exar Integrated Systems, Inc,** 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088.

Circle 378

Digital lock/address decoder circuit

Available as either a 2-push-button digital lock (LS7229) or an address decoder (LS7228) that accepts dual-train pulse input from electronic keying, the MOS/LSI circuit employs a 9-bit code, allowing two or more chips to be cascaded for more than 512 combinations. Both versions have 2.5- to 15-Vdc voltage range. The 2-push-button chip eliminates need for keyboard, and code can be entered without seeing the buttons. An anti-bounce network is also incorporated. Price is $1.25 each in 1k quantity. **LSI Computer Systems, Inc,** 1235 Walt Whitman Rd, Melville, NY 11747.

Circle 379

Sigate CMOS gate array

TM 4030 silicon gate 300-gate array carries a 10k-piece price of less than $4 in die form, and has typ gate propagation delays of 5 to 15 ns. One- to 12-V power supply, low power consumption, TTL and CMOS I/O compatibility, static charge protection on all inputs, pullup tabs, and pull-downs on all inputs are featured. Quick CAD turnaround time is guaranteed. The uncommitted logic array can directly replace the RCA 4000 series and 7400 TTL std logic families. Packaging varieties include die form, LCC, flat packs, 8-pin mini-DIP, cerDIPs, ceramic, 40-pin DIPs, and custom specified. **Telmos Inc,** 740 Kifer Rd, Sunnyvale, CA 94086.

Circle 380

CMOS gate array

Series 7CM 1440-gate array features 3-micron geometry for 1- to 3-ns gate delay performance. Array uses a double-level metal, Sigate CMOS process design. It is provided in a 40-pin side-braze, or 64/68-pin cerDIP. Other family members include the 7CL 600-gate array and the 7CK 1920-gate array. **Storage Technology Corp,** 2270 S 88th St, Louisville, CO 80028.

Circle 381

Tell us what you like

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CRT controller ICs

SY6845R, SY6845E, and SY68045 CRT controllers are 5-V only, 40-pin ICs that are pin compatible with std 6845 devices. These controllers adapt to most 8-bit microprocessor systems. SY6845R ($5.95) has full alphanumeric and limited graphics capabilities. It covers a fully programmable display, interlaced or noninterlaced scan, and lightpen interface. A 16k-char video display RAM can be addressed. SY6845E ($6.89) has all features of SY6845R and adds optional row/col or straight binary addressing of video display RAM, transparent addressing, and status register. SY68045 ($3.50) ROM programmed controller is a low cost replacement for SY6845R/E. **Synertek, a sub of Honeywell,** 3001 Stender Way, Santa Clara, CA 95054.

Circle 382

8-bit DAC

Monolithic 8-bit DAC AD9768 features typ settling time of 5 ns to ±0.2% and operation in either 2-quadrant multiplication with bandwidths to 40 MHz or in fixed reference applications using the onchip voltage reference. Capable of 100-MHz update rates, the device is ECL compatible and provides 20-mA full scale current output. Multiplying capability can be used in either voltage or current modes. Transmission lines can be driven directly with high current output; internal bandgap reference reduces support circuitry requirements. The DAC is $32.20. **Analog Devices, Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

Circle 383

15-bit ADC for bus and UART interface

TSC800 proprietary 15-bit plus sign, bus compatible, primary output ADC requires only 6 external components and voltage reference. Two data transfer modes allow the ADC to easily transfer data to a microprocessor/microcomputer data bus or UART. Data can be transferred in two 8-bit bytes or as one 16-bit word. Data valid signal indicates when converter data latches are being updated. Handshake mode actively controls data transfers to peripherals. Operating control features also include resolution dynamic range, low power, and less than $1/bit cost. Device is available in 40-pin plastic packages and cerDIPs. **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mountain View, CA 94043.

Circle 384

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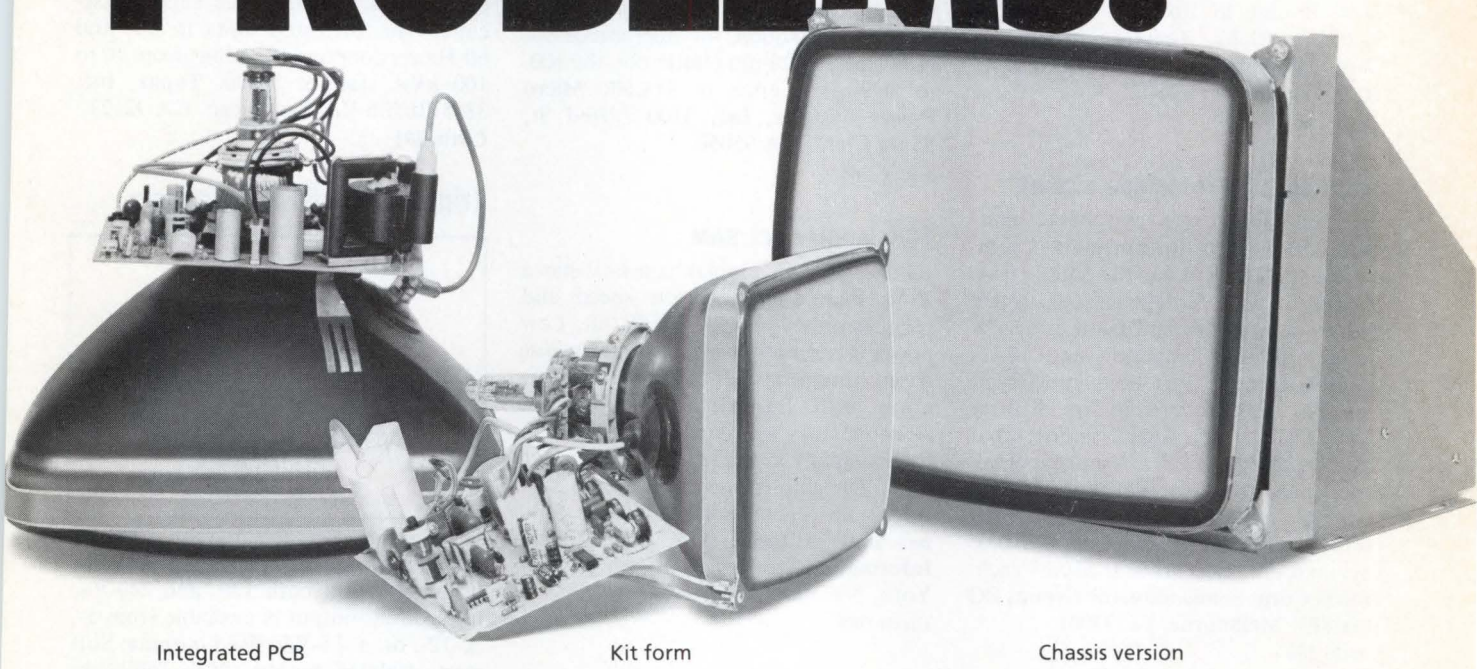

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CIRCLE 163

32k ROMs with electrostatic protection

Models R09413B/C/D 32K ROMs feature electrostatic discharge protection and MOS N-channel Sigate ion-implanted technology. The 4096 x 8 organized ROMs have fully static operation, single 5-V ±5% operation, and TTL compatibility. Access times are 450 ns (R094132B), 300 ns (R094132C), and 250 ns (R094132D). Inputs meet 2.3 kV per MIL-STD-883 method 3015.1. Three-state outputs are under control of 2 mask programmable chip selects, and can drive 1 std TTL load each. Pricing in 10k lots ranges from $1.65 to $1.82. **General Instrument Corp, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.
Circle 385

CMOS parallel interface circuit

Programmable CMOS peripheral interface 82C55A is a pin-for-pin and TTL compatible replacement for the NMOS 8255A. It operates in a 5-MHz 80C86/88 system with no wait states and features 55-μW standby power dissipation and 10-μA standby current. Bus hold circuitry is provided on each I/O pin for all three 8-bit parallel ports. High I/O port output drive capability of 2.5 mA/output eliminates need for external bus drivers. Available in 40-pin 0.6″ (1.5-cm) center cerDIP, industrial temp grade is $10.05 each and mil temp grade is $30.37 each. **Harris Corp, Semiconductor Group,** PO Box 883, Melbourne, FL 32901.
Circle 386

Video power op amps deliver 4 A, dissipate 70 W

PA09 and PA09A video power op amps operate with dual power supplies up to ±40 V or single supplies up to 80 V. Output currents are ±4 A. Output stage has complementary VMOS pair that slews at 500 V/μs and settles to 0.1% in 300 ns. Output transistors have thermal resistance of 1.6 °C/W and full electrical isolation from the 8-pin TO-3 package. Max power rating is 70 W at 25 °C. PA09 has dual FET front end. Prices range from $99.50 to $164.35. **APEX Microtechnology Corp,** 1130 E Pennsylvania St, Tucson, AZ 85714.
Circle 387

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We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Microprocessor compatible 8-bit, 8-channel CMOS DAS

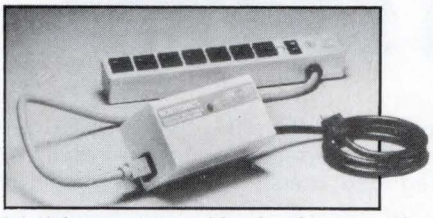
MP7581 contains an 8-bit successive approximation ADC, an 8-channel multiplexer, 8 x 8 dual-port RAM, 3-state data drivers for interface, address latches, and microprocessor compatible control logic. Device interfaces directly to 8080, 8085, Z80, 6800, and other microprocessor systems. Conversion time is 67 μs; data are never older than 533 μs. The data acquisition system is completely transparent to the microprocessor. Output signal can be decoded by external circuitry to derive conversion related timing information for microprocessor interrupts. In 28-pin plastic DIP, the 100- to 499-piece price is $13.60. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050.
Circle 388

16K bipolar ECL RAM

HM10480 16K-bit bipolar ECL RAM has a 25-ns max address access speed and requires only 750 or 0.05 mW/bit. Low power consumption ensures that HM10480 based storage devices have reliable operation with little increase in temp. Area/memory cell is 52% smaller than the company's 4K-bit 2.5-micron ECL RAM. The chip is housed in an industry std 20-pin cerDIP. Sample price is $140 per unit. **Hitachi, Ltd, c/o Hitachi Information Services,** 22 E 49th St, New York, NY 10017.
Circle 389

POWER SOURCES & PROTECTION

Voltage monitor/surge suppressor

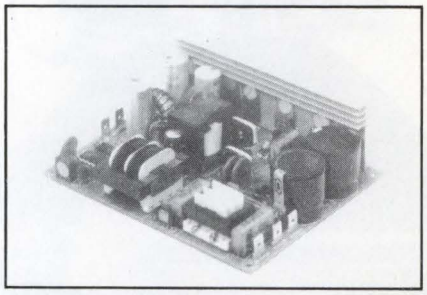


Model CMP-905 combined voltage monitor and surge suppressor includes a rugged Lexan housing, and LED line voltage monitor, an internal overload fuse, and 1 outlet that can be used with a multi-outlet bus strip. Fast action, high capacity metal oxide varistor diverts voltage transients before system damage can occur. A 2-pole LC filter reduces emi/rfi noise. **Nortronics Co Inc,** 8101 10th Ave N, Minneapolis, MN 55427.
Circle 390

Microcomputer controlled power conditioners

Three-phase power conditioners have an internal microcomputer that continuously monitors input voltage, determines required correction, then initiates the needed response during power fluctuations. Correction is made within 1 cycle of line frequency. Voltage variations of 20% above or below nominal are accepted and reduced to within 5% of nominal. Power line noise suppression is achieved via low pass filters, peak limiting circuits, resistor-capacitor snubber circuits, and dynamic clipping circuits. The UL listed units in 50- and 60-Hz versions and in ratings from 10 to 100 kVA start at $6950. **Topaz, Inc,** 3855 Ruffin Rd, San Diego, CA 92123.
Circle 391

Triple-output 60-W switchers



Delta series switchers have a 100-kHz switching frequency providing 60 W of dc power from both 120- and 240-Vac lines. Multi-output is available from 5-, ± 12-, or ± 15-Vdc fixed outputs. Soft start, isolated output, 50% foldback, ± 0.1% regulation, 80-dB transient rejection, up to 80% efficiency, and conformance to FCC, UL, and CSA standards are featured. PCB, open frame, or full enclosure models are available. **Energetec Systems, Inc,** 2204 Wellington Ct, Lisle, IL 60532. **Circle 392**

DC-DC converters

Series 200Z modular power supplies with single or dual outputs can deliver up to 12 W of output power. Output voltages can be varied ±20% by adjusting an externally accessible potentiometer. Options include output shutdown and preset voltage reduction capabilities. Customizing features include input voltages from 4 to 30 V, and dual-polarity, single-ended positive, and dual-positive output configurations. Dual outputs can be separately specified. Regulation is rated at ±3%. Op temp range is 0 to 70 °C. Efficiency at full load is typ 70%. **Sprague Electric Co,** 555 Marshall St, North Adams, MA 01247.
Circle 393

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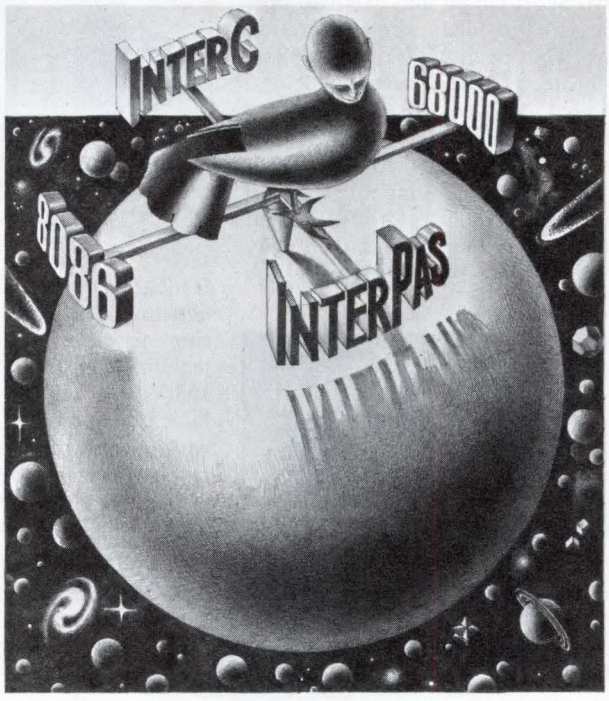

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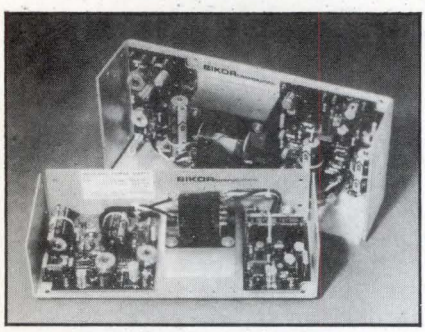
CIRCLE 164

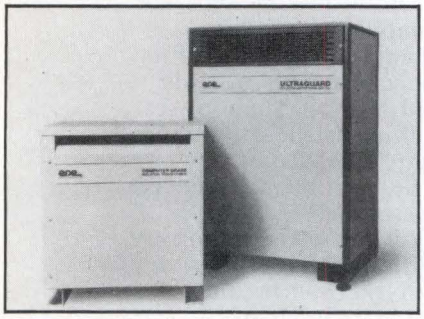
Multi-output, open frame linear power supplies



LT series of linear, multi-output power supplies features full output ratings to 50 °C, 115- and 230-Vac inputs, and remote sense. Foldback current limiting overload protection, overvoltage protection, reverse voltage protection, and oversized components to run cooler are included. Seven case sizes with output voltage combinations from 5 to 24 V and 0.5 to 12 A are available. Line regulation is ±0.05% for a 10% change and load regulation is ±0.05% for a 50% change. Ripple is 5 mV pk-pk; dc outputs can be adjusted ±5% min. Price range is $69.95 to $126.95. **Bikor Corp,** 1504 W 228th St, Torrance, CA 90501.

Circle 394

Computer grade isolation transformers

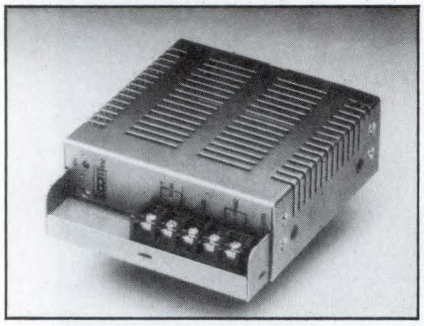


Computer Grade and Ultraguard isolation transformers provide 2 levels of power line noise protection and are available in std 15- to 500-kVA ratings. Ultraguard provides the greatest degree of noise protection and advantages of lightning arrester and surge suppressor. The transformers have over 98% typ efficiency and very low ac audible noise. Adaptable for outdoor use, the UL listed units are copper wound with electrostatic shield system with −120 to −140 dB typ attenuation. Compensation is provided for third harmonic problem caused by switching regulator power supplies. **Emergency Power Engineering, Inc,** 3580 Cadillac Ave, Costa Mesa, CA 92626.

Circle 395

Single-output switching power supplies

"A" series single-output switching power supplies have MTBF of 65k h and fully anodized metal enclosure to resist abuse and rfi. Short circuit and overload protections are provided; normal operation resumes when overload is removed. Soft start protects critical semiconductors. Line input is 85 to 132 Vac, and line regulation is 0.1% max for 10% change. Converter frequency is 50 kHz. Efficiency is 75% and op temp range is −10 to 50 °C. Series includes 5-, 12-, 15-, and 24-Vdc output versions. **L-com Inc,** 1545 Osgood St, North Andover, MA 01845.



Circle 396

UL recognized, multi-output, 65-W switchers

ME series of UL 478 recognized, multi-output 65-W switching power supplies provides up to 4 outputs and accepts a dual-input that is jumper selectable, 85 to 132 Vac and 170 to 264 Vac, 47 to 440 Hz, and 240 to 360 Vdc. Units can include up to two 1-A max separate regulators for individual outputs. Line regulation is down to 0.2%; load regulation is down to 0.3%; ripple and noise is 1% of 75 mV, pk-pk. Overcurrent, overvoltage, and short-circuit protections are provided. Op temp range is 0 to 50 °C without derating. Prices start at $80 each for a 4-output unit. **Panasonic Industrial Co,** One Panasonic Way, Secaucus, NJ 07094.

Circle 397

Switching power supplies for small computers

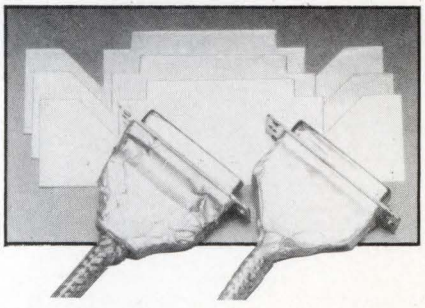
XL50 family of 4-output switching power supplies delivers 60 W in a std 4.25″ x 7.75″ x 2″ (10.80- x 19.69- x 5-cm) form factor. Proprietary current controlled feedback network yields tight regulation and low ripple/noise. All models have short circuit protection, input surge protection, 20-ms hold-up time, and 90- to 132-Vac or 180- to 264-Vac user selectable input voltage. The supplies operate with no power derating in a 50 °C ambient range and have overvoltage protection on the 5-V output. In 1k lots, price is $60. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.

Circle 398

EMI PROTECTION

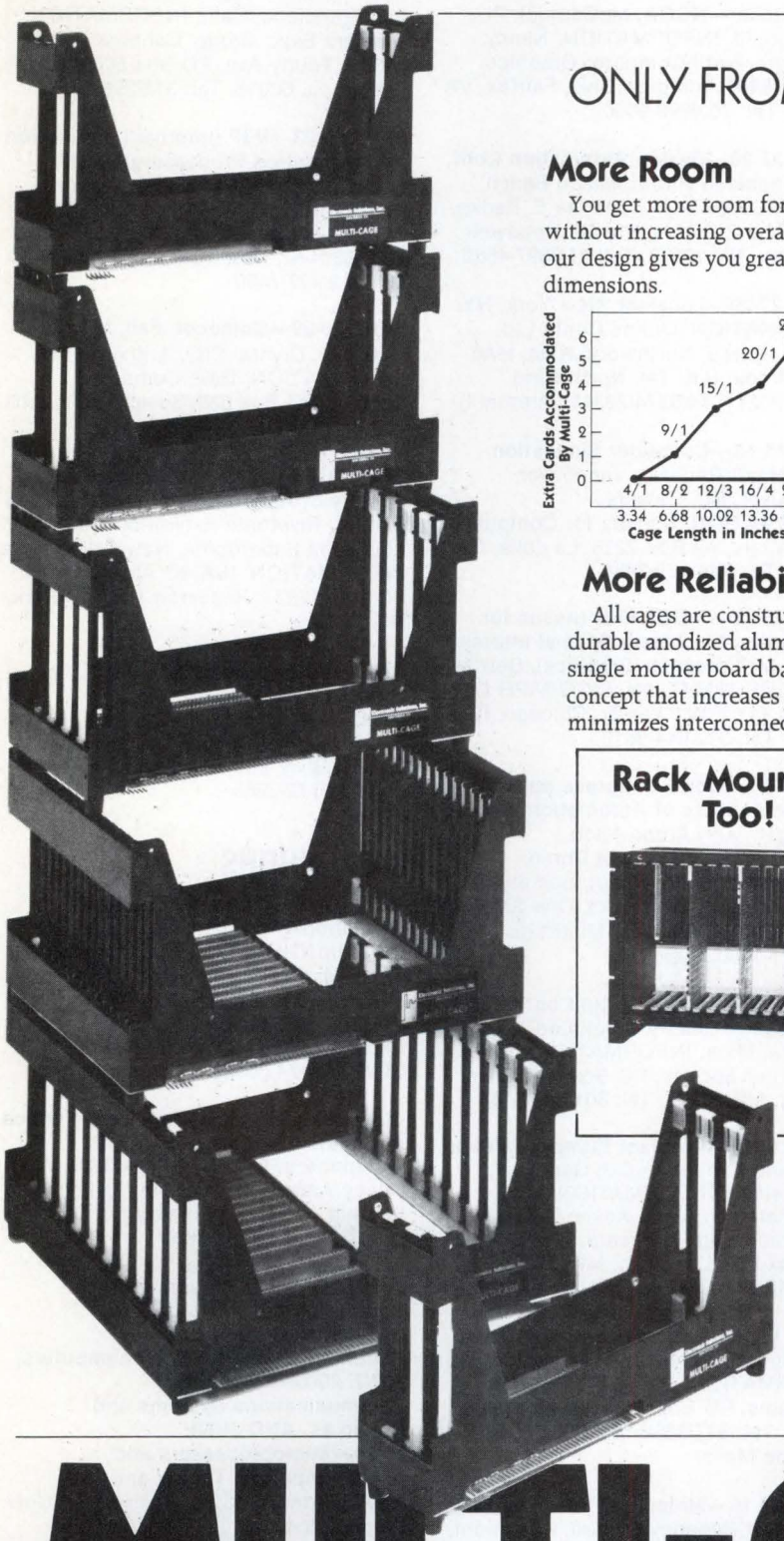
EMI/RFI shielding tape

Cho-Foil electrically conductive copper foil tape with conductive pressure sensitive adhesive has a 0.003-Ω/in^2 electrical resistance. Conductive particles are unaffected by extreme conditions, and typ adhesive peel strength per ASTM D-1000 is 23 oz-in. In addition to emi/rfi shielding applications, the tape can also be used to improve grounding to conductive materials that resist soldering. The tape is provided in 36- and 72-yd (36- and 66-m) rolls, and in widths from 0.5″ to 24″ (1.3 to 61 cm). **Chomerics, Inc,** 77 Dragon Ct, Woburn, MA 01888.



Circle 399

More Room... More Multibus® Cages.



ONLY FROM ELECTRONIC SOLUTIONS!

More Room

You get more room for extra cards without increasing overall size, because our design gives you greater inside dimensions.

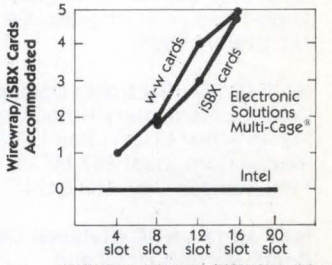
More Reliability

All cages are constructed of sturdy, durable anodized aluminum with a single mother board backplane . . . a concept that increases reliability and minimizes interconnections.

Rack Mounting Too!

More Models

We have more models than all our competitors combined. Choose a cage with 3, 4, 5, 6, 7, 8, 9, 12, 14, 15, 16, 20, 24 or 26 slots for the right solution to your problem. We have models with either 0.6" or 0.75" card centers and can even accommodate **wirewrap cards**.



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MULTI-CAGE®

CIRCLE 165

CALENDAR

CONFERENCES

MAY 2-5—Test and Measurement World Expo, San Jose Conv Ctr, San Jose, Calif. INFORMATION: Meg Bowen, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

MAY 9-13—SID (Society for Information Display) Internat'l Sym, Marriott Hotel, Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables FL 33134. Tel: 305/446-8193

MAY 10-12—Mini/Micro-Northwest, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 10-12—Northcon, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 16-18—Electronic Components Conf, Contemporary Hotel, Orlando, Fla. INFORMATION: Don L. Willyard, Bendix Corp, Dept 867 MF39, PO Box 1159, Kansas City, MO 64141

MAY 16-19—NCC (National Computer Conf), Marriott Hotel and Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3624

MAY 18-20—MIPRO (Microprocessors/ Microcomputers Course/Conf), Congress Ctr, Hotel Adriatic, Opatija, Yugoslavia. INFORMATION: P. Dragojlović, MIPRO Secretariat, Trg P. Togliatti 4, 51000 Rijeka, Yugoslavia. Tel: +38 51 31 211 X424 (am); +38 51 741 494 (pm)

MAY 25—Automating Intelligent Behavior: Applications and Frontiers, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Marvin Denicoff, Trends and Applications 83, PO Box 639, Silver Spring, MD 20901. Tel: 202/696-4302

JUNE 13-16—Internat'l Conf on Computer Architecture, Stockholm, Sweden. INFORMATION: H. W. Lawson, Jr, Linkoping Univ, S-581 83, Linkoping, Sweden

JUNE 14-16—Ohmcon, Cobo Hall, Detroit, Mich. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JUNE 19-23—Computer Vision and Pattern Recognition (formerly Pattern Recognition and Image Processing) Conf, Crystal City Hyatt, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 19-22—Internat'l Conf on Communications, Sheraton-Boston Hotel, Boston, Mass. INFORMATION: C. William Anderson, New England Telephone & Telegraph, 350 Cochituate Rd, Framingham, MA 01701. Tel: 617/879-9000

JUNE 26-30—NCGA, McCormick Pl, Chicago, Ill. INFORMATION: Nancy LeFebvre, Nat'l Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

JUNE 27-29—Design Automation Conf, Fontainebleau Hilton, Miami Beach, Fla. INFORMATION: Charles E. Radke, IBM Corp (ZIP-47A), Rte 52, Hopewell Junction, NY 12533. Tel: 914/897-4682

JUNE 27-29—Localnet, New York, NY. INFORMATION: Online Confs Ltd, Argyle House, Northwood Hills, HA6 1TS, Middx, U.K. Tel: Northwood 09274/28211; 44/9274/28211 (internat'l)

JULY 11-13—Computer Simulation Conf, Hyatt Regency Vancouver, Vancouver, BC, Canada. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 714/459-3888

JULY 25-29—SIGGRAPH (Assoc for Computing Machinery Special Interest Group on Computer Graphics), Detroit, Mich. INFORMATION: SIGGRAPH Conf Office, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

AUG 9-11—World Congress on the Human Aspects of Automation, Univ of Michigan, Ann Arbor, Mich. INFORMATION: Pat Van Doren, Technical Activities Dept, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1080 X369

AUG 23-26—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 13-15—Autofact Europe, Palexpo Conf and Exhibition Ctr, Geneva, Switzerland. INFORMATION: Automated Systems Assoc, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

SEPT 13-15—Federal Computer Conf, Washington Conv Ctr, Washington, DC. INFORMATION: Federal Education Programs, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181; 800/225-5926 (outside Mass)

SEPT 13-15—Midcon, O'Hare Expo Ctr and Hyatt Regency O'Hare, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Mini/Micro-Midwest, O'Hare Expo Ctr, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Peripherals, Moscone Ctr, San Francisco, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

SEPT 19-23—IFIP (Internat'l Federation for Information Processing) World Computer Congress, Paris, France. INFORMATION: Philip H. Dorn, Dorn Computer Consultants, Inc, 25 E 86th St, New York, NY 10028. Tel: 212/427-7460

SEPT 26-29—Compcon Fall, Marriott Gateway, Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 26-29—ISA (Instrumentation Society of America) Internat'l Conf and Exhibit, Rivergate Exhibition Ctr and Louisiana Superdome, New Orleans, La. INFORMATION: ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709

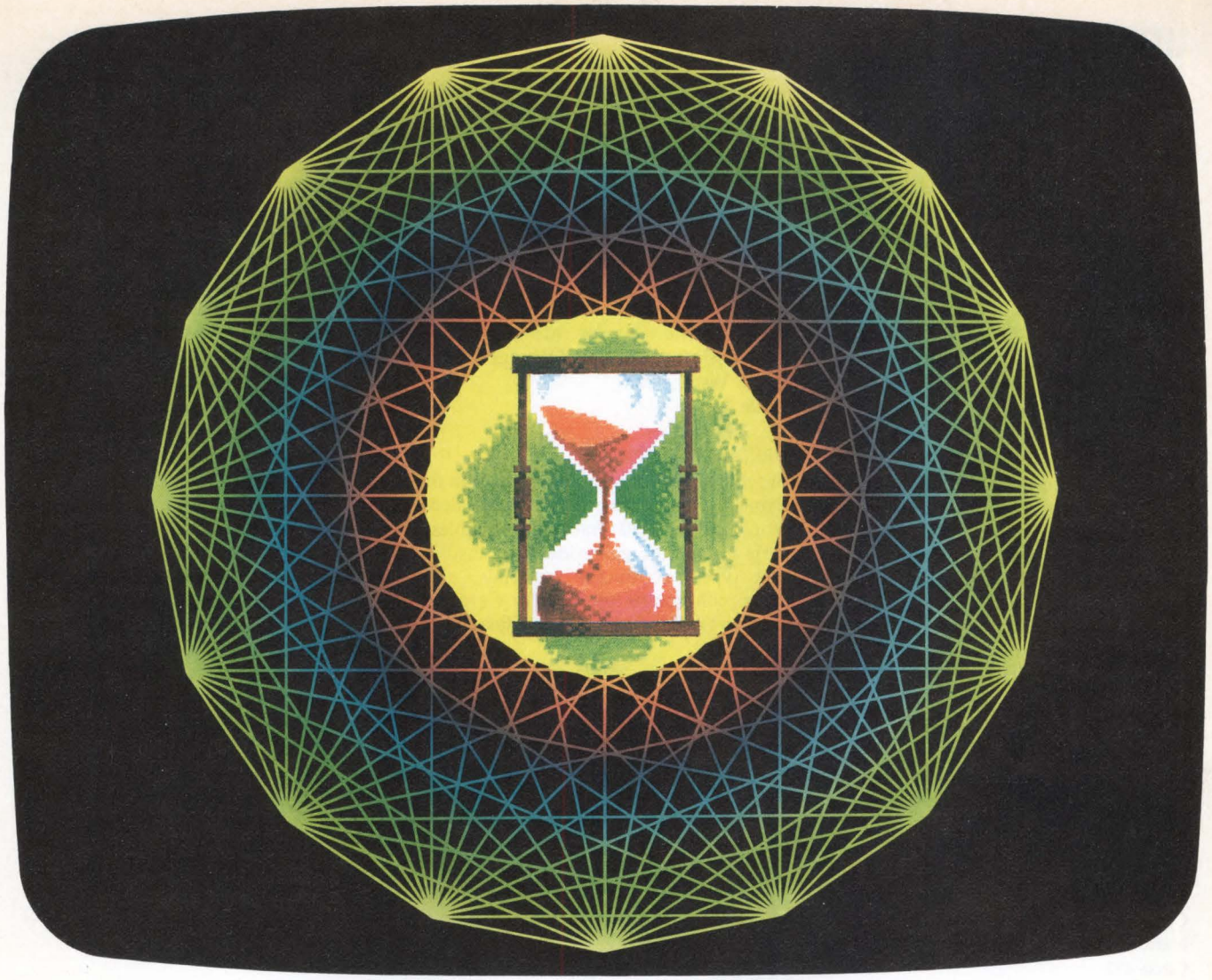
SEPT 26-28—Maecon, Kansas City Conv Ctr, Kansas City, Mo. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

WORKSHOPS

MAY-JUNE—Microcomputer Workshops, various cities and dates. INFORMATION: Intel Corp, Customer Training, 1350 Shorebird Dr, Bldg B, Mountain View, CA 94043. Tel: 415/940-7800 (San Francisco); 312/981-7250 (Chicago/Dallas); 617/256-1374 (Boston/Washington)

JUNE 1-2—Strategic Planning for Office Automation, Watergate Mall, Washington, DC. INFORMATION: Nancy Anderson, Micronet/KSI, 2551 Virginia Ave NW, Washington, DC 20037. Tel: 202/333-4800

JUNE 2-3—FCC Regulation of Computing Devices, JUNE 6-10—Workshop in Data Communications for Microcomputers, JUNE 20-24—Computer Communications Systems and Networks, AND JUNE 20-24—Microprocessors and Microcomputers: Theory and Applications, George Washington Univ, Washington, DC. INFORMATION: Douglas Green, Continuing Engineering Ed, George Washington Univ, Washington, DC 20052. Tel: 202/676-8512; 800/424-9773 (outside DC)



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For systems applications requiring high quality, dependable CRT display monitors, Ikegami brings you the technology of the future, today.

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CIRCLE 166

Power supplies and accessories
Catalog covers a range of modular supplies and custom systems, including laboratory and test equipment; detailed specs, dimensional drawings, and product/price index are included. **Lambda Electronics, div of Veeco Instruments, Inc,** Melville, NY.
Circle 410

Discrete semiconductor chips
Bulletin covers expanded line of discrete circuits for hybrid-circuit assembly, with dice geometry and technical information on U.S. and European transistors and diodes, jumper and MOS capacitor chips, and semiconductor-chip packaging. **Sprague Electric Co, sub of GK Technologies,** North Adams, Mass.
Circle 411

Multiple-access LAN
Data sheet examines Cinch Pac primary automation controller and Cinchnet network, which connects 125 devices and coordinates 2000 analog inputs plus 8000 digital data points or 2000 analog control loops; communication speeds reach 28.8k baud up to 4000′ (1219 m). **Iconix Corp, Control Logic Products Group,** Natick, Mass.
Circle 412

Elastomeric connectors
Application note introduces a silicone elastomer connector material, detailing electrical and physical properties of high density connectors for interconnecting plasma displays to PCBs; the solderless devices are also being used for display-device testing, burn-in, soft assembly, and prototyping. **Tecknit,** Cranford, NJ.
Circle 413

Digital LSI modem products
Booklet introduces development, test, and support for MP 14.4 and MP 16.0 microprocessor and LSI modems, which provide 14,400 and 16,000 bps, respectively, over voice grade circuits. **Paradyne Corp,** Largo, Fla.
Circle 414

Voice synthesis module
User's guide describes features and operation of the VSM2128-AL2, which incorporates the SP0256 speech processor and a single-chip N-channel MOS/LSI circuit that synthesizes English language phrases through allophone concatenation. **General Instrument Corp, Microelectronics Div,** Hicksville, NY.
Circle 415

Stepper and timing motors
Booklet specifies permanent magnet, hybrid, and variable reluctance 4-phase stepper motors and timing motors; detailed diagrams and performance characteristic graphs are included. **Inland Motor, Specialty Products Div,** Sierra Vista, Ariz.
Circle 416

Flat/planar cables
Brochure profiles planar construction of round and flat conductor, jacket shielded, groundplane, and flat woven cables; parts numbering guide identifies insulation types, conductor materials, and cable configurations. **Phalo Corp, a Transitron Co,** Shrewsbury, Mass.
Circle 417

Fiber optics for computer graphics
Technical bulletin examines configuration and operation of wideband T/R-201X series optical communication systems, in long distance remoting of high resolution RGB and monochrome graphics workstations; CAD/CAM, process control, and image processing applications are illustrated. **Artel Communications Corp,** Worcester, Mass.
Circle 418

16-bit microprocessors with support peripherals
Leaflet examines SAB 8086 microprocessor family, made with N-channel silicon-gate technology in industry standard 40-pin package; applications and technical data are given for associated peripheral configurations. **Siemens Components, Inc, Special Products Div,** Iselin, NJ.
Circle 419

Linear output Hall sensors
Application notes detail how to effectively use the 9SS linear output Hall effect transducer (LOHET), which produces an output voltage proportional to the magnetic field; illustrated with charts, wiring diagrams, and cutaway drawings, the notes review position sensing and techniques for interfacing the LOHET with comparators and op amps. **Micro Switch, div of Honeywell,** Freeport, Ill.
Circle 420

Transistorized inverter UPS
Data sheet highlights Transivert® static uninterruptible power supply systems ranging from 2.5 to 50 kVA, and details components and operation. **UPSystems, Inc,** Paramount, Calif.
Circle 421

Switching power
Foldout pamphlet provides power ratings and voltage/current outputs for 40- to 750-W equipment, along with dimensional drawings and ordering information. **Datapower, Inc,** Santa Ana, Calif.
Circle 422

DEC compatible peripherals
Product summary introduces disk and tape controllers, along with communications controllers and multiplexers, for DEC minis and micros. **Emulex Corp,** Santa Ana, Calif.
Circle 423

Upgrades for IBM Personal Computer
Brochure introduces MicroCard software compatible with Z80, 8086, 68000/Unix, iAPX 286, and 16032 processors, as well as VersaCard and RAM Module memory expansion up to 512k bytes. **Sritek Inc,** Cleveland, Ohio.
Circle 424

Data communication devices
Product reference describes and illustrates various communications equipment, and contains equivalency tables for EIA RS-449, RS-232-C, CCITT V.24, and hexadecimal. **Black Box Catalog, Inc,** Pittsburgh, Pa.
Circle 425

Power supplies
Catalog covers encapsulated modular models with vacuum impregnated transformers and switching power supplies, covering ranges from 1.5 to 500 W. **Calex Mfg Co, Inc,** Pleasant Hill, Calif.
Circle 426

Membrane keyboards
Pamphlet explains how membrane switching works and charts construction, circuitry, graphics, termination, and key arrays. **Cherry Electrical Products Corp,** Waukegan, Ill.
Circle 427

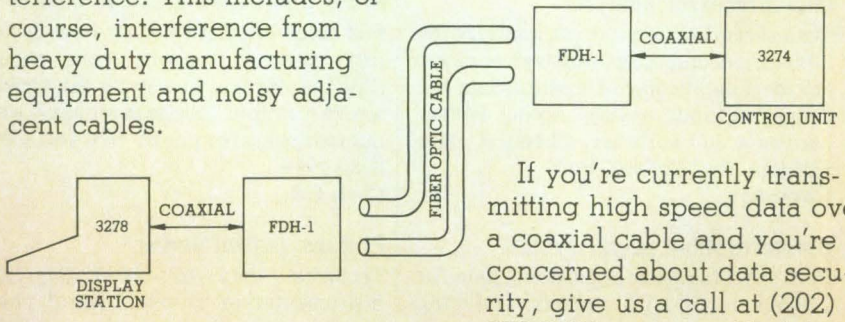
Assorted electronic components
Condensed catalog gives complete electrical and mechanical specs for OEM products such as potentiometers, resistor networks, PCBs, connectors, backplanes, hybrid circuits, DIP and rotary switches, and core memory systems. **CTS Corp,** Elkhart, Ind.
Circle 428

Video display monitors
Catalog specifies color and monochrome monitors and interface cables for small computers, with compatibility charts. **Amdek Corp,** Elk Grove Village, Ill.
Circle 429

Protect your sensitive IBM data with our new Fiber Optic Link

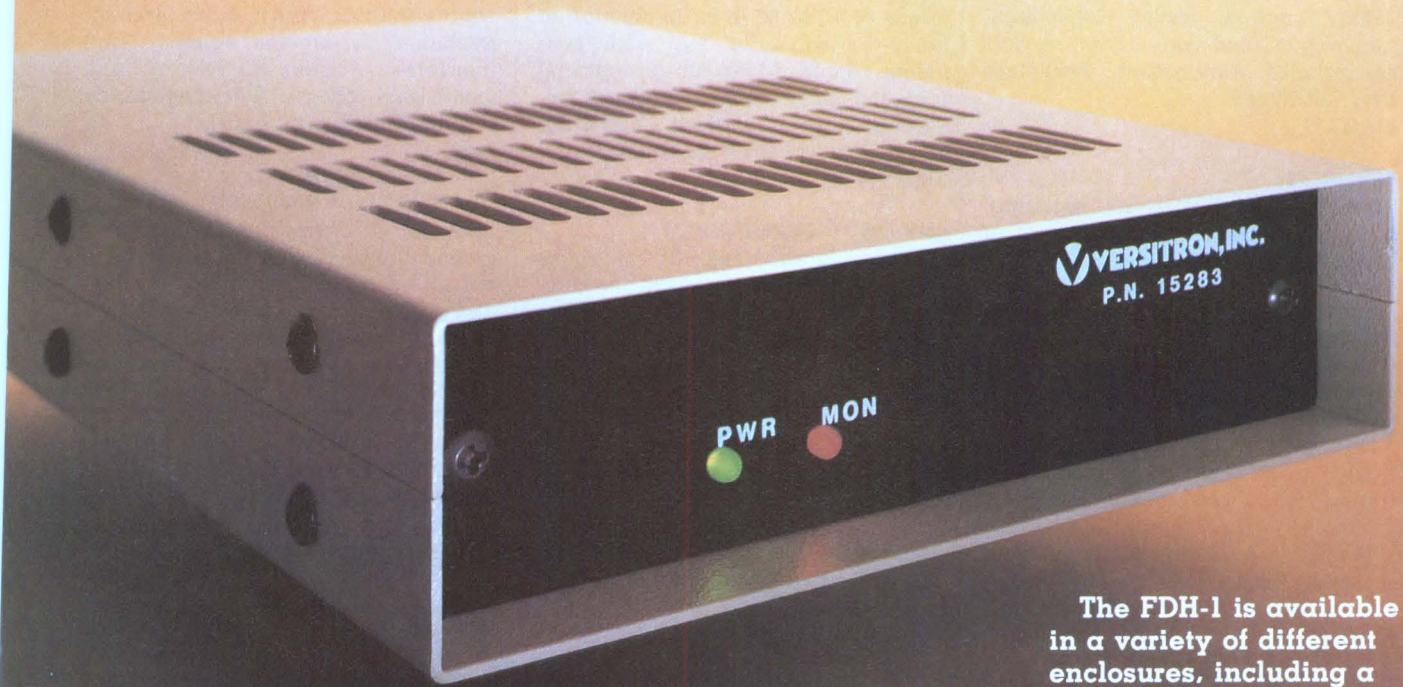
- **Plug compatible with IBM series 3250, 3270A, and 3270B equipment.**
- **Replaces coaxial cable with fiber optic cable.**
- **Up to 1 Km operating range — virtually immune to electromagnetic interference.**

Versitron's FDH-1 (fiber optic digital hybrid) was designed to replace the coaxial transmission path in systems equipped with the IBM 3250 or 3270 series equipment. The simple installation of a fiber optic link provides two very important benefits to the user. First of all, the security level of the transmission link is greatly improved since fiber optic cables are inherently immune to conventional wiretapping techniques. Secondly, the system operating capability will be enhanced since fiber optic cables are impervious to virtually all types of electromagnetic interference. This includes, of course, interference from heavy duty manufacturing equipment and noisy adjacent cables.



Versitron's FDH-1 combines the high speed capabilities of a coaxial cable with the inherent advantages of a fiber optic cable. By interfacing directly to the coaxial cable, the FDH-1 appears totally transparent to the rest of the system; thus eliminating any operating restrictions.

If you're currently transmitting high speed data over a coaxial cable and you're concerned about data security, give us a call at (202) 882-8464 and get all of the details on how our FDH-1 will not only protect your data; but may also actually increase the operating efficiency of your entire system.



The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

VERSITRON, INC.

6310 Chillum Place, N.W., Washington, D.C. 20011, TEL: (202) 882-8464
TWX: 710-822-1179

CIRCLE 167

Fiber optic connectors
Installation sheet gives step by step instructions for complete termination of JSC and DSC crimpless connectors, with 0.9-dB (100-μm core) typical connector to connector losses. **Augat Inc, Interconnection Systems Div,** Attleboro, Mass. **Circle 430**

Microprocessor analyzer
Data sheet describes CDS 460 analyzer for 8-bit microcomputers, which gives direct hexadecimal display of address data for debugging and troubleshooting system hardware and software. **Chemical Data Systems, Inc,** Oxford, Pa.
Circle 431

Uninterruptible power system
Spec sheet tabulates engineering data for 750-VA to 30-kVA models, including frequency output amps and harmonic distortion. **Clary Corp,** San Gabriel, Calif.
Circle 432

Multilayer backplanes
Pamphlet describes wide range of backplanes and connector systems available for special applications; information on quality control, testing capabilities, turnarounds, and consultation services are included. **HADCO Corp, Backplane Div,** Salem, NH.
Circle 433

DC motors
Series 1200 and 1300 models are introduced in separate technical bulletins that summarize performance characteristics; dimensional drawings are included. **Harowe Servo Controls Inc, sub of Bowmar Instrument Corp,** West Chester, Pa.
Circle 434

Power protection systems
Folder gives features and specs, illustrating typical construction and panel details for uninterruptible power systems, sinusoidal ferroresonant regulators, and ultra isolation systems. **Hitran Corp,** Flemington, NJ.
Circle 435

Low profile keyswitch
Pamphlet features DN series SilverLock® technology, a sealed contact design that uses a silicone rubber tube to protect high performance silver contacts from environmental conditions. **Mechanical Enterprises Inc,** Herndon, Va.
Circle 436

Power conditioning technology
Leaflet discusses Mini-Rups rotary uninterruptible power system for 12- to 50-kVA requirements and compares its performance with static type UPSs. **Computer Power Products, div of Sweinhart Electric Co, Inc,** Gardena, Calif.
Circle 437

Hi-res interactive graphics display
Full-color brochure depicts how System 1000's RGC-1000 controller pans, zooms, flips the display, and splits the viewing screen into four independent areas without redrawing the image. **IGC Inc,** Commack, NY.
Circle 438

Process control power
Technical data for laboratory and instrumentation process control power supplies cover models in 10- to 1000-V range with 1- to 50-A currents; output capacities are 100 W to 2 kW. **Fincor, Incom International Inc,** York, Pa.
Circle 439

Enclosed, nonventilated servos
Pamphlet features series C400 dust- and oil-sealed dc servos with continuous torque of 15 to 60 lb-in, in addition to heavy-shafted series F560 with continuous torque of 75 to 300 lb-in; general specs and applications in automated factories are covered. **Contraves Goerz Corp, Motion Control Div,** Pittsburgh, Pa.
Circle 440

Low cost D-subminiatures
All-plastic straight and 90° connectors PD*N and PD*S are described for computer, multicircuit, and telecommunications applications. **Cannon Electric Div, IT&T Corp,** Fountain Valley, Calif.
Circle 441

VLSI controller for Ethernet
Booklet highlights Am7990 LANCE/Am7991 SIA Ethernet node, which optimizes performance and ensures compatibility among components in an Ethernet local area network. **Advanced Micro Devices, Inc,** Sunnyvale, Calif.
Circle 442

Fiber optic kits
Data sheet 80-593 describes six kits: one builds six complete data links; one builds two 20M-baud, full-duplex transceivers; and four contain interconnection components for assorted system hookups. **AMP Inc,** Harrisburg, Pa.
Circle 443

Wire assemblies
Color folder presents line of electrical wiring harnesses, multiconductor cable assemblies, terminated wire, and electrical/electromechanical assemblies. **Custom Wire Assemblies, Inc,** Muskego, Wis.
Circle 444

Sockets, contactors, and carriers
Catalog specifies proprietary IC products, including burn-in, test, and screw machine sockets, in addition to contactors and carriers for flat pack, quad pack, DIP, and TO-5 devices. **Wells Electronics, Inc,** South Bend, Ind.
Circle 445

Fiber optic transmitter
"Understanding the FOT110 Fiber Optic Transmitter" contains detailed charts, performance specs, and explanations of input and operation; reference is aimed at applications design and cable/connector selection. **Burr-Brown Research Corp,** Tucson, Ariz.
Circle 446

16-Bit hybrid S-D converter
Bulletin examines HSD1106 (HRD1106) S/R-D converter, which offers 8/16-bit resolution, 1.3-arc-min accuracy, and transformer isolation for reference and input signal voltages. **Natel Engineering Co, Inc,** Chatsworth, Calif.
Circle 447

Streaming tape handbook
"Streaming" covers tutorial and background information on Winchester technology, along with streaming software and system considerations; one section compares mass storage technologies. Request on company letterhead (for $14.95) from **Archive Corp,** 3540 Cadillac Ave, Costa Mesa, CA 92626.

High temp fiber optics
Data sheet lists optical and mechanical specs for fiber optics in three operating ranges: type X to 260 °C, type XUH to 430 °C, and type XSUH to 650 °C. **Dolan-Jenner Industries, Inc,** Woburn, Mass. **Circle 448**

LED cluster indicator
Catalog describes 1″ (2.54-cm) dia, grouped-LED unit, which continues operating with reduced luminescence when a failure occurs within the light; chart compares LED with incandescent lights. **R. Stahl, Inc,** Woburn, Mass.
Circle 449

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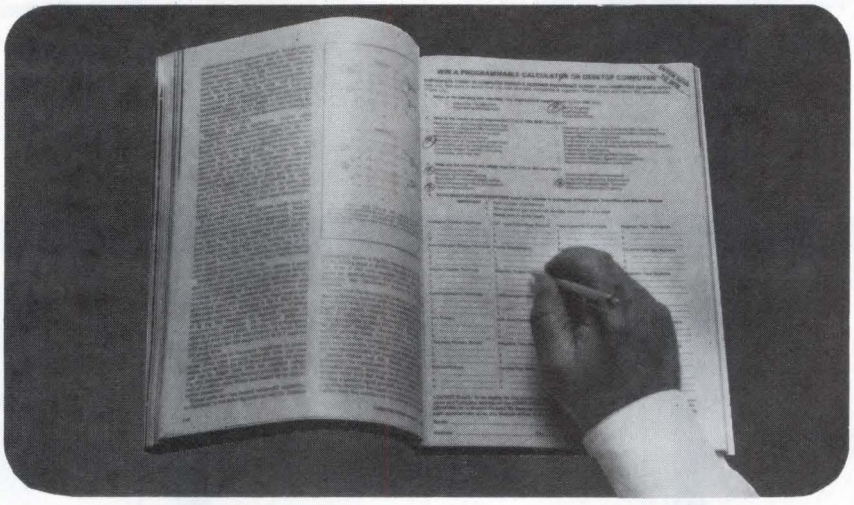

In every issue of *Computer Design* you'll find a bound-in survey questionnaire entitled "Designer Preference Survey." Your participation in these surveys is important. Your answers are significant. They tell our editors what's going on in the marketplace, what kinds of systems you are designing, how your product choices are shaping up, what products, subsystems, equipment and components you are using or would like to use.

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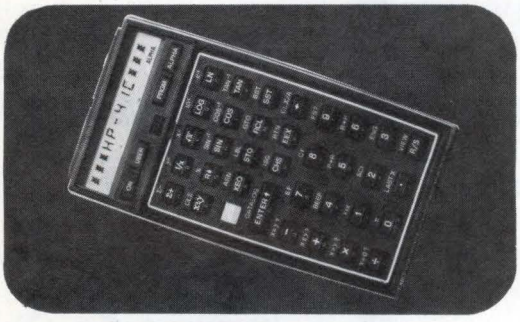
The questionnaires also alert manufacturers to your needs. The inputs you give us help them to develop products with the speeds, ranges, capacities, etc. that you require.

As an added incentive, each questionnaire returned gives you a chance to win a valuable prize. Drawings are made each month, with a grand prize drawing at year end.



MONTHLY DRAWING

HP 41C

PROGRAMMABLE CALCULATOR

The HP 41C offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total operations in function library. You can add peripherals and extension modules to expand capabilities.

ANNUAL DRAWING

HP 85

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This portable (20#) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56 K byte memory, CRT screen, and 150 built-in HP BASIC language commands. You can add peripherals and software packages to expand system capability. A $2800 value!

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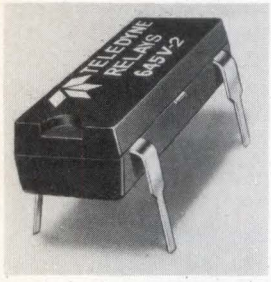

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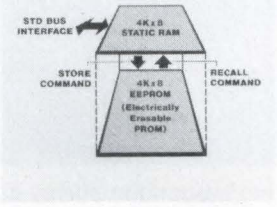

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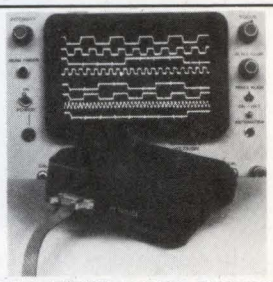

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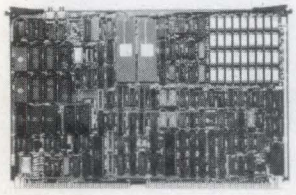

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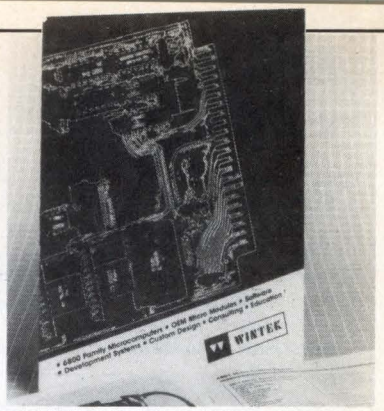

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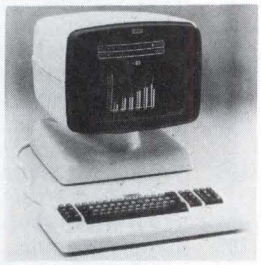

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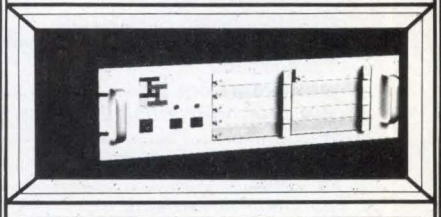

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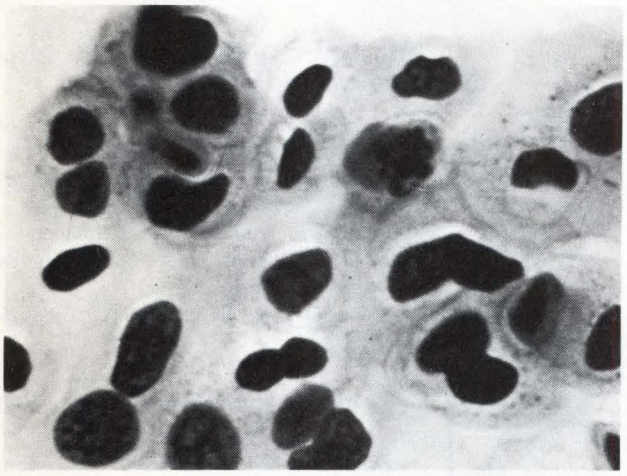

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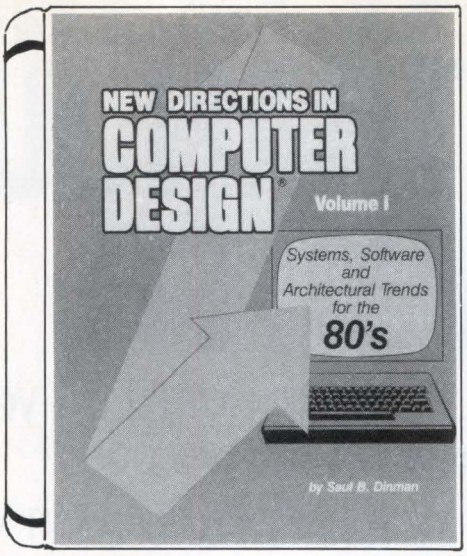

New Directions in Computer Design: Systems, Software and Architectural Trends for the 80's Volume 1, by *Saul Dinman*

Some 20 years of technological innovation have created dramatic developments and changes in the computer systems industry. The book presents systems, software, and architectural trends for the 80's through a collection of articles covering Minicomputers, Microcomputers, Memory Systems, Software, and Data Communications.

PennWell Books, 1982, 135 pages, ISBN 0-87814-209-6, $19.95. **Circle 455**

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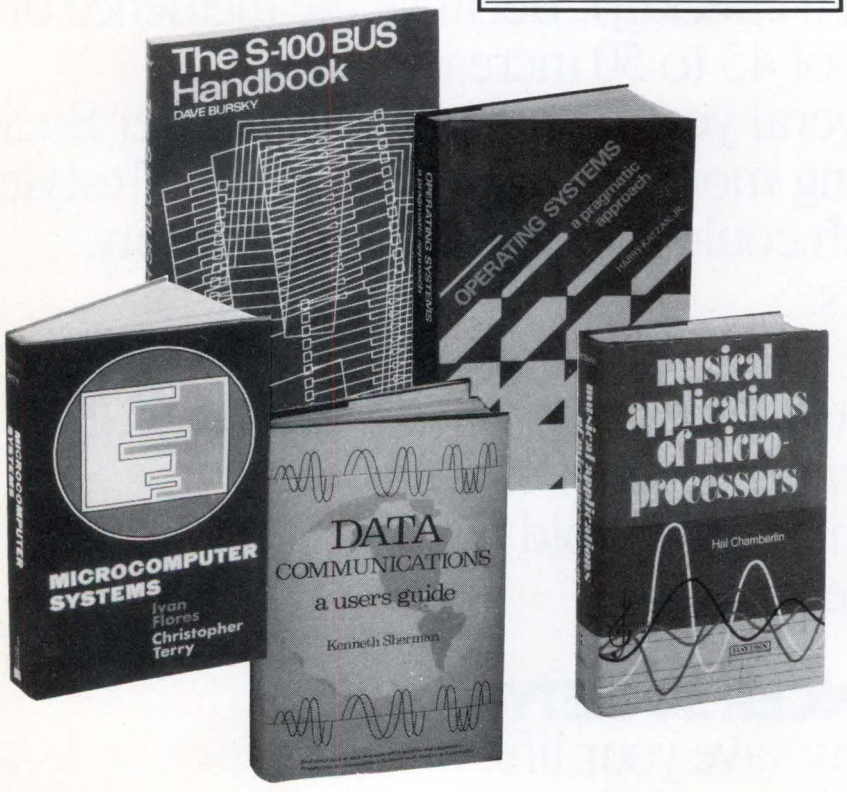

Microcomputer Systems by *Ivan Flores and Christopher Terry*

Until now, microcomputer books simply told how to buy a microcomputer and then summarized what was available, discussed specific computer language and operating systems, or described families of integrated circuits. But this one-of-a-kind guide on microcomputer systems clearly explains both how each part of the system works and how they all fit together.

208 pp, 6 x 9, $22.50, April **Circle 456**

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Immediately acclaimed as a classic! Covers all current electronic and computer music performance techniques as they apply to microprocessors. Signal-processing techniques are presented in nonmathematical language and applied to newer, more powerful 16-bit microprocessors.

#5753-9; 688 pages; Hayden Book Co, Inc.; $26.95
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The S-100 Bus Handbook by *David Bursky*

Exclusively discusses S-100 bus computer systems and how they are organized. Covers computer fundamentals, basic electronics and the parts of the computer. Explains all operating details of commonly available S-100 systems. Each major system board detailed as to its operation and how it connects to the rest of the system.

0897-X, 272 pages; Hayden Book Co., Inc. $15.75
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Operating Systems A Pragmatic Approach by *Harry Katzan*

Computer pro Harry Katzan provides here authoritative coverage of the construction, functions, and terminology of operating systems. He fully explains such areas as dynamic loading and address translation, use of public and private storage, and virtual memory, data sets, and access methods. "A valuable addition to any computing library."

374 pp, 6 x 9, $10.95, February **Circle 459**

DATA COMMUNICATIONS a user's guide by *Kenneth Sherman.*

A BRAND NEW quick and effective source for pinpointing and eliminating system malfunctions, discovering new, more efficient data movement, learning effective troubleshooting, ensuring strong, clear signal transmission and achieving maximum performance and value. Put these *all new* ideas and many others to work for you!

348 pages; 95 illustrations; Reston Publishing Company Inc; $21.95. 1981. **Circle 460**

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- 1K Complex FFT Performance
  1.05-msec Single Data Processor
  0.5-msec Dual Data Processor
- 100-ns Clock
- DMA Transfers at I/O Bus Rates of 20 Mbytes/second
- Modularized 16- or 32-bit Arithmetic Units
- Multiple Processor Configurations for Application Flexibility
- Low-cost OEM Configurations
- Full Software Support at Systems/Utilities/Applications Levels

MARS-232 Array Processor Software
In today's world it is not enough to have outstanding hardware. Our interactive software system, GSP, allows hands-on assembly/disassembly, loading, debugging, and diagnostic services – with multiple processor support built-in. For the real-time environment, we use ESP, a host-resident executive. It provides intelligent supervision for host programs that call applications library or user-defined subroutines, without compromising the speed of MARS.

MARS-232 Applications
With its high computational capacity and low cost, the MARS family provides solutions for a broad range of application areas – on-line video inspection and image analysis; front-end data acquisition, compression, and formatting; spectral analysis, filtering and thresholding.

MARS- a new world of performance for medical, seismic, radar, sonar, and communications systems.

NUMERIX

For additional information on the MARS Family of High Speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500

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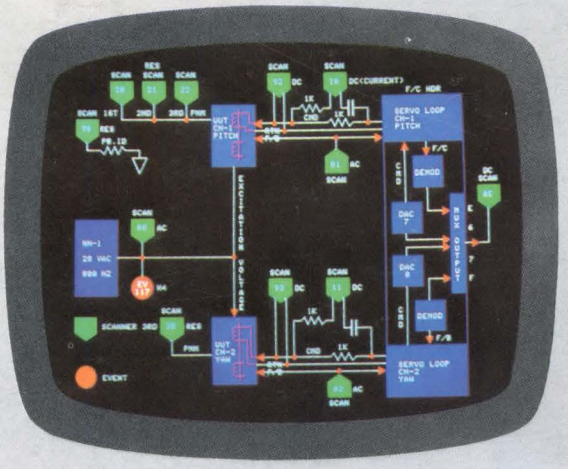

Ramtek's popular 6211 Colorgraphic Terminal is now just $4995.* This versatile desk-top unit is ideally suited for the majority of color graphic applications in CAD, science, business, and control systems. Rack mounted (without monitor), it's even more of a value at just $3995.

Need data terminal functions, too? The companion 6221 with full VT 100™ compatibility is priced at just $5995. Plus, a discount is available on 6211 and 6221 systems when both a color printer and 35 mm slide camera are purchased.

The price of quality has never been lower. Volume discounts are also available. For details, call our office nearest you. Or, contact us at 2211 Lawson Lane, Santa Clara, CA 95050. (408) 988-1044.

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*Light pen sold separately.

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