JANUARY 1983

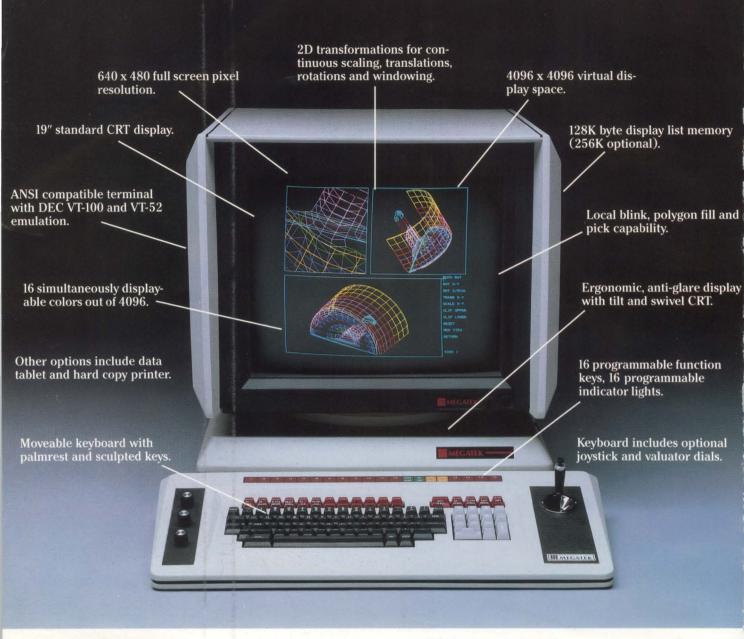
PennWell Publication **BODDEDITER DESIGN** HE MAGAZINE OF COMPUTER BASED SYSTEMS

> SPECIAL REPORT: DISK AND TAPE MEMORY SYSTEMS

OPTICAL DATA STORAGE TECHNOLOGY STATUS AND PROSPECTS

MICROFLOPPIES BATTLE FOR PREEMINENCE

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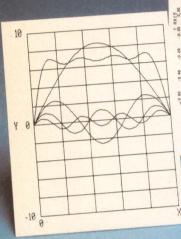
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UP FRONT

Acquisitions and cooperative agreements

Intelligent Systems Corp has agreed to acquire Quadram Corp, a manufacturer of accessories for the IBM PC, by issuing additional shares of Intelligent Systems stock.

Square D Co, througn stock and cash, has acquired U.S. Robots, manufacturer of the MAKER[™] line of robots for computer integrated factory automation.

American Microsystems, Inc, a subsidiary of Gould Inc, has announced a cooperative venture between AMI's subsidiary, Austria Microsystems International, GmbH; and Zeltron, Istituto Zanussi per l'Elettronica S.p.A. Their goal is to form a design center to serve the European custom and semicustom IC market.

Micro Focus Inc will become the main COBOL supplier for Intel Corp's entire line of 16- and 32-bit microprocessors under terms of an agreement. The software will run under the Microsoft XENIX and Intel RMX 86 operating systems and Intel's development systems.

Conferences call for papers

IECON '83, the Ninth Annual Conference on Industrial Electronics (control and instrumentation), will be held Nov 7 to 11 in San Francisco. Proposed papers are welcome on technical aspects of designing, implementing, and testing mini- and microcomputer systems for process control, data acquisition, and instrumentation. Five copies of an 800-word article summary and 40-word abstract should be sent by Mar 1 to R. C. Born, Eaton Corp, Cutler Hammer, 4201 N 27th St, Milwaukee, WI 53216 (Tel: 414/449-7474).

Proposed articles are being accepted for SME's Autofact[®]5 Conference and Exposition to be held in Detroit, Mich, from Nov 14 to 17. Suggested topics include CAD, CAM, CIM, analysis and simulation, graphics, robotics, and human factors, as they relate to tomorrow's automated, integrated factory. Mail 100-word comprehensive abstracts by Mar 15 to Gregg B. Balko, CASA/SME, 1 SME Dr, PO Box 930, Dearborn, MI 48128 (Tel: 313/271-1500, X368).

Abstracts are being solicited for the Oct 10 to 14 Atlantic City, NJ, Second International Exposition on Local Area Networks (LAN 83). Abstracts should be sent by Apr 1 to Paul Fitzgerald, Information Gatekeepers, 167 Corey Rd, Brookline, MA 02146 (Tel: 617/739-2022).

Authors are invited to submit abstracts for either regular or short papers to the 1983 International Conference on Parallel Processing (Aug 23 to 26 in Bellaire, Mich). Topics can be in any area of parallel/distributed processing. Send four copies of 100-word abstracts (including the full text for regular papers, and 500-word summaries for short papers) by Feb 14 to Howard J. Siegel or Leah J. Siegel, School of Electrical Engineering, Purdue Univ, W Lafayette, IN 47907 (Tel: 317/494-3444 or -3653).

Deadline is July 1 for submitting papers for the Orlando, Fla, Seventh International Conference on Software Engineering (Mar 26 to 28). Suggested paper topics include programming methodologies, software quality assurance, interaction between software engineering and related disciplines, and future directions in software. Five copies of 6000-word maximum papers (full-page figures equal 300 words) should be sent to William E. Howden, Dept of Electrical Engineering and Computer Science, Univ of Calif at San Diego, La Jolla, CA 90293.

UP FRONT

Pretriggers

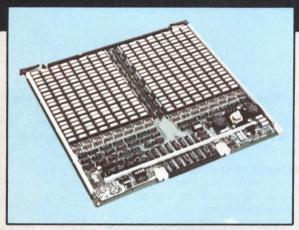
- **Providing resolution of 200 dots/in, an electrostatic color plotter** introduced by Versatec produces a full-color E-size drawing in 8 min, as well as color/monochrome plots in any length. It uses translucent toners in magenta, yellow, cyan, and black.
- A drop-on-demand color ink jet process is used by Tektronix for its model 4691 copier. Yellow, cyan, magenta, and black ink cartridges mix droplets to produce red, green, and blue; juxtaposing dots in a "dithering" process produces a full-color presentation.
- Super-dense ICs in a 5-chip set fabricated by the NMOS-III process pack the power of a mainframe computer into a desktop-size workstation. Hewlett-Packard's HP 9000 32-bit computer can be configured with up to 2.5M bytes of main memory. Operating systems are versions of either UNIX or BASIC.
- A communications package for 10M-bit Ethernet local area networks that enables data transfers at over 100k bytes/s has been developed by Network Research Corp. The FUSION package is available for several operating systems and handles multiple network protocols.
- Data link security in compliance with FED-STD 1027 is accomplished with a Paradyne Corp link encryptor inserted between data terminals and data communications equipment. Info-Lock uses the FIPS-46 data encryption standard algorithm.
- An entry level 32-bit industrial automation minicomputer, Data General's Eclipse MV/4000 supplies performance of 600k Whetstones. It runs under AOS/VS for multi-user applications or AOS/RT32 for dedicated realtime jobs.
- Bulk data point to point transmission over mixed media is accomplished by a multihop satellite data transmission system at rates to 6.3M bps. Bunker Ramo's BR 1720 overcomes database and distribution problems usually associated with satellite signal path delay.
- A transportable software system for designing logic arrays gives in-house capabilities for a wide range of automated tasks. Texas Instruments' transportable design utility now runs on DEC VAX 11/780 and IBM 4341 operating systems.
- 640- x 480-pixel resolution in a desktop color graphics terminal, plus the ability to simultaneously display and manipulate 16 windows independently, are features of Ithaca Intersystems' Graphos. A palette of 32,768 colors allows choice of up to 16 displayable colors within each window.
- CP/M based machines, ranging from 8-bit workstations to 16-bit standalone systems, bridge the gap between personal computers and minicomputers. Televideo Systems' microcomputers allow system growth without obsoleting any computer in the network.
- Measurement and control systems based on small microcomputers plus hardware and software packages have been developed by Data Acquisition Systems. These systems provide measurement speeds up to 20k data points/s with conversion accuracies of 12, 14, and 16 bits.

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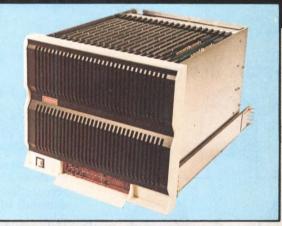


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32MB BULK SEMI

Dataram Corporation, the leader in Perkin-Elmer compatible memory, introduces two new memory products for the Perkin-Elmer 3200 — with storage capacities from 256KB to 128MB. A dramatic demonstration of our ongoing commitment to Perkin-Elmer users, these new memory products are the latest in an impressive family of products that has been meeting the memory needs of the minicomputer market since 1967.

Both feature speed, capacity, reliability, performance...and low price. Features you won't find in memory from any other Perkin-Elmer memory supplier. Products such as high-performance BULK SEMI that are available only from Dataram. All good reasons why Perkin-Elmer users should look to Dataram when they're looking to perk up their 3200 Series computers.

Dataram 2.0MB DR-330 semiconductor ADD-IN memory operates across the complete range of Perkin-Elmer 3200 Series — 3210, 3220, 3230, 3240 and 3250. Smaller capacities of 1.0MB, 512KB, and 256KB are also available and all are compatible with Perkin-Elmer memory management and ECC. Sockets are standard and a spare on-board RAM is provided. These simple-to-install, highly reliable memory boards are backed up by Dataram's standard one-year warranty.

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Dataram's new BS-702, the industry's only high-performance BULK SEMI to interface to Perkin-Elmer's 3200 Series. With everything you need to get optimum performance from your 3200 system. Compact size — 32 MB in 15³/₄". The I/O driver required to support the BS-702. And the impressive capability to drive up to four 32MB chassis...for a whopping capacity of 128MB!

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And when you talk about capability, you'll talk about the BS-702's unique dual-port operation that allows you to bring your image processing, array processing, or data acquisition input in on one port and off-load to your 3200 on the other.

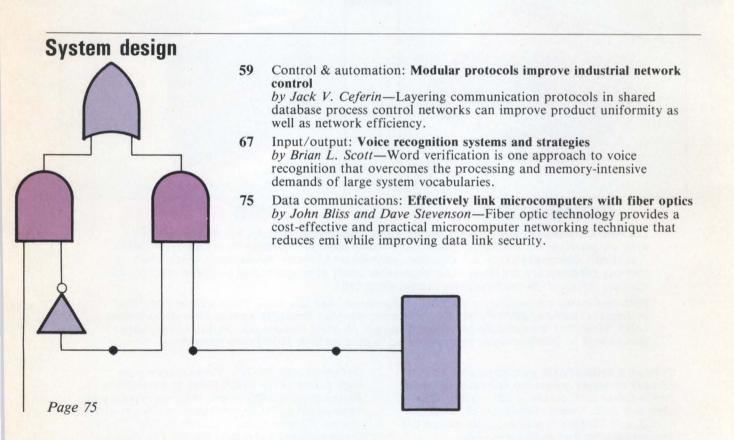


CIRCLE 4

COMPUTER DESIGN[®]

System technology

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- 54 Software: Relational database system uses Forth language for inter-computer portability



ISSCC '83



150 Circuit design, process technologies, and materials will come under scrutiny at the International Solid State Circuits Conference in New York next month. Attendees this year will mark the ongoing diversification of CMOS and GaAs technologies, and the increasing sophistication of dedicated chips.

Vol 22, No 1 Jan 1983

Special report on disk and tape memory systems

85

The mass storage demands of today's computer systems seem insatiable. Competition between the different technologies-and between the growing number of smart and aggressive companies in the memory industrycontinues to drive down prices, boost performance, and enhance reliability. Each breakthrough in mass storage cost and convenience opens up promising new markets. Yet, the proliferation of memory technology may prove a mixed blessing for system designers unless industry standards emerge to provide a path through the maze. Some of the mass storage trends examined in this month's "Design Frontier" include progress in Winchester disk systems (including the role of tape backup). emerging sub-4" floppy disk drives, and the status of optical storage.



This month's cover, entitled "Dueling Donuts," was created by Mark Lindquist and Robert C. Hoffman III on The Digital Effects Video Palette III and D-48 high resolution camera system.

System components

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Designers' preference survey'

Department

191 Computers, graphics & software

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No analyzer gives you better information or more ways to view it.

You're hot on the trail. You've got the best information the best logic analyzer can isolate. Now it's up to you.

You've got to turn that information inside out. Look at it from every possible angle. Close in on tiny segments and pull back for an overview.

And that's just what you can do with the K101-D. It not only captures and records the most precisely defined samples, it lets you display them in nearly infinite ways. Until you spot the clue that sparks the "Aha!"

Display the data.

Start with a data display. Look at all 48 inputs at once, or select any combination. Format them in binary, hex, octal, ASCII or EBCDIC. Mix formats if you like: display four hex and three binary characters, for example, to analyze a 16-bit bus and three control signals.

Search for specific words in your recording. Enter your search words as complete characters or as individual bits. The display automatically flags each match and tells you how often the word occurred, as well as the first and last places it appeared. Step through each occurrence with a single keystroke.

Compare your current recording to known-good system activity stored in the reference memory. All differences are flagged automatically. The first, last and total number of differences appear at the bottom of the screen.

Edit the reference memory directly from the keyboard to simulate desired program activity or suspected errors. Insert or delete whole lines, particular characters, or even individual bits.

Disassemble execution of microprocessor code into sophisticated mnemonics to speed up software debugging. With each disassembly module (8080, Z80, 8085, 8086, 8088 or 68000), you can see the actual instruction mnemonics, along with the address and object code. Full hardware execution is displayed sequentially, including highlighting of all memory and port activity.

Compare the waveforms.

Press the TIMING key and see up to 24 waveforms at one time. Scroll through 60 with the paging feature. Put any waveform next to any other for quick comparison. Delete waveforms for easier viewing. Expand horizontally and vertically for a closer look. Label individual waveforms with up to a 7-character name, like "READ" or "ADDRESS."

The K101-D gives you *two* movable cursors, so you can easily determine the timing interval and number of samples between any two events.



Clearly the Best.

Plot an overview.

Graph mode gives you a capsule summary of program execution, digitized analog signals, or machine cycle activity. Quickly spot address loops, program ranges, erroneous resets or unusual behavior by displaying your choice of inputs as a graph. Each sample is reduced to a single point with its magnitude plotted versus memory location.

The ultimate logic analysis tools.

O'internet

The K101-D (48 channels) and the K102-D (32 channels) are designed for the system problems you couldn't solve any other way.

Their 16 levels of trace control let you sort through long programs and record just the relevant portions, even those separated by many hours.

Their advanced clocking capabilities accommodate virtually any system

architecture—even multiphased, multiplexed and multi-processor systems. Without building some complicated clocking arrangement of your own.

Both perform high-speed timing analysis to 10 ns resolution. And they're fast enough for TTL, ECL and bit-slice devices.

Uncompromising dedication to high performance.

The Gould Biomation philosophy dictates that every instrument we make be the best for the job it's designed to do.

The impressive trace control, clocking and display capabilities of the K101-D and K102-D are evidence of that commitment to excellence.

For detailed application notes or a demonstration, write Gould Inc., Instru-



ments Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279, Gould Biomation and Gould Millennium Products.

For fastest response, call toll-free: Nationwide (800) 538-9320; in California (800) 662-9231 or (408) 988-6800.

Below are four actual K101-D screen displays—timing, data, mnemonics and graph. On all four, address 2121 is artificially highlighted in red to demonstrate how the same information can be viewed from four different perspectives.



Check The Chart Before You Choose Your New 16-Bit **Computer System.**

Columbia Data Products' New Multi-Personal® Computer, Featuring IBM-PC® Compatibility, **Excels In Professional, Business** And Industrial Applications. Check it out.

Columbia Data Products' MULTI-PERSONAL® COMPUTER can use software and hardware originally intended for the IBM® Personal Computer . . . while enjoying the flexibility and expandability of all Columbia Data's computer systems.

Available operating system software includes singleuser MS-DOS® or CP/M 86® or multi-user, multi-tasking MP/M 86® or OASIS-16®, with XENIX® available soon, providing users with a host of compatible software packages for personal and professional business and industrial applications. A large selection of higher level languages are also available, including BASIC, FORTRAN, COBOL, PASCAL and MACRO Assembler.

Our standard 16-Bit 8088 hardware configuration provides 128K RAM with parity, two RS-232 serial ports, Centronics parallel printer port, interrupt and DMA controllers, dual floppy disks with 640K storage, Winchester disk and keyboard interfaces, and eight IBM-PC compatible expansion slots ... and lists for only \$2995. Winchester hard disk configurations, featuring cache buffer controllers for enhanced disk access performance are also available, starting at \$4995.

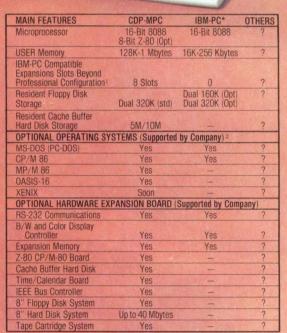
So, when you need to grow, why gamble and hassle with independent third party hardware and operating system vendors which may or may not be compatible. not to mention the hidden expense and frustration of implementing peripheral drivers in the different operating systems and upgrades? Who needs the finger-pointing when things don't work out?

After you review our chart, you will agree ... for overall 16-Bit microprocessor superiority, expandability, flexibility, compatibility and real economy, Columbia Data is your total source.

Our Multi-Personal Computer . . . the 16-Bit system born to grow!

Get yours now





¹For comparison purposes, typical professional configurations con-sist of 16-Bit 8088 Processor, 128K RAM with Parity, Dual 320K 5-Inch Floppies, DMA and Interrupt Controller, Dual RS-232 Serial Ports, Centronics Parallel Port and Dumb Computer Terminal or Equivalent 2Columbia Data Products also supports CP/M 80* with an optionally available Z-80 CP/M Expansion Board





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The design race boils in a lukewarm economy

The proliferation of new product introductions at the recent Comdex, Midcon, and Autofact conventions is a continuing testimonial to the creativity of today's system design engineer. While some proclaim that designers are constantly duplicating each other's efforts in the product race, our editors recognize that these highly motivated and competitive engineers are actually achieving similar design goals in many different ways.

In this month's issue the editorial staff has unearthed some of these latest developments in a Special Report on disk and tape technology. From $3\frac{1}{2}$ " (or is it $3\frac{1}{4}$ "?) floppies, to $5\frac{1}{4}$ " high density Winchester cartridges, the engineering driven product parade marches on. Our editors found that, in addition to cost performance improvements in the disk and tape arena, packaging is playing a very important part in successful product marketing.

With our lukewarm economy, market activity for disk and tape products is centering on the personal and office automation application areas. Here, fortunes are made and lost—sometimes thousands of drives are sold or not sold because of a one-inch package size reduction. For this issue the editors have churned through literally thousands of news releases, attended conferences from coast to coast, met with countless manufacturers, and made Ma Bell quite a bit richer to bring you this important report on disk and tape technology. The report includes major articles on Winchesters, floppies, and optical storage. I hope you enjoy it.

Amald W. fiams

Ronald W. Evans Publisher

FEBRUARY PREVIEW

Special Report on Advanced Digital ICs

As more and more functions are crammed onto a single chip, the decision between using standard or custom and semicustom LSI and VLSI circuits becomes less and less easy to make. In the February Design Frontier Special Report, *Computer Design* editors and invited authors will discuss the value of several alternatives and show how cost, quality, and delivery have become increasingly important factors.

Custom/semicustom IC selection strategies: A staff report indicates that, because custom circuits may represent 50% of the semiconductor market by the end of the decade, system designers should learn the new selection strategies and cost tradeoffs.

Plus other major articles including: Core microprocessor speeds chip development...Crafting a custom sorted access memory...Bringing semicustom IC design in-house...Growth of processor family boosts system options...Minimal solutions to logical dilemmas...The common sense of object oriented languages...Can computers really be friendly?...Providing CMOS benefits to peripheral chips...

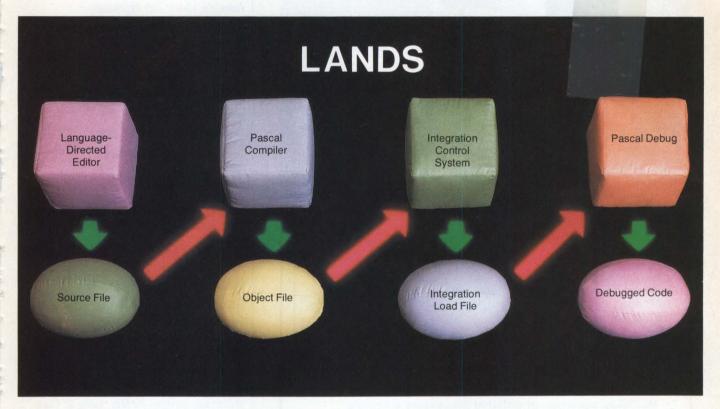
For the microcomputer software engineer who doesn't have time to make mistakes.



EK MICROCOMPUTER SOFTWARE

FLEXIBLE SOLUTIONS FOR A FUTURE OF CHANGE

Tek's new Pascal Language Development System supports you from the first line of source code to the last line of debug.



Conventional Pascal has supported only certain phases of microcomputer software design. Until now.

Tek goes all the way with the Pascal Language Development System (LANDS) for the 8560 Multi-User Development System. A Language-Directed Editor cuts time recompiling.

The Pascal Language-Directed Editor catches and flags syntax errors before they ever reach the compiler.

A Pascal Compiler targets directly to microcomputer design.

The Pascal LANDS Compiler has an extensive array of microcomputer enhancements, including full I/O access and interrupt servicing. Even complete support of I/O simulation during initial emulation and debug. And an optimizer that typically reduces code by 20 to 40 percent compared to other compilers.

An Integration Control System automatically configures the hardware/software interface.

An exclusive from Tek, the Integration Control System (ICS) works from a simple list of usersupplied parameters to generate the hardware/software interface code. Including memory configuration, interrupt handling and initialization/reset code. Integration tasks now take minutes instead of days.

Pascal Debug speeds hardware/software integration.

Pascal Debug completely eliminates time-consuming translations of low-level debug information back into its Pascal counterparts. You can now debug in the same language you programmed in. **Put Pascal LANDS on your design team today.**

Contact your local sales engineer or write us at the addresses below.

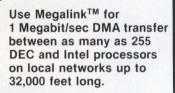
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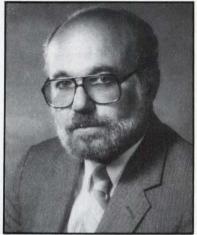


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IF THIS IS A BAD ECONOMY...

If this is a bad economy, and Comdex '82 turned out some 1800 exhibitors with about 50,000 attendees, then what is a good economy going to look like? Though many companies in our field are furloughing employees for the last couple of weeks of the year, and freezing salaries and hiring, you certainly couldn't tell from the looks of the show floor that we are still in an economic slump. Besides the lack of a few large, long time exhibitors, about the only indication that something was still wrong with the economy was the absence of headhunters, their hospitality suite notices, and their flyers delivered to hotels.

Japanese vendors, of course, were present in full force, all of them offering at least one microcomputer. Very little software aimed at closing the man/machine gap was exhibited. Although the CP/M people can't be counted out yet, it certainly looks like UNIX (or variations thereof) is



well on its way to becoming the 16-bit operating system heavy. It was a decided pleasure to find many vendors talking about the C language as a tool for making system software portable. Many of them already have rewritten, or are in the process of rewriting, their current offerings in C to be readily ported into the 16-bit world.

Microfloppies were also much in evidence, not only in OEM form from just about every peripheral vendor, but also in several microcomputer box level products unveiled at the show. The microfloppy, however, did seem to be in a seriously confused state about whether it is going to take 3", 3.5", or just under 4" media. I know that microfloppy boosters like to think of the diskette as a cartridge-like device, but we really can all live without returning to the front load/top load (and worse) days of the 5440 media. Let's all hope that cooperative intracompany efforts already exhibited in the areas of data communications, graphics, and microcomputer bus structures will lead to a quick resolution among the front runners in the diskette business. Otherwise, it's going to be quite a mess next year. Ironically, just as we are on the verge of having portable (or almost portable) system level software, the disk drive vendors are likely to bring home the point that portability is, after all, in the eye of the beholder.

Hinnay

Saul B. Dinman Editor in Chief

Best Technical Article of the Month—May "Compact Code—iAPX 432 Addressing Techniques" Stan Mazor and Sandy Wharton, Intel Corp

Best Technical Article of the Month—June "16-bit Operating Systems, a Whole New Ball Game" Andrea Lewis, Microsoft

These articles will now compete with other monthly winning articles for the 1982 editorial excellence award.

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Power and flexibility in a compact system.

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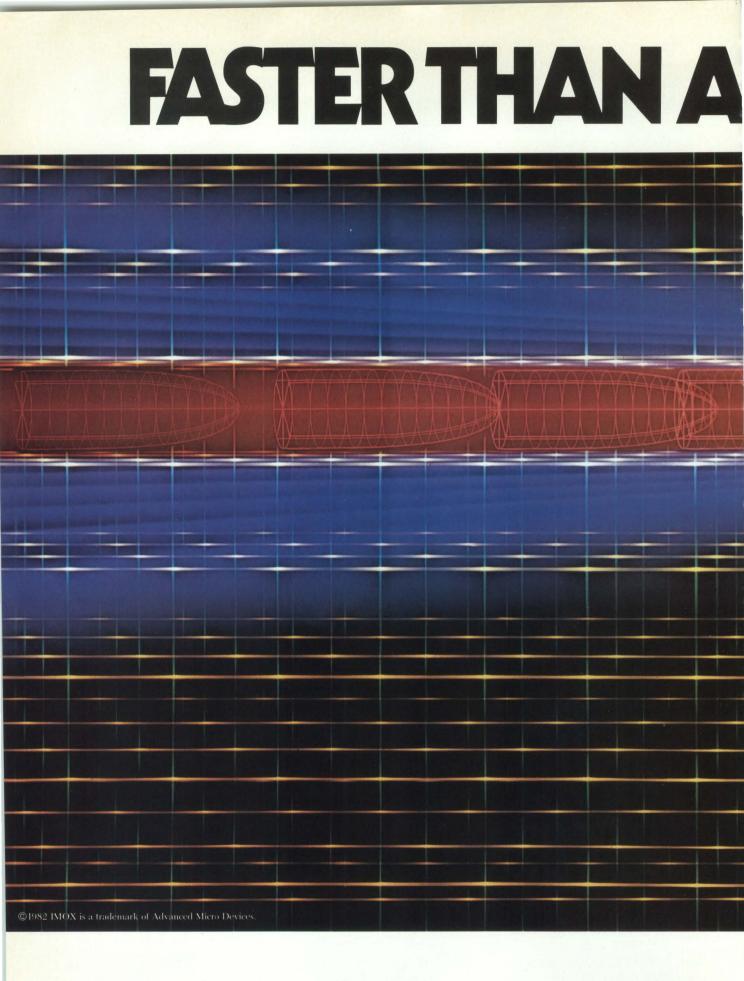
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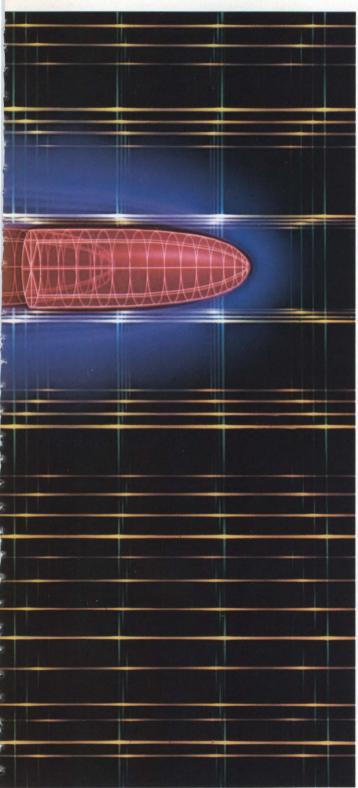
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The Am29116 can control <u>any</u> peripheral. It can do bit manipulation, data merge under mask control, even multiple bit rotate in a single 100ns cycle.

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Ask for the chip that flies.



Fault-tolerant systems lead push for factory automation

eeking to provide the necessary com-S ponents for the factory of the future, Hewlett-Packard has announced the first fault-tolerant computer system for process control, machine monitoring and control, communications control, and facilities management. Systemsafe/1000 pairs two HP 1000 Model 60 or 65 minicomputers executing the same software. User transparent data redundancy is made possible with the Datasafe/1000 software package that provides up to 960M bytes of mirrored disk storage. High speed realtime control is possible with the top-of-the-line A900 technical computer. This computer has cache memory and pipelined architecture for a system throughput of 3 million instructions/s (MIPS).

Complementing the processor offerings are the Process Monitoring and Control/ 1000 software package that supervises and controls continuous industrial processes, and the Programmable Controller (PC) Link/1000-AB that enables HP 1000 systems to monitor and control programmable controllers and any other devices connected to an Allen-Bradley (A-B) Data Highway. The company claims that these products allow manufacturers to get immediate status reports and, if needed, make production changes.

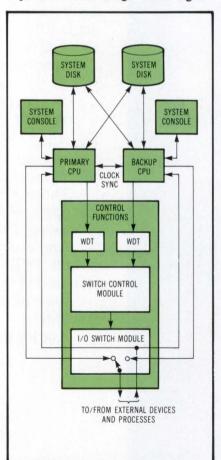
Fault-tolerant techniques reduce error detection and recovery in the Systemsafe/1000 by as few as 200 ms, thus assuring continuous operation of realtime processes. A Systemsafe/1000 system includes dual HP 1000 F-Series computers with hardware floating point processor, for 1 MIPS and 200,000 floating point operations/s (flops). Each computer uses HP's RTE-6/VM realtime, virtual memory operating system for high performance system operation, with fault-tolerant functions handled by a new 1/0 switch subsystem. The Datasafe/1000 software pairs mirrored disk drives and Datashare/1000 software for user transparent disk file sharing by multiple CPUs. Both systems read all serial input data from selected external devices or processors, but only the primary system is allowed output data or control commands. The backup system functions as a "hot-standby." If a failure is detected in the primary, serial I/O control is switched to the backup and system operation resumes in real time. Datasafe/1000 provides uninterrupted read/write disk access even if one of the mirrored disk drives goes down. A fault alarm signals a failure, and a utilities package provides verification and restoration of a failed drive.

Systemsafe/1000 has a price of \$199,000. If purchased as individual

system components, the configuration would cost \$233,000, including freight, within the United States. Current delivery estimate is 12 weeks ARO, with first shipments expected by April 1, 1983.

A typical Systemsafe/1000 configuration also includes redundant HP 1000 Model 60/65 systems with RTE-6/VM and 2M bytes of error-correcting memory, 19.6M bytes of mirrored disk storage, system console ANSI standard FORTRAN 77, and HP Pascal. Datasafe/1000 is available separately at \$5000 for the first copy and \$2500 for a right to reproduce version.

For those users who need higher performance, HP promises that systems incorporating the A900 will be available later this year. The A900 is targeted primarily for the OEM market as a very high performance, realtime engine for industrial automation and process applications. It is well-suited for process monitoring and control, high speed data acquisition and image- and signal-



Systemsafe/1000 uses dual HP 1000 Series F computers sharing serial input from external devices. Serial 1/0 control is switched within 200 ms of error detection. Data redundancy is maintained with mirrored disk storage. processing applications, where the A900's raw computational speed, floating point performance, and sophisticated 1/O capabilities are required.

The computer features a high speed 4k-byte cache memory, 2-level pipelined architecture, 3.7M bytes/s peak I/O bandwidth, and a standard floating point processor capable of performing a typical mix of floating point instructions at 560,000 instructions/s. Implemented in Schottky TTL discrete logic, its CPU comes standard with a hardware floating point processor and HP's scientific instruction set (SIS) and vector instruction set (VIS) firmware. The floating point capability is implemented through three LSI chips developed in HP's CMOS/SOS technology. Unlike most processors requiring a separate board for hardware floating point, the A900 floating point chips are designed as an integral part of the CPU for maximum performance and efficiency. When executing the single-precision Whetstone benchmark (B1), the A900 is capable of nearly 1.2 MIPS.

To complement its processing power, the A900 supports up to 6M bytes of main memory, available in the latest generation 64k-RAM technology. A single memory array board is offered with 768k bytes of storage. Up to eight boards can be configured in the A900 computer. Add-on memory packages of 768k bytes, 1.5M bytes, and 3M bytes are available for \$6000, \$10,000, and \$16,000, respectively.

Available in both box and systemlevel products, the A900 is priced in OEM quantities of 100 at \$15,500 for the A900 CPU set, 768k bytes of ECC memory, memory controller card with 32-bit memory data bus in a rackmountable chassis with power supply, and 15 available 1/O slots. The system price of \$42,675 includes the CPU set, 768k-byte ECC memory, serial and HP-IB interfaces, RTE A.1 operating system, HP 2621B CRT terminal, 16.5M-byte Winchester disk drive, desk style cabinet, freight, and installation.

Extending the reach of these systems is the aim of the PC Link/1000-AB that allows users to supervise and transmit information to any device on an Allen-Bradley Data Highway. One HP 1000 computer accommodates up to 1512 programmable controllers on 24 such highways.

Because access to the controllers is "masterless," the system will not be disabled if a machine-level device goes down. A user interface isolates PC Link/1000-AB from the computer's RTE-(continued on page 26)

It's not Magic, it's NEC.

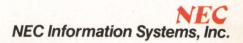
Spinwriters" and disk drives with supernatural reliability.

NEC peripherals are amazingly reliable. For example, our Spinwriter[™] printers often run two years without a failure. Typically, our Winchesters run more than five years without a failure. One of our diskette drives has a field-proven reliability of 24,000 hours—that's an incredible 12 years in normal operation between unit failures. When the rare failure does occur, usually it can be fixed in less than 30 minutes.

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But where do we get 96 UNIXbased systems?

From disk sizes, RAM sizes and user configurations.

The options available to you, with the P/25 and the P/40.

The P/25 offers 24 possible system combinations. With three disk sizes. (22, 36 and 72 megabytes.) Four memory sizes. ($\frac{1}{2}$, 1, 1 $\frac{1}{2}$ and 2 megabytes.) And two user configurations. (8 or 16 terminals.)

The P/40 offers an impressive 72 system combinations. With its three disk sizes. (72, 145 and 290 megabytes.) Eight memory sizes. $(\frac{1}{2}, 1, \frac{1}{2}, 2, \frac{2}{2}, 3, \frac{3}{2}$ and 4 megabytes.) And three user configurations. (8, 16 and 24 terminals.)

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Compare our two systems to the others. Price, performance, delivery, support and configurations. Once you do, you'll see. There's more to Plexus, than what meets the eye.

IPILIEXIUS

Fault-tolerant systems

(continued from page 22)

6/VM operating system and automatically handles error conditions. Unsolicited messages, such as a controller signifying an alarm condition or completion of a task, automatically update user programs. The microprocessor based, multiplexed interface card permits full duplex communications at 9600 baud. A "state of health" verifier provides loopback testing of both the interface card and all components of the A-B Data Highway.

Information collected from these controllers can be managed with the Process Monitoring and Control (PMC)/1000 menu-driven software package designed for small to medium scale processes found in both process and discrete manufacturing environments. A large number of process strategies (eg, feed forward, cascade, cross coupled, and nonlinear control) are within its capabilities. They provide a good fit for such sophisticated applications as material and energy balancing. Customizable capabilities include flexible scanning and updating of all measured and controlled process parameters. Control actions include both proportional integral derivative (PID) loop control and Boolean logic control. Standard functions include engineering unit conversions and averaging, accumulation, and ratio computations. Dead-time, filtering, and nonlinear functions are provided, and user defined algorithms can also be accommodated. In the event of an alarm condition, PMC/1000 ensures that appropriate action is taken automaticallyfrom simple operator notification to shutdown of the process. A logging feature for historical data provides longterm graphical trending, as well as information needed for statistical analysis and management reports.

Prices for complete systems, including an HP 1000 computer and PMC/1000 software, start at \$130,000. A large HP system capable of controlling 100 loops and monitoring 500 process parametersincluding all necessary computer hardware, software, and instrumentation interfaces-would cost \$280,000. The PC Link/1000-AB-including software for up to three interfaces, an interface card, a multiplexer panel, and cabling for connection to an Allen-Bradley 1771-KC/KD communications controller-has a U.S. list price of \$7200, including freight. Multiple unit discounts are available, and current delivery estimate is eight weeks ARO. Contact local Hewlett-Packard sales offices.

-Joseph Aseo, Field Editor

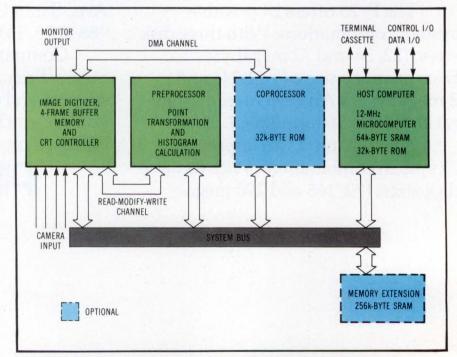
Machine vision system combines low cost and high performance

The "affordable vision system," a graylevel image analysis system from International Robomation/Intelligence, provides a resolution of 256 x 256 pixels with 256 gray levels. An OEM quantity price of \$4995 results from use of a 12-MHz MC68000 16-bit processor capable of 1 million instructions/s (MIPS). Dedicated hardware logic is responsible for image preprocessing and segmentation functions. An optional coprocessor operates in a single instruction multiple data (SIMD) stream mode to process 30,000 to 50,000 complex algorithms/s.

Grav-level image analysis was chosen because it does not have the limitations of binary vision systems. That is, binary vision systems need sufficient ambient illumination and can only extract information in silhouettes, not in contours or edges. A gray-level image analysis can control and stabilize lighting conditions necessary to hold threshold settingsgray levels that determine whether a pixel is black or white-constant. This is not always possible in such instances, as the inspection of objects passing by on a conveyer belt. Silhouette extraction does not work if the inspected objects overlap, in which case contours of the objects must be identified. A similar problem occurs when edges must be detected, but an insufficient contrast in gray level between the object and its background is present.

The vision system consists of three components: a host MC68000 microcomputer with its own 64k-byte static RAM and a 16k-byte ROM, an image digitizer and preprocessor, and an optional coprocessor. Four camera inputs can be selected under program control, digitized by an 8-bit AD converter, and stored in a 64k-byte frame buffer memory (256k bytes total). Conversion and storage take only a single TV raster frame (20 ms). The frame memory is organized so that four bytes can be written or read simultaneously. The preprocessor operates "on the fly" during image input as it is inserted in the read-modifywrite loop of the frame buffer memory. Another DMA channel is dedicated to the coprocessor, complete with special address generation schemes used to perform a variety of operations in SIMD mode.

Preprocessing functions include point transformations of 256- x 256-pixel matrices; equalization of the gray-level distribution of a picture for better contrast enhancement; and setting of multiple thresholds at several arbitrary gray levels. The histogram processor calculates a 127-point histogram simultaneously with preprocessor operations in *(continued on page 29)*



Optional coprocessor processes pixel arrays 10x faster than software routines executed in the 68000 host computer. Digitizer and preprocessor are also implemented in bipolar logic to gain realtime performance.

Circle 240

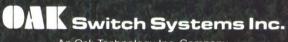
Avoid being called for interference.

October 1, 1983 is coming fast. That's when the FCC Article 15 RFI/EMI requirements become effective. Lucky for you, the Oak FTM (Full Travel Membrane) is ready right now.

The FTM keyboard has an inherent design that offers an optional shielding system which can be easily designed right in. You don't have to re-design your equipment with cumbersome shielding. Or, wait for other types of keyboards that have added shielding with substantial added expense. Oak's FTM[™] keyboard. Fully shielded against RFI/EMI to meet the FCC Article 15, Class A&B deadline and VDE requirements. Right now. At the right price.

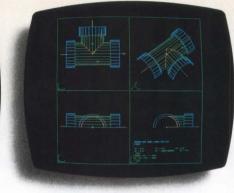
Find out how FTM keyboards block out interference. And they're available now for a surprisingly low cost.

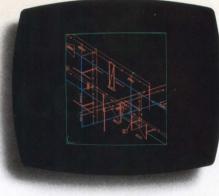
You can't afford not to call Oak. Phone 815/459-5000,TWX 910-634-3353, Telex 72-2447



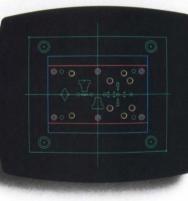
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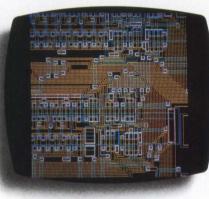












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CIRCLE 18

20-in. x 20-in. digitizing tablet

GR-2412 with standard

SYSTEM TECHNOLOGY/ GONTROL & AUTOMATION

Affordable vision system (continued from page 26)

a single read-modify-write cycle (20 ms). If programmed on the microcomputer, these operations would each take 200 ms.

The optional coprocessor acts as a hardware accelerator for software routines executed in the microcomputer that typically run 1x to 2x slower. For example, convolution of the 256- x 256-pixel matrix with a 3 x 3 coefficient matrix takes 50 ms if performed by the coprocessor, while a programmed routine in the microcomputer requires 3.5 s. Coprocessor operations need only a single instruction fetched by the microcomputer for the entire sequence, with each pixel processed simultaneously along each axis several times before returning to the frame buffer memory. Consisting of a microprogrammed controller; systolic array processor, and buffer coefficients and intermediate values; high speed scratchpad memory; and DMA channel interface, the coprocessor operates in a pipelined fashion capable of performing 20 MIPS.

The host processor performs high level routines such as gray-scale image subtraction, fusing and shrinking of images, stereoscopic image analysis, and color image analysis. The operating system is an extended version of UNIX-7 with a realtime core added to coordinate the system processors. An extended version of C is also available for program development, with direct access to library routines.

A basic system consisting of the host computer and digitizer/preprocessor boards costs \$4995, with the price of the optional coprocessor available upon request. Any vidicon or solid state camera can be used that operates according to either the EAI 525 line or European 625 line standards. The camera must also have an RS-422 interface and an input for external synchronization. **International Robomation/Intelligence**, 6353 El Camino Real, Carlsbad, CA 92008.

—Joseph Aseo, Field Editor Circle 241

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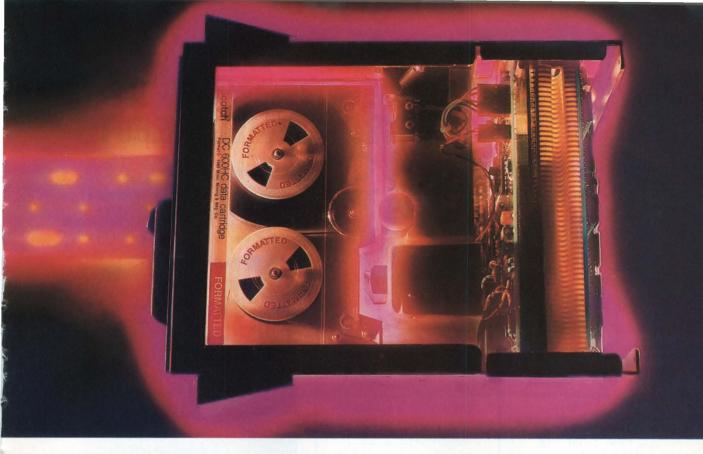
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HCD-75: so much for so little.

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The reason is simple. The 3M Brand HCD-75 Data Cartridge Drive System gives you 67 Mbyte per cartridge formatted. No other cartridge drive gives you so much capacity.

There's nothing medium about the medium, either. Each Scotch[®] DC 600HC cartridge is pre-recorded with permanent forward/reverse-reading block keys. They give you block-addressable storage. You get compact recording on all 16 tracks, with a density of 10,000 frpi, without rewinds.

The HCD-75 system, including drive and controller, is about one-fifth the size of a $\frac{1}{2}$ " tape drive. You don't have to put back-up and I/O plans on the back burner because of size constraints.

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Cartridges interchange quickly and

easily. Tape-to-head alignment is ensured by a special sub-routine. It automatically aligns the read-write head and stepper motor controller to the tape edge each and every time the operator puts a cartridge in the system.

There's brain to this back-up, too. First, all its functions are handled through its controller. And second, there's minimal host involvement, so host time can be freed up for more critical functions.

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You can run one HCD-75 drive off the controller, or two, or three, or four. You still get all the reliability of the high-priced drives. The HCD-75 runs self-test routines to ensure proper operation. It gives you sophisticated error messages when faults are detected.

Advanced error-detection/correction routines keep working to deliver extremely low error rates. The micro-processor controls the drive functions; so potentiometer adjustments are a thing of the past.

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The whole shooting match—drive, controller, preformatted Scotch DC 600HC cartridges—is ready for immediate delivery. One at a time or in production quantities—you name it. (Also ask about 3M's proven family of 8" Winchester compact disk drives.) Haven't you waited long enough for a reasonable, reliable, truly highcapacity alternative to ½" drives?

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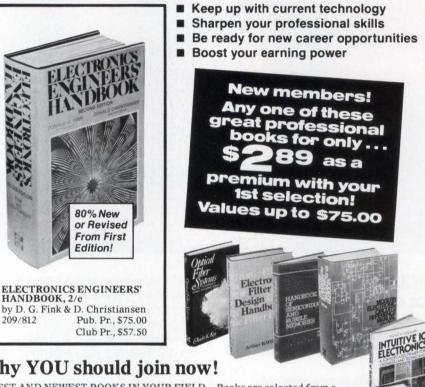
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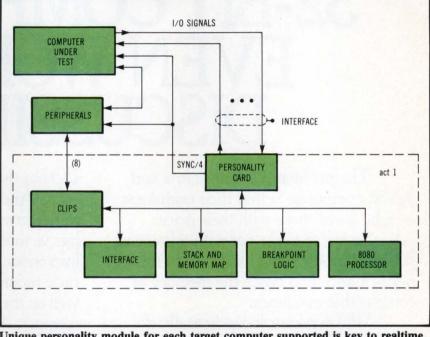
Test system debugs embedded computers without diagnostic software

o ease the task of hardware and software integration for systems that have embedded computers, the act 1 (advanced computer tester) from Loral Instrumentation eliminates diagnostic software and special purpose test equipment. The tester provides a window into the memory and registers of the target computer and enables the user to dynamically alter their contents without interrupting normal system operations. It is intended to aid the development of minicomputer applications, such as the ROLM AN/UYK 19 series embedded in the system, without such typical peripheral devices as video display terminals or line printers.

Functionally similar to a logic state analyzer, the act 1 interrogates up to four of the target computer's 16-bit data buses via a pesonality module unique to that processor. 16k bytes of PROM contain the machine-dependent subroutines required for the act 1 to examine the internal contents, with the needed I/O signal levels provided by signal conditioning circuitry. A typical configuration would include access to the computer data bus, memory address, micromemory address bus, instruction register, control and clock signals, and synchronization outputs. Programmed breakpoints could be evaluated from these buses, or from external signals monitored by an 8-input clip probe. Such signals can either be functions not already monitored within the four main buses, or system events (eg, switch closure, scale change, message acknowledge) controlled by the target system. Users can select breakpoints to execute on values less than, equal to, or greater than a specified value with a programmable mask also available to disregard unwanted bits.

Other options include the ability to specify which portion of the instruction cycle (read, write, or execute) to trigger upon and the use of a programmable counter to measure events in microseconds, milliseconds, or seconds. An external event counter measures the machine clock cycles. Detection of the breakpoint condition will either halt the machine or be flagged to the visual display as an asterisk while the target computers continue running. Up to three breakpoints may be logically linked (AND/OR), or used independently.

Three 1k-bit stacks capture data from the 16-bit data bus, 16-bit memory address bus, and 8-input clip probe.



Unique personality module for each target computer supported is key to realtime operation of act 1. Personality module generates necessary control and I/O signals needed for act 1 to interface independently with target processor. Module also aids disassembly of programs.

Stacks are loaded when programmed breakpoints occur, selected registers or I/O channels are accessed, or all data from the target computer can be stored. Contents of each stack are viewed through an onboard 7" (17-cm) CRT in groups of 16 locations. Scrolling or modification is possible with the hexadecimal keyboard located on the processor, or with an external ASCII keyboard. Data and address stacks are displayed in hexadecimal format, while clip probe data are displayed as eight binary bits similar to a logic analyzer.

Memory locations within the target computer can be viewed and manipulated as well. Up to 48 consecutive memory locations can be displayed in groups of 16 words, or a work area of 18 consecutive locations can be scrolled to change the contents. Users can also configure an overlay map of the target computer's memory to provide read/ write protection, or provide an optional external high speed (70-ns) read/write memory of up to 64k words that can replace or extend the target computer's memory. Finally, a disassembled area of memory can be viewed complete with mnemonics and operands.

Actual runtime execution can be viewed with 40-column trace pages that

display the contents of registers, memory locations, and disassembly of programs as they are being executed. Fifty-three commands within the act 1 monitor and modify the target commands. Up to 16 command sequences are stored for loading and execution from the half-inch magnetic tape cartridge drive. These commands are contained in a 16k-byte PROM and executed by an 8080 microprocessor.

Personality modules are available for the Texas Instruments 2520, Applied Technology ATAC 16M, and ROLM 1602/1664/1666 computers at \$4500 each in addition to the act 1 price of \$19,500 each. Custom personality modules can be designed by the company, or the customer can receive design assistance for his own module. External keyboards are priced at \$1500 each, and high speed 16k- x 16k-bit memory boards cost \$2995 each. Loral Instrumentation, 9020 Balboa Ave, San Diego, CA 92123. Circle 242

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THE ECLIPSE MV/4000[™] COMPUTER. The ECLIPSE MV/4000 has 600K-Whetstone compute power. And an

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600K-Whetstone	-
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CIRCLE 124

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Toshiba's Sunnyvale, California plant which opened over two years ago is finetuned and fully operational. For starters, the 2,000,000 plus ROMs per month being produced, include 16K, 32K, and 64K. Also, at another of our facilities, we're producing the 256K ROM.

The 16K is organized as a 2K x 8 and is pin compatible with the 2716 EPROM. **32** The 32Ks are 4K x 8. They are pin compatible with either 2732 or 4732 type EPROMs.

> Our 64Ks are 8K x 8s. They're available in either

a 24 pin package or a 28 pin compatible with 2764 type EPROMs. Optional features include

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256K Out 32K is a

Our 256K is a 32K x 8 and is available

in the standard 28 pin package. It has fast access time of 150 ns. Standby mode cuts current down to 10 mA maximum. What's also cut down to common sense levels is our lead times, so, delivery's a snap. And the code logistics are quickly and easily handled.

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Serial buses provide small area networks between system ICs, and modules

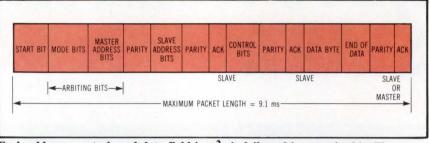
A recent licensing agreement between Signetics Corp, Philips Corp, and Intel Corp will make Intel 8048 and 8051 microcomputers, fabricated in CHMOS, available in the United States. As part of the same agreement, two new serial bus standards, known as "small area networks" (SANS) are also being introduced in the U.S. Philips introduced SANS in Europe to cope with interconnect and modularity issues in microcomputer based equipment design.

One bus, known as the inter-IC or I²C, has been used in Europe for about two years, and provides for serial data communications between ICs on the same board or within the same box. It is used for distances up to 4 m. The digital data bus or D²B now being introduced, connects systems in a network of up to 150 m. Since both buses operate over relatively short distances, they are able to use fairly simple arbitration schemes to avoid bus contention. In the 1²C this means waiting until there is no activity on the bus and then issuing a unique start bit. Units that use the bus issue bits and monitor the bus simultaneously. Thus, if a unit sees a bit other than the one it has just issued, it interprets that bit as a signal to immediately retire from the bus. Immediate retirement is made possible by the short distances that result in short propagation delays.

Both buses distinguish between master/slave and receiver/transmitter units. A master unit can initiate communication with a slave, making those two units transmitter and receiver, respectively. But the master can also request data from the slave, making it the transmitter. In addition, interface logic can be saved in some situations by making certain units slave only devices.

The $1^{2}C$ bus uses only two wires or traces: serial clock and serial data. This allows the designer to distribute functions within a system while paying minimal attention to interconnection problems. Thus, a reduction in the amount of wiring and interconnect routing is one main design savings. In addition, functions can be placed where they are best utilized for display, data sensing, and human interface.

The 1^{2} C uses a packet protocol consisting of a start bit, a 7-bit slave address (SADD), an R/W bit that defines slave as transmitter or receiver, an acknowledge bit (ACK) for the preceding field, 8-bit data characters with no preset limit on the maximum number of characters, and a stop bit. The 1^{2} C's throughput speed is largely determined by whether it is



Each address, control, and data field in D^2B is followed by a parity bit. The amount of information contained in data field depends on transfer mode selected. Information must fall within 9.1-ms limit for message duration.

implemented in hardware or software. An implementation using 64 bytes/ message could transfer 10,900 usable characters per second (cps) in hardware or 153 cps in software implementations. The I²C is intended for applications that are shielded from noise, shielded from or insensitive to radiation, and have modularity that can be foreseen at design time. That is, the desired functions are known and need only be placed in the most convenient way. The bus approach avoids function placement dictated by wiring constraints. Thus I²C is meant to be used within a box such as a TV or a keyboard.

Like the I^2C , the D^2B is a multimaster distributed control bus that uses wire-AND hardware arbitration and ACK bits after each field. It also separates the functions of master/slave and transmitter/ receiver. The D^2B , however, provides data communications between separate boxes; consequently, it must work over a larger area and be both insensitive to radiation and emit very little radiation itself.

The D^2B uses differential signal transmission over a twisted pair that is time multiplexed between clock and data. To accommodate devices with different throughput capabilities, it can operate in three throughput modes. The only requirement is that high speed bus units be capable of switching to lower speeds to communicate with slower devices. All messages on the D^2B are restricted to less than 9 ms, but higher data rates can transfer more data within that time. Throughput for mode 0 is 110 bytes/s, 2423 bytes/s for mode 1, and 8282 bytes/s for mode 2.

 D^2B protocol follows all fields except the start and mode bits with a parity bit. Although the D^2B standard allows only 50 devices to be connected to the bus, the 12-bit address fields for both master and slave units provide 4096 addresses. This permits various types of units such as FM tuners and VCRs to be uniquely defined. The data field can consist of one or more data bytes depending on the mode used for a maximum master to slave rate of 75 bytes/message (given the 9.1-ms constraint). Each data byte consists of 11 bits: 8 data bits, 1 parity bit, 1 ACK bit, and 1 end of message (EOM) bit. **Signetics Corp**, 811 East Arques Ave, PO Box 409, Sunnyvale, CA 94086.

—Tom Williams West Coast Managing Editor Circle 243

Non-networked device linking and X.25 hook-up provided by Ethernet products

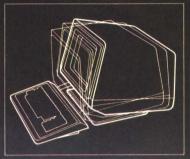
Bridge Communications' Ethernet system product line is claimed to be the first implementation, outside Xerox Corp, of the Xerox Network System (XNS) high level protocols. System throughput for all protocol layers is 1M bit/s.

The recently announced communications server/1 (CS/1) connects up to 32 non-networked devices with RS-232 or RS-423 serial interfaces to an Ethernet network. The gateway server/1 (GS/1) connects an XNS Ethernet network to a host or network with an X.25 interface and two serial ports. Both the CS/1 and the GS/1 are constructed from logical modules.

The CS/1 provides Ethernet access to computers and peripheral terminals, printers, modems, and plotters. Several CS/1s can be used to create a network composed of terminals, computers, and Xerox or Xerox plug compatible equipment.

GS/1 can be used to connect multiple Ethernets in remote locations that are linked by an X.25 network. It can also connect minicomputer and mainframe computers with an X.25 interface to Ethernet.

VISUAL presents ergonomic elegance and high performance in a low-cost terminal.



Tilt: 10° forward, 15° backward



Swivel: 270°

The VISUAL 50 represents a new approach in low cost terminals. Although it costs drastically less, it offers the features you expect from the high priced units.

For example, the VISUAL 50 enclosure is ergonomically designed in light weight plastic and can easily be swiveled and tilted for maximum operator comfort. A detached keyboard, smooth scroll, large 7×9 dot matrix characters and non-glare screen are a few of the many human engineering features normally offered only on much higher priced terminals.

Another distinctive feature of the VISUAL 50 is its emulation capability. VISUAL 50 is code-for-code compatible with the Hazeltine Esprit," ADDS Viewpoint," Lear Siegler ADM-3A" and DEC VT-52.* Menu driven set-up modes in non-volatile memory allow easy selection of terminal parameters.

And you're not limited to mere emulation. As the chart shows, the VISUAL 50 has features and versatility the older, less powerful low cost terminals simply cannot match.



Visual Technology Incorporated 540 Main Street, Tewksbury, MA 01876 Telephone (617) 851-5000. Telex 951-539

\$695 list

FEATURE	VISUAL	Hazeltine Esprit	ADDS Viewpoint	Lear Siegler ADM-5	TeleVideo 910
Tilt and Swivel	YES	NO	NO	NO	NO
Detached Keyboard	YES	NO	YES	NO	NO
N-Key Rollover	YES	NO	YES	NO	NO
Audible Key Click	YES	YES	NO	NO	NO
Menu Set-Up Mode	YES	NO	NO	NO	NO
Status Line	YES	NO	NO	NO	NO
Full 5 Attribute Selection	YES	NO	NO	NO	YES
Smooth Scroll	YES	NO	NO	NO	NO
Line Drawing Character Set	YES	NO	NO	NO	NO
Block Mode	YES	YES	NO	NO	YES
Insert/Delete Line	YES	YES	NO	NO	YES
Bi-Directional Aux Port	YES	YES	NO	YES	NO
Columnar Tabbing	YES	YES	NO	NO	YES
Independent RCV/TX Rates	YES	NO	NO	NO	NO
Answerback User Programmable	YES	NO	NO	OPT.	NO

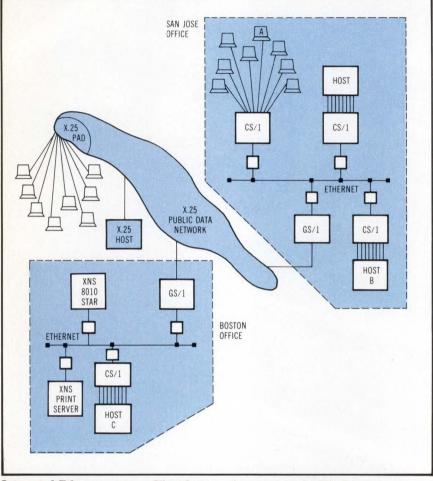
FEATURE COMPARISON CHART

CIRCLE 126

SYSTEM TECHNOLOGY/ DATA GOMMUNICATIONS

Non-networked device

(continued from page 40)



Integrated Ethernet systems. Virtual connection can be established between terminal A and host B or C. Virtual connection supports logical name to physical address name mapping.

Both the communications server and gateway server are based on the company's dual-board MULTIBUS based EC/1 Ethernet controller. The controller fully conforms to Ethernet specification version 1.0 and interfaces to the network at the physical and data-link levels. One board is an Ethernet transceiver interface; the other is a shared buffer board. The transceiver interface is connected to the Ethernet transceiver and performs carrier sense, serialization, deserialization, Manchester encoding and decoding, CRC checking and generation, collision detection, address recognition, loopback, interlock checks, and error reporting. It communicates over the MULTIBUS connector to the shared buffer board. The buffer board has an intelligent DMA to transfer packets between the transceiver interface and its 128k-byte dual-ported shared buffer. A 10-MHz, 68000 microprocessor manages the DMA as a buffer, runs the data-link

software, and optionally executes user installed protocols or other software. The EC/1 controller can be purchased separately.

Hardware modularity is bolstered by the use of the MULTIBUS. Sufficient power supply margin is present to accommodate additional boards in the spare backplane slots. OEMs can easily add value. For example, by using one or more of the spare slots for a special application, a gateway interface module can be added to provide an interface to another kind of local or long-haul network, replacing the Bridge module. A different type of device interface can be used to control devices with interfaces other than RS-232-C. The addition of a disk controller supports disk or file systems not supported by existing Ethernet file servers. A printer controller is able to support specialized printing equipment not currently supported by Ethernet.

Software is also modular. An existing software module can be replaced with a customer's module. Debugging support is available on the central communications processing unit (CCPU), including multibreakpoint capability, program or instruction disassembly, multiple memory inspection modes, and debugger extension support. The CCPU module contains the 10-MHz 68000 and 128k bytes of RAM. Software is downloaded either from a local load device (usually the optional floppy disk unit), from a host, or from the network. If download is from a host, the interface to the host is through the RS-232-C console port using Motorola Standard s Hex format. Typically, software is assembled or crosscompiled on a host.

The 2-board controller set will be available in February and lists at \$3000. CS/1 will be available in March and is priced at \$9900. GS/1 is expected to be available in the second quarter of 1983 for \$15,000. These prices are for single quantity. Discounts are available for higher volumes. **Bridge Communica**tions Inc, 10401 Bubb Rd, Cupertino, CA 95014. Circle 244

Party line network shares printers and disk drives

System resources such as line printers and disk drives can now be shared between several multi-user systems with a local networking scheme developed by Action Computer Enterprise. Networking software allows any user on a DISCOVERY multiprocessor system to assign a remote printer or drive for his dedicated use. Subsequent requests are routed to the DISCOVERY system that actually has the device. For example, user 3 of node 1 can access logical drive D by assigning that particular drive as his own logical drive E. Network information is passed via an RS-422 interface for distances up to 4000 ' (1219 m) at 100k-baud transmission rates.

With each DISCOVERY system capable of supporting 16 user processors (Z80 or 8086/8087 based), a network of 10 nodes can support 150 8-bit and 16-bit users, with a single processor at each node dedicated to network communications. This processor is connected to a high speed serial interface that supports the SDLC communications protocol. It is primarily used to arbitrate competing requests for shared remote resources, respond to resource requests from other (continued on page 44)

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A sophisticated automatic dialer, which allows up to 32 digits to be stored in memory and instantly retrieved by the terminal operator, is included in the V5212P. The modem provides a unique digital or analog input/ output capability and can be used in systems where voice and data transmissions are required.

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Your component-level disk controller project will go much smoother and quicker with our WD1010 LSI Winchester controller. It's a 40-pin device with all the control circuitry needed to control ST500/SA1000 type drives and is compatible with most 8and 16-bit microprocessor busses, handling data rates up to 5MHz.

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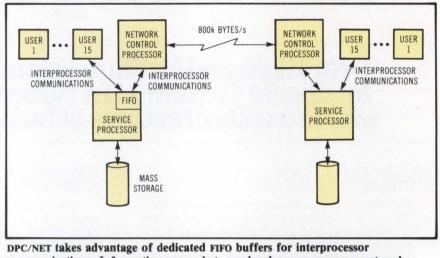
WD1011: Digital Data Separator WD1012: Write Precompensation WD1014: ECC WD1015: Buffer Manager WD1510: LIFO/FIFO external sector buffer WD279X: Single Chip Floppy Disk Controller. Interested? Write on your letterhead for a free sample.



SYSTEM TECHNOLOGY/DATA COMMUNICATIONS

Party line network

(continued from page 42)



DPC/NET takes advantage of dedicated FIFO buffers for interprocessor communications. Information passes between local user processors, network processors, and other nodes in the network via 800k-byte lines with RS-422 interfaces.

nodes, and transfer data from remote resources to local processors.

DPC/NET transmissions use separate clock and data channels driven at different RS-422 levels. Five-conductor cables are used with independent ground to send wake and identify global messages. These messages are sent to all nodes to initialize the line or request an ID exchange conversation. "Get line" and "send request" obtain line ownership if it is not busy, and then send the request portion of the conversation. "Send request" transmits a request block if line ownership is assumed. Conditional "get request" acknowledges a request block or wake-up and identify. "Don't receive" signals that receive buffers are full.

The DPC/NET party line permits brief 2-way conversations (typically 5 ms in duration) between two nodes. Requests for data and actual data transmission are regarded as separate conversations. Line ownership is asserted with individual clock signals that differ by duration (node 1 asserts the clock for 1 ms, node 2 asserts the clock for 2 ms, etc). The conversation can last no longer than 15 ms. Nodes that do not respond within this interval are automatically taken out of the configuration list. No conversations are initiated to that node, except in response to a wake-up and identify message.

Low level software implemented with DPC/NET handles collision avoidance, acknowledge, and line turnaround. High level software is responsible for providing the length, local memory address, party line address, and direction for the next message in the conversation. DPC/NET also handles record and file locking resolution among remote users. Remote private directory drives are not accessible. Individual user I/O directories determine whether the request destination will be the network communication processor or the local service processor.

Network commands are passed from user processors to network processors via FIFO buffers. These buffers are contained in the local service processor dedicated to interprocessor communications. Information from remote resources to local user processors is handled the same way. The company claims that because individual users have dedicated CPUs and memories, there will be no noticeable performance degradation as users are added to the network.

Pricing information for DPC/NET networks is available upon request. Action Computer Enterprise, Inc, 55 W Del Mar Blvd, Pasadena, CA 91105. Circle 245

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Other system designers face the same problems you've already solved. You could help them by writing a technical article for Computer Design. For a free copy of our Author's Guide, circle **503** on the Reader Inquiry Card. Introducing a brainy new solution from the Wizards of Winchester Disk Controllers.

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A new Winchester controller. Plus floppy controller. On one low cost board. Small enough to mount atop a 5¼″ drive. And ST500/SA1000 compatible. "Smart," you say? What did you expect from the Wizards of Winchester Disk Controllers?

We promised you more for less. Our new WD1002 delivers. At \$195 (U.S. OEM quantities) it's \$50 less than its predecessor, the WD1001.

The big news, though, is that we've made the WDI002 the brainiest disk controller yet, with an abundance of new LSI innovations. Such as our WDI010 single-chip Winchester controller device. It replaces the microprocessor on our earlier boards. And about 25 other devices. Plus we've added the new WDI014 Error Correction device and the WD1015 Buffer Manager device.

Because just about every system with a Winchester has a floppy nearby, we included our new WD279X single chip floppy disk controller, too. So you get a complete, powerful solution on one reliable 5¾" x 8" board. And you're on the upgrade path to our upcoming WD1003 and WD1004 boards.

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Components Group, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550

Multiprocessing superminicomputer puts 2 to 10 processors to work under single operating system

inking 2 to 10 processors to shared global memory through a memory bus, the 3200MPS forms a tightly coupled asymmetrical multiprocessor system. Multiplying previous top of the line performance by a factor of 6, Perkin-Elmer's newest creation claims to achieve processing rates of 18.8M singleprecision Whetstones/s.

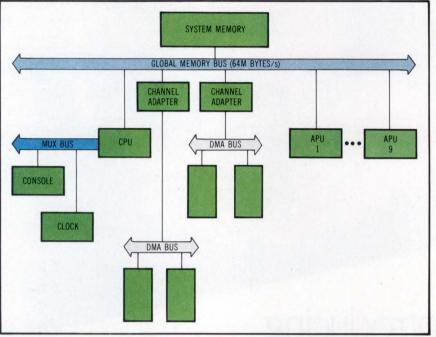
High performance is achieved costeffectively by adding auxiliary processors to the CPU. Built on 32-bit parallel architecture, the system uses 64-bit floating point arithmetic units with dual 32-bit data paths within the global memory bus. Memory modules, general purpose registers, and writable fixed control store also use 32-bit data paths.

Taking advantage of the multiprocessor architecture, extensions to the OS/32 operating system and FORTRAN 7 language are supported. Under OS/32, user written APU tasks run unmodified on the CPU unless they contain calls to the APU microprogram. Control mechanisms for the APU and associated tasks are available to both operator and privileged tasks. Task assignments to APU or CPU can be changed during operation from the console or user written program.

Heart of the system is a 32-bit CPU, built using MSI/LSI Schottky TTL. This CPU monitors all system activity, including I/O and memory management. It also loads all tasks and dispatches application tasks to APUs for execution, and it can perform computation, serving particularly well in I/O intensive tasks.

APUs are general purpose processing units, each with arithmetic processor, floating point processor, and global memory interface with its own 4k-byte cache. Each APU also supplies writable control store, shared memory bank controller, and a pair of realtime support modules (RTSMS) for communication with the CPU. Tasks are scheduled through a microprogrammed scheduler in the APU, cutting operating system overhead. Switching between tasks takes only 200 ns.

Each APU maintains a queue of ready tasks that are processed round robin via the microprogrammed scheduler. Tasks are processed until they either complete or generate a request for CPU service. Instead of executing supervisor calls, the



Growing from 2 to 10 processors, Perkin-Elmer's tightly coupled multiprocessor system 3200MPS handles communications between processors through a 16M-byte global memory over a full 64-bit bus. I/O transfers occur over four independent buses with 40M-byte/s bandwidth.

APU then passes control to the CPU for normal processing.

The global memory system supports up to 16M bytes of directly addressable memory. All APUs and the CPU share global memory, which is implemented on 1M- or 2M-byte boards using 64k chips. Organized in 2- or 4-way interleaved banks, memory has a 64M-byte/s bandwidth on the global memory bus. This bus, made up of two unidirectional asynchronous 32-bit buses, transfers addresses and data to be read or written on one bus and uses the other just for reading data. The system also provides error correction, an error logger, and a memory scrubber.

Serving as the control interface between the APU and the CPU, the RTSM supplies additional synchronization and coordination of processing units. The RTSM is composed of interprocessor data link, identification code, realtime counter with 1- μ s resolution, and eight user-programmable output lines. One RTSM connects to the APU and the second to the CPU's multiplexer bus. The data link is an 8-bit parallel full-duplex, I/O line between the CPU and an APU. A basic configuration of CPU and one APU achieves 4.7M-Whetstone/s performance. Each additional APU raises this number by another 1.8M Whetstones, achieving a total of 18.8M when a full 9-APU configuration is installed. A standard configuration consists of a CPU cabinet and an APU cabinet holding from one to three APUs. Each system supports one shared memory interface through which a number of systems can be tied to an external shared memory system; systems can also be interconnected through the interface.

An entry level system is made up of CPU with 8k-byte cache, floating point processor, writable control store, two communications lines, universal clock, loader storage unit, 2M-byte 2-way interleaved system memory, and I/O chassis; and APU with global memory interface with 4k-byte cache, floating point processor, writable control store, arithmetic processor, shared memory bank controller, and pair of RTSMS. Price is \$185,000. Additional APUs are priced at \$35,000 each. Perkin-Elmer Corp, Data Systems Group, 2 Crescent Pl, Oceanport, NJ 07757. Circle 246

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Fault-tolerant computer systems based on productive redundancy concept

Designed to prevent system failure by automatically compensating for individual downed components, Power_{5/55} systems' fault-tolerant architecture serves in online transaction processing. From Computer Consoles, these systems combine multiple central processors, frontend communications processors, and disk subsystems. All elements function independently, yet in parallel, in a multipathing environment. Thus, the system contains multiple copies of the data base.

Up to eight processors, ranging from M68000 microcomputers to 32-bit superminicomputers, can be implemented in a



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system. Each operates full time, but can compensate for any processor that fails. Processors are linked using a high speed local network and a common operating system.

The entry level family member, Power_{5/20} includes a proprietary CPU based on the MC68000 with 4M-byte memory, 35M- or 70M-byte disk, 20M-byte streaming tape, and the capacity to handle 32 RS-232-C communications ports. Mixtures of RS-232 with RS-422; RS-232 and RS-422 with modem control or parallel ports; or links with the company's Data Highway are communications options.

All systems run PERPOSTM, the company's proprietary operating system. This UNIX compatible system accommodates a high volume, high throughput transaction environment, while providing a development environment. The systems also support FORTRAN 77, COBOL 74, C, and BASIC; database management; and networking capability.

The subsystem of micro based processors performs the bulk of system computation and handles data access transactions to mass storage. Mass storage subsystems provide a global data base; the CPU/disk interface facilitates efficient sharing of disk resources by CPUs and supports data replication techniques. Consisting of dual coaxial cables interconnecting the CPU, distributed communications applications processors, and interprocessor coordination controller, the Data Highway communications subsystem forms a local area network.

All components throughout the system are compatible with the 32-bit VERSAbus. Every subsystem uses a processor board that enhances microcomputer performance by adding instruction cache, memory management, online diagnostics, and diagnostic ports. Memories are designed using 64k-bit chips, and peripheral controllers are equipped with an onboard microprocessor that is linked to the common bus, allowing direct access to memory.

Each CPU operates independently but in cooperation with the others; they communicate by the Data Highway. Distributed communications/applications processors and disk drives can be directly accessed by any CPU. I/O communications use any available path, eliminating bottlenecks and ensuring high throughput. Synchronization is done by the interprocessor coordination controller (ICC) subsystem; although ICCs are replicated, CPUs can assume (continued on page 50)

A new, improved way to give your competition headaches.

he Lexidata System 2000. In terms of price, it's the most affordable step forward in raster technology since the development of raster technology.

In terms of performance, System 2000 will outdo any terminal near it in price and many that cost considerably more.

The combination of which will give you an edge if you're an OEM. In fact, quite a considerable edge.

And what will it give your competition? Something to keep them awake nights. **More OEM flexibility** There are five processor option slots in a System 2000 terminal. They'll allow you to add more serial ports, and more program memory (up to 1.28 megabytes).

A detachable keyboard with integral joystick is standard with preprogrammed peripheral interfaces. User

code may be down-

loaded to augment the system's capabilities, off-load the host CPU, and increase system response time.

Low price. High performance. And a whole new bend in flexibility.

A new ergonomic policy

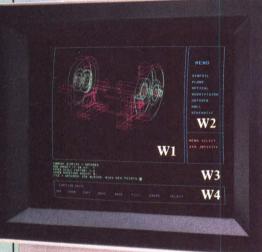
On the screen, there are four hardware assisted work spaces. Each with a set of functions that

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you can call up with simple English commands.

These individual workspaces reduce the overall system cost by eliminating the need for a separate alphanumeric display and a menu space on the digitizer work surface.



What the 4 workspaces do:

W1 Supports pan and zoom. Ideal for interactive graphics.

W2 Accommodates system-select menus.

W3 Is perfect for processing text.

W4 Is used for logging messages or annotating keyboard function keys. Note: Each workspace has graphics and text cursors and is adjustable in size. This feature, plus the fact that the System 2000 has a multitasking operating system, contribute to two very important aspects of customer concern: Ease of learning and ease of use.

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You can put the System

2000 in a PLOT-10 environment very simply. And very quickly, you can improve that environment.

The System 2000 will give you a 62.5% higher resolution on a 1280 by 1024 line screen.

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flicker-free graphics. At a refresh rate of 60 Hz.

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There's more, too. Standard features like zoom, pan, text scroll and independently controlled cursors. And options like an 11" x 11" data tablet and a hard copy interface.

If you're interested in a demonstration of all this call (617) 663-8550 or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

The clear choice in raster graphics.

Productive redundancy concept

(continued from page 48)

their functions in case of multiple failure. Contention among CPUs for resources is eliminated by having the ICC function as a slave rather than as a master to the CPUs.

Every component and interconnection in the system has fault detection logic to detect errors before they propagate to other components. Extensive error checking is done between components and subsystems. When a fault is suspected, the CPU initiates a voting procedure in which all other CPUs check for faults. When a fault is nonrecoverable the failed unit is "contained" and temporarily removed from the system. **Computer Consoles**, **Inc**, 1212 Pittsford-Victor Rd, Pittsford, NY 14534.

Circle 247

Technological and architectural strides produce powerful large scale mainframe

Deriving power from its design, the DPS 88 mainframe computer achieves processing rates $3\frac{1}{2}$ to $4\frac{1}{2}$ times better than its predecessor, the DPS 8/70, and throughput rates 12 times higher. The units' central system components are formed using CML technology and liquid cooled micropackaging. Other attributes are 64k-bit MOS memory chips and 64k-byte fast cache memory.

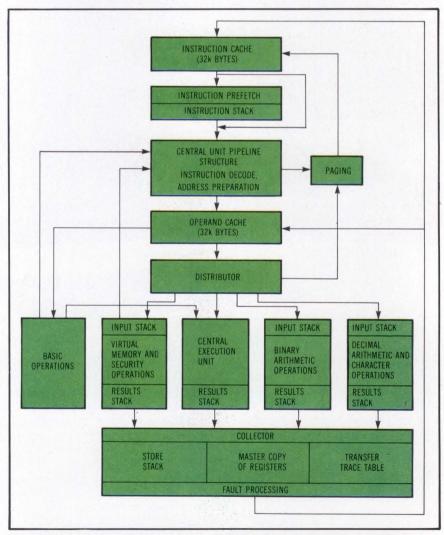
Architectural features encompass a store into cache policy, a 5-stage instruction pipeline, 4-way memory interleaving, native fault testing, and standalone system support facility. High technology circuits combine with the architecture and network oriented operation to provide power to as many as 2000 timesharing users. Single- and dual-processor models operate under the GCOS 8 operating system and serve as hosts in distributed networks, or handle traditional batch, remote batch, timesharing, and interactive workloads.

Modular hardware within the central system consists of 11 components that allow for expansion. Components consist of the CPU, central interface unit (CIU), main memory unit (MMU), 1/0 transfer unit (IOX), channel adapter unit (CAU), system support facility (SSF), system support unit (SSU), central system console, maintenance console, and thermal exchange pump.

All processing occurs in the CPU, with the CIU directing information transfers between the CPU, MMU, and IOX. Coupled with the CAU, the IOX provides the interface between the network or peripheral subsystems and the CIU. These components operate synchronously with circuit clocking distributed from the system clock. A freestanding maintenance processor with special hardware and software, the system support facility implements diagnostic and protection features. The system support unit supplies power entry to CPU, CIU, and IOX and houses the system clock.

Responsible for full program execution and all computations, the CPU performs data and instruction fetching, memory addressing and protection, relative and absolute address preparation, and cache memory management. Each major component within the CPU—instruction fetch (IF) unit, central instruction preparation (CIP) and operand fetch unit, instruction execution units, and result collection unit—operates independently and simultaneously. IF and CIP both use a 5-stage pipeline that permits up to 10 operations to be in process concurrently. Parallel operation of the 5-stage execution pipeline and execution units permits up to 16 instructions to be in various stages of completion simultaneously; maximum instruction completion rate is one per machine cycle.

Typically retrieving instruction and indirect words from the 32k-byte instruction cache, the instruction fetch unit also occasionally fetches from the operand cache or main memory. Up to 30 words can be prefetched and stored in the instruction stack that feeds the CIP. By maintaining a record of transfer and *(continued on page 52)*



Microprogrammed central processor in Honeywell's DPS 88 uses 5-stage pipeline architecture to increase system performance. Responsible for program execution and all computation, CPU components include two 32k-byte cache memories, instruction unit, and five specialized units for executing instructions.

Meet the newest members of our family.

The 1720A Instrument Controller has found a home in a wide range of industrial, factory automation and OEM applications. This powerful microcomputer comes complete with floppy disk, touch-sensitive interface, dual IEEE-488 compatible and RS-232-C interfaces along with our FDOS operating system and enhanced BASIC language.

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1780A InfoTouch Display.

This RS-232-C compatible touch-sensitive display allows you

to fashion a more effective manmachine interface. Use it as a remote display for the 1720A or integrate it into any kind of computer-based system.

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For higher density mass storage, you can't beat bubble memory. And when you add our new Bubble Memory Module to the 1720A, you have up to 512k bytes of non-

volatile file storage that operates in a temperature range of 0°C to 50°C. Helpful when working in hostile

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Large scale mainframe computer (continued from page 50)

indirect instructions, the IF unit can accurately predict changes in the instruction sequence to keep the CIP pipeline flowing with minimum interruption.

The CIP unit decodes instructions, generates memory addresses for the data on which to operate, and fetches data from the 32k-byte operand cache or system main memory. The unit's 5-stage pipeline permits 5 instructions to be in preparation simultaneously, allowing data and operations commands to be dispatched from there to an execution unit at a rate of one per machine cycle.

Interacting with the collector, each of the five execution units handles a particular class of instructions at maximum speed. The collector performs the final

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- 9 slots, 0.6" spacing—or 7 slots, 0.75" spacing
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phase of all instructions, ensures proper instruction sequencing, manages fault handling, participates with the system support facility in instruction retry, and updates operand cache memory.

Cache memory is divided into two segments: one for instructions, one for data. Each block of data in cache consists of eight consecutive main memory words. A program reference to any one word causes the entire block to be read from memory and retained in cache until displaced by another block or cleared from cache by the least recently used algorithm. Cache hit ratio is approximately 95%.

The CPU operates in one of three standard modes: privileged master, master, and slave. With the GCOS 8 operating system, privileged master mode allows unrestricted access to all of memory; master allows access only to authorized portions of memory; and slave is used to restrict user program access. A fourth mode-hypermode-consists of a special set of CPU instructions and related hardware logic. Hyperswitchers, software executing in hypermode in conjunction with SSF software, CIU hardware, and IOX logic, allow the system to divide resources between the operating system and SSF software that controls the functional test system.

Passing information between the CPU, MMU, and IOX, the CIU acts as a traffic controller. Error detection and correction functions are performed in parallel with data flow from the single MMU. Configured with 16M 9-bit bytes expandable in 16M increments to 64M bytes, memory resides in 2 arrays, each having at least 16 memory boards. Fourway interlaced interconnection allows simultaneous access to up to 32 bytes. As seen by the CIU, memory access time is eight words every 225 ns.

Data transfers between main memory and communications lines, peripheral devices, and system support facility pass through the I/O transfer unit that acts in conjunction with the channel adapter. Transfer rates up to 48M bytes/s accommodate multiprocessing and multiprogramming systems.

The dual-processor DPS 88/82 version parallels the single-processor DPS 88/81 configuration, except that two CPUs and two system support units are included. This provides main memory expandability to 128M bytes. Three- and fourprocessor models to come will operate in tightly coupled multiprocessor mode or as cluster systems accessing command files and single data bases. **Honeywell Information Systems Inc**, 200 Smith St, Waltham, MA 02154. Circle 248

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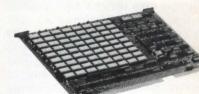




MM-8086E

512K, 256K bytes

- Error detection and correction
- 1000_H boundaries/16 Mbyte address
- Access/Cycle: 300/500 nsec
- CSR/ESR for EDC control and LED error correction indication
- Battery backup option



MM-8086D

- 512K, 256K, 128K, 64K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/16 Mbyte address
- Even parity with output selectable to any of bus interrupts
- ACCESS/Cycle: 250/400 nsec

NON-VOLATILE CMOS RAM (IEEE P796-COMPATIBLE)





MM-8000C

128K, 64K bytes

- · Data retention (on-board batt.): 2 weeks rechargeable batteries
- 4000_H boundaries/16 Mbyte address
- Access/Cycle: 220/220 nsec
- Battery status line allows monitored battery condition Redundant batteries provide improved reliability
- Accommodates 2716 EROM

MM-8086C

- · 64K, 32K, 16K bytes
- Data retention (on-board batt.): 3 weeks rechargeable batteries 2 yrs. non-rechargeable batteries
- 1000_H boundaries/16 Mbyte address
- On-board calendar/clock
- Access/Cycle: 250/250 nsec
- Redundant batteries provide improved reliability
- Accommodates 2716 EROM

NON-VOLATILE CORE MEMORY



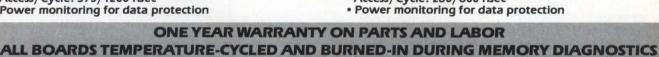


MM-8086/16

- 16K bytes
- For 8 and 16-bit processors
- 4000_H boundaries/1 Mbyte address
- Access/Cycle: 280/800 nsec

MM-8086

- 32K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/1 Mbyte address
- Access/Cycle: 375/1200 nsec
- Power monitoring for data protection



emory

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*Trademark of Intel Corp.

3-D color workstation allows solid modeling

Not only does the CS-3 color graphics workstation allow creation and manipulation of 3-dimensional solid objects, it also provides color shading and antialiasing. The 3-D system from Cubic Systems incorporates 3-D imaging firmware and two 512- x 512-pixel image planes with 12 bits/pixel. It is based on the MULTIBUS (IEEE 796) and uses a 5-MHz 8086 CPU with an 8087 numeric coprocessor. The CPU board also provides an interface to a host computer via an RS-232 serial port or three 8-bit parallel ports.

When the CS-3 is used as an intelligent terminal to communicate with a host, the user can specify a wireframe 3-D object and then fill it in with planar patches. Another method is to build up an object by creating planes and higher order surfaces, interactively scaling and positioning them, and removing hidden lines and surfaces.

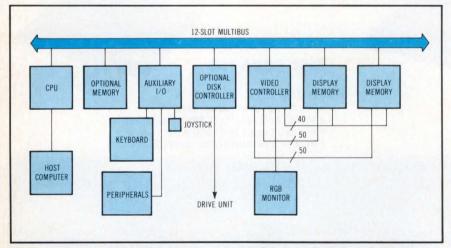
A graphics data set and an instruction set are provided. The firmware instruction set consists of 95 primitive function calls that operate on the graphics data set, the graphics work space, the two image planes, the color map, the 1/0 devices, the host interface, and the memory. These instructions form a complete set and can also be used in a local mode to construct objects without the host's aid.

The system creates images by specifying coordinates, angles, colors, and other attributes as graphics data set elements. Elements in the graphics data set (either integers, groups of integers, or flags) specify attributes in "screen coordinates" (pixel position) or "scene coordinates" (position in 3-D space). Screen coordinates can be from 0 to 511 and scene coordinates can be from -32,768 to 32,768. Firmware instruction can be called from a program or interactively by the user in standalone operation.

The video controller board has a worst-case pixel writing time of 750 ns, or 1.33M pixels/s. This board generates the timing and control signal required by display memory and also contains a MULTIBUS interface that allows the CPU to directly address any individual pixel. Because the system cannot read its contents for numeric values, but can only display them on the screen, the color map is write only.

Two features that aid representation of solid objects are antialiasing, or smoothing jagged lines caused by the raster display, and surface shading. Lines can be antialiased at any stage of the process and surface textures of solids can be shaded to reflect their shape. The system is also able to simulate light falling on the object from any specified point. In addition, texture mapping allows text or any form of texture to be mapped into a given polygon. Texture mapping can also paint a partial polygon in the other image plane.

An auxiliary 1/0 board allows the system to interface with a variety of graphics peripherals such as joysticks and graphics tablets. The system is available in two configuration. Features of graphics terminal version include display memory and processors, color monitor, keyboard, 128k bytes of scratchpad RAM, three RS-232 ports, graphics firm-



Cubic System CS-3 block diagram. A total of 718k bytes of display memory are organized as two 512- x 512-pixel image planes with 12 bits/pixel. To upgrade the system from a graphics workstation to a standalone computer, the optional memory, disk controller, and CP/M-86 operating system may be added.

ware, and 12-slot MULTIBUS card cage. Price is \$9870.

The system can also be expanded into a standalone graphics computer system with the addition of up to 512k bytes of memory with error correction and a disk subsystem. The disk controller board, supplied with the system in its standalone version, allows the addition of up to four drives in any combination of Winchester or floppy. It also provides a DMA controller with 16, 20, or 24 bits of address space. Formatted Winchester storage of 8.4M bytes can be selected. A standalone configuration of the CS-3 uses the CP/M-86 operating system and is priced at \$17,870. Cubic Systems, 2372 Ellsworth St, Berkeley, CA 94704. Circle 249

SOFTWARE

Relational database system uses Forth language for inter-computer portability

C omputer Software Design has implemented a relational database system in Forth to provide compact code size (as little as 64k bytes of RAM). Portability to such disparate systems as the Radio Shack Model II, DEC PDP-11/23, and IBM 3330 computers is also provided. DATA ACE can operate under an operating system or standalone with its own integrated operating system.

Forth was selected as the system's implementation language because of its ability to define complex functions (Forth words) in terms of simpler functions/words. DATA ACE uses a version of Forth that requires only a kernel of 13 primary words, defined in machinedependent code, that varies in size from 200 to 1k bytes. Memory requirements are reduced with the Forth assembler and editor requiring only 16k bytes of memory. A single user version of DATA ACE needs only 48k bytes of memory. Functions are added directly by using the function's name.

As with other relational database systems, data storage is kept separate from the actual application programs. The data remains constant while new applications are developed to manipulate them. Separate query languages manipulate data, fields, and relations (or files). The data interrogation language allows the user to browse through individual records or groups of records and *(continued on page 56)*

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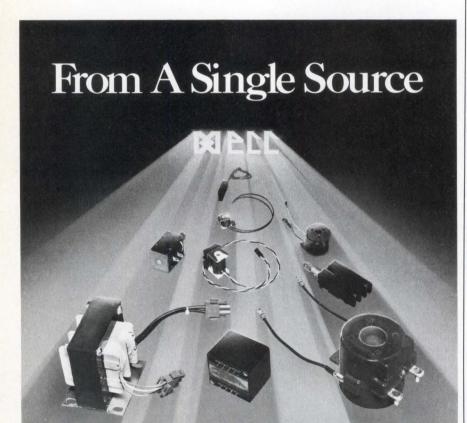
digi-pad

Relative database system

(continued from page 54)

selectively add, delete, or change these records by ADD, DELETE, and LIST commands. Record selection also can be performed with logical operators as $\langle, \rangle, =$, and WHERE. A series of commands can be stored in a catalog mode for speed and simplified access. If a user wishes to merge groups of records together, the JOIN command can select and process data from one relation (or file) based on the value of the data in one or more other relations (eg, list the quantities of components in inventory that are listed on a bill of materials).

The data definition language allows users to change the classifications used to organize the records. Users can define the fields of records up to 256 bytes in



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length as either alphanumeric, signed binary (single precision or double precision), decimal, or date. The total number of records is limited only by disk storage capacity. As with individual records, relations can be added, deleted, or changed with a series of commands. There is a possibility of naming new relations for existing groups of records without modifying programs that access the names of existing relations. Singlelayer sorts based on one key field are possible, as is ability to add a group of numeric fields. Notional relations allow sorts by alternate paths. The notional relation has data identical to the original relation except the order is different. For example, an inventory relation with fields component type and supplier also can be supported by these fields, as well as by inventory. When a user updates the original relation, the notional relations are updated as well.

If a user wishes to manipulate data and relations beyond what is provided in the data interrogation or definition languages, DATA ACE provides a programming language based on polyForth. This language allows users to open up to 12 different relations, input data, move data between relations, and output the desired results in user defined formats. Structured programming statements include if-then-else, begin-while, beginuntil, case, and do loops. Programs can be either compiled or interpreted. The company claims that a compiled program, implemented with three relations and processing both input and output of several forms, has a size of 2k bytes.

The price for single-user versions of DATA ACE for use on Z80 based microcomputers with floppy drives is quoted at \$850, with versions for TRSDOS, CPM86, and MSDOS planned. Multi-user versions of the database manager for IBM 370/3330 processors running under VM/CMS, or PDP-11/23 executing RSTS operating system, will be available later this year with a projected price of under \$3000. Computer Software Design, 1911 Wright Circle, Anaheim, CA 92806. Circle 250

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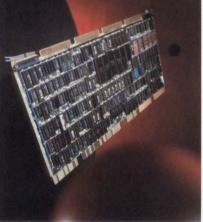
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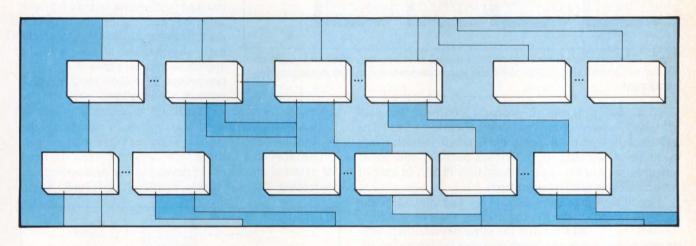


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MODULAR PROTOCOLS IMPROVE INDUSTRIAL NETWORK CONTROL

Layering communication protocols in shared database process control networks can improve product uniformity as well as network efficiency.



by Jack V. Ceferin

icrocomputers in today's industrial environments perform a wide variety of tasks, including operating machinery, mixing chemicals, controlling temperatures, and testing products on an assembly line. Most of these tasks require the microcomputer to have access to and control of large data bases of product information. By providing ready access to such data bases, product uniformity and quality control are easier to maintain.

Connecting such process control computers to a larger host via a network is one way to provide database information to the entire system. (See Fig 1.) With such a network, data are stored in a host computer's data bases and accessed as needed by the smaller computers overseeing process control or product testing operations. In some cases, the data can be stored at intermediate levels

Jack V. Ceferin is a development engineer in the Computer Aided Manufacture and Test Development Engineering Group at Western Electric Corp, 4513 Western Ave, Lisle, IL 60532. His previous experience includes processor test engineering and circuit pack test development. Mr Ceferin has a BSEE and an MSEE from the University of Illinois. on minicomputers acting as minihosts for the controlling microcomputers. When new versions of data are needed, the minihost can procure them by communicating with the host. Data uniformity is maintained since all controlling microcomputers enjoy access to the same master data base. Where the minihosts store the data, it is essential that one mechanism control the transfer of updated data bases so that all process control computers are updated simultaneously.

To facilitate the transfer of these data, each network node needs a protocol—a formal set of conventions and formats regulating communication. Ideally, protocols should be uniform throughout the network and incorporate adequate error detection and correction. In addition, protocols should be modular, allowing the construction of protocol subsets. Each microcomputer performing process control can then concern itself with only those functions necessitated by the manufacturing stage it oversees. An added plus of such protocol modularity is that such a scheme is easily expandable. Changes to the network architecture can be easily incorporated without disrupting ongoing operations.

Network protocols

A typical set of protocols that can be used in a factory network with a master data base is illustrated in Fig 2. The protocols are layered in four levels: hardware, physical link control, logical link control, and dialogue.

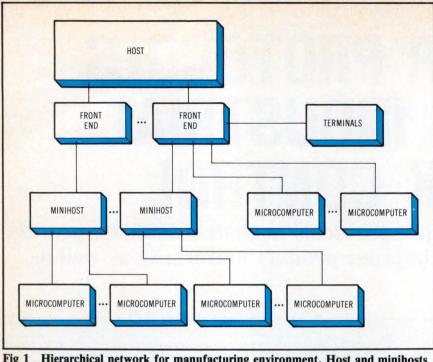


Fig 1 Hierarchical network for manufacturing environment. Host and minihosts administer technical data that drive the microcomputer controlled manufacturing equipment.

The hardware layer of protocol controls the data transmission/reception over the network's wires. The physical link control performs startup handshaking, message sequencing on individual packets, and 16-bit error correction via cyclic redundancy check. In case of error, packets are retransmitted.

The logical link layer establishes and maintains the communication channels required by the system. Since several logical links can use the same physical link, protocols must ensure that each message is directed to the appropriate receiver. The logical link layer also handles message routing and detection of logical link errors as well as flow control. Flow control ensures that a message is not sent until a process control application task is ready to receive it.

By designing network software in layered modules...a flexible software package for industrial control results.

Loosely defined, the task dialogue layer allows two microcomputer controlled tasks to communicate. Two separate tasks can establish a logical link, then talk to each other using any of a number of dialogue protocols. For example, one protocol may transfer files between nodes. A subset of the file transfer protocol might allow the microcomputer to read, write, append, and delete files and to execute command files on a remote node. Generally, a software designer can add further protocols to the dialogue level without disturbing the other layers.

The software package can be divided into two broad parts: a fixed section—stored in programmable read only memory (PROM)—that provides the basic protocol to bootstrap the rest of the software, and a changeable portion stored in random access memory (RAM) that contains dialogue protocols and manufacturing tasks.

The 8k-byte portion in PROM includes interrupt service routine addresses, initialization, physical and logical link layers, and a loader routine-with an abbreviated version of the file transfer protocols-to bootstrap the network from a remote node. The 6k bytes of RAM allocated to network operations include jump tables, the file transfer protocol, and utility tasks. Additional RAM contains the application task codes for the manufacturing operation. The RAM software is stored as downline loadable files on the hosts or the minihosts.

To initialize the network microcomputers, the loader must be invoked twice—first to load network software and again to load the manufacturing applications task. The network file name is fixed, while the application code name is partially determined by microcomputer switch settings. This allows each micro-

computer to select its particular application program. Once the application code is loaded, it can access the network module if it needs to communicate with its host.

This downline loading technique eliminates the need for external mass storage devices at the microcomputer containing the network's operating software. Jump

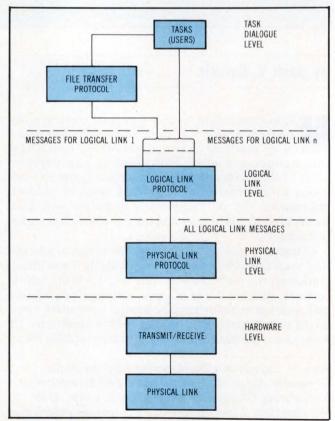


Fig 2 Layered structure of network protocols. User application tasks access network through logical link level or through dialogue level protocol such as a file transfer.

tables allow the RAM resident portion to be changed easily without reassembling the PROM resident portion. Changes to the RAM resident portions merely require reassembling the programs and installing the new version on the host or minihost. New network software and appropriate jump tables can be loaded when the microcomputers are rebootstrapped.

User interfaces

In modular software, communications take place via interfaces that provide the structure for passing commands, responses, and data between modules. In the network package described, these interfaces are structured as commands, associated argument lists to the called module, and answer schemes to the requester. Since all microcomputer software is assembled using cross assemblers on the host computers, the macro capabilities of cross assemblers are exploited to simplify the user to network interface. (In this context, a macro is a programmer defined instruction and associated arguments.) Each requested network function is implemented as a macro plus arguments. (see the Table).

For example, \$CONECT NODE1, TASK1, FAIL, LINK commands the network to establish a logical link to TASK1 on NODE1. If the request is accepted, the network returns control to the user program, with the local link number in symbolic address LINK. If the request is refused, the network module branches to FAIL. The advantages of using macro commands are threefold: they are simpler than the interface's argument lists; they can provide defaults for some arguments; and, of course, they request the function with one program statement, leaving the cross assembler to generate inline code.

Information that needs to be sent asynchronously from one module to the user, such as the successful completion of a connect, is handled by a mailbox and

	User Network Access Macros
Command	Function
\$CONECT	Connect to task
\$DISCO	Disconnect from task
\$TRANS	Transmit message
\$INTRR	Transmit interrupt message
\$RECVE	Enable receive of one message
\$OPENR	Open file for reading
\$OPENW	Open file for writing
\$OPENA	Open file for appending
\$TREC	Transmit record to remote disk
\$RDREC	Read one record from remote disk
\$CLOSE	Close the file
\$CLOP	Close and delete the file
\$DELET	Delete a file
\$SKIP	Skip to next record
\$SCOMF	Open new, temporary command file for execution
\$EXCF	Submit existing command file for execution
\$DCNST	Initialize this node
\$LOAD	Downline load a program file
\$OLOAD	Overlay load a program file
\$DUMP	Dump a contiguous block of bytes to a file
\$PRINT	Print a message on the terminal

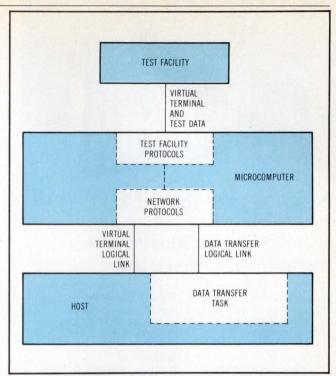
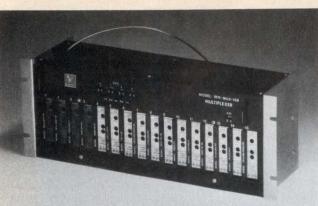


Fig 3 Test computer/host interface scheme. Microcomputer acts as protocol converter, exchanging messages between test computer and host. Multiple logical links allow one link to be used to make test computer's terminal into virtual terminal of host, while another link transfers test data.

software interrupts. Every time the network package loads the mailbox, a subroutine is called from the user's program that logs the message for later action or—if necessary—the user's program takes immediate action. Without the subroutine, an entry in a jump table immediately returns from this call. Then the user must monitor the mailbox so that no messages are missed.

To increase this network's flexibility, the software includes a number of utility programs. The previously mentioned loader is available for loading files that are specially formatted by a postprocessing program. There are two ways to load a file: normal loading (the file is loaded, and control is returned to the calling program) and overlay loading (the file is loaded, but control is transferred to the loaded program). Dumper—a routine that dumps any contiguous block of memory in a loader compatible format to a host file—is useful when two programs cannot simultaneously reside in memory. Program A is dumped to the host, and program B is overlay loaded in the same RAM area. After program B is finished, it calls loader to overlay load program A again.

Another utility allows a minihost and a microcomputer to pass console messages to each other that are transparent to the application running on the microcomputer. The network debugging technique (NDT) also operates transparently to the application code. Initiated by the host, the NDT allows a programmer to remotely analyze the microcomputer software and to debug it from a host terminal without physically disturbing the microcomputer. This technique provides more complete access to the microcomputer than is possible from the microcomputer's console. The NDT also examines or modifies bytes, words, or registers; removes and inserts breakpoints; halts the microcomputer and restarts it



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from that same point; starts execution from a specified address; and dumps up to 128 bytes of microcomputer memory back to the host.

Layered networking sample

Interfacing computer controlled test equipment to the host where test data reside illustrates one use of layered networking. Such a scheme is accomplished using multiple logical links. Rather than design sophisticated protocols for each device to be tested, a microcomputer is used to interface the network data base with a single test computer. (See Fig 3.) A simple message protocol transfer between the testing computer and the microcomputer -and, consequently, the host-is all that is needed.

According to the philosophy of layered networking, the microcomputer should do as little data manipulation as possible. Instead, it should act primarily as a data transfer medium. Most of the system's intelligence resides in the end processors. In a configuration such as this, the microcomputer merely converts from one protocol to another. Therefore, a test computer operator can command the microcomputer to connect the host over one logical link; this allows the test computer to become a "virtual" terminal providing the benefits of a timesharing terminal. Now, the test computer operator logs in to the host and runs a data transfer task from the host that connects to the microcomputer on a second logical link. Using another level of protocol that is transparent to the network, this data transfer task actually transmits the test files. The test computer operator can now select any number of commands in the host program, including file editing, through the host's own microcomputer controlled terminal link.

By designing network software in layered modules, interfaced by calling routines from one section to another, a flexible software package for industrial control results. This modular approach yields several benefits. First, such an approach is easier to implement than an all-inclusive network software package. Second, the use of downline loadable files makes protocol code changes much easier. Modularity, in union with network utilities, also results in easier and quicker debugging of network software. Finally, by layering network protocols in a modular software implementation, the network gains the flexibility needed to maintain multiple logical links. Operating in unison, such links allow the network to communicate with the host while it transfers data to a microcomputer. The resulting increase in network efficiency can help keep the production line moving.

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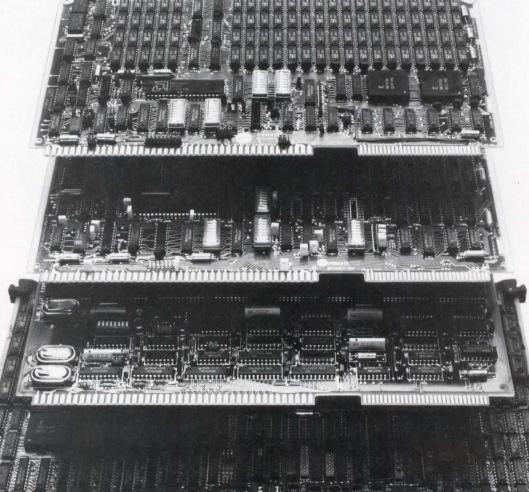
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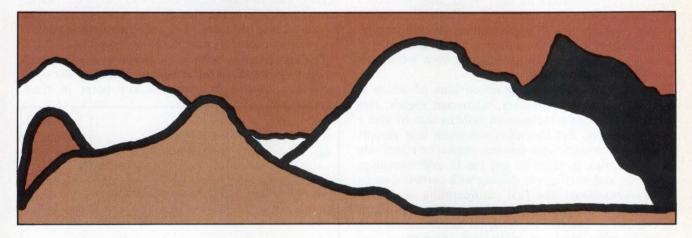
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by Brian L. Scott

peech recognition technology, though still imperfect, can be used effectively in many ways. Incorporating a technique called word verification, low cost recognition devices can perform flawlessly wherever the computer expects a specific input. The computer must simply verify that the specific input has occurred. It is, however, important to know the limitations of current speech recognition technology before attempting to design this technology into products.

Speech recognition is a process of matching an unknown utterance against a number of known utterances, and selecting the closest match. (See Fig 1.) The elements required to make an inexpensive, fast, accurate, and simple to use recognition unit are cost-effective acoustic analysis, efficient data reduction techniques,

Brian L. Scott is president of Scott Instruments Corp, 1111 Willow Springs Dr, Denton, TX 76201, where he is responsible for guiding the research and development of speech recognition projects. Mr Scott holds a BA in psychology from the University of California, Riverside, and an MA and a PhD in psychology from the University of Waterloo. and effective pattern-matching algorithms. The highest performance, costliest recognition systems use linear predictive coding (LPC) for acoustic analysis and dynamic programming (DP)—nonlinear time warping for pattern matching. DP's strengths are that it does not throw away any data when setting up templates and that it forces the best possible fit with the unknown utterance. Computational speed and memory requirements keep the price of high performance recognizers high. Low cost uses of these techniques have tended to suffer in response time. New chips, however, are being introduced that will soon enable these techniques to be incorporated into low cost, accurate, and fast recognition systems.

Dealing with limitations

There are limitations to LPC and DP. Most LPC analysis is done with fixed sampling intervals that tend to smear fine temporal events. Adding to the problems of temporal smear are the inevitable temporal distortion problems of DP. The strength of nonlinear time warping forcing the best possible fit—can also be its curse when fine phonetic distinctions often rely so heavily on rapid temporal events.

Memory requirements are another limitation of DP. DP works because it retains a detailed description of each word. Large vocabularies soon become taxing if an

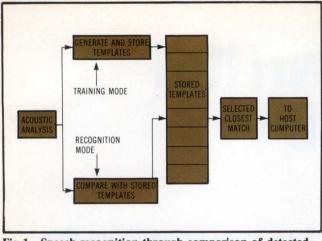


Fig 1 Speech recognition through comparison of detected and stored voice templates. Computer detects closest match between spoken and stored templates but falls prey to time distortion errors and memory limitations.

accurate representation of each word must be stored and matched with each unknown. Perhaps the solution to this problem lies in segmentation techniques that allow recognition of the smallest building blocks of speech, the phoneme. Unfortunately, such techniques have yet to be developed.

There are barriers-the most obvious of which is memory-to large vocabulary, connected speech, and speaker-independent recognition systems that fit into a small computer. But that does not mean that current technology, even low cost systems, cannot be effectively used. The trick to effective use lies in understanding, accepting, and intelligently dealing with current state of the art limitations. The first consideration in dealing with these limitations is the price/performance ratio. Zero-crossing analysis (zero signal amplitude) is one possibility that may not work quite as well as LPC analysis for extracting formant data, but with a clear speech signal, it does a passable job. The analysis consists of first dividing the speech signal into two frequency regions. Fig 2 shows oscillograms of a zero-crossing analysis of the words one, two, and three. F1 includes the range from 250 to 1000 Hz, and F2 includes the range from 1000 to 5000 Hz. For each frequency channel, zero-crossings are detected and then integrated by a low pass filter. This inexpensive preprocessor system clearly estimates the major formants of speech. The component cost is minimal.

An alternative to nonlinear time warping is linear time compression. In Scott Instruments Corp's VET* series, an utterance of any length up to 1.5 s is divided into eight equal parts, and an interpolated point at each of the eight spacings is stored as part of the template. A spectral histogram is also generated to compensate for durational differences of utterances without changing the overall length of each template. Variances are calculated and stored for each data point to help account for random variations in the template. This use of linear time compression and feature extraction is simpler than DP, but the associated data reduction may be detrimental to performance. However, an Apple computer can perform realtime recognition using the linear time technique as a background program to a VET system. Response time is fast—typically within 200 ms of the end of the utterance—even with a full vocabulary.

Reducing vocabulary size

Of all the factors involved in making the technology work, perhaps the most important for the system designer is vocabulary size. In fact, vocabulary size is the only one under the designer's control. A small vocabulary is easy to use, easy to remember, less prone to errors, and does not necessarily limit applications. Computers, after all, only understand "yes" and "no."

Larger vocabularies should only be used when the end user is willing to take the time to learn how to talk effectively to a machine. Individuals must learn to speak consistently and tailor their vocabulary for maximum effectiveness. Because of the learning required to talk effectively to a computer, the user must be strongly motivated before voice is an acceptable alternative to keyboard or touch-sensitive screen input. Handicapped persons who have lost motor control of one or both hands have benefited considerably through voice control. The time it takes to learn voice control is trivial when voice is the primary means of operating the computer.

The simplest way to improve performance in speech recognition is to limit the effective vocabulary size—the number of allowable words at any point in time.

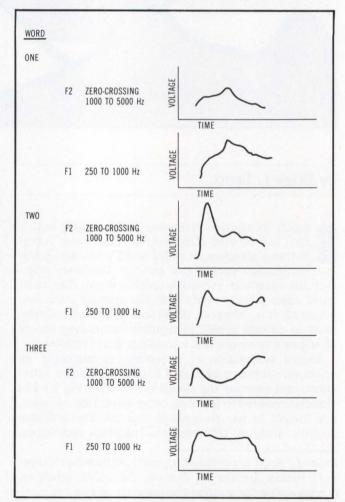


Fig 2 Zero-crossing analysis of words "one," "two," and "three" provides estimate of major resonant frequencies of speech. Signals are derived by first dividing speech into frequency regions F1 and F2.

^{*} VETTM is a trademark of Scott Instruments Corp.

However, the smaller the active vocabularies, the more stilted the user speech and the more difficult the software design. This is a critical point for the designer. Although the best system for the current technology is one that limits active words to two or three at once, the best recognition system for the user has the maximum vocabulary. That is, operators want to talk to the computer in their own language, but the computer is most comfortable with "yes" and "no."

The crux of the problem-and the reason that so many speech recognition applications have failed—is that the speech habits of the system operator are not yet compatible with the needs of the machine. The attraction of voice is that it allows a natural mode of communicationhuman language. But that natural, overlearned mode of communication is not easily modified. The machine's need for a simple language makes it seem primitive to users. When the human response to input problems encountered with touch-sensitive screen technology or bar-code systems is compared with the response elicited by voice input systems, the problem becomes more understandable. When the touch-sensitive screen does not work, it is assumed to be the operator's fault. The operator adapts to the bar-code reader or perhaps goes back to the instructions to find out exactly how to hold the wand. If the bar-code reader errs, users ask what they did wrong. But no machine is going to indicate that the operator spoke incorrectly. The point of this analogy is that when new methods of input are learned. users assume errors are their fault. But users cannot tolerate errors when the machine begins to tread on their area of expertise-natural language.

System designers should realize that voice data entry is not the only application for recognition devices.

One way to combat this basic psychological barrier to speech recognition technology is through word verification. (See Fig 3.) Word verification actually represents a shift in thinking about the use of voice. As discussed above, most applications to date have attempted to place the user in control of the computer through speech. The computer must struggle in vain with its limited vocabulary and capabilities to discern the operator's desires. When using word verification, the computer calls the shots and checks to see if the operator understands by verifying computer-selected keywords.

Word verification techniques

Word verification is based on the 1-word vocabulary. That is, regardless of total vocabulary size, only one word or phrase is acceptable at a time. If there is only one active word, then the task becomes to verify the active word, not to select the correct word from among several as is done in most speech recognition applications. Word verification is much simpler for the recognizer than word selection, a fact that makes the system much more effective. More data can be kept on each word, and more processing time can be devoted to the single word. The vocabulary becomes completely

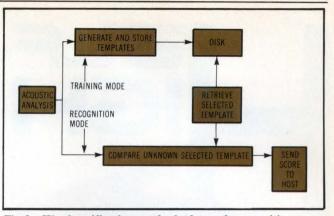


Fig 3 Word verification method of speech recognition. Computer drives interaction with its user by selecting word from its vocabulary and then verifying user's response to it. Memory and processing demands are reduced since only one word is under analysis at a time.

disk based and the limitations on the total vocabulary size are dictated solely by the mass storage capabilities of the system. Thus, the technical advantages of word verification are improved accuracy (the task is simpler), faster response time (only one word to process), and an extended disk based vocabulary.

An experimental system called voice-aided wirewrapping is an example of word verification. Hand wirewrapping is a tedious task that requires constant checking and rechecking. A common technique for reducing errors is to supply voice prompts of the locations to be wrapped via a tape recorder so that the operator need not continually glance from board to list. The problem comes when the user needs to have a location repeated. Rewinding the tape is time-consuming and inaccurate, and magnetic recording in general gives no indication of the person's performance.

Voice-aided wirewrapping can be accomplished with an Apple computer that has voice input and output capabilities. The user sits in front of the board to be wrapped and activates the system. The computer speaks the location of the first integrated circuit (IC). The user locates the IC and repeats the number. Upon verifying the correct IC number, the appropriate pin number is spoken by the machine. The operator locates the pin number and repeats. The computer then tells the operator where to wrap the other end of the wire, and the process continues. The system-rich in checks and rechecks—focuses the user's attention on the operation at hand and works because the computer sets the rhythm of speech and because it always knows what to expect. Improvements in performance can be expected because the computer will not allow the operator to advance to the next step until it has verified the current command. If the machine hears an incorrect command, it will continue repeating the same command, thereby drawing the user's attention back to the last step.

This application's effectiveness stems from the overall system design. Speech recognition is not the key feature of the system. It is one of several techniques for error reductions. If the recognizer is only 80% accurate at rejecting errors, the error rate has still been significantly reduced. In addition, the use of voice adds a method of pacing the machine and asking for repetition if the command is not understood. These factors alone help reduce error rate. 5¹/₄ Floppy Disk Drives TEAC FD-55

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in Scott Instruments' VBLS* system. This voice based learning system is a software/hardware package designed for education and training. The idea behind this system is that the computer asks the questions and the user answers them. The Scott system is actually an authoring system that enables the computer novice to generate educational courseware. The system is straightforward and easy to use. Any application where some repetition learning strategy is required can benefit immeasurably from voice input. When one considers that the option to voice in this application is multiple choice or direct keyboard input, the value added through voice recognition is obvious. The training of speech recognition systems is always

Another application of word verification is illustrated

considered a problem. In the VBLS systems is always considered a problem. In the VBLS system, training becomes part of the user's learning process. For example, when used to aid the training of foreign languages, the VBLS system can be installed in the traditional language lab. The student hears the word or phrase from the tape recorder and repeats it, as always. However, this repetition is then used by the computer as the training template. After completing the traditional lesson, the student can then practice the new vocabulary while being drilled by the computer on translations and pronunciation. The strength of this system is that voice is integrated into a complete system where the computer demands performance of the user rather than vice versa.

System designers should realize that voice data entry is not the only application for recognition devices. In fact, given current technology and short term prospects for speech recognition, voice data entry may be one of the poorest applications. The designer may be much better off considering systems that use the computer to guide users through a complex task, such as voice-aided wirewrapping. Other possibilities include data verification where error-free data are critical, a redundant check on input, or many training applications.

Speech recognition may still be in its infancy but, even today, it is good and inexpensive enough to be cost effective. The keys to cost effectiveness are understanding what voice can and cannot do and developing user friendly systems that accentuate the positive aspects of speech recognition while recovering gracefully from errors.

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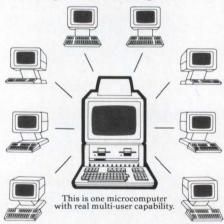
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EFFECTIVELY LINK MICROCOMPUTERS WITH FIBER OPTICS

Fiber optic technology provides a cost-effective and practical microcomputer networking technique that reduces emi while improving data link security.

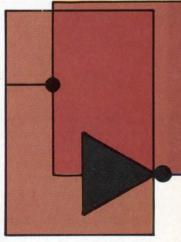
by John Bliss and Dave Stevenson

s microcomputer control becomes more common in industrial environments, the engineer's concern about electromagnetic interference rises. Electromagnetic interference can result in lost information or the transmission of erroneous information. It can also cause computer controlled machinery to fail. In an automated environment, such factors create a serious safety question. A practical technique that drastically reduces interference problems, if not eliminates them, is to interface hardware with a serial fiber optic communication line.

Although fiber optics dates back to the seventies, its expense made it untenable as a solution to data

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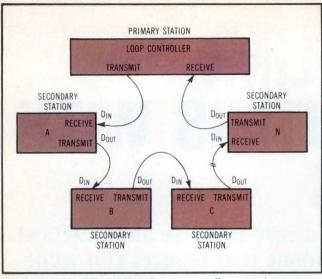
communications problems. However, thanks to improved manufacturing techniques and higher volume production, the present cost of a fiber optic line is competitive with coaxial cables of equal transmission capability. In fact, short distance, low data rate (tens of kilobits per second) communications systems, using plastic fiber that sells for less than thirty cents a meter, can be designed. Plastic, field-installable

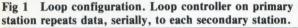


connectors are available at about twenty-five cents per termination; light sources and detectors cost one to two dollars; higher quality glass fibers and appropriate connectors for long range, high data rate systems are not appreciably higher in cost.

Besides cost-effectiveness, fiber optic line has a number of advantages over twisted pair or coaxial wire: electromagnetic interference (emi) immunity, broad bandwidth, security, size, and weight. Because optical fibers neither radiate nor pick up emi, crosstalk between signals and radio frequency interference errors are eliminated. Fiber optic line can be installed adjacent to high voltage cables without fear of interference. This emi immunity also eliminates the need for expensive shielding or conduit pipe required by most electrical codes. The use of optical fibers is well within the recent FCC regulations restricting the magnitude of emi

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generation in data communications systems. Today's optical fibers also have bandwidths up to several hundred megahertz, while some fibers are good up to several gigahertz.

Since optical fibers are extremely difficult to tap, data transmitted optically are secure. To insert a tap, the fibers must be broken or the fiber cladding stripped to allow contact with another fiber's core. Both methods are easy to detect and difficult to execute. Finally, a 1-km reel of optical fiber line, which is capable of equal or greater data handling capacity, is about one-tenth the weight of a corresponding coaxial cable. The optical fiber's diameter is also considerably smaller than coaxial cable's, allowing more signal-handling capacity per unit cross-section of a conduit or cable trough. This lighter weight also eliminates the need for the load bearing strength members of traditional cable.

Fiber optics line networking

The basic network architecture of a fiber optic line uses a full-duplex transmitter and receiver connected by a pair of optical fibers. The transmitter-receiver pair can be used for either two terminals or multiple terminals. A multiterminal network requires a looping configuration (Fig 1).

The primary or host station initiates the data flow. Data are then passed serially through the secondary terminals and back to the primary. The result of this loop arrangement is that each terminal operates in a half-duplex, 1-direction mode; that is, each secondary station receives optical data, feeds them to its terminal, and retransmits the data to the next terminal.

As data pass around the loop, any secondary terminal recognizing its address in the address field of the information frame reads and acts on Since optical fibers are extremely difficult to tap, data transmitted optically are secure.

that frame. The data continue to pass down the loop whether a terminal has acted or not.

Secondary stations are given an opportunity to transmit local data when the central terminal transmits a poll command. If a secondary station desires loop control, the host must grant it by a "go ahead" flag following the poll command.

The network illustrated operates from the Motorola EXORbus, which interconnects a group of EXORterm 155 terminals with an EXORcisor development system. The system uses a fiber optic network interfaced with an MEX6854 advanced data link controller (ADLC) supporting the transmitter and the receiver. The fiber optic transmitter and receiver are interfaced to the ADLC in the clock recovery and loop-through circuit (Fig 2). The clock recovery circuit synchronizes a 1-MHz oscillator (divided down to the 62.5k-bps data rate) to the incoming data from the receiver. Both the data and separated clock information are delivered to the ADLC. The data rate clock then routes data back to the transmitter to be sent to the next station.

In the event of a power loss to any terminal in the loop, a separate power supply or battery pack operates the transmitter and receiver circuits. This allows the loop-through control to repeat its information to the rest of the network during one terminal's power-down.

The fiber optic transmitter uses an MFOE1200 light emitting diode (LED) [Fig 3(a)]; the receiver is an MFOD1100 p-i-n (intrinsic semiconductor diode) photodiode [Fig 3(b)]; the driver circuit for the transmitter uses an MC74LS04 inverter and one discrete driver transistor. The circuit can drive the LED at a 1M-bps data rate.

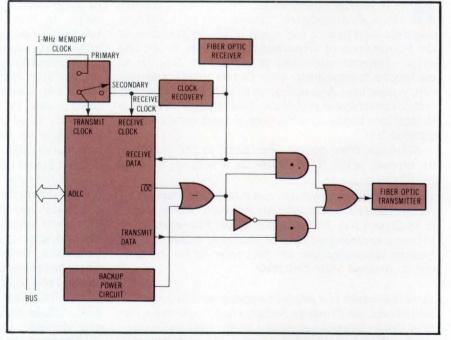


Fig 2 Clock recovery and loop-through circuit. ADLC interfaces to fiber optic transmitter and fiber optic receiver in clock recovery circuit. Power backup on board prevents network crash, should one terminal fail.

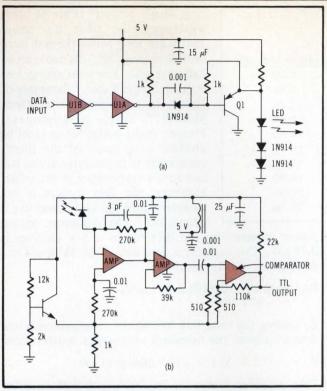


Fig 3 Optical transmitter with LED (a). Circuit can drive LED at a 1M-bps data rate, far in excess of 62.5k-bps link illustrated. Receiver is p-i-n photodiode, requiring shielding from emi (b).

Although the optical fiber is impervious to emi, the actual receiver circuit is not. It is shielded, therefore, to prevent noise pickup. At 100k bps, the receiver has a bit error rate of 10^{-9} .

Analyzing the link's performance

The fiber optic's performance should be evaluated by calculating first a flux budget and then a rise time budget. The fiber optic link is not immune to flux loss, which occurs in two ways: fiber attenuation and connector loss. Fiber attenuation is power loss due to material properties, impurities, or mechanical imperfections within the fiber. This loss varies with wavelength. For this calculation, the link uses Siecor Twin S-155 Super Fat FiberTM cable. This cable contains two all-glass fibers, each having core diameters of 200 μ m. Fig 4(a) shows the attenuation due to wavelength, while Fig 4(b)

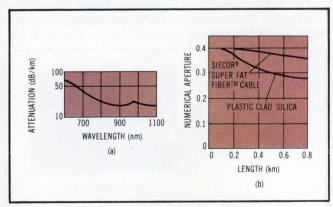


Fig 4 Attenuation of optical fiber accounts for greatest decibel loss to network. Loss associated with wavelength of emitting diode is shown in (a). Loss due to length of cable is shown in (b).

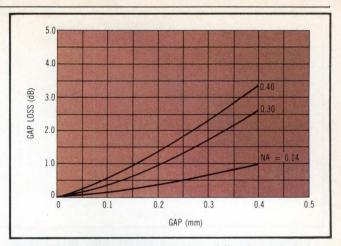


Fig 5 Gap loss increases as function of fiber's NA and size of gap. By holding gap to 0.05 mm, energy loss from LED to fiber is only 0.30 dB.

shows the cable's numerical aperture at different lengths.

Connector losses occur in a variety of ways throughout the link: numerical aperture (NA) loss, gap loss, axial misalignment loss, Fresnel loss, and angular loss.

NA loss. Although a calculated NA suggests a sharp cutoff of emission or acceptance angle for a fiber optic element, a measured plot of the emission or acceptance pattern usually results in a bell curve. This analysis defines the NA relative to the point at which the emission or acceptance is down 10 dB. If a source of optical power has a larger NA than that of the element receiving the power, some of the energy will be lost. The magnitude of this loss is given by

NA loss = 20 log (NA1/NA2)

In the case of coupling from a lower NA source into a larger NA fiber, the equation goes to zero.

Gap loss. Ideally, the optical source (the LED) and the fiber are joined so that no gap exists between them. In practice, however, a small gap is intentionally maintained to prevent mechanical damage to the glass surfaces. Motorola's devices, together with AMP and Amphenol connectors, are designed to hold this gap to 0.05 mm (Fig 5).

Axial misalignment loss. If the core area of the receiving fiber is not concentrically aligned to the projected beam, a loss of coupled power occurs. As might be expected, the magnitude of loss varies with both the fiber's diameter and the NA (Fig 6). In the case of coupling to fibers with core diameters either much larger or much smaller than the emitting device, the axial misalignment loss is insignificant.

Angular loss. Angular loss occurs if the surfaces of the source and the receiving fiber are not parallel. Angular loss increases with the fiber's NA (Fig 7).

Fresnel loss. Whenever light passes through an interface, a portion of the total energy passes through, and the remainder is lost by reflection and scattering. This is Fresnel loss. The magnitude of the loss depends on the refraction index of the materials forming the interface and the quality of the surface polish. For a high quality polished fiber to air interface, the Fresnel loss is a fairly consistent 0.1 to 0.2 dB/interface. Index matching fluids can reduce this loss, but the improvement is usually not worth the extra trouble.

Summary of Losses in a Typical Fiber Optic System				
Loss Parameter	Loss (dB)	Cumulative Loss (dB)		
LED-fiber gap loss	0.30	0.30		
LED-fiber misalignment loss	0.50	0.80		
LED-fiber angular loss	0.40	1.20		
Fiber input Fresnel loss	0.20	1.40		
Fiber attenuation	17.50	18.90		
Fiber exit Fresnel loss	0.20	19.10		
Fiber-determined gap loss	0.30	19.40		
Fiber-determined misalignment loss	0.50	19.90		
Fiber-determined angular loss	0.40	20.30		
Total link loss		20.30		

Formulating the microcomputer link flux budget. Once the elements of loss are defined, it is possible to formulate an accurate flux budget analysis for a single terminal to terminal fiber optic link 500 m in length. The calculation assumes the following mechanical parameters for each connection (LED to fiber, fiber to detector):

Gap = 0.05 mmAngular deviation = 1.0° Misalignment = 0.05 mm

The coupling loss incurred because of these factors is determined by consulting the loss graphs (Figs 5 to 7).

Gap loss = 0.30 dBAngular loss = 0.40 dBMisalignment loss = 0.50 dB

A further Fresnel loss occurs at the input fiber surface, which is assumed to be 0.20 dB.

According to its data sheet, the LED has a - 10 dB NA of 0.30, and the Siecor fiber has an NA of 0.40. Because the source has a smaller numerical aperture, no loss will result from the NA mismatch. At the detector end of the fiber optic link, there are again losses due to gap, misalignment, angular deviation, and Fresnel loss. The p-i-n diode has an acceptance -10 dB NA of 0.50. Again, because the source element—in this case the fiber (NA = 0.40)—has the smaller NA, there is no loss due to NA mismatch.

Fiber attenuation is the final system loss to be included. The LED emits at a peak wavelength of 812 nm. The attenuation curve for the Siecor fiber

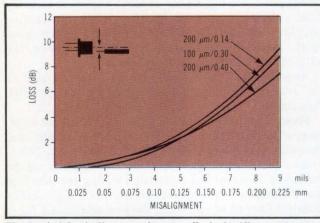


Fig 6 Axial misalignment is generally insignificant when optical fiber's core is much greater, or much smaller, than emitting device.

[Fig 4(a)] shows that at this wavelength the fiber has about 35-dB/km loss. Since the link is to be 500 m long, 17.5-dB cable attenuation results. The total energy loss is shown in the Table, "Summary of Losses in a Typical Fiber Optic System." Gap, misalignment, Fresnel, and angular losses must be doubled as a result of the fiber's connection to the receiver at one end and to the transmitter at the other. However, the flux budget is not complete until the LED power use is determined. The minimum optical

power required by the detector in a 5-V receiver is 0.75 μ W. This sustains a data rate of 62.5k bps. Converting this to dBm results in

 $P_{min} = 10 \log_{10} (0.00075 \text{ mW}/1 \text{ mW})$ = -31.2 dBm

By adding the total link loss to the minimum required detector signal, the necessary LED output is determined

$$P_o = -31.2 + 20.3 = -10.9 \text{ dBm or } 81 \,\mu\text{W}$$

This, however, leaves the link without a built-in safety factor. If the assumptions about connector gaps are off and if the LED degrades over time or is affected by temperature, the link is somewhat marginal at 81 μ W. To protect the link, a degree of margin—typically 3 to 5 dB—should be added to the budget. If 5 dB are added to the LED output (-10.9 + 5), the required source power is -5.9 dBm or 257 μ W. According to its data sheet, the MFOE1200 LED requires a current of 20 mA to reach the required 257 μ W.

Calculating the rise time budget. The network rise time—the time required for a pulse to reach maximum amplitude—is defined as the square root of the sum of the squares of the rise times of the link's components:

$$(t_r^2 \text{ system})^{\frac{1}{2}} = (t_r^2 \text{ LED} + t_r^2 \text{ fiber} + t_r^2 \text{ det})^{\frac{1}{2}}$$

This could be broken down further to the components within the transmitter and the receiver, but that would be unnecessary for the link's relatively slow data rate. This analysis assumes that a 62.5k-bps network must exhibit a rise time (10% to 90%) of about 5.6 μ s (t_r = 0.35/bandwidth) to effectively discern 1s and 0s.

The Siecor fiber has a length/bandwidth product of 5 MHz/km. This equates to a fiber rise time of 70 ns/km. Since our link is 500 m long, the fiber rise time is 35 ns.

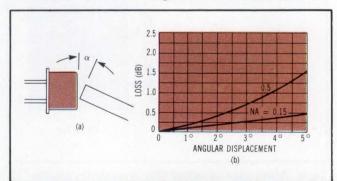


Fig 7 When fiber is not parallel to its emitting source or its receiver (a), some power loss occurs. Loss depends on angle of junction (b).

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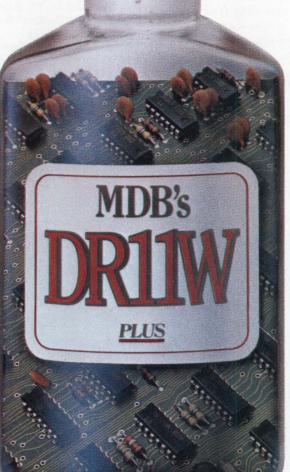
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FOR LSI-11 CIRCLE 38



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This is insignificant in comparison to the 5.6 μ s total system rise time and can therefore be ignored.

Thus, using this calculation, the network's rise time is limited by its electronics. In particular, the limiting rise time comes from the amplifier components in the transmitter and the receiver. The LED has a rise time of about 8 ns, and the p-i-n diode has a rise time of about 1 ns.

Extending the length of the system

The link between the terminals described above is only 500 m. It would be helpful to know what the maximum length of this network can be using the same components and cable. Since the maximum continuous current rating for the MFOE1200 is 100 mA, an assumed duty cycle of 50%—depending on the coding scheme used—would operate at a peak current of about 200 mA. The MFOE1200 power output at that current is 1500 μ W or 1.76 dBm. The total link loss, excluding fiber attenuation, is 2.8 dB. Adding a 5-dB power margin and subtracting the total from the minimum power required at the detector, the equation yields

 $-31.2 + (2.8 + 5.0) = -23.4 \, \text{dBm}$

Subtracting the power output of the LED and dividing by the loss of the fiber (35 dB/km), the maximum network length is determined

 $(-23.4 - 1.76) \, dB/35 \, dB/km = 719 \, m$

If this is still below the desired length, the link can employ a higher power LED, such as the MFOE1202, yielding a maximum system length of 787 m. Another option for extending a network's length is to use a lower loss fiber. If a different fiber is used, the various connector losses—gap, misalignment, angle must be recalculated.

It is clear from the foregoing example that a functional fiber optic network can be built at a reasonable cost. With fiber optic technology in place, falling component costs can only add impetus to the use of fiber optic techniques in tomorrow's networks. In light of this, the future of fiber optic network applications seems bright indeed.

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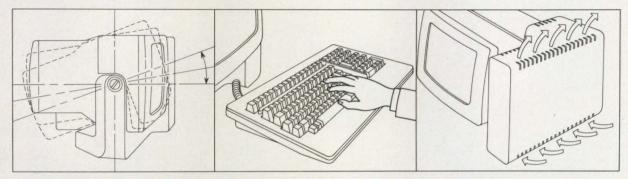
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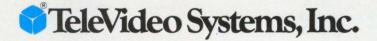
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CIRCLE 41



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QUALITY LIVES CIRCLE 42

COMPUTER DESIGN

SPECIAL REPORT ON DISK AND TAPE MEMORY SYSTEMS

When early mass storage systems were developed, few people could foresee the dense data storage requirements that exist today. In the days of batch processing with punched cards, it would have taken a small army of keypunch operators to prepare the records to fill, say, only a megabyte of storage. Also, of course, early disk and drum systems were extremely expensive. Therefore, computer systems emphasized processor-intensive rather than memory-intensive operations.

Today, a few thousand dollars can buy a powerful desktop computer system with over a megabyte of removable floppy disk storage. Several thousand dollars more buys a Winchester drive with maybe a hundred megabytes of storage. And large mainframe systems can work with gigabytes of stored data.

People who predicted that semiconductor technology would displace magnetic storage techniques have, so far, proved wrong. Instead, semiconductor developments have pushed memory technology onward and upward. Microprocessors created a need for fast random access memory that was filled by semiconductors. This, in turn, created a need for high density removable storage filled by relatively inexpensive floppy disks. The pressure then was on manufacturers of fixed media mass storage systems—such as those using hard disk or optical techniques—to lower their costs and remain competitive.

All this progress has left a few technological casualties along the way. Charge coupled devices, of course, were run over by the semiconductor RAM bandwagon, which was propelled by the competitive bit densities, lower cost, and faster access of RAMs. Magnetic bubble devices found themselves squeezed by simultaneous progress in semiconductor RAMs and floppy disks. As a result, today's bubble technology has been relegated largely to portable and ruggedized applications. Magnetic tape, because of slow random access, now tends to be used for backup rather than for primary storage. Even this backup role for tape may be threatened by such developments as low cost removable disk cartridges for Winchester systems. Optical storage, though not a casualty of the dramatic progress of magnetic storage, has been forced to wait in the wings while it gets its act together. However, thanks partly to accelerated research into optical techniques for video recording, optical storage may soon be ready to play its destined role of providing extremely high density storage for archival files.

More dramatic improvements—such as vertical recording for disks—are just around the corner. But the booming market growth that supported the research may be slowed by a lack of industry standards. Or—possibly worse—progress may be halted by hastily drawn standards that fail to meet the real needs of system designers.

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CIRCLE 43

Special report on disk and tape memory systems

89 Winchester disk technology spins into new orbits by Michael Elphick and Richard Parker—To meet an insatiable demand for more data storage in smaller systems, designers of hard disk systems continue to find better ways to cram in the bits.

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SPECIAL REPORT ON DISK AND TAPE MEMORY SYSTEMS

WINCHESTER DISK TECHNOLOGY SPINS INTO NEW ORBITS

To meet an insatiable demand for more data storage in smaller systems, designers of hard disk systems continue to find better ways to cram in the bits.

by Michael Elphick, Executive Editor and Richard Parker, Contributing Editor

f all mass storage technologies, Winchester magnetic disk drives enjoy the greatest performance advances. As testimony to the ongoing dynamic activity in Winchester technology, witness the number of companies in the field and the multitude of Winchester disk drive shapes and sizes on the market. Putting more and more storage capacity onto the same, if not smaller sized disks, leads to lower cost per megabyte of stored data. Winchester disk drive storage capacities have been soaring into the gigabyte range on larger 14" types.

It began in 1973 with the 14" Winchester disk drive from IBM Corp (the 3-platter 70M-byte model 3340). Now modern 14" Winchester disk drives can provide up to 5G bytes of storage capacity. Within the 14" club, Winchester disk drives range in storage capacity from 5M bytes to 5G bytes, with a large number aimed at the 200M-byte to 1.5G-byte range. Even smaller 8" Winchesters are moving upward in storage capacities, ranging from 5M to 200M bytes. And the hottest action is in $5\frac{1}{4}$ " mini Winchesters that sport storage capacities of 2M to almost 150M bytes.

Smartness is in with Winchester disk drives, thanks to microprocessors. Spurred by the need for better interfaces and more self-diagnostics, an increasing number of Winchester disk drive manufacturers are building microprocessors in their products. The more intelligent systems make drive interfacing simpler and easier. And given the large number of Winchester disk drive shapes and sizes, all with different mechanical and electrical parameters, such intelligent interfacing is welcome news.

The same driving forces pushing advances in other mass storage technologies are stimulating progress in Winchester disk drive technology. They include a prolif-

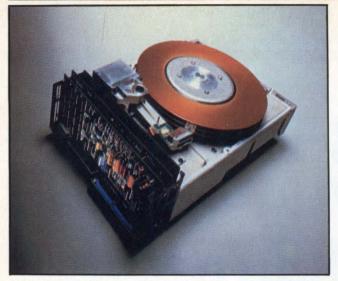


A 31.2M-byte Winchester system, the DSD890 from Data Systems Design, includes a quarter-inch tape backup. The DEC-compatible system replaces more expensive equipment that uses half-inch tape for backup. Its Winchester drive can replace a system that uses three cartridge disks.

eration of distributed processing; the spread of desktop, small business, and personal computers; the increased intelligence of computer terminals; and the general flow of computer technology out from the domain of the specialists and into the hands of average people (eg, businesspeople, professionals, students, academicians, and consumers).

High capacity progression

One look at the XT-1105 5¹/₄ " mini Winchester disk drive from Maxtor Corp (Santa Clara, Calif), with a gigantic storage capacity of 105M bytes (unformatted data), shows how far Winchester disk drive storage capacities



Using a voice-coil servo rotary actuator, compact hard disk drives in the 8500 series from 3M provide a storage capacity of 60M bytes and a random average seek time of 29 ms. The package is the same size as a standard 8" floppy disk drive.

have increased. The drive employs 12 recording surfaces and has a 35-ms average access time. It transfers data at 625k bps. The XT-1105 uses a rotary voice-coil actuator and is compatible with Seagate Technology's (Scotts Valley, Calif) ST506.

Micropolis Corp (Chatsworth, Calif) offers up to 200M bytes of unformatted data storage capacities in its 8" American National Standards Institute (ANSI) Winchester disk drives. The drives feature a 28-ms average access time, a 1.248M-bps data transfer rate, and ANSI X3T9.3 compatibility. Voice-coil actuators are utilized for read/write head positioning.

For truly huge storage capacities, one can step up to the model B-4 14" Winchester disk drive from IBIS Systems Inc (Duarte, Calif). The drive can store up to 2818M bytes of unformatted data by using 32 recording surfaces. It has a linear voice-coil actuator for read/ write head positioning and a 16-ms average access time. The data transfer rate is 3M bps. One reason why the drive can store so much data is its thin-film disk.

Manufacturers of 14" Winchester disk drives are not only increasing storage capacities, but they are also reducing their drives' physical dimensions. The Advanced Marksman Series model 315 from Century Data Systems (Anaheim, Calif), for example, can store 315M bytes of data in one-third the drive size of others with similar storage capacities.

One potential problem with higher capacity Winchester disk drives of all sizes is that the standard Seagate Technology data transfer rate of 5M bps may no longer suffice for many disk controllers. Experts are looking at future data transfer rates of 10M bps to as high as 30M bps. Higher data transfer rate requirements will mean a redesign of existing disk controller circuits. Already, Winchester disk drives from Rotating Memory Systems, Inc (Milpitas, Calif) and Evotek Corp (Fremont, Calif), employing run-length limited (RLL) encoding schemes, have 7.5M-bps data transfer rates. Interphase Corp (Dallas, Tex), a manufacturer of intelligent and high speed controllers, is evaluating a Fujitsu 10.5" Winchester drive, operating with a controller that transfers data at 20M bps.

Thin film leading the way

A major effort is under way in the disk drive industry to implement thin-film read/write heads and thin-film media for increased storage bit densities. Plated thinfilm media offer durability advantages over conventional oxide-coated media, besides higher recording densities. For example, the thin-film media can better withstand damage due to read/write head and media contact, a common problem known as head crashing. The thin-film disk resists gouging of the magnetic particles on the disk's surface, and is less prone to wedging, whereby the magnetic material becomes thicker on the outside, a major problem with standard oxide coatings.

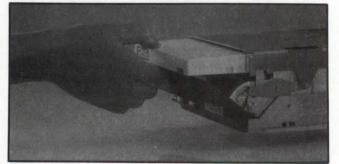
Furthermore, unlike oxide-coated media, which require a protective lubricating film, the thin-film media with its metallic finish can simply be wiped clean with a fluorocarbon solvent if inadvertently touched during the manufacturing process—leading to lower manufacturing costs. With thin-film coatings, tighter track densities are possible on the disk's surface because plated media have more uniform magnetic characteristics.

On conventional oxide-coated media, one can typically obtain about 8000 magnetic flux reversals per inch (fr/in), a figure that jumps to 12,000 fr/in with plated thin-film media. Using thin-film read/write heads can further increase this figure.

One reason why Vertex Peripherals Inc (San Jose, Calif) can offer storage capacities of 72.3M bytes of unformatted data in a $5\frac{1}{4}$ " mini Winchester disk drive is the drive's thin-film media. The v170 drive employs conventional manganese-zinc-ferrite read/write heads. Vertex also uses thin-film media on its smaller capacity 31M-byte v130 and 51.7M-byte v150 $5\frac{1}{4}$ " mini Winchester disk drives.

Another firm using thin-film media on its $5\frac{1}{4}$ "Winchester disk drives is Evotek Corp. The company offers it on its ET-5000 line of drives that span storage capacities of 7.81M bytes to 51.6M bytes (unformatted data). The drives have 49-ms average access times and are available in 5M-bps and 8.2M-bps data transfer rate versions.

As for thin-film read/write heads, IBM Corp (San Jose, Calif) was the first to use them on its series 3300 14" Winchester disk drives. Now Memorex (Santa Clara, Calif) has introduced thin-film read/write heads on its models 3690 and 3689 14" Winchester disk drives that also use special thick-substrate particulate media for increased storage densities. The Memorex drives are plug compatible with the IBM 3370 and 3380 drives.



New 5¹/₄" fixed/removable disk drives from DMA Systems provide higher storage capacities than earlier versions in the Micro Magnum family. Total unformatted storage capacities are 19.5M bytes and 26M bytes, respectively, for models 5/10 and 5/15. Of the total capacity, 6.5M bytes are on the removable cartridge for each drive version.

A thick particulate media on the Memorex drives was needed to make the disk's surface less prone to vibration and wobbling, since the thin-film read/write head flies much closer to the disk's surface than a conventional ferrite read/write head would. The thin-film read/write head flies just 10 μ in above the disk's surface.

Thin-film read/write heads provide higher storage capacities than conventional ferrite read/write heads. This capacity increase results from the much smaller size of the former, which allows the drive system to write much smaller flux reversals per inch of disk surface. For a 14" Winchester disk drive, a thin-film read/write head can typically have about one-half the head-gap length and about one-half the head-gap width of a conventional ferrite read/write head. Such factors, along with the thin-film head's smaller dimensions (about one-fifth the volume of a ferrite read/write head) and lighter weight (less than one-twentieth of a ferrite head's weight) allow a thin-film read/write head to fly at half the distance from a disk's surface, as compared to a ferrite head.

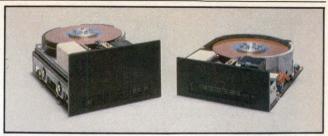
Conventional ferrite read/write heads can provide maximum storage and track densities of approximately 9000 bps and 480 tpi, respectively. Compare that with the 15,000-bpi bit densities and 480-tpi track densities that thin-film read/write heads can attain.

Experts predict that, together with plated thin-film media, thin-film read/write heads will provide storage densities on the order of 50M bits/in² by the mid-1980s, and 100M bits/in² by the end of this decade. Such media/head combinations will make possible Win-chester disk drives with 3000 tpi and 20M bpi. According to industry experts, the future of magnetic disk technology will be largely driven by thin-film read/write heads.

Despite all this, few Winchester disk drive manufacturers are using thin-film read/write heads on their products, primarily due to the higher cost and lack of multiple sourcing of heads. Many Winchester disk drive manufacturers argue that it is foolish to jump headlong into an advanced storage technology that will cost quite a bit more, because a gap between such a high-end technology and what is already available on the market may be filled at a lower cost. Nevertheless, some firms like Seagate Technology have applied thin-film read/write heads on smaller Winchester disk drives like their ST506, a 5¼" mini Winchester with 38M-byte (unformatted



A half-height 5¼" Winchester from Seagate Technology is the first of its class to use thin-film media for added durability. The ST206 (left) is compared with a Seagate standard-height unit. Both drives store 6.38M bytes of unformatted data. The ST206 has an 85-ms average access time and is fully compatible with the widely accepted ST506 interface standard.



Both standard- and half-height 5¹/₄" Winchesters are offered by MiniScribe. Standard-size versions have storage capacities from 6.4M bytes to 20M bytes, while the half-height versions store 6.4M bytes or 12.8M bytes. Average access times range from 85 ms to 120 ms.

data) storage capacity. The drive features a 540-tpi track density and a 10,202-bpi linear density. Still, Seagate Technology has stopped using thin-film read/write heads on its 12M-byte Winchester disk drive—instead, the 12M-byte ST412 uses conventional manganese-zincferrite read/write heads.

Apparently, the key to widespread use of thin-film read/write heads lies in lower unit costs, which mean higher manufacturing yields. Lower costs are attainable because thin-film heads can be made photolithographically, much like semiconductor integrated circuits. Memorex reports that it can fabricate 700 thinfilm read/write heads on a 3" diameter wafer and that, on a pilot production basis, 400 such heads are functional.

Two paths to head positioning

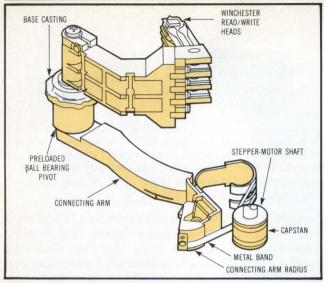
With so many form factor and storage capacity similarities among Winchester disk drives, it is difficult if not impossible to differentiate between them. One area, however, where some drives stand above the others is in head positioning method. In this area at least, Winchester disk drive manufacturers are trying to outdo one another.

There is intense activity in more advanced read/write head positioning developments for Winchester disk drives, particularly for the smaller mini and micro (under $5\frac{1}{4}$ ") drives. Closed loop and open loop control are the two main head positioning methods.

With closed loop control, the read/write head senses its location on the disk from reference data stored on the disk's surface. Reference data are then fed to an actuator that more precisely positions the read/write head on the right disk track.

In an open loop system, the read/write head has no reference data to guide it. Instead, it relies on the actuator mechanism's mechanical accuracy to find the right track. Either a rotary voice-coil actuator mechanism or, more commonly, a stepper-motor mechanism positions the read/write head on the proper track. A voice coil allows continuous read/write head movement, leading to increased positioning accuracy and higher track densities. But it is also more expensive than a stepper-motor actuator.

Because of its operational simplicity, an open loop control system offers less expensive and usually more reliable operation than a closed loop control system, which has many more components. A single stepper motor, motor controller, amplifier, and a radial armature (to connect the stepper motor to the read/write head) often suffice for an open loop control system.

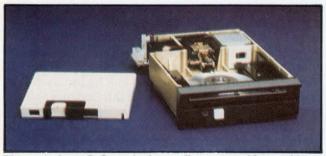


With this split-band capstan head positioner, Computer Memories solves the shock and vibration problems that affect open loop disk drive systems. The positioner assembly is used in the firm's CM5000 series of $5\frac{1}{4}$ "Winchester drives. The read/write head assembly is at the end of an arm that pivots around a setpoint, allowing the assembly to more easily absorb shock without moving the head.

On the other hand, an open loop system's positioning accuracy is limited to the accuracy of the stepper motor and to the precision of the mechanical radial armature. Furthermore, open loop systems are prone to vibration and thermal-expansion effects, which lessen their accuracy. Overcoming differences in thermal-expansion characteristics between various drive components is difficult. For example, a steel head-flexure mechanism and the aluminum disk with which it interfaces have different first order thermal-expansion coefficients, thus restricting track densities and storage capacities.

Additional problems can result from stepper-motor hysteresis, drive spindle run-out, and stepper-motor settling time. Because of these factors, open loop control systems are usually found in lower capacity Winchester disk drives—namely those drives with track densities of 200 to 300 tpi.

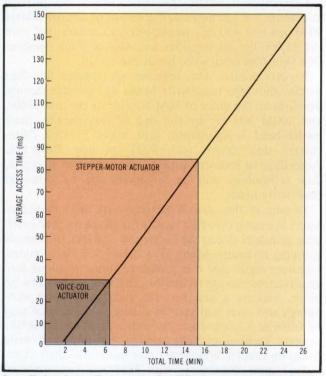
One firm, Computer Memories (Chatsworth, Calif), has solved shock and vibration problems in an open loop system by using a split-band capstan head positioner in its CM5000 series of $5\frac{1}{4}$ " mini Winchester disk drives. The read/write head assembly is placed at the end of a rotary arm that pivots around a setpoint, allowing the head positioning assembly to more easily absorb



The SQ306 from SyQuest is the smallest removable-cartridge Winchester drive available. Fitting the standard half-height 5¹/₄" space requirements, the unit has a 3.9" platter in its removable pack and provides 6.38M bytes of unformatted data storage.

lateral shock without translating any movement to the read/write head. The CM5000 Winchester disk drives span storage capacities of 6.4M to 19.1M bytes (unformatted data), with 72-ms average access times, and a 625k-bps data transfer rate. A closed loop version (the CM5640) has 40M-byte (unformatted data) storage capacity, 40-ms average access time, and a 625k-bps data transfer rate. This drive employs an optical sensor in the closed loop servo arrangement.

Voice-coil actuated drive systems provide faster average access times than stepper-motor designs, though not all disk drive experts agree on the relative importance of this. With voice-coil actuated mechanisms, a host of Winchester disk drives now have average access times under 30 to 40 ms. Though some experts claim that average disk access time with a voice-coil actuator is not that much faster than one with a stepper-motor actuator, the difference in speed becomes more noticeable if several tracks of data were moved instead of one or two. In addition, the kind of host computer operating system and the number of workstations sharing a disk drive



So-called voice-coil actuators for Winchester recording heads are much faster than conventional stepper motors, as shown in data prepared by Vertex. The graph compares the two techniques in terms of average access time and the total time to perform 10,000 random seeks while transferring one 256-byte sector per seek.

may require the higher performance provided by a voice-coil actuator. Operating systems like UNIX, for example, require efficient rapid access times.

For the most accurate head positioning, closed loop systems are the answer. Because of their better positioning accuracies compared to open loop systems, they offer higher track densities. Closed loop systems, also known as servo systems, are most often found in Winchester disk drives with high track densities of up to 600 tpi. Though there are many variations of closed loop systems, the dedicated and the embedded servo systems are the two main approaches.

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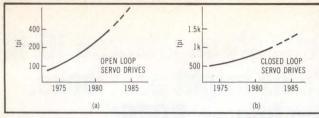
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Track densities for both open loop and closed loop servo disk drives are increasing. The latter type of control system can provide higher track densities (b) than open loop types (a) since it provides greater read/write head positioning accuracy. Source: Seagate Technology.

In the dedicated type, one surface of the disk is reserved for reference information. A servo head that flies over that surface senses this information. The servo head is physically attached to the disk's read/write head, which senses track data on the other side of the disk. Although a dedicated closed loop servo system offers higher tracking accuracy than an open loop system, reserving an entire disk surface for reference information seriously limits the disk drive's storage capacity. Furthermore, environmental and mechanical stresses can cause erroneous read/write head tracking. For example, the servo head may be exactly on track, but the physically attached read/write head can be off track very slightly due to misalignments between both heads.

Embedded closed loop servo systems eliminate these mechanical and environmental stress problems. Here, reference data are stored on the same disk track that holds the stored data. Now both sides of the disk can be used for data storage, increasing the disk drive's storage capacity. System operating speed is the tradeoff. Since the read/write head must now do double duty by reading and writing stored data, as well as reading reference information, disk drive throughput is compromised.

Despite this drawback, many disk drive experts foresee the embedded servo approach as promising future high capacity and high density Winchester disk drives. They are certainly more accurate than dedicated servo systems. As $5\frac{1}{4}$ " and sub $5\frac{1}{4}$ " Winchester disk drives gain storage capacity, requirements for more accurate track positioning for the read/write heads will increase. The embedded closed loop servo approach appears to be one feasible alternative that carefully balances storage space requirements with system access time.



Compact $5\frac{1}{4}$ " Winchester disk drives from Atasi offer up to 46M bytes of storage capacity. Another advantage of the Series 3000 units is a 30-ms access time, which rivals the speed of larger 8" and 14" drives.



The Irwin 516 subsystem includes a 16M-byte Winchester drive and cartridge tape backup. Fitting a standard $5\frac{1}{4}$ " configuration, the unit claims high storage capacity on a single platter. Average access time is under 35 ms including move and settling times.

Converter increases accuracy

One development from Evotek Corp in closed loop Winchester disk control promises to double and possibly triple $5\frac{1}{4}$ " mini Winchester disk drive storage capacity. The firm has developed a microprocessor controlled servo tracking system that uses an analog to digital converter (ADC) to position the disk's read/write head, instead of the usual comparator circuit.

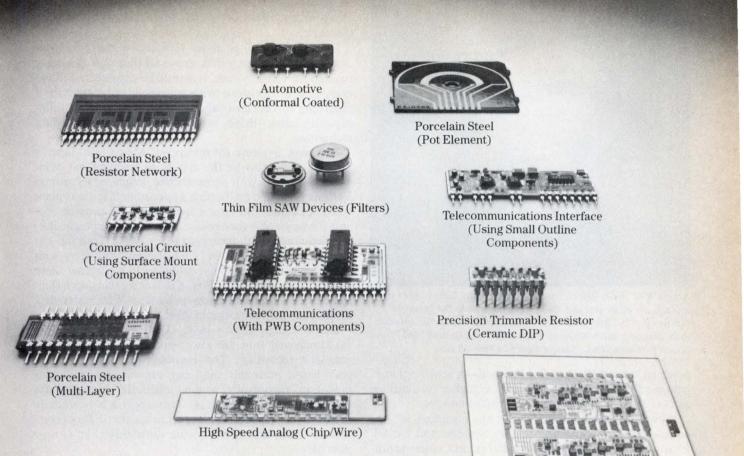
Based on a 6800 microprocessor, the system uses a Signetics NE5037 6-bit ADC to account for soft errors in the tracking mechanism. A much tighter tracking control than is possible with a comparator circuit results, although the converter approach costs slightly more. One benefit of the converter approach is that it is faster than a comparator circuit, thereby contributing to faster disk system access time.

With the new servo system, tracks can be placed closer together on the disk's surface. Thus, Evotek claims that $5\frac{1}{4}$ " Winchester disk drives with 600 tpi are possible—or nearly double the current track density of 375 tpi on the firm's 51.6M-byte ET5840 $5\frac{1}{4}$ " mini Winchester disk drive, a product with thin-film media and a 5-phase stepper motor. Such high track densities could translate into $5\frac{1}{4}$ " Winchester disk drives that can store up to 150M bytes, or roughly triple what is now available from the firm.

The ADC digitizes voltage changes in a particular data track as the read/write head is placed on the track. These changes occur as the head moves from the track's center to either side of the center. The voltage is the highest at the center and drops off in a bell-shaped curve on either side; voltage levels vary from 1 mV to 10 mV, depending on the sensitivity of the read/write head. The position of the read/write head on the track is almost linearly related to the voltage amplitude. Once the error voltages are digitized, the microprocessor, which provides closed loop control, controls the signals.

Denser encoding methods abound

Many Winchester disk drive experts believe that more efficient encoding schemes are needed for a dramatic increase in disk drive storage capacity. One common disk drive encoding technique is the modified frequency



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A new $5\frac{1}{4}$ " Winchester from Maxtor packs 140M bytes of storage on eight stacked disks. The xT-1140 is the latest in a family of $5\frac{1}{4}$ " drives that have the motor inside the spindle, thus allowing more disks to be stacked within standard physical dimensions. Access time is a low 30 ms.

modulation (MFM) encoding method—a scheme that is being examined for improvements as higher bit densities in ever smaller Winchester disk drives emerge.

A more recent approach is the RLL encoding scheme as practiced by Rotating Memory Systems and Evotek Corp on their Winchester disk drives. RLL codes promise to boost Winchester disk drive storage capacities by 50%, given the same physical drive hardware and read/ write heads. With RLL codes, larger amounts of data are represented on the disk's surface for the same number of flux reversals than with an MFM code.

Unlike MFM encoding, which requires a one to one data storage overhead, RLL codes require a smaller overhead and are therefore more efficient. That is, an MFM code for one bit of data actually consists of two bits, one for the data, and one for clocking information. Thus, four data bits would be represented by eight MFM bits. With an RLL encoding scheme, on the other hand, the four data bits can be represented by just five bits.

The tradeoff is that the RLL code requires precise synchronization and more sophisticated error correction and detection circuitry than used in MFM encoded systems. In an RLL encoded system, even a 1-bit shift in the decode frame due to synchronization offsets can cause massive system errors. Furthermore, much higher clock rates than the typical 20-MHz clock rate for disk drives are required—on the order of 400 MHz.

Perpendicular recording-a promising technique

Since 1975, perpendicular-magnetic-recording research has been going on at Tohoku University in Japan. The results of that research promise a dramatic increase in Winchester disk drive storage densities and capacities. Capacity increases of 50 to 100 times are being routinely predicted for perpendicular magnetic recording.

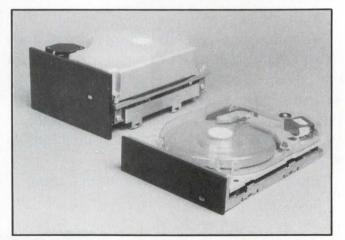
Moreover, the level of research has reached the point where linear recording densities of at least 200k bpi (400k bpi unofficially), track densities of 12.5k bpi, and storage densities of 12.5G bits/in² have been reported. Experts predict that with perpendicular magnetic recording, 3M to 5M bytes of data can be stored in a microfloppy disk drive as small as $3\frac{1}{2}$ " (platter diameter).

Indeed, research is under way in a number of locations, and Winchester disk drives of that type are being readied for introduction. It should be emphasized, however, that a disk drive with a perpendicular-magneticrecording surface costs about twice as much as a similar capacity disk drive with conventional recording techniques.

Vertimag Systems (Minneapolis, Minn) and Japan's Toshiba appear to be the closest to bringing out Winchester products with perpendicular magnetic recording. Vertimag, funded by Sweden's telecommunications giant L. M. Ericsson, has announced that it will provide 5M-and 10M-byte Winchester disk drives with perpendicular-magnetic-recording technology in 1983. Toshiba has already announced a $3\frac{1}{2}$ " microfloppy disk drive with 3M-byte storage capacity using such recording. And Ampex Corp (Redwood City, Calif) is working on a thin-film process that will allow prototype Winchester disk drives with perpendicular magnetic recording by 1984.

Lanx Corp (San Jose, Calif) and France's CII-Honeywell Bull are also researching perpendicular magnetic recording. The French firm is working on glass-based materials that can support perpendicular magnetic recording, where magnetic particles are embedded within the glass. This approach reportedly offers higher track densities, more magnetic flux reversals per inch, and better media durability than is now possible.

With conventional longitudinal recording techniques used on oxide-coated and plated thin-film media, the recorded magnetic fields resemble an array of bar magnets lying end to end. With no change in the binary data being recorded on the disk drive, no transitions occur between the magnetic fields and no signals are generated in the read/write heads that effectively rotate above the fields. (Actually, of course, the disk itself rotates beneath the read/write heads.) When a change occurs in the binary data, the poles of the magnetic field are reversed horizontally, creating a flux transition that is picked up by the read/write heads. The resultant output voltages are generated at the heads. The sharper the



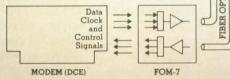
System designers can place two $5\frac{1}{4}$ " hard disk drives in the space of one by using half-height units, as shown in this comparison from Shugart Associates. The SA706 has a single platter and stores 6.67M bytes (unformatted), while the SA712 stores 133M bytes on two disks.

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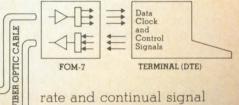
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With perpendicular magnetic recording, the poles of the magnetic field are stood on end and arranged like bars in a row. When no magnetic field transition occurs, data are clocked off the disk drive. Transitions that do occur provide for sharper and narrower voltage pulses at the read/write heads. Much higher recording densities result.

Backing up with cartridges

Backing up a Winchester to preserve the data in case of system failure is one of the most widely discussed issues in disk drives. And, as Winchester disk drive designs proliferate, backup becomes increasingly important. Backup candidates include floppy disk drives, reel-toreel tape, streaming tape drives, and even Winchester disk drives themselves (in the form of removable cartridges).

A host of 5¼" and 8" mini Winchester removable disk cartridges are offered by DMA Systems (Goleta, Calif), Seagate Technology, Western Dynex Corp (Phoenix, Ariz), Dicom Industries (Sunnyvale, Calif), New World Computer Co (Irvine, Calif), Cynthia Peripheral Corp (Palo Alto, Calif), Advanced Electronics Design, Inc (Sunnyvale, Calif), and Data Peripherals (Milpitas, Calif). Even larger 14" removable Winchester disk cartridges are offered by Control Data Corp (Minneapolis, Minn), Ampex Corp, Ball Computer Products Inc (Sunnyvale, Calif), Vermont Research Corp (N Springfield, Ver), IBM Corp, Data General Corp (Westboro, Mass), Wang Laboratories Inc (Lowell, Mass), and Western Dynex Corp.

SyQuest Technology (Fremont, Calif) offers the smallest removable Winchester disk cartridge in its half-height SQ306R, a 3.9" platter removable pack with 6.38M-byte storage capacity (unformatted data) arranged in 8192 bytes/track, 32 sectors/track, and 256 bytes/ sector. The Seagate compatible drive is a tiny 8" x 4.8" x 1.625" that can transfer 5M bps (the cartridge itself has dimensions of just 4.41" x 4.33" x 0.43").

First to exploit the idea of removable Winchester 5¹/₄" cartridges was the New World Computer Co in 1981



Interphase Corp, a manufacturer of bus-compatible controller boards, also sells complete Winchester disk systems. The subsystem shown includes an 8" Winchester drive, plus a power supply and fan. Various drive types and storage capacities are available.



Half-height $5\frac{1}{4}$ " drives from Disctron store 25.5M bytes (model 620) or 42.5M bytes (model 640). Both versions have a 40-ms average access time. Head positioning employs voicecoil and closed loop servo technology.

with a drive that offered both fixed and removable storage. Model 2/2 with one fixed and one removable recording surface, each of which stored 2M bytes of unformatted data, was an interim step to the allcartridge removable Winchester disk drive. New World Computer later added model 4/2 with 4M bytes of fixed and 2M bytes of removable storage capacity for unformatted data (two fixed and one removable surface), and model 4/4 with 4M bytes of fixed and 4M bytes of removable storage capacity for unformatted data (two fixed and two removable recording surfaces). In the company's design, the cartridge contains the recording platter, the read/write head, and the control arm.

However, the first to offer a truly removable 5¹/₄" Winchester cartridge media in which only the media were removable (not the read/write head and control arm) was DMA Systems. Micro Magnum 5 has a 6.75M-byte storage capacity (unformatted data) in a removable cartridge, with a 40-ms average access time and a 5M-bps data transfer rate. Its companion Micro Magnum 5/5 employs an extra fixed platter with an additional 6.75M bytes of storage capacity (unformatted data). Recently, the company introduced versions of the Micro Magnum with higher storage capacities.

Others, like Century Data Systems, followed with even higher capacity fixed/removable Winchester disk drives with cartridges. The firm's C8048 is an 8" Winchester disk drive with three fixed recording surfaces that can store 33.45M bytes of unformatted data, and one removable surface in a cartridge capable of storing 16.73M bytes of unformatted data.

Using Winchester removable cartridges to back up other fixed Winchester disk drives is gaining favor. This is because the technique simplifies the system integrator's job. Instead of having both primary disk and backup tape technologies operating differently—the former with random access and the latter with sequential access—the same mass storage technology is provided for primary and backup storage. However, Winchester removable cartridges cannot yet compete with streaming tape drives—at least on a low cost per bit level—nor can they store the massive amounts of data that tape can. On this score, though, storage capacities for Winchester removable cartridges are rapidly improving.

System purging is an important aspect of removable Winchester cartridges. Since the read/write heads fly very close to the disk's surface, the drive system must be purged of any dirt or contaminant after the media have been removed and reinserted. Otherwise, a system crash could result. Even the smallest of dirt particles have

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caused read/write head crashes with a resulting data loss—not to mention possible disk surface damage due to the head/media collision. These purging requirements, however, have led to complex system drive mechanisms and delays.

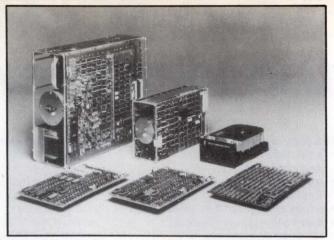
SyQuest Technology claims to have eliminated the usual purge cycle in removable Winchester cartridges with its SQ306R micro Winchester cartridge. It has achieved this by coating the thin-film media surface of the 3.9" diameter platter with a special lubricant that reportedly eliminates head crashes. With the SyQuest Winchester cartridge, the drive spins up to speed as soon as the cartridge is inserted in the drive. The actual purge cycle occurs as the drive initially comes up to speed. This contrasts with all other removable Winchester cartridge drives that require a wait of about 1.5 to 2 min after a cartridge is inserted before the purging operation is completed.

Groping for standards

Most industry disk standards are informal and revolve around disk drive dimensions. As each new disk drive is introduced, the manufacturer attempts to establish it as a *de facto* standard, particularly if it has an unusual or unconventional size or features. Many manufacturers have followed Shugart Associates (Sunnyvale, Calif), the disk drive industry leader.

One area in need of standardization is the disk drive interface. In this area, many disk controllers of the devicedependent variety have hitherto adopted different hardware and software specifications. Device-dependent controllers burden the host computer's central processing unit (CPU) with mundane tasks (eg, controlling the drive itself, formatting the data, and providing error detection and correction). This situation led to the emergence of intelligent controllers. These controllers are based on microprocessors that perform housekeeping chores for the disk drive, lighten the CPU's load, and provide for an intelligent host computer interface. An example of this is the Shugart Associates Systems Interface (SASI).

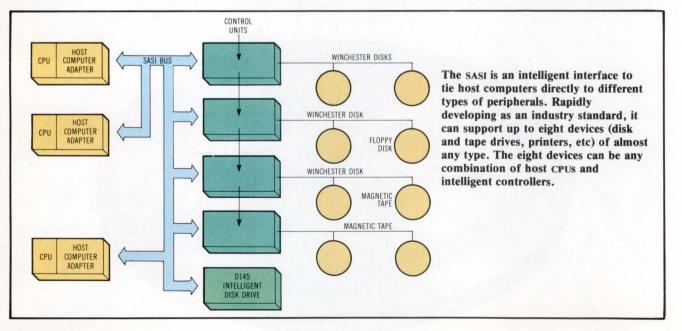
SASI is an 8-bit parallel bus containing control/status and data lines. It offers a high level command set for the host computer to use, regardless of the drive type. SASI



A family of Winchester drives from Priam includes $5\frac{1}{4}$ ", 8", and 14" drives, plus intelligent interface boards. The boards allow system designers to connect any combination of four Winchester drives—plus either tape or floppy disk backup—to a host processor.

defines a set of hardware and software specifications that allow a host computer's CPU to interface directly with any peripheral device, regardless of type (eg, disk drive, tape drive, printer, and communications device). SASI seems to be rapidly developing into an industry standard. ANSI currently has the SASI specifications under consideration before its X3T9.2 committee as a proposed standard. However, another ANSI committee (X3T9.3) is looking at an alternative proposal known as IPI or Intelligent Peripheral Interface. SASI-compatible Winchester disk drives incorporate within the drive system many functions normally found on separate controllers. SASI can support up to eight devices, including host processors, in any combination.

The SASI document defines a 50-pin connector for each of up to 8 bus ports. Each port has nine data lines and a timing line. In addition, software command and message protocols are specified along with a logical interface. A SASI controller interface has open-collector lines or differential driver/receiver lines. Seagate Technology has also established a *de facto* standard for 5¹/₄" mini Winchester disk drives with its ST506 drive.



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Eliminate the Software Overhead Associated with Electrostatics

The VP-30 eliminates the need to burden the host computer with the time consuming and expensive vector-to-raster data conversion task. The VP-30 accepts random vectors, symbols, and other graphic data from the host mainframe, reduces it to raster form and outputs it to the electrostatic plotter.

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CONNEC	TOR-PIN	SSIGNMENTS (J1/P1)	COMPUTER	DRIVE
GND RTN			DRIVE SELECT (4 LINES)	
PIN	PIN	SIGNAL NAME	In Brits Francisco In	
1	2	REDUCED WRITE CURRENT	HEAD SELECT (2 LINES)	
3	4	RESERVED	STEP	
5	6	WRITE GATE	SIEF	
7	8	SEEK COMPLETE	DIRECTION	A CARLES AND
9	10	TRACK 0	DIRECTION	
11 13	12 14	WRITE FAULT HEAD SELECT 20	TRACK 00	Л
15	14	RESERVED (TO J2 PIN 7)		DAISY CHAIN
17	18	HEAD SELECT 21	SEEK COMPLETE	OR RADIAL
19	20	INDEX		CONNECTED
21	22	READY		
23	24	STEP	READY	
25 27	26 28	DRIVE SELECT 1 DRIVE SELECT 2		
29	30	DRIVE SELECT 2	REDUCE WRITE CURRENT	
31	32	DRIVE SELECT 4		
33	34	DIRECTION IN	WRITE GATE	
CONN	ECTOR-PIN	ASSIGNMENTS (J2/P2)	WRITE FAULT	
	SIGNAL			
PIN	PIN	SIGNAL NAME	MFM WRITE DATA	10
2	1	DRIVE SELECTED	MITWI WRITE DATA	F J2 RADIAL
4	3	RESERVED	MFM READ DATA	CONNECTED
6	5	RESERVED		ONLY
8	7	RESERVED (TO J1 PIN 16)		
10	9, 10	RESERVED	5 Vdc	
12	11 13	GROUND + MFM WRITE DATA		
	13	- MFM WRITE DATA	5-V RETURN	J3
16	15	GROUND	12 Vdc	dc POWER
	17	+ MFM READ DATA	12 V00	
	18	- MFM READ DATA	12-V RETURN	
20	19	GROUND		
CONN	ECTOR-PIN	ASSIGNMENTS (J3/P3)	FRAME GROUND	
VOLTAGE		GROUND		→ J4
PIN 1 12	Vdc PIN	2 12-V RETURN		FRAME
		3 5-V RETURN	ST506 INTERFACE	GROUND

The Seagate Technology interface connector pinout for $5\frac{1}{4}$ " Winchester disk drives (a), is based on Seagate Technology's ST506 $5\frac{1}{4}$ " Winchester disk drive. Interface lines to the host computer are shown in (b).

Mechanical interchangeability of Winchester disk drives has generally been less of a problem than electrical interfacing. Therefore, for example, many so-called ST506-compatible drives do not meet all of the ST506's electrical interfacing requirements.

If a Winchester disk drive is Seagate compatible, it should strictly adhere to the specified Seagate data transfer rate of 5M bps. This assumes that the drive uses an MFM encoding scheme and has a spindle that spins at 3600 rpm. It must also have a recording density between 7690 and 9074 bpi, and an average latency time of 8.3 ms $\pm 1\%$. Without all of the aforementioned features, software incompatibility could result. In reality, few Winchester disk drives on the market are totally Seagate compatible.

Even more dismal is the removable Winchester cartridge arena—absolutely no standards exist for either dimensions or type of disk. DMA Systems has proposed a 130- x 40-mm cartridge with a conventional ferrite medium as a standard (currently under consideration by ANSI). Other Winchester removable cartridge manufacturers are also preparing designs that conform to the DMA Systems proposal.

Western Dynex Corp, for example, has opted to conform to the proposed DMA Systems standard with its WD505 $5\frac{1}{4}$ " 6.38M-byte (unformatted data) removable Winchester cartridge. The cartridge has a 35-ms average access time. On the other hand, the Seagate Technology ST706 removable $5\frac{1}{4}$ " Winchester cartridge at least meets the DMA Systems cartridge's dimensions. However, unlike the DMA Systems cartridge, which uses an embedded closed loop servo system, the Seagate cartridge works with an open loop servo system. Furthermore, the Seagate product uses a plated thin-film media.

Certainly, Winchester technology has come a long way in its first decade. The many advances include efforts to implement thin-film read/write heads on disk drives, developments in head positioning and tracking techniques, better circuits, denser encoding methods, and significant progress in perpendicular magnetic recording. While these and other changes in Winchester technology have allowed dramatic improvements in storage density, reliability, and cost, they make the need for industry-wide standards that much more urgent. Progress in this area would avoid unnecessary duplication of effort, as well as simplify system design.

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TAILOR THE WINCHESTER TO THE SYSTEM

By analyzing performance needs with an eye on future system requirements, designers can build mass storage options into dedicated designs.

by Larry Jacob

Providing high capacity and low cost/megabyte, Winchester disk drives are a logical choice for a multi-user/multitask environment. The designer's next choice is the specific type of Winchester and interface to use. Defining system requirements begins this Winchester selection process.

The three fundamental system configurations—single user/single task (SU/ST), multi-user/multitask (MU/MT), and single user/multitask (SU/MT)—all have different mass storage requirements (see Table 1). Networks or distributed processing installations are really hybrids of the SU/ST and MU/MT types. High powered workstations frequently part of a network—can be thought of as SU/MT systems. In an SU/MT system, a single user may have several different programs (tasks) running in parallel. These tasks might include word processing, compiling a BASIC program, plotting financial information, and sending or receiving an electronic mail message.

Six types of original equipment manufacturer (OEM) Winchester disk drives serve the three system types.

Larry Jacob is currently the product marketing manager for 14" Winchester disk drives and SMART interfaces at Priam Corp, 3096 Orchard Dr, San Jose, CA 95134. He has held various disk drive engineering posts at several companies over the last 13 years. Mr Jacob has a BSEE from Oregon State University and an MSEE from Stanford University. These Winchester drives are built in one of the three currently available disk diameters (14", 8", and 5¹/₄"). Each uses either one of the two basic actuator systems—the low performance, open loop stepper motor and the high performance, closed loop voice-coil motor (VCM). Table 2 shows the typical capacity and access time range characteristics.

Mapping systems into drive types

To assist in choosing an appropriate Winchester disk, a mapping of the three system configurations into the basic drive types has been developed (see the Figure). The SU/ST small size and capacity, low cost, and light duty cycle storage requirements best fit the $5\frac{1}{4}$ " stepper motor Winchester. However, if the SU/ST system is to grow into an SU/MT system, plans must be made now for using a $5\frac{1}{4}$ " VCM later. Today, several years after low capacity (under 10M bytes) $5\frac{1}{4}$ " drives were introduced, high capacity $5\frac{1}{4}$ " drives in the 40M- to 55M-byte range have made their entrance.

Moderate capacity, performance, and very small size storage requirements of the SU/MT best suit the $5\frac{1}{4}$ " VCM Winchester. However, production quantities of these drives are not available, and the product and vendors still need to be field proven. For capacity and performance in a small package size in 1983 (maybe even 1984), it is safe to stay with an 8" VCM.

The MU/MT high capacity, low cost/megabyte, and heavy duty cycle storage requirements are most appropriate for the 14" VCM Winchester, except where size is more important than large storage capacity. In this case,

TABLE 1 Mass Storage Requirements for Three Popular System Types

SU/ST	MU/MT	SU/MT
Dedicated data base	Shared data base	Dedicated/shared data base
Jp to 20M bytes	30M to 400M bytes	20M to 50M bytes
ow cost per unit is key	Low cost/megabyte is key	Both cost/unit and cost/megabyte considerations
Slow data access acceptable	Fast data access required	Moderately fast data access required
Light duty cycle imposed on actuator	Heavy duty cycle	Moderate duty cycle
Small size is key: used in portable desktop systems, floppy disk cavities	Small size is helpful: used in pedestal or rackmount systems	Small size is key

the 8" VCM should be considered, as most 14" drives include space for a power supply and 8" drives do not. If an 8" drive is chosen, the drive power supply must be considered in space planning.

The capacity needs of the SU/ST and SU/MT applications are growing beyond the range of $5\frac{1}{4}$ " drives. However, if $5\frac{1}{4}$ " drive capacity reaches what is projected, and if these drives become available in volume, $5\frac{1}{4}$ " drives will eventually supplant 8" drives in some systems. This will happen first at the low end (open loop stepper motor) segment of the 8" market. At the opposite end of the scale, the portion of large existing size-sensitive MU/MT applications is also likely to grow, leading to increased use of compact 14" VCM and floppy-size 8" Winchesters.

Future system storage requirements will not necessarily coincide with 8" and 14" stepper motor Winchesters. Though the physical size of such Winchesters may fit the MU/MT system, their access time, duty cycle, and storage capabilities are more suited to SU/ST systems. Thus, the use of these Winchesters by system designers will decline.

Attention must be paid to the growth capacity of the chosen device. Lateral growth paths (ie, where the device's physical size remains the same) are relatively easy to implement without changing interface or system packaging. Vertical growth paths (ie, where the physical

size of the drive changes) occur less frequently due to the relentless capacity increases in the 51/4" and 8" disk sizes. Nevertheless, both growth paths are important due to the increasing propensity of system manufacturers to repackage successful systems for different markets. For example, standalone machines are souped up to serve multi-user markets, and multi-user systems are downsized to serve desktop markets. In both cases, travel along a growth path, where the drive interface is common, is much easier than if interface, power, and software changes are required.

A checklist for high performance

To evaluate high performance Winchesters, several other issues need to be addressed. These include system architecture, system integration, reliability, vendor viability, and total ownership cost.

Drive performance, which is key in MU/MT applications, is affected by system architecture. Small changes in disk drive specifications or system timing requirements can drastically affect total system performance. Consider a microsecond change in the time required to switch heads. This change could preclude reading the next disk sector, causing tens of milliseconds to be added to a multisector operation. Similarly, an increase in data rate could cause sectors to be missed because of a suboptimal interleaving factor, again adding tens of milliseconds to each operation.

When evaluating system performance with different Winchester drives, it is important to verify that the disk is not constrained by a system parameter (like interleave factors). In most disk drive applications, a significant portion of the total transfer time is spent in seeking and waiting. These times are overlapped and minimized as much as possible in a well-designed system. Many variations have minimal effect. When a boundary is approached, however, performance often changes suddenly and drastically.

	TABLE 2	
	Six Basic Types of Winchester Disk	C Drives
	Actuator Type	
Disk Size	Stepper Motor (low performance, open loop)	Voice-coil Motor (high performance, closed loop servo)
5¼″	Up to 20M bytes, 85 to 200 ms	20M to 50M bytes, 35 to 50 ms
8″	10M to 40M bytes, 70 to 80 ms	30M to 100M bytes 30 to 50 ms
14″	30M to 40M bytes, 70 to 80 ms	30M to 300M bytes 30 to 50 ms

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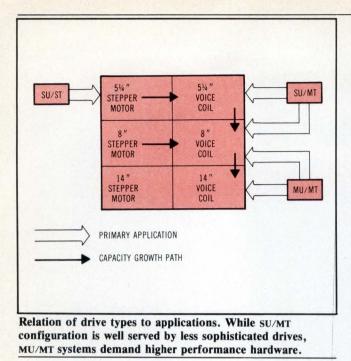
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The interface-a critical choice

Choosing the Winchester is just the first step in system integration. Making it work in a prototype and then in production systems is more difficult. The interface is intrinsic to this task. More decisions have to be made regarding a new system design than an enhanced or redefined system. In either case, the interface options must be evaluated on the basis of functional integrity, application requirements (perhaps emulation), controller availability, and projected longevity of the interface.

Choosing the disk drive interface may be a bigger commitment than choosing a particular drive capacity level because of the rapidly changing storage market. Projecting disk requirements for the future of a product line is an important factor, especially assuring that the interface choice will remain appropriate. In the long run, a high level interface makes the most sense; floppylike, external data separators make the least. Also, because the market is changing so quickly, choosing an intelligent controller or a memory subsystem may accelerate the product to production.

Higher level interfaces have technical advantages they all contain data separators. In truly high performance products, the data separator is fundamental to data integrity. Thus, it is advantageous to the OEM to have the disk vendor responsible for an appropriate data separator design. Another advantage of higher level interfaces is their ability to deliver diagnostic status information.

Interfaces can be very simple, unsophisticated, and merely approximate floppy disk drive control capabilities. They grow more sophisticated in capability and intelligence until the drive, with its interface, actually constitutes a disk subsystem. In such a subsystem, many sophisticated disk controller functions are added to the drive's data storage capability. For example, a low cost, low function interface provides the user with modified frequency modulation (MFM) data and bit oriented command and status information. Although this interface is the most difficult to use, it is the most economical. It may be attractive to the SU/ST large volume, cost-sensitive user who has substantial engineering and manufacturing resources, and is capable of designing, testing, and controlling the data separation circuitry required to process MFM data of higher and higher data rates.

An early OEM disk interface provides nonreturn to zero (NRZ) data (ie, data separation is performed onboard the drive). Commands are byte oriented; status is bit oriented. Control Data Corp's SMD interface, developed in the early 1970s, has become a standard interface for larger systems. Though most designers consider it technically obsolete (it is cumbersome to use and costly to implement), the wide range of disk drives available with the SMD interface contribute to its continuing popularity with system designers.

Making a designer's life easier

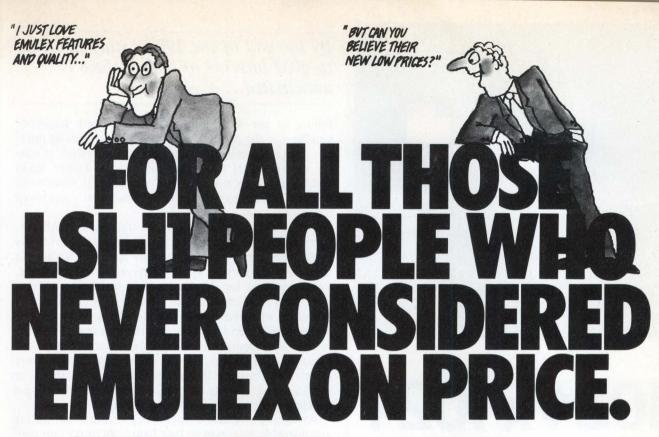
A modern disk bus interface has an NRZ data stream like its predecessor, but both command and status information are byte oriented and the interface is typically microprocessor driven. The modern disk bus interface costs a little more than the low cost, low function interface, but is substantially easier for the system designer to use. It provides better data integrity since the data separator circuitry is onboard the drive and thus defined by the disk drive supplier. Examples of this interface include the American National Standards Institute standard and Priam interfaces.

Intelligent bus interfaces such as ISI, SCSI, and SMART are indicative of the trend toward dispersing intelligence to components of computer systems and making disk drives easier for system designers to use. Using a microprocessor to provide broad control at low cost, the intelligent bus interface is completely byte oriented and is designed to adapt readily to commonly used microprocessor input/output buses. High level versions of the intelligent bus include disk formatting and defect mapping, implied seeks, daisy chaining capabilities, selectable sector sizes, automatic alternate sector and track assignment, overlapped commands, data buffering, error correction, nonbuffered data transfers at disk speed, interleaved formats, backup device support, and logical or physical sector addressing.

Choosing the disk drive interface may be a bigger commitment than choosing a particular drive capacity level...

When OEM systems use bus interfaces, integration problems are reduced and data integrity is improved. Moreover, the OEM system gets running and into production three to four times faster using fewer resources. With the economies of scale available through volume manufacture of intelligent interfaces, the disk manufacturer can cost-effectively bring this type of product to the system manufacturer.

Reliability is Winchester technology's key attribute. Some supporting areas need to be considered as well, since the term "Winchester" has many definitions. The essential ingredients of the IBM 3350's original Winchester technology consisted of low mass, low force heads with contact start/stop capability, fixed media, and a sealed environment. The most common causes of



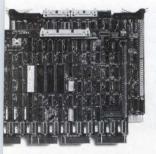
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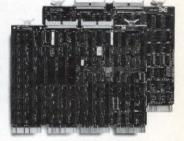


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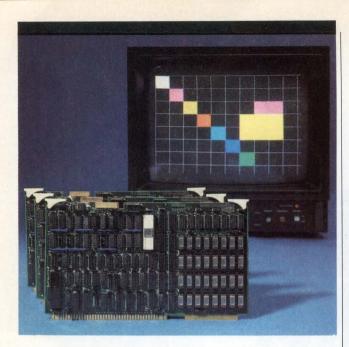
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By the end of the 1980s, storage of up to 60M bits/in² of disk surface is anticipated...

failure in pre-Winchester disk drives were improper handling of the packs and cartridges by computer operators, and exposure of disk packs and cartridges to hostile environments (including the office). Today, disks and heads are permanently enclosed in most Winchester drives. This design is vital to the Winchester's improved reliability.

Where reliability is concerned, the terms "high performance" and "stepper motor" are almost mutually exclusive. Stepper motors typically have shorter lives in the heavy duty cycle applications of MU/MT systems. VCMs designed for this kind of use last longer. Moreover, data recovery is not as affected by temperature or vibration in drives using closed loop servo voice-coil positioners. Open loop systems are more sensitive to the effects of temperature change and external vibration. Sampled data systems usually take care of temperature effects, but not the instantaneous effects of shock or vibration, which may be induced by simply bumping a desktop system.

Analyzing a vendor's track record before committing considerable resources to that firm is an important consideration. The vendor must not only be able to support the prototype systems, but also the follow-on production that will be put in place. The manufacturer's technical support staff is of basic importance in providing application assistance and servicing the disk drive products once on the market.

Worth the price

While some drives cost more initially, they may have more inherent reliability, and thus require fewer service calls or repair incidents in the long run. A higher initial cost drive may, in fact, have a lower life cost of ownership.

It is predicted that improvements to disk drive technology will vastly increase disk density. By the end of the 1980s, storage of up to 60M bits/in² of disk surface is anticipated through the use of plated or sputtered disk surfaces, new recording techniques, and thin-film heads. This potential for improvement in sealed disk drive technology ensures that disk drives will provide the most economical and reliable means of storing and retrieving large amounts of data in the future.

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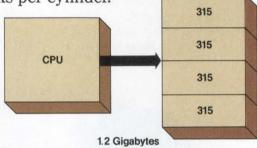
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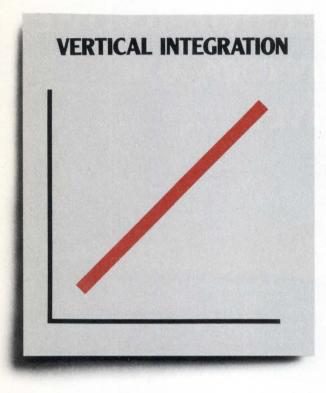
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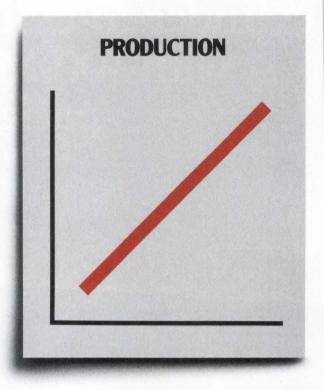


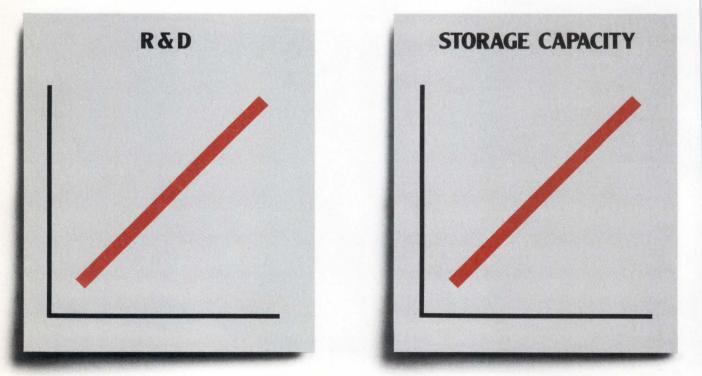
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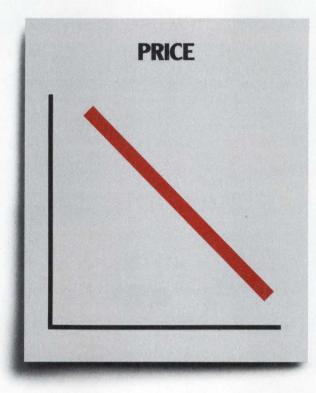






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MICROFLOPPIES BATTLE FOR PREEMINENCE

Designers face big decisions about tiny disk drive formats and standards. The reason: There is a large number of contenders about to slug it out in the sub-4" arena.

by Robert Abraham and Ron Munro

System designers and integrators have a new random access data storage system to consider—the sub-4" disk drive. Because its diameter is under 4" and its volume is about one fourth the standard 5¼" drive, these disk drives are destined for such applications as small computer systems, programmable instrumentation, electronic typewriters—any application where small physical size is a prime consideration. The first of the expected rush of competing designs and technologies has already been introduced, and drive and media manufacturers, as well as the American National Standards Institute (ANSI), are attempting to standardize media size and characteristics, drive capacity and configuration, and interface compatibility.

A major design goal for many computer systems has been smaller storage devices at lower costs. Now that floppy disk dimensions have shrunk to less than 4" in diameter, disk incompatibility is one of the key issues being confronted by the disk drive industry. Standardization is essential if interchangeability, secondsourcing, and software transportability are going to be possible. Media questions, such as oxide coating thick-

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Ron Munro is the director of engineering at Tandon Corp, Magnum Div, where he is responsible for 8" and Microfloppy disk drive engineering. Mr Munro has a BS and an MS in engineering from the University of California, Los Angeles. ness, protection, centering techniques, and packaging, need to be answered. Manufacturers are also dealing with such drive performance standardization issues as rotational speed, capacity, data transfer rates, physical configuration, and interface compatibility. Although one focus of the standardization effort is the ANSI committee, just as in the past the marketplace is helping to sort out the manufacturer's various alternatives.

The Microfloppy Standards Committee (MSC) consists of representatives from media manufacturers— Verbatim, Xidex, Brown Disk, and BASF—and drive manufacturers—Shugart, MPI, and Olivetti. Tandon, Seagate, HP, and Sony, once original members, withdrew for various reasons. The MSC diskette proposal incorporates much of the Sony diskette design, is based on a $3\frac{1}{2}$ " oxide-coated, hard-jacket diskette, and could be used by numerous drive manufacturers. Its specifications include 136 tracks per inch (tpi), 8178 bits per inch (bpi) linear density, 500k-byte storage capacity, 80-track single-sided format, and 500k bits per second (bps) transfer rate.

The diameter of the disks used in this generation of computer-grade sub-4" disk drives will be selected from at least five competing configurations. By late 1982, four sizes, all under 4" in diameter, had surfaced: Hitachi, 3"; Tabor/Dysan, $3\frac{1}{4}$ "; Sony, $3\frac{1}{2}$ "; MSC, $3\frac{1}{2}$ "; Canon, 3.8".

Disk diameters effect system parameters such as capacity, packaging, and access time. When compared to its larger $5\frac{1}{4}$ " and 8" cousins, the sub-4" disks provide higher density in a smaller package while offering similar performance. This phenomenon—higher track density on a smaller diameter disk—is due to the basic thermal and hygroscopic properties of the coated Mylar media.

In normal operation, a Mylar disk expands and contracts due to changes in ambient temperature and

Players and products in the sub-4" arena

Sony Corp introduced the first sub-4" disk drive and diskette almost two years ago. Based on their own 31/2" diskette, Sony's OA-D30V disk drive was originally aimed at Sony's office equipment market. Sony has since proposed a modified version of their diskette to ANSI that encompasses many existing 51/4" floppy characteristics. This new version, which should be available this spring, features an 80-track single-sided format. The diskette is encased in plastic, and has a metal hub that is intended to prevent wear and eliminate chucking error. A spring-loaded aperture cover opens automatically when the disk is inserted into the drive. Upon removal, it closes automatically preventing damage to the media. Sony indicates that the diskette can support a 1.6M-byte storage capacity-equal to that of an 8" drive-and is compatible with the original 70-track version.

The recording device is a magnesium-zinc crystal ferrite head that uses video recording techniques. A tunnel erase head with a narrow 125-micron track width is instrumental in achieving high density. A

stepper motor and lead screw comprise the positioning elements of the head.

Published performance characteristics of the Sony 70-track drive include an average access time of 365 ms, a track to track access time of 15 ms, a head settling time of 15 ms, and an average latency of 50 ms. Drive dimensions are 2" high by 4" wide by $5\frac{1}{6}$ " deep (5 x 10 x 12 cm).

Two configurations of Tandon's TM35 microfloppy have been designed to promote standardization of two classes of peripherals. TM35-4 is compatible with Sony's OA-D30V micro-floppy disk drive in three areas—interface, software, and diskette—but differs from the Sony OA-D30V drive in physical dimensions, mounting holes, and the fact that it is a double-sided recording drive.

The Tandon TM35-4 disk drive stores 875k bytes on a $3\frac{1}{2}$ " disk. It accesses data in an average time of 85 ms and moves from track to track in 3 ms. The Tandon TM35 occupies a space only $1\frac{5}{6}$ " high by 4" wide by $6\frac{1}{2}$ " deep. The Tandon TM35-4 has 88% of

Characteristics	Hitachi HFD-3055 (3")	Tabor/Seagate	Canon CMD 300/500 (3.8")	Tandon TM35-2 (3½")	Tandon TM35-4 (3½″)	Sony OA-D30V (
Recording density (bpi) Single/double-density	4473/8946	4625/9250	2792	3128/6255	3805/7610	3805/76
Encoding method Single/double-density	FM/MFM	FM/MFM	FM	FM/MFM	FM/MFM	FM/MFI
Capacity/side (kbytes) unformatted FM/MFM Single/double-density	125/250	250/500	40	125/250	218.8/437.5	218.8/43
Transfer rate (kbits/s) Single/double-density	125/250	250/250	33.32	125/250	250/500	250/50
Disk diameter (inch)	2.84	3.25	3.8	3.40	3.40	3.40
Cartridge dimension (inch)	0.197 x 3.15 x 3.94	0.06 x 3.268 x 3.425	0.197 x 4.0 x x 4.20	0.133 x 3.54 x 3.70	0.133 x 3.54 x 3.70	0.133 x 3 x 3.70
Drive dimension (inch)	1.58 x 3.55 x 5.83	1.625 x 4.0 x 5.5	2.91 x 4.29 x 5.91	1.62 x 4.0 x 6.50	1.62 x 4.0 x 6.50	2.0 x 4. x 5.12
Tracks/side	40	80	16	40	70	70
Tracks/in	100	140	25.4	135	135	135
Disk speed (rpm)	300	300	100	300	600	600
Power supply	5 Vdc 12 Vdc	5 Vdc 12 Vdc	5 Vdc 12 Vdc	5 Vdc 12 Vdc	5 Vdc 12 Vdc	5 Vdc 12 Vdc
Average access time (ms)	55	282	NA	55	85	365
Track to track access time (ms)	3	10	40	3	3	15
Settling time (ms)	15	15	60	15	15	15
Average latency (ms)	100	100	300	100	50	50
Sides	2	1	2	2	2	1
5¼″ minifloppy Interface compatible	Yes	Yes	No	Yes	No	No
Metal hub on media	No	Yes	No	Yes	Yes	Yes

Sub-4" Disk Drive Companion Chart

the data storage of a standard $5\frac{1}{4}$ " floppy drive, yet takes up only 25% of the volume. Moreover, this new $3\frac{1}{2}$ " floppy drive records more than half as much data as a standard 8" drive's 1.6M-byte capacity, while occupying 13% of the space.

The Tandon TM35-4 disk drive uses a $3\frac{1}{2}$ " Sonytype diskette with a rigid case, a hard metal hub, and an oxide coating. The diskette achieves 437.5k bytes/surface with standard frequency modulation/ modified frequency modulation encoding. The cost is commensurate with a $5\frac{1}{4}$ " diskette and has the added value of a firm jacket and a hard centering hub. A recording density of 7610 flux reversals/in has been achieved on the $3\frac{1}{2}$ " diameter disk. The capacity of 437.5k bytes/surface is achieved with 135 tpi, and 70 tracks/side. This compares to 5877 flux reversals/in, 96 tpi, and 80 tracks/side for a comparable $5\frac{1}{4}$ " drive.

Tandon's second microfloppy configuration, the TM35-2 is compatible with the 5¼" industry standard interface. This allows systems integrators who have existing 5¼" controllers and software to incorporate the new 3½" disk drive by simply making a change in the package. No controller redesign or software changes are required. Furthermore, the Tandon TM35-2 produces a disk format written as if it were a 5¼" disk, with 40 tracks/side, double-sided recording, 250k-bps transfer rate, and 500k-byte capacity. Read/write and control electronics are functionally similar to that of a 5¼" drive but occupy less space. An onboard Intel 8048 microprocessor controls the spindle motor, head positioning, power-up initialization, and some diagnostics.

Because of the smaller disk diameter in the $3\frac{1}{2}$ " drive and use of standard motor speeds in both Tandon drives, the bit density is adjusted to achieve the desired data transfer rates. The disk spins at 300 rpm in the TM35-2 to attain 250k bps and double-density, and at 600 rpm in the TM35-4 to achieve a transfer rate of 500k bps. The motors are direct-drive, brushless units mounted directly below the disk.

A variation of the patented Tandon double-sided floppy recording head is used. The original design features a fixed button-shaped head for recording on the bottom side of a floppy disk and a movable slidertype head for the top surface. The top head is mounted on a pivoted, low-mass, spring-loaded arm. This arm gently forces the head against the disk while recording, without causing undue wear on the disk or head. It also minimizes head settling time. For the TM35, a manganese-zinc head has been selected to match the narrower recording tracks. A band drive positions the head, and a track to track access time of 3 ms is achieved. This is up to five times faster than the speed attained with lead screws or other devices. The band-drive positioner is virtually frictionless, assuring accurate track positioning.

The TM35 drive provides a fail-safe feature that prevents improper loading of the diskette. An automatic shutter that will be available on the diskette will close over the exposed portion of the disk when it is not in use, keeping out dust and other contaminants. Since the TM35 is dc powered, it can be used in either domestic or overseas operations without making changes in the drive. Less than half of the power is required, and less heat is generated by this drive than by drives requiring both ac and dc power.

Hitachi has proposed a microfloppy drive based on a diskette with a 3" diameter. Drives utilizing the same 3" diskette will also be manufactured by Matsushita/Panasonic and Sankyo. The media will be manufactured by Hitachi/Maxell and TDK. The 3" diskette cartridge has been designed to be compatible with Japanese standard postal dimensions to avoid charges for odd-sized documents. The diskette features an automatic aperture shutter that prevents damage to the media. Its index can be detected optically by an index hole or mechanically by an index notch that is part of the hub. Thus, the diskette can be used in a variety of memory architectures.

The double-sided diskette format will feature 100 tpi, 8946-bpi linear density, 40 tracks/side, and a 0.5M-byte capacity. The media employs a 3-mil substrate and a 60- μ in oxide coating. Future double-sided versions of the diskette reportedly are planned that will feature 200 tpi, 9000 or 15,000 bpi, 80 tracks/side, and 1.0M- or 1.6M-byte capacity. It is reported that the 1.6M-byte diskette will use a new substrate material that has improved thermal and hygroscopic characteristics.

The Hitachi drive is characterized by an average access time of 55 ms, track to track access time of 3 ms, head settling time of 15 ms, and an average latency of 100 ms. Transfer rate is 125k bps for single-density and 250k bps for double-density. The Hitachi drive is interface-compatible with $5\frac{14}{7}$ floppy drives.

Tabor Corp, a startup disk drive company, split off from the original MSC. The company proposed a 31/4" diskette to ANSI to be manufactured by Dysan. Seagate Technology has reportedly agreed in principle to manufacture the Tabor drive under manufacture license. The diskette cartridge is rectangular, measuring 3.268" by 3.425". A soft, folded jacket similar to that used in 51/4" diskette encases the media. The diskette employs a self-indexing metal hub similar to the Sony diskette. Media coating is 600-oersted, 60-µin oxide coating on a 3-mil substrate. The Tabor drive has a capacity of 500k bytes. The format is 80 double-sided tracks, and the transfer rate is 250k bps. Disk rotation speed is 300 rpm. The drive will be interface-compatible with 51/4" floppy drives.

Canon Electronics has developed its CMD500 disk drive around a 3.8" diskette. Drive dimensions are 2.91" high by 4.29" wide, and the diskette is housed in a flexible jacket. A capacity of 40k bytes is the smallest of the computer-grade drives offered. As such, the CMD500 appears to be designed for program loading functions. Recording density is 2792 bpi, track density is 25.4 tpi. There are 16 recording tracks. The disk rotates at 100 rpm, permitting a data transfer rate of 33.32k bps. Rotational latency is 300 ms, and head settling time is 60 ms. The head positioning mechanism is a steel band, driven by a stepper motor. A belt drive is used for disk rotation. Developed as an extension of the floppy disk drive, the Canon CMD500 has an interface similar to a 51/4" mini-floppy drive.

humidity. A data track can physically wander within a certain tolerance on a disk and still be read accurately. However, beyond this allowable tolerance, the recording head—which steps across the disk to preset track positions—cannot recover the data. The magnitude of the thermal expansion increases proportionally with disk size—the smaller the disk, the less expansion and the higher the achievable track density.

A comparison of the recording areas available on $3\frac{1}{2}$ ", $5\frac{1}{4}$ ", and 8" disks is shown in Fig 1. The $3\frac{1}{2}$ " disk packs 437.5k bytes into a 135-tps and 70-tracks/ surface configuration. The $5\frac{1}{4}$ " disk achieves only 13% more capacity—500k bytes—from a 96-tpi and 80-tracks/ surface format. The 8" offers less than 50% more capacity—800k bytes with a 48-tpi and 76-tracks/surface layout.

What is the optimal diameter and resulting track count for microfloppies? Sony chose the $3\frac{1}{2}$ " diameter.

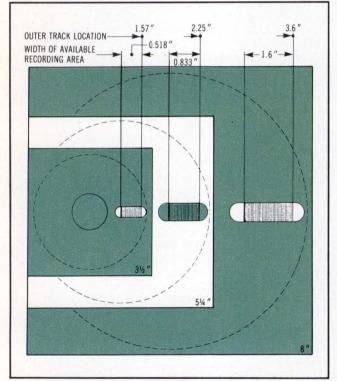


Fig 1 Radial positions of disk areas available for recording. Comparison reveals that density can be increased on smaller disks due to reduced thermal and hygroscopic properties of Mylar media.

Originally a 70-track configuration, the disk has a linear density of 3805 bpi single-density and 7610 bpi doubledensity. Unformatted capacity per side is 218.8k bytes single-density and 437.5k bytes double-density. Unfortunately, this configuration is not compatible with the $5\frac{1}{4}$ " mini-floppy disk drive controllers or software.

The $3\frac{1}{2}$ " disk diameter, however, has enough area (4.1 in²) to accommodate 80 tracks/surface at 135 tpi, making a 125k-byte/side, single-density capacity possible. Tandon, using the Sony $3\frac{1}{2}$ " diskette in its TM35-2 disk drive, obtains this $5\frac{1}{4}$ " compatible format. Sony is expected to introduce a product in early 1983 that uses an 80-track/side configuration and double-density recording. Drives with 250k-byte, 500k-byte, or 1M-byte capacities can be easily designed that are the exact capacities of existing $5\frac{1}{4}$ " disk drives. A

1.6M-byte capacity on a $3\frac{1}{2}$ " surface is also possible. This capacity—the same as that of a standard 8" disk—could be achieved by a combination of closer track spacing and increased linear density on improved disk substrate and coating.

Hitachi's 3" diskette dimension results in a somewhat smaller—2.76 in²—disk area. This 3" diskette is capable of recording 40 tracks/side with a 100-tpi track density. With this format and area, a 1M-byte capacity/disk is not as easily achievable.

The Canon 3.8" diskette has the most available area of the announced disks. However, the drive using this disk employs a 16-track layout and a track density of 25.4 tpi, and offers a recording density of 2792 bpi and a capacity of 40k bytes. Although program loading is apparently an application for this disk drive, the Canon drive falls short of the higher storage capacities that are expected from sub-4" drives.

In addition to disk size, the thickness of both the oxide coating and the substrate are under scrutiny in the standardization effort. The MSC is recommending a coating that is 40- to 50- μ in thick and a 650-oersted level of coercivity. Sony is proposing a 100- μ in and 500-oersted coating. Media interchangeability between drives would be furthered by a coating standard.

The packaging of the microfloppy diskette is yet another standardization issue. Two basic packaging schemes exist. The first uses a hard jacket to encase the disk. The second uses a flexible jacket, similar to that used on mini-floppies. Sony is the leading advocate of the hard jacket—their OM-D30V diskette is encased in hard plastic. Hard jackets reduce friction between the moving disk and its stationary envelope and protect the recording medium from damage during handling. Hard jackets also benefit prerecorded floppy disks because the jackets allow greater yields and easier automated handling in recording equipment. The flexible jackets, on the other hand, offer user familiarity, minimal cost, and minimum storage space requirements.

The MSC favors incorporating an automatic shutter into the hard disk jacket. Sony, which introduced its diskette with a manual shutter, is expected to add a spring-loaded aperture cover. The shutter will then open automatically when the disk is inserted in the drive and close automatically when the disk is removed. Dust, dirt, fingerprints, and other performance inhibitors are kept out. Hitachi's 3" diskette also features an automatic shutter.

The dimension of the centering hole is an issue. A metal centering hub, part of Sony's $3\frac{1}{2}$ " diskette, allows accurate track positioning without causing eccentricity or wear. Fig 2 compares conventional mechanisms and Sony's disk chucking mechanisms. The MSC is recommending a 3-mm hole, 1 mm smaller than the hole in the Sony diskette.

Two disk rotational speeds are contending for acceptance as the standard, and data transfer rates will be determined by the choice made. The $5\frac{1}{4}$ " standard speed of 300 revolutions per minute (rpm) allows a sub-4" drive to transfer data at 250k bps—the same rate as that of a $5\frac{1}{4}$ " mini-floppy drive. Compatibility with the existing $5\frac{1}{4}$ " software base is an obvious benefit. A 600-rpm rotational rate—the second contender—doubles the data transfer rate to 500k bps. This rate coincides with 8" floppy rates and provides the higher surface



*SA-600 disk drive photo and media platters courtesy of Shugart Associates, and head arm assembly courtesy of INFOMAG.

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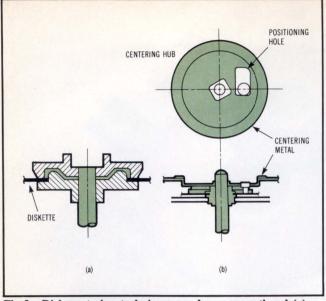


Fig 2 Disk centering techniques used on conventional (a) and Sony (b) hubs. Surrounding disk centering hole with rugged metal ring prolongs disk life, improves centering accuracy, and ultimately reduces inner track errors.

velocities and data transfer rates needed in future office systems that will be using small storage peripherals. In an attempt to satisfy diverse market needs, Tandon offers drives capable of operating at both speeds.

A concerted effort to make the emerging sub-4" microfloppy disk drive compatible with existing 5¼" drives is underway. The MSC recommended to ANSI that both software and controller compatibility be standardized. The large 5¼" software base and huge population of 5¼" drive users will be available to the microfloppy supplier. As the comparison chart in the Panel shows, 5¼" compatibility is built into the majority of sub-4" drives. Tandon's TM35-2, for example, is compatible with the 5¼" industry standard interface, transfer rate, and software.

This interface (Fig 3) uses a 34-pin edge connector to standardize the communications between the controller and the disk drive. The controller signals the selection of the drive, motor startup, head movement, data to be recorded, write enabling, and disk-side selection through predetermined pin assignments. (See the Table.) Drive to controller signals move through the remaining pins. They communicate ready status, index location, position of the first track, read data, and write protection status.

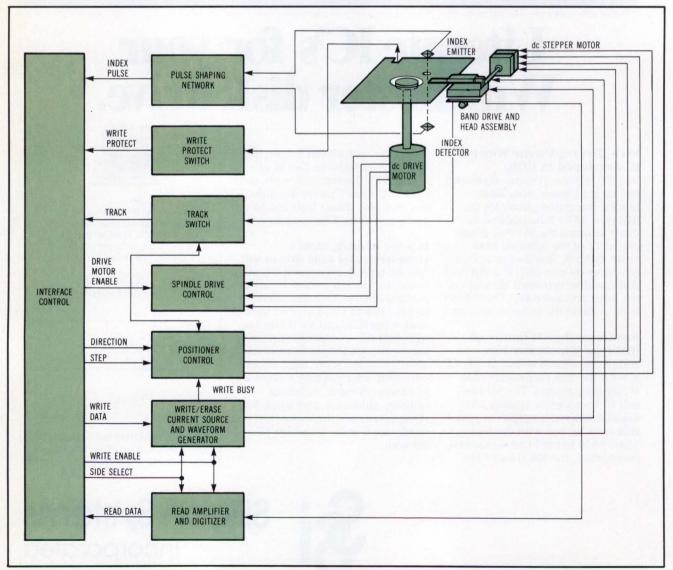


Fig 3 Tandon TM35 microfloppy disk drive interface lines. The 34-pin edge connector used in interface provides compatibility with 51/4 " disk drives.

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3	4	Spare
5	6	Drive select 3
9	10	Drive select O
11	12	Drive select 1
13	14	Drive select 2
15	16	Motor on
17	18	Direction select
19	20	Step
21	22	Composite write data
23	24	Write enable
31	32	Side one select
	Output	status lines
	(Disk drive	e to controller)
Ground	Pin	Signal
7	8	Index/sector
25	26	Track O
27	28	Write protected
29	30	Composite read data
33	34	Connector clamp

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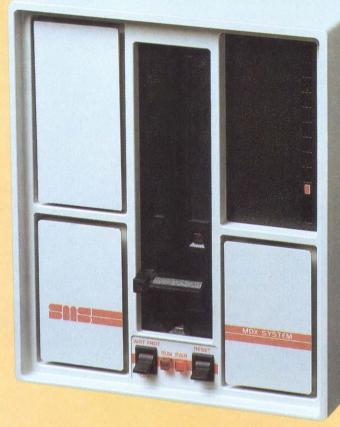
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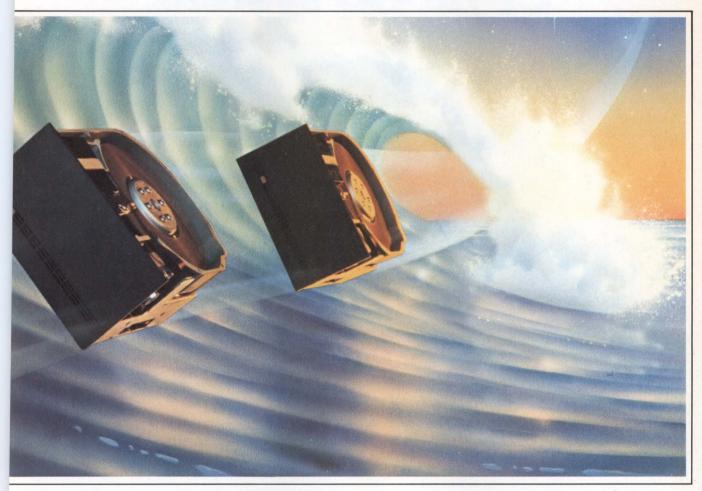
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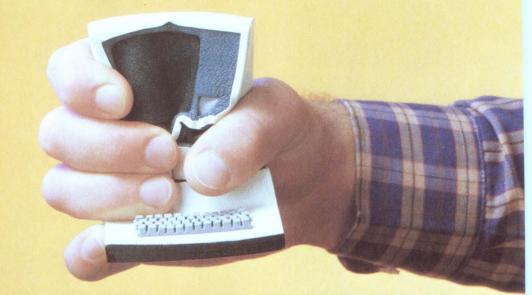
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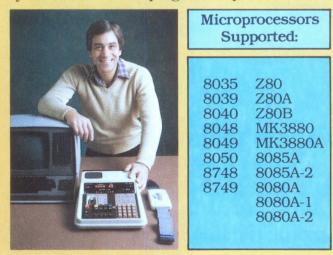


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OPTICAL DATA STORAGE TECHNOLOGY STATUS AND PROSPECTS

Many critical technical issues have been solved, and progress continues in diode lasers and storage media.

by Alan E. Bell

Research and development of high density optical data storage began almost 20 years ago, shortly after the laser's invention. A fundamental property of laser (ie, coherent) light is that it can be tightly focused to form an extremely small spot with a very high lightpower density. Peak intensities of a few megawatts/ square centimeter within a micron-sized write spot are not unusual in optical recording systems. The industry has recognized that this single property of laser light offers the potential for optical data storage systems with exceptionally high density. Indeed, this potential has been the driving force behind research and development.

In recent years prototype optical data storage systems have been demonstrated that use focused optical read/ write (R/W) beams with a diameter of one micron or less to store data at densities of 10^8 bits/cm² or more.^{1,2,3} Active programs in the United States, Japan, and Europe are expected to lead to optical storage product introductions across a broad segment of the cost/ performance spectrum during the next three years.

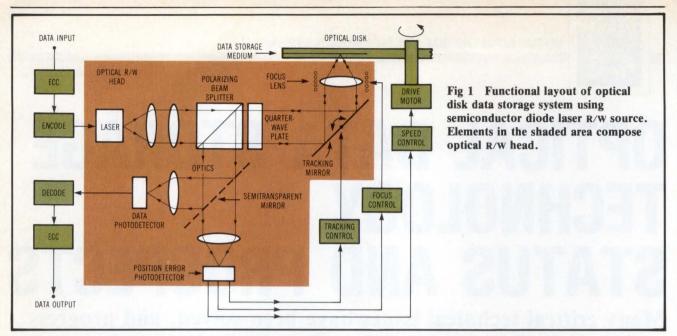
Optical data storage: its scope and status

Like magnetic storage technology, optical storage technology encompasses a family of configurations that address the many requirements of data storage products' end users. In optical storage technology three configurations exist: read only, write once (archival), and erasable (reversible). The system design of these configurations is quite similar, reflecting the fundamental issues of optical recording and retrieval of data that are stored at densities of 10^8 bits/cm² or beyond. On the other hand, the general types of optical storage media are uniquely defined by the functional classification of the optical storage devices; the fabrication of acceptable optical storage media in general presents a broad challenge in the areas of materials and process science and technology.

Read only optical storage systems are already available. The video disk⁴ and the recently introduced digital audio disk (DAD)⁵ are examples of products that employ factory replicated media for the low cost distribution of large volumes of prerecorded video and digital audio information. In these cases the media are plastic disks that contain the prerecorded information in the form of micron-sized pits embossed or molded into their surfaces. By way of comparing this kind of information storage, consider that the 1-h playing time for the consumer video disk represents an equivalent informational capacity in excess of 50G bytes. Even taking into account that the error rate requirement for a video (analog) channel is far less stringent than that demanded by a digital channel associated with a data processing system, the digital storage potential of optical media is enormous.

The read only optical disk has clear applications in such areas as low cost program and data base distribution, particularly with respect to the flourishing field of small-system and personal computers. A single $5\frac{1}{4}$ " read only optical disk offers a data capacity of a few hundred megabytes, coupled with a media replication cost of significantly less than \$10 and a drive cost consistent with extremely large markets. In this application area, the optical read only memory's cost/performance cannot be approached using current magnetic storage device configurations.

Alan E. Bell is with IBM Research Laboratory, 5600 Cottle Rd, San Jose, CA 95193, where he works in the development of optical data storage systems and media. He holds 17 U.S. patents in optical data storage and has written over 25 publications. Mr Bell has BSc and PhD degrees in physics from Imperial College, London University.



Several corporations around the world are involved in programs aimed at the introduction of write-once optical storage systems planned for 1983 to 1985.6 At the high performance level, these products are expected to offer single-surface 14" removable disks with capacities in the 2G- to 4G-byte range, data transfer rates of 3M bytes/s, and access times of less than 100 ms. In the middle range, products offering doublesided 12" removable disks with capacities of about 1G byte, data transfer rates of about 0.3M bytes/s, and access times of 150 to 250 ms are forthcoming. The lowest cost write-once optical storage peripherals, offering perhaps 200M bytes on a removable 51/4 " disk, will be introduced as market volume growth for optical data storage devices permits reduction of the manufacturing cost of certain key components, such as the R/W laser and associated optics.

The materials proposed for the data storage medium of write-once optical disks vary from thin metal films to organic media and multilayer structures. The optimal design and fabrication of write-once optical media are sufficiently complex that no consensus toward standardization has yet emerged. However, several proposed media appear to satisfy the basic requirements of sensitivity and playback signal to noise ratio, leaving defect density and media lifetime as the most contentious and critical issues. The initial price for these media is expected to range from \$50 to \$100/gigabyte.

Through the sixties and early seventies, optical data storage media research was almost exclusively directed toward those materials that offered hope of reversibility. This fact reflects the previous higher cost of conventional magnetic storage, whose erasability was an important factor for increasing its cost effectiveness. The initial research of reversible optical storage media was not completely successful, and during the seventies activity in this area was significantly reduced. In the past few years, a resurgence of interest in reversible magneto-optic data storage has taken place, largely fueled by new developments in magneto-optic media reported by certain Japanese companies.⁷

The new magneto-optic media are certainly at an earlier development stage than the write-once media; however, the cultural and software barriers—ie, access methods to a reversible magneto-optic memory are considerably smaller than those confronting write-once optical peripherals. As a result, once reversible optical memory is developed, its acceptance could be extremely rapid.

Optical data storage systems

The major functional elements within an optical data storage system consist of the laser source and associated R/W spot-forming optics (ie, the optical R/W head), electro-optical systems for the detection and correction of positional errors between the R/W spot and the data track, the R/W data channel encode/decode and error correction and control (ECC) electronics, the optical data storage medium or disk, and the drive unit itself. A schematic of the basic functional elements of an optical data storage system is shown in Fig 1. In this example, the R/W light source is a semiconductor diode laser.

In order to record the nonreturn to zero (NRZ) input data, the signal first passes through the ECC and modulation encoding circuitry to directly modulate the diode laser's light output. This high intensity modulated light output is collected by the optics, collimated, and directed via the tracking mirror to the focusing lens, which is mounted within a voice-coil type actuator. The focusing lens is similar in principle and optical quality to a high power microscope objective with numerical apertures between 0.45 and 0.65, and focuses the modulated record beam to a spot approximately one micron in diameter at the data storage medium plane. As the storage medium passes beneath the intensity modulated write spot, the stream of optical pulses causes a circular data track to be written. The data track consists of a string of physical "marks" burned in the storage medium by the recording pulses. In the simplest case of a metallic thin-film medium, the marks would take the form of micron-sized melted or ablated holes, and the presence or absence of the melted hole would represent a binary 1 or 0 stored along the data track. From this point of view, the optical disk is nothing more than an extremely high density punched card. If such a disk were expanded to yield the same storage density as a punched card, its diameter would approach one-quarter of a mile.

In order to read the stored data, a relatively low dc voltage is applied to the diode laser, resulting in a correspondingly low power and constant amplitude light continuous wave (CW) output. The read beam power level is deliberately chosen to be less than the storage medium's recording threshold to prevent degradation of the stored data track during readout. As before, the read beam is focused into a micron-sized read spot at the data storage medium. The presence of the optical marks along the data track results in an intensity modulation of the reflected component of the incident read beam. The intensity modulated reflected beam is collected by the focusing lens and directed via the tracking mirror to the guarter-wave plate and polarizing beam splitter optical components. The diode laser's output beam is plane-polarized, allowing the quarter-wave plate/polarizing beam splitter combination to separate the returning reflected component of the read beam and direct it to the photodetector elements. A semitransparent mirror divides the reflected read beam between the data photodetector and the position error sensing photodetector. In practice these two photodetectors can be combined into a single-quadrant type detector, making the beam division at the semitransparent mirror unnecessary.

A generic problem that must be resolved...is the positional accuracy of the R/W element....

The playback signal appears at the data photodetector output. After data detection, demodulation, and ECC, the playback data stream is directed to the optical memory system output. The modulation scheme adopted for optical data storage will probably be a runlength limited (RLL) code, such as the (2,7) code favored in current magnetic storage devices. In this case, the stored data are determined by the location of the optical marks along the data track—that is, they are dependent on timing rather than on the simple presence or absence of the marks-allowing more than one bit to be stored per optical mark. The optical analog of the magnetic transition or flux reversal-the optical transition-is the edge of the optical mark, since this is where optical properties of the data track change abruptly and the transition from high to low reflectivity occurs.

A generic problem that must be resolved by any data storage technology that proposes to store data at 10⁸ bits/cm² is the positional accuracy of the R/W element with respect to the truly microscopic dimensions of the data location (on record cycles) or stored data bit (on read cycles). Indeed, the practical employment of position sensing and correcting transducers and actuators is crucial in enabling significant advances beyond the data storage density levels available in today's magnetic storage devices. These issues were squarely confronted during the optical video disk's development in the late sixties through early seventies. A number of techniques were devised to optically detect both focus errors and radial tracking errors with a very high degree of precision-a small fraction of the R/W spot diameter.8,9 In brief, the consumer read only video disk systems, currently retailing for about \$500, contain servo control elements that maintain the read spot's plane of focus to

within approximately ± 1 micron of the data storage plane, and the read spot's radial position to within a few tenths of a micron of the data track center. This level of low cost positional accuracy is even more impressive considering that the data storage medium in this case is a low cost, mass-produced plastic disk that can be removed and replaced in the drive at whim.

In the R/W system shown in Fig 1, the positional error signals are generated from the portion of the reflected read beam that is directed to the position error photodetector array. The focus error signal is fed back via the focus servo circuitry to the voice-coil actuator where the focusing lens is mounted. The tolerable closed loop or residual focus error for R/W systems is significantly less than that for optical read only systems, since the error content of the recorded data is more sensitive to residual focus errors than is the detected read signal. As a consequence, R/W systems must have a residual focus error less than a few tenths of a micron, and the focus servo bandwidth must extend to a few kilohertz (unity gain) for disk rotational velocities of 30 revolutions/s.

The radial tracking error signal in Fig 1 is fed back from the position error photodetector via the tracking servo circuitry to the tracking mirror. An extremely small angular rotation of the tracking mirror causes a substantial radial displacement or deflection of the R/W spot. The minuscule rotational inertia of the tracking mirror permits relatively high gain (about 30 dB), high bandwidth radial tracking servos of a few kilohertz at unity gain. The existence of practical high performance optical track following servos is the most important factor in making possible removable optical storage media. Because of them, relatively large track eccentricities caused by centering errors after remounting the disk can be tolerated by the optical data storage system.

The shaded area in Fig 1 contains the optical R/W head components. Considerable progress has been made in integrating and miniaturizing such heads, by designing them around a semiconductor laser R/W source.1,10 Designs have been created¹¹ with external head dimensions reduced to a rectangular prism measuring 4 x 1 x 1 cm and with total mass reduced to 50 g.¹² Low total mass for the optical R/W head is an important factor in determining the optical storage system's access times. In addition, a low mass for the radial beam deflection elements minimizes the local seek time $(\pm 10 \text{ tracks},$ ≤ 1 ms) and maximizes the radial tracking servo bandwidth. Compact physical dimensions for the optical R/W head permits configurations with multiple heads/ data surface-which will somewhat lessen the access bottleneck associated with any data storage technology that stores 1G byte or more on a single disk surface.

None of the system components discussed so far are expected to critically affect plans for optical storage products. Rather, these issues largely concern clever engineering design aimed at the joint goals of cost effectiveness and reliability. There remain, however, important technical issues to be resolved regarding the R/W lasers and the storage media.

The availability of relatively high power, long-lived semiconductor lasers is not yet certain, particularly with respect to high performance systems operating with a R/W rate of about 3M bytes/s. In addition, it is generally accepted that the most critical element in the entire data storage system is the optical disk itself. Several proposed configurations for storage media have been promoted by their originators, but not enough objective testing of these media has taken place for a consensus of choice to even begin to emerge.

Lasers and media for optical data storage

In order for optical data storage to become widely accepted, the semiconductor diode laser must be employed as the R/W source. (See Fig 2.) The reasons are as obvious as they are compelling: extremely small size, light output that can be directly modulated, low input power requirements (< 0.5 W) and relatively high electro-optic conversion efficiency (about 10%), batch fabrication process leading to potential low cost, solid state device leading to potential long life (10,000 h), and reliability.

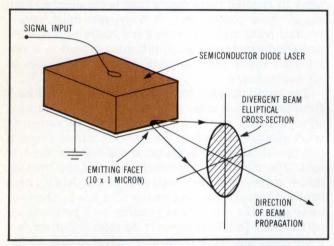


Fig 2 Output beam from semiconductor diode laser is strongly divergent due to diffraction that occurs at extremely small region of emitting facet. Slot-shaped geometry of emitting facet gives rise to divergent beam with an elliptical cross-section.

The recently introduced read only DAD systems incorporate relatively low power semiconductor lasers with a few milliwatts of output, CW, in the read head. Since the read head's optical efficiency can be 50% or greater, the disk's incident read beam power is approximately 1 mW or greater-more than adequate for such a read only application. The current sensitivity of write-once or erasable optical storage media is such that in order to write at a data rate of 3M bytes/s, a semiconductor laser rated for long-term (10,000 h) CW output in the 15- to 30-mW range is required. Such devices have recently become available in sample quantities, but they are still costly and largely unproven. This situation may result in those initial optical data storage products targeted for high performance applications having gas laser R/W sources to ensure reliability. However, R/W products designed for operation at reduced data rates (< 1Mbyte/s) will undoubtedly incorporate semiconductor lasers from the outset.

An important potential for optical data storage systems is the use of integrated arrays of semiconductor laser R/W sources. Although research in this area is still in its infancy, a recent paper describes the performance of an array with 16 diode lasers that can be modulated independently, each providing an output beam of up to 10 mW Cw.¹³ Using such an array, a single optical head could focus 16 independent R/W spots onto the optical data storage medium to provide a total channel capacity/head in excess of 25M bytes/s. There is presently no analog in magnetic data storage to the multiple channel R/W head designed around the integrated semiconductor laser array.

The design and fabrication of optical data storage media is seen as the single most critical factor in determining the ultimate usefulness of high density optical data storage. For data processing applications, this fact reflects the current status of all three media classifications read only, write once, and erasable—albeit to different degrees.

When the goal is to store media in densities of about 10^8 bits/cm², there are several critical issues that generically affect media of all types, not just optical storage media. These issues must be addressed and resolved independent of the particular data storage technology chosen.

Media resolution and noise is one such issue. At 10^8 bits/cm², each bit occupies only one square micron of the storage medium. The media must be capable of sustaining such microscopic marks, and also resolve their location to a somewhat higher degree of precision, as was previously discussed in connection with the use of RLL coding of the data. The resolution issue, and to a greater extent the media noise requirements, tend to favor vacuum deposited or plated media. Unless the particles are extremely small (≤ 10 nm) and uniformly dispersed, particulate media—optical or magnetic—may contribute excessive noise to the playback data signal.

Media microdefect density is another issue that must be considered. A media defect such as a pinhole or dust particle of one square micron will result in a single-bit error at storage densities of 10^8 bits/cm². The current residual or uncorrectable bit error rate (BER) requirement for data processing applications is 10^{-12} . In order to limit the ECC overhead to proportions of less than 25% of raw disk capacity, for example, the raw BER due to media microdefects should be about 10^{-5} or less. That is, one square centimeter of data storage surface should contain fewer than 1000 defects larger than approximately 0.5 microns; furthermore, this average must be maintained across the entire disk surface some 100 square inches for a 14" disk.

The ability to verify data during the recording cycle, and to immediately rewrite erroneous characters in specially reserved segments of the track, represents an important element in the overall strategy to control errors resulting from media microdefects. In optical R/W systems the direct read after write (DRAW) function is readily implemented using a secondary read only laser source, mounted within the optical head to form a CW read spot that trails the primary R/W spot by several microns. (See Fig 3.) Approximately 1 µs after the data are recorded, the trailing beam reads the data and verifies that they are correct. If a write error has occurred, the data are rerecorded at some alternate and predesignated area along the track. Using this DRAW approach, the residual BER after recording and verification can be reduced several orders of magnitude below that of the intrinsic media microdefect density.

Particularly in the area of write-once optical data storage media, the issue of media microdefect density and associated BER as a function of time looms large.

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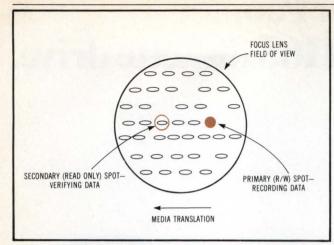


Fig 3 The principle of DRAW data verification. Focus lens is used to form two spots at surface of storage medium. Primary high power modulated beam records data. Secondary low power CW read beam trails recording beam and verifies accuracy of recorded data.

Since the main feature of this class of media is the permanence and nonalterability of the stored data, the selection of intrinsically stable materials presents a great scientific and technical challenge. Realtime testing of the proposed candidates has been limited to about two years, and although the results of accelerated aging tests are in some cases quite impressive, data of this kind are notoriously difficult to interpret quantitatively.

The high density data storage medium must play an additional key role. It must provide the necessary positional references-that is, embedded servo informationto close the loop on the positional error control system. In the case of optical data storage media this is quite straightforward in principle, and can be accomplished by embossing the optical disk substrate surface. It is thus possible to provide embedded positional reference information that can control the positional accuracy of the R/W spot in all the vertical (focus), radial (tracking), and longitudinal (timing) spatial dimensions, to a very high degree of accuracy and with no reduction of the user capacity of the disk. Formatting information such as sector and block addresses can also be included in the embossing procedure. This format information is represented by embossed data pits with $\lambda/8$ (about 100 nm) depth so that, in the detection channel, it can be readily distinguished from the user data.¹⁴

To maintain focus, servo control reference information is contained directly in the reflectance associated with the data storage media layer. The reference information necessary to control the radial tracking error is generated by embossing the entire disk substrate with a pattern of circular and concentric grooves, separated just enough to reduce intertrack crosstalk to acceptable levels—about -35 dB for a digital channel. The grooves' location is optically detectable regardless of the presence or absence of recorded data within the grooves. This approach allows random accessing and a high degree of radial position control during both the record and read cycles. For maximum sensitivity to offtrack positional errors, the groove depth is chosen to be about one-quarter of the R/W beam wavelength-about 200 nm with a diode laser R/W source. A further refinement of the embossed data groove, namely a small amplitude (approximately $\lambda/20$ or 40 nm) periodic modulation of the groove depth, provides an embedded timing signal that serves as a built-in reference for data detection clocking and drive motor speed control. The periodic groove depth modulation generates a small amplitude modulation of the detected playback data signal. The groove depth modulation's frequency is low compared to the data transfer rate, and is carefully selected to fall at a frequency that does not correspond to a component within the data signal spectrum.

Meeting the material requirements

Optical media have to deal not only with the generic issues of high density data storage media discussed thus far, but must also address some basic requirements of material properties that are unique to optical data storage. In view of the current status of high power semiconductor lasers, optical storage media must be sufficiently sensitive to permit optical marking or recording with an approximately 50-ns light pulse ($\lambda = 800$ nm) having a total power of 15 mW or less focused into a one square micron write spot. This level of sensitivity is required to make a recording rate of about 3M bytes/s with available diode lasers. A single recording pulse of these specifications thus delivers about 0.75 nJ of energy to the data-bit location, corresponding to a required media write sensitivity of 75 mJ/cm² or better at the diode laser wavelength. Several of the proposed media meet this requirement. Considered greater issues are media lifetime and fabrication cost.

The fundamental noise source in the optical storage system's data detection or playback channel is that due to the photon shot noise inherent in optical data sensing. In order to achieve an acceptable "soft" or read BER, the wideband playback signal to noise (S/N) ratio must exceed a well-defined level of about 20 dB, derived solely from the fundamental statistics of the data detection process. This S/N ratio requirement dictates a minimum power level for the CW read beam and, obviously, the optical media must be able to withstand indefinitely long or repetitive read cycles at this read spot intensity with no degradation in the stored information.

As long as a media damage threshold intensity exists for the R/W spot, and as long as this threshold is above the level at which the read spot yields the minimum required playback S/N ratio, then the optical storage media will be acceptable from the signal level's point of view. Thus, the basic issues of shot noise limited playback S/N ratio can, in principle, rule out the use of arbitrarily sensitive optical media. The proposed media are less sensitive by one or more orders of magnitude than the critical values for a 3M-byte/s data rate, leaving some room for improvement in sensitivity. With this in mind the proposed options for the materials and configuration of optical data disks can be discussed.

The materials system of the optical data disk¹⁵ in Fig 4 consists of three main, strongly interactive subsystems: the disk substrate, which provides the mechanical integrity, dimensional precision, and stability; the storage medium, where the data are recorded; and the encapsulation, which protects the storage medium from the degrading effects of ambient atmospheres and the accumulation of microscopic particulate matter. Overall disk configuration performance and suitability is limited by its weakest characteristic, and a sophisticated tradeoff between the desirable properties is needed to



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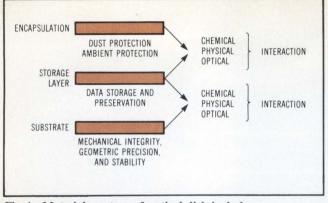


Fig 4 Materials system of optical disk includes encapsulation, data storage layer, and disk substrate.

arrive at the most practical solution. The performance of a given disk system is strongly dependent on the disk drive characteristics, a fact that requires the resolution of a further level of system optimization.

Glass was the first substrate that could be prepared with an adequately high surface quality to satisfy beginning of life BER requirements, but this quality was overshadowed by its relative expense, bulk, and fragility. Surface quality, ie, microdefect density of molded polymeric substrates, is inherently limited by the molding surface's quality. However, the ability to directly pattern the polymeric substrate surface with positional reference information provides a significant motivation to develop the required level of fabrication technique and control. Considerable experience, albeit for less stringent applications, is being gained by manufacturers of injection-molded consumer video disks. With experience and knowledge, the surface quality of fully patterned polymeric substrates should permit a microdefect density in the 10^{-5} to 10^{-6} range.

The aluminum disk substrate used in Winchester drives represents an intermediate cost alternative to glass and polymeric substrates, while offering excellent dimensional and chemical stability. Using a spin-coated surface layer can enhance the surface quality. However, the format and positional control information has to be "burned in" directly after disk fabrication—a timeconsuming and potentially costly procedure.

In practice, the media must also be protected from contamination. The main function of encapsulation is to keep particulate matter away from the plane of focus at the information storage layer in order to minimize its effect on playback signal quality, particularly BER. A second but equally desirable function of encapsulation

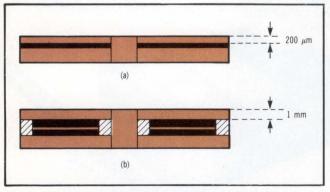


Fig 5 Direct encapsulation (a) and air-sandwich (b) schemes have been proposed for optical disk.

is to shield the storage layer from potentially corrosive materials, primarily water vapor, in the disk ambient.

The two major methods of optical data disk encapsulation are shown in Fig 5. Fig 5(a) shows the direct or in-contact approach in which a thin coat of a transparent polymer—about 200 μ m—is applied directly onto the storage layer surface. This approach protects the storage layer from its surroundings fairly well, particularly when the chosen polymer exhibits a low water vapor solubility. However, this is no substitute for using an intrinsically stable storage medium.

Fig 5(b) shows the air-sandwich approach¹⁶ in which the substrate and overcoat layer functions are combined. The air-sandwich configuration is essentially two optical disks bonded face to face with a small air gap maintained through spacer rings at the inner and outer diameters of the data storage band. Since both recording and playback functions take place through the substrate, the substrate disk must have excellent optical properties, in addition to its other chemical and mechanical requirements.

Practical difficulties of maintaining uniform thickness and optical quality of the substrate/overcoat disks make the air-sandwich approach most suited to middle or low performance applications that call for moderate data rates ($\leq 1M$ byte/s) and capacities ($\leq 1G$ byte/disk). The direct encapsulation approach, with its thinner overcoat requiring minimal mechanical integrity, is most suited to high end systems. However, in order to ensure adequate environmental protection of the data storage layer, the disk will probably be contained within a dust-proof cartridge.

Research into optical data storage media in the early sixties was, for the reasons already discussed, centered on the search for a viable, reversible data storage material. More vigorous research into write-once media, begun in the early seventies, has since represented the major thrust of research and development in the field. Recent developments in reversible magneto-optic materials, however, have resulted in a strong revival of interest in erasable optical storage.

Candidates for a data storage material

In write-once optical data storage media, the simplest data storage layer configuration consists of a single light-absorptive thin film about 30 nm thick deposited directly onto the substrate disk's surface. The optical marks that represent the stored data consist of micronsized holes formed by the localized ablation of the thinfilm layer [see Fig 6(a)]. The melted holes' reflectivity is less than that of the undisturbed regions of the disk, resulting in the modulation of the reflected component of the incident read spot. Tellurium based alloy materials^{17,18} appear to offer the best combination of properties including sensitivity adequate for diode laser R/W source implementation, playback signal S/N ratio and BER adequate for digital applications, and an archival lifetime estimated at 10 years or more. Tellurium based media are most often combined with the air-sandwich configuration.

Multilayer thin-film antireflective structures have also been proposed,¹⁹ as in the two examples shown in Fig 6(b) and (c). The advantages of these structures are twofold. First, the medium's low reflectivity allows a high fraction of the recording beam energy to couple

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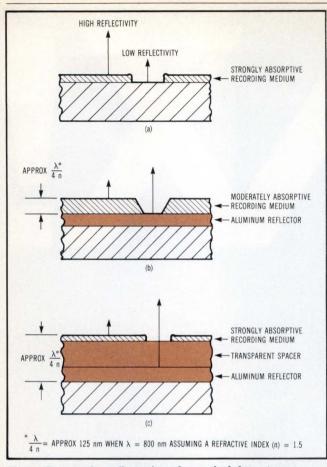


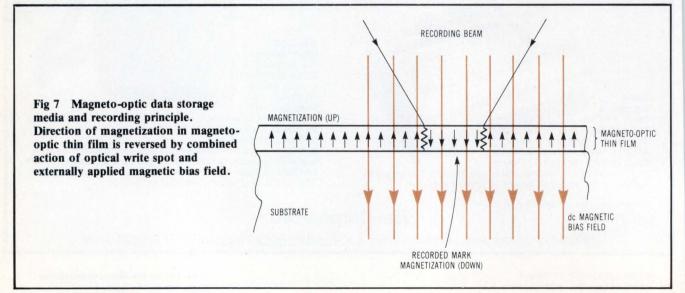
Fig 6 Proposed configurations for optical data storage medium. Single layer (a) offers simplicity; antireflection bilayer (b) and trilayer (c) structures broaden range of useful materials and recording mechanisms.

with the active layer, resulting in higher sensitivity. Second, since the structure is essentially "tuned" to capture the incident R/W beam, a variety of recording mechanisms can be employed to disrupt the optics of the tuning and yield a high reflectivity for the optical mark, leading to a high playback signal amplitude.^{20,21} The antireflection structures' active component can be an organic material such as a dye in the binder, or a metallic material. Recording mechanisms include simple melting or evaporation, bubble formation, or more subtle structural changes in the active layer's atomic configuration. The general characteristics of antireflection structures favor their use in high performance optical data storage systems, although their adoption in more moderate performance systems is also possible. As discussed previously, the most critical issues in the development of practical write-once optical storage media are those of lifetime and user media cost in cents/megabyte.

Magneto-optic materials are the leading candidates in the development of erasable, reusable optical data storage media. In magneto-optic media (Fig 7) the thin film is first uniformly magnetized perpendicular to the disk substrate plane (the up direction in Fig 7). In this respect magneto-optic media have strong similarities to the perpendicular magnetic media currently under development for use in conventional, that is, magneto-inductive, magnetic data storage. On recording, an external dc magnetic bias field is applied to the data storage layer, and the temperature rise due to the localized absorption of the optical write spot energy triggers a reversal to the down direction in the magnetization vector of the micron-sized exposed mark. The optical mark in magneto-optic media is very similar to the bubbles created to represent the data in magnetic bubble storage devices.

On playback, the presence of the reversed magnetization mark is detected by its effect on the polarization angle of the reflected component of the incident planepolarized read beam. Somewhat more complex arrangements for the data photodetector are required to implement this scheme. To erase, the data track is reexposed to the high power write spot, this time with the external dc magnetic bias field applied in the opposite direction, and the magnetization of the magnetic domain is returned to its initial direction. The erasure mode for a magneto-optic memory system will probably be sequential rather than direct overwrite. The existing data in the block to be modified are first erased; then, the updated data can be recorded on the next disk revolution.

Since the magneto-optic effects upon which the data detection scheme is based are relatively small, the playback S/N ratio for such media has always been the most critical parameter. Recent developments in both



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materials and the use of antireflection trilayer structures have produced some very encouraging results,^{22,23} although it seems that magneto-optic memories will offer somewhat reduced data rates (about 1M byte/s) and capacities (about 1G byte) compared to their writeonce counterparts. Recent reports of development prototypes for magneto-optic disk memories claim a data rate of 0.5M bytes/s and a 5¹/₄" disk capacity of 200M bytes. In this instance the magneto-optic medium was described as being an amorphous magnetic film integrated into the encapsulated bilayer antireflection structure on a glass substrate disk.

Issues that must be resolved before the introduction of magneto-optic data storage media include all those discussed in connection with archival write-once media. In addition, it is probable that a higher degree of disk fabrication process control will be necessary, suggesting a somewhat higher cost of magneto-optic media in cents/megabyte.

Optical mass storage systems

The first wave of optical data storage products will use the archival write-once optical disk. A significant amount of revision and further development of system software, primarily the access methods, is needed before such devices can achieve widespread use. The utility of write-once data storage media depends entirely on the archival lifetime and the cost of stored data/megabyte. Some argue that if truly archival storage media were cheap enough, then the most effective strategy for data storage would, in fact, use write-once nonalterable data storage media.²⁴ With this method the entire history of revisions of a given data file is maintained and available for the user's review.

Optical data storage media will certainly not be free. However, its extremely low cost (\leq \$0.10/megabyte), coupled with disk-like rapid random access (\leq 100 ms), makes archival write-once optical storage technology quite appropriate for applications involving very large data bases (\geq 1 terabyte) that require infrequent changes or updates. For these applications it is possible to configure optical mass storage systems (MSS) with online capacities of 1 or more terabyte. Offline data capacities of 100 or more terabytes are also feasible. The volumetric storage density and unit cost of system modules and media should provide an attractive alternative to current MSS configurations based on magnetic disk and tape media.

Fig 8 shows one possible configuration of an optical MSS, backed up by a very large capacity disk library. The MSS contains a controller and intelligent database management processor. In view of the enormous volume of data it is important that the logical control of the placement of records on disks, and disks into racks or into the library be performed to as large a degree as possible at the MSS level, rather than at the host processor level. The first level of MSS storage hierarchy takes the form of one to five optical disk drives. Each drive consists of a single, double-sided disk with 10G-byte capacity and less than 100-ms access time. The second level of storage, still within the MSS unit, takes the form of one to five disk racks, each holding 128 disks with about a 1-terabyte data capacity. A single disk rack's dimensions could be 40 x 40 x 125 cm. The access mechanism required to select a disk from a rack

and mount it on a drive is similar to that of a jukebox, with a possible disk mount/demount access time of 5 s or less.^{25,26} The tertiary level of data storage is represented by the disk library—a large ensemble of disk racks placed on shelves—that resembles existing magnetic tape libraries. A single corridor 9' (3-m) wide could contain the automated disk rack retrieval mechanism and allow access to two walls of disk racks. Assuming that four rows of racks are mounted on each wall, such a corridor would offer a data storage capacity of about 20 terabytes/10' (3.3 m) of corridor length.

Prototype optical MSS jukeboxes containing a single optical drive and a single disk rack are being developed and could become available soon after the introduction of the single-disk optical data storage devices.

Prospects for optical storage

Optical data storage is the most advanced technology in terms of read only or archival write-once data storage at densities in the 10^8 bits/cm² range. During the next few years optical storage products of this type are expected to be commercially introduced by several manufacturers. The introduction of optical MSS and reversible optical memories could follow in a relatively short time. Read only and archival write-once optical disk systems represent new opportunities to increase machine readable digital data storage applications into areas that are not cost effective with existing data storage technology. The storage of digitized images and office documents is one example. In short, reversible optical data storage systems will offer strong competition to magnetic data storage of the next decade.

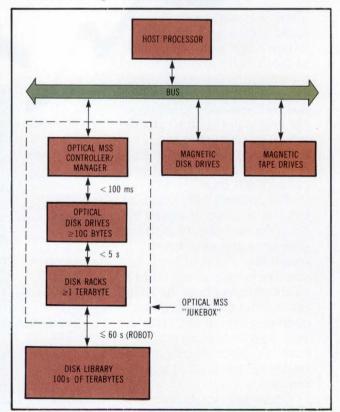


Fig 8 Possible configuration for an optical MSS and disk library with application to extremely large data bases. Library access could be manual (offline), or automated (similar in principle to current automated tape library design).

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146 COMPUTER DESIGN/January 1983

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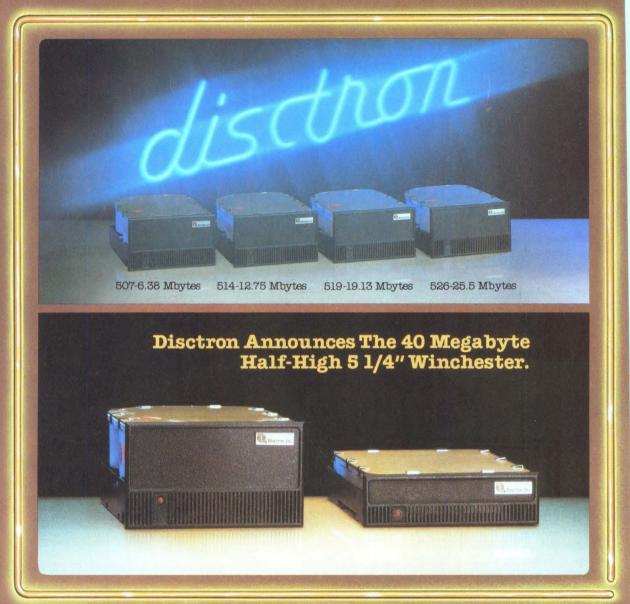
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ISSCC '83 International Solid State Circuits Conference

Sheraton Centre Hotel New York City, New York February 23 to 25, 1983

Long the conference to watch for vital signs of progress in the computer industry, ISSCC gives semiconductor manufacturers worldwide a forum in which to compare notes on their latest prototypes, as well as to debate untested ideas. At this conference as at no other, semiconductor researchers put their ideas on the line to vie for a place in the solid state circuit lexicon—the core of the computer industry.

Industry analysts predict that by the mid-1980s, CMOS will be the preferred MOS technology. Synthesizing advances in logic and memory design, moreover, CMOS is popping up more frequently alongside traditional approaches to both analog and digital ICs. The shift to CMOS will gain momentum—in great part from CMOS's key advantage of low power dissipation-as circuit integration levels spiral upward. However, manufacturers will have to confront a range of production issues in CMOS that have already been resolved for NMOS. Further fragmentation in CMOS technology is imminent as new approaches are developed for isolation, interconnection layers, and soft error immunity.

Memory design continues to be the proving ground for many developments in semiconductor and processing technologies, and high bit-density, fast-access CMOS RAMS are nearing center stage. Mitsubishi Electric's 8k x 8 n-well CMOS static RAM, for instance, slices access time to 50 ns while dissipating 100 mW. A divided word line architecture reduces column current and word line delay. On the processing side, designers will explain their choice of molybdenum silicide as a substitute for the second polysilicon layer. Then Intel will present a 64k dynamic RAM with 70-ns access time and 150-mW power dissipation. The chip is made via n-well CMOS technology with 137-µm², doublepolysilicon p-channel memory cells.

CMOS memory is also keeping abreast of the trend to put more functionality onchip. Nippon Electric Co will report on a 64k CMOS RAM with auto data retention mode, which is made via a double-level aluminum process technology. A split power control technique reduces active power in this 10-mW battery-backup device; access time is 80 ns.



George E. Pake Keynote Speaker



Lewis M. Terman Program Chairman

Nonvolatile memory is getting into the CMOS act with a 64k, n-well EPROM. Developed jointly by Signetics and Philips Research Lab, this chip has an 80-ns typical access time with $1-\mu W$ quiescent power dissipation. Onchip test circuits cut testing and reliability screening times.

CMOS has not cornered the memory market yet, however. ISSCC '83 will bring out a bumper crop of faster, denser circuits, and 256k dynamic RAMS may be the pick of the harvest. Nippon Electric has applied its double-level aluminum processing to a 256k dynamic RAM with 90-ns RAS access. Design rules for the 34-mm² chip are a lean 1.3 μ m, and effective oxide thickness is 160 Å in a 66.5- μ m² cell area.

Mitsubishi Electric is keeping pace with a 100-ns, 256k dynamic RAM that operates in both page and nibble mode—distinguished internally by CAS precharge time. The chip is immune to voltage bumping and incorporates laser programmable redundancy. Motorola Semiconductor will talk about its 90-ns, 256k dynamic RAM, which operates in a 15-ns, 4-bit nibble mode. Shared sense amplifiers, booted word lines, active restore, and vertical process scaling to improve alpha immunity will be detailed.

Toshiba chose molybdenum silicide gate transistors for its 256k MOS dynamic RAM. Dividing the chip into eight blocks gives 34-ns \overline{CAC} access, 94-ns \overline{RAC} , and 170-mW active power. Fujitsu adopted triple-polysilicon processing and 2.5- μ m layout rules for its 256k dynamic RAM, which offers nibble mode and \overline{CAS} before \overline{RAS} refresh. Die size for this one is 34.1 mm².

Sacrificed density when cutting access time continues to be a dilemma for memory designers, but Intel is making inroads with an 80-ns, 64k dynamic NMOS RAM that boasts a 65-ns fast-page-mode cycle time. The chip incorporates a conventional $77 \cdot \mu m^2$, 1-transistor cell with 150-Å capacitor oxide and double field oxidation to reduce "bird's beak." Across the ocean, IBM Labs in Boeblingen, Germany is developing an experimental 8k x 8 I²L/MTL static RAM with 25-ns access and 50-ns cycle times.

The chips need less than 1 μ W for data retention, and dissipate 8 mW standby and 210 mW selected.

Two ECL compatible, bipolar static RAMs are queuing up for the 16k league. Hitachi's 16-ns, 150-mW chip is made using oxide isolated polysilicon walled emitter transistors. Cell size is 569 μ m²; die size is 16.4-mm². Fujitsu will describe its 15-ns, 700-mW device, which incorporates a 750- μ m² active pnp load cell. It is made using a 21.4-mm² die.

For designers bent on speed first, it will be hard to beat Bell Labs' 5-ns, 4k NMOS static RAM, which dissipates 400 mW. Scientists will report on bootstrapped word drivers, per-column buffers, and 0.5- to 0.8- μ m channel lengths formed with single-level TaSi/n+ polysilicon. The chip also carries a 120- μ m², 6-transistor depletion-mode load cell.

CMOS and bipolar VLSIS can already fit tens of thousands of circuits on a chip, and with improved system architecture and software engineering, designers hope to put a million active elements onto that same space. An ad hoc discussion on logjams that keep designers from reaching the theoretical limits will top off a session on working VLSIS. Conference goers will join industry leaders in thrashing out design tradeoffs between scaling and reliability, circuit complexity and design tools/equipment, voltage thresholds, and development costs.

Juggling numbers like that demands flexibility, and configurable VLSI circuits promise to meet that need. CMOS leads the pack for such applications, because its lower (ie, than NMOS) power dissipation simplifies cooling and packaging problems while offering designers transistors of both polarities on the same chip. Hitachi is taking a modular approach to building a variable-sized memory for 10k to 20k CMOS VLSI chips. RAM and ROM sizes can be altered to facilitate custom high speed and automated design. In addition, Nippon Electric Co is making headway on a 20-ns, 4368-gate array with 2304 bits of configurable memory fabricated using $1.5-\mu m$ design rules. The memory's word and bit configurations can be altered to increase the gate array function.

Bipolar master slice LSI will be in attendance, with a 5000-gate array from NTT Musashino Electrical Communication Lab and a 4-level, 10,000-gate configuration from IBM with customized onchip logic array. NTT's circuit is fully ECL compatible and has a loaded gate delay of only 500 ps, with power dissipation under 6 W. A 1.5- μ m design rule bipolar process using three metalization levels is behind this chip. In digital ICs where flat-out performance is the top design criterion, engineers often turn to GaAs technology. However, despite their gigahertz clock rates, GaAs digital ICs have yet to match silicon IC functional complexity. At ISSCC '83, leading manufacturers will debate nearterm applications for GaAs digital ICs, arguing both sides of a crucial system design question: Can the high speed system segments be divided into a few medium scale functions, or must the entire system be constructed in GaAs on one chip?

Meanwhile, an assortment of prototypes for high speed GaAs digital ICS will characterize the range of present solutions, culminating with two 1k GaAs static RAMS. One, from Fujitsu, uses self-aligned tungsten silicide gates and ion implantation, and reports a 4-ns access time with 58-mW power dissipation. The other, from NTT Musashino Electrical Communication Lab, uses a self-aligned MESFET and low temperature, 2-level IC technology. This E/D DCFL 1k device runs a 2.6-ns access time with 291-mW power dissipation.

Other highlights of ISSCC '83 will include a session on high speed microprocessors. The computer-on-a-chip has come a long way since Intel's 4004, and this year's additions reinforce the trend toward dedicated functions. One, from National Semiconductor (Israel), is a virtual memory management chip with program debugging support for a 32-bit microprocessor. The 20k-transistor NMOS chip accesses memory based translation tables in under 100 ns, and maintains 32 translation entries in an associative cache memory.

Intel's 16-bit memory management and protection chip whizzes through 1.5M instructions/s. This microprocessor packs 120k transistors onto 334 x 340 mil², and runs a 242.5-ns data access at pin end by an 8-MHz clock. Another 16-bit chip, reported by Fairchild Advanced Research and Development Labs, fits 160k transistors onto an I³L chip measuring 128,000 mil². Fairchild has picked a 20-MHz clock to time 200-ns adds and $1.85-\mu$ s multiplies. The chip also handles floating point instructions, 16 interrupt levels, and 2 timers. Last but not least, IBM Federal System Div will detail its 55k-transistor, NMOS microprogrammable microprocessor. The 7.2-mm², 16-bit silicon-gate chip uses 80-bit microinstructions and simulates several computers at up to 900k instructions/s.

-Deb Highberger, Associate Editor

For registration information, contact Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193.

ISSCC '83

Technical Program Excerpts*

Session 1: Telecommunication Circuits Wed 9 to 11:45 am, Imperial Ballroom A

Chairman: H. E. Mussman, Bell Labs

- 1/1 "A Single-Chip Telephone Circuit"
- M. F. Akram and W. D. Pace, Motorola, Inc
- 1/2 "A Subscriber Line Interface Circuit with an Internal Switching Regulator"
 - R. J. Apfel, K. E. Fields, J. C. Kuklewicz, and
 - M. L. Stephens, Advanced Micro Devices
- 1/3 "A 2-Chip Subscriber Line Interface Circuit with Ringing"
- P. J. Meza, D. P. Laude, R. C. Strawbrich, and R. M. Sirsi, Harris Semiconductor
- 1/4 "A CMOS SLIC with an Automatic Balancing Hybrid"
 M. Shibukawa, E. Amada, Y. Hasegawa, and
 H. Shirasu, Hitachi Central Research Lab; and
 - F. Fujii and K. Yasunari, Hitachi Device Development
- 1/5 "A Fully Adaptive Transversal Canceler and Equalizer Chip"
 - E. J. Swanson, R. J. Starke, G. F. Gross, K. H. Olson,
 - C. J. Waldron, R. A. Copeland, S. A. Surek,
 - R. J. Ribble, and A. J. Vera, Bell Labs

Session 2: High Speed Microprocessors Wed 9 to 11:45 am, Imperial Ballroom B

- Chairman: D. A. Patterson, University of California, Berkeley
- 2/1 "A 16-Bit Microprocessor with Onchip Memory Protection"

G. Louie, T. Ho, J. Slager, and D. Vannier, Intel Corp; and L. Gindraux, Daisy Corp

2/2 "A Virtual Memory Management Chip with Program Debugging Support"

Y. Lavi and A. Mizrahi, National Semiconductor

2/3 "A 16-Bit Microprocessor for Realtime Applications"

H. Hingarh, S. Mor, M. Vora, D. Wilnai, and T. Longo, Fairchild Advanced Research and Development Labs

2/4 "A 55k-Transistor NMOS Microprogrammable Microprocessor" В. Grant, IBM Federal System Div

Session 3: GaAs High Speed Digital ICs Wed 9 to 11:45 am, Royal Ballroom

Chairman: L. J. Nevin, Hewlett-Packard Co 3/1 "GaAs E/D Logic Circuits"

- M. R. Namordi and W. A. White, Texas Instruments, Inc
- 3/2 "Depletion-Type GaAs MSI 32-Bit Adder"
 R. Yamamoto, A. Higashisaka, S. Asai, T. Tsuji,
 Y. Takayama, and S. Yano, Nippon Electric Microelectronics Research Labs, Computer Engineering Div

3/3 "A 4-GHz, 25-mW GaAs IC Using Source-Coupled FET Logic"

A. Shimano, S. Katsu, S. Nambu, and G. Kano, Matsushita Electronics Corp

 3/4 "A GaAs 1k Static RAM Using Tungsten Silicide Gate, Self-Aligned Technology"
 N. Yokoyama, T. Ohnishi, H. Onodera, T. Shinoki,

A. Shibatomi, and H. Ishikawa, Fujitsu Labs, Ltd

 3/5 "GaAs 1k-Bit Static RAM Using Self-Aligned FET Technology"
 K. Asai, K. Kurumada, M. Hirayama, and M. Ohmori,

NTT Musashino Electrical Communication Lab

Session 5: Keynote Address

Wed 2:05 to 2:45 pm, Imperial and Royal Ballrooms

- Chairman: L. M. Terman, IBM Research Center
- "Long-Range Research Investments for a Semiconductor Systems Future"
 - G. E. Pake, Xerox Corp

Session 6: CMOS Memory

Wed 3:30 to 6 pm, Imperial Ballroom A

Chairman: J. Lohstroh, Philips Research Labs

- 6/1 "A 70-ns, High Density 64k cmos Dynamic RAM"
 R. Chwang, M. Choi, D. Creek, S. Stern, P. Pelley,
 J. Schutz, M. Bohr, P. Warkentin, and K. Yu, Intel Corp.
- 6/2 "A 64k-Bit, Full-CMOS RAM with Divided Word-Line Structure"
 - M. Yoshimoto, K. Anami, H. Shinohara, T. Yoshihara, H. Takagi, S. Nagao, S. Kayano, and T. Nakano, Mitsubishi Electric Corp
- 6/3 "A Battery Backup 64k CMOS RAM with Double-Level Aluminum Technology"

T. Watanabe, M. Hayashi, I. Sasaki, Y. Akatsuka,

- T. Tsujide, H. Yamamoto, O. Kudoh, S. Takahashi,
- and T. Hara, Nippon Electric Co, Ltd
- 6/4 "A Sub 100-ns, Static 64k смоз EPROM with Onchip Test Functions"

M. W. Knecht, P. Keshtbod, and G. H. Simmons, Signetics Corp; and M. H. Manley, Philips Research Labs/Signetics Corp

Session 7: Circuits for Digital Communications

Wed 3:30 to 6 pm, Imperial Ballroom B

Chairman: G. L. Baldwin, Hewlett-Packard

- 7/1 "A Single-Chip NMOS Ethernet Controller" A. G. Bell and G. Borriello, Xerox Research Center
- 7/2 "A CMOS Adaptive Delta Modulation CODEC Chip for PABX Applications"

R. Gregorian and G. Wegner, American Microsystems, Inc; and S. D. Flanagan and J. G. Ford, United Technologies/Lexar

7/3 "A cmos Switched Capacitor Variable Line Equalizer"

T. Suzuki, H. Takatori, and H. Shirasu, Hitachi Central Research Lab; N. Kunimi, Hitachi Device Development Center; and M. Ogawa, Hitachi Totsuka Works

^{*}Technical Program sessions are subject to last minute changes.

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ISSCC '83

- 7/4 "Peripheral Board Controller for Digital Exchange Systems"
 - L. Lerach, G. Geiger, and M. Strafner, Siemens AG

Session 8: Modeling and Technology Wed 3:30 to 6 pm, Royal Baliroom

- Chairman: R. D. Baertsch, General Electric Corporate Research
- 8/1 "Inverter Chain Test Structure for Yield Improvement and Projection" Н. Н. Berger, івм Labs
- 8/2 "Modeling Redundancy in 64k- to 16M-Bit DRAMS" С. Н. Stapper, IBM Corp
- 8/3 "Correlating the Channel, Substrate, Gate, and Minority-Carrier Currents in MOSFETS"
 C. Hu, S. Tam, F. C. Hsu, and R. S. Muller, University of California, Berkeley; and P. Ko, Bell Labs
- 8/4 "An 18-V, Double-Level Poly CMOS Technology for Nonvolatile Memory and Linear Applications"
 R. A. Haken, I. A. Groves, C. S. Wang, W. E. Feger, D. B. Scott, Y. C. See, and R. D. Davies, Texas
 - Instruments, Inc

Informal Discussion: Near-Term Applications for GaAs Digital ICs

Wed 3:30 to 6 pm, Versailles Ballroom-Versailles Terrace

- Moderator: D. H. Phillips, Aerospace Corp
- Panel: F. A. Blum, Gigabit Logic; B. K. Gilbert, Mayo Clinic; C. F. Krumm, Hughes Research Labs; G. Nuzillat, Thomson-csF; T. M. Reeder, Tektronix, Inc; G. A. Works, Texas Instruments, Inc; and N. Yokoyama, Fujitsu Labs

Informal Discussion: Joint R and D—Current and Future Plans

Wed 8 pm, Imperial Ballroom-Royal Ballroom

Moderator: G. A. Pake, Xerox Corp

Panel: G. E. Moore, Intel Corp; W. J. Sanders III, Advanced Micro Devices; E. Bloch, IBM Corp; J. W. Lacy, Control Data Corp; and J. D. Meindl, Stanford University

Session 9: Fast RAMs

Thurs 9 am to 12:15 pm, Imperial Ballroom A

- Chairman: W. W. Herndon, Fairchild Research 9/1 "An 80-ns, 64k DRAM"
- A. Mohsen, P. Madland, C. Simonsen, E. Hamdy, G. King, J. McCollum, and A. Wood, Intel Corp
- 9/2 "A 5-ns, 4k x 1 NMOS Static RAM" K. J. O'Connor and R. A. Kushner, Bell Labs
- 9/3 "A 16-ns, 16k Bipolar RAM"
 Y. Kato, M. Odaka, and M. Ogiue, Hitachi Device Development Center; and H. Miwa and K. Matsumura, Hitachi Microcomputer Engineering, Ltd
- 9/4 "A 15-ns, 16k-Bit ECL RAM with a pnp Load Cell" K. Toyoda, M. Tanaka, H. Isogai, C. Ono, Y. Kawabe, and H. Goto, Fujitsu, Ltd

9/5 "A 25-ns, 8k x 8-Bit Static MTL/I²L RAM" S. K. Wiedmann and K. Heuber, IBM Labs

Session 10: Speech Recognition Thurs 9 am to 12:15 pm, Imperial Ballroom B

Chairman: T. Foxall, Pacific Microcircuits, Ltd

- 10/1 "An Architecture for a Speech and Recognition System"
 - M. Lowy, H. Murveit, D. M. Mintz, and R. W. Brodersen, University of California, Berkeley
- 10/2 "A Speech Recognition Processor"
 T. Iwata, H. Ishizuka, T. Hoshi, M. Watari,
 Y. Kawakami, and M. Mizuno, Nippon Electric Co, Ltd
- 10/3 "A Monolithic Data Acquisition Channel" R. K. Hester, K. S. Tan, and C. R. Hewes, Texas Instruments, Inc
- 10/4 "A 2-μ NMOS 256-Point Discrete Fourier Transform Processor"
 J. L. van Meerbergen and F. J. van Wyk, Philips Research Labs
- 10/5 "A Switched-Capacitor Adaptive Lattice Filter"
 R. D. Fellman and R. W. Brodersen, University of California, Berkeley

Session 11: Design Techniques Thurs 9 am to 12:15 pm, Royal Ballroom

- Chairman: A. R. Newton, University of California, Berkeley
- 11/1 "Automatically Generated Area, Power, and Delay Optimized ALUS"
- R. K. Montoye and P. W. Cook, IBM Research Center 11/2 "A Circuit Design Methodology for cmos
- Microcomputer LSIS" H. Nakamura and H. Maejima, Hitachi Research Lab; and T. Kihara, Hitachi, Ltd
- 11/3 "An Interactive, Integrated, Hierarchical CAD System for Microprocessor Design"
 P. J. Cavill, H. M. Chesney, A. Fuge, G. Harriman, J. Jakson, and R. Shepherd, INMOS, Ltd
- 11/4 "A Fault-Tolerant моз Lsi for Train Controller Applications"

K. Tashiro, M. Ueno, and I. Masuda, Hitachi Research Lab; and S. Oomura and M. Yasunami, Hitachi Mito Works

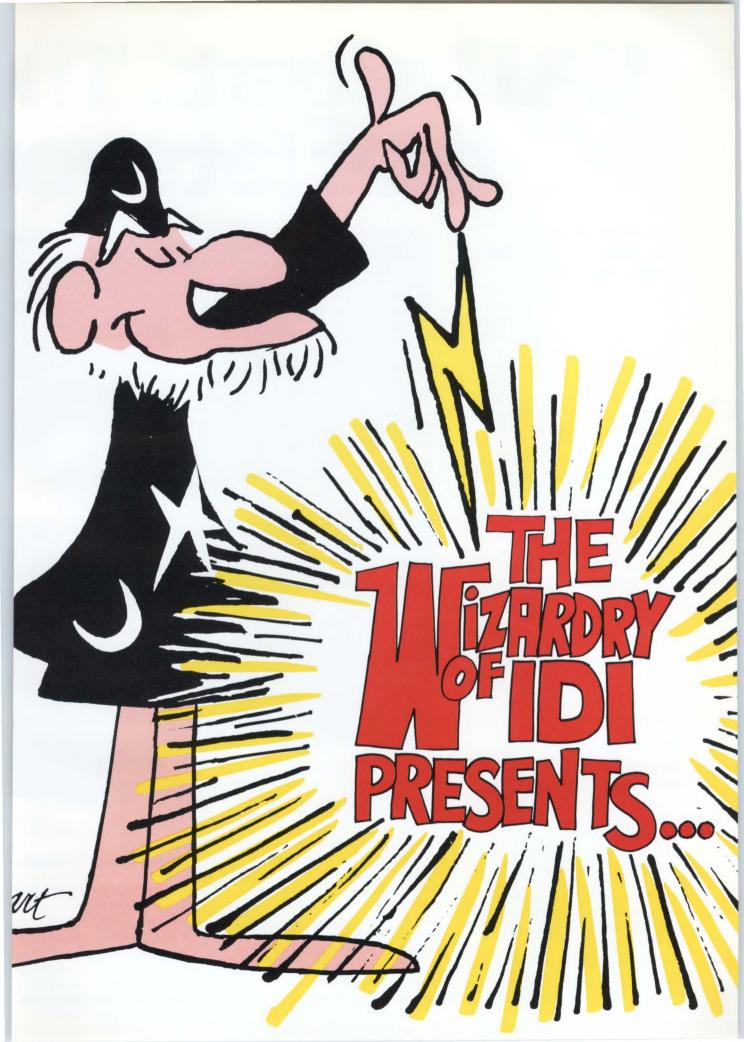
Informal Discussion: Wideband Microwave/ Millimeter Wave Solid-State Amplifiers

Thurs 9 am to 12:15 pm, Versailles Ballroom-Versailles Terrace

Moderator: H. Huang, RCA Labs

Panel: Y. Ayasli, Raytheon Research; J. Kukielka, Avantek; S. Nambu, Matsushita Electronics Corp; J. Obregon, Laboratoire d'Electronique; F. Sechi, RCA Labs; and H. Q. Tserng, Texas Instruments, Inc

(continued on page 159)



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Since 1975, IDI has been developing graphics and application software packages highly regarded for ease of use and operational effectiveness. Complete programs for *Technical Publishing*, AE&C, Mechanical and Electrical Design Drafting have been integrated into CADalyst, and are ready to start working immediately.

CADalyst supplies new operating system support to these industry-accepted packages, enhancing their performance and opening the way to new applications previously reserved for supermini and mainframe computers.

Unlimited system flexibility with no degradation of performance.

INET Local Area Networking inter-unit communication allows data and drawing exchange throughout a distributed network of CADalyst systems.

Local Peripheral Support – peripherals such as plotters, printers and telecommunications equipment are supported with no central computer required.

Host Computer Compatible – interconnection with a mainframe enables centralization of many engineering and database management functions at a single location.

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Best of all, IDI's relationship with CADalyst owners doesn't end in the start-up stage. We offer ongoing training programs, hardware support, special applications assistance, periodic software updates, a 24 hour—7 day Customer Response Center with a toll free number, and we strongly encourage continous customer feedback.

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Session 12: Gate and Programmable Logic Arrays

Thurs 1:30 to 5 pm, Imperial Ballroom A

- Chairman: H. Borkan, Electronic Technology and Devices Lab
- 12/1 "A 20-ns смоs Functional Gate Array with Configurable Memory"

T. Sano, S. Matsukuma, Y. Ohuchi, O. Kudo, H. Yamamoto, and K. Hashimoto, Nippon Electric Co, Ltd

12/2 "Building Block Approach and Variable-Size Memory for CMOS VLSIS"

T. Obha, K. Koioe, K. Ikuzaki, and M. Fujita, Hitachi Device Development Center; A. Masaki, Hitachi Central Research Lab; and M. Kato and S. Murata, Hitachi Kanagawa Works

- 12/3 "A 5000-Gate Bipolar Master Slice Lsi with 500-ps Loaded Gate Delay"
 M. Suzuki, S. Horiguchi, and T. Sudo, NTT Musashino Electrical Communication Lab
- 12/4 "A 10,000-Gate Bipolar VLSI Master Slice Utilizing Four Levels of Metal"
 S. Brenner, T. A. Bartush, D. J. Swietek, D. C. Banker,

F. J. Crispi, D. J. Delotto, D. L. Merrill, J. P. Norsworthy, M-N. Shen, and C. D. Waggoner, IBM Corp

12/5 "A 4-ns Laser-Customized PLA with Preprogram Test Capability"

D. W. Still, Honeywell Information Systems, Inc.

Session 13: Nonvolatile Memory Thurs 1:30 to 5 pm, Imperial Ballroom B

Chairman: R. Pashley, Intel Corp

- 13/1 "A 200-ns, 256k нмоз II ЕРКОМ"
- M. F. van Buskirk, W. Fisher, M. Holler, and G. Korsh, Intel Corp
- 13/2 "A 5-V Only, 64k EEPROM with Internal Program/ Erase Control"
 - A. Lancaster, R. Johnstone, J. Chrutz, G. Talbot, and D. Wooten, INMOS Corp
- 13/3 "A 5-V Only, ε²PROM Using 1.5-μ Lithography"
 V. K. Dham, K. H. Gudger, Y. W. Hu, S. Nieh, J. Olund, and D. Oto, Intel Corp
- 13/4 "A 5-V Only, 32k EEPROM" D. D. Donaldson, E. H. Honnigford, and L. J. Toth, NCR Corp
- 13/5 "A 5-V Only, 4k Nonvolatile Static RAM" N. Becker, V. K. Dham, Y. W. Hu, D. Lee, A. Schlafly, and J. Skupnjak, Intel Corp
- 13/6 "A 40-ns Junction-Shorting PROM"
 T. Fukushima, K. Ueno, Y. Matsuzaki, and K. Tanaka, Fujitsu, Ltd, Memory-Bipolar Divs

Session 14: Data Acquisition and Conversion Thurs 1:30 to 5 pm, Royal Ballroom

Chairman: J. McCreary, Intel Corp

- 14/1 "An 8-Bit/50-ns Monolithic ADC with Internal Sample and Hold"
 - R. A. Blauschild, Linear Design, Inc

14/2 "A Monolithic Sample and Hold Amplifier for Digital Audio"

R. J. van de Plassche and H. J. Schouwenaars, Philips Research Labs

- 14/3 "A Monolithic 12-Bit System DAC" B. Harvey, Advanced Micro Devices
- 14/4 "A Trimless 14-Bit/20-μs Dual-Channel ADC for PCM Audio"
 - S. Sugawara, M. Ishibe, S-I. Majima, S. Komatsu, and H. Yamada, Toshiba Research and Development Center
- 14/5 "A 16-Bit Monolithic DAC with Voltage Output" J. R. Naylor, Burr-Brown Research Corp
- 14/6 "A 60-ns Glitch-Free NMOS DAC" V. W-K. Shen and D. A. Hodges, University of California, Berkeley

Session 15: Microwave Circuits Thurs 1:30 to 5 pm, Versailles Ballroom-Versailles Terrace

Chairman: A. F. Podell, Podell Assocs

- 15/1 "A 2.2-dB NF, 30- to 1700-MHz Feedback Amplifier"
 - N. Nishiuma, S. Katsu, S. Nambu, M. Hagio, and
 - G. Kano, Matsushita Electronics Corp
- 15/2 "A 19.7- to 21.7-GHz Amplifier"
 W. Kennan, P. Chye, C. Huang, and M. Pardo, Avantek, Inc
- 15/3 "A 20-GHz немт Amplifier for Satellite Communications"

M. Niori, T. Saito, S. Joshin, and T. Mimura, Fujitsu Labs, Ltd

15/4 "A GaAs Dual-Gate Power FET for Operation up to K Band"

B. Kim, H. Q. Tserng, and P. Saunier, Texas Instruments, Inc

15/5 "A 33-dB Gain Monolithic X-Ku-Band Power Amplifier Module"

Y. Tajima, P. Miller, R. Mozzi, and E. Tong, Raytheon Research Div; and T. Tsukii, Raytheon Electromagnetic System Div

- 15/6 "A 1.0- x 1.6-mm² GaAs, 4-GHz Receiver" S. Jamison, M. Helix, J. Culp, R. Lokken, L. Almstead, and C. Chao, Honeywell; and A. F. Podell, Podell Assocs
- 15/7 "Reduced fm Noise GaAs FET Microwave Oscillators"

J. S. Joshi and B. T. Debney, Plessey Research (Caswell), Ltd

Informal Discussion: CMOS Technology Directions

Thurs 8 pm, Imperial Ballroom A

Moderator: T. J. Rodgers, Advanced Micro Devices Panel: R. Davies, Texas Instruments, Inc; G. Hwang, IDT; S. Kohyama, Toshiba; A. London, National Semiconductor; Y. Kosa, Hitachi, Ltd; Y. Okuto, NEC VLSI Lab; and R. J. Smith, Intel Corp

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Informal Discussion: Practical vs Theoretical Limits of VLSI

Thurs 8 pm, Imperial Ballroom B

Moderator: J. D. Meindl, Stanford University

Panel: H. J. Boll, Bell Labs; Y. A. Elmansy, Intel Corp; F. H. Gaensslen, IBM Research Center; W. R. Huber, General Electric Microelectronics Center; F. M. Klassen, Philips Research Labs; N. Sasaki, Nippon Electric Co; and A. F. Tasch, Jr, Motorola, Inc

Informal Discussion: Speech Recognition Thurs 8 pm, Royal Ballroom

Moderator: G. Doddington, Texas Instruments, Inc

Panel: J. Baker, Dragon Systems, Inc; S. Chiba, NEC System Research Lab; W. Hartwell, Bell Labs; and B. Warren, Auricle

Informal Discussion: Analog vs Digital Design Thurs 8 pm, Versailles Ballroom

Moderator: J. Solomon, National Semiconductor

Panel: R. Apfel, Advanced Micro Devices; R. Brodersen, University of California, Berkeley; P. Holloway, Analog Devices; J. M. Huggins, Intel Corp; M. McMahan, Texas Instruments, Inc; and N. Sevastopoulos, National Semiconductor

Informal Discussion: Complex vs Reduced Instruction Set Computers

Thurs 8 pm, Versailles Terrace

Moderator: P. Verhofstadt, Fairchild

Panel: D. Bhandarkar, Digital Equipment Corp;

- J. L. Hennessy, Stanford University; P. Lu, Bell Labs;
- D. Patterson, University of California, Berkeley; and
- G. Radin, IBM Corp

Informal Discussion: Are Static RAM Techniques Converging? Thurs 8 pm, Georgian A Ballroom

Moderator: R. C. Foss, Mosaid, Inc

Panel: J. Barnes, Motorola; A. Dantec, Matra-Harris; K. Hardee, INMOS; K. Kokkenen, Intel Corp;

- T. Masuhara, Hitachi Central Research Lab;
- T. Tanaka, Mitsubishi Electric Co, Ltd; and
- S. K. Wiedmann, IBM Labs

Session 16: 256k DRAMs Fri 9 am to 12:15 pm, Imperial Ballroom A

Chairman: R. C. Foss, Mosaid, Inc

- 16/1 "A Sub 100-ns, 256k-Bit DRAM"
 - T. Nakano, T. Yabu, E. Noguchi, K. Shirai, and K. Miyasaka, Fujitsu, Ltd
- 16/2 "A 90-ns, 256k x 1-Bit DRAM with Double-Level Al Technology"

H. Yamamoto, O. Kudo, H. Watanabe, Y. Inoue, K. Tada, K. Mitake, and T. Fujii, Nippon Electric Co, Ltd

- 16/3 "A 100-ns, 256k DRAM with Page-Nibble Mode"
 K. Shimotori, K. Fujishima, H. Ozaki, S. Uoya,
 M. Nagatomo, K. Saitoh, and H. Oka, Mitsubishi Electric Corp
- 16/4 "A Sub 100-ns, 256k DRAM"
 J. D. Moench, A. J. Lewandowski, B. L. Morton, F. A. Miller, and J. R. Yeargain, Motorola Semiconductor
- 16/5 "A 34-ns, 256k-Bit DRAM" K. Natori, T. Furuyama, S. Saito, S. Fujii, H. Toda, T. Tanaka, and O. Ozawa, Toshiba Corp

Session 17: Precision Analog Components Fri 9 am to 12:15 pm, Imperial Ballroom B

Chairman: C. R. Hewes, Texas Instruments, Inc

17/1 "A Monolithic Conditioner for Thermocouple Signals"

A. P. Brokaw, Analog Devices Semiconductor

- 17/2 "A Precision Curvature-Compensated смоз Bandgap Reference" B-S. Song and P. R. Gray, University of California, Berkeley
- 17/3 "A Bi-моs Signal Processor for vcR Audio"
 I. Fukushima and K. Kuwahara, Hitachi Consumer Products; K. Itoigawa, Hitachi Microcomputer Engineering; K. Hoya and N. Horie, Hitachi Takasaki Works; S. Ichimura, Hitachi Tokai Works; and M. Nagata, Hitachi Central Research Center
- 17/4 "Fully Integrated Active RC Filters in MOS Technology"
- H. Banu and Y. Tsividis, Columbia University/Bell Labs
- 17/5 "High Frequency смоз Switched Capacitor Filters"
 - T. Choi, R. T. Kaneshiro, R. W. Brodersen, and P. R. Gray, University of California, Berkeley
- 17/6 "A 600-MHz Transconductance Amplifier Using Cascomp Feed Forward Error Correction"
 S. Simpkins and W. Gross, Tektronix, Inc

Session 18: Imaging and Signal Processing Fri 9 am to 12:15 pm, Royal Ballroom

Chairman: R. P. Khosla, Eastman Kodak Co

- 18/1 "3533-Element Quadrilinear CCD Imager"
 L. S-P. Sheu, N. Kadekodi, T. Ngo, and A. Ibrahim, Xerox Corp
- 18/2 "A 256- x 256-Element, Si Monolithic IR-CCD Image Sensor"
 M. Kimata, M. Denda, N. Yutani, and N. Tsubouchi, Mitsubishi Electric Corp; and R. Tsunoda and
 - T. Kanno, Japan Defense Agency
- 18/3 "A 10-MHz ccd Time-Integrating Correlator" B. E. Burke, D. L. Smythe, D. J. Silversmith, W. H. McGonagle, R. W. Mountain, and B. J. Felton, мит Lincoln Lab
- 18/4 "An Image Signal Processor"
 - T. Fukushima, Y. Kobayashi, K. Hirasawa, and T. Bandoh, Hitachi Research Lab; M. Ejiri, Hitachi Central Research Lab; and H. Kuwahara, Hitachi Ohmika Works
- 18/5 "An 80-MHz Bipolar Dot Rate Generator"
 A. Lechner and H. Jeremias, Microelectronic Development Center; and B. Scheckel, Siemens AG

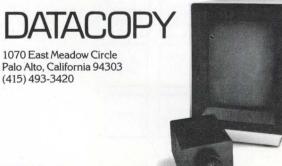
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Software for Ethernet LANS reaches transport level

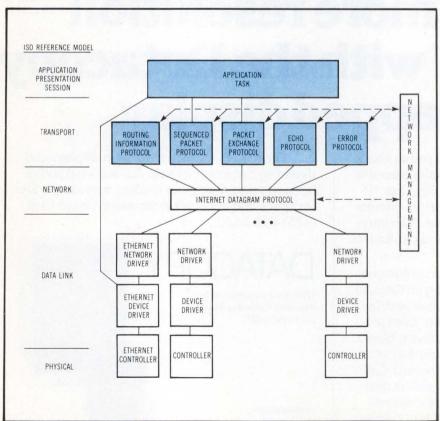
nternet Transport Protocol (ITP) NS4200 software packages from Interlan, Inc, provide task to task communications over Ethernet local area networks (LANS) for VAX/VMS and RSX-11M systems. The packages are claimed to be the first commercially available implementation of Xerox's higher level Network Systems' Ethernet transmission protocols that operate on DEC computers. The software provides reliable, flow controlled, interprocess communications between Ethernet connected systems.

In addition to supporting high bandwidth communications over an Ethernet LAN, an internetwork router facility is included for reliable end to end delivery between systems residing on different LANS. These LANS can be geographically distant and interconnected by long-haul channels or networks, or can consist of differing media such as baseband CSMA/CD, baseband token ring, or broadband token bus that are bridged together.

Transmission protocols were specified for use on an Ethernet channel, allowing the protocol's design to take advantage of Ethernet's packet addressing, error detection, and delay bandwidth characteristics. As a result, each ITP package provides a high bandwidth virtual circuit

communications service to a user's application task with minimum host CPU loading. The NS4200 ITP is specified to the Xerox Network Systems' Internet Transport Protocols, which are the architectural foundation for Xerox's distributed systems. As illustrated, the ITP protocols include internet datagram, routing information, sequenced packet, packet exchange, echo, and error protocols. With the NS4200 ITP package as a building block, the task of networking RSX-11M and VAX/VMS systems to Ethernet compatible systems is minimized. Only detailed file structures and command interpretations need be addressed to provide task to task communications between RSX-11M or VAX/VMS systems with other Ethernet compatible systems that use the Xerox Network Systems' higher level protocols.

The NS4200 ITP package contains a NETMANTM menu driven utility program that automatically tallies over 40 different network statistical values. NETMAN enables a network manager to acquire and display operational data from local/remote ITP nodes. NETMAN's parameters let a network manager identify connected ITP stations, identify congestion and flow control bottlenecks, understand traffic flow patterns, evalu-



ate the performance of virtual circuit connections, and assess the quality of network service.

In addition, Ethernet's 32-bit CRC error detection makes the checksum function optional. The 48-bit ITP addresses map directly into the 48-bit Ethernet data link addresses to eliminate need for address mapping typically required by other transmission protocols when used on Ethernet. Protocols such as the ECMA 72 Class 4 are planned for future implementation. DECnet Phase III Ethernet networking is also provided via ETHERWAY DECnet/Ethernet software. NS4200 Internet Transport Protocol package is provided in c language source form for \$25,000. Runtime licenses are also available.

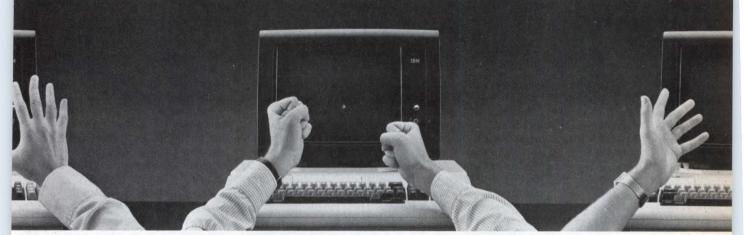
ETHERNODE 1000 series

The NS4200 ITP is also a part of the ETHERNODETM 1000 series data communications package that contains all the hardware and software required for RSX-11M and VAX/VMS systems to communicate over Ethernet. Depending on the type of processor and operating system, each ETHERNODE package contains the appropriate NS4200 ITP software, device driver, Ethernet communications controller board, nonintrusive tapping transceiver, and transmission cables. Either a NI1010 UNIBUS or NI2010 OBUS INTERLAN intelligent Ethernet communications controller board is included. These microprocessor based boards perform DMA data transfers, contain extensive receive data buffering for back to back frame reception, provide extensive diagnostics, and collect network statistics.

The NT10 Ethernet transceiver unit, an integral part of the ETHERNODE series, provides a nonintrusive coax cable tap that allows the unit to be installed/removed from an operational Ethernet without disrupting network communications. The NT10 also provides triple-redundancy control logic (jabber control) to protect the network against the effects of a continuously transmitting Ethernet station.

Included in the series are the ITP/RSX/UNIBUS, ITP/RSX/QBUS, and the ITP/VMS/UNIBUS configurations. The ITP/RSX versions are available immediately; ITP/VMS will be available in February 1983. ETHERNODE 1110 (ITP/RSX/ UNIBUS) and ETHERNODE 1310 (ITP/VMS/ UNIBUS) are priced at \$3100, quantity 25. ETHERNODE 1120 (ITP/RSX/QBUS) is priced at \$2335, quantity 25. Interlan, Inc, 3 Lyberty Way, Westford, MA 01886. Circle 261

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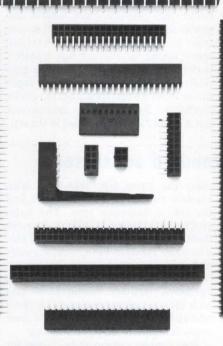
n the world of electronic data processing, choosing the wrong contact can result in lost nformation. And lost information means lost time and money. A simple error can cost you anywhere from \$50,000 to \$150,000 – or more.

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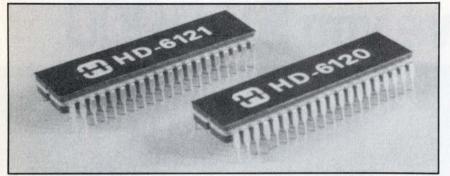
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SYSTEM COMPONENTS

High speed CMOS microprocessor and 1/0 controller upgrade family



Two added high performance CMOS microprocessor family members, the HD-6120 12-bit microprocessor and the fully compatible HD-6121 I/O controller are designed to recognize the instruction set of DEC's recently announced PDP-8/ETM (DECMATE IITM) minicomputer. An upgrade of the HD-6100 microprocessor, HD-6120 features a 5.1-MHz CPU and optimized microcode that minimizes the required number of clock cycles for all instructions, thereby reducing instruction execution time. Two onchip 12-bit stack pointer registers are included, along with onchip memory extension control hardware to address 64k words of memory divided between the 32k control panel and 32k main memory. Memory control is implemented in software and need not use any part of main memory or change the processor state-an important feature if the final configured system does not have a control panel and the main memory's entire capacity is used. The microprocessor works with either a parallel resonant, fundamental mode crystal or an external frequency source. Simplified memory, programmed data transfers, and interrupt transfer control signals ease hardware interfacing. Twelve-bit accuracy, rapid interrupt response, battery backup, and low power (sealed enclosure) capability suit the chip to realtime control applications.

The HD-6121 I/O controller provides independent control of any combination of five 12-bit I/O ports with handshaking capability. Used in conjunction with the HD-6120 microprocessor, the I/O controller chip provides basic control and enable signals for the device that it controls, but it is not involved in the critical speed timing of the DX bus transfers to/from these devices. Each I/O port retains its own output latch or input driver interface for maximum I/O device flexibility. Because these latches and input drivers are not included in the 6121, the device can provide complete handshaking for five I/O ports. Software programmable chip select decoding (enable outputs) allows 1/0 device addressing to be easily changed without changing the user's PCB. This onchip feature eliminates the need for the two to five ICs usually associated with chip select decoding. Also onchip is the priority interrupt controller that includes software programmable logic vectors and complete interrupt request/ grant handshaking for the 6120 microprocessor. A separate interrupt controller IC is not required. The priority in/priority out control signals allow up to eleven 6121s to be daisy chained without interfacing logic, for vectored interrupt control of up to 55 I/O ports. 1/0 port handshaking signals are included onchip for status polling of an input port and signaling an output port that has received data. These software programmable signals can be considered "input buffer full" and "output buffer full" status lines.

Both devices are available in the industry standard 40-pin 0.6" (1.5-cm) center spaced cerDIP. Power supply requirement is 5 V, $\pm 5\%$. Industrial temp version of the HD-6120 is \$55 and the mil temp version is \$96.25. HD-6121 is \$22 for the industrial temp version and \$38.50 for the mil temp version. Harris Corp, Semiconductor Digital Products Div, PO Box 883, Melbourne, FL 32901. Circle 262

Computer is based on standard subsystems



The 29" (74-cm) high Tower 1632 is built around a 16-bit 10-MHz MC68000 processor, a UNIX III based operating system, a MULTIBUS I/O subsystem, and fixed Winchester drives. The MC68000 supports up to 16 simultaneous local or remote users, each performing multiple functions. Up to six microprocessor based DMA controllers that handle the 51/4" disks, 8-channel 1/0, and multiprotocol communications offload I/O functions from the CPU. Up to 2M

bytes of main memory in 256k-byte increments and 60M bytes of Winchester disk mass storage in the main unit are supported. Add-on units can expand mass storage to more than 1G byte. Standard magnetic media interfaces include the SA400 for 1M-byte 5¹/₄ " floppies, the ST506 for 10M-byte Winchesters, an SMD for 8" Winchesters, and the QIC II streaming tape. The 6-slot MULTIBUS I/O system is separate from the dedicated 2-slot high speed memory bus. The buses function both simultaneously and independently to minimize contention and maximize throughput. UNIX optimized memory management unit with 256k ECC memory uses a full 24-bit addressing field and provides a clear migration path to 32-bit technology.

Five "menu personalities," one for each of five programming sophistication levels, are part of the enhanced UNIX. These personalities allow easy access to the system. To facilitate applications development, NCR'S N-GEN dictionarydriven applications generator contains the needed software tools to generate quick computer programs. COBOL, Business BASIC, FORTRAN, and C languages are supported. Two RS-232-C ports provide ASCII teletypewriter and Bisync 2780/3780 communications. Other protocols supported are NCR'S DLC, SDLC/SNA, X.21/X.25, and UNIX networking.

Carrying features beyond industry standards, the Tower 1632 includes a power fail recovery system that preserves data in memory (without specialized applications programming) until power is returned after an outage. In addition, the intellectual properties protection system prevents both proprietary operating and applications software from running on unlicensed machines.

The \$12,000 Tower 1632 will be sold to computer systems houses, OEMS, distributors, and dealers who can add applications software, specialized peripherals, and other subsystems to suit customized needs. NCR Corp, Dayton, OH 45479. Circle 263

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SYSTEM COMPONENTS

Programmable controllers store 10-year memory without external power



Three microprocessor based programmable controllers capable of solving more than 80% of the control problems in small industrial applications, the EPTAKTM 210, 220, and 240 are economical alternatives to hardwired control relays, card logic systems, and panel systems. Key to the systems is a compact controller with CPU; power supply; portable, remotely programmable 54-key programmer; realtime clock; and nonvolatile EEPROM. The EEPROM provides 10 years of memory protection without an external power source.

EPTAK 210 and 220 are based on Intel's 8049 microprocessor chip, and EPTAK 240 uses Intel's 8051 microprocessor. A permanent program storage, plug-in memory module that fits directly into the processor or programmer protects against data loss from power failures, time delays from programming to final equipment installation, or extended periods between editing and program use. Typical scan rates are 10 ms for model 210 and 20 ms for models 220 and 240. These times vary as the number of program instructions vary.

An RS-232 communications port links peripherals located up to 50' (15 m) from the

programmer to the unit. The processor controlled "operator interface" port accommodates bidirectional data transmissions to the programmer and the data access display modules (DADMS) for monitoring timers/counters or analog data at distances up to 1k' (305 m) from the processor.

1/O configuration delivers up to 16 dual-point modules for 32 max 1/O points per track. Each EPTAK system can interface to the same programmer, DADMS, and other peripherals for shared communications and control functions. A reversible step program function is accommodated via two 32-stage shift registers.

EPTAK 210 (\$361) replaces hardwired panels or control systems with as few as

two timers/counters and several relays. Space can be further cut by selecting either full-, half-, one-quarter, or oneeighth track size versions. EEPROM is 1k and 420 program statement capacity is provided.

EPTAK 220 (pictured) expands EEPROM to 4k and provides 820 program statement capacity. Add, subtract, and compare functions optimize data handling. It has 128 I/OS, controls 32 timers/ counters, and can be expanded to 4 I/O tracks for maximum control. Eight auxiliary ports for external I/O in binary or BCD format are provided. Price is \$1323.

EPTAK 240 (\$1778) with 16 analog I/Os increases device potential in process control applications. Accompanying analog I/O blocks fit the standard track; other digital blocks can be intermixed in unused analog block positions on the same track. Analog input values are setpoint, actual, and proportional integrated derivative (PID). If PID values are not defined, the PID loop defaults to ON/OFF control. Two subroutines permit common routines to be repeated without duplicating instructions. The 8k EEPROM provides a 1200 program statement capacity and 6 arithmetic functions. Eagle Signal Industrial Controls, a div of Gulf+Western Manufacturing Co. 736 Federal St, Davenport, IA 52803. Circle 264

Dual fixed/removable 51/4 " Winchester drive meets ANSI specs



Providing unformatted capacities of 13M bytes in fixed memory and 13M bytes on removable disk cartridge, the D520 5¹/4" Winchester also boasts 860-tpi/9200-bpi densities and 40-ms average access time. An embedded servo tracking system eliminates seek errors and need to align the oxide media and minicomposite read/write heads. The Winchester's removable front loading cartridge is compatible with the proposed ANSI standard cartridge (Computer Design, Oct 1982, p 3). When the cartridge is inserted into the drive, the drive/cartridge combination becomes a completely sealed unit allowing high pressured, closed-loop air flow and filtration. This absolute air filtration system allows the disks and heads to operate in a contamination free environment. Drive logic ensures that heads are loaded only after a completed air contamination purge cycle. Since the cartridge performance and capacity exactly match those of the drive's fixed memory, full backup is easily accomplished.

The drive provides 1 spare sector per track and 10 spare tracks per surface. Its magnetic rotary voice coil actuator is completely balanced to allow mounting in vertical and horizontal positions. Proprietary LSI chips have reduced the required number of discrete components by approximately 75. A brushless dc drive motor directly rotates the drive motor to eliminate need for belts or pulleys, and to increase reliability. The shock-mounted baseplate minimizes vibration. MTBF is specified at 8k POH, and the drive requires no preventive maintenance.

Rotational speed is 3400 rpm. Track to track access is 5 ms and transfer rate is 5M bps. Ambient temp range is 4 to 46 °C. The drive is built within the standard 5¹/₄ " minifloppy footprint of 5.75" x 3.25" x 8" (14.61 x 8.26 x 20 cm) and weighs 7 lb (3 kg). Internationally used dc voltage requirements are ± 12 Vdc and 5 Vdc; power consumption is 35 W

ST706 and DMA interface compatible the fixed/removable Winchester is the first 51/4" drive from Cynthi: Peripheral, a service subsidiary of the France based Cii Honeywell Bull that formerly specialized in 101/2" drives Price of the D520 is \$1350 in OEM quar tities. The company's compatible "Eas disk drive subsystem provide Box" immediate connection to built-i backup, controller, power supply, ar enclosure, for a price of \$1780. Cynth Peripheral Corp, 3606 W Bayshore R Circle 2 Palo Alto, CA 94303.

PROCESSING: Where to drill? Traditionally, exploring a 25,000 square mile frontier for an answer to that question could take months. And cost over a million dollars for consultant fees and aerial photography.

Today, a DeAnza Image Processing System can narrow the same frontier to a few miles using roughly \$100.00 worth of satellite data. And help

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Enhanced seismic data of an oil find.

Unenhanced LAMOSAT imaging of Central California

IMAGE

topographical, etc. Step-by-step, a DeAnza Image Processing System graphically displays faults, folds and stratigraphic units to pinpoint areas small enough for seismic exploration. Finally, the system enhances seismic data gathered in the field to project final drill sites. And these projections stay completely confidential, because they're done in-house.

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> 3. D Mich algorithm of Same Location

SYSTEM COMPONENTS

Full-color graphics added to workstation



With only an 18% price increase, AWS turbo color graphics workstation adds full-color graphics capability to the multifunction architecture of the yearold monochromatic AWS turbo workstation. Designed around a 16-bit 8-MHz 8086 CPU, LSI graphics processor, and 512k-byte RAM, the color workstations use an architecture that distributes intelligence to each unit. Up to 0.5M-byte memory, high resolution 15" (38-cm) VDU, programmable keyboard, and an intelligent color graphics board with dedicated NEC 7220 graphics processor are included. Mass storage options include either a 51/4" 630k-byte minifloppy unit or a 51/4 " mini-Winchester with 5M-, 10M-, or 16M-byte capacity.

The bit-mapped video with 128k-byte display memory and 16k-byte firmware that offloads the graphics overhead from the workstation's CPU is organized in three 512 x 512 display memory planes. As a combined graphics and alphanumeric subsystem, a proprietary page mode memory controller on the graphics board provides 3 bits/pixel via sixteen 64k dynamic RAMS. Vector drawing mode uses a full palette

of 64 colors, with 8 colors displayable at any time. Screen can display 80 chars x 29 lines and 7 x 9 pixels per char in a 9- x 11-pixel cell. Graphics resolution is 432 x 319. The alphanumeric/graphics displays can also be selectively disabled to present only text or only graphics, or to combine the two with text taking precedence.

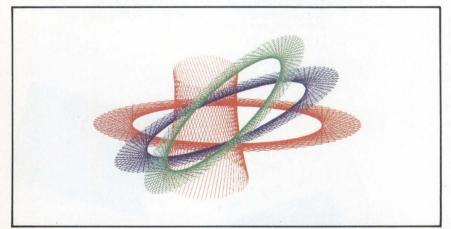
Although the units can be locally clustered for networking capabilities via a high speed data link, neither the central processor nor the graphics processor is shared by other workstations in the network. Diverse applications can simultaneously operate on the same data base. Hardware and software architectures are totally modular, designed to provide multiple upgrade paths. A standalone system can be upgraded to local networking without software modification. The workstations can also be connected to mainframe hosts via SNA, X.25, IBM 3270, and 2780/3780 communications protocols.

All AWS turbo color graphics workstations have four I/O ports—two RS-232-C serial ports, one RS-422 cluster port, and one Centronics compatible parallel port. The systems have a built-in spooler that permits queuing of an unlimited number of pictures for plotting or printing without interfering with simultaneous interactive processing operations.

Three levels of device-independent graphics software support include system-level primitives, applicationslevel primitives, and the Color Business Graphics Package. The device-independent graphics subroutines are callable from COBOL, BASIC, FORTRAN, and Pascal. Software controls character generation, multiple split screens, and a wide range of display attributes.

Pricing for the Aws color turbo graphics workstations in single units ranges from \$12,190 for a unit with 5M-byte Winchester to \$13,790 for a unit with 16M-byte disk. Convergent Technologies, 2500 Augustine Dr, Santa Clara, CA 95051. Circle 266

Ink-sheet copier blends color print, thermal transfer techniques



D-SCAN 5201 produces full-color copies of complex graphics directly from CRT displays in under one minute. To further enhance productivity, local video memory stores images before the output copies are generated, freeing the graphics workstation for continuous use. Copies come out on markable, fade-resistant paper with a 150-dot/in resolution. Per-copy cost is \$0.25.

Seiko's ink-sheet technology forms copies over a line-type thermal head.

The head transfers pigment dots from a wax coated, 3-color banded ink sheet to a sheet of normal grade paper that overlays the ink sheet. The specially treated paper comes in a segmented roll with consecutive page-sized bands of cyan, magenta, and yellow.

The 0.003-mm, transferable pigmenttype ink layer covers a 0.01-mm thick ink sheet, which passes over the thermal head to print the appropriate portion of each of the three primary colors onto the copy. Wire nibs in the thermal head heat up instantaneously to melt pinpoint spots of color into the print.

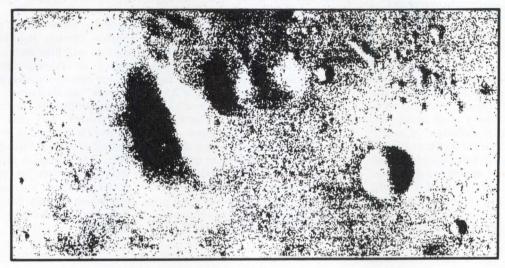
In turn, with images transformed onto plain paper, the cyan, magenta, and yellow combine to create a palette of eight saturated colors, including red, green, blue, black, and white. Apart from the standard and ink-sheet paper rolls, no resupplies, such as toner or ink, are needed. Final copies are automatically cut to standard 8.5" x 11" letter size.

One half of the D-SCAN 5201 controls critical ink-sheet and paper movements, and the other manages electronic duties such as input control, formatting, storing, and CRT graphic data output. The machine measures $26'' \times 12.8'' \times 17.5''$ (66 x 32.5 x 44.5 cm) and weighs 130 lb (59 kg).

Slated for shipment late in the first quarter of 1983, the base unit will cost about \$13,000, quantity-one. Optional and standard interfaces including RS-170 and RS-343, as well as a Centronics compatible parallel interface, will also be available. Seiko Instruments U.S.A., Inc, 2620 Augustine Dr, Santa Clara, CA 95051. Circle 267



OTHER ADDITIONAL STANDARD FEA 180 cps, 150 cps, 75 cps FULL DOT ADDRESSABLE GRAM COMPRESSED PITCH AT 10 AUTOMATIC BOLD, REPEAT, HORIZONTAL TABS FROM 1 TO VFU CONTROL UP TO 255 VE VERTICAL LINE SPACING OF 4.7 KBYTE BUFFER BOTTOM AND FRONT PAPER F ADJUSTABLE TRACTOR FEED SWITCH SELECTABLE 115 OR SWITCH SELECTABLE SERIAL HEAVY DUTY PRINT HEAD (50 6 PART FORM CAPABILITY (0



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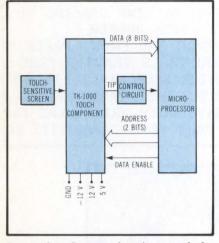
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SYSTEM COMPONENTS

Unpatterned faceplate detects continuous X-Y coordinates



Interaction Systems has improved the resolution of its capacitive-sensing technology with TK-1000, a touch sensor that allows unrestricted definition of touch-sensitive areas on one surface. Proprietary technology, which deposits indium tin oxide over an unpatterned glass face-plate, provides continuous X-Y coordinates of the touch point in 8-bit (0 to 255) numeric output for both dimensions. The unpatterned, temper-coated

technique substantially reduces production cost.

Early touch-sensitive screen coordinate systems were largely mechanical pushing one plastic layer embedded with wire mesh into another. Though active elements produce high resolution, numerous mechanical parts raise cost and lower reliability. In subsequent solid state versions, the faceplate was flooded with infrared light or high frequency sound, and each broken beam marked a touch coordinate.

TK-1000 touch-sensing system is designed to be incorporated into a microprocessor bus, and will control both video based and computer generated displays. It consists of the faceplate, a connecting cable, and a $2.5" \times 2.5" \times 0.75"$ (6.4- x 6.4- x 1.9-cm) component that outputs 8 bits of data and a "touch in progress" (TIP) signal.

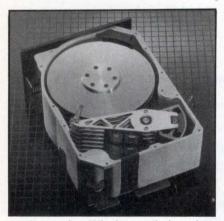
When a person touches the screen, the touch component detects an impedance change and lowers the TIP line. Control logic can program the microprocessor to monitor the TIP at intervals, or to provide an interrupt to the microprocessor. The microprocessor then reads X and Y coordinates from the touch position via address and data enable lines.

Microprocessor software that controls the touch component adjusts the time required for touch recognition. Browsing is allowed by not accepting a touch until the user stabilizes at a position or, alternately, lifts the finger.

The system can be used alone or in conjunction with a keyboard, which can be displayed on a video monitor for typing directly onto the screen. Moreover, with TK-1000 the computer will recognize letters drawn onto the video display. Directly touching the desired location will also move the cursor for adding or deleting text, which can replace conventional keyboard entries or "mouse" manipulations.

In quantity-1000, each touch-sensitive component will cost about \$200. Delivery is expected to be late in the first quarter or early in the second quarter of 1983. The company will offer manufacturing licenses for TK-1000 to companies with high volume requirements. Interaction Systems, Inc, 24 Munroe St, Newtonville, MA 02160. Circle 268

Winchester 5¹/₄" drive packs 140M bytes on eight disks



An innovative Winchester design gives the XT-1000 series of 5¹/₄ " drives 140M-byte max capacity and an average access time of 30 ms. The proprietary integral hub/dc motor design, with the spindle motor inside the disk hub, provides a deeper base casting and thus allows eight minifloppy sized disks to be stacked inside the enclosure.

A flexure design derived from ferrite recording heads with Whitney-type sliders (IBM 3380 technology) is incorporated instead of the conventional 3350 style head flexures used on many smaller Winchesters. This Whitney design allows a closer disk spacing to accommodate the increased number of platters per package. It also provides improved aerodynamic stability for the flying head, better head to disk compliance, and an improved signal to noise ratio. Additionally, the Whitney head/flexure design utilizes more of the disk surface to increase the total number of tracks per disk surface to 918. This flexure/ head concept will also allow thin-film read/write heads that provide at least 50% increased recording densities to be easily incorporated as they become available in low cost production quantities.

Currently ST506/412 compatible, subsequent drives are planned that will utilize intelligent interfaces such as Shugart's SASI. Although the read/write channel design is already optimized to handle MFM codes, when SASI is implemented, user transparent run-length limited (RLL) codes may be used on future generations of the drives. Through RLL codes, a 50% increase in storage capacity per disk can be realized with no corresponding increase in flux density.

XT-1000 drives use the 30-ms access time MAXTOROTM rotary voice-coil actuator to position the heads on the disks. It compares well to the performance usually achieved only by larger sized, high power consumption linear actuators. The rotary voice-coil design has 80% of its copper in the magnetic field throughout movement to improve torque. The closed loop servo system, dedicated servo surface, and plated recording media provide recording density of 980 tpi. Miniaturized LSI ICs packed on the single MAXPAKTM PCB work as functional TTL circuit equivalents, while occupying 50% less space. Rotational speed is 3600 rpm; average latency is 8.33 ms; and transfer rate is 5M bps.

Initial deliveries are scheduled for the first quarter of 1983, with volume shipments slated for the second quarter of 1983. Three models will be provided, ranging in unformatted capacities of the 65M-byte 4-disk XT-1065 (\$1520), the 105M-byte 6-disk XT-1105 (\$2100), and the 140M-byte 8-disk XT-1140 (\$2690). **Maxtor Corp**, 5201 Lafayette St, Santa Clara, CA 95050. Circle 269

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SYSTEM COMPONENTS/ PERIPHERALS

Portable plotter



DMP-40 single-pen drum plotter features pen speeds to 4.2 ips and format size to 11" x 17" (28 x 43 cm). Both pen and paper are directly driven by stepper motors. Step size is programmed to ensure resolution exceeding anticipated CAD/CAM or general plotting requirements. Unit generates circles, arcs, ellipses, and general curves on command. The 5 char sets resident in ROM can be presented normally or in italics with 255 sizes and 360° of rotation. Eleven line types are available. Plotter will also clip, window, viewport, and scale to size. Price is \$995. Bausch & Lomb, 8500 Cameron Rd, Austin, TX 78753. Circle 272

Multifunction serial dot-matrix printers

Microline models 92 and 93 dot-matrix printers provide bidirectional data processing print mode with short line seeking logic at 160 cps and high resolution correspondence print mode at 40 cps. Microline 92 (\$695) with a max col width of 136 at 17 cpi and Microline 93 (\$1249) with a max width of 233 cols at 17 cpi feature OkigraphTM dot-addressable graphics. Downline loadable char sets create custom chars and symbols. Centronics compatible parallel or RS-232-C serial interfaces are provided. MTBF is 4k h; MTTR is 15 min. **Okidata Corp**, 111 Gaither Dr, Mt Laurel, NJ 08054.



Circle 273

Industrial printer



Digistrip[®] model LP-1 is a sealed, panel mounting line printer for industrial and control applications. Paper path is totally self-contained. A full 11" x 8.5" (28- x 21.6-cm) print format is provided. Printer mechanism is 5 x 8 dot matrix and operates on pressure sensitive paper. No separate inks or ribbons are required. Accepting either RS-232-C or 20-mA current loop inputs, printer provides full ASCII upper/lowercase char set at 137 cols wide, 1 line/s. A 3k-char internal buffer allows error-free printing between 110 and 2400 baud. Kaye Instruments, Inc, 15 De Angelo Dr, Bedford, MA 01730.

Circle 274

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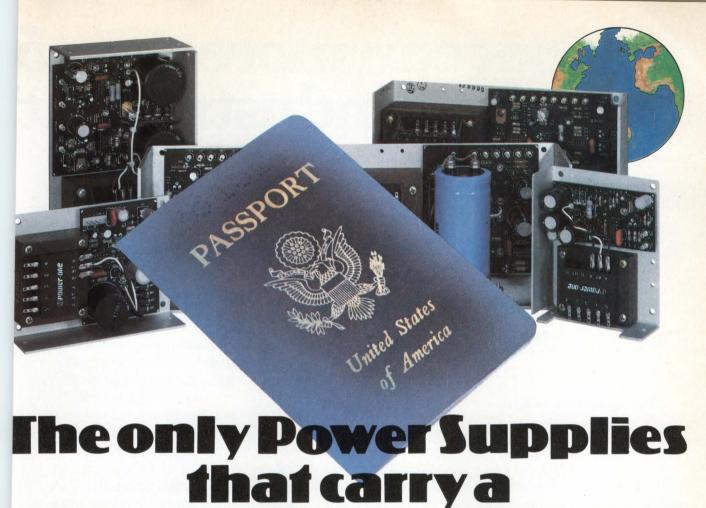
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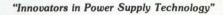
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CIRCLE 83

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It can bring you a touch panel that ultimately has a lot going for it.

There's more to a touch panel than what's in front, behind, and across it. Namely, the capabilities of the company selling it. At MICRO SWITCH these capabilities start with our people. Like direct salespeople and in-house application engineers who will work with your engineers to help develop a cost-effective solution to all of your manual control needs. They want to get involved early in your design process to help reduce the time and resources you need to invest.

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jacket construction, heat-resistant to 140°F, extends disk use without risk of mistracking. In effect, durability is redefined. And in accelerated tests against the most respected names in the industry, Maxell sustained the highest and most consistent output over time.

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It's worth it. Computer Products Division, Maxell Corporation of America, 60 Oxford Drive, Moonachie, N.J. 07074 201-440-8020

Matrix printer for microcomputers



MT 160 160-cps 80-col dot matrix printer features a 40 x 18 char matrix printed at 40 cps. Data processing mode uses a 9 x 7 char matrix at 160 cps and features bidirectional logic seeking printhead travel and accelerated tabbing to increase throughput. Dot addressable graphics produce bar and pie charts, curves, or other images on a video screen. Four double-wide, and 3 compressed print char pitches, and std 10 cpi can be printed. Friction feed and clip-on attachments accommodate paper handling. List prices begin at \$845. Mannesmann Tally, 8301 S 180th St, Kent, WA 98032. Circle 275

Low cost daisywheel printer

HP 2602A daisywheel printer, priced at \$1950, eliminates the need to remove the ribbon to insert the printwheel. The printwheels are aligned automatically within their enclosure. Printwheels in several languages and type styles are available. Modular design includes printer mechanism, power supply, 2-bolt cover design, control panel, and PCB. Printer features an RS-232-C interface with an HP-IB option, bidirectional printing, proportional spacing, and 132 cols at 10 pitch. Contact local **Hewlett-Packard** sales offices. **Circle 276**

Low cost terminal emulates HP 2624A

TS-2624 terminal emulates HP model 2624A display terminal and comes with P-31 green phosphor or amber screens. Optional microprocessor controlled 212A compatible modem (\$965) operates at either 300 or 1200 bps in full-duplex with originate and auto-answer modes. Four pages of screen memory and two RS-232 ports are std. Terminal has 128 displayable ASCII upper/lowercase chars and 64-char line drawing set. Display enhancements are provided. Single-unit price is \$1995. Falco Data Products, Inc. 1286 Lawrence Station Rd, Sunnyvale, CA 94086. Circle 277

Desktop alphanumeric raster graphics terminal

Whizzard 1650TM color graphics terminals are compatible with DEC VT100/52 and the Whizzard 6000 and 7000 series systems. Each unit utilizes an 8-MHz 8086 microprocessor as the graphics processor, and employs display list processing techniques. An 8085 microprocessor is used as keyboard/peripheral processor; digital vector generator processes display list vectors up to 10 times faster than a general purpose microprocessor. RS-232-C port interfaces to the host, and local intelligence offloads many processing tasks. Price is \$15,900; volume discounts are available. **Megatek Corp**, 3985 Sorrento Valley Blvd, San Diego, CA 92121. **Circle 278**

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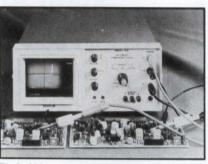
Portable 5¼" Winchester tester



DX525 microprocessor based test system automatically exercises ST506 type disk drives. Up to 16 prompted programmed test functions aid in the generation of a flaw map of bad tracks and overall error rate statistics. Tester connects to the drive through std 20- and 34-conductor flat ribbon cables. Functions evaluated include compatible interface, device selection, positioning electronics, and R/W circuits. It can operate in single cycle or continuous modes and provides selectable error thresholds. Price is \$2225 for single units. Applied Memory Technology, 2822 Walnut Ave, Tustin, CA 92680. Circle 279

In-circuit component tester

Model 3110 in-circuit component tester's CRT X-Y display presents E/I characteristic curve of component or circuit under test, and has a 1-Hz switching CRT rate compare mode. A 100-Hz triangle waveform test signal eliminates bright spots and other display aberrations. Low, medium, and high voltage ranges with a continuously variable divider are provided. LED annunciator around the CRT display indicates full-scale voltage range in use and A/B test signal in operation. All metal chassis eliminates external noise interference. Unit price is \$995. Vu-Data Corp, 7122 Convoy Court, San Diego, CA 92111.



Circle 280

Communications performance analyzer



Model CPA/7 monitors all data comm traffic and automatically prints a hardcopy report that includes over 70 categories of line utilization and transaction response time statistics. The unit can monitor for 1 or all transactions at 1 of 3 logical levels within the comm link-all stations level (up to 1024 addresses); cluster control unit level (all stations attached to a specific cluster); and logical unit level (1 device attached to a cluster control unit). Z80 based, the system supports 3270 Bisync and 3270 SDLC/SNA protocols in the same unit. Price is \$6300 with printer or \$5450 without printer. Questronics, Inc, 3565 S West Temple #5, Salt Lake City, UT 84115

Circle 281







Fiber optic connector for HP data links

The 906 series single-fiber, single-channel connector provides 1- to 2-dB insertion loss, and is intermateable with HP's HFBR-1201 transmitter and HFBR-2201 receiver data links. The optic connector also complements the HP links' 0.132" (0.335-cm) mounted height for applications requiring 0.5" (1.3-cm) board spacing. All metal construction maintains the package's emi/rfi integrity. Connector terminates HP's P/N HFBR-3000 glass fiber. The link is available with/ without installed connectors. The devices are \$5 for 1k-piece quantity. Amphenol, an Allied Co, World Headquarters, 2122 York Rd, Oak Brook, IL 60521. Circle 282

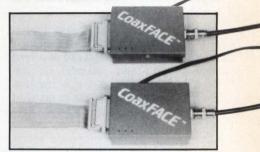
6-slot assembly for black box applications

Model 3200 backplane power supply assembly nests the SBC 11/21 Falcon, LSI-11/2, or -11/23, and up to 5 1/0, memory, and/or mass storage interface boards in NEMA compatible enclosures and other space restricted black box applications. In addition to front access power supply and card cage, the assembly features 16 captive mounting nuts and optional universal mounting bracket. Std equipment includes 5-V at 8-A and 12-V at 1.5-A plug-in power supply, 60-Hz line clock, emi shield between supply and card cage, front panel switch connector, and terminal block for ac power and access to 5 and 12 V for external use. In open configuration, price is \$695; in fully packaged version, price is \$850. ADAC Corp, 70 Tower Office Park, Woburn, MA 01801.



Circle 283

Interface links RS-232 and coaxial cable



CoaxFACETM connecting interface allows use of existing RG-62 coaxial cable to avoid the cost of installing special RS-232 cable. The interface (\$150/pair) connects RS-232-C links and IBM coaxial cable and is an option on the company's 1076. 1071, and 1051 protocol converters. The PCI converter interfaces between an IBM SNA/SDLC host and ASCII CRTS, personal computers, printers, and other devices. CoaxFACE is a connecting link on the ASCII device. Digital pulses are transmitted through the cable 300 to 9600 bps without reducing the RS-232-C data rate. Protocol Computers, Inc, 6430 Variel Ave, Woodland Hills, CA 91367. Circle 284

Archive backs up Winchesters 10 times faster than floppies.

Today's business computer system simply can't afford floppy Winchester back-up anymore. Not when our Archive Super Sidewinder ¼" Streaming Cartridge Tape Drive can copy 45MB in just nine minutes.

A floppy, on the other hand, takes more than an hour to do the same job. Not counting the time you spend inserting a new disk every few minutes.

Saves "handling" charges.

One Super Sidewinder cartridge is equal in capacity to 38 eight-inch disks.

That will save you over \$200, plus the cost of handling all those disks – inserting, removing, jacketing, labeling, and filing. In addition, a Sidewinder

cartridge is completely enclosed when out of the drive, virtually eliminating damage due to handling. **More than just a back-up.**

Our ¼" streaming tape drives pro-

vide the complete removable media needs of any system: Software distribution, data collection and program loading. All performed at the touch of a button.

System integration made simpler.

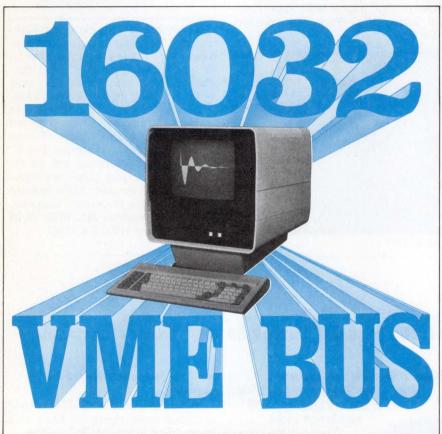
Both our 20MB and 45MB drives are specifically designed to fit an 8" floppy disk footprint. To use the same power supply. And to use the same simple 8-bit parallel interface.

We could go on. But let's get specific, contact us today. And ask for our new handbook on streaming tape drives and how to use them. Archive Corporation, 3540 Cadillac Ave., Costa Mesa, CA 92626. (714) 641-0279, Telex 4722063, TWX 183561. Distributed nationally by Hamilton/Avnet.



Signal conditioning subsystem for harsh environments

Analog 1/0 signal conditioning subsystem 3B series provides a modular interface that directly connects to low level sensor signals and produces simultaneous high level voltage and current outputs. The small modules can be matched on 4-, 8-, and 16-channel backplanes for custom-tailored signal conditioning. Specs include -25 to 85 °C op temp range, ± 1500 -V isolation, and 220-V RMS input protection. Modules are priced from \$135. **Analog Devices, Inc**, Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062. **Circle 285**



THE CONSULTANT

Industry standard 32 bit bus

Multi-processor capability

Demand paged virtual memory

High resolution graphics

512K, internally expandable to 1.75 megabyte

Hard disk, 5 megabyte fixed, 5 megabyte removable

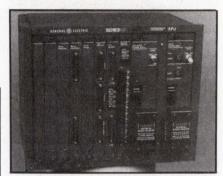
Multi-tasking operating system Pascal, LISP, PL/BASIC, SMPL Basic system under \$18,000



(316) 265-0959 906 N. Main, Wichita, Kansas 67203

CONSULTANT is a trademark of Elite Corporation.

Redundant processor unit for programmable controls



A redundant processor unit (RPU) for GE's Series Six programmable controller functions as a switch to perform a bumpless transfer of logic control to a backup CPU. Switching is done within a few milliseconds of a detected fault. Unit automatically switches to an auxiliary backup power supply if the RPU's main source fails. Failed modules can be replaced without removing power from the unit. Dual 1/0 system runs in parallel. CPUs are sweep interlocked for program synchronization. General Electric Co, 8150 Leesburg Pike, Vienna, VA 22180. Circle 286

Programmable controller features 32 1/0s and 5 timers

1000 series sequential programmable controller is prepacked and completely assembled for control panel mounting. Two I/O module boards provide up to 32 I/Os. One module board contains 8 dedicated inputs and 8 dedicated outputs. Optional second module board also has 2 groups of 8 that are switch selectable as 1/Os. Five independent internal timers are software programmed with multiples of timing functions/timer in any given cycle, each of which can be preset for 0.01 to 0.1 s, 0.1 to 10 s, 1 to 100 s, and 10 to 1k s. Customized preprogramming is available. Holmor, Inc, 169 Rte 206, Flanders, NJ 07836. Circle 287

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CIRCLE 90

MORE THAN A QUESTION OF PASS/FAIL

Testing is more than the simple question of pass/fail. It is a complex set of questions encompassing degree of test, test results needed, test procedure and many other aspects of both product and corporate needs. Applied Circuit Technology designs and manufactures volume test equipment to answer these important questions for rotating memory devices. Based upon six years of proven performance, ACT's equipment has tested more 51/4" Winchester disk drives than any other system in the world. ACT's expertise, however, does not stop at Winchester drives. Today, Applied Circuit Technology has systems involved in floppy systems test, tape systems test, fixed/ removable Winchester disk systems test,

plus Servo Writers and Spiral Testers. From 10 units to 100 units in simultaneous test with **one console**, Applied Circuit Technology provides the answer to high volume, in-depth end configuration testing.

If you believe testing is more than a question of pass/fail, contact Applied Circuit Technology.



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EINAL TEST

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Now with GEN.II,[™] choose a monochrome, gray-scale, or color-formatted terminal to deliver our Tek 4010/4027 compatible graphics.

For a variety of text terminals, the world of cost-efficient graphmaking is now made possible by Digital Engineering's GEN.II Retro-Graphics terminal enhancement — a "snap-in" PC card assembly that provides Tektronix®-based graphics software compatibility.

software compatibility. Once installed, GEN.II will perform monochrome imaging on the TeleVideo® 950, 925, 920, 912, and 910, Lear Siegler ADM 3A, 3A +, and 5, and ADDS VIEWPOINT and VIEWPOINT/3A PLUS; gray scale on TI's Model 940; and color on the Datamedia™ ColorScan™ 10, 30, 60, 70, and 10H.

But best of all a Retro-Graphics enhancement costs only a fraction of what you're paying now for an equivalent graphics terminal: about \$1200-1900, depending on the GEN.II model you order.

Introducing GEN.II Retro-Graphics. For superior bit-mapped technical plots and MIS charts.

Our second-generation enhancements provide emulation of the Tektronix 4010 graphics terminal *and* simulation of the Tek[™] 4027 color graphics terminal. In standard resolutions on all GEN.II models. And in medium resolution — 640 by 480 pixels — on Color Retro-Graphics[™] for the ColorScan 10H.

Because GEN II products are based on industry-standard Tek protocol, operation is both powerful and familiar to most programmers. Raster-scan images are generated quickly on GEN. II because up to 48 Kb's of graphics intelligence is "resident." This also means costly host-terminal data transmissions are held to a minimum.

English-like commands simplify graphics operation and programming. For example, entering from the keyboard or computer the following command string **!PIE, 200, 90, 120** will cause the upgraded terminal to draw a pie chart sector with a radius of 200 and fill in the area between 90 and 120 degrees. The filled area can be a color in the case of Color Retro-Graphics, an intensity level in the case of gray-scale GEN.II, or a dithered shade in the case of our one-color products.

In addition, GEN.II enables the programmer to draw *polygons* and *vectors*. *Define* and *shape text characters*. And *recall stored graphs* with similar high-level command strings. And you get all this without the loss of existing terminal features.

GEN.II software compatibility protects your hardware investment.

Since our products are compatible with Tek's 4027 and 4010, GEN.II's performance on utility and applications programs, both present and future, is ensured. Currently, more than 20,000 Retro-Graphics enhancements are successfully being used with DISSPLA® and TELLAGRAF®, PLOT 10™, Template™, DI-3000™, and ILS® graphics programs.

Comprehensive support at every level.

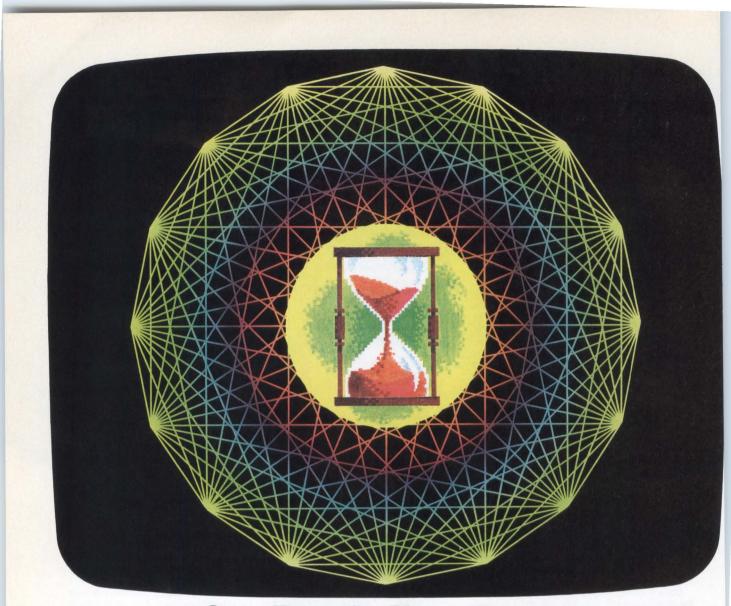
Good ideas mean little if you cannot build on them. Optional interfaces let you hook up a variety of input/output devices of your choice. These include a light pen and digitizers, impact and non-impact serial printers, and video devices. There's solid documentation at every level. And fast, accurate backup by our own customer service and worldwide distribution network.

Digital Engineering's GEN. II Retro-Graphics and your choice of terminal — for economy and compatibility in a sophisticated graphics workstation.

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Ikegami Technology

For systems applications requiring high quality, dependable CRT display monitors, Ikegami brings you the technology of the future, today.

An innovator in video technology for over 36 years and the world's leading producer of high quality broadcast camera systems and monitors, Ikegami has applied its unparalleled experience to the design and production of display monitors for the computer industry. Put Ikegami's Emmy award-winning digital techniques for automatic setup to work for you.



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HDM Series

Ultra high resolution for your most demanding graphics systems. Ikegami's HDM Series color and monochrome display monitors utilize a delta-gun, raster-scan CRT and superb quality wide band, high speed scan, video amplifiers to provide the precision you need (up to 1280 \times 1024 pixels interlace mode), plus the long life and easy maintenance you demand from a top quality graphics display. Available in 19V and 25V CRT sizes.

The CD Series (CDA/CDB)

to meet your needs, today and tomorrow,

For more information on highperformance CRT display units designed

write or call Ikegami today.

Quickly becoming our most popular line of high resolution in-line gun



color CRT display monitors. If your requirements are for high resolution (up to 1024×1024 pixels interlace mode), stable operation and very low maintenance, the CD Series may be your solution.

Available in 13V and 19V analog or digital models, the compact-size CD Series is perfect for simulation, medical, CAD/CAM and other high resolution applications.

The UD Series

Medium resolution, digital drive, color display monitors for business graphics systems. The Ikegami UD Series provides high performance (615×240 or more pixels interlace mode) at a very economical price.

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High performance, flicker-free monochrome CRT display units that bring lkegami quality to word processing or on-line data entry systems. Available in green or white display and standard CRT sizes (5", 9", 12", 14' and 15").

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West — 3445 Kashiwa Street Torrance, CA 90505 (213) 534-0050

We are the future.

CIRCLE 93

Easy to use data logger



Model 2500 data logger can be set up and operated through the front panel without a programming language. Pushbutton switches program 10 to 40 internal channels alone or in blocks, set scan interval, and select output conditions from the built-in 32-col printer. Unit holds 4 signal conditioners and accepts 35 types of sensors. Accuracy is rated at $\pm 0.015\%$ full scale. Five-digit display indicates polarity and is capable of 25k counts. Options include alarm package, RS-232-C/20-mA port, scan expanders to 240 channels, and extra signal conditioners. Digitec Corp, 918 Woodley Rd, PO Box 458, Dayton, OH 45401. Circle 288

Measurement/control unit works alone or as frontend interface



Model 10K7 DataPAC data acquisition and control system can interface with any computer in any programming language. Large scale integral black/white or color CRT display with up to 100 field composable format pages is featured. System scans up to 1k channels at 2500 channel/s min. Microprocessor based data acquisition and control program is completely transparent to the computer; 84k-byte memory (including 36k nonvolatile EEPROM) remembers all setup and calibration data even in total power loss. Computer interface is RS-232 or, optionally IEEE 488. Daytronic Corp, 2589 Corporate Pl, Miamisburg, OH 45342.

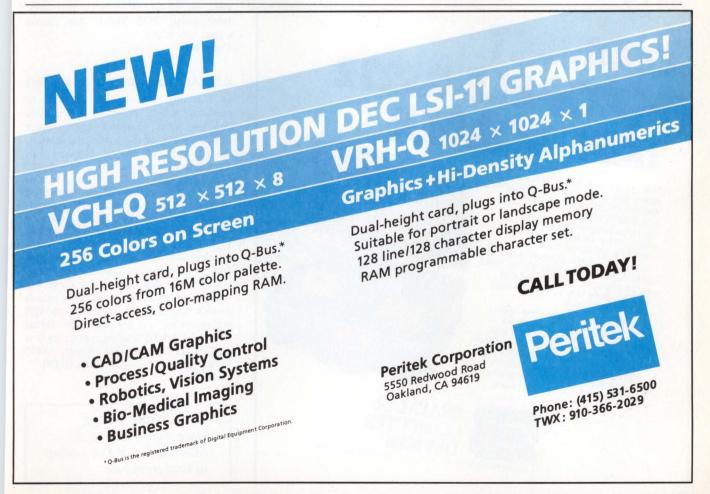
Circle 289

Dual-language programmable controller

CP73P executes a control program written in Tiny BASIC and in process state monitor (PSM) interpretive language. Handling sequential aspects of the application program, PSM can make calls to BASIC subroutines so that arithmetic, terminal 1/0, and other Tiny BASIC functions are accommodated. Program is entered from any ASCII terminal using PSM command chars, and the need to create a ladder diagram is eliminated. The \$625 controller has access to twentysix 16-bit variables, eight 0.01-s resolution timers, and 48 on/off 1/0 channels. Adaptive Automation Technology, PO Box 1339, Sandpoint, ID 83864. Circle 290

Programmable controllers for small computers

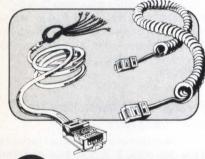
Programmable controller series includes Troll 300 with 8 digital 1/0s and the slightly wider Troll 310 with 16 digital 1/0s. Both are expandable to 256 digital 1/0 modules in groups of 16. Input voltage is 85 to 132 Vac or 170 to 265 (continued on page 186)



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Line Cords (Straight)

Full Modular, 8-position Modular plugs on both ends.

L-D871-BU-BK (unkeyed) L-M871-BU-BK (keyed) *Quarter Modular*, 8-position Modular plug one end, other end ring strain relief and spade tips. L-D871-AB-BK (unkeyed) L-M871-AB-BK (keyed)

Various lengths available

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Serving the electronics communications industries.

CIRCLE 133



SYSTEM COMPONENTS/ GONTROL & AUTOMATION

Vac, 47 to 63 Hz, single phase. Both units are expandable to 128 analog 1/0s in groups of 4. The series, which uses ladder logic, includes 32 timers/ counters, 128 control relays, 64 data registers, message register, and 32 software switch registers. The controllers are \$395 for board-level units. **Conrac Corp**, **Cramer Div**, Old Saybrook, CT 06475. **Circle 291**

SOFTWARE

CP/M on a chip

80150 CP/M combines CP/M-86 OS with essential os hardware on a single silicon device. The component is a processor extension for the 8086, 8088, and 80186 microprocessors. End user licensing is not required, and diskette serialization is eliminated. "Memory disk" capability creates portable, diskless microcomputer workstations by specifying a block of RAM that the 80150 will treat as a std floppy disk. The silicon component will be sampled in the fourth quarter of 1982, priced at \$57.15 in 1k quantities. Intel Corp, 2625 Walsh Ave, Santa Clara, CA 95051. Circle 292

X.25/HASP communications support

MP/X.25 interfaces small computers to public or private networks for realtime 2M-bps serial communications under direct control of the user's application. MP/X.25 supports the DG Network Bus System to interconnect up to 32 Eclipse® computers over 1 mi (1.6 km). It runs under MP/AOS; languages supported include SP/Pascal, MP/Pascal, MP/FORTRAN IV, and MP/BASIC. MP/HASP emulates the IBM HASP RJE workstation. It supports both point to point communications between any DG computer and an IBM 360/370 compatible system, and point to point communications between any 2 DG computers. Line speeds to 4800 bps under MP/OS and up to 9600 bps under MP/AOS are supported. Initial license fee for both MP/X.25 and /HASP is \$1500. Data General Corp. 4400 Computer Dr, Westboro, MA 01580. Circle 293

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World's smallest impact printers

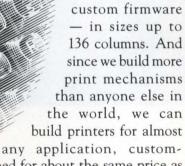
When you need small printers to integrate into calculators, handheld or portable computers, electronic games, or other products, come to Epson OEM. Our 150/160 Series Ultra Micro dot matrix impact print mechanisms are the world's smallest and lightest, yet each is manufactured to standards of precision that yield astonishing reliability.

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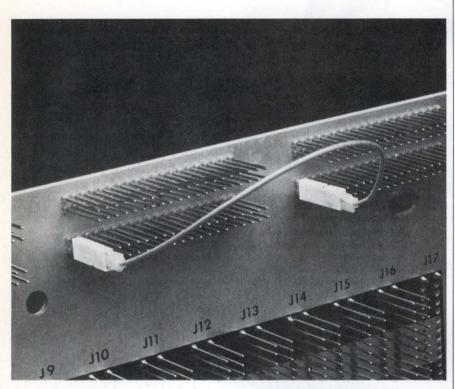


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CIRCLE 96

Low cost array processor has 3.6-ms execution time

AP490 array processor, with execution times of 3.6 ms for a 1024-point real FFT, has a basic configuration of 2k program memory and 4k x 24 bits of data memory. The 4-card set with card cage mountable backplane simultaneously performs 6.3M adds/s, 2.1M multiplies/s, and 1M I/O operations/s. Interfaces for HP 1000 series; PDP-11, LSI-11, VAX; and NOVA and Eclipse are available. The array processor is expandable to 4k words of program memory and 64k words of data memory. Price is \$6450. Analogic Corp, Audubon Rd, Wakefield, MA 01880. Circle 294



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TRANSMISSION LINE SPECIALISTS

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COMPAOTM self-contained system includes a high resolution 9" (23-cm) diagonal video display, 16-bit 8088 microprocessor with 128k-byte RAM (expandable to 256k bytes), a 51/4" floppy disk drive with 320k-byte storage, and room for an optional second 320k-byte floppy. Ports for an optional red-greenblue video monitor, for composite video, and for connection to a std TV set are provided, along with parallel printer interface and socket for an Intel 8087 coprocessor. Asynchronous communications interface is optional. Price is \$2995. COMPAQ Computer Corp, 12330 Perry Rd, Houston, TX 77070. Circle 295

Q-bus compatible computer



System 94 fully integrated DEC PDP-11/23 microcomputer with 70M-byte Winchester and 20M-byte streaming tape provides 256k bytes of MOS RAM (expandable to 4M bytes), 4 serial 1/0 ports, an extended LSI backplane, and 25-ms average access time. Memory management allows direct access of up to 22 bits of address space or 4M bytes of RAM. Floating point processors and an array processor are available as enhancements, along with realtime clock, ADCs and DACs, serial 1/0 multiplexers, synchronous I/O ports, and floppy disk subsystems. The computer sells for under \$20,000. Cambridge Digital Systems, 65 Bent St, Cambridge, MA 02139. Circle 296

MODEMS SHOULD BEHEARD

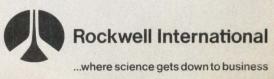
As you can't see, the terminal on the left has a low-cost Rockwell R24DC modern built in. It's connected directly to the U.S. dial-up network with nothing more than a standard telephone jack. No acoustic coupler. No phone. No tangled wires.

It's easy to connect the R24DC modern inside your terminal. It's LSI-based, with the entire 2400 bps modern and data access arrangement on a single 5''x 7.85'' plug-in card. With power requirements of $\pm 12V$ and $\pm 5V$, it consumes only 3 watts.

Rockwell's R24DC integral modems are FCC-registered and both Bell- and CCITT-compatible. And they're widely used in point-of-sale terminals, and for cleaning up PBXs, data concentrators and data communications devices.

To get the inside story on Rockwell modems, call the Electronic Devices Division, Rockwell International at (800) 854-8099.

n California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, California 92660.



AND

SFF



Kiss the 5¹/₄" floppydisk goodbye!

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- Drive has built-in power supply.

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CIDCI E 00

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(quantity one)

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Our 212LP is a low-priced, line-powered modem that's fully 212A-compatible for full-duplex, 1200 bps asynchronous communication only.

No AC connection is required, since operating power comes directly from the telco line. The unit is FCC certified for direct connection to the DDD network and it fits under your telephone handset.

For down-to-earth modem buyers, the message is simple: if 1200 bps capability is all you

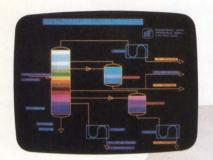
need, that's all you should pay for! Add that saving to the economies of scale in UDS' high-volume delivery capability and you'll find real modem economy. Get details from your UDS distributor, or contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805-1953. Phone 205/837-8100; TWX 810-726-2100.

Universal Data Systems

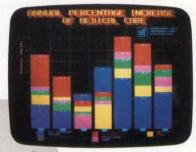
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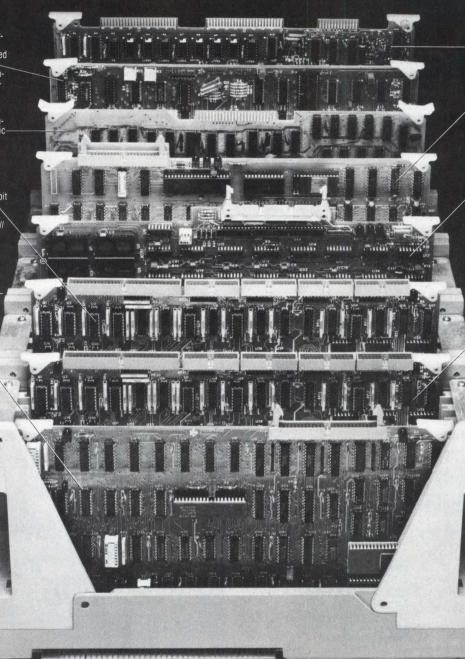
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MC 186 VIDEO MONITOR CON-ROLLER 80 Character X 24 ne alphanumeric and limited raphic display. Upper and wer case. Reverse, half-innsity, flashing, and underne attributes.

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CADMAX-II CAD 2-D system based on high speed, bipolar processors incorporates onscreen menus, vector refresh displays, and human-engineered workstations. Smooth line graphics, clear images, and instant updates are possible. The system features a multitasking os for simultaneous design and plot. The 2-workstation system sells for \$109,700 complete with the 2-D drafting software. One-station and multistation configurations are also available as well as plotter and other output devices. Vector Automation, Inc. Village of Cross Keys. Baltimore, MD 21210. Circle 297

EPROM programming from CP/M files

EPM version 1.1 hardware independent software package programs EPROMS directly from CP/M disk files and allows existing EPROMs to be read directly to a disk file. EPROM programmer I/O routines in source form provide custom interfacing to EPROM programming hardware. Program is menu driven and automatically verifies EPROM erasure prior to programming. Utility is included for hex file conversion. Program runs under CP/M version 2.0 or later with at least 24k RAM. Package is \$75. Dantek Software, Inc, 4550 Schoolhouse Rd, Batavia, OH 45103. Circle 298

Development system for single-chip micro

Microcomputer development environment (MDE) chip system develops/debugs applications for the T-11 single-chip microcomputer via realtime in-circuit emulation. MDE comprises a tabletop LSI-11/23 based system, buffered T-11 emulation hardware, and associated software. For use with VAX and PDP-11 computers using MACRO-11 programming language, system enables software to be downline loaded into the target circuit. Host communications are via an RS-232 compatible serial asynchronous line. Price is \$24,900. Digital Equipment Corp, Maynard, MA 01754. Circle 299

Development system supports CIMBUS™ microcomputer

COMMANDER/800TM development system. optimized for CIMBUSTM microcomputer systems, features a complete development software package, dual-floppy disk drives, RS-232-C ports, and front access to all 16 CIMBUS card slots. A single-card cage holds both the target system and cards that control software/ hardware development. During debug, development cards exercise, monitor, and control the target system via standardized CIMBUS bus. System includes a CPU card with CMOS NSC800 microprocessor that executes Z80 software. Standard system is \$9950. Micro/Sys, 1367 Foothill Blvd, La Canada, CA 91011. Circle 300



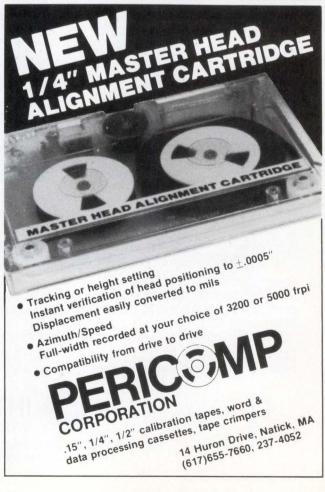
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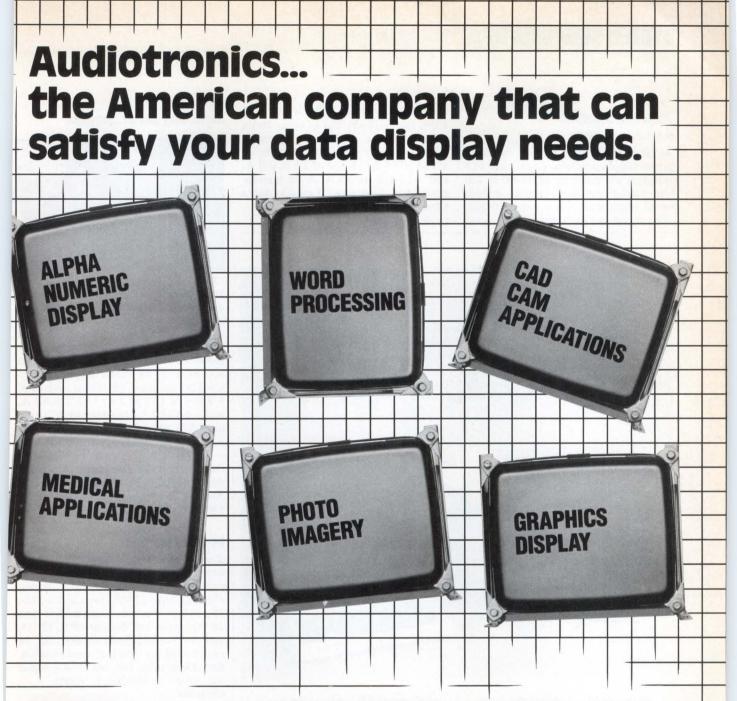
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CIRCLE 104



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CIRCLE 105

SYSTEM COMPONENTS/ POWER SOURGES & PROTECTION

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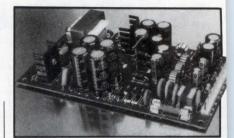
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DC-DC converters

The EP series single-output mini dc-dc converters include 4 models with 5-Vdc input and 5-, 12-, 15-, and 24-V output; 4 models have 12-Vdc input and 5-, 12-, 15-, and 24-V output. Four models have 24-Vdc input and outputs of 5, 12, 15, and 24 V. Additional models can be customized to specific requirements. **KSC Electronics, Inc,** 543 W Algonquin Rd, Arlington Heights, IL 60005. Circle 303

DATA CONVERSION

1.5-VA output, 16-bit DRC

Offering 8- and 16-bit microprocessor compatibility, the HDR2106 hybrid digital to resolver converter provides 1.5-VA output drive, 16-bit resolution, and 1 arc-min accuracy. Double-buffered inputs, 0.03% vector accuracy, and fully protected analog sine and cosine outputs are featured. Packaged in a 32-pin triple DIP, the converter does not require a 5-V logic supply. Digital inputs are TTL/CMOS compatible. Output power stage can be driven by ± 15 Vdc or pulsating supplies. Output protection is provided. Price is \$495. Natel Engineering Co, Inc, 8954 Mason Ave, Chatsworth CA 91311. Circle 304

198 COMPUTER DESIGN/January 1983

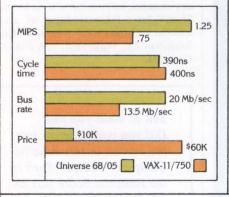
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TITUTI

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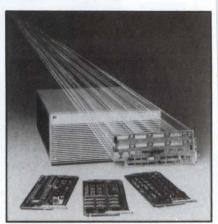
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SYSTEM COMPONENTS/ DATA GONVERSION

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HP 69752A 64-channel and HP 69755A 16-channel scanner cards for the HP 6942A multiprogrammer use FET switching to scan single-ended voltage channels at speeds up to 25k channels/s. Up to 960 channels in the \pm 10.24-V range can be scanned by cascading up to 14 scanner cards in a single multiprogrammer. Both random access and sequential scan measurements can be made. The 64-channel scanner card costs \$1200; the 16-channel costs \$550. A scan control/pacer card, for use with multicard scanners, is \$650. Call local **Hewlett-Packard** sales office. **Circle 305**

Simultaneously sampling ADC

Self-contained 2-channel ADC model A/D/A/M-822 has input sample and hold amplifiers, stable reference source, and 12-bit ADC. The simultaneously sampling, 0.025% accurate system has 5-ns aperture uncertainty time. Output codes are natural binary, offset binary, or 2's complement. Four analog inputs can be chosen in 2 groups of 2 each. Better than 110-dB interchannel crosstalk isolation is ensured. Offset error on any channel, adjustable to 0, is less than 25 mV for a full-scale input of ± 10 V without adjustment. Analogic Corp, Audubon Rd, Wakefield, MA 01880. Circle 306

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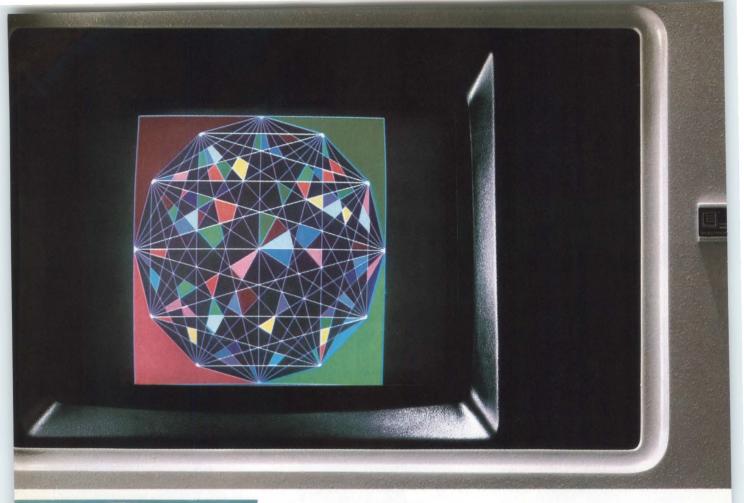
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TRAFFIC SNA Q





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SYSTEM COMPONENTS/ MIGROPROGESSORS/ MIGROGOMPUTERS

DEC compatible microcomputer



MDP-11 microcomputer system has builtin LSI-11 microcomputer, hard and floppy disk, or cartridge tape system. Disk and tape systems are compatible with std DEC RL01/02, RX01/02, and TM-11. 4M-byte direct addressing is provided. RT-11, RSX-11M, and RSTS-11 operating systems are accommodated. Either 0.5M- or 20M-byte removable media and 5M- or 10M-byte hard disk are provided. MEDICOM/Medische Elektronica en Computer Systemen, Postbus 2070, 2800 BE Gouda, The Netherlands. Circle 307

Z80A/B based microcomputer

DSB-4/6 single-board Z80 microcomputer has 64k RAM and a choice of 4- or 6-MHz CPUs. Disk controller automatically interfaces with both 51/4" or 8" drives in either single- or double-density recording formats. DMA is fully supported. Up to 3 RS-232 serial I/O ports, a modem port, and a std Centronics style parallel port are provided. For hard disk interface, a second parallel port provides 8-bit bidirectional 1/0, address lines, read/write, data and interrupt requests, and data enable. Single-unit price range is \$695 to \$995. Davidge Corp, 1951 Colony St, Mountain View, CA 94043. Circle 308

Single-board computer

HART-09 single-board standalone computer is based on the MC6809 microprocessor. It features a std RS-232 port, five 16-bit timer/counters, an 8-bit DAC, 1k bits of nonvolatile RAM, 64k EPROM and RAM memory, hex keypad interface, and a general purpose parallel port for interface with a digital display, printer, floppy disk, or other peripheral. Modular multitasking OS interfaces with most 1/O devices. Application programs can be written in BASIC, assembly, COBOL, or Pascal. **Hart Scientific**, PO Box 934, Provo, UT 84630. **Circle 309**

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CIRCLE 139 COMPUTE

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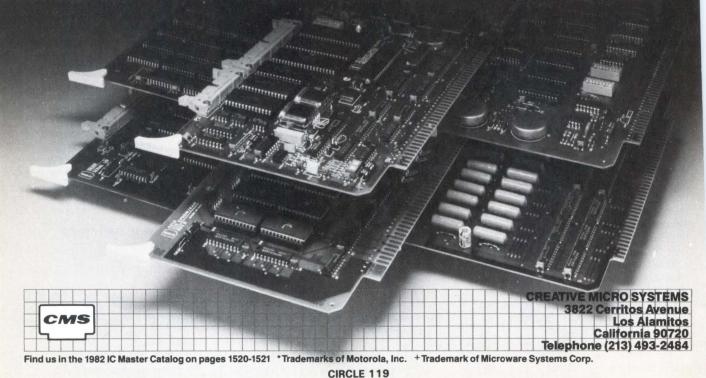
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CMOS 8-bit A-D peripheral chips

Series of A-D ICs interfaces analog inputs to 8- and 16-bit microprocessor systems and features an 8-line TTL compatible 3-state bidirectional data bus. The TL530, TL531, TL532, and TL533 can be addressed by, and supply data directly to, memory, microprocessors, or other peripherals. Onchip multiplexers and 16-bit analog/ digital data registers are provided. TL530 and TL531 (\$8.97 and \$4.81) are 40-pin devices that accept up to 15 analog inputs and 12 digital inputs. TL532 and TL533 (\$7.34 and \$4.32) are 28-pin versions that handle up to 11 analog and 6 digital inputs. Texas Instruments Inc, PO Box 202129, Dallas, TX 75220. Circle 310

Single-chip logic arrays combine digital/linear functions

ULA Digilin logic arrays, with digital and linear functions on the same chip, range from 100 gates with 356 active and 531 passive components to 730 gates with 1644 active and 2660 passive components. Packed with 14 to 40 pins, the devices can form precision references, voltage regulators, comparators, amplifiers, or sample and hold circuits. Std predefined support functions required by digital signal conditioning of analog circuits are included. Interconnection pattern is generated from user's specs. Development range is \$8000 to \$40,000. Ferranti Semiconductors, 87 Modular Ave, Commack, NY 11725. Circle 311

Pulse width modulator with bandgap reference

SG1524B single-chip pulse width modulator features undervoltage lockout, double-pulse suppression, and improved current limiting. Output transistor voltage is 60 V max; output drive is 100 mA max (200 mA pk) from 50 mA. Bandgap reference lowers min supply voltage to 7 V, allowing battery powered portable applications. Reference also lowers typ output noise voltage, improves longterm drift, and decreases turn-on drift. Available in mil, industrial, and commercial grades, price in 100-piece 16-cerDIP ranges from \$4.55 to \$13.90; device is \$4.30 in a 16-pin plastic DIP. Silicon General, Inc, 11651 Monarch St, Garden Grove, CA 92641. Circle 312

6-bit ADC operates at 100 MHz

SPH9756 ADC runs at sampling rates from dc to 70 MHz, with a typ 100-MHz speed with analog inputs up to nyquist frequencies. Latch function onchip sampling eliminates need for external sample and hold. Data clocking through the device in a master/slave configuration ensures outputs are synchronous and valid for the complete clock period. All outputs are ECL compatible. Op temp range is -30 to 85 °C; device meets MIL-STD-883, level B. The 6-bit hybrid ADC, in a 32-pin DIP, is \$560 each in single quantity. Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714. Circle 313

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SYSTEM COMPONENTS/ DATA GOMMUNIGATIONS

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New freedom for 3D digitizers.

Here's great news for users of three dimensional digitizers like our SAC® Model GP-6-3D: New point microphones are now available to provide larger active volumes and to simplify three dimensional motion studies.

Rather than limiting the area to be digitized with a "picture frame" style linear microphone assembly, our new point microphones allow the placement of sonic receivers precisely where needed for digitizing three dimensional objects. This new digitizing technique provides ease of installation and larger active volumes, of direct benefit to those involved in motion studies in areas such as sports medicine, industrial modeling, robotics quality control, animation, and physical therapy. Now, each $6'' \times 2''$ x 31/2''', 8-ounce point microphone assembly can be placed as required to define the active area when digitizing.

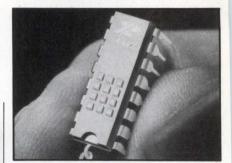
Like standard two dimensional digitizers, 3D digitizers derive distance information by measuring the time required for a sound wave generated by a spark gap built into the point of a stylus to reach a microphone sensor. The distances measured by 3D systems are the slant ranges to each of the sensors; a microprocessor is incorporated to convert this information into X-Y-Z cartesian coordinates. With our GP-6-3D, a multiplexer is available to allow input from 8 individual sound sources, or from 16 sources with the addition of a second multiplexer. This three dimensional digitizing technique is frequently used in conjunction with an intelligent graphics terminal to allow 3D images to be displayed and qualitative measurements performed on the data. Typically, the user may program the graphics terminal to perform a number of functions such as volumetric measurements, as well as rotate and view the image from any angle.

And now, in all cases, our point microphones mean the ultimate in digitizing freedom for you.

Don't you think it's time to learn about our GP-6-3D digitizer and point microphones? The whole story is yours for the asking. We're-ready. We're Science Accessories Corporation, 970 Kings Highway West, Southport, Connecticut 06490, (203) 255-1526.



CMOS single-chip FSK modem



Single-chip XR-14412 contains circuitry necessary to construct a complete FSK modem with simplex, half-duplex, and full-duplex operation. Modem has onboard crystal oscillator. Device operates in answer or originate mode and is pin programmable to either Bell or CCITT standards. Interfacing with CMOS or TTL devices, modem can be programmed for 200, 300, or 600 baud. Operating voltages are 4.75 to 15 V, and 4.75 to 6 V. Unit is a second source to the MC14412. Available in a 16-pin plastic DIP or cerDIP, price range is \$8.88 to \$10.66. EXAR Integrated Systems, Inc, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088. Circle 315

High speed synchronous modem

9600 data modem for 4-wire point to point operation processes 9600 bps of synchronous digital data. Built-in test functions of the CCITT V.29 compatible modem allow a rapid 4-step check of data terminals, modems, and telephone lines. An automatic digital adaptive equalizer overcomes effects of large variations in delay and amplitude distortion. Modem operates at a 2400-baud signaling rate, encoding 4 bits/signal element. If operating conditions deteriorate, fallback rates of 7200 or 4800 bps can be used. **Universal Data Systems**, 5000 Bradford Dr, Huntsville, AL 35805.



Circle 316

Talk to the editors Have you written to us lately? We're waiting to hear from you.

DIALIGHT LED CIRCUIT BOARD INDICATORS STEP UP YOUR PRODUCTION BY MINATIN

You'll save money when you stop mounting LEDs on PC boards the old way - bending leads, inserting holders, adding resistors – and start using LED Circuit Board Indicators from Dialight.

Mounting our LED Circuit Board Indicators is easier and less time-consuming. They eliminate production steps and reduce labor costs. Not only is positioning faster, it's far more accurate. As soon as

you insert the assembly you are ready for wave soldering. Dialight origi-

nated the idea of packaging LEDs for easy

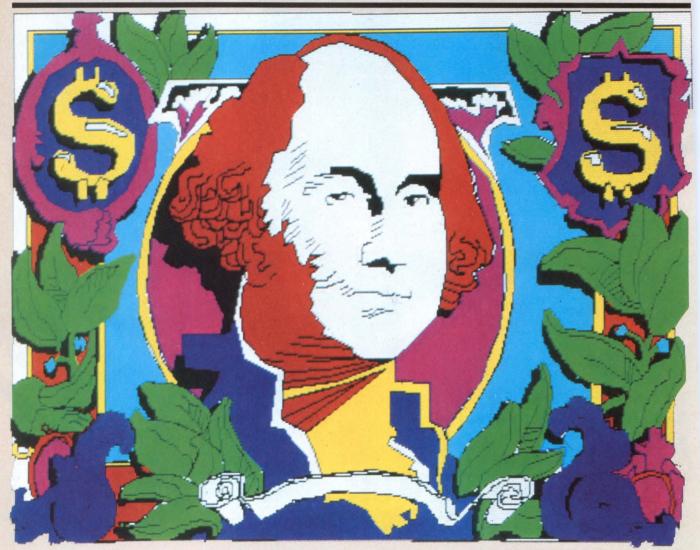
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DIALI meets your needs. A North American Philips Company

How to get a lot more color for your money.



Introducing the HP 2627A Color Graphics Terminal.

Now you can have a bright, sharp image that's easy to read. For only \$5,975. Which means our compact new color graphics terminal is setting completely new price/performance standards.

You get 8 basic colors, plus hundreds of additional user-defined ones. Including colors that match our plotter pens. On a black screen with 512 x 390 line resolution. You get raster display technology for fast, selective screen updates. You get vector graphics and polygonal area fills, a combination that makes it easy to create complex shapes, symbols, and even typestyles. In a lot less time. With a lot more precision.

Of course, it's also software-compatible. In addition to HP's DSG/3000 and Graphics/1000-II software, the 2627A runs PLOT 10 from Tektronix, SAS's SAS/GRAPH, Precision Visual's DI-3000 and GRAFMAKER, ISSCO'S DISSPLA and TELL-A-GRAF.

But that's not all; the 2627A has

user-definable softkeys and graphics edit keys that make this one of the easiest-to-use terminals on the market. It even gives you complete alphanumeric Actual unretouched 35mm slide taken directly from screen.

capability. In a separate memory. So whether you're interested in business or technical applications, just return this coupon and we'll send you more information. Or call your local HP sales office. We're listed in the white pages.

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CIDCLE 111

Positive protection for personal computers.





Airpax magnetic circuit breakers.

Whether the surroundings are hot or cold, Airpax magnetic circuit breakers' minimum trip current is not affected by temperature extremes, as is the case with fuses and thermal devices. These "trip-free" breakers won't stay closed on an overload even if the handle is held in the "on" position. Their built-in inertia delay avoids nuisance trip-outs due to transient surges.

Designed to conform with VDE and IEC standards 380 and 435, Airpax SNAPAK[®] breakers make your product ready for export markets. A wide choice of handle actuations, colors, illumination, terminals and hardware gives you the styling and selection you want. They are tested, listed and qualified under various military, UL, CSA and SEV specifications. Proven performance has made them the choice of leading manufacturers of computers, peripherals, broadcast equipment and machine controllers.

Because they combine the functions of power switching and overload protection and have zero replacement requirements, Airpax breakers are an affordable option to fuse-switch combinations.

For complete specifications, write or call Airpax Corporation, a North American Philips Company, Cambridge Division, Woods Road, P.O. Box 520, Cambridge, MD 21613. (301) 228-4600.



CAMBRIDGE DIVISION

PAYEE J.B. HDWR. GMAC Peco Acme

At last, plug-in parallel processing in a 32-bit supermini system.



Perkin-Elmer announces the Model 3200 Multiple Processing System, an exciting new concept for demanding real-time applications.

Room to grow

The Model 3200MPS gives you extraordinary system expandibility. You can start with a host CPU and one auxiliary processing unit (APU). Then as your needs grow you can plug in more performance by adding as many as eight additional APUs.

Should you need even more horsepower, plug-in parallel processing lets you add exactly what you need as you need it from a single APU to a whole fleet of multiple processing systems.

And no matter what the size of your configuration, a central point of control and management is provided by a single copy of our fieldproven OS/32 operating system. **Design flexibility**

With parallel-processing APUs you can take advantage of application segmentation and structured programming techniques to speed system development. You can segment your application into multiple task modules, with each APU performing a set of related functions. To further optimize system performance, you can easily re-allocate tasks among the APUs.

Your Model 3200MPS provides maximum flexibility for software development, reliability, and system maintenance. To incorporate new design changes or correct problem modules, simply work on the problem module while your system continues to operate. And the Model 3200MPS can be structured to permit continued system operation though one or multiple APUs may fail. When so structured, the APUs can receive immediate maintenance attention while the system continues to run or they can wait for routine scheduled maintenance.

And our state-of-the-art universally optimizing FORTRAN VIIZ enables you to use modular programming techniques without sacrificing real-time efficiencies.

To find out more about how you can plug into all the advantages of plug-in parallel processing minis, mail the coupon or call today: The Perkin-Elmer Corporation, Two Crescent Place, Oceanport, NJ 07757.

Tel: 800-631-2154. In NJ, 201-870-4712.



8" half-height flexible drive



Model FD1164 flexible disk drive is a single-sided, single-density version of the FD1165 double-sided, double-density 8" drive. Unformatted capacity is 400k bytes. Included are built-in NEC interface with 3M type connector or with variable frequency oscillator (VFO) option, and std Shugart type interface with edge card connector or vFo option. Microprocessor controls head loading mechanism that extends media life to more than 7M passes, spindle speed, and internal diagnostics. Drive is \$475 in quantities of 100. NEC Information Systems, Inc, 5 Militia Dr, Lexington, MA 02173. Circle 317

Half-height Winchester uses thin-film disks

ST206 half-height 51/4" Winchester drive incorporates thin-film plated media and ferrite R/W heads. It stores 6.38M-byte max unformatted data (5M bytes formatted) on 2 surfaces of a single film plated rigid disk. Drive is fully compatible with std ST506 interface. Data density is 10,416 bytes/track on a total of 306 cylinders. Transfer rate is 5M bps. Average access is 85 ms (including settling) using a split-band positioner and stepper motor driven actuator. Price is \$745 in quantities of 500. Evaluation units will be available in the first quarter 1983. Seagate Technology, 360 El Pueblo Rd, Scotts Valley, CA 95066. Circle 318

DEC replacement drives

Increased capacity Micro-Magnum 5/5 fixed/removable cartridge and Micro-Magnum 5 removable-only disk drives provide a 5¼" replacement for DEC's RL01 and RL02 disk drives. Cylinder count is increased from 312 to 320/disk, giving Micro-Magnum 5/5 formatted capacity of 10.48M bytes and Micro-Magnum 5 formatted storage of 5.24M bytes. The drives have an embedded servo and SASI interface. Micro-Magnum 5/5 OEM price is \$1275 and the Micro-Magnum 5 is \$995. DMA Systems Corp, 601 Pine Ave, Goleta, CA 93117. Circle 319

SYSTEM ELEMENTS

VMEbus compatible boards

Three single-function general purpose modules include VME-SBC (\$1695) singleboard 6800 microprocessor based computer that features 12k-byte static RAM and 2 monitor/debugger PROMS. Optional version (\$1555) features 4k-byte static RAM and 6 empty BytewydeTM memory sockets for std 2764 EPROMS, VME-DRAM 256 (\$2395) 5-V RAM board has 256k-byte memory and onboard refresh. This dualconnector memory card features selfcontained Bytewyde parity generation/ checking. Double-Eurocard serial 1/0 VME-SIO (\$925) features 2 fixed RS-232 channels and a population option of 2 RS-232 OF RS-422 channels. Mostek Corp, a sub of United Technologies Corp, 1215 W Crosby Rd, Carrollton, TX 75006. Circle 320

Low cost R-D converter

160B series resolver to digital converters provide up to a 4:1 reduction in the cost of angle or distance encoding in robotic/ machine tool applications. Total monitoring costs are \$100/axis including brushless resolver. Single low profile module comprises a complete 4-channel resolver or synchro to digital converter. Four- or 8-channel expansion modules can be added up to a max 40 input channels. Device provides 12-bit resolution, 8.5-min accuracy, and less than 100-ms conversion time. Logic 1/0s are TTL/CMOS compatible. Four-channel unit is \$495. Control Sciences, Inc, 9601-1 Owensmouth Ave, Chatsworth, CA 91311. Circle 321

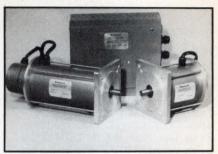
Wideband fast settling op amp

AH0605 op amp, available in 3 drift grades, is suited for both ac/dc applications. Settling time is 400 ns max to 0.1%. The 400-MHz gain bandwidth product slews at 500 V/ μ s. Output current is \pm 30 mA at \pm 10 V. Gain is 80 dB min at \pm 30-mA output. Voltage offset and drift is 5 mV max, 10 μ V/°C. Prices range from \$37.50 to \$53 in 100-piece quantities. **Optical Electronics Inc**, PO Box 11140, Tucson, AZ 85734. **Circle 322**

Like to write?

The editors invite you to write technical articles for Computer Design. For a free copy of our Author's Guide, circle **503** on the Reader Inquiry Card.

Brushless motors



Line of brushless servo and general purpose permanent magnet motors includes over 50 listings with ratings from 0.1 to 1 hp and up to 32 1b/in (4N·m) continuous torque at stall. Motor life exceeds 15k h, rfi/emi are virtually eliminated, and speed is to 7200 rpm. Magnets are on the rotor, and motor windings are the stator. Windings are held stationary and can be commutated electronically to eliminate need for a mechanical commutator and brushes. Three Hall effect sensors are provided. Brushless tachometer uses the same internal electronic commutation as the brushless motor. Honeywell, Inc. Motor Products Div. PO Box 106, Rockford, IL 61105. Circle 323

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Cordially,

Bob Dromgoole

Robert P. Dromgoole Circulation Director

CALENDAR

CONFERENCES

FEB 21-23—Office Automation Conf, Civic Ctr, Philadelphia, Pa. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3614

FEB 23-25—ISSCC (Internat'l Solid State Circuits Conf), Sheraton Center Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 28-MAR 4—Compcon Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 8-10—Localnet, London, England. INFORMATION: Online Confs Ltd, Argyle House, Northwood Hills, HA6 1TS, Middx, U.K. Tel: Northwood 09274/28211; 44/9274 28211 (internat'l)

MAR 10-12—Internat'l Computer Color Graphics Conf, Tallahassee-Leon County Civic Ctr, Tallahassee, Fla. INFORMATION: Ron Spencer, 555 W Pensacola St, PO Box 10604, Tallahassee, FL 32302. Tel: 904/487-1691

MAR 14-16—Phoenix Conf on Computers and Communications, Phoenix, Ariz. INFORMATION: Gerald Fetterer, GTE Automatic Electric Lab, 2500 W Utopia, Phoenix, AZ 85027

MAR 21-24—Interface, Miami Beach Conv Ctr, Miami Beach, Fla. INFORMATION: The Interface Group, 160 Speen St, PO Box 927, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 21-24—Powercon 10 (Internat'l Power Electronics Conf and Exhibit), Sheraton Harbor Island Hotel, San Diego, Calif. INFORMATION: Ronald Birdsall, Gen'l Chmn, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/656-1890

MAR 22-23—Office Automation Conf and Expo, Holiday Inn Mövenpick Hotel, Zurich-Regensdorf, Switzerland. INFORMATION: Foreign Commercial Service, American Embassy, PO Box 1065, CH-3001, Bern, Switzerland. Tel: 031/437011

APR 4-8—Tutorial Week East (including sessions on interactive computer graphics; robotics; data communication; and software design, development, management, and testing), Orlando, Fla. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142 APR 5-8—Communications Tokyo, Tokyo Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak Internat'l, PO Box 70007, Washington, DC 20088. Tel: 301/657-3090

APR 18-21—Internat'l Sym on Industrial Robots/Robots 7 Conf and Expo,

Conrad Hilton Hotel and McCormick PI, Chicago, III. INFORMATION: Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

APR 19-21 — Electro, New York Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Eileen Algaze, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 19-21 — Mini/Micro-Northeast, New York Conv Ctr, New York, NY. INFORMATION: Eileen Algaze, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 27-29—Satellite and Computer Communications Internat'l Sym, Versailles, France. INFORMATION: T. Bricheteau, Secretariat du Symposium, Domaine de Voluceau, Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France. Tel: 3/954.9020; Poste 600

MAY 2-5—Test and Measurement World Expo, San Jose Conv Ctr, San Jose, Calif. INFORMATION: Meg Bowen, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

MAY 9-13—SID (Society for Information Display) Internat'l Sym, Marriott Hotel, Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables FL 33134. Tel: 305/446-8193

MAY 16-19—National Computer Conf, Disneyland Hotel and Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3624

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

SEMINARS

MAR 7-11—Computer Aided Engineering and Manufacturing Seminars and Exhibition, North Carolina State Univ, Raleigh, NC. INFORMATION: R. L. Edwards, Industrial Extension Service, North Carolina State Univ, PO Box 5506, Raleigh, NC 27650. Tel: 919/737-3470

MAR 21-23—Digital Control, Boston, Mass. INFORMATION: Hellman Assocs, Inc, Dept R, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

SHORT COURSES

FEB 14-18—Database Concepts and Design, San Francisco, Calif. INFORMATION: American Mgmt Assocs, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

FEB 15-18—Peripheral Array Processors for Signal Processing and Simulation, Univ of California, Los Angeles. INFORMATION: Marc Rosenberg, UCLA Extension, Continuing Ed in Engineering and Math, 6266 Boelter Hall, Los Angeles, CA 90024. Tel: 213/825-1047

FEB 23-25—Local Communication Networks and Digital PBXs; AND FEB 28-MAR 4—Computer Communication Systems and Networks, George Washington Univ, Washington, DC. INFORMATION: George Washington Univ, Continuing Engineering Ed, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

FEB 23-25—Practical CAD/CAM Considerations (Concept through Operation), Univ of California, Los Angeles. INFORMATION: Marc Rosenberg, UCLA Extension, Continuing Ed in Engineering and Math, 6266 Boelter Hall, Los Angeles, CA 90024. Tel: 213/825-1047

MAR 21-24—Personal Microcomputer Interfacing and Scientific

Instrumentation Automation, Virginia Polytechnic Institute and State Univ, Blacksburg, Va. INFORMATION: Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. Tel: 703/961-4848

MAR 30-31—IEEE VLSI Test Workshop, Bally's Park Place Casino Hotel, Atlantic City, NJ. INFORMATION: Jerry Kunert, Naval Air Engineering Ctr, Code 92A32, Lakehurst, NJ 08733. Tel: 201/323-2663



LSI-11[®] compatible controller for 80-300MB SMD and Winchester drives from CDC, Ampex, and Fujitsu

Dataram Corporation offers the industry's widest range of DEC-compatible peripheral controllers — from comparatively simple NRZI tape controllers to complex 300 MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11, PDP®-11, or VAX® minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and, more importantly, space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

The chart shows our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.



Princeton Road Cranbury, New Jersey 08512 Tel: 609-799-0071 TWX: 510-685-2542

CONTROLLER	DESCRIPTION	COMPATIBILITY
C03	Cartridge disk controller	RK05
C33	Cartridge disk controller	RK05
Т03	NRZI mag tape controller	TM11/TU10
T04/C	Mag tape streamer coupler	TM11/TU10
T04/N	NRZI mag tape controller	TM11/TU10
T04/D	Dual density mag tape controller	TM11/TU10
T34/C	Mag tape streamer coupler	TM11/TU10
T34/N	NRZI mag tape controller	TM11/TU10
T34/D	Dual density mag tape controller	TM11/TU10
T36	Dual density mag tape controller	TM11/TU10
T34/T	GCR mag tape controller	TM11/TU10
S03/A, S04/A	80 MB/300 MB SMD controller	RM02/RM05
S03/A1, S04/A1	80 MB/160 MB SMD controller	R M02
S03/B	80 MB/300 MB SMD controller	RK07
S03/C	200 MB/300 MB SMD controller	RP06
S03/D, S04/D	96 MB CMD controller	RK06
S33/A	80 MB/300 MB SMD controller	RM02/RM05
S33/A1	80 MB/160 MB SMD controller	RM02
S33/B	80 MB/300 MB SMD controller	RK07
S33/C	200 MB/300 MB SMD controller	R P06
S33/D	96 MB CMD controller	RK06

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LITERATURE

Custom/semicustom chip conversion

Brochure introduces CMOS LSI/VLSI gate array design and fabrication facility, highlighting "technology center" approach to CAE that integrates design, simulation, layout, tooling, and test generation functions while converting discrete or MSI TTL circuits to custom or semicustom ICs. Storage Technology Corp, Microtechnology Div, Louisville, Colo. Circle 410

Test switching system

Booklet examines how TESSTM test equipment switching system can simplify test instrument selection and sharing, fault isolation, test sequencing, excitation, scanning, data acquisition, and record keeping. **T-bar Inc**, **Switching Components Div**, Wilton, Conn. **Circle 411**

Guide to gate array use

Document covers topics that help evaluate existing gate arrays and specify new ones; metal and silicon arrays are described, including the TM5000 (which controls 300 V) and the TM6000 (which provides precision analog functions). Telmos Inc, Sunnyvale, Calif. Circle 412

Versatile multiport modem with network capabilities

Data sheet examines v.29 Plus modem with time division multiplexer that accepts synchronous or asynchronous input with aggregate speeds to 9600 bps; network enhancing features, system applications, and complete specs are discussed. **Timeplex**, **Inc**, Rochelle Park, NJ. **Circle 413**

Indicator and illumination lamps

Miniature, subminiature, and lens-end lamps designated by industry standard numbers are specified in booklet. Gilway Technical Lamp, Woburn, Mass. Circle 414

Isolation transformers and ac line conditioners

Units rated from 100 VA to 60 kVA are outlined in selection guide that discusses ac power problems and suggests appropriate line conditioning devices to solve them. Gould Inc, Electronic Power Conversion Div, San Diego, Calif. Circle 415

Comm network testing system

Brochure profiles integrated REACT remote access and test system, with full Bell System 41009 capabilities. Hekimian Laboratories, Inc, Gaithersburg, Md. Circle 416

Mass-terminated conductors

Bulletin covers MAS-CON[®] insulation displacement connector systems, along with termination tooling and machines. **Panduit Corp**, Tinley Park, Ill. **Circle 417**

Standard relays

General purpose, midget, power, powerminiature, low profile, telephone-type, and automotive-type relays are detailed in catalog, together with sockets and accessories. Schrack North America, Inc, Irvington, NY. Circle 418

International standards

for 19" casings

Brochure summarizes DIN, ANSI/EIA, BSI, and IEC standards and specs for 19" enclosure systems; multidimensional isometric diagrams detail test dimensions, mounting hole patterns, nominal apertures, etc. Schroff Inc, sub of The Schroff Group, Warwick, RI. Circle 419

Matrix programming and switching systems

Handbook highlights single-, dual-, and multideck matrix boards and their applications. Sealectro Corp, Programming Devices Div, Mamaroneck, NY. Circle 420

AC and dc power supplies

Guide presents electrical specs and case dimensions for power sources and switchers in all standard series. Semiconductor Circuits, Inc, Windham, NH. Circle 421

Electrical accessories

Catalog introduces DataGuard spike, transient, and noise protection power conditioners for small computers, as well as electrical and telephone cable ducting. SGL Waber Electric, Div of SGL Industries, Inc, Westville, NJ. Circle 422

Data comm equipment

Synchronous and asynchronous limited distance modems; terminal, port, and modem sharing devices; and modem eliminators are included in product overview. International Data Sciences, Inc, Lincoln, RI. Circle 423

Remote terminal UNIBUS interface

Brochure discusses Series 11 BusDriver, a statistically multiplexed remote cluster and local terminal interface for DEC PDP-11 and VAX-11 computers. **Micom Systems, Inc,** Chatsworth, Calif. Circle 424

Design application notes

Five new application notes are available: "PROMS, PALS, FIFOS, and Multipliers Team Up to Implement Single-Board High Performance Audio Spectrum Analyzer"; "A Dedicated Multiplier/ Divider Speeds Up Multiplication and Division for 8-Bit Microprocessors"; "FIFOS: Rubber-Band Memories to Hold Your System Together"; "Big, Fast, and Simple—Algorithms, Architecture, and Components for High-End Superminis"; and "Using ADPCM for Image Compression." Monolithic Memories, Inc, Sunnyvale, Calif. Circle 425

Switch components and assemblies

Guide covers operating and performance characteristics, circuit configurations, and mounting instructions for a range of switches, keypads, ac and dc solenoids, and power relays. **Oak Switch Systems Inc**, Crystal Lake, Ill. **Circle 426**

Standard filters for custom needs

Brochure describes how to specify standard design filters to meet custom filter requirements, and profiles normalized filter-response curves at any impedance or cutoff frequency within wide feasibility ranges. **OPT Industries Inc**, Phillipsburg, NJ. **Circle 427**

Computer power conditioners

Product guide outlines standard and optional features of 17 WhisperPac models ranging from 12.5 to 500 kVA, tabulates specs and efficiency ratings, and summarizes installation, maintenance, and warranty information. **Computer Power Products**, Gardena, Calif.

Circle 428

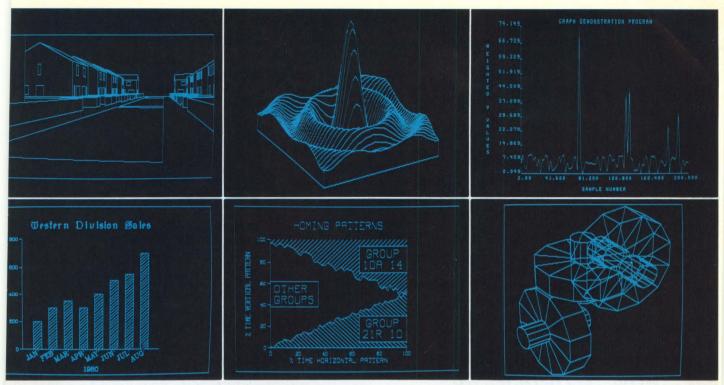
Signal converter and terminating unit

Solid state, plug-in module STU-5M interfaces tactical or fixed 2- or 4-wire telephone equipment with 4-wire VF channels and converts ringing and dc supervision to tone on/off signals; leaflet includes performance characteristics and logistic support data. **Dataproducts New England, Inc,** Wallingford, Conn. **Circle 429**

Flexible flat cables

Catalog displays complete line of PVC insulated cables for use with masstermination, insulation displacement connectors. **Hitachi Cable America Inc**, New York, NY. **Circle 430**

214 COMPUTER DESIGN/January 1983



Give your VT100 a new image in 4.4 minutes.

If you have a VT100 terminal, you're just 4.4 minutes away from a high quality, versatile graphics system. At a very low price.

Our SG100 Plus graphics enhancement gives you full Tektronix[®] 4010 emulation on DEC[™] VT100, 103, 105, and 132 terminals.

But chances are you'll prefer our built-in native mode graphics capability, a powerful tool that makes it easy to program graphics applications. Even if you're not a programmer.

You won't have to give up your regular VT100 capabilities. And our separate graphics memory means you can switch from graphics to standard mode without losing data.

Our features have exceptional drawing power.

There are a lot of other reasons why our retro-fitted graphics are the best choice: Higher X-axis resolution than the competition. Larger addressable plot area, too—65K x 65K dots. The SG100 Plus printer port is totally transparent to the system, so you can print alphanumerics and graphics interchangeably on one printer. Cross hair cursor and light pen options. And our easy-to-use software is compatible with many operating systems.

High quality graphics on your LA120. If you have an LA120 printer, our SG120R board can

If you have an LA120 printer, our SG120R board can give it fast raster graphics capabilities. We can also interface with many other popular printers.

If you want to give your VT100 a new image, call Selanar. We're the experts in high-quality, low-cost graphics.



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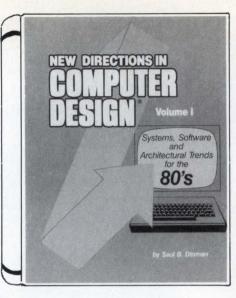
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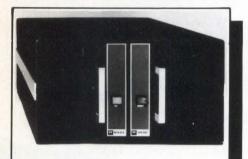
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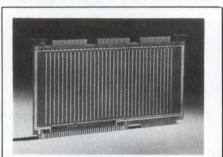


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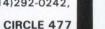
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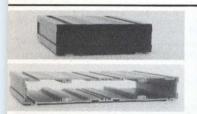


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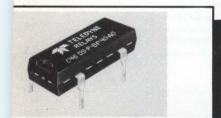
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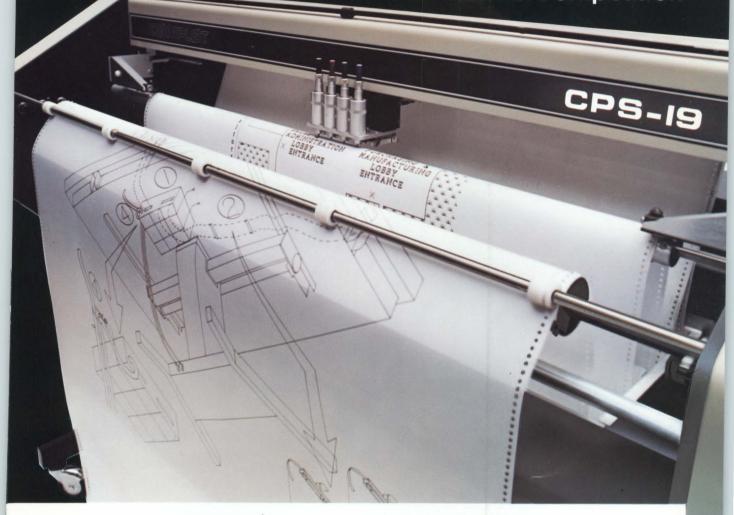
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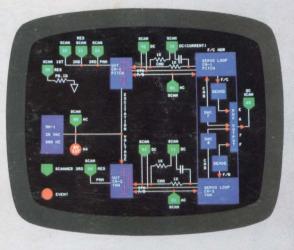
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