

Christoph Eck on:
Real-time standards

A PENNWELL PUBLICATION

OCTOBER 1991

COMPUTER DESIGN

*Technology
and Design
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



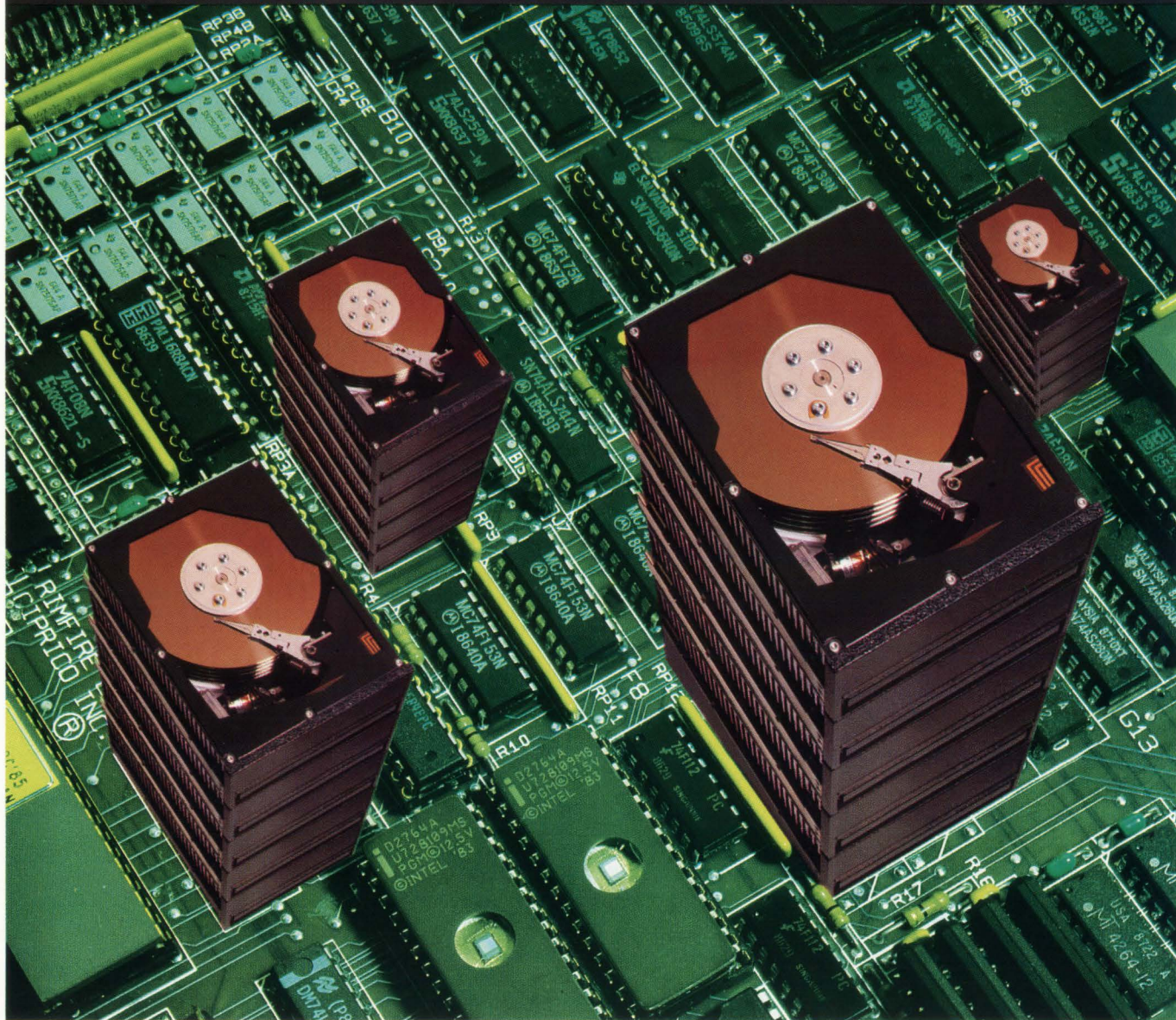
RISC champions challenge Moto in embedded control

RISC-based boards make headway
in real-time applications

Pinouts and performance
drive PAL choices

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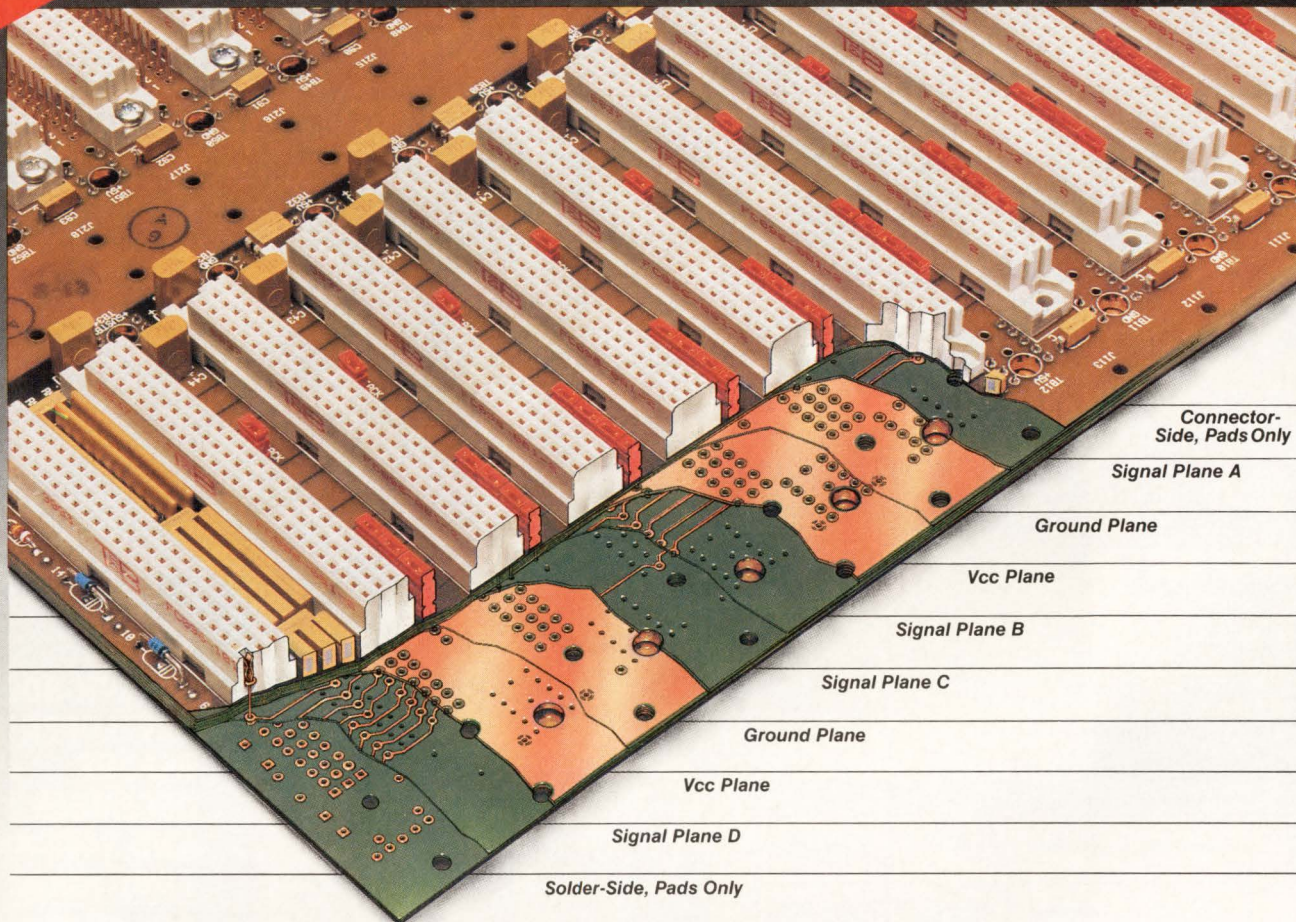
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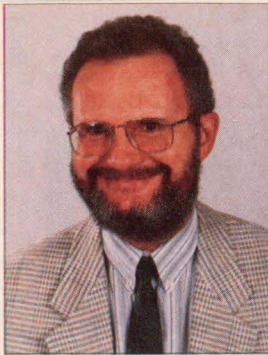
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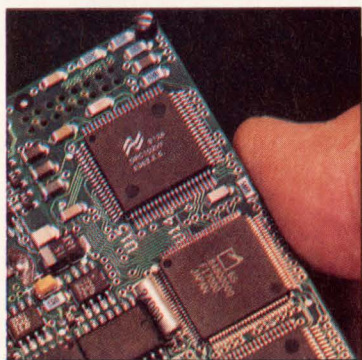


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COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



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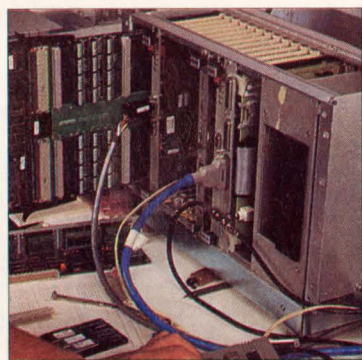
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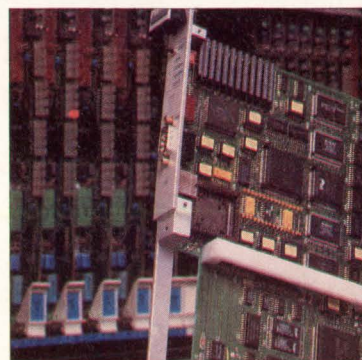
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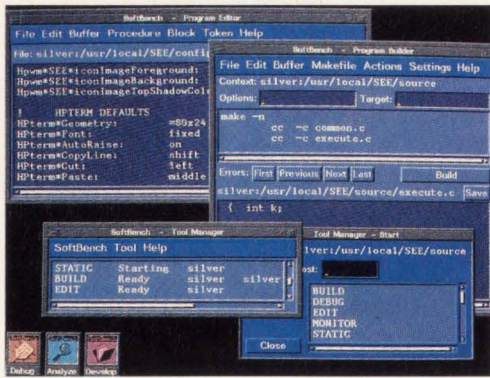
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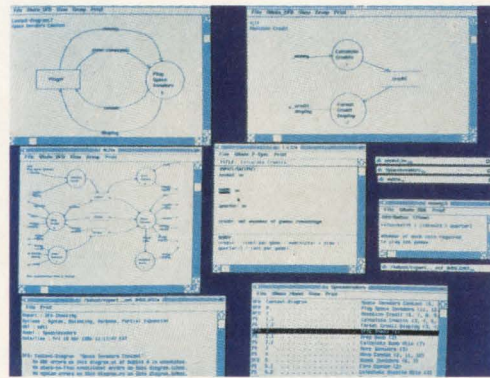
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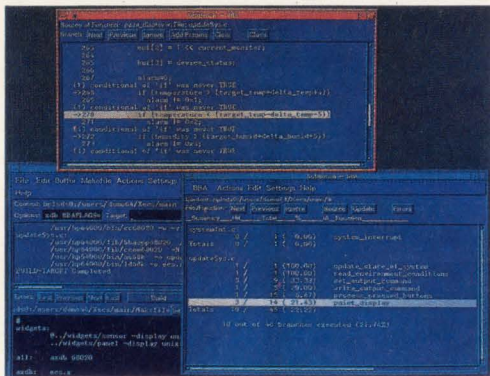
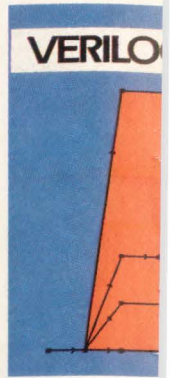
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HP's SoftBench: A tool integration framework and a program construction toolset.

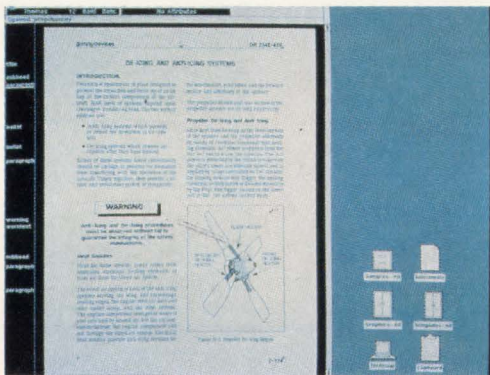


Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.

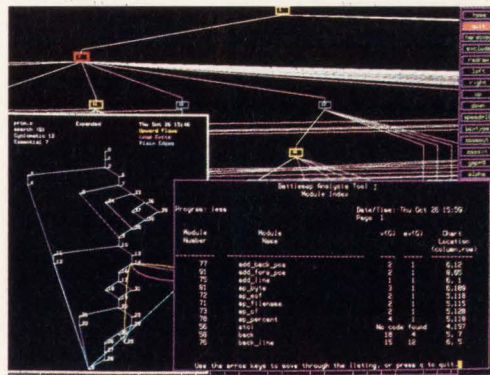


HP Branch Validator: Provides accurate branch information quickly and easily, reducing software test time while increasing confidence.

Best CA

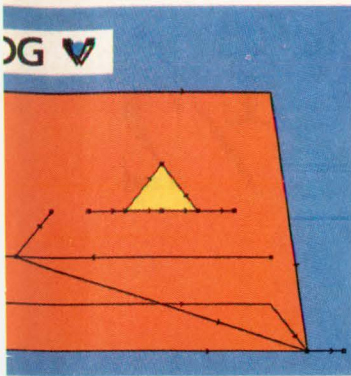


Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.

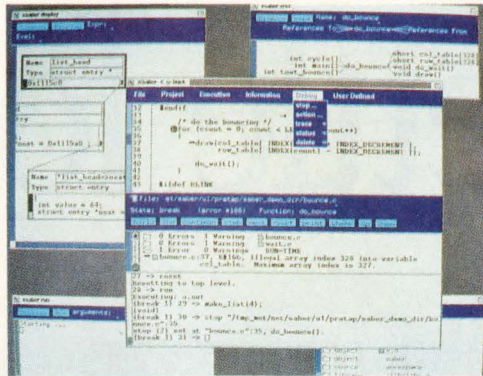


McCabe Test Tools: An automated software testing and reverse engineering application.

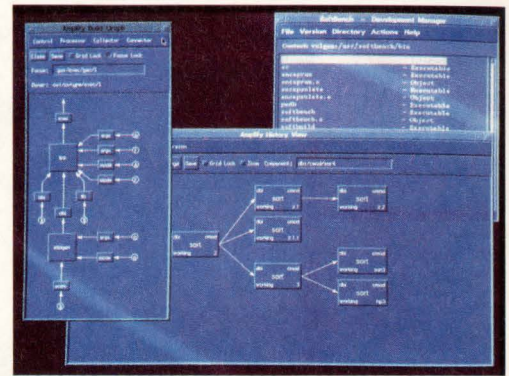




Verilog LOGISCOPE:
Automated testing of source code analysis for reverse engineering.

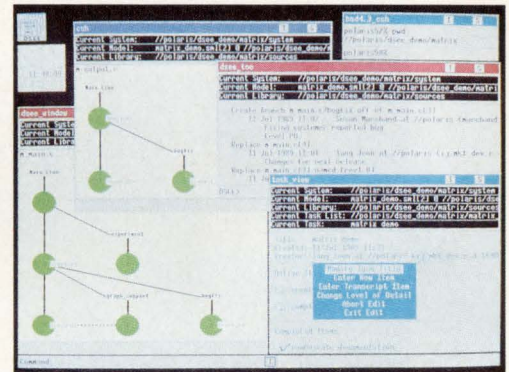


Saber-C: A set of integrated tools for development, testing, maintaining and debugging C programs.



CaseWare® AMPLIFY® CONTROL:
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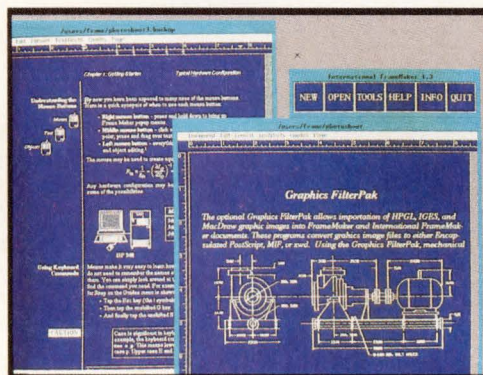
SE scenario.



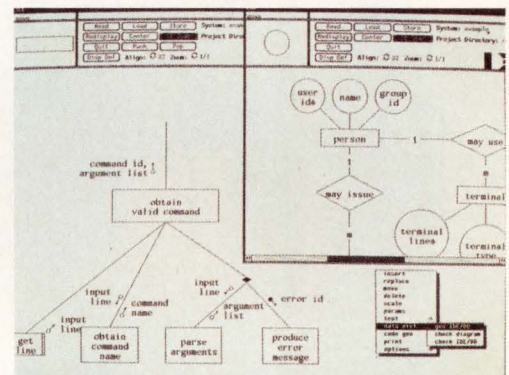
Apollo DSEE: Offers unequaled software development support and configuration management for complex, team-oriented projects.



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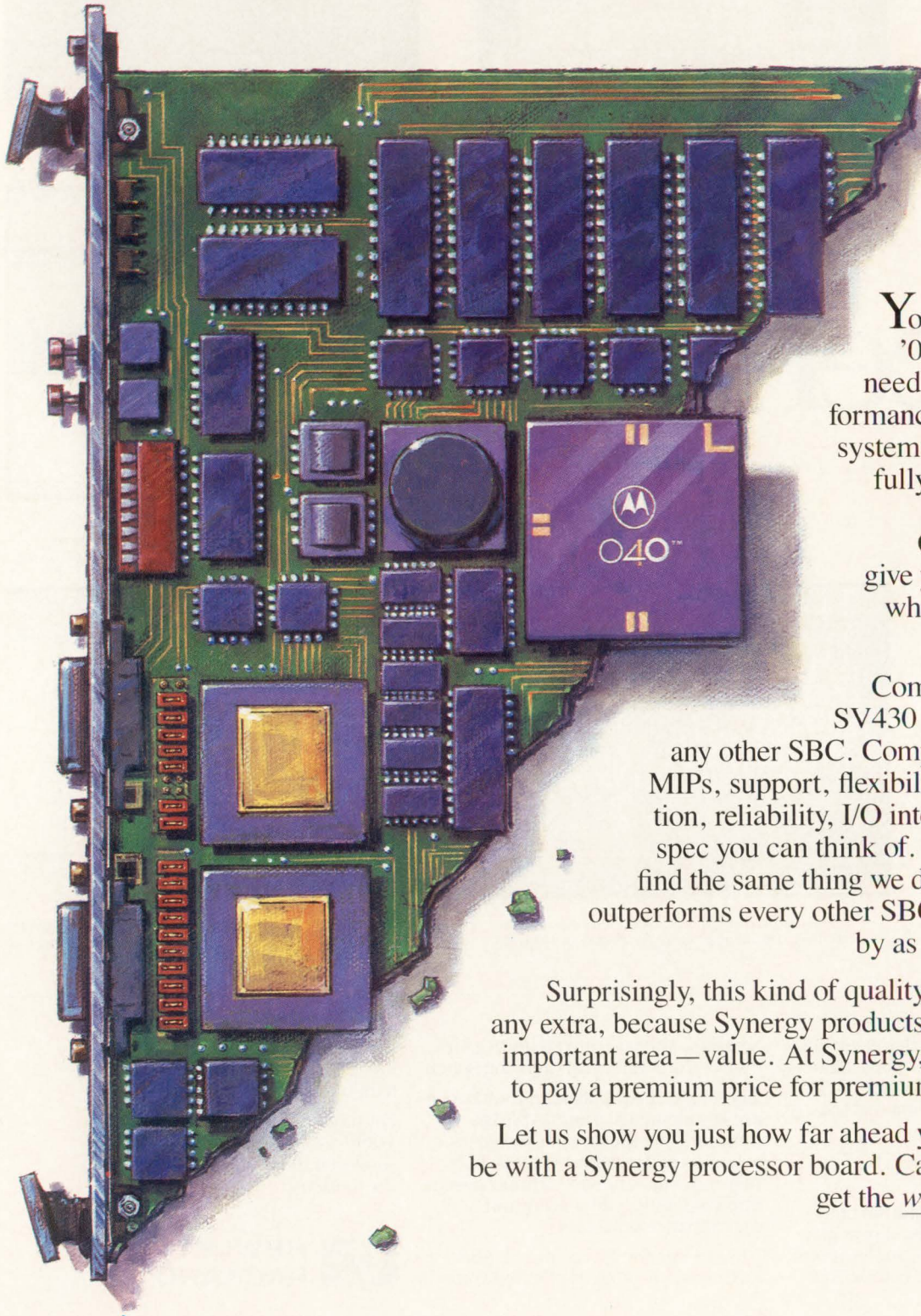
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Why Settle for 1/2



You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may give you only half of what you expected from the '040.

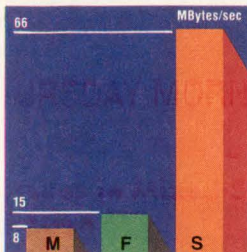
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPS, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the whole '040 story.

an '040 Board?

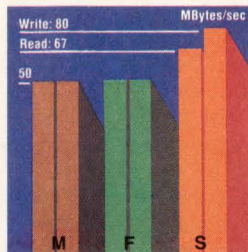
Compare our specs.
Synergy is superior across the board!



VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison.

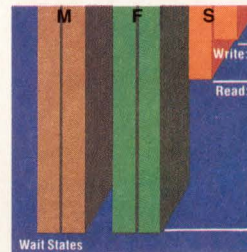
Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



DRAM Burst Rates

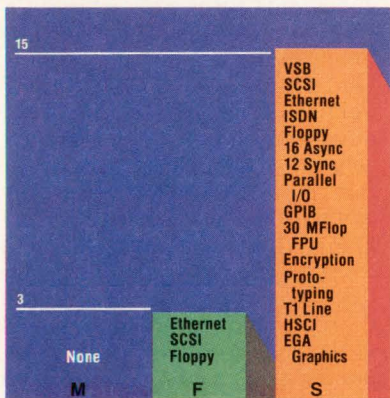
A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining.

SV430 bursts are 26% faster than Force and Motorola.



DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

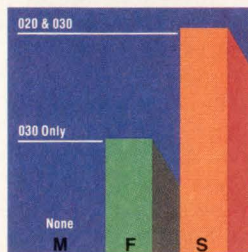


I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

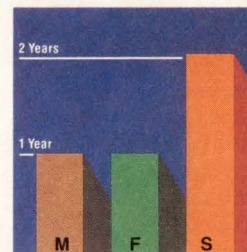
VME64 is a trademark of Performance Technologies, Inc.



'020/'030 Compatibility

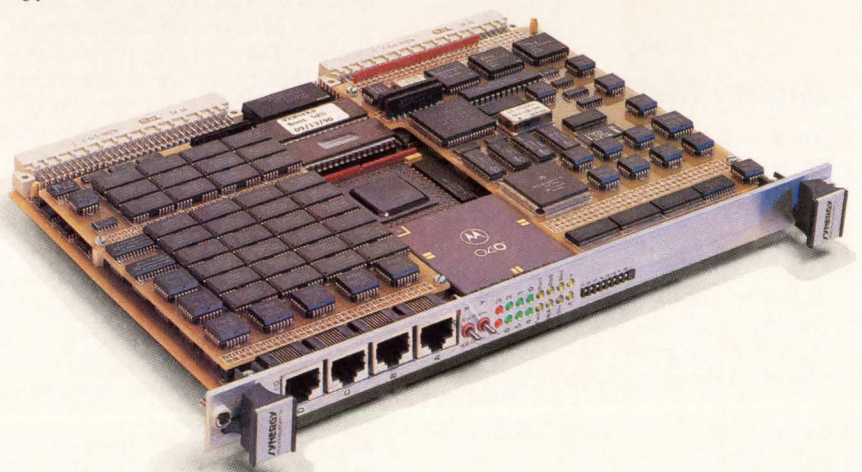
Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and

'030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



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CIRCLE NO. 5

IBM chooses Valid as EDA supplier

After a year and a half of evaluating design tools from leading EDA vendors, IBM (Armonk, NY) has awarded Valid Logic Systems (San Jose, CA) a three-year, multimillion-dollar contract to supply IBM's worldwide development labs with design tools. While neither company would comment on the exact dollar amount of the contract at press time, a Valid spokesman confirmed it exceeded a \$25 million deal Valid recently inked with SGS-Thomson Microelectronics (Phoenix, AZ).

The award is significant because it represents the first time IBM has made a corporate-wide commitment to a third-party EDA tool suite. IBM confirmed it will continue to develop in-house tools, as well as purchase point solutions from other vendors, but will use Valid's suite for design capture, simulation, PCB layout, and framework management.

The main competition for the contract came from Mentor Graphics (Wilsonville, OR) and Cadence Design Systems (San Jose, CA). Mentor lost out because its tools didn't run on IBM's RS/6000, while Cadence was passed by because it didn't have a fully integrated PCB design system.

—Mike Donlin

Mighty Mentor slips a bit

After two quarters of losses, Mentor Graphics (Wilsonville, OR) has announced the first layoff in its 10-year history—a move that affects about 400 employees, or 15 percent of Mentor's workforce. In addition to abandoning its efforts in CASE, mechanical CAD and documentation services, Mentor also trimmed its European sales force and sold its hardware service business to Hewlett Packard (Palo Alto, CA).

Though analysts blame Mentor's woes on the recession and failure to deliver its Falcon 8.0 software on schedule, a deeper cause may be Mentor's transition from a turnkey total EDA supplier

to a vendor with focused technology solutions. The days of being all things to all people are ending in the EDA marketplace, as suppliers like Mentor and Valid Logic Systems (San Jose, CA) shed the expensive yolk of proprietary hardware constraints and move on to roles as software suppliers.

—Mike Donlin

RISC, Take 1

Don't refer to Texas Instruments' (Dallas, TX) Sparc chip as "Viking" from now on. TI has officially named the device "Super-Sparc." With the christening came news that there's not just one chip, but two. A highly integrated 3.1-million-transistor BiCMOS Sparc CPU will be complemented by a second-level cache controller. The CPU, housed in a 293-pin PGA, will contain a superscalar integer unit (IU), floating-point unit, and the largest caches yet to be placed on a single chip—a 20-kbyte instruction cache and a 16-kbyte data cache. The superscalar IU features two ALUs and can perform 64-bit loads and stores. The processor will be capable of four instruction/cycle fetch and three instruction/cycle issue and execution. The optional 369-pin PGA cache controller sports fully integrated on-chip cache tags and supports 1 Mbyte of direct-mapped cache. "Tape out" of the devices has already occurred, according to John Hughes, TI's manager of open systems.

—Dave Wilson

RISC, Take 2

Coincidental with TI's RISC news come more details on the R4000 RISC processor from MIPS Computer Systems (Sunnyvale, CA). The R4000 will come in three versions—the PC, SC and MP each aimed at different price/performance points. An IU, MMU, FPU, primary cache with primary cache controller, as well as a secondary cache controller can all be found on the R4000. Standard RAM is used for secondary cache off-chip.

Although the processor die may be the same in all three versions, each version will be unique. The first version, the PC, is a small, low-cost 179-pin PGA package that has no support for secondary cache. Performance will be 40 Specmarks at 50 MHz. Packaged in a 447-pin package, the SC will be available as a PGA. With a small 1-Mbyte secondary cache, designers should realize 60 Specmarks, according to MIPS. The R4000 MP, housed in the same size package as the SC, will support a secondary cache in addition to multiprocessing.

—Dave Wilson

Companies form mixed-signal merger

In an effort to boost their analog and mixed-signal capability, Cirrus Logic (Milpitas, CA) has penned an agreement with Crystal Semiconductor (Austin, TX). Under the agreement, Crystal Semiconductor, a manufacturer of advanced analog circuits for audio, communications and data acquisition applications, will become a wholly-owned subsidiary of Cirrus Logic. The two companies plan to work on projects that integrate Crystal's analog technology into Cirrus Logic's digital controller devices. A data communications IC, jointly developed by both companies, is already in the works, and will be announced next month.

For Cirrus Logic, known mostly for integrating digital functions for mass-storage and graphics chips, the acquisition of Crystal lets it accelerate the addition of analog functions on its digital chips. Last year, Cirrus began developing its own limited in-house analog capability, which let it make a graphics controller chip with a RAMDAC on-chip. With Crystal's technology in its portfolio, Cirrus should be able to make a quantum leap in analog and mixed-signal integration, instead of moving in the step-by-step way it's done in the past.

—Jeffrey Child

Continued on page 10



THE MAN FROM IKOS:

*Does he know
something about
VHDL system
simulation you
should know?*

IKOS File: Case No.101

The Accelerated VHDL Solution

I got a tip that a major military contractor had to simulate a system defined in VHDL at the behavioral level. The problem was, they had to process a minute of real time data through the design to verify it. Using a SPARC 2 with enough memory for a herd of elephants, it still would have taken months. But these guys simulated that minute of real time data on the entire design in a few hours. How? Turns out they were a beta site for the new IKOS VHDL Accelerator. The brass was impressed.

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Continued from page 8

Process could lower fine-line PCB costs

Velie Circuit (Costa Mesa, CA) is claiming a breakthrough in manufacturing technology that could have an impact on the cost of fine-line printed circuit boards. Called Optipad, the technique provides a new way to regulate the size and uniformity of solder pads on PCBs.

Like a drop of water on a hard surface, solder pads vary in size and shape, making the application of solder very difficult. In contrast, Optipad creates solder pads that are flat and uniform in height, width and thickness, with no run-off into the line spaces between conductors. The process could greatly reduce assembly costs by reducing the need for rework after assembly and eliminating the need for solder paste. —Jeffrey Child

IC inventor protests patent violations

At a recent Tech-Trends, Texas Instrument's annual technology conference in Dallas TX, Jack Kilby, inventor of the IC, commented on the lawsuit filed by TI against Fujitsu. Filed three months ago in Tokyo, Japan, the lawsuit specifically alleges that Fujitsu's production of DRAM's infringes TI's patent.

Referring to the number of times his invention is repeated on a typical circuit, Kilby quipped, "We looked at the Fujitsu 1-Mbit DRAM and we estimate that it infringes the patent somewhere between 1 million and 1.5 million times." Would a jury use the same approach as memory vendors and base an award on cents/bit? —Jeffrey Child

IBM farms out graphics chip production

IBM (Armonk, NY) must be expecting extreme demand for systems using its XGA graphics technology. Billed as a follow-on to its very

successful and widely imitated VGA standard, IBM's latest effort tries to leapfrog the stalled 8514/A technology, the original successor, to VGA with 1024x768, 256-color graphics. Inmos/SGS Thompson (Bristol, UK) has announced it will be manufacturing the XGA chip under license from IBM. Apparently, production is only for IBM's internal consumption as Inmos/SGS is to produce a version of the chip for the Micro Channel architecture only.

Whatever the arrangements, the widely ballyhooed announcement may not signal more than an interesting business departure for IBM—having silicon of its own design manufactured by a third-party for internal consumption. Software standards such as X-Windows and Microsoft Windows have broken free of hardware standards for graphical user interfaces (GUIs). Silicon that can run these standards efficiently will find acceptance regardless of some internal register specification, so XGA as such can never hope to dominate designers' considerations the way VGA did. —Tom Williams

ASIC vendor eases FPGA-to-gate array migration

In a move to capture PLD and FPGA designers who want to migrate to gate arrays—but don't have the know-how to do so—gate array vendor S-MOS Systems (San Jose, CA) has announced that it will resell the ViewLogic Systems (Marlboro, MA) Retargeter FPGA-optimization software. S-MOS, thus, becomes the first gate array vendor to join ViewLogic's Silicon Design Alliance partnership program for the purpose of giving its users a path for migrating from PLD- and FPGA-based designs to gate arrays. ViewLogic's initial eight partners—Actel, AT&T, Gould AMI, Intel, National Semiconductor, Plessey, Plus Logic, and Xilinx—joined the Silicon Design Alliance to provide their customers with ViewLogic's schematic capture and simulation tools.

Through the library-generating

tool that's an integral part of both the Retargeter and ViewLogic's VHDL Designer, S-MOS users will now be able to create synthesis libraries when they wish to explore speed and area improvements. The library-generating tool extracts logic functions from simulation data to create the synthesis library elements.

S-MOS users will be able to do technology remapping, translate from one technology to another or implement a design in an FPGA as a prototyping step in the design process. —Barbara Tuck

Windows easing data exchange for control applications

Microsoft Windows is proving to be a big help for users wishing to design control applications requiring easy transfer of data between programs. Windows' dynamic data exchange (DDE) facility provides a ready-made communication protocol. Originally conceived for office applications, DDE is finding increasing acceptance in the industrial world. Radisys (Beaverton, OR) and Xycom (Saline, MI) are two suppliers of PC-compatible VME board-level computers that support DDE and Windows for implementing control applications.

Xycom has implemented a DDE server that contains knowledge of the company's own board products to ease set-up. Using DDE and Windows along with real-time control programs, users can set up system configurations and user interfaces without detailed programming knowledge. A Windows-based package from Wonderware (Irvine, CA) even lets users draw representations of a plant and link data to display status. Bob Patterson, marketing manager for Radisys, predicts that the usefulness of Windows for industrial control will grow even greater when Microsoft finishes work on its object linking environment (OLE) which will allow data exchange in an object-oriented environment where users can encapsulate certain ways of automatically processing the incoming data. —Tom Williams



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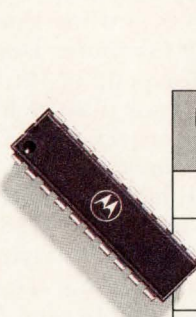
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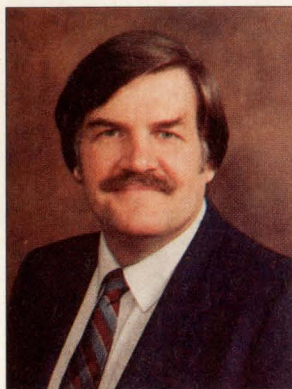
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Rather than fighting with each other, Intel and AMD should be looking to where the real threats lie to their prosperity.



John C. Miklosz
Associate Publisher/
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Necessary evils

Not only do I not like big business, big government, big sports and big entertainment—I don't like lawyers, big or little. Lawyers are to be avoided at all costs, something like dentists, undertakers or traffic cops. Like these, the best that can be said for lawyers is they're necessary evils. Even more so today because lawyers seem more interested in stirring things up than in settling things down. (Good thing we don't count lawyers among *Computer Design's* readers.) It may not be lawyers stirring things up at Intel and AMD, but the results are the same—two major players in the semiconductor industry are engaging in internecine warfare, which in the long run will do neither of them much good.

Intel and Microsoft have had a lock on the personal computer world since the PC revolution began. But both the 80X86 architecture and MS-DOS are running out of steam—Intel's trying to fend off inroads by RISC processors and Microsoft's doing the same with the Unix threat. While Microsoft is looking beyond MS-DOS to multimedia for its future prosperity, Intel wants to milk the 80X86 and keep the revenue stream flowing as long as possible. And why not? It was inevitable that as PCs proliferated, the stakes would get higher and clones would also proliferate. AMD was first with the AM386, Chips and Technologies is introducing its Super386 this month and another clone (actually a superscalar 386 emulator) from a startup called Meridian Semiconductor may soon be with us.

The merits of AMD's claims against Intel—its right to use Intel microcode, whether or not Intel broke its agreement with AMD to transfer 386 technology, AMD's right to use the "386" moniker on its clone, and whether or not Intel has engaged in monopolistic and anticompetitive trade practices—could, and will be, debated ad nauseam. Some of these claims have already been settled in AMD's favor, and maybe that's gotten every lawyer's blood up. This business about monopolistic practices and anticompetitiveness are another matter and a bit foolish, if not folly.

AMD and Intel should be settling their differences facing each other, not facing a judge, squabbling over monopolistic practices. Why Intel never struck a deal with AMD (or stuck to the one that AMD says it did strike) to second source all of the 80X87 family is incomprehensible. Of course, such a deal could easily be viewed as anticompetitive and maybe Intel and AMD would have found themselves fighting other challengers. But anticompetitive practices are nothing new to the electronics business and the Japanese achieved their dominance of the consumer electronics business in just that way. Rather than fighting with each other, Intel and AMD should be looking to where the real threats lie to their prosperity.

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Circle 366

October 21 - 25

COMDEX/Fall '91

Las Vegas, NV. The 13th international fall trade show for computer distribution professionals has been expanded into three programs: the main conference program, the network computing conference and the multimedia conference. The main conference will feature discussions about the industry in transition, marketing, new technology, pen-based computing, resellers and vendors coping with changes in distribution channels, applications software, multimedia applications and systems and portable computing. The network computing conference features more than 25 detailed technical sessions about the fundamentals, applications, design, and the managing and planning of network computing. Also, this series will coincide with a network computing exhibition. The multimedia conference features sessions about the evolution of multimedia, its applications, software and hardware. Information: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, fax (617) 444-0165.



Circle 367

October 26 - 30

International Test Conference 1991

Opryland Hotel, Nashville, TN. The 22nd International Test Conference offers technical programs and exhibits of test-related hardware and software. A three-day technical program reflects the theme: "Test: Faster, Better, Sooner." This program consists of a plenary session, 40 formal paper sessions, a poster session and panel sessions. Papers and posters will cover numerous aspects of test from chip through system level and present innovative ways to solve today's design and test problems. The test week is rounded out by two days of tutorials that explain or expand on test topics presented in the technical sessions. Information: International Test Conference, 514 Pleasant Valley Blvd, Suite 3, Altoona, PA 16602, (814) 941-4666, fax (814) 941-4668.



Circle 368

October 30 - November 1

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Santa Clara Marriott, Santa Clara, CA. The Analog & Mixed-Signal Conference is dedicated to the unique needs of mixed-signal design. Over 50 lectures and workshops will focus on subjects including transmission line effects in high-speed design; mixed ana-



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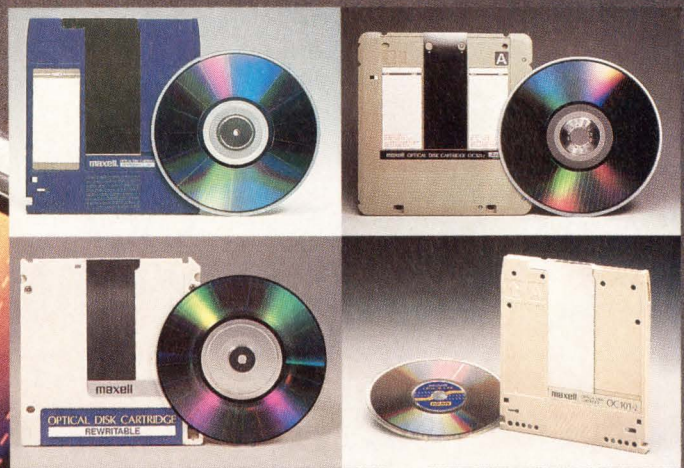
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log/digital design; modeling, simulation and test; and much more. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2630, fax (415) 905-2630. **Circle 369**

November 5 - 8

SMTCON West

San Diego Convention Center, San Diego, CA. The Surface Mount Technology Conference and Exposition is Southern California's only dedicated SMT event. The conference will feature workshops, technical sessions and courses on SMT, inspection and test, design and assembly, electronic packaging, quality control, tape automated bonding, applied electronics cooling, SMT manufacturing operations enhancement, and more. Information: IC Management, 900 N Franklin St, Suite 700, Chicago, IL 60610, (312) 944-3434, fax (312) 944-5289. **Circle 370**



November 19 - 21

WESCON

Moscone Convention Center, San Francisco, CA. More than 45,000 are expected to attend the 40th annual WESCON conference and exhibition. Exhibits, technical sessions, short courses, and several special events will be featured during the three-day confer-



ence. There will be sessions on design, test and production engineering focusing on semi-conductors, EDA tools and board-level components; test and measurement sessions; and manufacturing sessions on materials and supplies. There will be a special conference on exploring business opportunities in Eastern Europe. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, fax (213) 641-5117. **Circle 371**

November 19 - 21

AFCEA Hawaii

Sheraton Waikiki Hotel, Honolulu, Hawaii. The sixth annual AFCEA Pacific international defense electronics conference and exhibition provides an opportunity for discussions between the military and the industry leaders from the United States and the Pacific region. Information: Beth Blose, Spargo & Associates, 4400 Fair Lakes Court, Fairfax, VA 22033, (703) 361-6200 or (800) 336-4583, fax (703) 818-9177. **Circle 372**



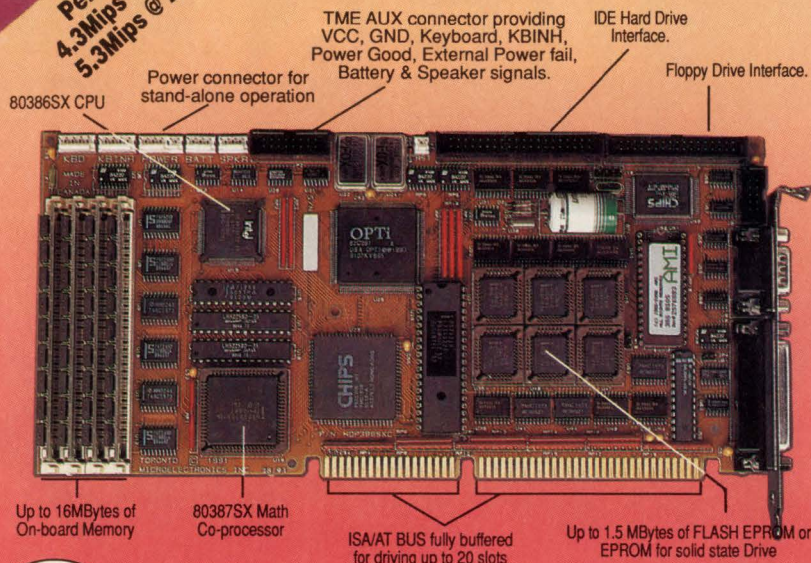
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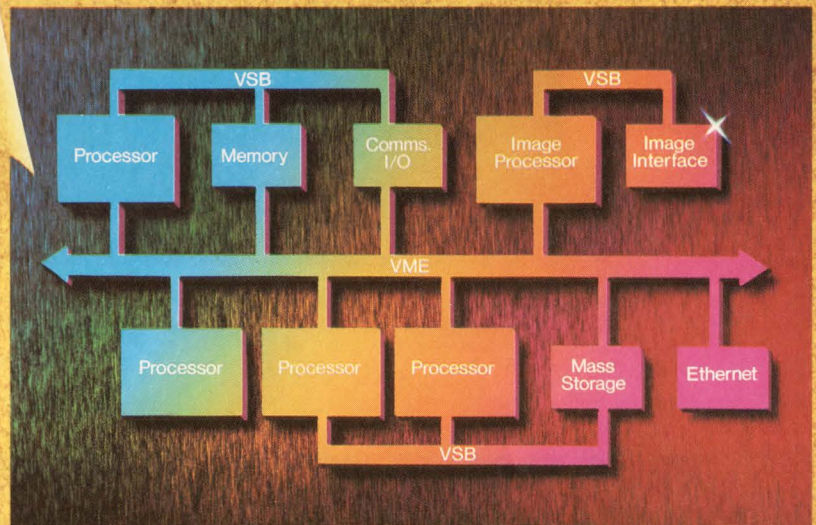


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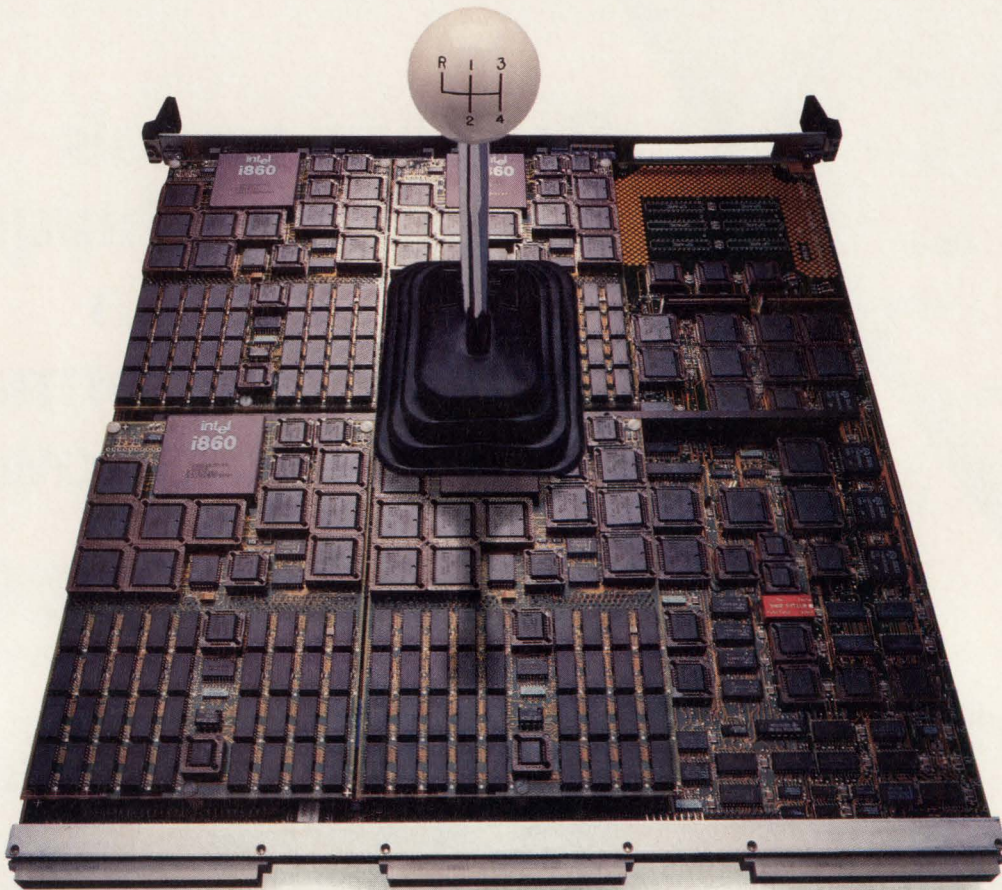
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Christoph Eck on: Real-time standards

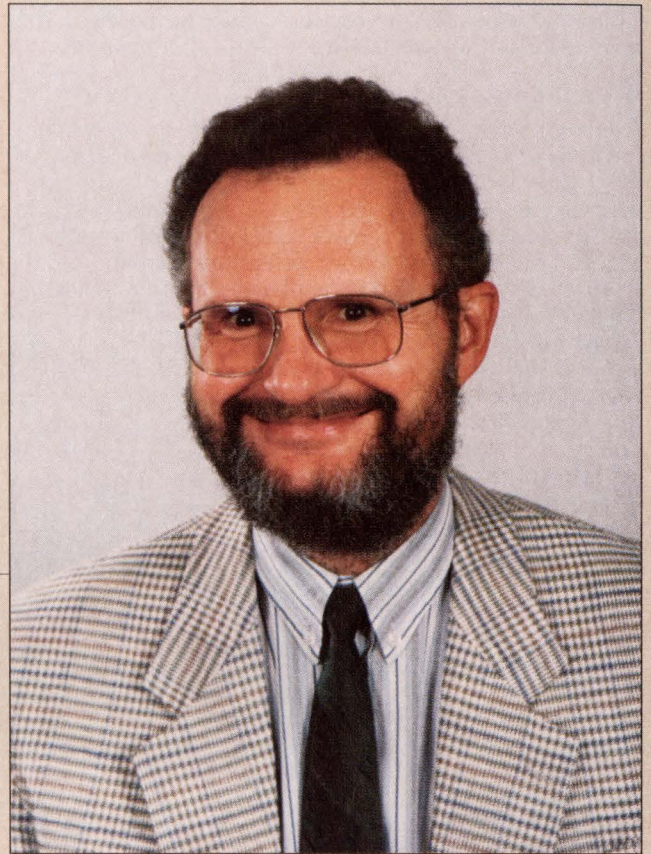
By now, it's obvious to most users that there's a need for standards for all computer-related products. Most manufacturers acknowledge the importance of standards by participating in standardization projects. After reviewing the history of standards in the computer industry, however, one learns quickly that manufacturers often paid only lip service to the idea of standardization. They were happy to support "de facto" standards, either as the original manufacturer of a leading product or as a follower of a profitable market. Their reluctant bow to user demands is understandable. Why should a manufacturer support a move which could only lead the user community to become more independent.

The first "real" standards were developed in areas where standardization was practically unavoidable. These areas include systems, from different manufacturers, that had to exchange data or had to be networked together. The first manufacturers who understood standardization as a tool to improve their time-to-market figures were those who were building modular computers based on standard buses. Hardware, however, is only part (and the easier part) of a computer system. For a long time the "black art" of software was covered in a very limited way by the standardization process. There have been standard high-level languages, but in the operating system area we were still dealing with de facto standards at best. Microsoft's DOS can claim this status and so can Unix. Still, DOS serves only one architecture and Unix comes in too many, partially incompatible flavors.

■ The Unix standard

By now, one can find Unix everywhere. It runs on all sizes of systems from micros to supercomputers. Most computer manufacturers support Unix, either as their sole offering or in parallel to their proprietary operating system (notably Digital Equipment Corp and IBM). Proprietary systems seem to have a slim chance of survival because of Unix's growing success.

For these reasons, it's not surprising to see the amount of effort invested in the creation of a Unix standard. Even if part of this effort is masked by fights for market share, exemplified by the formation of



groups like Unix International, the Open Software Foundation and the Advanced Computing Environment (ACE), many basic standard documents in this area are finding general acceptance: SVID (System V Interface Definition), the X/Open guide and, most importantly, the Posix standards written by IEEE.

■ Posix

Posix is the most widely accepted group of standards in the traditional Unix environment. IEEE working groups are developing a group of standards as components of Posix. IEEE focuses on developing U.S. standards, but Posix has achieved international status via its acceptance by the International Standards Organization (ISO) and the International Electrotechnical Commission (IEC) as International Standard 9945.

Posix is a software interface standard that guarantees portability of application source code and should not be confused with an operating system implementation standard. This distinction is made because widely different operating systems, such as VMS and OS/2, will become Posix compliant.

Currently, work on the Posix standard is split into roughly 20 projects labelled IEEE P1003.n. Until now, only one of these projects has its document agreed upon as an official standard: the System Application Program Interface, IEEE Std 1003.1-1990, ISO/IEC 9945-1:1990(E).

The Posix 1003.4 Working Group has been preparing the document "Real-time Extension for Portable Operating Systems" for several years. Real-time Posix addresses the full extent of real-time systems, from

full-scale Unix down to small embedded kernels with the greatest emphasis on critical real-time performance.

Real-time system standards

Defining "real-time" as it relates to an operating system is a necessary prelude to any discussion of real-time system standardization. Most people associate execution speed with real-time behavior. While speed is important for most real-time applications, it doesn't define the essential difference between a real-time system and a fast time-sharing system. Quoting the definition from a Posix document, real-time is "the ability of the operating system to provide a required level of service in a bounded response time." This implies a guarantee for worst-case response. Basic Unix isn't designed to be a real-time system. Its goal is to give a fair share of system resources to every user, and not let, for example, a high priority process take the CPU and keep it as long as necessary.

Standard (timesharing) Unix was not much use for real-time applications. At one time there was no hope for a de facto standard in the real-time system or kernel area. There are many (perhaps too many) kernels and systems on the market, most with nearly identical functions but none that are compatible with each other. And none of those systems have a sufficient share of the real-time market to be a candidate for a de facto standard.

Therefore, the VFEA, (VME-to-Futurebus Extended Architecture) International Trade Association started the Orkid (Open Real-time Kernel Definition) project with the hope to create a standard kernel definition via a consistent amalgamation of existing products. Although the resulting document is a solid piece of technical work, the project was killed by political battles among members of the project committee. These battles provided one more lesson on the difficulty of convincing manufacturers of the intrinsic value of software standardization.

Fortunately, all was not lost. The Posix work had gained so much general support that its real-time extension project was still viable. It became clear that IEEE P1003.4 was the last and only chance for arriving at a standard real-time system. The Orkid group joined the P1003.4 project at the end of 1990.

The aims of the Posix.4 group are best defined as the P1003.4 draft states: "To make Posix.1 minimally usable for real-time applications on single processor systems. The scope is to take existing real-time operating system practice and add it to the base standard."

This statement needs some interpretation. Multi-processor support is under discussion in the working group because it's now clear that an exclusive mono-processor standard would not cover a fast-growing class of systems. The addition of real-time capabilities to Posix doesn't mean that every compliant real-time system will have to carry a full Posix-compliant operating system. Posix.4 compliance will cover a wide range of systems from small embedded kernels in ROM to large full-function Posix systems, the smaller systems being completely compatible subsets of the larger systems.

Profile of an IEEE working group

The Posix.4 group is made of mostly professionals from computer companies and software houses. The others, a surprisingly strong subgroup, are either users of real-time software or come from universities or other organizations doing research related to real-time systems. Although there are about 129 participants, only 40 to 50 people go to the meetings. Officially, members of IEEE working groups participate as private individuals and cannot represent a company. In reality, participants from industry have the interests of their companies in mind, although most discussions in the group are based solely on technical arguments. Working group etiquette forbids the use of "we" in all discussions, a prohibition that probably has something to do with the success of working groups.

The Posix.4 group meets four times a year. These meetings are scheduled together with the meetings of all other Posix projects, bringing together about 400 people. Until now, all meetings were held in a large U.S. hotel, moving as fairly as possible across the country.

Meetings continue from 8 a.m. to 6 p.m. for a week and much work is accomplished on the standards. Apparently, only a few participants have the time to work on the standard for more than a few days between meetings.

POSIX D1003.4

The Posix.4 group has created drafts of four documents: P1003.4, P1003.4a, P1003.4b, and P1003.13. The base document is P1003.4, "Real-time Extension for Portable Operating Systems." At the time of this writing, the most recent version was draft 10, dated February 6, 1991. P1003.4 contains the specification of interfaces to handle the following functions: binary semaphores; memory locking (permits whole real-time processes or parts of them to be declared unswappable to guarantee worst-case response times); shared memory and memory-mapped files; and fully preemptive, priority-

based scheduling that's supported by two main scheduling policies, FIFO and round-robin. FIFO scheduling establishes process lists on each priority level. The lists are ordered by the time that level's processes have been awaiting execution. Round-robin scheduling establishes separate time-slices for processes on each priority level.

P1003.4 also includes real-time signals, clocks and timers, interprocess communications (IPC), asynchronous and synchronous I/O, and real-time files. Real-time signals are a minimal extension to the Posix.1 signals that avoid the possible loss of asynchronous event notification, enable their prioritized handling of asynchronous events and differentiate between multiple occurrences of events of the same type. High-resolution clocks (with periods down to nanoseconds) and absolute, relative and periodic timers are supported. IPC is supported via message queues for passing arbitrary amounts of data between processes in a deterministic way. Asynchronous I/O provides the ability for the system to initiate an I/O operation and then perform other operations without having to wait for the I/O process to finish. Synchronous I/O guarantees that data is recorded on the output medium when the I/O operation finishes. Real-time files support fast I/O onto contiguous files or equivalent structures.

Each chapter of P1003.4 ends with a "Performance Metrics" section. This section specifies how to measure the execution time of the different operations in a given implementation. Manufacturers claiming compliance of their system with P1003.4 have to document these times in the user manual for the system.

Draft 9 of P1003.4 was the first draft to undergo the IEEE balloting process. Each IEEE standard has a balloting body, a representative group of IEEE members who vote to either accept or defeat a standard. For acceptance, more than 75 percent of this body has to vote and more than 75 percent of the voters have to accept the standard as it is.

Draft 9 was balloted at the end of last year and failed with around 3,000 objections (many directed at the same points). The latest document, draft 10, was balloted last spring and failed with 1,500 objections. These figures document the level of scrutiny the Posix standards are submitted to and indicate the standard's progress toward acceptability.

■ Other Posix documents

The Posix.4 group also prepared the P1003.4a, "Threads Extension for Portable Operating Systems." The most recent version is draft 5, dated December 7, 1990. Posix processes have a heavy context- and process-switching overhead. One process, however, can have multiple threads in a common-memory map, which reduces context-switching overhead. Conceptually, such a thread is similar to a typical real-time kernel task.

P1003.4a introduces mutexes and condition variables as further synchronization primitives. They are based on shared memory and allow very fast implementations. Mutexes also support priority inheritance, a feature specifically designed to avoid the common problem of priority inversion among priority-based schedulers. Priority inversion occurs when, for example, low-priority thread A has a resource and high-priority thread C needs it, but medium-priority thread B preempts and prevents A from releasing the resource. In this situation C can wait an unbounded time for lower-priority threads to complete their tasks.

The mutex uses the concept of ownership to assign priorities. The priority of the owner of the mutex can be temporarily raised to the highest priority of a thread connected to the mutex. In this way, priority inheritance allows a speedy release of the requested resource.

P1003.4a failed its first ballot this spring. Another document under preparation by the Posix.4 group is P1003.4b. This standard will contain additional extensions. Work has started on specifying timeouts for blocking operations, fast interrupt handling by user code, and the support for memory allocation from regions representing the different physical areas of memory available in real-time systems (fast or slow memory, ROM, battery-backed memory, memory shared between processors, etc.). More topics, most importantly multiprocessing, will also be addressed.

Yet another document prepared by Posix.4 is P1003.13, "Real-time Profiles." Draft 2 was scheduled for July 1991. A profile document describes a set of options from Posix and related standards. This handles the problem of compatibility between different implementations based on standards with a large number of options. According to this document, con-

formance of a product can only be claimed by referencing a specific profile(s).

P1003.13 profiles, each is a subset of a higher profile, will cover the full range of system sizes from small embedded kernels in ROM to full-fledged systems.

■ Where are the problems?

Obviously, the creation of a standard by consensus among a large group of individuals with different backgrounds isn't an easy matter. The main risk is everybody's pet idea gets included in a draft, making it too complex and cumbersome for the advocates of "hard" real-time systems. Opposition to this approach manifests itself clearly in the ballot results. It's interesting to note that during the pruning process demanded by the ballot, the Orkid document is increasingly viewed as a concise description of "industrial practice," defining the minimal level of required functionality.

Another difficulty stems from the real-time extensions covered in several documents that are in different stages of completion. Although this approach is justified by the Posix.4 group's wish to vote on parts of the standard that are approaching their final form, it also carries the risk of losing consistency between P1003.4, .4a and .4b.

Finally, at the request of ISO/IEC, two tasks must be completed to obtain formal approval. The first is developing a language-independent form of the standard (which is now written in the form of C-language function specifications). The second is the need to add test assertions for conformance testing. Neither of these will change the basic content of the standard.

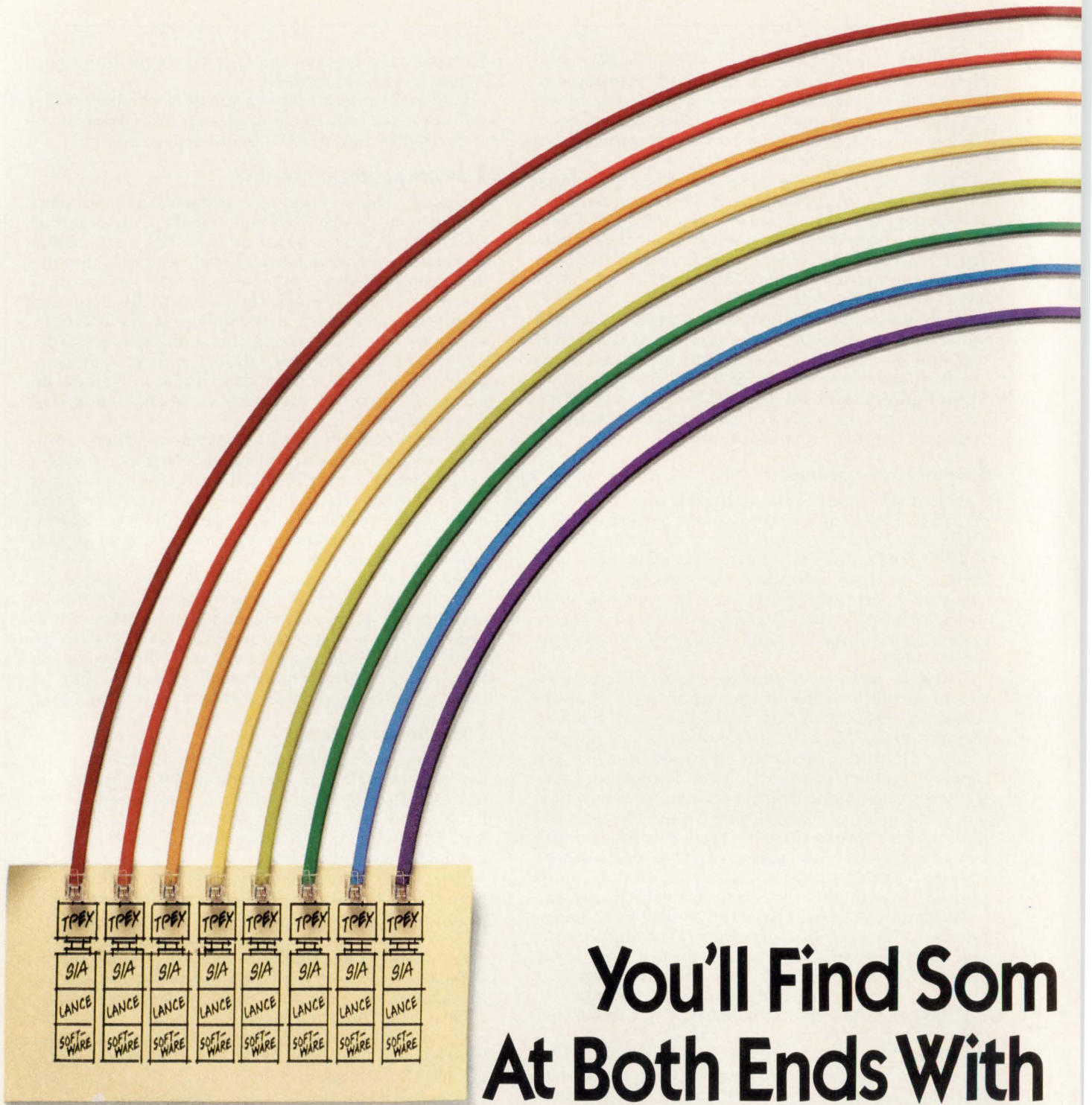
■ The future of Posix

The real-time extensions to Posix are not only a necessary step toward real-time system standardization but also the most promising. It's expected that P1003.4 will be accepted as an official standard in May 1992 while the other parts of the process will be finished sometime in 1993.

It looks as if most companies will make their products Posix compliant. Some companies are already claiming conformance for their systems. Officially, this is possible for Posix.1. For the real-time extensions, conformance claims are more of a problem. The standard is not yet frozen and the profiles defining the different sets of options are in a very early state.

Given the progress to date, and the reasonable expectation of a complete, stable standard in the near future, one thing is certain: Every professional working with real-time operating systems and real-time programs should begin to learn about Posix.

Christoph Eck is manager of the data handling division at CERN (Geneva, Switzerland).



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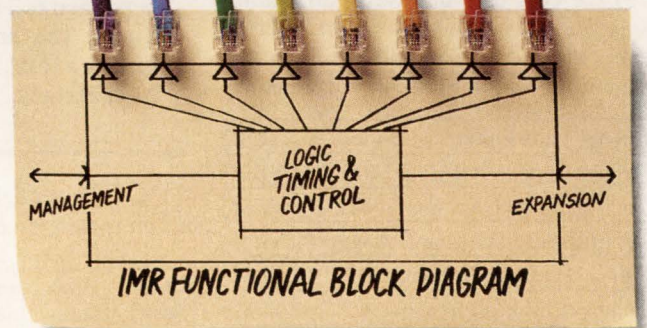
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CIRCLE NO. 21

Building a better PC processor



For Morris Jones, vice-president of technology at Chips and Technologies (San Jose, CA), it might seem a far cry from his last job, helping to create Amdahl machines. But last month's announcement of performance-enhanced, 80386-compatible processors and coprocessors, one highly integrated PC on a chip, and most importantly, a new system-management architecture, will certainly have more impact on the computer industry than any mainframe Jones may have built in the past.

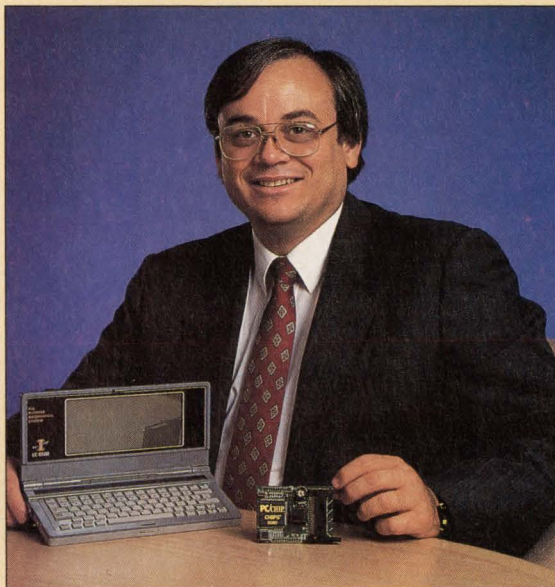
Morris Jones thinks that it's practically impossible to differentiate a personal computer design today. And it's obvious that he feels the blame lies with one company's inflexible PC processors that force a rigid design dogma onto engineers. So it's hardly surprising that instead of simply constructing a better mousetrap than his competitors, Jones wants to give the designer more creative ways to use the mousetrap itself. "The idea behind our new products is to put PC design back into the hands of the designer by providing a new PC-design ideology," he says.

The revolutionary new methodology Jones espouses is Superstate. Operating transparently to an application program, Superstate is a software/hardware environment that a designer uses to tailor a PC just the way he or she sees fit. To help designers take advantage of the idea, Jones has built hardware hooks for some of the Superstate features in Chips and Technologies' new processor offerings (see "386 processor clones run faster than the 'real thing'," p 35). Future Superstate features, to be included in future generations of processors, will even give designers the ability to design their own microcode.

Out of all Chips' new devices, the processor that highlights the Superstate concept best is PC/Chip. It's a highly integrated 80C86-compatible processor with all systems logic, graphics and communications functions on-chip. Clearly, with such functionality integrated onto a single piece of silicon, Chips and Technologies was obliged to provide a way to let designers differentiate product offerings

based on it. Otherwise, all the products based on the chip would look the same. Superstate was the way.

In a typical PC environment, the application program, operating system and BIOS interface directly with the system logic and CPU. With Superstate in the system, application and operating system software interact with the Superstate environment instead. Superstate talks to the hardware, but it's the designer that controls the behavior of the Superstate environment, using it to transparently monitor and control the activity of the system without affecting compatibility with it.



Morris Jones wants to offer the designer a way to differentiate personal computer designs. To help out, Jones has developed a new hardware/software concept called Superstate that will work in conjunction with his newly released forward-engineered 386 microprocessors.

When such a concept is coupled with hardware features of the PC/Chip, such as a 26-bit address space that lets the chip support a full 64-Mbyte memory map, the advantages become obvious. In most of today's laptops or notebooks, for example, power management software runs on a keyboard controller such as an 8051. This prohibits specific power-management routines from interfering with the system BIOS or operating system software running on the main CPU. But using the system

capability of Superstate, designers can not only use the main CPU to monitor the overall activity of the peripherals in the system for power-management purposes, but they can also control them by invoking software-management routines that reside in the address space of the Chips processor that's inaccessible to the application or OS software. Such a technique not only removes the necessity of a separate system processor, but ensures that power-management software routines will not conflict with BIOS or operating system calls.

But it's not just power management where Jones sees the benefits of the Superstate approach. Jones also emphasizes that Superstate gives designers the luxury of using any hardware or software in a PC system, since the goal of PC compatibility can be obtained through the use of the Superstate architecture. Devices such as memory cards, incompatible with existing PC software, can be emulated through the Superstate system. And it also gives designers the ability to run two incompatible operating systems such as DOS and Penpoint simultaneously.

In the design of his new processor hardware and the software concepts behind it, Jones and his engineering team have broken the rules of the chip set game. He has entered the territory once held exclusively by the processor vendor, and he has helped to destroy the myth that the heart of the PC must belong to one processor vendor alone. Clearly, Jones' products may not offer the Mips of the Amdahl machine, but both politically and technically, they offer a break from the traditions of the past.

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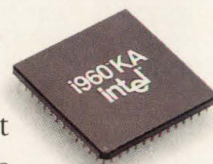
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CIRCLE NO. 23

386 processor clones run faster than the "real thing"

Dave Wilson, Senior Editor

Not content with just cloning an Intel 386 processor, Chips and Technologies (San Jose, CA) has deluged the designer with a slew of Intel 386 software-compatible processors and coprocessors, together with a highly integrated chip aimed at designers of low-power pocketbook computers. Rounding out these hardware offerings is a new hardware and software concept, called Superstate, which offers perestroika to designers shackled by hard-line restrictions imposed by Intel CPUs. By Comdex in October, many designs based on the Chips processors will be unveiled.

The Super 386 Chipsystem architecture consists of four processors divided into two families. First, there's the Intel pin-compatible 38600 DX and SX series which will buy the designer a 10 percent improvement in performance over the Intel line. Then, for higher performance, Chips and Technologies offers the extended-pin 38605 DX and SX series—Chips claims that these offer as much as a 40 percent improvement over Intel designs. The Super386 38600DX and 38605DX are available at speeds of 25, 33 and 40 MHz, while the 38600SX and 38605SX run somewhat slower at 16, 20 and 25 MHz. Intel offers neither 40-MHz versions of the 386DX or 25-MHz versions of the 386SX. "The 38605DX performs substantially better than an Intel 20-MHz 486," says Morris Jones, Chips and Technologies' vice-president of technology, who points to benchmarks the company has run. Prices for the new processors run the gamut from about \$200 for the 40-MHz 38605DX, to \$70 for the 20-MHz 38600SX.

The new processor introductions are not the first non-Intel 386s to hit the market. That honor goes to AMD (Sunnyvale, CA), who introduced the first members of its 132-lead PGA Am386 family of processors in March of this year. Those devices, the Am386DX and DXL processors, as well as the SX and SXL processors, are pin-for-pin, plug-in replacements for Intel's 386 designs. Last

month, AMD announced that the DX and DXL parts will be offered in plastic quad flatpacks (PQFPs). 33-MHz versions of the Am386 will cost about \$180.

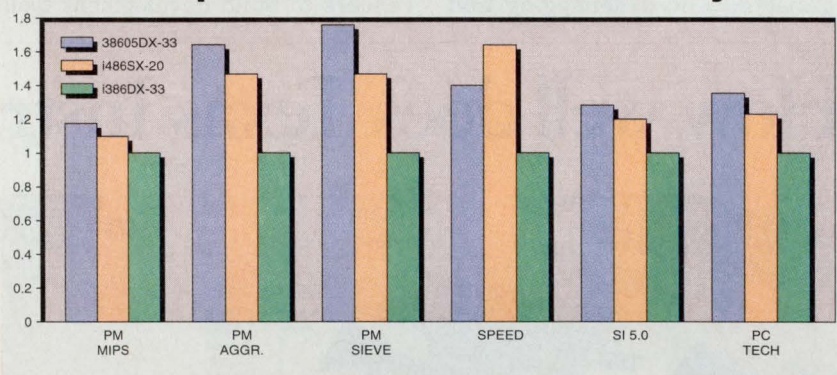
Improved, not just faster

Notably, Chips and Technologies' processors have actually improved upon the Intel architecture while offering Intel compatibility at the software level. The Super386 38600SX and DX microprocessors are not just faster but boast several architectural enhancements over

performance. What's more, the 605 processors have two additional address lines, expanding the addressing capabilities of the Chips parts by 4 Gbytes over their Intel counterparts. What's the benefit? "It gives designers the ability to run a complete LAN manager in its own protected address space, where it can't crash the system," says Chips' Jones.

While the 38600 series are pin-compatible with their Intel counterparts, the 38605 series isn't, because of its added features. The company refers to these as extended-pin parts. The 38605SX comes packaged in a 132-pin PQFP, compared with the 100-pin configuration found in the 38600SX. Similarly, the 38605DX is packaged in a 144-pin ceramic pin grid array (PGA), compared with the 132-pin ceramic PGA

38605DX performance cache-based system



Chips' 38605DX isn't pin-compatible with Intel's 386 because it sports extra features. Its designers added pipelining an on-chip cache as well as a greater addressing range. These benchmarks show the performance of the chip versus its Intel counterparts.

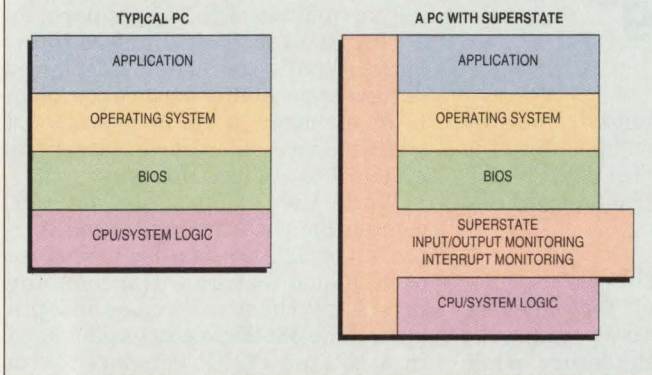
the Intel parts. In addition to a five-stage pipeline, Chips' designers made their processors fully static, just as AMD did—an advantage for designers of low-power portable equipment. More important, Chips' processors can also help designers lower system cost. Not only do the processors sport on-chip test logic, they also offer the ability to run from either a 1× or 2× system clock, unlike the Intel parts that force the designer to use a 2× clock. The 38605 SX and DX devices retain the features of the 38600 series, but add an integrated 512-byte instruction cache that helps the processors keep their pipelines loaded and contributes heavily to the increase in

found in 38600DX designs. For an easy system upgrade path, Chips' design notes show how a single-board design accommodates both the pin-compatible 38600 processor, as well as the extended-pin 38605 series parts, with the addition of a 176-pin socket that can accommodate 132- and 144-pin processors. All, according to Chips, for less than a \$2 increase in cost.

To help designers with development support, Microtek International (Hillsboro, OR) announced Mice-Super/386, an in-circuit emulator. Developed as a joint effort with Chips and Technologies, the emulator consists of a chassis and an in-circuit probe, which can con-

INTEGRATED CIRCUITS

Superstate monitors system activity



Superstate is a software and hardware concept designed to free the designer from the restrictions imposed by Intel CPUs and designs based around them. It monitors system activity and can emulate operating environments without affecting compatibility.

for the Chips processors.

The Chips PC/Chip is important to low-power laptop designers. As its name implies, it's a complete personal computer on a chip. Chips has integrated an 8086-compatible microprocessor running at up to 14 MHz, IBM XT-equivalent logic, a CGA-compatible flat panel/CRT controller, a serial port and hooks for power management in a single 160-pin package. The PC/Chip's DOS engine is fully integrated with XT-compatible logic, including the keyboard interface, a system clock and support for all industry-standard 8-bit peripherals. All this is priced about \$35 in volume quantities.

Chips' representatives say that the device was designed with power management as a priority. As such, it's fully static and offers the capabilities of being operated between 3 to 5 V. Operating at 8 MHz, it consumes less than 50 mA. PC/Chip's

nect directly to a processor socket that accommodates both 600 series processors and the extended-pin socket found on 605 processors. The product itself uses Chips' "bond-out" processor, a special version of the Super386 family processor designed to assist advanced debugging and

emulation by supplying information on the internal state of the processor on external pins. The bond-out is available exclusively to Microtek, says Rick Leatherman, Microtek's vice-president of marketing. That's not going to make it easy for other vendors to build development tools

How well does Texas Instruments support



processor and clock rate can all be slowed to save power. In addition, many of the on-chip processor subsystems, such as the serial port or graphics unit, can be disabled when not in use, so that power can be saved when that function isn't needed in a design, or isn't in use.

Rounding out the hardware offering is SuperMath, Chips' entry into the world of the numerics coprocessor. The family consists of two units, SuperMath DX and SuperMath SX, 387DX- and 387SX-compatible numerics coprocessors. Sporting an industry-standard pin out, Chips claims that, like its forward engineered 386s, the new processors are 100 percent compatible and, of course, faster, than the Intel solution. The price of those devices will range from \$300 for the 40-MHz DX to \$159 for the 20-MHz SX version.

As if this weren't enough, Chips has introduced Superstate, which gives PC designers more flexibility.

It can be used in conjunction with the additional hardware features provided by the extended-pin 386-like processors as well as the PC/Plus designs. Essentially, Superstate monitors system activity and can emulate operating environments without affecting system compatibility. I/O operations can be monitored, redirected, emulated or suppressed as the PC designer sees fit. Superstate can even be used to emulate a device that isn't present. Application programs can't distinguish Superstate operations from true I/O operations. The approach, therefore, avoids any conflict with DOS, while letting designers implement a number of sophisticated system features that include power management software, support for dual operating systems, as well as integrating "foreign" peripherals into PC-based systems.

All that remains now is to watch Intel's reaction to the forces at work

seeking to liberate designers from its processor monopoly. Considering past history, protracted legal wrangling is likely to be used in concert with 486 price restructuring. This is unlikely to stop designers from using the new devices. Board vendor Mylex (Fremont, CA), for example, is just one of many board vendors known to be readying a design for Comdex. ■

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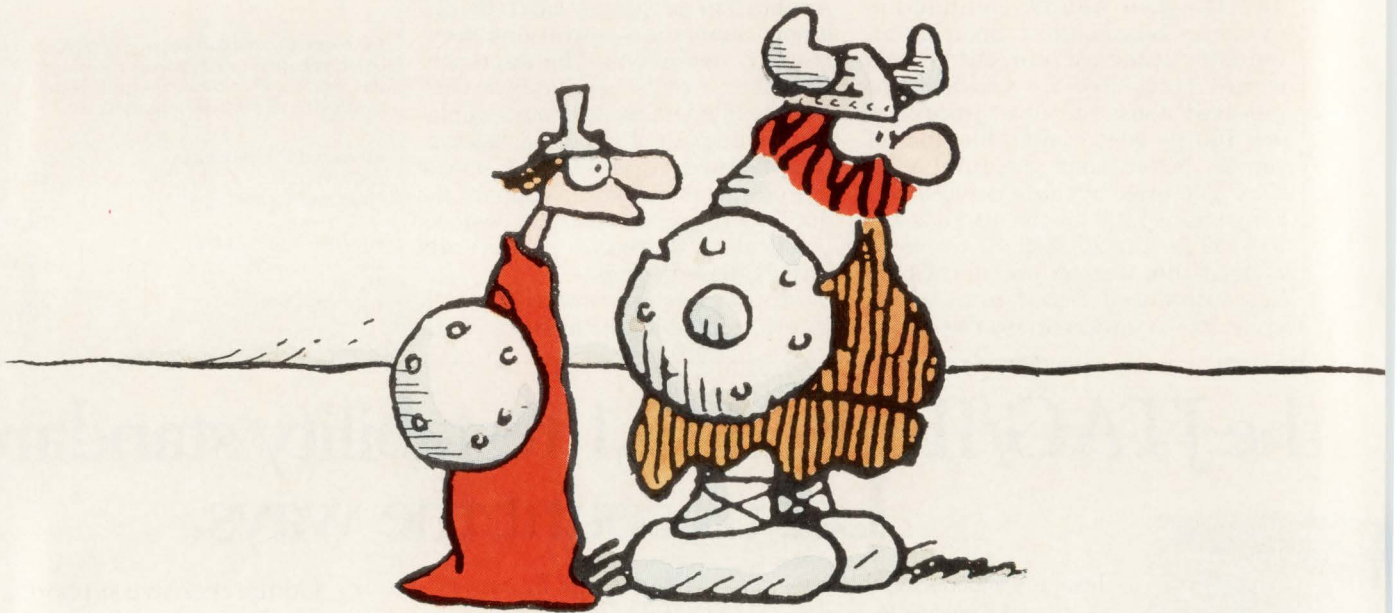
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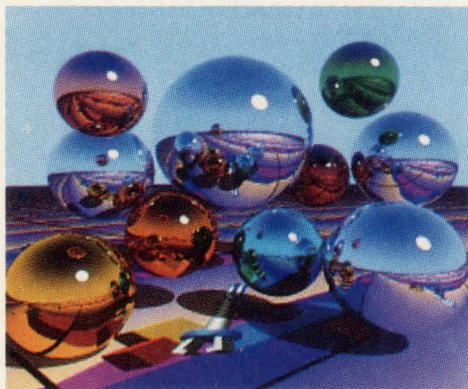
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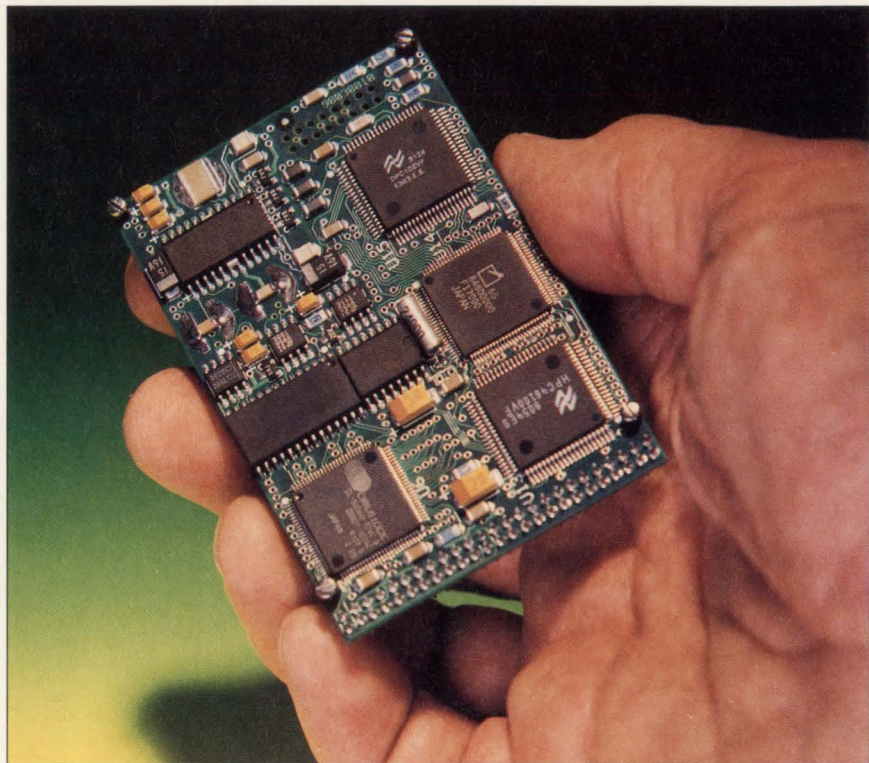
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For the Power Seeker.

DSP functions keep moving onto microcontrollers

Dave Wilson, Senior Editor



The controller of the Integral drive incorporates National Semiconductor's HPC46100 microcontroller as well as that company's read channel part announced earlier this year.

Whether or not it's an 8- or 16-bit microcontroller that designers of 1.8-in. embedded disk drives really need, chances are they do require some limited form of digital signal processing capability, especially if some servo functions need to be controlled. Indeed, DSP functionality may also be useful in automotive or industrial control applications as well. At least that's the conclusion of designers at both Zilog (Campbell, CA) and National Semiconductor (Santa Clara, CA). Over the past months, both have unveiled microcontrollers with some on-chip DSP functions. In August, Zilog disclosed its 8-bit Z8 microprocessor derivative, the Z86C94. In September, National followed suit with its HPC46100 16-bit microcontroller.

Neither vendor was first to recog-

nize the value of DSP functions on a microcontroller. Both products debuted almost one year after microcontroller mavens Motorola (Austin, TX) and Intel (Santa Clara, CA) disclosed their microcontrollers, the 68HC16Z1, and the 8XC196MC, respectively, which also included limited DSP functions on-chip.

Design considerations

When designing a chip specifically for a disk drive controller, a number of features must be included. The first is a fast-multiply accumulator that lets designers implement low-pass Butterworth filters. The second is a high-speed analog-to-digital converter which has been tuned to provide sampling rates that can meet the demands of the digital servo. Independent pulse-width modulators (PWMs) must be

incorporated to control a variety of servo motors. Finally, some form of digital-to-analog converter may be necessary as well.

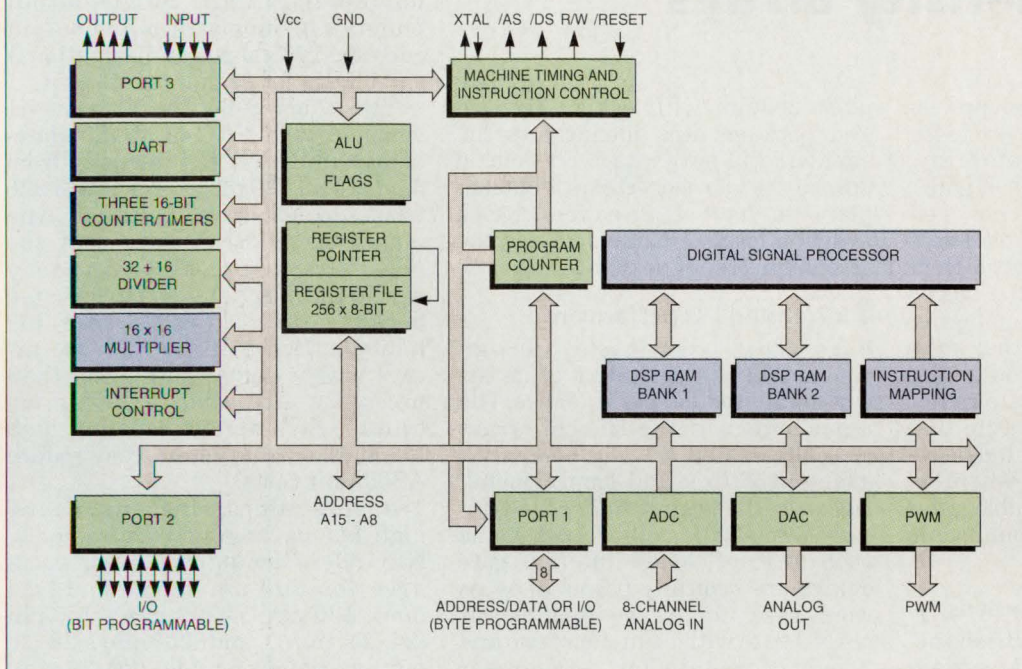
Of course, just how fast a processor can perform a multiply/accumulate (MAC) function is dependent on a number of factors. They include the architecture of the DSP subsystem as well as the clock speed of the chip. And just how fast the DSP needs to run depends on the way the designer partitions hardware and software in the controller subsystem. Zilog's CMOS Z86C94 is unique in that it sports both a microcontroller and a programmable DSP, in addition to a hardwired 16- \times 16-bit multiplier and 32-/16-bit divider. "We designed the 16-bit DSP such that it can operate in the servo environment while retaining an 8-bit microcontroller to control the rest of the disk subsystem," says Paul Vroomen, director of Zilog's consumer product line.

The on-chip DSP operates as a slave processor to the Z8. When executed from program RAM, Zilog claims the DSP can perform a 16- \times 16-bit signed integer multiplication and accumulation in one clock cycle, or in less than 100 ns with a 24-MHz external oscillator. National's part, the HPC46100, on the other hand, takes 8 cycles, or 400 ns at 40 MHz, to output a 32-bit result from a 16-bit signed integer multiply and accumulate instruction.

But how fast does the MAC function really need to be performed? Although there's no "magic number," one indicator can be found by looking at present disk controller designs that perform the function using dedicated DSP chips such as TI's TMS320C10s or C15s. "In general, our part competes with the TMS320C15-type devices that have multiply/accumulate times of the order of 320 to 460 ns, depending on the clock speed," says Walter Bacharowski, technical marketing manager at National Semiconductor. Parts such as TIs dedicated DSPs have already been used on 2.5-in. drives (see "Shrinking drives push controller integration," *Computer Design*, June, p 67).

On the A-D conversion front, most processors sport 8-bit converters. Zilog's processor has an 8-channel, 8-bit, half-flash A-D converter that has a maximum 2- μ s conversion

8-bit microcontroller with on-chip DSP



Zilog brings DSP on-chip with the Z86C94. The 8-bit microcontroller features a fast programmable DSP in addition to a hardwired 16-x 16-bit multiplier.

time. The National part, on the other hand, sports an 8-bit, 5- μ s successive-approximation device. Based on National's ADC0838, the A-D can continuously scan one or several channels, or it can be triggered to perform single readings or scan operations. When continuously scanning into one channel, the converter can load results sequentially into eight data registers. Zilog's on-chip A-D converter can be used in a similar fashion. Most disk drive applications demand a 5- μ s conversion time, but the smaller the conversion time, the more designers like it. Some don't care if the converter is flash, just as long as it's faster than 5 μ s. Some would rather not have flash, because flash is inherently a more-expensive conversion technique. Zilog, in fact, designed a half-flash for just that reason. There are designers, however, that demand the speed, and are willing to pay for it.

Intel's microcontroller ups the ante by incorporating an A-D converter on-chip that can be programmed to either 8- or 10-bit mode. But there are problems.

Few manufacturers can put a con-

verter on a controller that's fully accurate to 10 bits all the time. "One of the things you will find in Intel's spec sheets is that if you add up all the linearity errors and differential nonlinearity errors, at 10 bits Intel's converter is no better than an 8-bit converter," derides National's Bacharowski. "The faster the A-D converter, the faster you can execute a servo seek," says Zilog's Vroomen. "But speed is more important than resolution," he concludes.

■ PWMs must be accurate—and fast

When the output from a microcontroller's on-chip PWM is used, a question arises as to how much accuracy is required? Designers agree that the accuracy of the PWM should be at least equivalent to a 10-bit D-A converter. But not only must it be accurate, it must be fast. Hence, the frequency of the PWM has to be high. In low-power environments, however, high speed equates to high power—and that's undesirable. In general, PWM techniques don't supply sufficient speed for actuator servo control. In this application, designers would probably use a

10-bit D-A converter external to the processor instead, relegating the PWM channel to spindle motor control.

Unless, of course, a D-A converter was available on-chip. In the Zilog chip, it is. The device's D-A converter can be used directly as the output to the servo channel to drive the voice coil positioning motor. "Ideally a converter that offers between 8- and 10-bits of resolution is needed," says Vroomen. Zilog offers an 8-bit resistor-string D-A converter with a programmable-gain output buffer. The chip can be used to drive output loads directly.

The final question is whether or not designers need to embrace a 16-bit microcontroller part when so much of the functionality of the rest of their disk control

subsystem has been relegated to special function units. That's all going to depend on what price/performance point they're attempting to meet with the drive itself, as well as what added functionality or accuracy they may need to add to get an edge in the marketplace. But as for price, there really isn't much in it. In 1,000 piece quantities, Motorola's part, Intel's part, and National's part all cost between \$20 and \$25. Zilog's is \$15. ■

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Emphasis shifts from density to I/O in low-density arrays

Barbara Tuck, Senior Editor

After proving that silicon process technology has advanced to the point of turning out gate arrays with hundreds of thousands of gates, semiconductor vendors are now getting around to putting that advanced silicon to work for the majority of their customers. It seems that the silicon giants are finally looking at figures such as those from Instat that show the expected average gate count to be only 14,125 this year and 18,150 gates by 1994. These figures indicate that the majority of designers today require ASICs that have somewhere between 5,000 and 15,000 usable gates with lots of I/O pins to accommodate wider and wider buses.

Shifting away from gate density

Both Hitachi America (Brisbane, CA) and NEC Electronics (Mountain View, CA) recently introduced gate array masterslices with design changes that target the density and performance of I/Os rather than gate density. To reap the cost and performance benefits of smaller line widths, Hitachi has staggered the I/O pads and reduced the I/O pitch on its arrays. Hitachi even gives the cost per I/O rather than per gate for its four 0.8- μ m CMOS HG62G masterslices—approximately 7 to 10¢ per I/O in quantities of 10,000. NEC, which reduced the pad pitch on its eight new masterslices but didn't stagger I/Os, puts the cost per I/O of the 1- μ m CMOS-6V arrays at an average of 6¢. In addition to increasing I/O-to-gate ratios, the low-to mid-density arrays also address designers' packaging, testability and memory requirements.

The 0.8- μ m, two-layer-metal CMOS masterslices in the Hitachi HG62G series have from 14,000 to 35,000 raw gates and from 160 to 240 I/O pads. Whereas a standard 144-pin QFP, with a 0.65-mm pin pitch, has a body size of 28×28 mm and a total package area of 1,024 mm², the 0.50-mm fine-pitch 144-pin QFP that Hitachi plans to offer for all four of its masterslices (second quarter of next year) has a 20×20-mm body size, and 484-mm² total package area. A fine-

pitch 208-pin QFP, with body size and package area identical to the standard 144-pin package, is available now for the two denser arrays. Hitachi plans to have high-power PQFPs available for the HG62G arrays by the second quarter of next year.

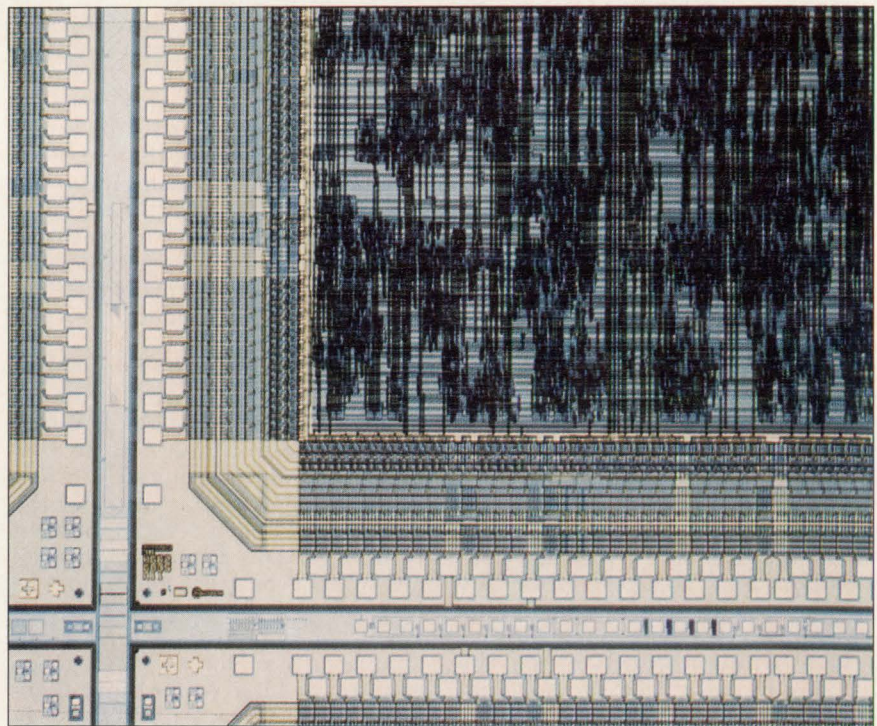
Increasing I/O performance

According to Hitachi, design changes to the periphery of its arrays increased I/O performance. The input buffers of the Hitachi arrays typically exhibit a 1.1-ns delay with a fan-out of three and 3 mm of metal. Delay in the output buffers is typically 1.8 ns with a 50-pF load (1.3 ns with a 15-pF load). Internal gate delays are typically 0.3 ns (0.54 ns worst-case) for a two-input power NAND gate with a fan-out of two and 2 mm of metal. For a nonpower NAND, the typical spec is 0.45 ns. With a fan-out of three and 3 mm of metal, internal gate delays are typi-

cally 0.56 ns (1 ns worst-case) for a two-input power NAND and 0.72 ns typically (1.3 ns worst-case) for a nonpower NAND. Single-output buffers can supply 24 mA of output current. Typical power dissipation is 9 μ W/MHz for each internal gate.

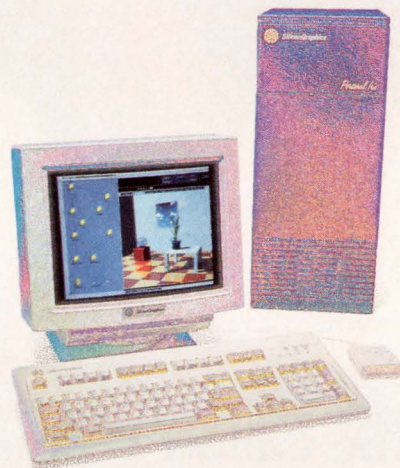
The CMOS-6V NEC arrays, which expand NEC's CMOS 6-gate-array family, range in density from 5,544 to 30,720 gates and 140 to 220 I/Os. Al Chiang, product line manager for NEC, says that the NEC arrays target PC designers who in the past have been frustrated because their designs were I/O limited. "Designers had to use arrays with a higher gate count than necessary." According to Chiang, because NEC's arrays combine high I/O and low gate count, they reduce ASIC unit costs.

As for addressing customers' high-I/O packaging requirements, NEC offers fine-pitch, 0.5-mm packages for 100-pin devices (14×14 mm), 120-pin (20×20 mm), 160-pin (24×24 mm), and 208-pin (28×28 mm). Packages for 144- (20×20 mm) and 176-pin (28×28 mm) devices presently come with a 0.65-mm pitch only.



Hitachi tightened the I/O pitch on its HG62G gate arrays by staggering the on-chip bonding pads, thus reducing die size up to 60 percent. HG62G arrays, with just 14,000 to 35,000 raw gates, target I/O-intensive applications.

When does it pay to synthesize?



Ask Silicon Graphics.

Ta-Wei Chien and his team have already designed ten chips with Synopsys. "Synthesis helps us meet very rigid price/performance ratios," says Ta-Wei. "We've been able to get to market faster by cutting our prototype development time and by streamlining the management of our chip databases." Using advanced design methodologies like synthesis, this group of engineers at Silicon Graphics is now seeing threefold gains in productivity. Measurable bottom-line results have convinced Ta-Wei: "Nobody wants to do schematic entry anymore."

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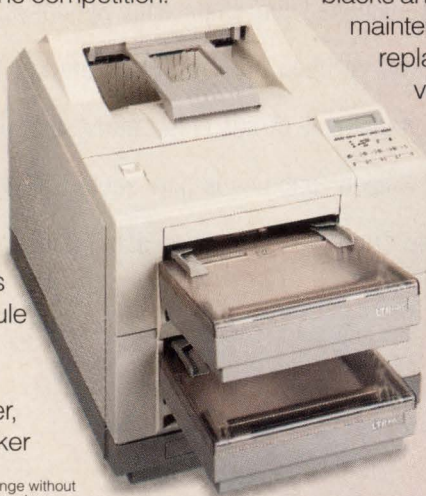


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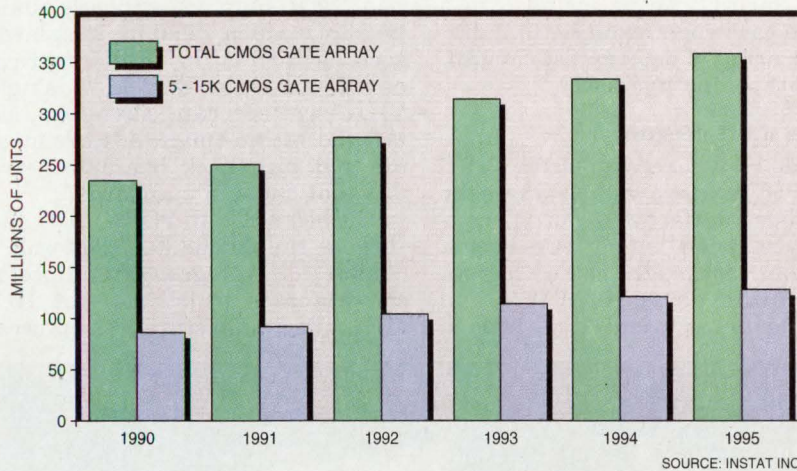
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Though this graph from Instat shows that the number of low-gate count designs will decline over the next four years, the average gate count worldwide, is expected to be only 14,125 this year and 18,150 by 1994.

The typical input buffer delay for NEC's arrays is 1.25 ns with a fan-out of three and 3 mm of metal. Output buffer delay is typically 2 ns with a 15-pF capacitive load. Internal gate delays are typically 0.4 ns for a two-input power NAND gate (0.5 ns typically for a nonpower gate) with a fan-out of two and 2 mm of metal. With a fan-out of three and 3 mm of metal, typical internal gate delay for a power NAND is 0.46 ns (0.7 ns typically for a nonpower gate). The CMOS-6V family has an output drive variable to 18 mA. NEC puts power dissipation at 8 μ W/MHz for each gate.

Testability

To address testability issues in the HG62G series, Hitachi has integrated a scan bus capability that it says improves fault-detection efficiency while remaining transparent to the design process. The scan-type auto diagnostics are useful even in circuits combining memory with random logic, according to Hitachi. Though an Hitachi RAM compiler won't be released until early next year, fixed RAM blocks are currently available for the HG62G arrays. Software support for Hitachi ASICs is available from Mentor Graphics, Valid Logic Systems, ViewLogic Systems, Cadence Design Systems,

and Synopsys.

NEC will make scan macrocells available for its gate arrays by December. For testing its fixed RAMs and ROMs, NEC has incorporated built-in self-test (BIST). Though a RAM compiler is expected to be made available in the future, NEC has no immediate plans for its release. Slow rate buffers that control the rise and fall times of the output buffer have been incorporated into the arrays. CMOS-6V arrays are supported by NEC's OpenCAD system. ■

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CIRCLE NO. 28

3U VME moves into PLC world

Warren Andrews, Senior Editor

Programmable logic controllers (PLCs) have long been the almost exclusive domain of proprietary architectures for a number of reasons. Aside from tradition, the most important factors in selecting conventional PLCs over more "intelligent," standard computer-based approaches are their special requirements for communication, I/O and programming environment. These obstacles are now addressed by a new family of VME-based PLC-like products. In addition, the approach being taken by PEP Modular Computers (Pittsburgh, PA) promises additional flexibility with a variety of networking schemes, as well as scaled-down versions, to lower node costs to as little as \$300 per node.

PEP's approach, dubbed VIUC (VMEbus Intelligent Universal Controller), combines a high-performance processor, a network controller and an I/O with VMEbus interface circuitry providing the essence of a PLC on a single 3U VME card. The approach lets PLC programming, maintenance and continuous process improvement take place in standard PLC languages, sequential function charts and relay ladder logic. C code programming can also be used.

PEP has also streamlined its approach somewhat, offering standard 3U VMEbus and scaled-down non-VME versions to handle the entire spectrum of automation tasks from PLCs and cell controllers, to higher-level computing roles on the factory floor and in the office. "The combination," says PEP president Josef Kreidl, "brings real-time intelligent performance and industry standards to a market dominated by single-vendor solutions."

In the VMEbus configuration, PEP's approach lets a VIUC handle either a full PLC's tasks as a single board, or operate in a larger system with other VME cards. In a system configuration, the VIUC handles all host processor and communication functions while 3U VMEbus boards from any VMEbus manufacturer can be used to provide I/O. As in any standard VMEbus configuration, up

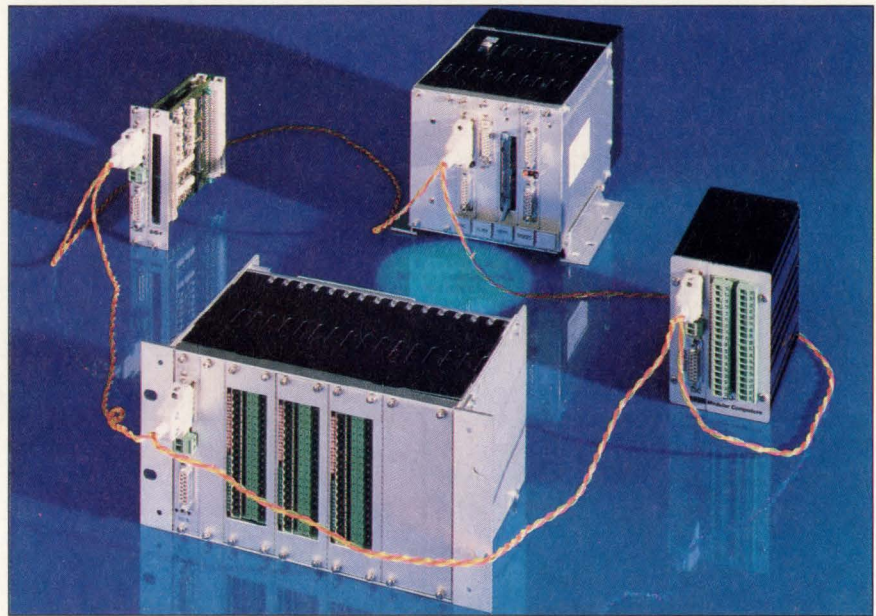
to 21 boards can be installed in a single card cage resulting in a dramatic array of deterministic, multi-tasking computing power.

■ The short version

A scaled-down version of the VIUC (the IUC) is also available where the VMEbus interface and controller circuitry has been "left off," says Kreidl. PEP has reduced the size of the card by scaling down the VIUC and making it easy to embed the node in

viding individual configurations via small piggy-back adapter (daughter) boards to meet a broad variety of serial needs from RS-232 and RS-485 to fiber-optic modems. In addition, PEP supplies software adaptation to various fieldbus standards such as BitBus in North America, and Profibus in Europe. A single VIUC system can, therefore, be tailored with a small software module and piggyback board to serve different network standards.

The heart of both PEP's VIUC and IUC is the MC68302, Motorola's (Austin, TX) integrated multiprotocol processor which runs at 16.7 MHz. The architecture of the proces-



PEP Modular Computers offers its PLC boards as standard 3U VMEbus boards, or without the VMEbus interface for embedded applications. The non-VME version of the processor/controller significantly reduces size, cost and power dissipation.

a robot arm or other machine; it's also reduced the cost from \$1,170 for the VME version to \$580 (quantity one) and it's scaled power dissipation to 1.5 W for the IUC from 3.5 W for the VIUC.

Both the VIUC and the IUC communicate via a twisted pair at distances up to 1,200 m. Using what has become a generic twisted-pair approach known as fieldbus, PEP's boards implement standard network protocols and protocol conversion such as Ethernet and X.25.

Systems provide three serial communications controllers with DMA and two front-panel I/O ports pro-

cessor gives the board 68000-class computing power in addition to providing a separate RISC-based processor core to handle the communications and protocols.

The VIUC and IUC also have a separate universal DMA channel, three timers, interrupt controller, and dual-ported RAM. Each board can accommodate up to 4 Mbytes of DRAM, 1 Mbyte of EPROM and 64 kbytes of EEPROM or battery-backed SRAM. The VIUC includes full VMEbus interface circuitry including master/slave capability and full system-controller functions.

Each board also provides a local

I/O extension bus that lets it accept a wide variety of PEP controller extension modules. These daughter-board modules are different from the small snap-in modules used in the communications port because they are larger and allow more flexible I/O. Either digital or analog I/O modules can be used from PEP's standard catalog of functions, or OEMs or users can design their own.

■ **Software approach**

The VIUC uses a software model that embraces every consideration for deterministic performance, fieldbus communications, standard network protocols and protocol conversion, applications, and system

To date, only a handful of OEMs supply PLCs based on both hardware and software standards. A handful of PC-bus-based PLCs are available, but do not truly adhere to the standards.



development. In the latter category, the VIUC software philosophy provides programming in both C and world-standard IEC848 sequential function charts and relay ladder logic. To implement graphical programming for both of the latter, PEP provides a comprehensive programming package it calls ISaGRAF which, in addition to easing development with inexpensive personal computers, provides on-line maintenance and upgrades using the same machines.

PEP's ISaGRAF is a graphical, windowing software toolkit that lets process and control engineers develop, simulate and debug control code the way they think, using well-known IEC-848 GRAFCET. The ISaGRAF-developed relay ladder logic code is then compiled and runs as a task on Microware's (Des Moines, IA) OS-9 multitasking real-time operating kernel.

"We're also developing ISaGRAF ports to Ready Systems' (Sunnyvale, CA) VRTX and Wind River Systems' (Alameda, CA) Wind real-time pro-

ducts," says Randy Ridenour, PEP's CEO and executive vice-president.

■ **A boost for 3U VME**

The advantages of using standard software and hardware in place of conventional PLCs has long been recognized, but OEMs have shied away from such approaches for much the same reasons that main-line computer makers kept clear of standard architectures—afraid of losing their proprietary, competitive edge. Now with PEP's family of products leveraging off the broad base of VMEbus products and accumulated experience, OEMs will be looking for such standard solutions.

To date, only a handful of OEMs supply PLCs based on both hardware and software standards. A handful of PC-bus-based PLCs are available, but do not truly adhere to software and hardware standards. Similarly, a number of 6U VMEbus systems are made, but the larger form factor makes them less attractive (and rugged) in many factory

environments.

Though most VMEbus card makers don't offer 3U cards, Ridenour points out that 3U VME is identical in interface and control as 6U and the expertise to do one is directly transferable to the other. "As the 3U business calls for new boards and demand ramps up, I expect the main-line VMEbus board makers like Motorola (Phoenix, AZ) will begin to offer 3U products," says Ridenour. ■

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Walls between E-CAD and M-CAD start to crumble

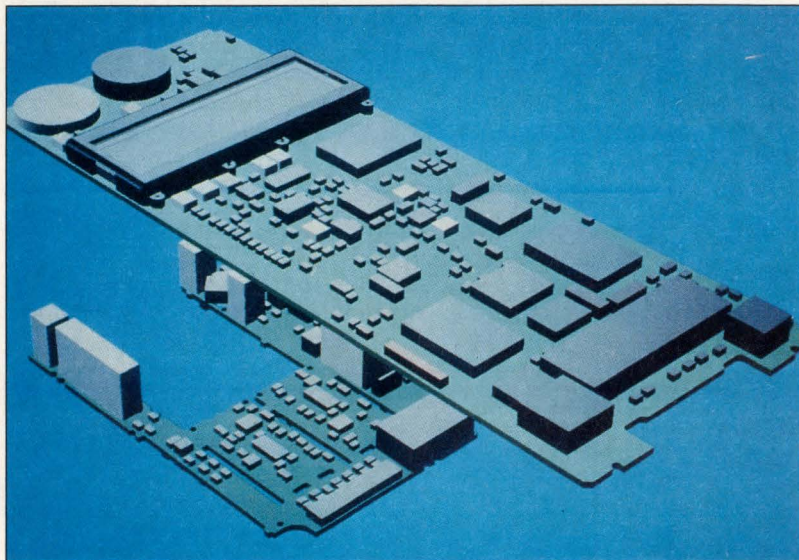
Mike Donlin, Senior Editor

System manufacturers are realizing that to overcome time-to-market pressures, they must integrate the electrical portions of a circuit board's design with the system's mechanical requirements. After all, a perfectly working PCB isn't much good if it doesn't fit into the backplane. As a result, many of the walls separating electronic and mechanical design environments are starting to crumble. Recent agreements between electronic CAD (E-CAD) and mechanical CAD (M-CAD) tool vendors signal that concurrent engineering—the solution to this necessary integration—is becoming more than a marketing buzzword.

Mentor Graphics (Wilsonville, OR), for instance, has entered into an agreement with M-CAD vendor Structural Dynamic Research Corporation (SDRC) (Milford, OH) to provide links between SDRC's I-DEAS mechanical tools and Mentor's Board Station PCB design tools. Essentially, the agreement means a mechanical engineer can take PCB designs from the Mentor tool and generate I-DEAS solid models, allowing for system-level design changes and analyses. Board geometry and layout modifications can then be back-annotated from the mechanical to the electrical design side. Though this transfer might seem an obvious connection between the two disciplines, the type of data each side needs differs and melding the needs of each to the other is a challenge. The interface SDRC has developed is a starting point in this transition.

"When we started our interface,

we had to decide on the specific types of data that we needed to send," says Edwina Wedeking, industry marketing manager at SDRC. "If you're not careful, you can end up sending a lot of information back and forth needlessly.



The I-DEAS interface from SDRC takes component shapes from a solid models library or from footprint and height information encoded in the PCB layout data. The resulting solid model can be used for interference checking, manufacturability requirements, structural, thermal, and vibration analysis.

In the case of creating a mechanical model of a PCB, for instance, you don't need routing information to know if the board is going to fit in a system."

Finding the right approach

Though Mentor and SDRC have agreed to use a custom interface to port data between tools, some companies have opted to use the standard Initial Graphics Exchange Specification (IGES) to translate design information. Hewlett Packard (Palo Alto, CA) decided to use IGES after it left the EDA business about a year ago to focus on its M-CAD and database tools. To ease customer anxiety, HP developed translators to other EDA vendors' tools and is providing customer support during the transition. Mentor Graphics was the

first EDA supplier to link to HP's ME 10 2-D mechanical design and drafting software via the IGES standard. Though IGES isn't as sophisticated as the custom links built by SDRC and Mentor, it had what HP needed—a readily available, workable format that both companies could immediately use. The interface is based on 2-D geometry, which means that HP's solid models must be flattened to 2-D to port its ME 10 product to the Mentor Board Station. Both Mentor and HP are working

to refine the interface to include more intelligent capabilities, such as the ability to recognize components and connectors as such, rather than as a series of arcs and lines.

In addition to Mentor, SDRC has used its interface to link up with other PCB tool vendors—Racal-Redac (Mahwah, NJ) and Valid Logic Systems (San Jose, CA)—agreements that further signal this trend of moving mechanical design concerns into traditional EDA environments. But as more of these relationships evolve, EDA

and M-CAD companies must decide to adopt and refine existing standards, or develop proprietary interfaces.

"There are problems with both of these approaches," says Keith Felton, manager of CAD/CAM at Racal-Redac (Tewksbury, Gloucestershire, U.K.) "If the interface that you use isn't independent, you end up tweaking it as the tools from each side develop. This can get to be difficult if you're supporting a number of different interfaces as Mentor is proposing to do."

Racal-Redac is developing a proprietary EDIF-based interface called CADIF, which it claims will address this problem of a truly neutral interface. "We take the data from our Visula design system and put in an EDIF-style syntax," explains Felton.

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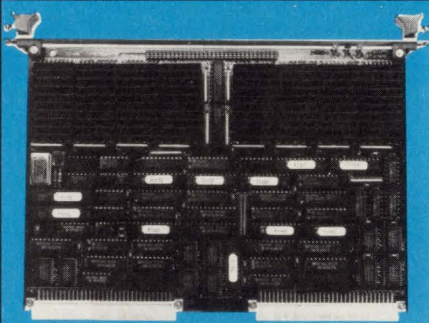
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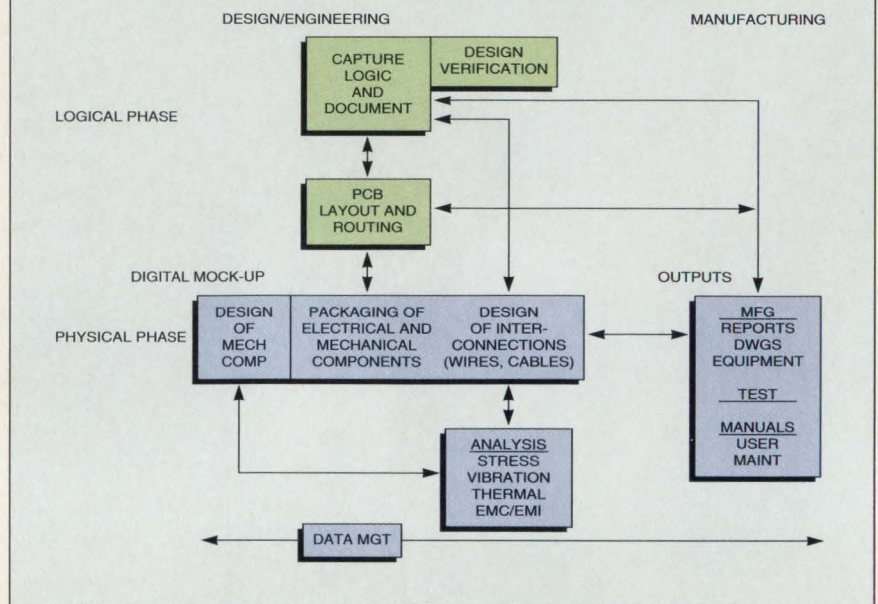
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TECHNOLOGY DIRECTIONS

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The Mechatronic approach



Computervision is integrating its electrical and mechanical design tools with a methodology dubbed the Mechatronic Approach. This divides system development into two phases—logical and physical—which must be executed simultaneously.

“We output that data and encrypt it so it can’t be directly read. We then provide C tools that act as a procedural interface to access that information. The data underneath—the CADIF part—can change as the tools change, but any interface written with our C tools will always work.”

Though the strategic alliances and interfaces are focusing on the integration of independent tool sets, some EDA vendors claim to already have all the necessary elements for such an integrated suite. For instance, Computervision (Bedford, MA), a part of Prime Computer (Natick, MA), has leveraged its M-CAD expertise and coupled its CADD5 4X mechanical design environment with its Auto-board PCB design tool. The CADD5 4X model of electrical and mechanical components and packaging can be used to determine the required board outline as well as height restrictions, keep-out areas and mounting hole locations. With its purchase of Dazix (Sunnyvale, CA), Intergraph (Huntsville, AL) has also entered the fray and boasts an impressive suite of electrical and mechanical design tools. But in spite of the strong showing both companies are making in the electromechanical arena, some

users are leery of buying into suites that contain proprietary tools and interfaces.

All's not rosy

Despite the apparently seamless integration of these disciplines—M-CAD and E-CAD—there are some users who aren’t satisfied with early results. Two users, who asked not to be quoted, hold out hope for smoother integration of these tools in the future, but pointed out many of these partnerships and tool suites leave something to be desired. One in particular, a European manufacturer of electronic modules for transportation equipment, said the information passed from the electronic to the mechanical side was helpful, but inadequate. The electrical design information passed along to the mechanical tools enabled them to predict the physical space required for an electrical housing, but the actual wiring of the module was done by hand. In other words, the electrical design data didn’t really represent the finished product.

Most of the work involved in melding the two design disciplines will undoubtedly take place in the library arena. The trick is to include enough information in the EDA

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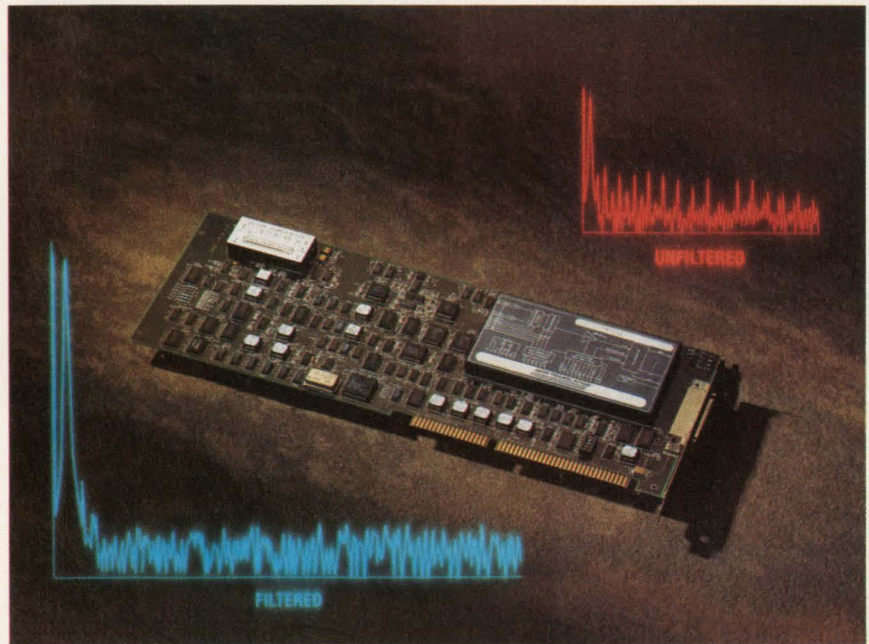
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model without ending up with a device model that's too unwieldy for use by either the electrical or mechanical tools. "There are basically two ways to generate the component's shape to three dimensions," says SDRC's Wedeking. "Either the interface looks at the data from the electronic design and cross references that to a library of parts for mechanical considerations, or the information is read directly from the layout to generate a model. Our latest enhancement lets us read the footprint and height of components directly from the electronic data to generate the model of the PCB for interference checking."

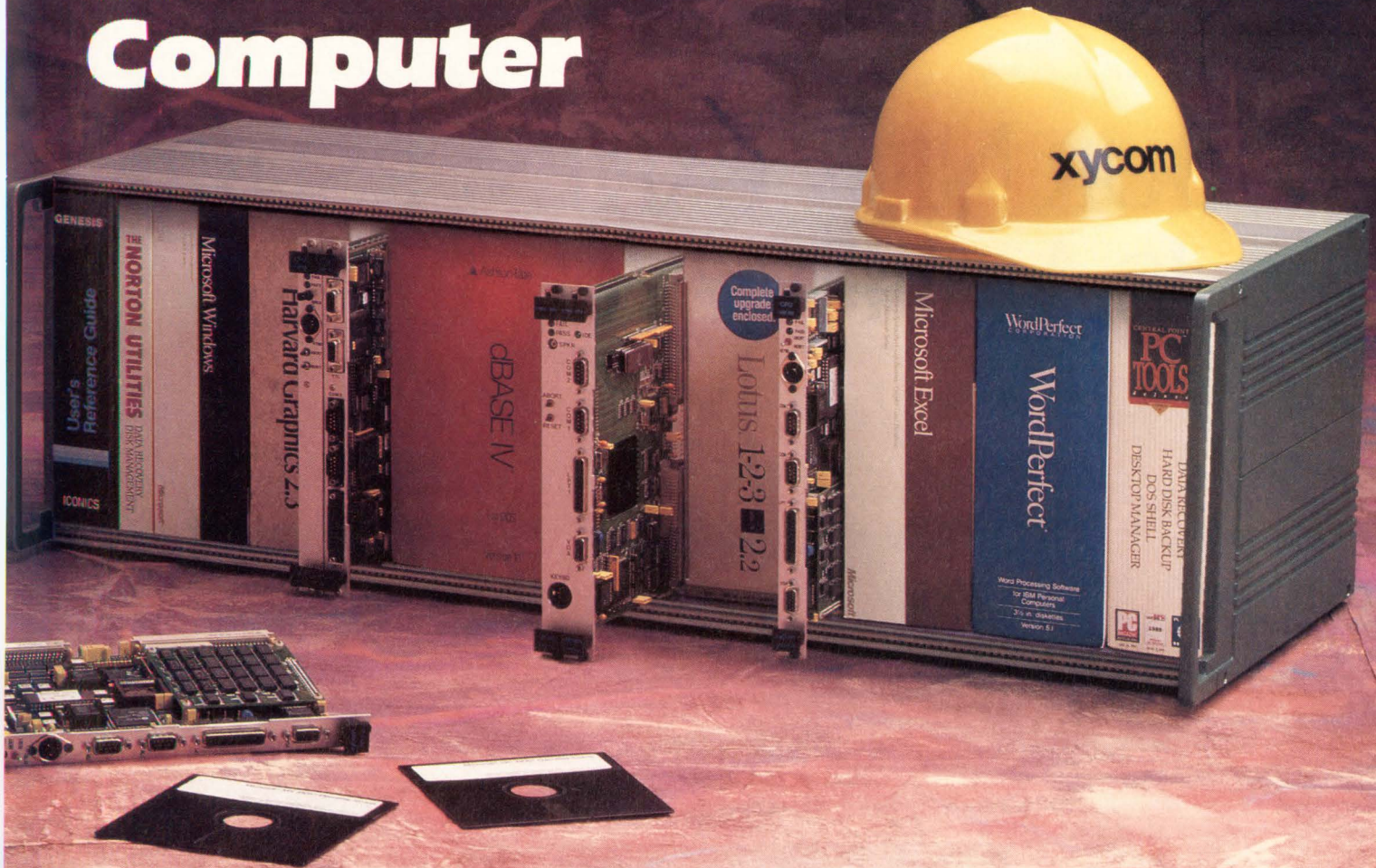
Such an approach, however, necessitates the inclusion of height and footprint data in the electronic model. At present, this must be provided by the EDA vendor, or in the case of a custom part or an ASIC, written by the customer.

The challenge in designing these interfaces is a technical concern, but there are also issues that strike at the heart of a company's design philosophy. Exactly who determines which needs are uppermost—mechanical or electrical—will be a source of debate as the two disciplines share data and engineering concerns. "The goal is to solve mechanical problems before committing to a layout," says Bob Kross, manager for mechanical products at Mentor. "If a designer can move a few components around without affecting the performance of a board, it's a lot better than having to add some extra cooling devices during manufacturing." ■

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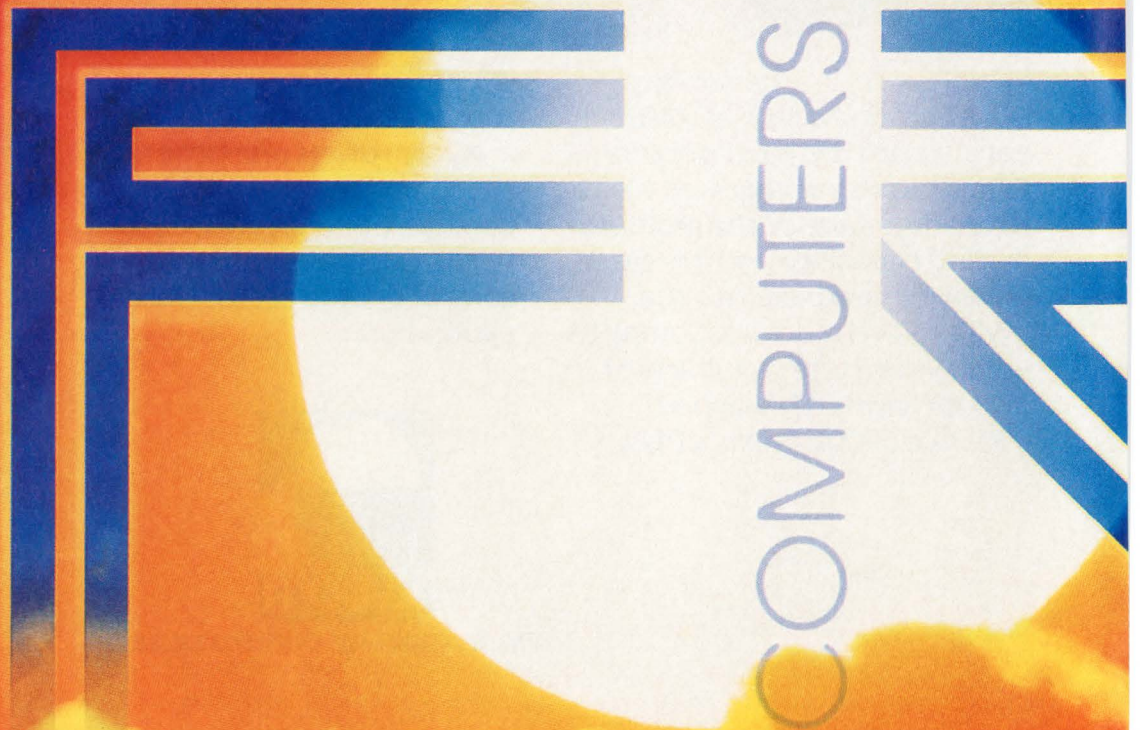


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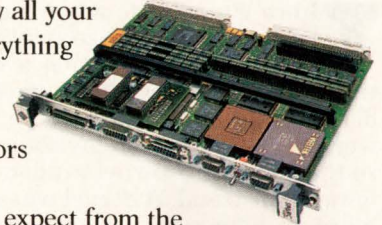
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CIRCLE NO. 34



User demands push real-time vendors into software alliances

Tom Williams, Senior Editor

There was a time when a company could make a secure living selling and supporting a real-time kernel. Then came increased demands for tool support and a networked development environment, so the successful kernel vendors followed that trend. A kernel was sold more in terms of its development tool support than by virtue of its raw performance. Now, the move toward open systems in the general-purpose computing world is spilling over into the real-time arena. The call for Unix compatibility is being heard more often, especially in the move toward a standard interface motivated primarily by the U.S. government. This will probably begin a move toward strategic alliances as kernel vendors seek to include additional Unix-like layers to enhance the applicability of their core products.

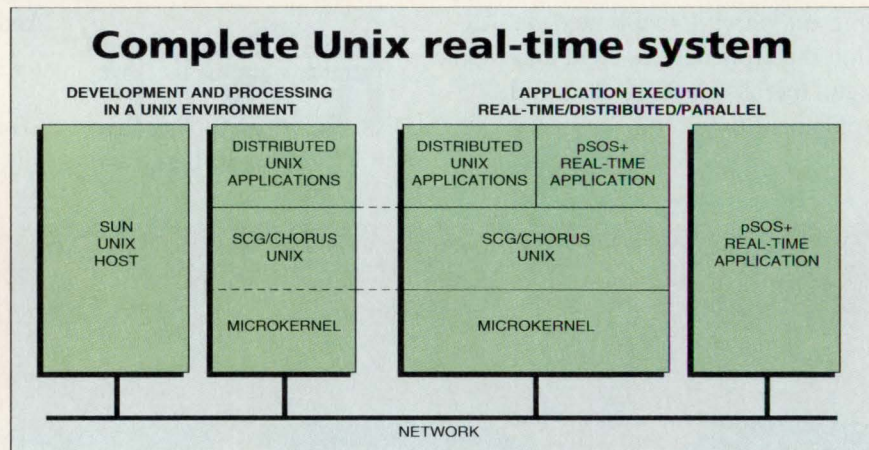
Finding the right mix

Real-time Unix systems that were conceived from the start to combine real-time performance with Unix compatibility may have an advantage when it comes to addressing the open systems/real-time trend. Companies that have developed these systems include VenturCom (Cambridge, MA), Modcomp (Ft. Lauderdale, FL), Lynx Real-Time Systems (Campbell, CA), and hardware vendors such as Hewlett-Packard (Palo Alto, CA) and Harris Semiconductor (Melbourne, FL). At least one kernel vendor, however, has seen the writing on the wall and is forming alliances to offer real-time, open systems software products across the wider range of system configurations. Software Components Group (San Jose, CA) has formed an alliance with Chorus Systemes (Paris, France) that will integrate SCG's pSOS+ real-time kernel with Chorus' Chorus Mix microkernel-based, Unix-compatible operating system technology.

The Chorus approach is based on a microkernel, but with a Unix-compatible application interface. Between the two is a set of services

called "servers" that are called by the Unix API (application programming interface) and make calls to the microkernel. The microkernel can run services on any processor in a multiprocessor system that's free. This results in dynamic load balancing and fast performance but lacks the strict determinism demanded by many real-time applications. Adding pSOS+ capability to such a system would let the designer

The product integration will cover what's loosely defined as a range of "hard" and "soft" real-time systems, according to SCG president Alfred Chao. Hard real-time systems are thought of as those traditionally served by the pSOS+ product with high speed and very strict timing requirements, such as avionics or real world device control. "Soft" real-time includes process-control applications with fairly loose timing requirements, switching systems and test and measurement. The systems are usually larger than the "hard" embedded types and may often require a user interface. "We entered into this relationship with Chorus to pro-



A networked system using a combination of standard Unix, Chorus microkernel- and pSOS+-based applications can combine different levels of real-time performance along with distributed nonreal-time applications and be accessible via the Unix user interface.

bind tasks, which demand such capability, to pSOS+ and to given hardware resources while leaving the overall system to Chorus.

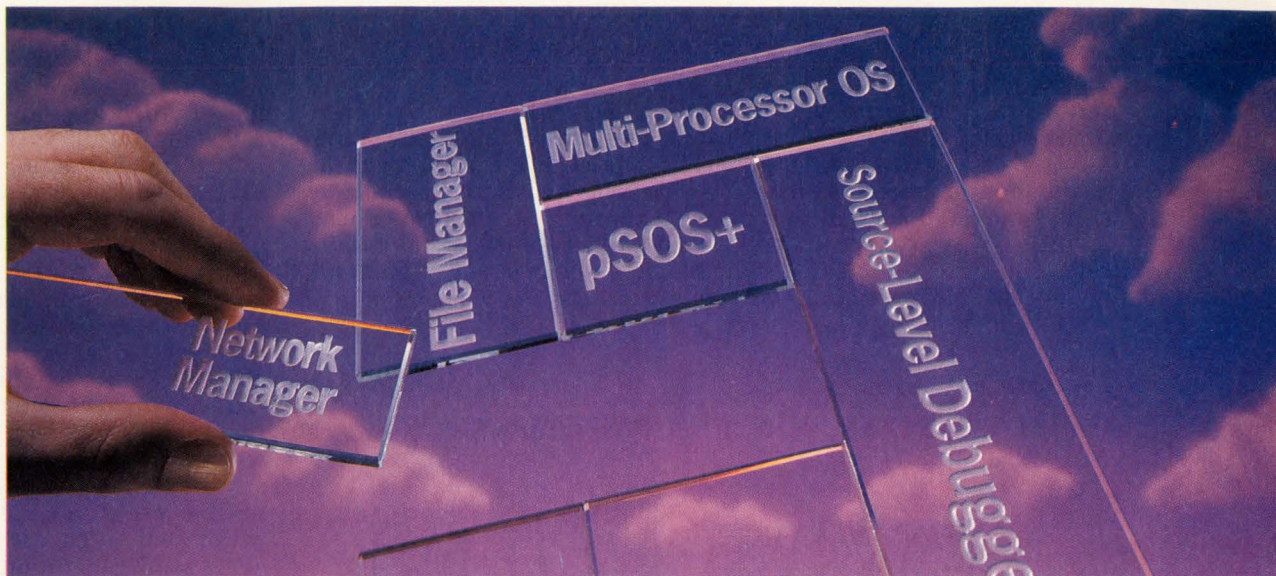
The server arrangement lets a user modify, for example, a process, a file or communications server without contaminating the rest of the Unix system, says Robert Anundson, vice-president of new business development and marketing for Chorus. "In a uniprocessor Unix system, that's pretty tough because Unix has a lot of global variables and if you touch one it can be bad news." Because Chorus servers are encapsulated, Chorus tracks standards as they emerge, Anundson says. This will include the Posix interface standards that have already been adopted and the emerging 1003.4 real-time extensions to Posix.

duce a 'real-time Unix engine' to address the open system end of the market place," says Chao.

One-stop shopping

To that end, SCG plans to productize the Chorus Mix system as a binary—Chorus in the past has only licensed source code to computer manufacturers—and eventually provide a set of options that will include pSOS+. "pSOS+ is very fast and efficient," says Chao. "You can ROM it in 14 kbytes of code. And yet it's a proprietary operating system." So the resulting product line should result in a "one-stop shopping" decision for OEMs that will let them take a migration path from pSOS+ to a Unix-compatible system or let them mix hard and

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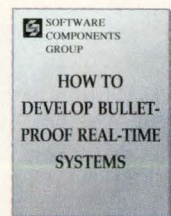
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soft real-time capabilities within the same system.

In another strategic move, SCG has also entered a merger with Integrated Systems, Inc (San Jose, CA). ISI has a very strong presence in the aerospace and automotive industry with its control engineering

design tools. Its SystemBuild product lets control engineers graphically represent a control algorithm as it's presented in control engineering texts and then engineers can use a tool called AutoCode to generate compilable source code. A limitation has been that the code is generated

for a hardware prototyping system called the AC-100 that consists of up to 10 80386-based single-board computers. ISI has written a specialized operating environment with drivers and communications facilities for the AC-100.

"But when people want to go to their own embedded environment they have to do extra work," says Naren Gupta, ISI president and CEO. The integration of pSOS+ into the ISI development environment will control code be generated for any processor that's supported by pSOS+ via AutoCode. AutoCode will be enhanced with a switch to allow code generation for the AC-100 or for pSOS+. "A system designer doesn't have to know a heck of a lot of code at all to implement a solution," says Gupta. PSOS+ will act as a sort of backplane that will let a user plug in hand-written or assembly code along with code generated from the System-Build/AutoCode environment. It will also allow the use of pSOS+ compatible debugging tools.

The SCG/Chorus/ISI constellation represents a strategic alliance model that other real-time software companies may follow to meet the demands of their customers, who are not only building larger and more open systems but are struggling with ever-increasing time-to-market pressures. "They need a more sophisticated implementation and a more integrated development environment," says Gupta. ■

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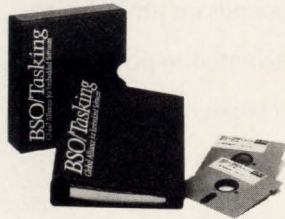
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RISC power moving scientific visualization onto the desktop

Tom Williams, Senior Editor

The concept of scientific visualization can be a slippery term because it's connected both with interactive (i.e., real-time) simulation and with the viewing of static data that has been collected from either a simulation or from events taking place in the real world. In both cases, the interactive viewing of 3-D color representations of data has until now been restricted to quite expensive systems. Now, thanks

blocks for OEMs to design desktop visualization systems and to upgrade existing designs with the needed graphics processing power.

Interactive visualization of a color 3-D model, such as a molecular model or a set of complex seismic data requires enormous amounts of number-crunching. An approximately equal amount of compute power is needed to produce a photo-realistic image from a set of design

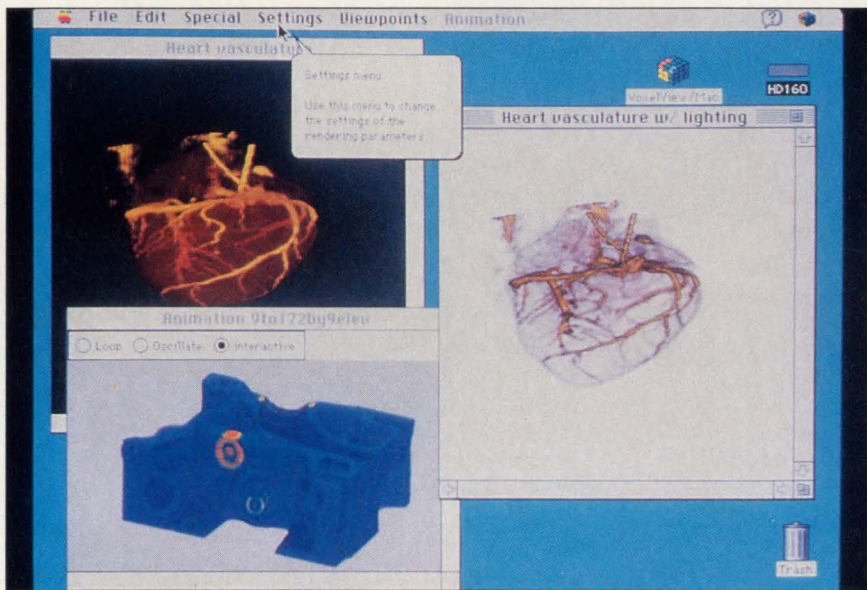
visualization to desktop workstations is the Fusion product line from DuPont Pixel (Newark, DE). The Fusion line consists of add-in boards for a variety of platforms along with an extensive array of software, including Fusix, an object-oriented programming environment for parallel processing. Fusix incorporates a portable application programming interface (API) and a microkernel for attached Intel i860 processors.

Desktop Fusion

The board products include the PX 10 and PX 20, called "Desktop Fusion," add-in cards which are available in a number of form factors including SBus, Micro Channel (MCA), ISA/EISA, and 6U VME. The PX 10 and PX 20 can be used to upgrade existing workstations such as the Sparcstation, the IBM R/6000 or 386/496 AT-compatible machines. The PX 10 contains one or two i860s running at 25 to 40 MHz. At full performance, it's capable of rendering 50,000 24-bit Gouraud-shaded, Z-buffered 50-pixel polygons/s.

The PX 20 has similar performance to the PX 10 but includes a 100-Mbyte/s inter-board bus called the PX bus. The PX bus can be used to communicate between multiple cards to increase performance or to multiple frame-store cards without burdening the backplane bus. Users are finding their own innovative applications for the PX bus as well, something DuPont Pixel encourages, says Mike King, marketing manager for DuPont Pixel.

The Power Fusion series, the PX 100 and PX 200, are implemented on 9U VME cards and are intended as add-ons for desk-side systems. The PX 100 has four i860s in a multiprocessing environment that can render 165,000 Gouraud-shaded polygons/s. The PX 200 uses the new i860XP processor for roughly twice the polygon processing of the PX 100. Each processor has a copy of the Fusix microkernel. The processors are tied together via the Fusix API, which is the layer to which Fusix applications make their operating system calls, so applications never really see the microkernel. The API/microkernel arrangement lets processors perform load balancing and also lets processors work on rendering operations or numeric processing of a simulation model if that's

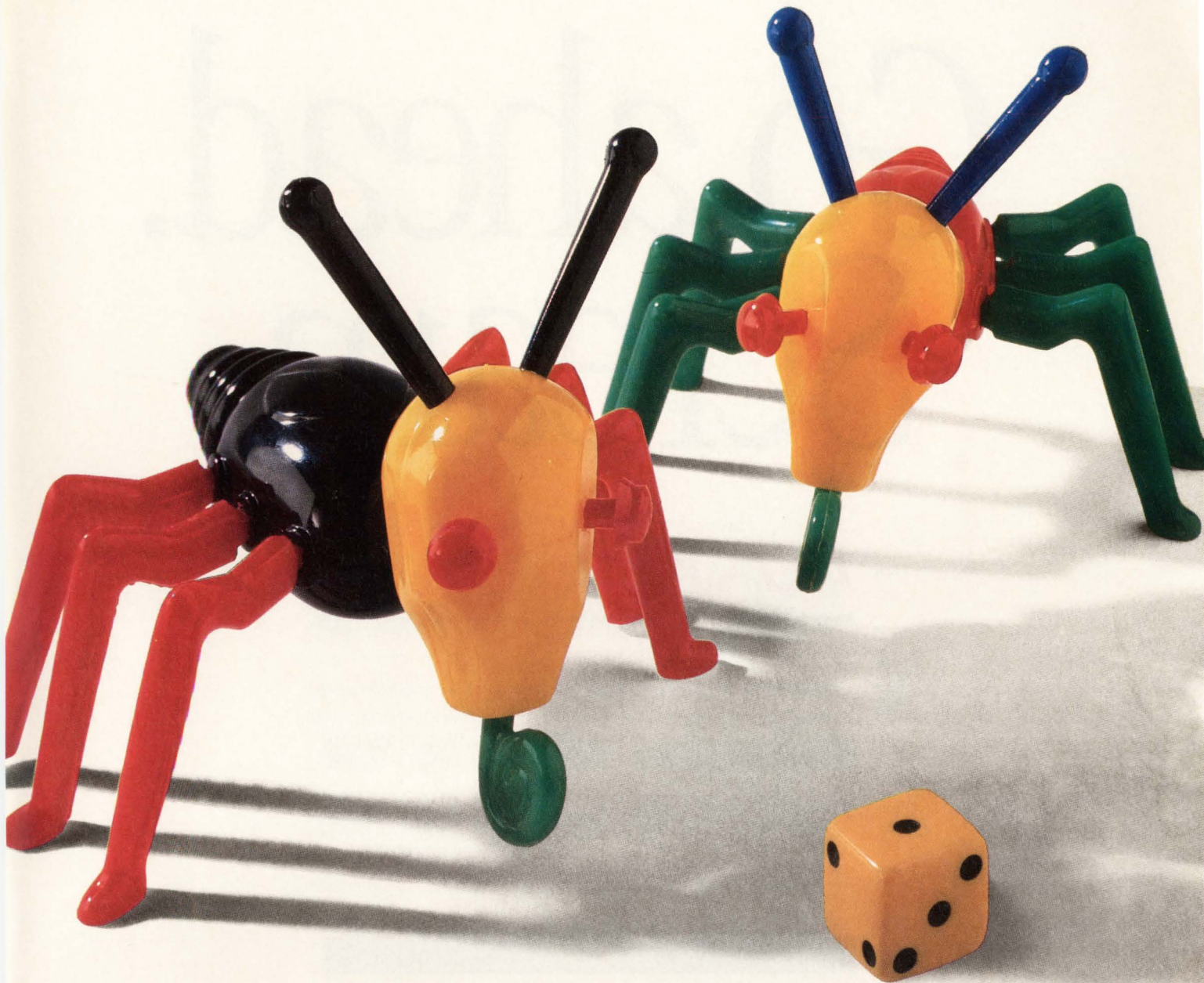


3-D data visualization on a desktop workstation with VoxelView by Vital Images. The computer tomography image of a heart can be filtered using image-processing techniques to highlight tissues of differing densities. Here the muscle tissue has been removed to view the network of blood vessels. The image can be rotated for viewing from all directions.

largely to RISC technologies, a good portion of scientific visualization is moving onto the desktop. In addition, another compute-intensive graphics operation, the photorealistic rendering of surfaces and lighting, is making the move as well. Not only are manufacturers such as IBM (Armonk, NY), Silicon Graphics (Mountain View, CA) and Stardent (Concord, MA) coming out with inexpensive systems with the power to view complex 3-D data, but board manufacturers and software vendors are producing the building

data. Such an image not only includes smooth surfaces and lighting models, but also textures, reflections of the surrounding scene, translucency, and shadows. When this kind of display is set in motion with a real-time simulation such as fluid dynamics, the processing demands skyrocket. Desktop visualization systems are starting to get a handle on the former (i.e., viewing the data) and to some extent on the latter (i.e., generating the data).

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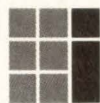


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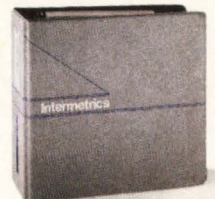
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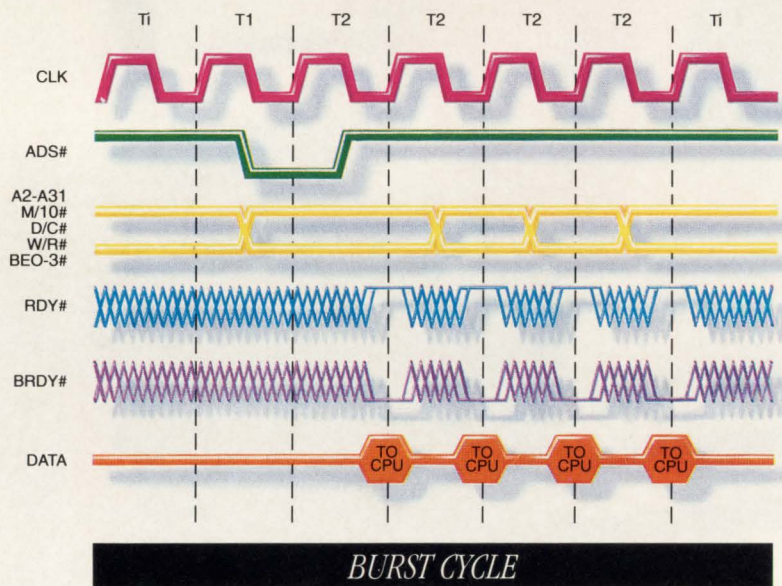


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what's needed at any given time.

The Fusix API represents a stable interface to the Fusix environment for porting a wide range of software. The Fusix API, for example, is the interface X-Windows is written to as well as Pex, the new 3-D protocols for X. In addition, DuPont Pixel has ported the Silicon Graphics' GL graphics library to the Fusix API, calling it PX/GL and providing portability to applications written to SG/GL. Silicon Graphics' GL is itself an API that's gaining ever wider acceptance in the industry. "It's very clear that the industry wants a single graphics API across all platforms and that PHIGS is not the API they want," notes King. PHIGS (Programmers Hierarchical Interface to Graphics Standard) had earlier been proposed as the API for Pex.

Aquest adds a board

The Intel i860 is showing up on board-level products for the AT ISA and EISA bus that are aimed at bringing visualization power to PC-compatible platforms as well. In addition to the DuPont Pixel Desktop Fusion products mentioned above, Aquest Products (Santa Clara, CA), for example, has combined an i860 along with a Texas Instruments TMS34020 video system processor on a single AT board. The ARC/1 uses an on-board 64-bit bus to connect the i860 with 2 to 16 Mbytes of DRAM and 2 Mbytes of VRAM and interfaces to the 32-bit TMS34020.

Aquest has developed a library of i860 routines that can be integrated with various CAD software packages, according to Aquest chairman Kanwar Chadha. The library routines process the wire frame models and render them as Gouraud-shaded solids that can then be manipulated for viewing by the user. While Intel has supplied an executive, called APX, which lets a host-based Unix operating system communicate with an i860 running on the same system, Aquest has developed its own executive that allows communication with the i860 from a DOS environment.

The i860 popular choice

Although many i860-based single-board computers can certainly be used for general computing applications, the i860 seems to be a favored

choice when it comes to graphics rendering because it contains multiple on-chip floating-point units and the circuitry to process 3-D graphics up to and including Gouraud-shaded surfaces. An almost identical architecture to the Aquest ARC/1 is the Superstation 3D by Hercules Computer Technology (Berkeley, CA). Hercules has teamed up with Modern Medium (Portland, OR) to port that company's RenderStar-2/i860 DOS-based rendering and animation software to the Superstation 3D.

RenderStar-2/i860 generates photorealistic images and animations from 3-D models. It includes high-

Many i860-based single-board computers can be used for general computing applications, but the i860 seems to be the favorite choice for graphics rendering.



end rendering techniques such as texture mapping; smooth shading; diffuse and reflective mapped surfaces; fast-shadow casting; and point, spot and linear light sources. A newer version of RenderStar-2/i860, RenderStar-2/Pro, will run in a dual-processing environment. The user interface will run on the DOS 386 or 486 while the rendering engine will run on the i860. According to Modern Medium technical sales support manager Larry Hewitt, "RenderStar is an entirely open system. That is, OEM companies can easily customize RenderStar," such as by integrating it into existing CAD software to produce photorealistic images of designs. "Our engineers provide 'hooks' in the software for outside developers' special needs," Hewitt says.

An exception to the dominance of the i860 is the Solids Engine board from Octree Corporation (Cupertino, CA). The Solids Engine is a 9U VME board for Sun-3 and -4 workstations and is also available as a desktop unit for Sparcstations. It incorporates a custom ASIC for dis-

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play of randomly placed voxels (the 3-D equivalent of pixels representing volumetric data) combined with constructive solid geometry (CSG). CSG combines points, lines, surfaces, and solid primitives with set operations to produce solid geometric forms. The Solids Engine also uses an Am29000 by Advanced Micro Devices (Austin, TX) for a shading processor.

Octree provides both turnkey application software, called TrueSolid, and OEM core libraries for custom visualization and modeling application development. TrueSolid is able to handle both CSG models of solid objects as well as volumetric data obtained from 3-D imaging systems such as CAT scanners, radar or sonar.

Superminis knocked back

High-performance desktop systems are attracting ports of rendering and visualization software systems that were originally intended for superminis, or "Crayettes." One example is VoxelView by Vital Images (Fairfield, IA). VoxelView performs image processing on 3-D volumetric data such as seismic data, CAT scan data, sonar and radar, and data generated by supercomputer simulations of

things such as fluid dynamics.

With VoxelView, it's possible to perform many of the kinds of image processing operations that are common to 2-D image data such as contrast enhancement and correction. The user can adjust rendering parameters such as opacity and filter out other densities to view, for example, only the blood vessels in a heart, or only saturated rock in a seismic survey. It's possible to explore a volume data set by rotating and slicing through it in any orthogonal plane to view the interior. VoxelView runs on Silicon Graphics' Iris systems using GL. The use of GL has made it relatively easy to port VoxelView to other systems supporting it such as the IBM RISC/6000.

Ready-made applications such as VoxelView and RenderStar-2 are already reaching end-users in low-cost systems designed around RISC processors. These include the Iris Indigo by Silicon Graphics, which is based on the MIPS R3000A processor and is priced under \$10,000, and the i860-based Vistra 800 series by Stardent. Stardent has ported its AVS visualization environment to the new "low-end" system for rendering and viewing static data.

These initial designs using RISC processors and, in many cases, software interface standards, show how quickly and inexpensively scientific visualization and photorealistic rendering—once the domain of supermini systems—are moving onto desktop machines. The existence of RISC-based board-level products oriented toward visualization and rendering will only accelerate this process. ■

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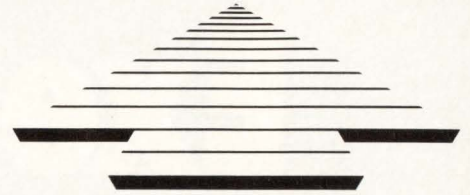
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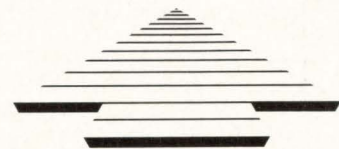
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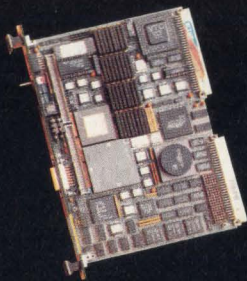
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CIRCLE NO. 44

RISC-based boards make headway in real-time applications

First-generation RISC-based boards are being replaced with zippy new models and real-time software support is becoming a reality.

Warren Andrews
Senior Editor

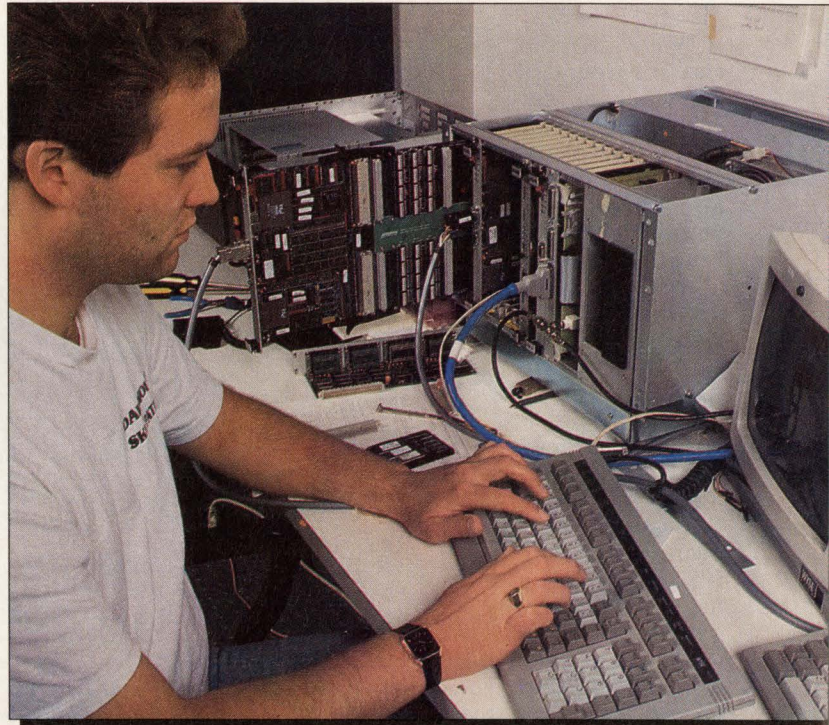
Only a few short years ago, RISC belonged to the realm of the academicians. Outside of classrooms and a few assorted research papers, no one believed it was a viable technology. Today, the tide has turned: traditional CISC architectures—the staid 680X0, and even the seemingly indomitable 80X86—are struggling for survival as advanced workstations, personal computers, real-time systems, and even embedded computers look to RISC for greater price/performance.

Real-time systems, particularly those based on standard-architecture boards, have been one of the last bastions of CISC. Protected on one side by a mountain of code that developers are reluctant to abandon, and on the other by delays in the availability of real-time kernels, CISC architectures have enjoyed protection from the RISC incursion. But that grace period is rapidly coming to an end.

Real-time kernels, as well as sophisticated development environments, are emerging for a variety of popular RISC architectures as kernel writers learn the intricacies of the various RISC architectures. And though designers may not be intimately familiar with the particular processor architecture, they are comfortable working with familiar tools such as VxWorks from Wind River Systems (Alameda, CA), pSOS+ from Software Components Group (San Jose, CA), and VRTX from Ready Systems (Sunnyvale, CA).

“There were two reasons for the slow acceptance of RISC CPU boards,” says Peter Zackin, marketing director for Cyclone Microsystems (New Haven, CT). “First, the tools were not there in terms of the development environment, and second, board makers had to travel at least some distance on the learning curve before products were viable.” Zackin’s evaluation proves itself in almost every case. As indicated, the tools are just now emerging, and almost every maker of RISC CPU boards has already developed a second-generation product—usually after some major problems with the first.

Cyclone, for example, had developed some 68000 family VME boards but



Software engineer Greg Ames is doing software development on several Cyclone Systems i960 CPU boards.

RISC-BASED BOARDS

became impatient with the time it took for major enhancements in processor performance. "We found that there was only about a 2x performance advantage with each new processor family generation (i.e., from the 68010 to the 20 to the 30, etc.) which takes about four years. System designers," he says, "continued to push for better and better performance. That's when we saw that RISC chips were starting to increase in performance at a much greater rate."

"We waited out the first round of RISC chips because there was a lack of real-time software—a critical component of board-level products. There are few developers out there willing to buy raw hardware, and even fewer willing to write their own real-time kernels," he says. Then Intel came along with the i960 and spent a lot of money getting a critical mass of software. It got Wind River to port VxWorks to the i960, which is now offered as Vx960, and it got Software Components to port its pSOS+.

More processors, more boards

The broad diversity of RISC processors has resulted in a number of new board types. With the advent of RISC, the traditional Intel and Motorola family processors have been augmented by at least five major RISC architectures: Sparc, MIPS, Motorola 88000, Intel i960 and AMD 29000. In addition, SGS Thompson's Transputer—which straddles the line between RISC and CISC—adds to the selection as do parts like Intel's i860 which straddles the general-purpose/specialized processor fence. To further cloud the issue, both the MIPS and Sparc processors are supported by a number of semiconductor vendors all with slightly different approaches, chip sets and levels of complexity. It's

expected this issue will become even more difficult as each chip manufacturer starts to offer multichip modules (MCMs) sporting different configurations of cache and other features such as floating-point processing, memory management and interface controllers.

While first-generation RISC-based boards have enjoyed only a modest success, a number of things have happened almost overnight to greatly enhance the acceptance of

ent versions are also specifically adapted for particular embedded applications or for more general-purpose use.

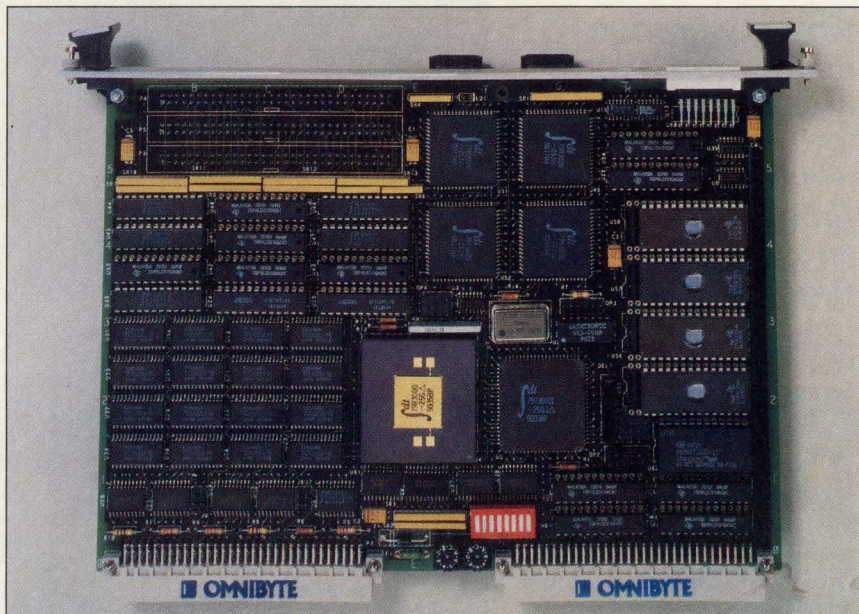
The wide acceptance of RISC machines in the Unix arena is having a significant effect on real-time applications for at least two important reasons. First, widespread use of RISC processors has served notice that the technology is real, and offers important price/performance advantages to system developers. Second, Unix-based machines provide a good development environment for real-time applications.

"The reality of RISC products," says Ed Schulman, vice-president of marketing at Ironics (Ithaca, NY), "is that it's necessary to focus on the board, rather than on the chip architecture. Many of the things often touted as major 'features' in CPUs, such as the chip architecture, register configuration, process parameters and other specifics of that particular RISC family, are totally irrelevant. The major thing

is that there are typically two types of boards—real-time and Unix-based."

"In the Sparc world," continues Schulman, "the Unix-based board is the Sun-1E board (alternately-sourced by Force Computers, Campbell, CA) which is a 6U VMEbus board running Sun/OS. Alternately, there's a Sun-2 board, which is a non-VME board and Force is expected to release a VME version of the Sun-2 later this year." Schulman says that these parts offer a solid host environment and provide a robust development environment for real-time applications.

"On the real-time side," he continues, "many of the CPU offerings—including the one from Ironics—don't run Sun/OS." Ironics' board, for example, is designed to run with VxWorks and pSOS+. In addition, it runs all the development tools that go along with VxWorks.



Omnibyte's MIPS R3000-based CPU has all the features of a full featured single-board computer. But the CPU is contained in two VME boards to take advantage of the additional P2 I/O space and to deliver additional power from the backplane to the second board.

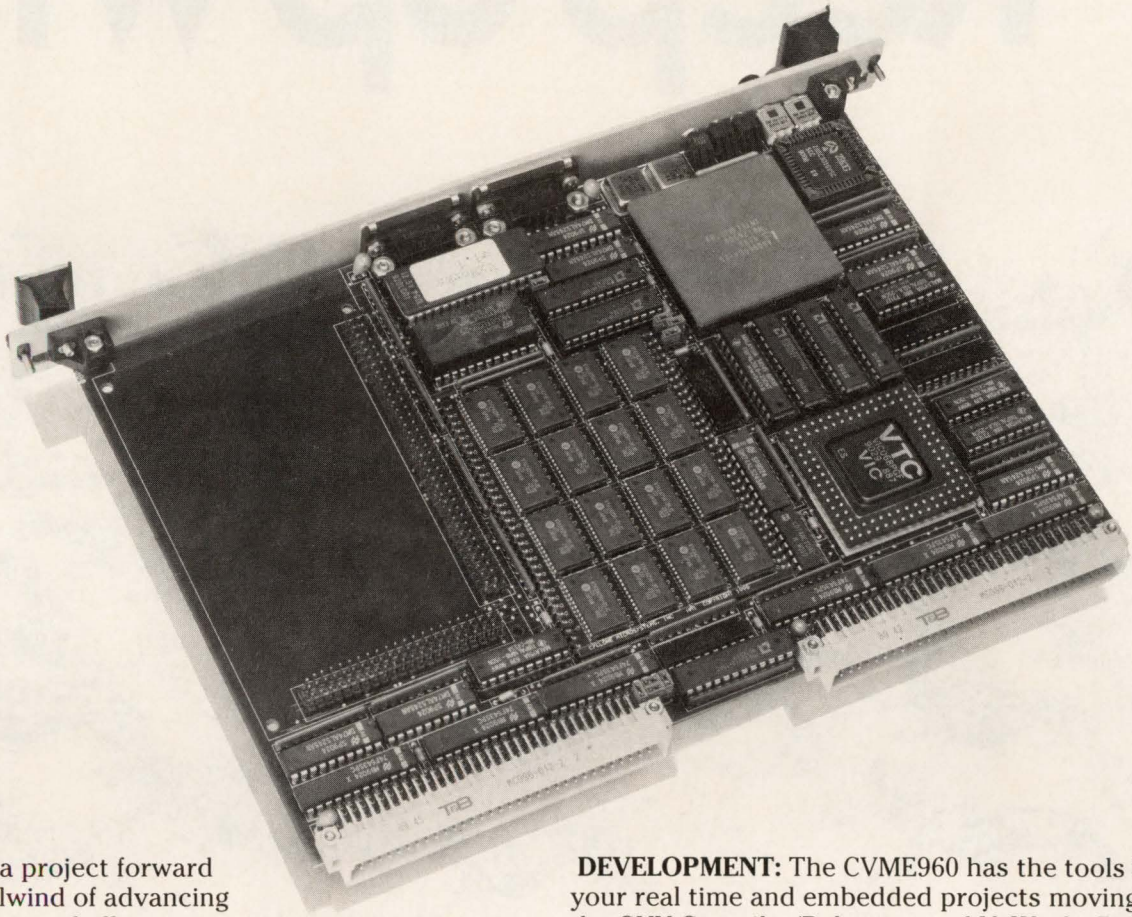
RISC CPU boards. First, and perhaps most important, developers of real-time kernels and operating systems completed versions for most of the popular RISC architectures.

Second, some popular RISC architectures have received widespread acceptance in the Unix environment. Sparc, with the backing of Sun Microsystems (Mountain View, CA), has spread as a number of Sparcstation clones have emerged. And the newly-formed ACE (Advanced Computing Environment) consortium representing some 42-odd makers of PCs, workstations, high-performance servers and superminicomputers has publicly rallied-round the MIPS architecture.

Finally, the makers of RISC chips have provided a wide range of chip types in different technologies with a number of options from low-power CMOS through high-performance bipolar and gallium arsenide. Differ-

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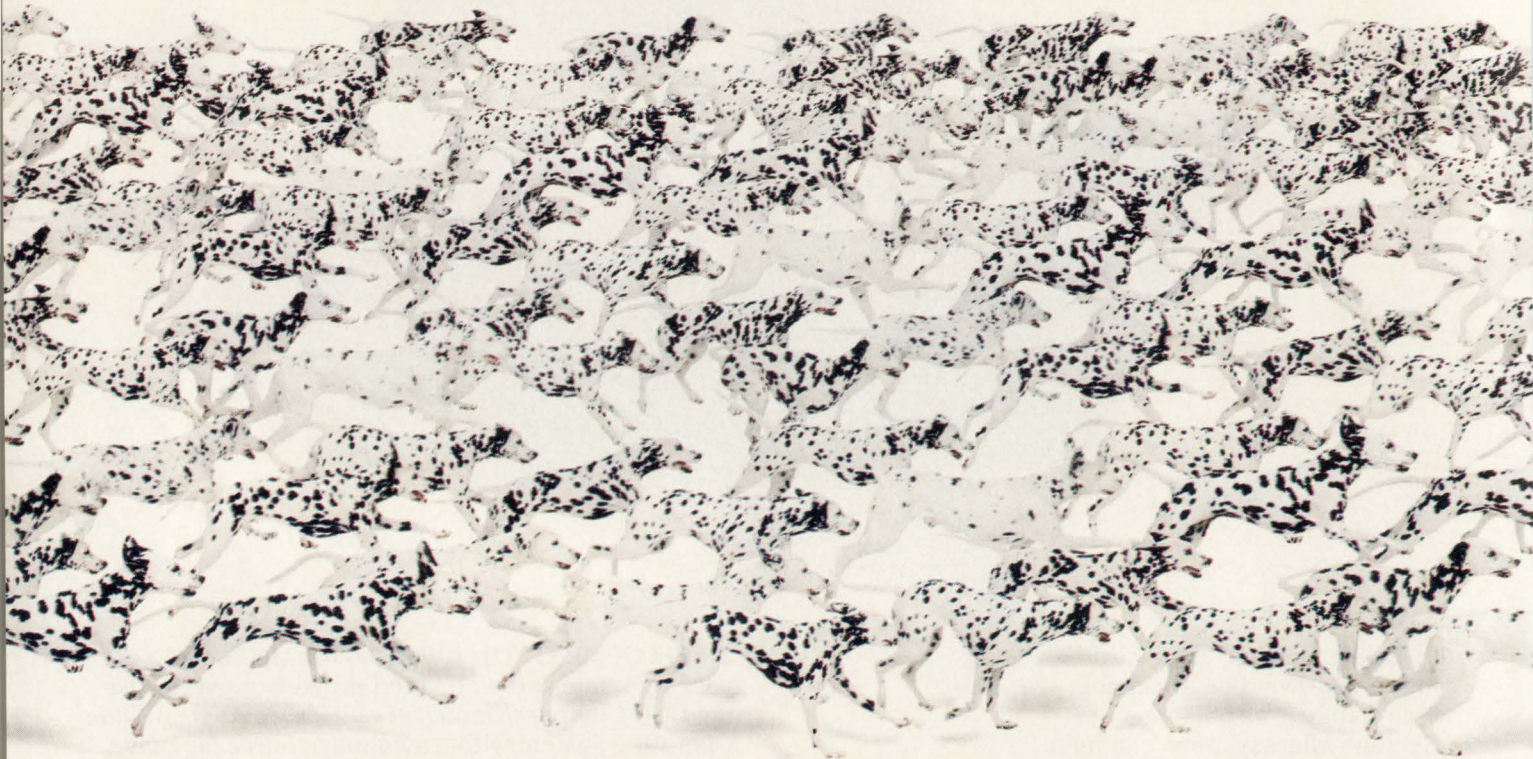
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■ RISC-BASED BOARDS

The advantage then is to have basically a Sun workstation tied to a VMEbus chassis—"You get all the advantages of VxWorks running on the host with Sun/OS and the advantages of VxWorks running on the target," says Schulman.

Similarly, pSOS+ will run on both environments with piece tools and development tools ported to that board. "So," he says, "We not only have a pSOS+ multiprocessing version, but we also have a complete tool kit called Caseworks RT from Multiprocessor Toolsmiths. There-

run 29000, i960 and 88000 boards as well as talk to Sparc boards.

An alternative is to use Sun's Sparcengine 2, which is essentially the "motherboard" of the Sparcstation 2. This approach offers advantages over the VME-based platform in that the connection between the VME chassis and the Sparcengine is via an SBus-to-VME adapter. A crash of the target system, therefore, doesn't put the designer back to square one—the buffer in the adapter saves the development work and operating system. When

Telecommunications companies, in particular, are often concerned with things such as fast integer processing and, therefore, the processor architecture can be a key element in the selection process," says Zackin. "But increasingly, developers are starting to look toward processor independence."

"You're getting to the point now where people are getting more attached to the real-time environment than to the processor architecture. But it's not as easy as simply swapping boards," cautions Zackin. "Depending on the application, there's always some degree of hard-wire changes, and often subtle coding changes, to make different boards work in different applications."

■ Get it your way

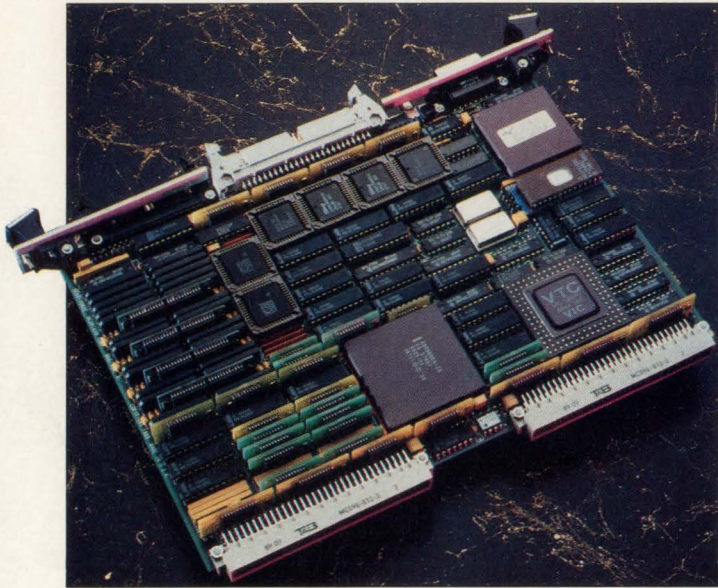
System developers are becoming increasingly critical in terms of what they want to get their job done. "Most of the applications we've run into call for very high-performance CPU engines oriented exclusively to real-time tasks," Zackin points out. These call for very fast integer processing with no MMU or floating-point capability. "We feel confident in the architectural approach we've taken—so much so that we're no longer offering our 030 product for new designs and have no plans for an 040 CPU," says Zackin.

Heurikon (Madison, WI) was probably first on the i960 bandwagon and also reports heavy interest from real-time developers.

Though Heurikon has not reversed the byte ordering of the Intel architecture on the board, marketing director Abe Hirsch says, "We know how to swap data on the bus because of our experience with Intel architectures—others have run into trouble with the i960 as well as the 80X86." Cyclone reverses byte ordering on its CPU board so it conforms with the Motorola Big Endian configuration. "The ACE has made byte ordering a lot less of an issue since it decided on a Little Endian configuration," adds Hirsch.

■ Price/performance

With any RISC discussion, the price/performance issue looms large. On one side, price sensitivities dictate certain limitations since the bulk of high-performance CPU business is in OEM products. On the other, performance is key to giving systems a competitive edge in their end-user markets. "We've bench-



Heurikon's HK80/V960E was one of the first CPU boards based on the i960CA, the superscalar RISC engine from Intel. "It provides between 80 to 90 percent the performance of comparable CISC boards," says Abe Hirsch, marketing director at Heurikon.

fore you get a complete set of graphical design tools that run on the Sun workstation for design work including a code generator that generates C code, an application-level simulator, a high-level debugger and a set of integration tools that puts them all together in terms of board initialization and other specialized requirements."

■ Implementation is important

The important thing, therefore, is not the Sparc chip, but rather its implementation. "But the real magic," Schulman goes on, "is that Sun's 1E board will plug directly into a VME chassis eliminating the need to play over Ethernet: the development and target environment reside in the same chassis." He says that Ironics plans to offer a new product called Galaxy 32 development/target platform comprising a 1E running Sun/OS and any one of the Ironics' real-time engines running on the backplane. Because it can run pSOS+, it can

Force releases its 2E board, that can also be an option instead of the Sun board.

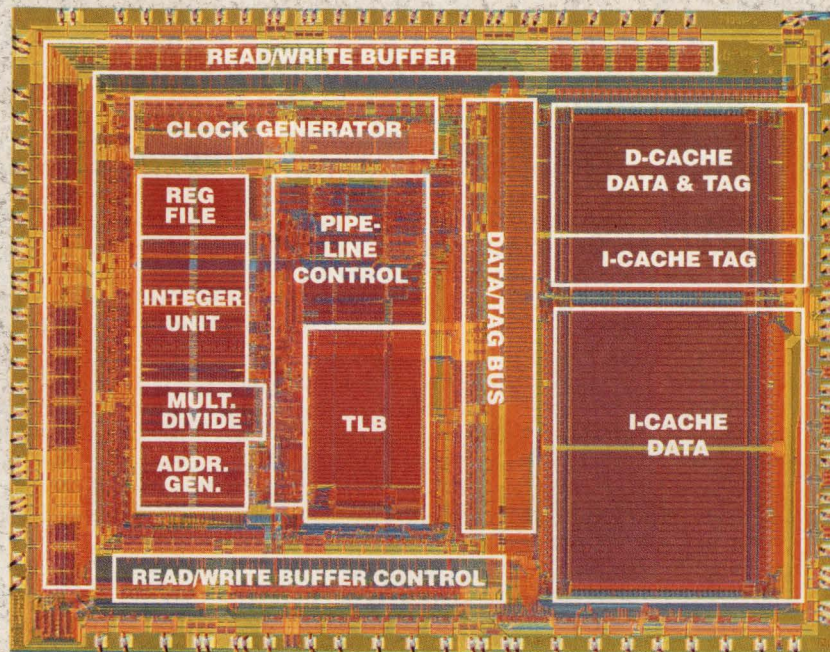
"But using a VME board as a host may not be the smartest thing," says Schulman. "Difficulties can arise because the Sun/OS is so tightly coupled to the target environment that it's difficult to separate the two for debugging purposes," he says. In addition, if the system crashes, valuable time is spent just to bring the Unix operating system back up again.

But Sparc is by far not the only RISC architecture in town though it's supported by Force, Ironics and Mizar (Carrollton, TX). Intel's i960, the MIPS family of processors and Motorola's 88000 are also in strong contention.

Cyclone's Zackin agrees largely with Schulman for many of the same reasons—the availability of both VxWorks, pSOS+ and development environments, except that Cyclone has focused on Intel's i960 processor.

"Some companies are particularly sensitive to architectural considera-

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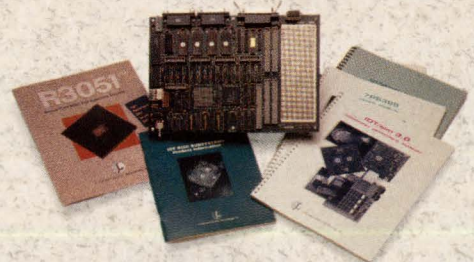
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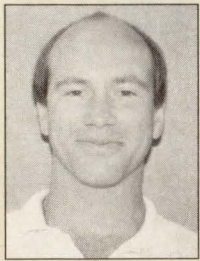
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The future of RISC microprocessors



The most popular RISC architectures today were developed in the late 1980s by companies like Sun Microsystems and MIPS Computer Systems. There are

two primary reasons behind the broad acceptance of these architectures. First, both companies realized that without direct access to leading-edge semiconductor processes and design tools, they couldn't advance their architectures alone. This led to the idea of licensing architectures to multiple semiconductor suppliers. Secondly, both companies—with the multiple source problem solved—further accelerated microprocessor user acceptance through an "open," as opposed to a proprietary, system approach. The fact that both were Unix-based chips sewed up MIPS' and Sparc's early adoption and success.

Much has happened since then. Using the MIPS architecture example, MIPS provides a fully-designed, full-custom data base to a total of five semiconductor partners (currently IDT, LSI Logic, NEC, Performance Semiconductor and Siemens). Each partner builds and brings to market a pin-compatible product. MIPS benefits because its architecture is more widely marketed, thus increasing its chances of becoming " pervasive."

Competition between these partners is intense since all start with the identical pin-compatible product. The R2000, R3000, R3000A and soon, the R4000 are all such examples. In this commodity-like world, only performance, price, quality and relationships are the differentiators between suppliers. These are all fleeting at best. As one would ex-

pect, all of the five partners are bringing (or will be soon) derivative products to market.

In the case of LSI Logic, it announced MIPS—derivative products that include high-performance processor modules, generic Unix-based workstation chip sets, and special-purpose RISC controllers. Typical application areas addressed are the workstation and embedded control markets. As an example of the latter, LSI Logic has introduced very cost competitive products (the LR33000 self-embedding processor) that are powerful, high-speed, general-purpose RISC controllers. Large instruction caches (up to 8-kbytes), data caches, single clock inputs, and high operating frequency (up to 40 MHz) are all part of this generation. Another feature is the integration of much of the system logic that's typically required by these types of systems. DRAM controllers, timer/counters, wait-state generators, write buffers, and a byte-wide PROM interface are all on-chip.

Future-generation products will contain more of the same. Logical blocks that will be integrated include floating-point, as well as higher-performance memory interfaces (e.g., direct support of interleaved DRAM systems). Larger cache sizes (16 kbytes and up) and higher clock speeds (50 MHz and above) will appear within the next 12 months.

Another path that will be followed are families that address the needs of high-volume "vertical" markets. Already some products that are touted to be laser-printer controllers have appeared on the scene. Specialized products that cater to other high-growth areas such as single-chip X-terminal controllers (see "X Windows terminals designers search for a single-processor solution," *Com-*

puter Design, Aug., p 77), data communication and military-aerospace. These will contain features that are tailor-made to these markets, and will be designed in conjunction with market leaders in each of these areas.

The trend toward specialization is key. There will, however, be smaller market niches, emerging growth opportunities and companies that wish to differentiate their products that may not choose to use these "single-chip" devices. These areas are best served by ASICs containing RISC microprocessor cores. Such a program will provide potential users the benefit of a standard instruction set (thereby preserving most, if not all, the software investment in compilers, assemblers, debuggers, etc.) while providing the ability to add proprietary capability and features not available from a standard, generic RISC controller. Today, RISC cores are small enough (20k-to-50k gates) to allow a great deal of customization using contemporary multiple 100K gate ASIC technology.

The one caveat pertinent to all these market-specific and ASIC versions is the potential for the silicon to be there before the tool base is ready. Great care will have to be taken to ensure the timely development of support tools for all new product initiatives arriving on the scene. The development of compilers, logic analyzers, hardware models, behavioral models and other third-party support will require close coordination between the semiconductor companies and tool vendors.

All this activity in the RISC marketplace by so many semiconductor vendors and their system partners is resulting in the world moving at a much quicker pace. Time-to-market, time-to-production and product differentiation will be the keys for success in the 1990s.

Rick Rasmussen, general manager, MIPS Division, LSI Logic

marked our i960 CPU versus many others in the market and demonstrated that it can consistently provide 80 to 90 percent of the performance of comparable CISC boards at one-half the price in real-time simulation and control applications," says Hirsch.

But performance measurement is difficult at best, and in many cases defies traditional wisdom. "Mips ratings have little importance in real-

time applications," says Hirsch. Zackin adds, "Around here, Mips stands for Mythical Indications of Performance. Each application is different, calling for a different set of metrics. Graphics processing, for example, is much different than running a small loop program," he adds.

Zackin continues, "The i960CA running at 30 MHz can actually perform the advertised 66 Mips. But that's when it's running a loop out of

its own internal cache. In real world applications—particularly in the real-time, real world—the best it can do—even using 35-ns SRAM—is about 30 Mips." More important than numerical Mips, adds Hirsch, are factors such as how much can be squeezed between interrupts, or how much context switching has to be done, and how fast it can be done, or what does the interrupt driver have to do before letting go of the processor.

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CIRCLE NO. 48

RISC-BASED BOARDS

Despite the blazingly fast performance of some of the newer processors with clock speeds now at 25 MHz, 33-MHz versions in the wings and even faster 50-MHz parts just behind, many designers still aren't satisfied. Array processors and some digital signal processors and specialized graphics processor boards offer multiple processors—CSPI (Billerica, MA), for example, offers a dual i860 board and Ariel (Highland Park, NJ) offers a VME board with four TMS320C40s—but there are only a handful of multiple-

Cyclone, for example, is working with a sophisticated real-time system designer looking to put as many as 1,000 processors in a system. The system is designed for very high-speed data-acquisition and processing. To increase processor density, Cyclone puts a second i960 on one of its small, mezzanine boards. In the high-speed data acquisition system, each VME rack has 19 dual-processor boards, and multiple racks are tied together.

Zackin is quick to point out, though, that Cyclone's i960 boards are used in

structure to accept any of the emerging number of Sparc Unimodules (MCMs) which will soon be offered by TI, Cypress Semiconductor, LSI Logic, Fujitsu, and others," says Schulman. He continues, "We're using the Cypress Sparc chip and by incorporating the Mbus and the 605 or equivalent cache MMU, multiple processors can easily be incorporated into a system either on a daughter board, or non-active (except for power and ground) companion board."

Motorola (Austin, TX) offers its MVME167 in flavors with one, two or four processors tied together on a single module Motorola calls a Hypermodule says Jerry Gipper, the company's VME board manager. "The 88000 is built with all the hooks necessary for tying multiple processors together," says Gipper. While it's possible to tie a pair of 040's together, it requires a significant amount of glue logic. "That's all inside the 88k," he says.

On the Unix side

While there's a great deal of activity on the real-time side of the fence, boards designed for both Unix and real-time applications—looking primarily like single-board computers rather than more conventional CPUs—continue to gain acceptance among designers. The leader is Sun with its 1E board. The 1E was first to define a new generation of high-performance, multifunction boards in the RISC area, much the way Motorola had done in the CISC arena with its MVME147. But while Sun defined compactness, performance and functionality, Motorola's Computer Group combined these with volume manufacturing technology, adding low cost to the equation.

The Sun 1E is a high-performance board capable of running Sun/OS and includes key features such as SCSI, Ethernet, parallel and serial ports, large memory, high-resolution clocks and multiprocessing hardware hooks such as special features for cache coherency, mailbox interrupts and read/modify/write operations.

Lockheed Sanders (Nashua, NH) took a similar approach with its MIPS R3000-based board offered in full military as well as commercial versions. Like the Sun board, Lockheed's CPU makes extensive use of ASICs—in fact, there are only a handful of parts in addition to the processor, memory and three large

THE RISC PROCESSOR SYSTEM BANDWAGON

LEAD HARDWARE COMPANY	88000 (RISC)	SPARC (RISC)	i960/i860 (RISC)	MIPS R- 3000/R-4000 (RISC)	HEWLETT PACKARD (RISC)	IBM (RISC)
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	UNISYS	TOSHIBA	ALLIANT	SILICON GRAPHICS	SAMSUNG	APPLE
	DATA GENERAL	FUJITSU/ICL	TANDEM	CDC		MOTOROLA
	SANYO-ICON	MATSUSHITA/ SOLBOURNE	TORQUE	BULL		
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	TWINHEAD					

RISC processors have begun an invasion of major systems companies. This chart shows significant affiliations of large systems companies with specific RISC architectures.

processor, general-purpose CPU boards.

In the CISC arena, Synergy Microsystems (Encinitas, CA) offers a dual 68040 board and Radstone (Montvale, NJ) a dual-processor 68040/020 board. But in the RISC area only Vista Controls (Valencia, CA) offers a dual processor (AMD 29000) board and it's designed for use in the fire control system of the Abrams A1 tank. But others have discovered clever ways to add processing power.

a wide variety of different systems from very large systems as that described above to multiple Ethernet and T1 wide area networks to a PC-sized box used in a color laser printer. Once again, he stresses, the combination of price and performance dictate design wins.

Still others are taking different approaches to offering multiple processors. Ironics points to the Sun-defined Mbus which lets it add multiple processors. "We've set up the bus



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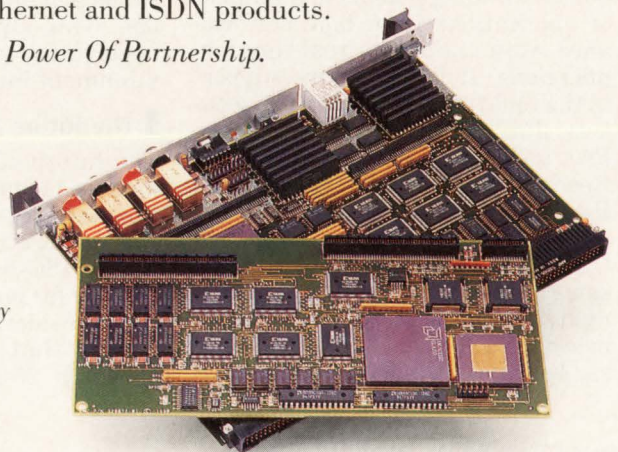
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CIRCLE NO. 49



■ RISC-BASED BOARDS

ASICs. And while Sun and Lockheed bring high levels of integration and performance to their boards, they both come down on the pricey side.

Omnibyte (West Chicago, IL) is also on the MIPS R3000 side of the fence with a second-generation R3000 board. "While we feel we were successful with our first generation," says planning director, Pete Czuchra, "we also gained a lot of experience which we were able to use in the second generation."

Like many of the other Unix/real-time RISC CPU offerings, Omnibyte's board, dubbed Pulsar, provides a variety of I/O including

The future of the CPU board business is faster boards with greater functionality and lower prices. For this generation, and perhaps the next, RISC-based designs will win the day for many applications.



Ethernet and SCSI as well as four serial and a real-time clock/calendar. But instead of providing the configuration on a single VME board, Omnibyte opted for a two-board version which provides a number of advantages. "First, the two boards provide a clean way to get I/O off to the P2 VME connector instead of from the front panel. Second, using two full slots, we can take advantage of the additional power and ground pins and not overload the single slot," says Czuchra.

Czuchra says that the company's board is finding a home in a number of applications from high-performance workstations to real-time applications. It has software support in the real-time arena from C Executive, JMI Software (Spring House, PA), to Wind River's VxWorks and Ready Systems' VRTX. In addition, the company offers an Ada compiler and MIPS' RISC/OS version of Unix. Czuchra is also singing out of the same price/performance hymnal as many of the other makers of RISC-based CPU boards. Omnibyte's Pulsar board in a 25-MHz version sells

in hundred quantities for under \$3,000 each—a price Czuchra says translates to about \$120/Mips.

Motorola's 88000 RISC family has gotten off to a relatively slow start. Early on, Motorola's computer group as well as Force, Eltec (Mainz, Germany) and a few other board makers jumped on the processor, but only to find a dearth of real-time support, and subsequently, customers. Force, for example, was one of the early adopters of the 88000, but switched over to the Sparc just over a year ago. "Motorola didn't offer the real-time support for the part that designers need," says Force vice-president of operations, Fred Rehhausser.

And true, Motorola has been slow in providing significant real-time support. Though some major announcements are expected before year-end, the chip is only supported by Lynx, Uniflex (a real-time to Unix bridge), and Motorola's own VME Exec. With Motorola's traditionally strong working relationship with Ready Systems and Software Components Group, it's expected both VRTX and pSOS+ will soon be announced for the 88000.

Other board makers that have stayed with the 88000 chip report brisk activity and are in eager expectation of new real-time support. At the present time, Gipper reports sales of Motorola's 187 board to be about 60 percent into Unix applications and 40 percent in real-time. In addition to applications in Motorola's own Multi-Personal Computer area, 88000 boards have been surfacing in medium-performance server products and a number of simulation products.

And Motorola's computer group itself has been through three iterations of its 88000 product before finally releasing its 187. The first two were multiple-board sets with hefty price tags. "The 187," Gipper says, "sells for only about \$2,500 in thousands and under \$4,000 for quantity one. This gives developers a good opportunity to get into the RISC environment inexpensively."

■ The future is faster

The future of the CPU board business is faster boards with greater functionality and lower prices. For this generation, and perhaps the next, RISC-based designs will win the day for many applications. Chip cost considerations alone help engender that decision. At current prices, a 25-MHz Motorola 68040

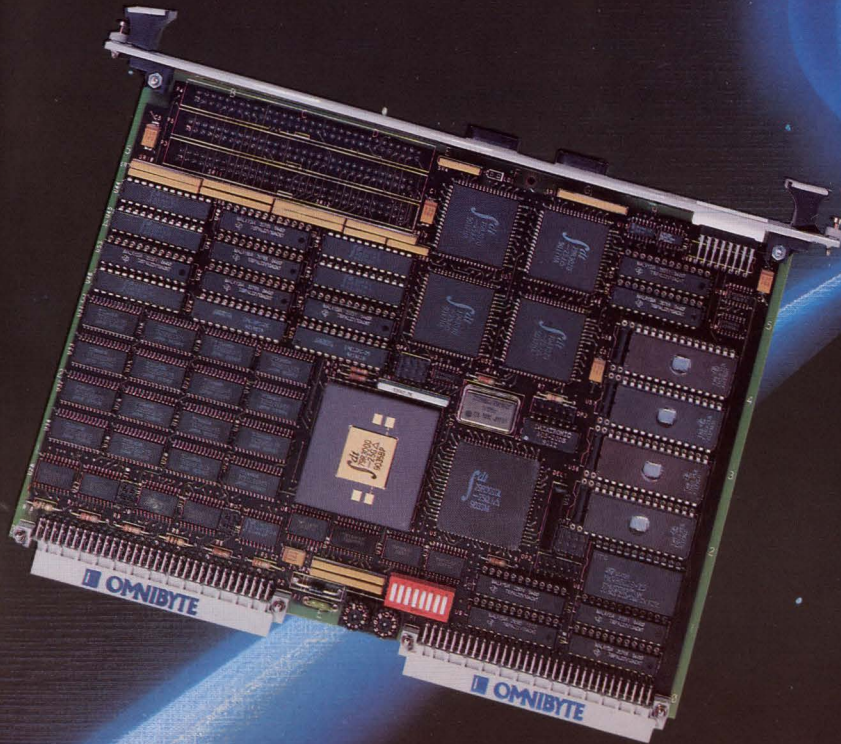
processor sells for somewhere in the \$750 price range in thousands compared with somewhere in the \$200 range for a MIPS R3000 of equivalent clock speed.

But microprocessor price alone won't be the determining factor. Processor speeds are increasing: 33-MHz clock speeds have arrived and before the year is out, 50-MHz parts may be here, possibly followed in a year by common 100-MHz parts. Whether CISC or RISC, these parts are going to call for increasingly speedy memory and peripheral components. And that translates to higher costs. The bottom line is that the board—and system—costs are going to be far more affected by memory content, memory architecture and peripheral components than processor alone. ■

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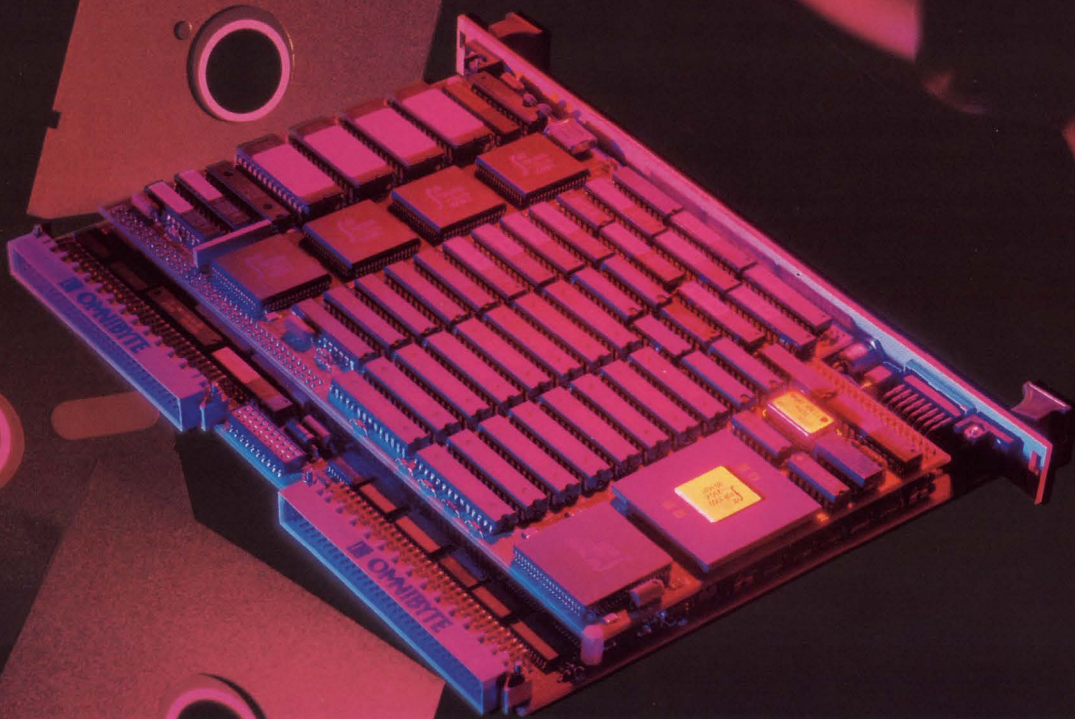
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Pinouts and performance drive PAL choices

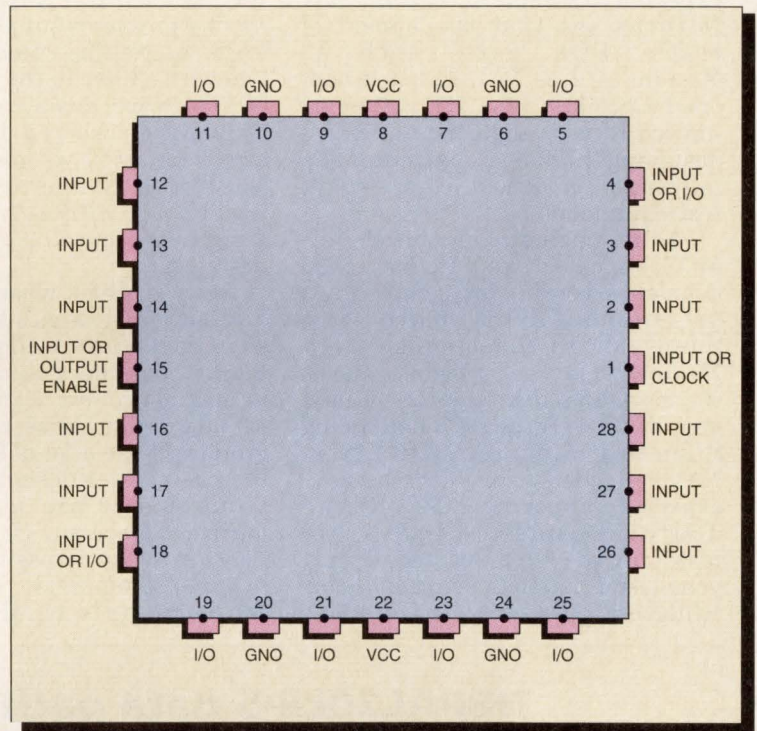
Though few 5-ns-and-faster PALs have been released to market, designers building prototypes around high-clock-rate processors are evaluating PAL contenders for pin-out and system performance.

Barbara Tuck
Senior Editor

Not much has happened with 5-ns-and-faster PAL products since focusing on that technology a year ago (see "High-speed PALs keep pace with today's processors," *Computer Design*, Oct. 1990, p 75). In fact, anticipated demands for the lightning-fast PALs have not materialized. Several factors are responsible for the reduced demand for the newest generation of high-speed PALs: one factor, no doubt, has been the downturn in the economy, specifically the slowdown in the PC market. Another factor has been that 40- to 60-MHz CISC and RISC microprocessors, which are pretty much driving the speed requirements for the 5-ns and faster PALs, are just now becoming available. The third, and perhaps the most interesting to ponder, is the ASIC factor. Can we expect the demand for high-speed PALs to ever be what it has been in the past, with ASICs themselves being faster and more affordable?

Standard package is the choice

With 5-ns-and-faster bipolar parts shipping from Texas Instruments (Houston, TX) and Advanced Micro Devices (Sunnyvale, CA), it's become clear that customers prefer the industry-standard pinout of the TI and AMD 5-ns PALs over the proprietary pinout of AMD's 4.5-ns parts. Now that National Semiconductor (Santa Clara, CA) has gone into production with its 5-ns bipolar PALs, also in an industry-standard pinout, designers have a third source from which to select high-speed PALs. And as designers qualify parts from TI, AMD and National, especially in the systems in which the parts will be operating, preferences are being formed for one vendor's PALs over another, whether it be for robustness of design or simply for a history of good experience with a certain vendor. In the meantime, an AMD/TI proposal for a new industry-standard package for faster-than-5-ns devices is going through the JEDEC approval process. At press time,



After going through the JEDEC approval process, this high-speed PLD pinout was agreed upon earlier this year as the standard for the next-generation of fast PLDs, expected to run at about 3.5 ns. The new pinout has ground and power pins interspersed among outputs to reduce ground bounce, minimize skew, and maximize speed.

■ HIGH-SPEED PALS

the announcement date for the compromise pinout hadn't been determined.

■ Two ECL PALs are MIA

But what about the blazingly fast ECL PALs from National and Cypress Semiconductor's subsidiary, Aspen Semiconductor (San Jose, CA)? And whatever happened to the 5-ns BiCMOS PALs that Philips/Signetics (Sunnyvale, CA) had expected to sample early this year? It turns out that the appeal of costly ECL parts such as National's 2-ns PAL hasn't broadened since last year. It's still being limited to very sophisticated users designing high-end machines like minisupers and, to a lesser extent, test equipment.

As for Signetics' promised BiCMOS, engineering efforts have been delayed, according to Signetics, by a production-facility move from Sunnyvale to Albuquerque, New Mexico. A revised schedule marks the second or third quarter of next year as the target date for sampling Signetics' 5-ns BiCMOS PALs. National, also a BiCMOS booster, expects to announce a BiCMOS industry-standard PLD part at 5 ns or faster in the first quarter of next year. And Lattice Semiconductor (Hillsboro, OR) is talking about 5-ns

PALs in pure CMOS but isn't offering a timetable for introduction.

From the relative numbers of users giving feedback on qualifying or designing in 5-ns PALs, it seems that getting to market early has been to TI's benefit. Dale Ray, design engineer at General Dynamics (Fort Worth, TX), ordered about 10 samples from TI when he needed a 25-MHz four-phase clock generator for a proprietary board. Though Ray had heard reports that TI was having problems supplying the fast PALs, as well as rumors of a problem with a knee in the output curve of TI's device, designers at General Dynamics received the samples they requested without delay and report that the 5-ns parts are working reliably within the system environments into which they've been designed.

Two years ago, when Ray's group at General Dynamics began the design series just being released to market, designers used 7.5-ns PALs in abundance. For General Dynamics' new design series, he expects the group will use a lot of 5-ns parts. In the case of Ray's design group, speed requirements are not driven so much by processor clock speeds as they are by the necessity to interface to other computers. "Our systems can handle up to 25-MHz bus cycles,

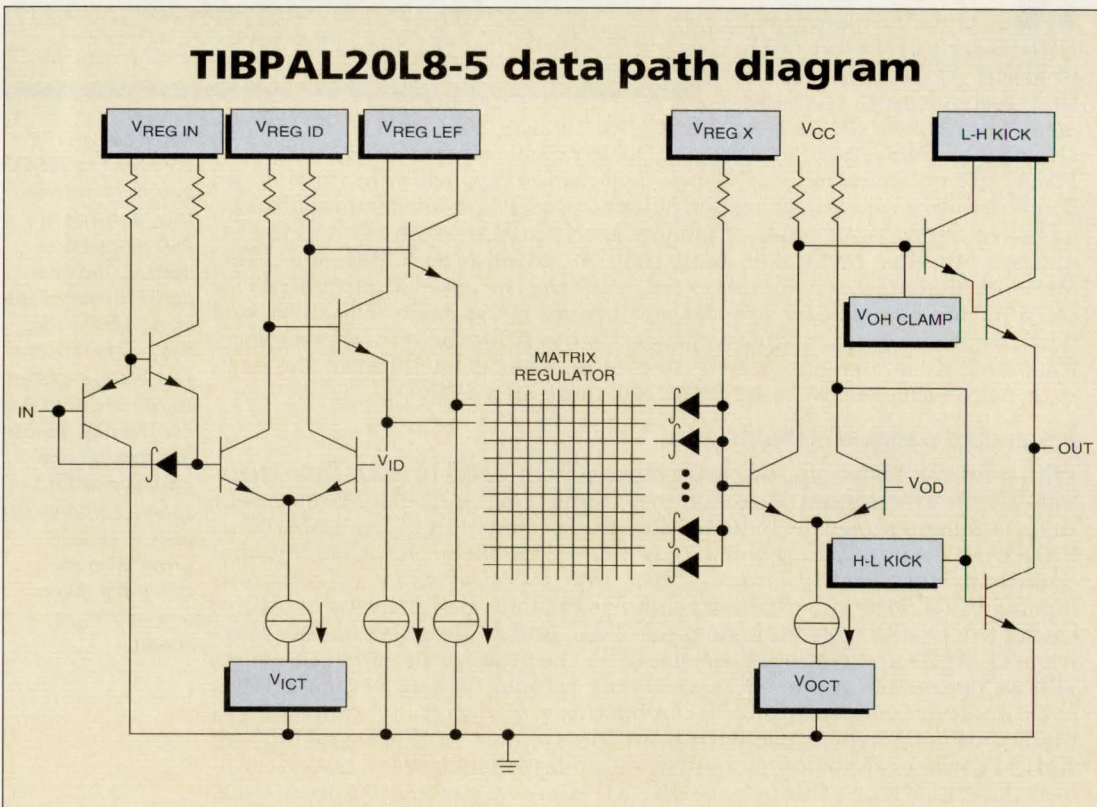
but by the time we do address comparisons and so on, 7.5 ns is right on the edge of getting the job done," he explains.

Mike Tubbs, design engineer at Compaq (Houston, TX), reports being forced to use 5-ns PALs to support cache memory and thus maintain system clock speed in a proprietary product about to go into production. Tubbs had also heard that TI was having some problems early on with its 5-ns parts, but Compaq found no glitches in the PALs' operation.

A product engineer qualifying PALs at another major computer vendor comments, "The 5-ns targets are achievable. The processes have been refined enough so that they will be reliable." As for setbacks that TI and AMD are both reported to have had somewhere along the 5-ns PAL internal-development curve, "a vendor pursuing such an aggressive product can't be expected to invent on schedule."

■ System tests significant

"Any vendor's 5-ns PALs, when run through traditional qualifications, will do well," says Christopher Lindstrom, supply quality engineer at NCR (Columbia, SC). "But put them in systems, and it's a different story," he says. Lindstrom has qual-



In designing its 5-ns PAL, TI minimized the effects of system-level noise on the workings of the TIBPAL20L8-5 by powering it from internally regulated supplies that remain invariant over large swings in temperature and V_{CC} and by using ECL-type circuit techniques. The voltage swing on the input emitter followers of TI's 5-ns PAL is determined by the input differential supply voltage ($V_{REG ID}$) on the high end, and the input current-tail voltage (V_{ICT}) on the low end. The swing can be adjusted by tailoring these local regulators.

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CIRCLE NO. 50

■ HIGH-SPEED PALs

ified the TI, AMD and National 5-ns bipolar PALs for NCR and leans toward the new devices from National. According to him, National is the only vendor to have addressed an undershoot problem in the high-speed PALs. "With built-in safeguards for system problems, National has a much more robust design," says Lindstrom.

So far, NCR has designed in TI's 5-ns PALs and is following up with AMD and National parts. Three or four of the high-speed PALs are going onto a 50-MHz processor

for going to production with R4 and R6 devices. "As we release those parts," says Lange, "they'll be up for sale, and users will have them within six weeks or less."

TI did separate designs for the four 5-ns PAL lead options "to extract the best possible output conditions," explains Lange. The design criteria TI adopted were aimed at faster devices and cleaner edges. "Users can't afford to design around a feature in a PAL that's not clean and predictable," says Lange. As for noise immunity, Lange says that

only fast enough to cycle an address, according to DEC, but it also eliminates parts and gates, thus reducing the number of components on a subsystem.

AMD is tempering its disappointment at not being able to deliver its proprietary 4.5-ns pinout to a broader market by devoting its efforts to pushing an industry-standard package for parts faster than 4.5 and 5 ns through the JEDEC approval process. "The new package doesn't have the same pinout as the 4.5-ns PAL but adopts the same philosophy as far as having more ground pins distributed among I/Os," says Robin. His best guess is that the next-generation PAL will be a 3.75-ns or 3.5-ns device.

■ More bipolar and then BiCMOS

After sampling for awhile, National recently went into production with its 5-ns bipolar PALs. The market demand has been slow but is picking up as customers build prototypes of 80386- and 80486-based PCs, says Jay Kamdar, director of marketing for programmable products. National has established a leadership position in ECL PALs, is now competing in 5-ns bipolar PALs, and with the introduction of a 5-ns-or-faster industry-standard PLD in BiCMOS early next year, hopes to establish market leadership. "Commitments to ECL are hard to come by," reports Kamdar. National's strategy for its 5-ns bipolar latecomer has been to design it more robustly than TI's or AMD's 5-ns parts. As for BiCMOS, National wouldn't divulge the specific part to be implemented or its exact speed—just that it's targeted at performance-critical applications. "It will offer the highest performance the industry has seen yet," predicts Kamdar.

In the meantime, Signetics has seen silicon on its much-delayed BiCMOS PALs and hopes to sample them in the second or third quarter of 1992. "Though Signetics will be slightly late to market with 5-ns PALs, we have a tighter distribution to 5 ns at a time when other makers are having difficulty shipping 5-ns devices reliably," says Paul Sasaki, Signetics strategic marketing manager for PLDs. The industry is at the edge with TTL, says Sasaki. National is counting on BiCMOS to be faster as well as to deliver a constant supply with good yield.

While Signetics and National are

GROUND BOUNCE TEST RESULTS

DEVICE TYPE	LOADING CONDITIONS	# OF OUTPUTS SWITCHED SIMULTANEOUSLY RESULTANT GROUND BOUNCE LEVEL (V)						
		1	2	3	4	5	6	7
GAL 16V8-7	CAP ONLY 50pF	.35	.45	.60	.75	.90	1.10	1.40
AMD's Bipolar 16L8-7	CAP ONLY 50 pF	.20	.30	.40	.60	.75	.90	1.10

This table from Lattice gives comparative ground-bounce figures for a Lattice 7.5-ns pure CMOS GAL16V8-7 and a bipolar 16L8-7 PAL. Both devices were tested with a 50-pF capacitive load at the device using a HP 54111D digital oscilloscope.

board, implemented as part of NCR's strategy for building seven levels of computing power, from notebook computers to powerful parallel-processing machines. For applications problems with the 5-ns devices, Lindstrom reports having found a problem when TI's part is subjected to a floating input. According to him, TI is examining that problem now.

■ Call TI hotline

At TI, PLD strategic marketing manager Jon Lange encourages designers encountering applications difficulties with TI parts to pick up the TI hotline. As for the rumored knee in the output curve of TI's 5-ns device, "We don't have a knee in any of our output circuits. As part of the breadboarding process, we did see a problem internally with early engineering units, but they were samples," says Lange.

As for vagueries related to supplying the L8 and R8 in 16- and 20-pin packages, Lange says that TI is in a position to deliver as many parts as users ask for. TI hit its internal schedule for introducing the L8 and R8, according to Lange, but didn't begin shipping as early in the second quarter as some users expected. The first week of this month is TI's target

TI's design innovations make its 5-ns PALs "very quiet and very true under all conditions. There's no chance of false switching."

■ Demand picking up

Lange says that TI has been somewhat surprised at the slow demand for high-speed PALs. "We were assuming production demand, but it hasn't materialized for the 5-ns devices." The demand has just recently picked up, according to Lange, as higher-speed versions of the 80386 and 80486 become available to users in volume.

Most of AMD's orders for a few hundred thousand 4.5- and 5-ns PALs have come in recently, says Andy Robin, director of PLD marketing at AMD. "Far and away, the demand is for the 5-ns part," says Robin. "We have a good following for the 4.5-ns part from sophisticated users, with more design wins every week. But we expect the majority of parts shipped to be 5-ns." Digital Equipment Corp (Maynard, MA) is using AMD's 4.5-ns PAL to boost speed in a cache address controller. DEC reports that before the 4.5-ns devices were available, PLDs couldn't be used in cache-controller applications. But AMD's part is not

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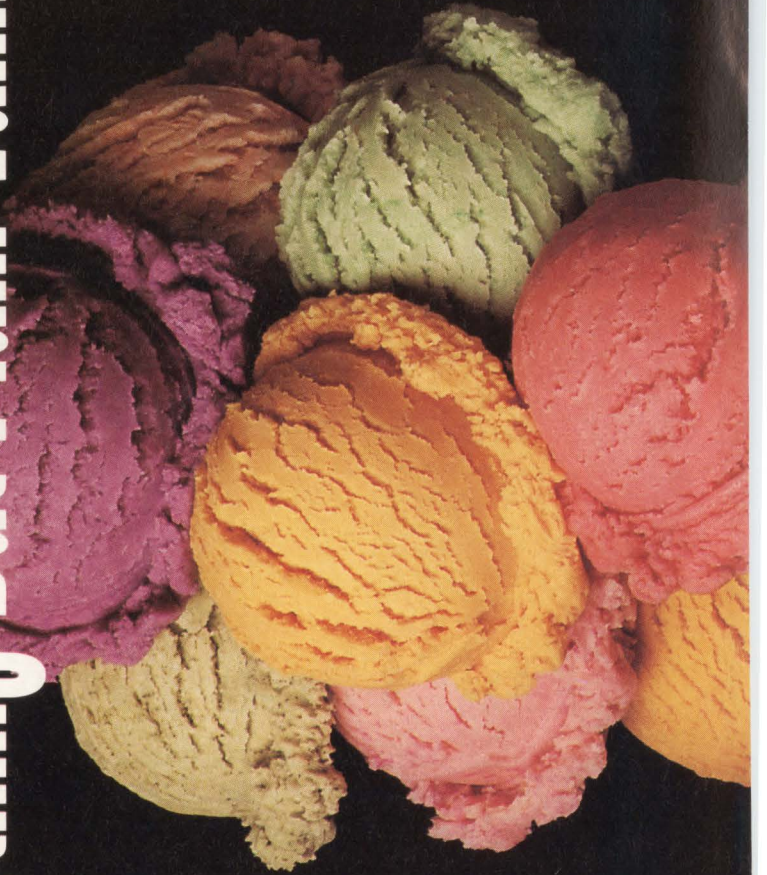


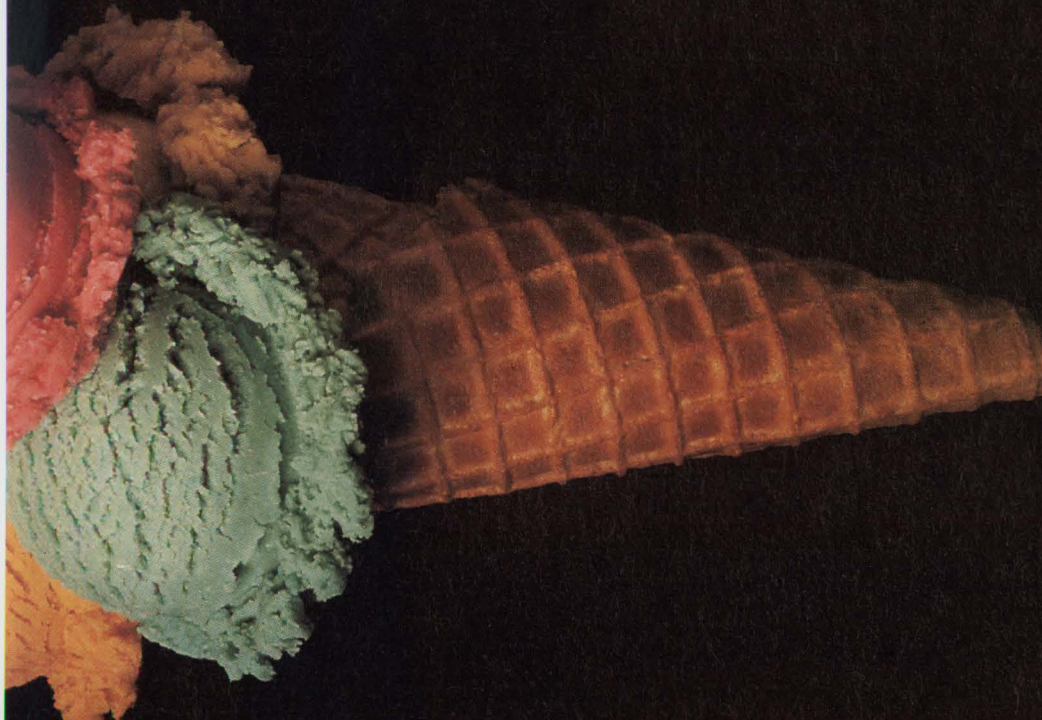
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Compensating for output undershoot

If output undershoot excursions caused by purely capacitive loads are large enough in magnitude and duration, they can affect the access times of high-speed PALs by many times their specification limits. The figure (upper right), showing a comparison of National's bipolar 5-ns PAL output characteristics with and without undershoot compensation, illustrates how a 150-pF load on all outputs can affect access time by dynamically altering the input threshold characteristics of the output buffer.

When an output high-to-low transition occurs, outputs undershoot below both system ground and the PAL's internal ground. With a large and purely capacitive output load, there's no current supplied to the load to pull it back above ground except what's delivered to the output driver internally (usually about a 1.5-K Ω equivalent resistance). That equivalent resistance, multiplied by the 150-pF load capacitance, creates a 200-ns-or-greater time constant.

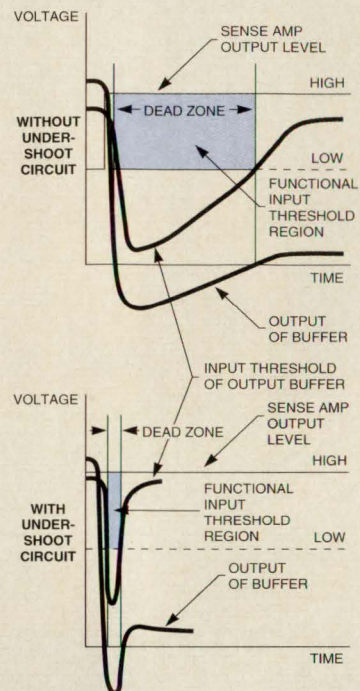
During the dead zone, or the time period the output is below ground, the input to the output buffer is pulled to a voltage lower than its normal operating range through the output driver's clamp diode. As a result, the output will effectively stay low since any subsequent edge arriving at the input of the buffer will not be recognized.

To reduce the output undershoot and its dependence on the load, National has added the simple circuit shown in the figure (lower right) to the output buffer. The comparator in the circuit senses the difference between the output driver's collector and emitter voltages. When the collector voltage falls below the emitter voltage as the output undershoots, the comparator delivers a predefined voltage to the base of the

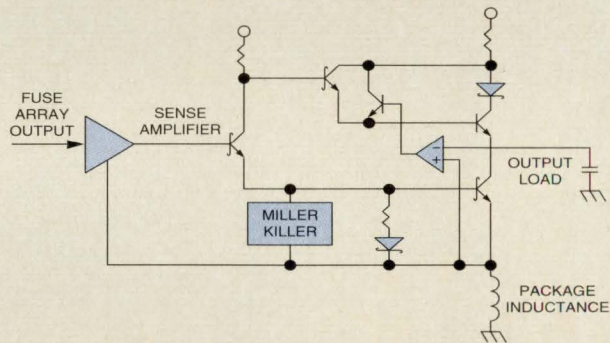
output pullup driver, thereby delivering I_{OS} current directly to the load capacitance and reducing the time constant of the dead zone to 6.75 ns (an equivalent resistance of about 45 Ω). This significantly reduces the window of time during which the next edge can be affected as well as the magnitude of that effect, according to National.

Measured data on National's 5-ns bipolar PAL, loaded with 150 pF, all outputs switching, and without undershoot compensation, shows a 25-ns access-time increase. Under the same conditions, with undershoot compensation, National says that access increase is reduced to less than 2 ns. National says the relative simplicity of the undershoot compensation circuit results in an additional current per output of only 150 μ A and less than 1 percent area increase to the output buffer.

Output buffer characteristics



Output buffer with undershoot compensation



counting on BiCMOS to give them market leadership, Lattice Semiconductor is planning to shrink its EECMOS technology down to 0.6 μ m (effective) from 0.75 μ m and apply this technology to the 16V8, now at 7 ns, to yield a 5-ns pure CMOS part. Lattice isn't ready to pin itself down to an introduction date, says Steve Donovan, Lattice's director of marketing. "I can't say it will happen in '92, and the 16V8 may not, in the end, be top priority. But Lattice is developing the technology for a 5-ns pure CMOS PAL

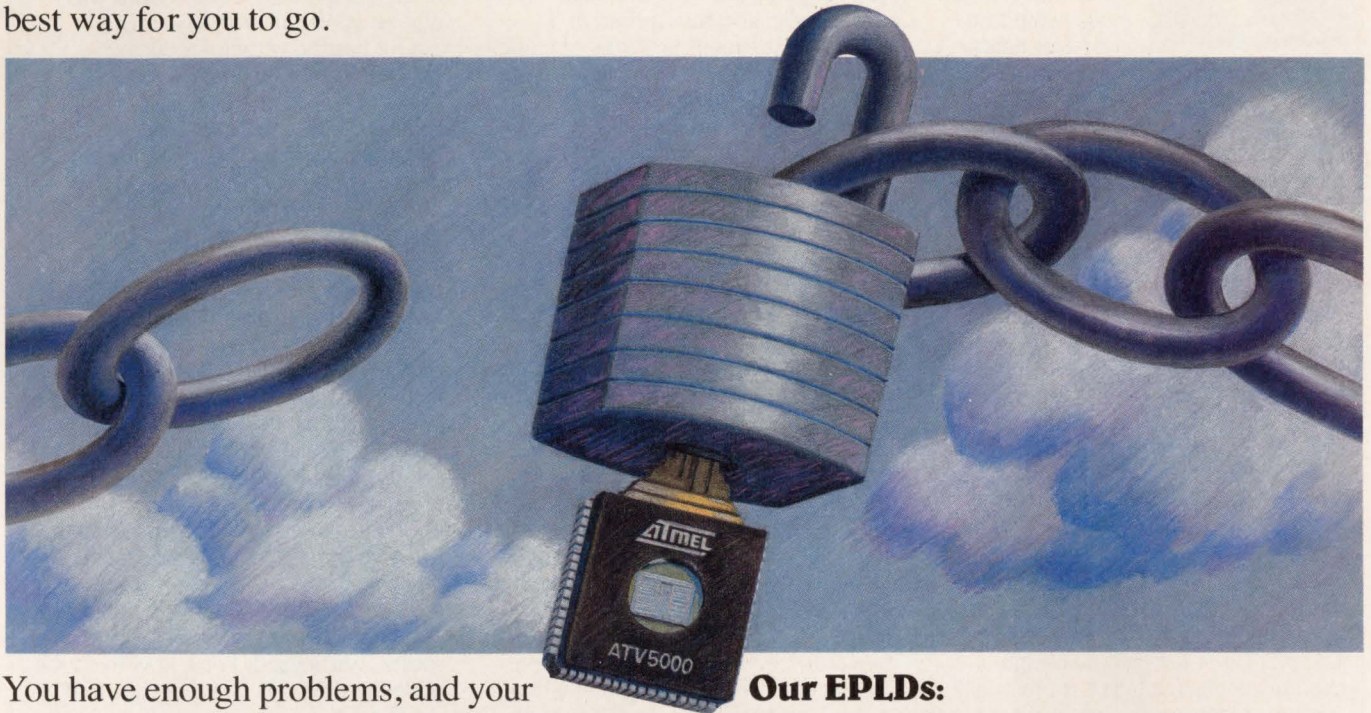
that will give faster edge rates than bipolar and BiCMOS as well as enhanced system-level performance." Donovan says that Lattice's target goal is to provide lower power than bipolar or BiCMOS in a standard package. The reprogrammability of Lattice's EECMOS technology also makes it attractive. Bipolar and BiCMOS are usually one-time programmable.

When questioned as to interest in 5-ns pure CMOS PALs, users tend to be negative, based on a belief that ground bounce for a pure CMOS 5-

ns device could get dangerously close to the threshold, causing some inadvertent switching. But Jock Tomlinson, field applications manager at Lattice, points to a comparison between the 7.5-ns Lattice GAL16V8B-7 and an AMD bipolar 16L8-7.5 PAL. "Both the AMD bipolar PAL and the Lattice GAL devices were tested with a 50-pF capacitive load at the device under test using the HP 5411D digital oscilloscope. The bipolar device had a resultant ground bounce of 1.1 V_{dc} compared to 1.4 V_{dc} for the Lattice

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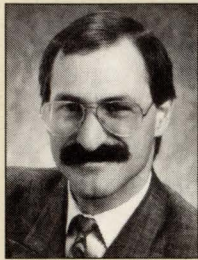
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New pinout standard embraced for faster-than-5-ns PALs



Keeping customers happy often requires faster and faster hardware. Keeping competitive often requires being first to market with faster and faster hardware. Microprocessors keep getting faster and have increasingly become central to delivering faster hardware. Over the last decade, CISC processors have gone from 8 bits at 4 MHz to products such as the 32-bit Am386 at 40 MHz. RISC processors are even faster, with the Am29000 and others delivering 40 to 60 MHz and more.

Being the firstest with the mostest isn't easy: even though many have the same microprocessors available to them, not everybody can be first to market with a hot new box. Especially when design errors occur and marketing people change the product definition at the last minute.

But being first with the most is key, so the pressure to reduce design cycles is enormous. And that pressure is what has fueled the terrific surge of the fastest growing segment of the logic market: PLD's. The last-minute design change capability of PLDs is practically legend—many are the engineers whose

projects have been saved by an edit to their PAL device codes.

Another nice virtue of PLDs is that they've gotten faster just when we need them. In fact, they have delivered a new burst of speed more frequently and faithfully than any other form of digital logic, and thus arrived at 5-ns/117-MHz speeds, an order of magnitude improved from their initial versions of 13 years ago. In fact, PAL devices are now the fastest form of TTL-compatible logic. Now, aside from being a great partner for fast microprocessors, PLDs are a simple and powerful tool kit for fixing critical-path timing problems.

There are some gotchas, though. If a collection of ultra high-speed parts are used to make an ultra high-speed board, it won't tolerate the loose design techniques that worked just a year or two ago. Ground bounce, ringing, reflections, excessive overshoot and undershoot, glitching, unaddressed electromagnetic interference and radio frequency interference issues, unconsidered transmission line effects, and other hazards await the designer who sticks to yesterday's long traces, unterminated lines, and generally cavalier approach. More than ever before, minimums can bite and skews can steal a board's performance potential. Fighting to wring out nanoseconds or even picoseconds

takes first-rate engineering.

Members of the JEDEC PLD committee decided that if PLDs were to continue to get faster, which they are, perhaps something should be done to make them easier to use. So a new, high-speed PLD pinout standard was agreed upon earlier this year. This pinout has the virtue of reducing ground bounce by interspersing grounds among the device's outputs. Likewise, putting power pins among the outputs maximizes the speed that the device can deliver. The power and ground scheme minimizes skew. And, finally, the power and ground distribution among the outputs may save a designer or two from creating crosstalk problems because of their board layouts.

So as PLDs move along to the break-neck rate of about 3 ns/135 MHz, a new pinout will make board designers' challenges surmountable. And AMD will ship an eighth generation of PLD speed into performance-hungry sockets throughout the world.

One last question is left. It seems almost a given that system performance and time-to-market will continue to be key. As microprocessor speeds continue to climb and PLDs get to 2-ns/175-MHz speeds, will anybody know how to do the good 80+MHz TTL board designs that use them?

Andy Robin, director of PLD marketing, Advanced Micro Devices

GAL device." When asked about a crossover point from CMOS to bipolar with regard to I_{cc} vs frequency, Tomlinson observes that at no point in the operation of the Lattice GAL16V8B-7 device does it come close to the bipolar 7.5-ns device. "The bipolar 7.5-ns device is specified at 210 mA I_{sb} (static) whereas at 25 MHz, 5.25 V_{dc} , the Lattice device is specified at $I_{cc}=115$ mA max. At 100 MHz, I_{cc} for the GAL16V8B will approach 117 mA max, but that's a long way from the bipolar's 210 mA," Tomlinson points out.

Tony Chatzigiannis, member of the technical staff at Silicon Graphics (Mountain View, CA), has tried Lattice's 7.5-ns GALs but hasn't tested them extensively. He would, though, be interested in 5-ns pure CMOS devices from Lattice because the

EECMOS parts are "very programmable—you don't have to waste the parts." Although Chatzigiannis didn't have data available on ground bounce figures for the 7.5-ns parts, he reports that, "We've had no problems with the CMOS GALs, even though we've really pushed the parts, with a lot of outputs switching at the same time."

Chatzigiannis is currently designing 5-ns PALs from AMD and TI into video graphics boards for Silicon Graphics' main graphics systems. Though system clocks on the boards aren't necessarily very fast, designers require tight timing for clock multiplexing. "We're playing games with system clocks and can't tolerate delays going through the clocks," notes Chatzigiannis. "We're using PALs to select clocks." Though Silicon Graphics is mixing AMD and

TI parts in its new system, Chatzigiannis tends to prefer AMD to TI. "I've never had a bad experience with AMD," he says.

With so few 5-ns-and-faster applications having been released to market, it seems doubtful that demand for high-speed PALs will ever again match the volumes of past-generation devices. Since ASICs have gone down in price and up in speed and density, they've gained in appeal. Not to mention FPGAs, which have taken over as the darlings of the industry. NCR's Christopher Lindstrom observes that at one time NCR would have put up to 50 PALs on a board, but now designers will use somewhere between three and 15. "ASICs are so much more affordable," Lindstrom says. "And what you can't do in ASICs, you can do in super PLDs

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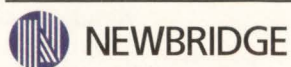
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■ HIGH-SPEED PALs

such as faster MACHs or low-gate-count, high-speed FPGAs." NCR is pushing the envelope of technology, notes Lindstrom, and will do as many as four or five passes of a board.

Compaq's Tubbs reports that while three designs in progress today at Compaq use 5-ns PALs, at least two of them will be moving to ASIC implementations. A cost-re-

duction group at Compaq does ASIC-based board revisions after products go to market.

■ PALs still needed

Nevertheless, the demand for PALs will always be with us. It's just the volume of that demand that's in question. There will be fewer PALs in the future, predicts Gary Gostin, senior system architect at Convex

Computer (Richardson, TX). "We're trying to put as much into ASICs as we can, but there will always be a need for glue logic." Convex is one of the small number of customers for National's 2- and 4-ns ECL PALs. The high-speed, high-cost ECL devices have been designed into the recently announced Convex C3800 supercomputer family, which run at 16 ns. "We needed something that was fast enough to go from one gate array through a PAL into another gate array in one clock cycle. We tried to pull as much as possible onto Vitesse GaAs gate arrays, but we still needed glue logic," says Gostin.

Semiconductor vendors, too, are seeing a shift away from PALs. TI's Lange says that PALs are no longer the logic people design around—now it's ASICs. "Customers will use



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With so few 5-ns-and-faster applications released to market, it seems doubtful that market demand for high-speed PALs will ever again match the volumes of past-generation devices.



PALs when they come up against a market window. A PAL will be the last thing in there to accomplish a design goal, to make up for speed lacking in other components. We call it 'oops logic'," says Lange.

And what does the future hold for PALs? Where will silicon technology go after 2-ns ECL PALs, 4.5- and 5-ns bipolar, 5-ns or faster BiCMOS and 5-ns pure CMOS? Will TTL continue as the standard as we go to even higher frequencies, or will the industry adopt a lower-voltage standard?

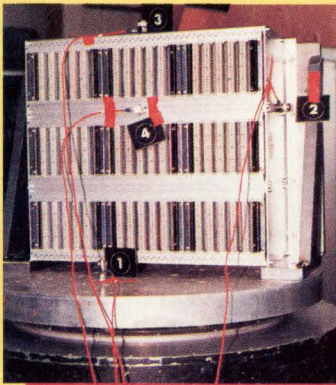
Feedback from users and vendors on these issues isn't definitive. "We're pretty much at the end of the road for 5-V PALs," says Signetics' Sasaki. "It may happen that we'll go to a lower voltage. The JEDEC committee is looking at a low-voltage standard, at about 3 V."

General Dynamics' Ray doesn't foresee his company designing with 3-V PALs, "unless a lot of logic is

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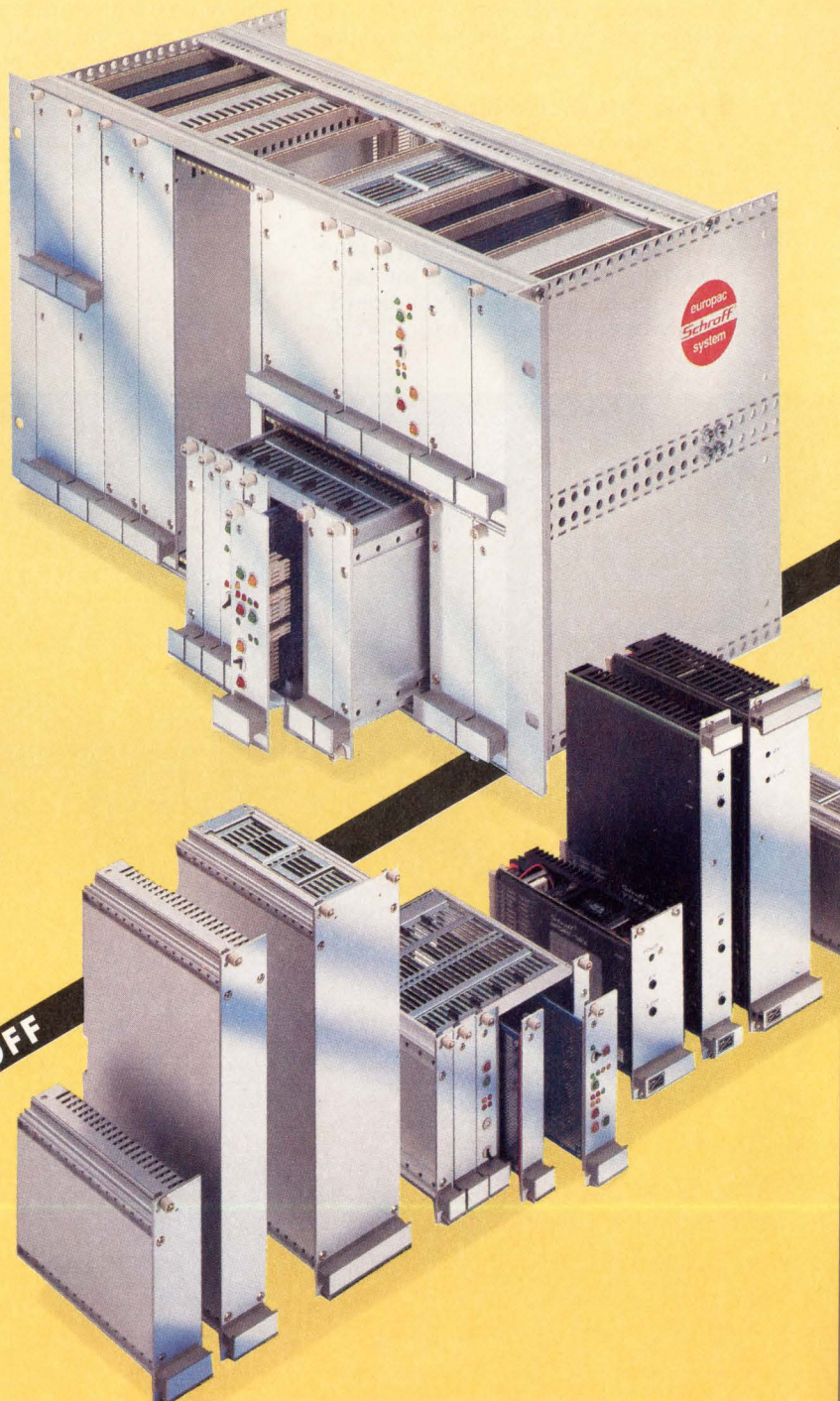
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■ HIGH-SPEED PALs

done in a 3-V standard. The functionality of 3-V stuff is limited. All of our interfacing is set up at TTL levels." Compaq's Tubbs, on the other hand, thinks it will be necessary for high-speed processors, as well as parts to go along with them, to go to smaller voltage swings before noise problems become tremendous. And Lattice's Donovan says that, as designers go up to higher frequencies and down to lower power, they're going to have to reduce the range they're swinging over.

■ How fast should it go?

As for the next generation of PALs, Donovan says that the benefit beyond 5 ns becomes questionable. "You'd have a very fast propagation delay through the IC, but then massive delays going through the package and the package to the board." Donovan suggests, instead, that de-

signers go to a higher level of integration to eliminate on-chip, off-chip, and chip-to-board delays.

If complex PLDs, FPGAs, and ASICs will give users the levels of speed they require for the systems they're designing at affordable prices, it's likely that we'll no longer see high-speed PALs being sold in tremendous volumes. Though the need for glue logic, or last-minute "oops logic," may always be with us, it may be a bit of an academic exercise to plan on solutions more elaborate than the 5-ns and faster PALs we already have. They themselves have not yet met with widespread market acceptance. ■

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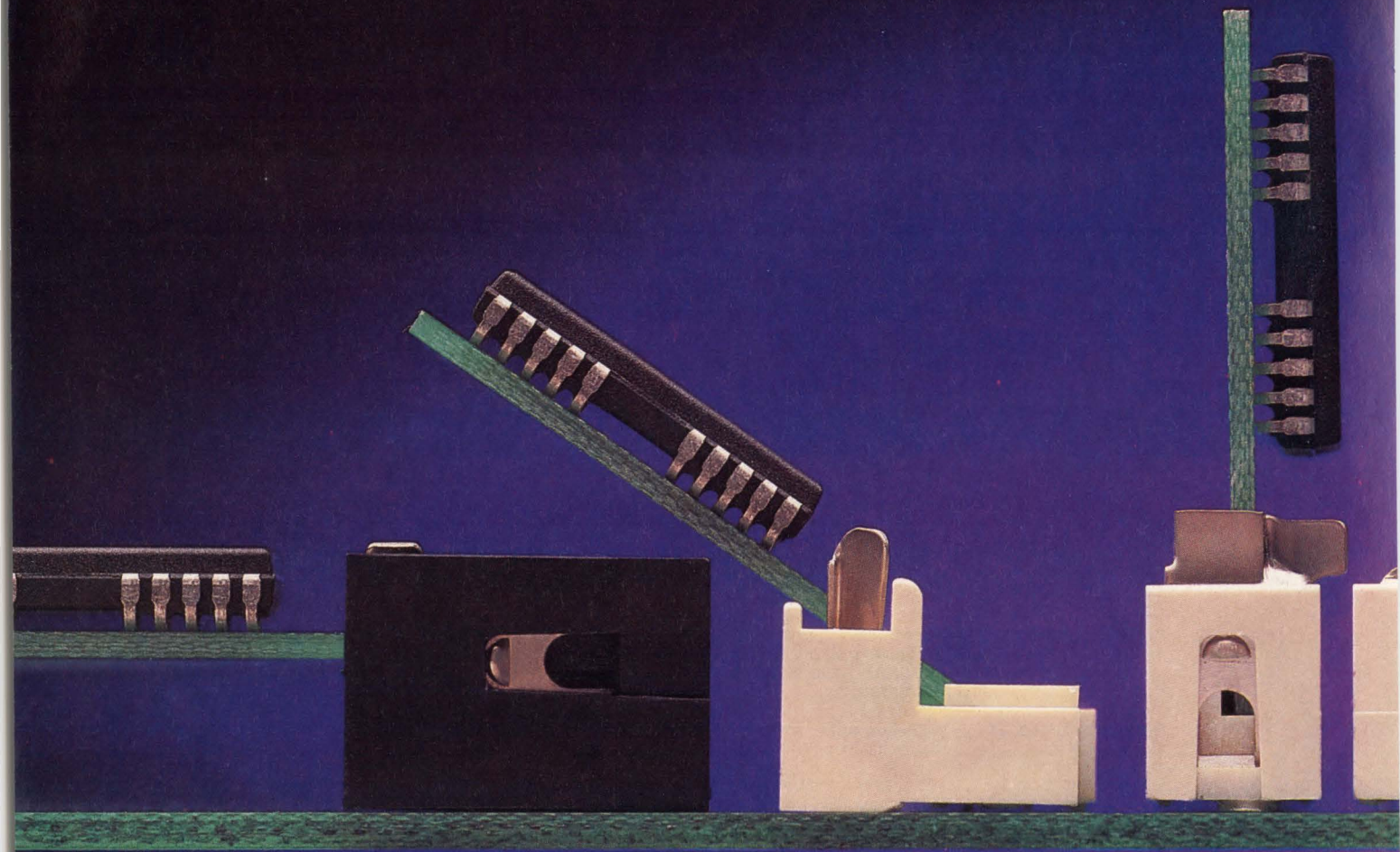
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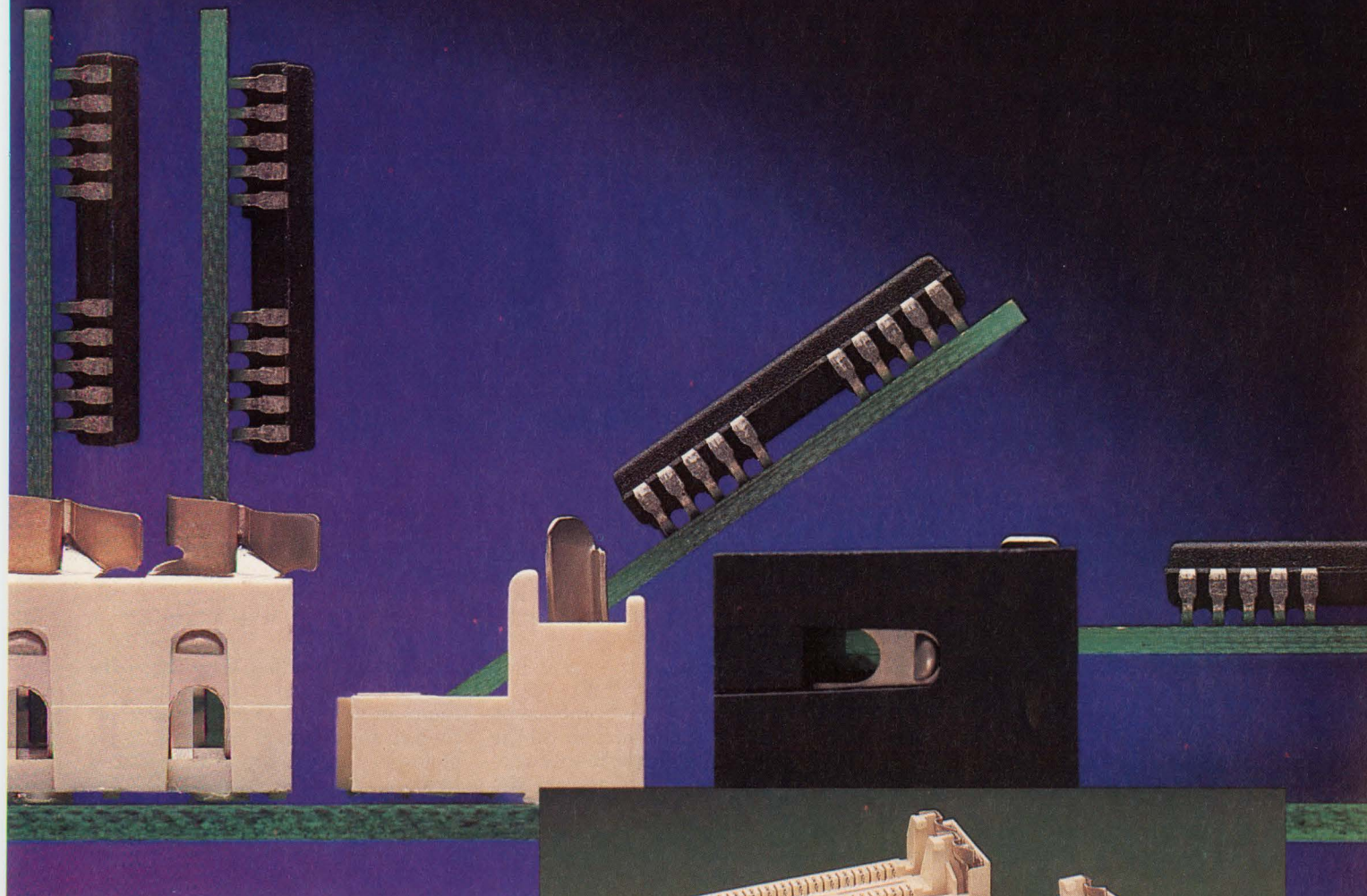
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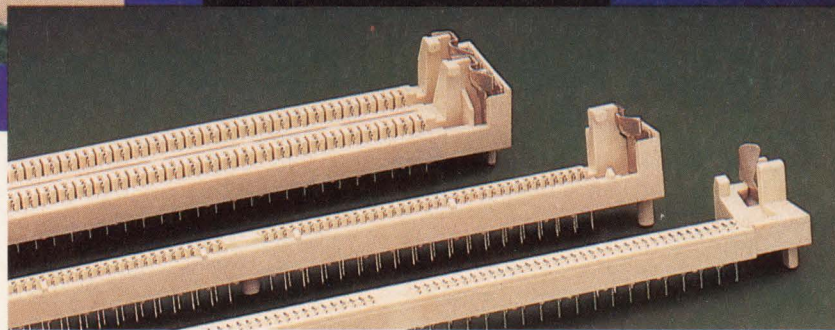


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CIRCLE NO. 57

RISC champions challenge Moto in embedded control

Jeff Child, Associate Editor and Dave Wilson, Senior Editor

As the younger, faster RISC tries to knock the spots off Motorola's CISC, the weary champion of embedded control is adding new weapons to its kit and gluing-up the chinks in its armour.

As the dark ages of CISC-based embedded control draws to a close, the curtain seems certain to rise on the RISC renaissance. But CISC is unwilling to abdicate its throne. Instead of playing dead, it produces many heirs willing to fight for the future of CISC in embedded control.

For years, Motorola's (Austin, TX) 68000 CISC processor has won the day in embedded control. So, it's hardly surprising that the 68000 is now the target of every other processor architected for embedded design. The assault on the 68000 family is coming from RISC-based embedded machines that promise a two- to five-time performance improvement at a similar cost. To counter this attack on its design base, Motorola has dressed up and stripped down the 68000 in an attempt to make it appeal to a broader audience. Currently, the company offers an integrated 32-bit microcontroller family, the 68300, as well as a cost-reduced family of derivatives, dubbed the 68EC000 series. The result—a range of processors that offer “near” 68000 software compatibility at prices that will eventually start at \$1. But if CISC isn't enough, Motorola is readying its own embedded RISC—a design based around the 88000. Whether you buy into Motorola's pitch, or buy a competing vendors RISC processor, depends on

application requirements, price, time-to-market, cost of development tools, and how much faith you have in superscalar C compilers, emulators and debuggers.

■ When Motorola has it all

Through the EC series of processors, Motorola is trying to accelerate the adoption rate of 68000 family processors in embedded system designs. Cost-reduced EC versions are becoming available just months after the mainstay 680X0 processor line. The company has already announced EC versions of the 020, 030 and 040, and has divulged that an EC050 will be available six months after the introduction of the 050.

Motivation for the EC series came after the 030 was developed. “The 030 design included an MMU on-chip which a lot of the embedded world didn't want,” says Motorola's Jim Reinhardt, 68000 family marketing manager. Motorola, therefore, offered the EC030—an 030 without an on-chip MMU. Next will come the EC040, a 040 derivative processor without the MMU or floating-point unit. Somewhere in between the 040 and EC040 will be a processor that may incorporate the MMU, but not the FPU, or vice versa.

Rather than strip functions, the 68300 processor family lets Motorola's chip designers add modular

microcontroller peripherals to the 68000 architecture via an on-chip bus. Motorola feels that it's this modularity that will let it design many derivatives in a relatively short time. “We don't redesign the modules—we just mix and match them in certain combinations according to designers' requests,” says Motorola's marketing manager Arie Brish.

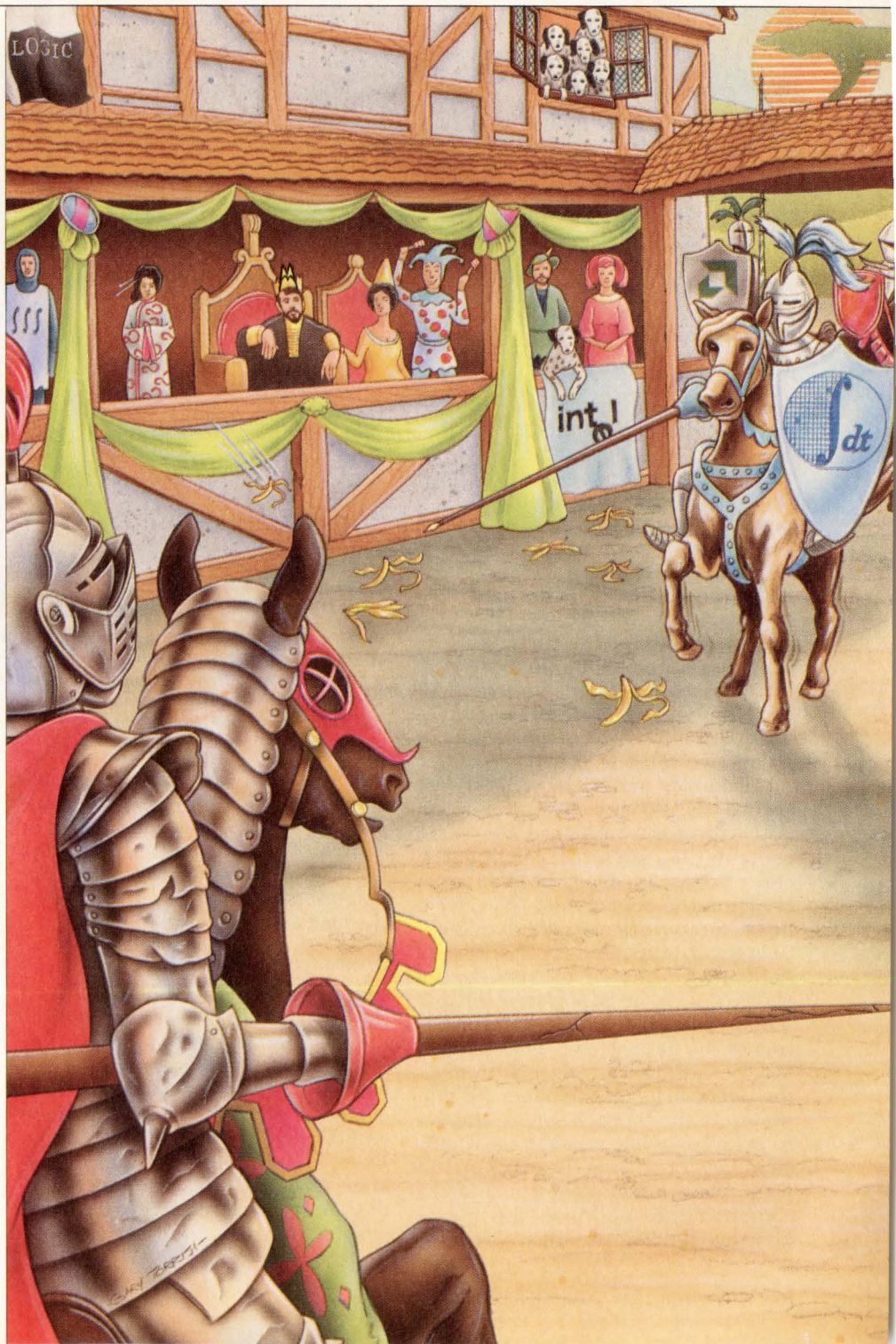
In addition to a 68020 core, the 68300 series sports smart peripherals that can help off-load tasks from the core processor. One example is the timer processor unit (TPU) found on the 68332. According to Brish, the TPU is an independent processor that doesn't need as much CPU intervention as conventional timers found in other microcontroller designs. The CPU can assign tasks to the TPU, and the timer controls the task to completion, only then interrupting the CPU. This approach minimizes the interruptions to the CPU, freeing it to perform other functions.

David Wilner, vice-president of engineering at Wind River Systems (Alameda, CA) feels that the 68000 is a well-liked, reliable workhorse. “The 68000 tools are good; there are good debuggers and development systems and emulators,” Wilner says. “And although the 68040 has been a disappointment in terms of getting to market on time, it's show-

ing enough horsepower to keep the family alive." Wind River also sees a lot of interest in the 68300 series, especially in specialized niches, Wilner says. "Although it was a bit annoying that the processor cores on the 68300 are not exactly the same as the 68010 and 68020, so our (real-time) kernel has had to be 'tweaked' a little in order to make it run."

Since many designs are currently based on the 68000, it may not be possible (for software reasons) nor rational (for economic reasons) to make the leap to a RISC architecture. If that's the case, designers can consider hooking their 68000 designs up to a custom gate array optimized to accelerate specific functions that may be faster, but more costly, to perform with a dedicated RISC engine. For \$40 or \$50, the combination of a 68000 with a gate array handling bitblt (bit boundary block transfer) in a graphics or laser printer application, for example, might be more cost effective than a \$75-\$100 RISC chip with its associated high interface costs.

Even Motorola sees the benefit of this approach, although the company may add dedicated logic around a 68000 core itself, rather than sell separate silicon. "A lot of the work in a laser printer engine involves transforming a page description language like Postscript



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into a rasterized image. Then, operations like a bitblt or a font rotation must be performed on that rasterized image," says Motorola's Brish. "Rotating a font is a horrible thing to do using conventional CISC instructions. It requires a lot of instructions and it takes 100 to 120 operations. Putting a dedicated hardware array on a processor to perform that operation reduces the 100 or so operations down to two. Such functions can be performed by adding a few thousand gates to a processor like the 68000. Furthermore, it provides about a 50:1 acceleration," Brish concludes.

Who needs more?

Not all embedded applications need to embrace the philosophy of RISC, says Fred Neuenschwander, manager of product development at Houston Instruments (Austin, TX). In Houston Instruments' DMP60 series of plotters, an embedded 8-MHz 68000 controls the whole plotter. "The processor parses incoming data, interprets the data, makes calculations based on the data, and drives the servo motors that control the pens that draw the picture," Neuenschwander says.

When Neuenschwander determined that controlling the servo mechanism was eating up a large percentage of the 68000 compute time, he chose to complement the processor with an NEC processor. "When we ran out of compute power with the 68000, we turned the servo control over to an NEC processor designed for servo control," he says. Off-loading the servo tasks to a coprocessor gave Houston the opportunity to perform more computations with the 68000 to optimize the pen movement in its higher-performance plotters. In the DMP61DL color pen plotter, for example, the 68000 handles interpretation of the data stream as well as all the computation involved with placing pen marks on the paper. "When we put in the coprocessor, we started to examine what was the most efficient way of putting the mark on the page. We wound up doing a lot more computing to optimize the movement of the pen," he says.

"We've looked at quite a few other processors," says Neuenschwander. And the 68332 is a processor he cites. "But before we launch off into a new product development, we look at code compatibility between the new processor and our existing development tools. There's got to be a strong, overwhelming reason if we want to make a change."

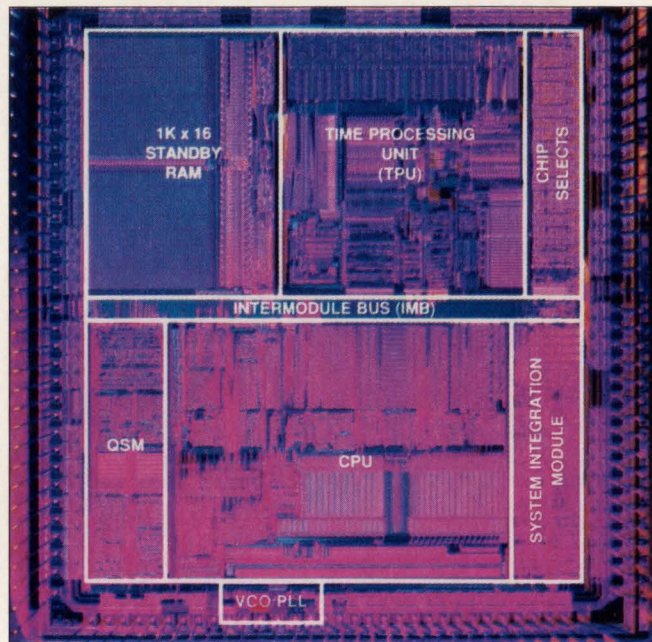
Neuenschwander says that he could design in a 16-MHz 68000 if he needed more processing power. "We're only running at 8 MHz now." By doing so, he says he could "double the processing without doing very

common bus to several pipelined digital signal processing chips that perform dedicated graphics operations—matrix calculations, perspective calculations, translation, clipping, and filling. The results of the calculations performed by the DSP chips are fed to a common frame buffer, where a Texas Instruments TMS34010 performs the graphics drawing function. The 68EC020, an EC part "not a RISC chip" is now being designed into a new Atari arcade game.

The EC020 has helped Atari improve the graphics performance of the system. "The removal of the MMU wasn't critical in our application," explains Richard Miller, Atari's vice-president of engineering. "What helped was the reduction in the processor cycle time that meant memory accesses were performed faster. For a standard operation like a memory fetch, a 68000/010 takes about four cycles. The EC020 brings that down to three," he says. That feature helped improve the graphics performance. Having previously used the 020, Miller said it was easy to use the EC020. "Even though Motorola added a couple of new instructions in the instruction set," he explains.

Beyond the EC020, Miller admits that he's interested in RISC. "But we're limited in the prices we can charge for our products. We have to go to the lower end for processors," he says. "Typically, we max out the capability of whatever system we design. What happens is that the programmers have to write some of their key software routines in assembly language. The big benefit we would get out of RISC is that our programmers can write code in C, saving them the time of having to optimize the code. It's a question of time-to-market and being more efficient with the design staff," he concludes.

Atari has looked at a number of RISC processors. "But to move over to RISC, the price/performance would have to be there," says Miller. "At present, most RISC solutions aren't quite where we would like them." Another concern Miller



By integrating more peripheral functions on-chip, Motorola hopes to retain its hold on the 32-bit embedded control world. The 68332 is a 68300-family derivative originally designed for the automotive industry. It sports an on-chip time-processing unit that can offload the core CPU from many interrupt handling chores.

much at all." But there are mechanical limitations. At present, plotters write with pens moving at 32 in/s. "It doesn't do me any good to use a processor that runs twice as fast because the pens won't write on the media any faster," he emphasizes.

Who can afford it?

Like Houston Instruments, Atari (Milpitas, CA) has used the 68000 as a workhorse processor for years. But unlike Houston Instruments, Atari's arcade video game applications could use all of the power that dedicated RISC processors could deliver—if only they were less expensive. Presently, a common Atari design approach uses a 680X0 as a system controller, talking across a

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raises is the availability, quality and cost of development systems, languages and compilers. "Poor to good," is how Miller describes them. "It seems like the best processors that are being supported by tools are in the PC family, and that's not really suitable for our particular applications," he adds.

Designers using RISC

Unlike Houston Instruments' Neuschwander, other designers do need more power. And some, unlike Atari's Miller, have big enough wal-

risking next-generation projects on untested tools, buggy chips and inoperative compilers is a practice even the most adventurous design-engineering managers don't welcome.

All embedded RISC chips share the same goal: to outperform the Motorola line. And many do. "The 29000 is two or three times as fast as a 68020 (at the same clock rate) doing system call functions," says Ed Rathje, vice-president of JMI Software (Spring House, PA), suppliers of Cexecutive, a real-time kernel that runs on virtually every

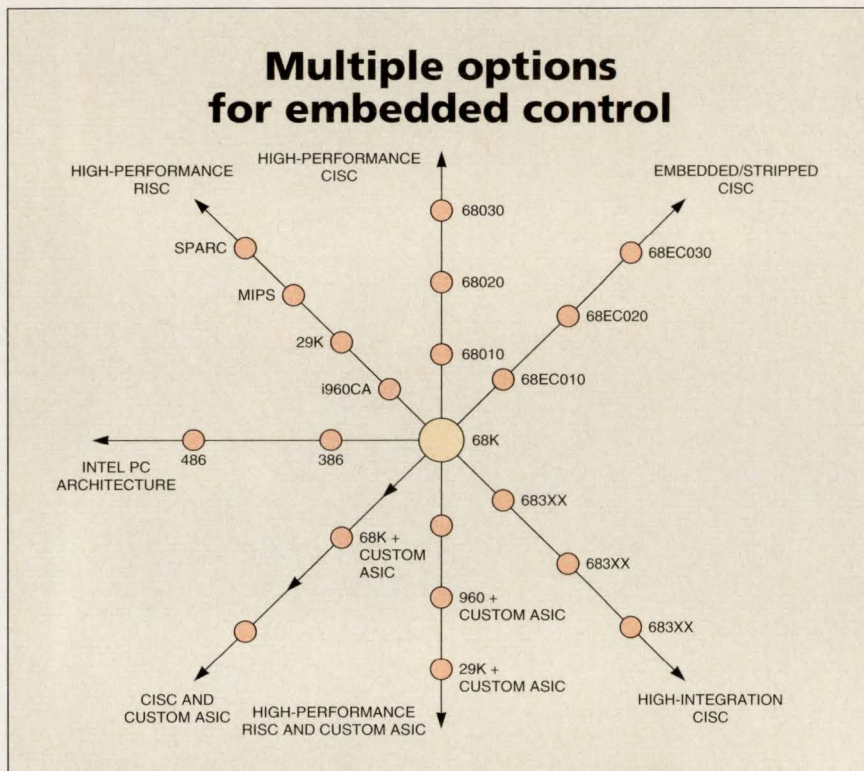
tion to memory controllers and, in some cases, hardwired accelerator functions as well.

In the RISC camp, Intel (Santa Clara, CA) offers nine variations of its i960 processor architecture. Intel has all the bases covered, from the \$1,500 i960MX (which incorporates a superscalar processor, FPU and MMU) to the SA, an under-\$50 part that just has a 32-bit core. AMD (Austin, TX) offers five versions of the 29000, from the low-end 29005 to the high-end 29050. Not to be left out, other vendors like LSI Logic (Milpitas, CA) and IDT (Santa Clara, CA) are aiming to put embedded MIPS on the map. The LR33000, also called the Pocket Rocket, is LSI Logic's contribution. And IDT offers the somewhat less expensive R3051 and R3052 MIPS processors. The IDT 3051 family integrates on-chip MMU, a DMA controller and read/write buffers. As for cache, the chip has 4 kbytes of instruction and 2 kbytes of data cache. The R3052 has even more—8 kbytes of instruction and 2 kbytes of data cache. The LSI Logic LR33000 part also integrates large caches (8 kbytes of instruction and 1 kbyte of data cache) onto the chip in addition to counter/timers, a DRAM controller, write buffers, and wait-state generators. LSI and Fujitsu (San Jose, CA) have also integrated many peripherals onto their embedded Sparc processors. Fujitsu's less filling processor, the MB86930 Sparclite, sports DRAM support logic as well as 2 kbytes each of instruction and data cache. For math-intensive applications, the Sparclite also has a one-chip hardwired 32- \times 32-bit multiplier.

All these RISCs are making headway in areas where high performance at low cost is an absolute requirement—such areas include laser printer controllers and X terminals. JMI's Rathje feels that "in low- to medium-performance applications, the 29000 and the i960 are fighting it out. Whereas in the medium- to high-performance ones, the MIPS R3000 is a hands-down winner." Rathje says that the Sparc front has been relatively quiet. "Sparc appears to be a minor player," he says.

Like JMI, Wind River Systems hasn't ignored RISC—both Sparc and the i960CA are supported. "The i960CA is popular in applications that don't have any connection to Unix," says Wind River's Wilner.

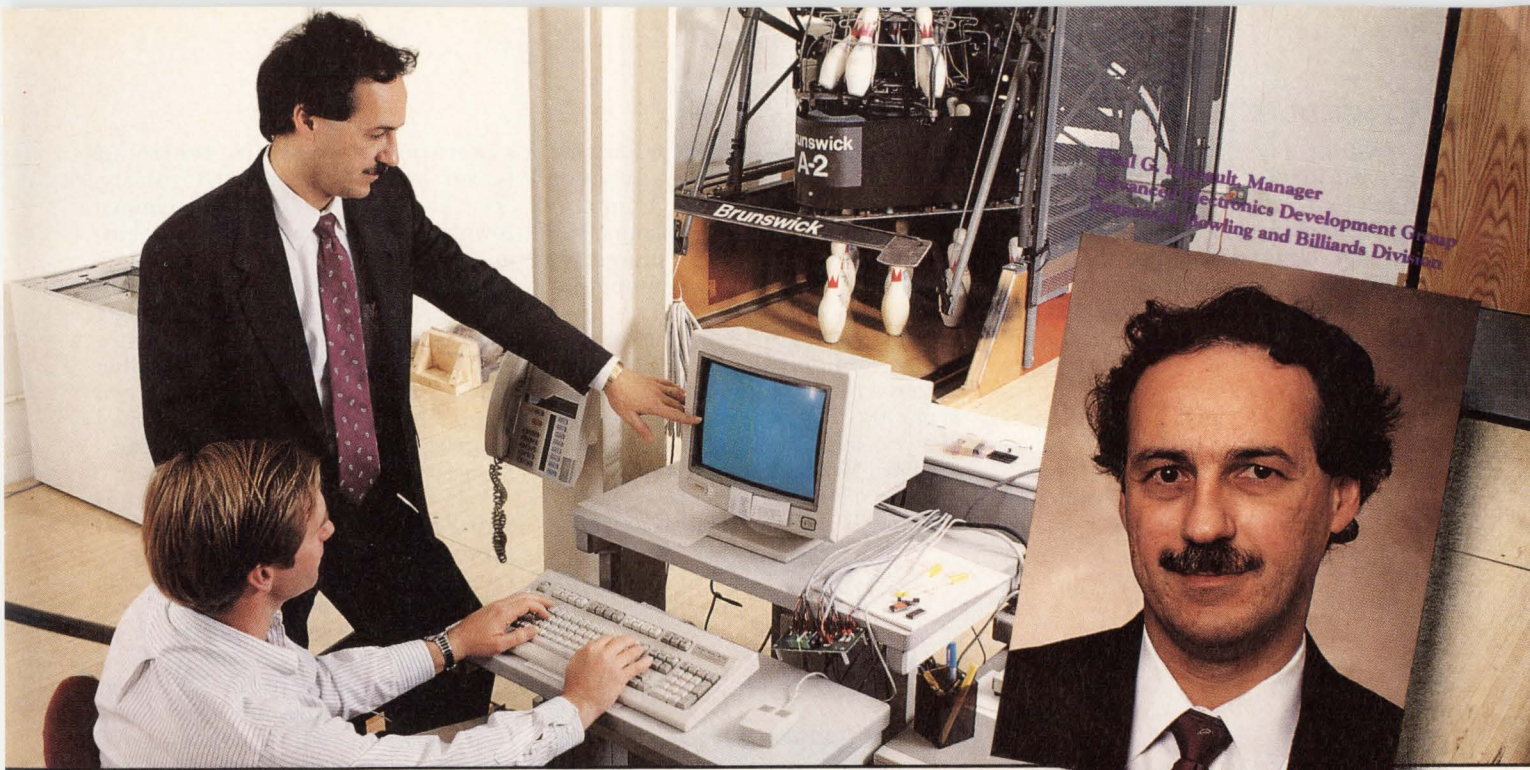
Multiple options for embedded control



For years, Motorola's 68000 CISC chip was the only sensible choice for embedded control. Today, there are a lot more processors to choose from—and they're not all Motorola designs. Aside from just adding an ASIC to rev up performance, designers can switch to Motorola's stripped-down or high-integration 68000 derivatives. If that's not enough, they might like to try picking a RISC—either Motorola's or someone else's.

lets to pay for it. Certainly, there are no lack of IC companies willing to sell RISC processors. To compete with Motorola's "cover all the bases" strategy, those vendors have debuted many devices spanning a range of price/performance points. They're racing to support them with development tools and operating systems, realizing that designers will shy away from any processor until some software development tools are in place. That's because success in the embedded marketplace is a cost/time-to-market issue, and

embedded RISC processor, including the Sparc, i960CA and 29000. Even more bullish is Bob Rowe, RISC product marketing manager for Integrated Device Technology (Santa Clara, CA). He says that his company's MIPS-based 3051 processor offers from five to 10 times the performance of the 68020. To enhance their appeal to embedded designers and to lessen the trauma of building high-performance processor/memory subsystems, RISC processor houses have integrated large caches on-chip in addi-



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Wilner says that one of the perceived problems with the Intel i960CA is that, unlike Sparc- and MIPS-based processors, it isn't used in any Unix development system. "Some people like to have similarity between the target and the host system. But for those that don't, the 960 fares quite well," Wilner says. "MIPS processors really shine where people need floating-point. That's its really spectacular benchmark," he concludes.

Another advantage of employing a "Unix/RISC" processor in an

series of RISC-based microcontrollers that has already been blessed by Ford Motor Company (Dearborn, MI). Cars, it seems, will soon have Motorola RISC processors in them even if Apple Computers' computers will not.

"When you start focusing on cost-per-performance basis, RISC architectures really stand out as a winner over CISC," says Sam Cole, manager of advanced powertrain electronics at the Ford Motor Company's electronics division. "For the same power, CISC is a much more expensive machine.

generation powertrain controller based on the Intel 8061 family. "But," he adds, "we're trying to move towards the use of high-level language for coding." Cole says that as the amount of code that Ford has to manage grows, the next strategic move is to be able to make software changes readily and design reusable blocks of code. To do that Ford needed to move towards a high-level language environment for programming and a 32-bit RISC processor.

When it first became apparent that Ford was settling upon a RISC processor/high-level language solution, concerns were raised about the cost of memory in the system. "Five or six years ago, memories were fairly expensive. So the cost of memory compared to the CPU cost was fairly significant," says Cole. "Furthermore, when you go to a high-level language there's an inefficiency associated with it—another 10 to 15 percent of added memory. But nowadays, memory is becoming less and less significant in terms of the total cost picture," he adds.

Ford was faced with tradeoffs. On one hand, it had the option of designing with a CISC machine with a large die size, slower throughput, but a smaller system memory size. On the other hand, was a RISC machine with a small die, fast throughput and a larger system memory. "When we costed it all out, and even added some margin for the larger memory size required by RISC and programming in high-level languages, Motorola's RISC still comes out to be a much more cost-effective solution," Cole concludes.

For routing and shooting

Despite all the problems associated with RISC, manufacturers of computationally intensive embedded equipment have migrated to RISC processors other than Motorola's. "We picked the i960CA because it was the fastest single-chip RISC processor that we could find at the time," says Joe Duran, vice-president of engineering at VideoTelecom (Austin, TX), manufacturer of teleconferencing systems. Even so, "we designed our own custom coprocessor for motion-compensation and DCT," Duran admits.

VideoTelecom has used no less than four i960CAs in the design of its latest system. Three of them are used together with a custom coprocessor simply to perform video processing. The first i960CA is used



While early RISC tools were poor, most designers admit the tools are getting better. Tools like this 29000 "Eclipse" emulator from Step Engineering are key to the design of successful embedded projects. Among other things, the Eclipse lets the designer examine processor execution statistics, including interrupt latency, instruction cache efficiency and event timing.

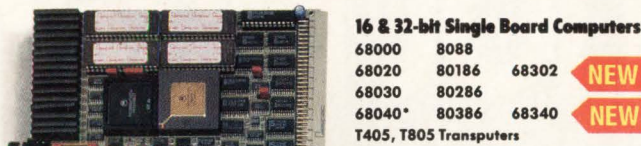
embedded processing application, is that bugs are more likely to have been discovered early on. "By the time the MIPS R3000 reached designers of embedded systems, it had already been running Unix in a workstation environment. We had no hardware or software bugs with the R3000 processor at all," says JMI's Rathje.

Despite the fact that designers complain of "bugs" in compilers and on some RISC processors too, even Motorola's vice-president and general manager Brian Wilkie admits that "in the short term we're losing some design-ins [to our competitors' RISC]. Although long term, we have the market pretty well covered." To beat back the wave of competitive RISC controller technology, Motorola has also embedded plans for its own 88000 series of RISC machines. The 88300 will be a

RISC is a clear winner in terms of price and performance," he concludes. But not everyone is so enthusiastic about the 88000. "We have no plans to support it," says JMI's Rathje. "We only had three phone calls last year (from designers) asking about it. We removed it from our plans."

Designers at Ford Motor Company would probably disagree. The choice of the 88300 as its next-generation processor design is an example of where the need for more computational muscle forced drastic changes. In one fell swoop, Ford moved from CISC to RISC, from 16- to 32-bits, and from a proprietary architecture to a standard processor. And Motorola won a design-in bigger, some say, than even Apple could have furnished. Like Atari's Miller, Ford's Cole admits writing code in assembler for his present

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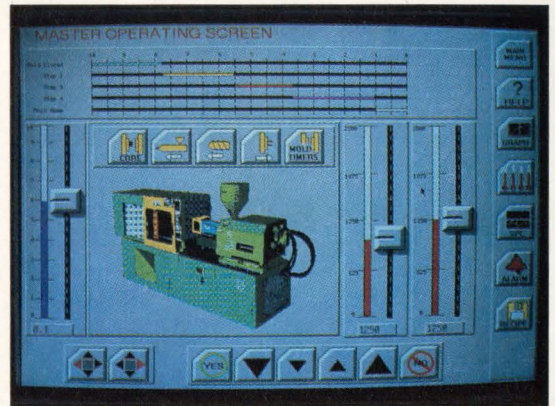
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to calculate different information between video frames. The second controls the discrete cosine transform (DCT) operation that's performed on the motion compensated difference by the dedicated custom processor. The third performs Huffman run-length encoding. Yet another additional i960CA processor acts as the communications multiplexer and implements the CCITT standard H.221 communications protocol. The i960CAs are front-ended by an Intel 386 so that the user can teleconference using PC-based material.

"The only reason we used three i960CAs is because one wasn't fast enough," says Duran. "The i960CA didn't have floating-point capabilities, but since MPEG and P×64 compression schemes don't require it, those capabilities would've been wasted anyway," he says. Although he's pleased with the performance of the device, he's concerned about support. "Chip vendors worry more about chip design and not enough about support," Duran says. "The situation wasn't worse than I expected. But I wasn't happy with it. Initially, my engineers decided not to buy any development tools because they couldn't find anything satisfactory," he concludes.

It appears bugs have been a problem with the i960CA. "The 960CA has been a pain because Intel has had trouble getting it working right," one designer told *Computer*

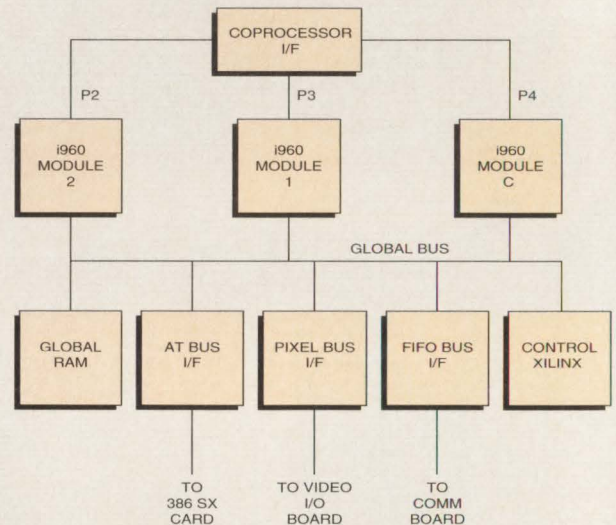
Design. "It's not always clear what the implications of a bug are when you have concurrent processes running in a superscalar processor," added another. Documentation may be hard to interpret too. On an earlier version of the i960 (the i960MC), microcode performed part of the function of iRMX, Intel's own real-time kernel. When the KB and the CA versions were developed, that microcode was removed from the chip. At the same time, Intel removed sections of the i960 documentation that described how the microcode worked. Consequently, no documentation existed that explained how the i960 KB and CA could be used to perform a context switch during an interrupt in a real-time application.

Aside from bugs, other vendors have found that the i860 RISC processor, the machine touted by Intel as a graphics/numerics coprocessor, may perform better in real-time applications than the i960CA, Intel's "embedded processor." "You would think that the i960CA would be the best processor for context switching," says JMI's Rathje. "But in our measurements at the same clock rate, the i860 is more than twice

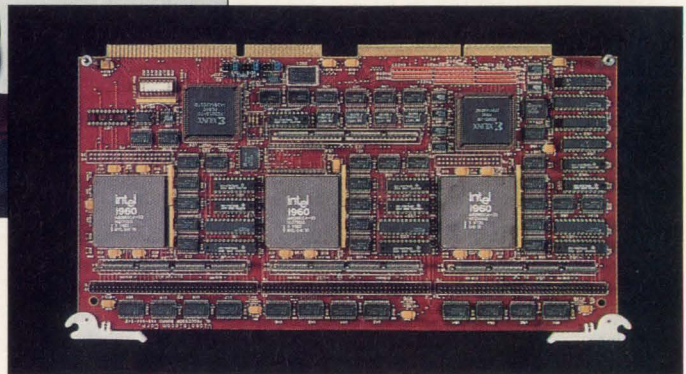
as fast as the i960CA," he adds. Intel, however, chooses not to market the i860 as an embedded processor. "At 33 MHz, the i960CA performs a context switch in 7 μ s; the i860 does it in 3 μ s," Rathje says. JMI's measurements were performed on a i960CA board called "the Tomcat." According to Rathje, that's a high-performance demo board used by Intel, but unavailable to designers. "Unfortunately, you can't buy it," Rathje says. "The i960CA board you can buy...is slower."

John Wakerly, vice-president of engineering at Alantec (Fremont, CA) chose to use the embedded MIPS processor from IDT instead of the i960CA for the design of his MIPS-based routing and bridging engine. Alantec's router lets a dozen

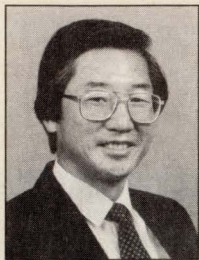
VideoTelecom's video teleconferencing system



The image processing heart of VideoTelecom's video teleconferencing system is a board using three Intel i960CAs and a custom coprocessor. A fourth i960CA was used in the system as a communications controller. A 386 PC-class machine lets the user incorporate PC-generated material during a teleconferencing session.



The best way to control laser printers—RISC, CISC or ASIC combo?



In the past, designers who wished to increase the performance of CISC-based laser printer controllers have had limited options: they could simply increase the speed of their design or they could redesign their hardware and port their PDL(page description language)/PCL software to a new RISC processor. In both scenarios, controller performance upgrades could be achieved through the use of a faster processor and faster memory devices. Fierce competition, however, imposes stringent cost-reduction pressures, thus limiting the approach of expensive cache RAM subsystems to improve performance.

Now, however, there's an alternative. It involves adding specialized hardware-assisted ASICs to speed up certain functions on a "tired" CISC design. Not only can the approach result in a 100 percent increase in performance over the RISC-only approach; it can also cost as much as 60 percent less than a RISC solution as well. Further, adding such devices to a RISC design can result in a solution with an 8x increase in printing speed at a cost increase of only 20 percent over that of an unassisted RISC design.

Interpreting, rendering, painting

Laser printer controllers perform three tasks: interpreting, rendering and painting. Of the three, interpreting involves the parsing of input commands (printer commands or page descriptions) into low-level symbolically represented page elements or graphic objects of three types: outline or bitmap fonts, line art or halftone images. Interpreting, as a general compilation process, requires a general-purpose engine like a CISC or RISC microprocessor.

Rendering, on the other hand, translates each object into bitmap form and places each into an object cache. Rendering typically involves special algorithms which convert the symbolic representation of graphic objects into bitmap representations. Here, custom hardware designed to execute the chosen algorithm can perform orders of magnitude faster than a general-purpose microprocessor.

Finally, painting merges the desired fill pattern (usually black for text) with the object and writes the resultant image to the frame buffer location specified by the interpreter. The basic painting operation is the movement of a block of bit-map (pixel) data from one memory location to another, (bitblt, or bit boundary block transfer). Since the address of a bit-map block is specified in pixel (dot) units, the address scheme differs from the byte/word address scheme of a general-purpose microprocessor. Here again, special hardware can be built into an ASIC to handle the tasks.

Differing design approaches

By comparing different design approaches, it's possible to analyze the performance of a laser printer by observing the time taken on the interpreting, rendering and printing phases, while the bitmap data for font, line art and image objects is being generated. The most common architectures either use a 68000, or a RISC processor, in conjunction with a bitblt ASIC engine to improve the performance of the painting stage.

The performance gains achieved through hardware assistance in the painting step lead us to believe that it's advantageous to accelerate the rendering step for graphics objects as well. Accelerating outline fonts is most important because text occupies more than 90 percent of the typical page content and rendering complex outlines requires significant computational power.

The Rida (raster image device accelerator) chip from Destiny Technology Corporation (Milpitas, CA) is a dedicated device that works as a slave processor to a CPU and allocates rendering of graphic objects (especially outline fonts). Conceptually, this rendering process consists of several steps. During curve generation, the CPU transfers character control points to a font imaging system, which can vary in its partitioning between software and hard-

ware depending on its design. Second, the outline font is expanded and rotated to the desired size and orientation. Next, scan conversion translates the outline into polyline segments composed of many short vectors; the contour closely approximates that of the original curve. The segments are next checked through dropout compensation by the Rida chip. The interior pixels are then turned on. The resulting bitmap is called the "cache." During painting, the cached character is used as a mask and the desired fill pattern is written to the frame buffer through the black pixels in the cache.

Cost and performance

Cost and performance of CISC and RISC controllers incorporating a Rida coprocessor as well as a bitblt ASIC are summarized below. Assumptions are

	IMAGING SPEED		COST	
	Index	Ratio	Index	Ratio
POSTSCRIPT CONTROLLER				
68000+ASIC+RIDA (avg.)	11.3	5.7	13.6	1.28
80960SB+ASIC+RIDA (avg.)	44.0	22.0	17.1	1.61
29035+ASIC+RIDA (avg.)	54.0	27.0	22.1	2.08
PCL 5 CONTROLLER				
68000+ASIC+RIDA (avg.)	8.0	4.0	11.8	1.51
80960SB+ASIC+RIDA (avg.)	24.0	12.0	14.1	1.81
29035+ASIC+RIDA (avg.)	47.3	23.7	19.1	2.45

that more than 90 percent of the page content is text and that the Rida subsystem cost is three times that of a base 16-MHz 68000. The analysis is based on a 16-MHz clock speed for all CPUs and a memory subsystem for each design that's balanced in terms of wait state and cost. The base 16-MHz 68000 is assumed to have a performance and cost index of 1.0.

David Larrimore, director of marketing at Destiny, also contributed to this panel.

James Lung, vice-president of engineering, Destiny Technology, Milpitas, CA.

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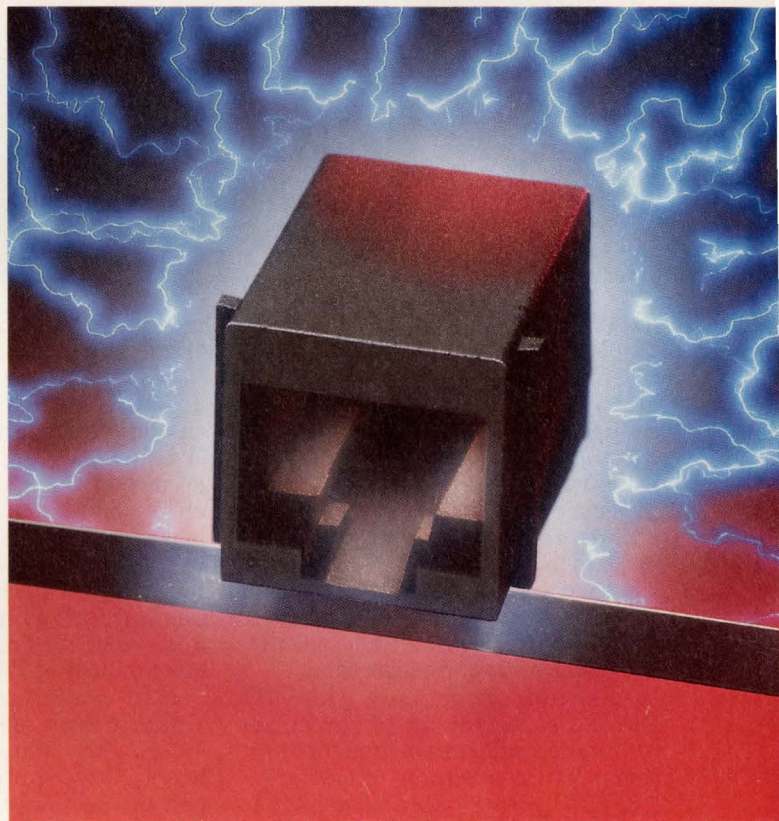
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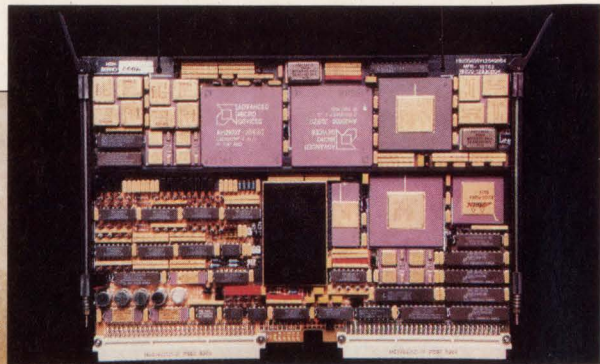
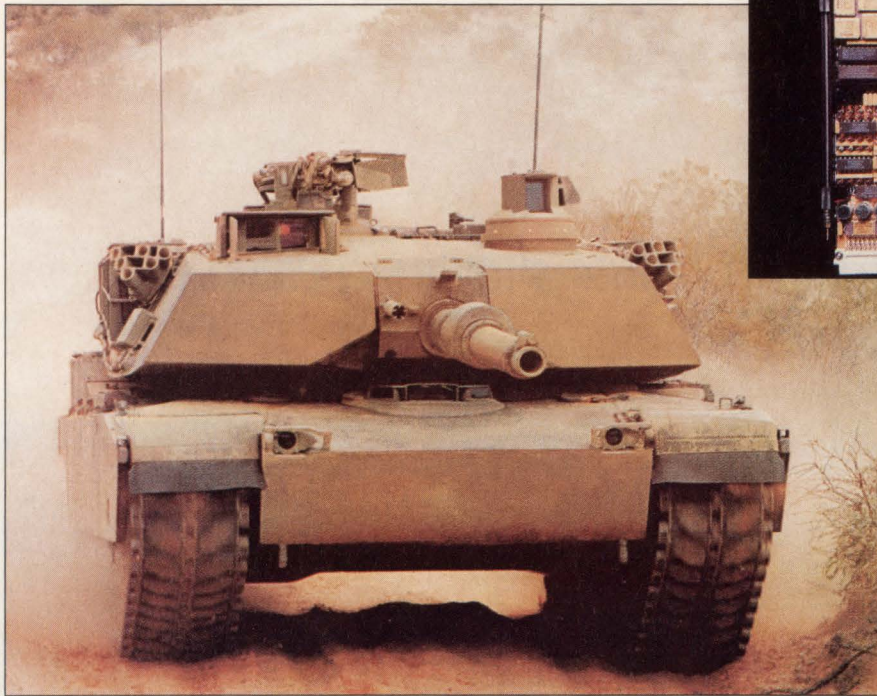


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CIRCLE NO. 63

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Dubbed the Scoreboard, Vista Systems' 29000-based VME card replaced two CISC boards in the fire control electronics unit of an M1A2 battle tank. Of the other two boards, one board carries a 68040, while the other incorporates a 68020 as well as a 56000 DSP.

Ethernets be connected to it in a star topology. The router has the processing power to forward packets among any combination of networks connected to it without any delay in throughput to individual users. An R3000 processor is used as the main processor. It executes the algorithms responsible for forwarding packets to and from the workstations, whether that might be a transparent bridging algorithm or a TCP/IP (Transmission Control Protocol/Internet Protocol) routing algorithm.

A second processor, the IDT R3052, is used as an I/O processor to handle buffer-management functions. "We needed lots of cost-effective CPU power, because we have to look at each and every packet that comes in from each network and make forwarding decisions to decide where each packet is sent. The R3052 is a high-performance dedicated control processor. It runs at 33 MHz and I expect to get 28 or 29 Mips from it," Wakerly says.

■ On-chip cache important

In Alantec's application, having enough on-chip cache was an important consideration, since all the real-time code fits in cache. "All the important code is in cache all the time. We're able to organize the code so that we have no cache misses. The LSI Logic part has only 1k of data cache and that would've really hurt

me (had I used it)," says Wakerly. "I'm just getting by with 2k as it is."

Like many designers, Wakerly realizes that the lowest-cost RISC processor is the one with the lowest die size and the smallest package. "The 84-pin PLCC format of the [IDT] chip was an absolute winner. I looked at the LSI LR33000, but it appeared to be twice the price in a much bigger package. It also had a nonmultiplexed address and data bus, which was not an advantage in our application," he concludes.

Had there not been a 3052, Wakerly may have looked at the i960SA (the 960 with a 16-bit data bus). "My application would've driven me toward a device with a relatively inexpensive pinout and had the potential for having very high performance as long as all the code can fit within the on-chip cache," he says. "Finally, we were buying MIPS compiler technology. That was very important," he adds.

The present Alantec product is based on the Intel 386. "We use an AT motherboard, with some custom interfaces we designed, to build our existing bridge product," says Wakerly.

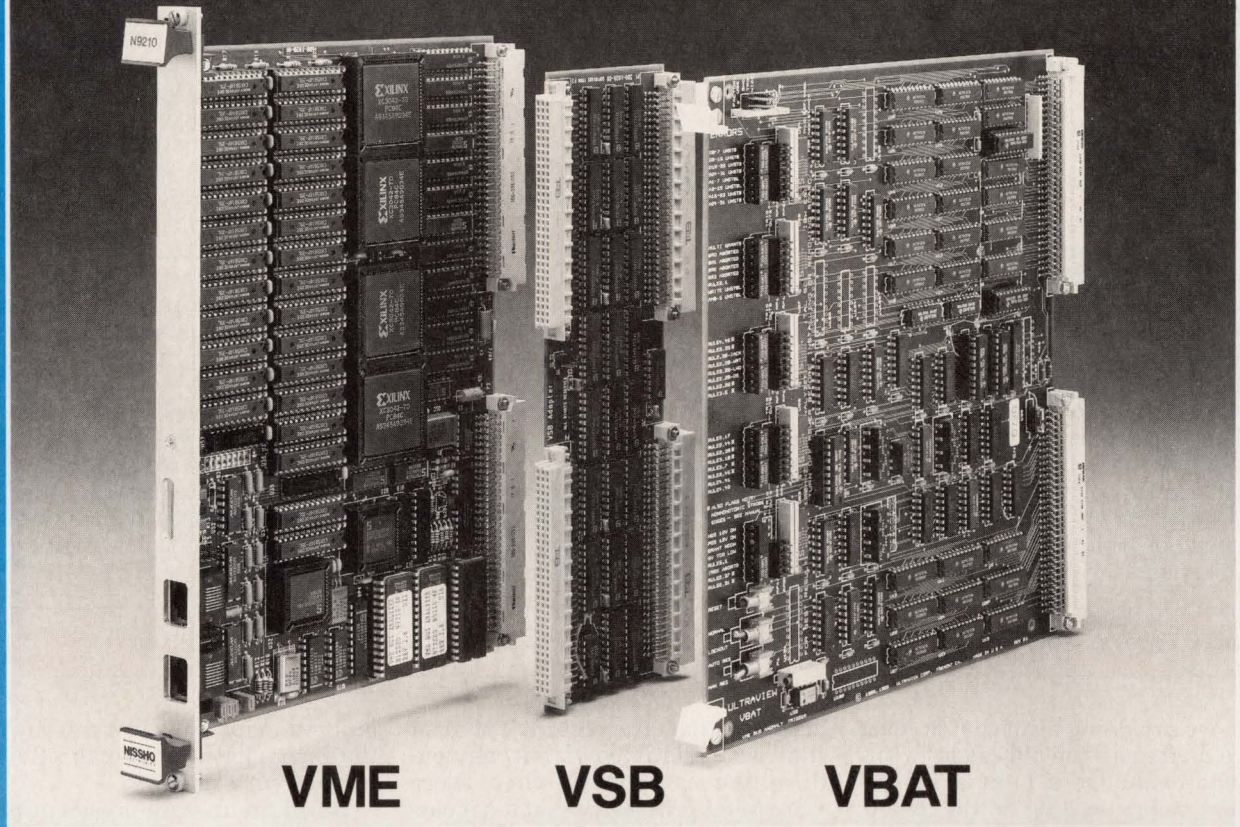
So how does the RISC solution compare? "Looking at the Intel 386, it costs \$200 to \$300 to get 4 or 5 Mips CPU power, versus an IDT 3052, where for \$75 to \$100, you can get 20 to 30 Mips," says Wakerly.

Other designers using MIPS noted that the IDT part is also less expensive than the LSI Logic processor. Aside from price, the DRAM controller on the LSI LR33000 was cited as an example of where some design flexibility could be lost. "You can get a competitive edge by designing a different DRAM controller than the one offered by the vendor," noted one designer (who wished to remain anonymous). "If you use the same as every one else, you don't get the advantage."

Although he looked at MIPS too, Gorky Chin, director of research and development at Vista Controls (Valencia, CA) chose the 29000 as the CPU for a single VME card that replaced two VME processor boards in the fire control electronic unit that sits in the turret of an M1A2 tank. The 29000 board, dubbed the Scoreboard (servo controls optimized RISC engine), controls not only the gun turret drive, but also performs system processor functions. Previously, the system processing was performed by a separate 68040 VME board, while the gun turret control function was performed by a VME card with a Motorola 56000 DSP working in conjunction with a 68020. "It turned out we could do the control function and still have significant capacity on the board to take over the system processor functions as well," Chin says.

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CIRCLE NO. 64

29000 helps speed up the Little Dipper



Clearpoint Research (Hopkinton, MA) researched several microprocessors for use in the design of the Little Dipper, a multiport media access control (MAC) learning

bridge router. The bridge itself is an eight-port Ethernet device that sits between eight different LAN segments. Segments can be thin- or thick-wire Ethernet; twisted pair Ethernet will soon be supported as well. In operation, a packet comes into the bridge addressed to a location on another segment and the bridge relays the packet across to that location.

In the design process, two main criteria emerged. First, the processor needed to be high performance. Second, the board area used by the design

needed to be small. The AMD 29000 was chosen because it offered a two to three times performance improvement over available CISC processors. Furthermore, the price of the memory subsystem is comparable to that of CISC in terms of cost, size and scale.

One advantage of the 29000 is the partial Harvard architecture. The device provides separate instruction and data buses brought to the outside of the chip. Using two buses avoids the contention that arises when data and instructions are cycled through the same bus. A Harvard architecture separates out the instruction references and lets slower SRAMs be used without a serious performance penalty. A cost-effective memory system, therefore, could be optimized for the bridge environment.

Several other RISC chip designs were investigated including Sparc, MIPS and the Intel i960CA. But at design time,

the 29000 was less than half the price of the other devices. Furthermore, the 29000 didn't require expensive surrounding cache logic to support it. Sparc and MIPS weren't as user-friendly for a small application.

To get real performance with MIPS, board designs should employ a cache. Because the 29000 lets sequential instructions be executed in single cycles, it works well without an instruction cache. The on-chip branch target cache improves program execution by supplying the processor execution unit with instructions. The Intel i960CA has a promising future, but at the time of the Little Dipper design, only the K series was available. Using a 1984 version of silicon, the K series didn't meet Clearpoint's performance demands. The i960CA had potential, but the product was not mature enough to meet the design schedules of the bridge.

David I. Emery, senior technical consultant, Clearpoint Research, Hopkinton, MA

"And we are doing all of that at least twice as fast as the old cards."

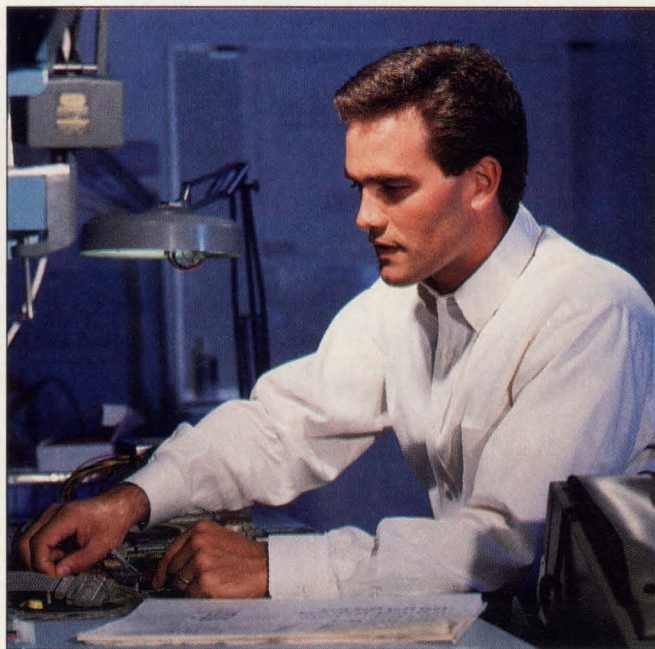
Vista evaluated a number of processors before settling on the 29000. "The performance of all the RISCs were very similar in the math intensive arena that we're concerned with. However, with the 29000, we could design a cheaper overall memory and control scheme," he adds. "When you look at RISC-based embedded applications, you don't want to starve the processor if you give it slow memory." On the Vista board, the program runs directly out of permanent EEPROM store, which saves in both real estate as well as cost, because Chin didn't need to design a bank of static memory to work with the RISC processor.

Vista Controls is currently reevaluating its choice of RISC processors. "We're looking at MIPS again because it's a more accepted military processor," explains Chin. "They came in a very close second a couple of years back," he adds. "The only thing that prevented us from going with them was that the performance didn't quite look as good on the floating-point. And the memory timing requirements were very complex. It was very complicated to implement the MIPS cache scheme because of all the half-cycle type memory

accesses that are required. It's not that we couldn't do it, but why endure the complexity when there were other processors that did it easier?" Apparently, however, Chin now feels that MIPS vendors have overcome the interfacing problems by introducing newer flavors of the processors with the cache interface

built on-chip. "Now you can say that the design job is similar to a 29000," he says with relief.

David Smith, vice-president of engineering at RasterOps (Santa Clara, CA) did choose the LSI Logic LR33000 as the heart of a new color printer controller the company announced this month. One feature that at-



Register windows were the reason Mark Vondenkamp, vice-president of hardware engineering at Advanced Encryption Systems (AES) (Santa Clara, CA), chose to base his encryption networking system around a Sparc-architecture processor. "We run four tasks within our system. We liked the register windows structure because we could switch the tasks and not have to swap register contents out to memory."



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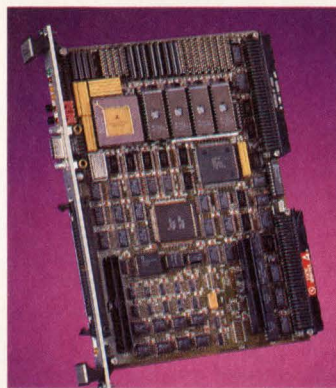
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CIRCLE NO. 65

EMBEDDED CONTROL

tracted RasterOps to the LR33000 was that the MIPS processors were implemented as ASIC cores. "This means that LSI can use these cores to quickly turn out new standard devices in the future," Smith says. Furthermore, LSI is offering these cores to system designers. This will let RasterOps merge its graphics technology with a MIPS CPU at some time in the future.

"RasterOps can control its system destiny by owning what gets integrated into the CPU and still remain compatible with previous generations of products," says Smith. "Software compatibility becomes more important as more and more features are added to color-processing systems, growing the amount of software substantially. If the software can be reused, both time and effort will be saved," Smith concludes.

Sparc solution

Sparc's register windows were the reason Mark Vondemkamp, vice-president of hardware engineering at Advanced Encryption Systems (AES) (Santa Clara, CA), chose the Sparc processor over the competition. Presently, Vondemkamp is designing a number of encryption networking products based around the Fujitsu Sparclite processor. "We're designing a suite of commercial network security products that will provide transmission, access and security control for Ethernet networks," he says. AES will initially debut four hardware products—a LAN adapter card with encryption for the AT bus, as well as three stand-alone units that will sit outside the workstation or host. They will take the data from the host and encrypt it before it goes out to the network. Similar units at the other end of the network will decrypt the data.

"We evaluated a variety of architectures before selecting Sparclite," says Vondemkamp. These included the 29000, MIPS, as well as the i960CA. But the company settled upon the Sparc architecture for its superior interrupt latency characteristics in real-time applications. "We run four tasks within our system. We liked the register windows structure (in the Sparc processor) because we could switch the tasks and not have to swap register contents out to memory," Vondemkamp says. In that way, the company was able to realize a fast context switch time. "The MIPS processor wouldn't have provided us with that capabil-

ity because only 32 registers are provided," says Vondemkamp. Like other RISC designers, Vondemkamp did admit that few development tools were available to support the use of the Sparc register windows in a real-time application.

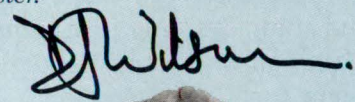
The AES designs were prototyped using a Cypress processor, but the company switched over to the Fujitsu Sparclite because the Fujitsu chip offers several important features the Cypress chip doesn't have. Foremost among these was the hardwired multiply function on-chip, and address and data latches that eliminate the need to perform that function externally. Another important issue for AES was cost. "We didn't want to pay an arm and a leg for a processor," Vondemkamp adds. "In that respect, we didn't think we could beat the Sparclite." Many other processors simply cost too much. "Intel put a \$250 price tag on the i960, and we couldn't justify the cost," he concludes. ■

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Postscript

Which processor should you choose to implement a RISC-based embedded system? It depends on four factors: the performance of the product, the cost of the processor, time-to-market, and what development tools are available. Given the perfect situation—that you were working for a start-up with lots of time and money to invest on design and development tools, as well as no prior record of using a Motorola architecture—you would have several options. If the design was a "low-to-medium performance" one, the choice would be between the i960CA or the 29K. If the design needed "medium- to high-" performance then choose between the MIPS or the Sparc architecture. Intel's i960CA may appear to offer the "superscalar" edge over the AMD29000, but ensure that Intel has removed all known nematodes in the hardware and software before embarking on using it in any design. If you had to choose between the Sparc and the MIPS, then MIPS would be your choice, especially if you had a military project on our hands. But if you could use the register windows to gain a performance advantage in a real-time application, you should consider Sparc. Don't discount Motorola as a player in the RISC business, especially since they inked the Ford deal. Remember, also, that Ford spent two years of active research before deciding to go with the 88K architecture. But for performance reasons, you probably wouldn't consider a high-performance design based around the 680X0 family. Simply put, RISC is faster.



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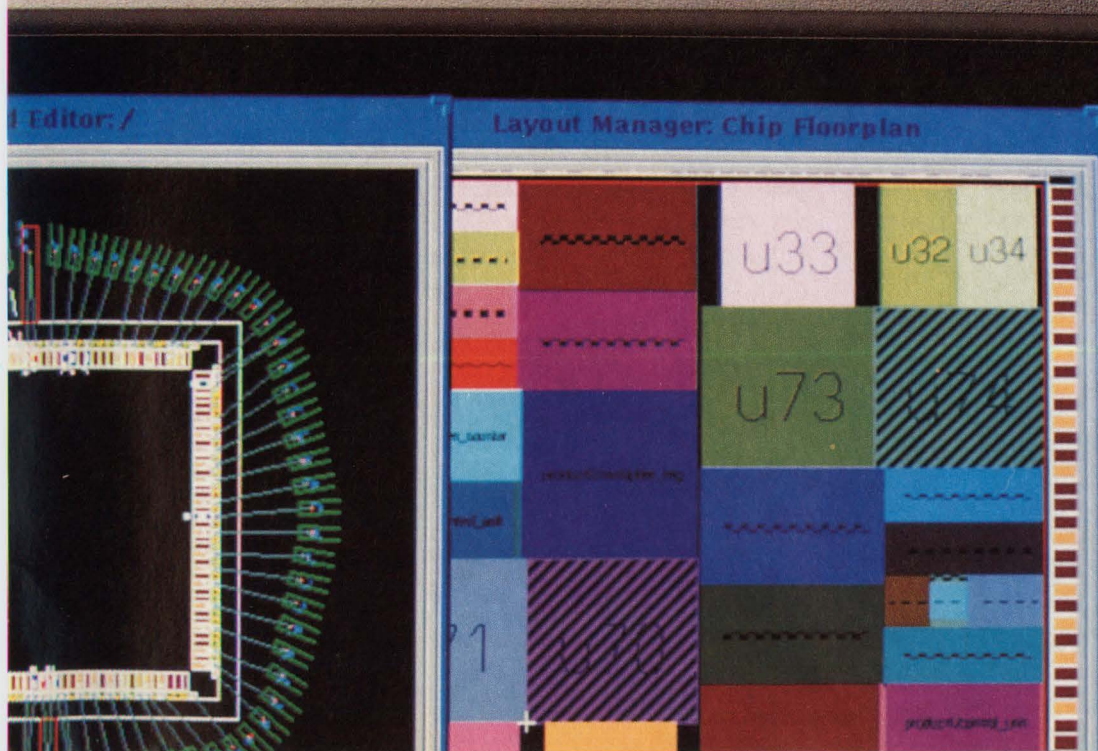
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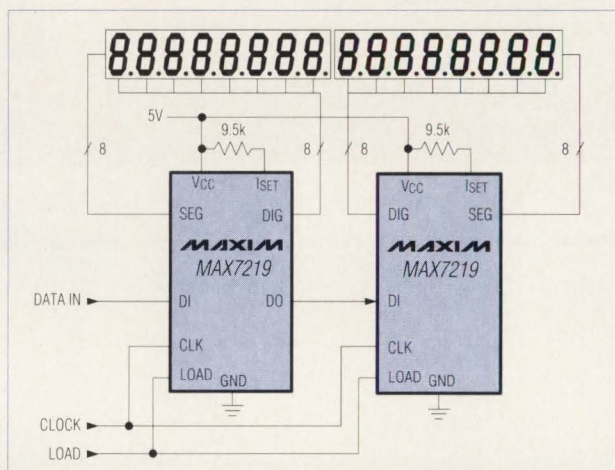
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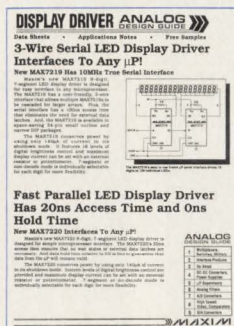
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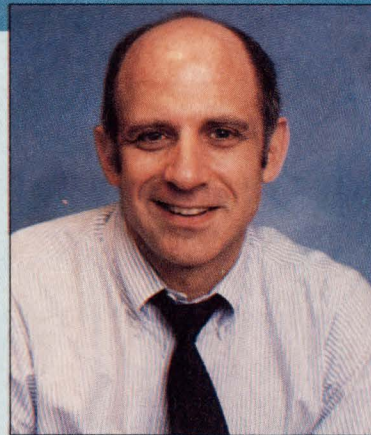


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Getting intimate with transistors

III



Readers of this column will probably be reassured by the fact that—month after month—I'll have only one thing to say: analog is different. What's interesting, of course, is the many ways analog differs. These are as varied as the real world phenomena that produce, or respond to, analog waveforms.

In a control system, for example, input sensors translate changes in temperature, pressure, speed, position, flow rate, light level, etc. into a change in voltage, current or frequency. On the output side of a system, changes in voltage and currents will drive the deflection beam on CRT screens (such as those found in televisions, computers, radar, or test instruments), magnetize coils (such as those on motors or audio speakers), plant magnetic spots (representing data) on the metal film covering a computer's hard disk, or energize a radio transmitter antenna or a laser beam.

The analog and mixed-signal system elements are those which manipulate currents and voltages and translate them into a digital pattern the central controller—invariably a microprocessor—can use. This makes up only a small portion of a largely digital system. As Charles Gopen, vice-president of marketing at Micro Linear (San Jose, CA) describes the electronics world, analog—the interface to real world phenomena—is the “eggshell” covering the otherwise digital electronics world. As this world expands, the shell gets thinner, says Gopen, but the area it covers grows broader and more varied.

While it makes up an increasingly smaller proportion of the electronics world, any kind of analog design—even a mixed-signal ASIC with small amounts of analog—will be experienced as the inverse of the businessman's “80-20 rule.” You know: spend 80 percent of your time with the 20 percent of your customers who generate 80 percent of your revenues. For digital designers, analog is just the opposite: at best it'll be 10 or 20 percent of your system, but it can absorb 80 or 90 percent of your energies.

Earl Reinkensmeyer, software director for NCR's Microelectronic Products Division (Fort Collins, CO), speculates that the analog portion of a mixed-signal ASIC using NCR's standard cell library, for example,

can add two-to-six man-weeks (at up to \$4,000 or \$5,000 per man-week) to an otherwise routine standard cell design. Part of the reason for this comments NCR product manager Jim Patella, is that the ASIC designer is frequently less sophisticated about analog or mixed-mode simulation. This requires NCR engineers not only to perform the simulations, but also help the customer tune the design to extract the best performance. More often, says Patella, the standard cell design is the starting point for a more-complicated customization project.

A major problem for system designers—especially architecture gurus with largely digital experience—is that analog or mixed-signal designs will force them to get much closer to electronic circuit design than they've likely been before. If you entertain the idea of incorporating the analog portion of your system onto a single ASIC device, along with data converters and digital control logic, you must not only use a different set—but a more complicated set—of design tools. You must also get much closer to the semiconductor fabrication processes than you've been before.

Rather than turning out a GDS-II tape and running it over to the local foundry, your design team will need to get very intimate with your ASIC vendor. This doesn't mean you need to worry about “trenching” or “oxide thickness” or other esoteric concerns of the fabrication expert. But it does require you to understand the differences between linear and digital fabrication technologies—CMOS, BiCMOS and bipolar—and to make appropriate choices between them.

■ Analog demands intimacy

At its heart, analog and mixed-signal design will force you to get intimate with some things digital designers seldom have to deal with; things you may have learned in engineering school and now forgotten, things the engineering schools may not teach anymore—specifically, how do transistors normally behave? and, how do you get them to behave the way you want them to?

At the risk of oversimplifying everything, let me suggest that there's a fundamental split—a Grand Schism—between analog and digital design philoso-

MIXED-SIGNAL DESIGN

phies and implementations. Digital circuits are basically binary counting circuits, which count up strings or patterns of logical 1s and 0s. Analog circuits—and all mixed-signal circuits will have some analog component—are typically control circuits, providing some control over voltage, currents and frequencies.

This paradigm works to the advantage of the digital designer: He can do his work at a high level of abstraction, remaining relatively indifferent to the means by which this circuit will be implemented. As long as the system manipulates data represented as logical 1s and 0s, it makes practically no difference what you use to represent the 1s and the 0s—just as long as your system can distinguish between them at the necessary speeds. Current-generation VLSI circuits use transistors with sub-micron dimensions, switching logic states at 33-, 40- or 50-MHz rates.

A 5-V system uses +5 V (actually, anything above 2.0 V) to register a logic “high” and 0 V (anything below 0.8 V) to register a logic “low.” Actually, it makes no difference to the system’s architect or the logic designer whether you use 5 V, 3.3 V, 100 V or 100 μ V to register a logic high. In IBM’s earliest computers, 1s and 0s were registered by vacuum tubes driving relays. In the 21st century, it’s possible that light pulses or perhaps biochemical reactions, rather than transistor switches, will execute the digital logical functions.

■ Digitally induced isolation

The digitization of the electronics world—a phenomenon covered in *Computer Design’s* 30th Anniversary Issue (January 1991)—has effectively buffered the system designer from electronic design. The most advanced design tools, in fact, maintain a separation between system behavior and function and the structure that implements it. This means that digital ASIC designers can use high-level languages—a C++ construct, Verilog or VHDL; a logic synthesis tool such as Synopsis’ or Racal-Redac’s SilcSyn; or a Boolean algebra construct such as Cupl, Abel or Palasm without knowing or caring whether the logic generated will implement a standard cell ASIC, gate array, FPGA, PLD, or a PCB with CMOS or 7400-series TTL logic.

In fact, you can choose how close you want to be to the implementation. You can farm the VHDL file out to a number of ASIC design centers. You can complete the logic synthesis and optimization, the simulation and timing checks, and turn over an EDIF netlist. You can direct the synthesis toward one semiconductor manufacturer’s standard cell library, or another manufacturer’s FPGAs. You have the option of laying out the circuit using automatic place-and-route-tools and delivering a GDS-II tape to a favorite foundry. There are many silicon foundries offering the same, nearly standardized CMOS processes. (The industry is currently rife with overcapacity.) Alternately, the design can be partitioned for PLDs and JEDEC programming files can be created with PC-based tools. As a digital ASIC designer, you can do as much or as little

as you want of the implementation. But you rarely have to worry about what the transistors are doing.

The major exception occurs where the system/logic designer is intent on pushing “the performance envelope.” This is usually synonymous with clock speed, although large VLSI chips—those with 50,000 gates or more—will force the ASIC designer to examine complex timing relationships, even at moderate clock speeds. Large off-chip fanout loading, or long interconnect lines, might force the logic designer to consider a shift from a CMOS to a BiCMOS process (one that implants large bipolar driver transistors on the same substrate with the smaller-geometry CMOS logic). Here, the designer isn’t really concerned with the current draw of the output transistors, but their effect on critical timing relationships. A large fanout, for example, will increase propagation delays. But problematic gate loading would likely be revealed by a readily-available timing analyzer and could be corrected by the systems designer in the logic optimization phase—that is, before a process switch is required.

Analog design, in contrast, (and any intensive mixed-signal design will require a great deal of attention to analog), forces the designer to get much more involved with the physical means of implementing a function. Invariably, the analog designer wants control of voltages and currents. This forces him or her closer to those devices on the IC that produce voltages and currents—the transistors and connected components, like resistors, capacitors and inductors—and the semiconductor processes used for making them.

■ No one process does it all

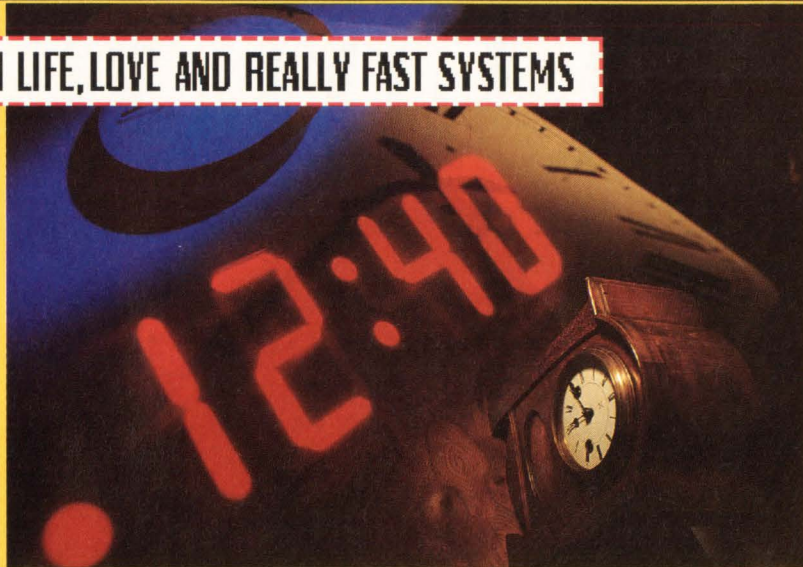
While submicron CMOS is the darling of the digital world because of its combination of speed, packing density and low-power consumption, the analog world will favor entirely different manufacturing processes. There’s no one process which enjoys the universal appeal of digital CMOS. Crossing over to the analog and mixed-signal world, the choices are linear-compatible CMOS (a different process than digital CMOS), BiCMOS (bipolar drivers on a CMOS substrate), and bipolar (the favored process). Even in bipolar realms, there’s a hierarchy among those processes based strictly on npn transistors, and those using complementary npn and pnp. (The latter is favored for high-speed amplifier design.) Dielectric isolation and junction isolation are high-end variations on bipolar processes. For those with high-voltage or high-current requirements, there are processes that combine power transistors on the same chip with control logic—generally known as “smart power” processes. Which process is used is usually dictated by the application requirement.

Stephan Ohr is editor/publisher of the monthly newsletter Mixed Signals.

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Editorial contributions: Tim Wilhelm, Luis Pineda, Ali Mesri and Cynthia Jones.

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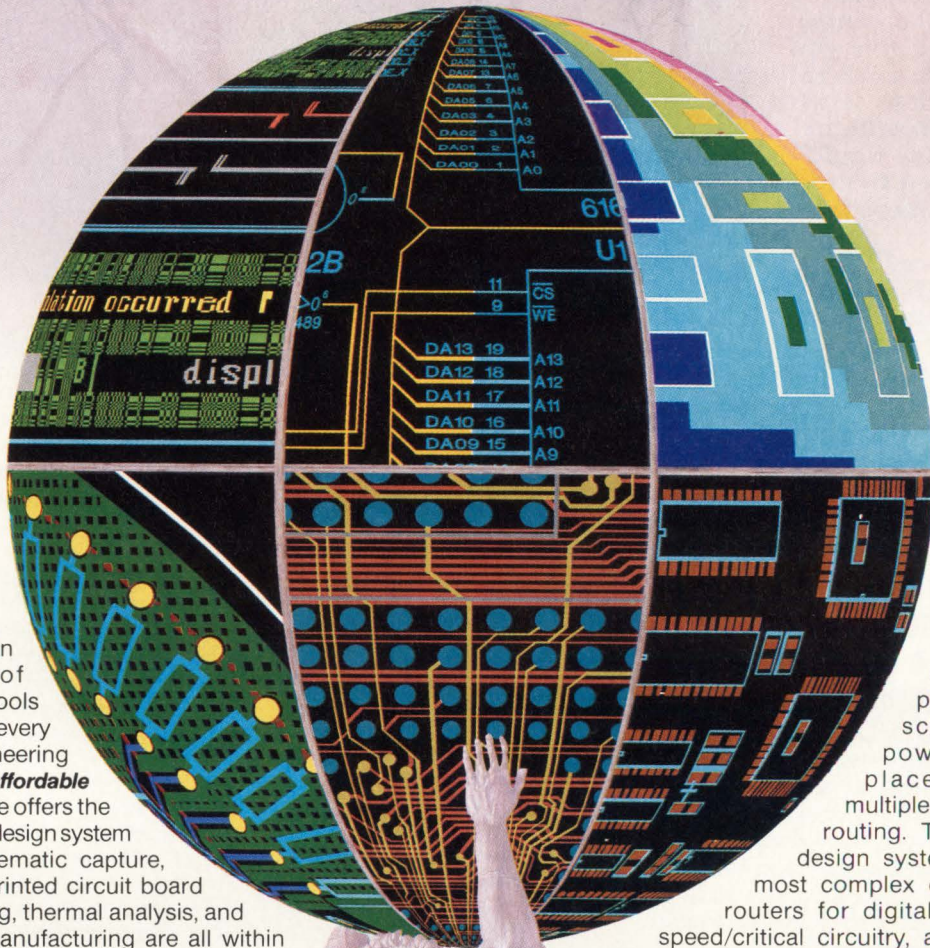
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PLD development tools come of age



It seems only a few years ago that a programmable logic device development tool was merely a software program that translated Boolean logic into JEDEC fusemaps. Devices were simple sum-of-product architectures and the big PLD development tool players were Abel and Cupl. Of course, PLD makers also had proprietary software for their own parts, such as Palasm (Monolithic Memories Inc) and Amaze (Signetics).

As earlier, the personal computer is host to more PLD development tools than all other platforms combined. Unlike earlier, though, is the more widespread use of PLDs in system design. Perhaps 75 percent of all new systems designs contain at least one PLD, with most containing several.

More need is more seed, and pioneering PLD development software from newer companies like Accel Technologies, Isdata, Minc, Orcad, and others have made the market more competitive and forced the older and more-mature players to keep up with the times.

■ Architectures the driving force

Key changes have occurred that make PLDs more popular and forced development tools to be more sophisticated today than ever before. First, parts have become larger to handle more inputs and outputs. Second, I/O lines have become programmable to overcome polarity and register constraints of earlier parts. But most important has been the deviation from the sum-of-products architecture. The generic term FPGA has been coined to describe super PLDs which boast densities up to 20,000 gates, even though many of their architectures in no way resemble a gate array.

The foldback array, for example, used in Signetics and Exar parts is no longer limited to sum-of-products single-level logic. Likewise, the Mach architecture from AMD, the Max architecture from Altera and the UIM architecture from Plus Logic are also capable of multiple levels of logic and deep sequencing, but their architectures more resemble a user-routable circuit board with multiple sum-of-products PLDs. The Xilinx and Actel parts architec-

turally resemble gate arrays but use internal cell programming to determine specific functions.

As a result, earlier PLD development tools just don't have the capacity to handle the 20,000+ gates that can now be replaced by a single PLD. New tools specifically aimed at FPGA design are emerging and combined PLD/FPGA tools capable of minimizing, optimizing, reducing, partitioning, selecting and fitting are bringing PLD and FPGA design development into the mainstream of modern digital circuit design.

■ House of mirrors

It used to be that PLD design tools had one way in (Boolean) and one way out (JEDEC) and specific designs were trapped within the confines of a particular tool. Fortunately, this has been left in the past. Today, Boolean entry is always a given, and every PLD/FPGA development tool still provides this most basic of input techniques. Also, schematic capture is a given, with every major PLD/FPGA development tool providing links into third-party or proprietary schematic capture programs. Other commonalities include truth-table input formats and state machine input formats. Some provide waveform entry and specialized languages.

Since VHDL allows the description of arbitrary digital circuits and contains constructs for timing and simulation, it's an ideal candidate for FPGA design, especially since FPGAs all have unique timing and place-and-route constraints. VHDL provides a very high-level descriptive format, bringing PLD/FPGA design into the ranks of ASIC. What's becoming apparent is that VHDL will become the next input format used for PLD/FPGA development. As an input format, it's interpreted, synthesized and minimized to provide one of the many doors into the PLD/FPGA design world.

Also driving VHDL into PLD/FPGA development is the forthcoming version of Mil-Std-454 which requires VHDL for qualified PLDs and ASICs, and the version following this will require the same for unqualified parts as well.

Also emerging is automated PLD/FPGA and device selection. While initially only Minc and

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Hewlett-Packard provided this capability on an automated level, other vendors are ramping up to make this a seamless and automated task.

While most older and more mature PLD development tools were designed as individual device compilers, today's tools need to handle multiple devices and partition a design. It used to be (and for some still is), that a PLD or FPGA was started with a specific device in mind. The ability to choose a single device or chip sets as alternative approaches is increasingly important as the price premium for using many of today's PLDs and FPGAs is rather high.

This leads to an important trend that has manifested itself—device independent design. Device-independent designs permit the generic logic to be described, compiled, optimized, reduced and simulated before a thought has been given to how the actual design will be implemented. This approach works equally well with PLDs, FPGAs, gate arrays and standard cell ASICs, or even chip sets. As a result, this approach provides a uniform design environment for an engineer who can implement a design in discrete TTL, simple PLDs, complex PLDs, FPGAs, ASICs or any combination of these. Ideally, this also provides the important benefit of migration. With a unified design approach, the same design database can aim at TTL, PLDs and FPGAs for quick, low-cost, low-risk prototyping, design verification, and short- and long-term production.

■ Current tools

While both silicon vendors' and third-party tools are commonly in use, third-party tools are quickly coming to the point where they'll be all that's required. The latest generation of third-party PLD and FPGA development tools utilizes fitters from the silicon vendors. This allows generic software to optimize designs for specific devices. This harmonious arrangement shortens lag time from the new part to product support, increasing the usability and value of the third-party development tools.

The following is a brief overview of four major third-party players that we'll be looking at much more closely in upcoming columns. The products described are listed in alphabetical order according to product names.

■ Data I/O and Abel

Abel from Data I/O (Redmond, WA) is an old-timer that keeps getting younger. Originally a single-PLD compiler, the latest Version 4.0x is a complete rewrite that specifically addresses today's needs. Currently available in two flavors (Abel PLD and Abel FPGA), the latest Abel adds automated device fitting, improved optimization, partitioning, automatic polarity, don't care generation, and device-fitter software modules from PLD vendors. Device-fitter modules let Abel target designs to Actel, Altera, AMD, Atmel, Plus Logic and Xilinx parts.

Abel works best as a module compiler. Here, individual functional blocks are designed and tested. Blocks are combined later to fill the resources of the

devices chosen to house the design. This is primarily because the capacity of Abel is relatively low; it can work with about 500 gates while Abel FPGA can work with about 1,000. Other limitations include a maximum of 25 outputs and 46 product terms.

Abel doesn't support VHDL directly. According to Data I/O, mainstream designers are not yet requiring this. Abel does have indirect links to VHDL through alliances with Cadence and ViewLogic so a customer can satisfy this need today.

Also, the simulator that comes with Abel is a unit delay functional verifier. Timing information for the route dependent devices like the Actel and Xilinx parts must be extracted from within the Actel and Xilinx tools themselves.

■ Logical devices and Cupl

Cupl, like Abel, has been around a long time and has a strong and loyal user base (20 percent of the market). Unlike Abel, Cupl ownership has changed and it's now flying the Logical Devices (Fort Lauderdale, FL) banner.

The current Cupl version 4.2, has matured to meet present day needs. Still supporting its simple and easy-to-use Boolean input format, Cupl also accepts input from third-party schematic capture programs (like Orcad, ViewLogic, and others through EDIF 2.0). Cupl also features simple proprietary syntax format for state machine designs and truth tables. What's more, nested variables, bit field grouping, and index variable features simplify complex equations with common term, address fields and states. In anticipation of need, Cupl also provides VHDL input support.

Keeping up to date, Cupl now supports device partitioning which can automatically split a design into one or more chips. Multiple PLD solutions are supported and the automated device selection accepts user defined constraints such as number of parts in the solution, cost, speed, and erasability. A history-based partitioning scheme is also employed which can reduce the number of different parts needed in inventory.

Device fitters are also used by Cupl which presently supports Actel, Altera, AMD, Atmel, Lattice, National Semiconductor, Plus Logic, and Xilinx.

The simulator that comes with Cupl is a unit delay functional verification tool only. The next release will include timing models which the designer can fill in to include critical path and place-and-route specific-timing information.

Cupl generates data in JEDEC format readable by its own and other programmers. Logical Devices has a functional VHDL output generator module but doesn't plan to release it immediately. This option will be of great benefit for designers who need to generate design information in VHDL form. Here, design information from all input formats are combined, minimized, reduced, and VHDL files are generated.

Cupl boasts a capacity of 50,000 gates, large enough to handle any of today's FPGAs. Presently Cupl supports over 2,500 devices (PLDs and FPGAs) and doesn't offer libraries for migration to gate arrays.

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Logical Devices has its hands full supporting the FPGAs, it does eventually plan to offer gate array migration late in 1992 or 1993.

■ Isdata and LOG/iC

Isdata (Monterey, CA) tools haven't been around as long as Abel or Cupl, and are lower in profile with a smaller user base. Since 1983, however, the LOG/iC family of PLD development systems has been servicing the needs of PLD designers with a slightly different approach.

Like other up-to-date tools, LOG/iC supports device-independent designing, optimization, minimization, partitioning, device fitting, device selection (or recommendations in this case), test vector generation, and documentation. Also like the others, LOG/iC lets different input formats mix and has links to popular third-party design tools.

Unlike the others, Isdata provides a large family of different software programs that tackle different tasks. Designers purchase only the specific modules they require for their needs. As designers' needs expand they add more software modules.

Among the modules are schematic libraries for popular third-party schematic capture programs from Mentor, Orcad, P-CAD, Valid, and Viewlogic. This lets in-place design systems serve as a schematic window into the Isdata software.

In addition to schematic capture, other standard features include Boolean input, truth-table input and state-machine language. A VHDL compiler is now available permitting simulation and synthesis from VHDL source code.

Unlike many other tools, LOG/iC doesn't provide a timing simulator. Instead, a functional verifier which uses unit delays is provided to test the logical concepts and implementation as well as results from optimization and minimization. To get detailed timing verification the company recommends a third-party simulator such as Susie from Aldec which can readily accept JEDEC files.

The current V3.4 of the LOG/iC software adds over 30 new devices bringing to over 400 the specific architectures supported. The latest versions also add device fitters for the newer PLD and FPGA architectures now supporting Actel, Mach, Max, and Xilinx. Gate array libraries for AT&T, Fujitsu, LSI, Siemens, and VLSI are available and net list files can be generated in the appropriate format to pass these designs along to a gate array vendor.

■ Minc and the PLD/FPGA Designers

The Minc (Colorado Springs, CO) PLD Designer was initially introduced in March 1988 and started shipping that May. When initially introduced, it caused quite a stir, because it brought automated PLD design to a new level of sophistication, all on a PC. Now it's integrated with the Mentor design environment (on an Apollo workstation), and is also available on the Sun workstations.

The PLD Designer provides a friendly integrated shell which makes using PLDs very easy, even to someone who has never used PLDs or PLD develop-

ment software before. To an experienced designer, the software lets rapid iterations and tradeoffs be explored and encourages "what if" design optimization.

Currently, the company provides PLD and FPGA Designer packages. Similar in personality and operation, they vary only in capacity, device selection and fitting. Common today, the FPGA Designer takes advantage of device fitters from device makers to best utilized selected devices resources. Presently, Actel, Altera, AMD, and Xilinx fitters are available with more coming.

The PLD Designer claims 10,000 gate capacities while the FPGA Designer claims about 20,000. Both these numbers are highly dependent on the configuration of the PC you plan to use. Both packages require extended memory and a 386- or 486-based machine is highly recommended.

The PLD Designer was among the first to provide an automated and tightly coupled environment for designing, verifying, programming, testing, and documenting PLD designs. The PLD Designer brought together many input formats including standards like Boolean, truth table, state notation, and high-level design language, as well as third-party schematic capture support.

In addition, PLD Designer offers waveform capture as input to synthesize logic, and as input to generate simulation and test vectors. Available now are VHDL input formats which are able to merge with any and all other formats supported.

When all of the design has been entered, PLD Designer performs a logic reduction/factoring pass using options such as factoring techniques, limits to the number of levels of logic and more. The resulting intermediate format is advantageous since now a part can be chosen manually at the last moment, or, automatically partitioned and chosen by the PLD Designer.

Selection constraints for PLD Designer include maximum number of parts, specific manufacturers, package type, technology (CMOS, TTL, ECL), maximum power supply, minimum clock frequency, maximum propagation delay, and more. In addition, each category can be weighed with a factor of importance, further optimizing device selection for a given design. FPGA Designer makes you choose which FPGA you plan to use.

In addition, the PLD Designer integrates a unit delay logic simulator which can test the functional correctness of a design. At this point in time, it doesn't perform timing analysis, so it can be used solely for functionality. It can, however, accept mouse or keyboard drawn test vectors from the waveform entry mode.

Jon Gabay is a free-lance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including High Performance Systems, Engineering Workstations and, most recently, Design Automation.

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What products are attendees designing?

- Within the computer and peripherals industry, designers are concerned with microprocessor architectures, operating systems, mass storage, display technologies, and input/output devices. And with the proliferation of laptop computers, compactness and ruggedness have become critical design and manufacturing issues.
- Within the telecommunications and networking industry, designers are developing new modems, MUXes, bridges, routers, etc. for LANs and WANs. They're concerned with protocols, standards, and physical and link layer solutions in silicon, modules, and at the board level.
- Within the process control and factory automation industries, data acquisition, motion control and robotic systems are being designed. Many of these are microprocessor based board-level systems and rely heavily on data converters, machine vision, and power handling subsystems.
- Within the military and aerospace industry, engineers are designing fault-tolerant systems, radiation-hardened computers, and hardware that meets appropriate emission specifications. These systems make heavy use of fiber optics and secure interconnects, EMI/RFI suppression techniques, and advanced packaging techniques.
- Consumer electronics engineers are designing low-cost systems that rely on automated assembly, clever packaging, and test—all at the lowest possible cost. Future applications such as HDTV and multimedia will play a major role in the revitalization of the U.S. electronics industry.

What's the focus of the Technical Program?

SysComp/92-West is a three-day systems-oriented conference and exhibition with opportunities for presentations on a wide variety of OEM system-level design and integration topics. **SysComp/92-West** is intended to bridge the information gap between passive/discrete component shows such as Wescon, and VAR/VAD/end-user exhibitions such as Comdex. The program will combine lectures and tutorials (of varying length) on a broad array of topics critical to the timely and cost-effective evaluation, selection, development and integration of major system components—both hardware and software. Several key areas of concern will be addressed in the Technical Program:



- Microprocessor/system architectures, and their impact on OEM integration.
- Bus architectures, including VMEbus, Multibus II, ISA/EISA, MicroChannel, and Futurebus+ bus, and their impact on OEM integration.
- Power sources, including developments in switching technologies, converters, and batteries, with emphasis on their relationship to the size, cost and manufacturability of electronic/computer products.
- Display and interface technology, including advances in hardware, hardware/software interfaces and graphical user interfaces.
- Mass storage technology and the impact of new developments in media (disk, tape, optical), interface standards, and controllers on system performance, cost and reliability.
- Embedded software programming, with an emphasis on realtime kernels, standards and development tools.
- System packaging, including EMI/RFI control, thermal management, and designing for manufacturability.
- Concurrent engineering and achieving cost, quality and time-to-market goals.

You are invited to submit proposals for presentations in the above areas of interest, addressing specific topics such as:

Microprocessor architectures and their impact on subsystem design.
Nonvolatile memory and its applications.
The system costs of microprocessor selection.
Embedded PCs as building blocks.
Backplane bus performance and selection.
Next-generation bus architectures.
Design for testability and built-in self test.
Distributed power systems.
FDDI and other high-performance interfaces.
Battery technology and its impact on portable system design.
Cost vs. performance tradeoffs in displays.
Emerging mass storage technologies and the impact on system design.
High-density cartridge tape drives.
Fault-tolerant and mission-critical software.
Advances in printed circuit board technology and impact on test and manufacturing.
Software quality control and maintenance.
Controlling EMI/RFI and EMI/RFI standards.
Cost/performance alternatives in electronic packaging.
Evaluating power supply performance vs. cost.
High-density packaging and interconnects.
ICs for power distribution and management.

Applications of "smart power" technology.
Flat panel display design, manufacturing, cost, yield and integration.
Optimizing quality through concurrent design.
Power-management schemes.
Power supply reliability.
Quick turnaround techniques for multi-chip module development.
Shock, vibration and reliability issues in hard disk drives.
Optical disk technology and operating systems.
Ruggedized system design.
Standards for real-time operating systems and kernels.
Trends in embedded software and software-development tools.
System considerations when moving to SMT.
Testing and evaluating disk drives.
Display specifications and choosing a display.
Design-for-manufacturability strategies and solutions.
Choosing the most cost-effective manufacturing process and contract manufacturing.
Using multichip modules to shrink product-development time.
Thermal management and system cooling.

How can you participate?

If you or your organization would like to participate in the **SysComp/92-West** Technical Program, submit a brief proposal to the Technical Program Coordinator no later than **November 8, 1991**.

Proposals should be 1- to 1 1/2-pages in length and contain a one-paragraph abstract that summarizes the content and goals of the presentation and a brief outline of the major topics that would be covered in the presentation. Presenters must be technically qualified and able to answer questions from attendees. A short biography of the presenter, describing his or her technical background and accomplishments must accompany the proposal.

Acceptance of proposed presentations will be made by November 15, 1991 and a complete copy of the presentation, including all visuals and graphics, will be required no later than **December 31, 1991**.

Presentations given at **SysComp/92-West** will be published in a Proceedings and copyrights shall be assigned to *Computer Design*.

For more information or to submit a proposal contact:

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Technical Program Coordinator
COMPUTER DESIGN
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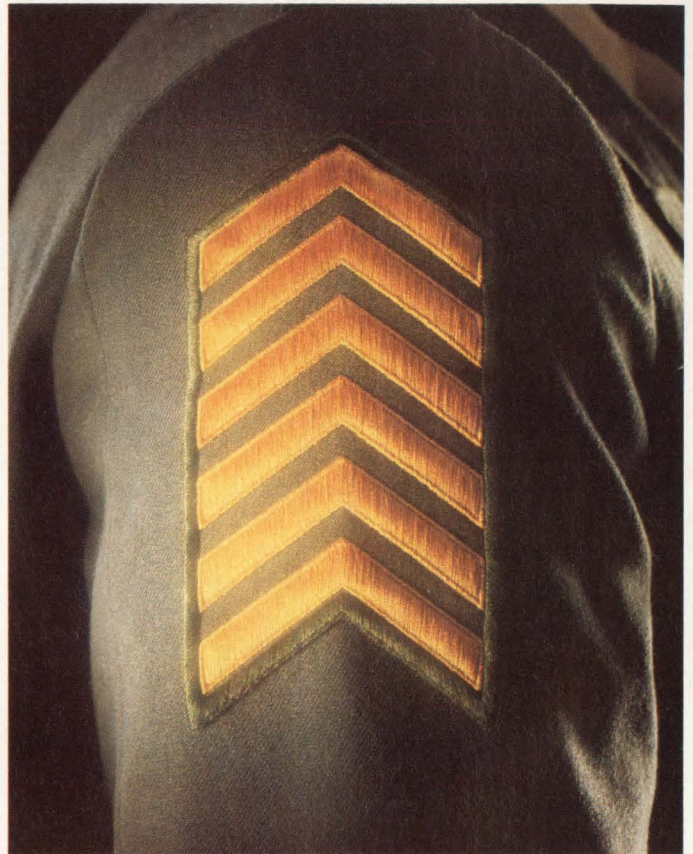
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In addition to the technical program, **SysComp/92-West** will feature exhibits by vendors of OEM computers, ICs, CPU boards and other board-level products, mass storage devices, displays, power sources, backplanes and enclosures, software and software development tools. For information about exhibiting at the conference, contact:

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Computer Design magazine will be publishing the **SysComp/92-West Conference Guide**. In addition to distribution at the conference, the Guide will be mailed with the February, 1992 issue of *Computer Design*. For information about advertising contact:

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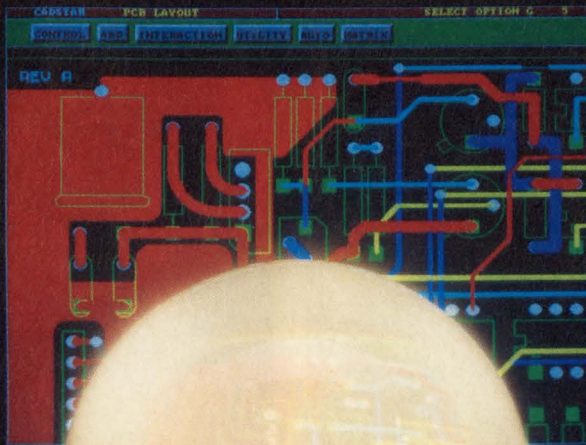
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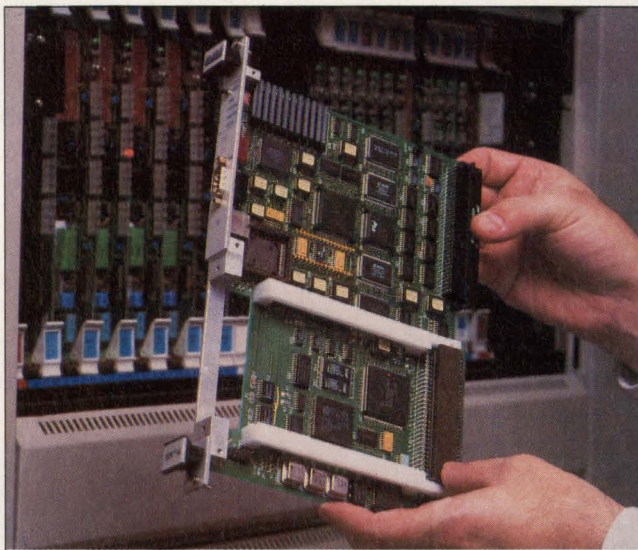
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CIRCLE NO. 73

INTEGRATED CIRCUITS

Cost, voltage and standards issues retard acceptance of flash

Jeff Child, Associate Editor



The density and ruggedness of flash drove designers at Radisys, a manufacturer of embedded PC boards, to use it on their EPC-6 controller. They wrote software that lets flash memory appear as another disk drive.

Since its invention in 1983, flash memory has evolved, from initial concept to 2-Mbit parts, faster than any other memory semiconductor. The key benefit of flash is in providing designers with non-volatile memory that can be reprogrammed without removing it from the circuit. While the same benefits are possible from either EEPROM or battery-backed SRAM, flash memories are less expensive than either of these solutions. Dataquest figures project the total flash market to reach \$1.5 billion by 1995. While flash memories are expected to capture new design wins, as densities increase and prices fall, designers remain reluctant to use them.

Three uses for flash

In general, designers are most likely to be interested in flash for one of three reasons: as a replacement for EEPROM or battery-backed SRAM; as a solid-state disk, to replace a hard disk; or as a replacement for standard UV-EPROM in low-chip count embedded applications.

Today, flash has found its way into many applications including cellular telephones, medical instruments and as a storage area for BIOS in personal computers. A few systems are already using flash as a solid-state disk, replacing a hard disk as the mass storage device. The fastest growing area where flash is being used is in PC memory cards.

Now in a standardized form factor, memory cards are expected to benefit from the high volumes associated

with the rapidly growing portable computer market. Of all the memory semiconductors available today, flash is the most appropriate for memory cards. "As far as user modifiable memory is concerned, there's really only two choices: battery-backed SRAM or flash," says Bill Densham, director of PC enhancements at Poqet Computer (Santa Clara, CA). "At the same density, however, SRAM is more than two times the cost. End-users love flash because it has a great cost/performance ratio in terms of dollars/Mbyte. But it needs to get much lower." Densham was the engineering manager that brought Poqet's first computer to market. Poqet's computers depend on memory cards for their operation.

At first blush, flash memories appear suited for any application that requires EPROM density and EEPROM's ability to be reprogrammed without removal from a system. Flash memories available today are based on the technology of either EPROMs or EEPROMs, with price and capabilities falling between the two. Upon close examination, however, designers are finding that using flash has drawbacks. While most agree that flash faces a bright future, many current and potential users of flash are reluctant about designing flash into their next product.

What's behind this skepticism? One reason is the lack of second sources. Many designers are frustrated at the slow rate at which flash memory manufacturers are

setting standards for flash. And while most makers of flash chips are now using a standard pinout, manufacturers have yet to firmly agree on any standard method for programming flash memories. Furthermore, many designers expected flash prices to have fallen below EPROM prices by now, but have been disappointed. Although flash prices continue to drop, they are still far above EPROM prices. Finally, many designers who would have used flash in their design haven't because of flash's 12-V requirement for reprogramming.

Wanted: Standards

Radisys (Beaverton, OR) made use of flash memory in its line of embedded PCs for VMEbus. It used 1-Mbit flash chips from Intel (Folsom, CA) in the design of one of its daughterboard modules—a solid-state disk in a 3-x6-in. form factor. Although the Intel 1-Mbit flash satisfied the design requirements for size and ruggedness, Radisys designers didn't like being tied to a single source. "The flash manufacturers have done a very poor job at standardization," says Steve Cooper, director of sales at Radisys. "Each flash chip is slightly different. Each uses a different programming method. That means that we can't switch to another vendor's chip without a board re-layout. So you're committing to a single source. It's unfortunate that there's been so much in-fighting."

For designers at Vocal Technologies (Santa Clara, CA), a manufac-

■ **PRODUCT FOCUS/Flash memories**

Model	Organization (bits)	Read access time (ns)	Write time per byte (μ s)	Power consumption	Program/erase voltage (V)	Endurance (cycles)	Packaging options	Price	Comments
Advanced Micro Devices 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088-3453 (800) 222-9323 Circle 301									
Am28F256	32k \times 8	90	10	30mA/100 μ A	12	1,000	DIP, PLCC	\$12.10 (100s)	—
Am28F512	64k \times 8	90	10	30mA/100 μ A	12	1,000	DIP, PLCC	\$15.05 (100s)	—
Am28F010	128k \times 8	90	10	30mA/100 μ A	12	1,000	DIP, PLCC, TSOP	\$22.05 (100s)	automatic program and erase operations
Am28F020	256k \times 8	90	10	30mA/100 μ A	12	1,000	DIP, PLCC, TSOP	\$39.15 (100s)	same as above
Atmel 2125 O'Nel Dr, San Jose, CA 95131 (408) 441-0311 Circle 302									
29C256	32k \times 8	120	156	80mA/300 μ A	5	1,000	DIP, LCC, PLCC, TSOP	\$11.40 (100s)	single supply 5V read and write, 64-byte page write and erase
29C257	32k \times 8	120	156	80mA/300 μ A	5	1,000	DIP, LCC, PLCC, TSOP	\$11.40 (100s)	same as above
29C010	128k \times 8	120	78	50mA/100 μ A	5	1,000	DIP, LCC, PLCC, TSOP	\$26.50 (100s)	single supply 5V read and write, 128-byte page write and erase
Catalyst Semiconductor 2231 Calle de Luna, Santa Clara, CA 95054 (408) 748-7700 Circle 303									
CAT28F512	64k \times 8	200, 250	10	50mA/500 μ A	12	1,000	PDIP, PLCC	\$11 (1,000s)	bulk erase, speed programming
CAT28F512V5	64k \times 8	200, 250	10	120mA/100 μ A	5	1,000	PDIP, PLCC	\$29 (1,000s)	sector erase
CAT28F010	128k \times 8	120, 150, 200	10	30mA/100 μ A	12	1,000	PDIP, PLCC	\$18 (1,000s)	bulk erase, speed programming
Dense-Pac Microsystems 7321 Lincoln Way, Garden Grove, CA 92641-1428 (800) 642-4477 Circle 304									
DPZ128M8Y	131 \times 8	120, 150, 200	25	50mA/20 μ A	12	10,000	Stacked LCC module	\$60 (100s)	available December '91
DPZ1024X16H3	1M \times 16	120, 150, 200	25	55mA/320 μ A	12	10,000	Stacked LCC module	\$550 (100s)	same as above
Exel Microelectronics 2150 Commerce Dr, PO Box 49038, San Jose, CA 95161-9038 (408) 432-0500 Circle 305									
28F256	32k \times 8	120	250	30mA/1mA	12	10,000	PDIP, PLCC, TSOP	\$8.50 (100s)	Intel-compatible, samples available now
28F010	128k \times 8	120	250	30mA/1mA	12	10,000	PDIP, PLCC, TSOP	\$14.85 (100s)	Intel-compatible, samples available May '92
Hitachi America, Semiconductor & IC Div 2000 Sierra Point Pkwy, Brisbane, CA 94005 (800) 448-2244 Circle 306									
HN29C101	128k \times 8	120, 150, 200	200	30mA/20 μ A	12	10,000	PDIP, TSOP	\$15.50 (100s)	single pulse erasing and programming with status polling
HN28F101	128k \times 8	120, 150, 200	25	30mA/20 μ A	12	10,000	PDIP, PLCC, PSOP, TSOP	\$14.50 (100s)	command mode interface, automatic chip erase with status polling
Intel 1900 Prairie City Rd, Folsom, CA 95630 (916) 351-8080 Circle 307									
28F256A	32k \times 8	120, 150, 200	10	10mA/50 μ A	12	10,000	CDIP, PLCC	\$7.25 (10,000s)	—
28F512	64k \times 8	120, 150, 200	10	10mA/50 μ A	12	10,000	PDIP, PLCC	\$8.30 (10,000s)	—
28F010	128k \times 8	120, 150, 200	10	10mA/50 μ A	12	10,000	PDIP, PLCC, TSOP	\$12.80 (10,000s)	—
28F020	256k \times 8	150, 200	10	10mA/50 μ A	12	10,000	PDIP, PLCC, TSOP	\$19.50 (10,000s)	—
iSM001FLKA	512k \times 16	120, 200	16	20.3mA/0.4mA	12	10,000	SIMM	\$137.50 (1,000s)	standard 80-pin module
28F001BX	128k \times 8	120, 150	15	30mA/100 μ A	12	10,000	PDIP, PLCC, TSOP	\$16.65 (10,000s)	block erase, automated algorithms, SRAM-compatible write interface

OEM PRODUCT UPDATE

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CIRCLE NO. 75



LBP-LX Laser Beam Printer Engine

A compact, affordable printer engine ideal for desktop applications. Utilizes the disposable EP-L cartridge. Available in both Video (external OEM controller) and PCB (internal OEM controller) models.

Monthly prints: 750
Resolution: 300/400 dpi
Print Speed (PPM): 4
Dimensions: 16.7"W x 14.1"D x 7.6"H

LBP-SX



The most popular laser beam printer in the world. Clamshell top cover permits easy access to paper path and disposable EP-S image cartridge. Available in Video and PCB models.

Monthly prints: 5000
Resolution: 300/400 dpi
Print speed (PPM): 8
Dimensions: 18"W x 19.5"D x 9.1"H

LBP-TX and LBP-RX



Hard-working laser beam printers featuring expanded paper handling. The RX model offers duplex capability. Dual cassettes hold up to 400 sheets and two types of paper. EP-S cartridge in all versions. Available in Video and PCB models.

Monthly prints: 5000
Resolution: 300/400 dpi
Print speed (PPM):
TX Simplex 8
RX Duplex 7 (impressions)
Dimensions: TX 18"W x 19.5"D x 12.5"H
RX 18"W x 25.0"D x 12.5"H

LBP-20



A heavy-duty laser beam printer for large-format printing. Modular design allows multiple product configurations.

Monthly prints: 30,000
Resolution: 300/400/480 dpi
Print speed (PPM):
Simplex: Letter 20
11" x 17" 10
Duplex: Letter 14 (impressions)
11" x 17" 8 (impressions)
Dimensions: 29"W x 24"D x 20"H

LBP-DX



Our largest-format laser beam printer. Outputs high-quality photographs, halftones and line art prints on vellum or paper. Ideal for engineering and graphics production. Handles 500-foot rolls of 24" wide paper or cut sheet sizes up to D (24" x 36").

Monthly prints: 5000
Resolution: 400/508 dpi
Print speed (PPM):
D size (24" x 36") 3
C size (18" x 24") 5
Dimensions: 30"W x 39"D x 46"H

PRODUCT FOCUS/Flash memories

Model	Organization (bits)	Read access time (ns)	Write time per byte (μ s)	Power consumption	Program/erase voltage (V)	Endurance (cycles)	Packaging options	Price	Comments
Mitsubishi Electronics America 1050 E Arques Ave, Sunnyvale, CA 94086 (408) 730-5900 Circle 308									
M5M28F102	64k \times 16	100, 120, 150	10	30mA/1mA	12	10,000	DIP, PLCC, SOP, TSOP	\$21 (100s)	automatic erase with status polling
M5M28F101	128k \times 8	100, 120, 150	10	30mA/1mA	12	10,000	DIP, PLCC, SOP, TSOP	\$21 (100s)	same as above
SGS-Thomson Microelectronics 1000 E Bell Rd, Phoenix, AZ 85022 (602) 867-6100 Circle 309									
M28F256	32k \times 8	100	10	30mA/100 μ A	12	10,000	CDIP, PDIP, PLCC	\$7 (1,000s)	—
M28F512	64k \times 8	100	10	30mA/100 μ A	12	10,000	CDIP, PDIP, PLCC	\$9 (1,000s)	—
M28F1001	128k \times 8	80	10	30mA/100 μ A	12	10,000	CDIP, PDIP, PLCC, TSOP	\$16 (1,000s)	—
M28F1024	64k \times 16	80	10	30mA/100 μ A	12	10,000	CDIP, PDIP, PLCC, TSOP	\$18 (1,000s)	—
M28F2001	256k \times 8	80	10	30mA/100 μ A	12	10,000	CDIP, PDIP, PLCC, TSOP	\$25 (1,000s)	—
Toshiba America Electronic Components 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000 Circle 310									
TC58257-20/-25	82k \times 8	200, 250	1ms	30mA/100 μ A	12	100	DIP, SOP	\$4 (100s)	—
TC58F1001-15/-20	128k \times 8	150, 200	125ms	30mA/100 μ A	12	100	DIP, SOP	\$8 (100s)	block erase, available Q192

turer of portable modem systems, cost was the reason that replacing 1-Mbit ROMs with 1-Mbit flash memories didn't make sense. Its application would require a flash chip with 100- μ A standby power consumption, 100-ns access speeds, in a 330-mil SOP, according to Fred Hirzel, president of Vocal. And with a total system cost of \$200 to contend with, the flash memory used would have to be priced much lower than any available today. And while flash would enable the modem to be upgraded in the field, such a feature would be too costly. "What's the point of putting in features that are expected in an \$800 modem when, at \$200, you could send it back and get another one instead of upgrading?" asks Hirzel.

One critical issue in designing with flash parts is the high voltage required to program them. Most flash memories need a 12-V source for programming. Whether this is a problem or not depends on the application. Many systems have 12-V

sources available anyway and for those that don't, there are voltage conversion techniques that can be employed. In the case of portable systems, though, where low power is a key issue, 12-V supplies are out of

One critical issue in designing with flash parts is the high voltage required to program them.



the question. Many memory card applications fall into this category. Since 12 V is impractical in portable systems, users generally cannot make changes to the flash memory card while they're on the road.

Not all flash memories require a 12-V programming source. Atmel (San Jose, CA), Catalyst Semicon-

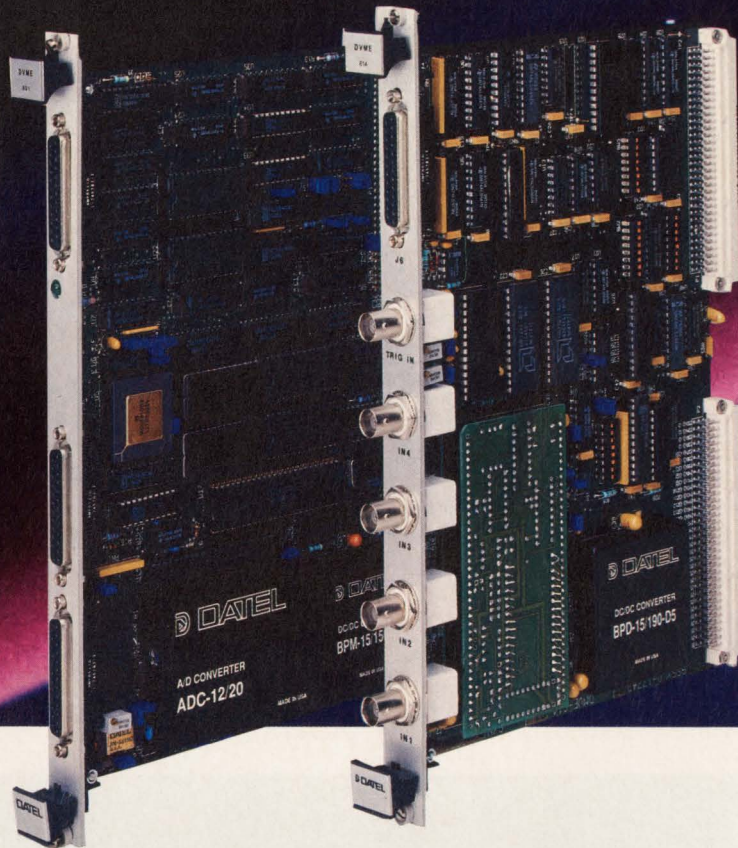
ductor (Santa Clara, CA) and Texas Instruments (Dallas, TX) all offer flash devices that generate the necessary programming and erase voltages internally. As a result, these parts only require 5-V supplies for programming. Unlike other flash memories, however, these parts have two transistors per cell, rather than one. This results in a bigger cell, making the chips more expensive than if they were based on single-transistor cell flash architectures.

Atmel's 29C010 is an example of 5-V flash. This 1-Mbit device offers a page-write cycle feature which includes automatic erase and takes only 10 ms to complete the cycle. With 128 bytes in a page, in effect each byte writes in roughly 78 μ s. In comparison, other flash memories take about 10 ms to write each byte. The 29C010 writes, therefore, about 1000 \times faster than other flash parts.

Because the 29C010 is programmed one page at a time, it's not necessary to write the whole chip at once. If desired, only a small amount

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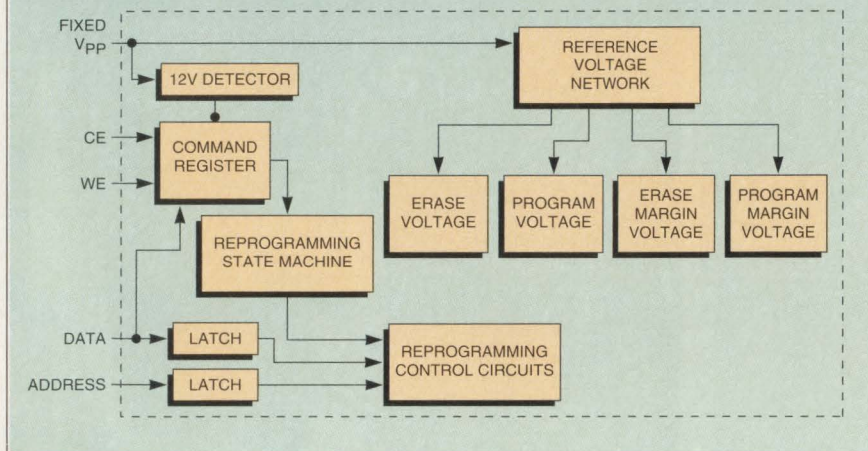
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Command register architecture for direct microprocessor interface



Created by Intel, this command register architecture is emerging as the de facto standard for flash memories. Other vendors, such as AMD, currently offer flash devices that use this architecture and others are following suit. When flash vendors settle on an official standard, designers won't have to risk becoming stuck with one vendor.

of the code can be updated. This is particularly useful when part of the flash contains code that shouldn't be overwritten, like the system's operating kernel, for example.

Flash evolves

The flash market that has developed has not evolved as an EPROM-replacement market, observes Marlene Hudson, product marketing manager for memory components at Intel. "With pricing that we've given flash, we haven't really positioned it as a replacement for EPROMs," says Hudson. "Designers that don't require frequent updates to their code should use an EPROM."

While Hudson declined to comment on Intel's strategy for future flash products, their current products hint that Intel's roadmap for flash will lead in two directions. One of these will be toward increasing density of flash memories for use in PC-memory cards. Last October, Intel introduced

When considering DSP, take



INTEGRATED CIRCUITS

its own flash memory card, which contained the industry's first 2-Mbit flash chips in TSOPs (thin small-outline packages).

Intel's other focus will be on flash memories for minimum chip embedded applications and for up-dateable BIOS in PCs. The 28F001BX, Intel's latest flash offering, exemplifies this trend. Also called a "boot-block" flash, this 1-Mbit device features an 8-kbyte boot-block section. This section has a hardware lock-out feature to ensure data security and integrity. The remainder of the chip is partitioned into two 4-kbyte parameter blocks, and one 112-kbyte main block. Available in two configurations, the device is compatible with microprocessors that boot from high memory, such as the 80486 or i860, or those that boot from low memory, such the i960KA/KB or Motorola's 68000 family.

In the last few months, some of

the decisions that designers have to make about flash have become easier, according to Steve Grossman, director of marketing for memory products at Advanced Micro Devices (Sunnyvale, CA). "Last year there was a lot of concern about which flash part to use," says Grossman. This situation improved somewhat last September when AMD started offering flash parts with an Intel-like command register architecture. Now, several other vendors appear to be headed in the same direction. When a de facto standard is settled on, many expect a second tier of flash vendors will enter the market and become compatible sources for flash. ■



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CIRCLE NO. 77

Two-chip set implements C-bus II spec

Following hard on the heels of its popular C-bus multiprocessor bus architecture, Corollary has debuted its next-generation design. Dubbed C-bus II, it's a fully symmetric bus designed to support multiple buses in a single system. To speed the creation of products based on the archi-

backplane bus capable of transfers up to 250 Mbyte/s. The bus can support 16 modules, each of which can support up to two CPUs.

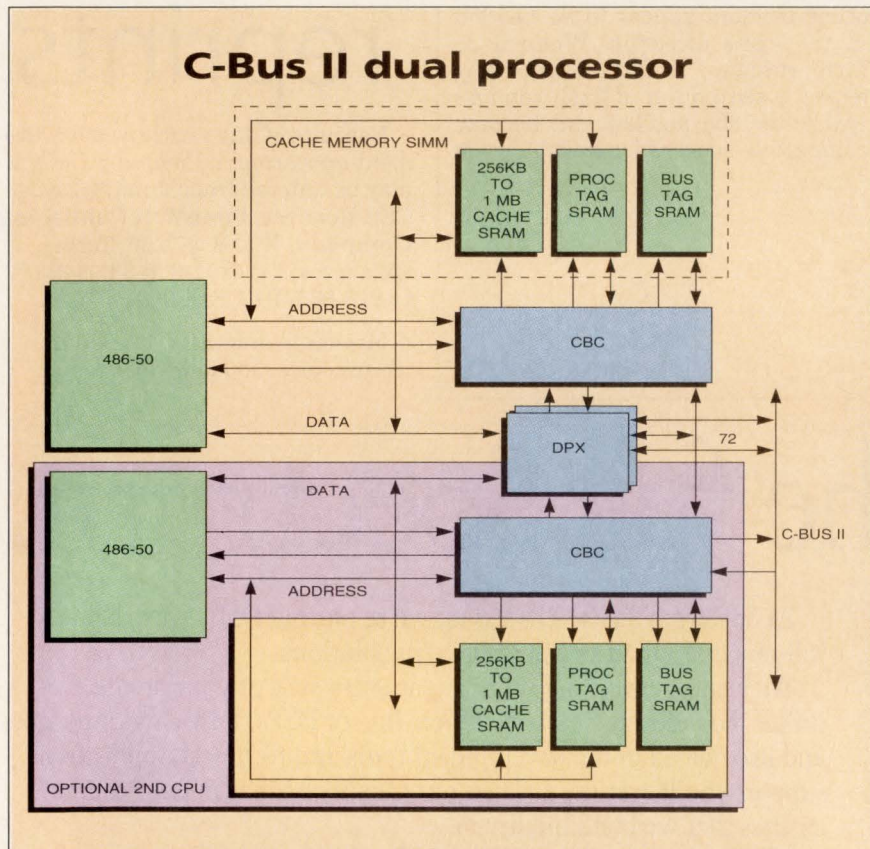
C-bus II has only six types of memory transactions to simplify the design of boards based around it. The four cached memory transac-

implemented in two ICs: a cache bus controller (CBC) chip and a data path exchange (DPX) chip. One CBC and two DPXs are required per single CPU board. The CBC provides integrated cache and bus management control facilities and interfaces directly to the 486. The DPX interfaces to the C-bus II. Together, these chips can support a direct-mapped second-level cache of 256k to 1 Mbyte, along with the 486 internal cache. In addition, a built-in third-level cache inside the DPX prevents cache evictions on common tasks such as block moves.

Because of the few chips needed to implement a system, designers can put two CPUs and their caches on a single board, as shown. Simpl normally consists of one CBC and two DPXs. A two-CPU board requires two CBCs and two DPXs as well as a second cache RAM and cache tag memories. Support for other processors is on the way. As a member of ACE (Advanced Computing Environment), Corollary says it will build a future version of the chip set to work with MIPS processors as well.

The system software for Simpl, developed by Corollary, is the SCO MPX kernel and is available from the Santa Cruz Operation (SCO). It's a modification to the standard Unix kernel that provides fully symmetric operation. The SCO kernel automatically detects the number of processors and spreads the work load over those processors, while retaining binary compatibility with SCO Unix.

— Dave Wilson



It doesn't take much to build dual 486 multiprocessing hardware using Corollary's C-bus II. Just two 486 processors, two cache bus controllers and two data path exchange ICs form the heart of this C-bus II dual-processor system.

itecture, the company has announced that it will sell a two-chip implementation of the C-bus specification dubbed Simpl (Symmetric Integrated MultiProcessor Logic).

C-bus II doesn't compete with industry standard buses such as EISA or MicroChannel. Rather, C-bus II is a cache memory bus only, designed to bridge to other buses so that a complete system can use one of them for I/O. The backbone of the C-bus II architecture is the C-bus II itself, a multiplexed, synchronous, 64-bit

tions include read, evict, read exclusive, and evict exclusive; the two I/O transactions are I/O read and I/O write. C-bus II also supports split transactions to prevent slow devices from consuming large amounts of the bus bandwidth. There are also split memory transactions for particular memory-mapped devices with caches.

An initial version of the Simpl chip set provides an interface between 50-MHz 486s and C-bus II. The entire C-bus II specification is

C-bus II at a glance

- Fully symmetrical processor support
- Up to 30 logical CPUs on the bus
- SCO MPX kernel support
- Multiplexed synchronous 64-bit data path
- 250-Mbyte/s burst transfer

Corollary
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Circle 351

As design engineers and managers you know that the higher speeds and greater complexity of electronic systems are making your jobs more challenging. As clock speeds climb to 50MHz and beyond, analog characteristics become major considerations for digital designs. In addition, demands for mixed-signal technology have increased in the consumer, automotive, and telecom markets. According to Technology Resource group, 40% of all ASICs will be mixed analog and digital by 1994.

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Comm chip set handles Ethernet and token ring

ChipsLAN is the first LAN chip set capable of handling both Ethernet and token-ring protocols. Two CMOS ICs comprise a multiprotocol LAN controller (the 82C581) and a multiprotocol LAN serial interface (82C585). They're designed to work with an Intel-compatible NEC V30H microprocessor that handles the media access control (MAC) services and other data-control functions such as protocol handling and DMA. In an Ethernet environment, the ChipsLAN devices support media rate data transfer between network media and host memory. For token ring, they can provide data transfer rates up to 20,000 (64 byte) frames/s. They support Ethernet on thick-, thin- and twisted-pair media and token ring on shielded and unshielded twisted-pair cables.

The 82C581 interfaces to an 80386 local bus or an AT bus. It communicates with a host CPU via a shared window in a private memory space and is designed so it can function as a bus master while

transferring data directly between host memory and the network. It also manages a FIFO data buffer of programmable size between 256 bytes and 64 kbytes, which can compensate for varying system bus latency.

The 82C585 multiprotocol LAN serial interface chip provides the interface between the physical network media and the 82C581. LAN selection is achieved under software control. The 82C585 has an attachment unit interface (AUI) for 10Base-5, 10Base-2 and has a built-in 10Base-T transceiver. Built-in Manchester encoder/decoder and constant-gain phase-locked loop (PLL) circuits provide the decoding and recovery of clock and data for receiving and the encoding for transmitting. Software pre-equalization and a second selectable PLL for jitter reduction on token ring are also built-in.

Two Application Programming Interfaces (APIs) are provided. The host application programming in-

terface (HAPI) is the software interface used by the host processor to communicate with the 82C581 and 82C585. A communications processor application programming interface (CPAPI) lets users' programs share the V30H processor that executes firmware implementing MAC layer functions. Such programs are written in assembly language and can provide product differentiation through such features as added network management capabilities or on-board processing. Software drivers to interface ChipsLAN to Netware, LAN manager and NetBIOS are also provided by Chips and Technologies.

The ChipsLAN chip set will be available in sample quantities by the end of the fourth quarter. Prices for the product will be set at that time. The 82C581 will be packaged in a 208-pin PQFP and a 68-pin plastic-leaded chip carrier. The 82C585 will be packaged in a 120-pin PQFP.

—Dave Wilson

ChipsLAN at a glance

- First Ethernet/token ring chip set
- Built in 10Base-T interface
- Software programmable configurations
- Built-in V30H interface
- Full duplex operation

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Placement evaluator predicts PCB routability

Automated PCB design tools often meet their match when they're faced with a complex placement and routing task. As a result, experienced designers scoff at the idea of using an automated tool for such a critical part of a circuit board's design. One of the main complaints about these tools is its lack of intelligence when placing components on a board. The resulting route can take an inordinate amount of system time to complete and sometimes produces an inefficient and expensive design.

Valid Logic Systems hopes to answer some of these complaints with the Allegro Placement Evaluator, a

because the rats nest rarely has any relationship to routing constraints," says Tom Leonard, member of the technical staff at Valid. "To perform a realistic evaluation, a designer must consider the things that a router will use during the route, like design rule checking, otherwise you're not really evaluating a placement for routability."

Using the Insight router parameters, feature sizes (tracks, vias and pads), actual spacing, and electrical constraints as inputs, the Placement Evaluator creates a density report as a color map that's overlaid on the routing channels. Each color

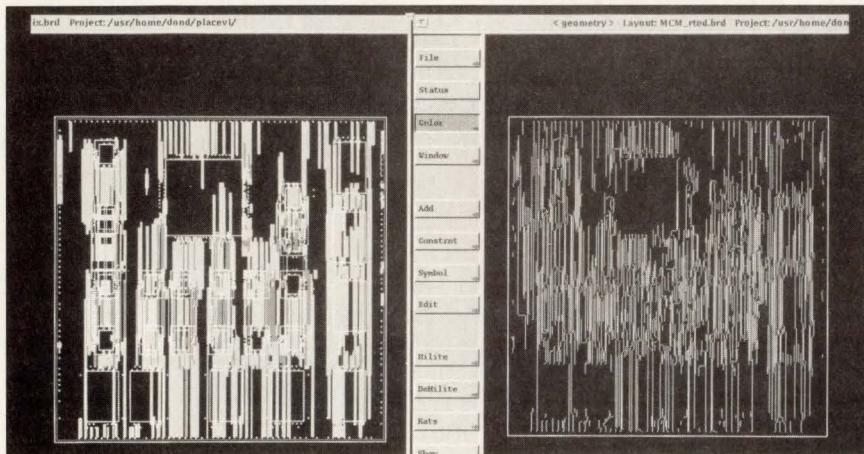
Valid's figures, a six-layer design costing about \$102 a board could be routed on four layers costing \$71.68 per board.

Valid has also enhanced its Insight routing system with more than 3,000 new rule options within the expert system, which let it recommend router sequences that utilize the algorithms more efficiently. The router's grid calculation capabilities include a direct path option that forces it to seek the straightest path with the fewest vias. Among the new algorithms that have been added are a new pattern router and a delay router that routes high-speed signals to user-specified delay values.

The Insight router assists in parameter-setting and ensures that the system's multiple routing algorithms (costed maze, pattern, delay, rip-up, and retry) are sequenced and used efficiently. Users specify a few directives, such as spacing rules and line widths, and Insight sets the routing parameters to provide an efficient route.

Both the Insight router and the Placement Evaluator are part of Valid's Allegro 5.0 PCB design tool suite. Allegro is available on Sun, Digital and IBM workstations and is priced from \$12,000 to \$50,000, depending on configuration.

—Mike Donlin



Based on many of the parameters and design rules used by the PCB router, Valid's Placement Evaluator can test a placement for routability after layout. As shown in this photo, the Placement Evaluator's predicted route densities (left image) closely follow the actual route patterns executed by the automatic router (right image).

tool that automatically analyzes the routability of PCBs, multiwire boards, hybrids and multichip modules (MCMs). The tool can analyze designs of up to 48 signal layers and highlight potential trouble spots where excessive nets are likely to contribute to congestion. Using this data, a designer can perform "what-if" analyses to determine the optimum placement of a design for routability by Valid's Insight router.

According to Valid, the Placement Evaluator is different from competitive tools that are based solely on manual interpretation of histograms representing rats nest density. These tools require an engineer to judge routability based solely on this visual information. "The traditional approach is often inaccurate

represents a density range and colors are assigned to overflow areas—locations where there are too few available channels for the router to complete the number of projected connections. In addition, a trace map can identify the nets most likely to travel through congested areas. This lets designers evaluate the routability of a design during various stages of component placement and experiment with different placement set-ups.

Considering alternatives

Tradeoffs such as increasing the number of layers, moving components versus swapping pins and comparing etch widths against various numbers of layers can be evaluated during layout. According to

Placement Evaluator at a glance

- Automatically analyzes routability of PCBs, multiwire boards, hybrids and MCMs
- Analyzes designs up to 48 layers
- Creates density report as a color map overlaid on routing channels
- Colors are assigned to overflow areas where routing is impossible
- Runs on Sun, Digital and IBM workstations
- Part of Allegro 5.0 which sells for \$12,000 to \$50,000 depending on configuration

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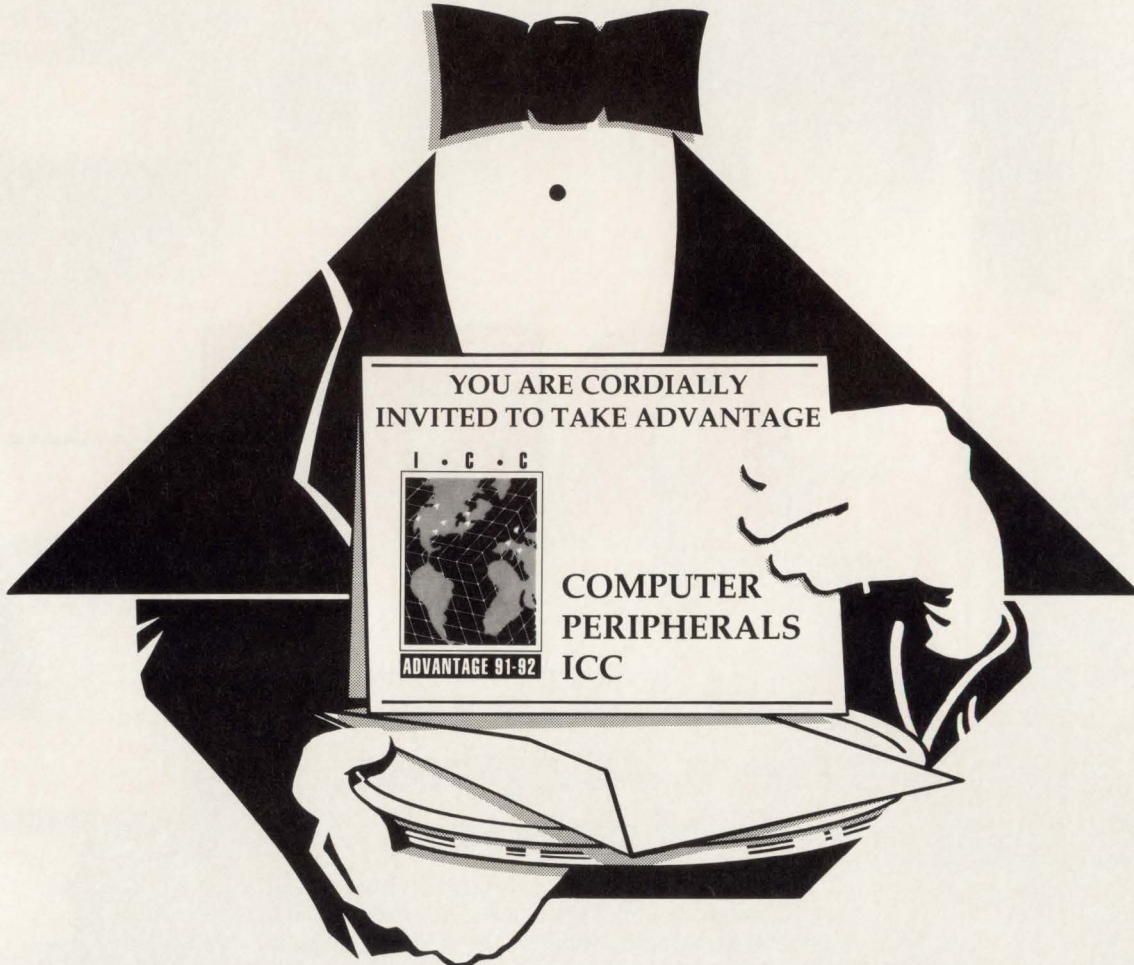
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CAE/CAD TOOLS

VXI-based test system targets application-specific solutions

A VXIbus-based system called S760VXI from Schlumberger Technology tackles traditional bottlenecks in instrument interfaces via a dual operating system, framework-based approach. A dual-processor design, the S760VXI provides real-time program execution and control of VXI instrumentation through a 25-MHz 68030 processor and a VXI slot 0 controller.

According to Schlumberger, the degradation of data manipulation processes, which is customary in single-processor systems, is eliminated by providing real-time computational capability in the same chassis as the VXI instruments. Two operating systems, Unix and VxWorks, let each perform tasks for which it's best suited. In addition, real-time distributed processing at

the backplane provides more accurate and synchronized measurement timing than the use of traditional IEEE 488 or MXI interfaces.

The newly introduced system functions within Schlumberger's Computer-Aided Test Engineering (CATE) framework, which provides a range of interactive point tools for test management and program development. For mixed-signal testing, a new tool, the Instrument Workbench, has been introduced into CATE. The Instrument Workbench is an object-oriented, graphical environment for managing, programming and debugging VXIbus and IEEE instruments.

The S760VXI is priced from \$75,000.

—Mike Donlin

S760VXI-based tester at a glance

- Hosts a 25-MHz 68030, slot 0 controller
- Real-time distributed processing eliminates instrumentation interface bottlenecks
- Two operating systems, Unix and VxWorks, each perform tasks for which it's best suited
- All systems operate within the CATE framework—a bidirectional design-to-test link which provides interactive point tools for test management.
- S760VXI system is priced from \$75,000.

Schlumberger Technology

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Circle 354

There's a Better Way to Develop Compatible Real-time Cross and Target Code.



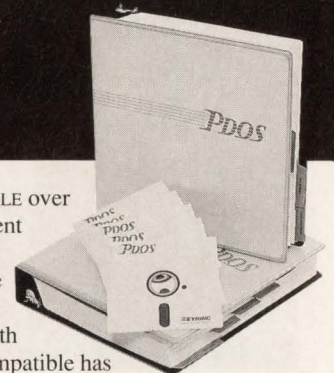
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CIRCLE NO. 84

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Tool eases GUI design for OS-9 and OS-9000 embedded control applications

A window-based ROMable user interface system for real-time and embedded applications running under the OS-9 and OS-9000 operating systems lets users design not only text-based user interfaces, but color graphics-based control panels with custom gauges, controls and indicators as well. The GS-9 system from Gespac, (Mesa, AZ) is designed especially for the real-time multitasking character of OS-9 by Microware (Des

Moines, IA) window consists of a frame and several "gadgets," graphical elements that are used to pass information to an application or to dynamically display the state of a variable. Basic gadgets move and resize a window, reduce it to an icon or terminate the application that's running in the window. Each window supports full VT-100 terminal emulation so that any OS-9 program normally written for a text terminal will run under

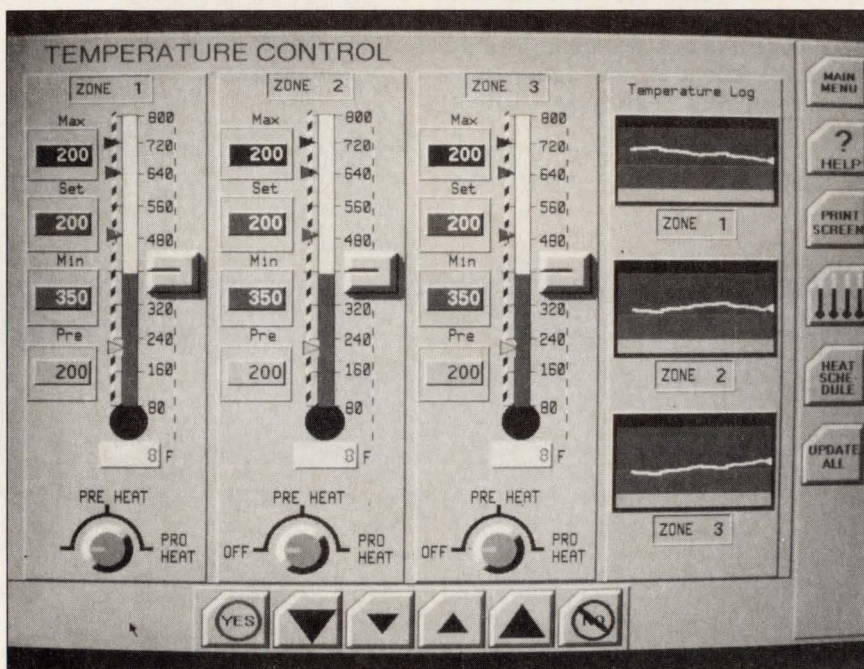
and colors; raster image-based toggle buttons and LEDs; single pen strip chart; radio buttons, X-boxes, needle gauges and many more. In addition, a versatile, configurable X-Y plot gadget lets the user set up dynamic plotting of data in a wide choice of formats. Gadgets appear to a C program as standard C structures.

For input gadgets such as buttons, toggles or slider controls, applications programs are alerted to user input via callback functions. A C function within the applications can be named from within the G-View editor or at run time. The gadget will automatically call the C function when the user clicks the mouse on the gadget.

G-Windows is hardware independent because it's supported by a number of VME and G-64 bus boards. It supports resolutions up to 1280x1024 pixels on color monitors and also Gespac's GESVIG-4 LCD panel controller. When used under OS-9000 on an 80386 or 80486 system, it requires a VGA display.

G-Windows is priced at \$2,950 for the G-View development environment. Each application requires a run-time copy of WFM which licenses for \$250 in single quantities with substantial volume discounts.

—Tom Williams



G-Windows permits flexible and easy design of user interfaces for embedded control systems. A library of "gadgets" to represent gauges and controls can be easily customized to suit an application's need, then linked to a control application program.

Moines, IA). It consists of three major components: a window file manager (WFM) and library, along with a graphics I/O manager and its support library; the G-View application editor, used for the design of graphical user interfaces; and G-Desktop, which acts as a general file manager and user interface for OS-9.

The WFM and its libraries are at the base of G-Windows. The G-View application builder uses WFM and its graphics and I/O libraries as the building blocks for custom user interfaces and WFM forms the basis of the G-Desktop shell—itsself a G-Windows application. A basic win-

G-Windows unmodified.

G-View is the application used to develop G-Windows user interfaces which are then integrated into application programs. The main tools for doing this are the edit window and gadgets. With the edit window, a user may set up static graphic elements such as text, raster images, lines, boxes, circles, arcs, etc. The user can also bring in gadgets from a growing gadget library supplied by Gespac, make new gadgets by combining existing gadgets, or write custom gadgets. Gadgets supplied by Gespac include: single bar graph with multiple limit regions

G-Windows at a glance

- Fully ROMable
- Runs on OS-9 and OS-9000 on 680X0 systems and under OS-9000 on 386/486 systems
- Full multitasking, all windows can be updated at once
- Support for multiple fonts, including Japanese
- Window file manager only 160 kbytes
- Library of customizable gadgets for user interface design
- Runs on a variety of color or monochrome graphics boards

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The MVC's advanced features benefit both the integrator and programmer. Port and VMEbus parameters are soft-configured and set line-by-line. Modem control is standard. Full software support is also included,

along with diagnostics and a Streams driver.

Advanced memory architecture and high-speed buffering eliminate overruns and port domination. Memory is expandable from 128KB to 1MB, so the MVC handles today's requirements and future application needs.

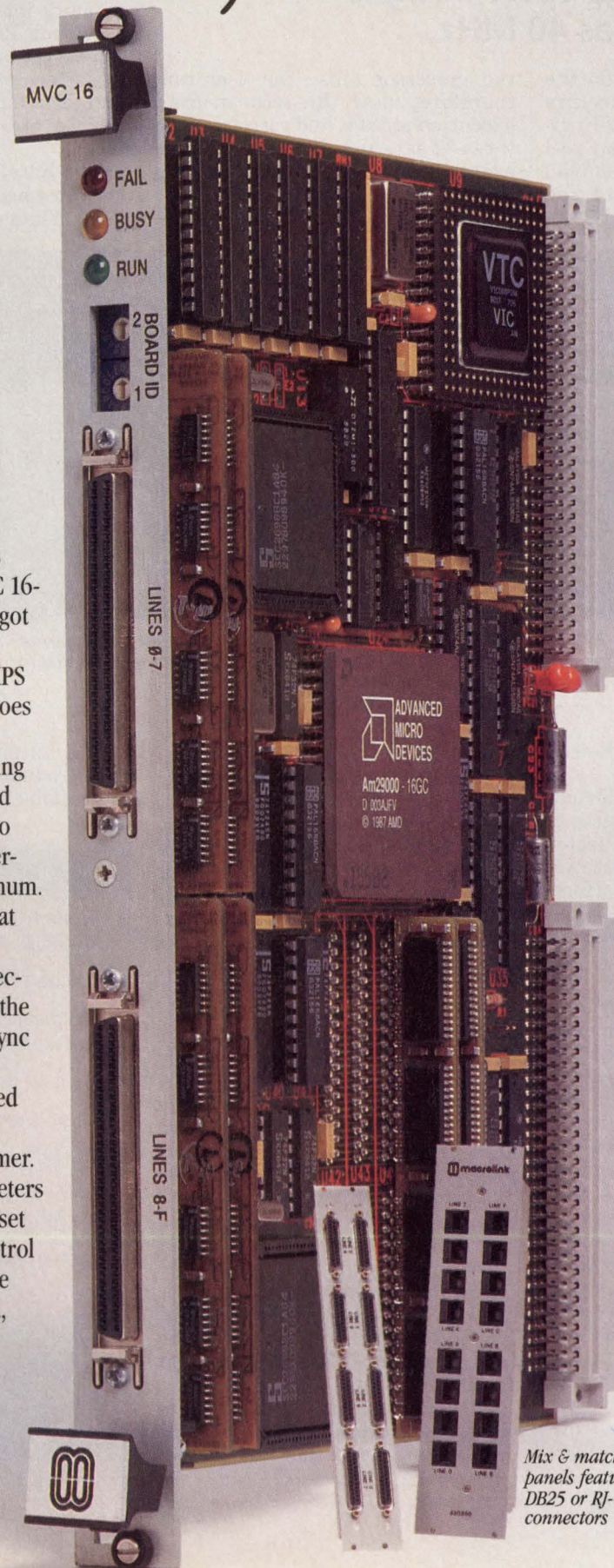
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Emulator debugs Sparc designs running as fast as 40 MHz

The first in-circuit emulator for the Sparc RISC processor architecture has been introduced by Step Engineering (Sunnyvale, CA). The Excel 930 supports the Fujitsu MB86930 Sparclite implementation of the Sparc architecture. The Excel 930's hardware-debug features let the designer bring up initial hardware requiring only power and a clock signal to begin testing. Nonintrusive operation up to 40 MHz is assured by repartitioning the debug elements with the user command program and the use of a specially designed cable. The target processor remains in the system while it's executing code and passively monitors processor bus activity and records it in an 8k-deep trace memory.

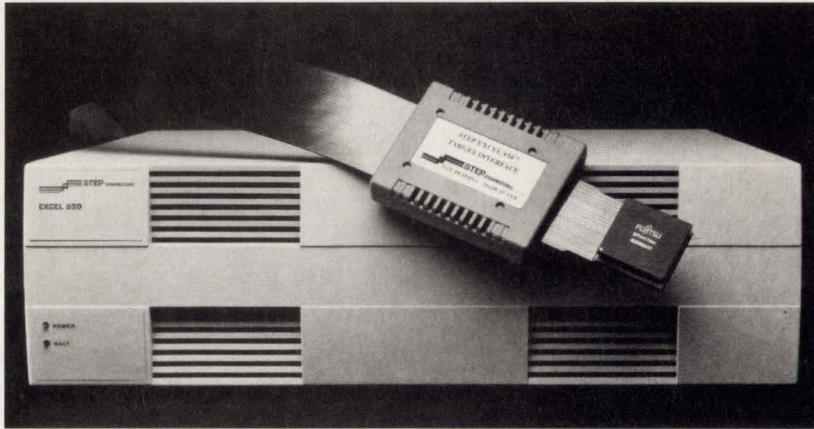
The 930 is hosted by an AT-compatible PC via a parallel interface. The parallel interface allows faster download of code to the target system than the usual serial interface, as well as higher throughput when debugging. The 930 also has an Ethernet interface for remote debugging and to let the designer communicate with the emulator from nonhost workstation environments, including Sun-4 workstations.

The Excel 930's trace buffer can be configured as either 8k×160 bits or 32k×256 bits. In addition to tracking activity on the processor's bus and control pins, the emulator can monitor 32 external inputs and correlate them with each bus cycle. A 48-bit time tag is used to mark each trace cycle for exact time correlation. For more complex triggering and breakpoint logic analysis, the 930 contains both trigger-in and -out connections.

The 32 external inputs can monitor and trace any signal on the target and are captured into the trace buffer along with the signals from

the processor pins. The user can, therefore, view the reconstructed execution stream and correlate it to these 32 external signals to examine events leading up to or resulting from program execution.

The Excel 930 includes a feature



The Excel 930 is hosted on an AT-compatible PC but also includes an Ethernet interface for remote debugging from networked workstations. It's the first in-circuit emulator for the Sparc RISC architecture.

essential for today's highly integrated microprocessors—the ability to reconstruct the execution stream from on-chip cache memory. By using the control information supplied by the Sparclite processor along with software developed by Step, the emulator can trace the execution of programs with the cache on. The designer, therefore, can debug code that may run entirely within the chip's 4 kbytes of on-chip cache.

The Excel 930 supports multiple hardware and software breakpoints. The five hardware breakpoints can be set up for instruction address, data address, data value or external-range break conditions. The two data address breakpoints can be configured as data address and/or a combination of address and value or a data address and value range. The hardware breakpoints will trigger on data-write values out-of-range. The 16 software breakpoints can be set by putting halt instructions at specified locations.

A system expansion bus is provided for addition of future product enhancements. Such future en-

hancements include a high-speed memory interface that lets designers debug ROM-resident code when the target isn't yet fully functional, a performance analysis package, and logic analyzer features such as multilevel triggering and store control.

The Excel 930 emulator provides an interface to the X-Ray source level debugger from Microtec Research (San Jose, CA). X-Ray permits debugging of optimized C code in a window environment. Among other things, it can start and stop execution with complex software breakpoints at both the C source and assembly level and monitor data variables at each breakpoint. It also provides an on-line C interpreter for source-level code patching without the need to leave the debug session and recompile.

The Excel 930 is being offered at an introductory price of \$15,875 and is available 60 days ARO.

—Tom Williams

Excel 930 at a glance

- Nonintrusive operation up to 40 MHz
- Cache execution trace
- Hardware and software breakpoints
- 32 user-defined inputs
- Logic analyzer interface
- X-Ray source debugger interface
- Remote debugging capability via Ethernet
- System expansion bus
- 8k or 32k trace buffer

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Board offers high-performance DSP for STD bus

One of the industry's first general-purpose STD digital signal processors—and the unqualified first STD 32 board—offers OEMs a wide selection of I/O options for either a stand-alone, single-board computer or as an intelligent control coprocessor board. Based on the 27-MHz DSP56001 processor from Motorola (Austin, TX), Ziatech's ZT89CT30 DSP board is designed to perform specialized signal processing operations as well as I/O management of a high-speed serial interface. The only other STD DSP board offering comes from WinSystems (Arlington, TX) and features the AT&T DSP32C floating-point processor.

As an I/O control processor communicating with a master processor on the STD or STD 32 Bus, Ziatech's DSP board talks to the master through designated I/O addresses. Eight I/O-addressed registers in the DSP chip are mapped into a jumper-selectable location in the main system's I/O address space.

Multiple DSP boards can be used in a single system for added processing power by jumpering each board so that it's selected when addressed at a unique set of 16 I/O addresses. The DSP chip occupies the first eight addresses and the on-board, slave-priority-interrupt controller redundantly occupies the second eight. The processing of the DSP chip isn't impaired by the master CPU's access to these addresses, nor is it put on hold during these accesses. The registers inside the DSP chip act like dual-port memory, buffering the chip from process interruption.

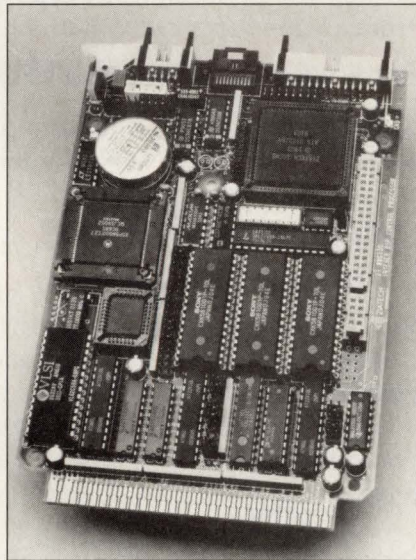
The 56001

The heart of Ziatech's board is Motorola's 24-bit 56001 DSP. Its instruction set is geared to perform DSP algorithms for processes such as fast Fourier transforms, digital filters, signal correlations, vision processing, and other mathematical functions that can take advantage of fast integer arithmetic.

One advantage of the 56001 with a 24-bit data path rather than the 16-bit data path of most other integer processors, is it provides a full 144 dB of dynamic range. Since intermediate results are held in 56-bit accumulators, it offers over 330 dB

dynamic range for intermediate results. The wide dynamic range is useful in many signal-filtering applications as well as in audio- and speech-processing applications.

Though the power behind the DSP board is its processor, the flexible I/O makes it useful in a broad variety of applications outside of traditional DSP. The board offers a serial channel (with an RS-232 or RS-485) which may be synchronous or asynchronous



Ziatech has produced the industry's first STD 32 board. The ZT89CT30 DSP is designed to perform more than just specialized signal processing operations.

and jumpered to be DCE or DTE. In the asynchronous mode, a clear-to-send input is available.

A 24-bit parallel I/O interface uses Ziatech's proprietary interface IC to connect an Opto 22 rack to the board using an adapter card or special cable. These bidirectional I/O signals can sink up to 12 mA when configured as outputs and have 100k- Ω pull-up resistors. In addition to the serial and parallel I/O, the board includes an iSBX expansion interface socket so OEMs can customize the card for specific applications.

The interface uses either 8- or 16-bit data and has limited DMA support. The iSBX can be interrupt/DMA driven and can execute much faster than other SBX interfaces if the software programs let the DSP chips have fewer wait

states. The iSBX socket supports hundreds of conventional iSBX, off-the-shelf modules, or for highly specialized applications, OEMs can tailor their own options.

Multiple options

Ziatech's ZT89CT30 is available with a variety of options including a high-capacity, back-up battery for the on-board SRAM; I/O cables; an iSBX prototyping board; and a number of memory selections. The 56001 has a 32-word (words are 24 bits in the 56000 word) bootstrap ROM for loading the user's application from the on-board PROM or the master CPU on the STD bus. The DSP chip also has a 512-word program memory and preprogrammed ROMs with ulaw and A law to linear expansion tables and a full, four-quadrant sine-wave table.

Three JEDEC 32-pin sockets for static RAM will accept either 32- or 128-kwords of SRAM which lets users store up to 32 kwords of program instructions and 48 kwords each of X-address data memory and Y-address data memory. To achieve zero-wait states, 32-kbyte parts must have access times less than 25 ns while 128-kbyte parts can slide by with 35-ns access times.

Available for immediate delivery, the ZT89CT30 is priced at \$1,050 in single quantities. A development kit including the board, 128 kwords of SRAM, the debugger, and downloader is priced at \$1,450.

—Warren Andrews

Ziatech's ZT89CT30 DSP board at a glance

- Motorola 56001 DSP
- Up to 128 kwords (24-bit) SRAM
- 24-bit parallel I/O port
- iSBX connector
- Serial port RS-232 or RS-485
- 144-dB dynamic range

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VME board hosts 12 DSPs

In compute-intensive applications, such as telecommunications and neural networking, a lot of floating-point processing has to occur as one chunk of data gets passed from one processor to the next. With this in mind, Communication Automation & Control has announced the VME9U12, a VMEbus board sporting 12 32-bit floating-point digital signal processors. The VME9U12 delivers a peak performance of 300 MFlops and 150 Mips. The board can act either as a VMEbus master or slave.

At the heart of the board are 12 of AT&T's DSP32C processors. Each DSP has its own local memory comprising 128 or 512 kbytes of zero-wait-state SRAM. Each DSP executes programs and accesses data out of its own local memory area.

The VME9U12 is offered with two daughterboard options. The T1D, a

T1 interface, sends demultiplexed T1 data to the VME9U12 and receives multiplexed data from the board. The T1D can accept differential clocked nonreturn to zero (NRZ) data. The card also supports Alternate Mark Inversion (AMI) data, so it can be interfaced directly with a T1 line.

The second daughterboard, called the C12, includes 12 8-bit companding codecs (coder/decoder). The codecs support both μ Law (the non-linear companding formats for the United States) and A law (the corresponding European format). The C12 also provides 12 balanced I/O channels. The I/O gain for each channel can be programmed independently of one another.

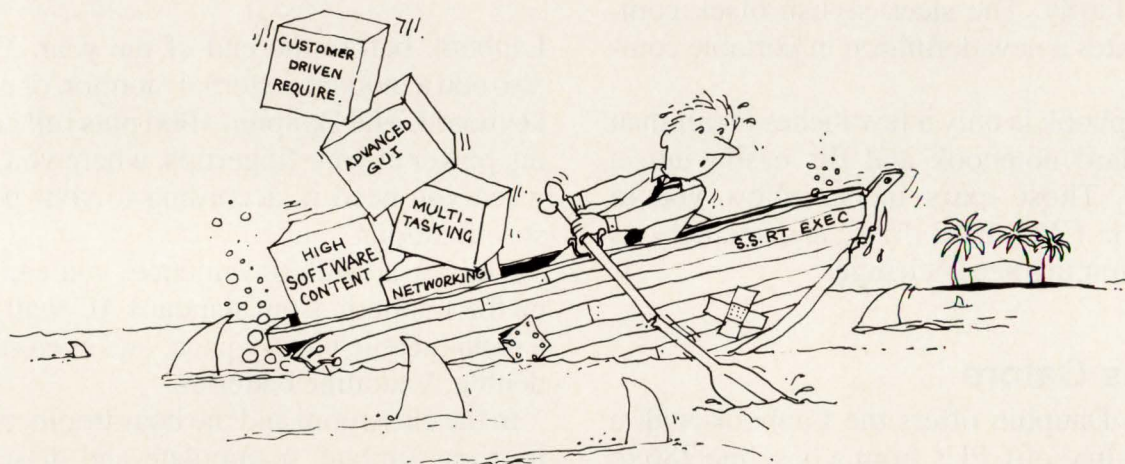
A matter of timing

The 12 DSP chips talk with each other and the daughterboards

through four on-board buses. Called time-division-multiplexed (TDM) buses, these serial interfaces operate at 16 Mbit/s. Time division multiplexing lets each bus carry data to and from multiple sources simultaneously. Each bus consists of a programmable number of time slots, each of which may be 8, 16 or 32 bits wide. Frames can contain a single or up to 128 time slots. The TDM bus is also available at three expansion ports, allowing multiple VME9U12 boards to be linked.

Through the T1 daughterboard, the TDM buses can be clocked internally or externally. Running at 16.384 MHz, the internal clock can be divided by 1, 2, 4, 8, or 10. The T1 clock operates at the standard T1 clock rate of 1.54 Mbit/s.

Any device (DSP, codec or T1 interface) can transmit data to any or all of the TDM buses during any number of time slots. Likewise, any device can receive data from any of



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the four TDM buses during any number of time slots. The source and destinations for each time slot can be reconfigured during the board's operation.

The four TDM buses are multiplexed onto the DSP's serial I/O pins. Six local controllers on the board determine which bus is tied to the DSP's I/O pins during any particular time slot.

The six controllers receive configuration information for each time slot from a centralized TDM serial bus controller. This controller consists of a dual-port RAM and a microsequencer. The host computer writes the TDM map configuration to one side of the bus controller's RAM. The microsequencer then broadcasts eight 16-bit words via a parallel bus to each of the six controllers. Configuration information is also broadcast to the codec daughterboard and TDM expansion buses.

A library of C-callable functions let designers configure the board from within their applications. The commands enable designers to produce functions that control the TDM buses. Examples of such functions include uploading/ downloading TDM configurations to/from RAM, initializing the TDM controller and changing a device's source/destination status.

Additional software support for the VME9U12 includes an AT&T C compiler, applications library and

Unix driver. Also included is a screen-oriented C source-level debugger.

Available now, the VME9U12 is priced at \$13,100 with two DSPs and 256 kbytes of SRAM per DSP. It's also available for \$18,800 with 12 DSPs and 128 kbytes of SRAM per DSP. The C12 codec daughter-

board costs \$3,500. The T1D daughterboard costs \$2,000.

—Jeff Child

Compact SCSI / Enet

Mizar's new MZ 8554 packs maximum I/O into minimum VME space.

The newest addition to Mizar's expanding line of 3U VMEbus boards is the perfect solution for your system I/O needs. The MZ 8554 provides intelligent, high speed SCSI and Ethernet interfaces based upon the latest IC technology. Designed for superior system performance, both interfaces provide direct memory access to on-board memory. In addition, both interfaces can execute command sequences independently of host processor intervention, freeing your main CPU from time consuming low-level protocol handling.

The economical alternative to expensive two board solutions, the MZ 8554 meets high-performance I/O requirements for both single-height and double-height VME systems. And, the MZ 8554's price can't be beaten! Support for the MZ 8554 includes drivers for both Microware's OS-9™ and Wind River Systems' VxWorks™ Real-Time Operating System.

The MZ 8554 is the perfect complement to Mizar's extensive line of 3U CPU's and other peripheral boards. To find out why more and more engineers are turning to VME boards from Mizar, call today.

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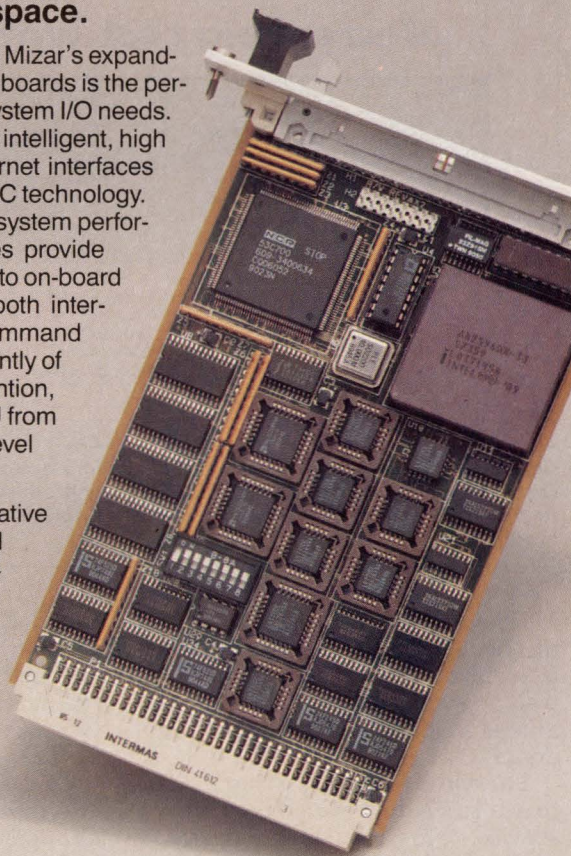
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VME9U12 at a glance

- 12 32-bit floating-point DSPs
- 300 Mflops, 150-Mips performance
- Up to 512 kbytes of local SRAM for each DSP
- T1 and codec daughterboards
- VMEbus master or slave
- Four 16-Mbit/s TDM buses link DSPs, codecs and T1 interface
- TDM bus links multiple boards

Communication Automation & Control

1642 Union Blvd, Suite 200
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Circle 359

Mask-programmed device integrates up to 40 EPLDs

The Altera N-to-1 mask-programmed logic device can merge up to 40 erasable programmable logic devices that have been used for prototyping and early production into a single MPLD for volume production. Proprietary logic synthesis software guarantees pin, function and timing compatibility between multiple EPLDs and the single MPLD that replaces them, according to Altera.

scripture language or waveforms—can be implemented without manual design partitioning. After the design is partitioned, designers can program EPLDs for board-level prototyping and then convert to a single masked device to reduce board space, decrease power consumption and lower the cost of the multiple-EPLD solution.

A special logic synthesis program

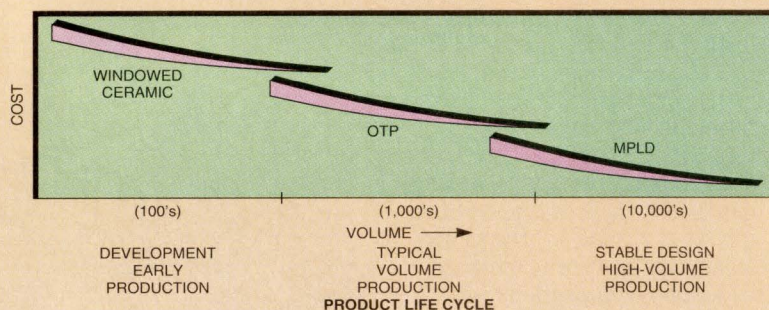
Altera is looking at other foundries. Altera is offering N-to-1 MPLDs as masked options for all of its high-density EPLDs, including members of both Classic and MAX 5000 EPLD families. MAX 7000 family MPLD conversions will be added sometime this quarter.

Design conversion cost for an N-to-1 MPLD varies between \$20,000 and \$60,000, depending on design size. Unit cost for N-to-1 MPLDs vary depending on the size of the design but averages about six cents per macrocell. A design, for example, that combines half a dozen EPM5032 devices (32 macrocells per device), according to Altera, could be placed into an MPLD with a unit price of \$11.50.

Delivery for prototype units is six weeks after final design sign-off. Production units are delivered 10 to 12 weeks after prototype sign-off.

—Barbara Tuck

Decreasing cost with volume



An Altera customer might choose to have MAX+PLUS II automatically partition a design into multiple windowed-ceramic EPLDs for development, then switch to less costly one-time programmable EPLDs for early production, and finally (to reduce cost further) move to either multiple MPLDs or a single N-to-1 MPLD for large volume production.

Moreover, a partial-scan-based test methodology, which detects faults associated with asynchronous, as well as synchronous circuitry, guarantees at least 95 percent fault coverage.

The conversion path from EPLDs to Altera's N-to-1 MPLD is a turnkey service. After debugging a design, a user submits design files to Altera for final sign-off and package selection. Altera then converts the design, generates test vectors, analyzes timing, and delivers prototypes within six weeks.

The multipart partitioning capabilities built into Altera's PC-based MAX+PLUS II logic development software, which runs under Microsoft Windows 3.0, facilitate the conversion path from EPLDs to the N-to-1 MPLD. With MAX+PLUS II, a logic design of over 50,000 gates—described in schematics, hardware de-

scribed in schematics, hardware description language or waveforms—can be implemented without manual design partitioning. After the design is partitioned, designers can program EPLDs for board-level prototyping and then convert to a single masked device to reduce board space, decrease power consumption and lower the cost of the multiple-EPLD solution. A special logic synthesis program called EMC (EPLD-to-MPLD Conversion) matches the timing between the multiple-chip EPLD and the single-chip MPLD implementations. Altera guarantees that the MPLD will meet the worst-case timing of the multiple-EPLD design. Testability software, based on partial scan techniques, embeds scan-test logic into the design and automatically generates test vectors. The testability scheme detects faults associated with register control logic such as register preset, clear and clock logic. Craig Lytle, strategic marketing manager for MPLDs, says that so far, Altera has averaged 98 percent fault coverage on 30 MPLD designs. Of the 30, only one was a purely synchronous design.

Though users would presently be locked into the single foundry Altera uses for its MPLDs, Lytle says that

N-to-1 at-a-glance

- High-volume, low-cost version of EPLD
- Pin-/function-/timing-compatible with EPLD
- Automatic design for testability
- DIP/PGA/PLCC/QFP package options available

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Fault simulator uses cycle-based algorithm

The ADAS fault simulator from start-up ADAS Software employs a proprietary algorithm based on parallel differential fault simulation to achieve fast simulation time and reduce hardware memory requirements. With the new fault simulator, engineers can verify test coverage on a desktop workstation without an additional hardware accelerator, according to ADAS. The fault simulator, which handles gate-level as well as mixed gate- and transistor-level designs, accepts a standard gate-level netlist and test vectors and then generates diagnostic reports to help users identify undetected, potential detect and solid detect faults.

The ADAS fault simulator takes full advantage of today's digital ICs, which have circuit behaviors well-defined within each clock cycle, says Dr. Wu-Tung Cheng, vice-president

of research and development at ADAS. The ADAS algorithm includes dynamic fault grouping to simultaneously simulate multiple faulted circuits; group identity techniques to achieve fast restoration of good values after each fault propagation; active and inactive faults to prevent eventless fault simulation; intelligent fault injection to accelerate overall simulation time; and efficient fault ordering to minimize fault events.

For reduced system memory requirements, the ADAS fault simulator records only the difference between each faulty machine and the master copy of the good machine at circuit memory elements such as latches and flip-flops. This recording mechanism can save up to an average of 90 percent of system memory usage, claims ADAS, when com-

pared to concurrent fault simulation. The cycle-based fault simulator also lets users run large circuits without partitioning fault lists. ADAS claims that the run time for circuits with more than 5,000 gates can be 50 times faster than traditional concurrent fault simulators. "Our fault simulator has just finished a test case with 100,000 gates from SMOS Systems in just 16 hours," reports Joe Leung, vice-president of marketing, "whereas it might have taken weeks to finish this test case if concurrent fault simulation had been used."

The ADAS fault simulator produces a fault dictionary with a full report of user-definable fault-simulation information. Users can generate reports on selected faults and nodes for detailed fault analysis.

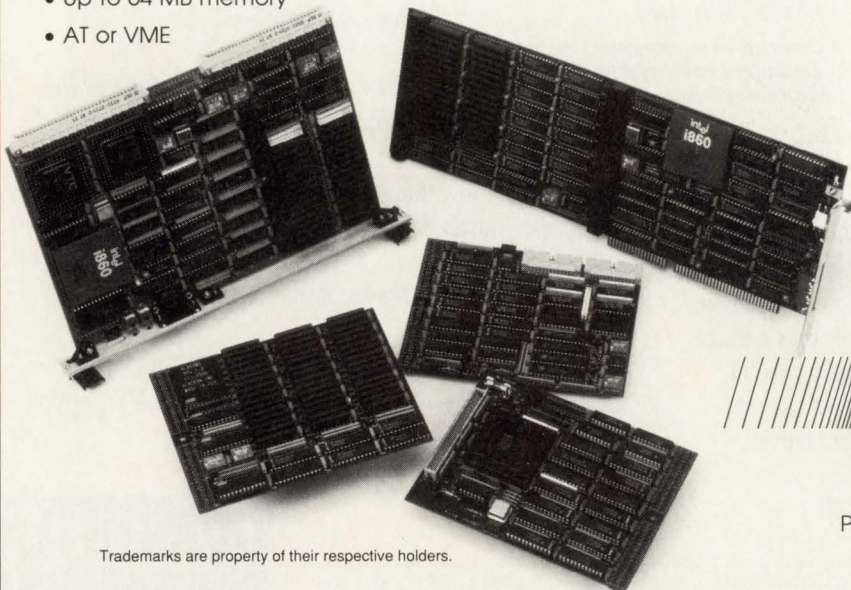
The cycle-based fault simulator supports RAMs, ROMs and bus structures. ADAS plans to embed

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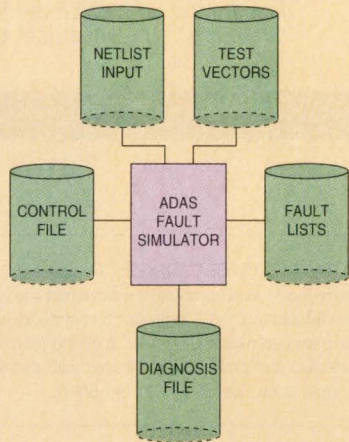
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Cycle-based fault simulation



The ADAS fault simulator takes a netlist and test vectors and generates diagnosis reports for users to analyze. Users can simulate large circuits without partitioning fault lists.

the fault simulator within a technology-independent automatic test pattern generator that will be suitable, according to ADAS, for all design-for-testability technologies including non-scan, full scan, partial scan, and BIST.

The ADAS Fault Simulator is available now at a cost of \$25,000 for a single-user license on a Sun workstation. —Barbara Tuck

ADAS fault simulator at a glance

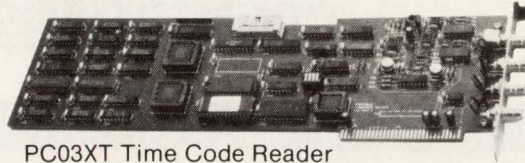
- Efficient memory utilization
- No partitioning fault lists
- Accepts standard gate-level netlists
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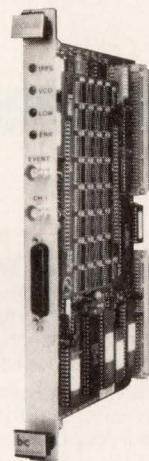
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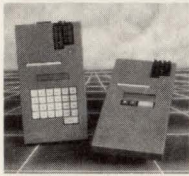
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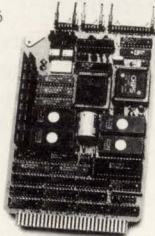
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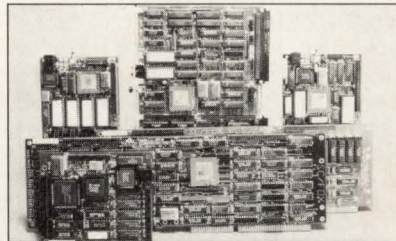
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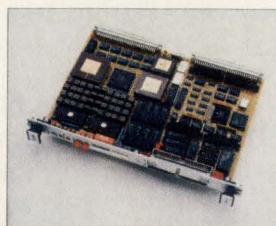
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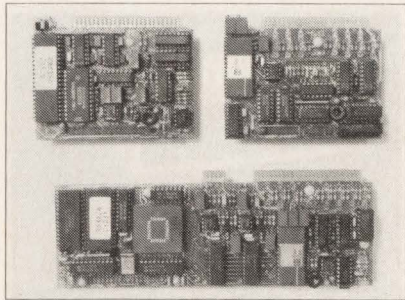
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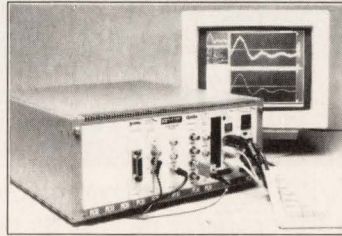
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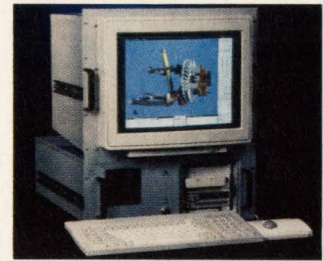


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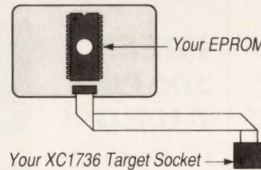


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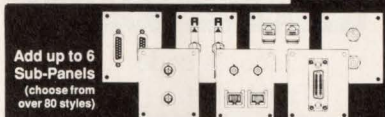
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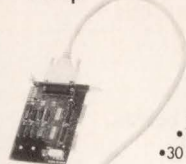
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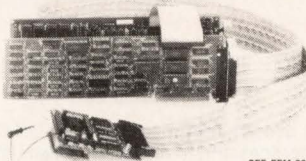
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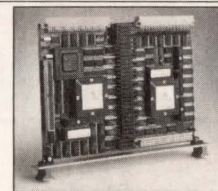
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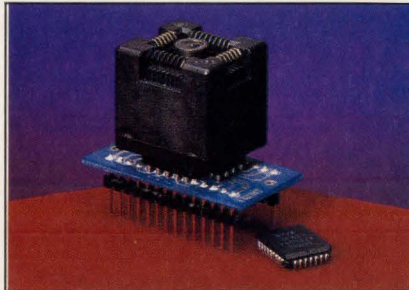
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ELECTROMAGNETIC FIELD RADIATION MONITOR

New literature is available on a new, low-cost monitor that is being introduced by Walker Scientific Inc. of Worcester, Massachusetts for measuring potentially hazardous low level electromagnetic field radiation generated by power lines,

TVs, VDTs, appliances and other electrical equipment. Walker's ELF-50 Field Monitor is a hand-held instrument that measures the extra-low-frequency (ELF) electromagnetic field radiation generated from any 50Hz or 60Hz device. Easy to operate, users just switch it on and place it where an ELF is suspected, then a 10 segment LED display will illuminate to indicate the level of radiation present.

Featuring two switch selectable measurement ranges: a low range from 1 to 512 milligauss and a high up to 51.2 gauss.

Walker's ELF-50 Field Monitor sells for \$179.95 (list). For more information contact:

Walker Scientific Inc.
Rockdale St., Worcester, MA 01606
(508) 852-3674

CIRCLE NO. 189

1991 UPCOMING ISSUES

Computer Design Magazine

MONTH	SPECIAL REPORT	TECHNOLOGY FOCUS	PRODUCT FOCUS
November 1 Wescon ITC	System simulation and verification <i>Mike Donlin</i>	High-density ASIC packaging — <i>Jeff Child</i> Multiprocessing in real-time — <i>Tom Williams</i>	STD CPU boards <i>Jeff Child</i>
December 2	Migrating PLDs to full ASICs <i>Barbara Tuck</i>	Accelerators to boost standard-bus performance <i>Warren Andrews</i> 8- and 16-bit microcontrollers	High-resolution A-D converters <i>Jeff Child</i>

*Starch Readership Study Issue

COMPUTER DESIGN Technology and Design Directions

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CIRCLE NO. 190

FINALLY!

A conference dedicated to the

MIXED AND

- SIGNAL ANALOG

designer!

By 1994, over 40% of all ASICs will be mixed analog and digital. The skyrocketing demands for mixed-signal technology in consumer, automotive and telecom markets will mean big profits for those positioned to meet the challenge.

Finally, there's a source for objective and up-to-date information on analog and mixed-signal design. The Analog & Mixed-Signal Design Conference features over 45 lectures, workshops, and tutorials dedicated to 100% of your needs as an analog or mixed-signal designer. Nowhere else will you find so much information, so much technology and so much expertise under one roof.



October 30-November 1, 1991
Santa Clara Marriott

- Learn how to bring mixed-signal design to market more quickly
- Find innovative solutions to your toughest design problems
- Know the capabilities and limitations of analog and mixed analog/digital ICs, ASICs and CAE/CAD tools
- Learn secrets to boosting your productivity from the best in the business
- Find cost effective ways to implement high-speed digital, mixed-signal, analog designs

Analog and Mixed-Signal Design

Dear Designer:

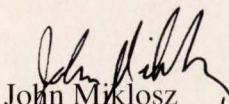
The **Analog & Mixed-Signal Design Conference** is dedicated to the unique needs of mixed-signal design. If you are an analog design engineer, a digital designer now tackling mixed-signal designs, a digital designer who must address the analog implications of high speed circuits, or an engineering manager, you should attend this conference.

This targeted technical conference, sponsored by Miller Freeman Inc. and *Computer Design* magazine, features over 50 lectures, workshops and tutorials dedicated to 100% of your needs as a mixed-signal designer. It's the only conference to focus exclusively on practical solutions to mixed-signal problems...and we've worked hard to make sure you get the information you're looking for.

Nowhere else will you find so many solutions to your mixed-signal design problems all under one roof—solutions that will help you complete your design projects more quickly, creatively, and elegantly. Journals and textbooks have their place—but at the **Analog & Mixed-Signal Design Conference** you'll learn more in three days than you could through months of research.

During three days at the **Analog & Mixed-Signal Design Conference**, you'll find insights and solutions suited specifically to your needs. Choose from the widest array of lectures, workshops, panel discussions, tutorials, and vendor information available at a single event. You'll have access to the most powerful tool in the marketplace—information—from the most widely respected professionals in the art and science of mixed-signal design.

Cordially,


John Miklosz
Associate Publisher/Editor-in-Chief
COMPUTER DESIGN
Hear From Industry Experts

CONFERENCE SCHEDULE

WEDNESDAY, OCTOBER 30

9:00 am - 10:00 am	Keynote Address
10:00 am - 8:00 pm	Exhibits Open
10:00 am - 11:00 am	Coffee Break
11:00 am - 12:00 n	Lectures
12:00 n - 2:00 pm	Lunch
2:00 pm - 5:30 pm	Half-Day Tutorials
2:00 pm - 3:00 pm	Lectures
3:00 pm - 3:45 pm	Coffee Break
3:45 pm - 5:30 pm	Workshops
3:45 pm - 4:45 pm	Lectures
6:00 pm - 8:00 pm	Reception

THURSDAY, OCTOBER 31

8:30 am - 12:00 n	Half-Day Tutorials
8:30 am - 10:15 am	Workshops
10:00 am - 6:00 pm	Exhibits Open
10:15 am - 11:15 am	Coffee Break
11:15 am - 12:15 pm	Lectures
12:15 pm - 1:45 pm	Lunch
1:45 pm - 2:45 pm	Lectures
2:45 pm - 3:30 pm	Coffee Break
3:30 pm - 5:15 pm	Workshops
3:30 pm - 4:30 pm	Lectures

FRIDAY, NOVEMBER 1

8:30 am - 12:00 n	Half-Day Tutorials
8:30 pm - 10:15 pm	Workshops
10:00 am - 1:45 pm	Exhibits Open
10:15 am - 11:15 am	Coffee Break
11:15 am - 12:15 pm	Lectures
12:15 am - 1:45 pm	Lunch
1:45 pm - 2:45 pm	Lectures
2:45 pm - 3:15 pm	Coffee Break
3:15 pm - 4:15 pm	Lectures

Listen, Brainstorm, Test Drive

No matter what program of classes you choose, you'll come away with fresh insight on the subject matter. That's because all the speakers share one thing: a commitment to excellence in design. Faculty members have been chosen for their contributions to the industry, their problem solving abilities, and their personal vision of the future. They'll offer in-depth, practical and real-world information you can bring to your design and development projects tomorrow.

Brainstorm With Faculty and Peers

One of the best ways to learn is by sharing ideas with your peers. And one of the key benefits of attending the Analog & Mixed-Signal Design Conference will be the insight you gain through this exchange. Workshops and informal receptions will provide an interactive opportunity for you to question leaders, comparing problems and experiences with your colleagues. Take advantage of the people resources that will be gathered at the Santa Clara Marriott during the conference by making lunch or dinner plans with others. And plan to attend our opening reception Wednesday evening where you will have the chance to meet faculty, fellow attendees, vendors, and the editors of *COMPUTER DESIGN* magazine.

Try Out The Latest Technology

The Analog & Mixed-Signal Design Conference will also be the site of the largest, most highly targeted exhibition of analog and mixed-signal design tools. Over 40 companies will exhibit the latest in mixed-signal ICs and design tools. As questions arise about different products or problems, you can go directly to the vendors on the exhibit floor for answers and solutions. Be sure to attend the Wednesday evening reception so you'll have plenty of time to explore and test all the latest products and tools on display. The industry's best will be there—and you'll be ready to discuss how their solutions might help solve

your special design problems. The list of exhibitors when this catalog went to press includes:

• ABB HAFO
• ANACAD
• Analog Devices
• ASIC Technology & News
• Contec Microelectronics
• Crystal Semiconductor
• Dazix/Intergraph
• Epic Design
• Gould/AMI
• Harris Semiconductor
• Mentor Graphics
• Meta-Software
• Motorola
• Racal-Redac
• Saronix
• SimExel
• Sipex
• Source Engineering
• Technology Information Publishing
• Texas Instruments
• Valid Logic
• Zeelan Technologies

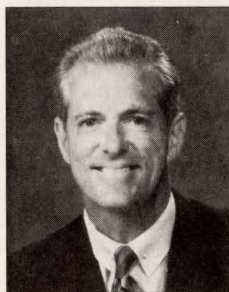
• And there are many more to come!

Take The Conference Back To Work

• As an attendee, you'll receive the complete 200-page bound proceedings including overviews and case studies from all the conference sessions (excluding panels). The Analog & Mixed-Signal Design Conference Proceedings is a powerful educational tool all by itself. You'll find yourself referring to it throughout the year seeking answers to your mixed-signal design problems.

Join Your Colleagues this October in Santa Clara

• Launched with your needs in mind, this in-depth, technical conference promises to be one of the most significant industry events of the year. Don't miss this opportunity to strengthen your skills and increase your designing power. Secure your spot today!



Harris' Jonathan E. Cornell To Open Conference

The first annual **Analog & Mixed-Signal Design Conference** will be launched at 9:00 a.m., Wednesday, October 30, with a keynote address by Jonathan E. Cornell, a senior vice president of Harris Corporation. Cornell, an "old analog hand," will give conference attendees his insights into the impact of mixed-signal ASIC technology on system design, on system designers and on the markets they're designing products for.

Cornell joined Harris in 1968 as an analog designer and since then has held various technical and managerial positions within the Semiconductor Sector and was vice president/general manager of the Analog Products Division. He was named senior vice president/sector executive in 1983 and promoted to Semiconductor Sector president in 1989. According to VLSI Research, Harris has become the largest mixed-signal ASIC supplier in the U.S.—an achievement in large measure due to Cornell's vision and leadership.

Cornell also holds positions on the board of directors of the Semiconductor Industry Association and Sematech. He is a member of the IEEE and on the engineering advisory board of the University of California at Berkeley and the University of South Florida.

FACULTY

Craig Aine

is an Applications Engineer at Signetics, a subsidiary of North American Philips. His responsibilities include applications support for digital audio and telecom products. He holds a BEE from California State University, Sacramento.

Dr. Hal Alles

is General Manager of the Simulation & Test Division at Mentor Graphics. He holds a BS in Physics from Case Institute of Technology, Cleveland, Ohio, and a PhD in Physics from the University of Oregon.

Jack Armijos

is with Siliconix.

Dr. Guido Arnout

is General Manager, & Vice-President of the Physical Design Systems Division at Silvar-Lisco. Prior to this position, Guido was Vice-President of Engineering. He received his MSEE and PhD from the University of Leuven, Belgium.

David Buchanan

is a Strategic Marketing Engineer for high-speed digital-to-analog converters and related products at Analog Devices' Computer Labs Division. He is involved in product planning, market strategy, applications, customer contact, and data sheet development. He has a BSEE from the University of Virginia.

Joe Buxton

is an Applications Engineer at Analog Devices/PMI. He has worked extensively on Spice op amp models, writes application notes and data sheets, and helps customers resolve their circuit and design problems. He has a BSEE from the University of California, Berkeley.

Christian Caillon

obtained his engineering degree from the Conservatoire National des Arts et Metiers of Paris. He is currently R&D Manager for mixed A/D semicustom for SGS-Thomson Microelectronics.

Don Cassidy

is responsible for definition of CAE/CAD tools and automation of the analog design process within NCR Microelectronic Products. He holds a BSEE from Colorado State.

Mark Chadwick

is the Product Marketing Manager of Mixed-Mode Simulation for Analog. He previously was an Analog System Designer with Eaton Corp. Chadwick holds a BSEE from the University of Wisconsin.

Dr. Moji C. Chian

is currently leading the Modeling and Advanced Simulation group at Harris Semiconductor. He has a BSEE, MSEE, MS in applied math, and a PhD in Electrical Engineering from Florida Institute of Technology. He is also an adjunct professor in the EE/CP department at the Florida Institute of Technology.

Carlo Cini

heads the Audio & Automotive IC Design Department in the Dedicated Products Group of SGS-Thomson Microelectronics. He has responsibility for the design department that specializes in power ICs for industrial and computer peripherals. Carlo graduated in Electronics at the Instituto Tecnico Leonardo da Vinci in Pisa.

Dan Curran

is a Field Design Engineer with NCR Microelectronics responsible for field application support for ASIC custom-

ers doing mixed-signal designs. He received his BSEE from Stanford University.

Rich Davis

is Regional Technical Manager for Valid's Northwest Region. Prior to his present position, Rich was Corporate Applications Manager for Analog Design Tools.

Harry Davoody

is with Texas Instruments.

Jim Dekis

is a senior member of the technical staff at Maxim and is responsible for new product research and design. His previous experience includes CMOS design at Teledyne Semiconductor and bipolar design at Fairchild. He did graduate work at Santa Clara University and holds a BSEE from Rutgers.

Peter Denyer

is a Product Marketing Manager in Mentor Graphics' Simulation & Test Division, responsible for the integration of third party and commercial simulators into the Explorer Lsim framework. He holds a BSEE from the University of Toronto.

Dr. Geert DeVeirman

received his PhD in electrical engineering from the University of Minnesota and has been a senior design engineer at Silicon Systems since 1988.

Dr. Dileep Divekar

is Director of Simulation and Modeling at CAE Division, Contec Microelectronics where he is responsible for the development of simulation and modeling software. He holds a PhD in electrical engineering with a minor in computer science, from Stanford University. He has con-

tributed over 30 articles to technical journals and conferences, and has authored a book titled "FET Modeling for Circuit Simulation."

Dr. Akis Doganis

is Vice-President of Research and Development at EES. He received a BS in Physics from Aristotelion University in Greece, and MS in Systems Science and Mathematics from Washington State University and the DEE from Stanford University.

Michael G. Donlin

is an Editor with Computer Design magazine covering CAE/CAD Tools. He holds a BA from Merrimack College.

Peter Ehlig

is a member of the technical staff at Texas Instruments. He was the lead architect of the TMS320C5X family of DSPs and is currently responsible for custom DSP design. He holds a BS in Mathematics and a BS in Electrical Engineering from the University of Houston.

Ken Fields

is Product Marketing Manager at Micro Linear, and is responsible for the USIC (semi-custom) and Semi-Standard product families. Ken holds a BEE.

Wanda Garrett

has been with National Semiconductor for eight years in the Linear Applications Group, working with switching regulators and standard linear products. She is currently the group manager for power management applications. She has a BSEE from Washington State University.

FACULTY

Bill Gazeley

has an MSEE from Oregon State University.

Alan E. Gorlick

is a consultant who specializes in solving complex problems in finance and sales for high tech electronics companies. He is also on the faculty of the University of St. Thomas, St. Paul, MN. He received his BSEE from Rensselaer Polytechnic Institute.

Jim Griffeth

is a Business Unit Director of the Simulation & Test Division at Mentor Graphics. Jim holds an MBA from Harvard University and a BSEE from Brown University at Providence, RI.

Dr. Max W. Hauser

has designed commercial solid-state circuits since 1971. He holds degrees in electrical engineering from the University of California at Berkeley and MIT, and has taught IC design at Cornell University.

Richard Hester

is with Texas Instruments

J. Richard Hines

is a Silicon Sensor Engineer for Micro Switch, a division of Honeywell. He holds a BA in math from the University of Colorado and a BSEE from Arizona State University.

Dr. Lawrence Horwitz

has been on the faculties of New York University, the Polytechnic Institute of Brooklyn, New Jersey Institute of Technology and Rutgers University. Horwitz has a PhD in Electrical Engineering from New York University.

Steven E. Hunt

is a Linear Applications Engineer for National Semiconductor in the fields of data acquisition, power management and motion control. He received his BSEE from the General Motors Institute.

Keith Jack

is a strategic product planner for Brooktree and is responsible for new product definition of VLSI products for the emerging desktop video market.

Paul Jennings

is currently European Director with Electrical Engineering Software. He received the BSc from North Staffordshire Polytechnic and worked for a PhD at Imperial College, London. From 1983 to 1988 he was a Lecturer in VLSI Design at the University of Bath.

Sarath Kallara

has been involved with the development of the Signal Processing WorkSystem for Comdisco Systems. He received a BSEE from University of Calicut, India and an MSEE from Tennessee Technological University.

Dr. Hans W. Klein

received the MS Eng. and the Dr.-Ing. (PhD) for his work on analog and mixed analog-digital integrated circuits from the Rheinisch Westphalische Universitat Aachen. He is a member of the IEEE, and has published over 20 papers in the fields of circuit design, design systems and design management.

Herb Kneiss

is with the Media Components Group at Signetics/Philips. He holds a BSET

from California Polytechnique State University.

Dr. Ken Kundert

is the architect of the Spectre general-purpose circuit simulator at Cadence. He holds a PhD in Electrical Engineering and Computer Sciences from the University of California, Berkeley. He is also the author of "Steady-State Methods for Simulating Analog and Microwave Circuits."

Kerry Lacanette

is the Data Acquisition Applications Manager for National Semiconductor Corporation, with responsibility for A-D converters, D-A converters, voltage references, switched-capacitor filters and sample-and-hold circuits. He has written and collaborated on several technical articles and books. He received his MSEE from University of California, Santa Barbara.

Judy Lee

is a Product Specialist at Valid Logic working with analog and mixed-signal automation tools. Judy holds a BSEE from the Georgia Institute of Technology.

Robert E. Leonard

is the Product Marketing Manager for component products at Datel. He received his BSEE degree from Northeastern University and has been with Datel since 1974.

Dr. Andrew Marshall

received his PhD in 1984 and is currently involved in mixed-signal CMOS design for automotive application at Texas Instruments.

Michael K. Mayes

received his BSEE and MSEE from San Jose State

University. Since 1987, he has worked as a circuit design engineer at National Semiconductor in the field of A-D converters.

Jean-Yves Michel

received his MS in Electrical Engineering from Ecole Central de Lyon, Lyon, France in 1977. He is now a Principal Engineer in the Data Acquisition IC Design Group at National Semiconductor.

Joseph A. Mielke

is a Senior Applications Engineer with Integrated Measurement Systems, Inc. He holds a bachelors degree from the University of Minnesota and is a member of the IEEE.

Guy M. Morency

is currently active in macro/behavioral modeling for circuit level simulation. He received his BSEE and MSEE from the University of South Florida.

Hassan Nosrati

is with Dazix as a Staff Consultant. In recent months his primary focus has been the development of Diablo. His prior experience includes work at Fairchild and Philips in electronic design automation research and development.

Stephan Ohr

is Editor and Publisher of "Mixed Signal," a monthly newsletter devoted to analog and mixed-signal technology and business issues. He holds a BSIE from Newark College of Engineering, and an MA from Rutgers.

Sangil Park

holds a PhD and is currently with Digital Signal Processing Operations at Motorola in Austin.

FACULTY

Stephen Parks

is currently the Manager of Marketing and Applications for the mixed-signal group at AT&T Microelectronics. His experience includes product design and engineering for semicustom and ASIC products. He holds a BSEE from Lafayette College and an MSEE from Lehigh University.

Dr. Raj Raghuram

has a PhD in Electrical Engineering from Stanford University. He was professor of electrical engineering at the Indian Institute of Technology, Kanpur, India, and a visiting professor at Trenton State College, NJ. He has authored over 30 papers and is author of the book, "Computer Simulation of Electronic Circuits."

Dr. Jean Remy

received MS and PhD degrees from the Universite Catholique de Louvain, Belgium. He is currently with the Anacad Department SGS-Thomson Microelectronics, working on mixed signal circuit simulation and multilevel simulation.

Gus Richard

is a Senior Research Analyst for VLSI Research Inc's "Mixed Signal ICs" subscription service. He holds an MS in Physics from Purdue University and a BS in Physics from the Rochester Institute of Technology.

Thierry Roullier

Field Applications Engineer, has been an analog FAE with Valid Logic since 1987. Prior to joining Valid he was an analog design engineer with Aerospatiale.

Santanu Roy

is an Application Engineer at National Semiconductor, sup-

porting microcontrollers for a wide variety of applications such as anti-lock brakes, motion controls, disc drives, cordless telephones, and consumer electronics. He holds a BSEE from Jadavpur University, India and an MSEE from Memphis State University.

Jonathan L. Sanders

is a Product Specialist for analog and mixed-signal simulation with Valid Logic's CAE Division.

Jeffrey Scott

holds an SMEE degree from MIT and is currently a design engineer at Crystal Semiconductor. He has designed a number of analog/digital ICs for a variety of mixed-signal applications.

Dick Simko

has a strong career in memory design, holding more than 20 patents. A founder of Information Storage Devices (ISD), he is its Vice President of Engineering and Chief Technical Officer. He holds a BSEE and an MSEE from Ohio State University.

Michael J.S. Smith

is a professor of electrical engineering at the University of Hawaii.

Mark Stansberry

is the founder of Cypress Information Resources, a technical and market research firm specializing in integrated circuits and CAE. He obtained his BSEE from San Jose State University, and has worked as an Applications Engineer and an ASIC Applications Engineer.

Lee L. Stoian

is Director for Data Acquisition Design and Linear Design Automation for National Semiconductor. His current

responsibilities cover the development of data acquisition products and mixed-signal design automation. He holds an MSEE.

Michael Tu

is a Senior Electronics Engineer at Valid, working with the analog modeling group. He holds a BCS and an MSEE from Santa Clara University.

Barbara Tuck

is an Editor with Computer Design magazine covering ASICs and ASIC design tools. Before joining Computer Design she wrote extensively about analog technology and design.

Shannon Tyson

is an Analog Design Engineer, NCR Analog Applications, with NCR Microelectronic Products, responsible for system design, IC design, simulation, and layout of customer designs. Shannon holds a BSEE from Texas A&M.

Naished Vashi

is currently Marketing Manager for Cirrus Logic's mass storage business unit. His previous experience includes peripheral circuit design for DEC, Versatec and Fairchild. He holds a BSEE from Gujarat University in India, an MS in Computer Engineering from Boston University and an MBA from the University of Phoenix.

Dr. Ronald Vogelsong

is a Principal Engineer with the Modeling & Advanced Simulation group at Harris Semiconductor. He has a BSEE/MSEE and PhD in Electrical Engineering from the University of South Florida in Tampa, Florida.

Dr. Paul K. U. Wang

is President, CAE Division, Contec Microelectronics. He was a professor at Mankato State University, Minnesota, and the University of Cincinnati, Ohio, where he taught electrical engineering. He has authored over 50 papers on simulation software and hardware.

Bruce Webster

is Manager of System Applications at Teradyne's Boston-based Industrial/Consumer Division. He currently focuses on computer-aided test development software. Bruce received his BSEE from Worcester Polytechnic Institute.

Dr. Eric Wildi

is Director of Intelligent Power Engineering at Harris Semiconductor. He holds an MS and a PhD from Stanford University.

Michael Yeung

is Director of Chip Design at Phylon. His responsibilities include development of mixed analog/digital circuits and systems. He received a BSEE in Electrical Engineering from the University of California at Berkeley.



Coffee breaks are generously sponsored by Analog Devices.

TECHNICAL PROGRAM WEDNESDAY

WEDNESDAY MORNING

Lectures 11:00-12:00

021 Unscrambling the Mixed-Signal Market

Mark Stansberry

The growth of the mixed-signal market is reviewed with special attention given to telecommunications (ISDN, fiber optics and mixed communications nodes), graphics and video, analog and digital compression, data storage, neural processors, intelligent power and multimedia. Development and market barriers are analyzed within the realm of process technology, fabrication, simulation, testing, noise and power considerations, and cost. The goal of this presentation is to emphasize the market potential of mixed-signal devices, for both the obvious and not-so-obvious applications.

022 Disk Drive Controllers

Naished Vashi

Improvements in VLSI, along with surface mount packaging, are driving a trend toward intelligent drives, in which the control electronics are shifted from the host to the hard disk drive itself. This presentation describes the different elements in the data storage chain from the host computer to the disk surface, as well as distinguishing between the intelligent and nonintelligent disk drive interfaces—SCSI, IPI, ESDI and ST-506. The analog and mixed-signal elements in the chain are highlighted and alternatives for bringing these elements together on a single substrate are described.

023 An Overview of Oversampling Data Converters

Max W. Hauser

Oversampling is important in A-D and D-A conversion, permitting high resolution with inexpensive components, simplified antialias and reconstruction filtering, and accelerated design cycles for custom mixed-signal ICs. This lecture emphasizes the practical concerns of designers accustomed to more traditional (i.e., nonoversampling) ADCs and DACs. It focuses on signal acquisition and regeneration; the theory of oversampling, including quantization noise, frequency-domain operation and noise shaping; antialias and reconstruction filtering; multibit vs. one-bit noise shaping; and performance limits.

024 Hierarchical Design Using a New Mixed-Signal Simulation Technique

Raj Raghuram, F. Balistreri, Dileep Divekar and Paul Wang

A new approach to native-mode, mixed-signal simulation is presented that lets a designer simulate an entire system without the need for artificial partitioning of the system. This approach provides for a hierarchical description and simulation of both the digital and analog portions of a circuit from the behavioral level, gate or analog macromodel level down to the transistor level. Designers can concentrate on one subsystem at a time until all subsystems are designed and verified and then simulate the entire system at the behavioral level. Phase-locked loop and communication system designs are used to demonstrate the applicability of the approach.

025 DSP Simulation of Mixed-Signal Systems

Sarath Kallara

The performance of a purely analog system such as a feedback servo system can be simulated and improved using double-precision DSP functions, once the analog transfer functions of all the blocks in the system are known. For example, the erratic step response can be greatly reduced by adding a compensator in the feedforward path. This presentation discusses the modeling of such a compensator as a purely digital system comprising an ADC, an optimized digital filter and a DAC, thereby making the system mixed analog-digital in nature.

026 Analog Memory in Cellular Telephone Applications

Dick Simko and Joe Jarrett

A low-power analog memory device lets cellular telephone users record conversations with their handsets. Functioning like a solid state tape recorder, current devices record 16 seconds of speech within a 3.4 kHz bandwidth. (Longer storage capacity is possible, although with a lower sampling frequency.) This application takes advantage of the analog memory's internal microphone pre-amplifier and AGC, and its ability to drive a 16-ohm speaker directly. The analog solid state memory device is a forerunner of "analog emulation" technology—the application of primarily digital techniques to solve primarily analog problems.

027 Safe Operating Area: Interfacing to the Real World

Andrew Marshall, J. Devore, T. Efland, C. Jones, J. Mings and T. Summerlin

The Safe Operating Area (SOA) defines a condition or set of conditions of permissible voltage and current stress on a semiconductor device during operation. In this lecture, the SOA performance of output device types for various mixed-signal IC processes are discussed, along with process enhancements for improved performance, design considerations, application needs and automatic testing of SOA. A comparison of SOAs under different load conditions is presented, with descriptions of the effects of device structure on SOA.

WEDNESDAY AFTERNOON

Tutorials 2:00-5:30

031 Spice Modeling

J. Richard Hines

Spice and its derivatives are the bulwark of analog and mixed-signal circuit simulation. But the key to Spice lies in the quality of the device models. This tutorial will examine device models in Spice 2G6 for passive and active components (a bandgap reference will be used as an example); new device models in Spice 3E, such as GaAs amplifiers; building more complex models; extending 2G6 and 3E built-in models in stand-alone Spice, with a saturated NPN output transistor and a silicon sensor used as examples; extending 2G6 and 3E built-in models with additional software, preprocessor programs, commercial models and modeling digital building blocks; and proprietary enhancements to Spice and approaches to modifying source code.

032 Monolithic ADCs

Lee L. Stoian and Kerry Lacanette

The advances in digital technology (and, in particular, digital signal processing) have increased the need to understand and use ICs that allow microprocessors to interface with the analog world. This tutorial covers the state-of-the-art in monolithic A-D converters (ADCs), emphasizing the various architectures and tradeoffs. Covered are the key specifications, architectures, features and applications of the most widely used converter types: integrating, successive approximation, flash,

TECHNICAL PROGRAM

WEDNESDAY-THURSDAY

and multistep/subranging. Delta-sigma converters are also discussed as well as algorithmic, pipeline, parallel/pipeline, folding and interleave.

Lectures 2:00-3:00

033 Power Supply Design for Portable Systems

Jim Dekis

A primary requirement for portable systems is rechargeable batteries and efficient, low-loss power supplies. Voltage regulators and dc-dc converters must be highly efficient and these components must be highly integrated to minimize power supply size and weight. Overall power supply efficiency can be increased by reducing the supply voltage requirement from +5 V to +3 V and by power monitoring to shut down parts of the system that are inactive. This presentation provides helpful pointers for minimizing power supply components and maximizing battery life.

034 Digital Video Encoding Standards and Techniques

Herb Kneiss

The process of converting video analog to digital data requires more than high speed A-D conversion technology. Various video broadcast and recording formats must first be implemented as luminance and chrominance vectors. These, in turn, must be converted to RGB or lookup table formats. This requires expertise in high-speed A-D conversion, digital multistandard color decoders, digital color space converters, and digital encoders. This lecture details how to implement video functions digitally, without degrading the analog signal.

035 Microstepping of Hybrid Step Motors

Steven E. Hunt and Santanu Roy

Recent advances in smart power drivers and sophisticated DACs make microstepping practical. Microstepping taps the latent analog nature of step motors and so requires control and drive electronics that are more analog in nature than traditional state machine and low-side switch schemes. This session details a complete microcontroller-based system for control of (hybrid) step motors and covers all aspects of the design, from theory to practical applications. Special emphasis is placed on the im-

part of device characteristics and specifications on system performance.

036 Integration of DSP and Data Acquisition Functions: Chip and System-Level Considerations

Peter Ehlig

High-precision data-acquisition circuits present new challenges when integrated with high-speed DSPs. System-partitioning issues also play an important role in determining the most cost-effective mixed-signal solution. This presentation focuses on when and why integration of high-performance DSPs, A-D and D-A functions is technically feasible and economical. The considerations involved in integration are discussed within the context of several common DSP applications.

037 Digital Noise Management Techniques to Realize 16-Bit A/D/A Converter Performance

Jeffrey Scott

The design challenges and tradeoffs facing both silicon and system designers wishing to integrate CD quality digital audio signal processing into the PC/workstation environment are legion. The central concern is the prevention of high-frequency digital noise from assuming the alias of audio band signals at the sensitive A/D conversion boundary. This lecture examines the techniques for the management of digital noise that threatens to limit the conversion accuracy of highly integrated systems.

Workshops 3:45-5:30

041 Impact of Mixed-Signal Simulation on Design Methodology

Hans W. Klein

There's a growing demand for mixed analog/digital circuits and the CAD support needed to make design tasks more efficient and less error prone. This workshop describes the essentials of a modern mixed-signal design system along with the essentials of a modern mixed-signal design methodology. It looks at what tools are really needed, what is realistic to expect in the near future, and how one should go about matching tools and design methodology. Practical examples of the challenges and trade-offs

provide insight into real mixed-signal issues related to multiple power sources, crosstalk minimization, libraries, simulation, layout, etc., and explain why design methodology and design systems are so tightly coupled.

042 Analog Switches and Multiplexers

Jack Armijos

CMOS transistors make natural switches and multiplexers. They have low power dissipation in the unused or quiescent state, and low on-resistance. But analog switch selection involves a consideration of breakdown voltages, switching speeds, and crosstalk between adjacent channels. In this workshop, the relevant specifications for analog switches are discussed. Special emphasis is placed on some of the newer applications of analog switches and muxes, such as video crosspoint switching or automotive power supply regulation.

Lectures 3:45-4:45

043 Understanding Semicustom Alternatives

Ken Fields

Semicustom analog designs can be implemented in tile arrays, standard cells or full custom and each requires tradeoffs in performance, development time and cost. This lecture presents a discussion and comparison of these approaches with special emphasis placed on the component modeling, circuit design, simulation, layout and packaging issues associated with analog ICs implemented in tile arrays.

044 Designing Front-Ends for Voice Band Modems

Mike Yeung

The front-end modem circuits operating in the voice band must perform a variety of analog and digital functions. A data pump, for example, transforms digital data into modulated analog signals and vice versa. This lecture will discuss some of the problems that arise in implementing the necessary high-speed modem functions, the design and simulation tools available, in particular, Mentor Graphics' Lsim, and provide a circuit with 30 poles of filtering, 40 op amps, three DACs and two ADCs and over 8,000 equivalent gates of digital logic as an example.

THURSDAY MORNING

Tutorials 8:30-12:00

051 Issues in Mixed-Signal ASIC Design

Don Cassidy, Shannon Tyson, Dan Curran and Bill Gazeley

The integration of analog functions onto an IC raises many questions for system designers who only have a board- or system-level perspective. This tutorial presents mixed-signal system and PCB designers insights into the advantages and disadvantages of a mixed-signal ASIC implementation, process and technology choices and trade-offs, device specification, evaluating libraries, design methodologies, simulation, layout, device testing and board-level considerations. These issues are presented within the context of real applications examples.

052 Understanding Data Converter Frequency Domain Specifications

Bob Leonard

The advent of sampling ADCs with internal sample-and-hold makes it possible to establish precise frequency domain specifications for these converters. This tutorial aims to provide designers with a comprehensive understanding of frequency domain specifications as they apply to precision ADCs. Covered are the time/frequency domain and FFTs, sample-and-hold, aliasing, signal-to-noise ratios, distortion, in-band harmonics, effective bits, noise/power ratios, input bandwidth, acquisition time, overvoltage recovery, coherent vs. noncoherent sampling, dynamic range, spectral leakage, equivalent noise bandwidth and process loss.

Workshops 8:30-10:15

053 Understanding Mixed-Mode Simulators

Mark Chadwick

Diverse approaches exist for building and using mixed-mode simulators, resulting in a broad spectrum of simulation capabilities. All mixed-mode simulators are either native (one algorithm for digital and analog elements) or mixed (using a combination of an analog and a digital algorithm). But there are much more subtle distinctions

that are critical. This workshop probes modeling and modeling languages, libraries, partitioning and modeling the interface between analog/digital circuits, and benchmarking.

054 Filter Design

Speaker to be announced

Though one of the most basic analog building blocks, filters are among the most difficult to understand and design. Analog filters are typically made up of passive components, sometimes in conjunction with op amps in a unity gain buffer configuration. This workshop provides an exposure to the basic filter topologies, including Butterworth, Chebyshev, Linear Phase, Elliptical and Bessel, as well as high- and low-pass configurations. It includes an introduction to modern DSPs, which provide filter functions close to the mathematical ideal, though at the expense of software complexity.

055 Basics of Power Supply Design

Wanda Garrett

How does a digital designer come up with a steady, dependable 5 V for a logic circuit? This workshop will not turn the logic designer into a wizard of power supply design, but it does cover the basics of transforming ac into ripple-free dc. Special emphasis is placed on the low- and medium-power solutions to on-board distributed power problems, including the use of single-chip switching regulators and dc-to-dc converters. Linear and switching regulator topologies are also discussed and compared.

Lectures 11:15-12:15

061 Spectre: A New Approach to Mixed-Signal Simulation

Ken Kundert

Spectre is a direct method circuit simulator similar in function and application to Spice but written from the beginning in C. Spectre uses the same basic methods—implicit integration, Newton-Raphson, and direct matrix solution—but every algorithm has been implemented from scratch. This presentation will detail how numerical errors are controlled, how larger circuits can be handled at faster speeds, the benefits of

dc conversion and transient convergence and provide some benchmark results.

062 Automated Generation and Simulation of Macro/Behavioral Models

Ron Vogelsong, Guy Morency and Mojoy C. Chian

Recently, macro (circuit-based) and behavioral (functional) modeling have opened a new avenue to circuit simulation. Replacing selected blocks of a large circuit with their macro or behavioral models significantly reduces the simulation time while retaining a comparable level of accuracy. This presentation discusses a collection of tools for automating the generation of macro/behavioral models for circuit simulation. These tools facilitate the generation of macro/behavioral models (using a high-level language) for a wide range of analog and digital blocks. For each block, several levels of models are available, letting designers choose between faster vs. more accurate models.

063 Applications of Sigma-Delta (Bitstream) Converters

Craig Aine

The implementation of complete stereo audio D-A conversion with oversampling, noise shaping, 1-bit DAC and post-filtering op amps can be achieved in several ways. The key differences between bitstream and multibit solutions are explored, with specific emphasis placed on how bitstream devices overcome the problems inherent in multibit designs and on the design issues, such as proper selection of external components and maintaining integrity of digital signals, that are specific to bitstream technology.

064 Optimizing High-Frequency Amplifier Bandwidth

Joe Buxton

Operational amplifiers are continually pushing the limits of bandwidth and speed well into the 100's of megahertz range but this can create problems in preserving an op amp's stability without sacrificing bandwidth. This lecture looks at the different areas of instability such as capacitive loading, power supply bypass, input capacitance and lead-lag compensation. Methods of compensation are discussed that will ensure stability under these various conditions.

TECHNICAL PROGRAM THURSDAY-FRIDAY

065 Advanced Graphics Back-End System Architecture

Harry Davoody and John Yin

The computer graphics market is driven by the need for lower systems-level cost, faster time to market, higher performance, and higher system integration. An example is the graphics back-end subsystem where similar concerns among graphics system designers have led to advances in back-end architectural integration. This presentation explores system level design considerations for a flexible video interface palette, VRAM interface system timing, video control and pixel processing, true color support, independent resolution and color depth programmability, and system level testability.

THURSDAY AFTERNOON

Lectures 1:45-2:45

071 Analog Behavioral Modeling of Op Amps

Jonathan L. Sanders and Michael Tu

Operational amplifiers, a fundamental building block for analog and mixed-signal circuits, are usually modeled using standard macromodeling techniques, often based on the well-known Boyle model. This lecture describes the development of a sophisticated new model for op amps that uses a combination of macromodeling and pure behavioral modeling. The benefits and advantages of using this mixed approach, performance benchmarking against other approaches, and how the method might be extended to other kinds of devices are discussed in detail.

072 Diablo: An Analog Behavioral Modeling Tool

Hassan Nosrati and Lawrence Horwitz

Diablo is a new analog behavioral modeling tool that works in concert with existing analog toolsets and is intended to significantly enhance a designer's ability to solve complex analog design problems. The Diablo behavioral description syntax builds upon and extends the universally familiar Spice syntax so that it makes no demands on the analog designer to learn a complex language syntax.

073 Simulation Algorithms

Jim Griffeth

All simulators and simulation algorithms trade speed of simulation off against some other parameters: accuracy, detail, generality, capacity, level of abstraction, specialized hardware, etc. This session reviews some popular algorithms with respect to the various trade-offs and how they can be used in the design process. The most practical long-term simulation solution couples multiple simulation algorithms so they can be used concurrently. This session also covers some techniques for integrating multiple analog and digital algorithms into a unified mixed-signal and multi-level simulator.

074 Choosing DACs for Direct Digital Synthesis

David Buchanan

Direct digital synthesis (DDS) is a technique for generating sine waves that is especially well-suited to digital control of frequency. Unlike older techniques that use oscillators to generate waveforms, DDS generates the waveform as a series of discrete digital points, then converts these to analog via a DAC. This lecture provides an overview of a DDS system, the relevant parameters that describe DDS, what characteristics are important to DAC selection, and some of the performance trade-offs that must be made.

075 Complementary Bipolar Processes for High Performance Analog ASICs

Stephen Parks

A junction-isolated process called Complementary Bipolar IC (CBIC) combines high speed and drive capability by building vertical NPNs and PNP's with comparable gain and frequency characteristics. This technology offers very high gain-bandwidth products, with low noise, low input capacitance, relatively low power dissipation and high common-mode rejection. Described is the CBIC-U process which offers 4.5-GHz, 12-V NPNs and 3.75-GHz, 11-V PNP's, and CBIC-R, a 33-V process offering 250 MHz f_s . Future enhancements to the CBIC process are also covered.

076 Managing and Reducing Risk When Selecting Mixed-Signal Tool and Silicon Vendors

Alan E. Gorlick

Because there are dramatically new tools and new methodologies for mixed-signal design, the tool- and vendor-selection process is especially complicated, with uncertain applications and real financial risks. Techniques for structuring transactions and negotiating with vendors to reduce, manage and share risk, finance and procurement processes, conforming to budget constraints and retaining flexibility all receive attention in this presentation.

077 Using Spreadsheets for Analog/Digital Design

Michael J. S. Smith

A spreadsheet program is ideal for the complicated "what-if" procedures used in analog/digital design. This presentation shows how to calculate circuit specifications directly, bypassing long and tedious iterative Spice simulations. By using simple fixed layout modules, the possible number of circuits the program can handle is constrained, reducing flexibility, but enormously simplifying design. A layout assembly program can be generated automatically from the computed device sizes and a sized Spice netlist is used to perform circuit simulation to confirm the performance predicted by the spreadsheet. It's even possible to produce a netlist which includes parasitics.

Workshops 3:30-5:15

081 Digitizing Analog Functions

Gus Richard, Moderator

The difficulties in designing and testing mixed-signal ICs are well known and they're perceived by many as key limitations for an emerging mixed-signal industry. But do the solutions lie in better tools for designing and testing mixed-signal ICs or in the digitization of analog functions? This panel discussion analyzes which approach is best, why and for which applications; what rules should be used for selecting an approach; and how will the digitized analog approach affect future designs. Panelists include representatives from analog and mixed-signal IC vendors.

082 Who really won BCTM?

Stephan Ohr, Moderator

Last year's IEEE Bipolar Circuits and Technology Meeting (BCTM) featured a "competition" among analog simulation vendors. They were given the task of simulating a 12-bit successive approximation ADC. The design contained 450 transistors and 200 resistors. (2/3 digital) Participants were to each present the minimum conversion time of the ADC, the simulation run time (for one bit and all 12 bits), and the approximations used. Some simulators turned in figures for the complete A-D conversion, while others turned in figures for only one clock cycle. One otherwise fast behavioral simulator functioned slowly on the transistor level, but was the only one to accurately predict conversion time. In this panel discussion, BCTM participants address who really "won?"

083 Who are Mixed-Signal Design Tools Intended For?

Barbara Tuck, Moderator

There seems to be some confusion about which products really address which problems in the area of mixed-signal simulation. This panel discussion looks at the products being used to design complete chips (ASIC, custom or standard product) and who they are intended for, the expert in analog design or the "novice." The discussion will also cover the products being used to design mixed-signal board-level products and the problems faced in combining standard digital libraries with analog libraries and relying on simulation to verify operation.

Lectures 3:30-4:30

084 Mixed-Signal ICs in Imaging and Graphics

Keith Jack

While the computer CRTs use RGB color space to visualize an image on the screen, scanners and video cameras, on the input side, and new-generation desktop color printers, on the output side, use somewhat different color space representations. RAMDAC systems with interface circuitry, SRAM color lookup tables and triple 8-bit DACs are required to produce a 24-bit RGB output. This paper describes the systems and components which are required to manipulate

and control a color image in its journey from scanner or other input to computer graphics screen, and from computer screen to printer.

085 Optimization and Design Centering to Improve Yield and Performance

Akis Doganis and Paul Jennings

Optimization and design centering algorithms, combined with circuit simulation as well as statistical and sensitivity techniques can improve yield and performance of analog ICs. Design variables are automatically determined to match the desired circuit performance to nominal process and environmental conditions while the design-centering algorithms improve the yield of the circuit by accounting for process extremes. An overview of the functional and numerical details of optimization and centering algorithms is provided as well as a three-step methodology for generating the optimum design and achieving improvements in circuit yield and performance.

086 Profile: A Spice-Based Analog and Mixed-Signal Modeling Language

Judy Lee

A new mixed-level simulator, Spice Plus 3.0, incorporates new algorithms and a behavioral language, Profile, to present a new approach to the problem of analog modeling. Profile lets designers write fast, compact descriptions of analog functions using Laplace transfer functions, differential equations, conditionals (IF-THEN-ELSE), state variables, branching and other functions. Difficult models such as DACs, track and hold amplifiers, pulse width modulators, VCOs, and digital filtering functions can be accomplished easily. Several examples and analyses are presented.

087 Digitally Programmable Continuous Time Linear Phase Lowpass Filter for Hard Disk Drives

Geert DeVeirman and Richard Yamasaki

This lecture discusses the filter and equalizer requirements of hard disk drives using constant density recording techniques, as well as a single chip solution suitable for data rates up to 24 Mbits/s. The major building blocks in

the read channel are briefly described and the desired filter specifications are addressed in detail. This is followed by a discussion of continuous-time integrated filter design, primarily focusing on the transconductance-capacitor approach. The main difficulties and performance limitations related to the IC process are outlined.

FRIDAY MORNING

Tutorials 8:30-12:00

091 Electrical Effects of Packaging, Connectors, PCBs, MCMs and Backplanes on IC and System Designs

Paul K.U. Wang, Dileep Divekar, F. Balistreri and Raj Raghuram

Transmission line effects result in signal distortion, ringing, overshoot and similar problems because of reflections and crosstalk arising from impedance mismatches, improper terminations or mutual couplings. This tutorial is designed to allow digital/analog designers to become familiar with transmission lines, mixed-signal simulation and the interaction between nonlinear ICs and transmission lines. Available public domain and commercial modeling and simulation programs are reviewed and the strengths and weaknesses of different approaches to transmission line modeling and simulation of ICs and packaging, traces, connectors, PCBs and multichip modules are covered.

092 DSP Techniques in Mixed-Signal Testing

Joseph A. Mielke

This tutorial is an introduction to the verification and test of mixed-signal devices. The major emphasis in this session is on digital signal processing (DSP) techniques used for mixed-signal testing and their implementation in a test system. The techniques presented include Fast Fourier Transforms, histograms, noncoherent digitizing, sampling theory and coherent test methods. The Fast Fourier Transform with coherent testing is presented to find the signal-to-noise ratios and harmonic distortion. The use of histograms and coherent testing to find the offset error, gain error, and linearity errors are also explained.

TECHNICAL PROGRAM FRIDAY

Workshops 8:30-10:15

093 Simulation and Device Modeling

Stephan Ohr and Mike Donlin, Moderators

No matter what their claims to speed and accuracy, the best analog and mixed-signal simulators will depend on complete and accurate device or ASIC cell models. But not everyone agrees on who should provide these models or what they should include. On one hand, simulation tool vendors will work hard to control their intellectual property. And while behavioral or block-level models are accused of replacing calculated behavior with algorithmic approximations—of sacrificing accuracy for simulation speed—Spice models distributed by ASIC vendors are often neutered to protect proprietary process information. This panel explores how good the available device models might be, and alternatives for filling gaps. Panelists include authorities in modeling and simulation, and some formidable analog and mixed-signal ASIC vendors.

094 How to Work With an ASIC Vendor

Alan Gorlick, Moderator

Several leading ASIC vendors give their views on the most important factors leading toward success in mixed-signal design. The role of technology, design tools, cell libraries, systems-level expertise, and vendor-customer relationships will be prioritized and discussed. Differences between ASIC vendors who interpret their role as primarily “silicon suppliers,” and those who see themselves as “design partners,” will frequently affect the complexity of designs undertaken, the NRE costs, and chances given to first-time success. Panelists will include representatives from Harris, Texas Instruments, NCR, AT&T Microelectronics, and Gould/AMI.

Lectures 11:15-12:15

101 Benchmarks, Benchmarking and Other Forms of Deception

Hal Alles

Every CAE tool is engineered to perform a particular task in a particular way. Digital, analog and mixed-signal

simulators are especially difficult to benchmark because a complex set of tradeoffs are required to achieve state-of-the-art performance. A well-conceived benchmark can predict the value of the simulator in a particular design environment while a poor benchmark can lead to a costly mistake. This lecture covers some of the engineering trade-offs made in developing simulators and how benchmarks might hide or expose potential problems. A list of rules, practices and pitfalls is provided.

102 CMOS Processes for Mixed-Signal Applications

Richard Hester, Lou Hutter and Johnson Lin

CMOS has become the preferred digital process for its combination of high-speed, high packing density and low power consumption. But the process has frequently been overlooked for analog applications. CMOS can be used to build high-resolution mixed-signal devices, and, as this presentation points out, op amps with high gain-bandwidth products. When integrated on the same chip with an ADC and a microprocessor, these CMOS op amps form the signal conditioning front-end for thoroughly integrated controller ICs.

103 Progress in Developing an Analog HDL

Stephan Ohr

Currently, efforts to construct an Analog Hardware Description Language (AHDL) are driven by a Darpa-funded project to construct a MIMIC (microwave) HDL. This doesn't necessarily mean that an AHDL will reflect microwave design constructs, but it will reflect the preferences of MHDL committee members; in particular, the desire to link existing analog and microwave toolsets together through a vendor-independent framework and windows environment. This presentation discusses the latest thinking driving MHDL.

104 Simulating Phase-Locked Loops in Spice

Thierry Roullier and Rich Davis

Phase-locked loops represent one of the more difficult analog simulation problems because of the wide range of time constants within such a circuit. This paper presents a behavioral modeling technique for analyzing the steady-state operation of phase-locked loops that does

not require enormous amounts of computing power. Although the technique can benefit from the use of a behavioral modeling language, it's not absolutely necessary and the technique is compatible with generic versions of Spice. The advantages and limitations of the technique are discussed as well as work-arounds that may be necessary.

105 A Novel Multi-Stage Filter Design Technique for Low Sampling Rate and High-Resolution Applications

Sangil Park and Lew Chua-Eoan

This presentation discusses a real-time implementation of a multistage half-band filter structure to enhance the effective resolution using a general-purpose digital signal processor chip. In particular, a series of six half-band filters is implemented to obtain more than 18 bits of effective resolution from a digital signal with 12-bit dynamic resolution. The number of stages in the decimation process can be adjusted to fit the needs of a specific application and the oversampling methodology can be used to achieve more than 120 dB of SNR.

FRIDAY AFTERNOON

Lectures 1:45-2:45

111 Handling Delay, Noise and Power Problems in ASICs Using Automatic Place and Route Tools

Guido Arnout

Because of time-to-market pressures, the system designer must get involved in the physical design (place and route) of high-performance and mixed-signal chips. This lecture addresses issues of floorplanning to achieve minimum die size when mixing analog and digital circuitry; segregation of analog and digital functions to limit interference or noise; automatic power supply routing and tapered supply lines; gridless routing; multiple-width routing and multilayer routing; timing-driven layout and the backannotation needs of mixed analog and digital designs.

112 Analog-Verilog Quasi Mixed-Signal Simulation Model for ADCs

Michael K. Mayes

Separate simulation of the analog and digital blocks in an ADC may lead to undetected design errors at the interface between the two domains. Rather than use a mixed-signal simulator, an analog library of capacitors, resistors, multiplexers, and comparators has been developed for Verilog, a digital simulator. Complex ADC architectures are simulated using Verilog where analog voltages are replaced with vector quantities such as resistor ladders and capacitor arrays. This quasi analog-Verilog simulation model provides the circuit designer with a simple method of architecture verification.

113 Smart Power Processes for LSI Circuits

Carlo Cini

The integration of power driving circuits and complex control logic on the same chip requires a BCD process technology with high density and very low power dissipation. Smart power circuits using such a process become key motion-control components in printers, disk drives and fax machines. In automotive applications, smart power devices serve as engine controls, remote mirror, and passenger climate controls. This lecture describes the characteristics of smart power technologies and provides real examples of circuits that exploit the power LSI approach. In addition, available partitioning options are discussed.

114 Implementing Concurrency in Mixed-Signal IC Design and Test

Bruce Webster

Linking design and test databases can speed product development by allowing test program development to run in parallel with design, rather than waiting for real silicon. The problem of mixed-signal design/test integration is being tackled on two major fronts: top-down test program development in which mixed-signal simulators are being augmented with the ability to model devices against specific types of tests and to transfer the simulation results through coded test program templates; and design/test simulation integration to provide program-defined test events in a format usable by

design simulators. This lecture discusses these approaches and the modeling issues they have in common.

115 Simulation of Switched Capacitor Filters

Mojo Chian

Modern nonlinear signal processing and conditioning circuits consist of switched capacitor blocks with the clocks and input signals supplied by analog and/or digital blocks. Traditionally, the only viable approach to the nonlinear transient simulation of such mixed switched cap, analog and digital circuits was to use macro/behavioral models for the op amps and switches in the switched cap block and then simulate the entire circuit with a circuit simulator. This presentation reviews these traditional approaches as well as a new switched capacitor analysis algorithm designed to operate in a mixed-signal simulation environment.

116 BiCMOS Processes for Mixed-Signal Devices

Eric Wildi

BiCMOS options go far beyond the much-discussed speed enhancements for digital ICs. This lecture focuses on how to choose the best process for a particular application, including the choice of primarily digital ICs with analog interface, as well as mixed-signal ICs optimized for medium to high-performance analog, which can't be achieved with a 5-V supply. Issues addressed include noise, thermal interaction, process compatibility and subtle parasitics.

Lectures 3:15-4:15

121 Behavioral Modeling Techniques in the Analysis of a Bipolar IC

Peter Denyer

Behavioral models can mitigate the excessive run times typically encountered in analog-only simulation. These models can also be used to develop a test bench environment, allowing a consistent set of test information to be applied to all levels of abstraction for the circuit under development. This can result in considerable savings in analysis time. As an example, attention is focused on one of the many analysis requirements in the design of a mixed-signal bipolar integrated circuit.

123 ADCs for Microprocessor Systems

Jean-Yves Michel

Designing ADCs inside microprocessor systems is difficult because any analog function requires special attention when mixed with digital functions on the same board. What's more, ADCs usually require a large overhead of hardware (digital and analog glue circuits) and a large overhead of software because they're slow and asynchronous. This paper describes the ADCs available, from the bare-bones ADC to the analog interface chip and shows how the latest types can greatly reduce hardware and software costs. These interface circuits, which look more like microprocessor peripherals than converters, reduce the software overhead and offer flexibility and ease of integration.

124 A Macromodel Compiler for Op Amps

Jean Remy and Christian Caillon

A new top-down design methodology provides fast and accurate macromodels for the simulation of large analog and mixed-signal circuits. A one-pass compiler, using parameters extracted from a cell library or detailed data sheet, automatically generates macromodels for large analog circuit blocks, such as op amps, AGCs and VCOs. This top-down methodology offers simulation speed improvements of 5x to 40x. This improvement in simulation speed allows designers to make rapid system-level assessments for the performance of a new circuit.

That's all for this year,
but there will be
more in 1992.

The second annual
**Analog &
Mixed-Signal
Design Conference**
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Don't miss it!

PROGRAM AT A GLANCE

WEDNESDAY

KEYNOTE ADDRESS 9:00 - 10:00

020 Impact of Mixed-Signal ASICs on Design and on System Designers Cornell

LECTURES 11:00 - 12:00

021 Unscrambling the Mixed-Signal Market Stansberry
 022 Disk Drive Controllers Vashi
 023 An Overview of Oversampling Data Converters Hauser
 024 Hierarchical Design Using a New Mixed-Signal Simulation Technique Raghuram, Balistreri, Divekar & Wang
 025 DSP Simulation of Mixed-Signal Systems Kallara
 026 Analog Memory in Cellular Telephone Applications Simko & Jarrett
 027 Safe Operating Area: Interfacing to the Real World Marshall, Devore, Efland, Jones, Summerlin, & Mings

TUTORIALS 2:00 - 5:30

031 Spice Modeling Hines
 032 Monolithic ADCs Stoian & Lacanette

LECTURES 2:00 - 3:00

033 Power Supply Design for Portable Systems Dekis
 034 Digital Video Encoding Standards and Techniques Kneiss
 035 Microstepping of Hybrid Step Motors Hunt & Roy
 036 Integration of DSP and Data Acquisition Functions: Chip and System-Level Considerations Ehlig
 037 Digital Noise Management Techniques to Realize 16-Bit A/D/A Converter Performance Scott

WORKSHOPS 3:45 - 5:30

041 Impact of Mixed-Signal Simulation on Design Methodology Klein
 042 Analog Switches and Multiplexers Armijos

LECTURES 3:45-4:45

043 Understanding Semi-Custom Alternatives Fields
 044 Designing Front-Ends for Voice Band Modems Yeung

THURSDAY

TUTORIALS 8:30 - 12:00

051 Issues in Mixed-Signal ASIC Design Cassidy, Tyson, Curran & Gazeley
 052 Understanding Data Converter Frequency Domain Specifications Leonard

WORKSHOPS 8:30 - 10:15

053 Understanding Mixed-Mode Simulators Chadwick
 054 Filter Design TBA
 055 Basics of Power Supply Design Garrett

LECTURES 11:15 - 12:15

061 Spectre: A New Approach to Mixed-Signal Simulation Kundert
 062 Automated Generation and Simulation of Macro/Behavioral Models Vogelsong, Morency & Chian
 063 Applications of Sigma-Delta (Bitstream) Converters Aine
 064 Optimizing High Frequency Amplifier Bandwidth Buxton
 065 Advanced Graphics Back-End System Architecture Davoody & Yin

LECTURES 1:45 - 2:45

071 Analog Behavioral Modeling of Op Amps Sanders & Tu
 072 Diablo: An Analog Behavioral Modeling Tool Nosrati & Horwitz
 073 Simulation Algorithms Griffeth
 074 Choosing DACs for Direct Digital Synthesis Buchanan
 075 Complementary Bipolar Processes for High Performance Analog ASICs Parks
 076 Managing and Reducing Risk When Selecting Mixed-Signal Tool and Silicon Vendors Gorlick
 077 Using Spreadsheets for Analog/Digital Design Smith

WORKSHOPS 3:30 - 5:15

081 Digitizing Analog Functions Richard
 082 Who Really Won BCTM? Ohr
 083 Who Are Mixed-Signal Design Tools Intended For? Tuck

LECTURES 3:30 - 4:30

084 Mixed-Signal ICs in Imaging and Graphics Jack
 085 Optimization and Design Centering to Improve Yield and Performance Doganis & Jennings
 086 Profile: A Spice-Based Analog and Mixed-Signal Modeling Language Lee
 087 Digitally Programmable Continuous Time Linear Phase Lowpass Filter for Hard Disk Drives DeVairman & Yamasaki

FRIDAY

TUTORIALS 8:30 - 12:00

091 Electrical Effects of Packaging, Connectors, PCBs, MCMs and Backplanes on IC and System Designs Wang, Divekar, Raghuram, & Balistreri
 092 DSP Techniques in Mixed-Signal Testing Mielke

WORKSHOPS 8:30 - 10:15

093 Simulation and Device Modeling Ohr & Donlin
 094 How to Work With an ASIC Vendor Gorlick

LECTURES 11:15 - 12:15

101 Benchmarks, Benchmarking and Other Forms of Deception Alles
 102 CMOS Processes for Mixed-Signal Applications Hester, Hutter, & Lin
 103 Progress in Developing an Analog HDL Ohr
 104 Simulating Phase-Locked Loops in Spice Roullier & Davis
 105 A Novel Multi-Stage Filter Design Technique for Low Sampling Rate and High-Resolution Applications Park

LECTURES 1:45 - 2:45

111 Handling Delay, Noise and Power Problems in ASICs Using Automatic Place and Route Tools Arnout
 112 Analog-Verilog Quasi Mixed-Signal Simulation Model for ADCs Mayes
 113 Smart Power Processes for LSI Circuits Cini
 114 Implementing Concurrency in Mixed-Signal IC Design and Test Webster
 115 Simulation of Switched Capacitor Filters Chian
 116 BiCMOS Processes for Mixed-Signal Devices Wildi

LECTURES 3:15 - 4:15

121 Behavioral Modeling Techniques in the Analysis of a Bipolar IC Denyer
 123 ADCs for Microprocessor Systems Michel
 124 A Macromodel Compiler for Op Amps Remy & Caillon

REGISTRATION INFORMATION

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Take advantage of our early bird discounts. Save up to \$100 by returning your registration form today. The full registration rate is \$495. Early and group registrations earn additional savings on the already low fee:

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To qualify for a registration discount, payment (or government purchase order) must be postmarked before the cut-off date. Space at the conference cannot be confirmed until payment is received. We will be happy to take your registration without payment and invoice you for the balance due.

CANCELLATIONS




Cancellations with full registration refunds will be accepted if they are received in writing by October 19, 1991. No shows will be liable for 100% of the registration fee.

WHEN TO CHECK IN

All conference materials including your badge, program, and proceedings should be picked up at the Conference Registration Desk in the Santa Clara Marriott between 7:00 and 9:00 am Wednesday, October 30. Late arrivals can check in through 4:00 pm Wednesday.

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You can register any of these three ways:

-  **1. FAX** your registration form and class selections to Pat Clarke at (503) 624-2904.
-  **2. CALL** Pat to register over the phone at (503) 624-2118.
-  **3. MAIL** a registration form to Analog & Mixed-Signal Design Conference
c/o Classic Data Systems
17300 SW Upper Boones Ferry Rd.
Portland, OR 97224

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OCTOBER 30–NOVEMBER 1, 1991
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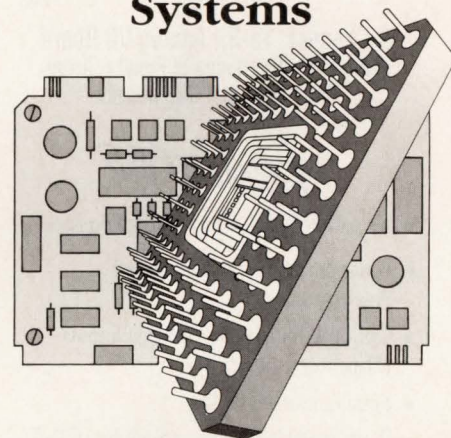
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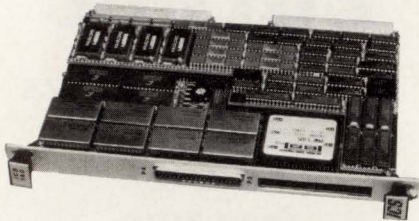
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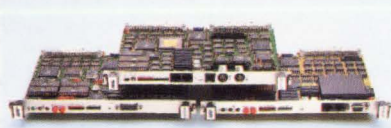
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