PCI 9610

64-bit/66MHz PCI I/O FlexPORT Chip

Highlights

- 64-/32-bit PCI v2.2 Bus Master Interface Chip supports up to 66MHz and allows PCI↔Local Bus data transfers up to 528 MB/s
- Four Independent DMA Channels provide Flexible Prioritization Scheme and Bi-directional Mastering
- Advanced DMA Functions including Scatter/Gather List Management, Demand Mode, Shuttle Mode, and Block Mode
- Robust PCI Initiator supports Configuration Cycles, Programmable Burst, Unaligned Transfers and Endian Swapping
- Advanced Programmable PCI Arbiter
- PCI Target support includes Multiple Address Spaces, Dynamic Local Bus Width, Read Prefetching, and Endian Swapping
- Enhanced PCI Messaging Unit includes Mailboxes, Doorbells, Doorbell Queues, Strong Ordered Transactions, and I2O Messaging
- Memory Fat Pipe allows 32-bit Local Bus Designs to achieve 64-bit Burst Data Transfers between the PCI and Local Bus Interleaved Memory
- Adaptive FIFO Architecture for Efficient Channel Memory Utilization
- Local Bus Asynchronous Operation supports Direct Interface to Motorola MPC8260, MPC 850/860, PPC 603e, PLX IOP 480, Intel i960Hx,Cx, Jx RISC processors
- Exceptional Interrupt Handling including PCI v2.2 Message Signaled Interrupts
- PICMG v2.1, CompactPCI Hot Swap Friendly
- 3.3 V/5V Tolerant CMOS in 27x27mm 328-ball PBGA Package with JTAG

The mission is clear: get your data there faster and wider. The PCI 9610 64-bit/66MHz I/O FlexPORT™ bus master interface chip from PLX Technology, Inc., achieves this task by enabling a wide variety of 64- and 32-bit RISC processors, memory, and I/O to exist within 64-bit and 66MHz systems. The PCI 9610 builds upon PLX's industry leading PCI I/O Accelerator products and extends the Data Pipe Architecture™ technology to new performance levels with FlexPORT enhancements.

Motorola® MPC8260 PowerQUICC® II Designs

The 3.3v PCI 9610 is a perfect fit for networking and telecommunications applications using the MPC8260 PowerQUICC II available from Motorola. Through the enhanced PLX Data Pipe Architecture technology, the PCI 9610 enables the PowerQUICC II architecture to achieve its maximum performance potential in PCI applications.

Moving up to 64-bits and 66MHz

The PCI 9610 provides a platform for scaleable migration of 32-bit PCI and Local designs up to full 64-bits and 66MHz. The flexible PCI 9610 supports a variety of bus widths and speeds in order to maximize the flow of data particular to your PCI or CompactPCI® application.

FlexPORT Technology

The new FlexPORT technology is an extension of the proven Data Pipe Architecture available exclusively through PLX products with two major enhancements: (1) the Memory Fat Pipe feature allows users of 32-bit processors to achieve 64-bit performance up to a full 528 Mbytes/sec and (2) the Adaptive FIFO Architecture optimizes the burst transfer performance of your application.

The PCI 9610 continues the tradition of flexibility and performance that have made PLX PCI interface chips the gold standard of the industry.

PCI 9610 I/O FlexPORT

The PCI 9610, a 64-bit 66MHz Bus Master I/O FlexPORT interface chip is the most advanced general purpose bus master device available. It offers a robust PCI v2.2 specification implementation enabling burst transfers up to 528 Mbytes/second. Based on PLX's Data Pipe Architecture technology, the PCI 9610 I/O FlexPORT elements bring you such features as the Adaptive FIFO Architecture, Memory Fat Pipe, quad DMA engines, programmable PCI Initiator and Target data transfer modes, and PCI messaging functions.

Data Pipe Architecture

Quad DMA channels

- Four independent channels provide flexible prioritization scheme and bi-directional mastering
- Demand mode DMA operation
- Block mode DMA operation
- End of Transfer (EOT) signal
- Programmable burst length including unlimited burst
- Unaligned transfer support
- Endian swapping
- Supports PCI bus mastering from local-slave only devices
- Flexible scatter/gather list management
  - Descriptors may be located in PCI or Local Bus memory
  - Support for long and short descriptor formats
  - Fast DMA descriptor load capability
  - Shuttle mode DMA channel support
  - Automatic invalidation of used DMA descriptors
  - Provides independent scatter/gather list management per channel

PCI Initiator

- Type 0 and Type 1 configuration cycles
- All PCI Memory and I/O cycle types supported
- Initiator READ prefetching per address space
- Programmable burst lengths
- Programmable threshold pointers
- Unaligned transfer support
- Endian swapping
- Read-Around-Writes and Write-Around-Reads support
- Advanced PCI arbiter with programmable round robin scheme.

PCI Target

- Multiple independent address spaces
- Dynamic local bus width control
- Target READ prefetching per address space
- Endian Swapping
- Local Bus priority control
- Programmable threshold support, including latency timer
- PCI-to-Local Delayed Read mode.
- Local-to-PCI Deferred Read mode.

PCI Messaging Unit

- Mailbox and doorbell registers
- Doorbell queues support strong ordered transactions
- Independent I_2O messaging unit, including pull model, for I_2O or custom protocols

I/O FlexPORT enhancements to the Data Pipe Architecture

Memory Fat Pipe

- Allows 32-bit Local Bus designs to achieve 64-bit burst data transfers between PCI and Local bus interleaved memory

Adaptive FIFO Architecture

- Eight FIFO channels which are used for Initiator, Target, and DMA operations
- Total memory pool of 1280 bytes or 160 Qwords may be dynamically allocated among FIFO channels

PCI 9610 Applications

High Performance Motorola MPC8260 PowerQUICC II Designs

The PCI 9610 is ideally suited for MPC8260 PowerQUICC II based 64- or 32-bit PCI or CompactPCI adapters in networking and telecommunications applications such as WAN/LAN controller cards, high speed modems, frame relay cards, and networking cards for routers and switches, among others. In addition to directly supporting the MPC8260 and PowerPC® 60x processor bus, the PCI 9610 enhances the interface by providing features like bi-directional mastering capability, and unlimited burst capability through the use of the Data Pipe Architecture technology, maximizing the performance envelope of your communications design.

Migrating to 64-bit/66MHz PCI and Local Bus Designs

In addition to supporting the MPC8260, the PCI 9610 enhances PLX's industry leading support for the Motorola MPC 860/850 PowerQUICC family of RISC processors. The Memory Fat Pipe feature enables MPC860 designers to achieve 64-bit performance in PCI applications by providing a full data transfer width of 64-bits between the PCI and Local bus using interleaved memory. The PCI 9610 incorporates the necessary hardware control support for the Memory Fat Pipe design. This allows cost and space sensitive 32-bit designs to be quickly ported to 64-bit bus designs.

The PCI 9610 allows for scalability in your approach to high performance design. The implementation options available

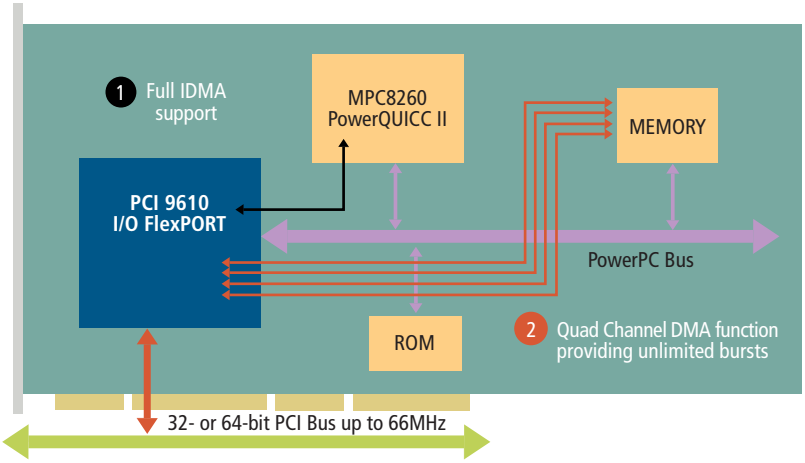


Figure 1. MPC8260 PowerQUICC II Adapter Design

through the exclusive Adaptive FIFO Architecture allow for optimum bus utilization and can operate in various combinations of bus widths and speeds, including 32-bit/33MHz, 32-bit/66MHz, 64-bit/33MHz, and 64-bit/66MHz on both the PCI and Local busses.

Furthermore, users of PLX's 32-bit I/O Accelerator line, including the PCI 9080 or PCI 9054 interface chips, and their associated Reference Design Kits (RDKs) and Software Development Kits (SDKs) have the added benefit of easily migrating their designs up to 64-bits and 66MHz.

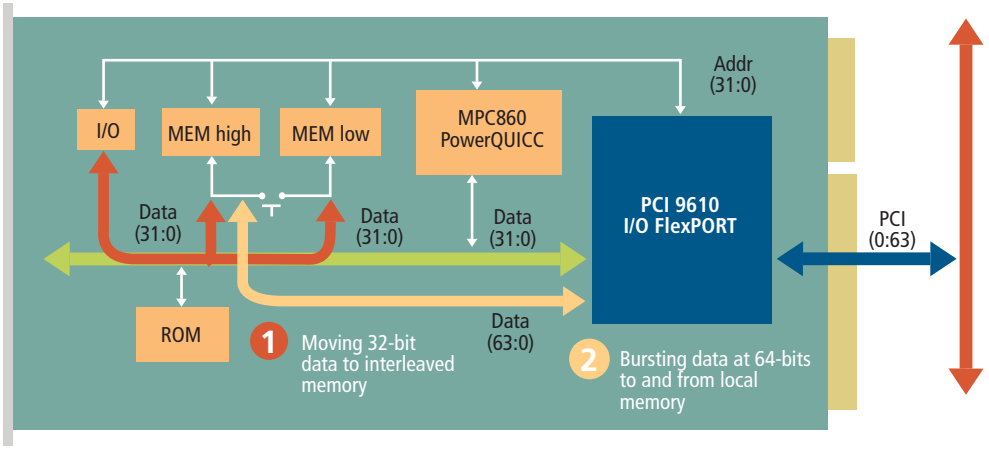


Figure 2. Memory Fat Pipe CompactPCI Adapter design

PCI Bus Embedded Host Designs

In addition to supporting adapter card designs, the PCI 9610 is also ideally suited for PCI bus embedded host designs using the PowerQUICC II or other 64- or 32- bit RISC processors. These applications include remote access servers, network switches and routers, PBX boxes, cellular base stations, storage, imaging, data encryption, and others requiring the high bandwidth PCI bus. In this configuration, the PCI 9610 is capable of supporting Type 0 and Type 1 PCI configuration cycles, allowing the PCI 9610 to configure other PCI devices or cards in the system. The on-board programmable PCI arbiter supports a variety of schemes, including round robin and fixed priority.

Additional Features

General Purpose Bus Master Operation

- 64-Bit PCI address spaces – supports 64-bit PCI address spaces. When in 32-bit mode, Dual Address Cycles (DAC) provide access beyond the 4 GB boundary
- 3.3 and 5 volt operation – requires 3.3 volt V_{CC}. Provides 3.3 volt signaling with 5 volt tolerance on the PCI and Local Busses allowing universal PCI implementations
- I_2O compatible messaging unit – enables I_2O IOP designs to communicate with other I_2O supported devices using push model or pull model implementation
- Programmable interrupt controller – contains an advanced programmable interrupt controller and supports PCI v2.2 Message Signaled Interrupts
- Serial EEPROM Interface – contains a serial EEPROM interface that can be used to load configuration information from serial EEPROMs. This is useful for storing information that is unique to a particular adapter (such as Network ID or Vendor ID).
- Programmable Prefetch Counter – can prefetch data during Target and Initiator read operations, programmable per address space. The prefetch size can be programmed to match the initiator (CPU) burst length, or can be used as Read Ahead mode data.
- Continuous Prefetch Mode – can prefetch until the FIFO is full
- Posted Memory Writes – supports the Posted Memory Writes (PMW), required by PCI v2.2
- New Capabilities Structure – supports new capabilities registers to define additional capabilities and functions

Local Bus Operation

- PPC Mode operation – interface to the Motorola PowerQUICC II and PowerPC 603e/7xx family of 64-bit RISC processors. PowerPC local bus arbitration is provided for up to three bus masters.
- M Mode operation – interface to the Motorola MPC 850/860 RISC processors
- C and J operation modes – interface to the PLX IOP 480, as well as Intel i960Hx, Cx and Jx families
- Programmable Local Bus wait states

PCI Bus Operation

- Subsystem and Subsystem Vendor IDs – contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration Register Space in addition to System and Vendor IDs
- VPD support – supports the Vital Product Data (VPD) PCI extension
- CompactPCI Hot Swap Friendly – as defined in the PICMG registered CompactPCI Hot Swap Specification

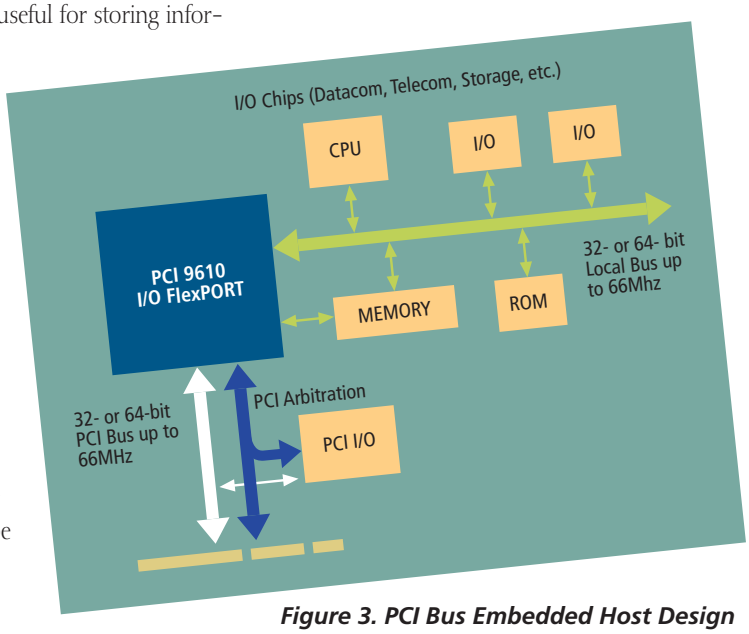
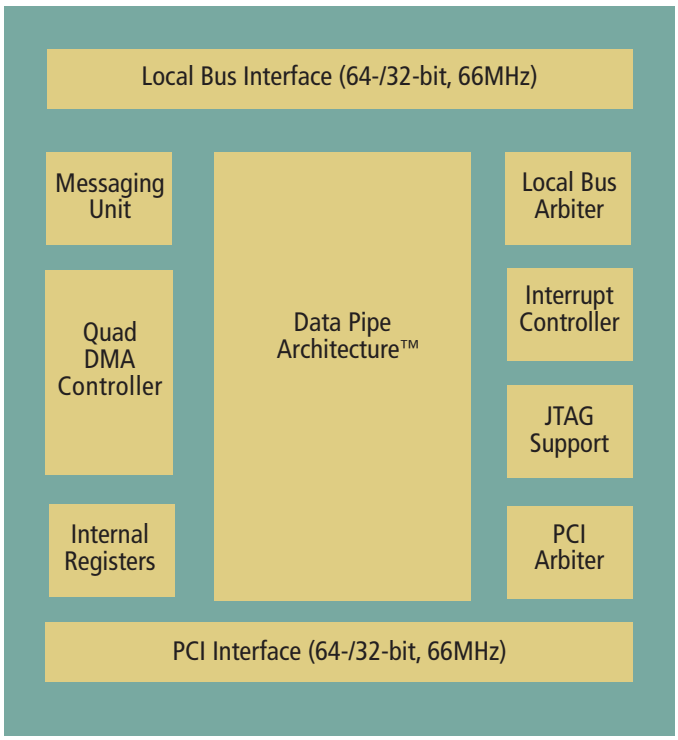


Figure 3. PCI Bus Embedded Host Design



PCI 9610 Internal Block Diagram

Development Tool Support

PLX applies a highly systematic approach to silicon technology and recognizes that software often represents the largest investment in development. The PCI 9610 is the silicon platform by which 64-bit and 66MHz designs are achieved. The silicon platforms from PLX are supported by a variety of development tools to assist the designer. Reference Design Kits (RDK) and Software Development Kits (SDK) are available to enable designers to quickly bring new designs to production without worrying about the complexities of implementing PCI.

The PCI 9610 is fully compatible with PLX's PCI SDK and I_2O SDK software development kits which allow simple and painless development of high performance local and PCI software through standard APIs, I_2O messaging protocols, PCI debug tools, and example drivers.

PCI 9610 design support is provided through RDKs which provide a flexible PCI development board, complete with OrCAD® schematics, documentation, and software.

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Product Ordering Information

PCI 9610	64-bit/66MHz PCI to Local Bus Master I/O FlexPORT Chip
CompactPCI 9610RDK-860	PCI 9610 Reference Design Kit, Motorola MPC860 PowerQUICC CPU
PCI 9610RDK-8260	PCI 9610 Reference Design Kit, Motorola MPC8260 PowerQUICC II CPU
PCI SDK	PCI Software Development Kit
I_2O SDK	I_2O Software Development Kit