A. Product Status

The scope of this document encompasses the PCI 9080-3

Product status	Description	Samples	Production	Collateral Documentation
PCI 9080-3	Fixes selected errata	31 October 1997	January 1998	Technical update rev 08
				Data sheet v1.04

B. PCI 9080 Design Note

1. Recover from a Master Abort during a Non-Chain DMA operation:

When the master or target abort condition occurs during a Non-Chain DMA operation, the PCI 9080's DMA controller can be recovered by performing these steps in sequence:

a. Set the Abort bit to 1 in the DMA Channel Control/Status register (LOC 128h bit 4, LOC 129h bit 4)
b. Clear the Master or Target Abort bit in the PCI Command/Status register (LOC 6h bit 13 or bit 11)
c. Configure the DMA Configuration Registers to start a new DMA operation

2. Recover from a Master Abort during a Chain DMA operation:

When the master or target abort condition occurs during a Chain DMA operation, the PCI 9080's DMA controller can be recovered by performing these steps in sequence:

a. Set the Software Reset bit to 1 (LOC ECh bit 30) – the Local Configuration Registers and DMA registers get reset
b. Clear the Software Reset bit by writing 0 to this bit
c. Reload the Local Configuration Registers from the Serial EEPROM by writing a 1 to the Reload Configuration Registers bit (LOC ECh bit 29) or from the Local bus master
d. Configure the DMA Configuration Registers to start a new Chain DMA operation

3. DMA Done PCI Interrupt

The PCI 9080 can be programmed to generate either Local or PCI interrupt when a DMA operation is done. To select PCI Interrupt:

a. Set DMAMODE0, LOC100h or DMAMODE1, LOC 114h bit 10 to 1 – Done Interrupt Enable bit
b. Set DMAMODE0, LOC100h or DMAMODE1, LOC 114h bit 17 to 1 – DMA (PCI) Interrupt Select bit
c. Set INTCSR, LOC E8h bit 8 to 1 – PCI Interrupt Enable bit
d. Set INTCSR, LOC E8h bit 18 or bit 19 to 1 – Local DMA Channel 0 (or Channel 1) Interrupt Enable bit

When the DMA operation is finished (DMACSR0, LOC 128h or DMACSR1, LOC 129h bit 4 -DMA Done bit is set), PCI 9080 generates PCI interrupt. The status bit in INTCSR, LOC E8h bit 21 or bit 22 is also set to indicate DMA channel 0 or DMA channel 1 interrupt is active.

If the Local DMA Channel 0 (or Channel 1) Interrupt (INTCSR, LOC E8h bit 18 or bit 19) bit is mistakenly not enabled, PCI 9080 still generates the PCI interrupt. However, the status bit in INTCSR, LOC E8h bit 21 or bit 22 will not get set. The ISR (Interrupt Service Routine) might not be able to clear the interrupt since the source of the PCI interrupt can not be identified.