PCI 9060/403 AN

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Version 0.4

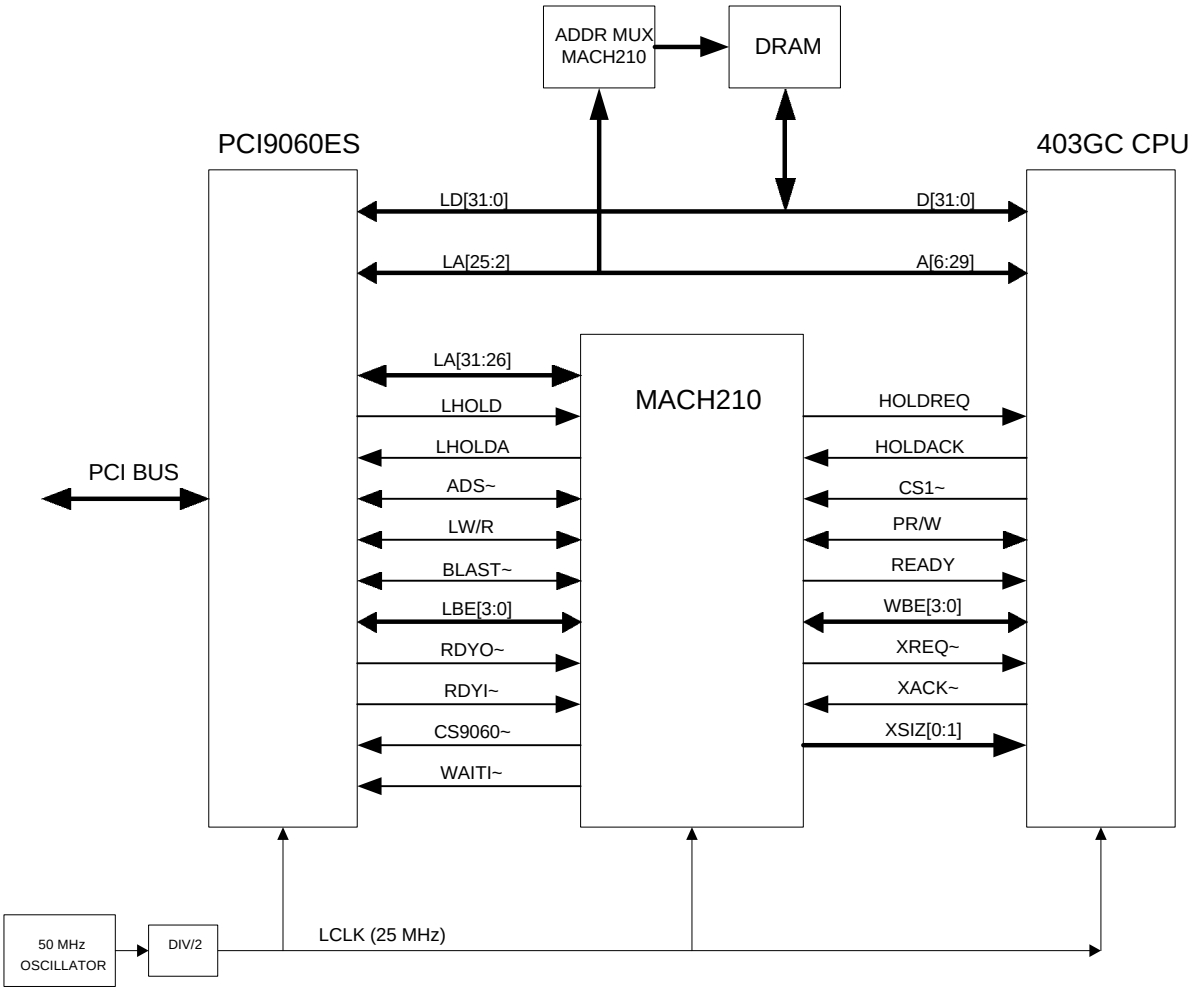
PowerPC 403 to PCIbus Application Note

Features

- Embedded system containing PowerPC 403 with a PCIbus interface
- PCI 9060ES chip supports master, slave and PCI configuration cycles
- 403local bus runs asynchronously to the PCI clock.
- FIFOs in PCI 9060ES support continuous burst transfers between 403 local bus and PCIbus

General Description

This application note describes how to interface the PowerPC 403GC CPU to the PCI bus using the PLX PCI9060ES PCI to Local Bus Bridge chip. The PCI9060ES has both direct master and direct slave transfer capabilities. The direct master mode allows a device (403GC) on the local bus to perform memory, I/O and configuration cycles to the PCI bus. The direct slave mode allows a master device on the PCI bus to access memory (DRAM) on the local bus. **The 403GA may also be used with little or no modification to the design.**



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1. Introduction

This application note describes how to interface the PowerPC 403GC CPU to the PCI bus using the PLX PCI9060ES Local Bus Bridge chip. **The 403GA may be used in place of the GC with little or no modification to the design.** (Contact PLX for more information). The PCI9060ES has both direct master and direct slave transfer capabilities. The direct master mode allows a device (403GC) on the local bus to perform memory, I/O and configuration cycles to the PCI bus. The direct slave mode allows a master device on the PCI bus to access memory (DRAM) on the local bus. The PCI9060ES allows the local bus to operate asynchronously to the PCI bus through the use of bi-directional FIFOs. In this application the PCI bus operates at 33 MHz while the local bus is clocked at 25 MHz. The following block diagram shows the basic connections between the major components required for this application.

IMPORTANT NOTE ABOUT REVISION 0.3: The design in Revision 0.3 (this revision) of this application note allows 16 word bursting. In Revision 0.1 the design allowed only four word bursting. To achieve this improvement, the design was changed from using two Mach 210's (Rev 0.1 design) to one Mach 210 and three 16V8's. The PAL equations and schematics included with this application note reflect the changes. However, the text and timing diagrams still reflect the 0.1 (4 word burst) operation. Although the differences are minor, this is noted to avoid confusion. PLX is now updating the text and timing diagrams to reflect the change from four word burst to 16 word burst.

Note that the address and data buses on the 403GC designate bit 0 as the **most** significant bit. Also, the 403GC does not produce the upper 6 address bits, so its maximum addressing range for one bank is 64 Mbytes.

NOTE: PLX provides a "Technical Update", available from the FTP site on the Web page that contains design notes, spec updates and errata on the PLX chips. All designers should obtain this information when performing a design. The web page is atwww.plxtech.com. Contact PLX by e-mail, phone or fax for the FTP passwords.

2. Direct Master Mode

2.1 Overview

In the direct master mode, the 403GC can access the PCI bus using memory, I/O or configuration cycles. One of the 8 available memory banks provided by the 403GC is used to access the PCI bus through the PCI9060ES.

There are also a number of local configuration registers in the PCI9060ES which must be programmed by the 403GC before accesses can be made to the PCI bus. These configuration registers define base addresses, address ranges, and local bus characteristics.

2.2 403GC Bank Register

One of the eight 403GC bank registers is used to access the PCI9060ES. The size of this bank register should be programmed to 64 Mbytes to provide the largest possible window into the PCI address space. The 64 Mbytes is then subdivided into three spaces:

- Internal PCI9060ES Local Configuration Registers
- PCI I/O or Configuration Cycles
- PCI Memory Cycles

In this application, the first 16 Mbytes is allocated to configuration registers, the second 16 Mbytes to I/O and configuration cycles, and the last 32 Mbytes to PCI memory cycles. Other configurations are possible if more 403GC bank registers are used, or if the resolution of the address space decoder is increased. Following is a suggested configuration for the bank register used to access the PCI9060ES:

Configuration Bit	Suggested Value	Description
31 (SD) SRAM	1	SRAM style interface
30:28 (TH)	000	Transfer hold count
27 (WFB)	0	Write byte enable off timing
26 (WBN)	0	Write byte enable on timing
25 (OEN)	0	Output enable on timing
24 (CSN)	0	Chip select on timing
23:18 (TWT)	00000	Transfer wait
17 (RE)	1	Ready Enable
16:15 (BW)	10	Bus Width (32 bits)
14 (BME)	0	Burst mode enable (disabled)
13 (SLF)	1	Sequential Line Fills
12:11 (BU)	11	Bank Usage (R/W)
10:8 (BS)	110	Bank Size (64 Mbytes)
7:0 (BAS)	user defined	Bank Address Select

2.3 Bursting

Since the 403GC only performs burst cycles when accessing cached memory, this bank will not be configured for bursting. Also, the 403GC gives no indication during a cycle that it is performing a burst. Therefore, BLAST (end of burst) will always be asserted into the PCI9060ES during direct master or internal register cycles. The PCI9060ES does support bursting to the PCI bus if the master of the local bus is capable of bursting to the local side of the PCI9060. Applications which have a DMA controller on the local bus could utilize the direct master bursting feature of the PCI9060ES.

2.4 Read Cycles

A direct master or configuration read cycle is initiated by the 403GC when it asserts the chip select assigned to the PCI9060 and PCI bus. It also asserts an address (A6:29), read/write status (PR/W), and byte enables (WBE[0:3]). The PCI state machine in the PCI MACH device detects this cycle and transitions to state P4 where the address is strobed into the PCI9060ES using ADS. The WBE signals are mapped into the LBE inputs to the PCI9060ES, and the PR/W signal is inverted to become LW/R. Since the 403GC only produces 26 address bits, the upper six address bits to the PCI9060ES are forced to zero.

The READY input to the 403GC is negated, causing it to insert wait states. The PCI9060ES has a WAITI~ input pin which allows a master to control the duration of the read data presented by the PCI9060ES. At the beginning of a read cycle, this input is asserted. The PCI9060ES then runs the requested PCI or internal register cycle and asserts RDYO~ when the data is available. The state machine jumps to state P6 where READY is asserted to the 403GC. Once READY has been detected, the data will be sampled by the 403GC at the end of the next clock period. The state machine jumps to state P7 where the WAITI~ signal is negated, allowing the PCI9060ES to complete the read cycle. The 403GC reads the data at the end of this cycle. The state machine returns to PIDLE and waits for another chip select from the 403GC.

2.5 Write Cycles

A direct master or configuration write cycle is initiated by the 403GC when it asserts the chip select assigned to the PCI9060 and PCI bus. As with read cycles, it also asserts an address (A6:29), read/write status (PR/W), and byte enables (WBE[0:3]). The PCI state machine in the PCI MACH device detects this cycle and transitions to state P0 where the address is strobed into the PCI9060ES using ADS. The byte enables, read/write status, and address are mapped in the same way as read cycles.

The READY input to the 403GC is negated, causing it to insert wait states. The PCI9060ES then runs the requested PCI or internal register cycle and asserts RDYO~ when the write has been completed. The state machine jumps to state P2 where READY is asserted to the 403GC. Once READY has been detected, the 403GC will complete the write cycle at the end of the next clock period. The state machine jumps to state P3 during the last clock cycle of the transfer. The state machine then returns to PIDLE and waits for another chip select from the 403GC.

2.6 PCI9060ES Configuration Registers

The following local configuration registers must be programmed before direct master accesses to the PCI bus can occur:

Register	Offset
Range for Direct Master to PCI	9Ch
Local Base Address for Direct Master to PCI Memory	A0h
Local Base Address for Direct Master to PCI IO/CFG	A4h
PCI Base Address (Re-Map) for Direct Master to PCI	A8h
PCI Configuration Address Register for Direct Master to PCI IO/CFG	ACh

These registers are accessed by running a 403GC cycle to the PCI9060ES with the 9060 chip select (CS9060~) asserted. The address offsets for each register are shown in the table.

3. Direct Slave Mode

3.1 Overview

In the direct slave mode, a master device on the PCI bus can access the DRAM which is connected to the 403GC bus. The direct slave FIFOS in the PCI9060ES allows 3-2-2-2 bursting to and from the fast page mode DRAM.

3.2 Arbitration

When the PCI9060ES has decoded and accepted a PCI cycle which is to be passed through to the local bus, the LHOLD output is asserted. This signal is passed on through the PCI MACH to the 403GC HOLDREQ input. When the 403GC is ready to release the local bus, it asserts HOLDACK. This signal is connected directly to the LHOLDA input of the PCI9060ES. The PCI9060ES now has control of the local bus, and can begin its cycle. When the PCI9060ES is finished, it negates LHOLD, thus giving the bus back to the 403GC. During burst reads, the 403GC doesn't finish the DRAM cycle until after the PCI9060ES is done, so the HOLDREQ signal is held for two extra clock cycles.

3.3 Read Cycles

A direct master read cycle is initiated by the PCI9060ES when it asserts address strobe (ADS~). It also asserts an address (A[31:2]), write/read status (LW/R), byte enables (LBE[3:0]), and burst last (BLAST~). The DRAMCTL state machine in the PCI MACH device detects this cycle and transitions to state S7 where a DRAM read cycle is initiated.

The XREQ~ and XSIZ[0:1] inputs to the 403GC are used to initiate a DRAM cycle. The XSIZ inputs are decoded as follows:

XSIZ[0:1]	Operation

00	Byte Transfer (8 bits)
01	Halfword Transfer (16 bits)
10	Fullword Transfer (32 bits)
11	Burst Fullword Transfer

The byte address is determined by the WBE2(A30) and WBE3(A31) inputs to the 403GC, and are derived from the LBE outputs of the PCI9060ES. During read cycles, all transfers are converted to full word transfers by the PCI9060ES. After the state machine asserts XREQ, it checks BLAST~ to determine if this is a single or burst transfer. If it is a single transfer, it waits in state S11 for the 403GC to assert XACK~, indicating that the read data is available. The RDYI~ input to the PCI9060ES is asserted, causing the read data to be loaded into the direct slave read FIFO. For a burst cycle, the state machine waits in state S8, where XREQ~ is continuously activated. When BLAST~ is asserted, the PCI9060ES is ready to finish the read burst. The 403GC always reads one extra word after XREQ~ is negated, but in this application, the extra data is simply ignored.

In this application the PCI9060ES is programmed to burst a maximum of 4 fullwords for every address strobe. Burst transfers do not cross 16 byte boundaries, and are sequential. Therefore the column address counter in the DRAMMUX MACH only needs to be two bits wide. For longer burst lengths, the size of the column address burst counter must be increased, and a carry output is needed to stop the PCI9060ES from bursting when the counter is about to roll over. The BTERM input to the PCI9060ES is used to perform this function.

3.4 Write Cycles

A direct master write cycle is initiated by the PCI9060ES when it asserts address strobe (ADS~). It also asserts an address (A[31:2]), write/read status (LW/R), byte enables (LBE[3:0]), and burst last (BLAST~). The DRAMCTL state machine in the PCI MACH device detects this cycle and transitions to state S1 where a DRAM write cycle is initiated. If an unaligned write cycle is detected, then the state machine will go to state S5. More about unaligned transfers later.

The XREQ and XSIZ[0:1] inputs to the 403GC are used to initiate a DRAM cycle. The XSIZ inputs are decoded as follows:

XSIZ[0:1]	Operation
00	Byte Transfer (8 bits)
01	Halfword Transfer (16 bits)
10	Fullword Transfer (32 bits)
11	Burst Fullword Transfer

The byte address is determined by the WBE2(A30) and WBE3(A31) inputs to the 403GC, and is derived from the LBE outputs of the PCI9060ES. After the state machine asserts XREQ~, it checks BLAST~ to determine if this is a single or burst transfer. If it is a single transfer, it waits in state S4 for the 403GC to assert XACK~, indicating that the data has been written. The RDYI~ input to the PCI9060ES is asserted, causing the write cycle to be completed. For a burst cycle, the state machine waits in state S2, where

XREQ~ is continuously activated. When BLAST~ is asserted, the PCI9060ES is ready to finish the write burst. The 403GC always writes one extra word after XREQ~ is negated. In this application, the RDYI~ input to the PCI9060ES is negated while the last word is being written into the 403GC twice. The causes the PCI9060ES to keep the same data on the bus. The address counter in the DRAMMUX is also prevented from incrementing, so the last word is just written to the same location twice. When the last word is being written, RDYI~ is re-asserted to allow the PCI9060ES to complete the write burst.

3.4.1 Unaligned transfers

The 403GC only accepts the following types of transfers to DRAM from an external master:

- Fullword transfer
- Halfword transfers on halfword boundaries
- Single Byte transfer

The PCI bus allows any combination of byte enables during a write cycle. There are eight different 2 and 3 byte transfers which are considered unaligned by the 403GC. These transfers are converted to multiple single byte transfers by the DRAMCTL state machine in the PCI MACH. The first byte address is loaded into a counter at the beginning of the cycle. This counter is then incremented after each byte transferred by a value determined by the arrangement of bytes being written. The XSIZ inputs to the 403GC are forced to 00, thus requesting single byte transfers. A byte counter is also loaded at the beginning of the cycle, and is used to keep track of how many bytes to transfer.

3.5 PCI9060ES Configuration Registers

The following local configuration registers must be programmed before direct slave accesses to the local bus DRAM can occur:

Register	Offset
PCI Command Register	04h
PCI Base Address for Local Address Space 0	18h
Range for PCI to Local Address Space 0	80h
Local Base Address (Re-map) for PCI to Local Address Space 0	84h
Local Arbitration Register	88h
Big/Little Endian Descriptor Register	8Ch
Bus Region Descriptors for PCI to Local Accesses	98h

These registers are accessed by running a 403GC cycle to the PCI9060ES with the 9060 chip select (CS9060~) asserted. The address offsets for each register are shown in the table.

4. Critical Timing

4.1 DRAM Timing

The most critical timing parameter in this design is the DRAM address mux when the 403GC is bursting to or from DRAM. The 25 MHz 403GC has a clock to address delay of 4 to 15 nsec. The delay of the DRAMMUX mach is 7.5 nsec. The minimum clock to CAS delay is ½ the clock period (20 nsec at 25 MHz) plus 4 nsec. If the clock has a 50% duty cycle, then a column address setup time of only 1.5 nsec is provided. This setup time could be increased by using a 33 MHz 403GC which has a clock to address of 4 to 13 nsec, or by using several 5 nsec PALs.

The write data setup time is also very tight. The clock to data of the PCI9060ES is 20 nsec, providing 4 nsec of setup time before the falling edge of CAS.

APPENDIX

Schematics, PAL equations and Timing Diagrams for 16 Word Burst Implementation