PCI 9060

December, 1995
VERSION 1.2

PCI Bus Master Interface Chip for
Adapters and Embedded Systems

Features

- PCI Bus Master Interface supporting adapters and embedded systems
- Two independent DMA channels for local bus memory to/from PCI host bus data transfers
- Four bi-directional FIFOs for zero wait-state burst operation; one for each DMA channel, one for Direct Master interface and one for slave interface
- PCI Bus Master transfers up to 132 MBytes/sec
- Supports both multiplexed and non-multiplexed local buses, 32, 16 or 8 bit. May connect directly to Intel i960®Cx, Hx, Jx, Kx and Sx processors
- Local bus can run asynchronously to the PCI clock.
- Eight 32 bit mailbox and two 32 bit doorbell registers
- Low power CMOS in 208 Pin Plastic QFP Package

General Description

The PCI9060 provides a compact high performance PCI bus master interface for adapter boards and embedded systems. The chip's local bus follows the protocol of the Intel i960® microprocessor family.

The PCI9060 provides two independent bi-directional DMA channels with bi-directional FIFOs supporting zero wait-state burst transfers between host and local memory. Each channel also supports full data chaining modes which allows concurrent operations. The chip also contains a bi-directional FIFO for efficient slave access. In addition, another bi-directional FIFO ensures high speed Direct Bus Master transfers.

The PCI9060 also allows the local processor and other intelligent controllers to perform direct bus master transfers on the PCI bus. As an option, the PCI9060 can enable the local processor to configure other PCI devices in the system.

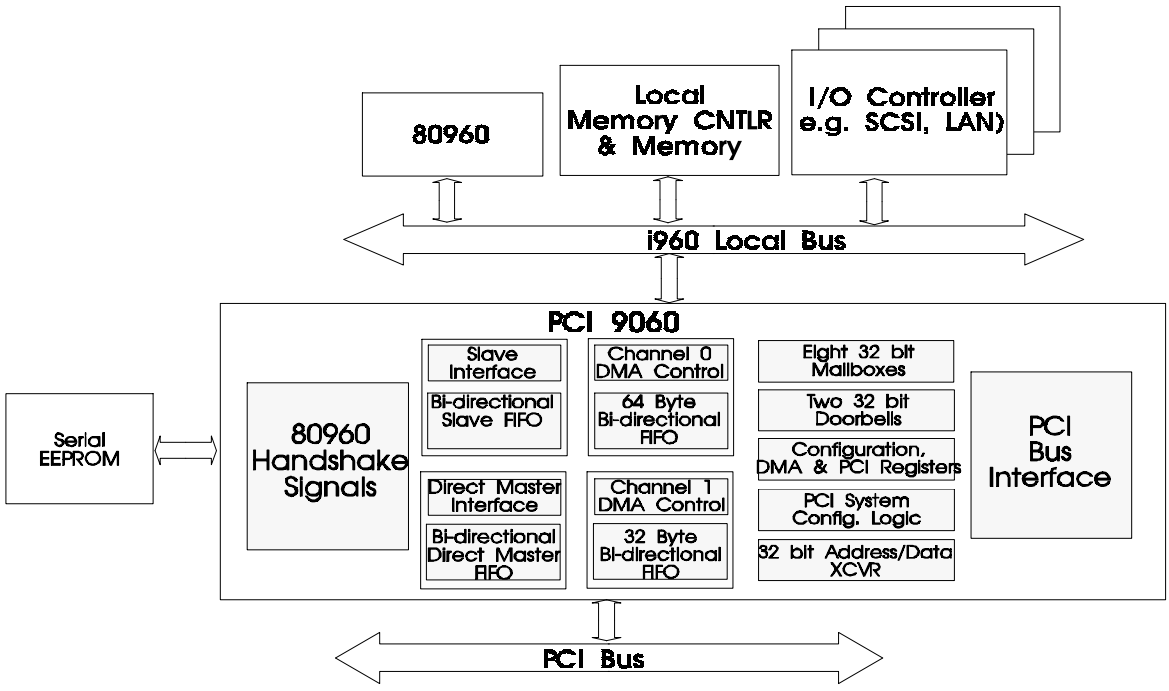

Figure 1. Typical Adapter or Embedded System Block Diagram

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REVISION HISTORY

Date	Revision	Comment
03/01/95	1.0	1. DEN# is an I/O pin in Jx mode. DEN# should be tied high if unused. 2. For **PCI9060 Rev 2A** parts or later, A PCI master can access the DMA registers by performing a Direct Slave access to the local bus. The local address should be that of the desired DMA register. 3. Timing Diagram updates
08/15/95	1.1	Corrected typographical errors, Clarified specifications, and Updated Timing Diagrams.

12/12/95	1.2	A. Updates from Rev. 2 chip to Rev. 3 chip : In addition to correcting errata, PLX made changes to the PCI 9060 to improve performance, flexibility and ease of use. The Rev. 3 is also entirely pin and software compatible with the Rev. 2. 1. Errata 1 through 13 from Rev. 2 chip were corrected. 2. Direct Slave Read FIFO = 8 Words (32 Bytes) vs. 4 in Rev. 2 Direct Slave Write FIFO = 8 Words (32 Bytes) vs. 4 in Rev. 2 The increase in FIFO depths requires no software or hardware changes. The only difference the user will observe is an increase in Direct Slave throughput. 3. DMA registers may be accessed from PCI bus as well as local bus as described in Version 1.2 data sheet. 4. 0 ns hold time on all PCI signals. 5. Local pre-fetch can be disabled (PCI disconnect after 1 data read) Default state is pre-fetch enabled. To disable address space 0 pre-fetch set bit 8, Table 29 to 1. To disable expansion ROM pre-fetch set bit 9, Table 29 to 1. 6. Many users want to have an option of mapping the entire PCI address space to the local bus. To accommodate this Rev. 3 acts as follows: If the PCI address space for Direct Master accesses overlaps the 128 byte space for the run time registers, an access to that 128 byte space will access the run-time registers. No Direct Master access will occur in the run-time address space. 7. For the same reasons as in 6, if the PCI address space for Direct Slave accesses overlaps the space for the run time registers, an access to that space will access the run-time registers. No Direct Slave access will occur in the run-time address space. 8. LSERR# is driven high during reset (instead of driven low in Rev. 2), to avoid erroneous LSERR# assertion. 9. Most NC pins in Rev. 3 are driven and must not be connected. In the Rev. 2 chip, most of the NC pins are floating. 10. In Rev. 2 BREQo was asserted if there was any data in the FIFO during a write and deadlock situation. In Rev. 3, BREQo is asserted only if DM FIFO is full during a write and deadlock situation. 11. During Direct Slave reads, the 9060 gives up the local bus if BREQi is asserted or it's internal local bus latency timer expires. The individual data cycles still need to be completed. 12. The 9060 keeps the local bus until the entire Direct Slave write cycle is complete, not just when the write FIFO is empty. The 9060 still gives up the local bus if BREQi is asserted or it's internal local bus latency timer expires. B. Revised Local Bus Maximum Setup and Hold times. Refer to Section 6 for complete AC/DC Electrical Characteristics.

Local Bus Maximum setup and hold time comparison(Version 1.1 vs. 1.2 data sheet).

Signal	Version 1.1 setup time	Version 1.1 hold time	Version 1.2 setup time	Version 1.2 hold time
ADS#	4	3	9	1
LAD	4	3	3	N.A.
LD	4	3	7	1
RDYi#	4	3	9	1
BLAST#	4	3	6	1
LDP	4	3	4	1
BTERM#	4	3	5	1
BREQ	4	3	N.A.	1
HOLDA	4	3	5	1
DREQ#	4	3	6	1

Local Bus Maximum T_{VALID} (Version 1.1 vs. 1.2 data sheet)

Signal	Version 1.1 $T_{VALID\ (MAX)}$ NSEC (WORST CASE)	Version 1.2 $T_{VALID\ (MAX)}$ NSEC (WORST CASE)
USERo	13	21
BREQo	18	21
DACK[1:0]#	18	20

1. SECTION 1 - PCI 9060 GENERAL DESCRIPTION

The PCI9060 is a PCI bus master interface chip that connects a PCI host bus to three local bus types, selected through mode pins. Each local bus configuration matches the protocol of an Intel 80960 processor, but the PCI 9060 may be connected to any local bus with a similar design.

Mode	Description	80960 processor
Cx	32 bit address / 32 bit data, non-multiplexed	Cx, Hx
Jx	32 bit address / 32 bit data, multiplexed	Jx, Kx
Sx	32 bit address / 16 bit data, multiplexed	Sx

The PCI9060 bus interface chip offers substantial performance advantages over slave adapters or other bus master adapters that rely on the local or host processor to transfer large amounts of data to and from the adapter. The PCI9060 provides two independent bi-directional DMA channels each with FIFOs for maximum burst transfers in and out of the adapter. This feature significantly improves overall performance by greatly reducing local or host processor involvement with actual data transfers. The FIFOs ensure that data is transferred at maximum bus efficiency and burst rates even when the local bus is operating at a different (and potentially slower) speed than the PCI bus.

Using the PLX PCI9060 bus master chip also reduces total hardware and software development costs for disk controller, communication adapter and embedded system designs. The PCI9060 provides a single chip interface solution that minimizes board space requirements and ensures PCI hardware compatibility compliance. Because the PCI9060 can be used for all intelligent subsystem designs, common driver and initialization software can be used, thus maximizing development resources and increasing the quality of the design.

Major Features

Dual independent programmable DMA controllers with bi-directional FIFOs. The PCI9060 provides two independent programmable DMA controllers with bi-directional FIFOs for each channel. Each channel supports both non-chaining and chaining DMA modes.

Direct bus master. The PCI9060 supports the direct access of the PCI bus by either a local bus processor or an intelligent controller. The PCI9060 supports PCI bus interlock ("LOCK#") cycles as well. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

Direct slave. The PCI9060 supports both memory mapped and I/O mapped burst accesses to the local bus from the PCI bus. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

PCI Host Capability. In direct master mode, the PCI9060 can generate type 0 and type 1 PCI configuration cycles.

Interrupt generator. The PCI9060 can generate PCI and local interrupts from several sources.

Clock. The PCI9060 local bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock can run asynchronously to the PCI clock.

Programmable local bus configurations. The PCI9060 supports: a 32 bit non-multiplexed bus (Cx mode), a 32 bit multiplexed bus (Jx mode), and a 16 bit multiplexed (Sx mode). The PCI9060 operates in one of three modes, selected through mode pins, corresponding to three bus types; Cx, Jx and Sx.

Bus drivers. All control, address, and data signals generated by the PCI9060 directly drive the PCI bus, without requiring any external drivers.

Serial EEPROM interface. The PCI9060 contains an optional serial EEPROM interface that can be used to load configuration information. This is useful for loading information which is unique to a particular adapter (e.g. Network ID, Vendor ID, etc.).

Mailbox Registers. The PCI9060 contains eight 32 bit mailbox registers that may be accessed from either the PCI or the local bus.

Doorbell Registers. The PCI9060 includes two 32 bit doorbell registers. One generates interrupts from the PCI bus to the local bus. The other generates interrupts from the local bus to PCI bus.

Unaligned DMA Transfer Support. The PCI9060 can transfer data on any byte boundary.

2. SECTION 2 - BUS OPERATION

2.1 PCI BUS CYCLES

The PCI9060 is PCI Compliant.

2.1.1 PCI Target Command Codes

As a target, the PCI9060 allows access to the PCI9060 internal registers and the local bus using the following commands;

Command Type	Code(C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All read or write accesses to the PCI9060 can be byte, word or long word accesses. All memory commands are aliased to the basic memory commands. All I/O accesses to the PCI9060 are decoded to a long word boundary. The byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.1.2 PCI Master Command Codes

The PCI9060 can access the PCI bus to perform DMA transfers or Direct Local to PCI bus transfers.

2.1.2.1 DMA Master Command Codes

The PCI9060's DMA controllers can generate the following memory cycles:

Command Type	Code(C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)

2.1.2.2 Direct Local to PCI Command Codes

For direct local to PCI bus accesses, the PCI9060 can generate the following cycles:

Local to PCI Memory Access

Command Type	Code(C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)

Local to PCI I/O Access

Command Type	**Code(C/BE[3:0]#)**
I/O Read	0010 (2h)
I/O Write	0011 (3h)

Local to PCI Configuration Access

Command Type	Code(C/BE[3:0]#)
Configuration Memory Read	1010 (Ah)
Configuration Memory Write	1011 (Bh)

2.2 LOCAL BUS CYCLES

The PCI9060 is a PCI bus master interface chip that connects a PCI host bus to several local processor buses: 32 bit non-multiplexed (Cx mode), 32 bit multiplexed (Jx mode), and 16 bit multiplexed (Sx mode). The PCI9060 operates in one of three modes, selected through mode pins, corresponding to three bus types; Cx, Jx and Sx.

2.2.1 Local Bus Slave

As a local bus target, the PCI9060 allows access to the PCI9060 internal registers and PCI bus.

In the Cx and Jx modes, local bus slave accesses to the PCI9060 must be for a 32 bit non-pipelined bus. In the Sx mode, local bus slave accesses to the PCI9060 must be for a 16 bit non-pipelined bus. The PCI9060 READYo# indicates that a data transfer has completed.

2.2.2 Local Bus Master

2.2.2.1 Ready/Wait State Control

If the READY input is disabled, the external READY input has no effect on wait states for a local access. Wait states between data cycles are generated internally by a wait state counter. The wait state counter is initialized with its configuration register value at the start of each data access.

If the READY input is enabled, the READY input has no effect until the wait state counter is 0. The READY input then controls the number of additional wait states.

BTERM input is not sampled until the wait state counter is 0.

2.2.2.2 Burst Mode and Continuous Burst Mode (BTERM "Burst Terminate" mode)

Burst Mode

If Bursting is enabled and the BTERM input is not enabled, the PCI9060 emulates the 80960Sx, 80960Jx or 80960Cx mode of bursting with the exception of the starting burst address. Bursting can start on any boundary and continue up to an address boundary as described below. After the data at the boundary has been transferred, the PCI9060 generates a new address cycle (ADS#).

Cx,Jx	32 bit bus: 4 Lwords or up to a quad Lword boundary (LA3,LA2 = 11)
Cx,Jx	16 bit bus: 4 words or up to a quad word boundary (LA2,LA1 = 11)
Cx,Jx	8 bit bus: 4 bytes or up to a quad byte boundary (LA1,LA0 = 11)
Sx	16 bit bus: 8 words or up to a quad Lword boundary (LA3,LA2 = 11)

Continuous Burst Mode (Bterm "Burst Terminate" mode)

BTERM mode enables the PCI9060 to perform long bursts to devices that can accept longer than 4 Lword bursts. The PCI9060 generates one address cycle and then continues to burst data. If a device requires a new address cycle after a certain address boundary, it can assert BTERM# input to cause the PCI9060 to generate a new address cycle. BTERM# input is a ready input that acknowledges the current data transfer and requests that a new address cycle be generated (ADS#). The address will be for the next data transfer. If BTERM mode is enabled, the PCI9060 asserts BLAST# only if its FIFOs become FULL/EMPTY or a transfer is complete.

Partial Lwords Accesses

Lword accesses in which not all byte enables are asserted are broken into single address and data cycles.

2.2.2.3 Recovery States

In the Jx and Sx mode, the PCI9060 inserts one recovery state between the last data transfer and the next address cycle.

The PCI9060 does not support the 80960Jx feature of using the READY input to add recovery states. No additional recovery states are added if the READY input remains asserted during the last data cycle.

2.2.2.4 Local Bus Read Accesses

For all local bus read accesses, the PCI9060 reads an entire long word. To a 32 bit local bus the PCI9060 performs one read with all byte enables asserted for each Lword. To a 16 bit local bus, the PCI9060 performs two 16 bit reads for each Lword. To an 8 bit local bus, the PCI9060 performs four 8 bit reads for each Lword.

In other words, for Direct Slave read accesses, the PCI9060 reads 4 bytes of data starting at an Lword boundary regardless of the PCI byte enables. For a DMA local bus to PCI bus transfer, the PCI9060 reads 4 bytes of data starting at an Lword boundary regardless of the DMA start address and DMA byte count.

2.2.2.5 Local Bus Write Accesses

No matter how many bytes, or which byte in the Lword is requested by the PCI bus, the Local Bus always read 4 bytes(32 bits), starting at Lword boundary. For local bus writes, only the bytes specified by a PCI bus master or the PCI9060's DMA controller are written. An access to an 8 or 16 bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded as in the 80960Cx to provide local address bits [LA1:LA0].

2.2.2.6 Direct Slave Write Access to 8 and 16 bit bus

A Direct PCI access to an 8 or 16 bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded as in the 80960Cx to provide local address bits [LA1:LA0].

A Direct PCI access to an 8 bit bus with non-adjacent byte enables in a PCI Lword must not be used. Non-adjacent byte enables cause an incorrect [LA1:LA0] address sequence when bursting to memory. Therefore, for each Lword write to an 8 bit bus, the PCI9060 does not write data after the first gap. For reads accesses, the PCI9060 reads all bytes of the Lword. Direct PCI accesses to an 8 bit bus with non-adjacent byte enables are not terminated with a Target Abort.

2.2.2.7 Local Bus Data Parity

There is one data parity pin for each byte lane of the PCI9060 data bus (DP[3:0]). Even data parity is generated for each lane during local bus reads from the PCI9060 and during PCI9060 master writes to the local bus.

Even data parity is checked during local bus writes to the PCI9060 and during PCI9060 reads from the local bus. Parity is checked for each byte lane with an asserted byte enable. PCHK# is asserted in the clock cycle following the data being checked if a parity error is detected.

Generation or use of local bus data parity is optional. The signals on the data parity pins do not effect operation of the PCI9060. PCI bus parity checking and generation is independent of local bus parity checking and generation.

3. SECTION 3 - FUNCTIONAL DESCRIPTION

3.1 PCI 9060 Initialization

The PCI9060 configuration registers can be programmed by an optional serial EEPROM and/or by a local processor.

EEPROM Initialization

During serial EEPROM initialization, the PCI9060 response to PCI target accesses is RETRYs. During serial EEPROM initialization, the PCI9060 response to a local processor is to hold off READY.

Local Initialization

The PCI9060 will issue RETRYs to all PCI accesses until the Local Init Done bit in the Init Control Register is set. The Init Done bit is programmable through local bus configuration accesses. If this bit is not going to be set by a local processor, then NB# input should be tied low. Holding NB# input low externally forces the Local Init Done bit to 1.

If an EEPROM is not present and the local init status bit is set to "done" by holding the NB# input low, the PCI9060 default values are used.

3.2 RESET

3.2.1 PCI Bus Input RST#

The PCI bus RST# input, causes all PCI bus outputs to float, resets the entire PCI9060 and causes the local reset output LRESETo# to be asserted.

3.2.2 Local Bus Input LRESETi#

When asserted, the LRESETi# input resets the local bus portion of the PCI9060, clears all local configuration registers, and causes the LRESETo# output to be asserted.

3.2.3 Local Bus Output LRESETo#

LRESETo# is asserted when PCI bus RST# input is asserted, the LRESETi# input is asserted, or the software reset bit in the Init Control Register is set to a 1.

3.2.4 Software Reset

A host on the PCI bus can set the software reset bit in the Init Control Register to reset the PCI9060 and assert the LRESETo# output. The PCI configuration registers will not be reset.

When the software reset bit is set, the PCI9060 responds to PCI accesses but not local bus accesses. The PCI9060 remains in this reset condition until the PCI host clears the bit.

3.3 EEPROM

After reset, the PCI9060SD attempts to read the EEPROM to determine its presence. An active low start bit indicates the EEPROM is present. Refer to the manufacturer's data sheet for the particular EEPROM being used.

The EEPROM can be read or programmed from the PCI or local bus. Bits 24 through 27 of the EEPROM Control Register control the PCI9060SD pins which enable the reading or writing of EEPROM bits. Refer to the manufacturer's data sheet for the particular EEPROM being used.

3.3.1 SHORT EEPROM LOAD

The following registers are loaded from EEPROM after reset is de-asserted if the SHORT# pin is low. The bits are organized such that the most significant bit of each 32-bit word is stored first in EEPROM. (The first bit in the EEPROM is bit 15 of the Device ID). The five 32-bit words are stored sequentially in the EEPROM. Therefore, a 256 bit device can be used. (Example: National NM93CS06 or compatible. **Note: 93C06 is not supported**)

EEPROM Offset	EEPROM Value	Description
0	9060	Device ID.
2	10B5	Vendor ID.
4	0680	Class Code.
6	0002	Class Code, Revision.
8	0000	Maximum Latency, Minimum Grant.
A	0100	Interrupt Pin, Interrupt Line Routing.
C	xxxx	MSW of Mailbox 0 (User Defined).
E	xxxx	LSW of Mailbox 0 (User Defined).
10	xxxx	MSW of Mailbox 1 (User Defined).
12	xxxx	LSW of Mailbox 1 (User Defined).

3.3.2 LONG EEPROM LOAD

The following registers are loaded from EEPROM after reset is de-asserted if the SHORT# pin is high. The bits are organized such that the most significant bit of each 16-bit word is stored first in the EEPROM (The first bit in the EEPROM is bit 15 of the Device ID). The EEPROM value can be entered into a DATA I/O programmer in the order shown below. The value shown are examples, and will need to be modified for each particular application. The 34 16-bit words shown above are stored sequentially in the EEPROM. A 1K bit device can be used. (Example: National NM93CS46 or compatible.) **Note: 93CS56 is not supported**.

MSW = Most Significant Word(bits 31 - 16)
LSW = Least Significant Word(bits 15 - 0)

EEPROM Offset	EEPROM Value	Description
0	9060	Device ID.
2	10B5	Vendor ID.
4	0680	Class Code.
6	0002	Class Code, Revision.
8	0000	Maximum Latency, Minimum Grant.
A	0100	Interrupt Pin, Interrupt Line Routing.
C	xxxx	MSW of Mailbox 0 (User Defined).
E	xxxx	LSW of Mailbox 0 (User Defined).
10	xxxx	MSW of Mailbox 1 (User Defined).
12	xxxx	LSW of Mailbox 1 (User Defined).
14	FF00	MSW of Range for PCI to Local Address Space 0 (16Mbytes).
16	0000	LSW of Range for PCI to Local Address Space 0 (16Mbytes).
18	0000	MSW of Local Base Address (Re-Map) for PCI to Local Address Space 0.
1A	0001	LSW of Local Base Address (Re-Map) for PCI to Local Address Space 0
1C	0000	Not Used.
1E	0000	Not Used.
20	0000	Not Used.
22	0000	Not Used.
24	0000	MSW of Range for PCI to Local Expansion ROM.
26	0000	LSW of Range for PCI to Local Expansion ROM.
28	0000	MSW of Local Base Address (Re-Map) for PCI to Local Expansion ROM.
2A	0000	LSW of Local Base Address (Re-Map) for PCI to Local Expansion ROM.
2C	4903	MSW of Bus Region Descriptors for PCI to Local Accesses.
2E	00C3	LSW of Bus Region Descriptors for PCI to Local Accesses.
30	0000	MSW of Range for Direct Master to PCI.
32	0000	LSW of Range for Direct Master to PCI.
34	0000	MSW of Local Base Address for Direct Master to PCI Memory.
36	0000	LSW of Local Base Address for Direct Master to PCI Memory.
38	0000	MSW of Local Base Address for Direct Master to PCI IO/CFG.
3A	0000	LSW of Local Base Address for Direct Master to PCI IO/CFG.
3C	0000	MSW of PCI Base Address (Re-Map) for Direct Master to PCI.
3E	0000	LSW of PCI Base Address (Re-Map) for Direct Master to PCI.
40	0000	MSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG.
42	0000	LSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG.

There are 60 unused bytes in the EEPROM which can be used for user defined applications.

3.4 Internal Register Access

The PCI9060 chip provides several internal registers allowing for maximum flexibility in bus interface design and performance. Among the register types are:

PCI Registers (accessible from PCI bus and Local bus)
Local Configuration Registers (Accessible from PCI and Local bus)
DMA Registers (Accessible from Local bus)
Mailbox Registers (Accessible from PCI and Local bus)
Doorbell Registers (Accessible from PCI and Local bus)

The following figure shows how these registers are accessed:

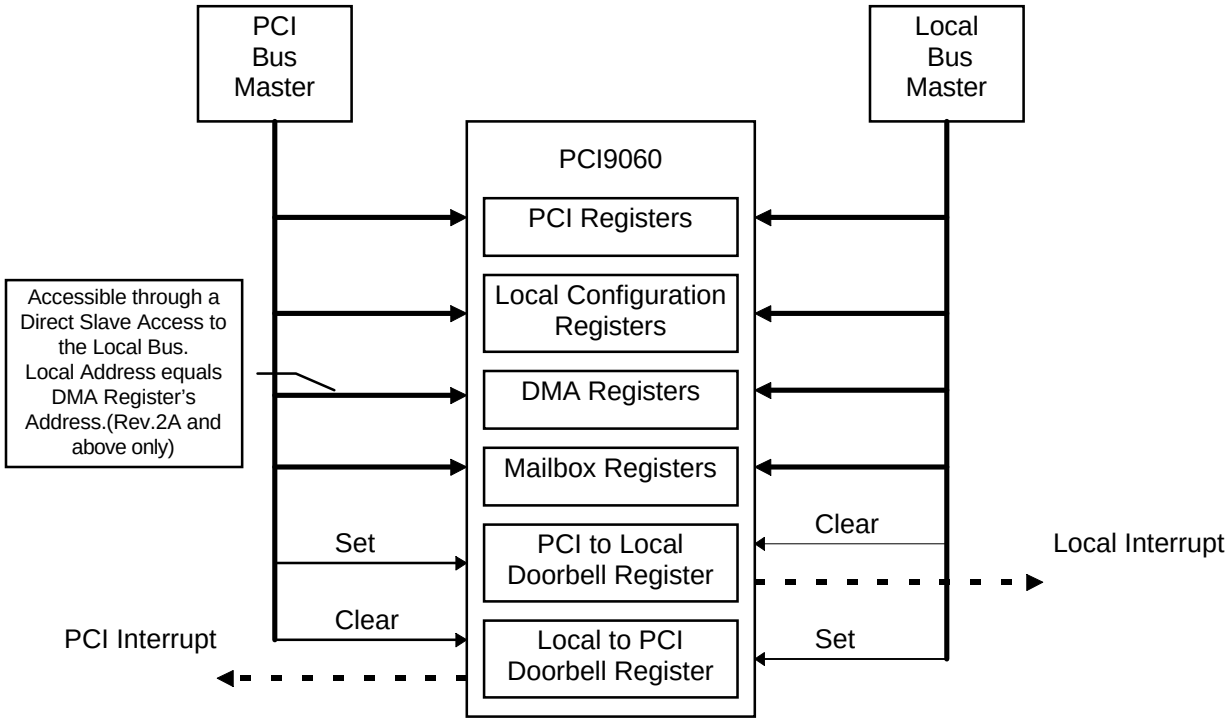


Figure 1. PCI9060 Internal Register Access

3.4.1 PCI Bus Access to Internal Registers

The PCI9060 configuration registers can be accessed from the PCI bus via a configuration type 0 cycle.

The PCI9060 local configuration and shared runtime registers can be accessed via a memory cycle with the PCI bus address matching the base address specified in the PCI9060's PCI Base Address for Memory Mapped Runtime Register or an I/O cycle with the PCI bus address matching the base address specified in the PCI9060's PCI Base Address for I/O Mapped Runtime Register.

All PCI read or write accesses to the PCI9060 registers can be byte, word or long word accesses. All PCI memory accesses to the PCI9060 registers can be burst or non-burst. The PCI9060 responds with a PCI Disconnect for all I/O accesses to the PCI9060 registers.

3.4.2 Local Bus Access to Internal Registers

The local processor can access all the internal registers of the PCI9060 through either internal or external address decode logic. The PCI9060 provides an Address decode Mode Pin (ADMODE) that selects whether the internal address decode logic is used or whether the designer will supply an external chip select from an external address decoder. The following Figure shows how the dual address decode logic works.

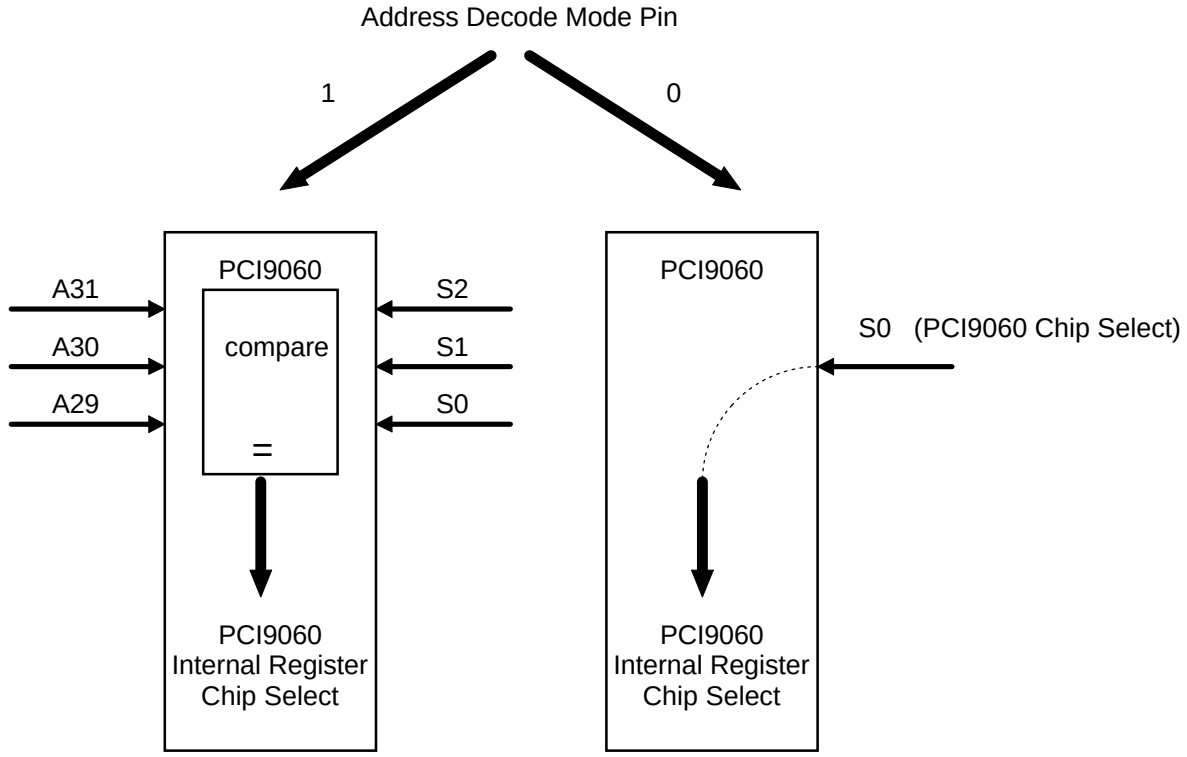


Figure 2. Dual Address Decode Mode

If the Address Decode Mode pin is set to a 1, the internal PCI9060 address decode logic is enabled. In this mode, the PCI9060 internal registers are selected when local address bits A[31:29] match input address select pins S[2:0]. If the Address Decode Mode pin is set to a 0, the PCI9060 responds to local bus access when S0 is asserted low through external chip select logic.

All local read or write accesses to the PCI9060 registers can be byte, word or long word accesses. All local accesses to the PCI9060 registers can be burst or non-burst.

For the Cx and Jx modes, accesses must be for a 32 bit non-pipelined bus. The PCI9060 READYo# indicates that a data transfer has completed.

For the Sx mode, accesses must be for a 16 bit non-pipelined bus. The PCI9060 READYo# indicates that a data transfer has completed.

3.5 Direct Data Transfer Modes

The PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI9060 control the decoding and re-mapping of these accesses to the local address space. The local processor (or intelligent controller) can also directly access the PCI bus. Again, configuration registers within the PCI9060 controls the decoding and re-mapping of these accesses to the PCI bus address space. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

3.5.1 Direct Bus Master Operation (Local Master to PCI Bus Access)

The PCI9060 supports the direct access of the PCI bus by either the local processor or an intelligent controller. Five Registers are used to define Local to PCI access; Range, Local Base Address for Direct Master to PCI Memory Register, Local Base Address for Direct Master to PCI IO/CFG Register, PCI Configuration Address Register, PCI Base Address.

Decode

The Range register specifies the local address bits that are to be used to decode a Local to PCI access. The local processor can only perform memory cycles. Therefore, the Local Base Address for Direct Master to PCI Memory Register is used to decode an access to PCI memory space and the Local Base Address for Direct Master to PCI IO/CFG Register is used to decode an access to PCI I/O space.

FIFOs

For Local Direct Master memory access to the PCI bus, the PCI9060 has an 8 Lword (32 byte) write FIFO and a 4 Lword read FIFO. The FIFO enables the local bus to operate independently of the PCI bus and allows high-performance bursting on the local and PCI bus.

Memory Access

Writes: The PCI9060 continues to accept writes and return READYo# until the write FIFO is full. It then holds off READYo# until space becomes available in the write FIFO. A programmable Direct Master FIFO ‘almost full’ status output is provided (DMPAF#).

Reads: The PCI9060 holds off READYo# while gathering an Lword from the PCI bus. A programmable prefetch or prefetch4 mode is available. In prefetch mode, the PCI9060 continues to prefetch reads while there is space in the read FIFO. In the prefetch4 mode, the PCI9060 reads only 4 Lwords from the PCI bus. In either mode, the read cycle is terminated when the local BLAST# input is asserted. Unused read data is flushed from the FIFO.

The PCI9060 does not prefetch read data for single cycle Direct Master reads (local BLAST# input asserted during 1st data phase). The PCI9060 reads a single PCI Lword.

For all DMA and Direct Master Memory reads, the PCI9060 reads an entire long word (all PCI byte enables are asserted).

IO/CFG Access

For Direct Master I/O or Configuration cycles, the PCI9060 asserts the same PCI bus byte enables as asserted on the local bus. When a Local Direct Master I/O access to the PCI bus is made, the PCI Configuration Address Register’s Configuration Enable bit determines if an I/O or Configuration access is to be made to the PCI bus .Local burst accesses are broken into single PCI I/O address/data cycles. The PCI9060 does not prefetch read data for I/O and CFG reads.

All Direct Master transfers (Cx and Jx) and Local bus accesses to the configuration registers are for a 32 bit data bus.
All Direct Master transfers(Sx mode) and Local bus accesses to the configuration registers are for a 16 bit data bus.

I/O
If the Configuration Enable bit is clear, a single I/O access is made to the PCI bus. The local address, re-mapped decode address bits, and the Local byte enables are encoded to provide the address and is output with an I/O read or write command during the PCI address cycle.

For writes, data is loaded into the write FIFO and READYo# returned to the Local bus. For reads, the PCI9060 holds off READYo# while gathering a Lword from the PCI bus.

CFG (PCI Configuration Type 0 or Type 1 Cycles)
If the Configuration Enable bit is set, a CFG access is made to the PCI bus. If the PCI configuration Address Register selects a type 0 command, bits 0-10 from the register are copied to address bits 0-10. Bits 11-15 'device number' are translated into a single bit being set in PCI address bits 11-31. PCI address bits 11-31 can be used as a device select. For a type 1 command, bits 0-23 are copied from the register to bits 0-23 of the PCI address. PCI address bits 24-31 are 0. A configuration read or write command code is output with the address during the PCI address cycle.
For writes, local data is loaded into the write FIFO and READYo# returned. For reads, the PCI9060 holds off READYo# while gathering a Lword from the PCI bus.

Direct Bus Master Lock.
The PCI9060 supports direct local to PCI bus exclusive accesses (locked atomic operations). A locked operation must start with the local bus input LLOCK# being asserted during a direct local from PCI bus read cycle. Refer to the timing diagrams included in this specification. Locked operations are enabled or disabled through the PCI Base Address for Direct Master to PCI Register.

Master/Target Abort.
The PCI9060 Master/Target abort logic enables a local bus master to perform a Direct local bus to PCI bus poll of devices to determine if they exist (Typically when the local bus performs configuration cycles to the PCI bus).

If a PCI Master, Target Abort, or Retry Time-out is encountered during a transfer, the PCI9060 asserts LSERR# (can be used as a NMI). If the local bus master is waiting for a READYo#, it is asserted along with BTERMo#. The local master's interrupt handler can take the appropriate application specific action. It can then clear the abort bits in the PCI9060's PCI Status Register in order to clear the LSERR# interrupt and re-enable Direct Master transfers.

If a local bus master is attempting a burst read from a non-responding PCI device (Master/Target abort), it receives the READYo# and BTERMo# for the 1st cycle only. If the local processor cannot terminate its burst cycle, it may cause the local processor to hang. The local bus will then have to be reset from the PCI bus or by a local watch-dog timer asserting RESETi#. If the local bus master can not terminate its cycle with BTERMo#, it should not perform burst cycles when attempting to determine if a PCI device exists.

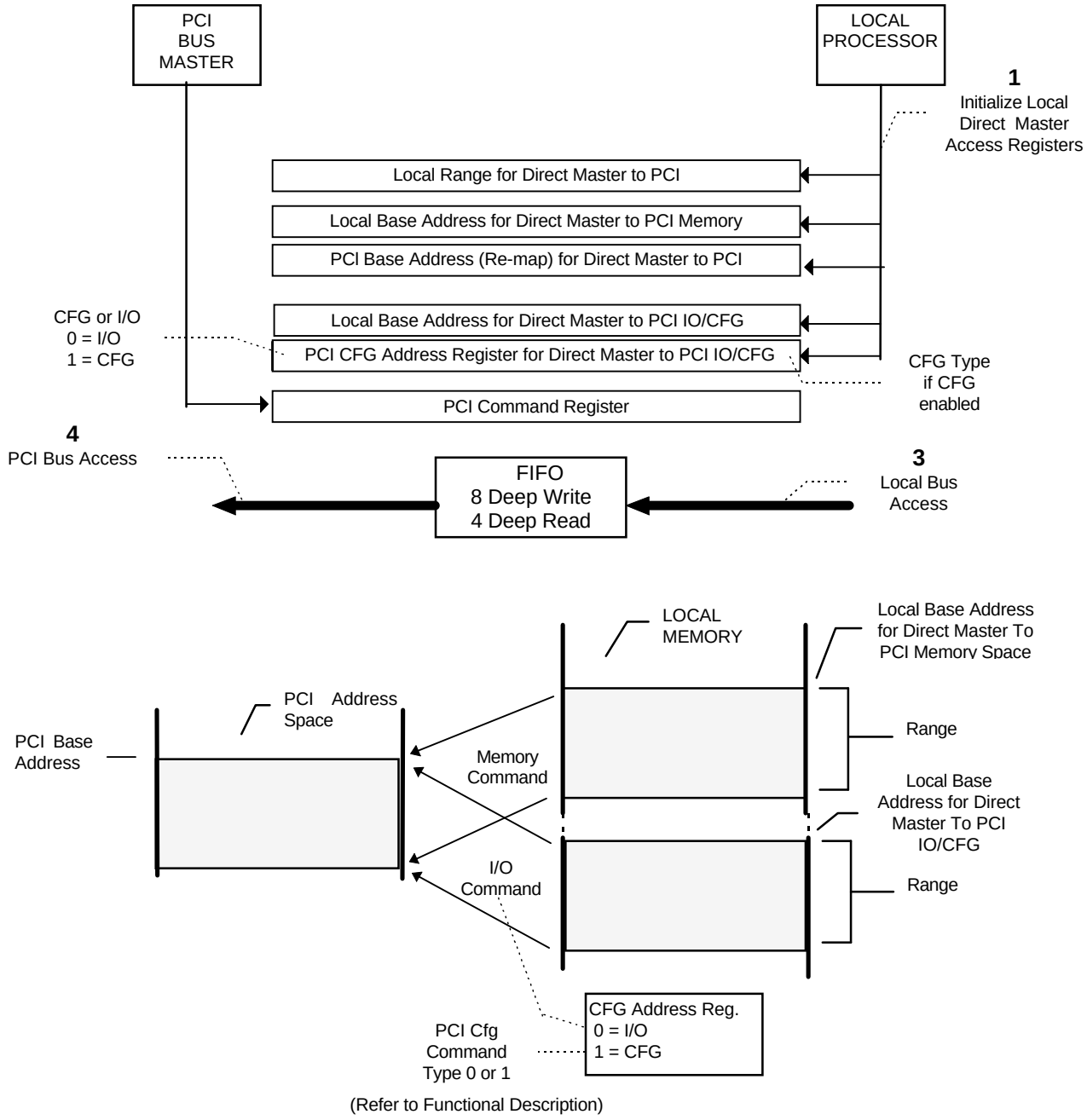


Figure 3. Local Master Direct Access of PCI Bus

3.5.2 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI9060 supports both memory mapped and I/O mapped burst accesses to the local bus from the PCI bus. PCI Base Address registers are provided to set up the adapter's location in PCI memory and I/O space. In addition, local mapping registers are provided to allow address translation from PCI address space to local address space.

The PCI9060 disconnects after one transfer for all Direct Slave I/O accesses. Memory access pre-fetching can be enabled or disabled through the Local Bus Region Descriptor for PCI to Local Accesses Register. If read prefetching is disabled, the PCI9060 disconnects after one read transfer.

3.5.2.1 PCI to Local Address Mapping

Two local address spaces, space 0 and expansion ROM, are accessible from the PCI bus. Each space is defined by a set of three registers: Local Address Range, Local Base Address, and PCI Base Address. A fourth register (Bus Region Descriptors for PCI to Local Accesses Register) defines the local bus characteristics for both regions. Refer to the Figure 5.

Byte Enables (LBE[3:0]#, Pin 139, 140, 141, 142) are encoded based on configured bus width as follows:

32 bit bus: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle.
- BE3# Byte Enable 3 - LD[31:24]
- BE2# Byte Enable 2 - LD[23-16]
- BE1# Byte Enable 1 - LD[15-8]
- BE0# Byte Enable 0 - LD[7-0]

16 bit bus: For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provide BHE#, LA1, and BLE# respectively.
- BE3# Byte High Enable (BHE#) - LD[15:8]
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Byte Low Enable (BLE#) - LD[7-0]

8 bit bus: For an 8 bit bus BE1# and BE0# are encoded to provide LA1 and LA0 respectively.
- BE3# not used
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Address bit 0 (LA0)

Each PCI to Local Address space is defined as part of reset initialization as follows:

Local Bus Initialization Software:

Range: Specifies which PCI address bits are to be used to decode a PCI access to Local bus space. Each of the bits corresponds to an address bit with Bit 31 corresponds to Address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others.

Re-map PCI to Local Addresses into a Local Address space: The bits in this register re-map (replace) the PCI address bits used in decode as the Local Address bits.

Local Bus Region Description: Specifies the local bus characteristics.

PCI Initialization Software:

PCI reset software determines how much address space is required by writing a value of all ones (1) to a PCI Base Address register and then reading the value back. The PCI9060 return 0s in don't care address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register.

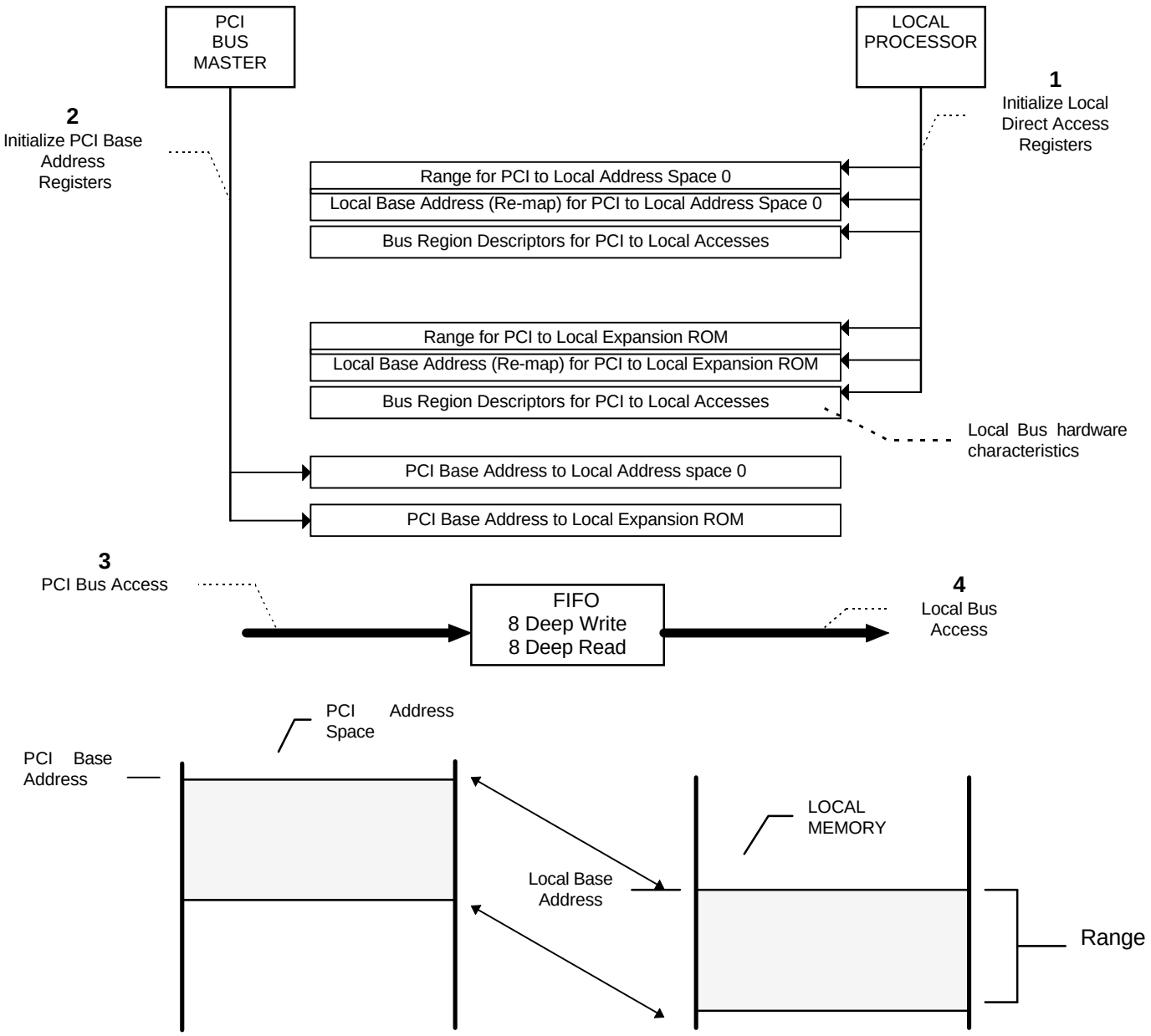


Figure 4. PCI Master Direct Access of Local Bus

Example: A 1 MB local address space 12300000h through 123FFFFFh is accessible from the PCI bus at PCI addresses 78900000h through 789FFFFFh.

1. Local initialization software sets the Range and Local Base address registers as follows:
   Range- FFF00000h (1 MB, decode the upper 12 PCI address bits)
   Local Base Address(re-map)- 123XXXXXh (Local Base Address for PCI to Local accesses)

2. PCI Initialization software writes all 1s to the PCI Base Address and then read it back. The PCI9060 returns a value FFF00000h. The PCI software then writes to the PCI Base Address register.
   PCI Base Address- 789XXXXXh (PCI Base Address for access to Local Address space)

For PCI direct access to the local bus, the PCI9060 has an 8 Lword (32 byte) write FIFO and a 8 Lword read FIFO. The FIFO enables the local bus to operate independent of the PCI bus. The PCI9060 can be programmed to return a RETRY response or to throttle TRDY for any PCI bus transaction that is attempting to write to the PCI9060 local bus when the FIFO is full.

For PCI read transactions from the PCI9060 local bus, the PCI9060 holds off TRDY while gathering the local bus Lword to be returned. For read accesses mapped to the PCI memory space, the PCI9060 prefetches up to 4 Lwords from the local bus. Unused read data is flushed from the FIFO. For read accesses mapped to the PCI I/O space the PCI9060 does not prefetch read data, it breaks each read of the burst cycle into a single address/data cycle on the local bus.

The period of time that the PCI9060 holds off TRDY can be programmed in the Local Bus Region Descriptor register. The PCI9060 issues a RETRY to the PCI bus transaction master when the programmed time period expires. This would happen when the PCI9060 can not gain control of the local bus and return TRDY within the programmed time period.

3.5.2.2 Deadlock and BREQo

A deadlock situation can occur when a master on the PCI bus wants to access the PCI9060 local bus at the same time that a master on the local PCI9060 bus wants to access the PCI bus. Two types of deadlock situations can occur:

1. A master on the local bus is performing a direct bus master access to a PCI bus device other than the PCI bus device that is trying to access the local bus at the same time (PARTIAL DEADLOCK).

2. A master on the local bus is performing a direct bus master access to the same PCI bus device that is trying to access the local bus at the same time (FULL DEADLOCK).

This applies only to direct ("pass through") master and slave accesses through the PCI9060. Deadlock will not occur in transfers through the PCI9060 DMA controller or the mailboxes.

For PARTIAL DEADLOCK, the PCI access to the local bus times out (programmable through the Local Bus Region Description for PCI to Local Accesses Register) and the PCI9060 responds with a PCI RETRY. The PCI specification requires that a PCI master release its request for the PCI bus (deasserts REQ#) for a minimum of 2 PCI clocks after receiving a RETRY. This allows the PCI bus arbiter to grant the PCI bus to the PCI9060 so that it can complete its direct master access and free up the local bus. Possible solutions are described below for cases in which the PCI bus arbiter does not function as described (PCI bus architecture dependent), waiting for a time-out is undesirable, or a FULL DEADLOCK condition exists.

Backoff
The PCI9060 contains a pin (BREQo) that indicates that a possible deadlock condition exists. The PCI9060 starts the BREQo timer (programmable through registers) when it detects the following conditions:

a. A master on the local bus is performing a direct bus master access to the PCI bus.
b. A master on the PCI bus is trying to access memory or an I/O device on the local bus and is not gaining access (i.e. has not received HOLDA).

If the timer expires and the PCI9060 still has not received HOLDA, the PCI9060 asserts BREQo. External bus logic can use this as a signal to perform backoff.

A backoff cycle is device/bus architecture dependent. External logic (arbiter) can assert the necessary signals to cause the local master to release the local bus (backoff). After backing off the local master, it can grant the bus to the PCI9060 (by asserting HOLDA).
The PCI9060 considers the local master to PCI bus access terminated when it detects HOLDA. It then proceeds with the PCI master to local bus access. When this access is complete and the PCI9060 releases the local bus, the external logic can release backoff and the local master can resume the cycle that was interrupted by the backoff cycle. The write FIFO of the PCI9060 retains all the data it has acknowledged (i.e. the last data for which READYo# was asserted and HOLDA was not asserted).
After the backoff condition ends the local master restarts the last cycle with ADS#. For writes, the data following this ADS# should be the data that was not acknowledged by the PCI9060 prior to the backoff cycle (i.e. the last data for which there was no READYo# asserted or HOLDA was asserted).

Software/Hardware Solution for systems without backoff capability
For adapters which do not support backoff, a possible deadlock solution is as follows:
PCI host software, external local bus hardware, general purpose output USERO, and general purpose input (USERI) can be used by PCI host software to prevent deadlock. USERO can be set to request that the external arbiter not grant the bus to any local bus master except the PCI9060. A status output from the local arbiter can be connected to general purpose input USERI to indicate that no local bus master owns the local bus. The input can be read by the PCI host to determine that no local bus master currently owns the local bus. The PCI host can then do a direct slave access. When the host is done it clears USERO. For devices that support pre-empt, USERO can be used to pre-empt the current bus master device. The current local bus master device completes its current cycle and gives up the local bus (deasserts LHOLD).

Software Solutions to Deadlock
PCI Host Software and Local Bus Software can use a combination of mailbox registers, doorbell registers, interrupts, direct local to PCI accesses and direct PCI to local accesses to avoid deadlock.

3.5.3 Direct Slave Priority
Direct Slave accesses have higher priority than DMA accesses.

Direct Slave accesses pre-empt DMA transfers. When the PCI9060 DMA controller owns the local bus, its LHOLD output is asserted, its LDSHOLD output is deasserted and its LHOLDA input is asserted. When a Direct Slave access is made, the PCI9060 gives up the local bus within two Lword transfers by deasserting LHOLD and floating its local bus outputs. After the PCI9060 samples its LHOLDA input deasserted, it requests the local bus for a Direct Slave transfer by asserting LHOLD and LDSHOLD. When the PCI9060 receives LHOLDA it drives the bus and performs the Direct Slave transfer. Upon completion of the Direct Slave transfer, the PCI9060 gives up the local bus by deasserting LHOLD, deasserting LDSHOLD and floating its local bus outputs. After the PCI9060 samples its LHOLDA deasserted and its local pause timer is zero, it requests the local bus for a DMA transfer by re-asserting LHOLD. When it receives LHOLDA it drives the bus and continues with the DMA transfer.

3.6 DMA Operation

The PCI9060 supports two independent DMA channels capable of transferring data from the local bus to the PCI bus or from the PCI bus to the local bus. Each channel consists of a DMA controller and a bi-directional FIFO. Both channels support chaining and non-chaining DMA transfers. The DMA registers may be accessed from PCI bus on REV. 3 (some additional design considerations required.)

3.6.1 Non-Chaining Mode DMA

The local or the host processor sets the local address, PCI address, transfer count, and transfer direction. The local or the host processor then sets a control bit to initiate the transfer. Once the transfer is complete, the PCI9060 generates an interrupt to the local processor (programmable). The local interrupt can be routed to the LINTi# input to generate a PCI interrupt (INTA#).

DMA registers are accessible from the Local and PCI bus. A PCI master can access the DMA registers by performing a Direct Slave access to the local bus (Rev. 3 only). The local address should be that of the desired DMA register.

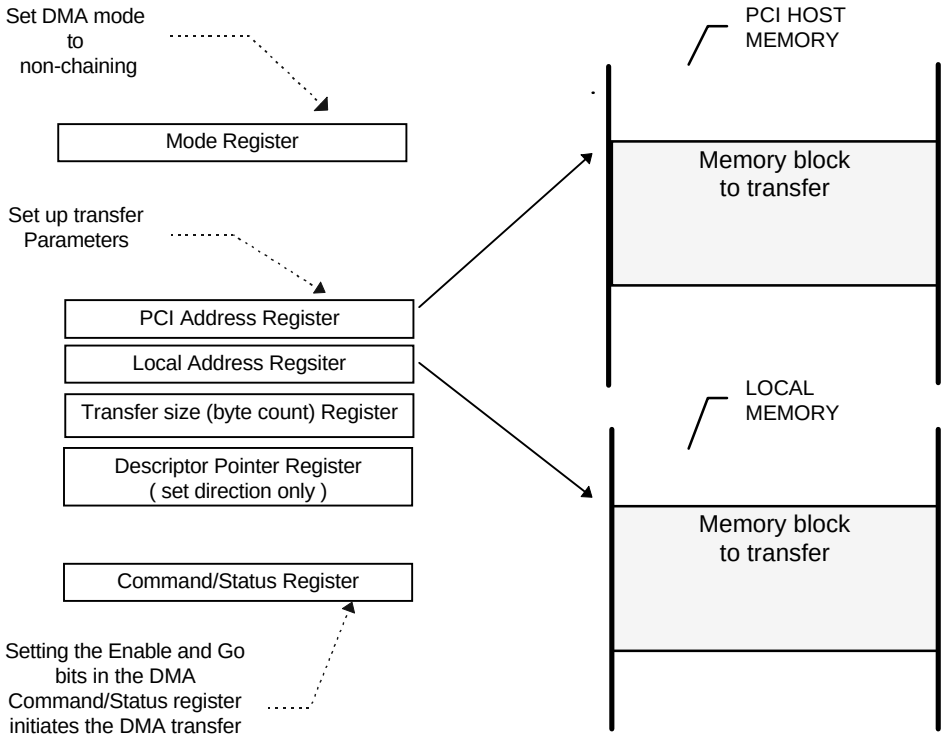


Figure 5. Non-Chaining DMA Initialization

3.6.2 Chaining Mode DMA

Chaining DMA operates as follows:

The local or the host processor sets up descriptor blocks in local memory which are composed of a PCI address, Local address, transfer count, transfer direction, and address of the next descriptor block. The local or the host processor then sets up the initial descriptor block's address in the PCI9060's descriptor pointer register and initiates the transfer by setting a control bit. The PCI9060 loads the 1st descriptor block and initiates the data transfer. The PCI9060 continues to load descriptor blocks and transfer data until it detects the end of chain bit set in the next descriptor pointer register. The PCI9060 can be programmed to interrupt the local processor upon completion of each block transfer and after all block transfers have been completed (done).

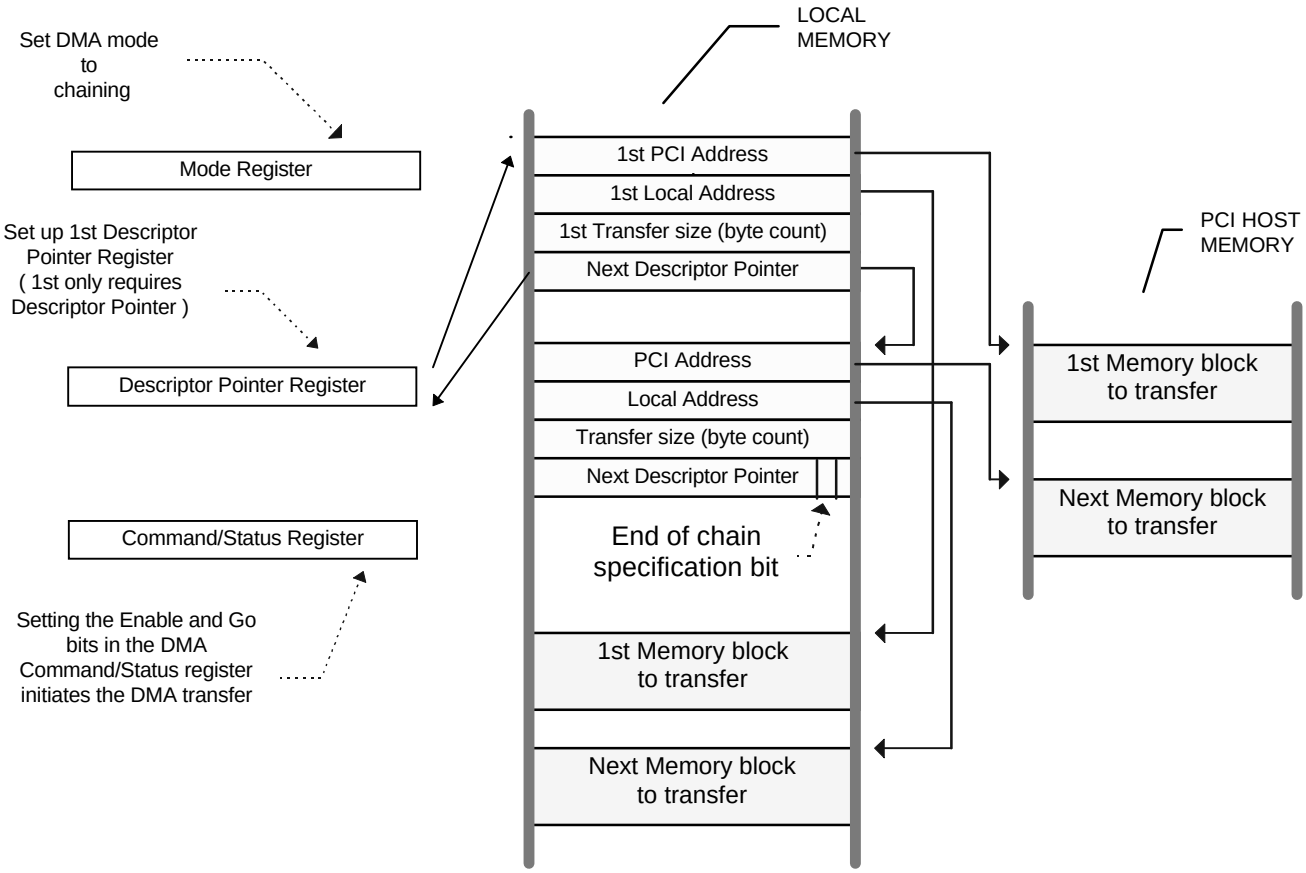


Figure 6. Chaining DMA Initialization

3.6.3 DMA Data Transfers

The PCI9060 supports two independent DMA channels (Ch 0 with 64 byte FIFO and Ch 1 with 32 byte FIFO). Either can be programmed to transfer data from the PCI bus side to the local bus side or from the local bus side to the PCI bus side. Refer to the following figures for a description of operation:

3.6.3.1 Local to PCI Bus DMA Transfer

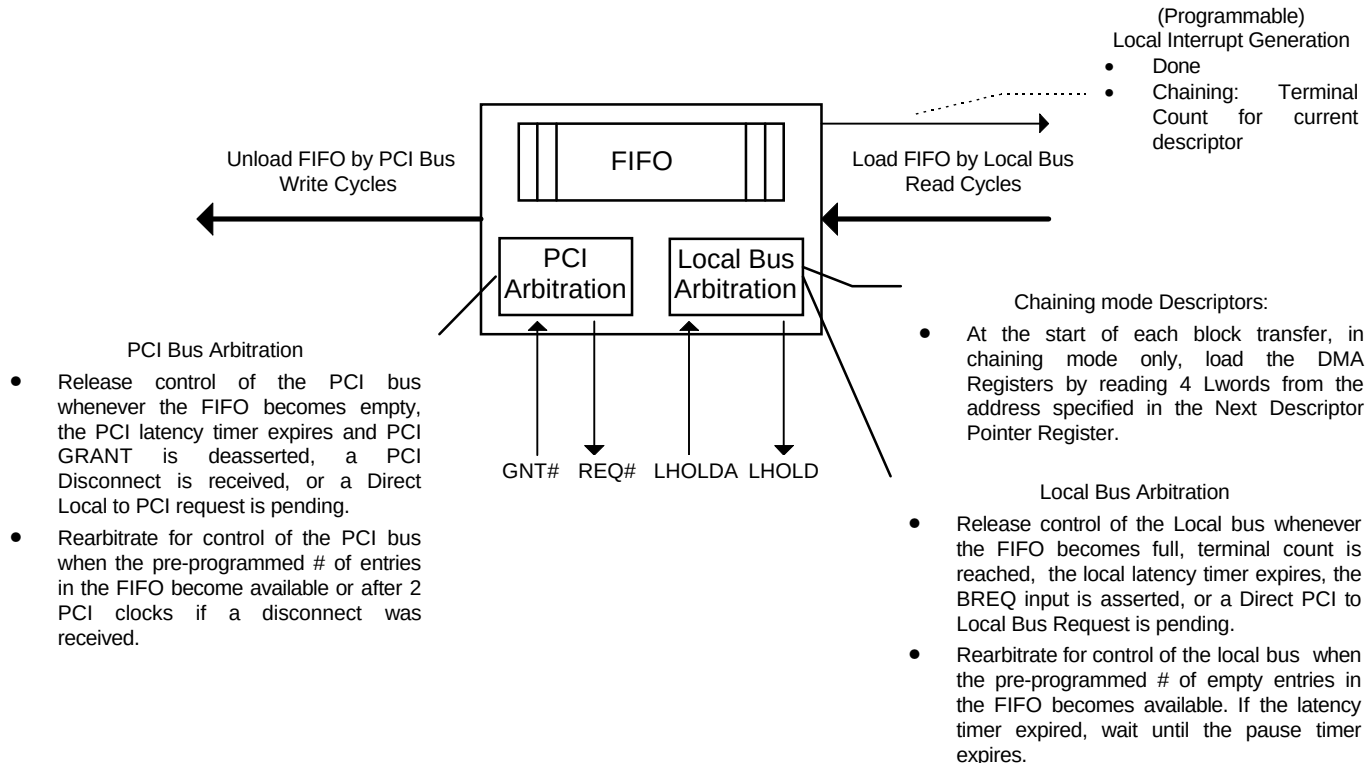


Figure 7. Local to PCI Bus DMA Data Transfer Operation

3.6.3.2 PCI to Local Bus DMA Transfer

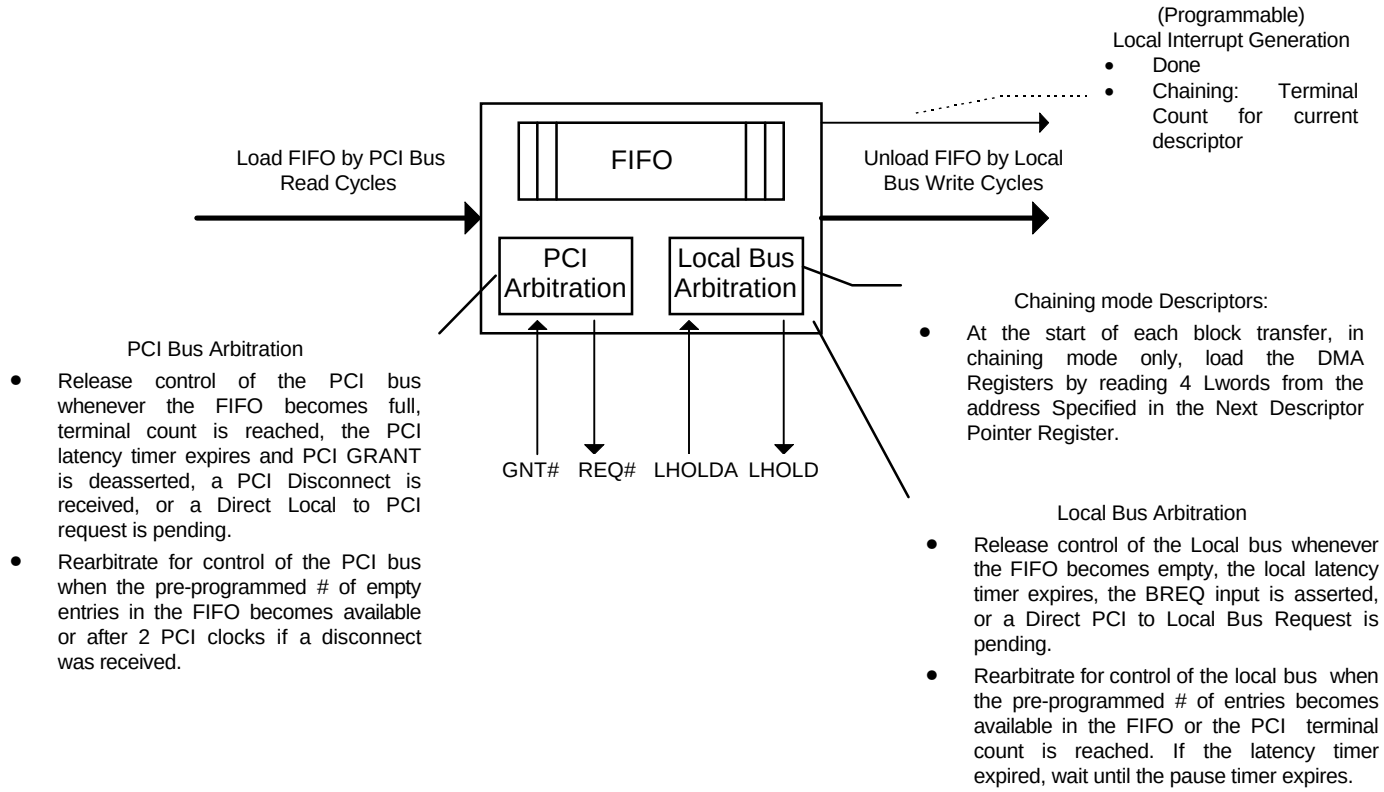


Figure 8. PCI to Local Bus DMA Data Transfer Operation

3.6.3.3 Unaligned Transfers

For unaligned local to PCI transfers, the PCI9060 reads a partial Lword from the local bus. It then continues to read Lwords from the local bus. The Lwords are assembled, aligned to the PCI bus address and loaded into the FIFO.

For PCI to local transfers, Lwords are read from the PCI bus and loaded into the FIFO. On the local side, the Lwords are assembled from the FIFO, aligned to the local bus address and written to the local bus. On both the local and PCI buses, the byte enables for writes determine LA0, LA1 for the start of a transfer. For the last transfer the byte enables specify the bytes to be written. All reads are Lwords.

All PCI transfers(reads and writes) are Lwords(32 bits).

3.6.4 Demand Mode DMA

A bit in each channel can specify that the channel operate in Demand Mode. In Demand Mode, the user sets up the DMA controller's configuration registers and initiates a transfer. Data is transferred when the DMA channels DREQ# input is asserted. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers data until the transfer count is reached. The minimum transfer size per DREQ# input is one Lword (32bits). This may result in multiple transfers for an 8 or 16 bit bus. Refer to the timing diagrams included in this specification.

3.6.5 DMA Priority

DMA channel 0 priority, DMA channel 1 priority or rotating priority can be specified in the DMA Arbitration Register.

3.6.6 DMA Arbitration

The PCI9060 DMA controller releases control of the local bus (deassert LHOLD) once its FIFOs are full in a local to PCI transfer, its FIFOs are empty in a PCI to local transfer, when the local latency timer expires, when the BREQ input is asserted or a Direct Slave access is pending.

The DMA controller releases control of the PCI bus when the FIFOs are full/empty, when the PCI latency timer expires and it loses the PCI grant signal, or a Target Disconnect response is received. It de-asserts its PCI bus request (REQ#) for a minimum of 2 PCI clocks.

3.6.6.1 Local Latency and Pause Timers

A local bus latency timer and local bus pause timer are programmable through the DMA Arbitration Register. If the local latency timer expires, the PCI9060 completes the current Lword transfer and release LHOLD. After its programmable Pause Timer expires, it reasserts LHOLD. When it receives LHOLDA, it continues with the transfer. The PCI bus transfer continues until the FIFO is empty for a local to PCI transfer or until full for a PCI to local transfer.

3.7 BREQ input.

When the PCI9060 owns the local bus, its LHOLD output is asserted and its LHOLDA input is asserted. When the PCI9060 samples BREQ asserted during a DMA transfer or a Direct Slave read or write transfer, it gives up the local bus within two Lword transfers by deasserting LHOLD and floating its local bus outputs. The local arbiter can now grant the local bus to another local master. After the PCI9060 samples that its LHOLDA is deasserted and its local pause timer is zero, it will re-assert LHOLD to request the local bus. When the PCI9060 receives LHOLDA it will drive the bus and continue where it left off.

3.8 Doorbell Registers

There are two 32 bit doorbell interrupt/status registers in the PCI9060. One is assigned to the PCI bus interface, while the other is assigned to the local bus interface.

The local processor can generate a PCI bus interrupt by writing to the PCI doorbell register

A PCI host can generate a local bus interrupt by writing to the local doorbell register.

3.9 Mailbox Registers

There are eight 32 bit mailbox registers in the PCI9060 that can be written and read by both buses. These registers can be used to pass command and status information directly between PCI bus devices and local bus devices.

3.10 Interrupts

3.10.1 PCI Interrupts (INTA#)

The local to PCI doorbell register, local interrupt input, or a master/target abort status condition, can generate a PCI9060 PCI Interrupt (INTA#).

INTA# or individual sources of an interrupt can be enabled or disabled through the PCI9060 Interrupt Control/Status Register. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI9060 PCI bus interrupt is an asynchronous level output. An interrupt can be cleared by disabling a sources interrupt enable bit or clearing the cause of an interrupt.

3.10.1.1 Doorbell Interrupt

A local bus master can generate a PCI bus interrupt by writing to the Local to PCI Doorbell Register. The PCI host processor can then read the PCI9060 Interrupt Control/Status Register to determine that a doorbell interrupt is pending. It can then read the PCI9060 Local to PCI Doorbell Register.

Each bit in the Local to PCI Doorbell register is individually controlled. Bits in the Doorbell Register can only be set by the Local side.. From the local side, writing a 1 to any bit position sets that bit and writing a 0 to a bit position has no effect. Bits in the Local to PCI Doorbell Register can only be cleared from the PCI side. From the PCI side, writing a 1 to any bit position clears that bit and writing a 0 to a bit position has no effect.

The interrupt remains asserted as long any of the Local to PCI Doorbell Registers bits is set and the PCI Doorbell interrupt is enabled.

When the PCI bus is accessing the Doorbell Register (or any configuration register), the Local bus is held off from accessing the PCI9060 registers and the local READYo# signal is deasserted.

3.10.1.2 Local Interrupt Input

Asserting Local bus input pin LINTi# can generate a PCI bus interrupt. The PCI host processor can read the PCI9060 Interrupt Control/Status Register to determine that an interrupt is pending due to the LINTi# pin being asserted.

The interrupt remains asserted as long as the LINTi# pin is asserted and the Local Interrupt input is enabled. Adapter specific action can be taken by the PCI host processor to cause the Local bus to release LINTi#.

3.10.1.3 Master/Target Abort Interrupt

The PCI9060 sets the master abort or target abort status bit in the PCI configuration register upon detection of a master or target abort. These status bits cause PCI INTA# to be asserted if interrupts are enabled.

The interrupt remains asserted as long as the master or target abort bits remain set in the PCI Configuration Status Register and master/target abort interrupt is enabled. A PCI type 0 configuration access or a local access must be used to clear the master abort and target abort interrupt bits in the PCI Configuration Status Register.

Bits 24-26 of the Interrupt Control/Status Register are latched at the time of a target abort interrupt or a master abort interrupt. They provide information as to who was master when an abort occurred. They are updated whenever an abort occurs. If an abort interrupt is not pending, they have are not defined.

3.10.2 Local Interrupts (LINTo#)

The PCI to local doorbell register, a PCI BIST interrupt, DMA channel 0, or DMA channel 1 can generate a PCI9060 local interrupt. (LINT0#)

LINTo# or individual sources of an interrupt can be enabled or disabled through the PCI9060 Interrupt Control/Status Register. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI9060 local interrupt is a synchronous level output. An interrupt can be cleared by disabling a source's interrupt enable bit or clearing the cause of an interrupt.

3.10.2.1 Doorbell Interrupt

A PCI bus master can generate a local bus interrupt by writing to the PCI to Local Doorbell Register. The Local processor can then read the PCI9060 Interrupt Control/Status Register to determine that a doorbell interrupt is pending. It can then read the PCI9060 PCI to Local Doorbell Register.

Each bit in the PCI to Local Doorbell register is individually controlled. Bits in the Doorbell Register can only be set by the PCI side.. From the PCI side, writing a 1 to any bit position sets that bit and writing a 0 to a bit position has no effect. Bits in the PCI to Local Doorbell Register can only be cleared from the Local side. From the Local side, writing a 1 to any bit position clears that bit and writing a 0 to a bit position has no effect.

The interrupt remains asserted as long any of the PCI to Local Doorbell Registers bits is set and the Local Doorbell interrupt is enabled.

When the Local bus is accessing the Doorbell Register (or any configuration register), the PCI bus is issued a RETRY.

3.10.2.2 Built In Self Test Interrupt (BIST)

A PCI bus master can generate a local bus interrupt by performing a PCI type 0 configuration write to a bit in the PCI BIST register. The Local processor can then read the PCI9060 Interrupt Control/Status Register to determine that a BIST interrupt is pending.

The interrupt remains asserted as long as the bit is set and the BIST interrupt is enabled. The Local bus should reset the bit when BIST is complete. PCI Host software may fail the device if the bit is not reset after 2 seconds.

3.10.2.3 DMA Channel 0/Channel 1 Interrupts

A DMA channel can generate a local bus interrupt when done (transfer complete) or after a transfer is complete for a descriptor in chaining mode. The Local processor can then read the PCI9060 Interrupt Control/Status Register to determine that a DMA channel's interrupt is pending. A Done Status Bit in the Control/Status Register can be used to determine if the interrupt is a done interrupt or as the result of a transfer for a descriptor in a chain completing.

A channel's Mode Register is used to enable a done interrupt. In chaining mode, a bit in the channel's Next Descriptor Pointer Register (loaded from local memory) specifies if an interrupt should be generated at the end of the transfer for the current descriptor.

A channel's interrupt is cleared by writing to a bit in the DMA Command/Status Register.

3.10.3 PCI SERR# (PCI NMI)

The PCI9060 generates an SERR# pulse if parity checking is enabled in the PCI Command Register and it detects an address parity error or the Generate SERR# Bit in the Interrupt Control/Status Register is 0 and a 1 is written.

The SERR# output can be enabled or disabled through the PCI Command Register.

3.10.4 Local LSERR# (Local NMI)

The LSERR# interrupt output is asserted if the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register or a parity error status bit is set in the PCI Status Configuration Register.

If parity error checking is enabled in the PCI Command Register, the PCI9060 sets the Master Detected Parity Error Status bit in the PCI Status Register if it detects a parity error during a PCI9060 master read or it detects the PCI bus signal PERR# being asserted during a PCI9060 master write.

If the PCI9060 detects a data parity error during a PCI9060 master read, a data parity error during a slave write access to the PCI9060 or the PCI9060 detects an address parity error, it sets a parity error bit in the PCI Status Register.

The PCI9060 Interrupt Control/Status Register can be used to individually enable or disable LSERR# for an abort or parity error. LSERR# is a level output which remains asserted as long as the Abort or Parity Error Status Bits are set.

4. SECTION 4 - REGISTERS

4.1 Register Address Mapping

PCI CONFIGURATION REGISTERS

Local (Offset from chip select address)	**To ensure software compatibility with other versions of PCI9060 family and to ensure compatibility with future enhancement, all unused bits should be written to 0.** 31 23 15 7 0				PCI CFG register address
00h	Device ID		Vendor ID		00h
04h	Status		Command		04h
08h	Class Code			Revision ID	08h
0ch	BIST	Header Type	Latency Timer	Cache Line Size	0Ch
10h	PCI Base Address for Memory Mapped Runtime Registers				10h
14h	PCI Base Address for I/O Mapped Runtime Registers				14h
18h	PCI Base Address for Local Address Space 0				18h
1Ch					1Ch
20h					20h
24h					24h
28h	Reserved				28h
2Ch	Reserved				2Ch
30h	PCI Base Address to local Expansion ROM				30h
34h	Reserved				34h
38h	Reserved				38h
3Ch	Max_lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

LOCAL CONFIGURATION REGISTERS

Local (Offset from chip select address)	**To ensure software compatibility with other versions of PCI9060 family and to ensure compatibility with future enhancement, all unused bits should be written to 0.** 31 0	PCI (Offset from Runtime Base addr)
80h	Range for PCI to Local Address Space 0	00h
84h	Local Base Address (Re-map) for PCI to Local Address Space 0	04h
88h	Reserved	08h
8Ch	Reserved	0Ch
90h	Range for PCI to Local Expansion ROM	10h
94h	Local Base Address (Re-map) for PCI to Local Expansion ROM and BREQo control	14h
98h	Bus Region Descriptors for PCI to Local Accesses	18h
9Ch	Range for Direct Master to PCI	1Ch
A0h	Local Base Address for Direct Master to PCI Memory	20h
A4h	Local Base Address for Direct Master to PCI IO/CFG	24h
A8h	PCI Base Address (Re-map) for Direct Master to PCI	28h
ACh	PCI Configuration Address Register for Direct Master to PCI IO/CFG	2Ch

SHARED RUN TIME REGISTERS

Local (Offset from chip select address)	**To ensure software compatibility with other versions of PCI9060 family and to ensure compatibility with future enhancement, all unused bits should be written to 0.** 31 0	PCI (Offset from Runtime Base addr)
C0h	Mailbox Register 0	40h
C4h	Mailbox Register 1	44h
C8h	Mailbox Register 2	48h
CCh	Mailbox Register 3	4Ch
D0h	Mailbox Register 4	50h
D4h	Mailbox Register 5	54h
D8h	Mailbox Register 6	58h
DCh	Mailbox Register 7	5Ch
E0h	PCI to Local Doorbell Register	60h
E4h	Local to PCI Doorbell Register	64h
E8h	Interrupt Control / Status	68h
ECh	EEPROM Control, PCI Command Codes, User I/O Control, Init Control	6Ch

LOCAL DMA REGISTERS

Local (Offset from chip select address)	**To ensure software compatibility with other versions of PCI9060 family and to ensure compatibility with future enhancement, all unused bits should be written to 0.** 31 0	PCI (Offset from Runtime Base addr) (See Note 1)
100h	DMA Ch 0 Mode	100h
104h	DMA Ch 0 PCI Address	104h
108h	DMA Ch 0 Local Address	108h
10Ch	DMA Ch 0 Transfer Byte Count	10Ch
110h	DMA Ch 0 Descriptor Pointer	110h
114h	DMA Ch 1 Mode	114h
118h	DMA Ch 1 PCI Address	118h
11Ch	DMA Ch 1 Local Address	11Ch
120h	DMA Ch 1 Transfer Byte Count	120h
124h	DMA Ch 1 Descriptor Pointer	124h
128h	DMA Command/Status Register	128h
12Ch	DMA Arbitration Register 0	12Ch
130h	DMA Arbitration Register 1	130h

Note 1: The DMA Registers are accessible from the PCI side for the 9060 REV. 3. The special design consideration requirements are as follows:

Method I: Direct Slave access (Space 0) to DMA Registers.

1. Set the Local Base Address (Re-map) Register (Table 24) for Space 0 to point to the address space in which the local bus accesses the PCI9060 local register.
2. Program the Local Bus Region Descriptor Register (Table 29) to bit[1:0]=11; 32 bit bus, and bit[7]=0; Bterm input disabled.
3. If PCI9060 READYo# pin is connected or driven by the PCI9060 READYi#, then set the bit[5:2]=0000; 0 wait state, and bit[6]=1; Ready input enabled, on Table 29(Local Bus Descriptor Register).
4. If PCI9060 READYo# pin does not cause the PCI9060 READYi#, then set the bit[5:2]=0010; 2 wait states, and bit[6]=0; Ready input disabled, on Table 29(Local Bus Descriptor Register).
5. Read or write the PCI9060 DMA Registers by performing a PCI to Local access to Local Address Space 0. (Address bits[8:2] specify the DMA Register offset.)

Method II: Direct Slave access (Expansion ROM) to DMA Registers

1. set the Local Base Address (Re-map) Register (Table 28) for the Expansion ROM to point to the address space in which the local bus accesses the PCI9060 local register.
2. Program the Local Bus Region Descriptor Register (Table 29) to bit[17:16]=11; 32 bit bus, and bit[23]=0; Bterm input disabled.
3. If PCI9060 READYo# pin is connected or driven by the PCI9060 READYi#, then set the bit[21:18]=0000; 0 wait state, and bit[22]=1; Ready input enabled, on the Table 29(Local Bus Descriptor Register).
4. If PCI9060 READYo# pin does not cause the PCI9060 READYi#, then set the bit[21:18]=0010; 2 wait states, and bit[22]=0; Ready input disabled, on the Table 29(Local Bus Descriptor Register).
5. Read or write the PCI9060 DMA Registers by performing a PCI to Local access to Local Address Expansion ROM (Address bits[8:2] specify the DMA Register offset.)

4.2 PCI Configuration Registers

All registers may be written to or read from in byte, word or long word accesses.

4.2.1 PCI Configuration ID Register (Offset 00h)

Table 1: PCI Configuration ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX (10B5h) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low.	Yes	Local Bus	10B5h or 0
31:16	Device ID - Identifies the particular device. Defaults to the PLX part number for PCI interface chip (9060h) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low.	Yes	Local Bus	9060h or 0

4.2.2 PCI Command Register (Offset 04h)

Table 2: PCI Command Register Description

Field	Description	Read	Write	Value after Reset
0	I/O Space. A value of 1 allows the device to respond to I/O space accesses. A value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. A value of 1 allows the device to respond to memory space accesses. A value of 0 disables the device from responding to memory space accesses.	Yes	Yes	0
2	Master Enable. Controls a device's ability to act as a master on the PCI bus. A value of 1 allows the device to behave as a bus master. A value of 0 disables the device from generating bus master accesses. State after RST# is 0.	Yes	Yes	0
3	Special Cycle. This bit is not supported.	Yes	No	0
4	Memory Write/Invalidate. This bit is not supported.	Yes	No	0
5	VGA Palette Snoop. This bit is not supported.	Yes	No	0
6	Parity Error Response. A value of 0 indicates that a parity error is ignored and operation continues. A value of 1 indicates that parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether or not the device does address/data stepping. A 0 value indicates the device never does stepping. A value of 1 indicates that the device always does stepping. This value is hardwired to 0.	Yes	No	0
8	SERR# Enable. A value of 1 enables the SERR# driver. A value of 0 disables the driver	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. A value of 1 indicates that fast back-to-back transfers can occur to any agent on the bus. A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15:10	Reserved.	Yes	No	0

4.2.3 PCI Status Register (Offset 06h)

Table 3: PCI Status Register Description

Field	Description	Read	Write	Value after Reset
6:0	Reserved	Yes	No	0
7	Fast Back-to-Back Capable. When this bit is set to a 1, it indicates the adapter can accept fast back-to-back transactions. A 0 indicates the adapter cannot.	Yes	No	1
8	Master Data Parity Error Detected. This bit is set to a 1 when three conditions are met: 1) the PCI9060 asserted PERR# itself or observed PERR# asserted; 2) the PCI9060 was the bus master for the operation in which the error occurred; 3) the Parity Error Response bit in the Command Register is set. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. a value of 01 is medium.	Yes	No	01
11	Target Abort. When this bit is set to a 1, this bit indicates the PCI9060 has signaled a target abort. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
12	Received Target Abort. When set to a 1, this bit indicates the PCI9060 has received a target abort signal. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
13	Received Master Abort. When set to a 1, this bit indicates the PCI9060 has received a master abort signal. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
14	Signaled System Error. When set to a 1, this bit indicates the PCI9060 has reported a system error on the SERR# signal. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
15	Detected Parity Error. When set to a 1, this bit indicates the PCI9060 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). One of three conditions can cause this bit to be set. 1) the PCI9060 detected a parity error during a PCI address phase; 2) the PCI9060 detected a data parity error when it was the target of a write; 3) the PCI9060 detected a data parity error when performing a master read operation. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0

4.2.4 PCI Revision ID Register (Offset 08h)

Table 4: PCI Revision ID Register Description

Field	Description	Read	Write	Value after Reset
7:0	Revision ID. The silicon revision of the PCI9060.	Yes	Local Bus	Current Rev #

4.2.5 PCI Class Code Register (Offset 09 - 0Bh)

Table 5: PCI Class Code Register Description

Field	Description	Read	Write	Value after Reset
7:0	Specific register level programming interface (00h). No interface defined.	Yes	Local Bus	00
15:8	Sub-class Encoding (80h). Other bridge device.	Yes	Local Bus	80h
23:16	Base Class Encoding other Bridge Device	Yes	Local Bus	06h

4.2.6 PCI Cache Line Size Register (Offset 0Ch)

Table 6: PCI Cache Line Size Register Description

Field	Description	Read	Write	Value after Reset
7:0	System cache line size in units of 32-bit words. Not supported.	Yes	No	0

4.2.7 PCI Latency Timer Register (Offset 0Dh)

Table 7: PCI Latency Timer Register Description

Field	Description	Read	Write	Value after Reset
7:0	Latency Timer. Specifies in units of PCI bus clocks, the amount of time the PCI9060, as a bus master, can burst data on the PCI bus.	Yes	Yes	0

4.2.8 PCI Header Type Register (Offset 0Eh)

Table 8: PCI Header Type Register Description

Field	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies the layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	Local Bus	0
7	Header Type. A 1 indicates multiple functions, a 0 indicates a single function.	Yes	Local Bus	0

4.2.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0Fh)

Table 9: PCI Built-in Self Test (BIST) Register Description

Field	Description	Read	Write	Value after Reset
3:0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device specific failure codes can be encoded in the non-zero value.	Yes	Local Bus	0
5:4	Reserved, Device returns 0.	Yes	No	0
6	PCI writes a 1 to invoke BIST. Generates an interrupt to local bus. Local bus resets the bit when BIST is complete. Software should fail device if BIST is not complete after 2 seconds. Refer to run time registers for interrupt control/status.	Yes	Yes	0
7	Return 1 if device supports BIST. Return 0 if the device is not BIST compatible.	Yes	Local Bus	0

4.2.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 10h)

Table 10: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space.	Yes	No	0
2:1	Location of register: 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 MByte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved	Yes	No	0
3	Prefetchable. A value of 1 indicates there are no side effects on reads.	Yes	No	0
6:4	Memory Base Address. Memory base address for access to runtime registers. (Minimum Back Size = 128 bytes.)	Yes	No	0
31:7	Memory Base Address. Memory base address for access to Local Configuration and Shared Run Time registers. (Minimum Block Size = 128 bytes.)	Yes	Yes	0

4.2.11 PCI Base Address Register for I/O Access to Runtime Registers(Offset 14h)

Table 11: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space.	Yes	No	1h
1	Reserved	Yes	No	0
6:2	I/O Base Address. Base Address for I/O access to runtime registers. (Minimum Block Size = 128 bytes.)	Yes	No	0
31:7	I/O Base Address. Base Address for I/O access to Local Configuration and Shared Run Time Registers. (Minimum Block Size = 128 bytes.)	Yes	Yes	0

4.2.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 18h)

Table 12: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in Table 23: Local Address Space 0 Range Register Description, LOC 80h.)	Yes	No	0
2:1	Location of register: 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 MByte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved (Specified in Table 23: Local Address Space 0 Range Register Description, LOC 80h.)	Yes	No	0
3	Prefetchable. A value of 1 indicates there are no side effects on reads. Refer to bit #3 on the Table 23. (Specified in Table 23: Local Address Space 0 Range Register Description, LOC 80h.)	Yes	No	0
31:4	Memory Base Address. Memory base address for access to local address space (Used in conjunction with PCI Configuration Resister LOC 80h).	Yes	Yes	0

4.2.13 PCI Base Address Register (Offset 1Ch)

Table 13: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	0

4.2.14 PCI Base Address Register (Offset 20h)

Table 14: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	0

4.2.15 PCI Base Address Register (Offset 24h)

Table 15: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	0

4.2.16 PCI Base Address Register (Offset 28h)

Table 16: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	0

4.2.17 PCI Base Address Register (Offset 2Ch)

Table 17: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	0

4.2.18 PCI Expansion ROM Base Register (Offset 30h)

Table 18: PCI Expansion ROM Base Register Description

Field	Description	Read	Write	Value after Reset
0	Address Decode Enable. A value of 1 indicates the device accepts accesses to the expansion ROM address. A value of 0 indicates the device does not accept accesses to expansion ROM space. Should be set to 0 if no Expansion ROM.	Yes	Yes	1
10:1	Reserved	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits)	Yes	Yes	0

4.2.19 PCI Interrupt Line Register (Offset 3Ch)

Table 19: PCI Interrupt Line Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Value indicates which input of the system interrupt controller(s) the device's interrupt line is connected to.	Yes	Yes	0

4.2.20 PCI Interrupt Pin Register (Offset 3Dh)

Table 20: PCI Interrupt Pin Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Pin register. Indicates which interrupt pin the device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Local Bus	1h

4.2.21 PCI Min_Gnt Register (Offset 3Eh)

Table 21: PCI Min_Gnt Register Description

Field	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Used to specify how long a burst period the device needs assuming a clock rate of 33 MHz. Value is multiple of 1/4 usec increments.	Yes	Local Bus	0

4.2.22 PCI Max_Lat Register (Offset 3Fh)

Table 22: PCI Max_Lat Register Description

Field	Description	Read	Write	Value after Reset
7:0	Max_Lat. Used to specify how often the device needs to gain access to the PCI bus. Value is multiple of 1/4 usec increments.	Yes	Local Bus	0

4.3 Local Configuration Registers

4.3.1 Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h)

Table 23: Local Address Space 0 Range Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 0 maps into PCI memory space. A value of 1 indicates address space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: 2/1 Meaning 0 0 locate anywhere in 32 bit PCI address space 0 1 locate below 1 Meg in PCI address space 10 locate anywhere in 64 bit PCI address space 1 1 reserved If mapped into I/O space, bit 1 must be a 0. bit 2 is included with bits 3 through 31 to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates that reads are pre-fetch able. If mapped into I/O space, bit is included with bits 2 through 31 to indicate decoding range.	Yes	Yes	0
31:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 0. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 18h). Default is 1 Meg.	Yes	Yes	FFF0000h

4.3.2 Local Address Space 0 Local Base Address (Re-map) Register for PCI to Local Bus (PCI 04h) (LOC 84h)

Table 24: Local Address Space 0 Local Base Address (Re-map) Register Description

Field	Description	Read	Write	Value after Reset
0	Space 0 Enable. A 1 value enables Decode of PCI addresses for Direct Slave access to local space 0. A value of 0 disables Decode.	Yes	Yes	0
1	Not Used	Yes	Yes	0
3:2	If local space 0 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits 4 through 31 for re-mapping.	Yes	Yes	0
31:4	Re-map of PCI Address to Local Address Space 0 into a Local Address Space. The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0

4.3.3 Local Register (PCI 08h) (LOC 88h)

Table 25: Local Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	000000FFh

4.3.4 Local Register (PCI 0ch) (LOC 8ch)

Table 26: Local Register Description

Field	Description	Read	Write	Value after Reset
31:0	Reserved	Yes	No	000000FFh

4.3.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 10h) (LOC 90h)

Table 27: Local Expansion ROM Range register Description

Field	Description	Read	Write	Value after Reset
10:0	Not used	Yes	Yes	0
31:11	Specifies which PCI address bits will be used to decode a PCI to local bus expansion ROM. Each of the bits corresponds to an Address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 30h). Default is 64 KBytes.	Yes	Yes	FFFF00h

4.3.6 Local Expansion ROM Local Base Address (Re-map) register for PCI to Local Bus and BREQo Control (PCI 14h) (LOC 94h)

Table 28: Local Expansion ROM Local Base Address(Re-map) and BREQo register Description

Field	Description	Read	Write	Value after Reset
3:0	Direct Slave BREQo Delay Clocks . (# of local bus clocks in which a Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (HOLDA) before asserting BREQo. Once asserted, BREQo remains asserted until the PCI9060 receives HOLDA (LSB= 8 clocks)	Yes	Yes	0
4	Local Bus BREQo Enable. A 1 value enables the PCI9060 to assert the BREQo output.	Yes	Yes	0
10:5	Not Used	Yes	No	0
31:11	Re-map of PCI Expansion ROM space into a Local address space. The bits in this register re-map (replace) the PCI address bits used in decode as the Local address bits.	Yes	Yes	0

4.3.7 Local Bus Region Descriptor for PCI to Local Accesses Register (PCI 18h) (LOC 98h)

Table 29: Local Bus Region Descriptor for PCI to Local Accesses Register Description

Field	Description	Read	Write	Value after Reset
1:0	Memory Space 0 Local Bus Width. Programmable for the Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 or 11 indicates a bus width of 32 bits. The bus width is forced to 16 bits for the Sx mode	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Memory Space 0 Internal Wait States (data to data).	Yes	Yes	0
6	Memory Space 0 Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
7	Memory Space 0 Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
8	Memory Space 0 Prefetch Disable. If mapped into memory space, a 0 enables read pre-fetching, a value of 1 disables prefetching. If pre-fetching is disabled, the PCI9060 will disconnect after each memory read.	Yes	Yes	0
9	Expansion ROM Space Prefetch Disable. A 0 enables read pre-fetching, a value of 1 disables prefetching. If pre-fetching is disabled, the PCI9060 will disconnect after each memory read.	Yes	Yes	0
15:10	Not Used	Yes	Yes	0
17:16	Expansion ROM Space Local Bus Width. Programmable for the Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 or 11 indicates a bus width of 32 bits. The bus width is forced to 16 bits for the Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
21:18	Expansion ROM Space Internal Wait States (data to data).	Yes	Yes	0
22	Expansion ROM Space Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
23	Expansion ROM Space Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
24	Memory Space 0 Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
25	Not Used	Yes	Yes	0
26	Expansion ROM Space Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
27	Direct Slave PCI write mode. A 0 indicates that the PCI9060 should disconnect when the Direct Slave write FIFO is full. A 1 indicates that the PCI9060 should de-assert TRDY when the write FIFO is full.	Yes	Yes	0
31:28	PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the # of PCI bus clocks after receiving a PCI-Local read or write access and not successfully completing a transfer. Only pertains to Direct Slave writes when bit 27 is set to 1.	Yes	Yes	4 (32 clocks)

4.3.8 Local Range register for Direct Master to PCI (PCI 1Ch) (LOC 9Ch)

Table 30: Local Range register for Direct Master to PCI Description

Field	Description	Read	Write	Value after Reset
15:0	Not Used (64KByte increments)	Yes	No	0
31:16	Specifies which Local address bits will be used to decode a Local to PCI bus access. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others.	Yes	Yes	0

4.3.9 Local Bus Base Address register for Direct Master to PCI Memory (PCI 20h) (LOC A0h)

Table 31: Local Bus Base Address register for Direct Master to PCI Memory

Field	Description	Read	Write	Value after Reset
15:0	Not Used.	Yes	No	0
31:16	Assigns a value to the bits which will be used to decode a Local to PCI memory access.	Yes	Yes	0

4.3.10 Local Base Address for Direct Master to PCI IO/CFG Register (PCI 24h) (LOC A4h)

Table 32: Local Base Address for Direct Master to PCI IO/CFG Register

Field	Description	Read	Write	Value after Reset
15:0	Not Used	Yes	No	0
31:16	Assigns a value to the bits which will be used to decode a Local to PCI I/O or configuration access	Yes	Yes	0

4.3.11 PCI Base Address (Re-map) register for Direct Master to PCI (PCI 28h) (LOC A8h)

Table 33: PCI Base Address (Re-map) register for Direct Master to PCI Description

Field	Description	Read	Write	Value after Reset
0	Direct Master Memory Access Enable. A 1 value enables decode of Direct Master Memory accesses. A value of 0 disables decode of Direct Master Memory accesses.	Yes	Yes	0
1	Direct Master I/O Access Enable. A 1 value enables decode of Direct Master I/O accesses. A value of 0 disables decode of Direct Master I/O accesses.	Yes	Yes	0
2	LOCK Input Enable. A 1 value enables LOCK input, enabling PCI locked sequences. A value of 0 disables the LOCK input.	Yes	Yes	0
3	Direct Master Read Prefetch Size control. If set to a value of 0, the PCI9060 continues to prefetch read data until the Direct Master access is finished. This may result in an additional 4 un-needed Lwords being pre-fetched from the PCI bus. If set to a value of 1 the PCI9060 reads up to 4 Lwords from the PCI bus for each Direct Master burst read access. This mode must not be used for direct master burst reads that exceed 4 Lwords.	Yes	Yes	0
4	Direct Master PCI read mode. A value of 0 indicates that the PCI9060 should release the PCI bus when the read FIFO becomes full. A value of 1 indicates that the PCI9060 should keep the PCI bus and de-assert IRDY when the read FIFO becomes full.	Yes	Yes	0
7:5	Programmable Almost Full Flag. When the number of entries in the 8 deep direct master write FIFO exceed this value, the output pin DMPAF# is asserted low.	Yes	Yes	0
15:8	Not Used.	Yes	No	0
31:16	Re-map of Local to PCI space into a PCI address space. The bits in this register re-map (replace) the Local address bits used in decode as the PCI address bits.	Yes	Yes	0

4.3.12 PCI Configuration Address Register for Direct Master to PCI IO/CFG (PCI 2Ch) (LOC ACh)

Table 34: PCI Configuration Address Register for Direct Master to PCI IO/CFG

Field	Description	Read	Write	Value after Reset
1:0	Configuration Type. 00=Type 0 01=Type 1	Yes	Yes	0
7:2	Register Number	Yes	Yes	0
10:8	Function Number	Yes	Yes	0
15:11	Device Number	Yes	Yes	0
23:16	Bus Number	Yes	Yes	0
30:24	Reserved	Yes	Yes	0
31	Configuration Enable. A value of 1 allows Local to PCI I/O accesses to be converted to a PCI configuration cycle. The Parameters in this table are used to generate the PCI configuration address.	Yes	Yes	0

4.4 Shared Runtime Registers

4.4.1 Mailbox Register 0 (PCI 40h) (LOC C0h)

Table 35: Mailbox Register 0 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.2 Mailbox Register 1 (PCI 44h) (LOC C4h)

Table 36: Mailbox Register 1 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.3 Mailbox Register 2 (PCI 48h) (LOC C8h)

Table 37: Mailbox Register 2 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.4 Mailbox Register 3 (PCI 4Ch) (LOC CCh)

Table 38: Mailbox Register 3 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.5 Mailbox Register 4 (PCI 50h) (LOC D0h)

Table 39: Mailbox Register 4 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.6 Mailbox Register 5 (PCI 54h) (LOC D4h)

Table 40: Mailbox Register 5 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.7 Mailbox Register 6 (PCI 58h) (LOC D8h)

Table 41: Mailbox Register 6 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.8 Mailbox Register 7 (PCI 5Ch) (LOC DCh)

Table 42: Mailbox Register 7 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.9 PCI to Local Doorbell Register (PCI 60h) (LOC E0h)

Table 43: PCI to Local Doorbell Register Description

Field	Description	Read	Write	Value after Reset
31:0	Doorbell register. A PCI master can write to this register and it will generate a local interrupt to the local processor. The local processor can then read this register to determine which doorbell bit was asserted. The PCI master sets a doorbell by writing a 1 to a particular bit. The local processor can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

4.4.10 Local to PCI Doorbell Register (PCI 64h) (LOC E4h)

Table 44: Local to PCI Doorbell Register Description

Field	Description	Read	Write	Value after Reset
31:0	Doorbell register. The local processor can write to this register and it will generate a PCI interrupt. A PCI master can then read this register to determine which doorbell bit was asserted. The local processor sets a doorbell by writing a 1 to a particular bit. The PCI master can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

4.4.11 Interrupt Control/Status (PCI 68h) (LOC E8h)

Table 45: Interrupt Control/Status

Field	Description	Read	Write	Value after Reset
0	Enable Local bus LSERR#. A value of 1 will enable the PCI9060 to assert LSERR# interrupt output when the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register.	Yes	Yes	0
1	Enable Local bus LSERR# when a PCI parity error occurs during a PCI9060 Master Transfer or a PCI9060 Slave access.	Yes	Yes	0
2	Generate PCI bus SERR#. When this bit is 0, writing a 1 generates a PCI bus SERR#.	Yes	Yes	0
7:3	Not Used	Yes	No	0
8	PCI interrupt enable. A value of 1 will enable PCI interrupts .	Yes	Yes	1
9	PCI doorbell interrupt enable. A value of 1 will enable doorbell interrupts . Used in conjunction with PCI interrupt enable. Clearing the doorbell interrupt bits causing the interrupt will clear the interrupt.	Yes	Yes	0
10	PCI Abort interrupt enable. A value of 1 will enable a master abort or master detect of a target abort to generate a PCI interrupt . Used in conjunction with PCI interrupt enable. Clearing the abort status bits will clear the PCI interrupt.	Yes	Yes	0
11	PCI local interrupt enable. A value of 1 will enable a local interrupt input to generate a PCI interrupt . Use in conjunction with PCI interrupt enable. Clearing the local bus cause of the interrupt will clear the interrupt.	Yes	Yes	0
12	Retry Abort Enable. A value of 1 will enable the PCI9060 to treat 256 Master consecutive retries to a Target as a Target Abort. A value of 0 will enable the PCI9060 to attempt Master Retries indefinitely.	Yes	Yes	0
13	A value of 1 indicates that the PCI doorbell interrupt is active.	Yes	No	0
14	A value of 1 indicates that the PCI abort interrupt is active.	Yes	No	0
15	A value of 1 indicates that the local interrupt input is active.	Yes	No	0
16	Local interrupt output enable. A value of 1 will enable Local interrupt output .	Yes	Yes	1
17	Local doorbell interrupt enable. A value of 1 will enable doorbell interrupts . Used in conjunction with Local interrupt enable. Clearing the Local doorbell interrupt bits causing the interrupt will clear the interrupt.	Yes	Yes	0
18	Local DMA channel 0 interrupt enable. A value of 1 will enable DMA channel 0 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits will clear the interrupt.	Yes	Yes	0
19	Local DMA channel 1 interrupt enable. A value of 1 will enable DMA channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits will clear the interrupt.	Yes	Yes	0
20	A value of 1 indicates that the Local doorbell interrupt is active.	Yes	No	0
21	A value of 1 indicates that the DMA ch 0 interrupt is active.	Yes	No	0
22	A value of 1 indicates that the DMA ch 1 interrupt is active.	Yes	No	0
23	A value of 1 indicates that the BIST interrupt is active. The BIST (built in self test) interrupt is generated by writing a 1 to bit 6 of the PCI Configuration BIST register. Clearing bit 6 clears the interrupt. Refer to the BIST register for a description of self test.	Yes	No	0
24	A value of 0 indicates that a Direct Master was the bus master during a Master or Target abort.	Yes	No	0
25	A value of 0 indicates that DMA CH 0 was the bus master during a Master or Target abort.	Yes	No	0
26	A value of 0 indicates that a DMA CH 1 was the bus master during a Master or Target abort.	Yes	No	0
27	A value of 0 indicates that a Target Abort was generated by the PCI9060 after 256 consecutive Master retries to a Target.	Yes	Yes	0
31:28	Not Used	Yes	No	0

4.4.12 EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 6Ch) (LOC ECh)

Table 46: EEPROM Control, PCI Command Codes, User I/O Control, Init Control

Field	Description	Read	Write	Value after Reset
3:0	PCI Read Command Code for DMA	Yes	Yes	1110
7:4	PCI Write Command Code for DMA	Yes	Yes	0111
11:8	PCI Memory Read Command Code for Direct Master	Yes	Yes	0110
15:12	PCI Memory Write Command Code for Direct Master	Yes	Yes	0111
16	General Purpose Output. A value of 1 will cause the USERO output to go high . A value of 0 will cause the output to go low.	Yes	Yes	1h
17	General Purpose Input. A value of 1 indicates that USERI input pin is high. A value of 0 indicates that USERI pin is low.	Yes	No	--
23:18	Not Used	Yes	No	0
24	EEPROM clock for Local or PCI bus reads or writes to EEPROM. Toggling this bit generates an EEPROM clock. Refer to the manufacturer's data sheet for the particular EEPROM being used.	Yes	Yes	0
25	EEPROM chip select. For Local or PCI bus reads or writes to EEPROM, setting this bit to a 1 provides the EEPROM chip select.	Yes	Yes	0
26	Write bit to EEPROM. For writes, this output bit is the input to the EEPROM. It is clocked into the EEPROM by the EEPROM clock.	Yes	Yes	0
27	Read EEPROM data bit. For reads, this input bit is the output of the EEPROM. It is clocked out of the EEPROM by the EEPROM clock.	Yes	No	--
28	EEPROM present. A 1 in this bit indicates that an EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When this bit is 0, writing a 1 causes the PCI9060 to reload the PCI configuration registers from EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. A value of 1 written to this bit will hold the local bus logic in the PCI9060 reset and LRESETO# asserted. The contents of the PCI configuration registers and Shared Run Time registers will not be reset. Software Reset can only be cleared from the PCI bus.	Yes	Yes	0
31	Local Init Status 1 = local init done. Responses to PCI accesses will be RETRYs until this bit is set. While Input NB# is asserted low this bit will be forced to 1.	Yes	Yes	0

4.5 Local DMA Registers

4.5.1 DMA Channel 0 Mode Register (LOC 100h)

Table 47: DMA Channel 0 Mode Register Description

Field	Description	Read	Write	Value after Reset
1:0	Local DMA Bus Width. Programmable for the Cx and Jx modes only. A value of 00 indicates a DMA bus width of 8 bits, a value of 01 indicates a DMA bus width of 16 bits, a value of 11 indicates a DMA bus width of 32 bits(or 10 for 32 bit aligned only). The bus width is forced to 16 bits for the Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Internal Wait States (data to data).	Yes	Yes	0
6	Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
7	Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
8	Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
9	Chaining. A 0 value indicates non-chaining mode enabled. A 1 value indicates chaining mode enabled. For chaining mode, **Descriptor must be in memory rather than the registers in the Tables 48, 49, and 50.**	Yes	Yes	0
10	Done Interrupt Enable. A 1 value enables interrupt when done. A 0 value disables interrupt when done.	Yes	Yes	0
11	Local Addressing Mode. A 1 value indicates local address LA [31:2] to be held constant. A 0 value indicates local address is incremented.	Yes	Yes	0
12	Demand Mode. A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ# input is asserted. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers Lwords (32bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.	Yes	Yes	0
31:13	Reserved	Yes	No	0

4.5.2 DMA Channel 0 PCI Address Register (LOC 104h)

Table 48: DMA Channel 0 PCI Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	PCI Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) will start from.	Yes	Yes	0

4.5.3 DMA Channel 0 Local Address Register (LOC 108h)

Table 49: DMA Channel 0 Local Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Local Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) will start from.	Yes	Yes	0

4.5.4 DMA Channel 0 Transfer Size (Bytes) Register (LOC 10Ch)

Table 50: DMA Channel 0 Transfer Size (Bytes) Register Description

Field	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to be transferred during DMA operation.	Yes	Yes	0
31:23	Not Used	Yes	Yes	0

4.5.5 DMA Channel 0 Descriptor Pointer Register (LOC 110h)

Table 51: DMA Channel 0 Descriptor Pointer Register Description

Field	Description	Read	Write	Value after Reset
0	Reserved	Yes	Yes	0
1	End of Chain. A 1 value indicates end of chain. A 0 value indicates not end of chain descriptor. Note: 0 chaining mode implies that there is no chain (Same as Non-Chaining Mode.)	Yes	Yes	0
2	Interrupt after Terminal Count. A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached. A 0 value disables interrupts from being generated.	Yes	Yes	0
3	Direction of transfer. A 1 value indicates transfers from local bus to PCI bus. A 0 value indicates transfers from PCI bus to local bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned(Bit[3:0] = 0000).	Yes	Yes	0

4.5.6 DMA Channel 1 Mode Register (LOC 114h)

Table 52: DMA Channel 1 Mode Register Description

Field	Description	Read	Write	Value after Reset
1:0	Local Bus Width. Programmable for the Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 11 indicates a bus width of 32 bits(or 10 for 32 bit aligned only). The bus width is forced to 16 bits for the Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Internal Wait States (data to data).	Yes	Yes	0
6	Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
7	Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
8	Local Burst Enable. A 1 value enables Local bursting. A value of 0 disables Local bursting.	Yes	Yes	0
9	Chaining. A 1 value indicates chaining mode enabled. A 0 value indicates non-chaining mode enabled.	Yes	Yes	0
10	Done Interrupt Enable. A 1 value enables interrupt when done. A 0 value disables interrupt when done.	Yes	Yes	0
11	Local Addressing Mode. A 1 value indicates local address LA[31:2] to be held constant. A 0 value indicates local address is incremented.	Yes	Yes	0
12	Demand Mode. A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ# input is asserted. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers Lwords (32bits) of data . This may result in multiple transfers for an 8 or 16 bit bus.	Yes	Yes	0
31:13	Reserved	Yes	No	0

4.5.7 DMA Channel 1 PCI Data Address Register (LOC 118h)

Table 53: DMA Channel 1 PCI Data Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	PCI Data Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) will start from.	Yes	Yes	0

4.5.8 DMA Channel 1 Local Data Address Register (LOC 11Ch)

Table 54: DMA Channel 1 Local Data Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Local Data Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) will start from.	Yes	Yes	0

4.5.9 DMA Channel 1 Transfer Size (Bytes) Register (LOC 120h)

Table 55: DMA Channel 1 Transfer Size (Bytes) Register Description

Field	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to be transferred during DMA operation.	Yes	Yes	0
31:23	Not Used	Yes	Yes	0

4.5.10 DMA Channel 1 Descriptor Pointer Register (LOC 124h)

Table 56: DMA Channel 1 Descriptor Pointer Register Description

Field	Description	Read	Write	Value after Reset
0	Reserved	Yes	Yes	0
1	End of Chain. A 1 value indicates end of chain. A 0 value indicates not end of chain descriptor.	Yes	Yes	0
2	Interrupt after Terminal Count. A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached. A 0 value disables interrupts from being generated.	Yes	Yes	0
3	Direction of transfer. A 1 value indicates transfers from local bus to PCI bus. A 0 value indicates transfers from PCI bus to local bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned.	Yes	Yes	0

4.5.11 DMA Command/Status Register (LOC 128h)

Table 57: DMA Command/Status Register Description

Field	Description	Read	Write	Value after Reset
0	Channel 0 Enable. A 1 value enables the channel to transfer data. A 0 value disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (Pause).	Yes	Yes	0
1	Channel 0 Control. Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.	No	Yes	0
2	Channel 0 Control. Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. The channel complete bit is set when the abort has completed.	No	Yes	0
3	Writing a 1 to this bit clears channel 0 interrupts	No	Yes	0
4	Channel 0 Done. A 1 value indicates this channels transfer is complete. A 0 value indicates the channel transfer is not complete.	Yes	No	1
7:5	User Defined	Yes	Yes	0
8	Channel 1 Enable. A 1 value enables the channel to transfer data. A 0 value disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (Pause).	Yes	Yes	0
9	Channel 1 Control. Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.	No	Yes	0
10	Channel 1 Control. Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must cleared. The channel complete bit is set when the abort has completed.	No	Yes	0
11	Writing a 1 to this bit clears channel 1 interrupts	No	Yes	0
12	Channel 1 Done. A 1 value indicates this channel's transfer is complete. A 0 value indicates the channel transfer is not complete.	Yes	No	1
15:13	User Defined	Yes	Yes	0
31:16	Not Used	Yes	No	0

4.5.12 DMA Arbitration Register 0 (LOC 12Ch)

Table 58: DMA Arbitration Register 0 Description

Field	Description	Read	Write	Value after Reset
7:0	Local Bus Latency Timer. Number of local bus clock cycles before deasserting HOLD and releasing the local bus.	Yes	Yes	0
15:8	Local Bus Pause Timer. Number of local bus clock cycles before reasserting HOLD after releasing the local bus.	Yes	Yes	0
16	Local Bus Latency Timer Enable. A 1 value enables the latency timer.	Yes	Yes	0
17	Local Bus Pause Timer Enable. A 1 value enables the pause timer (Used for DMA only.)	Yes	Yes	0
18	Local Bus BREQ Enable. A 1 value enables the local bus BREQ input. When the BREQ input is active, the PCI9060 de-asserts HOLD and releases the local bus.	Yes	Yes	0
20:19	DMA Channel Priority. A value of 00 indicates a rotational priority scheme. A value of 01 indicates channel 0 has priority. A value of 10 indicates channel 1 has priority. A 11 value is reserved	Yes	Yes	0
31:21	Not Used	Yes	No	--

4.5.13 DMA Arbitration Register 1 (LOC 130h)

Table 59: DMA Arbitration Register 1 Description

Field	Description	Read	Write	Value after Reset
3:0	DMA Channel 0 PCI to Local Almost Full (C0PLAF): # of Full Entries (minus 1) in FIFO before Requesting Local Bus for Writes. (C0PLAF+1) + (C0PLAE+1) should be <= FIFO Depth of 16	Yes	Yes	0
7:4	DMA Channel 0 Local to PCI Almost Empty (C0LPAE): # of Empty Entries (minus 1) in FIFO before Requesting Local Bus for Reads. (C0LPAF+1) + (C0LPAE+1) should be <= FIFO depth of 16	Yes	Yes	0
11:8	DMA Channel 0 Local to PCI Almost Full (C0LPAF): # of Full Entries (minus 1) in FIFO before Requesting PCI Bus for Writes.	Yes	Yes	0
15:12	DMA Channel 0 PCI to Local Almost Empty (C0PLAE): # of Empty Entries (minus 1) in FIFO before Requesting PCI Bus for Reads.	Yes	Yes	0
18:16	DMA Channel 1 PCI to Local Almost Full (C1PLAF): # of Full Entries (minus 1) in FIFO before Requesting Local Bus for Writes . (C1PLAF+1) + (C1PLAE+1) should be <= FIFO depth of 8	Yes	Yes	0
19	Reserved	Yes	No	0
22:20	DMA Channel 1 Local to PCI Almost Empty (C1LPAE): # of Empty Entries (minus 1) in FIFO before Requesting Local Bus for Reads. (C1PLAF+1) + (C1PLAE+1) should be <= FIFO depth of 8	Yes	Yes	0
23	Reserved	Yes	No	0
26:24	DMA Channel 1 Local to PCI Almost Full (C1LPAF): # of Full Entries (minus 1) in FIFO before Requesting PCI Bus for Writes.	Yes	Yes	0
27	Reserved	Yes	No	0
30:28	DMA Channel 1 PCI to Local Almost Empty (C1PLAE): # of Empty Entries (minus 1) in FIFO before Requesting PCI Bus for Reads.	Yes	Yes	0
31	Reserved	Yes	No	0

5. SECTION 5 - PIN DESCRIPTION

5.1 Pin Summary

The following tables describe the PCI9060 pins. The pins in the following tables are common to all three local bus modes of operation (i.e. Cx mode, Jx mode, and Sx mode):

PCI System Bus Interface Pin Description
Local Bus Mode and Processor Independent Interface Pin Description
EEPROM interface Pin Description
Power and Ground Pin Description

The following tables correspond to the local bus mode of the PCI9060:

Cx Bus Mode Interface Pin Description (i960®Cx and Hx processors)
Jx Bus Mode Interface Pin Description (i960®Jx and Kx processors)
Sx Bus Mode Interface Pin Description (i960®Sx processor)

Unspecified pins are no connects.

The following abbreviations are used:

I/O	-	Input and Output Pin
I	-	Input Pin Only
O	-	Output Pin Only
TS	-	Tri-state Pin
OC	-	Open Collector Pin
TP	-	Totem Pole Pin
STS	-	Sustained Tri-state Pin, driven high for 1 CLK before float
DTS	-	Driven Tri-state Pin, driven high for 1/2 CLK before float

All local bus inputs (Pin Type I) are internally connected to Vcc through a 10k ohm pull-up resistor.
All Local tristate I/O pins should have pull-ups.

Design Notes: PULL up/down (use 3k - 10kΩ).

For PCI Pins, DO NOT pull up/down any pins unless you are using PCI9060 for an embedded design.
Please refer to “PCI Local Bus Specification”, Revision 2.1, pg123.

Table 60 Power and Ground Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	49	Test Pin. Pull high for test, low for normal operation. When TEST is pulled high, all outputs except USERO (pin 27) are placed in tri-state. USERO provides a NAND-TREE output when TEST is pulled high.
VDD	Power	12	I	1,38,53, 60,68,83, 105,124, 144,157, 167,184	Five volt power supply pins. Liberal .01 uF to .1 uF decoupling capacitors should be placed near the PCI9060.
VSS	Ground	20	I	22,37,45, 52,59,67, 75,82,90, 98,104, 114,123, 134,143, 156,166, 183,193, 208	Ground pins.

Table 61 EEPROM Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
CLKSEL	Clock Select	1	I	170	When set to 0 EE1MC will be used to clock the EEPROM. When set to 1 an internally generated clock will be used to clock the EEPROM. The clock is generated from the PCI Clock.
EE1MC	1 MHz Clock	1	I	175	Optional EEPROM clock source
EECS	EEPROM Chip Select	1	O TP 6 mA	176	EEPROM chip select
EEDI	EEPROM Data IN	1	O TP 6 mA	172	Write data to EEPROM
EEDO	EEPROM Data OUT	1	I	171	Read data from EEPROM
EESK	Serial Data Clock	1	O TP 6 mA	173	EEPROM Clock
SHORT#	Load Short	1	I	174	When active low only five 32-bit registers are loaded from the EEPROM. When active high all local configuration registers are also loaded from EEPROM.

Table 62 PCI System Bus Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS 6mA	32-36, 39-44,46-47, 76-81,84-89, 91-97	These are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The PCI9060 supports both read and write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I/O TS 6mA	70,71,72, 73	These are multiplexed on the same PCI pins. During the address phase of a transaction C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. Refer to PCI spec for further detail if needed.
CLK	Clock	1	I	54	This provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33MHz.
DEVSEL#	Device Select	1	I/O STS 6mA	64	When a device has decoded its address as the target of the current access, the device asserts DEVSEL#. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	Cycle Frame	1	I/O STS 6mA	57	This is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
GNT#	Grant	1	I	51	This indicates to the agent that access to the bus has been granted. Every master has its own REQ# and GNT#.
IDSEL	Initialization Device Select	1	I	63	This is used as a chip select during configuration read and write transactions.
INTA#	Interrupt A	1	O OC 6mA	55	This is used to request an interrupt.
IRDY#	Initiator Ready	1	I/O STS 6mA	61	This indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
LOCK#	Lock	1	I/O STS 6mA	69	Lock indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS 6mA	74	This is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.
PERR#	Parity Error	1	I/O STS 6mA	65	This is only the reporting of data parity errors during all PCI transactions except a Special Cycle.

REQ#	Request	1	O 6mA	50	This indicates to the arbiter that this agent desires use of the bus. Every master has its own GNT# and REQ#.
RST#	Reset	1	I	56	This is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	Systems Error	1	O OC 6mA	66	This is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	I/O STS 6mA	62	This indicates the current target is requesting the master to stop the current transaction.
TRDY#	Target Ready	1	I/O STS 6mA	58	This indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.

Table 63 Local Bus Mode and Processor Independent Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADMODE	Address Decode Mode	1	I	20	Determines how S[2:0] are used to access the PCI9060 internal registers
BREQ	Bus Request	1	I	169	BREQ is asserted to indicate that a local bus master requires the bus. If enabled through the PCI9060 configuration registers, the PCI9060 will release the bus during a DMA transfer if this signal is asserted.
BREQo	Bus Request Out	1	O TP 6 mA	21	BREQo is asserted to indicate that the PCI9060 requires the bus to perform a direct PCI to local bus access while a Direct Master access is pending on the Local bus. It can be used with external logic to generate backoff to a Local bus Master. Its operational parameters are set up through PCI9060 configuration registers.
BTERMo#	Burst Terminate Out	1	O DTS 6mA	28	BTERMo# is asserted along with READYo# to request that a burst be broken up and that a new address cycle be started. (Abort only)
DACK[1:0]#	DMA request outputs	2	O TP 6 mA	25,30	When a channel is programmed through the configuration registers to operate in demand mode, its DACK output indicates a DMA transfer is being executed. DACK0# corresponds to PCI9060 DMA channel 0 and DACK1# to DMA channel 1.
DMPAF#	Direct Master Programmable almost full	1	O TP 6 mA	8	Direct Master write FIFO almost full status output. Programmable through a configuration register.
DP[3:0]	Data Parity	4	I/O TS 6 mA	12,13,14, 15	Parity is even for each of up to 4 byte lanes on the local bus. Parity is checked for writes to the PCI9060 or reads by the PCI9060. Parity is generated for reads from the PCI9060 or writes by the PCI9060.
DREQ[1:0]#	DMA request inputs	2	I	24,29	When a channel is programmed through the configuration registers to operate in demand mode, its DREQ input serves as a DMA request. DREQ0# corresponds to PCI9060 DMA channel 0 and DREQ1# to DMA channel 1.
LDSHOLD	Direct Slave HOLD Request	1	O TP 6mA	165	Asserted coincident with LHOLD to indicate that the PCI9060 is requesting use of the Local Bus in order to perform a Direct Slave transfer.
LINTi#	Local Interrupt In	1	I	151	When asserted low causes a PCI interrupt.
LINTo#	Local Interrupt Out	1	O TP 6 mA	152	The interrupt output is a synchronous level output. The output will remain asserted as long as an interrupt condition exists. If an edge level interrupt is required, disabling and then enabling local interrupts though the interrupt/control status register will create an edge if an interrupt condition still exists or a new interrupt condition occurs.
LRESETi#	Local Reset In	1	I	150	This pin resets the local bus portion of the PCI9060 chip and causes the local reset output to be asserted.

LSERR#	System Error	1	O TP 6mA	23	The LSERR# interrupt output is a synchronous level output. LSERR# interrupt output is asserted when the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register. If an edge level interrupt is required, disabling and then enabling LSERR# interrupts though the interrupt/control status will create an edge if an interrupt condition still exists or a new interrupt condition occurs.
MODE[1:0]	Bus Mode	2	I	9,10	Selects the bus operation mode of the PCI9060: bit 1 bit 0 Bus Mode 0 0 C 0 1 J 1 0 S 1 1 Reserved
NB#	No Local Bus Initialization	1	I	26	Pull up if PCI9060 Local_Init_Done_Bit will be set by local processor. Otherwise, this pin must be 0 in order to work properly. See Note 1. at the bottom.
PCHK#	Data Parity Check	1	O TP 6 mA	16	Parity is checked for writes to the PCI9060 or reads by the PCI9060. Parity is checked for each byte lane with its byte enable asserted. PCHK# is asserted in the clock cycle following the data being checked if a parity error is detected.
S[2:0]	Address Select	3	I	17,18,19	If ADMODE is high, internal PCI9060 registers are selected when A[31:29] match S[2..0]. If ADMODE is low, the internal PCI9060 registers are selected when S0 is asserted low.
USERI	User Input	1	I	31	This is a general purpose input that can be read from the PCI9060 configuration registers.
USERO	User Output	1	O TP 24 mA	27	This is a general purpose output controlled from the PCI9060 configuration registers.
WAITO#	Wait Out	1	O TS 6 mA	149	This output indicates the PCI9060 programmable wait state generator status. WAITO# is asserted when wait states are being caused by the internal wait state generator. It can be thought of as an output providing ready out status.

Note 1:

When pulled down, this pin externally forces Local Init Done bit in the Init Control Register to 1. If NB# is pulled up, the Init Done bit is programmable through local bus configuration accesses. The PCI9060 will issue RETRYs to all PCI accesses until the Local Init Done bit is set. If this bit is not going to be set by a local processor, then NB# must be tied low. Please refer to Section 3.1 on page 10 for further information.

Table 64 Cx Bus Mode Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. ADS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960®Cx processor bursts up to 4 Lwords. If BTERM# is disabled through the PCI9060 configuration registers, the PCI9060 will also burst up to 4 Lwords. If enabled, the PCI9060 will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI9060 programmable wait state generator.
DEN#	Data Enable	1	O TS 24 mA	145	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates that the PCI9060 receives data.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
LLOCK#	Bus Lock	1	I	153	Lock indicates an atomic operation that may require multiple transactions to complete. Used by the PCI9060 for direct local access to the PCI bus.
LA[31:2]	Address Bus	30	I/O TS 6 mA	136,135, 133-125, 122-115, 113-106, 103-101	Address bus carries the upper 30 bits of the physical address bus. During bursts LA3 and LA2 increment to indicate successive data cycles.
LD[31:0]	Data Bus	32	I/O TS 6 mA	177-182, 185-192, 194-207, 2-5	Data bus carries 32,16, or 8 bit data quantities depending on bus width configuration.

LBE[3:0]#	Byte Enables	4	I/O TS 24 mA	139,140, 141,142	The byte enables are encoded based on configured bus width as follows: 32 bit bus: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LD[31:24] BE2# Byte Enable 2 - LD[23-16] BE1# Byte Enable 1 - LD[15-8] BE0# Byte Enable 0 - LD[7-0] 16 bit bus: For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provied BHE#, LA1, and BLE# respectively. BE3# Byte High Enable (BHE#) - LD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#) - LD[7-0] 8 bit bus: For an 8 bit bus BE1# and BE0# are encoded to provide LA1 and LA0 respectively. BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)
LCLK	local Processor clock	1	I	160	Local clock or i960®Cx processor PCLK1 or PCLK2 output
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Cx processor or local bus arbiter asserts LHOLDA when control has been granted.
LHOLDA	Hold Acknowledge	1	I	159	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Cx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI9060 unless requested by LHOLD.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI9060 chip is reset. It is used to drive the RESET# input of the local processor.
READYi#	Ready In	1	I	147	When the PCI9060 is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI9060 programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI9060, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.

Table 65 Jx Mode Bus Interface Pin Description (Also used for Kx processor interface)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 6 mA	161	ALE is asserted during the address phase and deasserted before the data phase.
ADS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. ADS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960®Jx processor bursts up to 4 Lwords. If BTERM# is disabled through the PCI9060 configuration registers, the PCI9060 will also burst up to 4 Lwords. If enabled, the PCI9060 will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI9060 programmable wait state generator.
DEN#	Data Enable	1	I/O TS 24 mA	145	As an input, DEN# must only be asserted during data phases. In i960®Kx systems, DEN# is used internally to block i960®Kx processor assertions of ADS# during data phases of a burst. For non i960®Kx processor systems or systems in which ADS# is not asserted during the data phase, DEN# can be pulled high. As an output, DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates that the PCI9060 receives data.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
LABS[3:2]	Address Bus Burst	2	I/O TS 6 mA	162,163	Carries the word address of the 32 bit memory address. These bits are incremented during a burst access.
LAD[31:0]	Address/Data Bus	32	I/O TS 6 mA	136,135 133-125, 122-115, 113-106, 103-99	During the address phase the bus carries the upper 30 bits of the physical address bus. During the data phase, the bus carries 32 bits of data.

LBE[3:0]#	Byte Enables	4	I/O TS 24 mA	139,140, 141,142	The byte enables are encoded based on configured bus width as follows: 32 bit bus: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LAD[31:24] BE2# Byte Enable 2 - LAD[23-16] BE1# Byte Enable 1 - LAD[15-8] BE0# Byte Enable 0 - LAD[7-0] 16 bit bus: For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provied BHE#, LA1, and BLE# respectively. BE3# Byte High Enable (BHE#) - LAD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#) - LAD[7-0] 8 bit bus: For an 8 bit bus BE1# and BE0# are encoded to provide LA1 and LA0 respectively. BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)
LCLK	System Clock	1	I	160	Local clock or i960®Jx processor clock.
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Jx processor or local bus arbiter asserts LHOLDA when control has been granted.
LHOLDA	Hold Acknowledge	1	I	159	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Jx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI9060 unless requested by LHOLD.
LLOCK#	Bus Lock	1	I	153	Lock indicates an atomic operation that may require multiple transactions to complete. Used by the PCI9060 for direct local access to the PCI bus.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI9060 chip is reset.
READYi#	Ready In	1	I	147	When the PCI9060 is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI9060 programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI9060, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.

Table 66 Sx Mode Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 6 mA	161	ALE is asserted during the address phase and deasserted before the data phase.
AS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. AS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960®Sx processor does not use a BTERM# input. It bursts up to 8 words. If BTERM# is disabled through the PCI9060 configuration registers, the PCI9060 will also burst up to 8 words. If enabled, the PCI9060 will continue to burst until a BTERM# input is asserted. BTERM# breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI9060 programmable wait state generator.
DEN#	Data Enable	1	O TS 24 mA	145	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates that the PCI9060 receives data.
LA[31:16]	Address Bus	16	I/O TS 6 mA	136,135 133-125 122-118	Carries the upper 32 bits of the address.
LABS[3:1]	Address Bus Burst	3	I/O TS 6 mA	162-164	Carries the word address of the 32 bit memory address. These bits are incremented during a burst access.
LAD[15:1],D0	Address/Data Bus	16	I/O TS 6 mA	117-115 113-106 103-99	During the address phase the bus carries the lower physical address bits. During the data phase, the bus carries 16 bits of data.
LBE[1:0]#	Byte Enables	2	I/O TS 24 mA	141,142	Byte enables indicate which of the two bytes are active during a data cycle.
LCLK	System Clock	1	I	160	i960®Sx processor's CLK2 input. The i960®Sx processor's RESET# input must be connected to the PCI9060 LRESETo# output. This enables the PCI9060 to determine the phase of the 2x clock processor.
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Sx processor or local bus arbiter asserts LHOLDA when control has been granted.

LHOLDA	Hold Acknowledge	1	I	159	The PCI9060 asserts LHOLD to request use of the local bus. The i960®Sx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI9060 unless requested by LHOLD.
LLOCK#	Bus Lock	1	I	153	Lock indicates an atomic operation that may require multiple transactions to complete. Used by the PCI9060 for direct local access to the PCI bus.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI9060 chip is reset. Note: this output must be used to drive the Reset Input of the i960®Sx processor. This enables the PCI9060 to determine the phase of the 2x clock processor.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
READYi#	Ready In	1	I	147	When the PCI9060 is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI9060 programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI9060, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.

6. SECTION 6 - ELECTRICAL AND TIMING SPECIFICATIONS

Absolute Maximum Ratings

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS -0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS -0.5V VDD + 0.5V

Operating Ranges

Ambient Temp.	Junc-tion Temp.	Supply Voltage (VDD)	Input Voltage (VIN)
0 °C to +70 °C	115 °C Maximum	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Para-meter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -4.0 mA	2.4		V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Tables		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD VDD = Max		-10	+10	µA
IOZ	Tri-state Output Leakage Current	VDD = Max VSS ≤ VIN ≤ VDD		-10	+10	µA
ICC	Power Supply Current	VDD=5.25V, PCLK=LCLK=33Mhz			130	mA

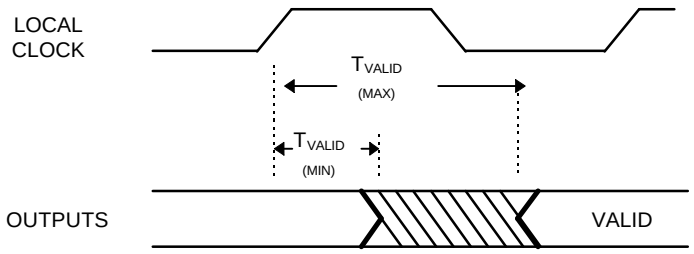


Figure 9. PCI9060 Local Output Delay

AC Electrical Characteristics (Local Outputs) Measured Over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, VCC = 5.0 ± 5%	T_{VALID} (MIN) NSEC (HOLD)	T_{VALID} (MAX) NSEC (WORST CASE)
LHOLD	5	17
LDSHOLD	5	16
ADS#	6	13
BLAST# *(see note below)	8	16
LBE[3:0]#	8	16
LW/R#	6	17
LD[31:0]	9	20
LA[31:0]	8	20
DT/R#	6	17
DEN#	5	13
READYO#	5	14
DP[3:0]	12	20
LRESETO#	5	17
LAD[31:0] (Jx,Sx Mode)	9	20
LABS[3:1] (Jx,Sx Mode)	8	20
BTERMo#	8	19
BREQo	5	21
LINTO	5	16
LSERR#	9	16
PCHK#	6	20
USERO	5	21
WAITO	6	14
DACK[1:0]#	6	20
DMPAF#	5	17
LALE (Jx,Sx Mode) (address setup and hold relative to LALE negative edge)	5	---

Specification Changes

Direct Slave Write BLAST# Tvalid: If the PCI 9060 is performing a Direct Slave burst write to the local bus, write cycles in which not all byte enables are asserted are broken into single address and data cycles. In this case, the Tvalid time to the BLAST# signal preceding the single cycle (BLAST# prior to the new ADS#) can be as much as 25 ns

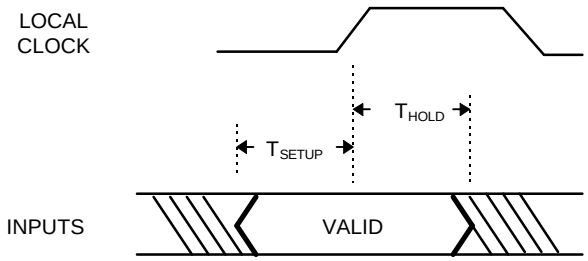


Figure 10. PCI9060 Local Input Setup and Hold Waveform

AC Electrical Characteristics (Local Inputs) Measured Over Operating Range

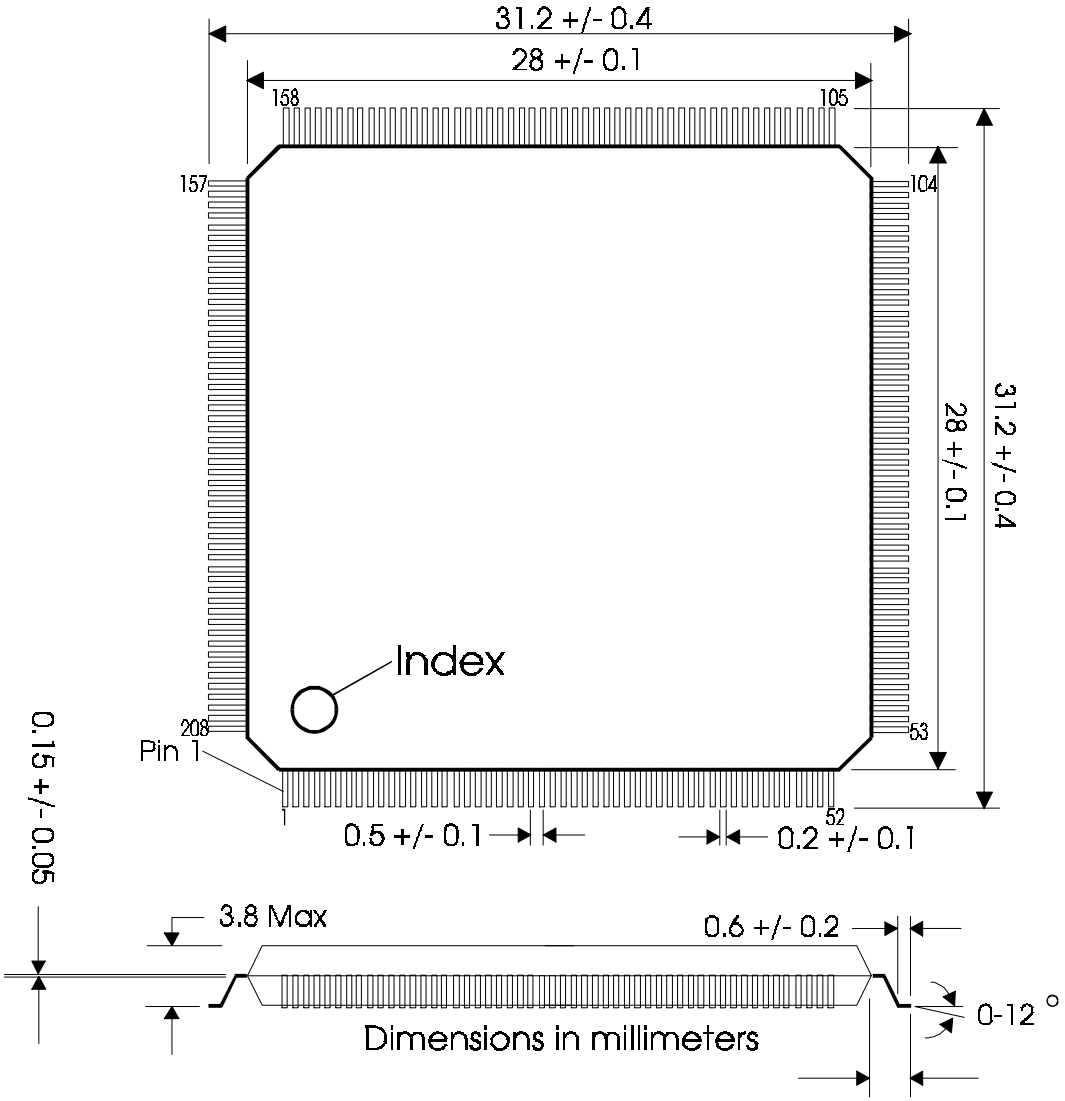
Signals (Synchronous Inputs) C_L = 50 pF, VCC = 5.0 ± 5%	T_{SETUP} (nsec)	T_{HOLD} (nsec) (worst case)
LHOLDA	5	1
ADS#	9	1
BLAST#	6	1
LD[31:0]	7	1
LAD[31:0]	3	-
DP[3:0]	4	1
BTERM#	5	1
DREQ[1:0]#	6	1
READYi#	9	1

	Min	Max
Local Clock Input Frequency	0	40 MHz
PCI Clock Input Frequency	0	33 MHz

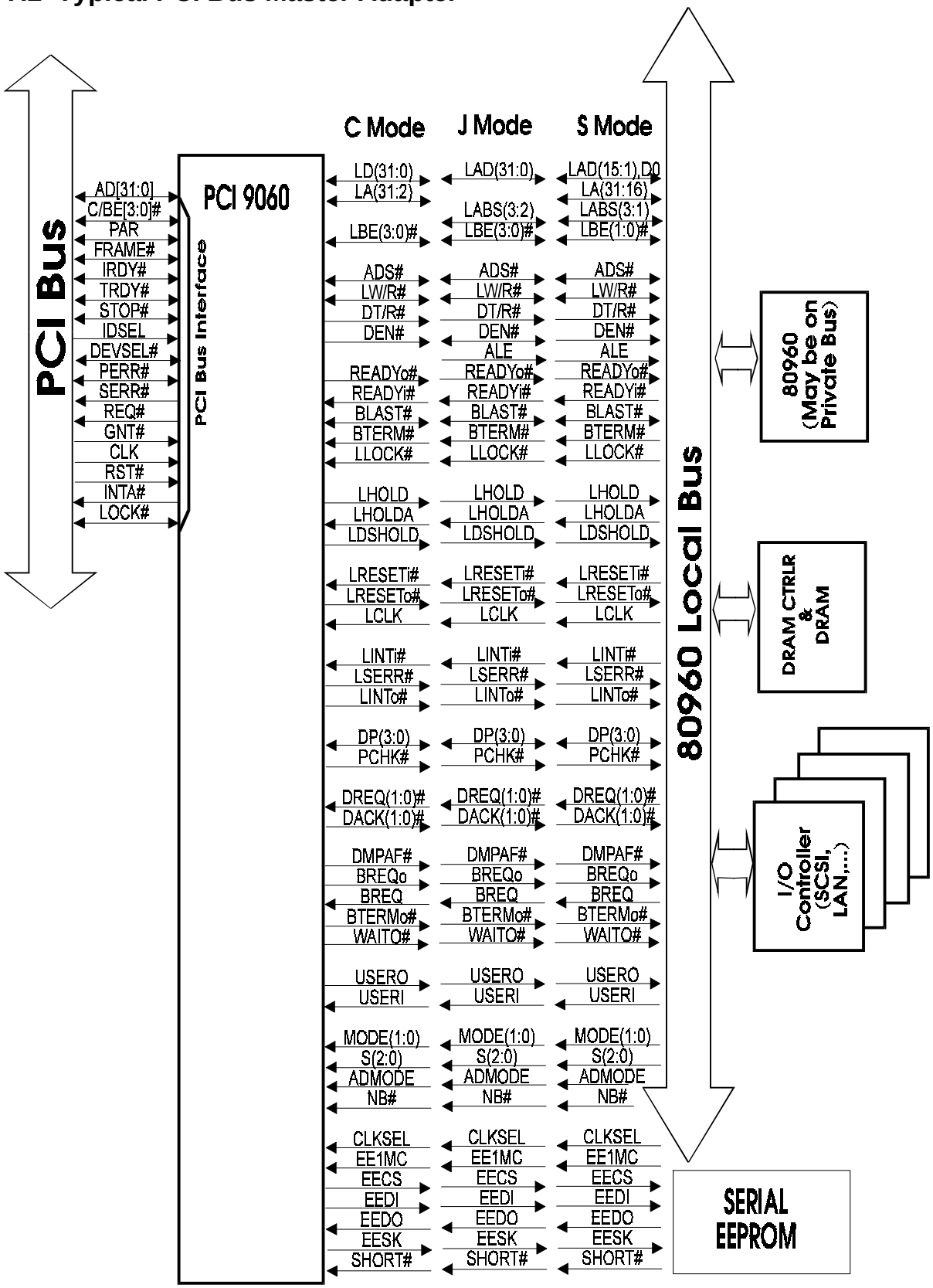
7. SECTION 7 - PACKAGE MECHANICAL DIMENSIONS

7.1 Package Mechanical Dimensions

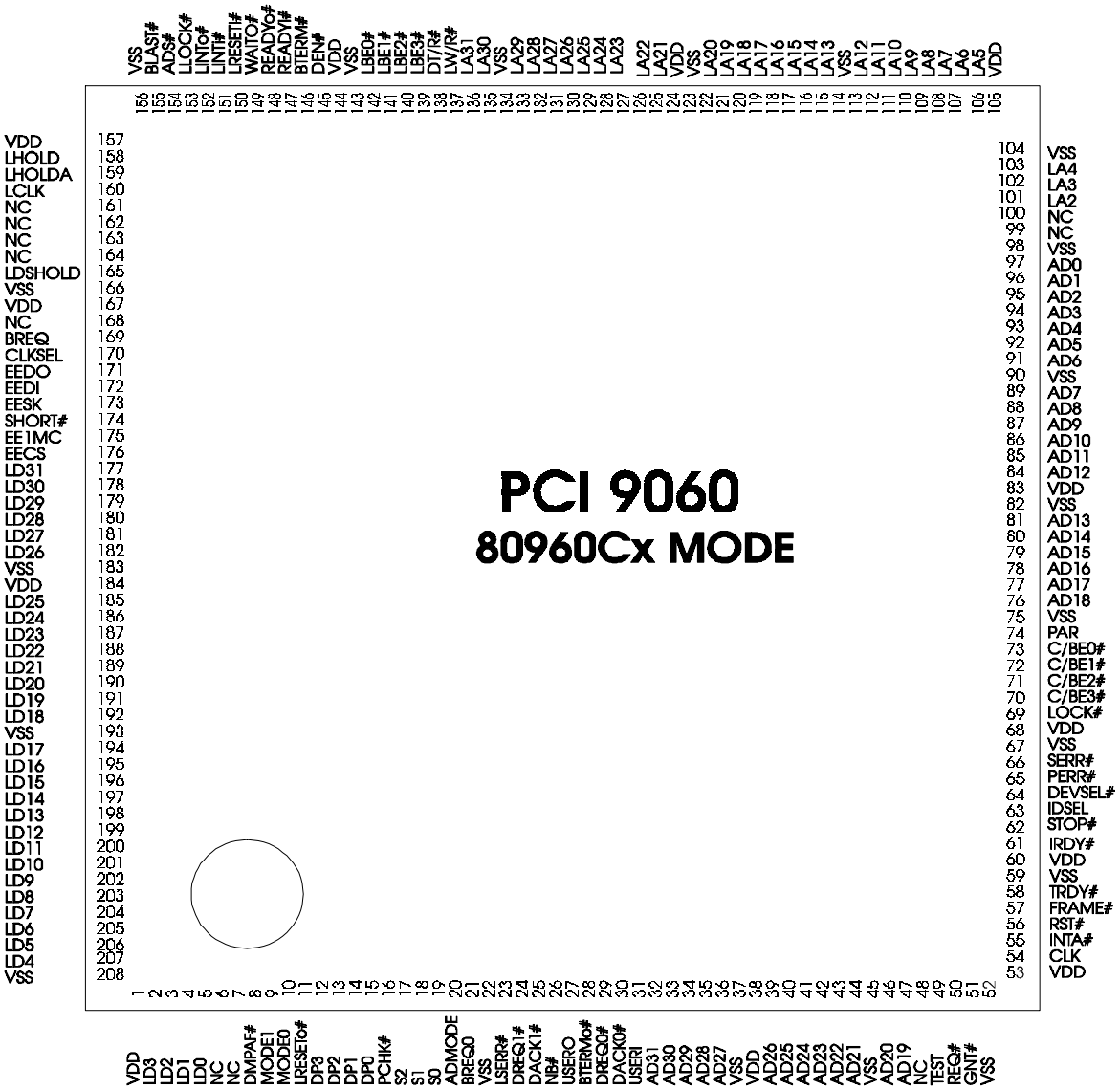
For 208 PQFP, θJC = 5°C/Watt



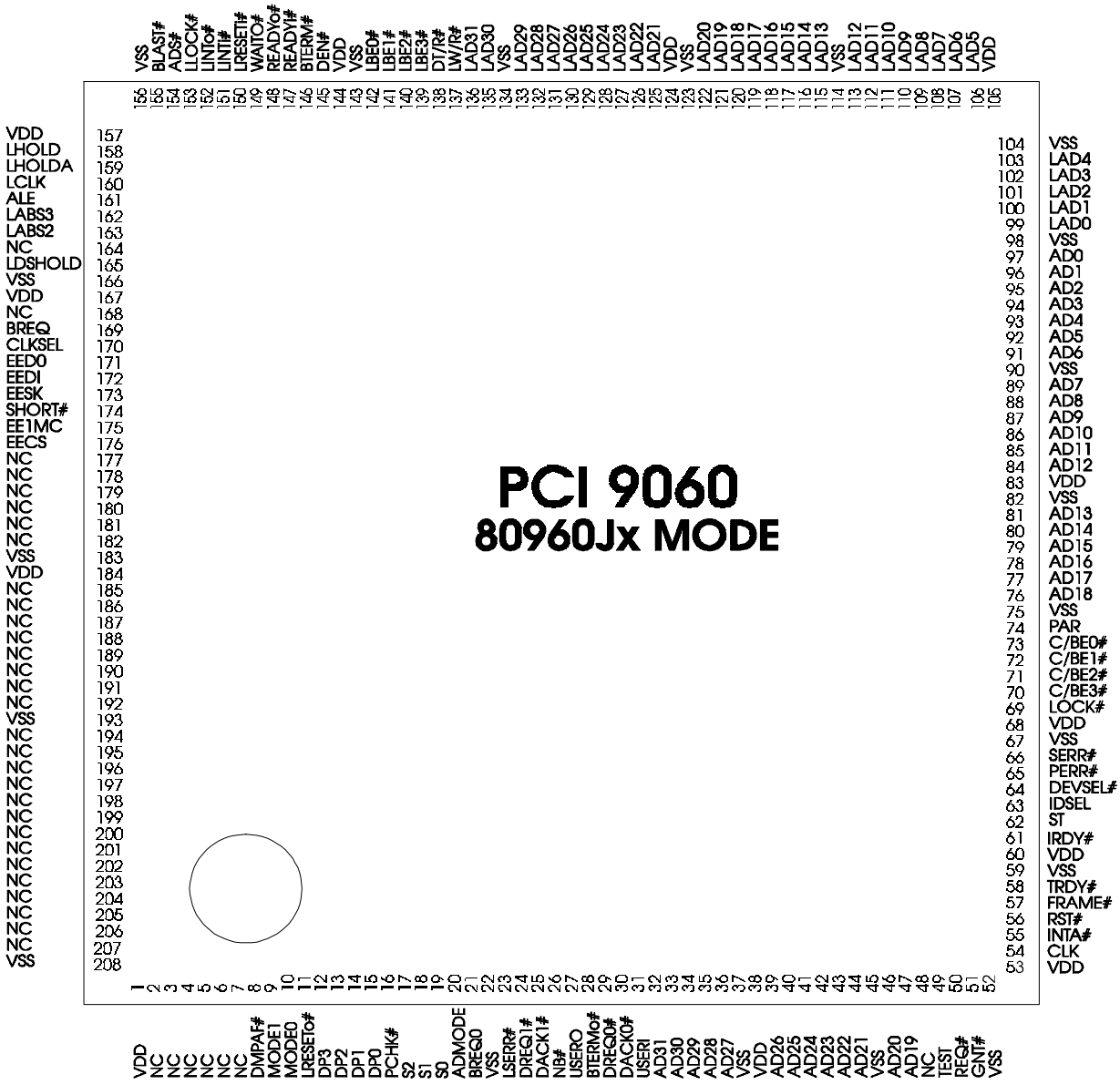
7.2 Typical PCI Bus Master Adapter



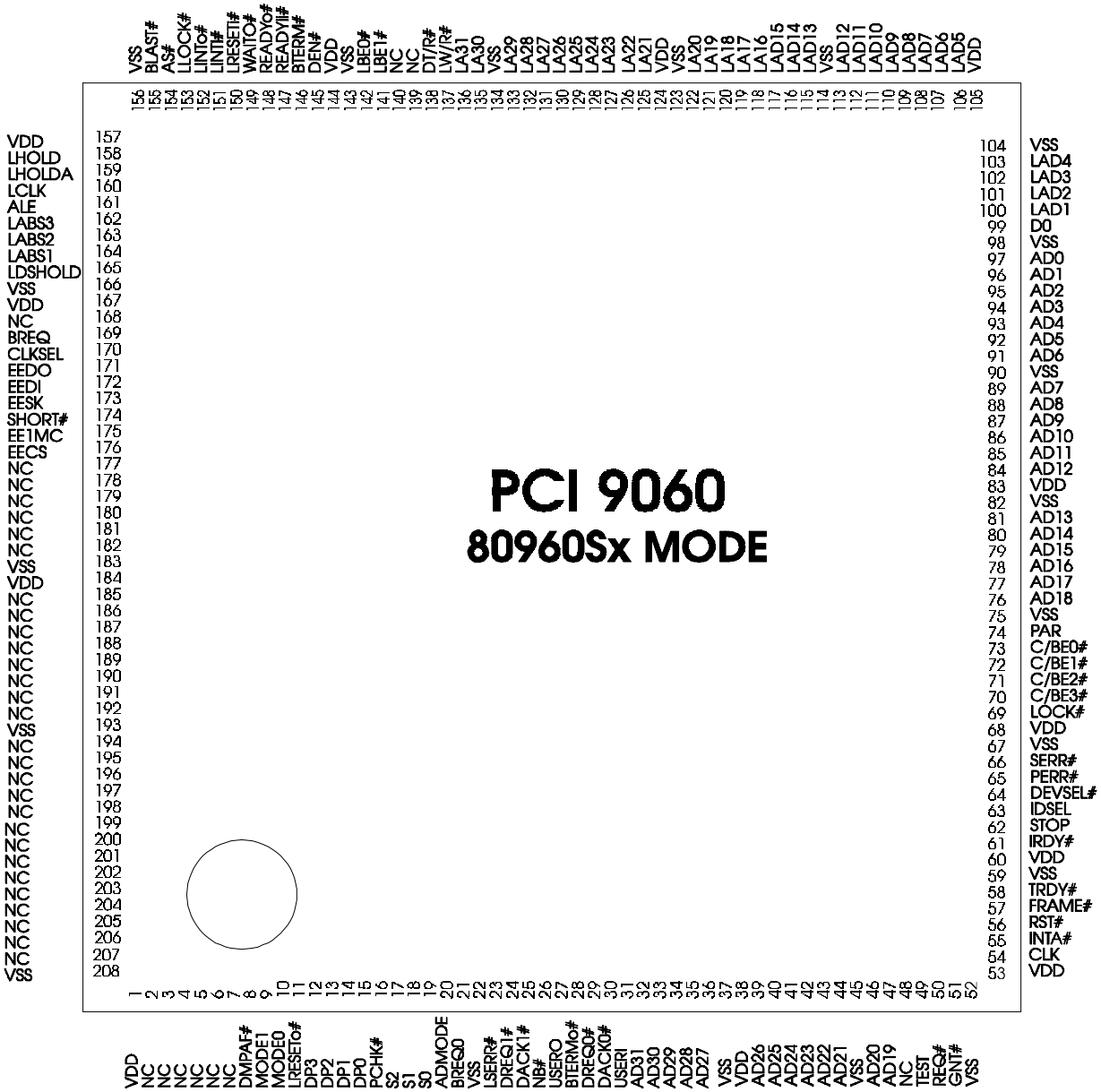
7.3 I960Cx® MODE PIN OUT



7.4 I960Jx® MODE PIN OUT



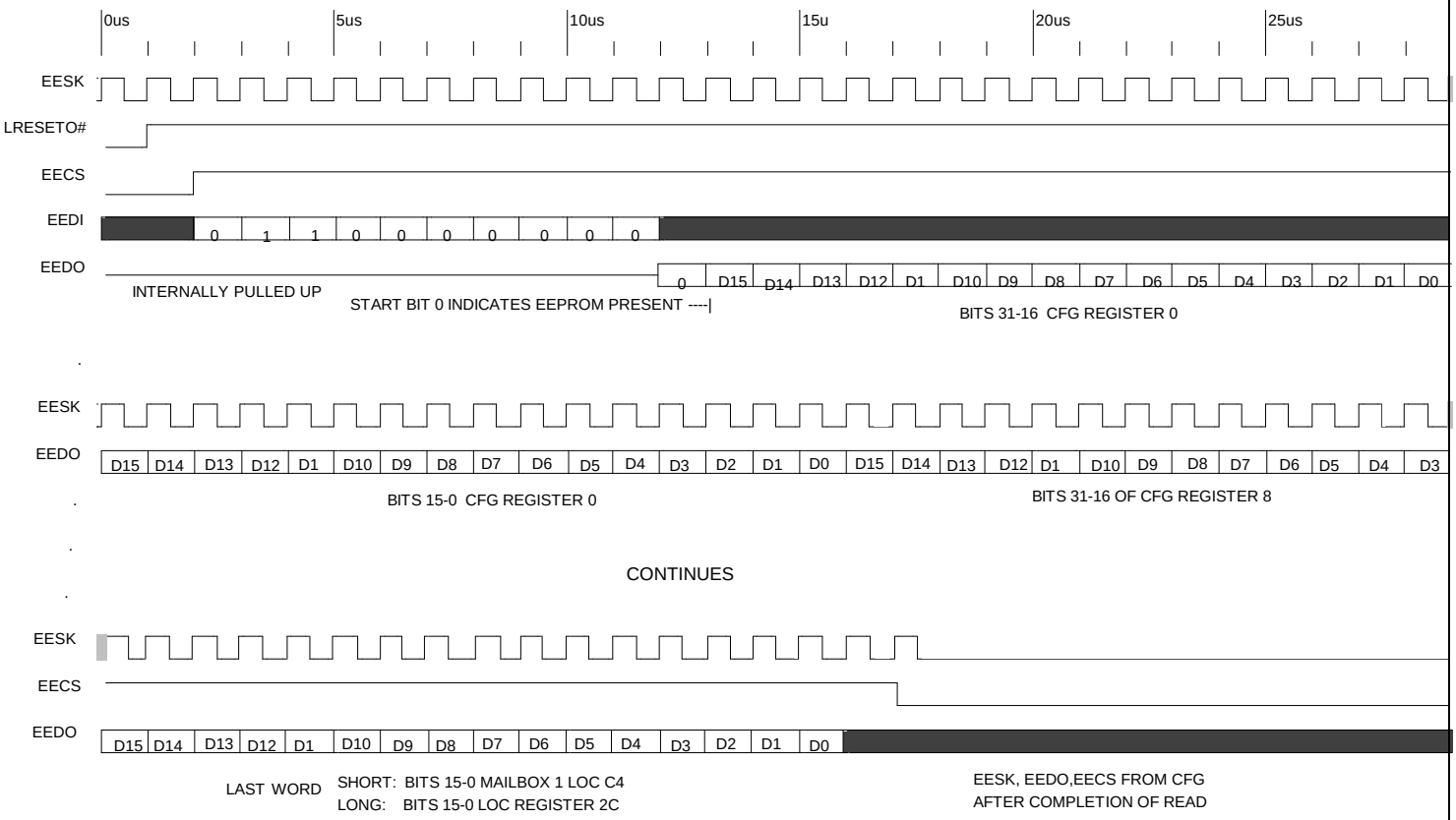
7.5 I960Sx® MODE PIN OUT



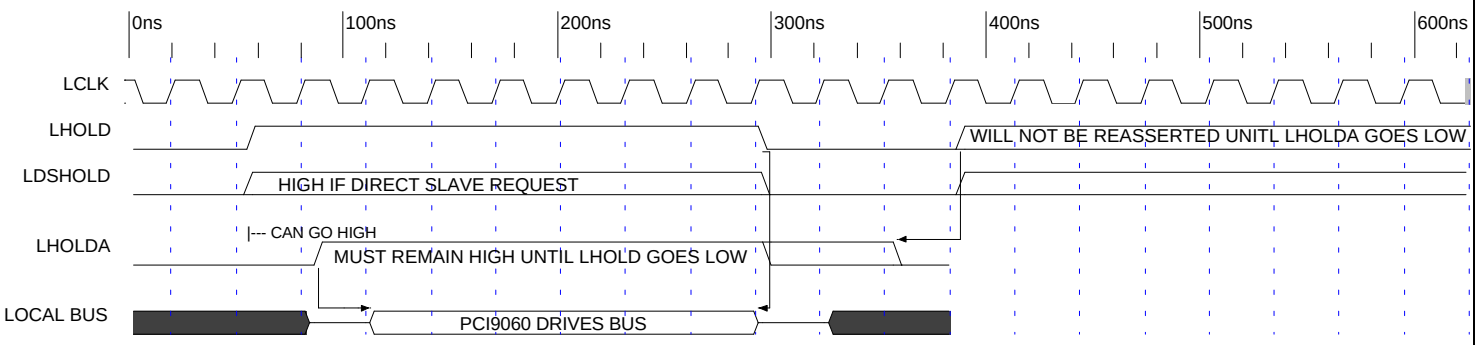
8. SECTION 8- TIMING DIAGRAMS

The PCI9060 operates in three modes, selected through mode pins, corresponding to three processor types; Cx, Jx and Sx. Timing Diagrams are provided for the three operating modes. For some functions, a timing diagram may only be provided for one mode of operation. Even though a different mode is used, that timing diagram can be used to determine functionality.

8.1 List of Timing Diagrams

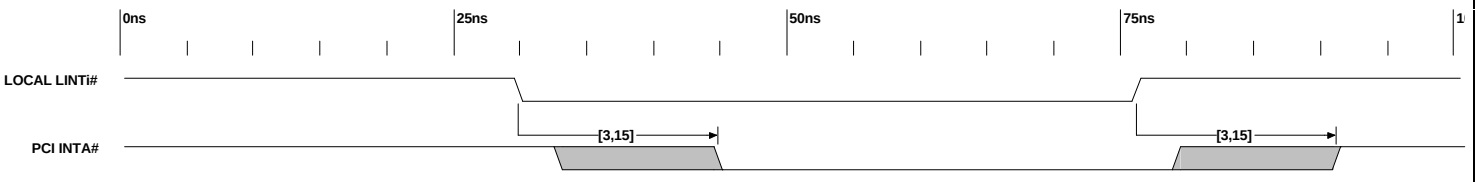


Timing Diagram 1. Initialization from Serial EEPROM

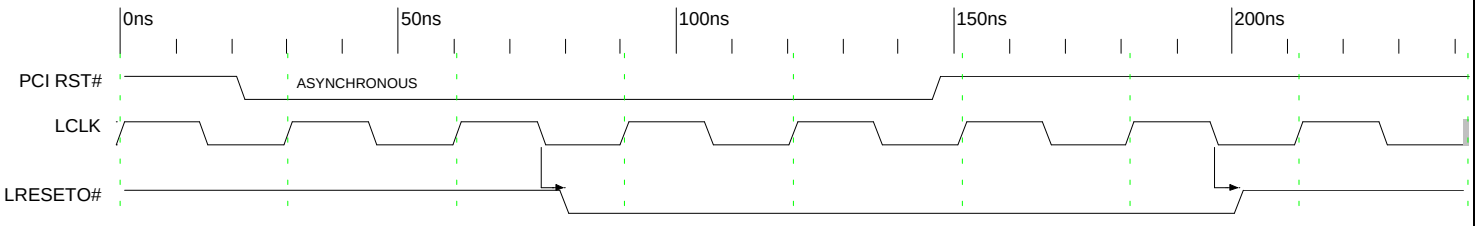


PCI9060 always gives up bus between different local bus accesses:
different direct slave access, different DMA access, between direct slave/DMA accesses

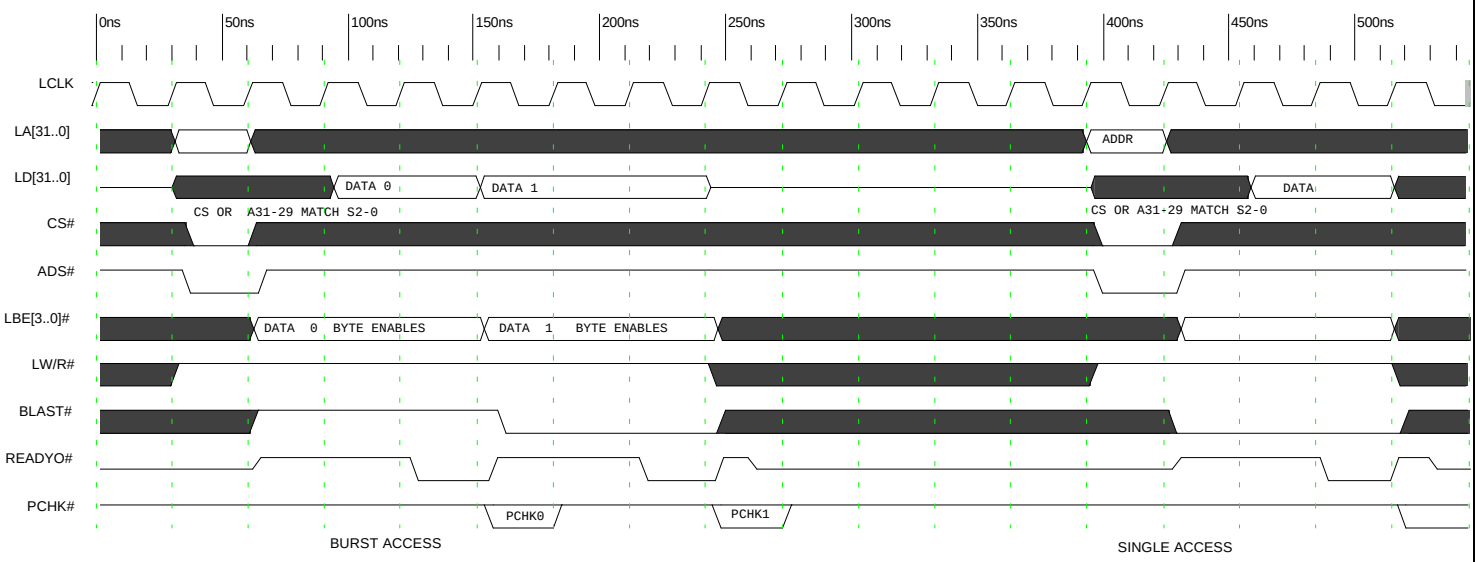
Timing Diagram 2. PCI9060 Local bus Arbitration



Timing Diagram 3. Local LINTi# Input Asserting PCI Output INTA#

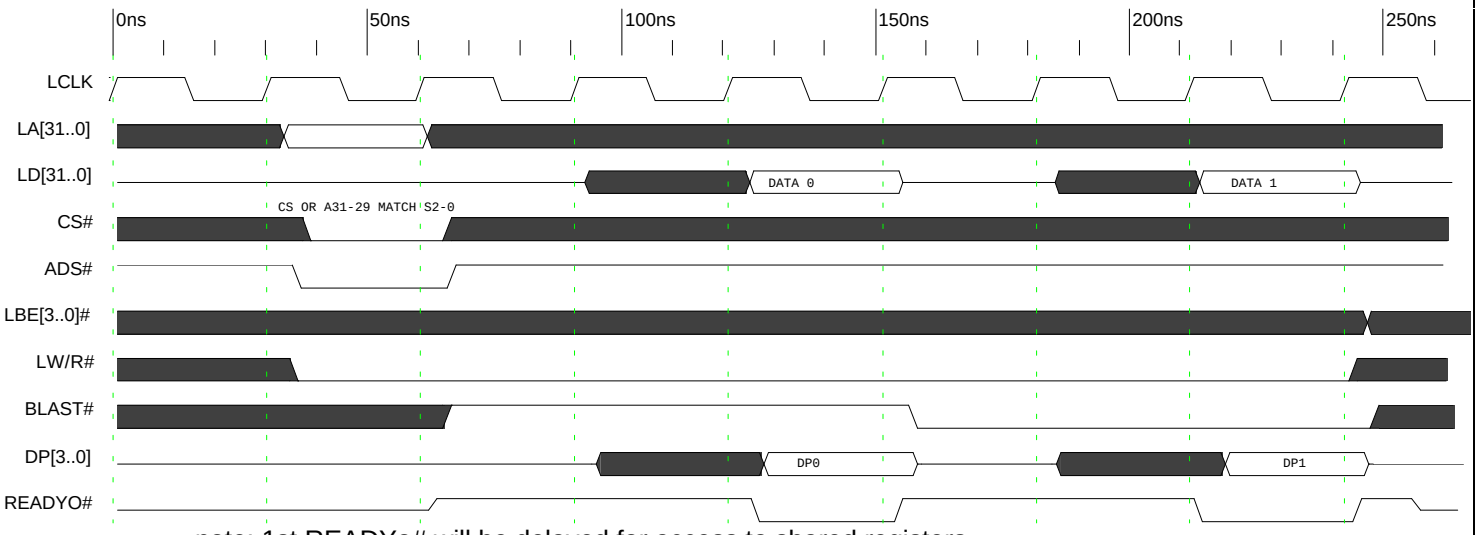


Timing Diagram 4. (CX,JX Mode) PCI RST# Asserting Local Output LRESETO#



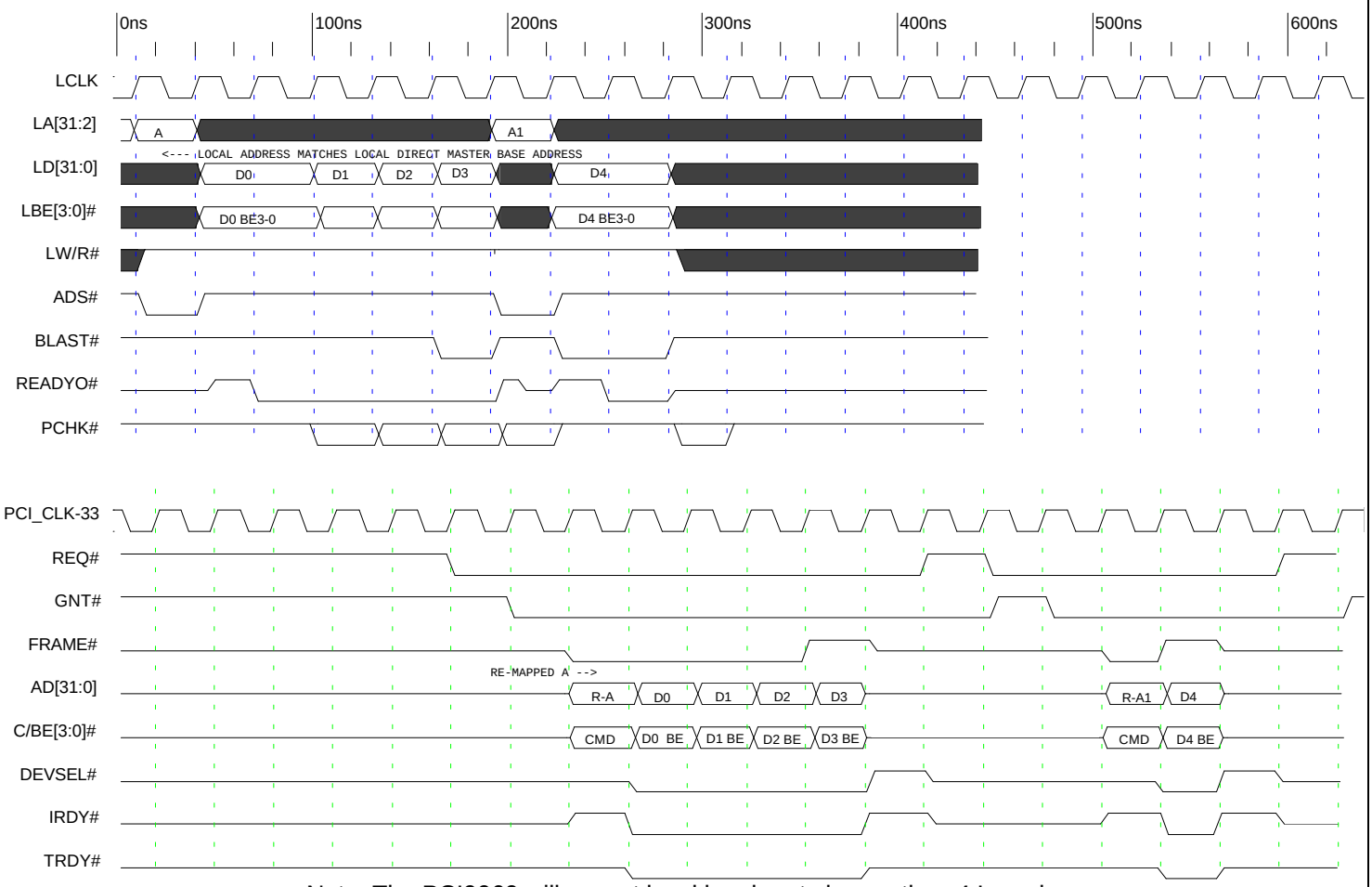
note: 1st READYo# will be delayed for access to shared registers

Timing Diagram 5. (CX Mode) Local Bus Write to PCI9060 Configuration Register



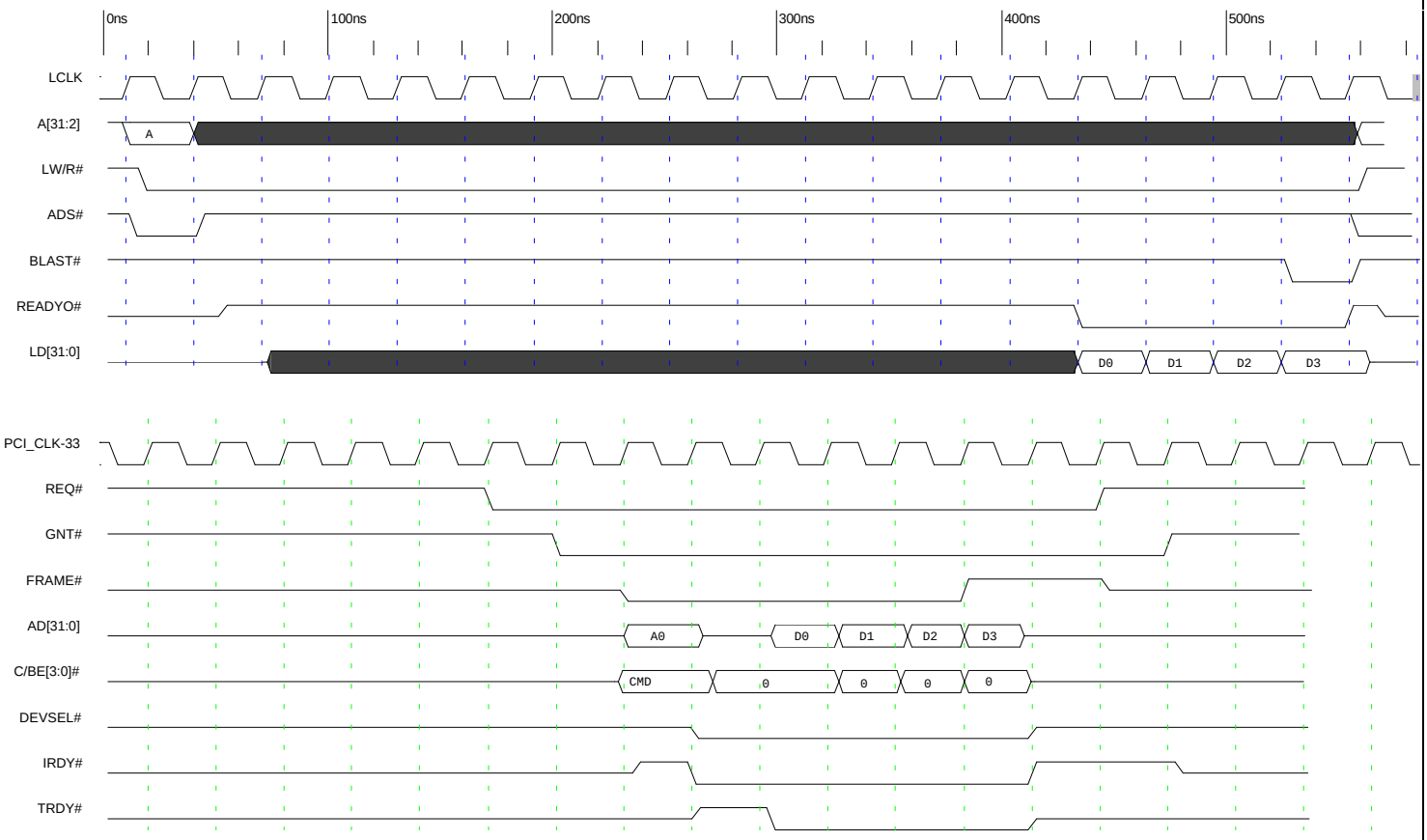
note: 1st READYo# will be delayed for access to shared registers

Timing Diagram 6. (CX Mode) Local Bus Read from PCI9060 Configuration Register



Note: The PCI9060 will accept local bus bursts longer than 4 Lwords

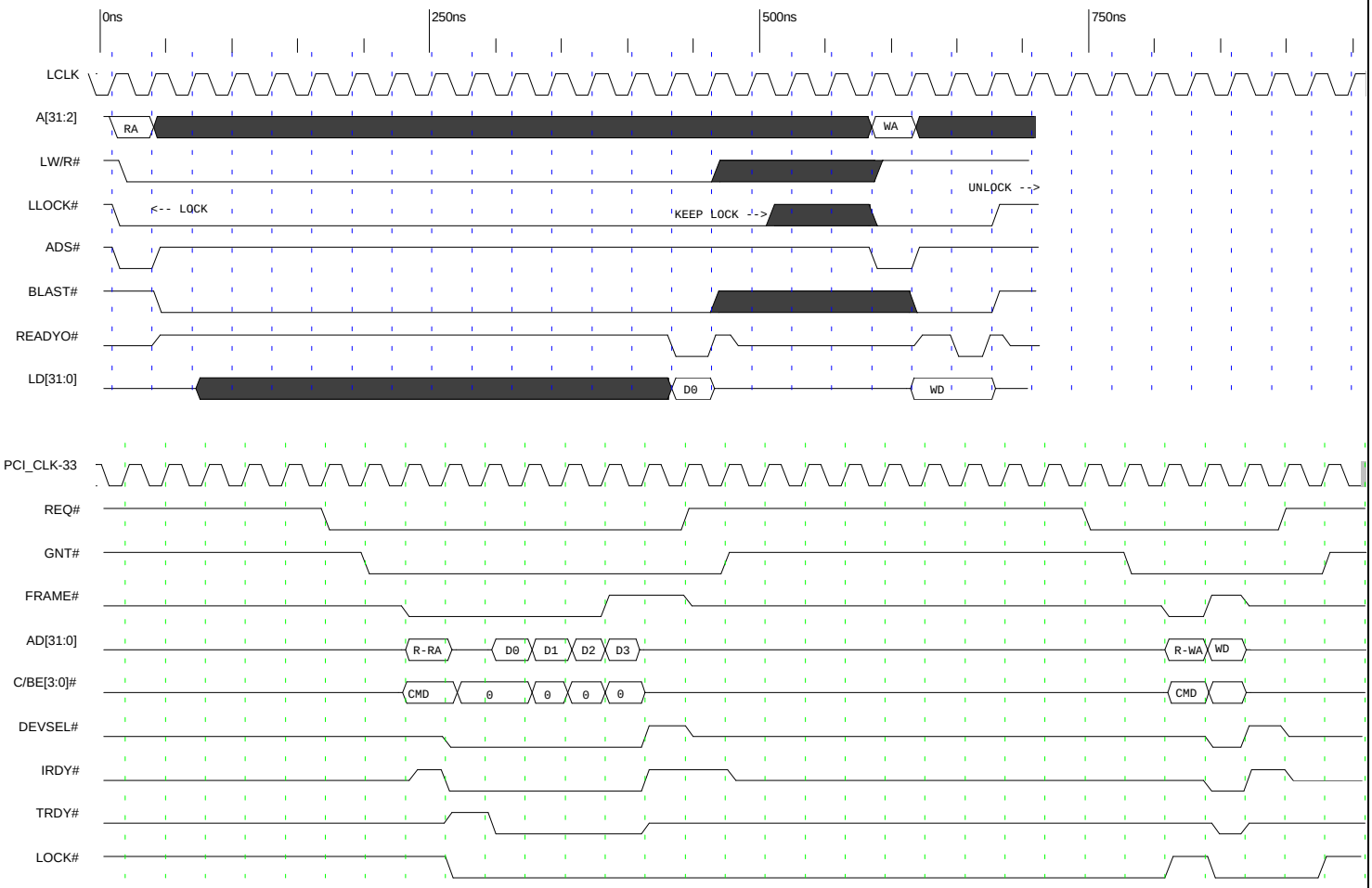
Timing Diagram 7. (CX Mode) Local Bus Direct Master Memory Write Cycles to PCI Bus



(PCI preread 4 mode)

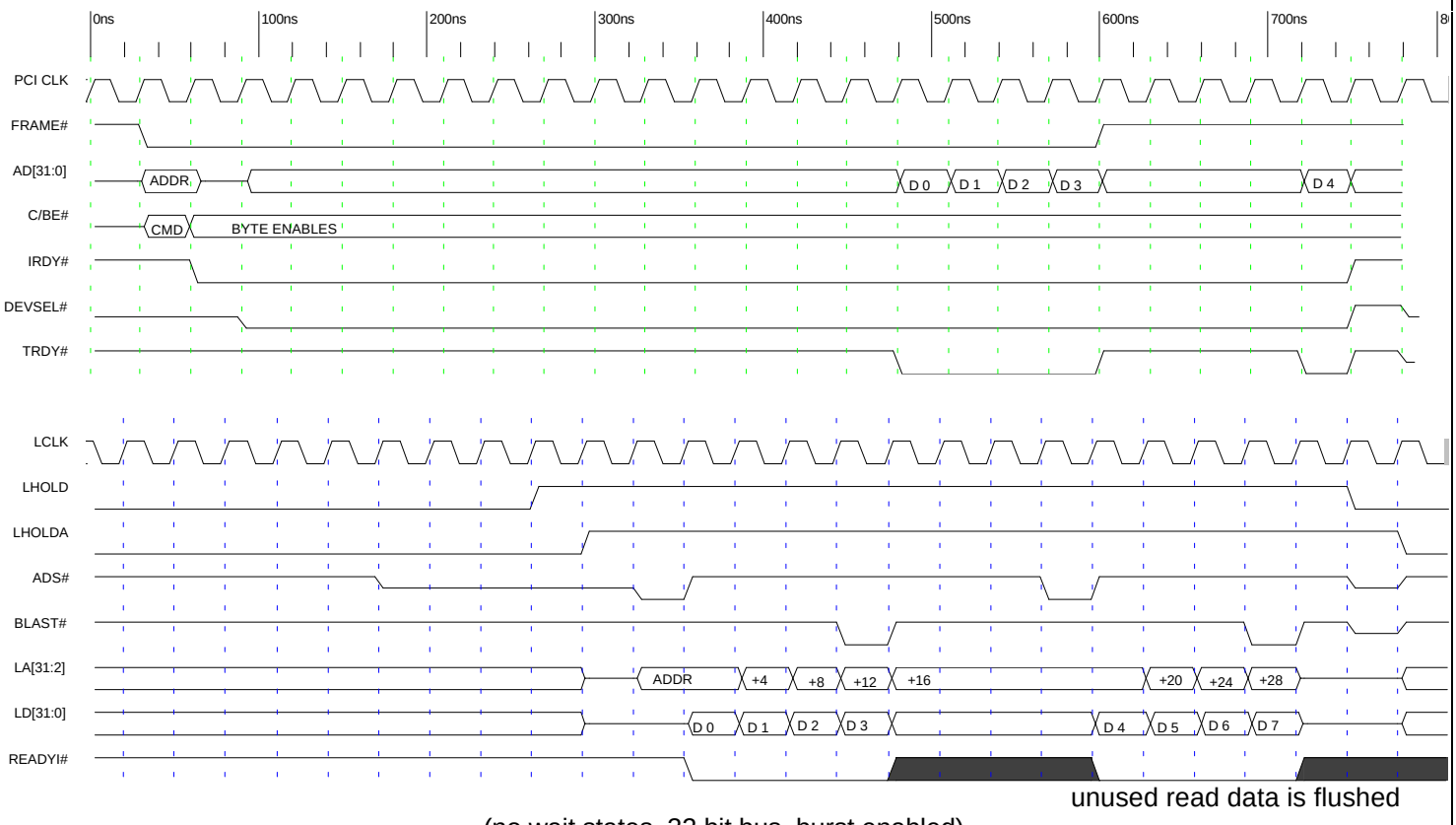
Note: Unused read data is flushed in cases in which more read data is prefetched than used

Timing Diagram 8. (CX Mode) Local Bus Direct Master Memory Read from PCI Bus



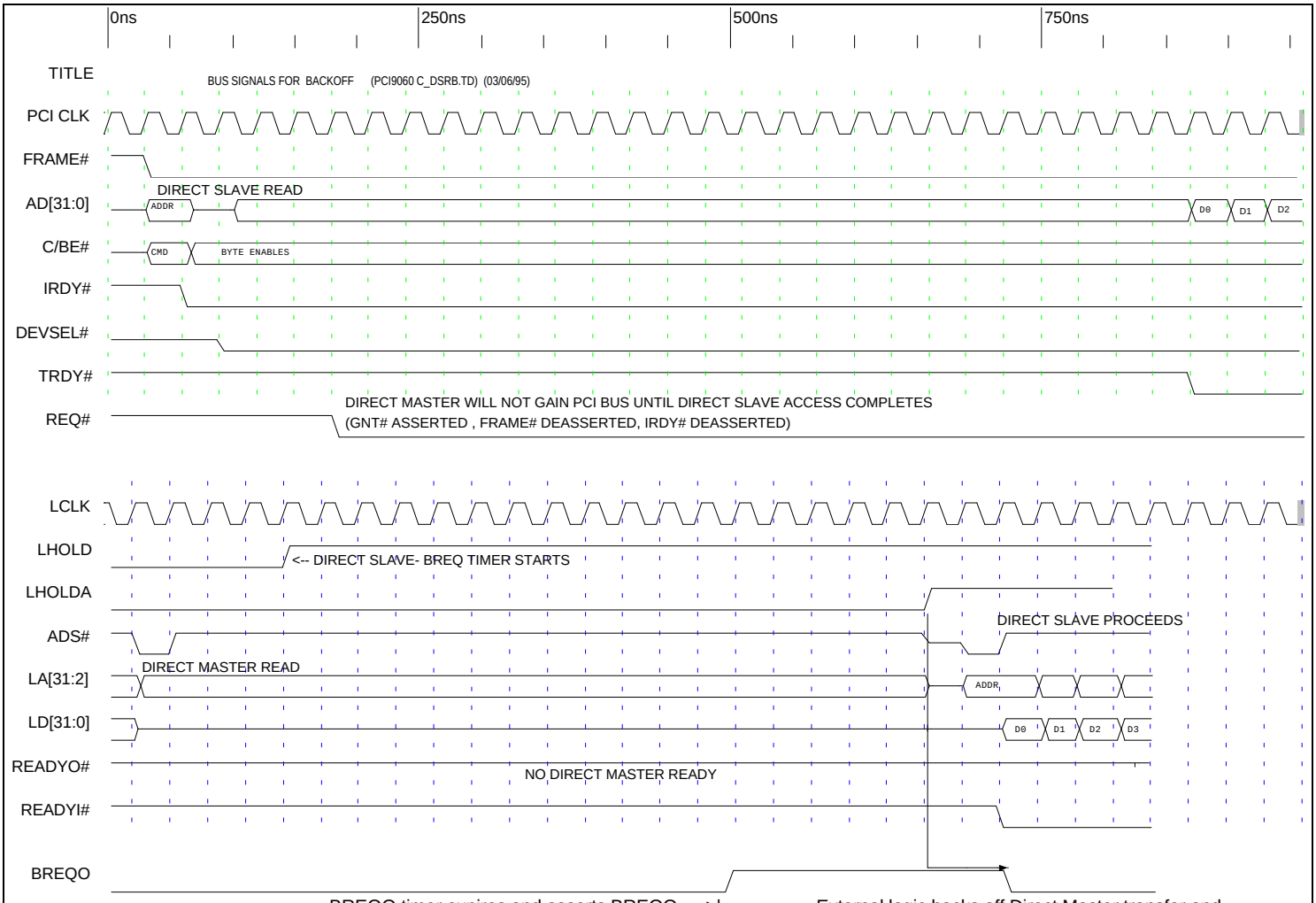
(1 Lword burst read, PCI preread 4 mode)

Timing Diagram 9. (CX Mode) Local Bus Direct Master Locked Read Followed by Write and Release

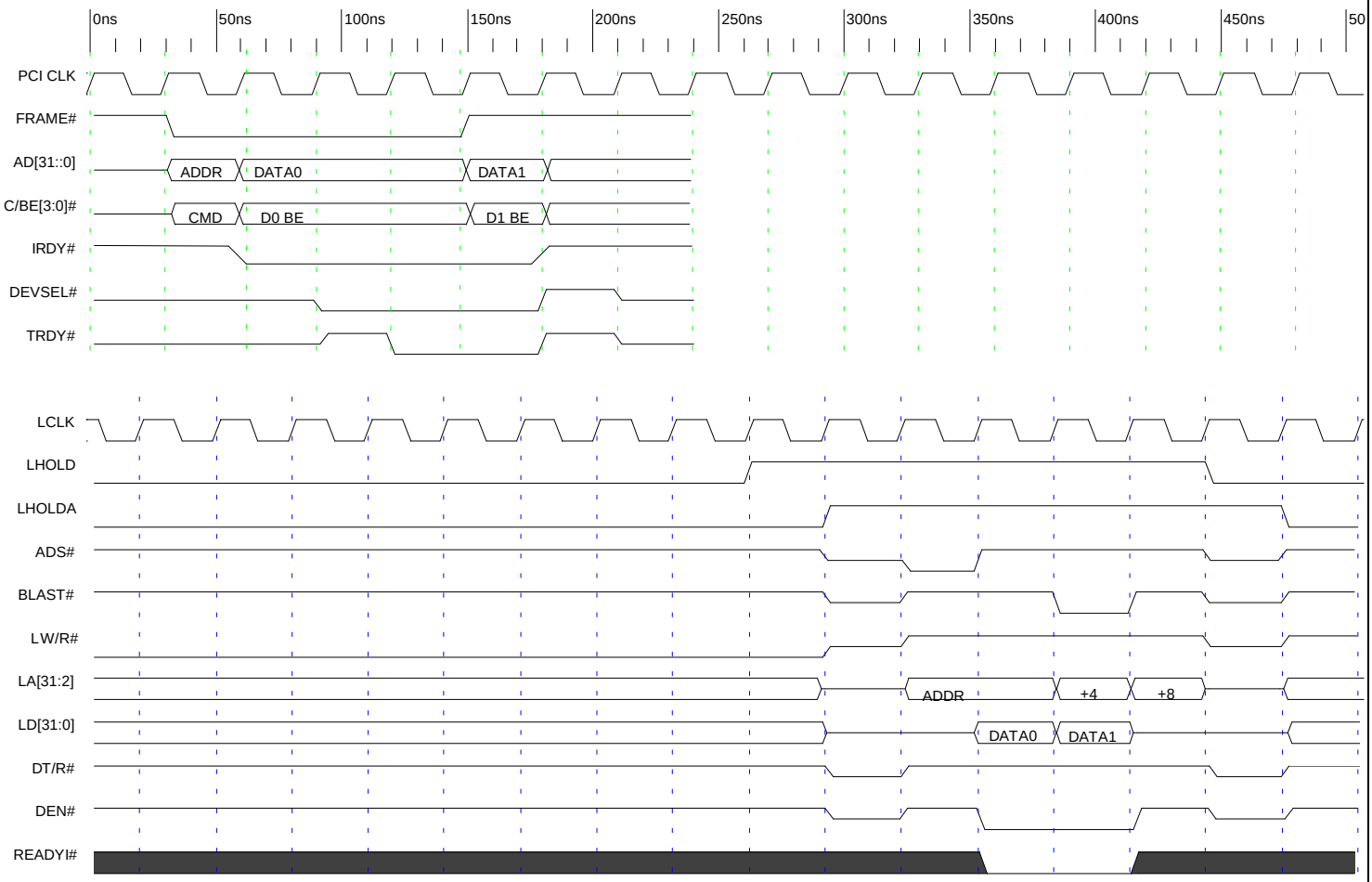


(no wait states, 32 bit bus, burst enabled)

Timing Diagram 10. (CX Mode) Direct Slave PCI to Local burst Read of 5

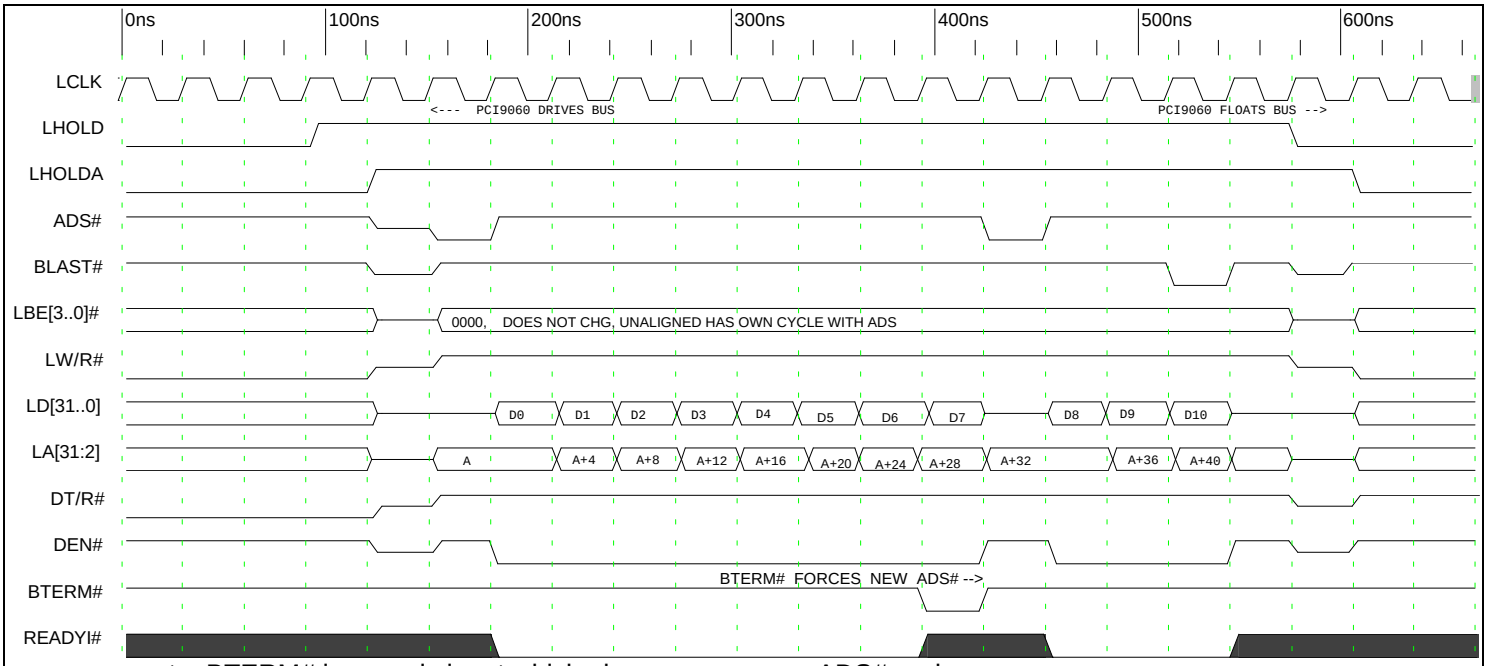


Timing Diagram 11. (CX Mode) BREQO & Deadlock



(no wait states, 32 bit bus, burst enabled)

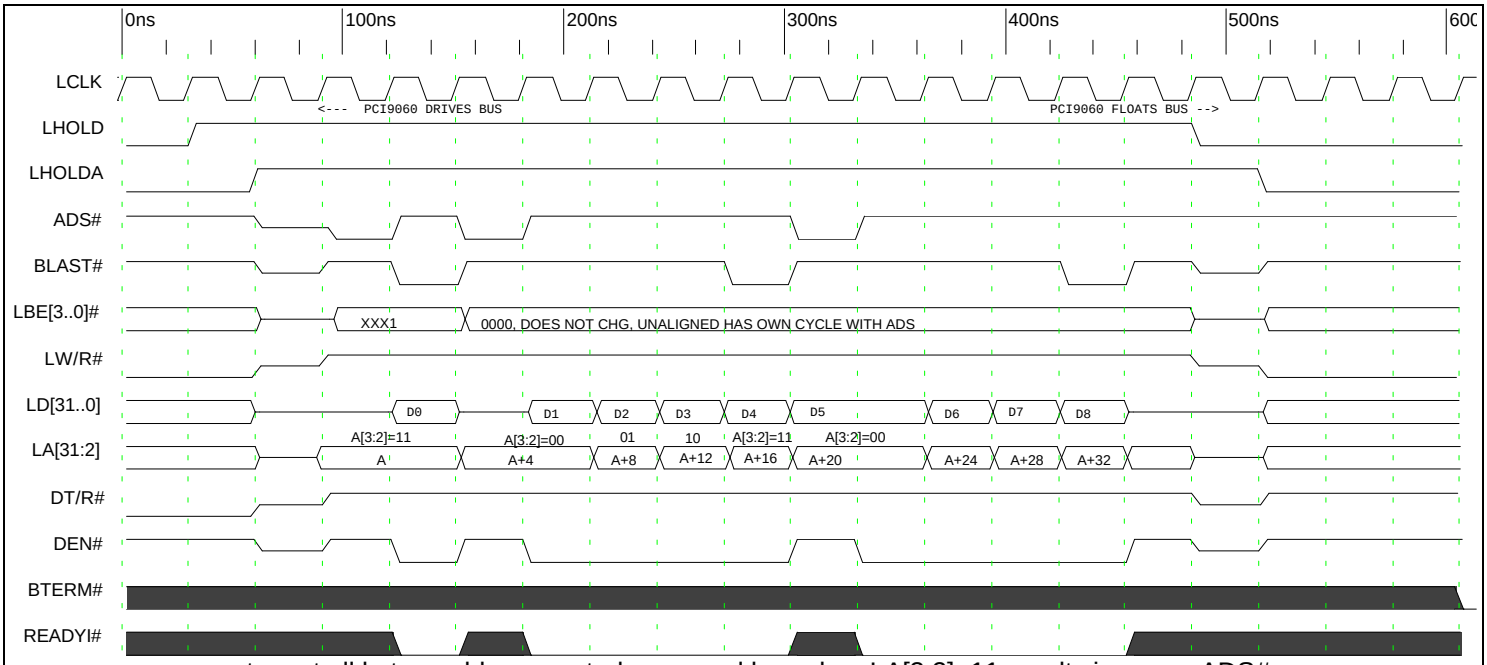
Timing Diagram 12. (CX Mode) Direct Slave PCI to Local burst write



note: BTERM# is a ready input which also causes a new ADS# cycle
note: not all byte enables asserted will cause a new ADS# cycle

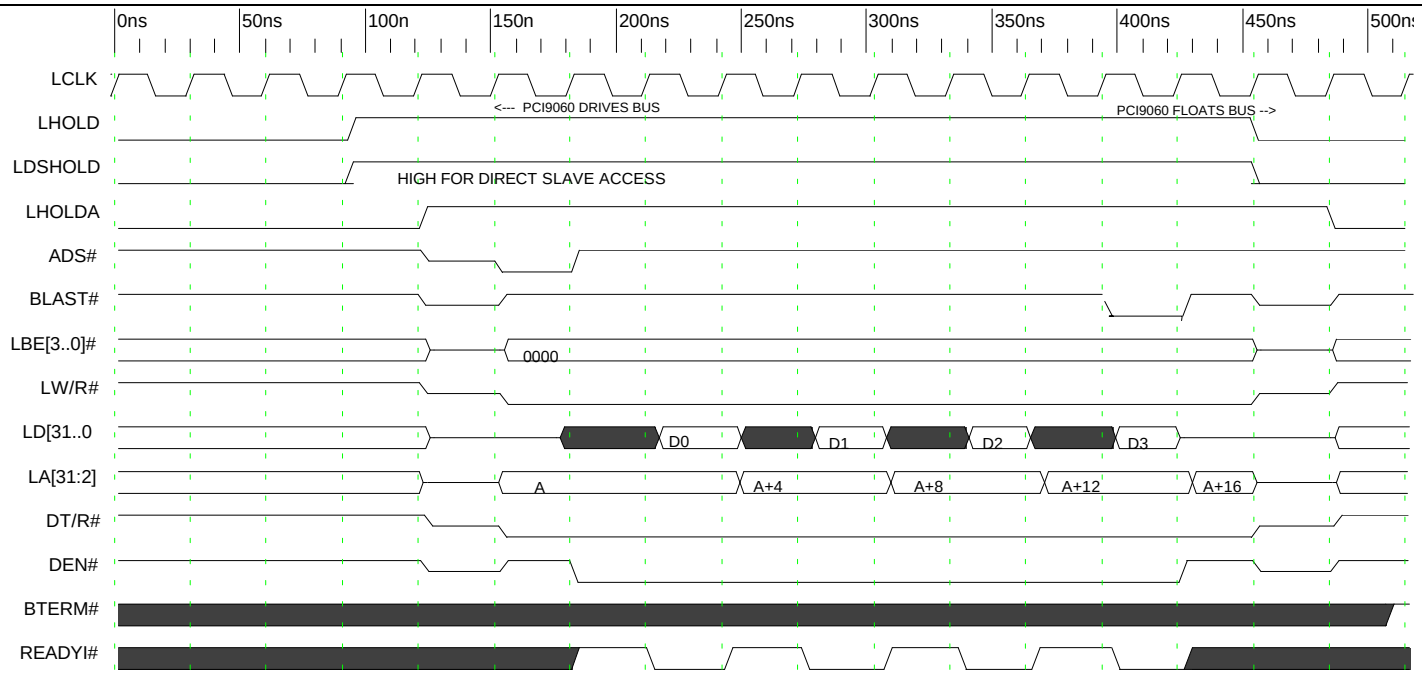
(no wait states, 32 bit bus,burst enabled, BTERM enabled)

Timing Diagram 13. (CX Mode) PCI9060 DMA or Direct Slave Burst Write, Bterm Enabled



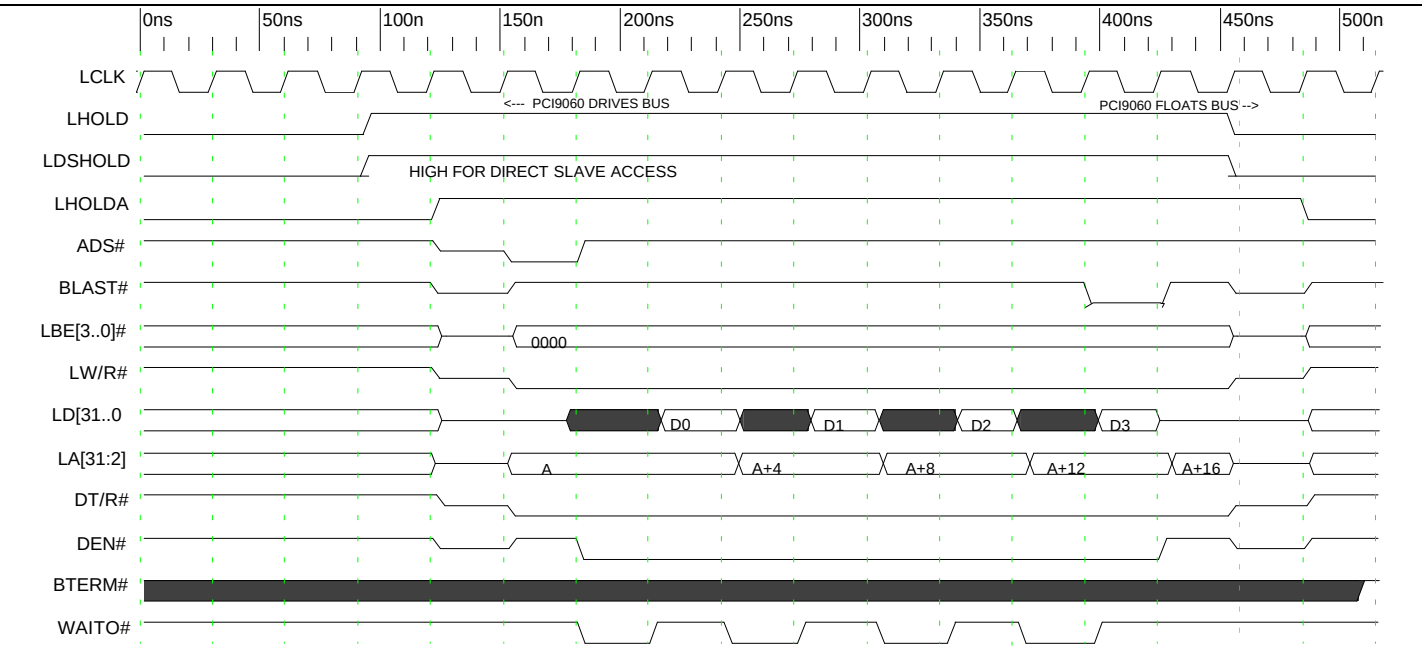
note: not all byte enables asserted or a quad boundary LA[3:2]=11 results in a new ADS#
(no wait states, 32 bit bus,burst enabled,bterm disabled)

Timing Diagram 14. (CX Mode) PCI9060 DMA or Direct Slave Burst Write, Bterm Disabled



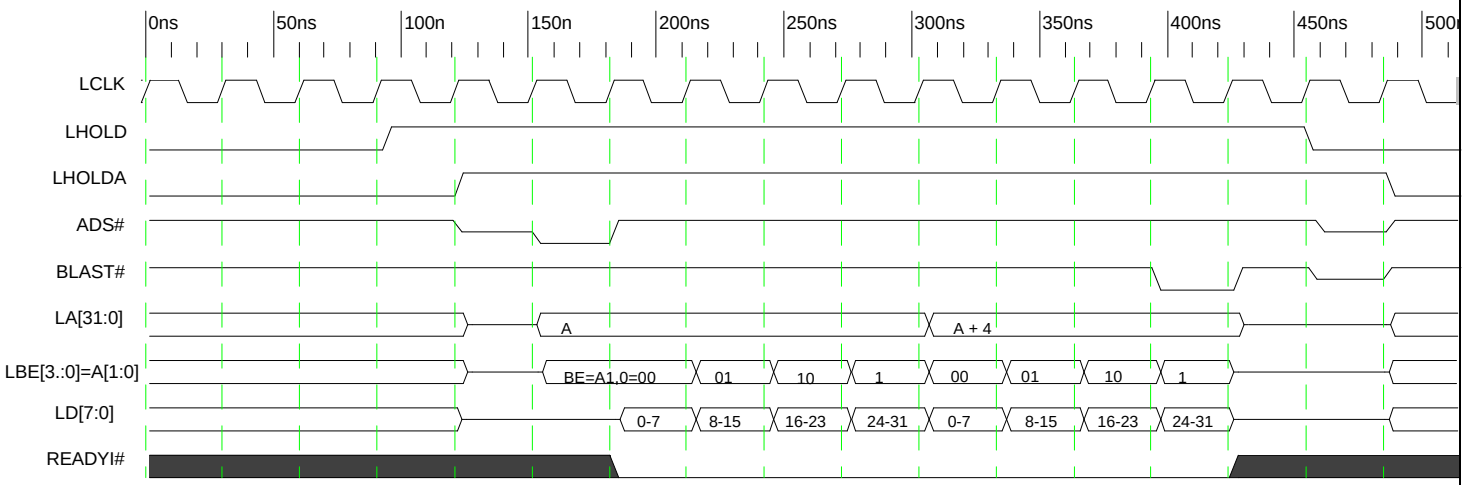
(32 Bit Local Bus, burst enabled, Bterm Disabled)

Timing Diagram 15. (CX Mode) Direct Slave or DMA Burst Read from Local Bus (1 Wait State)



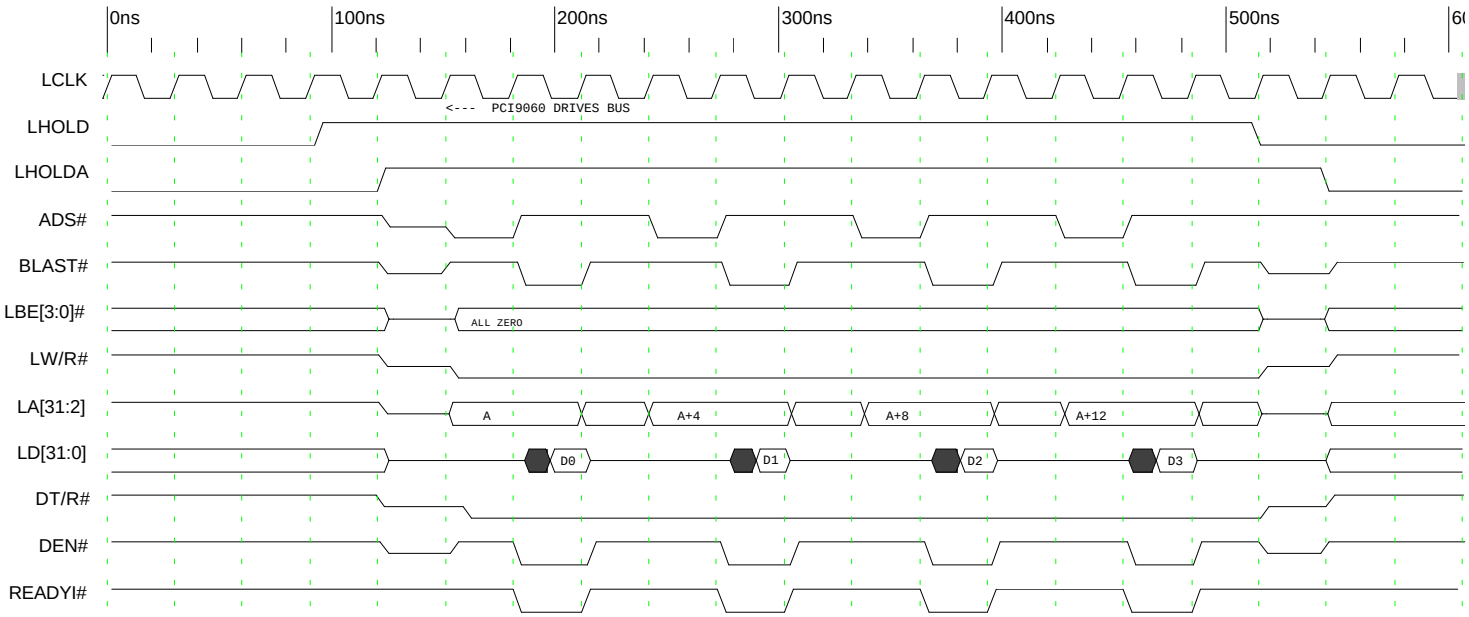
If ready input is enabled in bus region register, additional wait states can be asserted externally
(32 Bit Local Bus, burst enabled, Bterm Disabled)

Timing Diagram 16. (CX Mode) Burst Read from Local Bus (1 Wait State Programmed)



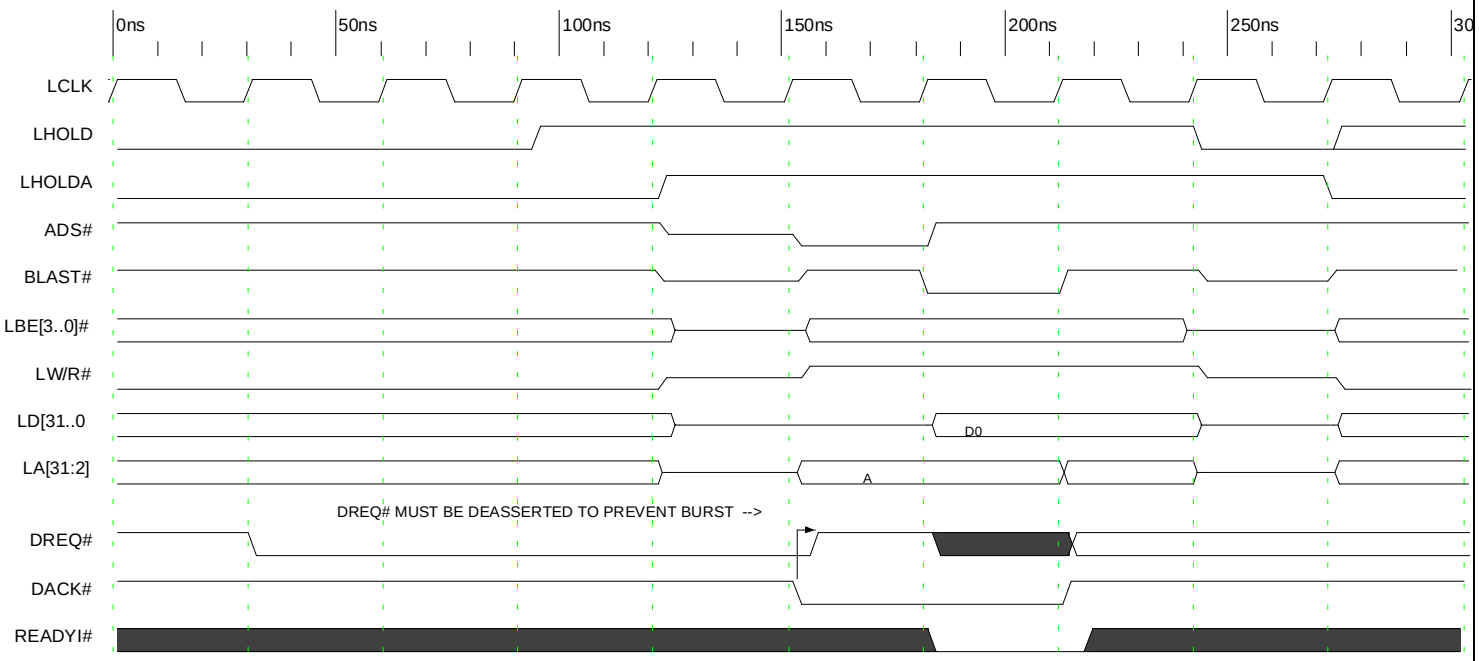
(no wait states, 8 bit bus,burst enabled)

Timing Diagram 17. (CX Mode) DMA or Direct Slave 2 Lword Burst Write to 8 Bit Local Bus



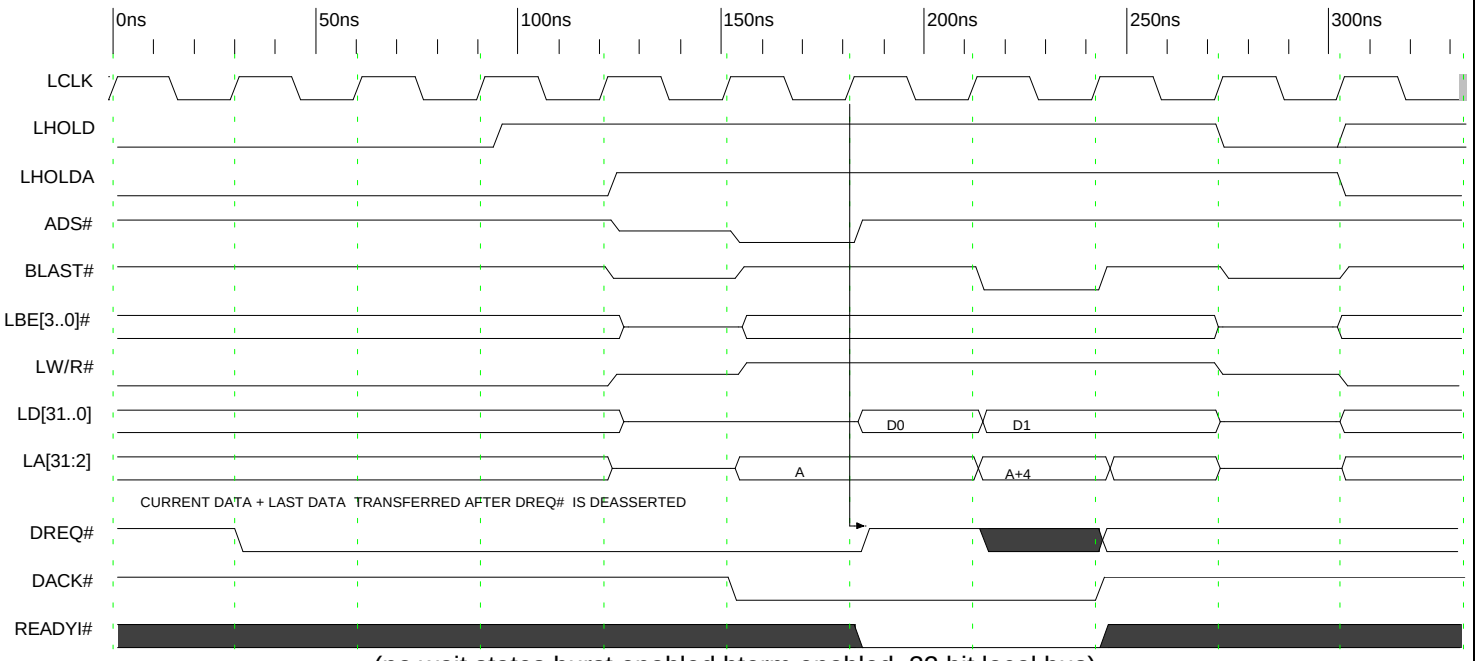
(no wait states, 32 bit bus)
1st Address A are bits 4..31 of the next descriptors pointer register
D0: PCI Start Address, D1: Local Start Address, D2: Transfer Count (bytes), D3: Next Descriptor Pointer

Timing Diagram 18. (CX Mode) PCI9060 Read of DMA Chaining Parameters from Local Bus



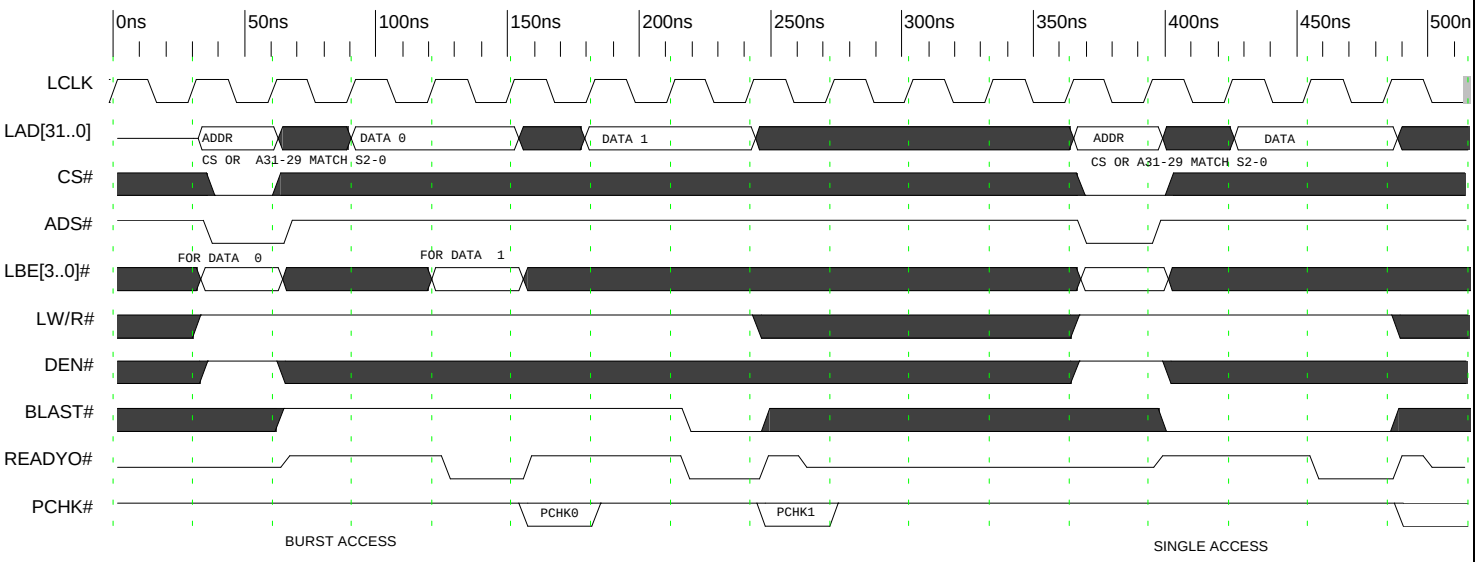
(no wait states, 32 bit local bus)

Timing Diagram 19. (CX Mode) Single Cycle DMA Demand Mode PCI to Local



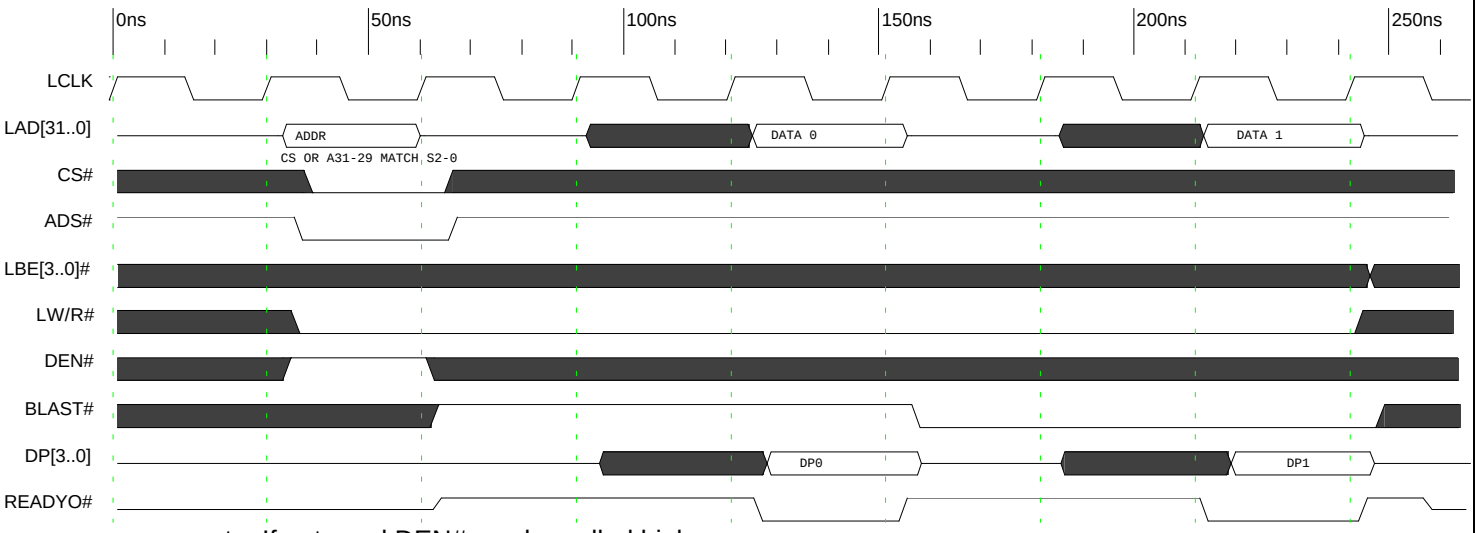
(no wait states,burst enabled,bterm enabled, 32 bit local bus)

Timing Diagram 20. (CX Mode) Multiple Cycle DMA Demand Mode PCI to Local



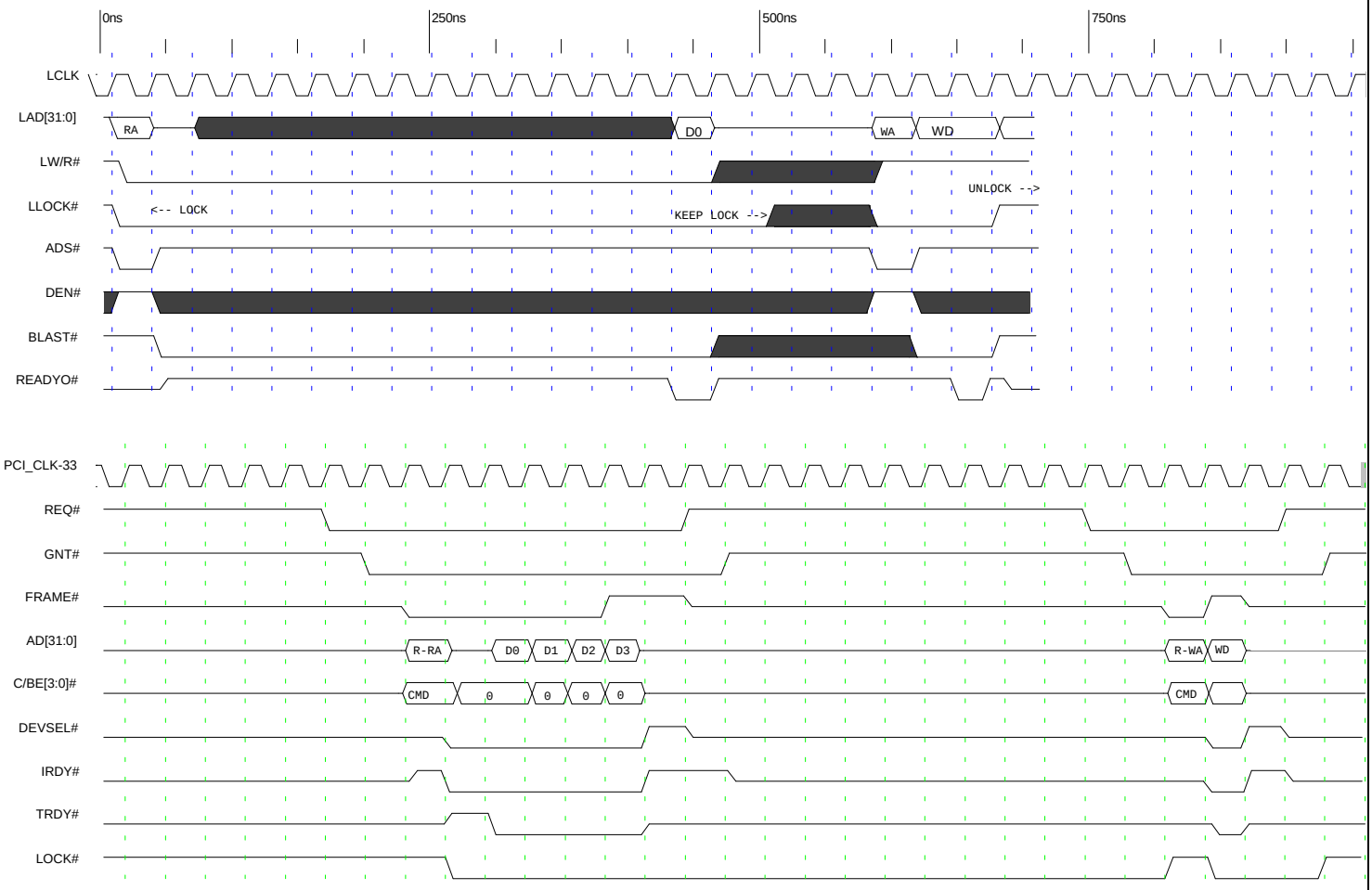
note: If not used DEN# can be pulled high
note: 1st READYo# will be delayed for access to shared registers

Timing Diagram 21. (JX Mode) Local Bus Write to PCI9060 Configuration Register



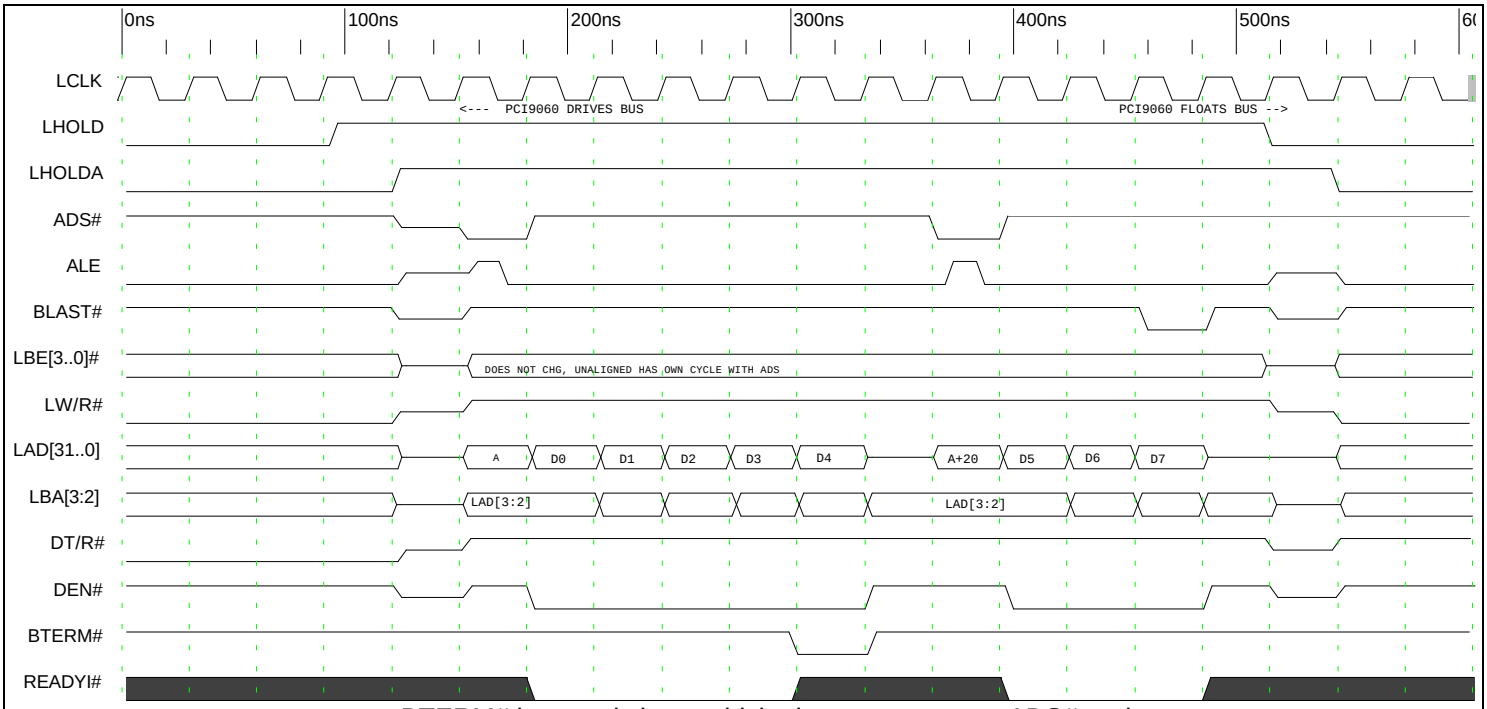
note: If not used DEN# can be pulled high
note: 1st READYo# will be delayed for access to shared registers

Timing Diagram 22. (JX Mode) Local Bus Read from PCI9060 Configuration Register



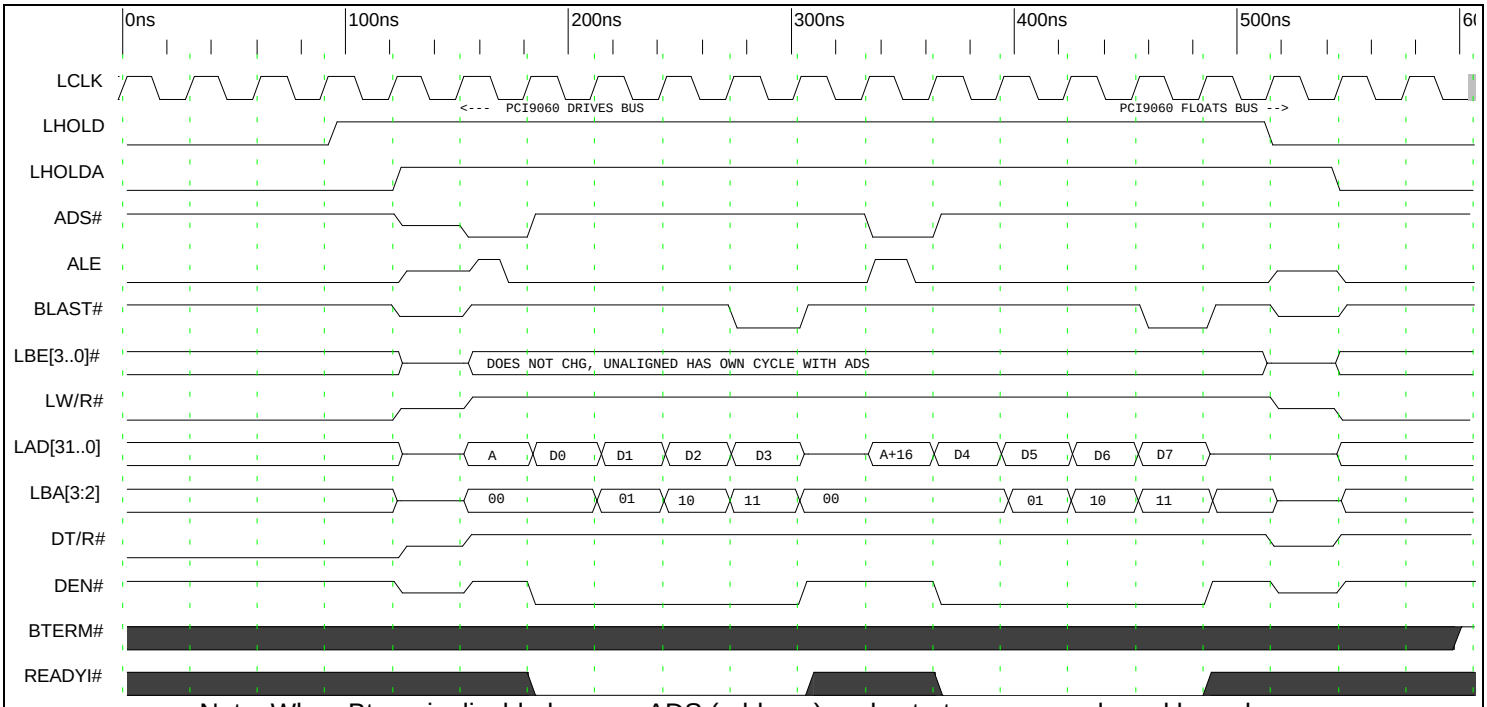
(1 Lword burst read, PCI preread 4 mode)

Timing Diagram 23. (JX Mode) Local Bus Direct Master Locked Read Followed by Write and Release



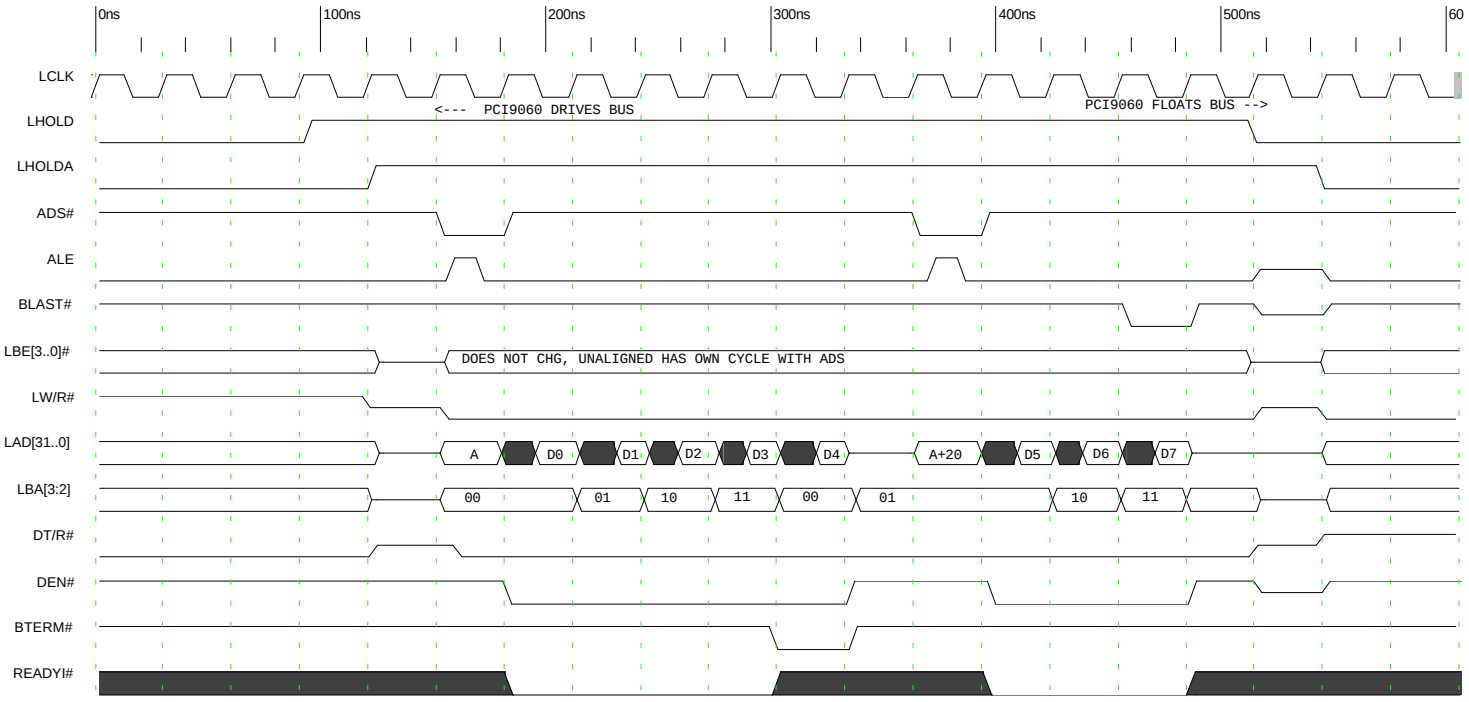
note BTERM# is a ready input which also causes a new ADS# cycle
(no wait states, 32 bit bus,burst enabled)

Timing Diagram 24. (JX Mode) DMA or Direct Slave Burst Write, Bterm Enabled



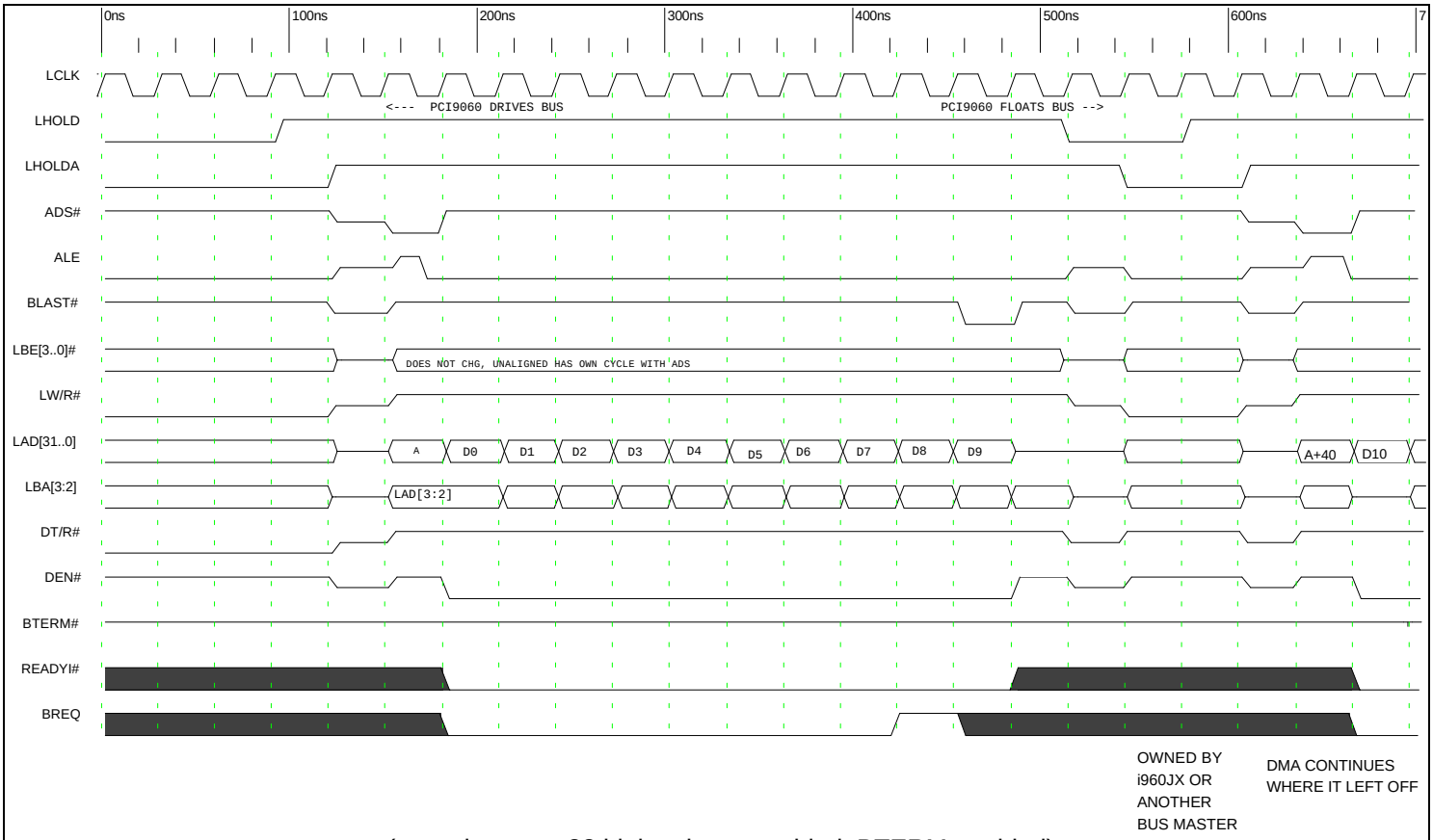
Note: When Bterm is disabled, a new ADS (address) cycle starts every quad word boundary
(no wait states, 32 bit bus,burst enabled)

Timing Diagram 25. (JX Mode) DMA or Direct Slave Burst Write, Bterm Disabled



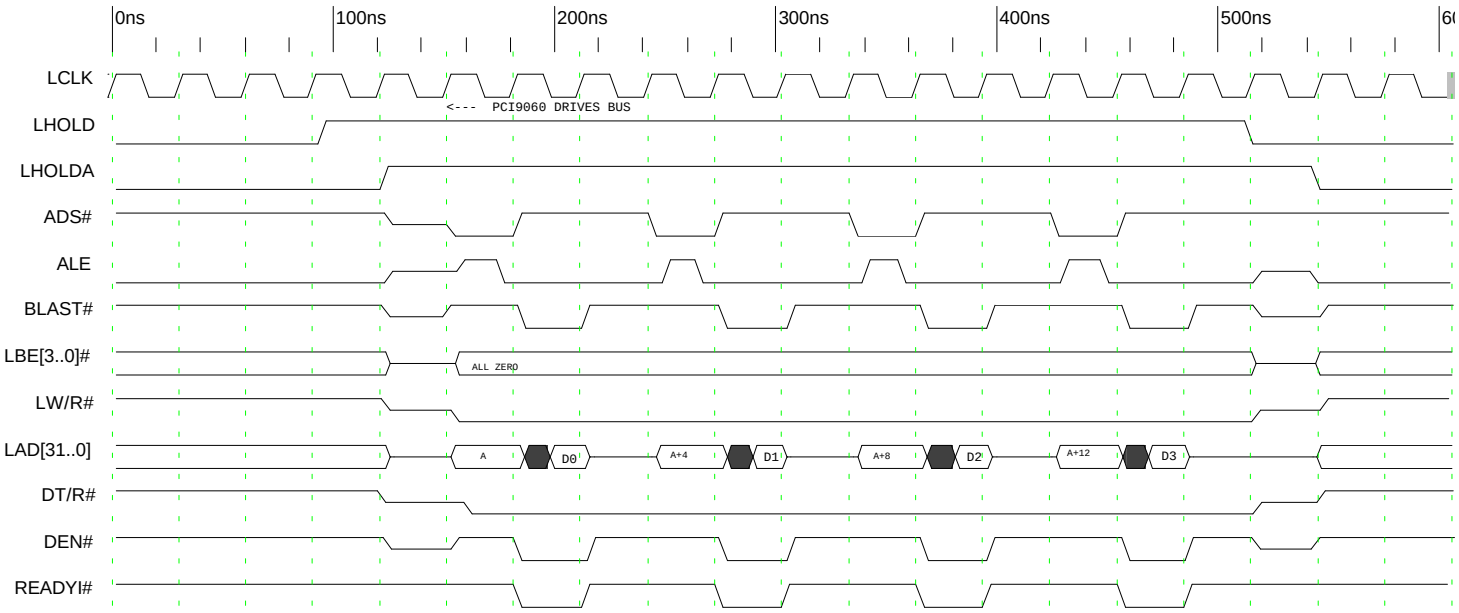
(no wait states, 32 bit bus,burst enabled, BTERM enabled)

Timing Diagram 26. (JX Mode) DMA or Direct Slave Burst Read, Bterm Enabled



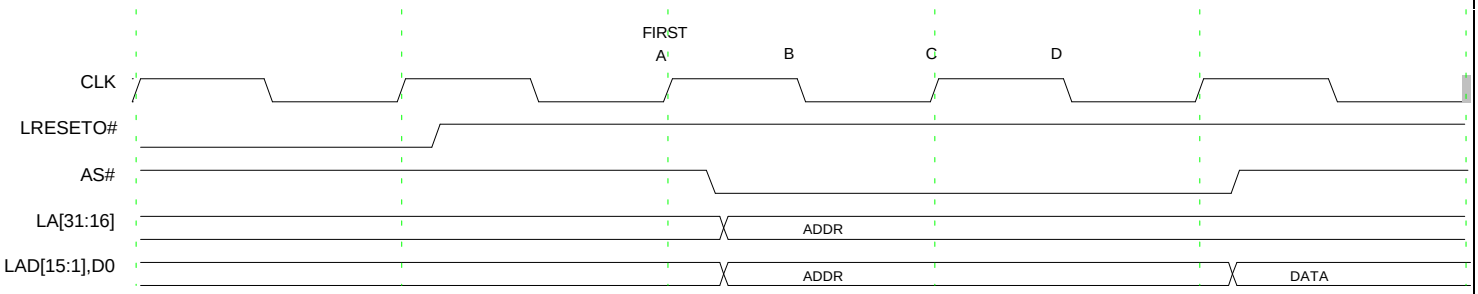
(no wait states, 32 bit bus,burst enabled, BTERM enabled)

Timing Diagram 27. (JX Mode) DMA Burst Write to 32 Bit Local Bus Suspended by BREQ input



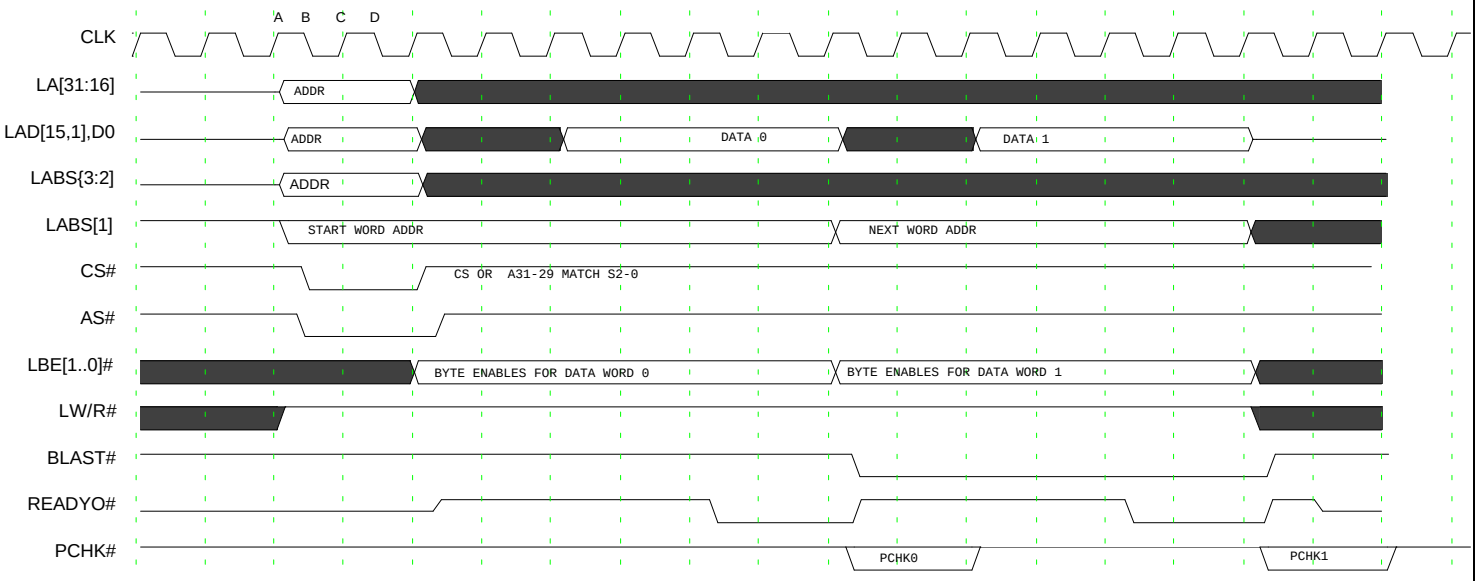
(no wait states, 32 bit bus)
1st Address A are bits 4..31 of the next descriptors pointer register
D0: PCI Start Address, D1: Local Start Address, D2: Transfer Count (bytes), D3: Next Descriptor Pointer

Timing Diagram 28. (JX Mode) Read of DMA Chaining Parameters from Local Bus

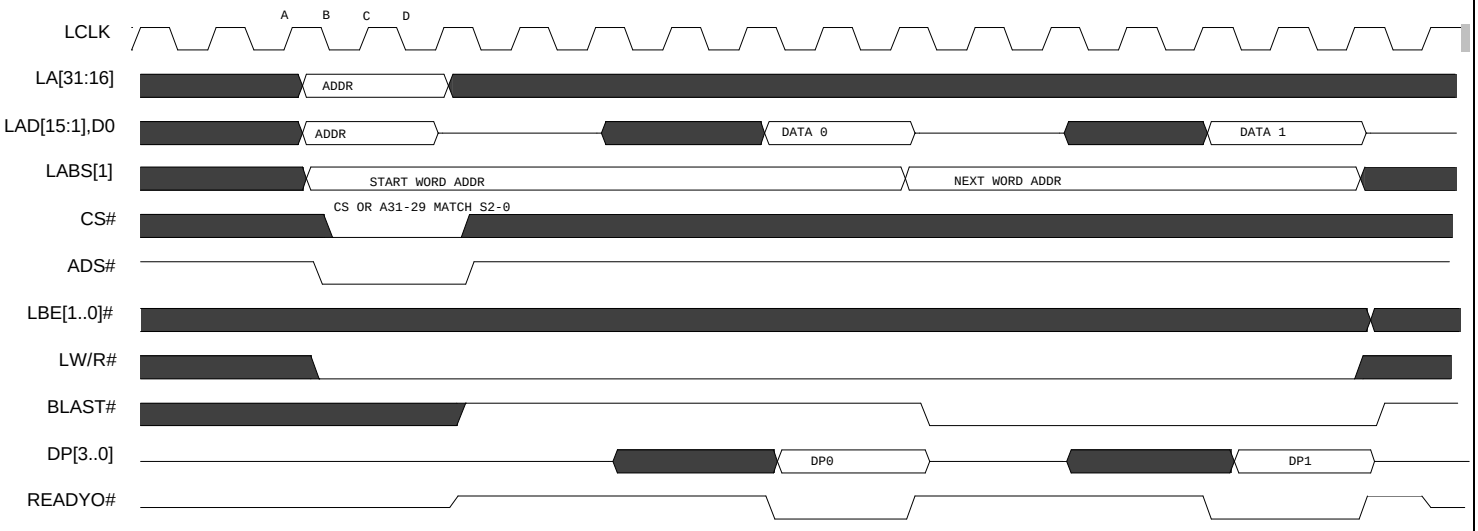


LRESETO# must be used to establish phase A relationship as shown

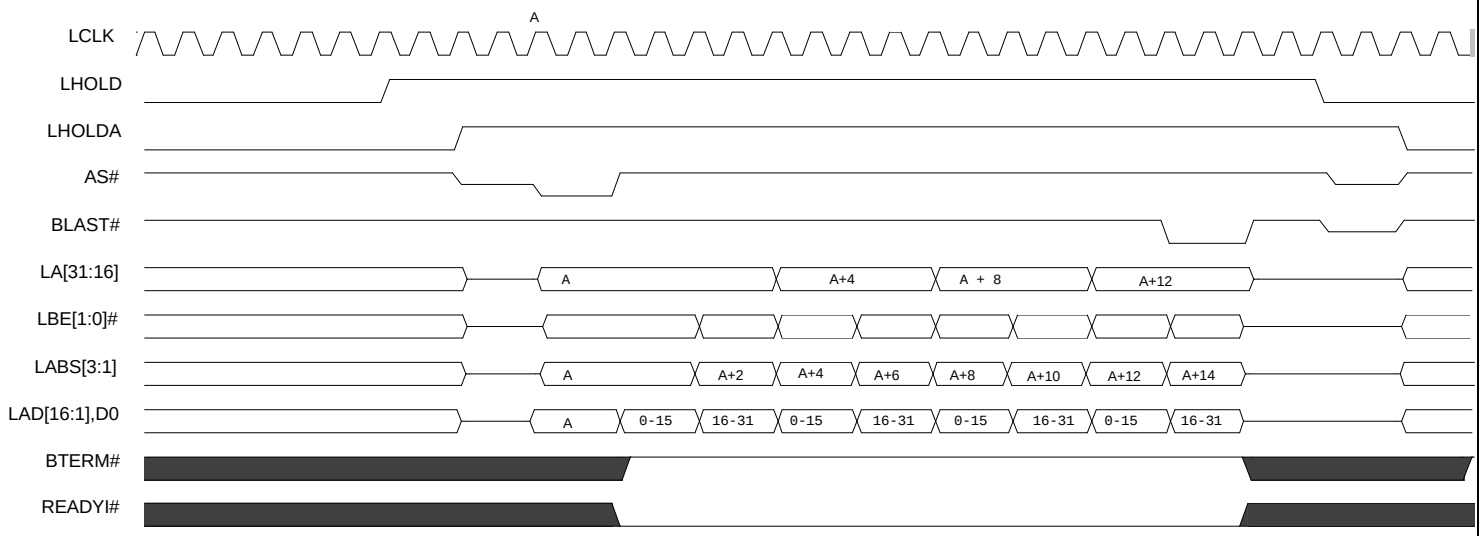
Timing Diagram 29. (SX Mode) Two Phase Clock Synchronization using LRESETO#



Timing Diagram 30. (SX Mode) Local Bus Write to Configuration Register



Timing Diagram 31. (SX Mode) Local Bus Read from Configuration Register



note: not all byte enables asserted results in a new AS#
(no wait states, bus,burst enabled, BTERM enabled)

Timing Diagram 32. (SX Mode) Direct Slave or DMA Burst Write to Local Bus