PCI 9054AC

Errata Rev. 1.3
May 2002

Errata Documentation

A. Affected Silicon Revision

This document details errata in the following silicon:

Product	Part Number	Description	Status
PCI 9054AC	PCI9054-AC50PES	Engineering Samples	September 2001
PCI 9054AC	PCI9054-AC50BES	Engineering Samples	September 2001

B. Documentation Revision

The following documentation is the baseline functional description of the silicon. Errata are defined as behaviors in the affected silicon that do not match behaviors detailed in this documentation.

Document	Revision	Description	Publication Date
PCI 9054 Data Book	2.1	Data Book	January 2000
PCI 9054 Design Notes Documentation	See www.plxtech.com for latest revision	Design Notes Documentation	

C. Errata Summary for the PCI 9054AC is as follows:

#	Description
1	Unaligned DMA transfers with EOT# asserted on the last data
2	Simultaneous Access to Queue Register in Messaging Unit
3	Direct Master Read with PCI Initiator Cache enabled
4	PCI Device ID value
5	Cannot perform a new read or write after backoff – Must resume with last address
6	PCI 9054AC behavior to a TEA# assertion
7	Local Parity Error Status Bit and Interrupt Assertion
8	C/J-mode DMA Burst-4 Mode with Constant Address
9	J-mode DMA with Constant Address for 8- or 16-bit Local Buses
10	DMA Scatter-Gather Descriptor IRDY# PCI Protocol Violation

D. Errata

1. Unaligned DMA transfers with EOT# asserted on the last data

Erratum Issue: During a Local-to-PCI DMA transfer with unaligned addresses, if EOT# is asserted either on the last data phase in Fast Terminate mode (DMAMODEx[15] = 1), or on the next-to-last data phase in Slow Terminate mode (DMAMODEx[15] = 0), a partial transfer of the last data into the DMA Channel FIFO will occur. That partial transfer data will remain in the FIFO and will not be transferred to the PCI bus. On the following Local-to-PCI DMA transfer, the remaining data that should have been flushed from the internal FIFO will be the first data transferred on the PCI Bus.

Solutions/Workarounds: (any)

1. If Demand mode DMA is used (DMAMODE0[12] = 1), instead of aborting DMA with EOT#, first pause the DMA operation by de-asserting DREQ0# and then abort the DMA by setting the DMA Abort bit (DMACSR0[2] = 1). Note that after DREQ# is de-asserted, one or two Local Bus data transfers will move data into the DMA Channel 0 FIFO. This is not an issue because asserting Channel Abort throws away all data in the FIFO.
2. Instead of aborting the DMA with EOT#, first pause the DMA operation by clearing the Channel Enable bit (DMACSRx[0] = 0), and then abort the DMA operation by setting the DMA Abort bit (DMACSRx[2] = 1).
3. In the case where infinite transfers are not being used, since the user knows the transfer count, EOT# should not be asserted on the last data phase of the DMA transfer in Fast Terminate mode, nor on the next-to-last data phase in a Slow Terminate mode.
4. Use only aligned DMA addresses.

2. Simultaneous Access to Queue Register in Messaging Unit

Erratum Issue: The PCI 9054 updates one of four queue pointers automatically each time there is a Read or Write to the messaging unit Inbound (Port 40h) or Outbound (Port 44h) ports. The four registers are the inbound free tail pointer (IFTPR), the inbound post head pointer (IPHPR), the outbound free head pointer (OFHPR), and outbound post tail pointer (OPTPR). If a local master initiates a write to the PCI 9054 messaging unit queue registers simultaneous to a PCI access to the Inbound or Outbound ports, the PCI 9054 will fail to automatically increment the appropriate pointers to reflect this. This can result in overwriting a previous message or retrieving a previously read message from the queue. These pointers cannot be ‘corrected’ due to the fact that the IOP cannot determine if an increment failure has occurred. The failure only occurs when the

PCI 9054 returns READY#/TA# to the local master simultaneous with the PCI 9054 returning TRDY# to the PCI master on an Inbound or Outbound port access that has been retried.

This erratum does not affect the I_2O protocol. It only affects custom messaging unit implementations.

Solutions/Workarounds: (use any)

1. Disable the PCI r2.1 Features Enable bit by clearing MARBR[24]. With this bit clear, the PCI Target Retry Delay Clocks register bits (LBRD0[31:28]) should be set to a value of 3h or greater.

2. **For Multiple Initiator Implementations:**
   a. Implement a semaphore using two on-chip mailboxes or any shared memory region, so that the local master can access the messaging unit queue registers only when the PCI master is not accessing them. Use one mailbox to signal that the PCI bus wants to access the messaging unit and the other mailbox to signal that the Local bus wants to access the messaging unit. Before accessing the messaging unit read the status of the opposite side's mailbox. If the other side has access then Backoff (attempt access later) or else write a flag in the mailbox to claim access. Then read the other mailbox to ensure that both the PCI and Local sides did not write their flags simultaneously. If they did each side will need to Backoff, otherwise access the messaging unit and then clear the flag in the mailbox.
   b. Update the interfering queue registers only from the PCI side, via messages passed through the PCI 9054 internal mailbox registers.

   For Single Initiator Implementations:
   Implement a single request/reply message protocol for custom message passing. This is recommended for applications where there is a single host and the host waits for a reply before initiating a new request.

3. Direct Master Read with PCI Initiator Cache enabled

Erratum Issue: PCI 9054 PCI Initiator (Direct Master) reads with PCI Initiator Cache enabled (DMPBAM[2] = 1) will result in 32-bit data reads intermittently returning incorrect data. The incorrect data returned will be the Lword value at the 32-bit aligned address that immediately precedes the correct value. In other words, data that has been previously cached and read out of the PCI Initiator Read FIFO will be repeated on a subsequent read. This erratum occurs in all three local bus modes (C, J, and M).

Solution/Workaround: Disable PCI Initiator Cache by clearing the PCI Initiator Cache Enable bit (DMPBAM[2] = 0).

4. PCI Device ID value

Erratum Issue: If the PCI 9054 registers are initialized from EEPROM and the PCI Device ID value is less than 0010h, the Initialization Done bit (LMISC[2]) will be set before EEPROM initialization is complete. Consequently PCI BIOS will be allowed access to the PCI 9054 before the chip is ready.

Solutions/Workarounds: (either)

1. Use a Device ID value that is not less than 0010h, for EEPROM loading.
2. Use a local bus processor to initialize the PCI 9054 registers. In such case the local processor must set the Initialization Done bit (LMISC[2]) when initialization is complete.

5. Cannot perform a new read or write after backoff – Must resume with last address

The PCI 9054 Data Book version 2.1 pages 3-16 and 5-14 states:

"A new PCI read is performed if the resumed Local Bus cycle is not the same as the Backed Off cycle". Page 5-14 excludes PCI in the above quote.

Erratum Issue: When the PCI 9054 BREQo/RETRY# signal is enabled (EROMBA[4] = 1) to back off a Direct Master transaction (to resolve a potential deadlock), if the local master does not resume a backed-off transfer with the originally backed-off address, the PCI 9054 will incorrectly assert BREQo/RETRY# without asserting LHOLD. If the local master does not apply the correct continuation address, BREQo/RETRY# will be asserted without LHOLD two clocks after the local master asserts ADS#.

Solution/Workaround:

> Only resume a backed-off transfer with the continuation address, that is, the Master must resume the backed-off transfer with the address that it was backed-off from. Note: when using a TI DSP, make sure it is programmed to correctly resume the read or write from the backed-off address.

6. PCI 9054AC behavior to a TEA# assertion

General functional description of proper TEA# assertion

TEA#, Transfer Error Acknowledge, is a wired-OR M-mode bus signal that is asserted by a Slave device on the Local Bus. The MPC 860 can assert TEA# as a Master or Slave if its Bus Monitor times out (if programmed to do so). TEA# is only to be asserted by a local bus device during a transfer in which it is participating. If the Bus Monitor does time out and the MPC 860 asserts TEA#, the device it is communicating with needs to detect this regardless of its configuration (Master or Slave) and get off the Local bus in one clock cycle. Additionally the device should terminate any active PCI bus activity via an abort and set its status bits/registers appropriately.

Item #1

Erratum Issue:

The MPC 860 can (if programmed to do so) assert TEA# as a Master or Slave if its Bus Monitor times out.

- If TEA# is asserted by the MPC 860 while the PCI 9054AC is the local bus master, TEA# will preempt TA# input and terminate the current cycle. If the burst isn't completed, the PCI 9054AC will generate a new TS# and continue. This applies for Direct Slave and DMA transfers.
- If TEA# is asserted by the MPC 860 while the PCI 9054AC is the local bus slave, the PCI 9054AC ignores TEA#.

Solution/Workaround 1:

Disable or program the MPC 860 Bus Monitor to a value high enough so that it exceeds the amount of time necessary to get the bus and execute the transfer.

Solution/Workaround 2:

Have the MPC 860 assert the LINT# pin instead of TEA# when the Bus Monitor times out. That will cause the PCI INTA# interrupt pin to assert so that the system can issue a software reset to the local section, by setting the PCI 9054AC CNTRL register bit [30] to 1, and then clearing it after the reset is completed.

Item #2

Erratum Issue: If a Target Abort is received on any transfer, the PCI 9054AC may continue to drive the LD[0:31] pins for up to 4 cycles after TEA# has been asserted.

Solution/Workaround:

Do not start a new Local bus cycle for at least four clocks after the PCI 9054AC asserts TEA#.

7. Local Parity Error Status Bit and Interrupt Assertion

Erratum Issue: Parity is checked for Direct Slave Reads, Direct Master Writes and DMA Local Bus Reads. If a parity error is detected, the PCI 9054 will set a status bit, then assert an interrupt (LSERR# C/J-modes, LINT# M-mode) in the clock cycle following that data being checked. However, the data Parity Error status bit will never be set and the interrupt will not be asserted unless the READY# signal for C/J-modes or TA# for M-mode is enabled and asserted low. This will only apply to Direct Slave and DMA transfers when the READY#/TA# signal is disabled in the PCI 9054 register bit(s) for address spaces as indicated below:

- LBRDx[6] for Local Address Spaces 0 and 1
- LBRD0[22] for Expansion ROM space
- DMAMODEx[6] for DMA channels 0 and 1

This erratum does not apply to PCI 9054 parity checking of Direct Master Writes (for which READY#/TA# output cannot be disabled).

Solution/Workaround:

If local parity is to be used for Direct Slave Reads or DMA Local Bus Reads, and the READY# signal (C/J-modes) or TA# signal (M-mode) is not used for these transfers, then the READY# enable bit (LBRDx[6], LBRD0[22], and/or DMAMODEx[6]) should be enabled and the READY#/TA# line pulled low.

8. C/J-mode DMA Burst-4 Mode with Constant Address

Erratum Issue: This erratum applies to PCI 9054 C/J-modes and not to M-mode. When the PCI 9054 performs a DMA cycle in Burst-4 mode (Burst enabled and BTERM# disabled, DMAMODEx[8:7] = 10b) with a Constant Address (DMAMODEx[11] = 1), if the Local starting address is xCh, the PCI 9054 performs single cycles (ADS# & BLAST# are asserted for each data) rather than a burst. However if the starting address is x0h (or x4h, x8h) the PCI 9054 performs a continuous burst cycle, even though BTERM# is disabled.

Solution/Workaround:

If Constant Address DMA is required use either continuous burst mode (both Burst and Bterm mode bits enabled, DMAMODEx[8:7] = 11b) or non-burst (DMAMODEx[8] = 0) modes, or M-mode, rather than C/J-mode Burst-4 mode.

9. J-mode DMA with Constant Address for 8- or 16-bit Local Buses

Erratum Issue: This erratum applies to PCI 9054 J-mode and not to C- or M-modes. For DMA the Local Addressing Mode register bit can be set to enable Constant Address on the LA[28:2] and multiplexed LAD[31:0] address buses (DMAMODEx[11] = 1), or this bit can be cleared (default) to cause the local address to increment during DMA. In J-mode, during the address phase, LAD[1:0]# are valid address bits (and these bits toggle to match the LBE[1:0]# state), regardless of whether Constant Address is enabled. Thus with an 8- or 16-bit Local bus the LAD[1:0] address is not held constant.

Solution/Workaround:

For 8- or 16-bit data widths decode the address to an Lword boundary using only the upper address lines (LAD[27:2]) to select the appropriate port.

10. DMA Scatter-Gather Descriptor IRDY# PCI Protocol Violation

Erratum issue: If the PCI 9054 receives a PCI Target Abort when reading a Scatter-Gather DMA descriptor from the PCI bus, the PCI 9054 will immediately float the IRDY# signal, rather than drive the IRDY# signal from active (level 0) to inactive (level 1) for 1 PCI clock period before floating, as is required by the PCI Specification for STS I/O buffer protocol. As a result, it may take several PCI clocks for the IRDY# signal to reach a TTL logic level high.

Solution/Workaround:

No fix is required, and no failures have been observed. The PCI Specification also requires that IRDY# have a pull-up resistor on the motherboard. If the above condition is encountered, adding an external pull-up (in parallel with motherboard pull-up) will decrease the resistance to allow the signal to reach a TTL logic high more quickly.
