Addendum to the PCI 9054 Data Book Revision 2.1

A. Affected Silicon Revisions

Product	Part Number	Description	Production
PCI 9054	PCI 9054-AC50PI	Released 176-pin PQFP Product	February 2002
PCI 9054	PCI 9054-AC50BI	Released 225-pin PBGA Product	February 2002

B. Documentation Revision

Document	Revision	Description	Publication Date
PCI 9054 Data Book	2.1	Data Book	January 2000
PCI 9054 Data Book Addendum	2.2	Data Book Addendum	April 2002
PCI 9054AC Errata	See www.plxtech.com for latest revision	Errata Documentation	
PCI 9054 Design Notes	See www.plxtech.com for latest revision	Design Note Documentation	
PCI 9054 AB to AC Conversion Document	See www.plxtech.com for latest revision	PCI 9054 Conversion from Rev. AB to Rev. AC	

C. M-Mode AC Timing Changes

When the PCI 9054 is operated in M-Mode, the AC timing for the signals listed in the table below take precedence over the values published in Table 13-8 of the PCI 9054 Data Book, revision 2.1.

M-Mode Output Delay Timing Table Changes

Signal (Synchronous Outputs) C_L = 50 pF, VCC = 3.0V, Ta = 85 °C	**Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AC** (Data Book Addendum Rev 2.2)	**Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AB** (Data Book Rev 2.1)
BDIP#	13.2	10.5
LA[0:31]	10.2	10.0
DMPAF	N/A*	13.0
TEA#	9.3	8.5

* Note that the DMPAF signal is an asynchronous signal; therefore, it will be caught on the next clock edge.

D. Hot Swap Control/Status Register Reset Value Change

The specified reset value of the Board Insertion ENUM# Status Indicator, bit 7 of the Hot Swap Control/Status register (HS_CSR: PCI:4Ah, LOC:18Ah) has been changed from the value published on page 11-17 of the PCI 9054 Data Book, revision 2.1. The new reset value is shown below.

Register 11-33 (HS_CSR; PCI:4Ah, LOC:18Ah) Hot Swap Control/Status

Bit	**Description**	**Value After Reset PCI 9054 Revision AC** (Data Book Addendum Rev 2.2)	**Value After Reset PCI 9054 Revision AB** (Data Book Rev 2.1)
7	Board Insertion ENUM# Status Indicator	0	1

E. TEA# Functional Description for PCI 9054 Revision AC

The functionality of TEA# has been changed relative to the PCI 9054 Data Book, revision 2.1.

PCI 9054 TEA# assertion

The PCI 9054 will assert the TEA# signal in response to Master Aborts, Target Aborts and other specified error conditions that may occur during DM reads or writes, CFG reads or writes, or DMA accesses.

Depending upon the error/abort condition and when it is detected, TEA# will either be asserted during the currently active local bus transfer or when the Motorola MPC860 returns to attempt a new DM R/W, CFG R/W or DMA transfer, or resumes a deferred read.

When it is asserted, TEA# is always a one-clock-pulse-wide signal, synchronous to the rising edge of the clock.

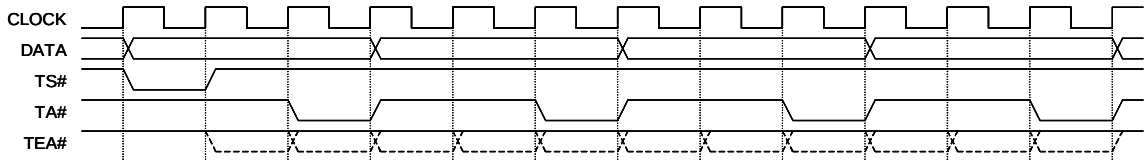
When enabled (INTCSR[0] = 1), TEA# will be asserted under the following error/abort conditions:

1. A Master Abort condition occurs (PCISR[13] = 1) during a CFG R/W or DM R/W or DMA.
2. A Target Abort is received (PCISR[12] = 1) during a CFG R/W or DM R/W or DMA.
3. A transfer is retried 256 times by the Target (PCISR[12] = 1) during a CFG R/W or DM R/W or DMA.

TEA# will be asserted regardless of the Deferred Read Enable bit (LMISC[4]) setting.

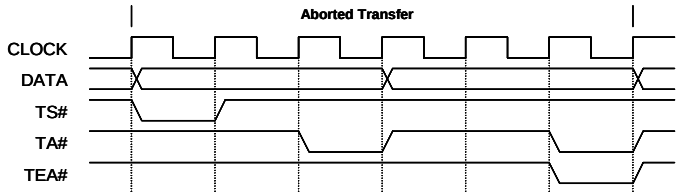
The PCI 9054 can assert TEA# anytime during the transfer, following the clock period during which TS# was asserted as shown in Figure 1.

Figure 1. Normally Terminated Bus Transfer



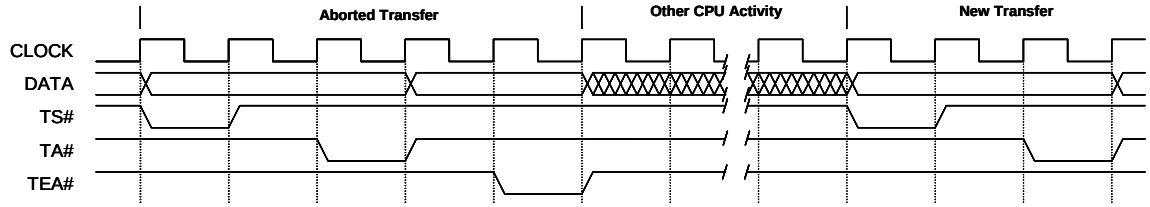
The PCI 9054 can assert TEA# at the same time as TA# to abort the transfer, as shown in Figure 2.

Figure 2. Transfer Aborted with TEA# and TA# Assertion



The PCI 9054AC can assert TEA# to abort the transfer before TA# would have been asserted. When this occurs, TA# will not be asserted until a new transfer begins as shown in Figure 3.

Figure 3. Transfer Aborted with TEA# Asserted Before TA#



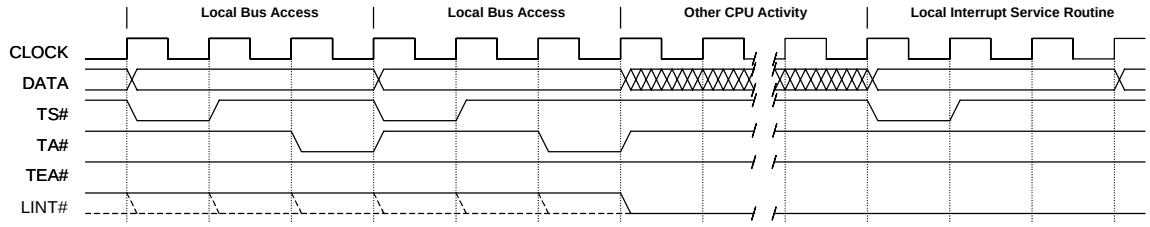
Using LINT# with TEA#

The PCI 9054 will assert the LINT# signal under the following circumstances:

1. Messaging Queue outbound overflow or inbound not empty.
2. DMA Channel 0 or 1 Transfer is done or has reached a terminal count.
3. A Local or PCI Parity error has been detected.
4. A Doorbell, BIST, Mailbox or Power Management interrupt has been set.
5. A Master Abort (No DEVSEL) was received during a DMW, DMA, CFG, DMR transfer.
6. A Target Abort was received or 256 Retries was detected during a DMW, DMA, CFG, DMR transfer.

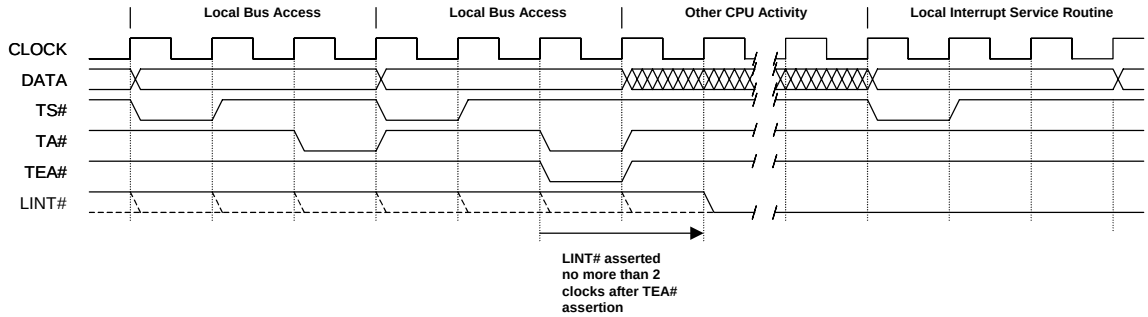
Unlike TEA#, LINT# may be asserted at any time, even when the PCI 9054 is not performing a local bus transfer as shown in Figure 4.

Figure 4. LINT# Assertion without TEA#



If TEA# is asserted during a local bus transfer, LINT# will be asserted within two clock cycles as shown in Figure 5.

Figure 5. LINT# Assertion with TEA#



If the abort bits PCISR [13:12] that caused LINT# are cleared before a DM R/W, CFG R/W or DMA transfer is attempted, the new transfer will proceed normally (TEA# is not issued).

PCI 9054 Response to a TEA# assertion – Bus Monitor Timeout
The Motorola MPC860 can (if programmed to do so) assert TEA# as a Master or Slave if its Bus Monitor times out.

1. If TEA# is asserted by the MPC860 while the PCI 9054 is the local bus master, TEA# will preempt the TA# input and terminate the current cycle. If the burst isn't completed, the PCI 9054 will generate a new TS# and continue. This applies for DS and DMA transfers.
2. If TEA# is asserted by the MPC860 while the PCI 9054 is the local bus slave, the PCI 9054 ignores TEA#.

If LMISC[5] =1, the PCI 9054 can generate a SERR# on the PCI bus upon detection of TEA# being asserted, as described on page 11-22 of the PCI 9054 Data Book, revision 2.1.