PCI 9054/SA-1110 AN

July 7, 2000

Version 2.1

PCI 9054 to StrongARM™ SA-1110 Application Note

Features

- PCI 9054
- SA-1110 Processor Local bus running at 47.925MHz.
- SDRAM 8M x 32bit
- Shared Memory SDRAM

General Description

The PCI 9054/SA-1110 Application Note connects a PCI 9054 with a StrongARM™ SA-1110 processor. The two devices share a common SDRAM.

This application note uses the PLX Technology PCI 9054 v2.2 compliant 32 bit, 33MHz PCI Bus Master I/O Accelerator with PCI power management features for adapters and embedded systems. The PCI 9054 has Direct Master, DMA and Direct Slave data transfer capabilities. Direct Slave gives a master device on the PCI Bus the ability to access memory on the Local bus. The PCI 9054 allows the Local bus to run asynchronously to the PCI Bus through the use of bi-directional FIFOs.

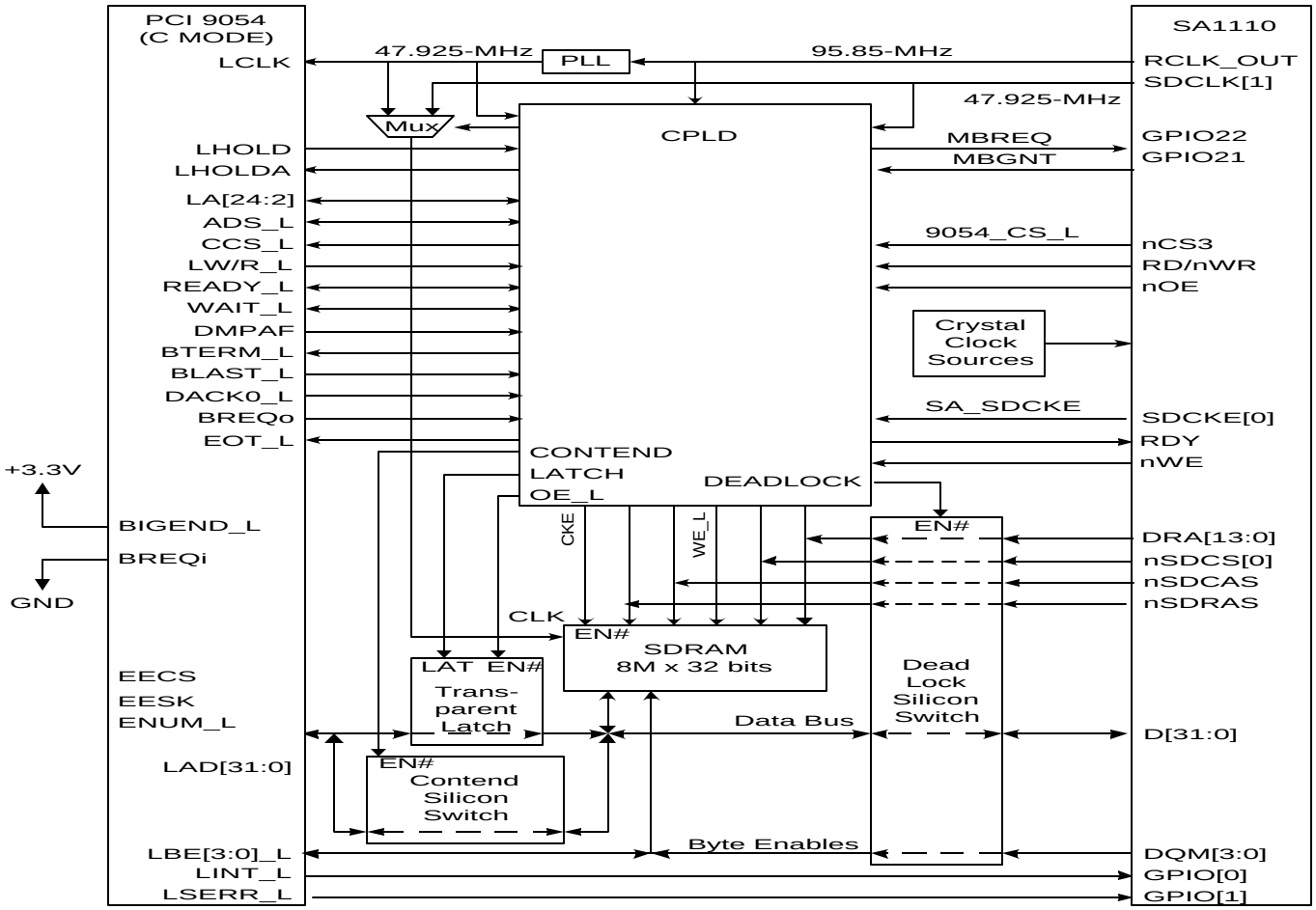

Figure 1. PCI 9054/SA-1110 Block Diagram

TABLE OF CONTENTS

LIST OF FIGURES

1. Block Diagram Components

The Block Diagram for the PCI 9054/SA-1110 Application Note is shown in Figure 1. The following subsections describe each block of the diagram.

1.1. PCI 9054

The PCI 9054 is the PCI Interface chip, which can become the Local bus master to access the SDRAM. It also provides the PCI deadlock detection signal BREQo.

1.2. Crystal Clock Sources

The Crystal Clock Sources provide the two crystals (3.6864-MHz and 32.768-KHz), which the SA-1110 needs to operate.

1.3. PLL

The PLL (Phase Lock Loop) inputs the SA-1110 RCLK_OUT signal (95.85-MHz) and outputs a phase locked 47.925-MHz signal to the PCI 9054, CPLD, and MUX. This 47.925-MHz signal is used to clock the SDRAM when the PCI 9054 is accessing the SDRAM.

1.4. SA-1110

The SA-1110 is the local processor. Upon power up the SA-1110 is bus master. The SA-1110 outputs a 95.85-MHz clock continuously on the RCLK_OUT pin. For SDRAM accesses the SA-1110 outputs a 47.925-MHz clock on the SDCLK[1] pin which is used to clock the SDRAM.

1.5. MUX

The MUX passes either the SA-1110 SDRAM clock signal SDCLK[1] or the PLL clock signal to the SDRAM. The CPLD controls which of the clock signals is passed.

1.6. SDRAM

The SDRAM is the shared memory accessed by both the SA-1110 and the PCI 9054. The SDRAM operating mode with the SA-1110 is sequential burst length of one. The operating mode of the SDRAM with the PCI 9054 is Full Page.

1.7. CPLD

The CPLD performs many functions. It does the bus arbitration. It reconfigures the SDRAM mode for the SA-1110 and the PCI 9054. The CPLD is the SDRAM interface for PCI 9054 accesses. The CPLD implements deadlock recovery. The CPLD controls the MUX, Transparent Latch, and the switches. The CPLD is clocked at 95.85-MHz. I have estimated the CPLD to be a Xilinx XC9572XL-5TQ100 with 5ns delay. This CPLD costs about $8.40 in quantity.

1.8. Contend Silicon Switch

This Contend Silicon Switch is used to avoid bus contention between the SDRAM and the PCI 9054. The potential contention occurs when the PCI 9054 does a burst read from the SDRAM followed by a write. The CPLDs CONTEND signal disables the Contend Silicon Switch during this time and prevents the bus contention.

1.9. Deadlock Silicon Switch

The Deadlock Silicon Switch is used to recover from PCI deadlock. Deadlock recovery requires that the SA-1110 is backed off the local bus so that the PCI 9054 Direct Slave access can complete its bus cycle. See section 2.3 for details on deadlock recovery.

1.10. Transparent Latch

The Transparent Latch is used on SA-1110 reads of the PCI 9054 to extend the data valid time. See section 2.1.2.1 for details on the Transparent Latch.

2. Functional Description

The SA-1110 processor and the PCI 9054 are the two bus masters that transfer data on the local bus. The CPLD is bus master only between the bus masterships of the SA-1110 and the PCI 9054. The CPLD is bus master only long enough to reconfigure the SDRAM mode for the SA-1110 and the PCI 9054. The operations of these bus masters are discussed in the following subsections.

2.1. SA-1110 bus master

The SA-1110 can access both the SDRAM and the PCI 9054. These accesses are discussed in the following subsections.

2.1.1. SDRAM Access

The SA-1110 should be the power up bus master. Upon power the SA-1110 configures the SDRAM for sequential burst length of one access. When the SA-1110 is bus master it is effectively connected directly to the SDRAM through the Deadlock Silicon Switch, MUX, and CPLD. The CPLD tells the MUX to pass the SA-1110 SDCLK[1] signal to the SDRAMs. The CPLD passes the SA-1110 SDCKE[0] signal on to the SDRAM with no clock delay.
The SA-1110 performs all SDRAM refresh operations. When the PCI 9054 is bus master it must return the local bus to the SA-1110 in time for the SA-1110 to perform any required refresh operations. The PCI 9054 and the CPLD do not interfere with the SA-1110 interface with the SDRAM.

2.1.2. PCI 9054 Access

When the SA-1110 accesses the PCI 9054 it asserts nCS3. The CPLD uses this output to assert the PCI 9054 CCS_L pin. The CPLD uses READY_L, RDY and other signals to complete any SA-1110 access. The SA-1110 writes data to the PCI 9054 through the Contend Silicon Switch. The SA-1110 reads PCI 9054 data through the Transparent Latch. The Transparent latch is controlled by the CPLD to extend the data valid time for the SA-1110.

2.1.2.1. Why the Transparent Latch is needed

Combinations of factors contribute to the need for the Transparent Latch. These factors are shown below:

- There is no specified phase relationship between the SA-1110 RCLK_OUT and its internal (hidden) memory clock. Therefore there is no assured phase relationship between LCLK and memory clock.
- SA-1110 requires three sequential samplings or the RDY pin by memory clock (rising edge, falling edge, and rising edge) before it is accepted as valid.
- The PCI 9054 asserts READY_L for only one LCLK period.
- The read data from the PCI 9054 invalids with the negation of READY_L.

This requires that the RDY signal must be an extended version of the PCI 9054 READY_L output to account for worse case clock phase, and setup/hold time requirements. This also means that the earliest confirmation provided by the SA-1110 that is has accepted its RDY pin as asserted is the negation of signals nWE or nOE.

2.2. PCI 9054 Bus Master

The PCI 9054 gets the bus only when a Direct Slave access is pending. Normally when this happens the PCI 9054 requests the bus from the SA-1110. The CPLD changes the mode of the SDRAM from SA-1110 mode (sequential burst length of one) to PCI 9054 mode (Full Page). The PCI 9054 accesses the SDRAM. When done the CPLD changes the mode of the SDRAM back to SA-1110 mode and releases the bus to the SA-1110. This sequence is discussed in detail in the following subsection.

2.2.1. SDRAM Mode Change

The PCI 9054 has a burst forever feature. The PCI 9054 can burst an entire page of SDRAM memory and so provides higher burst performance. Zero wait state burst read performance requires that the SDRAM be in Full Page mode.

2.2.2. PCI 9054 Access Sequence of Events

A sequential description of the events involved with a PCI 9054 local bus mastership is shown below. Note that pull up or pull down resistors negate any floating signals.

1. The SA-1110 is Local bus master.
2. The PCI 9054 requests the bus by asserting LHOLDA.
3. The CPLD asserts MBREQ to the SA-1110.
4. The SA-1110 completes its current bus cycle.
5. The SA-1110 asserts MBGNT. The SA-1110 has granted the local bus to the CPLD.
6. The SA-1110 tri-states its SDRAM control signals.
7. The CPLD negates the SDRAM CKE pin.
8. The CPLD switched the SDRAM CLK source from SA-1110 SDCLK[1] to the PLL at the MUX.
9. The CPLD asserts the SDRAM CKE pin.
10. The CPLD changes the mode of the SDRAM to Full Page.
11. The CPLD asserts LHOLDA to the PCI 9054. The CPLD has granted the local bus to the PCI 9054.
12. PCI 9054 accesses the SDRAM. The CPLD drives the SDRAM control signals.
13. PCI 9054 completes its SDRAM access and negates LHOLD. The PCI 9054 had released the local bus to the CPLD.
14. The CPLD negates LHOLDA.
15. The CPLD changes the SDRAM mode back to sequential burst length of one.
16. The CPLD negates the SDRAM CKE pin.
17. The CPLD switches the SDRAM CLK source from the PLL to the SA-1110 SDCLK[1] at the MUX.
18. The CPLD negates MBREQ.
19. The CPLD tri-states its SDRAM control signals.
20. The CPLD has granted the local bus back to the SA-1110.
21. The SA-1110 negates MBGNT.
22. The CPLD passes on the SA-1110 SDCKE[0] signal to SDRAM CKE with no clock delay.
23. The SA-1110 is local bus master again.

2.3. Handling Deadlock

PCI chips have an inherent stuck condition called deadlock. This occurs when a direct slave and a direct master access are attempted simultaneously through the same PCI chip. Under deadlock neither access can complete due to their need to gain simultaneous mastership of both the PCI and local bus to complete their transaction. The sequence of deadlock recovery is discussed in the following subsection.

2.3.1. Deadlock Recovery Sequence

Deadlock recovery is described below as a sequence of events. During deadlock the SA-1110 is only accessing the PCI 9054. There is no possibility that a SDRAM access is occurring. Note that the pull up or pull down resistors negates any floating signals.

1. Simultaneously a direct slave and direct master accesses are attempted across the PCI 9054 while the SA-1110 is local bus master.
2. The PCI 9054 asserts LHOLD to the CPLD.
3. The PCI 9054 detects deadlock and asserts BREQo.
4. The CPLD maintains a negated RDY to the SA-1110.
5. The CPLD asserts DEADLOCK to the Deadlock Silicon Switch. This isolates the SA-1110 from the SDRAM and makes the CPLD the effective bus master.
6. The CPLD drives the SDRAM control signals.
7. The CPLD negates SDRAM CKE.
8. The CPLD switches the MUX to pass the PLL clock to the SDRAM.

9. The CPLD asserts SDRAM CKE.
10. The CPLD maintains a negated CONTEND output to enable the SDRAM silicon switch.
11. The CPLD changes the mode of the SDRAM to Full Page for PCI 9054 access.
12. The CPLD asserts LHOLDA to the PCI 9054. The CPLD has granted the local bus to the PCI 9054.
13. PCI 9054 accesses the SDRAM.
14. PCI 9054 completes its SDRAM access and negates LHOLD. The PCI 9054 has released the local bus to the CPLD.
15. The CPLD negates LHOLDA.
16. The CPLD changes the mode of the SDRAM back to sequential burst length of one for SA-1110 access
17. The CPLD negate SDRAM CKE.
18. The CPLD switches the MUX to pass the SA-1110 SDCLK[1] to the SDRAM.
19. The CPLD passes on the SA-1110 SDCKE[0] signal to SDRAM CKE with no clock delay.
20. The CPLD tri-states its SDRAM control signals.
21. The CPLD negates DEADLOCK. The SA-1110 is now the local bus master again.
22. The SA-1110 continues its access to the PCI 9054.
23. The PCI 9054 asserts READY_L., which causes the CPLD to assert RDY ending the SA-1110 access.
24. The SA-1110 completes its access to the PCI 9054.
25. All pending accesses are now complete.

3. Restrictions

This application note places some restrictions on the use of the SA-1110 and the PCI 9054 as follows.

- The user must consider the enabling of SA-1110 data caching and buffering because data coherence cannot be assured for all applications. SA-1110 instruction caching is allowed provided that direct slave operations do not modify instruction memory.

4. Summary

The PCI 9054 and SA-1110 can share the SDRAM. The PCI 9054 makes zero wait state burst accesses to the SDRAM. The PCI 9054 bursts are continuous and can cover an entire SDRAM page, allowing high burst transfer rates.

5. ASSUMPTIONS

This application note is based on the following assumption:

- Some typically necessary design components and functions (i.e. boot and code memory, EEPROM, and System Reset) are not included in this application note.

The designer is expected to add such components and functions, as their design requires.

6. REFERENCES

- PCI 9054 Data Book v2.1
  PLX Technology, Inc.
  390 Potrero Avenue
  Sunnyvale, CA 94085 USA
  Tel: 408 774-9060, 800 759-3735,
  Fax: 408 774-2169,
  http://www.plxtech.com/

- StrongARM™ SA-1110 Data Book Advanced Developer's Manual
  Intel Cooperation
  2200 Mission College Blvd.
  Santa Clara, California 95052-8119 USA
  Tel: 408-765-8080
  Fax: 408-765-9904
  http://www.intel.com/design/strong/

- SYNCHRONOUS DRAM Data Sheet
  64MB: x4, x8, x16 SDRAM
  Micron Semiconductor Products, Inc.
  8000 S. Federal Way
  P.O. Box 6
  Boise, Idaho 83707-0006
  Tel: 208-368-3900
  Fax: 208-368-4617
  http://www.micron.com/mti/index.html
  Customer Comment Line:
  U.S.A. 800-932-4992
  Intl.: 01-208-368-5090
  Fax: 208-368-5018