PCI 9054/POM1 AN

July 31, 2000
Version 2.0

POM1 to PCI 9054
Application Note

Features

- Local Master cycle to the host PCI bus through the IOP 480
- Expand the IOP 480 RDK with the private PCI bus
- PCI Arbiter
- IOP 480 RDK Fly-By DMA Transfer from Local Memory to PCI 9054

General Description

The PCI 9054 POM1 (PLX Option Module 1) is designed to plug into the POM1 connector of the IOP 480RDK. It enables designers to initiate a Local Master cycle to the host PCI bus through the IOP 480 and expand IOP 480 RDK with the private PCI bus. The PCI 9054 is the main component of the PCI 9054 POM1 in addition to the Serial EEPROM, PCI Connector and Arbiter. The PCI 9054's Local bus is programmed to operate in Jx bus mode so that it can connect directly to the IOP 480 Local bus.

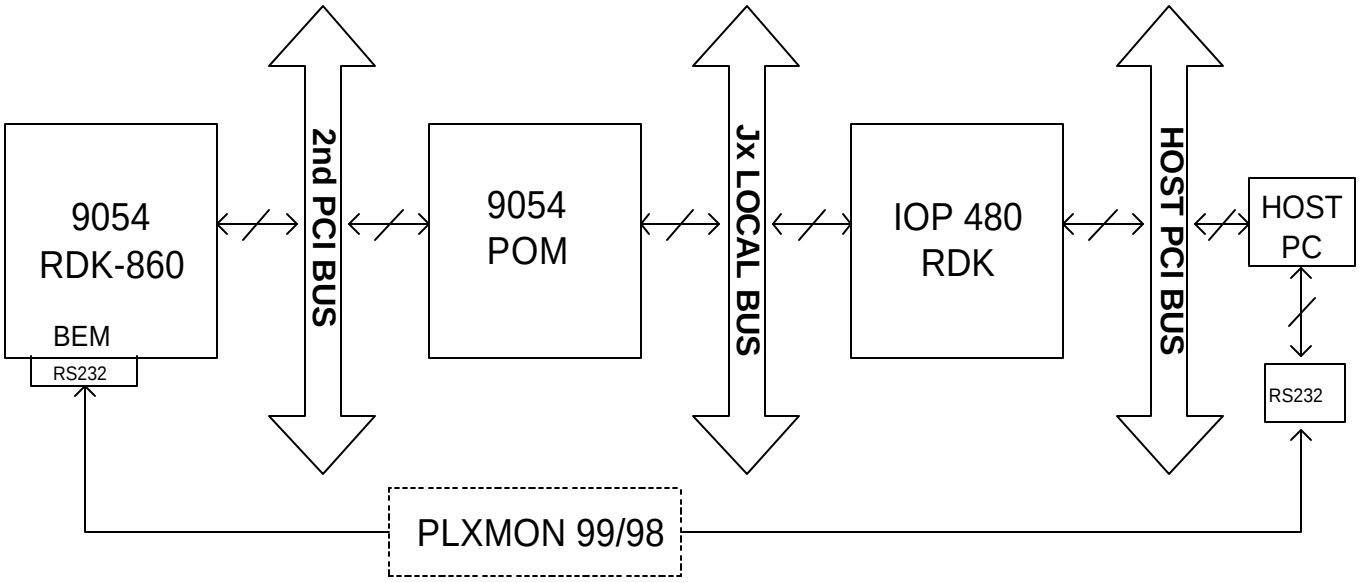

Figure 1. PCI 9054 POM1 Application Block Diagram

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TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1. INTRODUCTION

The PCI 9054 POM1 (PLX Option Module 1) is designed to plug into the POM1 connector of the IOP 480. It enables designers to initiate a Local Master cycle to the host PCI bus through the IOP 480 and expand the IOP 480 RDK with the private PCI bus. The PCI 9054 is the main component of the PCI 9054 POM1 in addition to the Serial EEPROM, PCI Connector and Arbiter. The PCI 9054's Local bus is programmed to operate in Jx bus mode so that it can connect directly to the IOP 480 Local bus.

2. POM1 CONNECTOR

The PCI 9054 POM1 connects directly to the IOP 480's PLX Option Module connector. The PCI 9054's Local bus is programmed to operate in Jx bus mode so that additional glue logic is not required.

3. PCI CONNECTOR

The PCI 9054 POM1 supports one 5.0 volts 32-bit female PCI connector. The integrated PCI arbiter allows PCI master capability adapter cards, such as the PCI 9054RDK-860 or other PLX RDK's to be installed in this slot. In this configuration the user can utilize the PLXMON 99/98 executable file from the PCI SDK to program the PCI 9054 POM1 internal registers and perform PCI read/write cycle to the PCI 9054; which in turn generates the Local bus master cycle to the IOP 480 (see Figure 1).

Procedure to Access PCI 9054 POM1:

1. Connect one end of the 9-pin serial cable to the serial port of the PCI 9054RDK-860 and the others to the open serial port of the host PC

2. Execute PLXMON 99/98 from the host PC

3. Switch to serial mode and use PLXMON command to perform read/write cycle to the PCI 9054 on the PCI 9054 POM1. Refer to the PLXMON 99/98 manual for the list of PLXMON commands.

The IDSEL on the PCI connector is connected to AD12 and the PCI 9054 on the PCI 9054 POM1 IDSEL is connected to AD11. All of the PCI signals have been external pulled-up through the 10K network resistors.

4. RESET AND REGISTER INITIALIZATION

During power on reset, the IOP 480 generates the local reset to the PLX Option Module (POM1). This local reset signal is connected to the PCI 9054 RST# pin and PCI slot RST# pin and is used to reset the PCI 9054 POM1.

Right after reset, the PCI 9054 POM1 loads from the 2K Serial EEPROM. This Serial EEPROM contains all critical configuration data for the Local Configuration Registers. These include PnP data, PCI memory resource allocation, and Local memory resource allocation. The PCI configuration of the PCI 9054 must be programmed before it can respond to the PCI bus operations. This can be done in two ways:

1. Configure the PCI 9054RDK-860 to set up the PCI 9054 POM1 PCI Configuration Register or

2. Configure the IOP 480 to set up the PCI 9054 POM1 PCI Configuration Register. (Option: install jumper on pin 7-8 of JP2 and remove R10 to drive CCS# active at all time.)

5. CLOCKS

PCI Clock – The PCI 9054 and PCI slot clock operates up to 33Mhz. An external 33MHz oscillator, in conjunction with a clock buffer, is used to provide the clock for the PCI 9054 and PCI slot.

Local Clock – The PCI 9054 POM1 Local bus clock uses the supplied clock from the IOP 480 POM1 connector. The PCI 9054 operates up to 50Mhz on the Local bus. Therefore, the IOP 480 RDK Local bus clock (oscillator) must be changed from 60MHz to 50MHz.

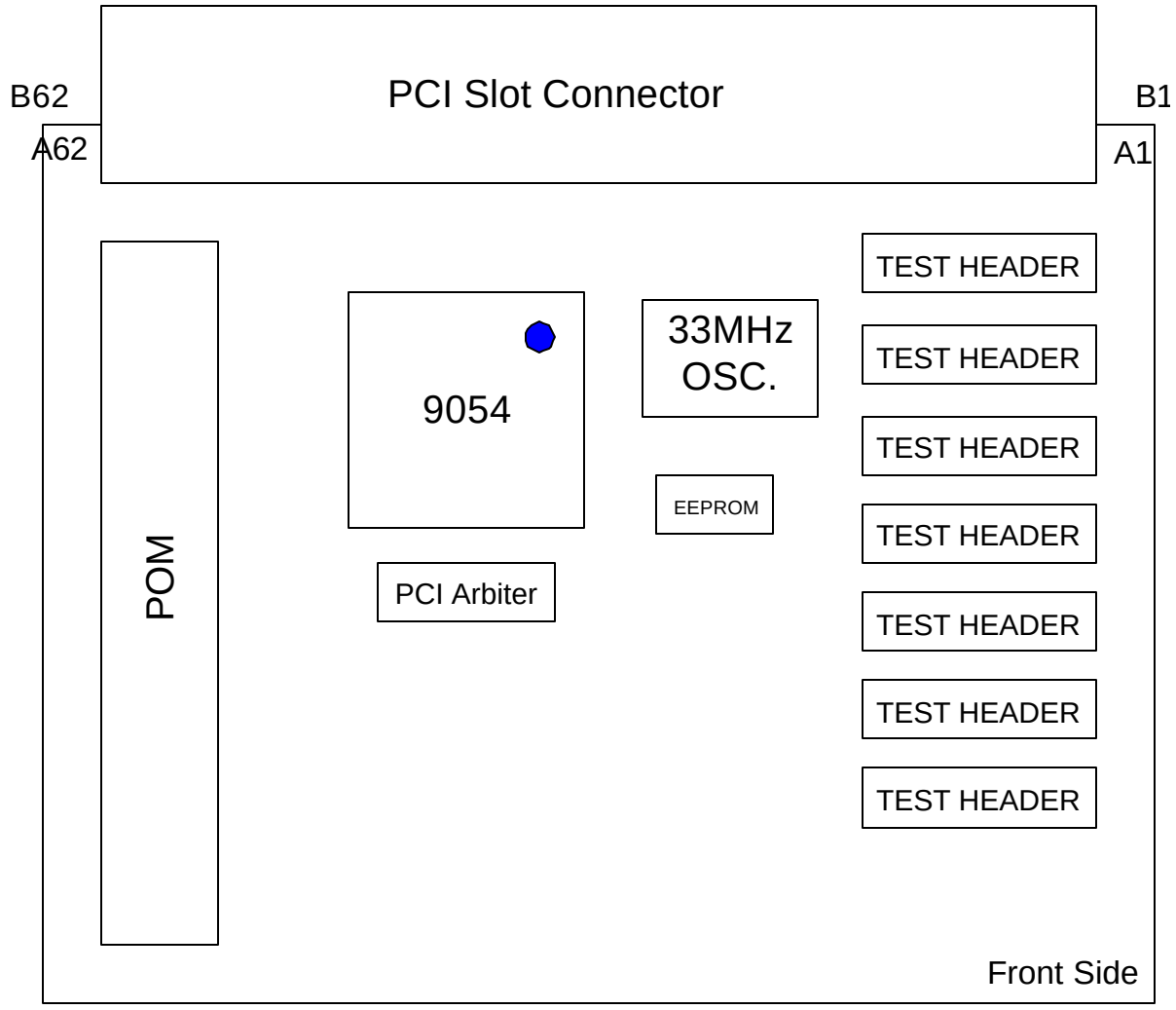
6. PCI ARBITER

The PCI 9054 POM1 PCI arbiter supports two PCI masters with a fixed priority. The arbiter receives two request inputs, REQ1# and REQ2#. One request is from the PCI 9054 and the other is from the PCI slot. It grants the bus to the PCI 9054 (GNT1#) when both REQ1# and REQ2# asserts at the same time. Therefore, the PCI 9054 has a higher priority than the PCI slot adapter. Three 2-Input NAND Gate Tiny Logic from Fairchild NC7SZ00 was used to implement the PCI arbiter. This Tiny Ultra-High Speed series has a propagation delay of 2.2ns. The PCI bus is parked on the PCI 9054 POM1.

Table 1. Arbiter Truth Table

REQ1#	REQ2#	GNT1#	GNT2#
1	0	1	0
0	1	0	1
0	0	0	1
1	1	0	1

7. PCI 9054 POM1 BOARD LAYOUT

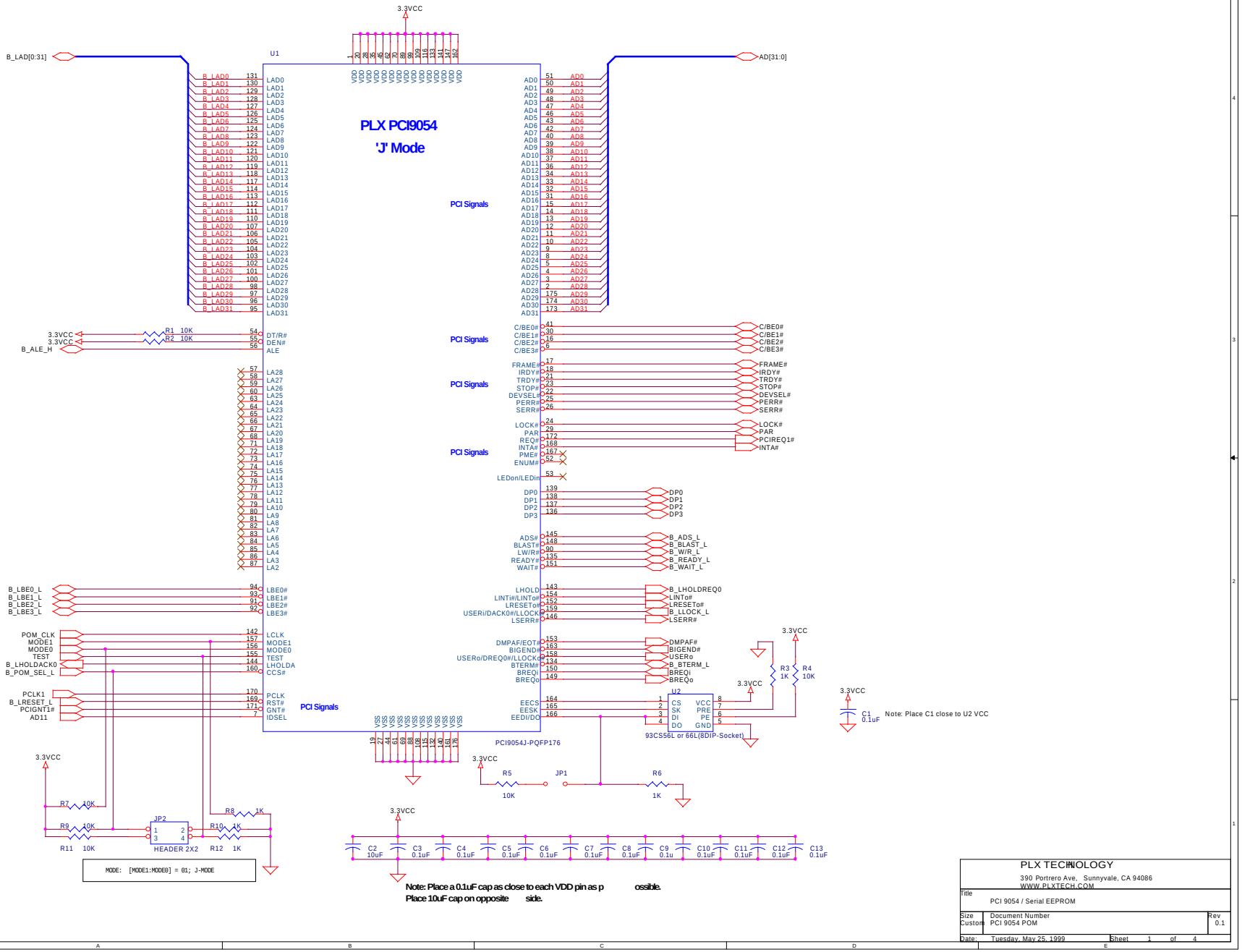


8. JUMPERS

Jumper #	Jumper Location	Description
JP1	1-2 Open (Default)	CCS# Pull-high
	1-2 Short	CCS# Pull-low ; Remove R9
	3-4 Open (Default)	Normal Operation
	3-4 Short	Test Mode ; Remove R12
JP2	Open (Default)	EEDI/EEDO Pull-down
	Short	EEDI/EEDO Pull-up ; Remove R6

9. BILL OF MATERIALS / SCHEMATICS

Item #	Qty	Part Reference	Value	Description	Mfgr.	Mfgr. P/N
1	1	U1	PCI 9054 (PQFP)	PLX PCI 9054 Bridge Chip	PLX	PCI 9054C-PQFP176
2	1	U2	93CS56L	2 kilobit serial eeprom	National	NM93CS56 LZN
3	3	U3, U4, U5	NC7SZ00	2-Input NAND Gate Tiny Logic	Fairchild	NC7SZ00M 5X
4	1	U6	CY2305	3.3V Zero Delay Buffer	Cypress	CY2305SC -1
5	3	U7	33.33 MHz OSC.	33.33 MHz 3.3V SM Oscillator	MTRON	M213TAN3 3.33
6	1	U8	NC7SZD38 4P5	1-bit bus Switch	Fairchild	NC7SZD38 4P5
7	1	JP1	2X2 Pin Jumper	4 Pins Dual-Row .1" Unshrouded Header	Molex	
8	1	JP2	2X1 Pin Jumper	2 Pins Single Row .1" Unshrouded Header	Molex	
9	1	J1		PCI 5V 32-bit PCI Card Edge Connectors 0.05in	FCI	CEE2X60S MV3Z14W
10	1	J2		POM1		
11	7	J3, J4, J5, J6, J7, J8	10X2 Pin Header	20 Pins Dual Row .1" Unshrouded Header	Molex	
12	18	C1-C12, C17-C20, C26, C27	0.1uF	50V 0.1uF 20% Capacitor –size 0805	Kemet	C0805C10 4M5UAC
13	1	C21	0.01uF	50V 0.01uF 20% Capacitor –size 0805	Kemet	C0805C10 3M5UAC
14	8	C13-C16, C22-C25	10uF	20V 10uF Tantalum Capacitor Ccase	Panasonic	AEC-T1DC106R
15	1	L1	E400R Ferrite			
16	8	R1, R2, R4, R6, R8, R10, R12, R14	10K	10K ohm 1/10W 5% Resistor – 0805 size	Philips	RC11J10K 0
17	5	R3, R5, R7, R9, R11, R13	1K	1K ohm 1/10W 5% Resistor – 0805 size	Philips	RC11J1K0 0
18	5	R15-R19	33	33 ohm 1/10W 5% Resistor – 0805 size	Philips	RC11J33K 0
19	1	R20	110	110 ohm 1/10W 5% Resistor 0805 size	Philips	RC11J110 R1
20	6	RN1-RN6	10K	10K ohm Dual-Row Resistor network	Philips	
21	1	D1	Green-LED	Green LED	HP	HSMG-C650


PLX PCI9054
'J' Mode
U1
3.3VCC
B_LAD[0:31]
AD[31:0]
PCI Signals
PCI9054J-PQFP176
93CS56L or 66L(8DIP-Socket)
HEADER 2X2
MODE: [MODE1:MODE0] = 01; J-MODE
Note: Place C1 close to U2 VCC
Note: Place a 0.1uF cap as close to each VDD pin as p ossible.
Place 10uF cap on opposite side.
PLX TECHNOLOGY
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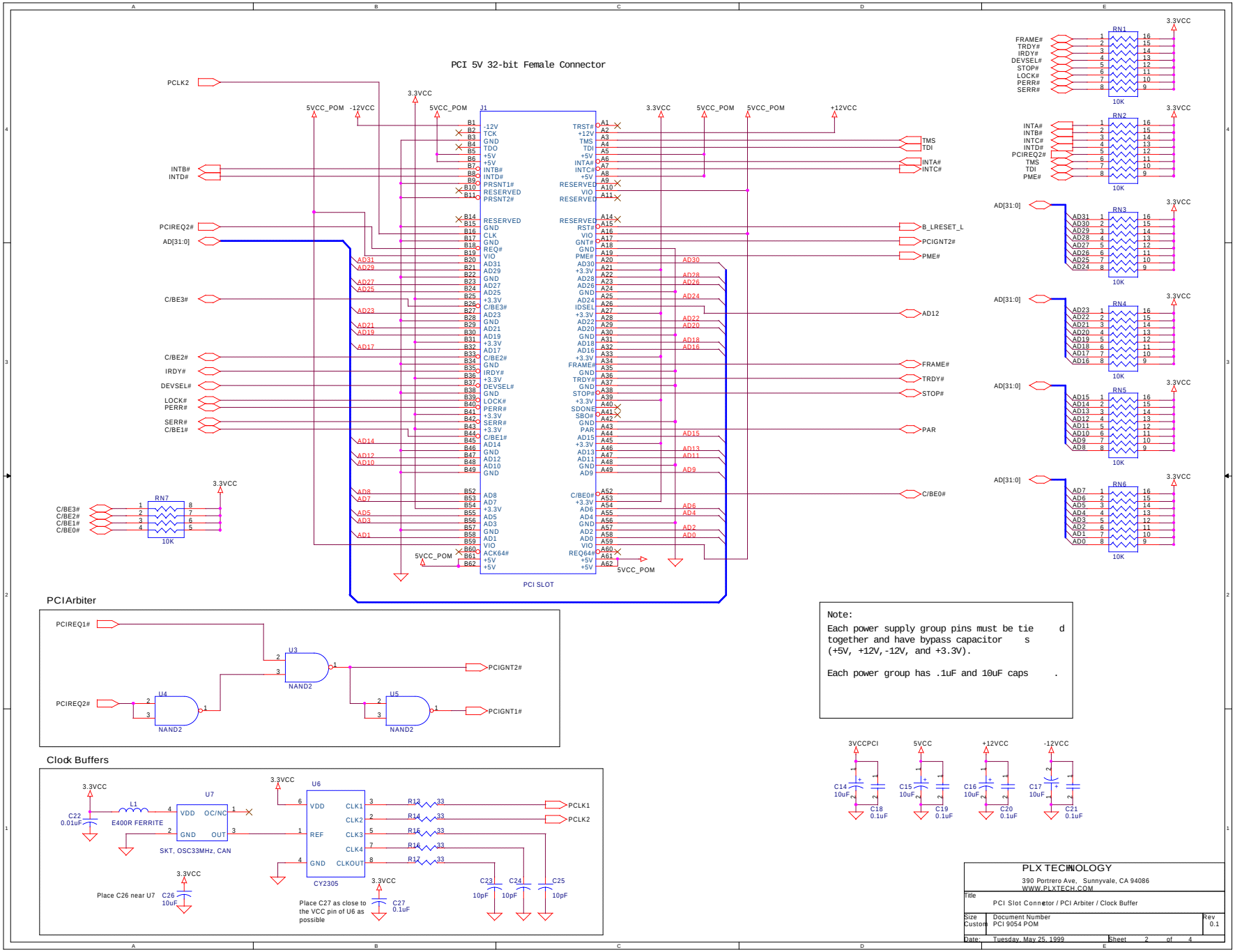
Title
PCI 9054 / Serial EEPROM
Size
Custom
Document Number
PCI 9054 POM
Rev
0.1
Date:
Tuesday, May 25, 1999
Sheet 1 of 4


PCI 5V 32-bit Female Connector
PCI SLOT
PCIArbiter
Clock Buffers
Note:
Each power supply group pins must be tied together and have bypass capacitors (+5V, +12V, -12V, and +3.3V).
Each power group has .1uF and 10uF caps.
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WWW.PLXTECH.COM
Title
PCI Slot Connector / PCI Arbiter / Clock Buffer
Size
Custom
Document Number
PCI 9054 POM
Rev
0.1
Date:
Tuesday, May 25, 1999
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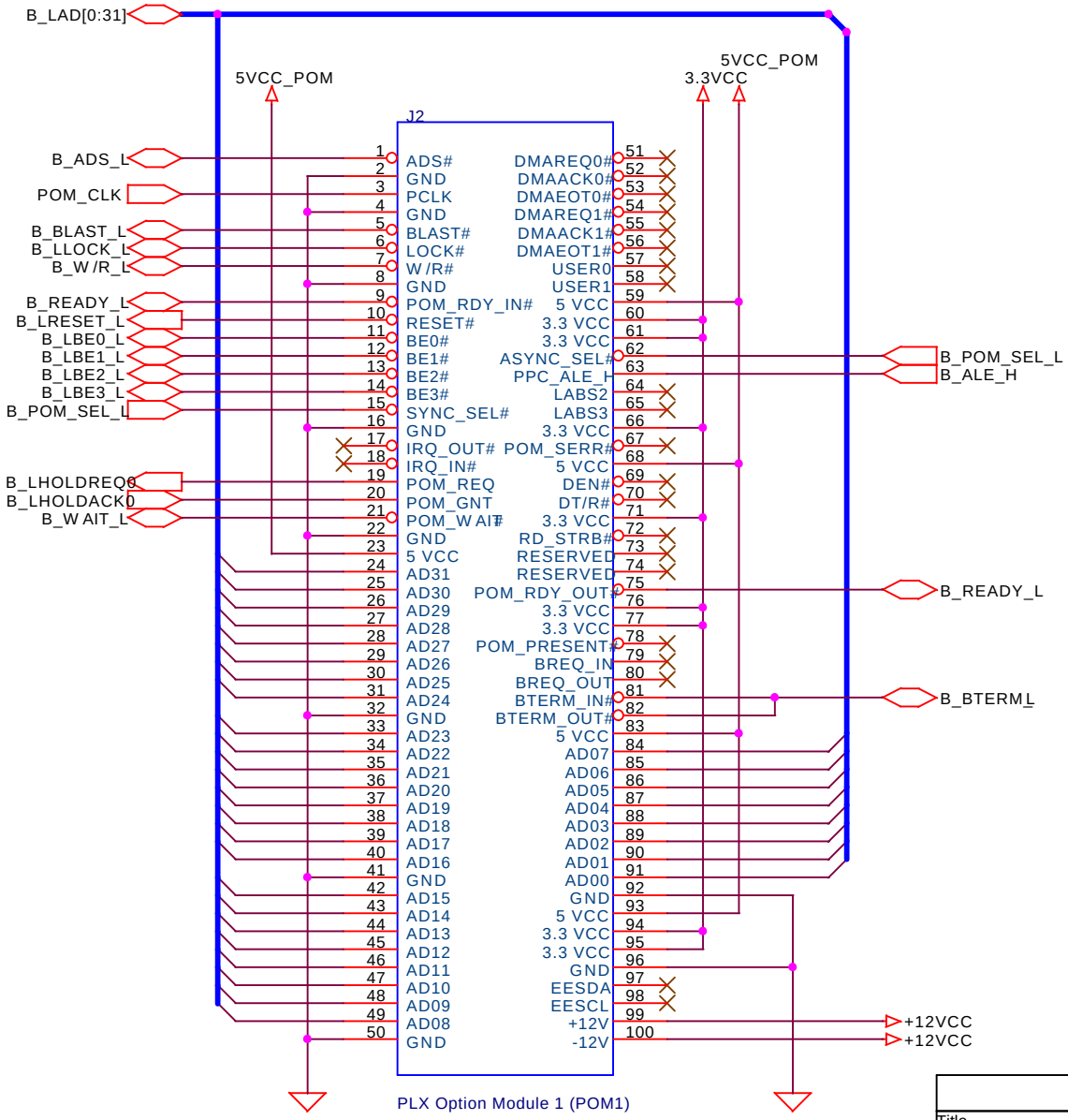

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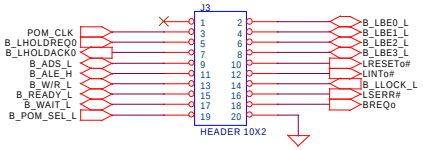
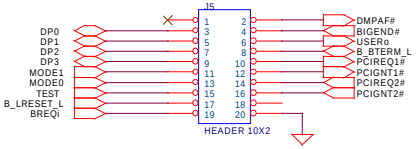
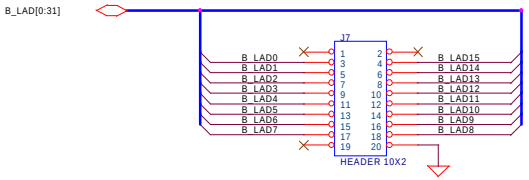
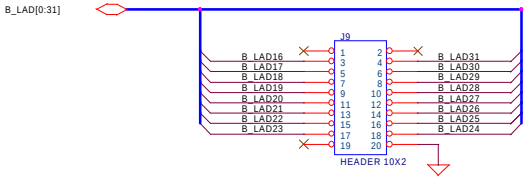
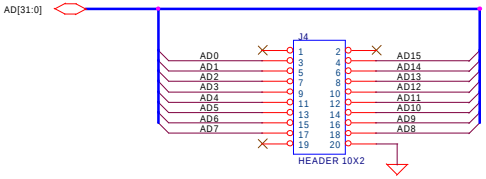
Size A	Document Number PCI 9054 POM	Rev 0.1
Date: Tuesday, May 25, 1999	Sheet 3 of 4	

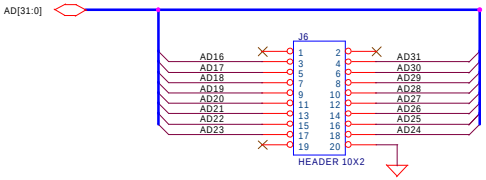


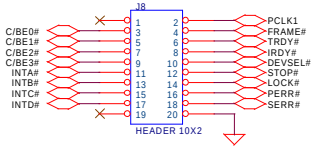




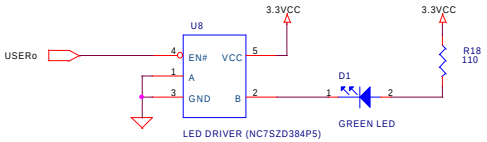


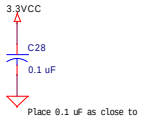






Debug LED





Place 0.1 uF as close to the VCC pin of LED driver as possible.

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