PCI 9054RDK-LITE
Hardware Reference Manual

Version 1.0

October 1999

Website: http://www.plxtech.com
Email: apps@plxtech.com
Phone: 408-774-9060
FAX: 408-774-2169

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About This Manual

This document describes the PLX PCI 9054RDK-LITE Reference Design Kit from a hardware perspective. It contains description of all major functional circuit blocks on board and also is a reference for the creation of software for this product. This manual also includes the complete schematics and bill of materials.

Document Information

Update History

Version	Date	Comments
Red Book	June 1999	First Version
Blue Book	September 1999	• Revised BOM and Schematics • Added CPLD Verilog Code Section • Other minor changes
Hardware Reference Manual	October 1999	• Added examples of using PLXMon 99 • Added RDK installation

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Order Number: 9054/LITE-RDK-HRM-P0-1.0

Printed in the USA 10/99

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1. General Information

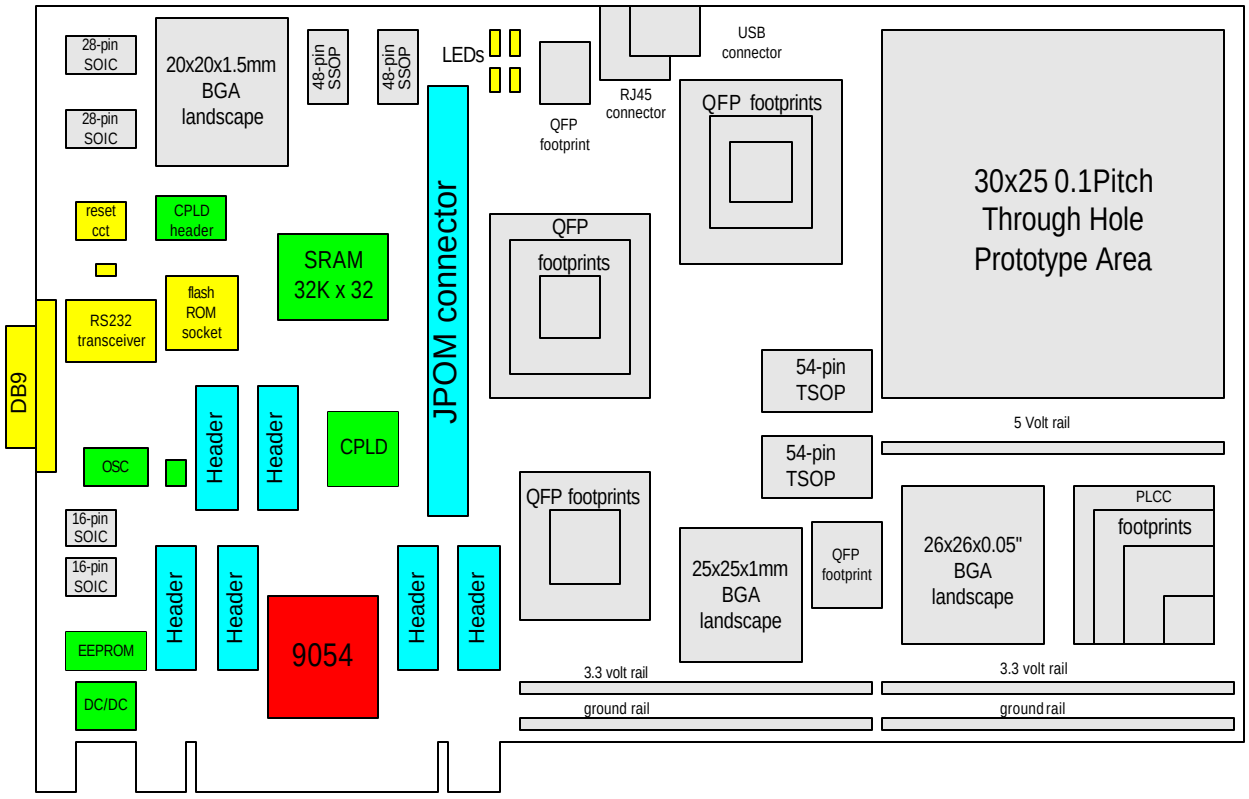


Figure 1-1. PCI 9054RDK-LITE Layout Diagram

The PCI 9054 RDK-LITE is a PCI prototyping kit targeting custom designs. It allows customers to create designs with either no microprocessor or one different from other RDKs offered by PLX.

1.1 Features

The PCI 9054RDK-LITE Reference Design Kit (RDK) is a PCI Bus Master Prototyping Kit, which contains a four-layer, assembled PC board with dimensions of 12.28"L x 5.20"W and the following features:

- PLX PCI 9054 PCI I/O Accelerator in 176-pin PQFP package
- Socketed serial EEPROM for configuring PCI 9054
- Support for all three bus modes (C, J and M modes)
- Thirty (30) surface mount prototyping footprints and three (3) common pitch BGA landscapes, which can be used with different packages of microprocessors, DSPs, FPGAs, CPLDs, SDRAMs, SRAMs, data transceivers, and general purpose logic devices
- Socketed 32-pin PLCC footprint provides designers a place for their flash boot ROM
- On-board 32K x 32 synchronous SRAM plus CPLD Memory Controller demonstrating PCI 9054 Data Pipe Architecture for both C and J modes. It allows the user to plug the board into a PCI system and be operational immediately
- Four (4) user defined status/debug LEDs
- In-system programmable CPLD with equations in Verilog provide chip selects, Local bus arbiter, and SRAM control.
- Built-in DB9 connector and programmable DTE/DCE RS232 transceiver for easy addition of a serial port
- A push button switch and a reset generator is capable of generating reset signals to any device on the board.
- Socketed oscillator for Local bus clock and PLL provide up to 50MHz clock to the Local bus.
- 5V to 3.3V voltage regulator to enable card to plug into 5 volt only PCI slot
- Six logic analyzer headers with standard HP footprint to allow easy probing of Local bus signals.
- Footprints of RJ45 connector and type A USB connector provide additional connections for customer prototyping.
- PLX J-Bus Option Module (POM) connector provides connection to other PLX POMs or customer devices
- A 25x30 0.1” grid through hole area allows easy prototyping with through hole components

1.2 RDK Installation

- Turn-off the computer and open the computer case
- Plug the PCI 9054RDK-LITE board into one of the PCI slots
- Close the computer case and turn on the computer

2. System Architecture

As shown in Figure 2-1, the RDK board contains

- PCI 9054 PCI I/O Accelerator
- Four components (CPLD, SRAM, Test Headers, and JPOM connector) connected to the PCI 9054 Local bus
- Four commonly used hardware modules (LEDs, Flash ROM Socket, Reset Circuitry, and RS232 Interface)
- More than 75% of the board area containing many carefully selected prototyping footprints.

The RDK is shipped with C mode as the default. Once the board is correctly installed into a PC computer system, the PCI master, such as the Intel microprocessor in the PC motherboard, can perform single memory read/write cycles, multiple memory read/write cycles, and continuous burst memory read/write cycles from/to the on-board synchronous SRAM in direct slave mode.

Four hardware modules on the RDK provide some basic hardware building blocks for almost any PCI 9054 design.

The thirty (30) surface mount footprints, and three (3) BGA landscapes support industry leading 16-bit and 32-bit embedded processors and DSPs from Hitachi, Motorola, IDT, TI, IBM and Analog Devices. Also, the PLCC footprints and PQFP footprints cover various common packages of CPLDs and FPGAs and PLX chips such as PCI 9054 and IOP 480.

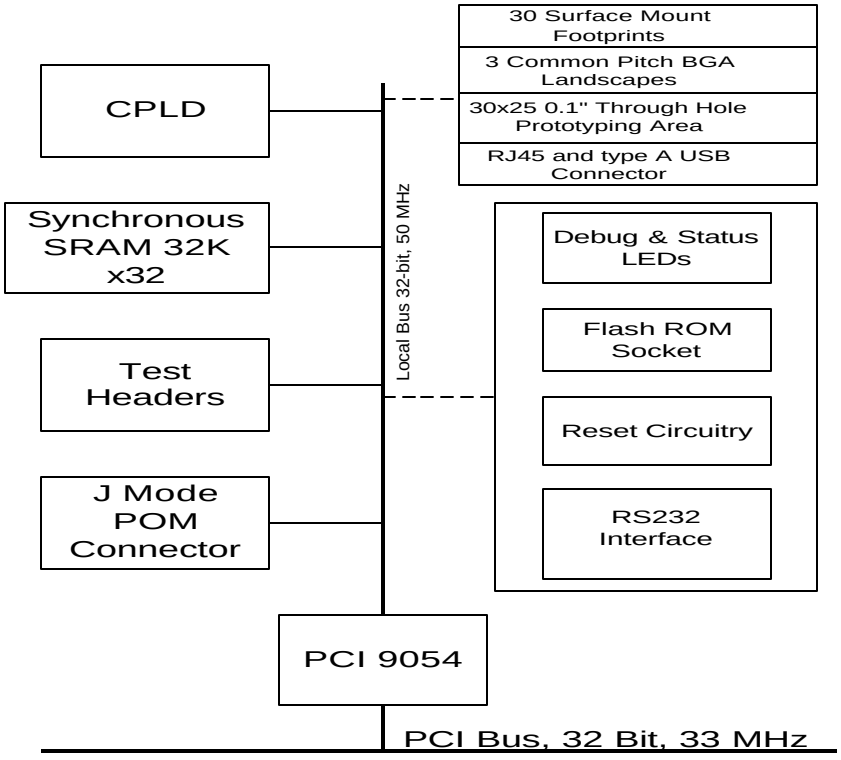


Figure 2-1. PCI 9054RDK-LITE System Architecture

3. Hardware Architecture

This section provides a detailed description of the hardware of the PCI 9054RDK-LITE. Figure 3-1 shows the hardware block diagram of the RDK.

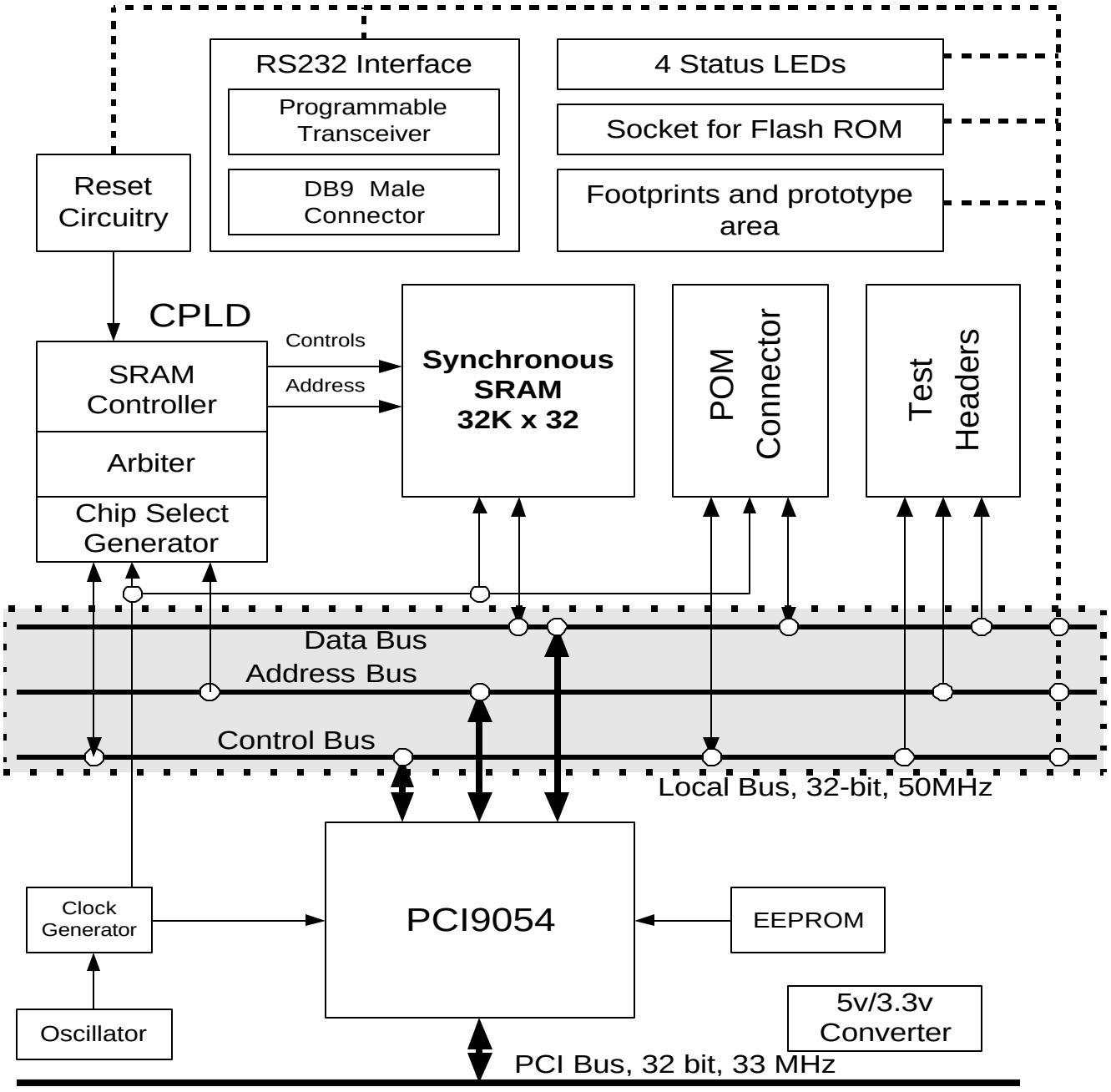


Figure 3-1. PCI 9054RDK-LITE Hardware Block Diagram

3.1 Hardware Memory Map

The following is the memory map of the PCI 9054RDK-LITE board.

Table 3-1. PCI 9054RDK-LITE Memory Map

Address Range	Device	Chip Select	Comments
FFFF FFFF 8000 0000	Unused	_	Available
7FFF FFFF 7000 0000	Unused	CS3#	Available & Re-programmable
6FFF FFFF 6000 0000	Unused	CS2#	Available & Re-programmable
5FFF FFFF 5000 0000	Unused	CS1#	Available & Re-programmable
4FFF FFFF 4000 0000	J mode POM connector	CS0#	32-bit, multiplexed address/data bus
3FFF FFFF 2002 0000	Unused	_	_
2001 FFFF 2000 0000	Synchronous SRAM 32K x 32	SRAMCS#	8, 16, 32-bit access
1FFF FFFF 0000 0000	Unused	_	Available

3.2 PCI 9054

The PCI 9054, a 32-bit 33MHz PCI Bus Master I/O Accelerator, is the most advanced general-purpose PCI bus master device available in the market today. It offers a robust PCI Specification v2.2 implementation enabling burst transfers up to 132 MB per second. The PCI 9054 incorporates the industry leading PLX data Pipe Architecture technology, including dual DMA engines, programmable PCI initiator and Target Data-Transfer modes, and PCI messaging functions.

3.2.1 Dual DMA Channels

- Dual independent channels provides flexible prioritization scheme
- Direct H/W control of DMA including Demand/Block/Scatter/Gather modes
- Programmable burst length, including unlimited burst
- Shuttle Mode automatic invalidation of used DMA descriptors
- Unaligned transfer support
- End of Transfer (EOT) support
- Support for PCI bus mastering from local slave-only devices
- Scatter-Gather list management

3.2.2 PCI Initiator

- Support for all PCI cycle types including Type 0 and Type 1 configuration cycles
- Read pre-fetching
- Burst-length-control
- Programmable threshold pointer
- Unaligned transfer support
- Dynamic Endian swapping

3.2.3 PCI Target

- Multiple independent address spaces dynamic Local bus width control
- Dynamic Endian swapping
- Read pre-fetching
- Local bus priority control latency timer

3.2.4 PCI Messaging

- Complete messaging unit mailbox and doorbell registers
- Queue management pointers, which can be used for message passing under the I_2O protocol or a custom protocol

3.3 Serial EEPROM

A 2 Kbit serial EEPROM is used in this RDK. It is directly connected to the 9054 and provides the configuration data to initialize the 9054 after the system reset. 86 bytes of configuration data are pre-programmed to the serial EEPROM. They include device and functional information for plug-and-play (PnP), PCI memory resource allocation and initial values of internal registers.

3.3.1 Contents in the Serial EEPROM

Table 3-2. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Value	Description	Register Bits Affected
0h	5406	Device ID	PCIIDR[31:16]
2h	10B5	Vendor ID	PCIIDR[15:0]
4h	0680	Class Code	PCICCR[23:8]
6h	000B	Class Code, Revision	PCICCR[7:0] / PCIREV[7:0]
8h	0000	Maximum Latency, Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	0100	Interrupt Pin, Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	0000	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	0000	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	0000	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	0000	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	FF00	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	0000	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	0000	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	0101	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	000C	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	0030	MSW of Local Bus Big/Little Endian Descriptor	PROT_AREA [15:0]
22h	5500	LSW of Local Bus Big/Little Endian Descriptor	LMISC [7:0] / BIGEND [7:0]
24h	0000	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	0000	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	0000	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	0010	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	8B43	MSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[31:16]
2Eh	0043	LSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[15:0]
30h	0000	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	0000	LSW of Range for Direct Master-to-PCI	DMRR[15:0]
34h	4000	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	0000	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	5000	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	0000	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	0000	MSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	0000	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMPBAM[15:0]
40h	0000	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCRGA[31:16]
42h	0000	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

Table 3-3. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Value	Description	Register Bits Affected
44h	9054	Subsystem ID	PCISID[15:0]
46h	10B5	Subsystem Vendor ID	PCISVID[15:0]
48h	FFFE	MSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[31:16]
4Ah	0000	LSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[15:0]
4Ch	2000	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	0000	MSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[31:16]
52h	0143	LSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[15:0]
54h	0000	MSW of Hot Swap Control Register	Reserved
56h	4C06	LSW of Hot Swap Control Register	HS_NEXT[7:0] / HS_CNTL[7:0]

3.4 Synchronous SRAM

A 100-pin 7.5ns 32K x 32 Micron SyncBurst SRAM is used as data storage in the RDK. It is used for demonstration of continuous burst cycles from the PCI 9054 chip. It takes 16 address lines (SA16-SA2) from the SRAM controller implemented in the Altera CPLD. The data lines of the SRAM are directly connected to the PCI 9054 local data bus (LD31-LD0). During memory burst cycles, the SRAM performs continuous single read cycles or single write cycles. The SRAM controller does all the timing conversion and generates the address to the SRAM.

3.5 Altera CPLD

The CPLD used in this RDK is a 4ns Altera EPM7064AE device. Referring to Figure 3-1, PCI 9054RDK-LITE hardware diagram, there are three functional blocks inside the CPLD: SRAM controller, external arbiter and chip select generator. During memory cycles, the SRAM controller generates all control signals, SRAM chip select (SRAMCS#), SRAM output enable (SRAMOE#), and SRAM byte write enables (SRAM_BW_(0:3)) to the Synchronous SRAM. During burst memory cycles, the SRAM controller will latch the starting address signals and use its built-in internal address counter to advance the addresses to the synchronous SRAM. On the PCI 9054 side, the SRAM controller would generate the active low ready signal (READY#) to terminate PCI 9054 memory cycles.

The external arbiter in the CPLD accepts two Local bus request signals, (LBR[1:0]), and the bus request from PCI 9054 (LHOLD) and generates bus grant signals, LBG[1:0], to the Local bus masters and LHOLDA to PCI 9054 chip.

Also, the built-in chip select generator in the CPLD provides four active-low chip select signals to the devices on the Local bus besides the chip select (SRAMCS#) to the synchronous SRAM. The chip select signals are partially decoded from the upper most four address lines (LA31-LA28) on the Local bus. They can be re-programmed by altering the Verilog code in the CPLD.

3.6 Test Headers

Six logic analyzer headers are implemented with standard 0.1", 2x10 headers. In this RDK, they serve two different functions. One is for easy probing. All PCI 9054 Local bus signals, configuration and status signals are well arranged with these headers. Headers LAH1 and LAH2 contain Local bus address signals. Headers LAH3 and LAH4 contain Local bus data signals (or multiplexed address/data signals in J mode). Headers LAH5 and LAH6 carry Local bus control and status signals. Second, these headers are centered on 0.1" grid spacing. Designers can use these headers to connect to a standard prototyping board for additional prototyping. The headers do not provide any power source; therefore this must be connected separately for protoyping daughterboards.

3.7 PLX Option Module Connector

The PLX Option Module Connector resides directly on the 32-bit multiplexed J mode Local Bus. Either/both a master and/or slave device may be connected to this connector, which resides at address range 4000 0000 - 4FFF FFFF. The external arbiter in the CPLD uses CS0# to select the POM module. Schematic #5 of the RDK provides information for all the signals for the 100-pin connector. If desired, this connector can be used for expansion and prototyping.

3.8 Hardware Modules

The RDK-LITE provides four hardware modules: 1) RS232 interface, 2) debug and status LEDs, 3) reset circuitry, and 4) flash ROM socket. This is in addition to the clock generator used to provide the 50MHz Local bus clock to the PCI 9054, CPLD, POM, and the Synchronous SRAM.

3.8.1 RS232 Interface

The RS232 interface circuit combines a DB9 male connector with an RS232 transceiver. The transceiver chip is made by Maxim Integrated Products and can be hardware configured or software programmed as Data Terminal Equipment (DTE) or Data Circuit Equipment (DCE).

3.8.2 Debug and Status LEDs

There are four green user-defined LEDs near the top edge of the RDK board. The anode of each LED is connected to 3.3VDC through a 150-ohm ¼ watt resistor. The cathode of the LED is connected to a prototyping pad for customer use. As long as an active low signal can sink 16 – 20 mA of current, it can directly drive the LEDs without changing the resistor value.

3.8.3 Reset Circuitry

3.8.3.1 Power-on-Reset

Power-on-reset is controlled by an external 3.3-Volt power supply supervisor. The valid power-on-reset period is 1ms, which is hardwired into the supply supervisor IC.

3.8.3.2 Reset Pushbutton Switch

The Reset Pushbutton switch allows the user to reset the Local Bus side of the board only. When this pushbutton switch is pressed, a manual reset can be generated to reset the devices on the PCI 9054 Local bus.

3.8.4 Flash ROM Socket

A 32-pin PLCC footprint and related PLCC socket are provided on the RDK. It can be used to install a 3.3 volt 512KB byte wide flash memory device. It can be used to store the firmware for booting Local bus master device such as microprocessors or DSPs. The flash ROM footprint is pre-connected to power and ground. The prototyping pads are provided for all control signal pins as well as all address and data lines.

3.9 Prototyping Area

The RDK board contains a huge prototyping area as mentioned before. To make the prototyping area more user friendly and cost effective, three key features are implemented. The first is 30+ surface mount footprints, the second is three common BGA landscapes and the last is a 30x25 0.1” grid through-hole prototyping area.

3.9.1 Thirty (30) Surface Mount Footprints

As shown in Table 3-4, the surface-mount footprints are carefully selected based on three factors.

1) The footprints can be used for industry leading embedded microprocessors and DSPs from PLX Technology, Hitachi, Motorola, IBM, TI, and Analog Devices.

2) The footprints are the common footprints for CPLDs and FPGAs in the current market.

3) If the designer wants to build a complex design on the Local bus, there are enough footprints for CPU, memory, programmable control logic, bus transceivers and discrete devices.

Package	Quantity	Pin Pitch	Examples of Applications
16-pin SOIC	2	0.05"	Discrete Logic
28-pin SOIC	2	0.05"	Discrete Logic
28-pin PLCC	3	0.05"	PALs
44-pin PLCC	1	0.05"	CPLDs
44-pin PQFP	2	0.8mm	CPLDs
48-pin SSOP	2	0.025"	Discrete Logic, data transceivers
54-pin TSOP	2	0.8mm	SDRAM, SRAM
68-pin PLCC	1	0.05"	CPLD, ADS-2104L
80-pin PQFP	2	0.5mm	PPC401GF,
84-pin PLCC	1	0.05"	CPLDs,MIPS CPUs, PPC401GF,
100-pin PQFP	2	0.5mm	CPLDs,TI 320C2602/C541/LC541/LC543/LC546, ADSP-2186L
112-pin PQFP	1	0.65mm	SH7032/7034/7040,
128-pin PQFP	1	0.4mm	TI 320C6202/LC542/545
144-pin PQFP	2	0.5mm	CPLDs, TI C542/KC542/LC548/LC549/VC549, SH7604, IDT RC32364
160-pin PQFP	1	0.65mm	FPGAs, PPC403GA, MCF5206e,
176-pin PQFP	2	0.5mm	SH7410,
208-pin PQFP	2	0.5mm	FPGAs,SH7707/7709/7750, ADSP 20165L
240-pin PQFP	1	0.5mm	FPGAs, ADSP 21061L/21062L
BGA (26x26)	1	0.05"	PMC801/821/823/850
BGA (20x20)	1	1.5mm	PCI 9054, IOP480
BGA (25x25)	1	1.0mm	PPC403GC/GCX, TI 320C6202

Table 3-4. Thirty (30) Surface Mount Footprints

3.10 Power Supply

All electronic devices on the RDK, except U7, the programmable RS232 transceiver, are 3.3V devices. The RDK uses a LDO regulator to convert the 5 VDC to 3.3 VDC for those devices. As long as the output current from the voltage converter remains less than 2A, the RDK board can work without any problem.

3.10.1 Three Common BGA Landscapes

This RDK provides three common pitch BGA landscapes in the prototyping area. BGA1 is a full matrix of 20x20 @ 1.5mm pitch with the plated hole size of 0.022" dia. +/-0.001". The BGA landscape labeled BGA2 is a full matrix of 26x26 @ 0.05" pitch with the same size of plated hole as BGA1. The BGA landscape labeled BGA3 is a full matrix of 25x25 @1.0mm pitch holes with the plated hole size of 0.0165" dia. +/-0.001".

We suggest using Ironwood Electronics (web site: www.ironwoodelectronics.com) BGA Land Sockets and/or Minigrid Sockets, designers can convert BGA to PGA and prototype BGA chip on this RDK.

Refer to Figure 3-2, if designers use either the BGA1 or BGA2 landscape, they can choose either a) or b) below:

a)

1. Buy both the Minigrid Socket and BGA Land Socket from Ironwood Electronics.
2. Solder the Minigrid Socket to the PC board.
3. Solder the BGA device to the Land Socket and plug the Land Socket to the Minigrid Socket.

b)

1. Buy only BGA Land Sockets from Ironwood Electronics.
2. Solder the BGA device on the top of the Land Socket and solder the Land Socket to the PC board.

If a designer uses the BGA3 landscape, they have only one choice; * to buy Ironwood's BGA Land Socket. Solder the BGA on the top of the Land Socket and solder the Land Socket to the PC board.

Note: The hole size on BGA3 is 0.0165" in diameter. It only fits with the Land Socket because the pin of Land Socket is 0.014" in diameter. Do not force the pin in the hole. It should fit snugly.

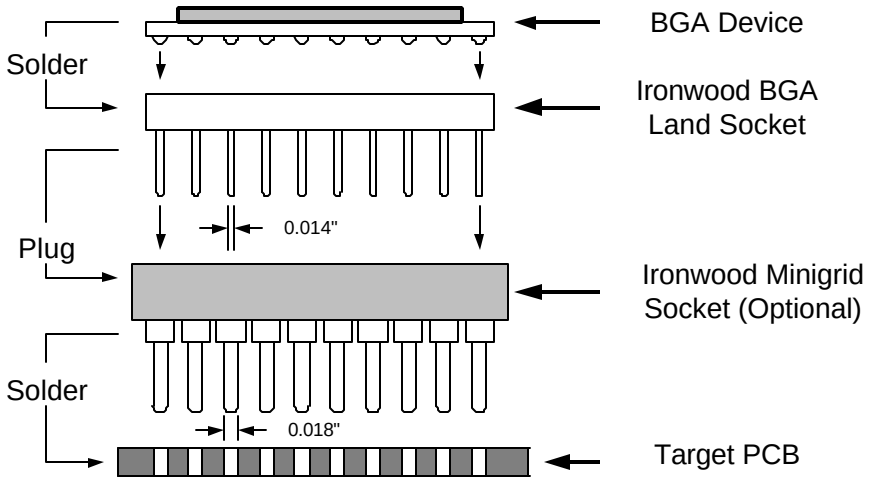


Figure 3-2. BGA Landscapes

3.11 Configuring the RDK board

Table 3-5. PCI 9054 Mode Setting

mode C	install R3, R4, R27, R28, R29, R30 and R26
mode J	install R1, R4, R27, R28, R29, R30 and R26
mode M	install R1, R2, R22, R23, R24, R25 and R31

4. Examples of Testing the On Board 32Kx32 SRAM with PLXMon 99

1) Single read/write from / to on board SRAM:

   a) At the lower command line window of PLXMon99, type in the following commands to perform single 32bit, 16bit and 8bit memory read/write from/to the on board SRAM.

dl s0 1
<= read a 32-bit long word from address s0

el s0 88888888
<= write 32-bit data, 88888888h, to address s0

dw s0 1
<= read a 16-bit word from address s0

ew s0 8888
<= write 16-bit data, 8888h, to address s0

db s0 1
<= read a byte from address s0

eb s0 88
<= write 8-bit data, 88h, to address s0

2) DMA burst read/write from/to on board SRAM:

   a) At lower pane of the PLXMon 99, type **Vars** to obtain the addresses for HBuf, 60K-byte DMA scratch buffer located at PC's main memory. For example, assume the HBuf has physical address starting at 01F80000h.

   b) Enter 8 long word test data to the SRAM. For example,

el s0	11111111
el s0+4	22222222
el s0+8	33333333
el s0+c	44444444
el s0+10	55555555
el s0+14	66666666
el s0+18	77777777
el s0+1c	88888888

   c) Click the DMA button on PLXMon 99 to open DMA registers window.

d) Configure DMA CH0 for burst transfer and the transfer direction is from local to PCI. The settings on DMA channel 0 would be similar to the following:

Mode (80h):	143
PCI address (84h):	**01F80000**
Local address (88h):	20000000
Transfer size (8ch):	100
Descriptor pointer (90h):	8

Check the box for data transfer enable

e) Click on [Start Transfer] button to transfer data from on Board SRAM to DMA scratch buffer.

f) Compare the data at step 'b' by typing in **dl HBuf** commend.

g) Change the contents at DMA scratch buffer

el HBuf	99999999
el HBuf+4	88888888
el HBuf+8	77777777
el HBuf+c	66666666
el HBuf+10	55555555
el HBuf+14	44444444
el HBuf +18	33333333
el HBuf+1c	22222222

h) Change the direction of DMA transfer from PCI to local at DMA CH0 by modifying descriptor pointer (90h) from zero to 0.

i) Click on [Start Transfer] button to perform DMA transfer again

j) Type in **dl s0** to compare the data at step G.

5. CPLD Verilog Code

```
====================================
8/12/99

Synchronous SRAM controller for PLX PCI 9054
mode C and J.  128K byte (32K x 32 bit)
synchronous SRAM is used.  The memory map for
the sync. SRAM is 2000_0000 - 2001_FFFFh.  A
partial memory decode is used. The decode is only
involved address lines A31 to A28 (or A31-A29 and
LD28 in J mode)

====================================

module SRAMCTR
  (
  // local bus signals

  CLK_50MHZ,     // clock to PCI9054, SRAM and
                 controller
  ADS_,          // address strobe from 9054
  BLAST_,        // burst last from 9054
  LBE_,          // byte enable from 9054
  LWDRD_,        // local bus read/write
  ADDR_IN,       // local bus address inputs
  ADDR_4MSBS,    // local bus address A31 - A28
  READY_,        // ready signal to PLX PCI9054

  // address and control signals to synchronous
  SRAM

  SRAM_ADDR,     // address outputs to the sync.
                 SRAM
  SRAMCS_,       // chip select to the SRAM
  SRAMOE_,       // output enable to the SRAM
  SRAM_BW_,      // byte enables in SRAM write
                 cycle

  //bus arbitration

  LHOLD,         // bus hold request from PLX
                 PCI9054
  LHOLDA,        // bus hold acknowledge
  LBR,           // two local bus request
  LBG,           // two local bus grant

  // chip selects

  CS_            // four chip select outputs

  ) ;

  // port declarations

  output         READY_;
```

```
output  [16:2]     SRAM_ADDR;
output             SRAMCS_;
output             SRAMOE_;
output  [3:0]      SRAM_BW_;
output             LHOLDA;
output  [1:0]      LBG;
output  [3:0]      CS_;

input              CLK_50MHZ;
input              ADS_, BLAST_;
input   [3:0]      LBE_;
input              LWDRD_;
input   [16:2]     ADDR_IN;
input   [31:28]    ADDR_4MSBS;
input              LHOLD;
input   [1:0]      LBR;

reg     [16:2]     SRAM_ADDR;
reg     [1:0]      LBG;
reg                LHOLDA;
reg                READY_;
reg                SRAMCS_;
reg                SRAMOE_;

// internal veriables

reg     [3:0]      A31_28;
reg     [2:0]      currentstate, nextstate;

// chip selects
// Four most upper address lines, A31-A28, are used
//to generate four chip select signals for the board.
//They are CS[3:0] with address as
//
//  CS_0: 4000_0000h
//  CS_1: 5000_0000h
//  CS_2: 6000_0000h
//  CS_3: 7000_0000h


wire  [3:0] CS_ =

(ADDR_4MSBS == 4'b0100) ?  4'b1110:
(ADDR_4MSBS == 4'b0101) ? 4'b1101:
(ADDR_4MSBS == 4'b0110) ? 4'b1011:
(ADDR_4MSBS == 4'b0111) ? 4'b0111: 4'b1111;

// byte enable encode for SRAM write cycles

wire [3:0] SRAM_BW_
=({LWDRD_,A31_28}=='b1_0010)
          ? LBE_[3:0] : 4'b1111;

// store the upper address LA31 - LA28

always @ (posedge CLK_50MHZ)
     if    (LHOLD & !ADS_ &
          (ADDR_4MSBS==4'b0010))
          A31_28[3:0] = ADDR_4MSBS[31:28];

     else A31_28[3:0] = A31_28;

// local bus arbitration

always @ (posedge CLK_50MHZ)
     if    (LHOLD)
          LHOLDA = LHOLD;
     else
          LHOLDA = 0;

always @ (posedge CLK_50MHZ)
     if (!LHOLD & LBR[1])
          LBG[1] = LBR[1];
     else
          LBG[1] = 0;

always @ (posedge CLK_50MHZ)
     if (!LBR[1] & LBR[0])
          LBG[0] = LBR[0];
     else
          LBG[0] = 0;


// State definition
parameter s0 = 4'b0000; // idle
parameter s1 = 4'b0001; // cycle start
parameter s2 = 4'b0010; // single cycle wait state
parameter s3 = 4'b0011; // single cycle last state
parameter s4 = 4'b0100; // burst cycle wait state
parameter s5 = 4'b0101; // burst cycle repeat state
parameter s6 = 4'b0110; // burst cycle last state

// SRAM address counter

always @ (posedge CLK_50MHZ)
     if (!ADS_)
          SRAM_ADDR[16:2] = ADDR_IN[16:2];

     else if (BLAST_ && !((currentstate == s1) &&
          LWDRD_))
          SRAM_ADDR[12:2] =
          SRAM_ADDR[12:2] +1;

     else SRAM_ADDR[16:2] =
          SRAM_ADDR[16:2];


//Next state logic

always @ (ADS_ or BLAST_ or ADDR_4MSBS)
          casex (currentstate)
```



```
s0: if (!ADS_ && (ADDR_4MSBS==4'b0010))
                nextstate = s1;
        else
                nextstate = s0;

s1: if (!BLAST_)
                nextstate = s2;
        else if (BLAST_)
                nextstate = s4;
        else nextstate = s1;

s2:     nextstate = s3;

s3: if (!ADS_)
                nextstate = s1;
        else
                nextstate = s0;

s4:             nextstate = s5;

s5: if (BLAST_)
                nextstate = s5;
        else
                nextstate = s6;

s6: if (!ADS_)
                nextstate = s1;
        else
                nextstate = s0;

endcase

//output logic

always @ (currentstate)
        casex(currentstate)

        s0: begin
                        READY_ =1;
                        SRAMCS_=1;
                        SRAMOE_=1;
                end
        s1: begin
                        READY_ =1;
                        SRAMCS_=0;
                        SRAMOE_=1;
                end
        s2:     begin
                        READY_=0;
                        SRAMCS_=0;
                        if (LWDRD_==0)
                                SRAMOE_=0;
                        else
                                SRAMOE_=1;
                end
```

```
s3:     begin
                        READY_=1;
                        SRAMCS_=1;
                        SRAMOE_=1;
                end
s4:     begin
                        READY_=0;
                        SRAMCS_=0;
                        if (LWDRD_==0)
                                SRAMOE_=0;
                        else
                                SRAMOE_=1;
                end
s5:     begin
                        READY_=0;
                        SRAMCS_=0;
                        if (LWDRD_==0)
                                SRAMOE_=0;
                        else
                                SRAMOE_=1;
                end
s6:     begin
                        READY_=1;
                        SRAMCS_=1;
                        SRAMOE_=1;
                end

endcase

always @(posedge CLK_50MHZ)
        currentstate <= nextstate;


 endmodule
```

6. Bill of Materials / Schematics

The following pages contain the bill of materials and the schematics for the PCI 9054RDK-LITE circuit board.

The PCI 9054 is available in both the 225-pin PBGA and the 176-pin PQFP packages. The schematics of PCI 9054RDK-LITE only show the 176-pin PQFP chip installed on the RDK board. The signal names of the PCI 9054 in the schematics are related to C mode of PCI 9054 device.

Table 6-1. Bill of Materials

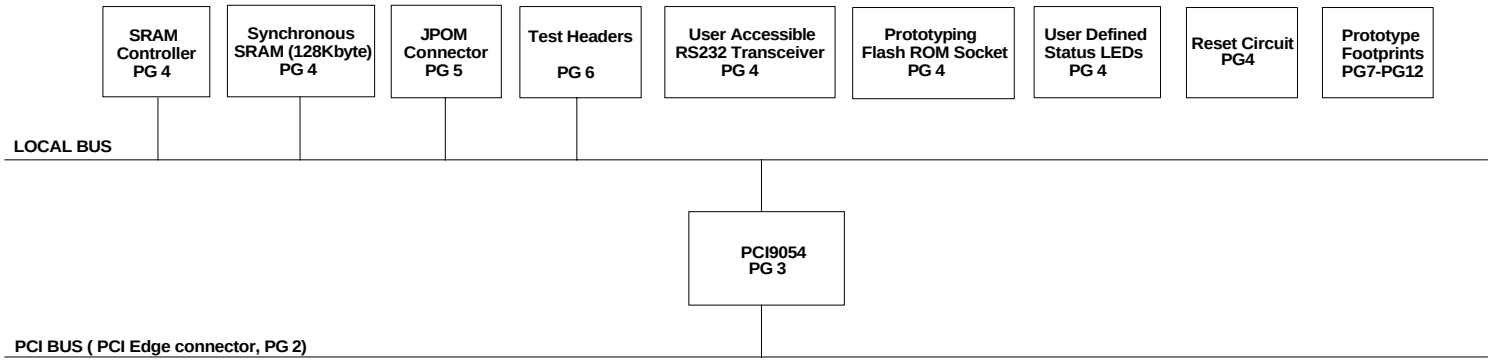
Item No.	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Source	Component Designator(s)
SURFACE MOUNT COMPONENTS							
1	1	Linear Technology	LT1587CM-3.3	IC, 3A 5V to 3.3V LDO regulator	SMT, M package, 3-lead plastic DD PAK	**Marshall	U1
2	1	PLX	PCI9054	IC, PCI I/O accelerator, 3.3V	PQFP-176	PLX	U2
3	1	Cypress	CY2305SC-1	IC, zero delay buffer, 3.3V, 250ps skew	8-pin 150-mil SOIC	FAI	U5
4	1	Altera	EPM7064AETC100-4	IC, CPLD, 64 IO-pin, 4ns delay, 3.3V	100-pin TQFP	Insight	U9
5	1	Maxim	MAX214CWI	IC, programmable DTE/DCE RS232 transceiver, 5V	28-pin wide SOP	Digi-Key	U7
6	1	Maxim	MAX6306UK30D3-T	IC, Reset Controller, 1ms reset	SOT23-5	Digi-Key	U8
7	1	Micron Technology	MT58LC32K32B3LG-8.5	IC, 1Mb Syncburst SRAM, 32Kx32, 8.5ns access time	100-pin TQFP	Marshall	U10
8	4	Hewlett Packard	HSMG-C650	LED, green, SMT	SMT, 1206	Digi-key	D1 - D4
9	1	Kycon	K20HT-E9P-N	Connector, DB9, plug	SMT	Digi-key	J2
10	1	AMP	1-104655-1	header assembly, two row 100-pin, 50 mil pitch	SMT	Electrosonic	J3
11	1	Samtec	TSM-105-01-T-DV	Terminal strip, 2x5, 0.1"oc, PCB mounted	SMT	FAI	JP1
12	6	Samtec	TSM-110-01-T-DV	Terminal strip, 2x10, 0.1"oc, PCB mounted	SMT	FAI	LAH1 - LAH6
13	1	Samtec	ICF-314-T-O	Socket, 14-pin DIP, 300mil	SMT, 14-pin DIP	FAI	U4
14	1	Samtec	ICF-308-T-O	Socket, 8-pin DIP, 300 mil, for serial EEPROM	SMT, 8-pin DIP	FAI	U6
15	1	AMP	822273-1	Socket, 32-pin PLCC	SMT, 32-pin PLCC	Digi-key	FP31
16	1	Omron	B3S1002	Switch, Push Button	SMT,	Digi-key	S1
17	5	Kemet	C0805C473M5UAC	Cap. ceramic, 0.047uF, 50V, 20%	SMT, 0805	Electrosonic	C1 - C5
18	37	Kemet	C0805C103M5UAC	Cap. ceramic, 0.01uF, 50V, 20%	SMT, 0805	Electrosonic	C6-C20,C24,C41-C45,C47-C52, C62-C65,C72-C77
19	24	Kemet	C0805C104M5UAC	Cap. ceramic, 0.1uF, 50V, 20%	SMT, 0805	Electrosonic	C22,C25,C28-C37,C39-C40, C58-C61,C66-C71
20	1	Kemet	C0805C101K5XAC	Cap. ceramic,100pF, 50V, 10%	SMT, 0805	Electrosonic	C27
21	5	Kemet	ECJ-3YB1C05K	Cap. ceramic, 1uF, 16V, 10%	SMT, 1206	Digi-Key	C53-C57
22	7	Panasonic	ECS-T1DC106R	Cap. tantalum, 10uF, 20V, Ccase	SMT, Ccase	Newark	C21,C23,C26,C78-C81

23	1	Murata	NFM40P12C223	EMI filter, 3-terminals, 0.022uF+-20%, 50VDC, 2A	SMT, 1206	**Avnet Electronics	CF1
24	1	Steward	L10805E400R	Ferrite chip, 500mA	SMT, 0805	Digi-Key	L1
25	13	CTS	742-08-3-103-J-BK	Res. Network, 10K, 5%, 4R, isolated	SMT,Ccase	Digi-Key	RN1-RN13
26	24	Panasonic	ERJ-6GEYJ0R0V	Res. 1/10W, zero ohm, 5%	SMT, 0805	Digi-Key	R3-R4,R8,R33,R39, R40,R42-R50,R65-R73
27	24	Panasonic	ERJ-6GEYJ103V	Res. 1/10W, 10K, 5%	SMT, 0805	Digi-Key	R1-R2,R5-7,R9-R10,R16-R17,R20-R23,R25-R32,R38, R41,R51
28	5	Panasonic	ERJ-6GEYJ220V	Res. 1/10W, 22 ohm, 5%	SMT, 0805	Digi-Key	R11-R15
29	2	Panasonic	ERJ-6GEYJ392V	Res. 1/10W, 3.9K, 5%	SMT, 0805	Digi_key	R24, R74
30	14	Panasonic	ERJ-6GEYJ102V	Res. 1/10W, 1K, 5%	SMT, 0805	Digi-Key	R19,R52-R64
31	1	Panasonic	ERJ-6GEYJ511V	Res. 1/10W, 510 ohm, 5%	SMT, 0805	Digi-Key	R18
32	4	Panasonic	ERJ-6GEYJ151V	Res. 1/10W, 150 ohm, 5%	SMT, 0805	Digi-Key	R34-R37
THROUGH-HOLE COMPONENTS							
33	1	AMP	520251-4	Modular jack assembly, 8 position	RJ45, PCB mounted	Digi-Key	J4
34	1	Molex	87531-0001	USB receptacle, 4 position, typeA	PCB mounted	Digi-Key	J5
MANUALLY INSERTED COMPONENTS							
35	1	Ecliptek	EP1345HSPD-50.000M	OSC, 50MHz clock oscillator, 3.3V, 50ppm, 40-60% duty cycle	8-pin half size DIP	Ecliptek	U3
36	1	National Semi.	93CS56L	IC, 2Kb serial EEPROM, 3.3V	8-pin DIP	National	U6
MISCELLANEOUS COMPONENTS							
37	1	Velostat	2100R/7X15	7" x 15" anti-static bag		FAI	BAG1
38	2		492-100	Phillips, 4-40, 1/4", PH screw (for PCB bracket)		Spaenaur	SCREW1 SCREW2
39	1		90-0006-000-A	9054RDK-LITE PCB Rev 000			
40	2	Kycon	JS-1000	Screw, Hex, Jack, 4-40		Kycon	
41	1	Keystone	CB-1095-PLX	PCI Bracket, with DB9 connector cut out		Keystone	
PARTS THAT SHOULD NOT BE ASSEMBLED							
26	6	Panasonic	ERJ-6GEYJ0R0V	Res. 1/10W, zero ohm,5%	SMT, 0805	Digi-Key	R33, R40, R43, R45, R47-48
27	8	Panasonic	ERJ-6GEYJ103V	Res. 1/10W, 10K ohm, 5%	SMT, 0805	Digi-Key	R1-R2, R6-R7, R22-R23,R25, R31
30	1	Panasonic	ERJ-6GEYJ102V	Res. 1/10W, 1K, 5%	SMT, 0805	Digi-Key	R19
42	1	Ecliptek	EP1345PD-50.000M	OSC, 50MHz clock oscillator, 3.3V, 50ppm, 40-60% duty cycle	14-pin full size DIP	Ecliptek	U4
Note 1:	Insight: (800) 677-7716						
Note 2:	Marshall Industries: 408-942-4600						
Note 3:	Avnet Electronics Marketing: 408-435-3500						
Note 4:	Rev.1: a. #19 changed Kygon to Kycon b. #32 changed NFM2012P13C104R to NFM40P12C223 (release date XX)						

PCI9054RDK-LITE BLOCK DIAGRAM

ECN HISTORY

ECN NUMBER	DATE	NOTE
001	5/3/1999	Updated BOM
002	5/17/1999	Updated schematics and BOM



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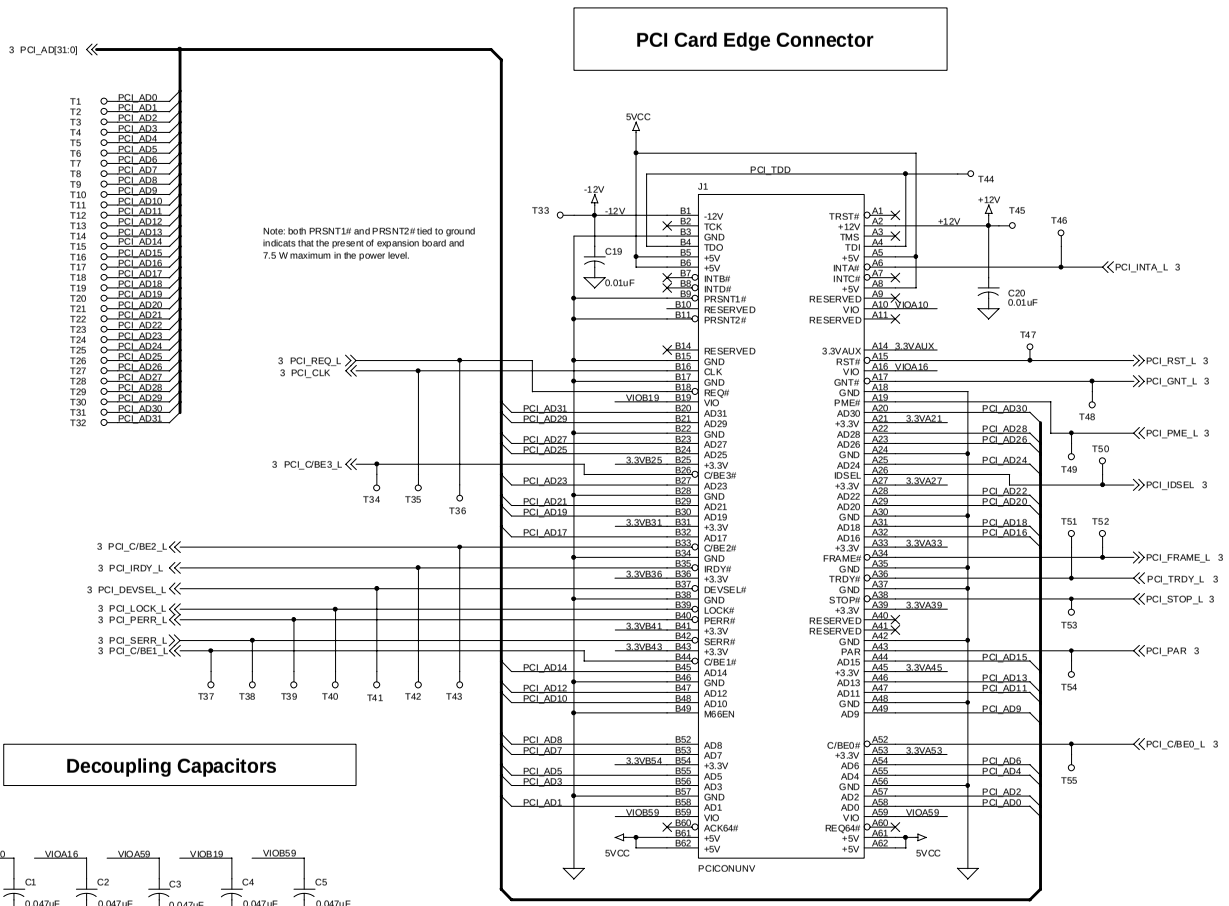
Title: **Electrical Block Diagram**

Size: Custom | Document Number: PCI9054RDK-LITE | Rev: 002

Date: Wednesday, September 01, 1999 | Sheet 1 of 13


PCI Card Edge Connector
3 PCI_AD[31:0]
Note: both PRSNT1# and PRSNT2# tied to ground indicats that the present of expansion board and 7.5 W maximum in the power level.
5VCC
PCI_TDD
-12V
+12V
J1
PCICONUNV
3 PCI_REQ_L
3 PCI_CLK
3 PCI_C/BE3_L
3 PCI_C/BE2_L
3 PCI_IRDY_L
3 PCI_DEVSEL_L
3 PCI_LOCK_L
3 PCI_PERR_L
3 PCI_SERR_L
3 PCI_C/BE1_L
PCI_INTA_L 3
PCI_RST_L 3
PCI_GNT_L 3
PCI_PME_L 3
PCI_IDSEL 3
PCI_FRAME_L 3
PCI_TRDY_L 3
PCI_STOP_L 3
PCI_PAR 3
PCI_C/BE0_L 3
Decoupling Capacitors
VIOA10
VIOA16
VIOA59
VIOB19
VIOB59
3.3VA21
3.3VA27
3.3VA33
3.3VA39
3.3VA45
3.3VA53
3.3VB25
3.3VB31
3.3VB36
3.3VB41
3.3VB43
3.3VB54
3.3VAUX
5V to 3.3V Voltage Conversion
U1
LT1587CM-3.3
VIN
VOUT
GND
2A max.
3.3VCC
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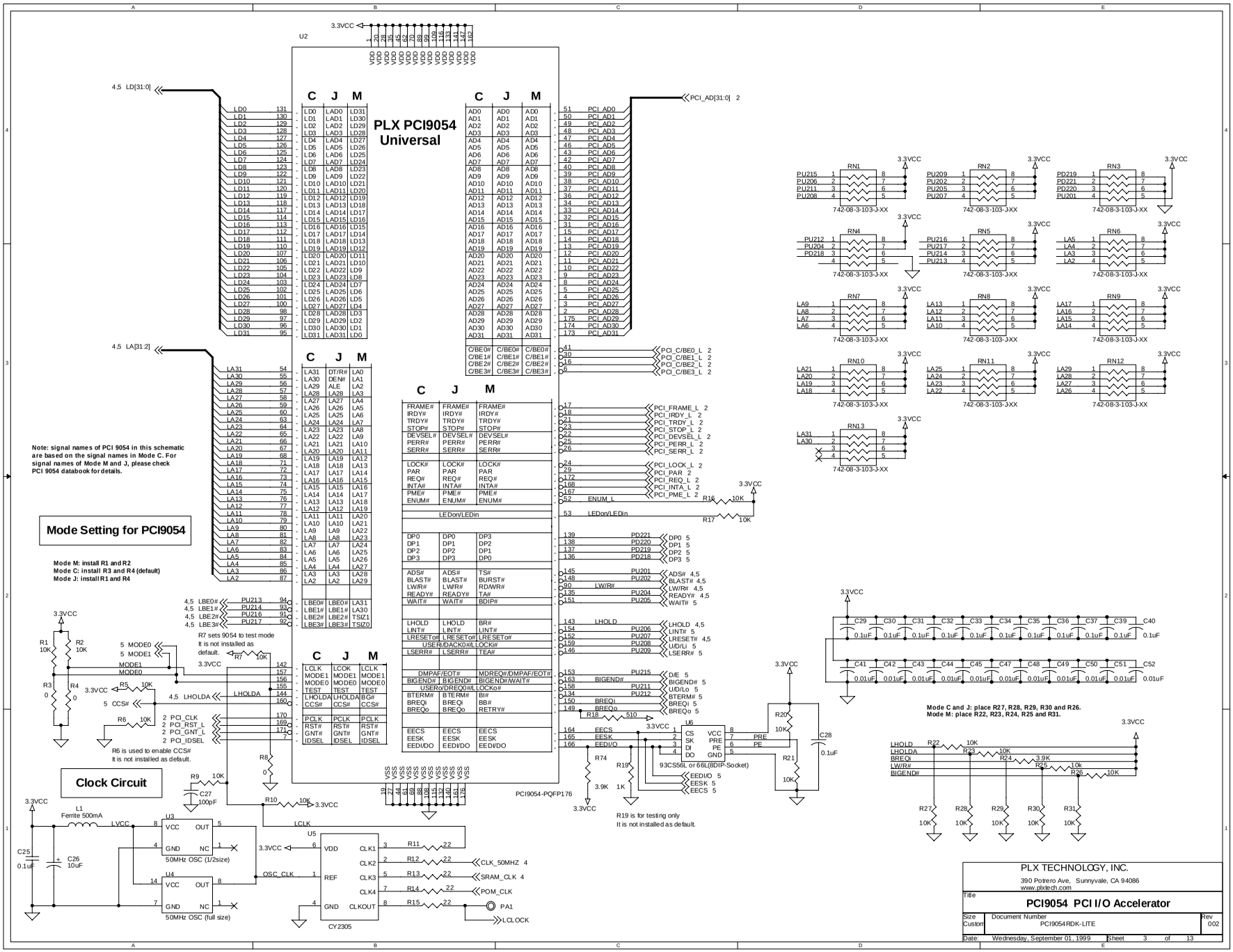
Title
PCI Card Edge Connector
Size Custom
Document Number PCI9054RDK-LITE
Rev 002
Date: Wednesday, September 01, 1999
Sheet 2 of 13


PLX PCI9054
Universal
U2
C J M
4,5 LD[31:0]
PCI_AD[31:0] 2
4,5 LA[31:2]
PCI_C/BE0_L 2
PCI_C/BE1_L 2
PCI_C/BE2_L 2
PCI_C/BE3_L 2
PCI_FRAME_L 2
PCI_IRDY_L 2
PCI_TRDY_L 2
PCI_STOP_L 2
PCI_DEVSEL_L 2
PCI_PERR_L 2
PCI_SERR_L 2
PCI_LOCK_L 2
PCI_PAR 2
PCI_REQ_L 2
PCI_INTA_L 2
PCI_PME_L 2
ENUM_L
LEDon/LEDin
R16 10K
R17 10K
DP0 5
DP1 5
DP2 5
DP3 5
ADS# 4,5
BLAST# 4,5
LW/R# 4,5
READY# 4,5
WAIT# 5
LHOLD 4,5
LINT# 5
LRESET# 4,5
U/D/Li 5
LSERR# 5
D/E 5
BIGEND# 5
U/D/Lo 5
BTERM# 5
BREQi 5
BREQo 5
EECS 5
EESK 5
EEDI/O 5
93CS56L or 66L(8DIP-Socket)
R19 is for testing only
It is not installed as default.
PCI9054-PQFP176
Note: signal names of PCI 9054 in this schematic are based on the signal names in Mode C. For signal names of Mode M and J, please check PCI 9054 databook for details.
Mode Setting for PCI9054
Mode M: install R1 and R2
Mode C: install R3 and R4 (default)
Mode J: install R1 and R4
4,5 LBE0# PU213
4,5 LBE1# PU214
4,5 LBE2# PU216
4,5 LBE3# PU217
R7 sets 9054 to test mode
It is not installed as default.
5 MODE0
5 MODE1
MODE1
MODE0
5 CCS#
4,5 LHOLDA
LHOLDA
2 PCI_CLK
2 PCI_RST_L
2 PCI_GNT_L
2 PCI_IDSEL
R6 is used to enable CCS#
It is not installed as default.
R8 0
Clock Circuit
L1
Ferrite 500mA
C25 0.1uF
C26 10uF
C27 100pF
U3
U4
50MHz OSC (1/2size)
50MHz OSC (full size)
U5
CY2305
OSC_CLK
LCLK
CLK_50MHZ 4
SRAM_CLK 4
POM_CLK
PA1
LCLOCK
Mode C and J: place R27, R28, R29, R30 and R26.
Mode M: place R22, R23, R24, R25 and R31.
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
RN13
742-08-3-103-J-XX
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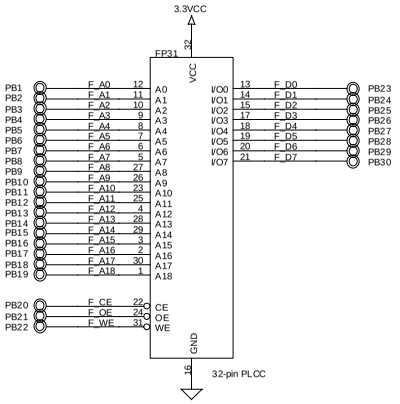
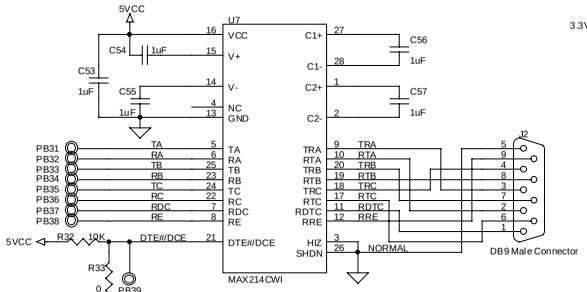
Title
PCI9054 PCI I/O Accelerator
Size Custom
Document Number PCI9054RDK-LITE
Rev 002
Date: Wednesday, September 01, 1999
Sheet 3 of 13

Prototyping Flash ROM Socket

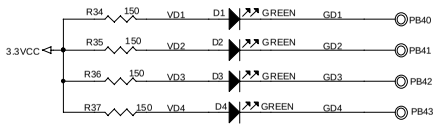


User Programmable DTE/DCE RS-232 Transceiver

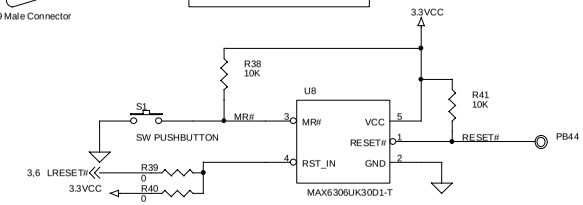


R33 is not installed as defualt.

User Defined Status LEDs



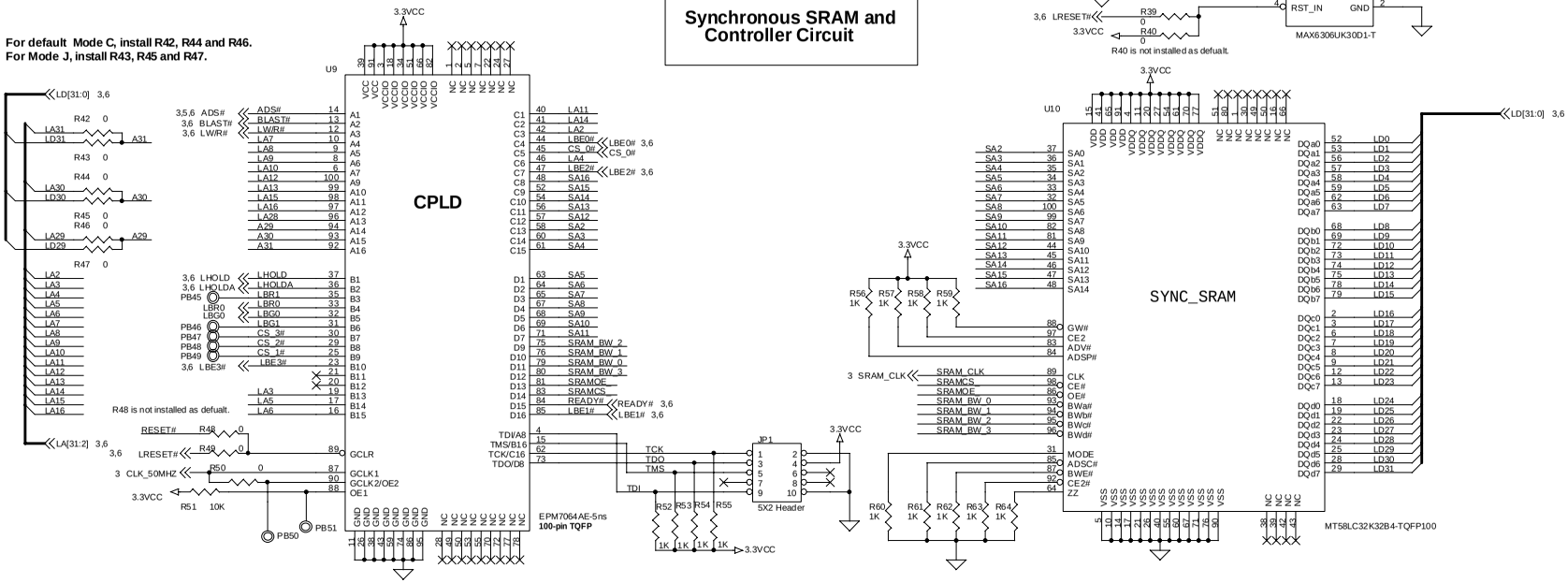
User Accessible Reset Circuit

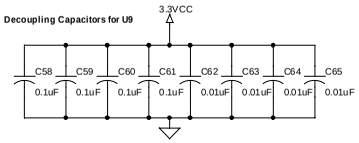


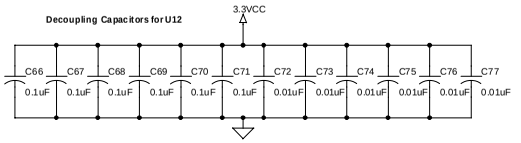
R40 is not installed as defualt.

Synchronous SRAM and Controller Circuit

For default Mode C, install R42, R44 and R46.
For Mode J, install R43, R45 and R47.







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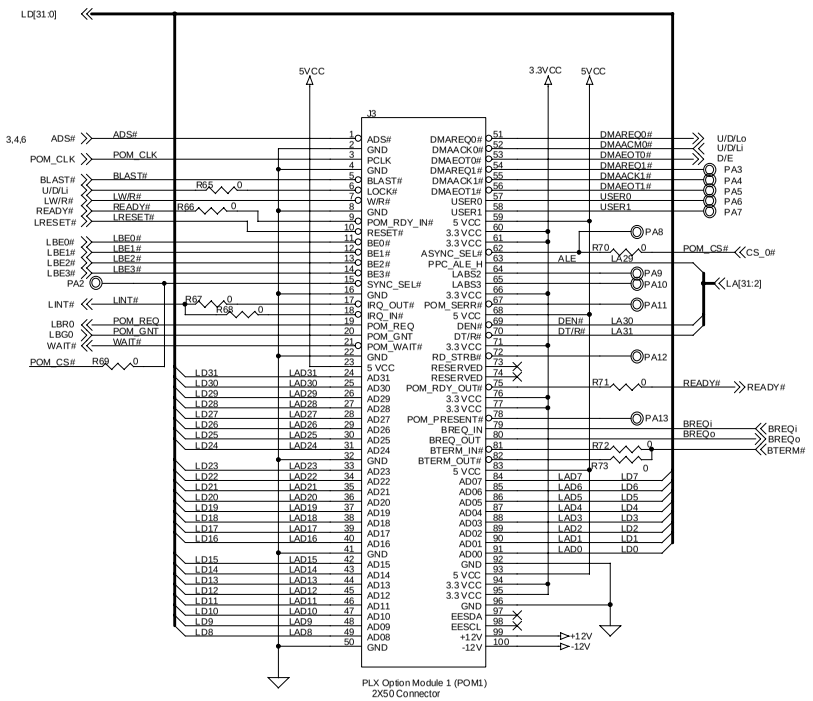
Title: **SRAM, CPLD, Serial Port, ROM Socket and LEDs**

Size	Document Number	Rev
Custom	PCI9054RDK-LITE	002

Date: Wednesday, September 01, 1999 Sheet 4 of 13

PLX Option Module Connector



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Title: **PLX Option Module C onnector**

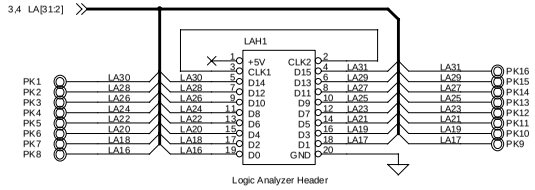
Size	Document Number	Rev
Custom	PCI9054RDK-LITE	002

Date: Wednesday, September 01, 1999 Sheet 5 of 13

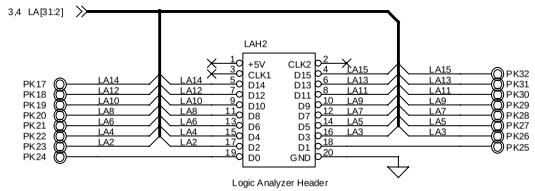
Test Headers

Note: these are designed to hook up directly to HP logic analyzer termination adapter01650-63203.

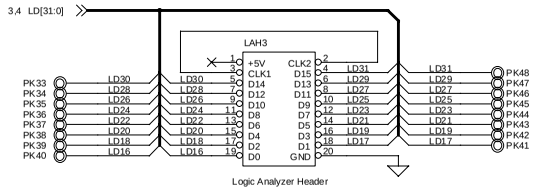
Local Address Bus -Upper Half



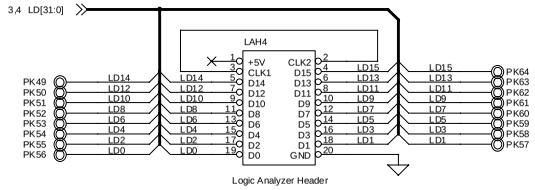
Local Address Bus - Lower Half



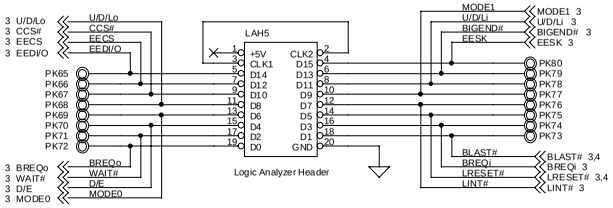
Local Data Bus - Upper Half



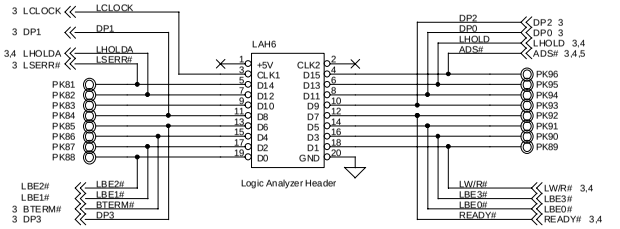
Local Data Bus - Lower Half



Control Signals in Local Bus (A)



Control Signals in Local Bus (B)



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Title: **Logic Analyzer Test Headers**

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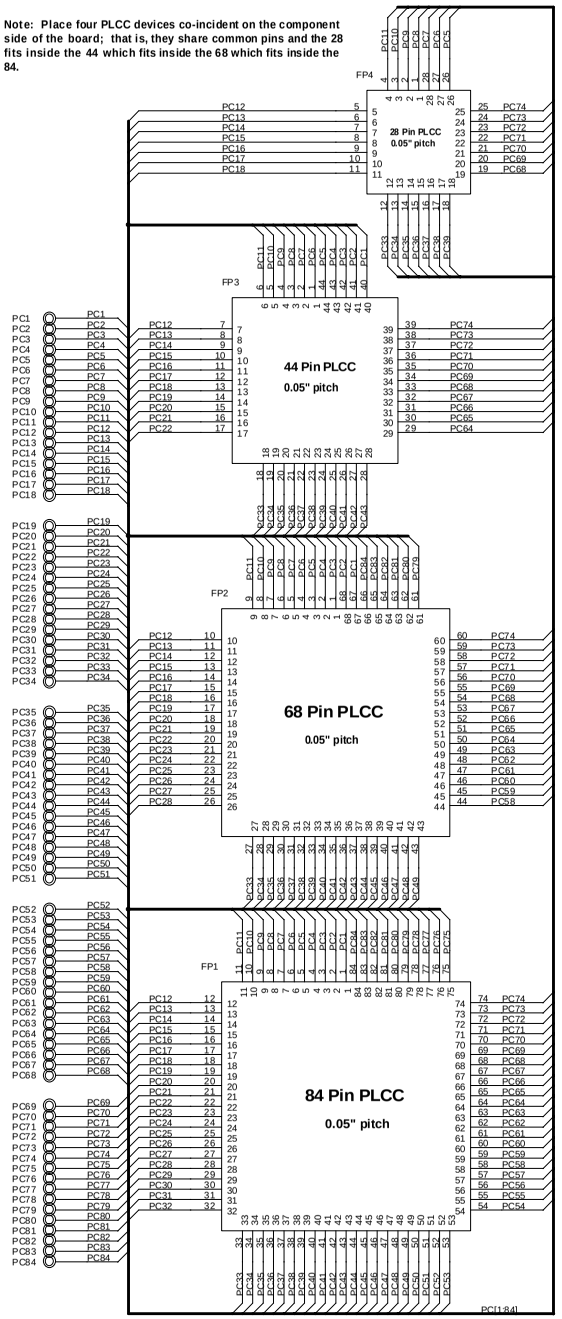
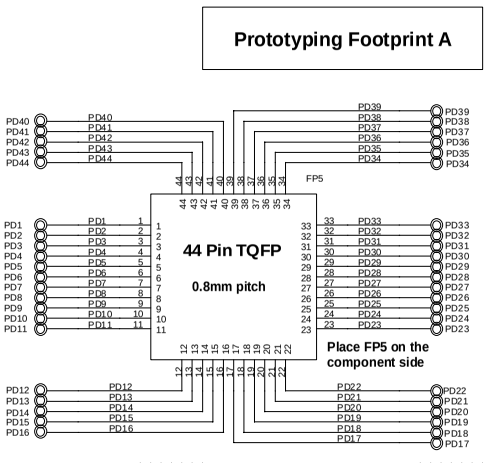
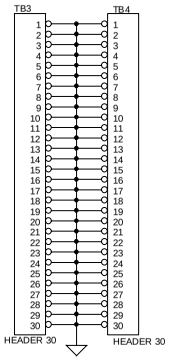
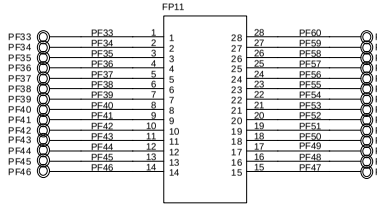
Prototyping Footprint A

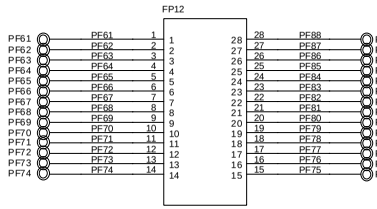
Note: Place four PLCC devices co-incident on the component side of the board; that is, they share common pins and the 28 fits inside the 44 which fits inside the 68 which fits inside the 84.

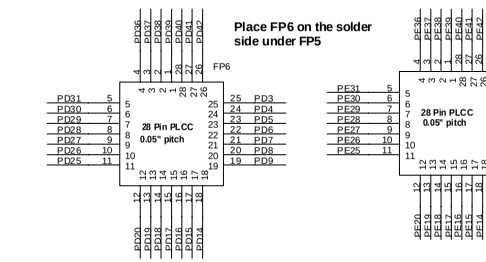


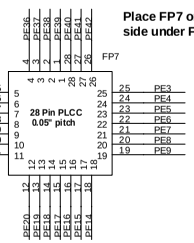


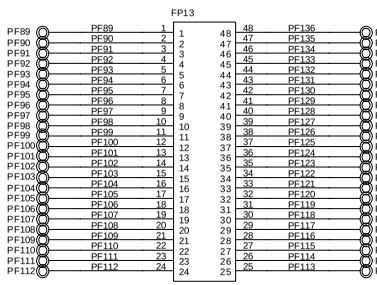


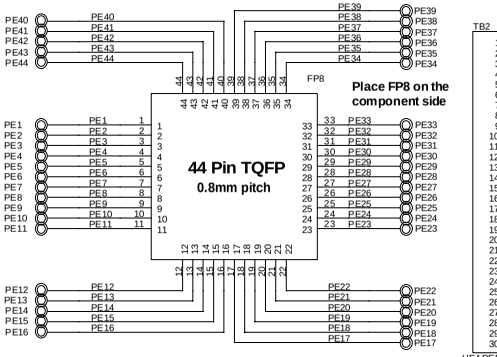


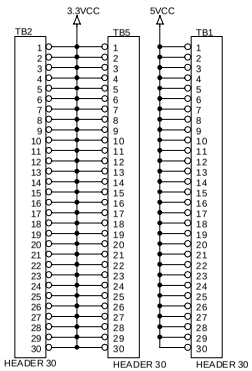


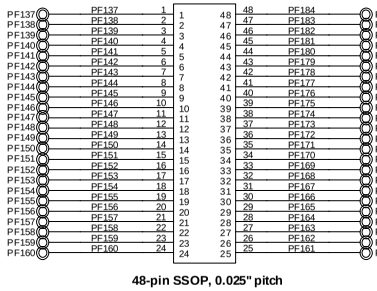


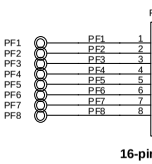


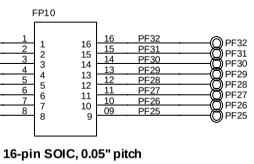












Place FP9-FP14 on the component side

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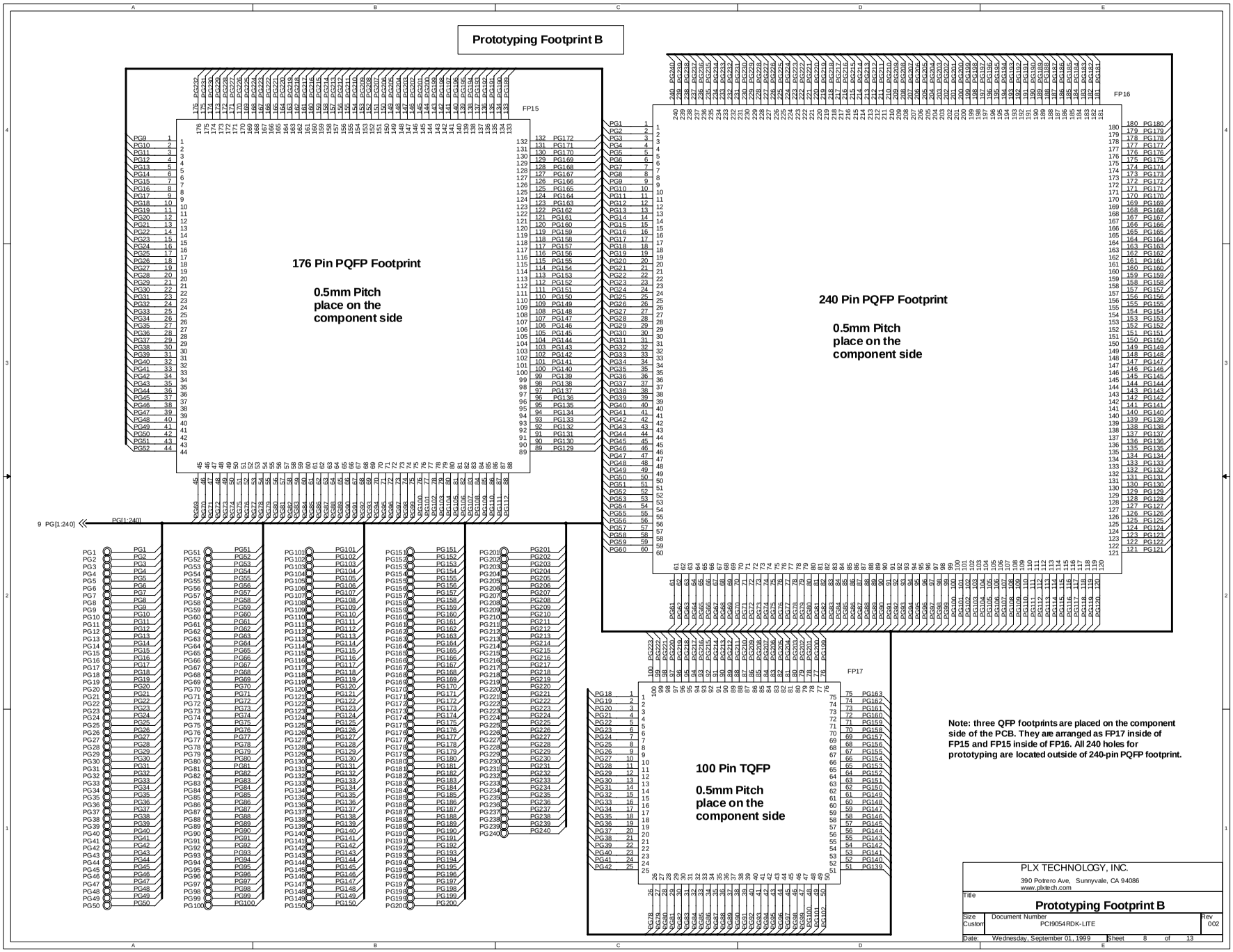
Prototyping Footprint B
176 Pin PQFP Footprint
0.5mm Pitch
place on the
component side
FP15
240 Pin PQFP Footprint
0.5mm Pitch
place on the
component side
FP16
100 Pin TQFP
0.5mm Pitch
place on the
component side
FP17
9 PG[1:240]
PG[1:240]
Note: three QFP footprints are placed on the component side of the PCB. They are arranged as FP17 inside of FP15 and FP15 inside of FP16. All 240 holes for prototyping are located outside of 240-pin PQFP footprint.
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Title
Prototyping Footprint B
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Custom
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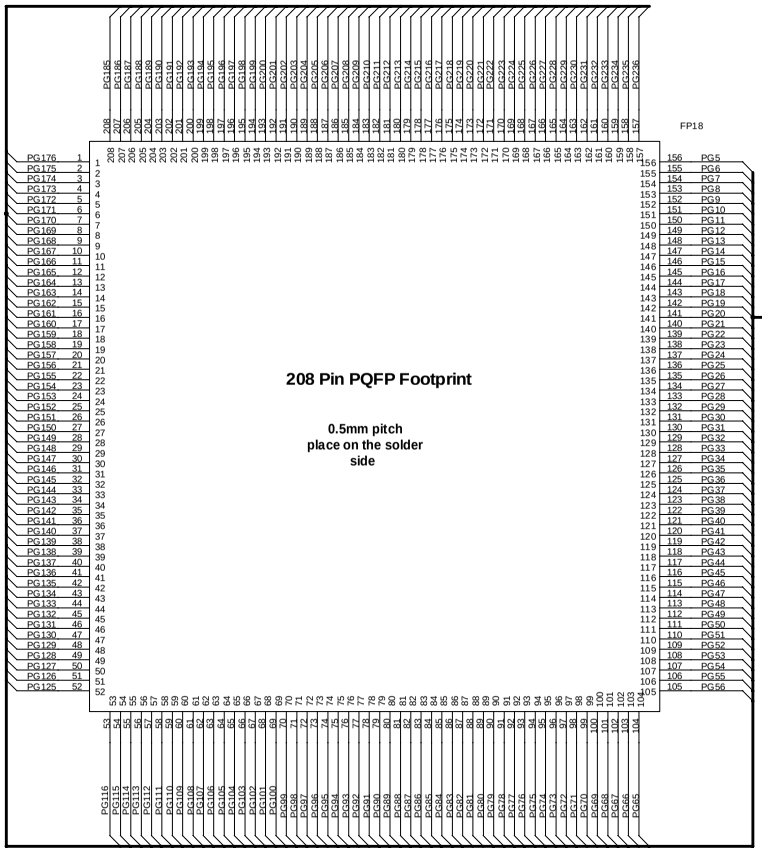
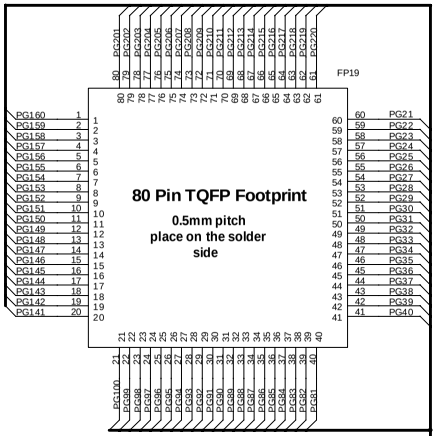
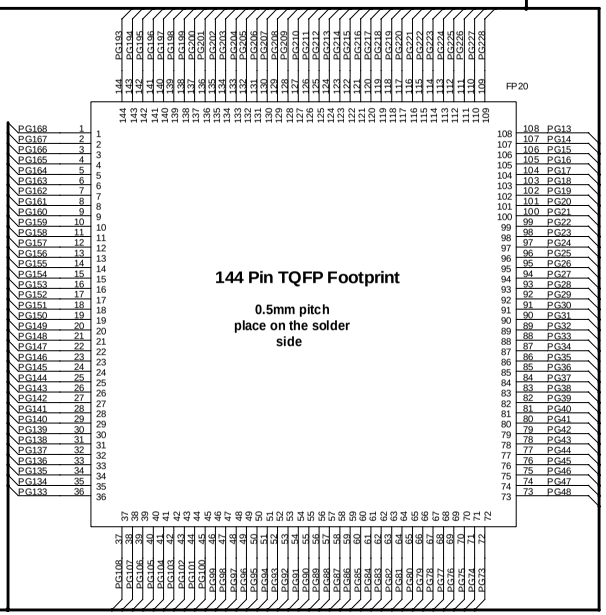
Prototyping Footprint C







8 PG[1:240]

PG[1:240]

Note: three footprints in this schematic are placed on the solder side of the PCB under the footprint of 240-pin PQFP (FP16). They are arranged as FP19 inside of FP20 and FP20 inside of FP18. All of them share prototyping holes with FP16.

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Title: **Prototyping Footprint C**

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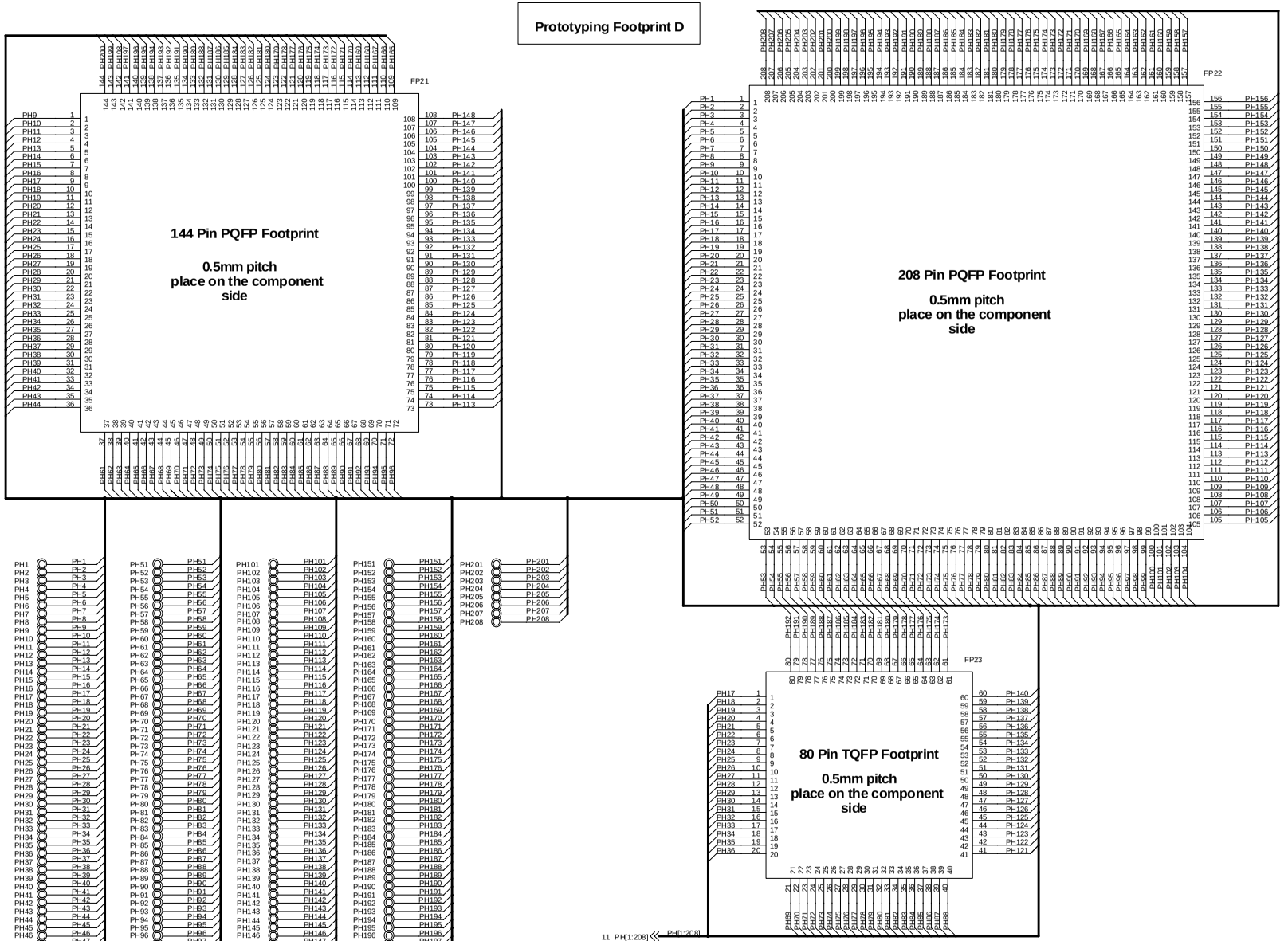
Prototyping Footprint D



Note: three footprints are placed on the component side of the PCB. They areарranged as FP23 inside of FP21 and FP21 insde of FP22. All 208 holes for prototyping are located outside of 208-pin PQFP footprint.

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Title: **Prototyping Footprint D**

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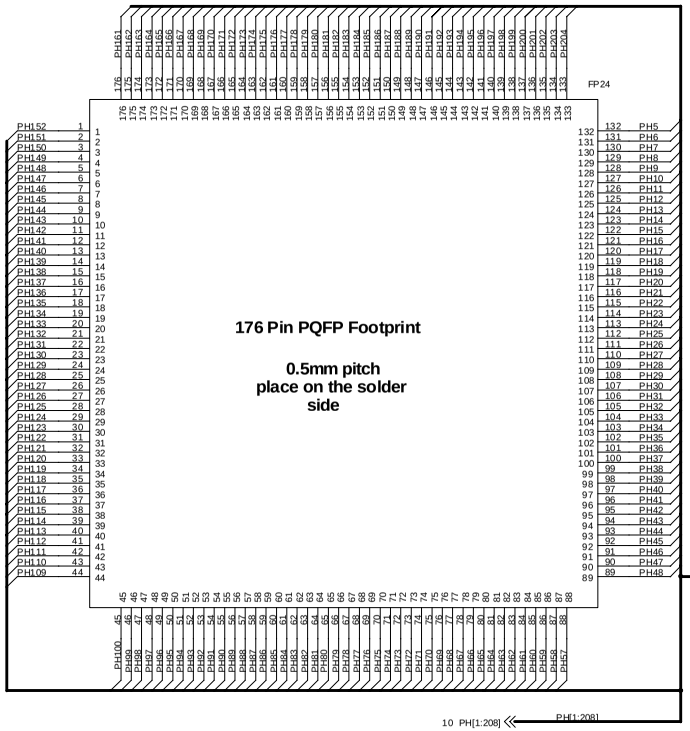
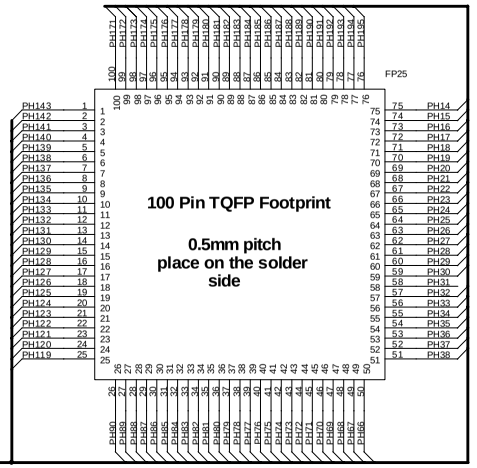
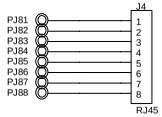
Prototyping Footprint E

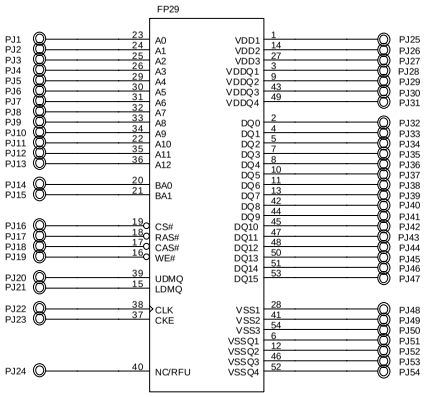




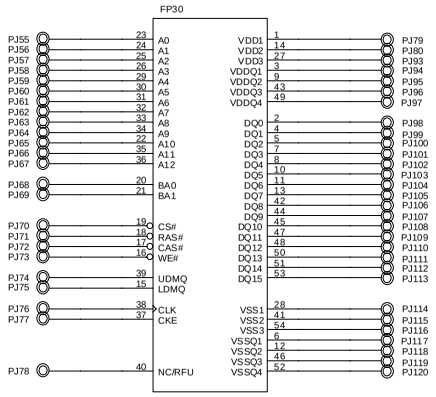
Note: two footprints, FP24 and FP25 are placed on the solder side of the PCB under the footprint of 208-pin PQFP (FP22). They are arranged as FP25 inside of FP24. All of them share prototyping holes with FP22.

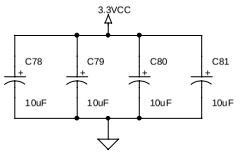


The above connectors are placed on the component side.



Note: FP29 and FP30 are placed on the component side.





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Title: **Prototyping Footprint E**

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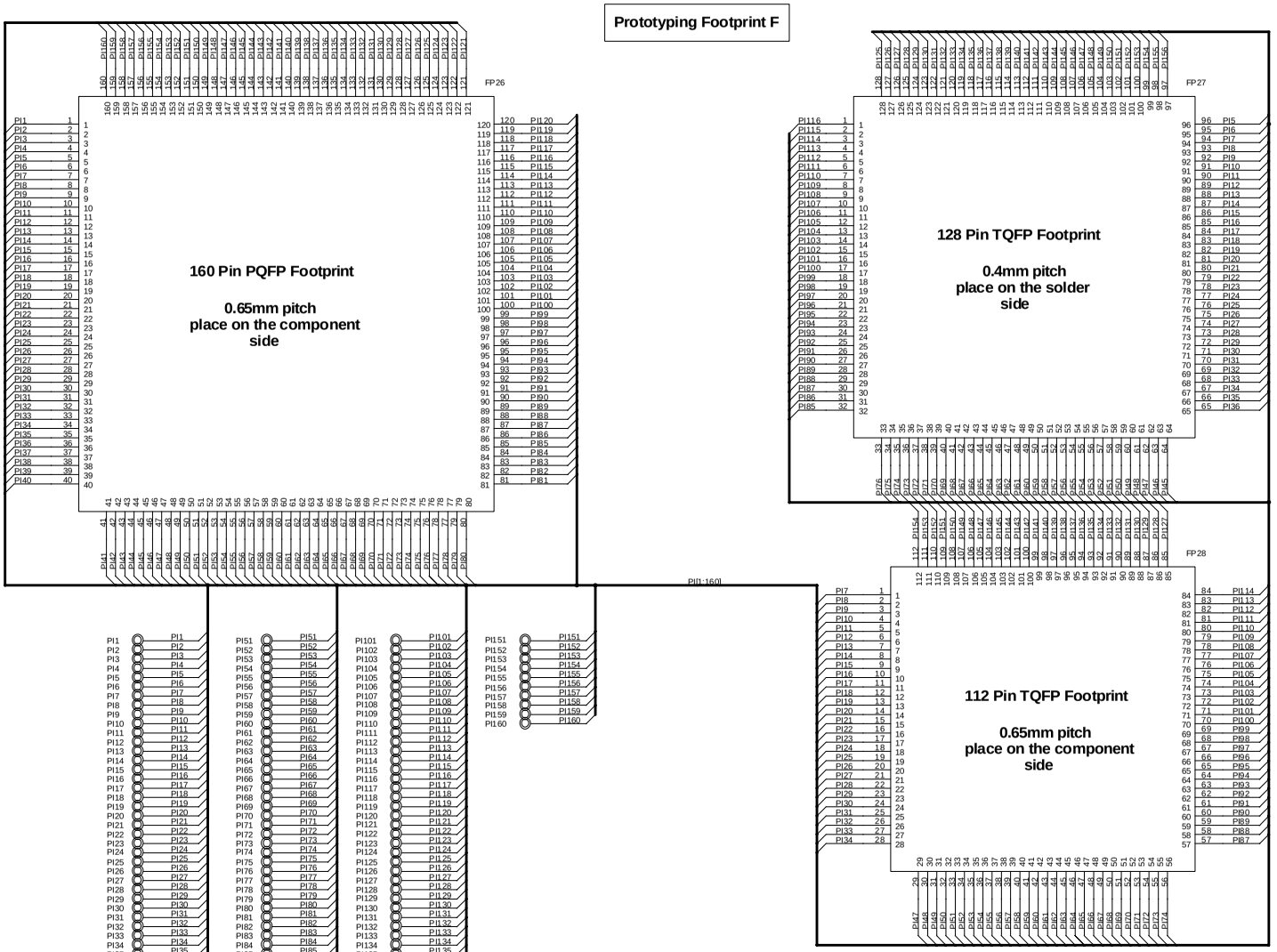

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Title: **Prototyping Footprint F**

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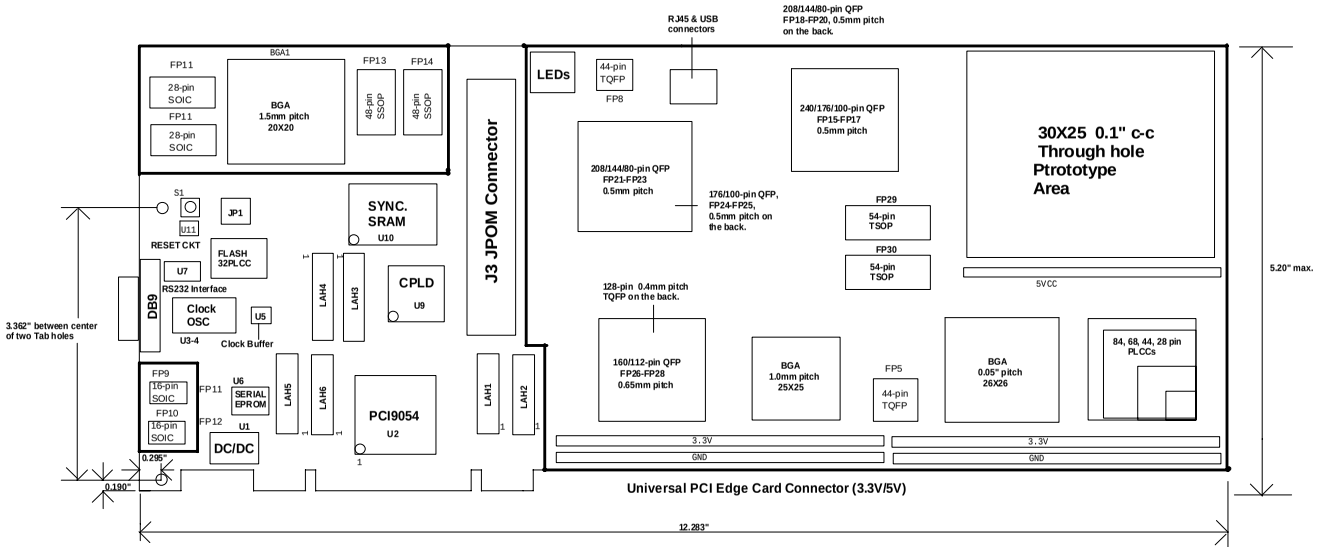

Note:

1. **Control Signal Connector (LAH5)**
2. **Control Signal Connector (LAH6)**
3. **Data Bus Connector (LAH3)**
4. **Data Bus Connector (LAH4)**
5. **Address Bus Connector (LAH1)**
6. **Address Bus Connector (LAH2)**
7. **Marked as ▭ is ptototyping area**

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Title: **Suggested Board Layout**		
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