PCI 9054RDK-LITE

Design Note Rev. 1.0
July 2000

A. Product Status

The scope of this document encompasses the PCI 9054RDK-LITE Reference Design Kit

Product	Revision	Description	Production
PCI 9054RDK-LITE	Version 1.0	PCI Bus Master prototyping design kit	June 1999

1. The PCI 9054RDK-LITE board with a blank serial EEPROM or no EEPROM will prevent the PC from booting

Problem:

The PCI 9054RDK-LITE board is designed with a programmed EEPROM for PC BIOS to access during the boot up

Solution/workaround:

To boot the PCI 9054RDK-LITE with either no serial EEPROM or a blank one, the board needs to be modified in order to pull the local READY# input to the PCI 9054 low. With READY# pulled low, the board can then be booted with either a programmed EEPROM or a blank one. In both cases, the EEDI/EEDO signal must have a pull-up resistor. To boot with no EEPROM, this pull-up resistor must be changed to a pull-down resistor, in addition to pulling READY# low.

To modify the PCI 9054RDK-LITE for READY# signal pull-down:

1. Lift the READY# output pin (pin 84) on the Altera CPLD from the board.
2. Tie the PCI 9054 READY# pin low through a 10K pull-down to ground.

This signal is available at the following locations:
PCI 9054 pin 185, the solder pad to CPLD pin 84, test header LAH[12], POM connector pin 75, and either side of R71.
Note that a spare 10K resistor is available at RN4[4:5]. Since pin 6 of RN4 is already grounded, pin 5 can be soldered to pin 6 to ground one leg of the resistor. A wire can then be soldered to connect R71 with RN4-4.

To change the EEDI/EEDO resistor from a pull-up to a pull-down:
Remove the 10K resistor R74, and install a 1K resistor at R19.