PCI 9052 Data Book

PCI 9052 Data Book

Version 2.0

September 2001

Website: http://www.plxtech.com
Email: apps@plxtech.com
Phone: 408 774-9060
800 759-3735
FAX: 408 774-2169

Order Number: 9052-SIL-DB-P1-2.0

Printed in the USA, September 2001

Contents

Figures . . . . . **ix**

Tables . . . . . **xi**

Registers . . . . . **xiii**

Timing Diagrams . . . . . **xv**

Preface . . . . . **xvii**

Supplemental Documentation xvii
Terms and Definitions xviii
Revision History xviii

1. Introduction **1-1**

1.1. Company and Product Background 1-1
1.2. General Description 1-1
1.3. PCI 9052 Major Features 1-1
1.4. PCI 9052 and PCI 9050 Compatibility 1-4
1.4.1. PCI 9052 New Features 1-4
1.4.2. Errata 1-4
1.4.2.1. PCI 9050 Issues Resolved in PCI 9052 1-4
1.4.2.2. PCI 9052 Issues Not Present in PCI 9050 1-4
1.4.3. Signaling 1-4
1.4.3.1. PCI Bus 1-4
1.4.3.2. Local Bus 1-4
1.4.3.3. Pull-Up and Pull-Down Resistor Recommendations 1-5
1.5. PCI 9052 Comparison with Other PLX Chips 1-7

2. Bus Operation **2-1**

2.1. PCI Bus 2-1
2.1.1. PCI Bus Interface and Bus Cycles 2-1
2.1.1.1. PCI Target (Direct Slave) Command Codes 2-1
2.1.1.2. Wait States—PCI Bus 2-1
2.1.1.3. PCI Bus Little Endian Mode 2-1
2.1.1.4. PCI Prefetchable Memory Mapping 2-1
2.1.1.5. PCI Target (Direct Slave) Accesses to an 8- or 16-Bit Local Bus Device 2-2
2.2. Local Bus 2-2
2.2.1. Introduction 2-2
2.2.1.1. Transactions 2-3
2.2.1.2. Basic Bus States 2-3
2.2.2. Local Bus Signals Used in Timing Diagrams 2-3
2.2.3. Local Bus Signals 2-3
2.2.3.1. Clock 2-3
2.2.3.2. Address/Data 2-3
2.2.3.2.1. LA[27:2] 2-3
2.2.3.2.2. LAD[31:0] 2-3
2.2.3.3. Control/Status 2-4
2.2.3.3.1. ADS#, ALE 2-4
2.2.3.3.2. LBE[3:0]# 2-4
2.2.3.3.3. LLOCKo# 2-4

2.2.3.3.4. LRDYi# . . . 2-4
2.2.3.3.5. LW/R# . . . 2-4
2.2.3.3.6. RD# . . . 2-4
2.2.3.3.7. WAITO# . . . 2-4
2.2.3.3.8. WR# . . . 2-5
2.2.3.4. Local Bus Arbitration . . . 2-5
2.2.3.4.1. LHOLD . . . 2-5
2.2.3.4.2. LHOLDA . . . 2-5
2.2.4. Local Bus Interface and Bus Cycles . . . 2-5
2.2.4.1. Bus Cycles . . . 2-5
2.2.4.2. Wait State Control . . . 2-7
2.2.4.2.1. Internal Wait State Generator . . . 2-7
2.2.4.2.2. Ready Signaling . . . 2-7
2.2.4.3. Burst Mode and Continuous Burst Mode (Bterm “Burst Terminate” Mode) . . . 2-8
2.2.4.3.1. Burst and Bterm Modes . . . 2-8
2.2.4.3.2. Burst-4 Lword Mode . . . 2-9
2.2.4.3.2.1. Continuous Burst Mode (Bterm “Burst Terminate” Mode) . . . 2-9
2.2.4.3.3. Partial Lword Accesses . . . 2-9
2.2.4.4. Recovery States . . . 2-9
2.2.4.5. Local Bus Read Accesses . . . 2-10
2.2.4.6. Local Bus Write Accesses . . . 2-10
2.2.5. Local Bus Big/Little Endian Mode . . . 2-10
2.2.5.1. 32-Bit Local Bus—Big Endian Mode . . . 2-10
2.2.5.2. 16-Bit Local Bus—Big Endian Mode . . . 2-11
2.2.5.3. 8-Bit Local Bus—Big Endian Mode . . . 2-11
2.3. Arbitration Timing Diagram . . . 2-12

3. Reset and Serial EEPROM Initialization . . . 3-1

3.1. Initialization . . . 3-1
3.2. Reset . . . 3-1
3.2.1. PCI Bus RST# Input . . . 3-1
3.2.2. Software Reset . . . 3-1
3.2.3. Local Bus Output LRESET# . . . 3-1
3.3. Serial EEPROM . . . 3-1
3.3.1. Serial EEPROM Load Sequence . . . 3-2
3.3.1.1. Serial EEPROM Load . . . 3-2
3.3.1.2. Recommended Serial EEPROMs . . . 3-2
3.4. Internal Registers . . . 3-4
3.4.1. PCI Configuration Registers . . . 3-4
3.4.2. PCI Bus Access to Internal Registers . . . 3-5
3.5. Timing Diagrams . . . 3-6

4. Direct Slave Operation . . . 4-1

4.1. Overview . . . 4-1
4.2. Direct Data Transfer Mode . . . 4-1
4.2.1. Direct Slave Operation (PCI Master-to-Local Bus Access) . . . 4-1
4.2.1.1. Direct Slave Lock . . . 4-1
4.2.1.2. *PCI r2.1* Features Enable . . . 4-2
4.2.1.2.1. Direct Slave Delayed Read Mode Operation . . . 4-2
4.2.1.2.2. 32000 PCI Clock Timeout . . . 4-2
4.2.1.2.3. *PCI r2.1* 16- and 8-Clock Rule . . . 4-2
4.2.1.3. Direct Slave Read Ahead Mode . . . 4-2
4.2.1.4. Direct Slave Transfer . . . 4-3
4.2.1.5. Direct Slave PCI-to-Local Address Mapping . . . 4-4
4.2.1.5.1. Direct Slave Local Bus Initialization . . . 4-4
4.2.1.5.2. Direct Slave Initialization . . . 4-4
4.2.1.5.3. Direct Slave Example . . . 4-6

4.2.1.5.4. Direct Slave Byte Enables (Non-Multiplexed Mode) 4-6
4.2.1.5.5. Direct Slave Byte Enables (Multiplexed Mode) 4-6
4.3. Response to FIFO Full or Empty 4-7
4.4. Timing Diagrams 4-8
4.4.1. Serial EEPROM and Configuration Initialization 4-9
4.4.2. Non-Multiplexed Mode Local Bus 4-17
4.4.3. Big Endian Mode and Multiplexed Mode Local Bus 4-37

5. ISA Interface Mode 5-1

5.1. Architecture 5-1
5.2. Pin Definitions 5-1
5.2.1. LRESET#/LRESET 5-2
5.2.2. CS0#/MEMRD# and CS1#/MEMWR# 5-2
5.2.3. USER0/WAITO#/IORD# and USER1/LLOCKo#/IOWR# 5-2
5.2.4. ALE/BALE 5-2
5.2.5. NC/CHRDY 5-2
5.2.6. NC/NOWS# 5-3
5.2.7. Other Local Bus Signals 5-3
5.3. Configuring Local Registers for ISA Interface Mode 5-3
5.4. Design Considerations 5-5
5.4.1. Interrupts 5-5
5.4.2. Address and Control Signals 5-5
5.4.3. Ready Signaling Protocol and Timing 5-6
5.4.3.1. Legacy ISA 5-6
5.4.3.2. ISA Interface Mode 5-6
5.4.3.2.1. NOWS# Input Sampling 5-7
5.5. Timing Diagrams 5-8

6. Local Chip Select 6-1

6.1. Overview 6-1
6.2. Chip Select Base Address Registers 6-1
6.3. Procedure for Using Chip Select Base Address Registers 6-2
6.3.1. Chip Select Base Address Register Programming Example 6-2
6.4. Timing Diagram 6-3

7. PCI/Local Interrupts and User I/O 7-1

7.1. Overview 7-1
7.2. Interrupts 7-1
7.2.1. PCI Interrupts (INTA#) 7-1
7.2.2. Local Interrupt Input (LINTi[2:1]) 7-2
7.2.3. All Modes PCI SERR# (PCINMI) 7-2
7.3. User I/O 7-2
7.4. Timing Diagrams 7-3

8. Registers 8-1

8.1. Register Address Mapping 8-1
8.2. PCI Configuration Registers 8-3
8.3. Local Configuration Registers 8-11
8.3.1. Chip Select Registers 8-22
8.3.2. Control Registers 8-24

9. Pin Descriptions 9-1

9.1. Pin Summary 9-1
9.2. Pull-Up/Pull-Down Resistor Recommendations 9-1
9.2.1. Input Pins (Pin Type I) 9-1
9.2.2. Output Pins (Pin Type O) 9-2
9.2.3. I/O Pins (Pin Type I/O) 9-2
9.3. Pinout 9-4

10. Electrical Specifications 10-1

10.1. General Electrical Specifications 10-1
10.2. Local Inputs 10-2
10.3. Local Outputs 10-3

11. Physical Specifications 11-1

11.1. Mechanical Layout 11-1
11.2. Typical Adapter Block Diagram. 11-2
11.3. Pin Assignments 11-4

A. General Information A-1

A.1. Ordering Instructions A-1
A.2. United States and International Representatives, and Distributors A-1
A.3. Technical Support A-1

Index Index-1

FIGURES

1-1. PCI 9052 Block Diagram 1-3
2-1. Local Bus Block Diagram 2-2
2-2. PCI 9052 Single Cycle Write 2-6
2-3. PCI 9052 Single Cycle Read 2-6
2-4. Wait States 2-7
2-5. Big/Little Endian—32-Bit Local Bus 2-10
2-6. Big/Little Endian—16-Bit Local Bus 2-11
2-7. Big/Little Endian—8-Bit Local Bus 2-11
3-1. Serial EEPROM Memory Map 3-2
4-1. Direct Slave Delayed Read Mode 4-2
4-2. Direct Slave Read Ahead Mode 4-3
4-3. Direct Slave Write 4-3
4-4. Direct Slave Read 4-3
4-5. Local Bus Direct Slave Access 4-5
5-1. Circuit for Delaying NOWS# Recognition 5-7
6-1. Chip Select Base Address and Range 6-2
6-2. Memory Map Example 6-2
7-1. Interrupt and Error Sources 7-1
10-1. PCI 9052 Local Input Setup and Hold Waveform 10-2
10-2. PCI 9052 Local Output Delay (Min/Max) 10-3
10-3. PCI 9052 ALE Output Delay (Min/Max) to the Local Clock 10-4
10-4. PCI 9052 BALE Output Delay (Min/Max) to the Local Clock 10-4
11-1. Mechanical Dimensions and Package Outline 11-1
11-2. PCI 9052 Adapter Block Diagram 11-2
11-3. Pin Assignments, Non-Multiplexed and Multiplexed Modes 11-4
11-4. Pin Assignments, ISA and Non-Multiplexed/ISA Interface Modes 11-5

TABLES

Supplemental Documentation Abbreviations xvii
Data Assignment Conventions xviii
1-1. Resistor Recommendations for PCI 9052 and PCI 9050 Input Pins 1-5
1-2. Resistor Recommendations for PCI 9052 and PCI 9050 Output Pins 1-5
1-3. Resistor Recommendations for PCI 9052 and PCI 9050 I/O Pins 1-6
1-4. PCI 9030, PCI 9050, and PCI 9052 Comparison 1-7
2-1. Direct Slave Command Codes 2-1
2-2. PCI Bus Little Endian Byte Lanes 2-1
2-3. LRDYi# Data Transfers, with PCI 9052 as Master Device 2-4
2-4. Local Bus Types 2-5
2-5. Local Address Space Bus Region Descriptor Internal Wait States 2-8
2-6. Burst and Bterm on the Local Bus 2-8
2-7. Burst-4 Lword Mode 2-9
2-8. Direct Slave Single and Burst Reads 2-9
2-9. Big/Little Endian Byte Number and Lane Cross-Reference 2-10
2-10. Lword Lane Transfer—32-Bit Local Bus 2-10
2-11. Upper Word Lane Transfer—16-Bit Local Bus 2-11
2-12. Lower Word Lane Transfer—16-Bit Local Bus 2-11
2-13. Upper Byte Lane Transfer—8-Bit Local Bus 2-11
2-14. Lower Byte Lane Transfer—8-Bit Local Bus 2-11
3-1. Serial EEPROM Guidelines 3-2
3-2. Serial EEPROM Register Load Sequence 3-3
4-1. Response to FIFO Full or Empty 4-7
5-1. ISA and Non-ISA Interface Mode Pin Definitions 5-1
5-2. Pin Functionality in ISA Interface Mode 5-1
5-3. INTCSR Register Settings in ISA Interface Mode 5-4
5-4. CNTRL Register Serial EEPROM Settings 5-4
5-5. LAS0RR and LAS1RR Register Serial EEPROM Settings 5-4
5-6. LAS0BRD and LAS1BRD Register Serial EEPROM Settings 5-5
6-1. Chip Select Base Address Register Signal Programming 6-1
8-1. PCI Configuration Registers 8-1
8-2. Local Configuration Registers 8-2
9-1. Pin Type Abbreviations 9-1
9-2. Input Pin Pull-Up and Pull-Down Resistor Recommendation Summary 9-1
9-3. Output Pin Pull-Up and Pull-Down Resistor Recommendation Summary 9-2
9-4. I/O Pin Pull-Up and Pull-Down Resistor Recommendation Summary 9-2
9-5. Power, Ground, and Unused Pins 9-4
9-6. Serial EEPROM Interface Pins 9-4
9-7. PCI System Bus Interface Pins 9-5
9-8. Local Bus Support Pins 9-6
9-9. Mode-Independent Local Bus Data Transfer Pins 9-9
9-10. Mode-Dependent Local Bus Data Transfer Pins 9-10
9-11. ISA Local Bus Data Transfer Pins (Non-Multiplexed Mode) 9-12

10-1. Absolute Maximum Ratings 10-1
10-2. Operating Ranges 10-1
10-3. Capacitance (Sample Tested Only) 10-1
10-4. Package Thermal Resistance 10-1
10-5. Electrical Characteristics over Operating Range 10-2
10-6. Clock Frequencies 10-2
10-7. AC Electrical Characteristics (Local Outputs) Measured over Operating Range 10-3

REGISTERS

8-1. (PCIIDR; 00h) PCI Configuration ID 8-3
8-2. (PCICR; 04h) PCI Command 8-3
8-3. (PCISR; 06h) PCI Status 8-4
8-4. (PCIREV; 08h) PCI Revision ID 8-4
8-5. (PCICCR; 09-0Bh) PCI Class Code 8-4
8-6. (PCICLSR; 0Ch) PCI Cache Line Size 8-5
8-7. (PCILTR; 0Dh) PCI Bus Latency Timer 8-5
8-8. (PCIHTR; 0Eh) PCI Header Type 8-5
8-9. (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST) 8-5
8-10. (PCIBAR0; 10h) PCI Base Address 0 for Memory Accesses to Local Configuration Registers 8-6
8-11. (PCIBAR1; 14h) PCI Base Address 1 for I/O Accesses to Local Configuration Registers 8-6
8-12. (PCIBAR2; 18h) PCI Base Address 2 for Accesses to Local Address Space 0 8-7
8-13. (PCIBAR3; 1Ch) PCI Base Address 3 for Accesses to Local Address Space 1 8-7
8-14. (PCIBAR4; 20h) PCI Base Address 4 for Accesses to Local Address Space 2 8-8
8-15. (PCIBAR5; 24h) PCI Base Address 5 for Accesses to Local Address Space 3 8-8
8-16. (PCICIS; 28h) PCI Cardbus Information Structure Pointer 8-9
8-17. (PCISVID; 2Ch) PCI Subsystem Vendor ID 8-9
8-18. (PCISID; 2Eh) PCI Subsystem ID 8-9
8-19. (PCIERBAR; 30h) PCI Expansion ROM Base Address 8-9
8-20. (PCIILR; 3Ch) PCI Interrupt Line 8-10
8-21. (PCIIPR; 3Dh) PCI Interrupt Pin 8-10
8-22. (PCIMGR; 3Eh) PCI Minimum Grant 8-10
8-23. (PCIMLR; 3Fh) PCI Maximum Latency 8-10
8-24. (LAS0RR; 00h) Local Address Space 0 Range 8-11
8-25. (LAS1RR; 04h) Local Address Space 1 Range 8-12
8-26. (LAS2RR; 08h) Local Address Space 2 Range 8-13
8-27. (LAS3RR; 0Ch) Local Address Space 3 Range 8-14
8-28. (EROMRR; 10h) Expansion ROM Range 8-14
8-29. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap) 8-15
8-30. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap) 8-15
8-31. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap) 8-16
8-32. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap) 8-16
8-33. (EROMBA; 24h) Expansion ROM Local Base Address (Remap) 8-16
8-34. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptors 8-17
8-35. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptors 8-18
8-36. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptors 8-19
8-37. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptors 8-20
8-38. (EROMBRD; 38h) Expansion ROM Bus Region Descriptors 8-21
8-39. (CS0BASE; 3Ch) Chip Select 0 Base Address 8-22
8-40. (CS1BASE; 40h) Chip Select 1 Base Address 8-22
8-41. (CS2BASE; 44h) Chip Select 2 Base Address 8-23
8-42. (CS3BASE; 48h) Chip Select 3 Base Address 8-23
8-43. (INTCSR; 4Ch) Interrupt Control/Status 8-24
8-44. (CNTRL; 50h) User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control 8-25

TIMING DIAGRAMS

2-1. PCI 9052 Local Bus Arbitration 2-12
3-1. Initialization from Serial EEPROM 3-6
3-2. PCI RST# Asserting Local Output LRESET# 3-6
4-1. PCI 9052 Local Bus Arbitration 4-8
4-2. PCI RST# Asserting Local Output LRESET# 4-9
4-3. Initialization from Serial EEPROM 4-9
4-4. PCI Configuration Write to PCI Configuration Register 4-10
4-5. PCI Configuration Read from PCI Configuration Register 4-10
4-6. PCI Memory Write to Local Configuration Register 4-11
4-7. PCI Memory Read from Local Configuration Register 4-11
4-8. Local Level-Triggered LINTi/LINTi2 Asserting PCI Output INTA# 4-12
4-9. Local Edge-Triggered Interrupt Asserting PCI Interrupt 4-13
4-10. USER[3:0] as Inputs 4-14
4-11. USER[3:0] as Outputs 4-15
4-12. Chip Select [3:0]# 4-16
4-13. Non-Multiplexed Mode, Direct Slave Single Write without Wait States (32-Bit Local Bus) 4-17
4-14. Non-Multiplexed Mode, Direct Slave Single Read without Wait States (32-Bit Local Bus) 4-18
4-15. Non-Multiplexed Mode, Direct Slave Single Read with External (LRDYi#) Wait States (32-Bit Local Bus) 4-19
4-16. Non-Multiplexed Mode, Direct Slave Non-Burst Write with Wait States (32-Bit Local Bus) 4-20
4-17. Non-Multiplexed Mode, Direct Slave Non-Burst Write (8-Bit Local Bus) 4-21
4-18. Non-Multiplexed Mode, Direct Slave Non-Burst Read (32-Bit Local Bus) 4-22
4-19. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Unaligned PCI Address (16-Bit Local Bus) 4-23
4-20. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Prefetch (16-Bit Local Bus) 4-24
4-21. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Continuous Prefetch (8-Bit Local Bus) 4-25
4-22. Non-Multiplexed Mode, Direct Slave Burst Write with Delayed Local Bus (32-Bit Local Bus) 4-26
4-23. Non-Multiplexed Mode, Direct Slave Burst Write with Wait States (16-Bit Local Bus) 4-27
4-24. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Disabled and Wait States (32-Bit Local Bus) . . 4-28
4-25. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus) 4-29
4-26. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Enabled (8-Bit Local Bus) 4-30
4-27. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Four Lwords (32-Bit Local Bus) 4-31
4-28. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Eight Lwords (16-Bit Local Bus) 4-32
4-29. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Four Lwords (8-Bit Local Bus) 4-33
4-30. Non-Multiplexed Mode, Direct Slave Read with Direct Slave Read Ahead Mode Enabled (CNTRL[16]=1) 4-34
4-31. Non-Multiplexed Mode, Direct Slave Burst Write with PCI Write Release Bus Mode Enabled (CNTRL[18]=1) . . 4-35
4-32. Non-Multiplexed Mode, Direct Slave Burst Read with PCI Write Release Bus Mode Disabled (PCI Write Hold Bus Mode Enabled), PCI Read No Write Mode and PCI Read No Flush Mode (Direct Slave Read Ahead Mode) Enabled, PCI Read with Write Flush Mode Disabled, and *PCI r2.1* Features Enabled (CNTRL[18:14]=01101) 4-36
4-33. Multiplexed Mode, Direct Slave Single Write, Local Bus Big Endian (32-Bit) 4-37
4-34. Multiplexed Mode, Direct Slave Single Read, Local Bus Big Endian (32-Bit) 4-38
4-35. Multiplexed Mode, Direct Slave Burst Write, Local Bus Big Endian (32-Bit) 4-39
4-36. Multiplexed Mode, Direct Slave Burst Write, Local Bus Big Endian (16-Bit) 4-40
4-37. Multiplexed Mode, Direct Slave Burst Read, Local Bus Big Endian (32-Bit) 4-41
4-38. Multiplexed Mode, Direct Slave Burst Read, Local Bus Big Endian (16-Bit) 4-42

5-1. 8-Bit Memory Read/Write Standard ISA Cycle (6 LCLK Shown) 5-8
5-2. 8-Bit Memory Read/Write Extended ISA Cycle (7 LCLK Shown) 5-8
5-3. 8-Bit Memory Read/Write Compressed ISA Cycle (3 LCLK Shown) 5-9
5-4. 8-Bit I/O Read/Write Standard ISA Cycle (6 LCLK Shown) 5-10
5-5. 8-Bit I/O Read/Write Extended ISA Cycle (7 LCLK Shown) 5-10
5-6. 8-Bit I/O Read/Write Compressed ISA Cycle (3 LCLK Shown) 5-11
5-7. 16-Bit Memory Read/Write Standard ISA Cycle (3 LCLK Shown) 5-12
5-8. 16-Bit Memory Read/Write Extended ISA Cycle (4 LCLK Shown) 5-12
5-9. 16-Bit Memory Read/Write Compressed ISA Cycle (2 LCLK Shown) 5-13
5-10. 16-Bit I/O Read/Write Standard ISA Cycle (3 LCLK Shown) 5-14
5-11. 16-Bit I/O Read/Write Extended ISA Cycle (4 LCLK Shown) 5-14
6-1. Chip Select [3:0]# 6-3
7-1. Local Level-Triggered LINTi/LINTi2 Asserting PCI Output INTA# 7-3
7-2. Local Edge-Triggered Interrupt Asserting PCI Interrupt 7-4
7-3. USER[3:0] as Inputs 7-5
7-4. USER[3:0] as Outputs 7-6

PREFACE

The information contained in this document is subject to change without notice. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein.

SUPPLEMENTAL DOCUMENTATION

The following is a list of additional documentation to provide the reader with further information:

- *PCI Local Bus Specification, Revision 2.1*, June 1, 1995
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Hot-Plug Specification, Revision 1.0*
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com

Note: *In this data book, shortened titles are given to the works listed above. The following table lists these abbreviations.*

Supplemental Documentation Abbreviations

Abbreviation	Document
PCI r2.1	*PCI Local Bus Specification, Revision 2.1*
PCI r2.2	*PCI Local Bus Specification, Revision 2.2*
Hot-Plug r1.0	*PCI Hot-Plug Specification, Revision 1.0*

TERMS AND DEFINITIONS

For other unfamiliar terms, refer to the index for text references.

- **Direct Slave**—External PCI Bus Master initiates Data write/read to/from the Non-Multiplexed or Multiplexed mode Local Bus.

Data Assignment Conventions

Data Width	PCI 9052 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

REVISION HISTORY

Date	Revision	Comments
8/16/1997	1.0	Initial release
12/02/1999	1.01	Applied minor format changes and corrected minor typographical errors. Changed title from “Data Sheet” to “Data Book.” Added 800 telephone number. Changed copyright date to 1999. Added primary title page, disclaimer and trademarks, part number, and list of Figures, Tables, and Timing Diagrams. Changed “negate” to “de-assert.” Added note to appropriate figures that represent a bus cycle. Changed “field” to “bit” in register-related tables. Table 5-15, PCIBAR3[3], corrected reference to LAS1BRD. Section 7, resequenced content, added section headings, and correctly mapped the input and output waveforms with their respective captions. Timing Diagram 9-24, corrected reference to Lword quantity.
2/09/2000	1.02	Corrected timing diagrams on pages 69-74 (last signal name was cut off from view).
9/2001	2.0	Initial version 2.0 release. Expanded descriptions of operation, registers, and signals. Added pull-up/pull-down resistor recommendations to the Pin Summary section. Renamed CNTRL[14] register bit from “PCI Read Mode” to “*PCI r2.1* Features Enable,” and added explanation of functionality into Section 4.2.1.2 (this bit must be programmed in serial EEPROM to a value of 1, rather than the default 0 to enable *PCI r2.1* protocol enhancements beyond PCI r2.0 operation).

September 2001
Version 2.0

PCI Bus Target Chip with Glueless
ISA Interface Logic for Low-Cost Adapters

1 INTRODUCTION

1.1 COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc., is the leading supplier of high-speed, interconnect silicon and software solutions for the networking and communications industry. These include high-speed silicon, reference design tools that minimize design risk, and software for managing data throughout the PCI Bus, as well as third-party development tool support through the PLX Partner Program, further extending our complete solution.

The PLX solution enables hardware designers and software developers to maximize system input/output (I/O), lower development costs, minimize system design risk, and accelerate time to market.

PLX PCI I/O Accelerator chips and I/O Processor devices are designed in a wide variety of embedded PCI communication systems, including switches, routers, media gateways, base stations, access multiplexors, and remote access concentrators. PLX customers include many of the leading communications equipment companies, including 3Com, Cisco Systems, Compaq Computer, Ericsson, Hewlett-Packard, Intel, IBM, Lucent Technologies, Marconi, Nortel Networks, and Siemens.

Founded in 1986, PLX has developed products based on the PCI industry standard since 1994.

PLX is publicly-traded (NASDAQ: PLXT) and headquartered in Sunnyvale, California, USA, with operations in the United Kingdom, Japan, and China.

1.2 GENERAL DESCRIPTION

The PCI 9052 provides a compact high performance PCI Bus Slave interface for adapter boards. The PCI 9052 is designed to connect a wide variety of Local Bus designs to the PCI Bus and allow relatively slow Local Bus designs to achieve 132 MB/s Burst transfers on the PCI Bus.

The PCI 9052 can be programmed to connect directly to the Non-Multiplexed or Multiplexed mode 8-, 16-, or 32-bit Local Bus. The 8-and 16-bit modes allow easy conversion of ISA designs to PCI. (Refer to Figure 1-1 on page 1-3.)

The PCI 9052 contains Read and Write FIFOs to speed match the 32-bit wide, 33 MHz PCI Bus to a Local Bus, which may be narrower or slower. Up to five Local Address spaces and four Chip Select outputs are supported.

1.3 PCI 9052 MAJOR FEATURES

***PCI Local Bus Specification, Revision 2.1*-Compliant.** The PCI 9052 is compliant with *PCI r2.1*, supporting low cost slave adapters. This allows simple conversion of ISA adapters to PCI.

Direct Slave (Target) Data Transfer Mode. The PCI 9052 supports Burst Memory-Mapped and single I/O-mapped accesses from the PCI-to-Local Bus. Read and Write FIFOs enable high-performance bursting on the Local and PCI Buses. The PCI Bus is always bursting; however, the Local Bus can be set to bursting or continuous single cycle.

ISA Interface Mode Logic on Board. The PCI 9052 supports single cycle reads/writes for 8- and 16-bit Memory and I/O accesses from the PCI Bus to the ISA Interface. Refer to Section 5, “ISA Interface Mode” to learn how to use the PCI 9052 in ISA Interface mode.

Interrupt Generator. The PCI 9052 can generate a PCI interrupt from two Local Bus interrupt inputs, or by software writing to an internal register bit.

Clock. The PCI 9052 Local Bus interface runs from a local TTL-compatible clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock, allowing the Local Bus to run at an independent rate from the PCI clock. The buffered PCI Bus clock (BCLKO) may be connected to the Local Bus clock (LCLK) through a 50-Ohm series resistor.

Programmable Local Bus Configurations. The PCI 9052 supports 8-, 16-, or 32-bit Local Buses, which may be Non-Multiplexed or Multiplexed mode.

In Non-Multiplexed mode, the PCI 9052 has four Local Byte Enables (LBE[3:0]#), 26 address lines (LA[27:2]), and 32, 16, or 8 data lines (LAD[31:0]).

In Multiplexed mode, the PCI 9052 has four Local Byte Enables (LBE[3:0]#), and 28 address lines (LAD[27:0]), multiplexed with 32, 16, or 8 data lines (LAD[31:0]).

Direct Slave Read Ahead Mode. The PCI PCI 9052 supports Direct Slave Read Ahead mode, where prefetched data can be read from the PCI 9052 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and be 32-bit aligned (next address = current address + 4).

Bus Drivers. All control, address, and data signals generated by the PCI 9052 directly drive the PCI and Local Buses, without external drivers.

Serial EEPROM Interface. The PCI 9052 contains a three-wire serial EEPROM interface that provides the option of loading configuration information from a serial EEPROM device. This is useful for loading information unique to a particular adapter (*such as* Vendor ID and chip selects).

Note: *A serial EEPROM is required when ISA Interface mode is selected.*

Four Local Chip Selects. The PCI 9052 provides up to four local chip selects. The base address and range of each chip select are independently programmable from the serial EEPROM or Host.

Five Local Address Spaces. The base address and range of each local address space are independently programmable from the serial EEPROM or Host.

Big/Little Endian Byte Swapping. The PCI 9052 supports Big and Little Endian byte ordering. The PCI 9052 also supports Big Endian Byte Lane mode to redirect the current word or byte lane during 16- or 8-bit Local Bus operation.

Local Bus Wait States. In addition to the LRDYi# (local ready input) handshake signal for variable wait state generation, the PCI 9052 has an internal wait state generator (Read and Write address-to-data, data-to-data, and data-to-address).

Read/Write Strobe Delay and Write Cycle Hold. Read and Write strobe (RD# and WR#, respectively) timings can be programmed independently for each Local Address Space. RD# and WR# strobe assertion at the beginning the cycle can be optionally delayed during address-to-data wait states. The Write Cycle Hold option extends data valid time for additional clock cycles beyond WR# strobe de-assertion.

Programmable Prefetch Counter. The Local Bus Prefetch Counter can be programmed to 0 (no prefetch), 4, 8, 16, or Continuous (Prefetch Counter turned off) Prefetch mode. The prefetched data can be used as cached data if a consecutive address is used (must be Lword-aligned).

Direct Slave Delayed Read Mode. The PCI 9052 supports *PCI r2.1* Delayed Read with:

- PCI Read with Write Flush mode
- PCI Read No Flush mode
- PCI Read No Write mode
- PCI Write Release Bus mode

PCI Read/Write Retry Delay Timer. The PCI 9052 has a programmable Direct Slave (PCI Target) Retry Delay timer, which, when expired, generates a Retry to the PCI Bus.

PCI LOCK Mechanism. The PCI 9052 supports Direct Slave LOCK sequences. A PCI Master can obtain exclusive access to the PCI 9052 device by locking to the PCI 9052.

PCI Bus Transfers up to 132 MB/s.

Low-Power CMOS in 160-pin Plastic QFP Package (PQFP).

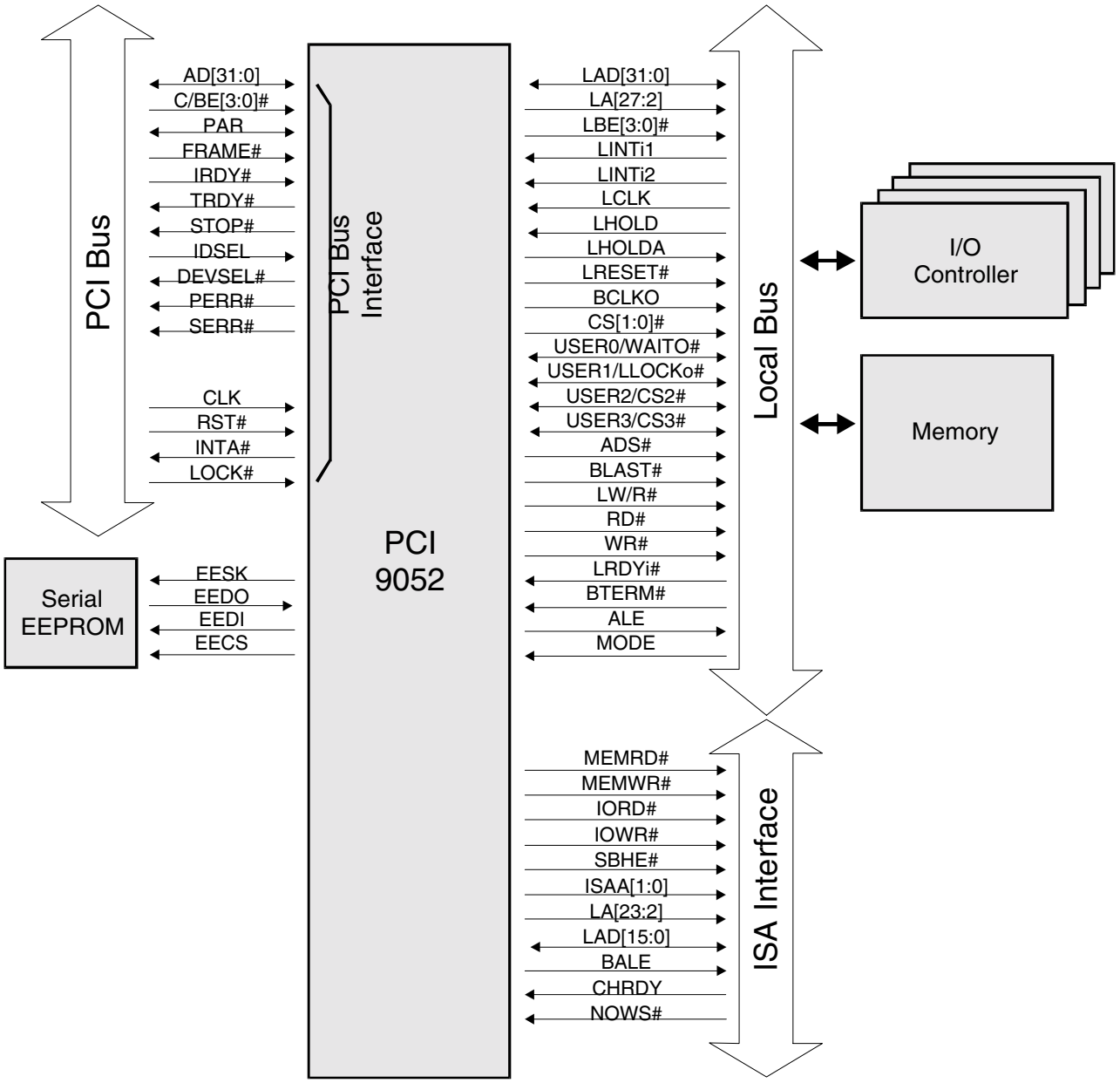


Figure 1-1. PCI 9052 Block Diagram

1.4 PCI 9052 AND PCI 9050 COMPATIBILITY

The PCI 9052 is pin- and register-compatible with the PCI 9050. It uses the same PCI Device ID value of 9050h used by the PCI 9050. Software can distinguish the PCI 9052 from the PCI 9050 by using the PCI Revision ID register (PCIREV) value, which is 02h in the PCI 9052 and 01h in the PCI 9050.

The following provides design migration compatibility information from the PCI 9050 to the PCI 9052.

1.4.1 PCI 9052 New Features

The PCI 9052 provides these additional features over the PCI 9050:

- ISA interface, configured with new INTCSR[12] register bit
- Positive edge-triggered latched Local interrupt inputs, configured and controlled with new INTCSR[11:8] register bits
- Manufactured using .5 micron process, while the PCI 9050 uses .6 micron

1.4.2 Errata

1.4.2.1 PCI 9050 Issues Resolved in PCI 9052

The following outlines the PCI 9050 issues resolved in the PCI 9052.

- *PCI 9050 Errata #1*
  (Reads from Local Configuration Registers)

  PCI 9052 Resolution—No restriction on reading Local Configuration registers.

- *PCI 9050 Errata #2*
  (Expansion ROM Space Enable)

  PCI 9052 Resolution—EROMRR[0] Decode Enable bit addition, allows the PCI 9052 to use Expansion ROM without BIOS modification, as needed for the PCI 9050.

- *PCI 9050 Errata #5*
  (Read Ahead Mode with Burst Enabled)

  PCI 9052 Resolution—Read Ahead mode and Local burst can be enabled concurrently, rather than being mutually exclusive, as in PCI 9050.

- *PCI 9050 Design Notes #1 (RD# Read Strobe Always Driven)*

  PCI 9052 Resolution—RD# is not driven when the PCI 9052 does not own the Local Bus.

- *PCI 9050 Design Notes #2 [Retry Delay Clock (CNTRL[22:19]) Value]*

  PCI 9052 Resolution—No programmed serial EEPROM required, as needed for the PCI 9050.

1.4.2.2 PCI 9052 Issues Not Present in PCI 9050

The PCI 9052 issues not present in the PCI 9050 are as follows:

- *PCI 9052 Errata #3* (Microsoft Windows 98 write to Subsystem Vendor ID register disables PCI 9052 PCI interrupt)
- *PCI 9052 Design Notes #7* [approximately 50-Ohm series resistor required, if BCLKO (buffered PCI clock) drives LCLK]
- *PCI 9052 Design Notes #8* (during PCI reset, LAD[31:0] data pins are driven to random power-up states)

1.4.3 Signaling

1.4.3.1 PCI Bus

The PCI 9052 PCI pins provide stronger drive current than the PCI 9050.

1.4.3.2 Local Bus

- PCI 9052 ALE output pulse width is dependent upon Local clock frequency, while the PCI 9050 ALE pulse width is frequency-independent.
- PCI 9052 drives Local Bus control signals when it owns the Local Bus and is idle, while the PCI 9050 does not. Impact—the PCI 9052 designs use fewer external pull-up/pull-down resistors than the PCI 9050.

1.4.3.3 Pull-Up and Pull-Down Resistor Recommendations

Table 1-1 through Table 1-3 detail pin pull-up/ pull-down resistor recommendations for the PCI 9052 and PCI 9050.

Table 1-1. Resistor Recommendations for PCI 9052 and PCI 9050 Input Pins

Pin	Signal	PCI 9052	PCI 9050
129	BTERM#	Internal 80K-Ohm pull-up; if used, add external pull-up	Internal 100K-Ohm pull-up; if used, add external pull-up
45	CHRDY/NC	None internal, pull or tie high	No Connect
143	EEDO	Pull-up required, if no EEPROM or blank serial EEPROM is present	Internal 100K-Ohm pull-up
135	LCLK	50-Ohm series resistor from BCLKO	None
134	LHOLD	None internal, drive or tie low	Internal 50K-Ohm pull-down
136, 137	LINTi[2:1]	None internal, pull to inactive state	Internal 100K-Ohm pull-up
128	LRDYi#	Internal 80K-Ohm pull-up; if used, add external pull-up	Internal 100K-Ohm pull-up; if used, add external pull-up
68	MODE	None internal, tie high or low	Internal 100K-Ohm pull-up
67	NOWS#/NC	Internal 80K-Ohm pull-up	No Connect
99	TEST	Internal 50K-Ohm pull-down	Internal 50K-Ohm pull-down

Table 1-2. Resistor Recommendations for PCI 9052 and PCI 9050 Output Pins

Pin	Signal	PCI 9052	PCI 9050
123	ADS#	None needed if always Local Master	If used, pull-up recommended
64	ALE/BALE	None needed if always Local Master	If used, pull-down recommended
63	BCLKO	50-Ohm series resistor to LCLK	None (always driven)
124	BLAST#	None needed if always Local Master	If used, pull-up recommended
131, 130	CS[1:0]#/ MEMWR#/MEMRD#	None (always driven)	None (always driven)
142	EECS	None (always driven)	None (always driven)
145	EEDI	None (always driven)	None (always driven)
144	EESK	None (always driven)	None (always driven)
122, 119-105, 102-100, 98-92	LA[27:2]	None needed if always Local Master	If used, pull-ups recommended
46-49	LBE[3:0]#/ SBHE#/ISAA[1:0]	None needed if always Local Master	If used, pull-ups recommended
133	LHOLDA	None (always driven)	None (always driven)
132	LRESET#/ LRESET	None (always driven)	None (always driven)
127	LW/R#	None needed if always Local Master	If used, pull-up recommended
126	RD#	None needed if always Local Master	None (always driven)
125	WR#	None needed if always Local Master	If used, pull-up recommended

Table 1-3. Resistor Recommendations for PCI 9052 and PCI 9050 I/O Pins

Pin	Signal	PCI 9052	PCI 9050
52-62, 69-79, 82-91	LAD[31:0]	Pull-downs recommended for unused	Pull-downs recommended for unused
138	USER0/ WAITO#/ IORD#	If USER0 input, pull to known state If WAITO#, pull-up if not sole Master If IORD#, pull-up if not sole Master	If USER0 input, pull to known state If USER0 output, none needed If WAITO# is used, pull-up recommended
139	USER1/ LLOCKo#/ IOWR#	If USER1 input, pull to known state If LLOCKo#, pull-up if not sole Master If IOWR#, pull-up if not sole Master	If USER1 input, pull to known state If USER1 output, none needed If LLOCKo# is used, pull-up recommended
140	USER2/CS2#	If USER2 input, pull to known state If CS2#, none (always driven)	If USER2 input, pull to known state If CS2#, none (always driven)
141	USER3/CS3#	If USER3 input, pull to known state If CS3#, none (always driven)	If USER3 input, pull to known state If CS3#, none (always driven)

1.5 PCI 9052 COMPARISON WITH OTHER PLX CHIPS

Table 1-4. PCI 9030, PCI 9050, and PCI 9052 Comparison

Feature	PCI 9030	PCI 9050	PCI 9052
Pin Count and Type	176 PQFP/180 µBGA	160 PQFP	160 PQFP
Package Size	27 x 27 mm	31 x 31 mm	31 x 31 mm
Local Address Spaces	5	5	5
PCI Initiator Mode	No	No	No
Number of FIFOs	2	2	2
FIFO Depth—PCI Target Write	32 Lwords (128 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)
FIFO Depth—PCI Target Read	16 Lwords (64 bytes)	8 Lwords (32 bytes)	8 Lwords (32 bytes)
LLOCKo# Pin for Lock Cycles	Yes	Yes	Yes
WAITO# Pin for Wait State Generation	Yes	Yes	Yes
BCLKO (BCLKo) Pin; Buffered PCI Clock	Yes	Yes	Yes
ISA Interface	No	No	Yes
Register Addresses	Identical to the PCI 9050 and PCI 9052, but contains additional registers for increased functionality	—	—
Big Endian ⇔ Little Endian Conversion	Yes	Yes	Yes
Direct Slave Delayed Read Transactions	Yes	Yes	Yes
Direct Slave Delayed Write Transactions	Yes	No	No
PCI Bus Power Management Interface r1.1	Yes	No	No
PCI r2.2 VPD Support	Yes	No	No
Programmable Prefetch Counter	Yes	Yes	Yes
Programmable Wait States	Yes	Yes	Yes
Programmable Local Bus READY# Timeout	Yes	No	No
Programmable GPIOs	9	4	4
Additional Device and Vendor ID Registers	Yes	Yes	Yes
Core and Local Bus V_{CC}	3.3V	5V	5V
PCI Bus V_{CC}	3.3V	5V	5V
3.3V PCI Bus and Local Bus Signaling	Yes	No	No
5V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes	Yes
Serial EEPROM Support	2K-, 4K-bit devices	1K-bit devices	1K-bit devices
Serial EEPROM Read Control	Reads allowed via VPD function and Serial EEPROM Control Register (CNTRL)	Reads allowed via Serial EEPROM Control register (CNTRL)	Reads allowed via Serial EEPROM Control register (CNTRL)
Direct Slave Read Ahead Mode	Yes	Yes	Yes
CompactPCI Hot Swap Capability	*Ready*	*Capable*	*Capable*

2 BUS OPERATION

This section discusses PCI and Local Bus operation.

2.1 PCI BUS

2.1.1 PCI Bus Interface and Bus Cycles

The PCI 9052 is compliant with *PCI r2.1*. Refer to it for specific PCI Bus functions as a Direct Slave Interface chip.

2.1.1.1 PCI Target (Direct Slave) Command Codes

As a Target, the PCI 9052 allows access to the PCI 9052 internal registers and the Local Bus, using the commands listed in Table 2-1.

All Read or Write accesses to the PCI 9052 can be Byte, Word, or Lword (32-bit data). All Memory commands are aliased to basic Memory commands. All PCI 9052 I/O accesses are decoded to an Lword boundary.

Note: *If no PCI Byte Enables (C/BE[3:0]#) are asserted with an I/O Command access, the PCI 9052 issues a Target Abort.*

Table 2-1. Direct Slave Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.1.2 Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to insert PCI Bus wait state(s).

2.1.1.3 PCI Bus Little Endian Mode

The PCI Bus is a Little Endian Bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 2-2. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

2.1.1.4 PCI Prefetchable Memory Mapping

PCI Memory Address spaces assigned to the PCI 9052 for its Local Address spaces can be mapped as either prefetchable or non-prefetchable memory within the system. Configuration software (PCI BIOS) checks the PCI 9052 PCI Configuration register Prefetchable bit(s) (PCIBAR*x*[3], where *x* is the number of the PCIBAR register) to determine whether the Target memory is prefetchable. This value of this bit(s) is set according to Local Configuration register settings (as configured by serial EEPROM values) at boot time.

When set to 1, the Prefetchable bit(s) signals that the Memory space can operate under a prefetching protocol, for improved performance. If a PCI Master initiates a read to a location that is mapped in the prefetchable address range, a Host-to-PCI or PCI-to-PCI bridge is permitted to extend the Read Transaction burst length in anticipation of the Master consuming the additional data. The Prefetchable bit(s) should normally be set if all the following conditions are met:

- Multiple Memory reads of an Lword result in the same data
- If Read data is discarded by the PCI Master, no negative side effects occur
- Address space is not mapped as I/O
- Local Target must be able to operate with byte merging

Byte merging is an optional function of a Host-to-PCI or PCI-to-PCI bridge in which bytes or combinations of bytes written in any order by multiple individual Memory Write cycles to one Lword address can be merged within the bridge's Posted Memory Write buffer into a single Lword Write cycle. Byte merging is possible when any of the bytes to be merged are written only once, and the Prefetchable bit(s) is set to 1 (PCIBAR*x*[3]=1).

The Prefetchable bit(s) setting has no effect on prefetching initiated by the PCI 9052. PCI 9052 prefetching is disabled, by default, in the Local Configuration registers, and should be enabled to support highest performance with Direct Slave Burst reads and Direct Slave Read Ahead mode. (Refer to Section 4.2.1.3.)

2.1.1.5 PCI Target (Direct Slave) Accesses to an 8- or 16-Bit Local Bus Device

Direct PCI access to an 8- or 16-bit Local Bus device results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each 8-bit transfer, byte enables are encoded to provide Local Address bits LA1 and LA0. For each 16-bit transfer, byte enables are encoded to provide BLE#, BHE#, and LA1.

Do not use direct PCI access to an 8-bit bus with nonadjacent byte enables in a PCI Lword. Nonadjacent byte enables cause an incorrect LA1 and LA0 address sequence when bursting to memory. Therefore, for each Lword written to an 8-bit bus, the PCI 9052 does not write data after the first gap. Direct PCI accesses to an 8-bit bus with nonadjacent byte enables are not terminated with a Target Abort. Therefore, for nonadjacent bytes (illegal byte enables), the PCI Master must perform single cycles.

2.2 LOCAL BUS

2.2.1 Introduction

The Local Bus provides a data path between the PCI Bus and non-PCI devices, including memory devices and peripherals. The Local Bus is a 32-bit Non-Multiplexed or Multiplexed mode bus, with Bus Memory regions that can be programmed for 8-, 16-, or 32-bit widths.

The PCI 9052 is the Local Bus Master. The PCI 9052 can transfer data between the Local Bus, internal registers and FIFOs. Burst lengths are not limited. The bus width depends upon the Local Address Space register setting. There are four address spaces and one default space (the Expansion ROM that can be used as another address space). Each space contains a set of Configuration registers that determine all Local Bus characteristics when that space is accessed.

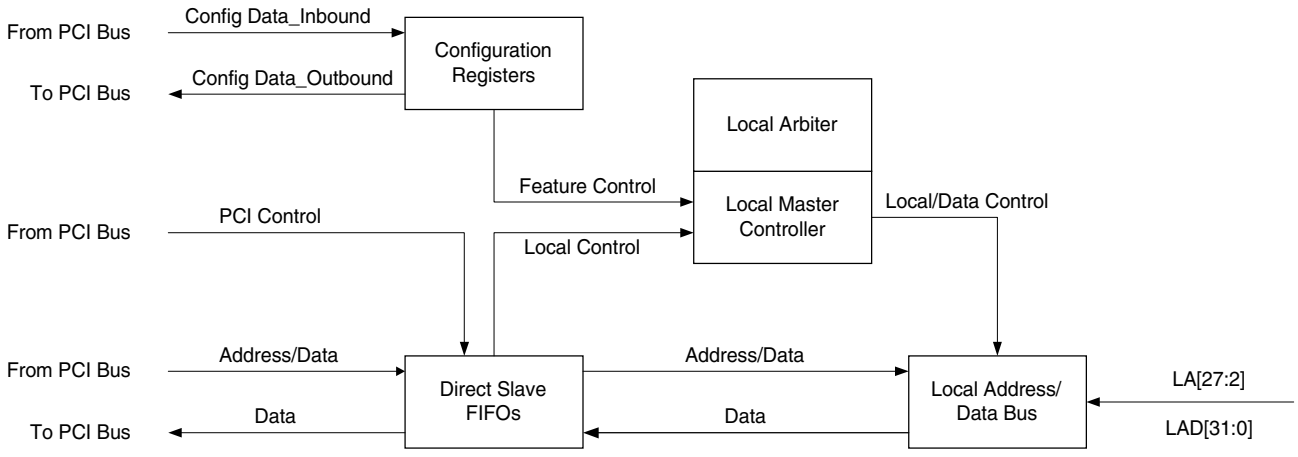


Figure 2-1. Local Bus Block Diagram

2.2.1.1 Transactions

Four types of transactions can occur on a Local Bus:

- Read
- Write
- Read Burst
- Write Burst

A Bus access is a transaction which is bounded by the assertion of ADS# at the beginning and de-assertion of BLAST# at the end. A Bus access consists of an Address cycle followed by one or more Data transfers. During each Clock cycle of an access, the Local Bus is in one of four basic states defined in Section 2.2.1.2. A Clock cycle consists of one Local Bus clock period.

2.2.1.2 Basic Bus States

The four basic bus states are *idle*, *address*, *data/wait*, and *recovery*. Once the Local Bus Master owns the Bus and needs to start a Bus access, the address state is entered, ADS# or ALE is asserted, and a valid address is presented on the Address/Data Bus. Data is then transferred while in a data/wait state. LRDYi# or the internal wait state generator is used to insert wait states. BLAST# is asserted during the last data/wait state to signify the last transfer of the access. In Multiplexed mode only, after all data is transferred, the Bus enters the recovery state to allow the Bus devices to recover. The Bus then enters the idle state and waits for another access.

2.2.2 Local Bus Signals Used in Timing Diagrams

The key Local Bus control signals listed in most timing diagram examples are as follows:

- ADS# or ALE indicates the start of an access
- LRDYi#, WAITO#, and BTERM# are used to insert wait states and terminate Burst cycles during Data transfers
- LW/R# indicates the Data transfer direction
- BLAST# and BTERM# indicate the end of an access

The key data signals are:

- LA Address Bus
- LAD Address, Data Bus
- LBE[3:0]# Local Byte Enables, indicating valid byte lanes

2.2.3 Local Bus Signals

Signal usage varies upon application. There are four groups of Local Bus signals:

- Clock
- Address/Data
- Control/Status
- Arbitration

2.2.3.1 Clock

LCLK, the Local Bus clock, operates at frequencies up to 40 MHz, and is asynchronous to the PCI Bus clock. Most Local Bus signals are driven and sampled on the rising edge of LCLK. Setup and hold times, with respect to LCLK, must be observed. (Refer to Section 10.2, “Local Inputs,” on page 10-2 for setup and hold timing requirements.)

2.2.3.2 Address/Data

2.2.3.2.1 LA[27:2]

LA[27:2] contains the transfer word address.

2.2.3.2.2 LAD[31:0]

In Non-Multiplexed mode, the LAD[31:0] Bus is a 32-bit Non-Multiplexed Data Bus. During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, data supplied by the PCI 9052 is replicated across the entire 32-bit wide bus.

In Multiplexed mode, the LAD[31:0] Bus is a 32-bit Multiplexed Address/Data Bus. During an Address phase, LAD[27:0] contains the transfer word address. LAD[1:0] have the same address value as LBE[1:0]#, for use with 8- or 16-bit bus width addressing.

Note: *Dedicated address pins are available.*

During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, data supplied by the PCI 9052 is replicated across the entire 32-bit wide bus.

2.2.3.3 Control/Status

The control/status signals control the address latches and flow of data across the Local Bus.

2.2.3.3.1 ADS#, ALE

A Local Bus access starts when ADS# (address strobe) is asserted during an address state by the PCI 9052 as the Local Bus Master. ALE is used to strobe the LA/LAD Bus into an external address latch. Refer to Figure 10-3 on page 10-4 for ALE timing specifications.

2.2.3.3.2 LBE[3:0]#

During an Address phase, the LBE[3:0]# Local Byte Enables denote which byte lanes are being used during access of a 32-bit bus. They remain asserted until the end of the Data transfer.

2.2.3.3.3 LLOCKo#

When the PCI 9052 owns the Local Bus, LLOCKo# is asserted to indicate that an atomic operation for a Direct Slave access may require multiple transactions to complete. LLOCKo# is asserted during the Address phase of the first transaction of the atomic operation, and de-asserted one clock after the last transaction of the atomic operation completes. If enabled, the Local Bus arbiter does not grant the Bus to another Master until the atomic operation is complete.

2.2.3.3.4 LRDYi#

The LRDYi# input pin has a corresponding Enable bit in the Bus Region Descriptor register for each Local address space. If LRDYi# is enabled, this indicates that Write data is being accepted or Read data is being provided by the Bus Slave. If a Bus Slave needs to insert wait states, it can de-assert LRDYi# until it is ready to accept or provide data. If LRDYi# is disabled, then the Local Bus transfer length can be determined by internal wait state generators. LRDYi# is not sampled until address-to-data or data-to-data wait states have expired. (Refer to Table 2-3.)

When BTERM# input is enabled for a Local Address space in the corresponding Bus Region Descriptor register, BTERM# can be used to complete an access in place of LRDYi#. When BTERM# is enabled and asserted, LRDYi# input is ignored. Further information regarding BTERM# is provided in Section 2.2.4.3.

2.2.3.3.5 LW/R#

During an Address phase, LW/R# is driven to a valid state, and signifies the data transfer direction. Because the PCI 9052 is the Local Bus Master, LW/R# is driven high when the PCI 9052 is writing data to the Local Bus, and low when it is reading the bus.

2.2.3.3.6 RD#

RD# is a general purpose read output strobe. The timing is controlled by the current Bus Region Descriptor register. The RD# strobe is asserted during the entire Data transfer. Normally, it is also asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. RD# remains asserted throughout Burst and NRDD wait states.

2.2.3.3.7 WAITO#

WAITO# is an output that provides status of the internal wait state generators. It is asserted while internal wait states are being inserted. LRDYi# input is not sampled until WAITO# is de-asserted.

Table 2-3. LRDYi# Data Transfers, with PCI 9052 as Master Device

Slave Device	LRDYi#		Description
	Input Enable	Signal	
Address Spaces	0	Ignored	LRDYi# is not sampled by the PCI 9052. Data transfers determined by the internal wait state generator. LRDYi# is ignored and the Data transfer occurs after the internal wait state counter expires.
	1	Sampled	LRDYi# is sampled by the PCI 9052. Data transfers are determined by an external device, which asserts LRDYi# to indicate a Data transfer is occurring. LRDYi# is not sampled until address-to-data or data-to-data wait states have expired.

2.2.3.3.8 WR#

WR# is a general purpose write output strobe. The timing is controlled by the current Bus Region Descriptor register. The WR# strobe is asserted during the entire Data transfer. WR# is normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. WR# remains asserted throughout Burst and NWDD wait states. The LAD data bus hold time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].

2.2.3.4 Local Bus Arbitration

The PCI 9052 is the Local Bus Master. When the PCI Bus initiates a new transfer request, the PCI 9052 takes control of the Local Bus. Another device can gain control of the Local Bus by asserting LHOLD. If the PCI 9052 has no cycles to run, it asserts LHOLDA, transferring control to the external Master. If the PCI 9052 requires the Local Bus before the external Master completes, LHOLDA is de-asserted (preempt condition).

LHOLD can be pulled low or grounded to provide permanent Local Bus ownership to the PCI 9052.

2.2.3.4.1 LHOLD

LHOLD is asserted by a Local Bus Master to request Local Bus use. The PCI 9052 can be made master of the Local Bus by pulling or driving LHOLD low (or by grounding LHOLD).

2.2.3.4.2 LHOLDA

LHOLDA is asserted by the PCI 9052 to grant Local Bus control to a Local Bus Master. When the PCI 9052 requires the Local Bus, it signals a preempt by de-asserting LHOLDA.

2.2.4 Local Bus Interface and Bus Cycles

The PCI 9052 is the Local Bus Master. The PCI 9052 interfaces a PCI Host Bus to a Non-Multiplexed or Multiplexed Local Bus, selected by the MODE pin, as listed in Table 2-4.

Notes: *No PCI Initiator (Direct Master) capability.*

Internal registers are not readable/writable from the Local Bus. The internal registers are accessible from the Host CPU on the PCI Bus or from the serial EEPROM.

Table 2-4. Local Bus Types

MODE Pin	Mode	Bus Width
0	Non-Multiplexed	32-, 16-, and/or 8-bit Non-ISA and/or 16- or 8-bit ISA
1	Multiplexed	32-, 16-, and/or 8-bit

2.2.4.1 Bus Cycles

In both Non-Multiplexed and Multiplexed modes, the LA[27:2] Address Bus drives an access address valid, beginning one clock prior to ADS# assertion (which signals the start of the Bus cycle) and continues until the cycle ends (signaled by BLAST# de-assertion). In Multiplexed mode (MODE=1), the LAD[31:0] Multiplexed Address/Data Bus also drives the access address valid onto LAD[27:0], beginning one clock prior to ADS# assertion and continuing until ADS# de-assertion one clock later, after which data is driven. The LAD[31:0] Data Bus drives Write data valid one clock after ADS# assertion when ADS# de-asserts, and continues until the cycle ends or until data-to-address wait states (or data-to-data wait states if burst is enabled) begin, if programmed. BLAST# assertion indicates the last Data cycle of an access. (Refer to Figure 2-2 and Figure 2-3.)

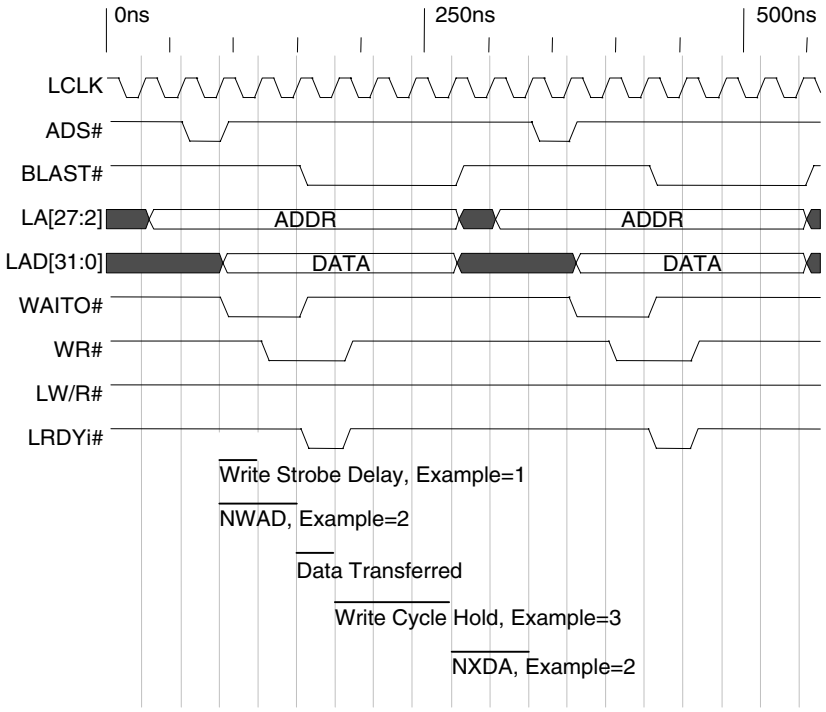


Figure 2-2. PCI 9052 Single Cycle Write

Note: *NWDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*

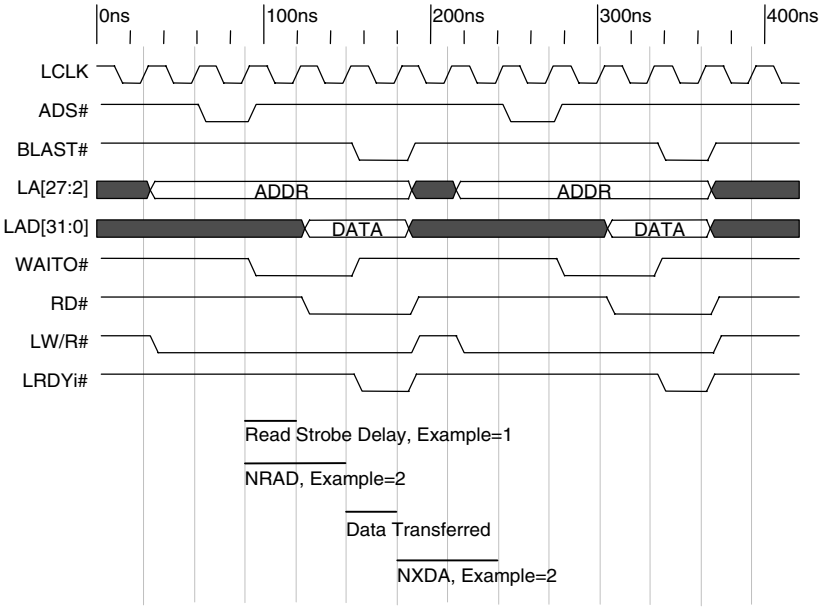


Figure 2-3. PCI 9052 Single Cycle Read

Note: *NRDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*

Write cycle data valid time and Read cycle data time can be extended with internally generated address-to-data wait states and/or by delaying LRDYi# ready input assertion if LRDYi# input is enabled for the Space. When enabled, LRDYi# input assertion indicates to the PCI 9052 that Read data on the bus is valid to accept or a Write Data transfer has completed. LRDYi# input is not sampled until address-to-data wait states (and/or data-to-data wait states with burst), which are signaled by WAITO# output assertion, expire (WAITO# output de-asserted). LRDYi# is ignored during the Address cycle (ADS# assertion), internally generated data-to-address wait states, and idle cycles between transfers. BTERM# input, if enabled, is used to break up a Burst access and also serves as a ready input. (Refer to Section 2.2.4.3.)

For non-ISA spaces, the RD# and WR# strobes can be independently programmed for each Local Address Space. RD# and/or WR# strobe assertion can be optionally delayed during address-to-data wait states. For non-ISA spaces, Write Cycle Hold clocks can be selectively programmed to extend data hold time beyond WR# strobe de-assertion.

Recovery (idle) cycles can be optionally programmed for each Space, using data-to-address wait states to extend time between Local bus accesses to allow sufficient time for an external device to float its data pins after a Read request.

2.2.4.2 Wait State Control

The PCI 9052 as a Local Bus Master signals internal wait states with the WAITO# signal. Local Bus devices can insert external wait states by delaying LRDYi# input assertion. (Refer to Figure 2-2 and Figure 2-3.) The following figure illustrates wait state control.

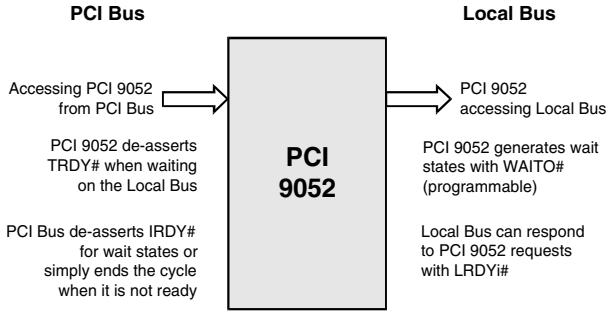


Figure 2-4. Wait States

Note: *The figure represents a sequence of Bus cycles.*

2.2.4.2.1 Internal Wait State Generator

The Local Address Space Bus Region Descriptor can be used to program the number of wait states (if any) generated by the internal wait state generator. (Refer to Table 2-5.)

NXDA wait states are inserted only after the last Data transfer of a Bus request. *For example*, for a Direct Slave single Cycle access to an 8-bit burst Local Bus, NXDA wait states are inserted only after the fourth byte, rather than after every byte.

2.2.4.2.2 Ready Signaling

If LRDYi# mode is disabled, the external LRDYi# input signal has no effect on wait states for a Local access. Wait states between Data cycles are inserted internally by a wait state counter. The wait state counter is initialized with its Configuration register value at the start of each Data access.

If LRDYi# mode is enabled and the internal wait state counter is zero (default value), the LRDYi# input controls the number of additional wait states.

If LRDYi# mode is enabled and the internal wait state counter is programmed to a non-zero value, LRDYi# has no effect until the wait state counter reaches 0. When it reaches 0, the LRDYi# input controls the number of additional wait states.

The BTERM# input can also be used as a ready input. (Refer to Section 2.2.4.3.) If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, BTERM# input is not sampled until the wait state counter reaches 0.

Table 2-5. Local Address Space Bus Region Descriptor Internal Wait States

Wait State	Bits	Description
NRAD	LAS*x*BRD[10:6] EROMBRD[10:6]	**N**umber of **R**ead **A**ddress-to-**D**ata wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)
NRDD	LAS*x*BRD[12:11] EROMBRD[12:11]	**N**umber of **R**ead **D**ata-to-**D**ata wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)
NXDA	LAS*x*BRD[14:13] EROMBRD[14:13]	**N**umber of **R**ead/**W**rite **D**ata-to-**A**ddress wait states (0-3). LAD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a Direct Slave access.)
NWAD	LAS*x*BRD[19:15] EROMBRD[19:15]	**N**umber of **W**rite **A**ddress-to-**D**ata wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)
NWDD	LAS*x*BRD[21:20] EROMBRD[21:20]	**N**umber of **W**rite **D**ata-to-**D**ata wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)

2.2.4.3 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9052 internal register bit and BTERM# refers to the PCI 9052 external signal.*

2.2.4.3.1 Burst and Bterm Modes

As an input, BTERM# is asserted by external logic. It instructs the PCI 9052 to break up a Burst cycle.

Table 2-6. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default)
	0	1	One ADS# per data
Burst-4 Lword	1	0	One ADS# per four data
Continuous Burst	1	1	One ADS# per BTERM# (refer to Section 2.2.4.3.2.1)

On the Local Bus, BLAST# and BTERM# perform the following:

- If Local Bus bursting is enabled for a Local Address space (LAS*x*BRD[0]=1 and/or EROMBRD[0]=1, where *x* is the Local Address Space number), but Bterm mode (continuous burst) and the BTERM# input are disabled (LAS*x*BRD[2]=0 and/or EROMBRD[2]=0), the PCI 9052 bursts (up to four Data phases). BLAST# is asserted at the beginning of the fourth Lword Data phase (LA[3:2]=11) and a new ADS# is asserted at the first Lword (LA[3:2]=00) of the next burst.
- If Bterm mode and the BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1) and asserted, the PCI 9052 terminates the Burst cycle at the end of the current Data phase without generating BLAST#. The PCI 9052 generates a new Burst transfer, starting with a new ADS#, and terminating it normally using BLAST#.
- The BTERM# input is valid only when the PCI 9052 is performing a Direct Slave transaction.
- BTERM# is used to indicate a Memory access is crossing a page boundary or requires a new Address cycle.
- If the internal wait state counter is programmed to a non-zero value and Bterm mode and the BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1), the BTERM# input is not sampled until the wait state counter reaches 0.
- BTERM# always overrides LRDYi#, even if both signals are asserted. BTERM# executes the ongoing transaction and causes the PCI 9052 to initiate a new Address/Data cycle for Burst transactions.

Note: *If the Bterm mode (continuous burst) and the BTERM# input are disabled (LASxBRD[2]=0 and/or EROMBRD[2]=0), the PCI 9052 performs the following:*

- ***32-bit Local Bus****—Bursts up to four Lwords*
- ***16-bit Local Bus****—Bursts up to two Lwords*
- ***8-bit Local Bus****—Bursts up to one Lword*

In every case, it performs four data beats.

2.2.4.3.2 Burst-4 Lword Mode

If Bterm mode (continuous burst) and the BTERM# input are disabled, and Local Bus bursting is enabled for a Local Address space (LAS*x*BRD[2,0]=01 and/or EROMBRD[2,0]=01, respectively), bursting can start on any Lword boundary and continue up to a 16-byte address boundary. After data up to the boundary is transferred, the PCI 9052 asserts a new Address cycle (ADS#).

Table 2-7. Burst-4 Lword Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad-Lword boundary (LA[3:2]=11)
16 bit	Four words or up to a quad-word boundary (LA[2:1]=11)
8 bit	Four bytes or up to a quad-byte boundary (LA[1:0]=11)

2.2.4.3.2.1 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If Bterm mode and the BTERM# input are enabled, and Local Bus bursting for a Local Address space is enabled (LAS*x*BRD[2, 0]=11 and/or EROMBRD[2, 0] =11, respectively), the PCI 9052 can operate beyond Burst-4 Lword mode.

Bterm mode enables the PCI 9052 to perform long bursts to devices that can accept bursts of longer than four Lwords. The PCI 9052 asserts one Address cycle and continues to burst data. If a device requires a new Address cycle (ADS#), it can assert the BTERM# input to cause the PCI 9052 to assert a new Address cycle. The BTERM# input acknowledges the current Data transfer (replacing LRDYi#) and requests that a new Address cycle be asserted (ADS#). The new address is for the next Data transfer.

If Bterm mode and BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1) and the BTERM# signal is asserted, the PCI 9052 asserts BLAST# only if its Read FIFO is full, its Write FIFO is empty, or a transfer is complete.

2.2.4.3.3 Partial Lword Accesses

Partial Lword accesses are Lword accesses in which not all byte enables are asserted.

Table 2-8. Direct Slave Single and Burst Reads

Bus	Direct Slave Single Reads	Direct Slave Burst Reads
32-, 16-, or 8-bit Local Bus	Passes the byte enables	Ignores the byte enables and all 32-bit data is passed

Burst Start addresses can be any Lword boundary. If the Burst Start address in a Direct Slave transfer is not aligned to an Lword boundary, the PCI 9052 first performs a single cycle. It then starts to burst on the Lword boundary.

2.2.4.4 Recovery States

In Non-Multiplexed mode, the PCI 9052 uses the NXDA (data-to-address wait states) value in the Bus Region Descriptor register(s) (LAS*x*BRD[14:13] and/or EROMBRD[14:13], where *x* is the Local Address Space number) to determine the number of recovery states to insert between the last data transfer and next address cycle. This value can be programmed between 0 and 3 clock cycles (default value is 0).

In Multiplexed mode, the PCI 9052 inserts a minimum of one recovery state between the last data transfer and the next address cycle. Add recovery states by programming values greater than one into the NXDA bits of the Bus Region Descriptor register(s) (LAS*x*BRD[14:13] and/or EROMBRD[14:13], where *x* is the Local Address Space number).

Note: *The PCI 9052 does not support the i960J function that uses the LRDYi# input to add recovery states. No additional recovery states are added if the LRDYi# input remains asserted during the last Data cycle.*

2.2.4.5 Local Bus Read Accesses

For all single cycle Local Bus Read accesses, the PCI 9052 reads only bytes corresponding to byte enables requested by a PCI Master. For all Burst Read cycles, the PCI 9052 can be programmed to:

- Perform Direct Slave Delayed Reads
- Perform Direct Slave Read Ahead
- Generate internal wait states
- Enable external wait control (LRDYi# input)
- Enable type of Burst mode to perform

2.2.4.6 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master are written. For all Burst Write cycles, the PCI 9052 can be programmed to:

- Generate internal wait states
- Enable external wait control (LRDYi# input)

2.2.5 Local Bus Big/Little Endian Mode

The PCI 9052 Local Bus can be independently programmed to operate in Little or Big Endian mode for each of the following transfer types:

- Direct Slave accesses to Local Address Space 0
- Direct Slave accesses to Local Address Space 1
- Direct Slave accesses to Local Address Space 2
- Direct Slave accesses to Local Address Space 3
- Direct Slave accesses to Expansion ROM

Notes: *The PCI Bus is always Little Endian.*
Only byte lanes are swapped, not individual bits.

The PCI 9052 Local Bus can be programmed to operate in Big or Little Endian mode, as listed in Table 2-9.

Table 2-9. Big/Little Endian Byte Number and Lane Cross-Reference

Byte Number		
Big Endian	**Little Endian**	**Byte Lane**
3	0	LAD[7:0]
2	1	LAD[15:8]
1	2	LAD[23:16]
0	3	LAD[31:24]

Big/Little Endian Control bits are as follows:

- LAS0BRD[24]—Space 0
- LAS1BRD[24]—Space 1
- LAS2BRD[24]—Space 2
- LAS3BRD[24]—Space 3
- EROMBRD[24]—Expansion ROM

In Big Endian mode, the PCI 9052 transposes data byte lanes. Data is transferred as listed in Table 2-10 through Table 2-14.

2.2.5.1 32-Bit Local Bus—Big Endian Mode

Data is Lword-aligned to the uppermost byte lane (Address Invariance).

Table 2-10. Lword Lane Transfer—32-Bit Local Bus

Burst Order	Byte Lane
First Transfer	PCI Byte 0 appears on Local Data [31:24]
	PCI Byte 1 appears on Local Data [23:16]
	PCI Byte 2 appears on Local Data [15:8]
	PCI Byte 3 appears on Local Data [7:0]

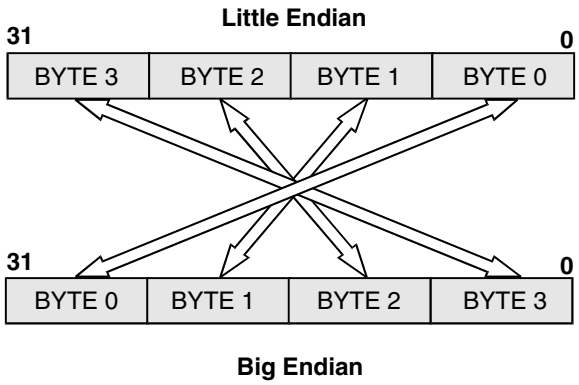


Figure 2-5. Big/Little Endian—32-Bit Local Bus

2.2.5.2 16-Bit Local Bus— Big Endian Mode

For a 16-bit Local Bus, the PCI 9052 can be programmed to use upper or lower word lanes.

Table 2-11. Upper Word Lane Transfer— 16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-12. Lower Word Lane Transfer— 16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

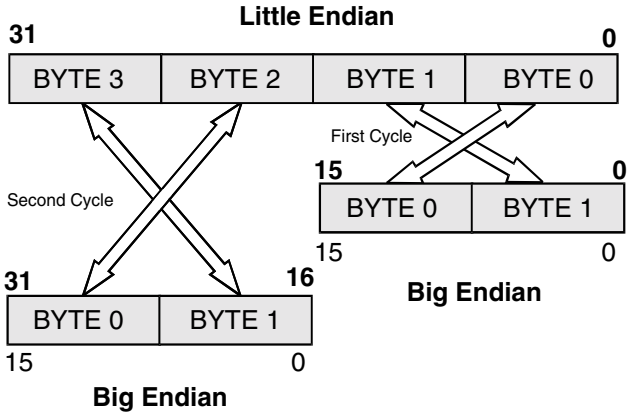


Figure 2-6. Big/Little Endian—16-Bit Local Bus

2.2.5.3 8-Bit Local Bus— Big Endian Mode

For an 8-bit Local Bus, the PCI 9052 can be programmed to use upper or lower byte lanes.

Table 2-13. Upper Byte Lane Transfer— 8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
Second Transfer	Byte 1 appears on Local Data [31:24]
Third Transfer	Byte 2 appears on Local Data [31:24]
Fourth Transfer	Byte 3 appears on Local Data [31:24]

Table 2-14. Lower Byte Lane Transfer— 8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

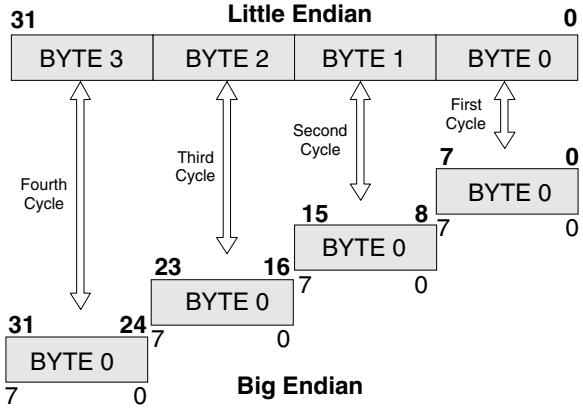
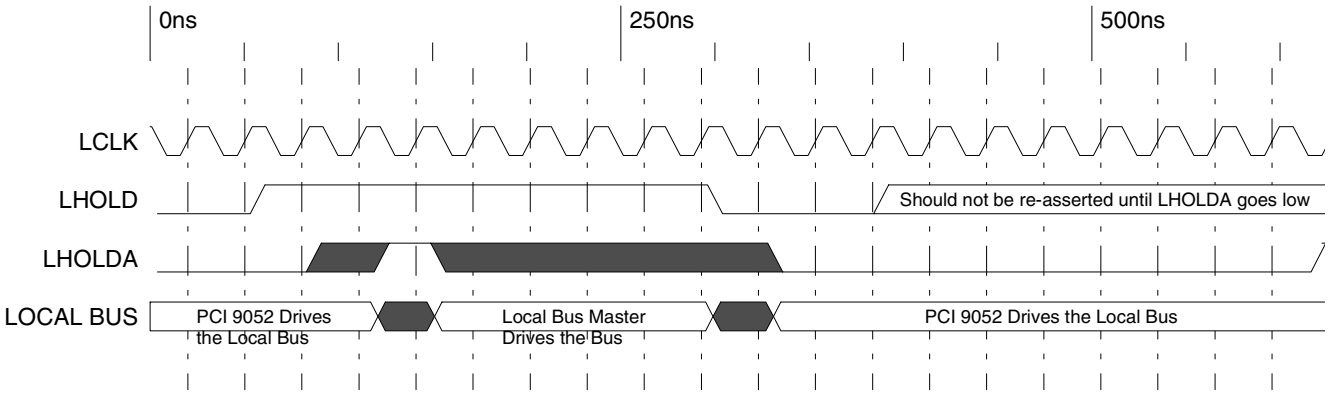


Figure 2-7. Big/Little Endian—8-Bit Local Bus

2.3 ARBITRATION TIMING DIAGRAM



Timing Diagram 2-1. PCI 9052 Local Bus Arbitration

3 RESET AND SERIAL EEPROM INITIALIZATION

3.1 INITIALIZATION

During power-on, the PCI RST# signal resets the default values of the PCI 9052 internal registers. In return, the PCI 9052 outputs the local LRESET# signal and checks for a serial EEPROM. If a serial EEPROM exists, and the first 48 bits are not all ones (1), the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9052 Configuration registers can be written only by the optional serial EEPROM or PCI Host processor. During serial EEPROM initialization, the PCI 9052 response to Direct Slave accesses is Retrys.

3.2 RESET

3.2.1 PCI Bus RST# Input

PCI Bus RST# input assertion causes all PCI Bus outputs to float, resets the entire PCI 9052, asserts Local reset output LRESET#, and floats all other Local Bus output and I/O pins except BCLKO, EECS, EEDI, EESK, and LHOLDA, and Local Data Bus signals (LAD[31:0]) which the PCI 9052 drives to a random power-up state during reset. (Refer to *PCI 9052 Design Notes #8*.)

3.2.2 Software Reset

A PCI host can set the PCI Adapter Software Reset bit (CNTRL[30]=1) to reset the PCI 9052, assert LRESET#/LRESET, and float Local Bus output and I/O pins as described in Section 3.2.1. (Refer to *PCI 9052 Design Notes #8*.) The PCI and Local Configuration register contents are not reset. When the PCI Adapter Software Reset bit is set, the PCI 9052 responds only to Configuration register accesses, and not to Local Bus accesses. The PCI 9052 remains in this reset condition until the PCI Host clears the PCI Adapter Software Reset bit (CNTRL[30]=0). The PCI Interface is not reset.

Note: *If Direct Slave Read Ahead mode is enabled (CNTRL[16]=1), disable it prior to a software reset, or if following a software reset, perform a Direct Slave read of any valid Local Bus address, except the next sequential Lword referenced from the last Direct Slave read, to flush the Direct Slave Read FIFO.*

3.2.3 Local Bus Output LRESET#

LRESET# is asserted when the PCI Bus RST# input is asserted (4 to 10 ns delay) or the PCI Adapter Software Reset bit is set (CNTRL[30]=1).

3.3 SERIAL EEPROM

After reset, the PCI 9052 attempts to read the serial EEPROM to determine its presence. An active low Start bit indicates the serial EEPROM is present. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.) If the first 48 bits in the serial EEPROM are not all ones (1), then the PCI 9052 assumes the device is not blank, and continues reading.

For blank serial EEPROM conditions, the PCI 9052 reverts to the default values. (Refer to Table 3-1.) When the Serial EEPROM Present bit is set to 1 (CNTRL[28]=1), if programmed, real or random data is detected in the serial EEPROM.

A serial data Start bit set to 1 indicates that a serial EEPROM is not present. For missing serial EEPROM conditions, the PCI 9052 stops the serial EEPROM load and reverts to the default values. If no serial EEPROM is present, pull EEDO high through a resistor to prevent false detection of a low Start bit. If no serial EEPROM is present and EEDO is not pulled high through a resistor, the PCI 9052 may load all zeros (0) into its registers, rather than chip default values.

The 5V serial EEPROM clock is derived from the PCI clock. The PCI 9052 generates the serial EEPROM clock by internally dividing the PCI clock by 32.

Table 3-1. Serial EEPROM Guidelines

Serial EEPROM	PCI 9052 System Boot Condition
None	Uses default values (Start bit is 1).
Programmed	Boots with serial EEPROM values (Start bit is 0).
Blank	Detects a blank device and reverts to default values (Start bit is 0).

Notes: *2K-bit devices, such as the FM93CS56, are not compatible.*

The PCI 9052 does not support serial EEPROMs that do not support sequential reads (such as the FM93C46L).

A PCI Bus host can read or program the serial EEPROM. Register bits CNTRL[29:24] control the PCI 9052 pins, enabling reading or writing of the serial EEPROM bits. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)

To reload serial EEPROM data into the PCI 9052 internal registers, write 1 to the Reload Configuration Registers bit (CNTRL[29]=1).

The following steps are necessary, to read or write to the serial EEPROM:

1. Enable the serial EEPROM Chip Select, EECS, by writing 1 to the Serial EEPROM Chip Select bit (CNTRL[25]=1).
2. Generate the serial EEPROM clock by writing 0 and then 1. The data is read or written during the zero-to-one transition. (Refer to CNTRL[24].)
3. Send the command code to the serial EEPROM.
4. If the serial EEPROM is present, 0 is returned as a Start bit after the command code.
5. Read or write the data.
6. Write 0 to CNTRL[25] to end serial EEPROM access (the serial EEPROM EECS pin goes low).

3.3.1 Serial EEPROM Load Sequence

The serial EEPROM load sequence, listed in Table 3-2, uses the following abbreviations:

- **MSW** = Most Significant Word bits [31:16]
- **LSW** = Least Significant Word bits [15:0]

3.3.1.1 Serial EEPROM Load

The registers listed in Table 3-2 are loaded from the serial EEPROM after a PCI reset is de-asserted. The serial EEPROM is organized in words (16-bit). The PCI 9052 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9052 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9052 loads the Device ID, Vendor ID, Class Code, and so forth.

The serial EEPROM values can be programmed using a serial EEPROM programmer or PLXMon™ software.

The CNTRL register allows programming of the serial EEPROM, one bit at a time. Values should be programmed in the order listed in Table 3-2. The 50, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

3.3.1.2 Recommended Serial EEPROMs

The PCI 9052 is designed to use serial EEPROMs with a three-wire serial interface, powered at 5V, and that support 1 MHz clocking and sequential reads.

For specific EEPROM recommendations, refer to the EEPROM Guidelines posted on the PLX website, http://www.plxtech.com/products/default.htm.

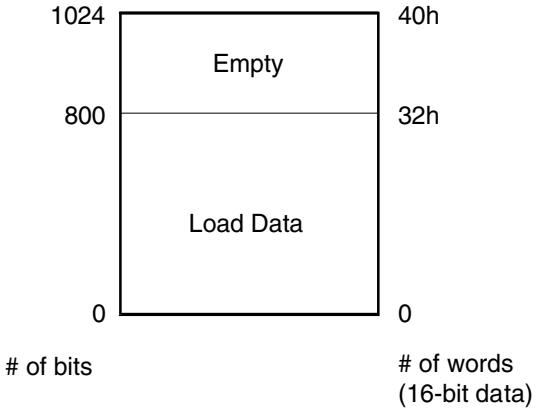


Figure 3-1. Serial EEPROM Memory Map

Note: *Serial EEPROM values shown are register values for the PCI 9052RDK.*

Table 3-2. Serial EEPROM Register Load Sequence

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Description
0h	PCI 02h	5201	Device ID
2h	PCI 00h	10B5	Vendor ID
4h	PCI 0Ah	0680	Class Code
6h	PCI 08h	00xx	Class Code (revision is not loadable)
8h	PCI 2Eh	9050	Subsystem ID
Ah	PCI 2Ch	10B5	Subsystem Vendor ID
Ch	PCI 3Eh	xxxx	(Maximum Latency and Minimum Grant are not loadable)
Eh	PCI 3Ch	01xx	Interrupt Pin (Interrupt Line Routing is not loadable)
10h	LOCAL 02h	FFF0	MSW of Range for PCI-to-Local Address Space 0 (1 MB)
12h	LOCAL 00h	0000	LSW of Range for PCI-to-Local Address Space 0 (1 MB)
14h	LOCAL 06h	FFFF	MSW of Range for PCI-to-Local Address Space 1
16h	LOCAL 04h	FFF1	LSW of Range for PCI-to-Local Address Space 1
18h	LOCAL 0Ah	FFFE	MSW of Range for PCI-to-Local Address Space 2
1Ah	LOCAL 08h	0000	LSW of Range for PCI-to-Local Address Space 2
1Ch	LOCAL 0Eh	FFF0	MSW of Range for PCI-to-Local Address Space 3
1Eh	LOCAL 0Ch	0000	LSW of Range for PCI-to-Local Address Space 3
20h	LOCAL 12h	0000	MSW of Range for PCI-to-Local Expansion ROM (64 KB)
22h	LOCAL 10h	0000	LSW of Range for PCI-to-Local Expansion ROM (64 KB)
24h	LOCAL 16h	0000	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0
26h	LOCAL 14h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0
28h	LOCAL 1Ah	0000	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1
2Ah	LOCAL 18h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1
2Ch	LOCAL 1Eh	0100	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2
2Eh	LOCAL 1Ch	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2
30h	LOCAL 22h	0200	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3
32h	LOCAL 20h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3
34h	LOCAL 26h	0000	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM
36h	LOCAL 24h	0000	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM
38h	LOCAL 2Ah	0040	MSW of Bus Region Descriptors for Local Address Space 0
3Ah	LOCAL 28h	0022	LSW of Bus Region Descriptors for Local Address Space 0
3Ch	LOCAL 2Eh	0000	MSW of Bus Region Descriptors for Local Address Space 1
3Eh	LOCAL 2Ch	0022	LSW of Bus Region Descriptors for Local Address Space 1
40h	LOCAL 32h	0080	MSW of Bus Region Descriptors for Local Address Space 2
42h	LOCAL 30h	0001	LSW of Bus Region Descriptors for Local Address Space 2
44h	LOCAL 36h	5421	MSW of Bus Region Descriptors for Local Address Space 3
46h	LOCAL 34h	38E9	LSW of Bus Region Descriptors for Local Address Space 3
48h	LOCAL 3Ah	0000	MSW of Bus Region Descriptors for Expansion ROM
4Ah	LOCAL 38h	0000	LSW of Bus Region Descriptors for Expansion ROM
4Ch	LOCAL 3Eh	0008	MSW of Chip Select (CS) 0 Base and Range
4Eh	LOCAL 3Ch	0001	LSW of Chip Select (CS) 0 Base and Range
50h	LOCAL 42h	0000	MSW of Chip Select (CS) 1 Base and Range

Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Description
52h	LOCAL 40h	0009	LSW of Chip Select (CS) 1 Base and Range
54h	LOCAL 46h	0101	MSW of Chip Select (CS) 2 Base and Range
56h	LOCAL 44h	0001	LSW of Chip Select (CS) 2 Base and Range
58h	LOCAL 4Ah	0208	MSW of Chip Select (CS) 3 Base and Range
5Ah	LOCAL 48h	0001	LSW of Chip Select (CS) 3 Base and Range
5Ch	LOCAL 4Eh	0000	MSW of Interrupt Control/Status
5Eh	LOCAL 4Ch	1043	LSW of Interrupt Control/Status
60h	LOCAL 52h	007C	MSW of User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control
62h	LOCAL 50h	4252	LSW of User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control

3.4 INTERNAL REGISTERS

The PCI 9052 chip provides several internal registers, allowing maximum flexibility in bus interface design and performance. The register types are as follows:

- PCI Configuration registers (accessible from the PCI Bus and serial EEPROM)
- Local Configuration registers (accessible from the PCI Bus and serial EEPROM)

Note: *Local Configuration register access can be limited to Memory- or I/O-Mapped. Access can also be disabled by way of the PCIBAR1 and PCIBAR0 Enable bits (CNTRL[13:12]). These bits should not be disabled for the PC platform.*

3.4.1 PCI Configuration Registers

Device and Vendor IDs. There are two sets of Device and Vendor IDs. The Device ID and Vendor ID are located at offset 00h of the PCI Configuration registers (PCIIDR[31:16] and PCIIDR[15:0], respectively). The Subsystem ID and Subsystem Vendor ID are located at offsets 2Eh and 2Ch, respectively, of the PCI Configuration registers (PCISID[15:0] and PCISVID [15:0], respectively). The Device ID and Vendor ID identify the particular device and its manufacturer. The Subsystem Vendor ID and Subsystem ID provide a way to distinguish between PCI interface chip vendors and add-in board manufacturers, using a PCI chip.

Note: *Subsystem ID and Subsystem Vendor ID registers at Configuration offset 2Ch are writable by serial EEPROM only. However, if a PCI master writes to these read-only registers, the value is written to offset 3Ch, the PCI Interrupt Line register (PCIILR), possibly disabling PCI interrupts originating from the PCI 9052. (Refer to PCI 9052 Errata #3.)*

Status. This register contains PCI Bus-related events information.

Command. This register controls the ability of a device to respond to PCI accesses. It controls whether the device responds to I/O or Memory Space accesses.

Class Code. This register identifies the general function of the device. (Refer to *PCI r2.2* for further details.)

Revision ID. The value read from this register represents the PCI 9052 current silicon revision.

Header Type. This register defines the device configuration header format and whether the device is single function or multi-function.

Note: *Multiple functions are not supported.*

Cache Line Size. This register defines the system cache line size in units of 32-bit Lwords.

PCI Base Address for Memory Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI Address space segment for Memory accesses to the PCI 9052 Local Configuration registers. The PCI Address Range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the Host writes FFFFFFFF to this register, then reads back FFFFFF80, determining the required Memory space of 128 bytes. The Host then writes the base address to PCIBAR0[31:7].

PCI Base Address for I/O Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI address space segment for I/O accesses to the PCI 9052 Local Configuration registers. The PCI address range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF81, determining a required 128 bytes of I/O space. The Host then writes the base address to PCIBAR1[31:7].

PCI Base Address for Accesses to Local Address Spaces 0, 1, 2, and 3. The system BIOS uses these registers to assign a PCI address space segment for accesses to Local Address Space 0, 1, 2, and 3. The PCI address range occupied by this space is determined by the Local Address Space Range registers. During initialization, the host writes FFFFFFFF to these registers, then reads back a value determined by the range. The Host then writes the base address to the upper bits of these registers.

PCI Expansion ROM Base Address. The system BIOS uses this register to assign a PCI address space segment for accesses to the Expansion ROM. The PCI address range occupied by this space is determined by the Expansion ROM Range register. During initialization, the host writes FFFFFFFF to this register, then reads back a value determined by the range. The Host then writes the base address to the upper bits of this register.

PCI Interrupt Line. This register identifies where the device interrupt line connects on the system interrupt controller(s).

PCI Interrupt Pin. This register specifies the interrupt request pin (if any) to be used.

3.4.2 PCI Bus Access to Internal Registers

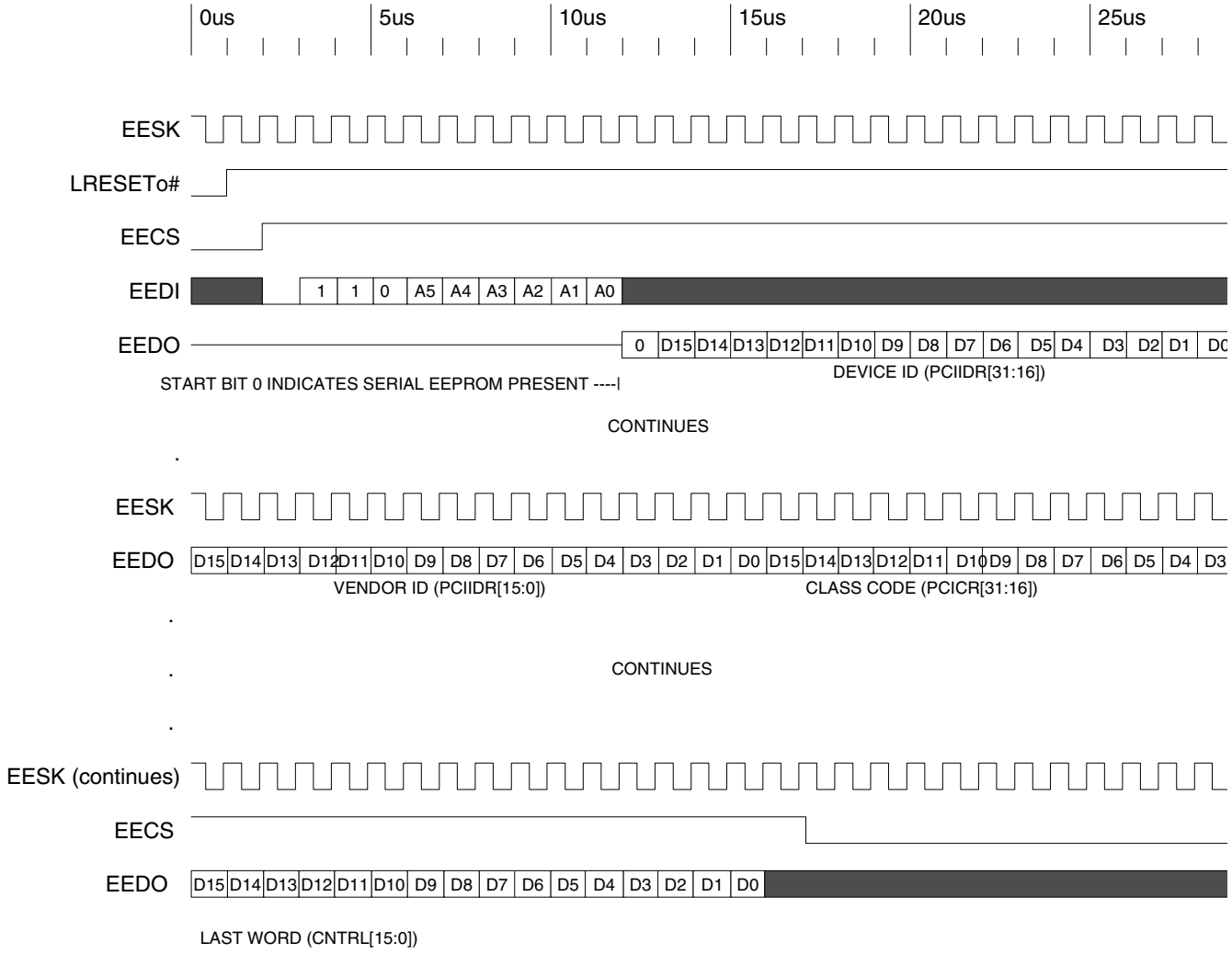
The PCI 9052 PCI Configuration registers are accessed from the PCI Bus with a Type 0 Configuration cycle.

The PCI 9052 Local Configuration registers are accessed by one of the following:

- A Memory cycle, with the PCI Bus address matching the base address specified in the PCI Base Address register for Memory Accesses to Local Configuration registers (PCIBAR0)
- An I/O cycle, with the PCI Bus address matching the base address specified in the PCI Base Address register for I/O Accesses to Local Configuration registers (PCIBAR1)

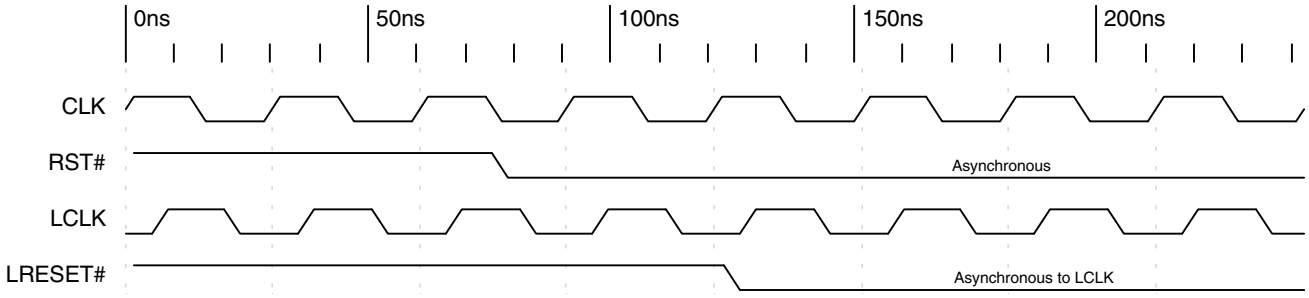
All PCI Read or Write accesses to the PCI 9052 registers can be Byte, Word, or Lword accesses. Memory accesses to the PCI 9052 registers can be burst or non-burst. The PCI 9052 responds with a PCI Bus disconnect for all Burst I/O accesses to the PCI 9052 registers.

3.5 TIMING DIAGRAMS



Note: Serial EEPROM initialization completes in approximately 780 µs, with a 33.3 MHz PCI clock.

Timing Diagram 3-1. Initialization from Serial EEPROM



Timing Diagram 3-2. PCI RST# Asserting Local Output LRESET#

4 DIRECT SLAVE OPERATION

The functional operation described can be modified through the PCI 9052 programmable internal registers.

4.1 OVERVIEW

Direct Slave operations originate on the PCI Bus, go through the PCI 9052, and finally access the Local Bus. The PCI 9052 is a PCI Bus slave and a Local Bus master.

4.2 DIRECT DATA TRANSFER MODE

The PCI 9052 supports Direct Slave accesses to Local Memory by way of Memory or I/O transfers.

4.2.1 Direct Slave Operation (PCI Master-to-Local Bus Access)

The PCI 9052 supports Burst Memory-Mapped Transfer accesses and single Memory- or I/O-Mapped Transfer accesses to the Local Bus from the PCI Bus through an 8-Lword (32-byte) Direct Slave Read FIFO and a 16-Lword (64-byte) Direct Slave Write FIFO. The PCI Base Address registers are provided to set up the adapter location in the PCI Memory and I/O space. In addition, Local Mapping registers allow address translation from the PCI Address Space to the Local Address Space. The following five spaces are available:

- Space 0
- Space 1
- Space 2
- Space 3
- Expansion ROM

Expansion ROM is intended to support a bootable ROM device for the Host.

For single cycle Direct Slave reads, the PCI 9052 reads a single Local Bus Lword or partial Lword. The PCI 9052 disconnects after one transfer for all Direct Slave I/O accesses.

Note: *If no PCI Byte Enables (C/BE[3:0]#) are asserted with an I/O Command access, the PCI 9052 issues a Target Abort.*

For higher data transfer rates, the PCI 9052 can be programmed to prefetch data during a PCI Burst read. The Prefetch size, when enabled, can be 4, 8, or 16 Lwords, or until the PCI Bus stops requesting. When the PCI 9052 prefetches, if enabled, it drops the Local Bus read after reaching the prefetch count. In Continuous Prefetch mode, the PCI 9052 prefetches as long as FIFO space is available and stops prefetching when the PCI Bus terminates the request. If Read prefetching is disabled, the PCI 9052 stops after one Read transfer.

In addition to Prefetch mode, the PCI 9052 supports Direct Slave Read Ahead mode. (Refer to Section 4.2.1.3.)

Each Local space can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width. The PCI 9052 contains an internal wait state generator and external wait state input, LRDYi#. LRDYi# can be disabled or enabled by way of the Internal Configuration registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can:

- Burst as long as data is available (Continuous Burst mode)
- Burst four Lwords at a time (Burst-4 Lword mode)
- Perform continuous single cycles

4.2.1.1 Direct Slave Lock

The PCI 9052 supports direct PCI-to-Local Bus Exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire Local Address Spaces 0, 1, 2, and 3, and Expansion ROM being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the Direct Slave LOCK# Enable bit (CNTRL[23]) for PCI-to-Local accesses.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. *For example*, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the Local Bus to other masters until the locked operation is complete.

4.2.1.2 *PCI r2.1* Features Enable

The PCI 9052 can be programmed through the *PCI r2.1* Features Enable bit (CNTRL[14]) to perform all PCI Read/Write transactions in compliance with *PCI r2.1*. The following PCI 9052 behavior occurs when CNTRL[14]=1.

4.2.1.2.1 Direct Slave Delayed Read Mode Operation

PCI Bus single cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a one-Lword single-cycle transfer on the Local Bus, with corresponding Local Byte Enables (LBE[3:0]#) asserted to reflect PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (CNTRL[16]=1). (Refer to Section 4.2.1.3.) This causes the PCI 9052 to Retry all PCI Bus Read requests that follow, until the original PCI Address and/or Byte Enables (C/BE[3:0]#) are matched. (Refer to Figure 4-1.)

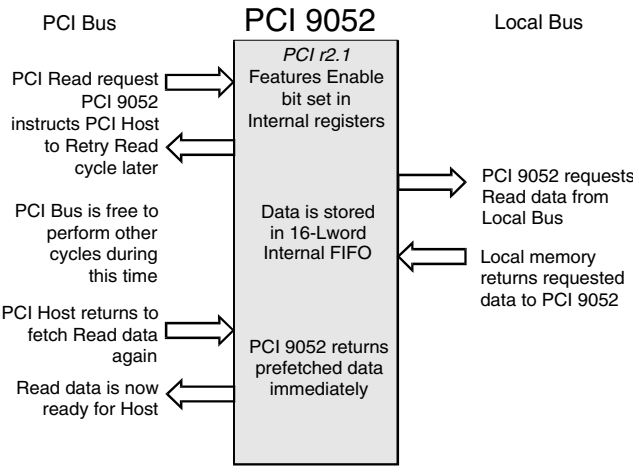


Figure 4-1. Direct Slave Delayed Read Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.2.2 32000 PCI Clock Timeout

If the PCI Master does not complete the originally requested Direct Slave Delayed Read transfer, the PCI 9052 flushes the Direct Slave Read FIFO after 32000 PCI clocks and grants an access to a new Direct Slave Read access. The PCI 9052 Retries all other Direct Slave Read accesses that occur before the 32000 PCI clock timeout.

4.2.1.2.3 *PCI r2.1* 16- and 8-Clock Rule

The PCI 9052 guarantees that if the first Direct Slave Write data cannot be accepted by the PCI 9052 and/or the first Direct Slave Read data cannot be returned by the PCI 9052 within 16 PCI clocks from the beginning of the Direct Slave cycle (FRAME# asserted), the PCI 9052 issues a Retry (STOP# asserted) to the PCI Bus.

During successful Direct Slave Read and/or Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in eight PCI clocks (TRDY# asserted). Otherwise, the PCI 9052 issues a PCI disconnect (STOP# asserted) to the PCI Master.

In addition, setting the *PCI r2.1* Features Enable bit [CNTRL[14]=1) allows optional enabling of the following *PCI r2.1* functions:

- No write while a Delayed Read is pending (PCI Retries for writes) (CNTRL[17])
- Write and flush pending Delayed Read (CNTRL[15])

4.2.1.3 Direct Slave Read Ahead Mode

The PCI 9052 also supports Direct Slave Read Ahead mode (CNTRL[16]), where prefetched data can be read from the PCI 9052 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). The Direct Slave Read Ahead mode functions can be used with or without Direct Slave Delayed Read mode. (Refer to Figure 4-2.)

Read Ahead mode requires that Prefetch be enabled in the LAS*x*BRD registers (where *x* is the Local Address Space number) for the Memory-Mapped spaces that use Read Ahead mode. The PCI 9052 flushes its Read FIFO for each I/O-Mapped access.

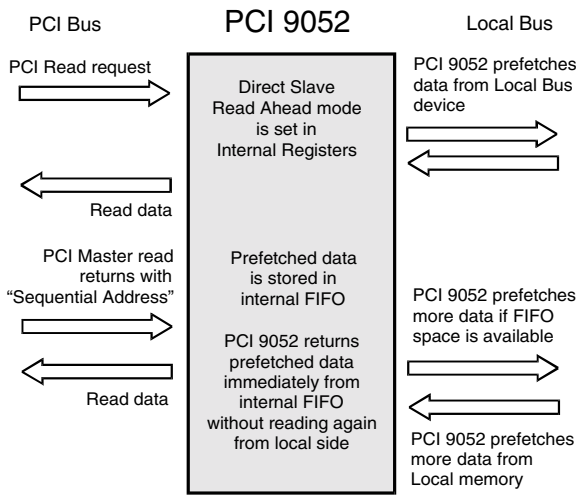


Figure 4-2. Direct Slave Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.4 Direct Slave Transfer

A PCI Bus Master addressing the Memory space decoded for the Local Bus initiates transactions. Upon a PCI Read/Write, the PCI 9052 being a Local Bus Master executes a transfer, at which time it reads data into the Direct Slave Read FIFO or writes data to the Local Bus.

For a PCI Direct access to the Local Bus, the PCI 9052 has a 16-Lword (64-byte) Write FIFO and an 8-Lword (32-byte) Read FIFO. The FIFOs enable the Local Bus to operate independently of the PCI Bus.

For Write transfers, if the Write FIFO becomes full, the PCI 9052 is programmable to disconnect, or retain the PCI Bus while generating wait states (TRDY# de-asserted) (CNTRL[18]).

For PCI Read transactions from the Local Bus, the PCI 9052 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9052 prefetches up to 16 Lwords (in Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9052 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a single Address/Data cycle on the Local Bus.

The PCI Direct Slave Retry Delay Clocks bits (CNTRL[22:19]) can be used to program the period of time in which the PCI 9052 holds off TRDY#. The PCI 9052 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9052 cannot gain Local Bus control and return TRDY# within the programmed time period or the Local Bus is slowly emptying the Write FIFO, and filling the Read FIFO.

The PCI 9052 supports on-the-fly Endian conversion for Local Address Spaces 0, 1, 2, and 3, and Expansion ROM. The Local Bus can be Big/Little Endian by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*

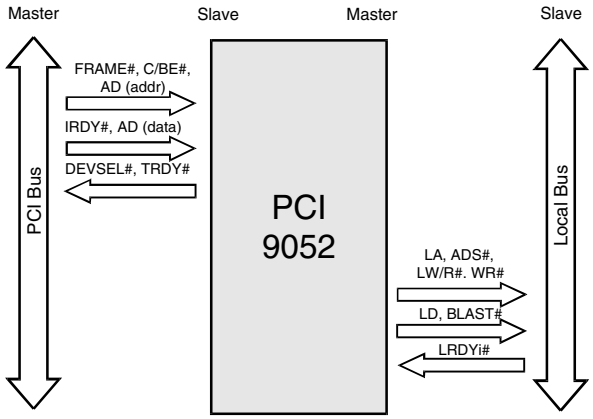


Figure 4-3. Direct Slave Write

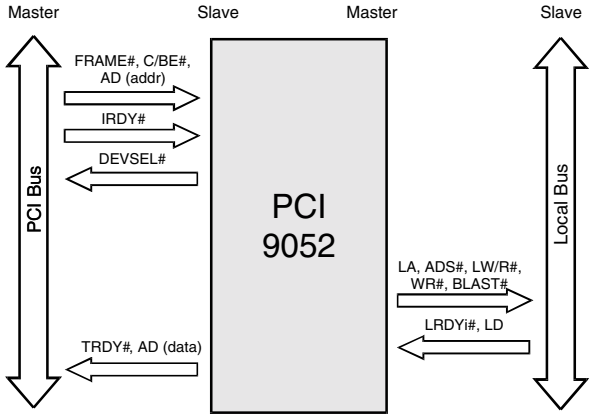


Figure 4-4. Direct Slave Read

Note: *The figures represent a sequence of Bus cycles.*

4.2.1.5 Direct Slave PCI-to-Local Address Mapping

Five Local Address spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- **Local Address Range**—LAS0RR, LAS1RR, LAS2RR, LAS3RR, and/or EROMRR
- **Local Base Address**—LAS0BA, LAS1BA, LAS2BA, LAS3BA, and/or EROMBA
- **PCI Base Address**—PCIBAR2, PCIBAR3, PCIBAR4, PCIBAR5, and/or PCIERBAR

A fourth register, the Bus Region Descriptor register for PCI-to-Local Accesses (LAS0BRD, LAS1BRD, LAS2BRD, LAS3BRD, and/or EROMBRD), defines the Local Bus characteristics for the Direct Slave regions. (Refer to Figure 4-5.)

Each PCI-to-Local Address space is defined as part of reset initialization. (Refer to Section 4.2.1.5.1.) These Local Bus characteristics can be modified at any time before actual data transactions.

4.2.1.5.1 Direct Slave Local Bus Initialization

Range—Specifies the PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits required to be included in decode, and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

4.2.1.5.2 Direct Slave Initialization

After a PCI reset and serial EEPROM load, the software determines the amount of required address space by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9052 returns zeros (0) in the Don't Care Address bits, effectively specifying the address space required, at which time the PCI software maps the Local Address space into the PCI Address space by programming the PCI Base Address register.

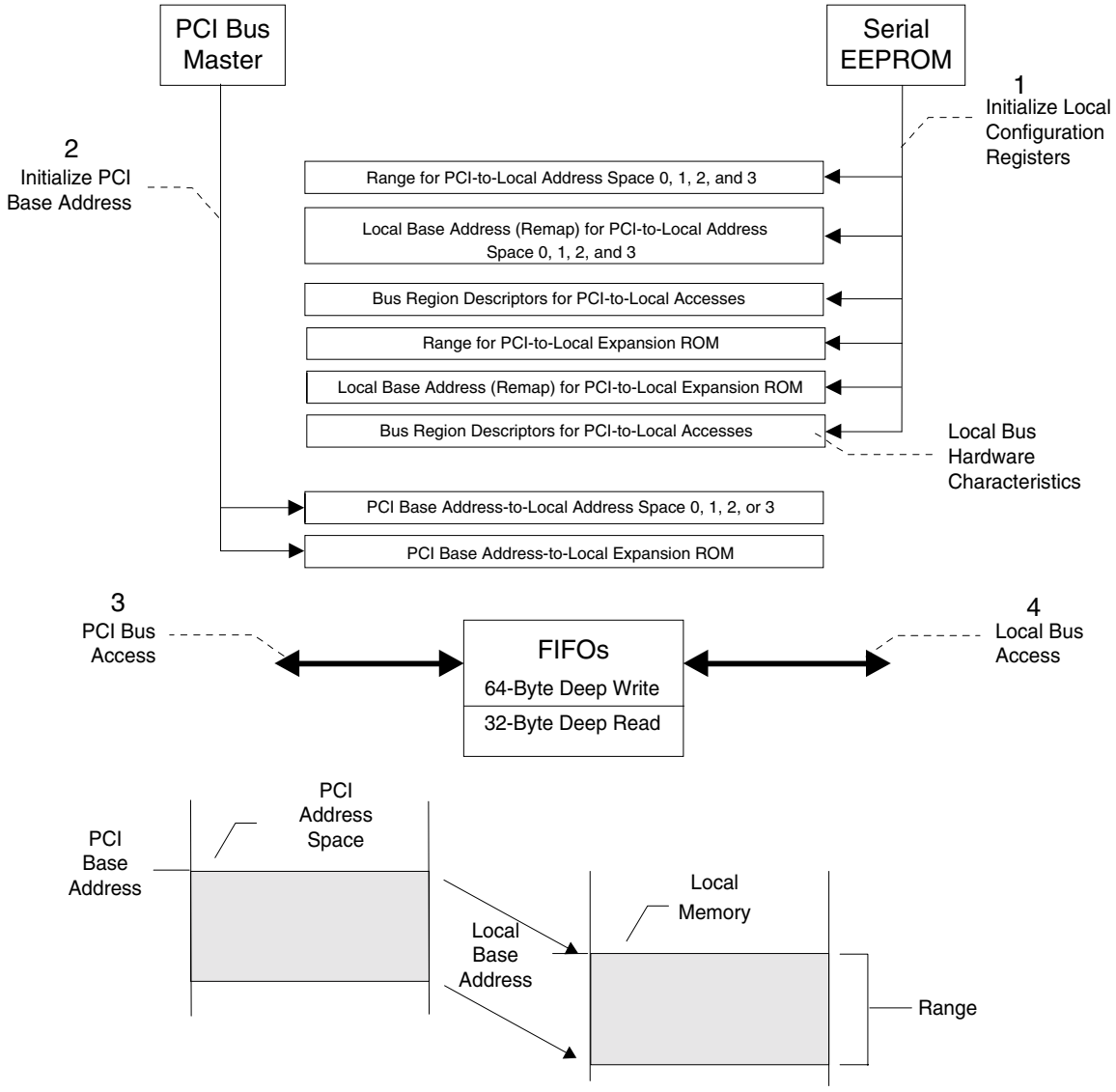


Figure 4-5. Local Bus Direct Slave Access

4.2.1.5.3 Direct Slave Example

A 1 MB prefetchable Local Address Space encompassing Local Bus Addresses 01200000h through 012FFFFFh is to be configured for Local Address Space 0. Assume the BIOS System Resource Manager allocates 1 MB with a PCI Base Address of 34500000h. The Local memory is then accessible at PCI Addresses 34500000h through 345FFFFFh.

a. Program the serial EEPROM as follows:
   - **Range**—FFF00008h [1 MB, decode the upper 12 PCI Address bits, and set the Prefetchable bit (LAS0RR[3]=1)].
   - **Local Base Address (Remap)**—01200001h (Local Base Address for PCI-to-Local accesses). Bit 0 must be set to enable address decoding (LAS0BA[0]=1).

b. PCI Initialization software writes all ones (1) to the PCI Base Address register, then reads it back.
   - The PCI 9052 returns a value of FFF00008h, after which the PCI software writes the base address it assigned into the PCI Base Address register(s).
   - **PCI Base Address**—34500008h (PCI Base Address for Access to Local Address Space 0 register, PCIBAR2). The PCI Base Address is always aligned on a boundary determined by address space size. The Prefetchable bit is set (PCIBAR2[3]=1).

4.2.1.5.4 Direct Slave Byte Enables (Non-Multiplexed Mode)

During a Direct Slave transfer, each of five spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# are encoded, based on the configured bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LA1 and LA0, respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

Note: *In ISA Interface mode (MODE=0 and INTCSR[12]=1), pins 46 through 49 have dual functionality, providing LBE[3:0]# for Local Address Spaces 2 and 3 and Expansion ROM, while providing ISAA0, ISAA1, and SBHE# signals for Local Address Spaces 0 and 1 (ISA Memory and I/O).*

4.2.1.5.5 Direct Slave Byte Enables (Multiplexed Mode)

During a Direct Slave transfer, each of five spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# are encoded, based on the configured Bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LAD1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LAD[1:0], respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Address bit 0 (LAD0)

During the address phase, LAD[1:0] are valid address bits with the same value as LBE[1:0]#.

4.3 RESPONSE TO FIFO FULL OR EMPTY

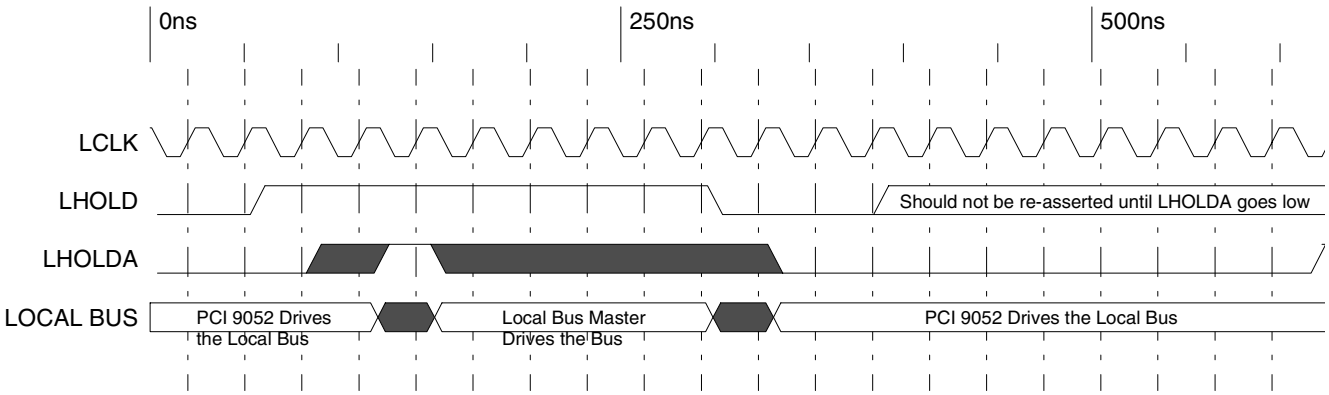
Table 4-1 lists the PCI 9052 response to full or empty FIFOs.

Table 4-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Slave Write	PCI-to-Local	Full	Disconnect or Throttle TRDY#[1]	De-assert LHOLDA if Local Bus is busy and wait for LHOLD to be de-asserted
		Empty	Normal	Normal, assert BLAST#
Direct Slave Read	Local-to-PCI	Full	Normal	Normal, assert BLAST#
		Empty	Disconnect or Throttle TRDY#[1]	Normal

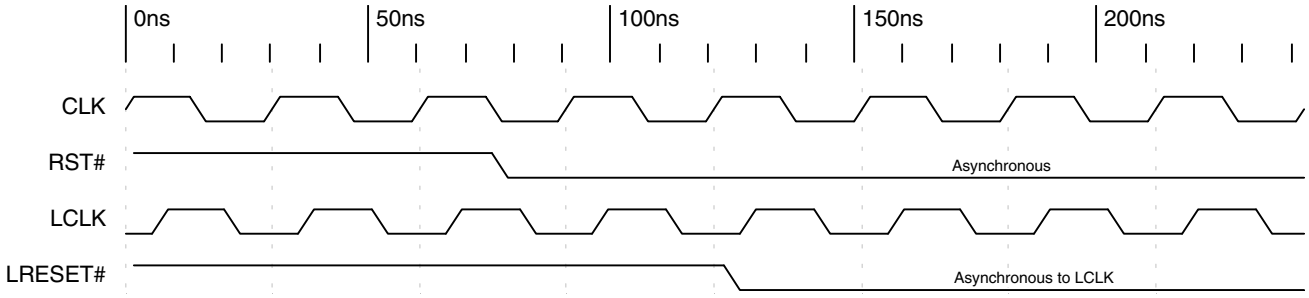
1. Throttle TRDY# depends on the PCI Direct Slave Retry Delay Clocks (CNTRL[22:19]).

4.4 TIMING DIAGRAMS

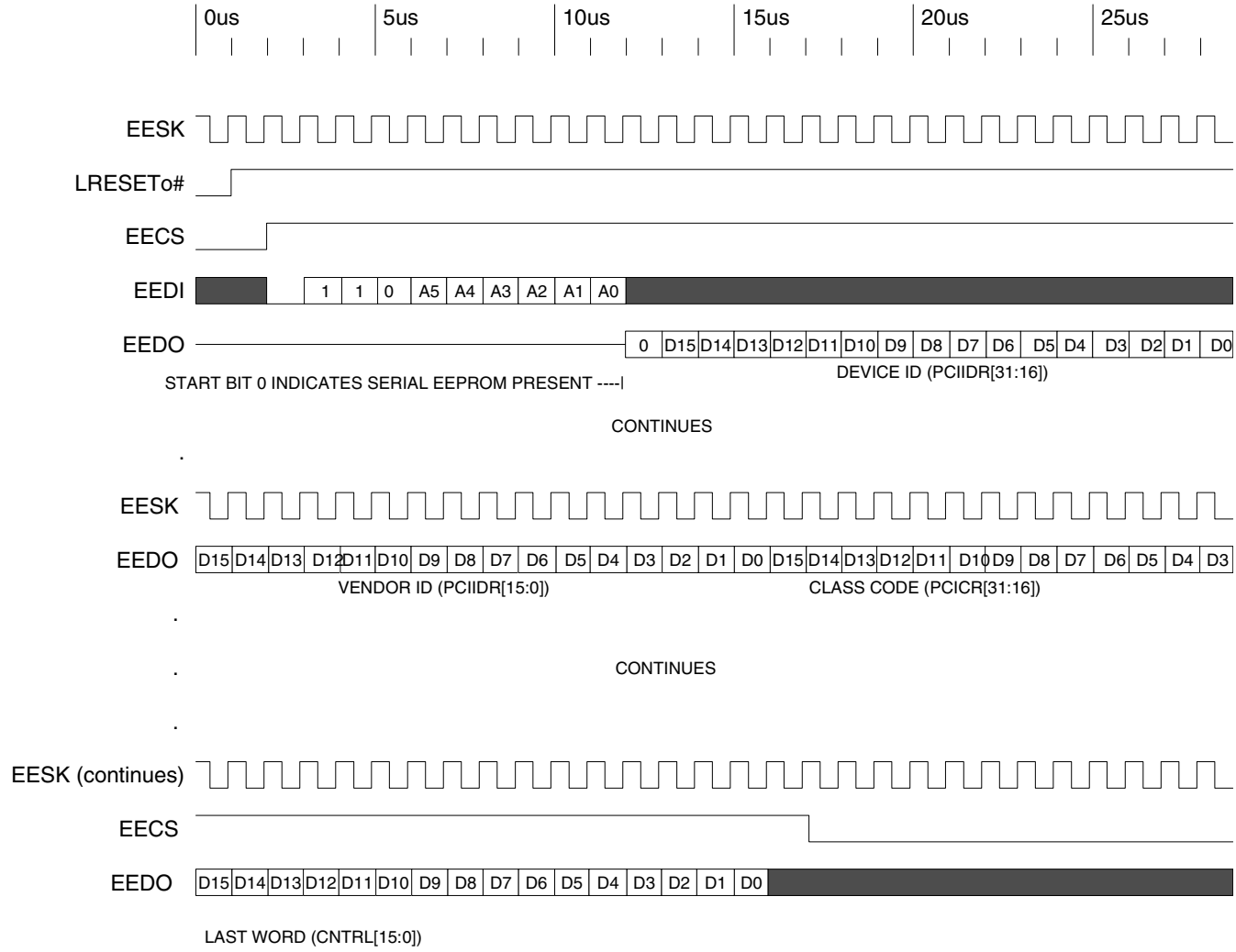


Timing Diagram 4-1. PCI 9052 Local Bus Arbitration

4.4.1 Serial EEPROM and Configuration Initialization

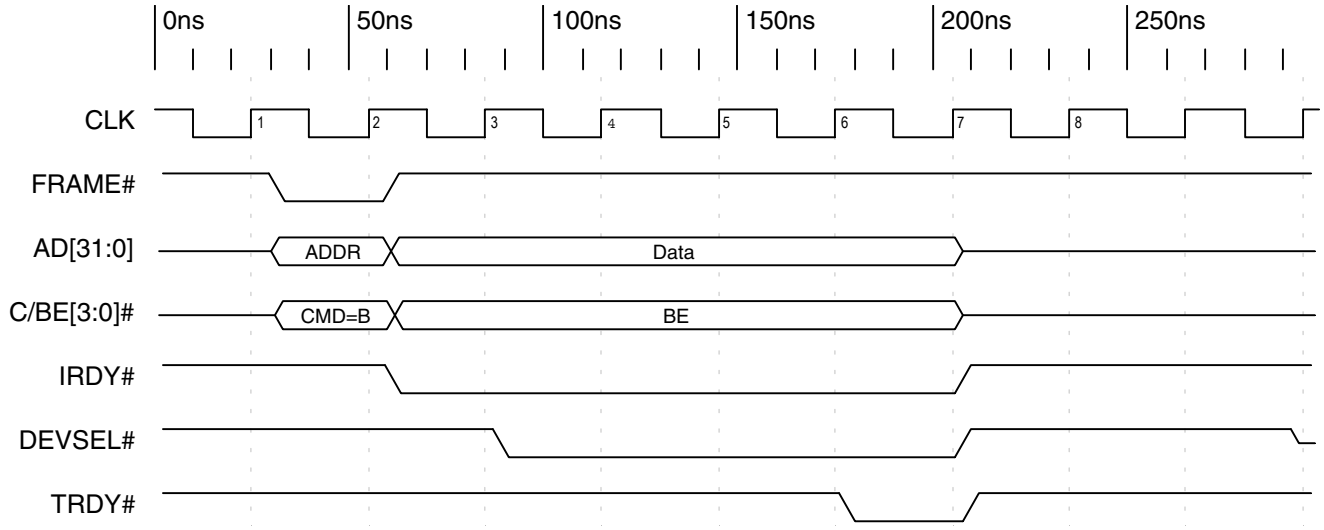


Timing Diagram 4-2. PCI RST# Asserting Local Output LRESET#

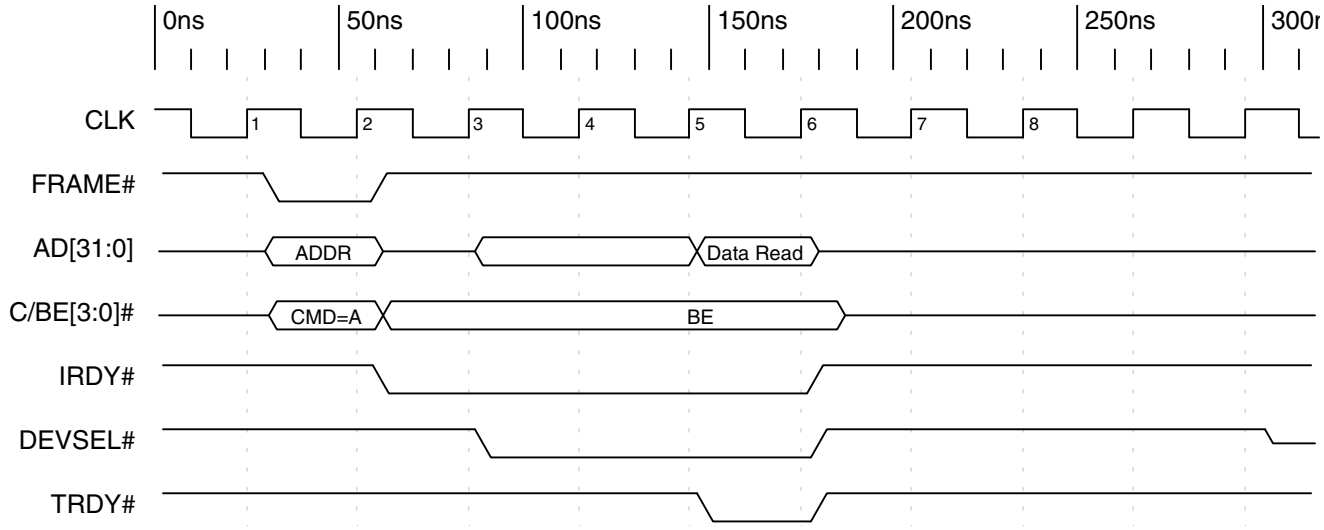


Note: Serial EEPROM initialization completes in approximately 780 µs, with a 33.3 MHz PCI clock.

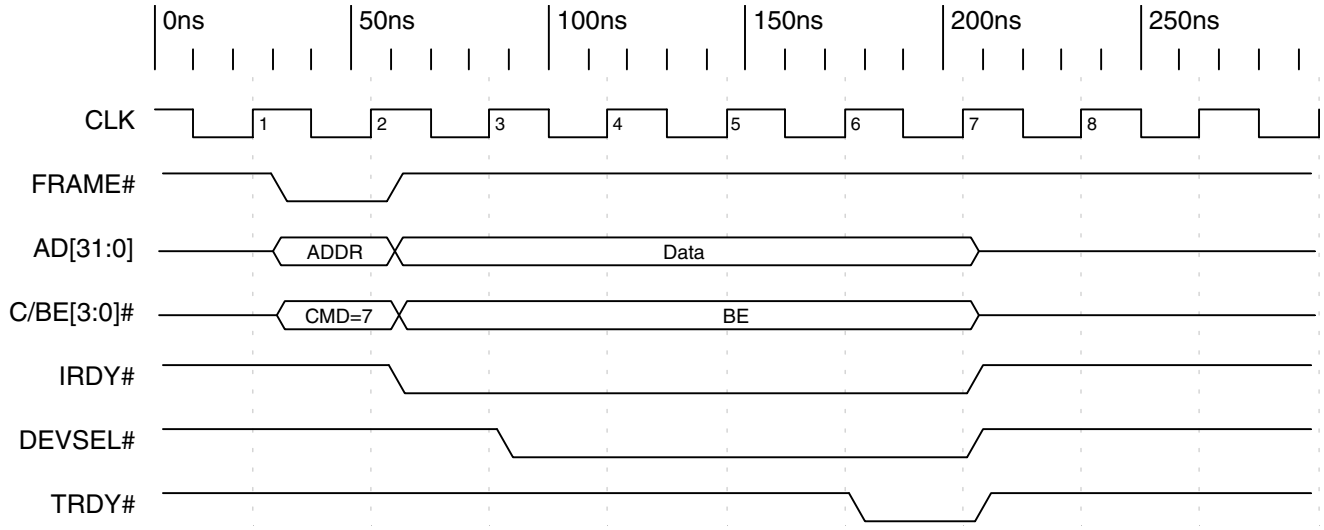
Timing Diagram 4-3. Initialization from Serial EEPROM



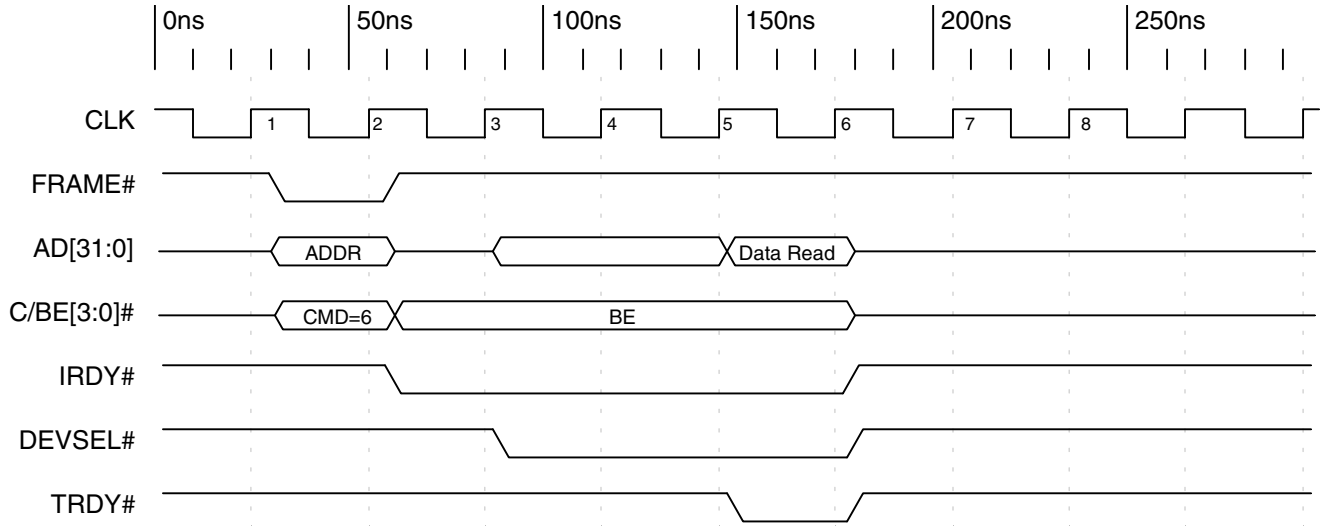
Timing Diagram 4-4. PCI Configuration Write to PCI Configuration Register



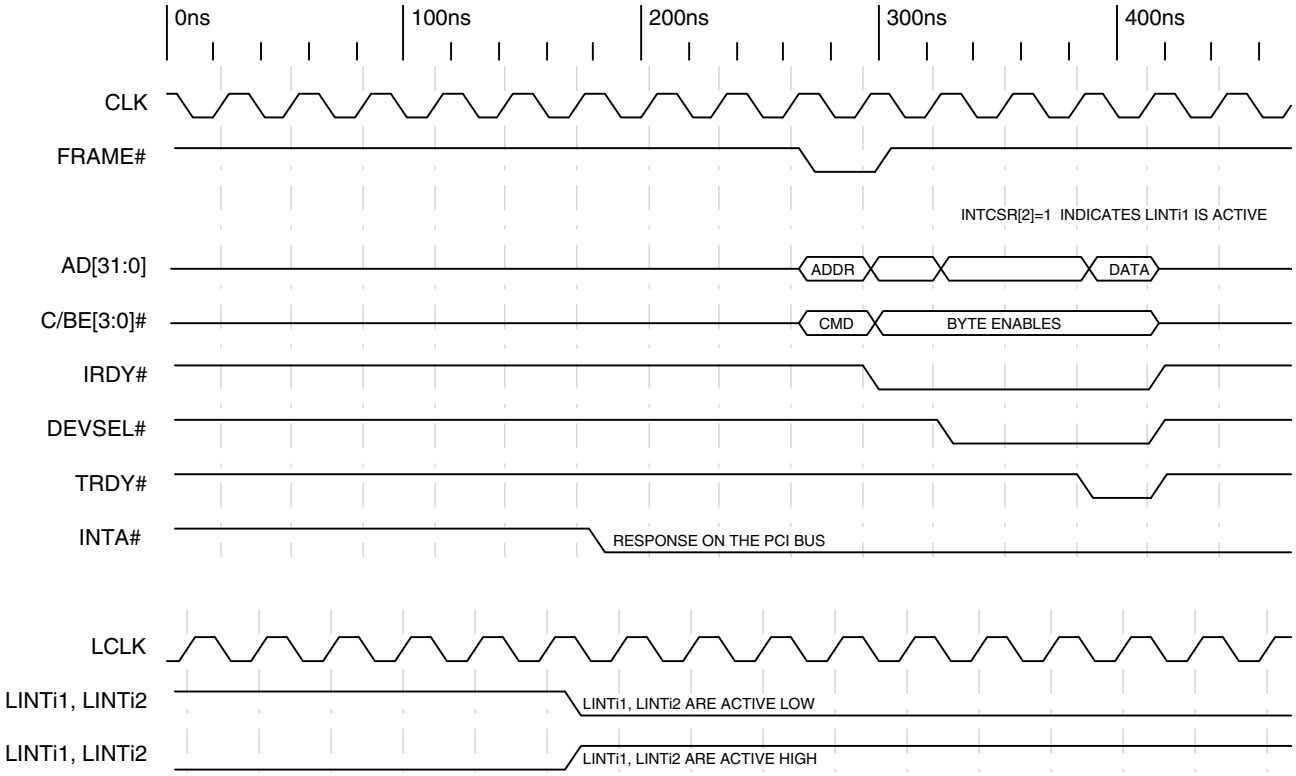
Timing Diagram 4-5. PCI Configuration Read from PCI Configuration Register



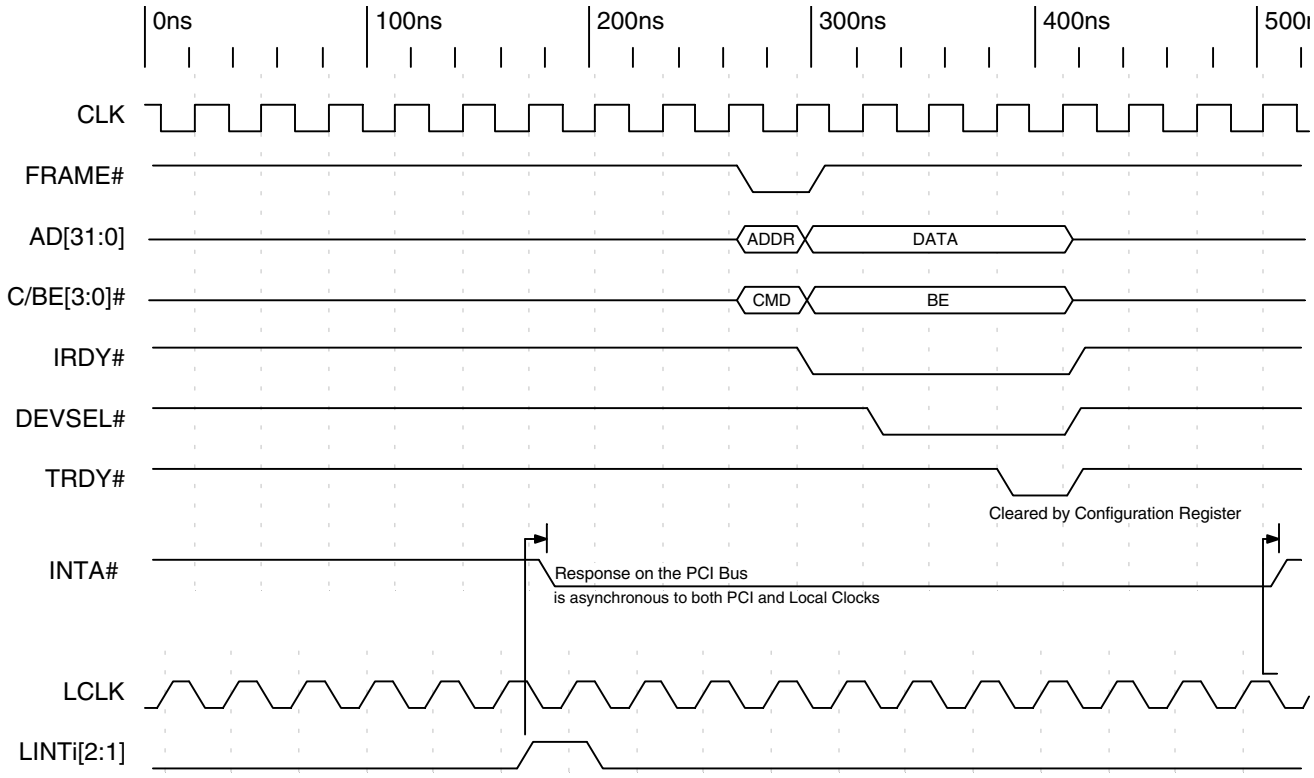
Timing Diagram 4-6. PCI Memory Write to Local Configuration Register



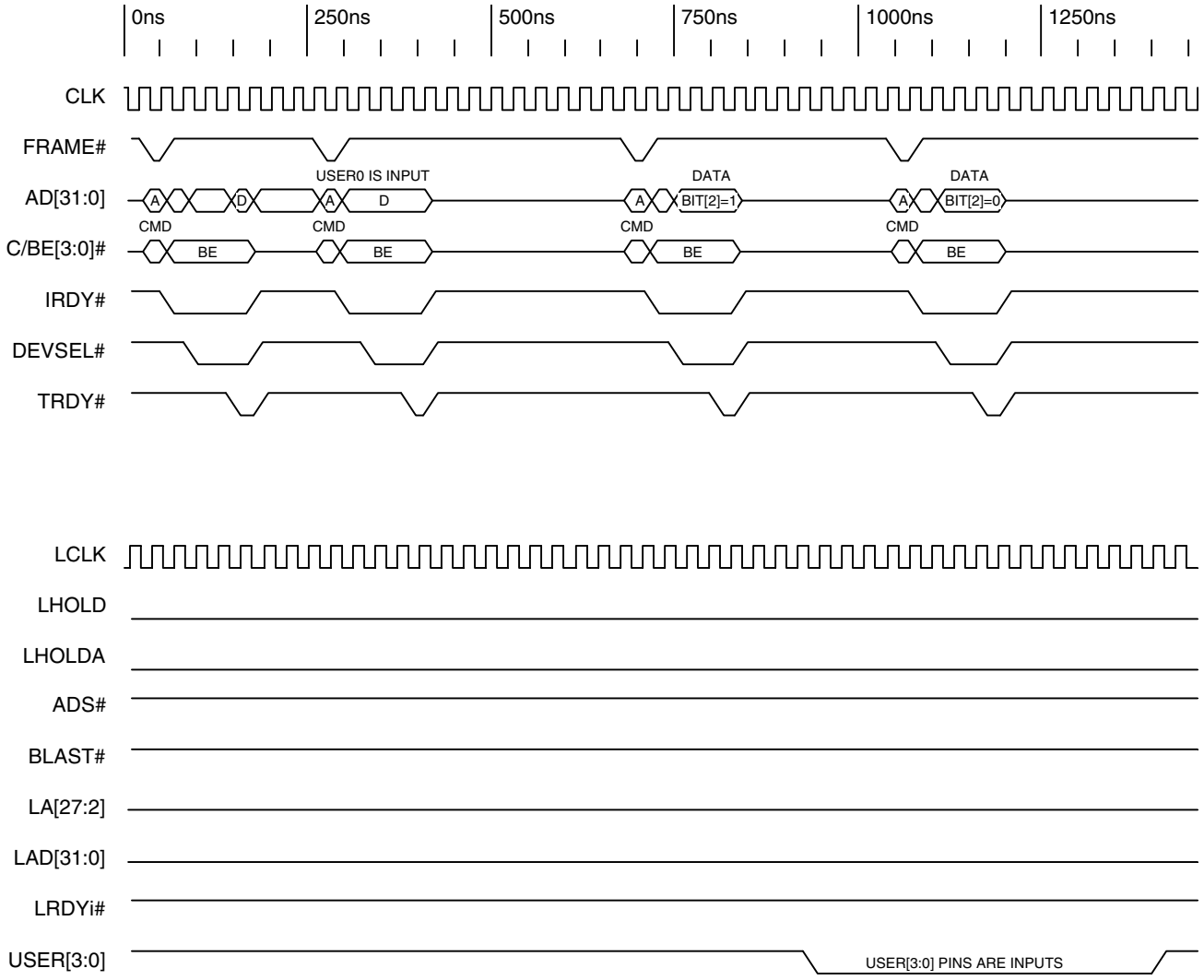
Timing Diagram 4-7. PCI Memory Read from Local Configuration Register



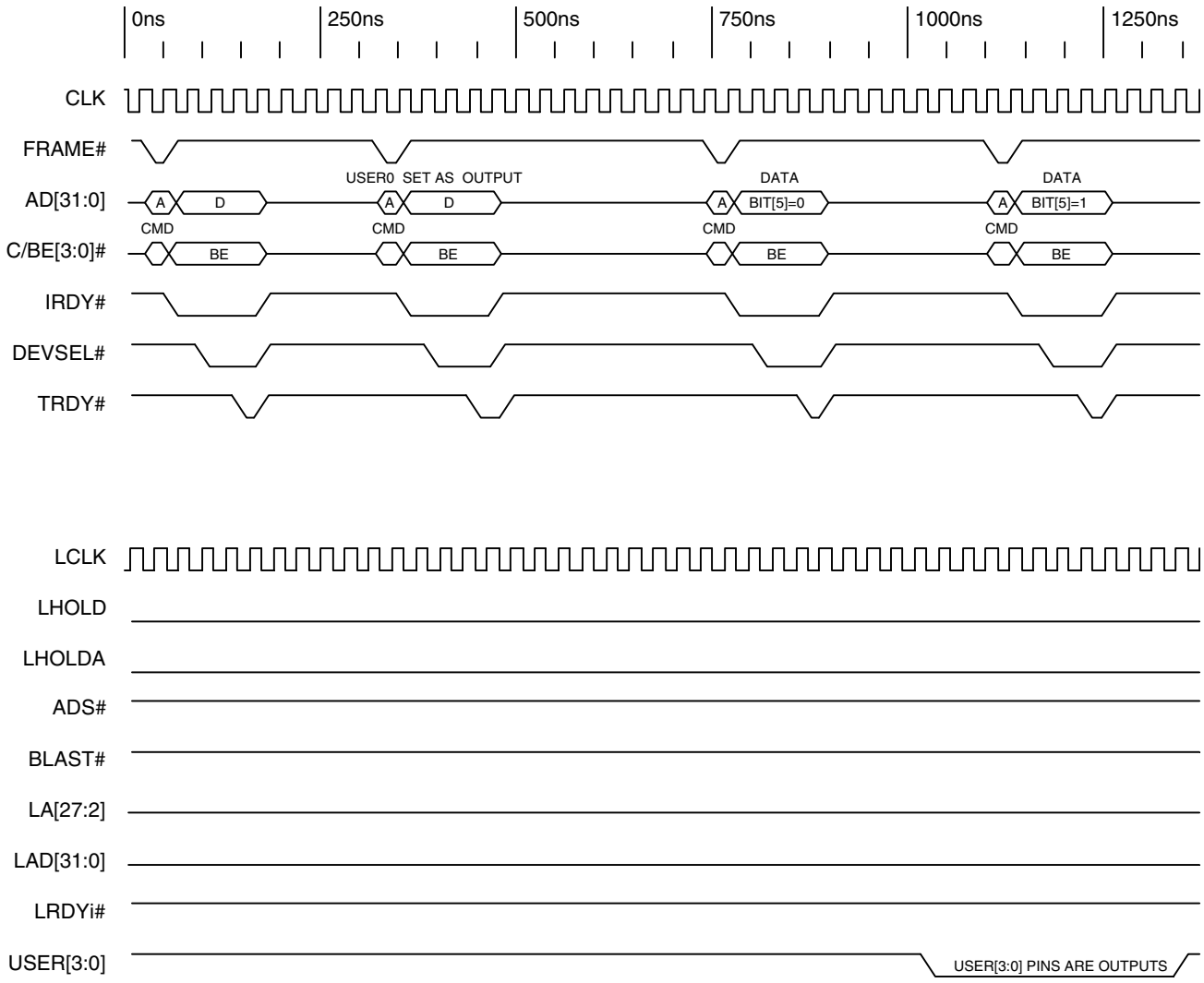
Timing Diagram 4-8. Local Level-Triggered LINTi/LINTi2 Asserting PCI Output INTA#



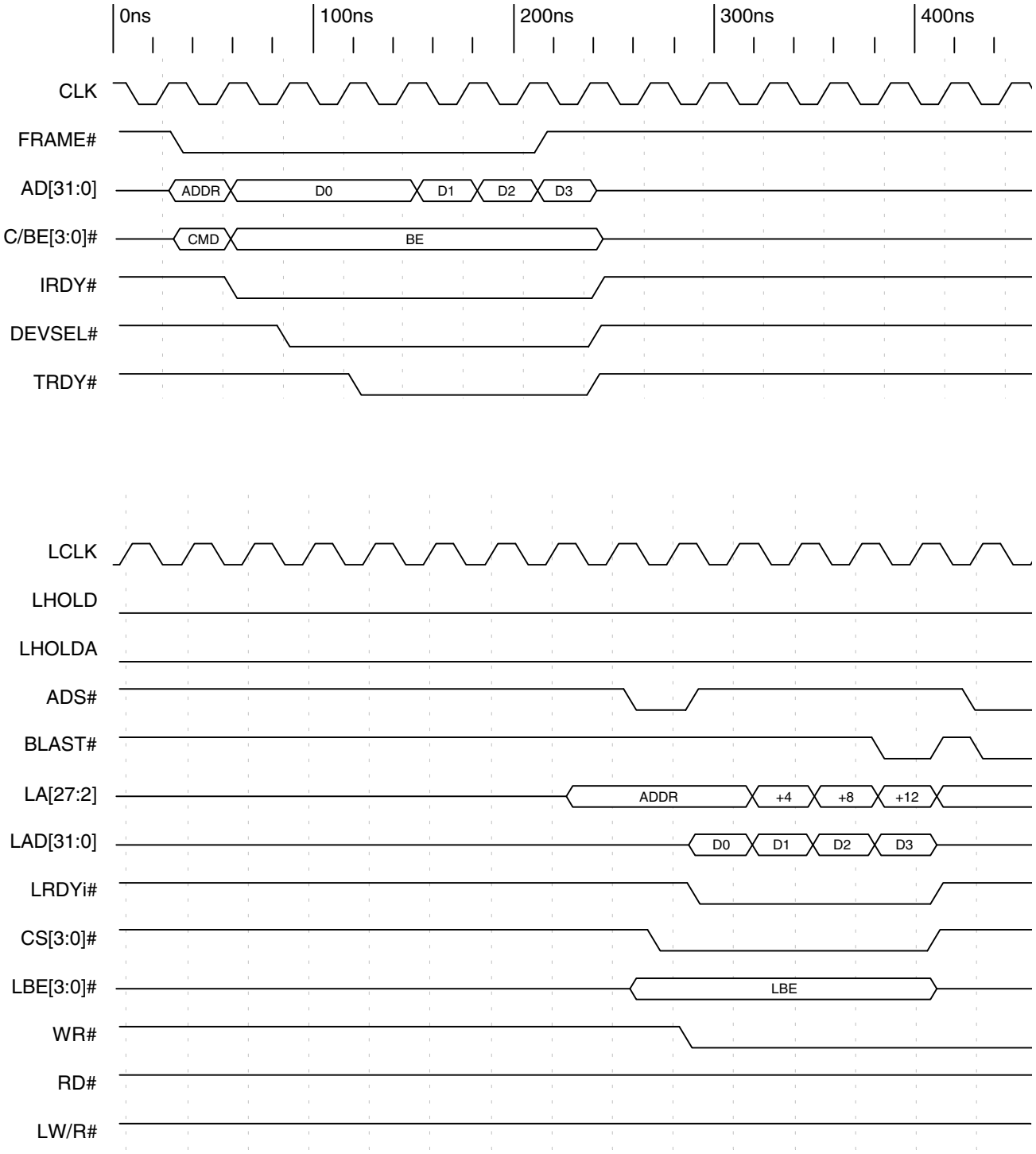
Timing Diagram 4-9. Local Edge-Triggered Interrupt Asserting PCI Interrupt



Timing Diagram 4-10. USER[3:0] as Inputs



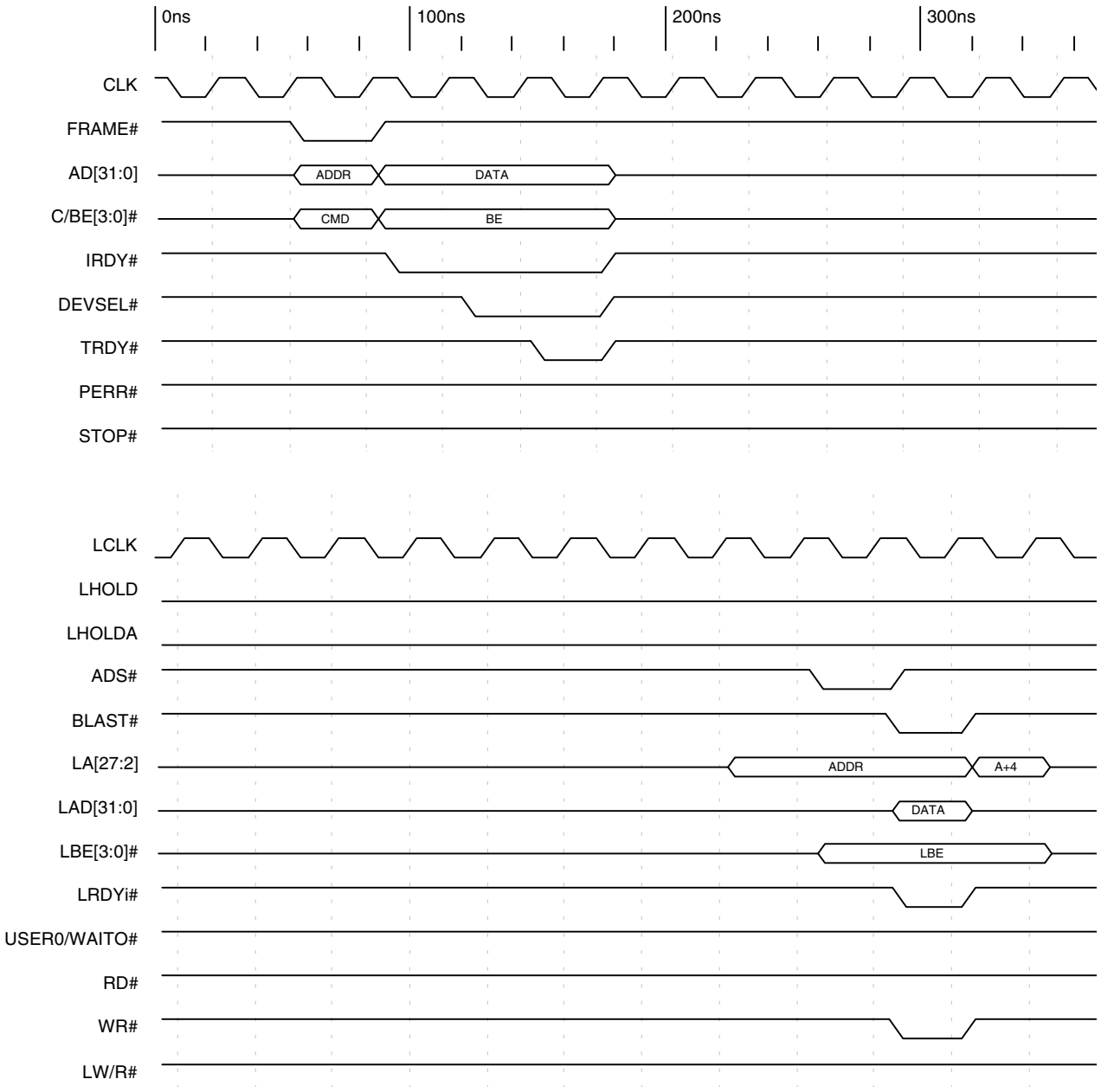
Timing Diagram 4-11. USER[3:0] as Outputs



Note: CS[3:0]# Base Address is in the range of Spaces 3 through 0

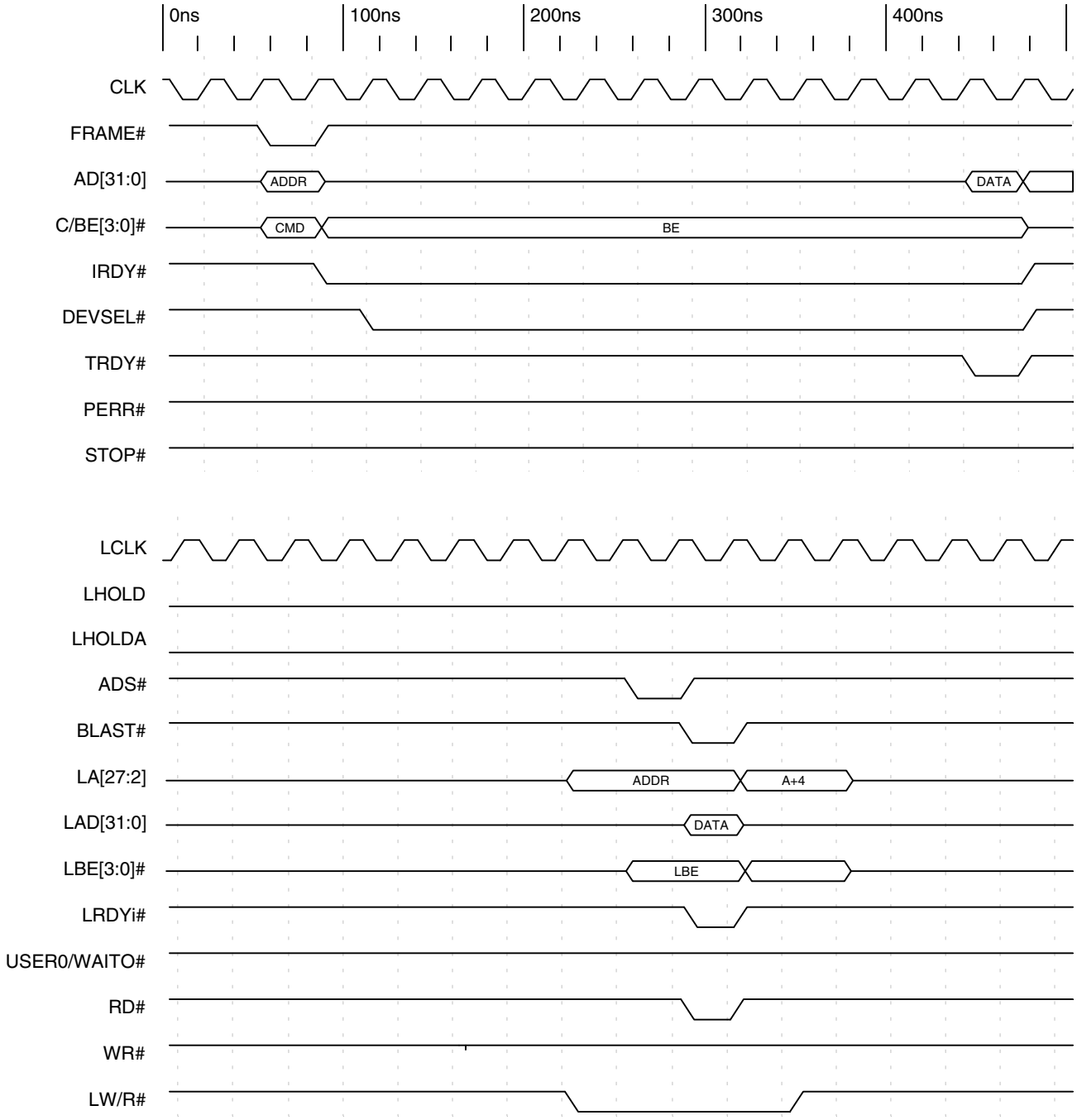
Timing Diagram 4-12. Chip Select [3:0]#

4.4.2 Non-Multiplexed Mode Local Bus



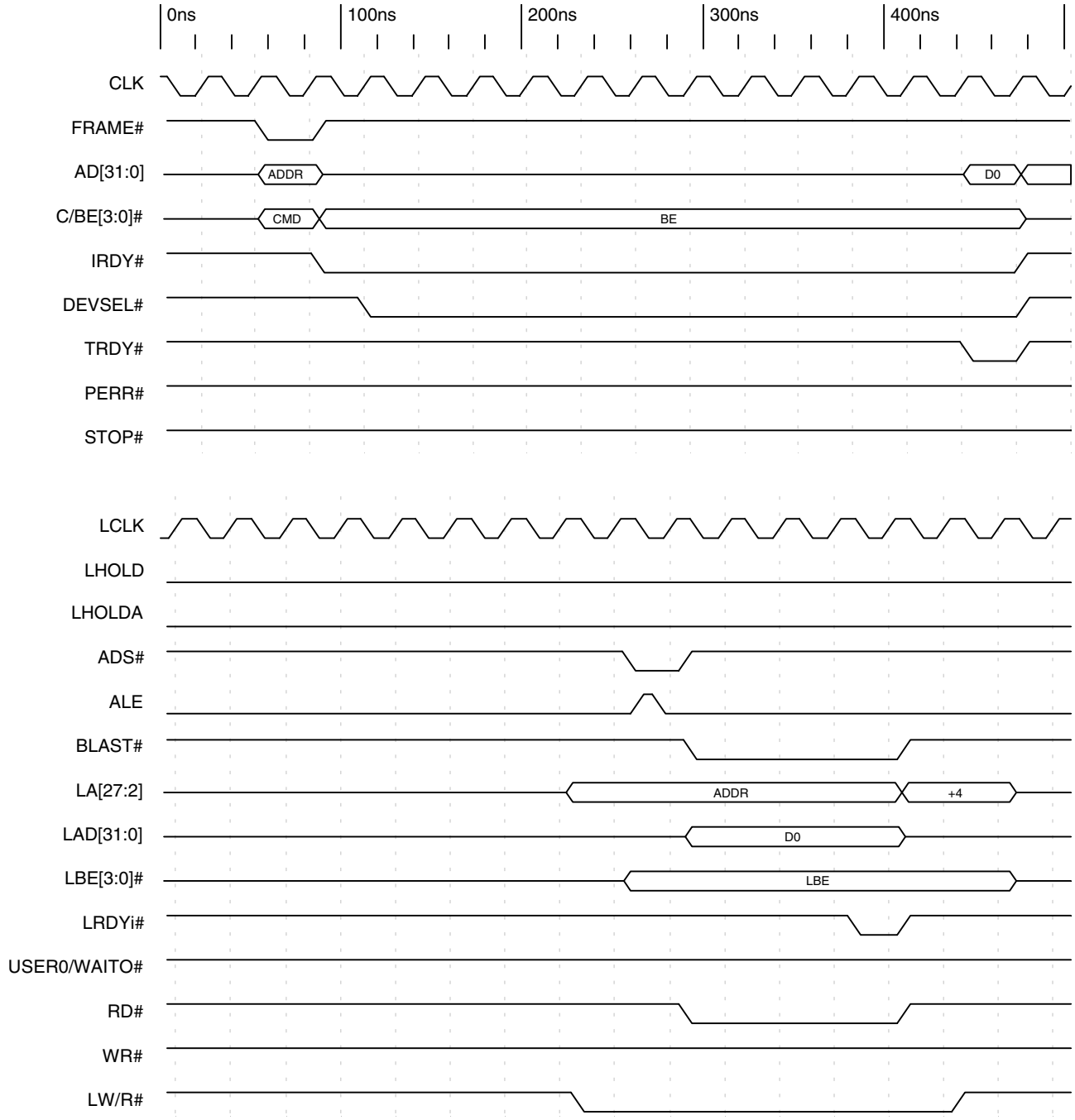
Note: Single write, 32-bit Local Bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-13. Non-Multiplexed Mode, Direct Slave Single Write without Wait States (32-Bit Local Bus)



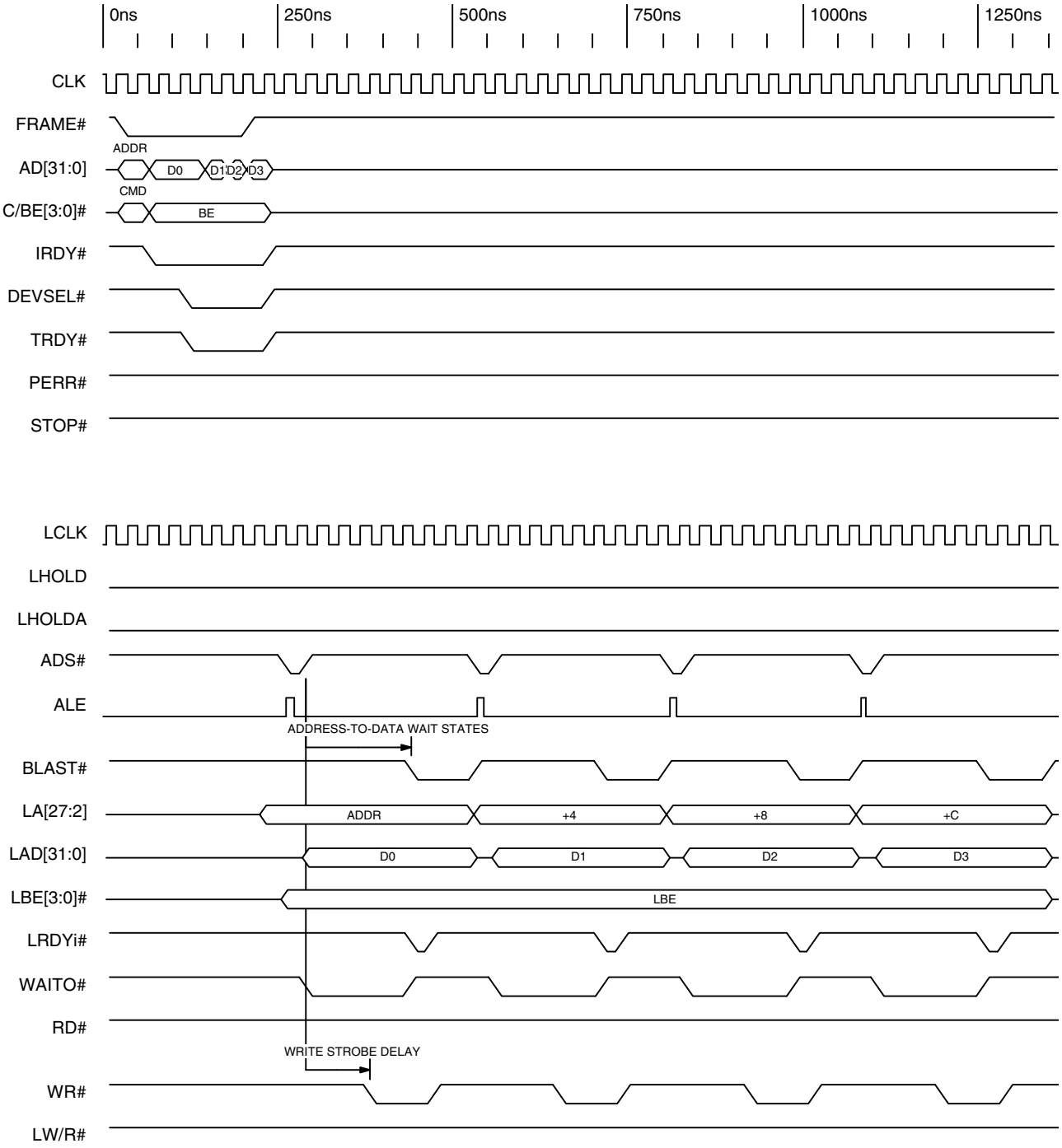
Note: Single read, 32-bit Local Bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-14. Non-Multiplexed Mode, Direct Slave Single Read without Wait States (32-Bit Local Bus)



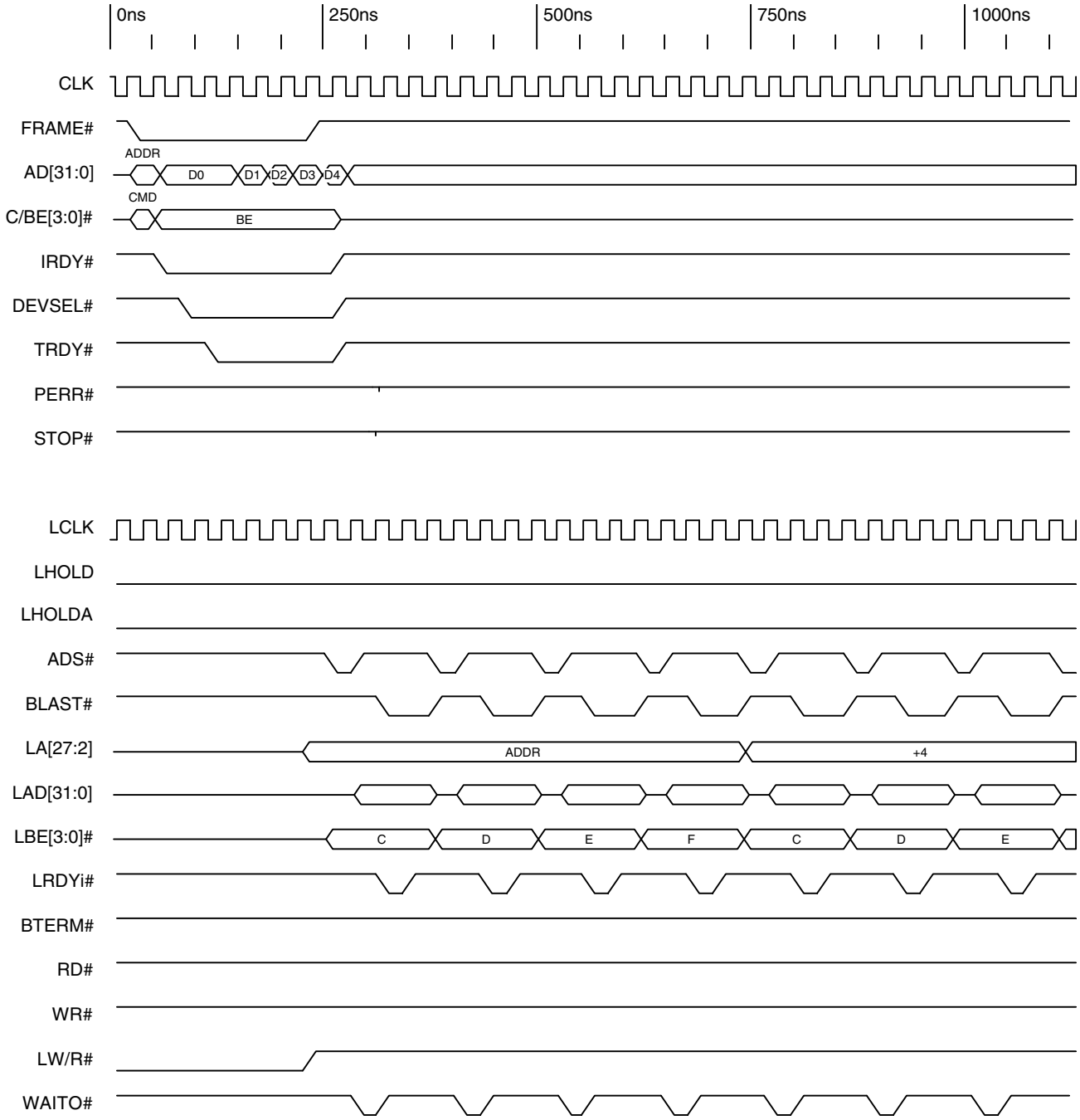
Note: Single read, 32-bit Local Bus, with wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states (NRAD)
Data-to-data = zero wait states (NRDD)
Read strobe delay = zero wait states

Timing Diagram 4-15. Non-Multiplexed Mode, Direct Slave Single Read with External (LRDYi#) Wait States (32-Bit Local Bus)



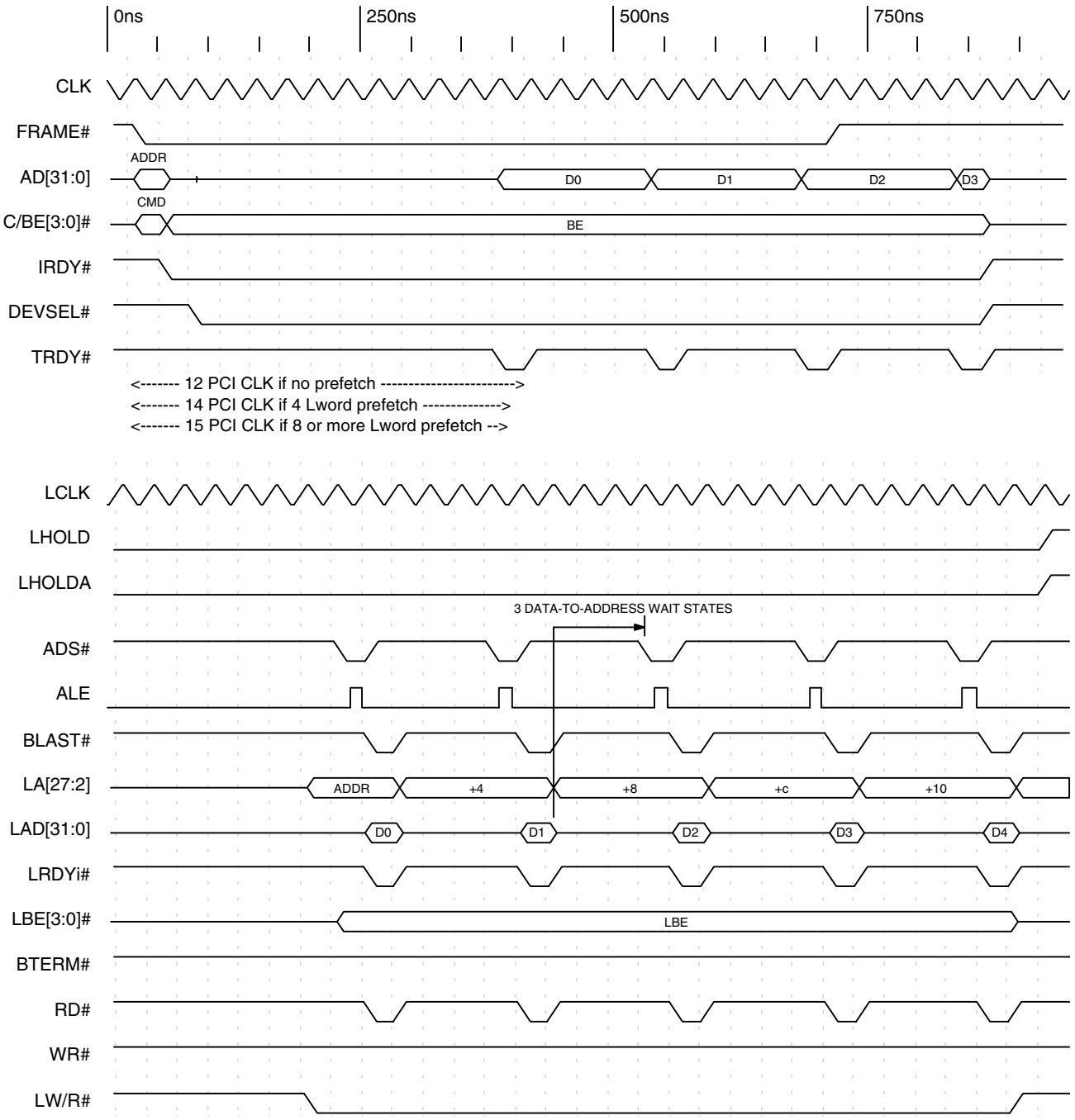
Note: Non-Burst write of four Lwords
32-bit Local Bus, BTERM# is disabled
Address-to-data = five NWAD wait states
Data-to-data = one NWDD wait state
Write strobe delay = three wait states
Write cycle hold = two wait states

Timing Diagram 4-16. Non-Multiplexed Mode, Direct Slave Non-Burst Write with Wait States (32-Bit Local Bus)



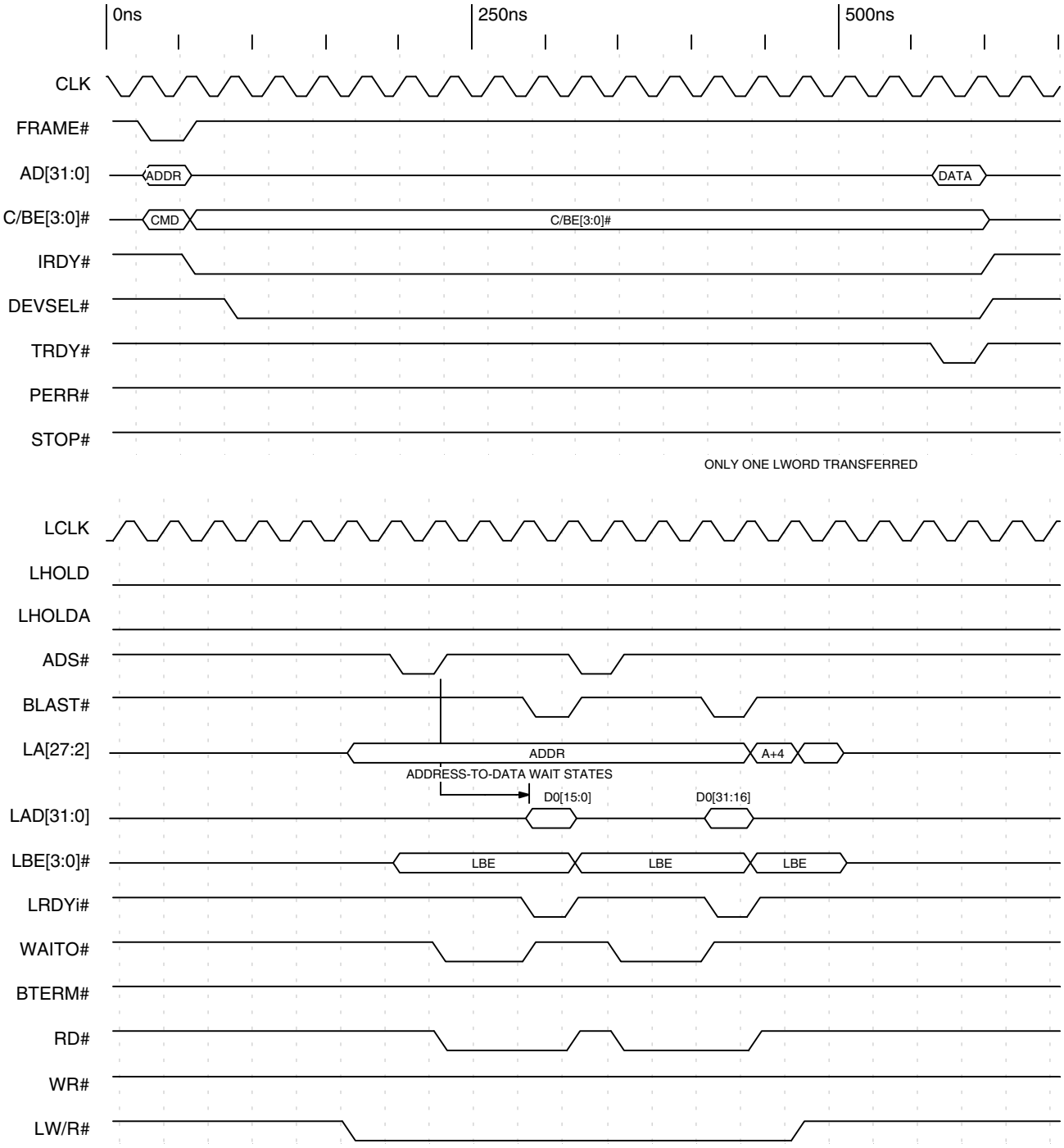
Note: Non-Burst write of five Lwords
8-bit Local Bus
Address-to-data = one NWAD wait state
Data-to-data = zero NWDD wait states
Write strobe delay = two wait states, WR# not asserted because the delay is not ≤ NWAD
Write hold cycle = one wait state

Timing Diagram 4-17. Non-Multiplexed Mode, Direct Slave Non-Burst Write (8-Bit Local Bus)



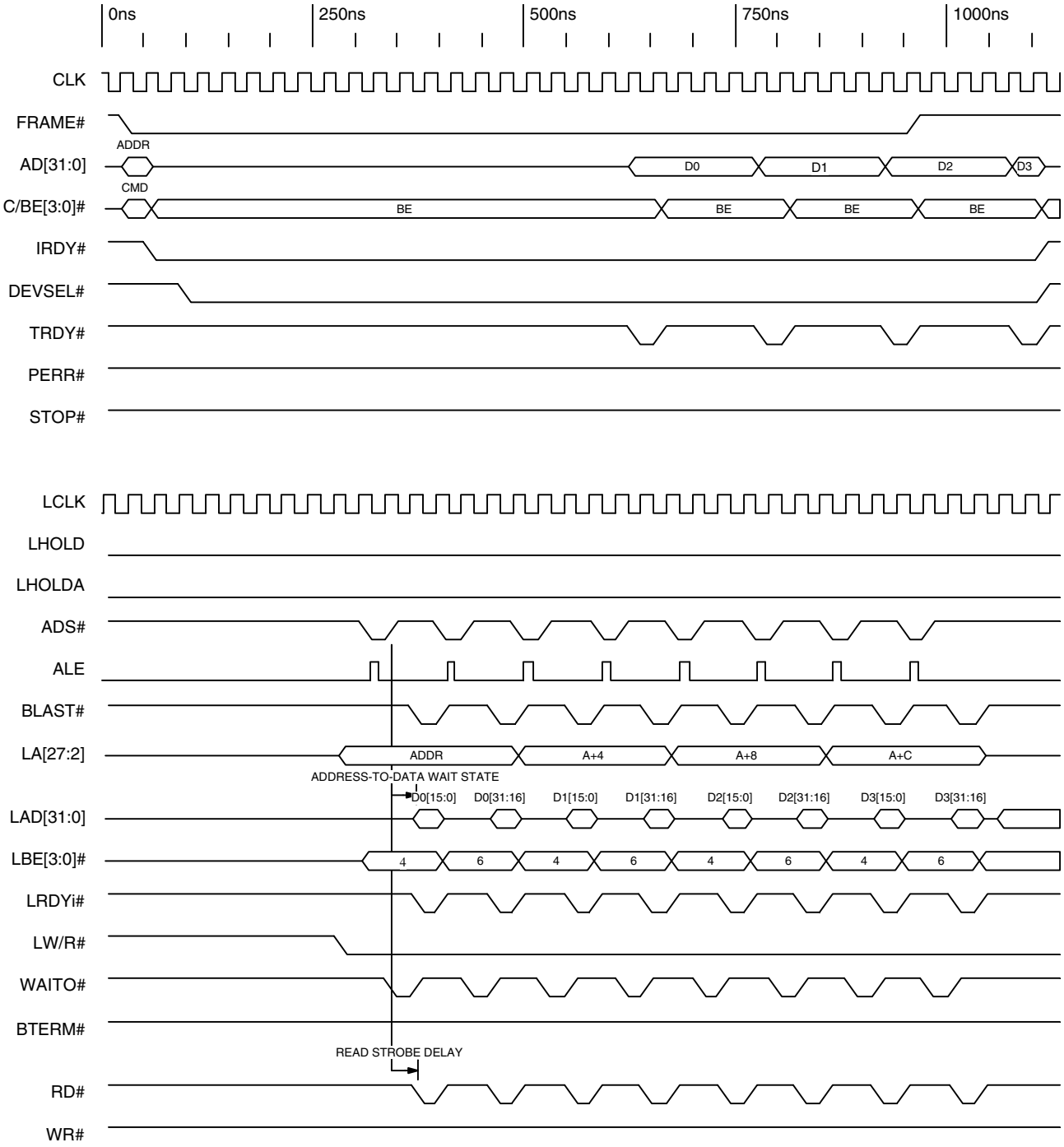
Note: Direct Slave read from Space 1
Burst disabled
Local Bus: Little Endian, 32-bit
Data-to-address = three NXDA wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-18. Non-Multiplexed Mode, Direct Slave Non-Burst Read (32-Bit Local Bus)



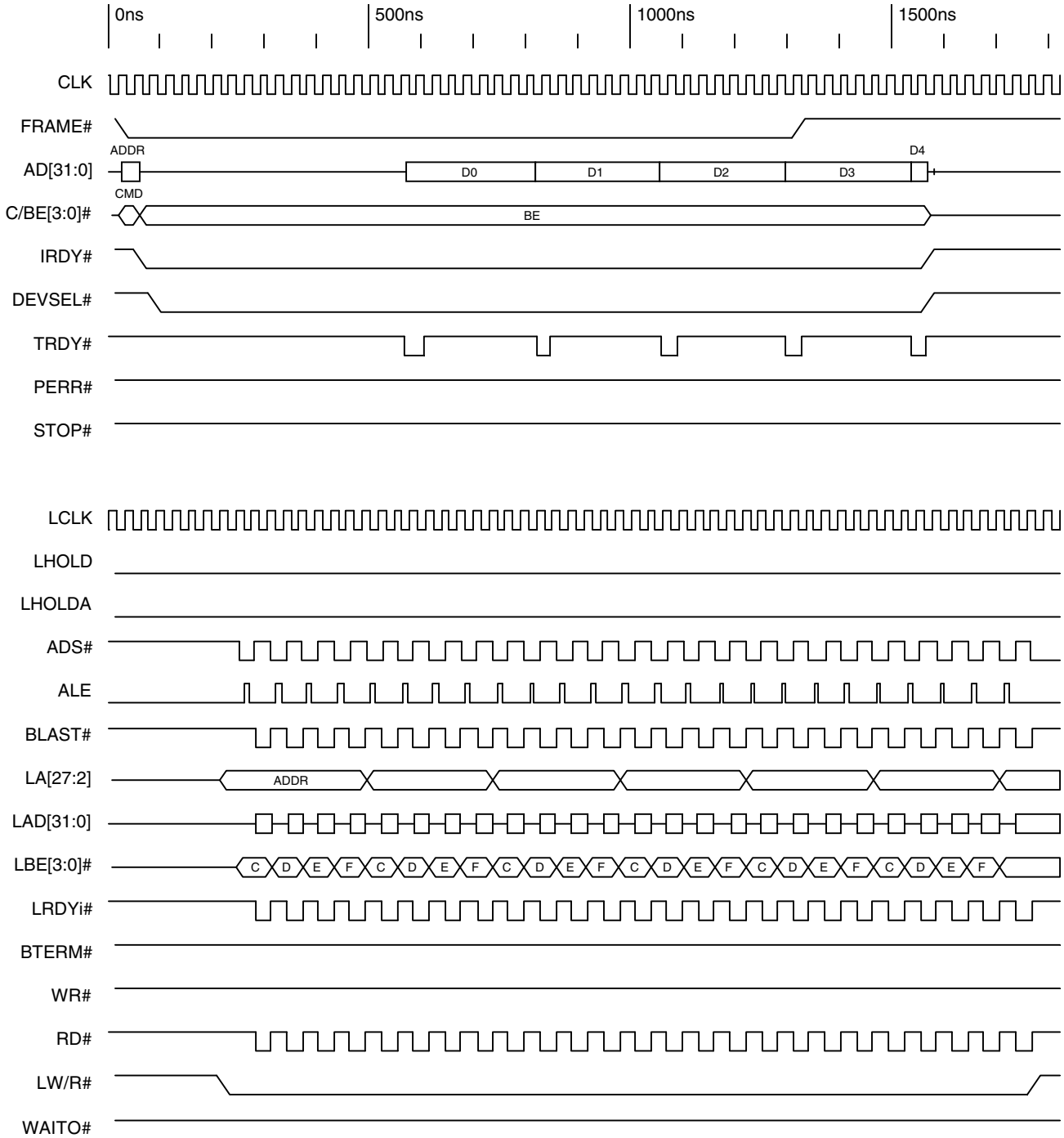
Note: Address-to-data = two NRAD wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-19. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Unaligned PCI Address (16-Bit Local Bus)

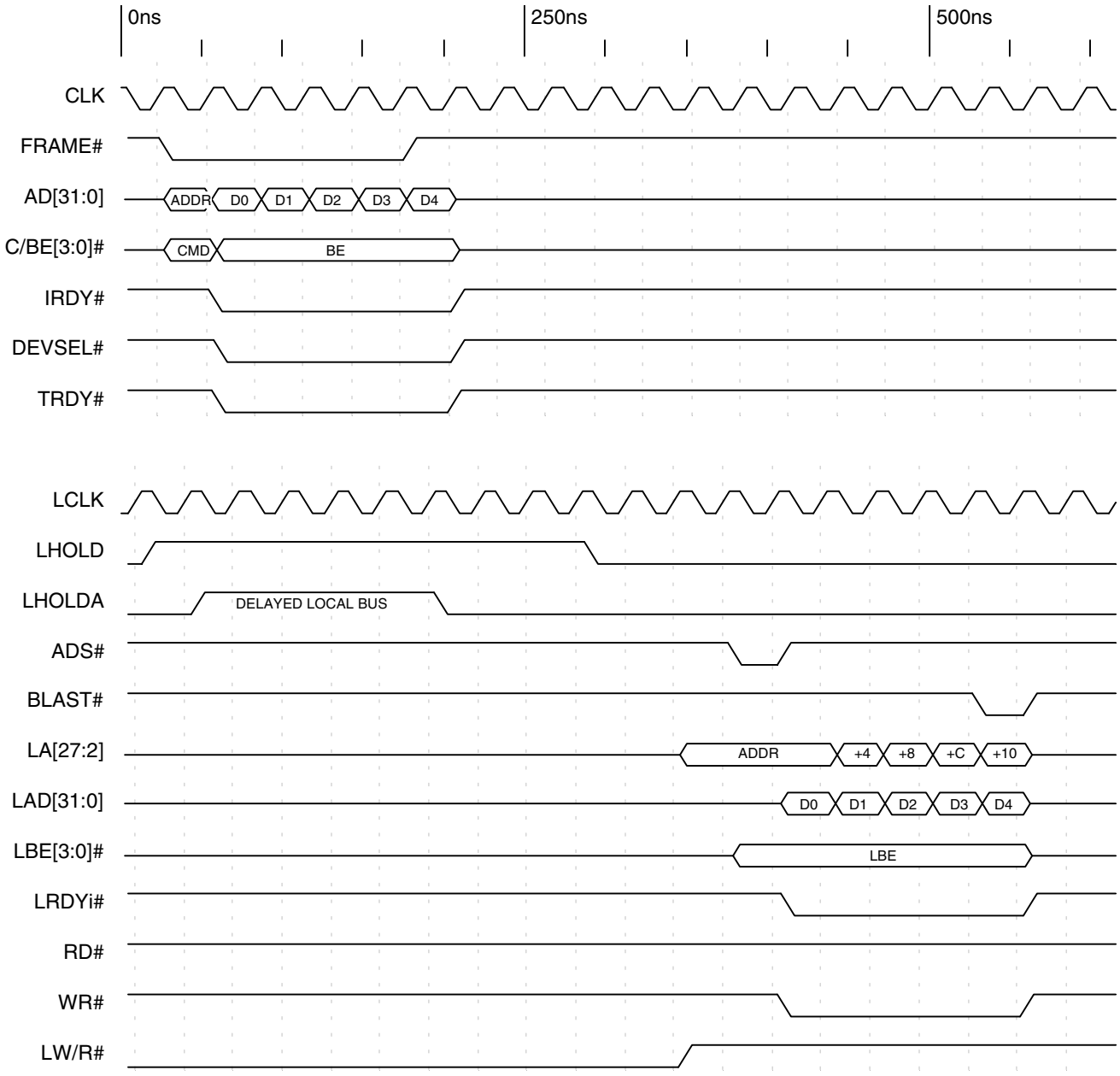


Note: 16-bit Local Bus
Non-burst read of four Lwords
Prefetch four Lwords
Address-to-data = one NRAD wait state
Data-to-data = one NRDD wait state
Read strobe delay = one wait state

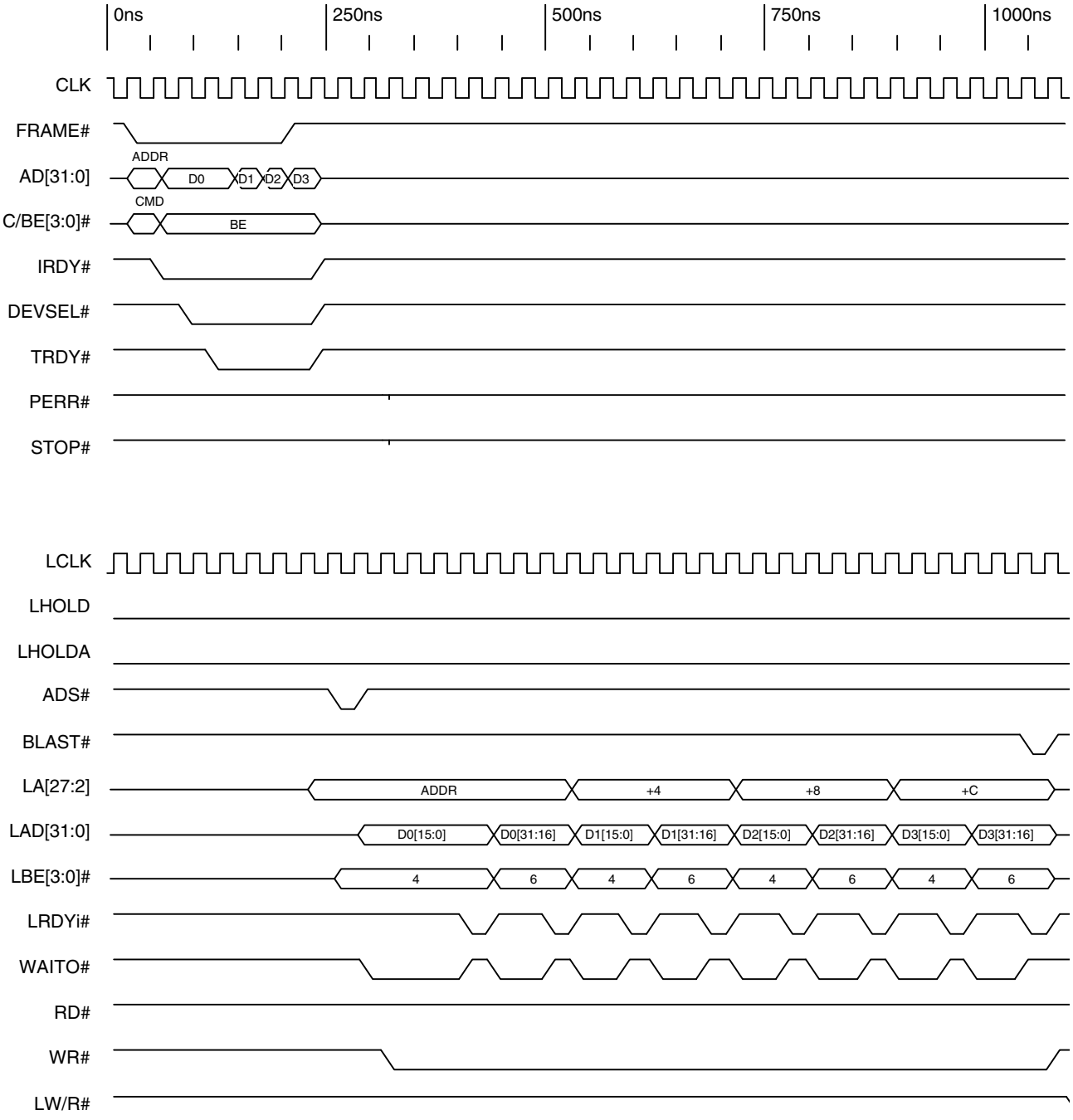
Timing Diagram 4-20. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Prefetch (16-Bit Local Bus)



Timing Diagram 4-21. Non-Multiplexed Mode, Direct Slave Non-Burst Read with Continuous Prefetch (8-Bit Local Bus)

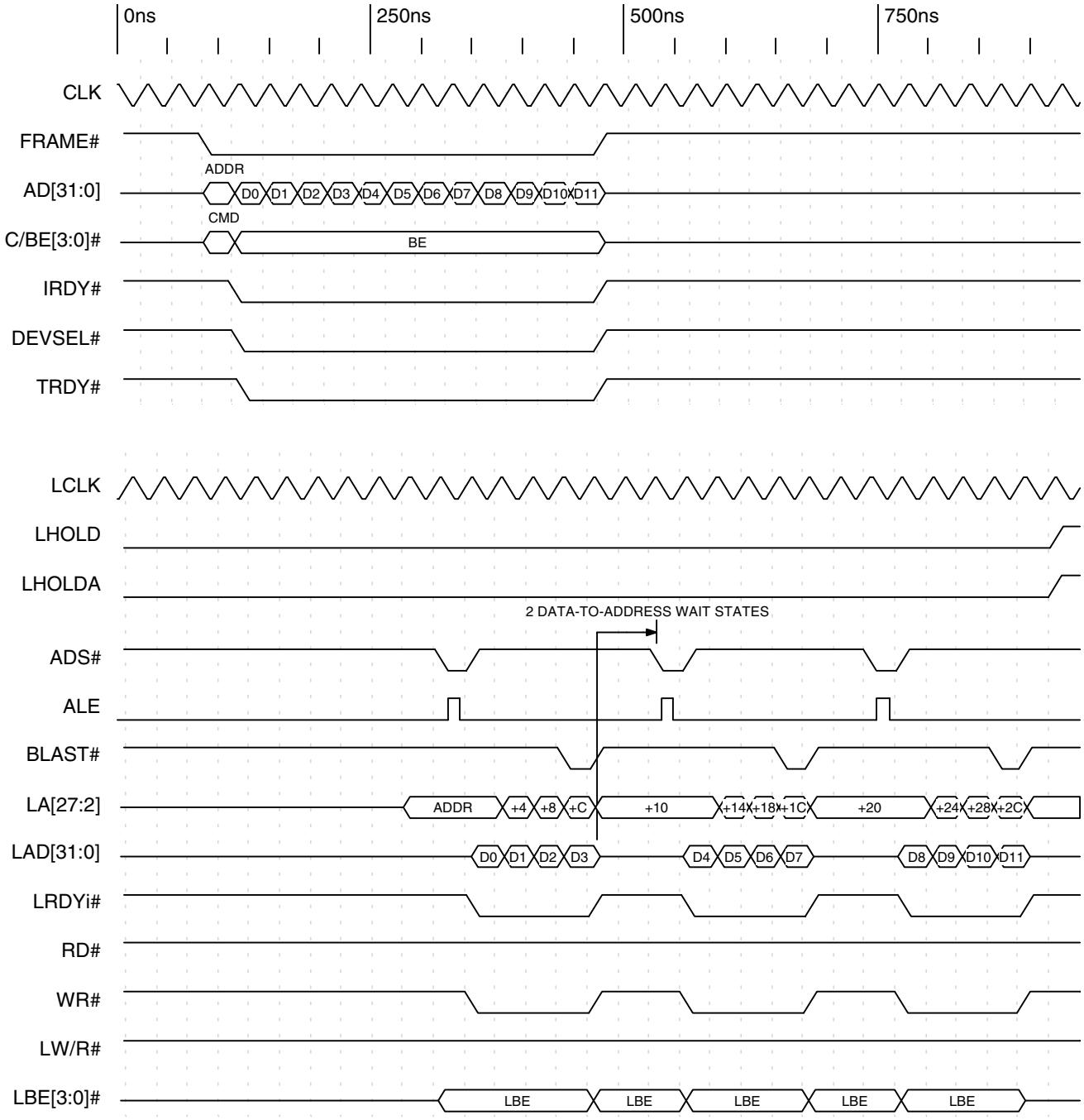


Timing Diagram 4-22. Non-Multiplexed Mode, Direct Slave Burst Write with Delayed Local Bus (32-Bit Local Bus)



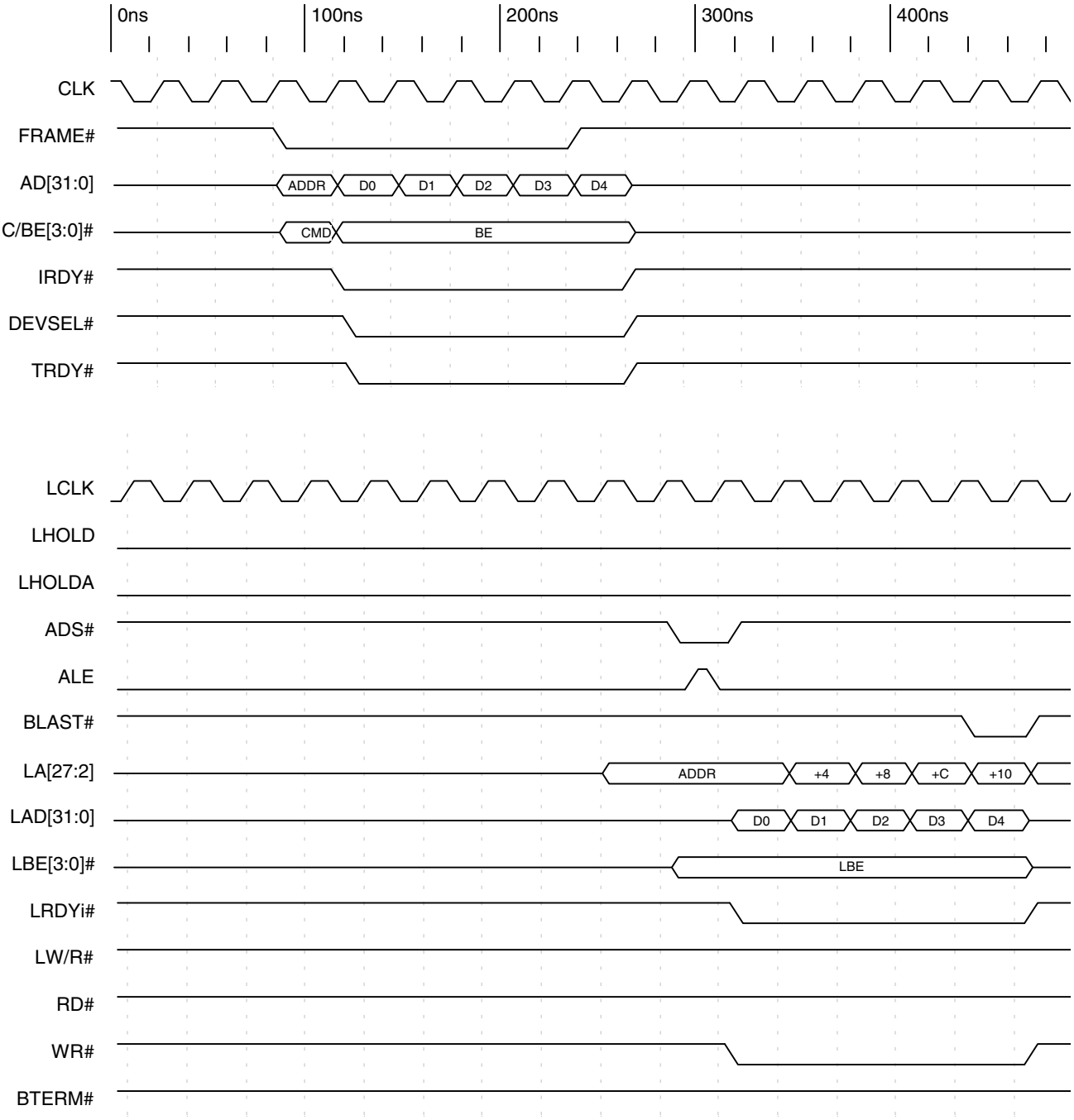
Note: Burst enabled (Burst write of four Lwords)
Address-to-data = four NWAD wait states
Data-to-data = two NWDD wait states
Write strobe delay = one wait state
Write cycle hold = zero wait states

Timing Diagram 4-23. Non-Multiplexed Mode, Direct Slave Burst Write with Wait States (16-Bit Local Bus)



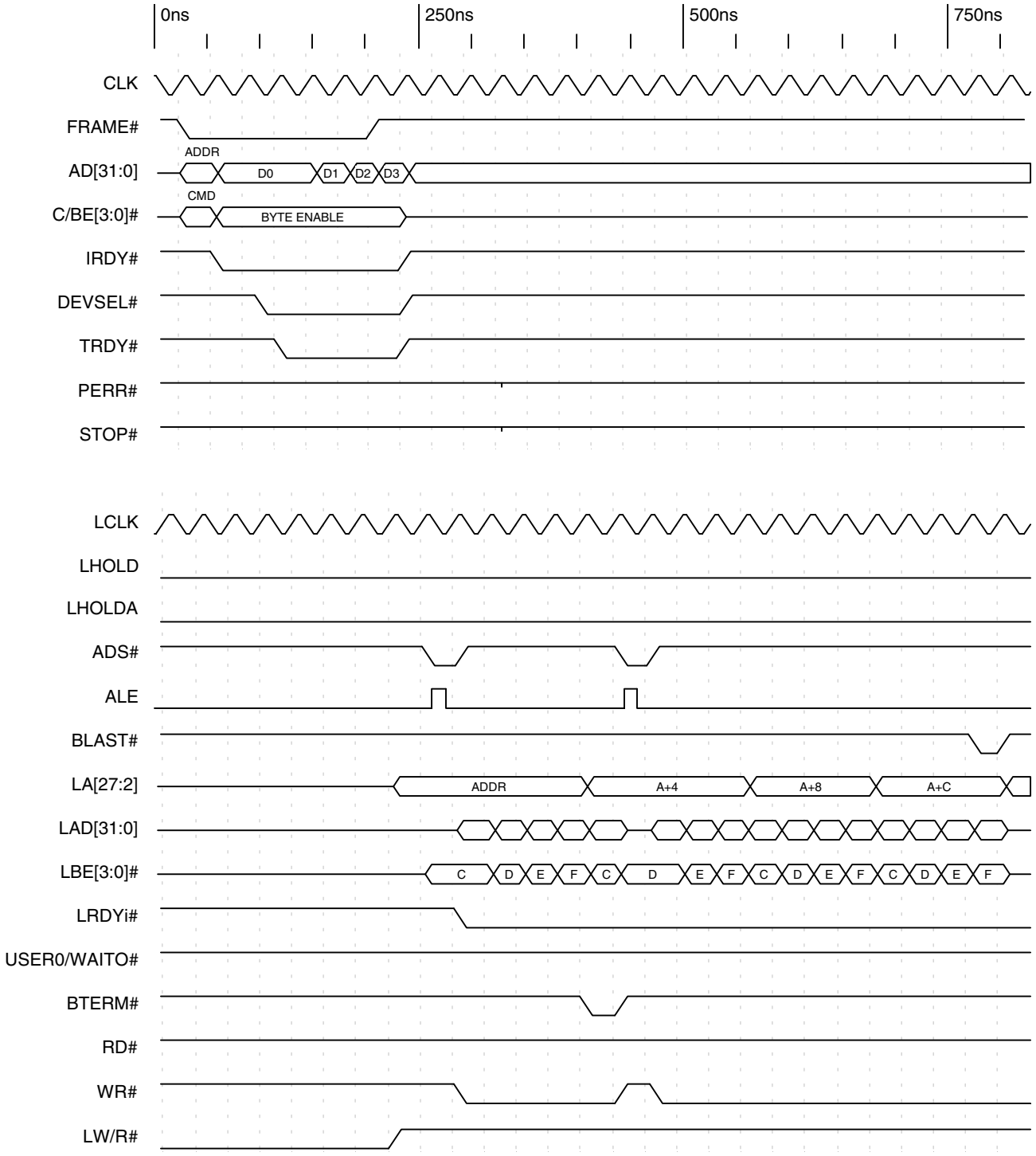
Note: Local Bus: Little Endian, 32-bit
Burst enabled (Burst write of four Lwords)
BTERM# disabled
Data-to-address = two NXDA wait states

Timing Diagram 4-24. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Disabled and Wait States (32-Bit Local Bus)



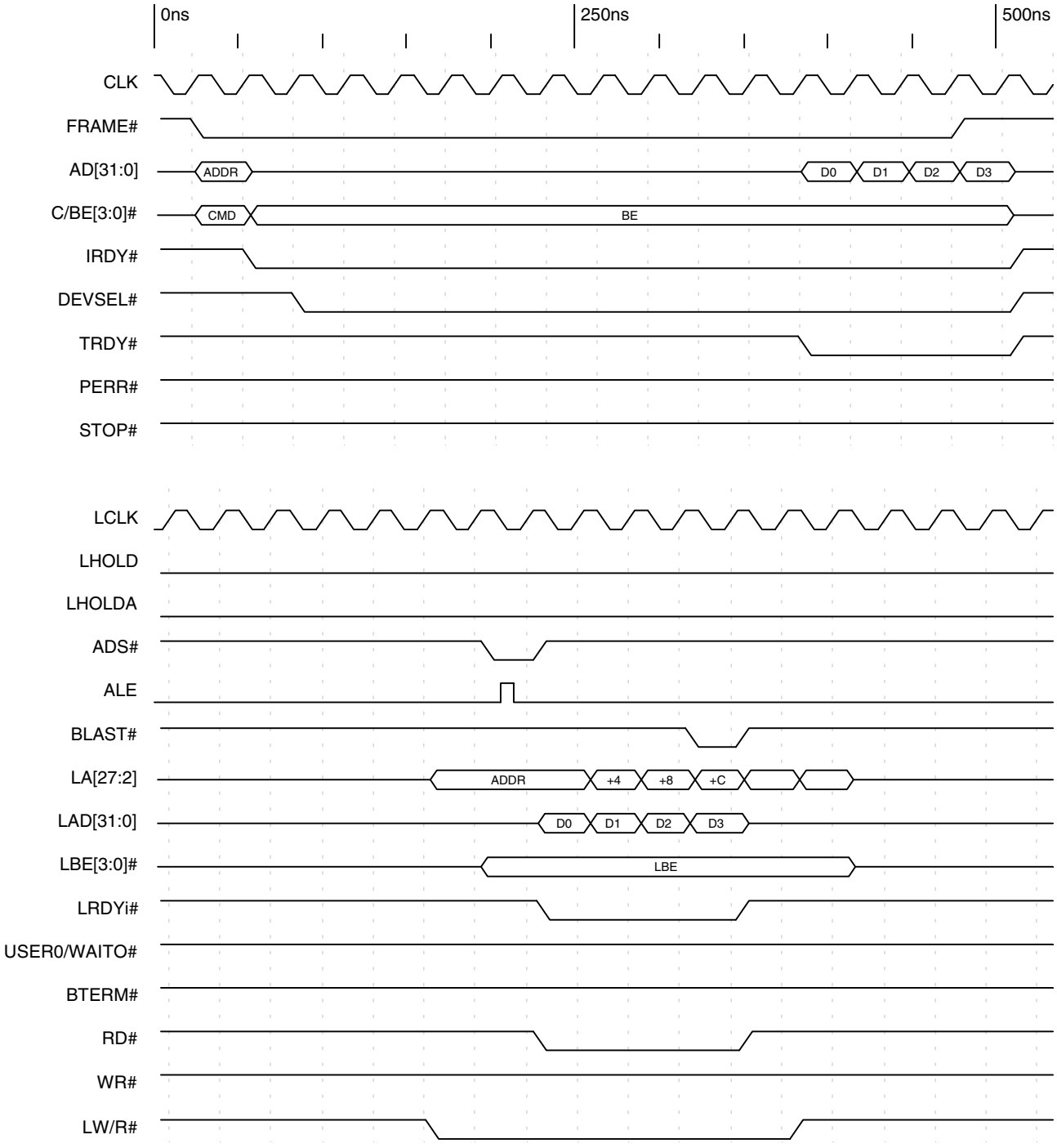
Note: Local Bus: Little Endian, 32-bit
Burst enabled (Burst write of five Lwords), BTERM# enabled
Address-to-data = zero wait states
Data-to-data = zero wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-25. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus)



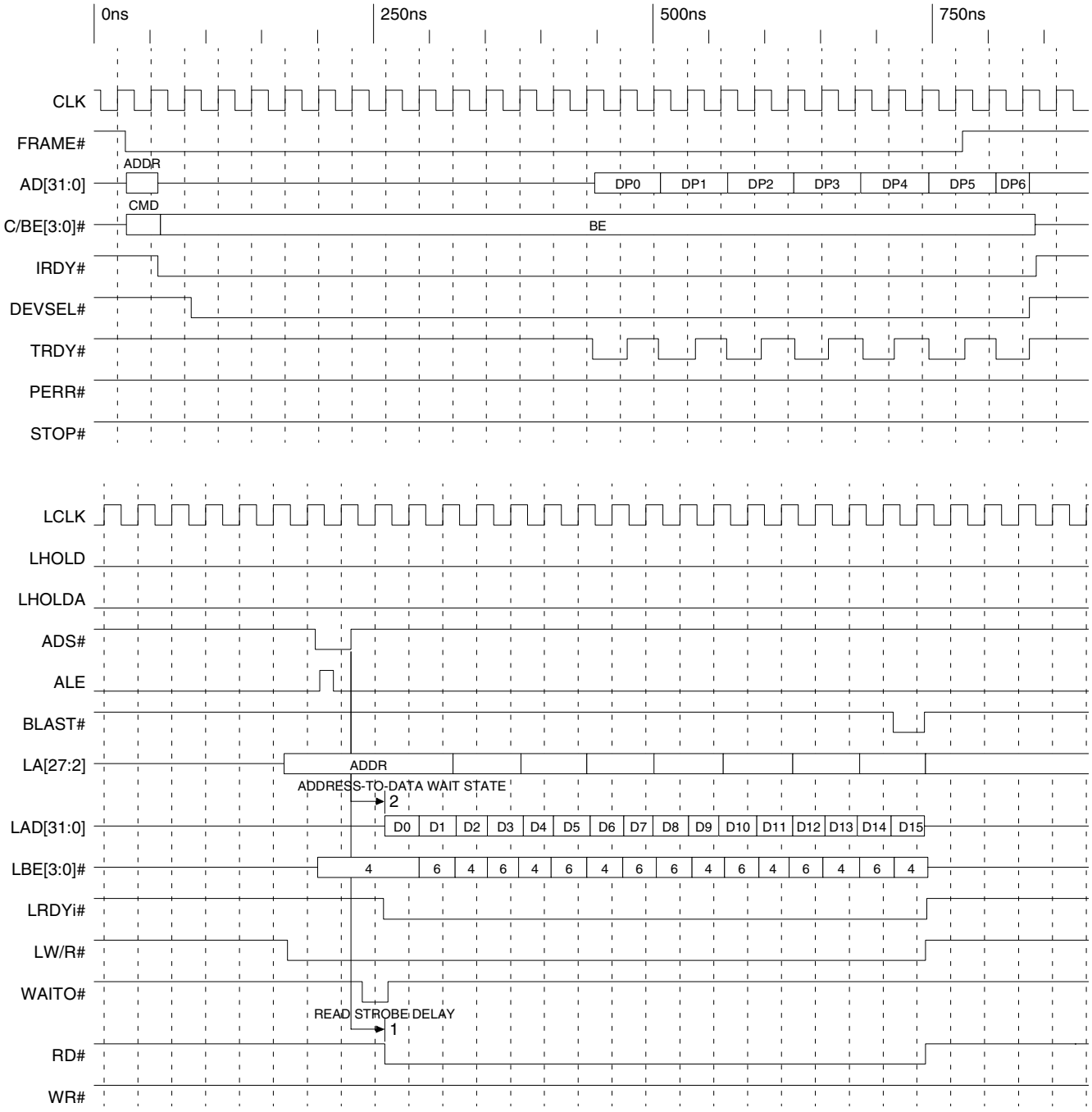
Note: Burst enabled (Burst write of four Lwords)
BTERM# enabled

Timing Diagram 4-26. Non-Multiplexed Mode, Direct Slave Burst Write with BTERM# Enabled (8-Bit Local Bus)



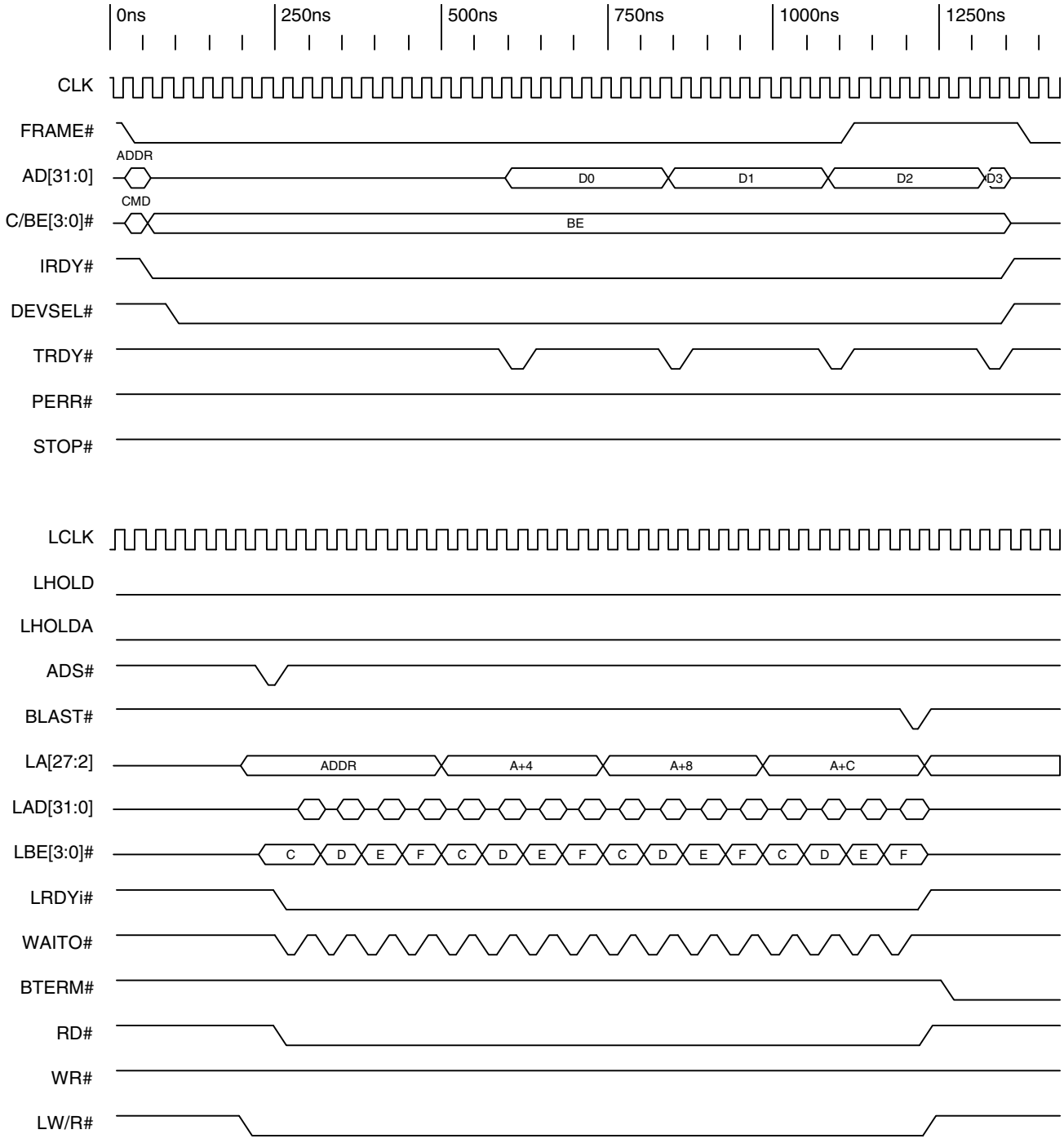
Note: Local burst
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delays = zero wait states

Timing Diagram 4-27. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Four Lwords (32-Bit Local Bus)



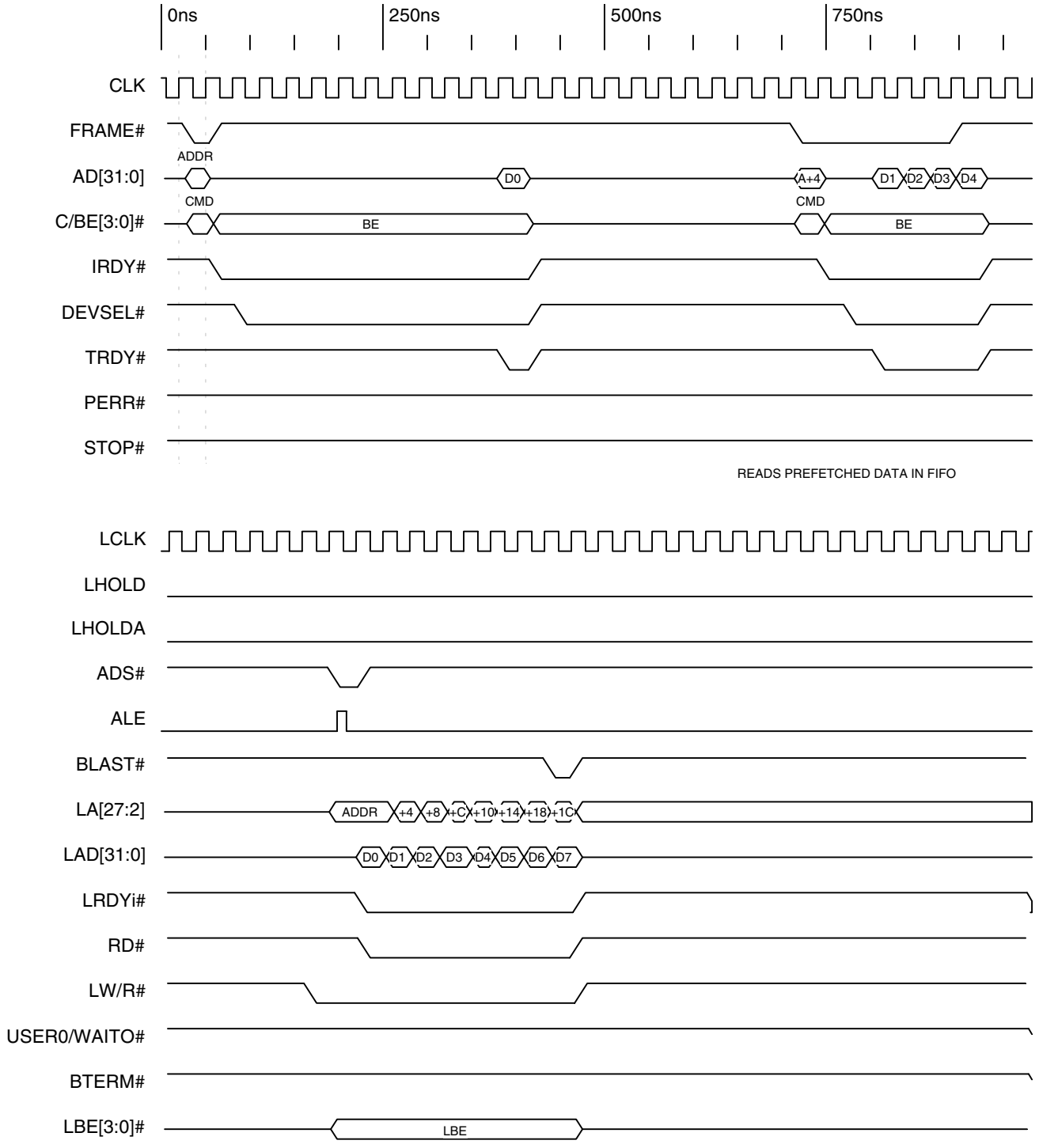
Note: Burst read eight Lwords
Address-to-data = one NRAD wait state
Data-to-data = zero wait states
Read strobe delay = one wait state

Timing Diagram 4-28. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Eight Lwords (16-Bit Local Bus)



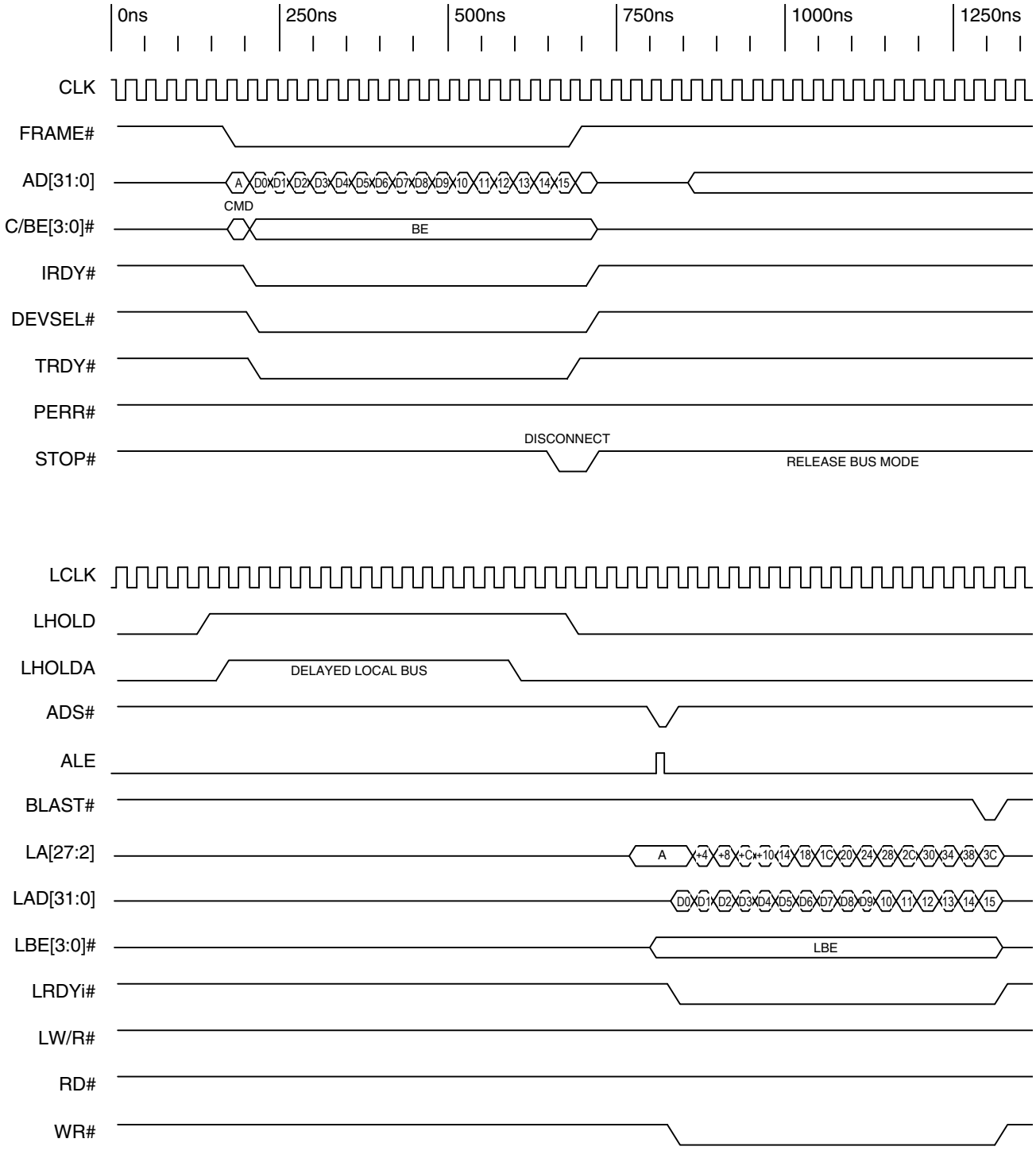
Note: Burst read four Lwords
Address-to-data = one NRAD wait state
Data-to-data = one NRDD wait state
Read strobe delay = zero wait states

Timing Diagram 4-29. Non-Multiplexed Mode, Direct Slave Burst Read with Prefetch of Four Lwords (8-Bit Local Bus)

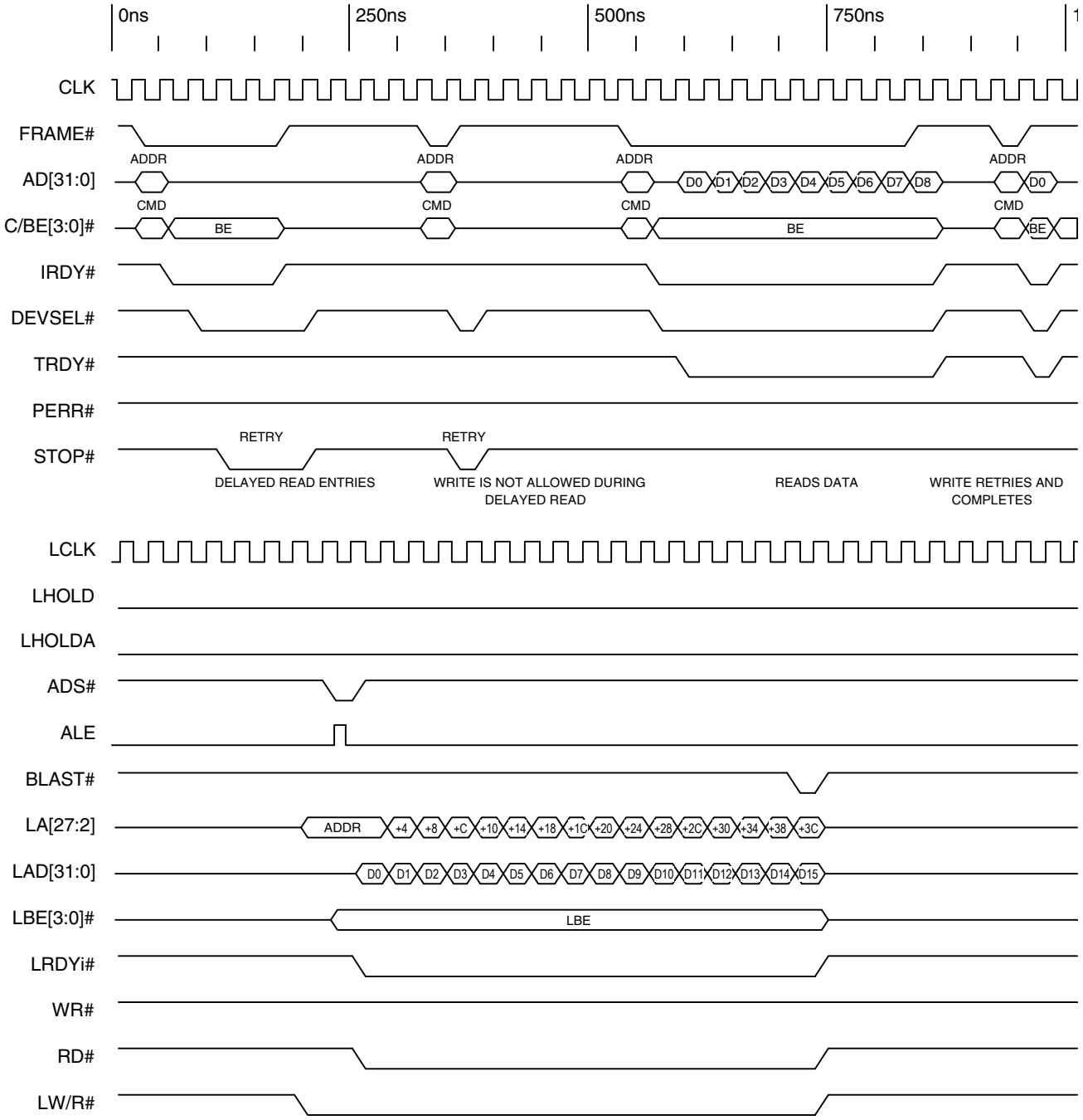


Note: Direct Slave read for Space 0 (same for Spaces 1, 2, and 3 and Expansion ROM)
Prefetch eight Lwords, 32-bit Local Bus

Timing Diagram 4-30. Non-Multiplexed Mode, Direct Slave Read with Direct Slave Read Ahead Mode Enabled (CNTRL[16]=1)



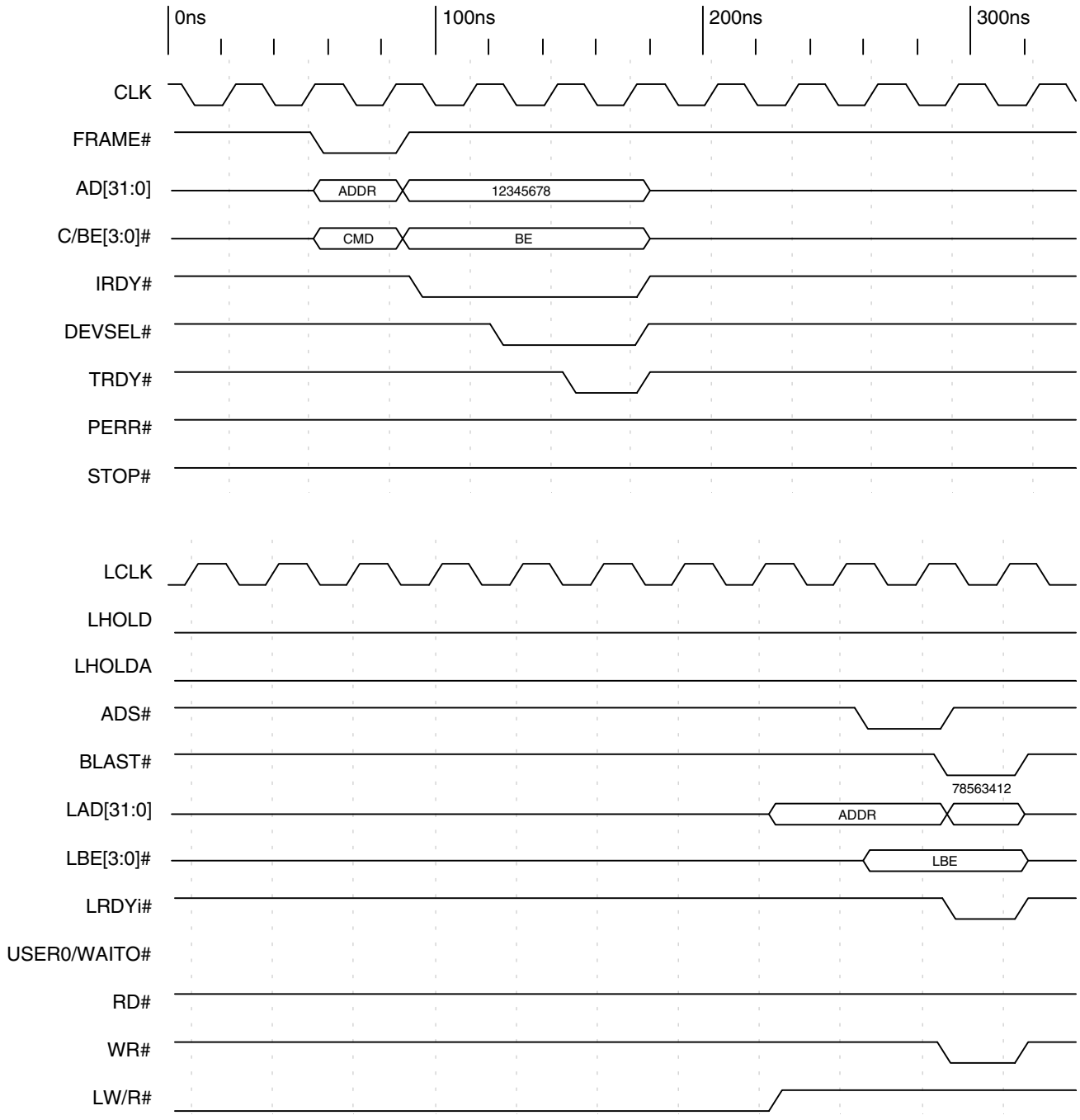
Timing Diagram 4-31. Non-Multiplexed Mode, Direct Slave Burst Write with PCI Write Release Bus Mode Enabled (CNTRL[18]=1)



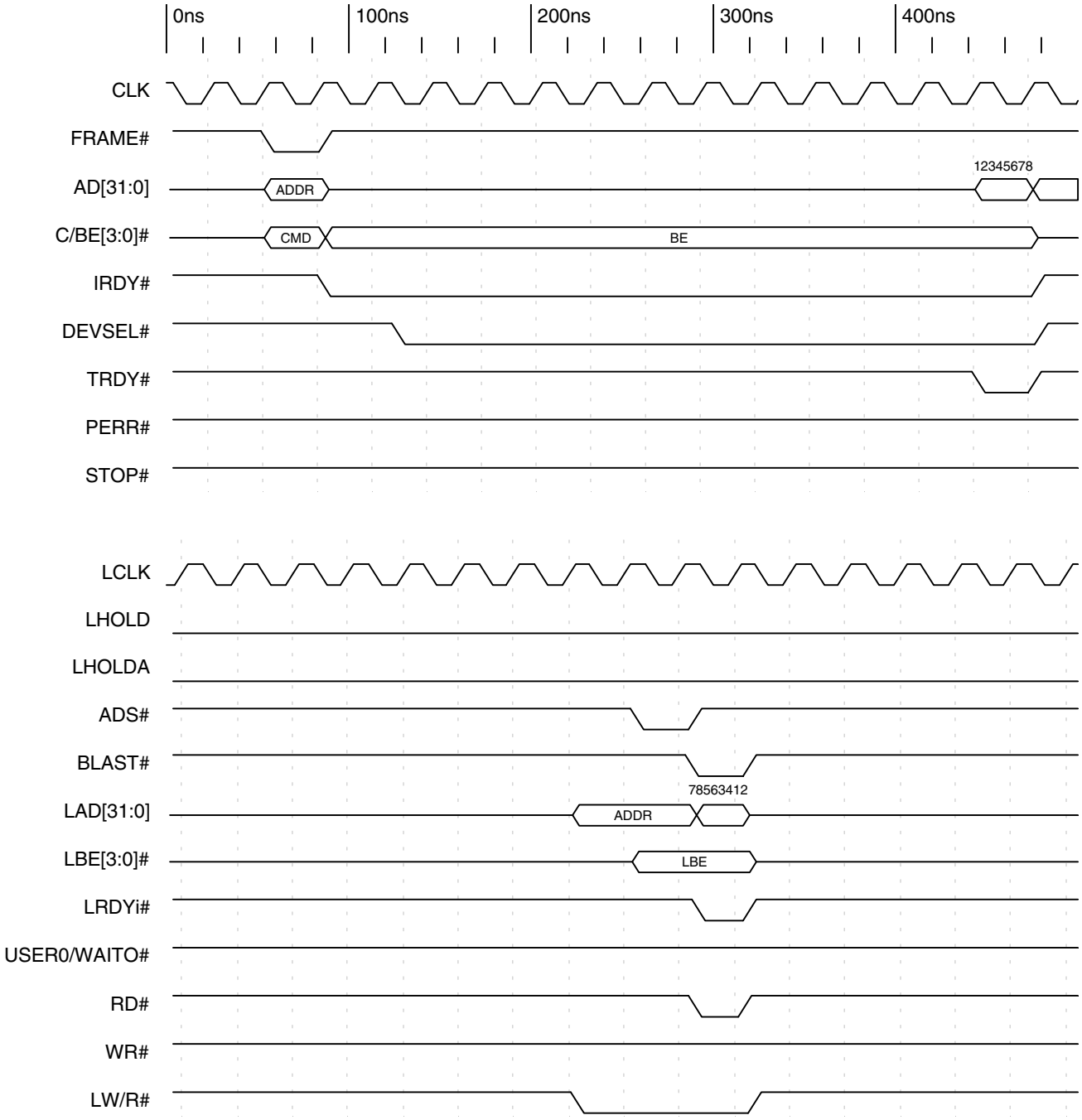
Note: Disconnect immediately for a read
Does not affect pending reads when Write cycle occurs
Does not flush the Read FIFO if PCI Read cycle completes
Force Retry on write if read is pending
De-assert TRDY# until space is available in the Direct Slave Write FIFO

Timing Diagram 4-32. Non-Multiplexed Mode, Direct Slave Burst Read with PCI Write Release Bus Mode Disabled (PCI Write Hold Bus Mode Enabled), PCI Read No Write Mode and PCI Read No Flush Mode (Direct Slave Read Ahead Mode) Enabled, PCI Read with Write Flush Mode Disabled, and *PCI r2.1* Features Enabled (CNTRL[18:14]=01101)

4.4.3 Big Endian Mode and Multiplexed Mode Local Bus

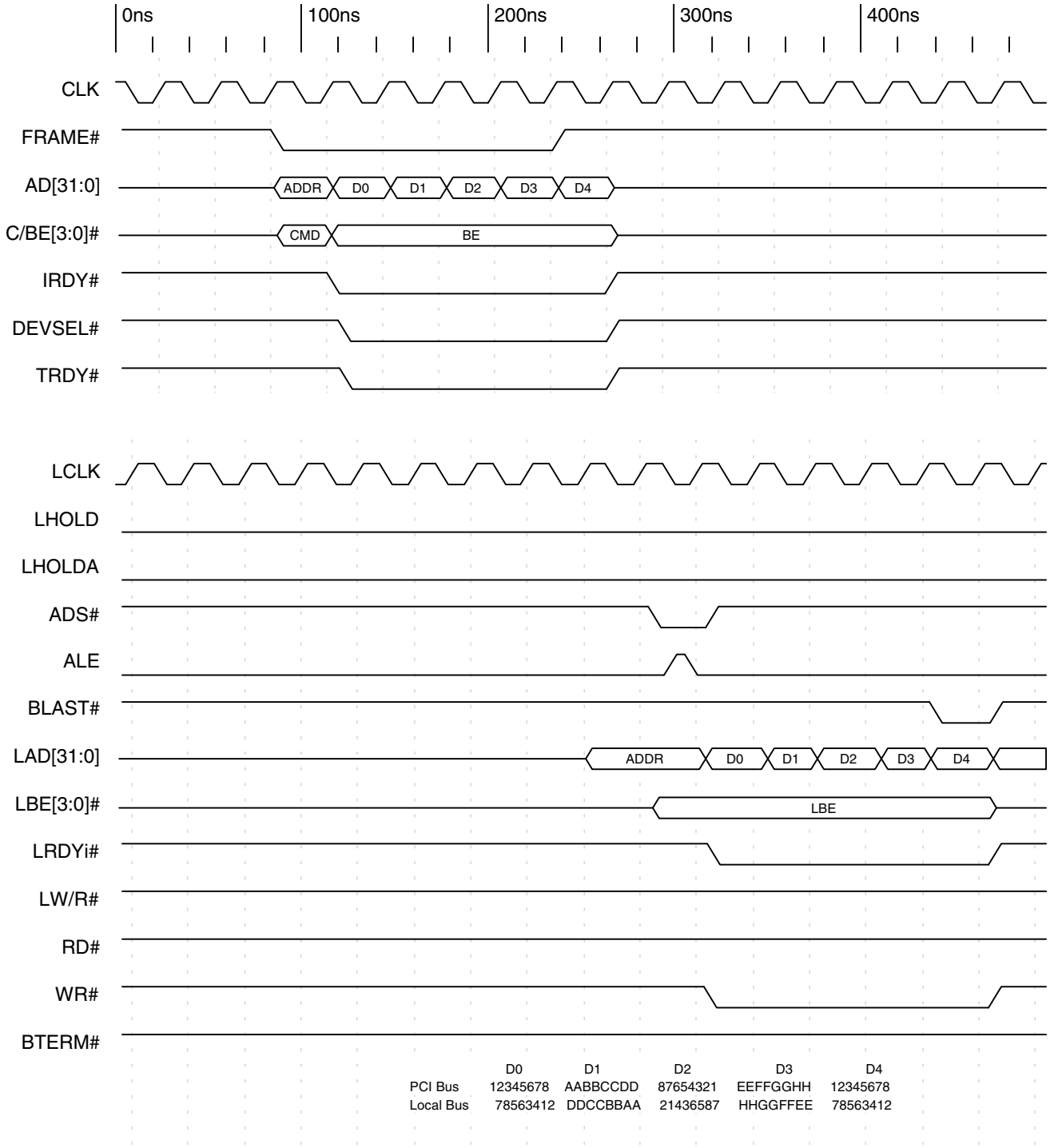


Timing Diagram 4-33. Multiplexed Mode, Direct Slave Single Write, Local Bus Big Endian (32-Bit)



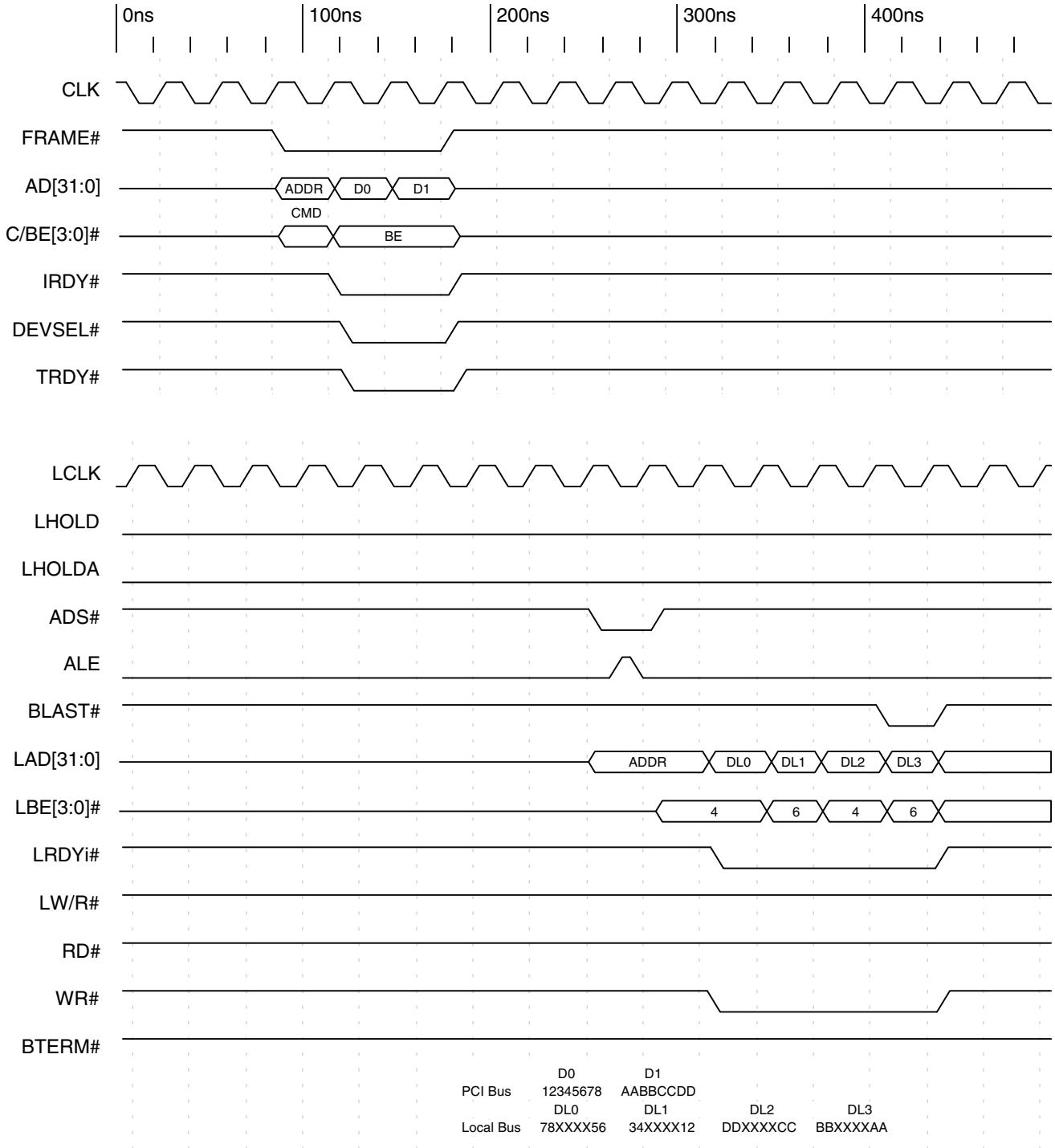
Note: Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-34. Multiplexed Mode, Direct Slave Single Read, Local Bus Big Endian (32-Bit)



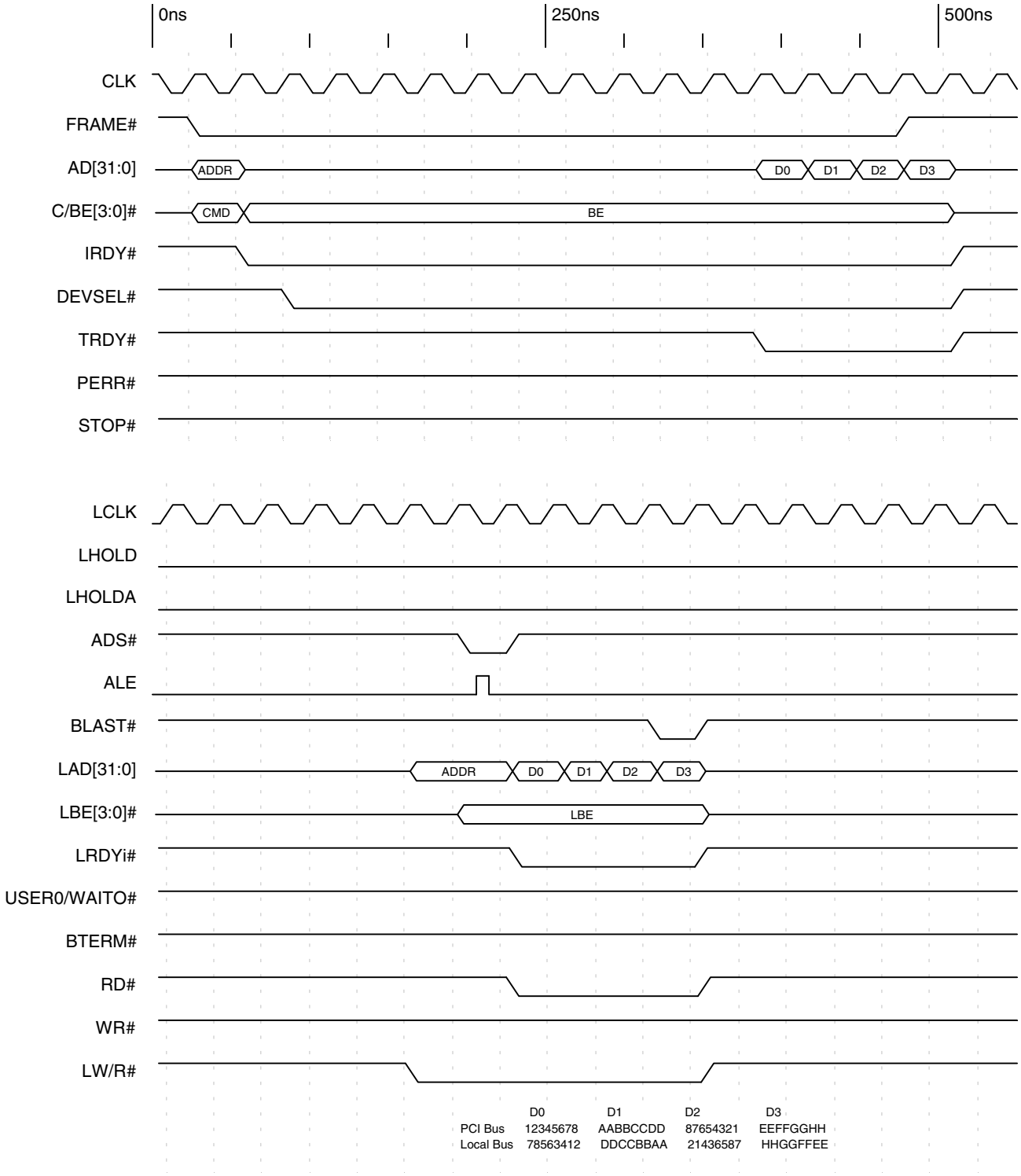
Note: Local Bus: Big Endian, 32 bit
Burst enabled (burst write of five Lwords), BTERM# enabled
Address-to-data = zero wait states (NWAD)
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-35. Multiplexed Mode, Direct Slave Burst Write, Local Bus Big Endian (32-Bit)



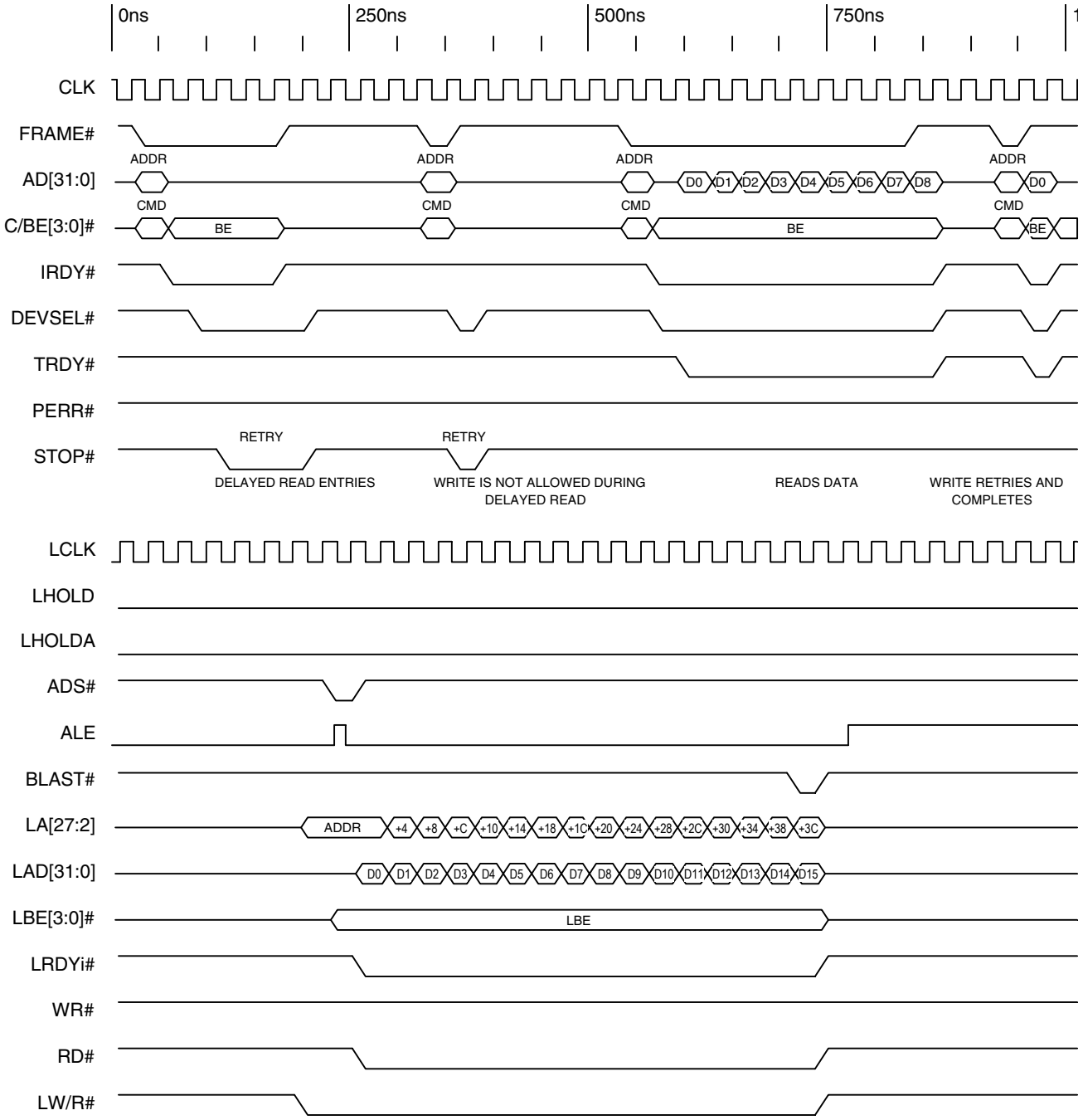
Note: Local Bus: Big Endian, 16 bit
Burst enabled (burst write of four Lwords), BTERM# enabled
Address-to-data = zero wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-36. Multiplexed Mode, Direct Slave Burst Write, Local Bus Big Endian (16-Bit)



Note: Prefetch four Lwords, Local burst
Address-to-data = zero wait states (NRAD)
Data-to-data = zero wait states (NRDD)
Read strobe delay = zero wait states

Timing Diagram 4-37. Multiplexed Mode, Direct Slave Burst Read, Local Bus Big Endian (32-Bit)



Note: Burst enabled (Burst read of four words)
Address-to-data = one NRAD wait state
Data-to-data = zero wait states
Read strobe delay = three wait states

Timing Diagram 4-38. Multiplexed Mode, Direct Slave Burst Read, Local Bus Big Endian (16-Bit)

5 ISA INTERFACE MODE

5.1 ARCHITECTURE

A major architectural feature of the PCI 9052 is the inclusion of a glueless ISA logic interface, which provides for a smooth ISA-to-PCI conversion. It supports 8- and 16-bit wide ISA slave devices, which can be Memory- or I/O-mapped. Direct Slave Read Ahead mode can be used to improve memory-mapped Read data throughput. The PCI 9052 performs only single cycles to ISA Interface Memory and I/O. The PCI 9052 ISA Interface does not support ISA Bus Master transfers nor ISA DMA.

The PCI 9052 ISA Interface is designed for ISA compatibility, using an approximately 8 MHz external clock input to the LCLK pin. ISA Interface mode requires that the PCI 9052 be configured for Non-Multiplexed mode (MODE pin low), and a programmed serial EEPROM be present with the ISA Interface Mode Enable bit set (INTCSR[12]=1). This bit is writable only by serial EEPROM.

In ISA Interface mode, Local Address Space 0 is assigned for Memory command access to the ISA interface, and Local Address Space 1 is assigned for I/O command access to the ISA interface. At boot time, the PCI BIOS writes the PCI base address it assigned for Local Address Space 0 (if enabled) into PCI Base Address register 2 (PCIBAR2), and the PCI base address it assigned for Local Address Space 1 (if enabled) into PCI Base Address register 3 (PCIBAR3). System I/O addressing typically uses 16 address lines ([15:0]) for addressing up to 64 KB; therefore, the PCIBAR3 value is generally a 16-bit rather than a 32-bit address.

A Memory access to an offset from the PCI base address that BIOS assigned in PCIBAR2 generates an ISA interface Memory access to the Local Address having the same offset referenced from the Local Base Address programmed in LAS0BA. An I/O access to an offset from the PCI Base Address that BIOS assigned in PCIBAR3 generates an ISA interface I/O access to the Local Address having the same offset referenced from the Local Base Address programmed in LAS1BA.

In ISA Interface mode, Local Addresses Spaces 2 and 3 and Expansion ROM can be used for additional 8-, 16-, and 32-bit Memory and/or I/O spaces, which can be accessed with Local Bus control and the Non-Multiplexed Address and Data Buses (LA[27:2] and LAD[31:0], respectively). Refer to Figure 11-2, "PCI 9052 Adapter Block Diagram," on page 11-2 and Figure 11-4, "Pin Assignments, ISA and Non-Multiplexed/ISA Interface Modes," on page 11-5 for Non-Multiplexed/ISA signals used for Local Address Spaces 2 and 3 and Expansion ROM.

5.2 PIN DEFINITIONS

In ISA Interface mode, the functionality of seven Local Bus pins changes. (Refer to Table 5-1 for pin definitions.)

Table 5-1. ISA and Non-ISA Interface Mode Pin Definitions

Pin	Non-ISA Interface Mode	ISA Interface Mode
45	NC	CHRDY
67	NC	NOWS#
130	CS0#	MEMRD#
131	CS1#	MEMWR#
132	LRESET#	LRESET
138	USER0/WAITO#	IORD#
139	USER1/LLOCKo#	IOWR#

In ISA Interface mode, four Local Bus pins have dual functionality. (Refer to Table 5-2 for pins with dual functionality.)

Table 5-2. Pin Functionality in ISA Interface Mode

Pin	Local Address Spaces 0 and 1	Local Address Spaces 2 and 3 and Expansion ROM
46	SBHE#	LBE3#
48	ISAA1	LBE1#
49	ISAA0	LBE0#
64	BALE	ALE

5.2.1 LRESET#/LRESET

In ISA Interface mode, the LRESET# pin polarity is switched from active-low to active-high to redefine the signal as LRESET. At boot time, LRESET is de-asserted during PCI reset, asserts a pulse width of approximately 750 µs, and de-asserts shortly before serial EEPROM initialization completes and PCI BIOS configuration is allowed (time assumes a 33.3 MHz PCI clock effecting a 960 ns serial EEPROM clock period, and INTCSR register loading to enable ISA Interface mode occurs after 780 serial EEPROM clocks).

Software reset (CNTRL[30]=1) asserts LRESET until cleared by software.

5.2.2 CS0#/MEMRD# and CS1#/MEMWR#

The CS0# and CS1# Chip Select signals are not available in ISA Interface mode, even if ISA Memory is not configured, as these pins are redefined as MEMRD# and MEMWR#, respectively. These pins are driven high, until an ISA Memory access causes assertion, and continue to be driven high when the PCI 9052 does not own the Local Bus (LHOLD input asserted by a Local Bus master).

For 16-bit transactions, MEMRD# and MEMWR# assert on the rising clock edge when BALE de-asserts. For 8-bit transactions, MEMRD# and MEMWR# assert on the falling clock edge after BALE de-asserts.

Some 8-bit ISA memory cards use SMEMRD# (System Memory Read) and SMEMWR# (System Memory Write) signals instead of MEMRD# and MEMWR#, respectively. These signals assert only if the address is within the lowest 1 MB of address space. For such cards, the PCI 9052 MEMRD# and MEMWR# signals can be used for SMEMRD# and SMEMWR# command strobes if the entire ISA memory is mapped below 1 MB. If only part of the memory is mapped below 1 MB, either of the PCI 9052 Chip Selects CS[3:2]# can be programmed for the lower 1 MB, and the signals ANDed with MEMRD# or MEMWR#, to generate SMEMRD# and SMEMWR#.

5.2.3 USER0/WAITO#/IORD# and USER1/LLOCKo#/IOWR#

The USER0/WAITO# and USER1/LLOCKo# signals are not available in ISA Interface mode, even if the ISA I/O space is not configured, as these pins (138 and 139, respectively) are redefined as IORD# and IOWR#, respectively. The associated register bits, CNTRL[5:0], must be x10x10b to set configuration as USER0 and USER1 outputs. The pins are initially USER0 and USER1 inputs, which are floated until ISA Interface mode is enabled by serial EEPROM initialization, approximately 750 µs after PCI reset de-assertion (assuming the PCI clock frequency is 33 MHz).

For 16-bit I/O and all 8-bit transactions, IORD# and IOWR# assert on the falling clock edge after BALE de-asserts.

5.2.4 ALE/BALE

In ISA Interface mode, the ALE signal remains defined as ALE for Local Address Spaces 2 and 3 and Expansion ROM, and is renamed BALE for Local Address Spaces 0 and 1 (ISA Interface Memory and I/O). BALE asserts on the falling edge of LCLK, and de-asserts on the next rising edge. BALE pulse width is dependent upon LCLK frequency.

ALE asserts during the same clock as ADS# assertion. BALE asserts in the following clock period; therefore, the address and byte enables are valid for a minimum of two clocks prior to BALE de-assertion. (Refer to Figures 10-3 and 10-4 for ALE and BALE timing, respectively.)

5.2.5 NC/CHRDY

In ISA Interface mode, pin 45 provides CHRDY input, and should be pulled high (in legacy ISA systems, the motherboard provides the pull-up resistor). An ISA slave device de-asserts CHRDY to insert wait states.

A standard 16-bit transaction lasts for three clock cycles, but can be extended by de-asserting CHRDY within one clock cycle after MEMRD#, MEMWR#, IORD#, or IOWR# assertion. A standard 8-bit transaction lasts for six clock cycles, but can be extended by de-asserting CHRDY within three clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion.

In non-ISA Interface mode, pin 45 is a No Connect (NC); however, as a floating input, it should be tied high.

5.2.6 NC/NOWS#

In ISA Interface mode, pin 67 provides NOWS# input, which can be asserted by an ISA slave device to reduce the number of wait states.

A standard 16-bit Memory transaction lasts for three clock cycles, but can be shortened to two clock cycles by asserting both CHRDY and NOWS# within about one-half clock cycle after MEMRD# or MEMWR# assertion (one-half clock period, less command strobe output delay and NOWS# setup time). A standard 16-bit I/O transaction lasts for three clock cycles, but can be shortened to two clock cycles by asserting both CHRDY and NOWS# prior to IORD# or IOWR# assertion at the falling edge of the clock. A standard 8-bit transaction lasts for six clock cycles, but can be shortened to as few as two clock cycles by asserting both CHRDY and NOWS# within two clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion (number of clock cycles between command strobe assertion and NOWS# assertion, less command strobe output delay and NOWS# setup time).

The NOWS# signal is clocked into an internal register on the falling edge of the clock. The internal state machine then samples the registered version of NOWS# on the next rising edge of the clock.

NOWS# input is ignored if CHRDY is de-asserted to insert wait states. NOWS# is not used by 16-bit I/O legacy ISA devices. This signal is held normally de-asserted by an internal 80K-Ohm pull-up resistor. In Non-ISA Interface mode, this pin is a No Connect (NC) and can be left unterminated or tied high.

5.2.7 Other Local Bus Signals

Non-ISA mode Local bus signals ADS#, LW/R#, RD#, WR# and BLAST# are active during ISA transactions. Configuring the RD# and WR# strobes in LAS0BRD and LAS1BRD (for ISA spaces) does not affect ISA signaling.

The ISA state machine generates an internal ready signal, ISARDY, for which timing is determined by CHRDY, NOWS#, and the width of the ISA transaction. ISARDY is a one-clock wide pulse, and is only sampled if the internal wait state generator has counted down to zero. If the internal wait state generator has not reached zero when ISARDY pulses, the pulse is missed and the Local Master state machine locks up. The duration of the ISA cycle is intended to be controlled only by IOCHRDY and NOWS#, not by the internal wait state generator.

5.3 CONFIGURING LOCAL REGISTERS FOR ISA INTERFACE MODE

Address space sizes are fixed at boot time and configured by programming the Local Address Space Range registers in the serial EEPROM. The LAS0RR register is used to program the ISA Interface Memory space size. The LAS1RR register is used to program the ISA Interface I/O space size. I/O space size is restricted to 256 bytes maximum, per *PCI r2.2*.

The Local base address (address generated on the Local Bus for the lowest address in the Space) must be programmed in the LAS0BA and LAS1BA registers for the ISA Interface Memory and I/O spaces, respectively. Chip Select 0 and 1 Base Address registers (CS0BASE and CS1BASE, respectively) must be programmed to match Local Address Space 0 configuration for ISA Interface Memory and Local Address Space 1 configuration for ISA Interface I/O, respectively; otherwise, the ISA Interface is never acknowledged.

In the Local Address Space Bus Region Descriptor registers (LAS0BRD for ISA Interface Memory and LAS1BRD for ISA Interface I/O), LRDYi# must be enabled, burst disabled, and internal wait state fields must be zero (0) for ISA Interface mode to properly function. Bus width for the ISA Interface Memory- and I/O-mapped spaces are independently configurable as 8 or 16 bit. Prefetch can be enabled in LAS0BRD for the ISA Interface Memory-Mapped Address space. I/O-Mapped Address space is not prefetched.

For unused spaces, program the serial EEPROM with register default values (generally 0h) for the associated LAS*x*RR, LAS*x*BA and LAS*x*BRD registers, as well as the CS*x*BASE register for the unused ISA Interface Memory or I/O space (where *x* is the Local Address Space number or Chip Select number, as appropriate).

Notes: *For ISA Interface mode register settings, use the following:*

- ***INTCSR Register Settings****—Table 5-3 and the INTCSR register description (Register 8-43)*
- ***CNTRL Register Settings****—Table 5-4 and the CNTRL register description (Register 8-44)*
- ***LAS0RR and LAS1RR Register Settings****—Table 5-5 and the LASxRR register descriptions (Registers 8-24 and 8-25)*
- ***LAS0BA and LAS1BA Register Settings****—LASxBA register descriptions (Registers 8-29 and 8-30)*
- ***LAS0BRD and LAS1BRD Register Settings****—Table 5-6 and the LASxBRD register descriptions (Registers 8-34 and 8-35)*
- ***CS0BASE and CS1BASE Register Settings****—Section 6 and the CSxBASE register descriptions (Registers 8-39 and 8-40)*

Local Base Addresses must be a multiple of the address space size (which is a power of 2) or 0h. This restriction may require increasing the range, lowering the base address, and adding a software offset to generate the desired ISA Interface addresses. Each of the Local Address Spaces should be configured to not overlap, by programming the Local Address Space Base Address registers (LAS*x*BA) with unique base addresses. It is possible for the Local Address Spaces to share common addresses, as independent sets of Read and Write control signals are provided (MEMRD# and MEMWR# for ISA Interface Memory, IORD# and IOWR# for ISA Interface I/O, and RD# and WR# and/or LW/R# for Spaces 2 and 3 and Expansion ROM in ISA Interface mode).

Also, if either of the available chip selects CS[3:2]# are programmed to enable access to shared Local addresses, each might enable multiple devices. *For example*, if LW/R# is used for Space 2 read/write access and MEMRD# is used for ISA Interface Memory, and the Local Address Spaces overlap, a read of Space 0 could cause a simultaneous write to the shared Local Address in Space 2.

Table 5-3. INTCSR Register Settings in ISA Interface Mode

Bit	Description	Value after Serial EEPROM Load
9:0	Refer to the INTCSR register (Register 8-43).	—
12	ISA_MODE feature enabled. Must be set to 1.	1

Note: *Serial EEPROM value of "X" represents "don't care."*

Table 5-4. CNTRL Register Serial EEPROM Settings

Bit	Value	Description
5:0	x10x10b	Enable USER[1:0] as outputs for IORD# and IOWR#.
11:6	xxxxxxb	USER2/CS#2 and USER3/CS3# configuration.
13:12	00b	Must be 0 for PC platform.
14	1	Must be 1 for *PCI r2.1* protocol.
15	x	Flush pending read for write.
16	x	Recommend 1 to enable Memory Read Ahead.
17	x	PCI Retries for Writes.
18	1	Disconnect PCI when Write FIFO is full.
22:19	3h to Fh	Used for reads only if CNTRL[14]=0. Used for writes only if CNTRL[18]=0.
31:23	000000000b	Refer to CNTRL register description (Register 8-44).

Table 5-5. LAS0RR and LAS1RR Register Serial EEPROM Settings

Bit	Memory LAS0RR	I/O LAS1RR	Comments
0	0	1	Memory- or I/O-mapping.
1	0	0	—
2	0	x	I/O space size of 4 bytes, 1; otherwise, 0.
3	x	x	Memory, 1, unless not prefetchable. I/O, 1, only for space size of 4 or 8 bytes.
27:4	xxxxxxh	FFFFFxh	Range, I/O maximum is 256 bytes.
31:28	xxxx	xxxx	Don't Care.

Table 5-6. LAS0BRD and LAS1BRD Register Serial EEPROM Settings

Bit	Memory LAS0BRD	I/O LAS1BRD	Comments
0	0	0	Burst is disabled on the Local Bus.
1	1	1	Enable internal ready logic for ISA interface.
2	0	0	BTERM# feature is not used.
4:3	xx	00b	Memory, non-zero Prefetch Count if bit [5]=1 for Read Ahead if CNTRL[16]=1. I/O, prefetch disabled with bits [5:3]=100b.
5	1	1	Prefetch enabled for Memory Read Ahead.
10:6	00000	00000	No NRAD Read Address-to-Data wait states.
12:11	00	00	No NRDD Read Data-to-Data wait states.
14:13	00	00	No NXDA Data-to-Address wait states.
19:15	00000	00000	No NWAD Write Address-to-Data wait states.
21:20	00b	00b	No NWDD Write Data-to-Data wait states.
23:22	0xb	0xb	Bus width, 00 for 8-bit or 01 for 16-bit.
25:24	xxb	xxb	Big/Little Endian and byte ordering.
27:26	xxb	xxb	RD# strobe delay is not used in ISA spaces.
29:28	xxb	xxb	WR# strobe delay is not used in ISA spaces.
31:30	xxb	xxb	Write Cycle Hold is not used in ISA spaces.

5.4 DESIGN CONSIDERATIONS

5.4.1 Interrupts

Legacy ISA cards configure a particular IRQ for interrupt routing, typically selected using jumpers. The selected IRQ signal (if any) should be routed to one of the LINTi[2:1] input pins.

Legacy ISA systems use a positive edge-triggered interrupt controller input to latch the interrupt, and the legacy ISA device is not required to hold an interrupt request asserted until serviced (although it may). The LINTi[2:1] pins are configured by default as active-low level-triggered inputs, for which an interrupt clears when the interrupt source is de-asserted. However, for ISA compatibility, either or both of the LINT[2:1] inputs can be configured as positive edge-triggered latched inputs, for which an interrupt can be cleared only by software.

Refer to Section 7 for additional interrupt information. Refer to Section 9.2.1 for pull-up/pull-down resistor recommendations for the LINT[2:1]# pins.

5.4.2 Address and Control Signals

In Legacy ISA cards, addressing is determined on the card (typically by jumpers). A legacy ISA design also contains address decode/comparator circuitry to enable read/write access within a range of addresses. When converting an ISA slave design to PCI, often the ISA address generation and comparator circuitry can be removed as the PCI 9052 performs the address decoding. Also the legacy ISA address can be replaced by a programmed base address, with a more convenient value for software (*such as* 0).

Legacy ISA addresses, *such as* those for COM ports, are not available in PCI I/O space because typically the first 1 KB of I/O addresses are reserved for PC compatibility, and the host bridge does not forward accesses in this range to the PCI Bus. However, each Local Address Space can be configured to generate a specific Local Bus base address for a PCI access to the address in a PCIBAR register for a Local Address Space, by programming the address into the Local Base Address register (each Local base address must always be a multiple of the size of its Local Address Space). Therefore, while legacy ISA hardware can be easily converted to a PCI 9052 design, any legacy ISA software for the design must be modified to obtain the base address PCI BIOS assigns, rather than use a fixed base address.

Often when converting an ISA slave design to PCI, additional chip select logic can be removed and replaced by PCI 9052 Chip Selects CS[3:2]#. With much of the front-end ISA logic removed, the simplicity of the core design may become apparent. Consideration should be given toward converting the design to a Non-ISA Interface mode Local Bus. Some advantages of Non-ISA Interface mode over ISA Interface mode are as follows:

- Bus width can be expanded to 32-bit
- CS[1:0]# chip select pins become available
- USER[1:0] general purpose I/O pins become available
- RD# and WR# strobe timing can be programmed
- Internal wait state generator can be used

In converting a legacy ISA design to PCI, ISA IORD# and IOWR# or MEMRD# and MEMWR# signals can be replaced with the PCI 9052 RD# and WR# signals. The ISA BALE address latch signal is the same as the ALE signal; however, the ADS# address strobe is recommended for address latching, because the pulse width is longer than BALE (which retains a shorter pulse width at 33 or 40 MHz than at 8 MHz). Legacy ISA CHRDY signaling can be inverted to drive the LRDYi# ready input signal, or ready logic can be eliminated by using the internal wait state generator if timing parameters are known and constant.

5.4.3 Ready Signaling Protocol and Timing

Converting a legacy ISA slave design to PCI 9052 ISA or Non-ISA Interface modes should include an analysis of the legacy ISA, PCI 9052 ISA Interface, and PCI 9052 Non-Multiplexed mode protocols and timings for optimal design. The ensuing sections summarize NOWS# and CHRDY signaling for legacy ISA slave devices, and NOWS# and CHRDY sampling by the PCI 9052 ISA Interface. For a description of PCI 9052 non-ISA LRDYi# sampling, refer to Section 2.2.4.1.

5.4.3.1 Legacy ISA

A standard ISA Bus cycle for 8-bit devices includes four wait states. ISA protocol for sampling CHRDY and NOWS# for 8-bit Memory and I/O devices is to not sample during the first data time, and sample on the falling clock edge during the second, third, and fourth data times. If NOWS# and CHRDY were not previously asserted together to end the cycle, sample CHRDY—not NOWS# (because standard 8-bit Memory and I/O cycles use four wait states and therefore can no longer be shortened) at the rising clock edge of the fifth and any additional data times.

A standard ISA bus cycle for 16-bit devices includes one wait state. ISA protocol for sampling CHRDY# and NOWS# for 16-bit Memory devices is to sample on the falling edge during the first data time, and if NOWS# and CHRDY were not previously asserted together to end the cycle, sample CHRDY—not NOWS# (because a standard 16-bit Memory cycle uses one wait state and therefore can no longer be shortened) at the rising clock edge of the second and any additional data times.

ISA protocol for sampling CHRDY for 16-bit I/O devices is to not sample during the first data time, and to sample CHRDY at the rising clock edge of the second and any additional data times. CHRDY is not sampled during the first data time, and NOWS# is ignored because only 16-bit Memory devices are allowed zero wait state operation.

5.4.3.2 ISA Interface Mode

A standard 16-bit transaction lasts for three clock cycles, but can be extended by de-asserting CHRDY within one clock cycle after MEMRD#, MEMWR#, IORD#, or IOWR# assertion. A standard 8-bit transaction lasts for six clock cycles, but can be extended by de-asserting CHRDY within three clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion.

A standard 16-bit Memory transaction lasts for three clock cycles, but can be shortened to two clock cycles by asserting both CHRDY and NOWS# within about one-half clock cycle after MEMRD# or MEMWR# assertion (one-half clock period, less command strobe output delay and NOWS# setup time). A standard 16-bit I/O transaction lasts for three clock cycles, but

can be shortened to two clock cycles by asserting both CHRDY and NOWS# prior to IORD# or IOWR# assertion at the falling edge of the clock. A standard 8-bit transaction lasts for six clock cycles, but can be shortened to as few as two clock cycles by asserting both CHRDY and NOWS# within two clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion.

The NOWS# signal is clocked into an internal register on the falling edge of the clock. The internal state machine then samples the registered version of NOWS# on the next rising edge of the clock.

5.4.3.2.1 NOWS# Input Sampling

ISA protocol for reducing the number of wait states (from the default of four wait states for 8-bit transfers or one wait state for 16-bit transfers) during a Bus cycle is as follows—sample NOWS# halfway through the second data time as well as halfway through each subsequent data time, except for 16-bit memory accesses, in which case sampling begins halfway through the first data time (for possible zero wait state operation if both NOWS# and CHRDY are asserted). ISA protocol for 16-bit I/O transfers is to ignore NOWS#, and not compress such cycles.

The PCI 9052 samples its NOWS# input halfway through the first data time and halfway through each subsequent data time, for all accesses. This allows all accesses to be truly "zero wait state," even though ISA protocol allows Zero Wait State transfers for 16-bit Memory transactions only. Sampling of NOWS# during the first data time may cause conflict with ISA designs that expect the signal to be first sampled during the second data time for all 8-bit accesses, or which expect no sampling for 16-bit I/O accesses (providing a minimum of one wait state in either case). Usually there is no conflict, as ISA designs typically generate NOWS# from the command strobe along with the address, and PCI 9052 command strobe assertion occurs after the first NOWS# sampling (following BALE de-assertion) for 16-bit I/O and all 8-bit transactions.

If a conflict does exist, one solution is to assert NOWS# after the command strobe (MEMRD#, MEMWR#, IORD#, or IOWR#) is asserted, guaranteeing a minimum of one wait state. Another solution is to delay recognition of the NOWS# signal.

The circuit illustrated in Figure 5-1 may be incorporated into designs to delay recognition of the NOWS# signal. However, this circuit also adds a wait state to "zero wait state" 16-bit Memory accesses, or to other accesses where the NOWS# signal is dynamically asserted.

Using this circuit, when BALE is inactive (low), the signal to the PCI 9052 (the modified NOWS# signal) is unimportant. Once BALE goes active, for its half cycle duration, it presets the signal to the PCI 9052. The flip-flop is clocked with the rising edge of the Bus clock, so when NOWS# is asserted early, it is delayed one clock and therefore not sensed by the PCI 9052 until the ISA card expects it to be sensed.

Designers should look at the components involved to determine whether the system may benefit from early detection of NOWS#, or if this or some other method should be implemented to delay its detection.

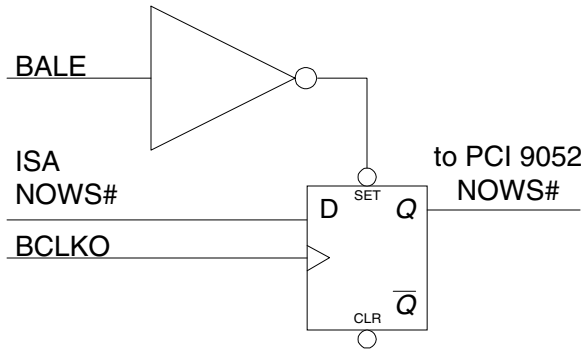
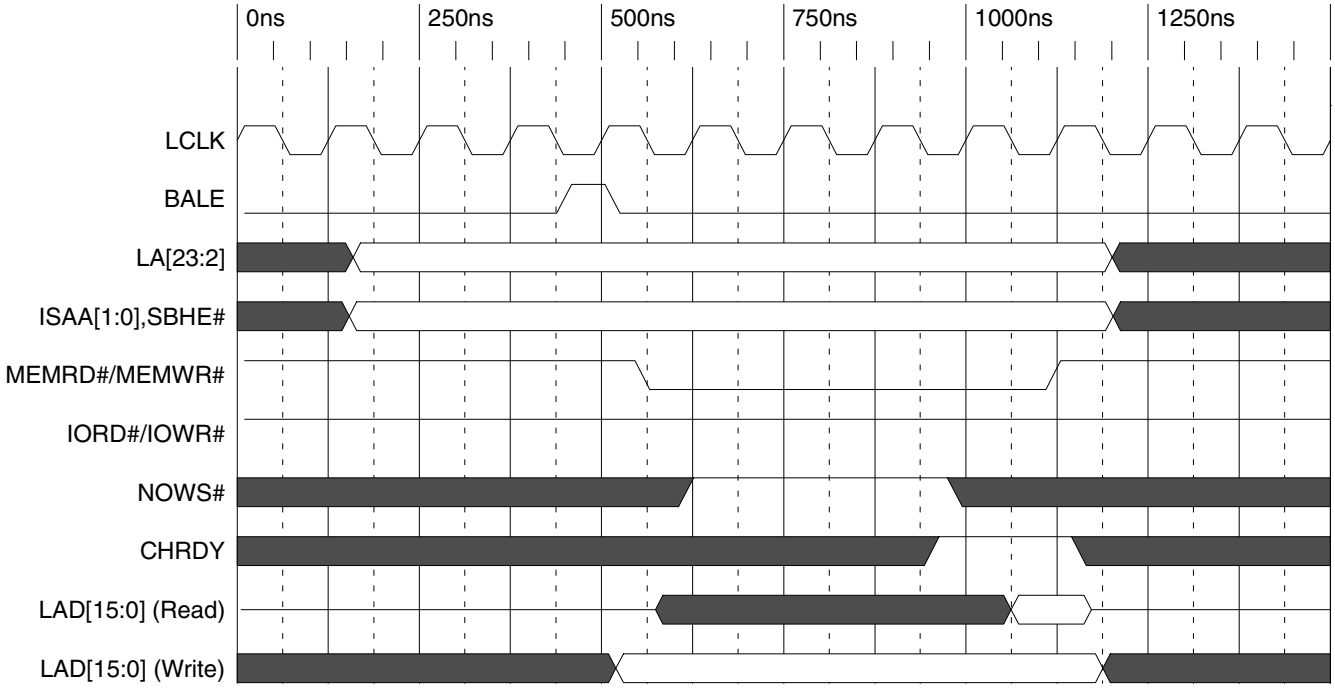
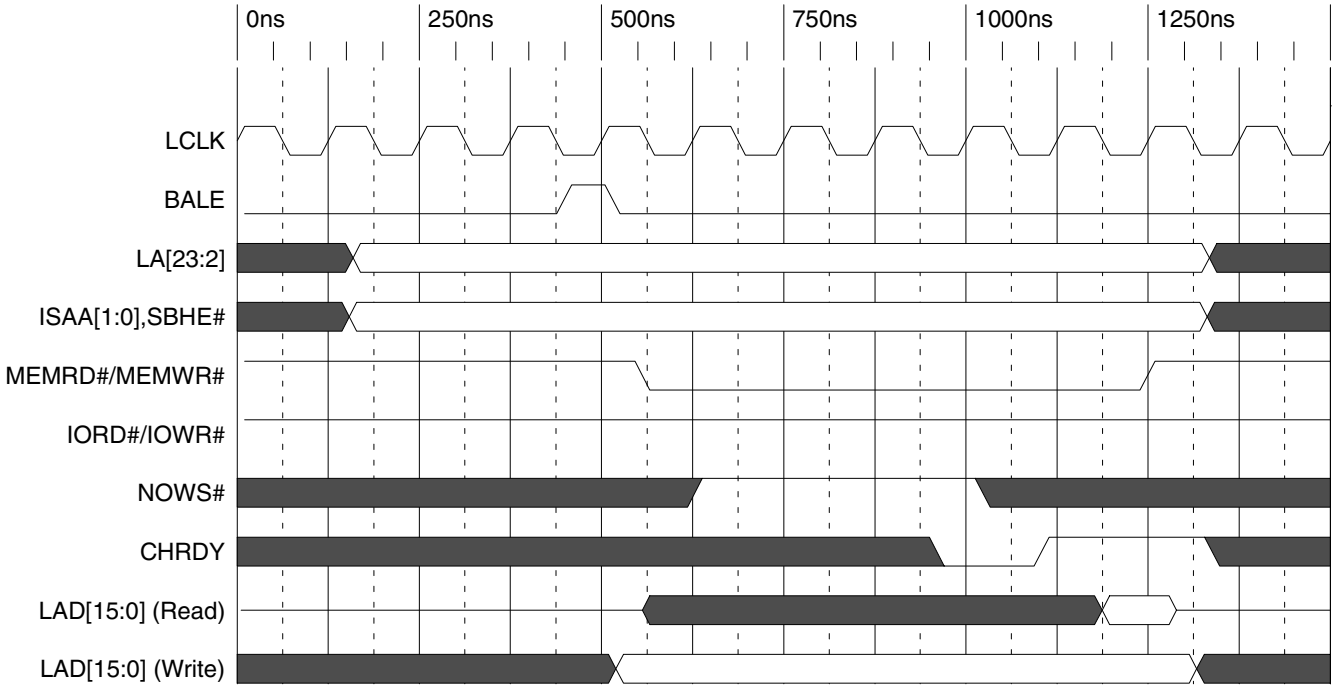


Figure 5-1. Circuit for Delaying NOWS# Recognition

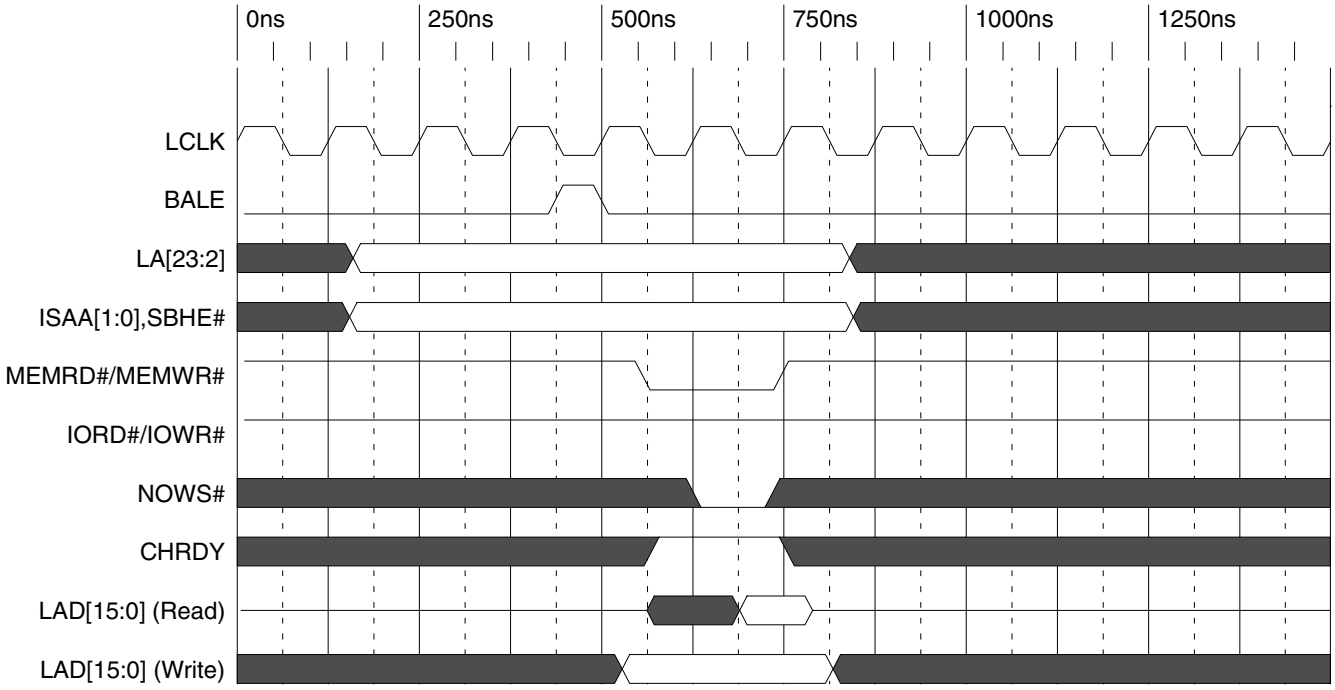
5.5 TIMING DIAGRAMS



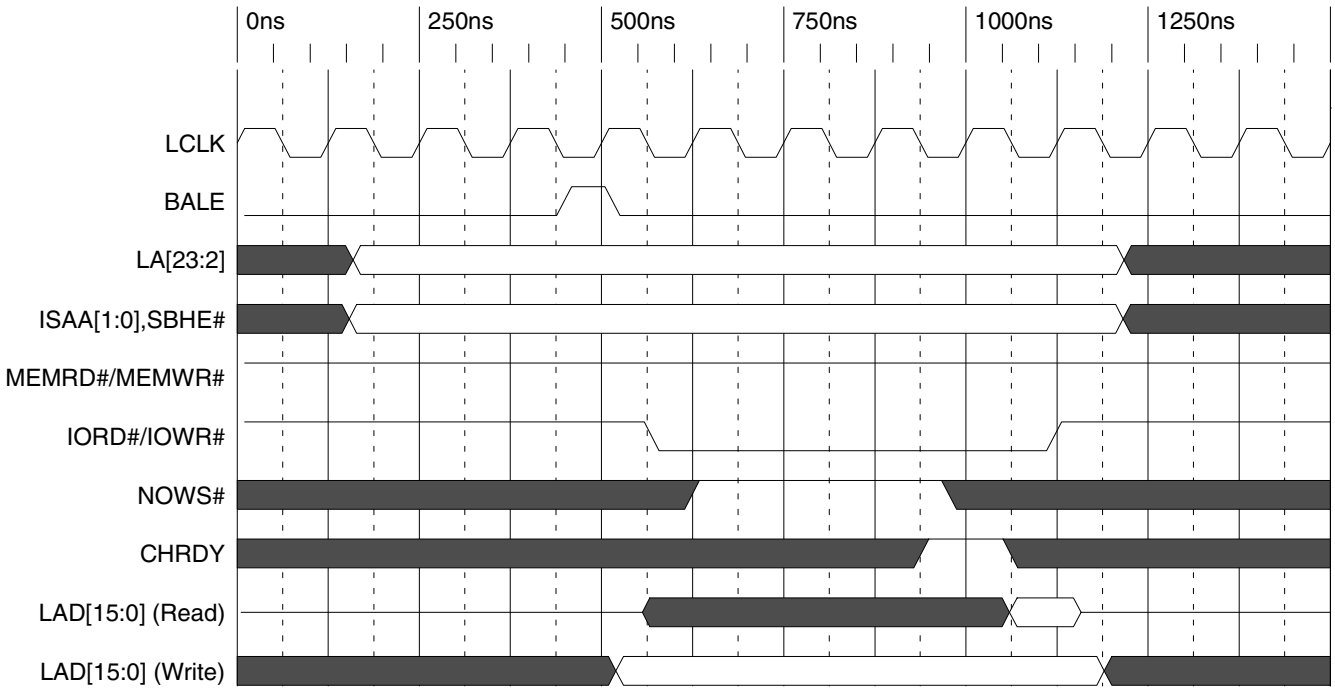
Timing Diagram 5-1. 8-Bit Memory Read/Write Standard ISA Cycle (6 LCLK Shown)



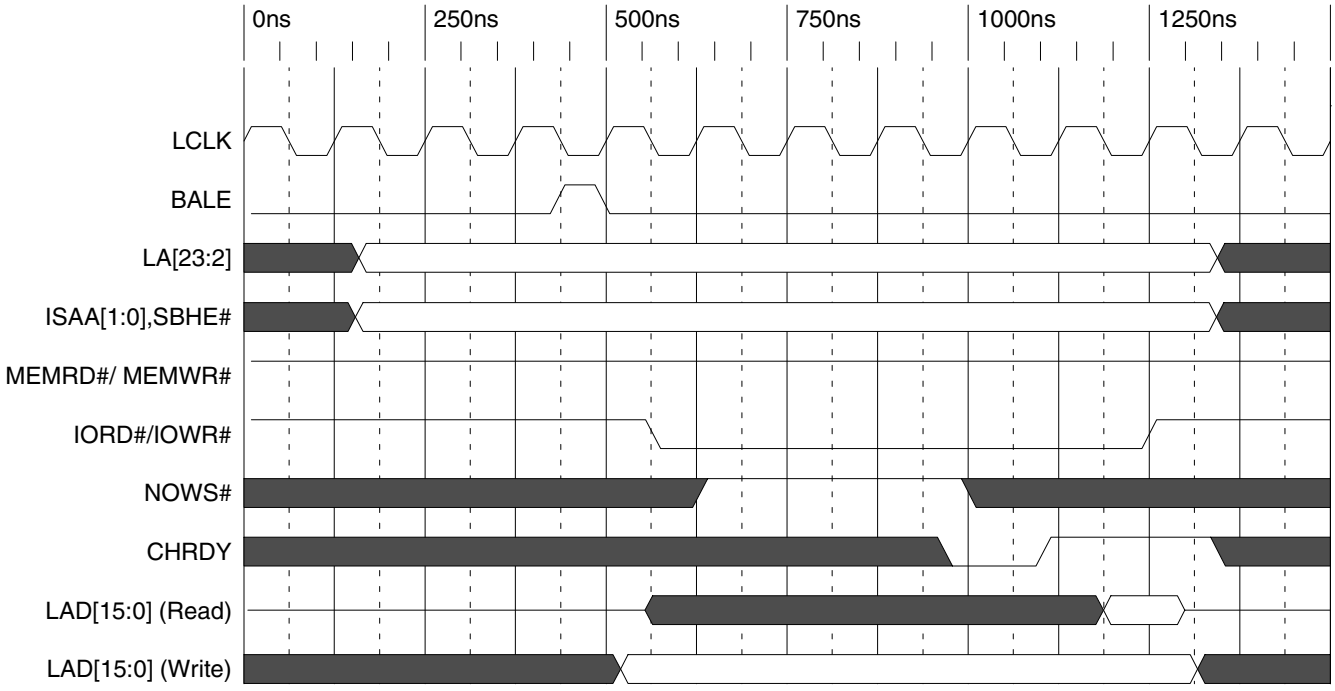
Timing Diagram 5-2. 8-Bit Memory Read/Write Extended ISA Cycle (7 LCLK Shown)



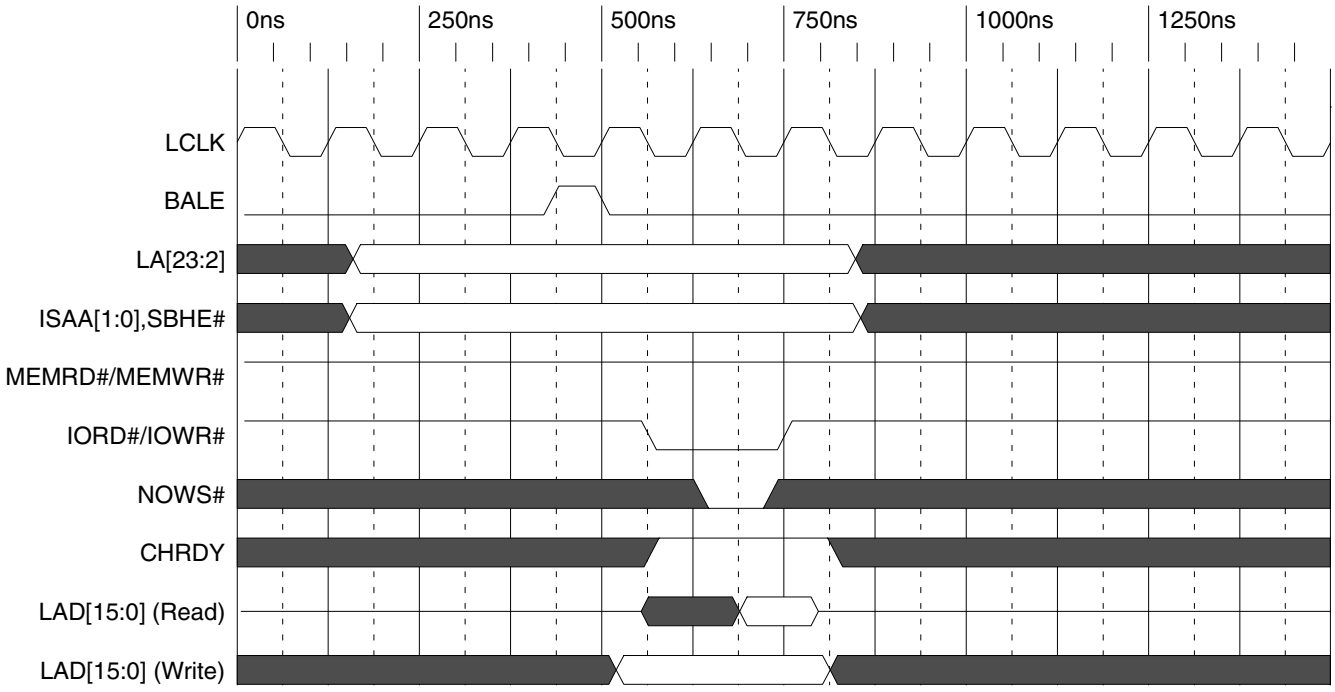
Timing Diagram 5-3. 8-Bit Memory Read/Write Compressed ISA Cycle (3 LCLK Shown)



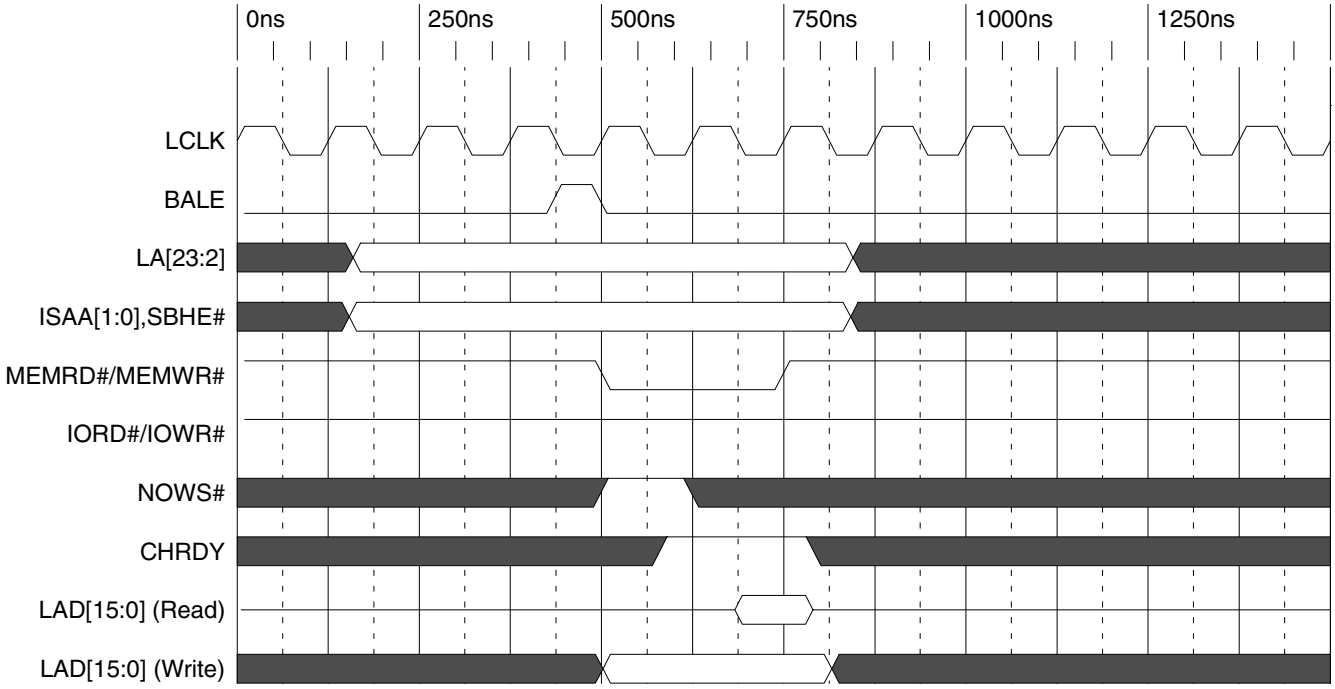
Timing Diagram 5-4. 8-Bit I/O Read/Write Standard ISA Cycle (6 LCLK Shown)



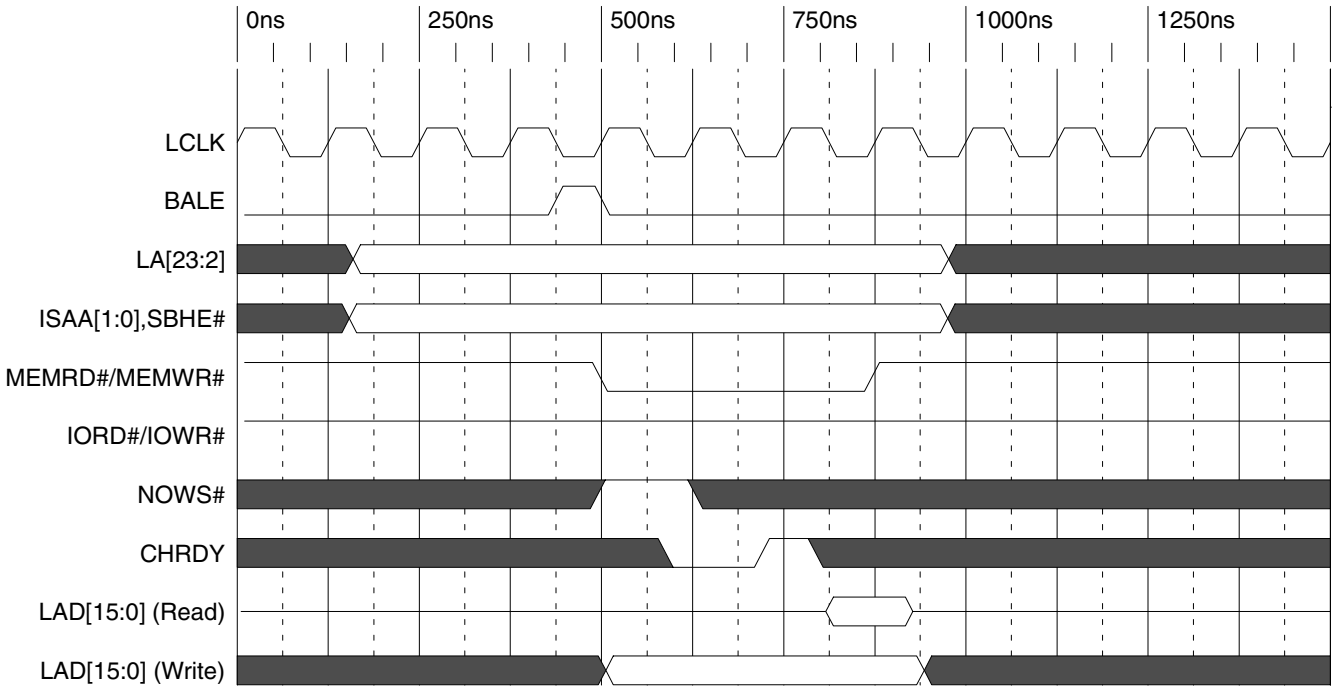
Timing Diagram 5-5. 8-Bit I/O Read/Write Extended ISA Cycle (7 LCLK Shown)



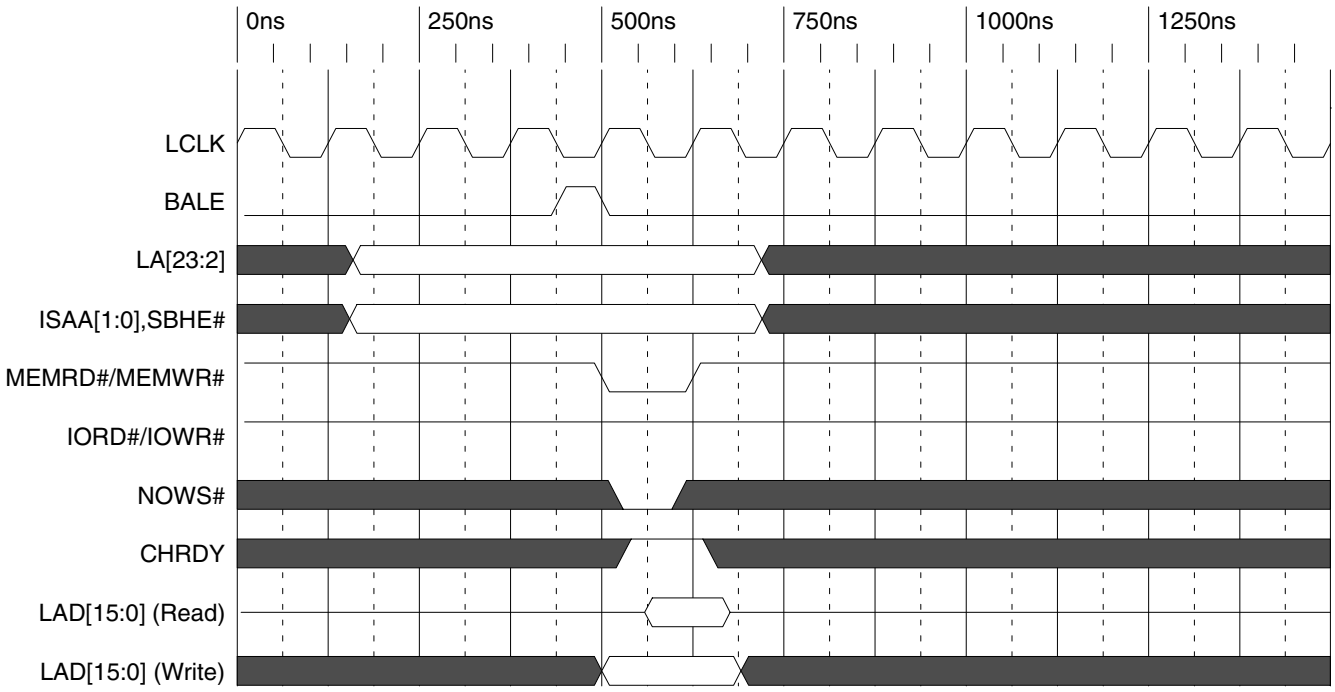
Timing Diagram 5-6. 8-Bit I/O Read/Write Compressed ISA Cycle (3 LCLK Shown)



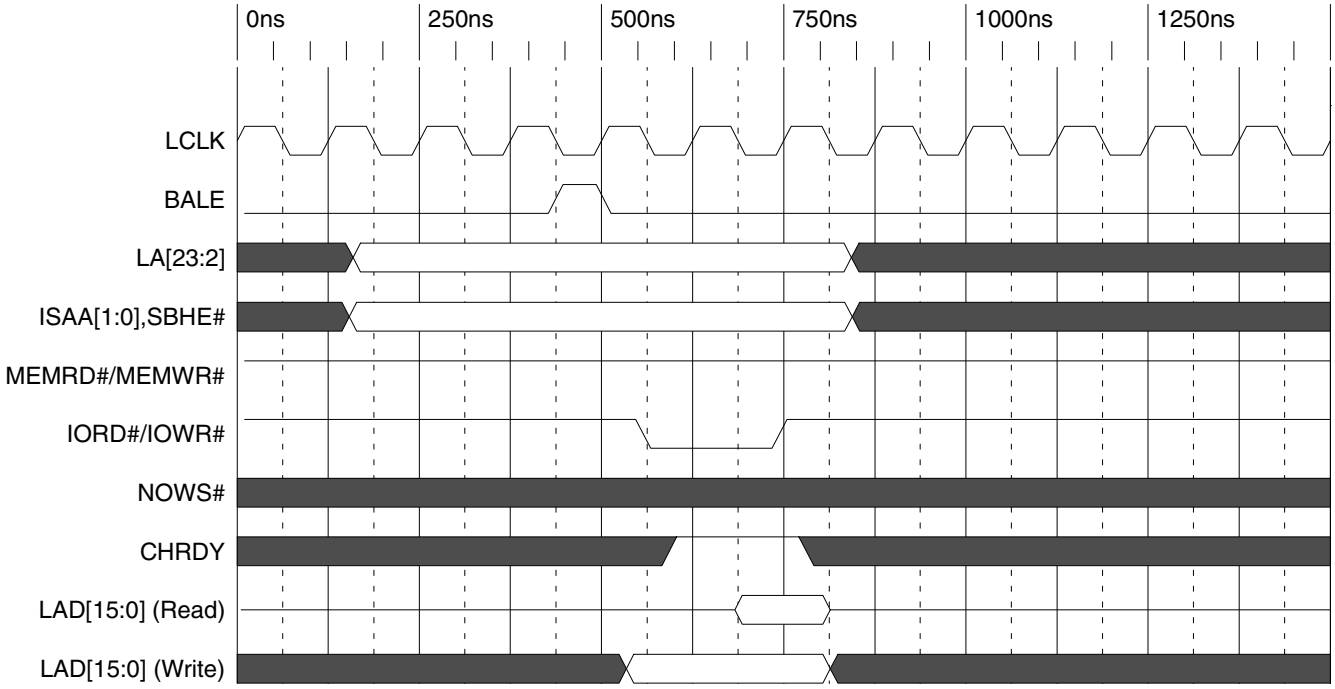
Timing Diagram 5-7. 16-Bit Memory Read/Write Standard ISA Cycle (3 LCLK Shown)



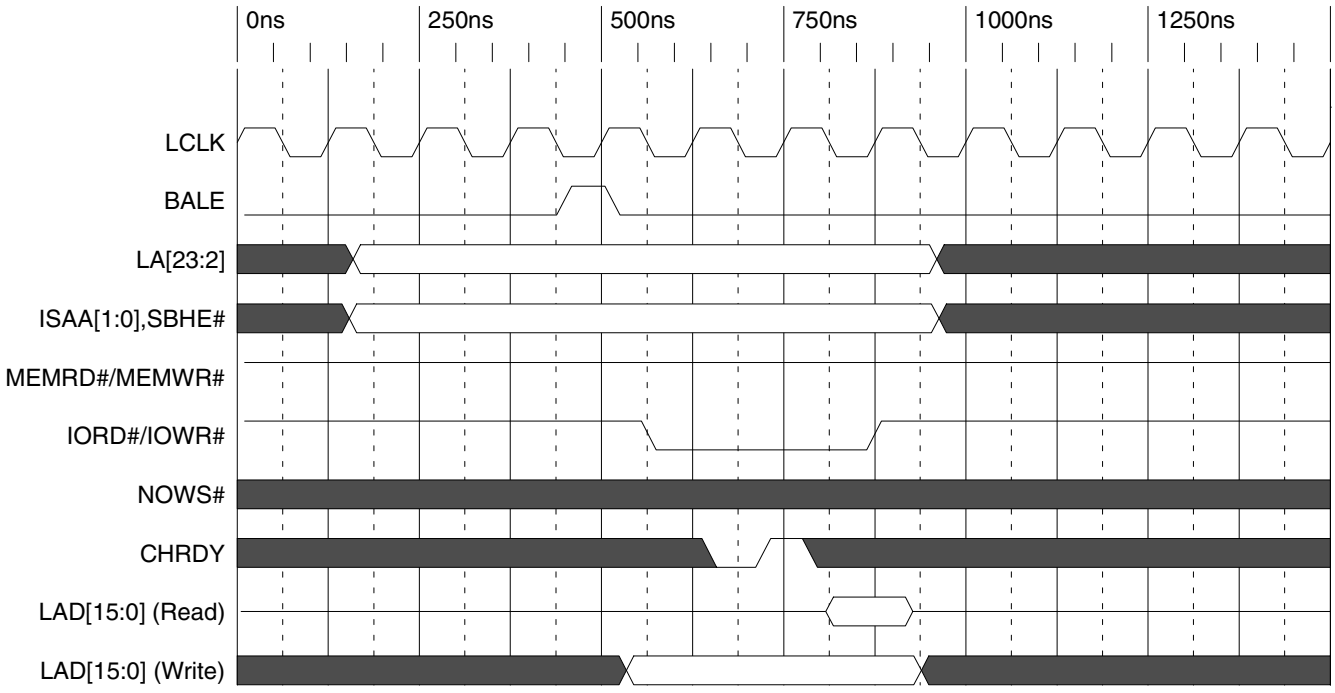
Timing Diagram 5-8. 16-Bit Memory Read/Write Extended ISA Cycle (4 LCLK Shown)



Timing Diagram 5-9. 16-Bit Memory Read/Write Compressed ISA Cycle (2 LCLK Shown)



Timing Diagram 5-10. 16-Bit I/O Read/Write Standard ISA Cycle (3 LCLK Shown)



Timing Diagram 5-11. 16-Bit I/O Read/Write Extended ISA Cycle (4 LCLK Shown)

6 LOCAL CHIP SELECT

6.1 OVERVIEW

The PCI 9052 provides four chip select outputs to selectively enable devices on its Local Bus. Each active-low chip select is programmable and independent of any local address space. Without this feature, external address decoding logic is required to implement chip selects.

6.2 CHIP SELECT BASE ADDRESS REGISTERS

There are four Chip Select Base Address registers. These registers control the four chip select pins on the PCI 9052. [*For example*, Chip Select 0 Base Address register (CS0BASE) controls CS0#, Chip Select 1 Base Address register (CS1BASE) controls CS1#, and so forth.]

Chip Select 0 and Chip Select 1 (CS0# and CS1#, respectively) are available in non-ISA Interface mode only (INTCSR[12]=0). In ISA Interface mode (INTCSR[12]=1), CS0BASE must be programmed to match valid LAS0RR and LAS0BA register configuration for ISA Memory (Space 0), and CS1BASE must be programmed to match valid LAS1RR and LAS1BA register configuration for ISA I/O (Space 1).

The Chip Select Base Address registers serve four purposes:

1. To enable or disable chip select functions within the PCI 9052. If enabled, the chip select signal is active if the Local Bus Address falls within the address specified by the range and base address. If disabled, the chip select signal is not active.
2. To set the range of the Local Bus Addresses for which the chip select signal(s) is active.
3. To set the Local Base Address, at which the range starts.
4. To configure ISA interface logic when in ISA Interface mode, for access to Space 0 Memory and Space 1 I/O addresses.

The three rules used to program the Chip Select Base Address registers are as follows:

1. Range must be a power of 2 (only the most significant bit is 1).
2. Base address must be a multiple of the range or 0.
3. Address range must be encompassed by one or more Local Address Spaces. Otherwise, the chip select decoder does not see addresses which have not been claimed by the PCI 9052 on behalf of a Local Address Space, and a chip select is not asserted.

   Chip selects are not bound to any particular Local Address Space unless programmed accordingly in the CS*x*BASE, LAS*x*RR, and LAS*x*BA registers (where *x* is the Chip Select number or Local Address Space number, as appropriate).

Each 28-bit Chip Select Base Address register is programmed, as listed in the following table.

Table 6-1. Chip Select Base Address Register Signal Programming

MSB=27						LSB=0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXY

The *Y* bit (bit 0) enables or disables the chip select signal. *X* bits are used to determine the range and base address of where the CS# pin is asserted. To program the base and range, the *X* bits are set as follows:

- Device length or range is specified by the first bit set above the *Y* bit. Determined by setting a bit in the register, calculated by shifting the range value (a power of 2) one bit to the right (range divided by 2).
- Base Address is determined by the bit(s) set above the range bit. The address is not shifted from its original value. The base address uses all bits in the register above (to the left of) the range bit, and none of the bits in the register at or below (to the right of) the range bit.

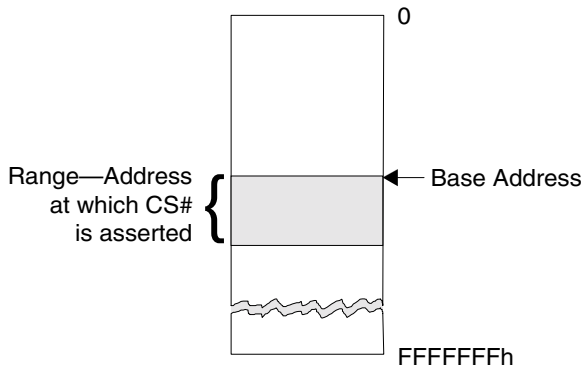


Figure 6-1. Chip Select Base Address and Range

6.3 PROCEDURE FOR USING CHIP SELECT BASE ADDRESS REGISTERS

The following describes the procedure for using the Chip Select Base Address registers.

1. Determine the range in hex. The range must be a power of 2 (only the highest order bit is set).
2. Set a bit in the Chip Select Base Address register to specify the range. Calculate this value by shifting the range value one bit to the right (range divided by 2). Only one bit may be set to encode the range.
3. Determine the base address. The base address must be a multiple of the range [the base address cannot contain ones (1) at or below (to the right of) the encoded range bit]. Set the base address directly into the bits above the range bit. The base address is not shifted from its original value.
4. Set the Enable bit (bit 0) in the Chip Select Base Address register to 1.

6.3.1 Chip Select Base Address Register Programming Example

A 16 KB SRAM device is attached to the Local Bus and a chip select is provided. The base address is specified to be 24000h. The following figure illustrates this example.

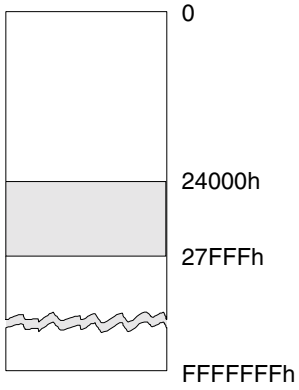


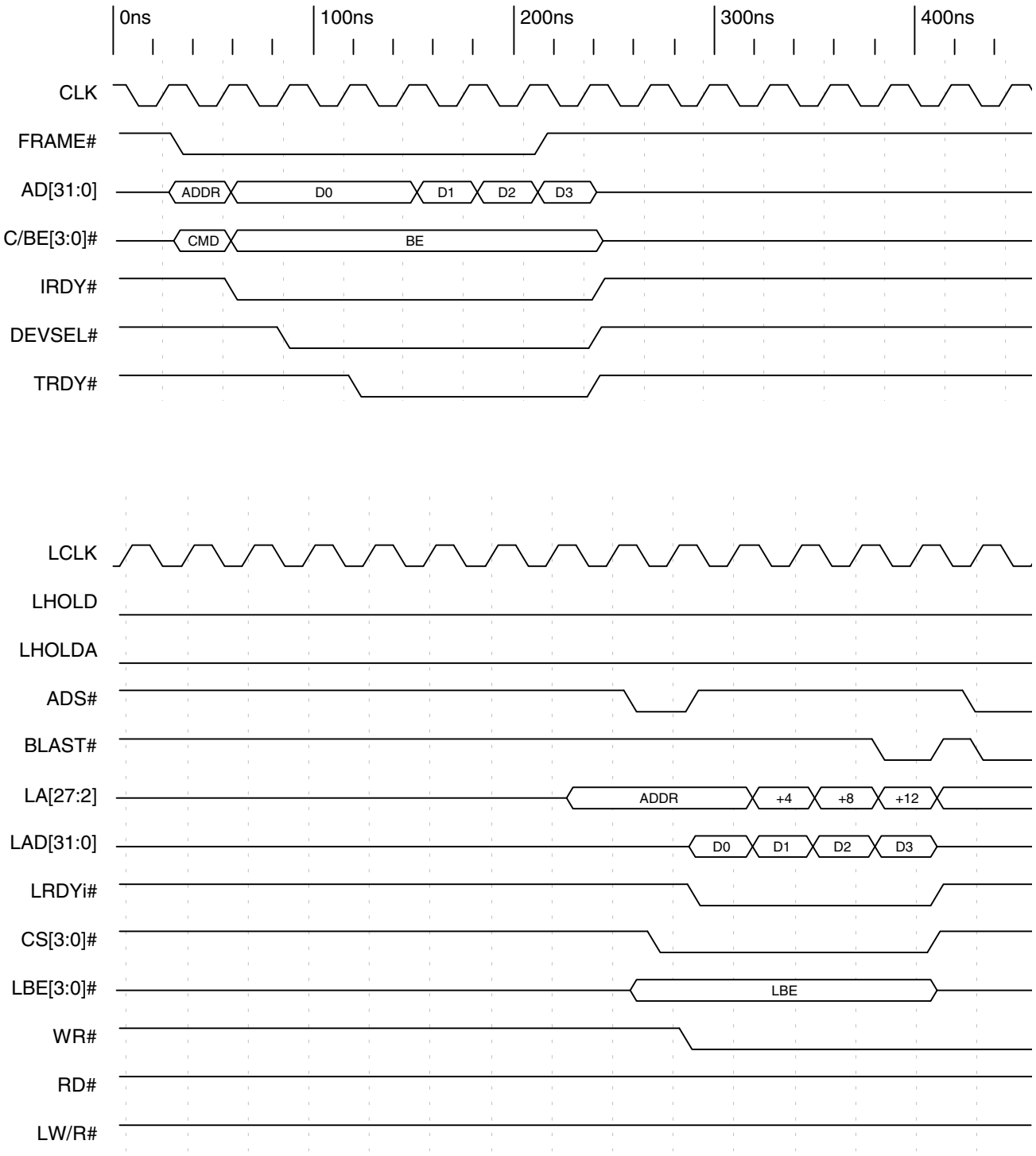
Figure 6-2. Memory Map Example

1. Determine the range in hex and divide the value by 2 (*for example*, 16 KB is equivalent to 4000h, leaving the range encoding at 2000h).
2. Determine the base address (*for example*, 24000h). Verify that the base address does not overwrite the range bit or any lower bits.
3. Set the base address into the bits above the range encoding. The base address is not shifted from its original value.
4. Set the Enable bit (bit 0).

The following is a complete example of setting the Chip Select Base Address register with a range of 4000h, a base address of 24000h, and enabled:

MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0001

6.4 TIMING DIAGRAM



Note: CS[3:0]# Base Address is in the range of Spaces 3 through 0

Timing Diagram 6-1. Chip Select [3:0]#

7 PCI/LOCAL INTERRUPTS AND USER I/O

7.1 OVERVIEW

The PCI 9052 provides two Local interrupt input pins (LINTi[2:1]) and a bit in the Interrupt Control/ Status register (INTCSR[7]) that can optionally trigger PCI interrupt INTA# output. The interrupt input pins have an associated register bit to enable or disable the pin (INTCSR[3, 0], respectively), and each has a Status bit to indicate whether an interrupt source is active (INTCSR[5, 2], respectively). The LINTi[2:1] pins are programmable for active-low or active-high polarity in the default Level-Sensitive mode. They can be optionally configured as a positive edge-triggered interrupt (*such as* for ISA compatibility).

Level-sensitive interrupts are cleared when the interrupt source is no longer active, or the interrupt input pin is disabled. Edge-triggered (latched) interrupts remain active until cleared by a software write, which either asserts the associated Interrupt Clear bit(s) (INTCSR[11 and/or 10]), or disables the interrupt input pin(s) (LINT[2:1]). INTA# output can also be de-asserted by clearing the PCI Interrupt Enable bit (INTCSR[6]=0).

7.2 INTERRUPTS

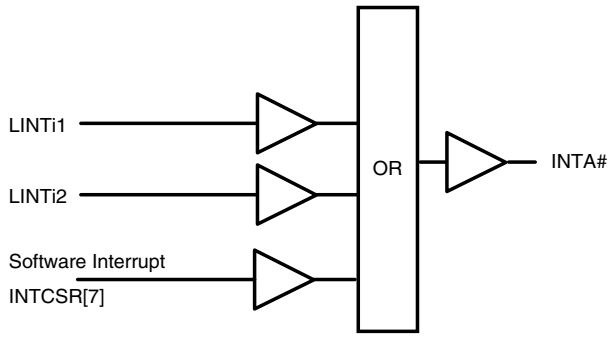


Figure 7-1. Interrupt and Error Sources

7.2.1 PCI Interrupts (INTA#)

A PCI 9052 PCI Interrupt (INTA#) can be asserted by Local Interrupt Input 2 or 1 (LINTi[2:1]), which are described in the next section. INTA# can also be asserted by setting the Software Interrupt bit (INTCSR[7]=1).

INTA# can be enabled or disabled (default configuration) in the PCI Interrupt Enable bit (INTCSR[6]). If a PCI interrupt is required, the PCI Interrupt Pin register must be set to a value of 1h at boot time by the serial EEPROM (PCIIPR[7:0]=1h), or chip default value 1h if a blank or no serial EEPROM is used, so that BIOS can route INTA# to an interrupt controller interrupt request (IRQ) input. BIOS writes the assigned IRQ number to the PCI Interrupt Line register (PCIILR). PCIILR register bit values are system-architecture specific.

An INTA# assertion generated from either LINTi[2:1] inputs, configured as level-sensitive interrupts, is cleared when one of the following occurs:

- Interrupt source is no longer active
- Interrupt input pin(s) (LINTi[2:1]) is disabled
- PCI interrupts are disabled (INTCSR[6]=0)

Subsequent to disabling interrupts, if the Local interrupt input remains asserted and interrupts are re-enabled, another interrupt is generated.

An INTA# assertion generated from either LINTi[2:1] inputs, configured as edge-triggered interrupts, remains active regardless of the LINTi[2:1] input pin state, until the interrupt is cleared with a software write that performs one of the following:

- Asserts the associated Interrupt Clear bit(s) (INTCSR[11 and/or 10])
- Disables the interrupt input pin(s) (LINTi[2:1])
- Disables PCI interrupts (INTCSR[6]=0)

Subsequent to disabling interrupts, if interrupts are re-enabled, another interrupt is not generated (even if the LINTi[2:1] input state remains high) until the next low-to-high transition on the LINTi[2:1] input pin occurs.

A software interrupt can be enabled by setting the Software Interrupt bit (INTCSR[7]=1). INTA# is asserted if the PCI Interrupt Enable bit is also set (INTCSR[6]=1). INTA# output is subsequently de-asserted when the Software Interrupt bit or PCI Interrupt Enable bit is cleared (INTCSR[7 or 6]=0, respectively).

INTA# is a level output. If INTA# is asserted or de-asserted in response to LINTi[2:1] input, INTA# output timing is asynchronous to the PCI and Local clocks. If INTA# is asserted or de-asserted by software, INTA# output timing is referenced to a rising edge of the PCI clock.

Note: *Regarding PLXMon, if PCI interrupts are enabled and the PCI 9052 generates an INTA#, the interrupt status displayed in PLXMon does not show the bit in the INTCSR runtime register as "active." This occurs because the PCI 9052 driver responds to the PCI interrupt and clears it. To test a PCI interrupt assertion and view active status with PLXMon, disable the PCI Interrupt Enable bit (INTCSR[6]=0), while keeping all other bit(s) required to generate the interrupt active. Then the driver does not see an INTA# assertion. After the screen is refreshed, following interrupt assertion, the active status can be seen in PLXMon.*

7.2.2 Local Interrupt Input (LINTi[2:1])

The PCI 9052 provides two local interrupt input pins, LINTi[2:1]. The Local interrupts can be used to generate a PCI interrupt, and/or software can poll the Interrupt Status bit(s) (INTCSR[5 and/or 2]). LINTi[2:1] are programmable for active-low or active-high polarity (INTCSR[4, 1]) in the default Level-Sensitive mode (INTCSR[9, 8]=00). Each pin can be optionally configured as a positive edge-triggered interrupt (INTCSR[8, 1, 0]=111b and INTCSR[9, 4, 3]=111b), *such as*, for ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or the interrupt input pin is disabled. Edge-triggered (latched) interrupts remain active until cleared by a software write, which asserts the associated Interrupt Clear bit(s) (INTCSR[11, 10]=11b), or disables the interrupt input pin (INTCSR[3, 0]=0). If the PCI Interrupt Enable bit is set (INTCSR[6]=1) and INTA# is asserted for a Local interrupt input assertion, INTA# can be de-asserted by clearing the PCI Interrupt Enable bit (INTCSR[6]=0).

PCI 9052 sampling of enabled LINTi[2:1] inputs, and INTA# output state changes (if PCI interrupts are enabled) in response to enabled LINT[2:1] input, are asynchronous to the PCI and Local clocks.

7.2.3 All Modes PCI SERR# (PCINMI)

The PCI 9052 asserts an SERR# pulse if Parity Error Response is enabled (PCICR[6]=1) and it detects an address parity error.

The SERR# output can be enabled or disabled with the SERR# Enable bit (PCICR[8]).

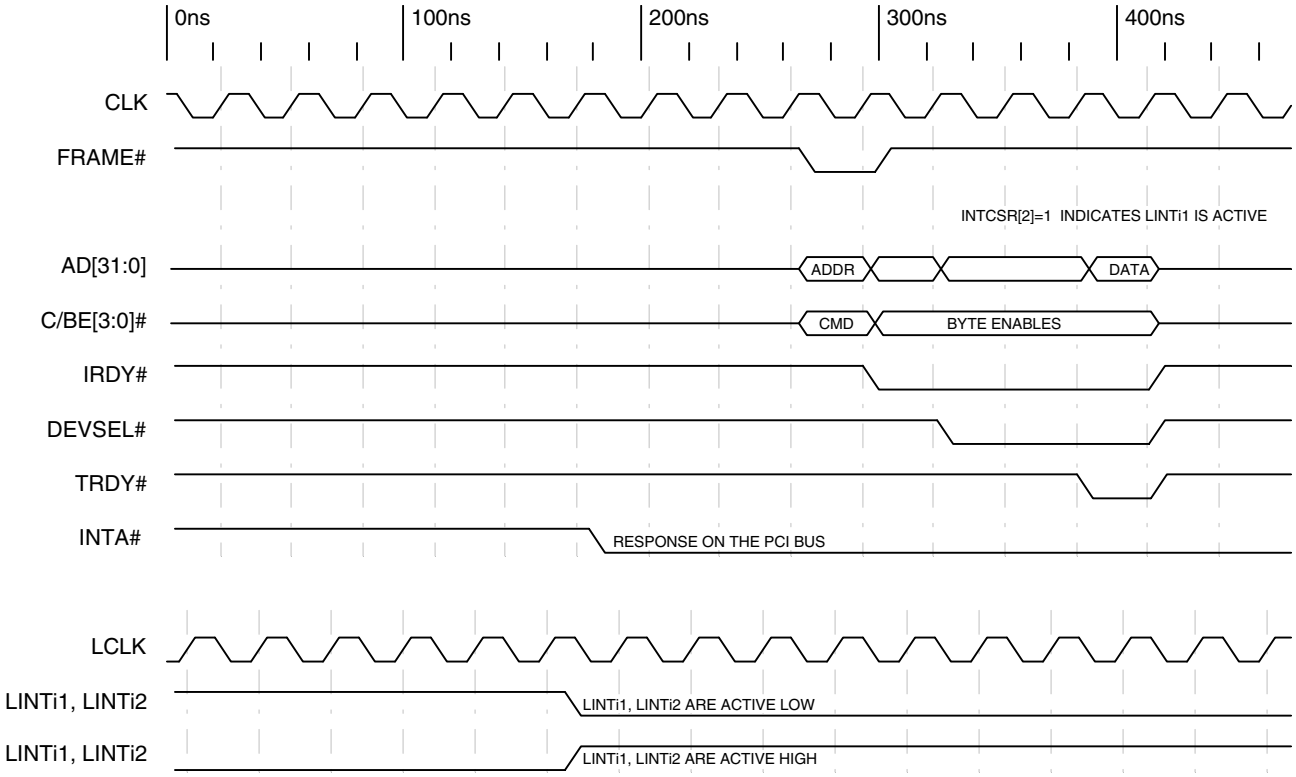
7.3 USER I/O

The PCI 9052 supports four user I/O pins, USER[3:0]. All are multiplexed with other functional pins—USER0/WAITO#, USER1/LLOCKo#, USER2/CS2#, and USER3/CS3#. Pin configuration is defined by bits in the CNTRL register. The default functionality for each of these pins is USER*x*. Default I/O configuration for all USER[3:0] pins is input.

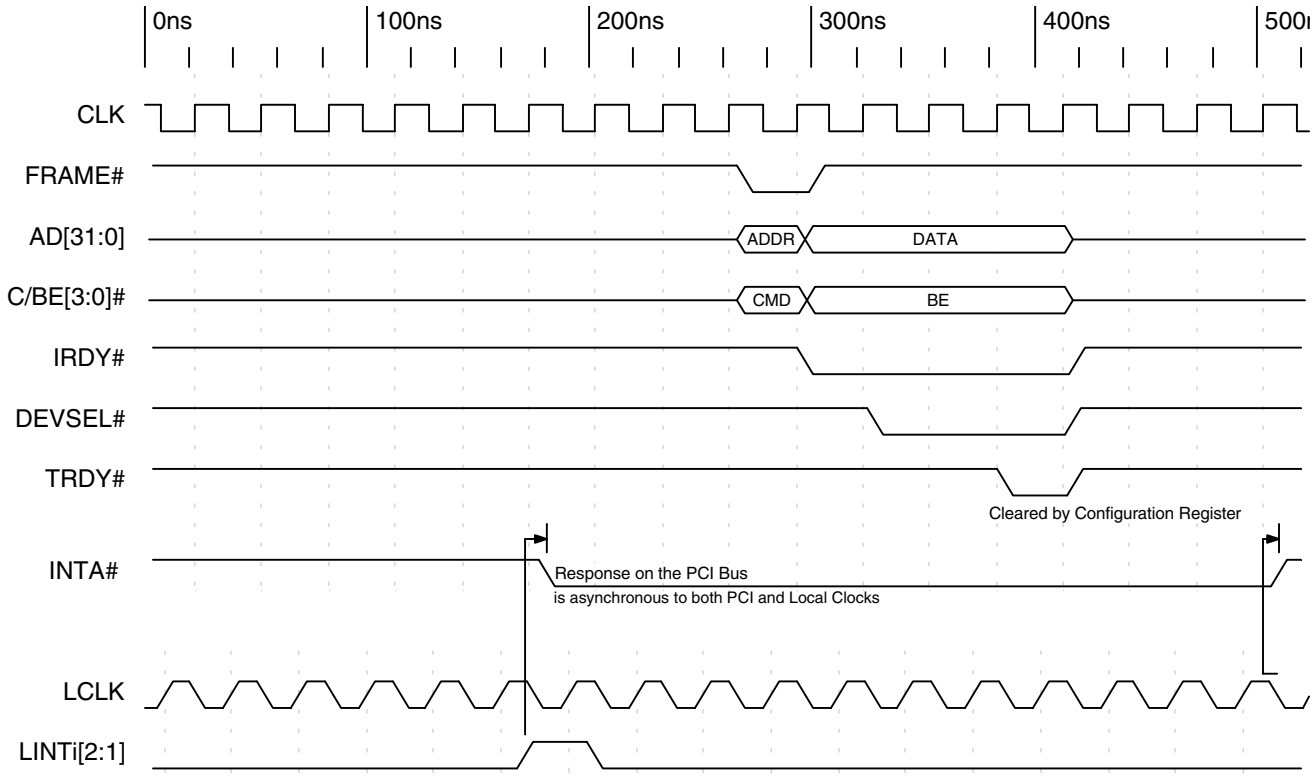
The PCI 9052 USER[3:0] I/O pins are active, regardless of whether the PCI 9052 owns the Local Bus.

It is recommended that unused USER I/O pins be configured as outputs, rather than the default setting as inputs; otherwise, input pins should be pulled to a known state.

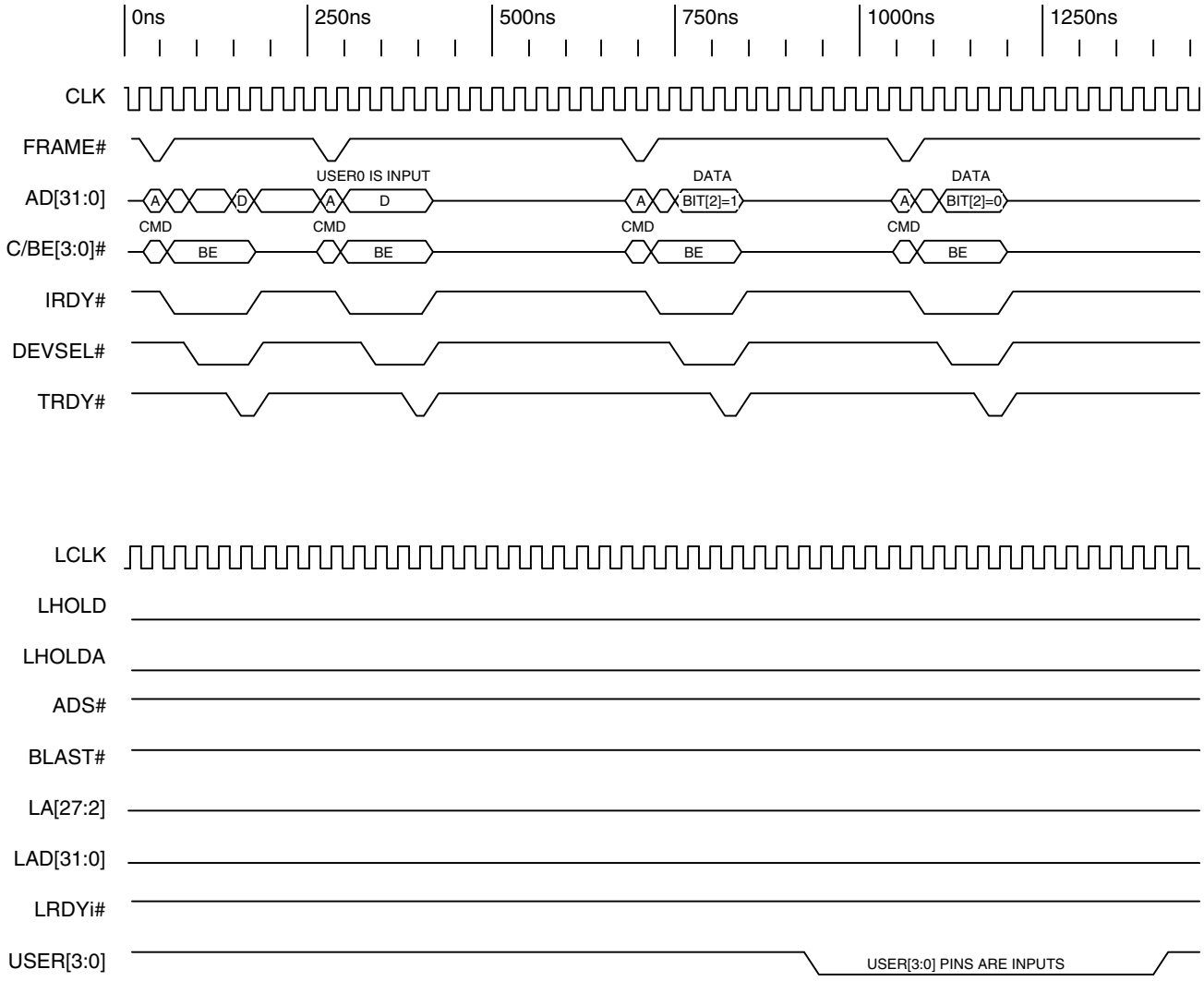
7.4 TIMING DIAGRAMS



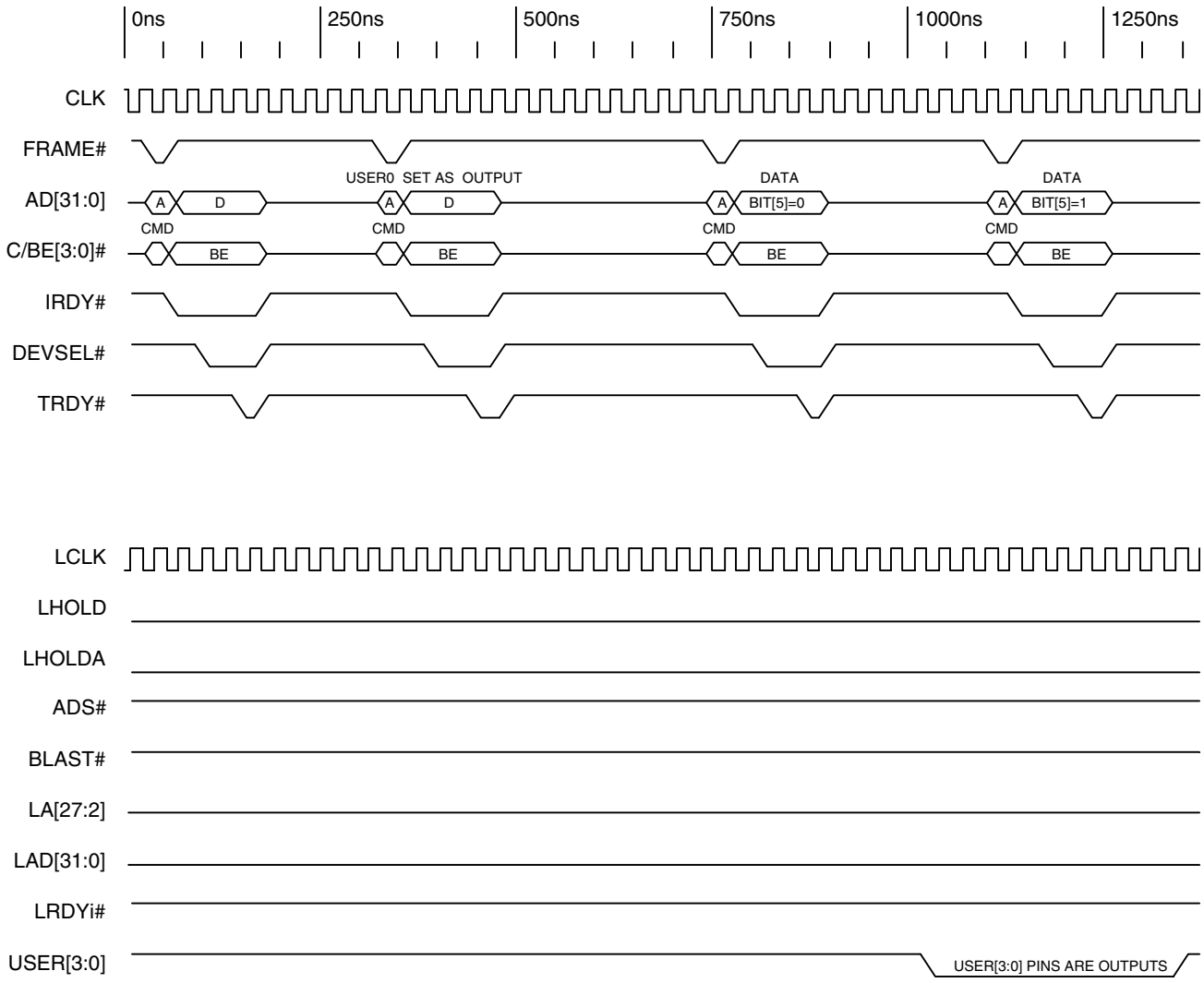
Timing Diagram 7-1. Local Level-Triggered LINTi/LINTi2 Asserting PCI Output INTA#



Timing Diagram 7-2. Local Edge-Triggered Interrupt Asserting PCI Interrupt



Timing Diagram 7-3. USER[3:0] as Inputs



Timing Diagram 7-4. USER[3:0] as Outputs

8 REGISTERS

8.1 REGISTER ADDRESS MAPPING

Table 8-1. PCI Configuration Registers

PCI Configuration Register Address	To ensure software compatibility with other versions of the PCI 9052 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24 23 16 15 8 7 0				PCI Writable	Serial EEPROM Writable
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	N
08h	Class Code			Revision ID	N	Y[31:8]
0Ch	Built-In Self Test ***(Not Supported)***	Header Type	PCI Bus Latency Timer ***(Not Supported)***	Cache Line Size	Y[7:0]	N
10h	PCI Base Address 0 for Memory Accesses to Local Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O Accesses to Local Configuration Registers				Y	N
18h	PCI Base Address 2 for Accesses to Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Accesses to Local Address Space 1				Y	N
20h	PCI Base Address 4 for Accesses to Local Address Space 2				Y	N
24h	PCI Base Address 5 for Accesses to Local Address Space 3				Y	N
28h	PCI Cardbus Information Structure (CIS) Pointer ***(Not Supported)***				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Expansion ROM Base Address				Y	N
34h	***Reserved***				N	N
38h	***Reserved***				N	N
3Ch	Maximum Latency ***(Not Supported)***	Minimum Grant ***(Not Supported)***	Interrupt Pin	Interrupt Line	Y[7:0]	Y[15:8]

Table 8-2. Local Configuration Registers

PCI (Offset from Local Base Address)	To ensure software compatibility with other versions of the PCI 9052 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI Writable	Serial EEPROM Writable
00h	Local Address Space 0 Range	Y	Y
04h	Local Address Space 1 Range	Y	Y
08h	Local Address Space 2 Range	Y	Y
0Ch	Local Address Space 3 Range	Y	Y
10h	Expansion ROM Range	Y	Y
14h	Local Address Space 0 Local Base Address (Remap)	Y	Y
18h	Local Address Space 1 Local Base Address (Remap)	Y	Y
1Ch	Local Address Space 2 Local Base Address (Remap)	Y	Y
20h	Local Address Space 3 Local Base Address (Remap)	Y	Y
24h	Expansion ROM Local Base Address (Remap)	Y	Y
28h	Local Address Space 0 Bus Region Descriptors	Y	Y
2Ch	Local Address Space 1 Bus Region Descriptors	Y	Y
30h	Local Address Space 2 Bus Region Descriptors	Y	Y
34h	Local Address Space 3 Bus Region Descriptors	Y	Y
38h	Expansion ROM Bus Region Descriptors	Y	Y
3Ch	Chip Select 0 Base Address	Y	Y
40h	Chip Select 1 Base Address	Y	Y
44h	Chip Select 2 Base Address	Y	Y
48h	Chip Select 3 Base Address	Y	Y
4Ch	Interrupt Control/Status	Y	Y
50h	User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control	Y	Y

8.2 PCI CONFIGURATION REGISTERS

All registers may be written to or read from using Byte, Word, or Lword accesses.

Register 8-1. (PCIIDR; 00h) PCI Configuration ID

Bit	Description	Read	Write	Value after Reset
15:0	**Vendor ID.** Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX, if blank or no serial EEPROM is present.	Yes	Serial EEPROM	10B5h
31:16	**Device ID.** Identifies particular device. Defaults to PLX part number for PCI interface chip if blank or no serial EEPROM is present.	Yes	Serial EEPROM	9050h

Register 8-2. (PCICR; 04h) PCI Command

Bit	Description	Read	Write	Value after Reset
0	**I/O Space.** Value of 1 allows the device to respond to I/O space accesses. Value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	**Memory Space.** Value of 1 allows the device to respond to Memory Space accesses. A value of 0 disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable.** ***Not Supported.***	Yes	No	0
3	**Special Cycle.** ***Not Supported.***	Yes	No	0
4	**Memory Write/Invalidate.** ***Not Supported.***	Yes	No	0
5	**VGA Palette Snoop.** ***Not Supported.***	Yes	No	0
6	**Parity Error Response.** Value of 0 indicates a parity error is ignored and operation continues. Value of 1 indicates parity error response is enabled [PERR# and SERR#, if SERR# is enabled (PCICR[8]=1)]. Parity error is always signaled in PCISR[15].	Yes	Yes	0
7	**Wait Cycle Control.** Controls whether the device does address/data stepping. Value of 0 indicates the device never does stepping. Value of 1 indicates the device always does stepping. ***Note:*** *Hardwired to 0.*	Yes	No	0
8	**SERR# Enable.** Value of 1 enables the SERR# driver. Value of 0 disables the SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable.** Indicates what type of fast back-to-back transfers a Master can perform on a bus. Value of 1 indicates fast back-to-back transfers can occur to any agent on the bus. Value of 0 indicates fast back-to-back transfers can occur only to the same agent as the previous cycle.	Yes	No	0
15:10	***Reserved***.	Yes	No	0h

Register 8-3. (PCISR; 06h) PCI Status

Bit	Description	Read	Write	Value after Reset
6:0	***Reserved.***	Yes	No	0h
7	**Fast Back-to-Back Capable.** Value of 1 indicates the adapter can accept fast back-to-back transactions. Value of 0 indicates the adapter cannot accept fast back-to-back transactions.	Yes	No	1
8	**Master Data Parity Error Detected.** ***Not Supported.***	Yes	No	0
10:9	**DEVSEL Timing**. Indicates timing for DEVSEL# assertion. Value of 01 is medium.	Yes	No	01
11	**Signaled Target Abort.** Value of 1 indicates the PCI 9052 signaled a Target Abort. Value of 1 clears the bit (0).	Yes	Yes/Clr	0
12	**Received Target Abort.** Value of 1 indicates the PCI 9052 received a Target Abort signal. ***Not Supported.***	Yes	No	0
13	**Received Master Abort.** Value of 1 indicates the PCI 9052 received a Master Abort signal. ***Not Supported.***	Yes	No	0
14	**Signaled System Error.** Value of 1 indicates the PCI 9052 reported a system error on the SERR# signal. Value of 1 clears the Error Status bit (0).	Yes	Yes/Clr	0
15	**Detected Parity Error.** Value of 1 indicates the PCI 9052 detected a PCI Bus parity error, even if parity error handling is disabled [the Parity Error Response bit in the Command register is clear (PCICR[6]=0)]. One of two conditions can cause this bit to be set when the PCI 9052 detects a parity error: 1) During a PCI Address phase; 2) When it was the Target of a write. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 8-4. (PCIREV; 08h) PCI Revision ID

Bit	Description	Read	Write	Value after Reset
7:0	**Revision ID.** PCI 9052 Silicon revision.	Yes	No	2h

Note: *Software can distinguish the PCI 9052 from the PCI 9050 using this register value, which is 1h in the PCI 9050.*

Register 8-5. (PCICCR; 09-0Bh) PCI Class Code

Bit	Description	Read	Write	Value after Reset
7:0	**Specific Register Level Programming Interface.** None defined.	Yes	Serial EEPROM	00h
15:8	**Subclass Encoding (80h).** (Other Bridge Device)**.**	Yes	Serial EEPROM	80h
23:16	**Base Class Encoding.** (Bridge Device).	Yes	Serial EEPROM	06h

Register 8-6. (PCICLSR; 0Ch) PCI Cache Line Size

Bit	Description	Read	Write	Value after Reset
7:0	**System Cache Line Size.** Specified in units of 32-bit Lwords. Can be written and read; however, the value does not affect PCI 9052 operation.	Yes	Yes	0h

Register 8-7. (PCILTR; 0Dh) PCI Bus Latency Timer

Bit	Description	Read	Write	Value after Reset
7:0	**PCI Bus Latency Timer.** ***Not Supported***.	Yes	No	0h

Register 8-8. (PCIHTR; 0Eh) PCI Header Type

Bit	Description	Read	Write	Value after Reset
6:0	**Configuration Layout Type.** Specifies layout of registers 10h through 3Fh in configuration space. Header Type 0 is defined for all PCI devices other than PCI-to-PCI bridges (Header Type 1) and Cardbus bridges (Header Type 2).	Yes	No	0h
7	**Multi-Function Device.** Value of 1 indicates multiple (up to eight) functions (logical devices) each containing its own, individually addressable configuration space, 64 Lwords in size. ***Note:*** *Hardwired to 0 (that is, device is single function, as multi-function = false).*	Yes	No	0

Register 8-9. (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST)

Bit	Description	Read	Write	Value after Reset
7:0	**Built-In Self Test.** Value of 0 indicates device passed its test. ***Not Supported***.	Yes	No	0

Register 8-10. (PCIBAR0; 10h) PCI Base Address 0 for Memory Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 0.*	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** ***Note:*** *Hardwired to 0.*	Yes	No	00
3	**Prefetchable.** Value of 1 indicates there are no side effects on reads. ***Note:*** *Hardwired to 0.*	Yes	No	0
6:4	**Memory Base Address.** Memory base address for access to Local Configuration registers (uses 128 bytes). ***Note:*** *Hardwired to 0.*	Yes	No	000
31:7	**Memory Base Address.** Memory base address for access to Local Configuration registers.	Yes	Yes	0h

Note: *PCIBAR0 can be enabled or disabled by using CNTRL[13:12].*

Register 8-11. (PCIBAR1; 14h) PCI Base Address 1 for I/O Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 1.*	Yes	No	1
1	***Reserved.***	Yes	No	0
6:2	**I/O Base Address.** Base Address for I/O access to Local Configuration registers (uses 128 bytes). ***Note:*** *Hardwired to 0.*	Yes	No	0h
31:7	**I/O Base Address.** Base Address for I/O access to Local Configuration registers.	Yes	Yes	0h

Note: *PCIBAR1 can be enabled or disabled by using CNTRL[13:12].*

Register 8-12. (PCIBAR2; 18h) PCI Base Address 2 for Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS0RR register.)	Yes	No	0
2:1	**Register Location (If Memory Space).** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect PCI 9052 operation. The associated Bus Region Descriptor register (LAS0BRD) controls prefetching functions of this address space. If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address Space 0.	Yes	Yes	0h

Note: *If allocated, Local Address Space 0 can be enabled or disabled by setting or clearing LAS0BA[0].*

Register 8-13. (PCIBAR3; 1Ch) PCI Base Address 3 for Accesses to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS1RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and provides only status to the system. Does not affect PCI 9052 operation. The associated Bus Region Descriptor register (LAS1BRD) controls prefetching functions of this address space. If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address Space 1.	Yes	Yes	0h

Note: *If allocated, Local Address Space 1 can be enabled or disabled by setting or clearing LAS1BA[0].*

Register 8-14. (PCIBAR4; 20h) PCI Base Address 4 for Accesses to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS2RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS2RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS2RR[3] and provides only status to the system. Does not affect PCI 9052 operation. The associated Bus Region Descriptor register (LAS2BRD) controls prefetching functions of this address space. If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address Space 2.	Yes	Yes	0h

Note: *If allocated, Local Address Space 2 can be enabled or disabled by setting or clearing LAS2BA[0].*

Register 8-15. (PCIBAR5; 24h) PCI Base Address 5 for Accesses to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS3RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS3RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS3RR[3] and provides only status to the system. Does not affect PCI 9052 operation. The associated Bus Region Descriptor register (LAS3BRD) controls prefetching functions of this address space. If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address Space 3.	Yes	Yes	0h

Note: *If allocated, Local Address Space 3 can be enabled or disabled by setting or clearing LAS3BA[0].*

Register 8-16. (PCICIS; 28h) PCI Cardbus Information Structure Pointer

Bit	Description	Read	Write	Value after Reset
31:0	**Cardbus Information Structure (CIS) Pointer for PC Cards.** ***Not Supported***.	Yes	No	0h

Register 8-17. (PCISVID; 2Ch) PCI Subsystem Vendor ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem Vendor ID.** Unique Add-in Board Vendor ID. ***Note:*** *PCISVID is a read-only register. However, a Configuration write to offset 2Ch overwrites the value in the PCI Interrupt Line register (PCIILR), possibly disabling PCI interrupt capability. (Refer to PCI 9052 Errata #3.)*	Yes	Serial EEPROM	0h

Register 8-18. (PCISID; 2Eh) PCI Subsystem ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem ID.** Unique Add-in Board Device ID. ***Note:*** *PCISID is a read-only register. However, a Configuration write to offset 2Ch overwrites the value in the PCI Interrupt Line register (PCIILR), possibly disabling PCI interrupt capability. (Refer to PCI 9052 Errata #3.)*	Yes	Serial EEPROM	0h

Register 8-19. (PCIERBAR; 30h) PCI Expansion ROM Base Address

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Value of 1 indicates a device accepts accesses to the Expansion ROM address. Value of 0 indicates a device does not accept accesses to Expansion ROM.	Yes	Yes	0
10:1	***Reserved***.	Yes	No	0h
31:11	**Expansion ROM Base Address (upper 21 bits).**	Yes	Yes	0h

Register 8-20. (PCIILR; 3Ch) PCI Interrupt Line

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Line Routing Value.** Indicates to which system interrupt controller(s) input the interrupt line is connected. The PCI 9052 does not use this value, rather the value is used by device drivers and operating systems for priority and vector information. Values in this register are system-architecture specific. For x86-based PCs, the values in this register correspond to IRQ numbers (0 through 15) of the standard dual 8259 interrupt controller configuration. The value 255 is defined as "unknown" or "no connection" to the interrupt controller. Values 15 through 255 are ***reserved***.	Yes	Yes	0h

Register 8-21. (PCIIPR; 3Dh) PCI Interrupt Pin

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Pin Register.** Indicates which interrupt pin the device uses. The following values are decoded: 0h = No Interrupt Pin 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# The PCI 9052 supports only INTA#. Because PCIHTR[7]=0, values 2h, 3h, and 4h have no meaning. All other values (05h through FFh) are reserved by *PCI r2.2*.	Yes	Serial EEPROM	1h

Register 8-22. (PCIMGR; 3Eh) PCI Minimum Grant

Bit	Description	Read	Write	Value after Reset
7:0	**Min_Gnt.** Specifies the necessary length of a burst period device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

Register 8-23. (PCIMLR; 3Fh) PCI Maximum Latency

Bit	Description	Read	Write	Value after Reset
7:0	**Max_Lat.** Specifies how often the device must gain access to the PCI Bus. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

8.3 LOCAL CONFIGURATION REGISTERS

Register 8-24. (LAS0RR; 00h) Local Address Space 0 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 0 maps into PCI Memory space. Value of 1 indicates Local Address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9052 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 0. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	FF0000h
31:28	***Reserved.*** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 8-25. (LAS1RR; 04h) Local Address Space 1 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 1 maps into PCI Memory space. Value of 1 indicates Local Address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9052 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 1. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR3). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 8-26. (LAS2RR; 08h) Local Address Space 2 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 2 maps into PCI Memory space. Value of 1 indicates Local Address Space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9052 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 2. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR4). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 8-27. (LAS3RR; 0Ch) Local Address Space 3 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 3 maps into PCI Memory space. Value of 1 indicates Local Address Space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9052 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 3. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR5). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 8-28. (EROMRR; 10h) Expansion ROM Range

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Enabled only from serial EEPROM. To disable, set the PCI Expansion ROM Address Decode Enable bit to 0 (PCIERBAR[0]=0).	No	Serial EEPROM Only	0
10:1	***Reserved***.	Yes	No	0h
27:11	Specifies PCI Address bits used to decode PCI-to-Local Bus Expansion ROM. Each of the bits corresponds to an Address bit. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCIERBAR). Default is 64 KB; minimum range, if enabled, is 2 KB, and maximum range allowed by *PCI r2.2* is 16 MB. ***Notes:*** *Range **(not** Range register) must be power of 2. "Range register value" is two's complement of range.* *EROMRR should normally be programmed by way of the serial EEPROM to a value of 0h, unless Expansion ROM is present on the Local Bus. If the value is not 0h (default value is 64 KB), system BIOS may attempt to allocate Expansion ROM address space and then access it at the local base address specified in EROMBA (default value is 1 MB) to determine whether the Expansion ROM image is valid. If the image is not valid, as defined in Section 6.3.1.1 (PCI Expansion ROM Header Format) of PCI r2.2, the system BIOS unmaps the Expansion ROM address space it initially allocated, by writing 0h to PCIERBAR[31:0].*	Yes	Yes	11111111111100000
31:28	***Reserved***. (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 8-29. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 0 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 0. Value of 0 disables decoding. ***Note:*** *PCIBAR2 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	Yes	0
3:2	If Local Address Space 0 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 0 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0h

Register 8-30. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 1 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 1. Value of 0 disables decoding. ***Note:*** *PCIBAR3 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	Yes	0
3:2	If Local Address Space 1 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 1 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0h

Register 8-31. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 2 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 2. Value of 0 disables decoding. ***Note:*** *PCIBAR4 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Address Space 2 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 2 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0h

Register 8-32. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 3 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 3. Value of 0 disables decoding. ***Note:*** *PCIBAR5 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Address Space 3 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 3 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0h

Register 8-33. (EROMBA; 24h) Expansion ROM Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
10:0	***Reserved.***	Yes	No	0h
27:11	**Remap PCI Expansion ROM Space into Local Address Space.** Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. Default base is 1 MB. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	00000001000000000
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0h

Register 8-34. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# Input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (LAS0BRD[5:3]=100b).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). (Wait states between consecutive bus requests. NXDA wait states are only inserted after the last Data transfer of a Direct Slave access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Note: *In ISA Interface mode (MODE=0, INTCSR[12]=1), bits [23, 21:6, 2, 0] must be 0, and bit 1 must be 1.*

Register 8-35. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (LAS1BRD[5:3]=100b).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). (Wait states between consecutive bus requests. NXDA wait states are only inserted after the last Data transfer of a Direct Slave access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay. N**umber of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Note: *In ISA Interface mode (MODE=0, INTCSR[12]=1), bits [23, 21:6, 4:2, 0] must be 0, and bits [5, 1] must be 1.*

Register 8-36. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (LAS2BRD[5:3]=100b).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). (Wait states between consecutive bus requests. NXDA wait states are only inserted after the last Data transfer of a Direct Slave access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 8-37. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (LAS3BRD[5:3]=100b).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). (Wait states between consecutive bus requests. NXDA wait states are only inserted after the last Data transfer of a Direct Slave access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe Is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 8-38. (EROMBRD; 38h) Expansion ROM Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count (bits [4:3]) are not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (EROMBRD[5:3]=100b).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). (Wait states between consecutive bus requests. NXDA wait states are only inserted after the last Data transfer of a Direct Slave access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

8.3.1 Chip Select Registers

Register 8-39. (CS0BASE; 3Ch) Chip Select 0 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 0 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 0.** Write zeros (0) in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Notes: *Chip Select 0 (CS0#) is available in non-ISA Interface mode only (INTCSR[12]=0). In ISA Interface mode (INTCSR[12]=1), pin 130 is the ISA MEMRD# signal, and CS0BASE must be programmed to match valid LAS0RR and LAS0BA register configuration for Local Address Space 0.*

For a chip select to assert, the address must be encompassed within a Local Address Space.

Register 8-40. (CS1BASE; 40h) Chip Select 1 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 1.** Write zeros (0) in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Notes: *Chip Select 1 (CS1#) is available in non-ISA Interface mode only (INTCSR[12]=0). In ISA Interface mode (INTCSR[12]=1), pin 131 is the ISA MEMWR# signal, and CS1BASE must be programmed to match valid LAS1RR and LAS1BA register configuration for Local Address Space 1.*

For a chip select to assert, the address must be encompassed within a Local Address Space.

Register 8-41. (CS2BASE; 44h) Chip Select 2 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 2.** Write zeros (0) in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define the base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Notes: *Chip Select 2 (CS2#) functionality of the USER2/CS2# multiplexed pin is enabled by configuring CNTRL[6] from the default value of 0 (USER2) to 1.*

For a chip select to assert, the address must be encompassed within a Local Address Space.

Register 8-42. (CS3BASE; 48h) Chip Select 3 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 3 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 3.** Write zeros (0) in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Notes: *Chip Select 3 (CS3#) functionality of the USER3/CS3# multiplexed pin is enabled by configuring CNTRL[9] from the default value of 0 (USER3) to 1.*

For a chip select to assert, the address must be encompassed within a Local Address Space.

8.3.2 Control Registers

Register 8-43. (INTCSR; 4Ch) Interrupt Control/Status

Bit	Description	Read	Write	Value after Reset
0	**LINTi1 Enable.** Value of 1 indicates LINTi1 is enabled. Value of 0 indicates LINTi1 is disabled.	Yes	Yes	0
1	**LINTi1 Polarity.** Value of 1 indicates LINTi1 is active high. Value of 0 indicates LINTi1 is active low.	Yes	Yes	0
2	**LINTi1 Status.** Value of 1 indicates LINTi1 is active. Value of 0 indicates LINTi1 is not active.	Yes	No	0
3	**LINTi2 Enable.** Value of 1 indicates LINTi2 is enabled. Value of 0 indicates LINTi2 is disabled.	Yes	Yes	0
4	**LINTi2 Polarity.** Value of 1 indicates LINTi2 is active high. Value of 0 indicates LINTi2 is active low.	Yes	Yes	0
5	**LINTi2 Status.** Value of 1 indicates LINTi2 is active. Value of 0 indicates LINTi2 is not active.	Yes	No	0
6	**PCI Interrupt Enable.** Value of 1 enables PCI interrupt.	Yes	Yes	0
7	**Software Interrupt.** Value of 1 generates PCI interrupt (INTA# output asserted) if the PCI Interrupt Enable bit is set (INTCSR[6]=1).	Yes	Yes	0
8	**LINTi1 Select Enable.** Value of 1 indicates enabled Edge Triggerable interrupt. Value of 0 indicates enabled Level Triggerable interrupt. ***Note:*** *Operates only in High-Polarity mode (INTCSR[1]=1).*	Yes	Yes	0
9	**LINTi2 Select Enable.** Value of 1 indicates enabled Edge Triggerable interrupt. Value of 0 indicates enabled Level Triggerable interrupt. ***Note:*** *Operates only in High-Polarity mode (INTCSR[4]=1).*	Yes	Yes	0
10	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears LINTi1.	Yes	Yes	0
11	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears LINTi2.	Yes	Yes	0
12	**ISA Interface Mode Enable.** Writing 1 enables ISA Interface mode. Writing 0 disables ISA Interface mode.	Yes	Serial EEPROM only	0
31:13	***Reserved***.	Yes	No	0

Register 8-44. (CNTRL; 50h) User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control

Bit	Description	Read	Write	Value after Reset
0	**User I/O 0 or WAITO# Pin Select.** Selects the USER0/WAITO# pin function. Value of 1 indicates pin is WAITO#. Value of 0 indicates pin is USER0.	Yes	Yes	0
1	**User I/O 0 Direction.** Value of 0 indicates Input. Value of 1 indicates output. The pin is always an output if the WAITO# function is selected.	Yes	Yes	0
2	**User I/O 0 Data.** If programmed as an output, writing 1 causes the corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
3	**User I/O 1 or LLOCKo# Pin Select.** Selects the USER1/LLOCKo# pin function. Value of 1 indicates pin is LLOCKo#. Value of 0 indicates pin is USER1.	Yes	Yes	0
4	**User I/O 1 Direction.** Value of 0 indicates Input. Value of 1 indicates output. The pin is always an output if the LLOCKo# function is selected.	Yes	Yes	0
5	**User I/O 1 Data.** If programmed as an output, writing 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
6	**User I/O 2 or CS2# Pin Select.** Selects the USER2/CS2# pin function. Value of 1 indicates pin is CS2#. Value of 0 indicates pin is USER2.	Yes	Yes	0
7	**User I/O 2 Direction.** Value of 0 indicates Input. Value of 1 indicates output. The pin is always an output if the CS2# function is selected.	Yes	Yes	0
8	**User I/O 2 Data.** If programmed as an output, writing 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
9	**User I/O 3 or CS3# Pin Select.** Selects the USER3/CS3# pin function. Value of 1 indicates pin is CS3#. Value of 0 indicates pin is USER3.	Yes	Yes	0
10	**User I/O 3 Direction.** Value of 0 indicates Input. Value of 1 indicates output. The pin is always an output if the CS3# function is selected.	Yes	Yes	0
11	**User I/O 3 Data.** If programmed as an output, writing 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
13:12	**PCI Configuration Base Address Register (PCIBAR) Enables.** Values: 00, 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled 01 = PCIBAR0 (Memory) only 10 = PCIBAR1 (I/O) only ***Note:*** *PCIBAR0 and PCIBAR1 should be enabled for the PC platform.*	Yes	Yes	00
14	***PCI r2.1* Features Enable.** When set to 1, the PCI 9052 performs all PCI Read and Write transactions in compliance with *PCI r2.1*. Setting this bit enables Delayed Reads, 32K PCI clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write mode (Retries for writes) (CNTRL[17]) and/or PCI Read with Write Flush mode (CNTRL[15]). Refer to Section 4.2.1.2 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Direct Slave Retry Delay Clocks counter (CNTRL[22:19]) expires, a PCI Retry is issued.	Yes	Yes	0
15	**PCI Read with Write Flush Mode.** When the *PCI r2.1* Features Enable bit is set (CNTRL[14]=1), value of 1 flushes a pending Delayed Read cycle if a Write cycle is detected. Value of 0 (or CNTRL[14]=0) does not affect a pending Delayed Read when a Write cycle occurs.	Yes	Yes	0

Register 8-44. (CNTRL; 50h) User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control (Continued)

Bit	Description	Read	Write	Value after Reset
16	**PCI Read No Flush Mode.** Value of 1 does not flush the Read FIFO if the PCI Read cycle completes (Direct Slave Read Ahead mode). Value of 0 flushes the Read FIFO if a PCI Read cycle completes. Read Ahead mode requires that Prefetch be enabled in the LAS*x*BRD registers (where *x* is the Local Address Space number) for the Memory-Mapped spaces that use Read Ahead mode. The PCI 9052 flushes its Read FIFO for each I/O-Mapped access.	Yes	Yes	0
17	**PCI Read No Write Mode (PCI Retries for Writes).** When the *PCI r2.1* Features Enable bit is set (CNTRL[14]=1), value of 1 forces a PCI Retry on writes if a Delayed Read is pending. Value of 0 (or CNTRL[14] =0) allows writes to occur while a Delayed Read is pending.	Yes	Yes	0
18	**PCI Write Release Bus Mode Enable.** Value of 1 disconnects if the Write FIFO becomes full. Value of 0 de-asserts TRDY# until space is available in the Write FIFO (PCI Write Hold Bus mode).	Yes	Yes	0
22:19	**PCI Direct Slave Retry Delay Clocks.** Number of PCI clocks (multiplied by 8) from the beginning of a Direct Slave access, after which a PCI Retry is issued if the transfer has not completed. Valid for Read cycles only if CNTRL[14]=0. Valid for Write cycles only if CNTRL[18]=0.	Yes	Yes	4h
23	**Direct Slave LOCK# Enable.** Value of 1 enables PCI Direct Slave locked sequences. Value of 0 disables Direct Slave locked sequences.	Yes	Yes	0
24	**Serial EEPROM Clock for PCI Bus Reads or Writes to Serial EEPROM.** Toggling this bit generates a serial EEPROM clock. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)	Yes	Yes	0
25	**Serial EEPROM Chip Select.** For PCI Bus reads or writes to serial EEPROM, setting this bit to 1 provides the serial EEPROM Chip Select.	Yes	Yes	0
26	**Write Bit to Serial EEPROM.** For writes, this output bit is the input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock.	Yes	Yes	0
27	**Read Serial EEPROM Data Bit.** For reads, this input bit is the serial EEPROM output. Clocked out of the serial EEPROM by the serial EEPROM clock.	Yes	No	—
28	**Serial EEPROM Present.** Value of 1 indicates a blank or programmed serial EEPROM is present.	Yes	No	0
29	**Reload Configuration Registers.** When set to 0, writing 1 causes the PCI 9052 to reload the Local Configuration registers from serial EEPROM.	Yes	Yes	0
30	**PCI Adapter Software Reset.** Value of 1 resets the PCI 9052 and issues a reset to the Local Bus. The PCI 9052 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI and Local Configuration registers are not reset. The PCI Interface is not reset. ***Note:*** *If Direct Slave Read Ahead mode is enabled (CNTRL[16]=1), disable it prior to a software reset, or if following a software reset, perform a Direct Slave read of any valid Local Bus address, except the next sequential Lword referenced from the last Direct Slave read, to flush the Direct Slave Read FIFO.*	Yes	Yes	0
31	**Mask Revision.**	Yes	No	0

9 PIN DESCRIPTIONS

9.1 PIN SUMMARY

Table 9-5 through Table 9-8 describe the pins common to all Bus modes:

- Power and Ground
- Serial EEPROM Interface
- PCI System Bus Interface
- Local Bus Support

Table 9-9 and Table 9-10 describe the Local Bus Data Transfer pins.

Unspecified pins are No Connects (NC).

For a visual view of the pinout, refer to Section 11.

The following table lists abbreviations used in this section to represent pin types.

Table 9-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output
I	Input only
O	Output only
TS	Three-state
OD	Open drain
TP	Totem pole
STS	Sustained three-state—driven high for one CLK before float

Note: *Internal resistor values are nominal and may vary widely from published values.*

9.2 PULL-UP/PULL-DOWN RESISTOR RECOMMENDATIONS

Suggested values for external pull-up and pull-down resistors are from 1K to 10K Ohms.

9.2.1 Input Pins (Pin Type I)

This section discusses the pull-up and pull-down resistor requirements for the following Local Bus input pins—BTERM#, EEDO, LCLK, LHOLD, LINTi[2:1], LRDYi#, MODE, TEST, pin 45 [CHRDY in ISA Interface mode (INTCSR[12]=1) or No Connect (NC) in non-ISA Interface mode (INTCSR[12]=0)], and pin 67 (NOWS# in ISA Interface mode or NC in non-ISA Interface mode). (Refer to Table 9-2.)

Table 9-2. Input Pin Pull-Up and Pull-Down Resistor Recommendation Summary

Signal	Recommendations
BTERM#	Internal 80K-Ohm pull-up; if used, add external pull-up
CHRDY/NC	None internal, pull or tie high
EEDO	Pull-up required, if no EEPROM or blank serial EEPROM is present
LCLK	50-Ohm series resistor from BCLKO
LHOLD	None internal, drive or tie low
LINTi[2:1]	None internal, pull to inactive state
LRDYi#	Internal 80K-Ohm pull-up; if used, add external pull-up
MODE	None internal, tie high or low
NOWS#/NC	Internal 80K-Ohm pull-up
TEST	Internal 50K-Ohm pull-down

The Local Bus TEST input internally connects to ground through a 50K-Ohm pull-down resistor. The internal pull-down resistor on the TEST input pin selects normal logic operation. Tie TEST to ground for normal operation.

The BTERM#, LRDYi#, and NOWS# Local Bus input pins internally connect to V_{CC} through an 80K-Ohm pull-up resistor:

- If using the BTERM# and LRDYi# inputs, external pull-up resistors are recommended.
- If using the NOWS# input (ISA Interface mode only), an external pull-up resistor is recommended. In non-ISA Interface mode, pin 67 (NC) can be tied high or left open.

The following Local Bus input pins have no internal pull-up/pull-down resistors:

- **EEDO**—Requires an external pull-up resistor if a blank serial EEPROM or no serial EEPROM is used.
- **LHOLD**—Should be pulled or driven low, or tied to ground, to provide Local Bus ownership to the PCI 9052.

- **LINTi[2:1]**—If configured as level-sensitive (default) in INTCSR[9:8], the pin should be connected to a pull-up or pull-down resistor to hold the signal in an inactive state, for the polarity configured in INTCSR[4, 1]. If LINTi[2:1] is configured as edge-triggered, the input is positive edge-triggered, and should be pulled down to an inactive state.
- **MODE**—Should be connected high for Multiplexed mode, or low for Non-Multiplexed and ISA Interface modes.
- **Pin 45 (NC in non-ISA Interface mode or CHRDY in ISA Interface mode)**—Should be connected to an external pull-up resistor. In non-ISA Interface mode, pin 45 should be tied high.

9.2.2 Output Pins (Pin Type O)

This section discusses the pull-up and pull-down resistor requirements for the following output pins—ADS#, ALE (BALE in ISA Interface mode), BLCKO, BLAST#, CS[1:0]# (MEMWR# and MEMRD#, respectively, in ISA Interface mode), EECS, EEDI, EESK, LA[27:2], LBE[3:0]# (SBHE, NC, ISAA1, and ISAA0, respectively, in ISA Interface mode), LHOLDA, LRESET# (LRESET in ISA Interface mode), LW/R#, RD#, and WR#. (Refer to Table 9-3.)

Table 9-3. Output Pin Pull-Up and Pull-Down Resistor Recommendation Summary

Signal	Recommendations
ADS#	None needed if always Local Master
ALE/BALE	
BCLKO	50-Ohm series resistor to LCLK
BLAST#	None needed if always Local Master
CS[1:0]#/ MEMWR#/MEMRD#	None (always driven)
EECS	
EEDI	
EESK	
LA[27:2]	None needed if always Local Master
LBE[3:0]#/ SBHE#/ISAA[1:0]	
LHOLDA	None (always driven)
LRESET#/ LRESET	
LW/R#	None needed if always Local Master
RD#	
WR#	

The PCI 9052 drives Local Bus output signals when it owns the Local Bus, and floats Local Bus output signals (except BCLKO, CS[1:0]#, EECS, EEDI, EESK, LHOLDA, and LRESET#/LRESET) when it does not own the Local Bus. Totem-pole outputs are always driven except during TEST pin assertion. The PCI 9052 Local Bus output pins do not have internal pull-up or pull-down resistors.

Three-state output pins are ADS#, ALE/BALE, BLAST#, CS0#/MEMRD#, CS1#/MEMWR#, LA[27:2], LBE0#/ISAA0, LBE1#/ISAA1, LBE2#, LBE3#/SBHE, LW/R#, RD#, and WR#.

Totem-Pole output pins are BCLKO, EECS, EEDI, EESK, LHOLDA, and LRESET#/LRESET.

9.2.3 I/O Pins (Pin Type I/O)

This section discusses the pull-up and pull-down resistor requirements for the following I/O pins—LAD[31:0], USER0/WAITO# (IORD# in ISA Interface mode), USER1/LLOCKo# (IOWR# in ISA Interface mode), USER2/CS2#, and USER3/CS3#. (Refer to Table 9-3.)

Table 9-4. I/O Pin Pull-Up and Pull-Down Resistor Recommendation Summary

Signal	Recommendations
LAD[31:0]	Pull-downs recommended for unused
USER0/WAITO#/ IORD#	If USER0 input, pull to known state If WAITO#, pull-up if not sole Master If IORD#, pull-up if not sole Master
USER1/LLOCKo#/ IOWR#	If USER1 input, pull to known state If LLOCKo#, pull-up if not sole Master If IOWR#, pull-up if not sole Master
USER2/CS2#	If USER2 input, pull to known state If CS2#, none (always driven)
USER3/CS3#	If USER3 input, pull to known state If CS3#, none (always driven)

The PCI 9052 drives Local Bus I/O signals when it owns the Local Bus. When the PCI 9052 does not own the Local Bus, it floats Local Bus I/O signals except USER0/WAITO#, USER1/LLOCKo#, USER2/CS2#, and USER3/CS3# configured as USER*x* outputs (and except USER2/CS2#, and USER3/CS3# configured as CS2# and CS3# outputs, refer to *PCI 9052 Design Notes #1*). The PCI 9052 Local Bus I/O pins do not have internal pull-up or pull-down resistors.

Pull-Up/Pull-Down Resistor Recommendations

External pull-down resistors are recommended on the LAD[31:0] I/O pins, to keep connected signals in a known state or to keep unconnected inputs from oscillating and using additional power.

External pull-up resistors are recommended on the following I/O pins to keep the output signals in an inactive state during float:

- USER0/WAITO# if configured as WAITO# output
- USER1/LLOCKo# if configured as LLOCKo# output

Note: *Multiplexed pins are configured as inputs at reset. If output functionality is programmed in serial EEPROM, pin configuration occurs when the serial EEPROM contents are loaded following PCI reset.*

If any of the USER[3:0] multiplexed pins are configured as USER inputs (default functionality), they should be pulled to a known state.

9.3 PINOUT

Table 9-5. Power, Ground, and Unused Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
NC	Spare	2	N/A	45, 67	No Connect pin in Non-Multiplexed and Multiplexed modes only. In ISA and Non-Multiplexed/ISA Interface modes, CHRDY is assigned to pin 45, and NOWS# is assigned to pin 67.
TEST	Test	1	I	99	Test pin. Pull high for test or reduced power state. Tie low for normal operation. When TEST is pulled high, all outputs except RD# (pin 126) are placed in high-impedance state. RD# provides a NANDTREE output when TEST is pulled high.
V_{DD}	Power	10	I	1, 10, 27, 41, 50, 66, 81, 103, 121, 146	Power supply pins (5V). Liberal .01 to .1 µF decoupling capacitors should be placed near the PCI 9052.
V_{SS}	Ground	10	I	9, 26, 40, 51, 65, 80, 104, 120, 147, 160	Ground pins.
Total		23			

Table 9-6. Serial EEPROM Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 8 mA	142	Serial EEPROM Chip Select.
EEDI	Serial EEPROM Data In	1	O TP 8 mA	145	Write data to serial EEPROM.
EEDO	Serial EEPROM Data Out	1	I	143	Read data from serial EEPROM.
EESK	Serial Data Clock	1	O TP 8 mA	144	Serial EEPROM clock pin.
Total		4			

Table 9-7. PCI System Bus Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	150-157, 2-8, 11, 23-25, 28-32, 34-39, 42-43	Multiplexed on the same PCI pins. A bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9052 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I PCI	158, 12, 22, 33	Multiplexed on the same PCI pins. During the Address phase of a transaction, defines the bus command. During the Data phase, used as byte enables. For additional information, refer to *PCI r2.1*.
CLK	Clock	1	I	149	Provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	O STS PCI	16	When actively driven, indicates the driving device decoded its address as the current access target.
FRAME#	Cycle Frame	1	I PCI	13	Driven by the current Master to indicate the beginning and duration of an access. Asserted to indicate a bus transaction is beginning. While asserted, Data transfers continue. When de-asserted, the transaction is in the final Data phase.
IDSEL	Initialization Device Select	1	I PCI	159	Chip select used during Configuration Read or Write transactions.
INTA#	Interrupt A	1	O OD PCI	44	Requests an interrupt.
IRDY#	Initiator Ready	1	I PCI	14	Indicates the ability of the initiating agent (Bus Master) to complete the current Data phase of the transaction.
LOCK#	Lock	1	I PCI	18	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS PCI	21	Indicates even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after completion of the current Data phase.
PERR#	Parity Error	1	O STS PCI	19	Indicates only the reporting of data parity errors during all PCI transactions, except during a Special cycle.

Table 9-7. PCI System Bus Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
RST#	Reset	1	I PCI	148	Brings PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	System Error	1	O OD PCI	20	For reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	O STS PCI	17	Indicates the current target is requesting the Master to stop the current transaction.
TRDY#	Target Ready	1	O STS PCI	15	Indicates the ability of the target agent (selected device) to complete the current Data phase of the transaction.
Total		49			

Table 9-8. Local Bus Support Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BCLKO	Buffered Clock Out	1	O TP 24 mA	63	Provides a buffered version of the PCI clock for optional use by the Local Bus. Not in phase with the PCI clock.
CS[1:0]#	Chip Selects 1 and 0	2	O TS 8 mA	131, 130	General purpose chip selects. The base and range of each may be programmed in the configuration registers. In ISA Interface mode (MODE=0 and INTCSR[12]=1), these pins are redefined as the MEMRD# and MEMWR# signals. (Refer to Table 9-11.) ***Note:*** *The PCI 9052 always drives CS[1:0]#. (Refer to PCI 9052 Design Notes #1.)*
LCLK	Local Bus Clock	1	I	135	Local clock (required) up to 40 MHz; may be asynchronous to the PCI clock.
LHOLD	Hold Request	1	I	134	LHOLD is asserted by a Local Bus Master to request Local Bus use. The PCI 9052 can be made master of the Local Bus by pulling LHOLD low (or by grounding LHOLD).
LHOLDA	Hold Acknowledge	1	O TP 8 mA	133	Asserted by the PCI 9052 to grant Local Bus control to a Local Bus Master. When the PCI 9052 needs the Local Bus, it signals a preempt by de-asserting LHOLDA.

Table 9-8. Local Bus Support Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LINTi1	Local Interrupt 1 In	1	I	137	When enabled (INTCSR[0]=1) and asserted, the LINTi1 Status bit sets (INTCSR[2]=1). If the PCI Interrupt Enable bit is also set (INTCSR[6]=1), then INTA# asserts. LINTi1 is programmable for active-low or active-high polarity in INTCSR[1] in the default Level-Sensitive mode (INTCSR[8]=0). Can be optionally configured as a positive edge-triggered interrupt (INTCSR[8, 1, 0]=111b) for ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or LINTi1 is disabled. An edge-triggered interrupt is set and latched by a LINTi1 low-to-high transition, and cleared by setting the LINTi1 Local Edge Triggerable Interrupt Clear bit (INTCSR[10]=1).
LINTi2	Local Interrupt 2 In	1	I	136	When enabled (INTCSR[3]=1) and asserted, the LINTi2 Status bit sets (INTCSR[5]=1). If the PCI Interrupt Enable bit is also set (INTCSR[6]=1), then INTA# asserts. LINTi2 is programmable for active-low or active-high polarity in INTCSR[4] in the default Level-Sensitive mode (INTCSR[9]=0). Can be optionally configured as a positive edge-triggered interrupt (INTCSR[9, 4, 3]=111b) for ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or LINTi2 is disabled. An edge-triggered interrupt is set and latched by a LINTi2 low-to-high transition, and cleared by setting the LINTi2 Local Edge Triggerable Interrupt Clear bit (INTCSR[11]=1).
LRESET#	Local Reset Out	1	O TP 8 mA	132	Asserted when the PCI 9052 is reset, and used to reset devices on the Local Bus. ***Note:*** *LRESET# is inverted (LRESET) when ISA Interface mode is enabled.*
MODE	Bus Mode	1	I	68	Selects the PCI 9052 Bus Operation mode. 0 = Non-Multiplexed mode 1 = Multiplexed mode Must be 0 for ISA Interface mode.
USER0 WAITO#	User I/O 0 WAIT Out	1	I/O TS 8 mA	138	Can be programmed to be a configurable User I/O pin, USER0, or the Local Bus WAIT Output pin, WAITO#. WAITO# is asserted when wait states are caused by the internal wait state generator. Serves as an output to provide ready-out status. Default functionality is USER0 input. In ISA Interface mode (MODE=0 and INTCSR[12]=1), this pin must be configured as USER0 output (CNTRL[1:0]=10b) and is redefined as the IORD# signal. (Refer to Table 9-11.) Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to CNTRL[1:0].

Table 9-8. Local Bus Support Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
USER1 LLOCKo#	User I/O 1 LLOCK Out	1	I/O TS 8 mA	139	Can be programmed to be a configurable User I/O pin, USER1, or the Local Bus LLOCK Output pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the Local Bus to lock resources. Default functionality is USER1 input. In ISA Interface mode (MODE=0 and INTCSR[12]=1), this pin must be configured as USER1 output (CNTRL[4:3]=10b) and is redefined as the IOWR# signal. (Refer to Table 9-11.) Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[4:3] register bits. The PCI 9052 asserts LLOCKo# during the first clock of an atomic operation (address cycle) and de-asserts it a minimum of one clock following the last bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9052 detects PCI FRAME#, with PCI LOCK# de-asserted at the same time.
USER2 CS2#	User I/O 2 Chip Select 2 Out	1	I/O TS 8 mA	140	Can be programmed to be a configurable User I/O pin, USER2, or as the Chip Select 2 Output pin, CS2#. Default functionality is USER2 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[7:6] register bits. ***Note:*** *The PCI 9052 always drives CS2#. (Refer to PCI 9052 Design Notes #1.)*
USER3 CS3#	User I/O 3 Chip Select 3 Out	1	I/O TS 8 mA	141	Can be programmed to be a configurable User I/O pin, USER3, or as the Chip Select 3 Output pin, CS3#. Default functionality is USER3 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[10:9] register bits. ***Note:*** *The PCI 9052 always drives CS3#. (Refer to PCI 9052 Design Notes #1.)*
Total		14			

Table 9-9. Mode-Independent Local Bus Data Transfer Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	123	Indicates valid address and the start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 8 mA	64	Asserted during the Address phase and de-asserted before the Data phase. Pulse width is dependent upon local clock (LCLK) frequency. In ISA mode (MODE=0, INTCSR[12]=1), this pin generates both the BALE signal for Local Address Spaces 0 and 1, and the ALE signal for Spaces 2, 3, and Expansion ROM.
BLAST#	Burst Last	1	O TS 8 mA	124	Signal driven by the current Local Bus Master to indicate the last transfer in a Bus access. BLAST# is not asserted until internal wait states expire.
LRDYi#	Local Ready In	1	I	128	Local ready input indicates Read data is on the Local Bus, or that Write data is accepted. LRDYi# is not sampled until internal wait states expire [WAITO# de-asserted, provided USER0/WAITO# is configured as WAITO# (CNTRL[0]=1)]. LRDYi# is ignored when BTERM# is enabled and asserted.
LW/R#	Write/Read	1	O TS 8 mA	127	Asserted low for reads and high for writes.
RD#	Read Strobe	1	O TS 12 mA	126	General purpose read strobe. The timing is controlled by the current Bus Region Descriptor register. Normally asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. Remains asserted throughout Burst and NRDD wait states.
WR#	Write Strobe	1	O TS 12 mA	125	General purpose write strobe. The timing is controlled by the current Bus Region Descriptor register. Normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. Remains asserted throughout Burst and NWDD wait states. The LAD data bus hold time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].
Total		7			

Table 9-10. Mode-Dependent Local Bus Data Transfer Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If disabled through the PCI 9052 Configuration registers, the PCI 9052 bursts up to four transactions, Lword transfer depends upon the bus width and type. If enabled, the PCI 9052 continues to burst until BTERM# input is asserted. BTERM# is a ready input that breaks up a Burst cycle and causes another Address cycle to occur. BTERM# is not sampled until internal wait states expire. LRDYi# is ignored when BTERM# is enabled and asserted. BTERM# is not sampled until external wait states expire [WAITO# de-asserted, provided USER0/WAITO# is configured as WAITO# (CNTRL[0]=1)].
LA[27:2]	Address Bus	26	O TS 8 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. Increments during bursts indicate successive Data cycles.
LAD[31:0]	Data Bus	32	I/O TS 8 mA	52-62, 69-79, 82-91	During the Data phase, the Bus carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration: • 8-bit = LAD[7:0] • 16-bit = LAD[15:0] • 32-bit = LAD[31:0] **Multiplexed Mode Only**—During the Address phase, the Bus carries the 28-bit physical address (LAD[27:0]).

Table 9-10. Mode-Dependent Local Bus Data Transfer Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LBE[3:0]#	Byte Enables	4	O TS 12 mA	46-49	Byte enables are encoded based on configured bus width. **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle: • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# ***Not Used*** • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA1 and LA0, respectively: • LBE3# ***Not Used*** • LBE2# ***Not Used*** • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0) ***Note:*** *In ISA Interface mode (MODE=0 and INTCSR[12]=1), pins 46 through 49 have dual functionality, providing LBE[3:0]# for Local Address Spaces 2 and 3 and Expansion ROM, while providing ISAA0, ISAA1, and SBHE# signals for Local Address Spaces 0 and 1 (ISA Memory and I/O).*
Total		63			

Table 9-11. ISA Local Bus Data Transfer Pins (Non-Multiplexed Mode)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BALE	Bus Address Latch Enable	1	O TS 8 mA	64	Asserted to indicate that the address and SBHE# signal lines are valid. Asserted on the falling edge of LCLK, and de-asserted on the next rising clock edge. The address and byte enables are valid for a minimum of two clocks prior to BALE de-assertion. BALE is generated for Local Address Spaces 0 and 1 (ISA Memory and I/0, respectively) accesses only. For Local Address Spaces 2, 3, and Expansion ROM, this pin generates the ALE signal.
CHRDY	Channel Ready	1	I	45	Input from the slave device to indicate that additional time (wait states) is required to complete cycle. A standard 16-bit transaction lasts for three clock cycles, but can be extended by de-asserting CHRDY within one clock cycle after MEMRD#, MEMWR#, IORD#, or IOWR# assertion. A standard 8-bit transaction lasts for six clock cycles, but can be extended by de-asserting CHRDY within three clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion.
IORD#	I/O Read	1	O TS 8 mA	138	Command given to an ISA I/O slave device to drive data onto the ISA Interface Data Bus. IORD# asserts on the falling clock edge after BALE de-asserts.
IOWR#	I/O Write	1	O TS 8 mA	139	Command given to an ISA I/O slave device to latch data from the ISA Interface Data Bus. IOWR# asserts on the falling clock edge after BALE de-asserts.
ISAA[1:0]	ISA Address Bus	2	O TS 12 mA	48, 49	The ISA Interface Address bits. Bits [1:0] should be used in conjunction with LA[23:2]. For a 16-bit ISA Interface, ISAA0 is used as an LBE# signal. For an 8-bit ISA Interface, ISAA0 is used as an address bit.
LA[23:2]	Address Bus	22	O TS 8 mA	116-105, 102-100, 98-92	Address Bus carries the upper 22 bits of the 28-bit physical address bus.
LAD[7:0]	Data Bus	8	I/O TS 8 mA	84-91	Bus carries 8-bit data quantities when configured to 8-bit wide. LAD[0] is the least significant bit
LAD[15:0]	Data Bus	16	I/O TS 8 mA	74-79, 82-91	Bus carries 16-bit data quantities when configured to 16-bit wide. LA[15:8] correspond to the high-order byte and LA[7:0] correspond to the low-order byte.

Table 9-11. ISA Local Bus Data Transfer Pins (Non-Multiplexed Mode) (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LRESET	ISA Interface RESET DRV Out	1	O TP 8 mA	132	ISA connector pin B2. Asserted high when the PCI 9052 is reset, and used to reset devices on the Local Bus. At boot time, LRESET is de-asserted during PCI reset, asserts a pulse width of approximately 750 µs, and de-asserts shortly before serial EEPROM initialization completes and PCI BIOS configuration is allowed (time assumes a 33.3 MHz PCI clock effecting a 960 ns serial EEPROM clock period, and INTCSR register loading to enable ISA Interface mode occurs after 780 serial EEPROM clocks). Software reset (CNTRL[30]=1) asserts LRESET until cleared by software.
MEMRD#	Memory Read	1	O TS 8 mA	130	Command given to a memory slave to drive data onto the ISA Interface Data Bus. For 16-bit transactions, MEMRD# asserts on the rising clock edge when BALE de-asserts. For 8-bit transactions, MEMRD# asserts on the falling clock edge after BALE de-asserts. ***Note:*** *The PCI 9052 always drives MEMRD#.*
MEMWR#	Memory Write	1	O TS 8 mA	131	Command given to a memory slave to latch data from the ISA Interface Data Bus. For 16-bit transactions, MEMWR# asserts on the rising clock edge when BALE de-asserts. For 8-bit transactions, MEMWR# asserts on the falling clock edge after BALE de-asserts. ***Note:*** *The PCI 9052 always drives MEMWR#.*

Table 9-11. ISA Local Bus Data Transfer Pins (Non-Multiplexed Mode) (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
NOWS#	No Wait States	1	I	67	Input from the slave device to indicate that current cycle can be shortened after the Slave decodes address and command signals. The NOWS# signal is clocked into an internal register on the falling edge of the clock. The internal state machine then samples the registered version of NOWS# on the next rising edge of the clock. A standard 16-bit memory transaction lasts for three clock cycles, but can be shortened to two clock cycles by asserting both CHRDY and NOWS# within about one-half clock cycle after MEMRD# or MEMWR# assertion (one-half clock period, less command strobe output delay and NOWS# setup time). A standard 16-bit I/O transaction lasts for three clock cycles, but can be shortened to two clock cycles by asserting both CHRDY and NOWS# prior to IORD# or IOWR# assertion at the falling edge of the clock. A standard 8-bit transaction lasts for six clock cycles, but can be shortened to as few as two clock cycles by asserting both CHRDY and NOWS# within two clock cycles after MEMRD#, MEMWR#, IORD#, or IOWR# assertion (number of clock cycles between command strobe assertion and NOWS# assertion, less command strobe output delay and NOWS# setup time). If CHRDY is de-asserted and NOWS# is asserted (*that is*, when both inputs are low) during the same clock, then NOWS# is ignored and wait states are added as a function of CHRDY.
SBHE#	System Byte High Enable	1	O TS 12 mA	46	When asserted, indicates that a byte is transferring onto the Data Bus upper byte lane [15:8].
Total		57			

Note: *In ISA Interface mode (MODE=0 and INTCSR[12]=1), pins 46, 48, and 49 have dual functionality, providing ISAA0, ISAA1, and SBHE# signals for Local Address Spaces 0 and 1 (ISA Memory and I/O), while providing LBE[3:0]# for Local Address Spaces 2 and 3 and Expansion ROM.*

10 ELECTRICAL SPECIFICATIONS

10.1 GENERAL ELECTRICAL SPECIFICATIONS

Table 10-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-65 to +150 °C
Ambient Temperature with Power Applied	-55 to +125 °C
Supply Voltage to Ground	-0.5 to +7.0V
Input Voltage (V_{IN})	V_{SS} -0.5V V_{DD} +0.5V
Output Voltage (V_{OUT})	V_{SS} -0.5V V_{DD} +0.5V
Maximum Package Power Dissipation	0.65W

Note: *Package Power Dissipation derived with assumption that 1.0m/s air flow is available.*

Table 10-2. Operating Ranges

Ambient Temperature	Junction Temperature	Supply Voltage (V_{DD})	Input Voltage (V_{IN})	
			Min	Max
-40 to +85 ºC	115 °C	5V ±5%	V_{SS}	V_{DD}

Table 10-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
C_{IN}	V_{IN} = 2.0V f = 1 MHz	Input	5	pF
C_{OUT}	V_{OUT} = 2.0V f = 1 MHz	Output	10	pF

The following table lists the package thermal resistance ($\Theta_{j\text{-}a}$).

Table 10-4. Package Thermal Resistance

Air Flow			
0m/s	1m/s	2m/s	3m/s
65 °C/W	45 °C/W	34 °C/W	30 °C/W

Table 10-5. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -4.0 mA	2.4	—	V
V_{OL}	Output Low Voltage		I_{OL} = per Tables 9-6 and 9-8 through 9-11	—	0.4	V
V_{IH}	Input High Level	—	—	2.0	—	V
V_{IL}	Input Low Level	—	—	—	0.8	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$, V_{DD} = Max		-10	+10	µA
I_{OZ}	Three-State Output Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$, V_{DD} = Max		-10	+10	µA
I_{CC}	Power Supply Current	V_{DD} = 5.25V, PCLK = LCLK = 33 MHz		—	130	mA

10.2 LOCAL INPUTS

Local Bus Input Setup and Hold Times (Figure 10-1):

- Setup time = 8 ns maximum
- Hold time = 2 ns minimum

Definitions:

- **T_{SETUP}**—Setup time. The time that an input signal is stable before the rising edge of the Local Clock.
- **T_{HOLD}**—Time that an input signal is stable after the rising edge of the Local Clock.

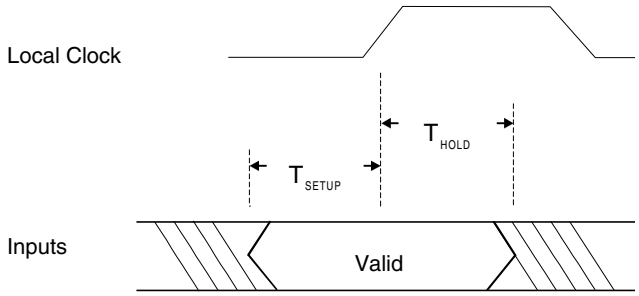


Figure 10-1. PCI 9052 Local Input Setup and Hold Waveform

Table 10-6. Clock Frequencies

Frequency	Min	Max
Local Clock Input	0	40 MHz
PCI Clock Input	0	33 MHz

10.3 LOCAL OUTPUTS

Definition:

- **T_{VALID}**—Output valid (clock-to-out). The time after the rising edge of the Local Clock until the output is stable.

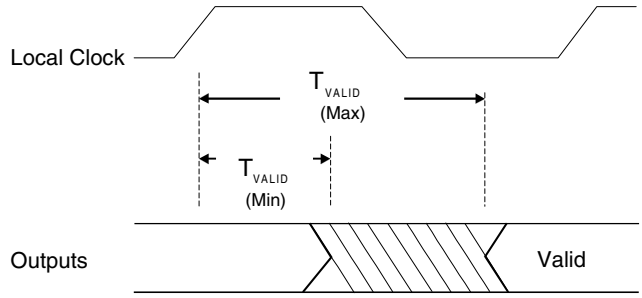


Figure 10-2. PCI 9052 Local Output Delay (Min/Max)

Table 10-7. AC Electrical Characteristics (Local Outputs) Measured over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, V_{CC} = 5.0 ±5%	T_{VALID} (Min) ns (Hold)	T_{VALID} ns Typical Min/Max	T_{VALID} (Max) ns (Worst Case)
ADS#	3	7.4	10
BCLKO	2	7	8
BLAST#	5	9.4	16
CS[3:0]#	4	11	17
LA[27:2]	5	14	18.6
LAD[31:0]	5	14.6	16
LBE[3:0]#	4	8.4	15
LHOLDA	3	—	9
LLOCKo#	—	8	—
LRESET#	5*	14	17*
LW/R#	4	7.8	12
RD#	7	13	16
USER[3:0]	4*	5*	12*
WAITO#	—	9.6	—
WR#	4	9	13

Note: *Values followed with an asterisk (*) are referenced from the PCI Bus.*

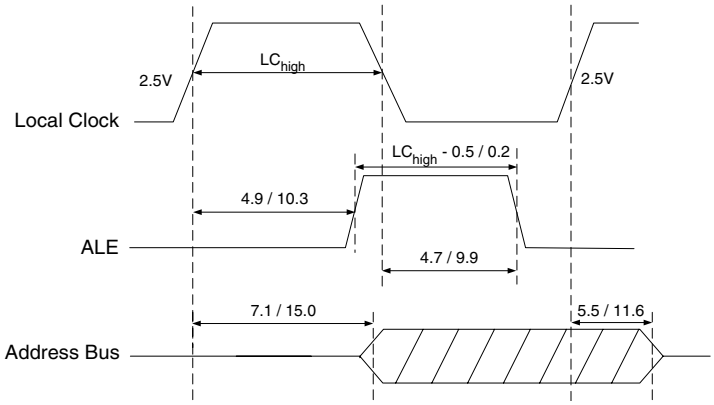


Figure 10-3. PCI 9052 ALE Output Delay (Min/Max) to the Local Clock

Note: *ALE pulse width is dependent upon clock frequency. This timing differs from the PCI 9050 ALE output.*

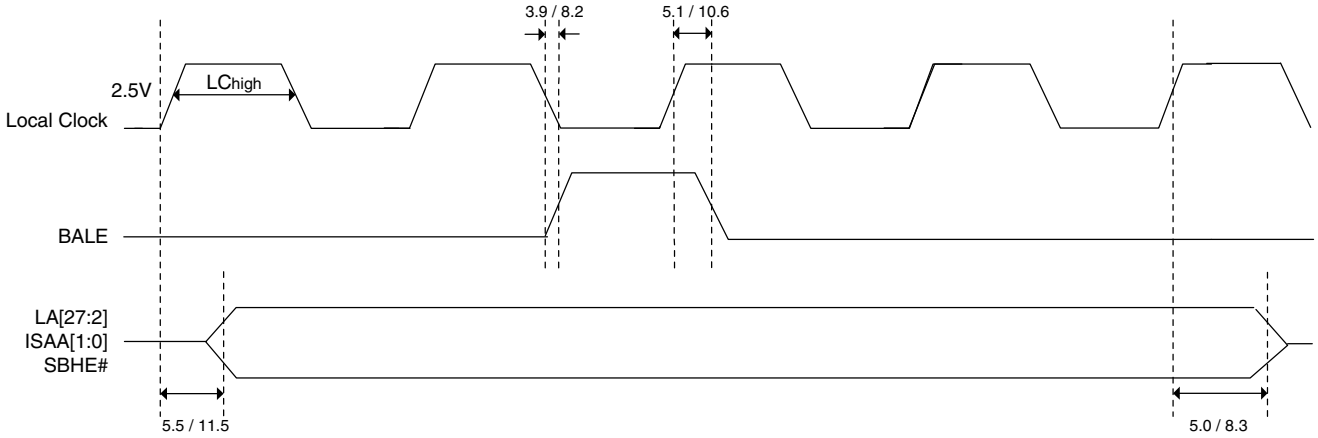


Figure 10-4. PCI 9052 BALE Output Delay (Min/Max) to the Local Clock

Note: *Minimum address setup and hold times are shown. These signals may assert earlier with respect to BALE assertion than shown, and are valid for the entire ISA transaction, which may extend for more clocks than shown.*

11 PHYSICAL SPECIFICATIONS

11.1 MECHANICAL LAYOUT

For 160-pin PQFP

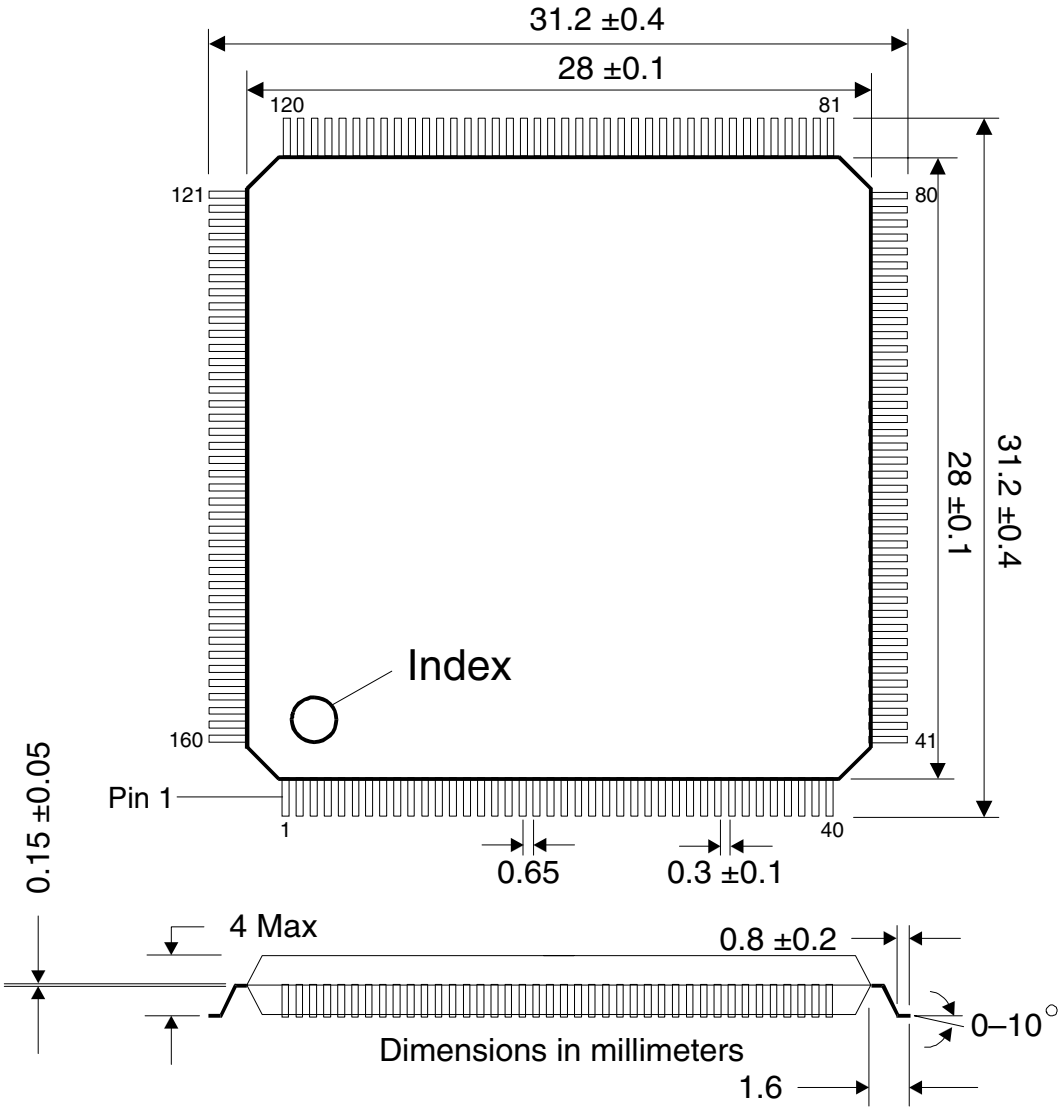


Figure 11-1. Mechanical Dimensions and Package Outline

11.2 TYPICAL ADAPTER BLOCK DIAGRAM

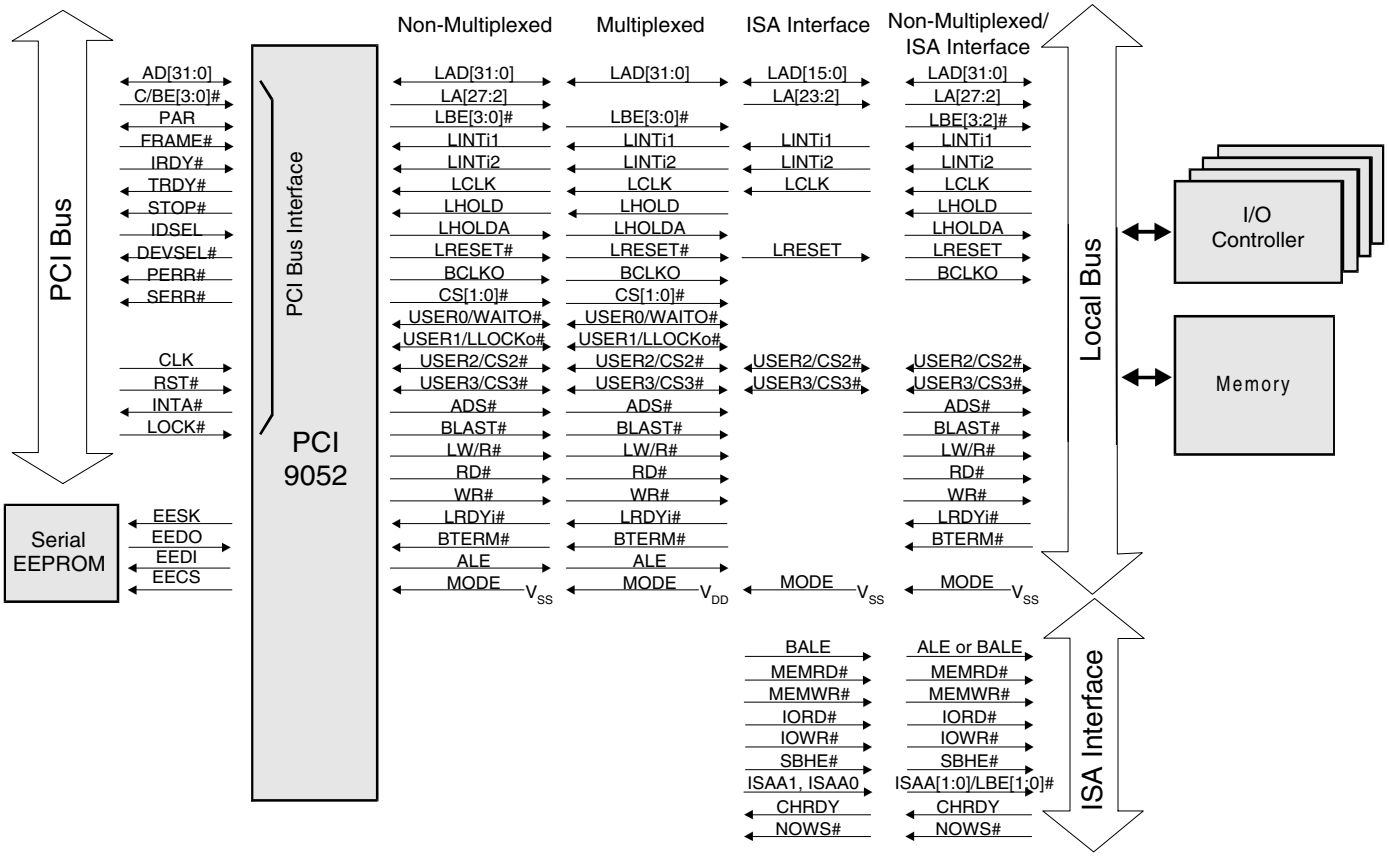


Figure 11-2. PCI 9052 Adapter Block Diagram

Note: *Non-Multiplexed/ISA Interface mode refers to signals for Local Address Spaces 2 and 3 and Expansion ROM with the PCI 9052 in ISA Interface mode (INTCSR[12]=1).*

This page intentionally left blank.

11.3 PIN ASSIGNMENTS

Note: *Refer to Section 9 for pin descriptions.*

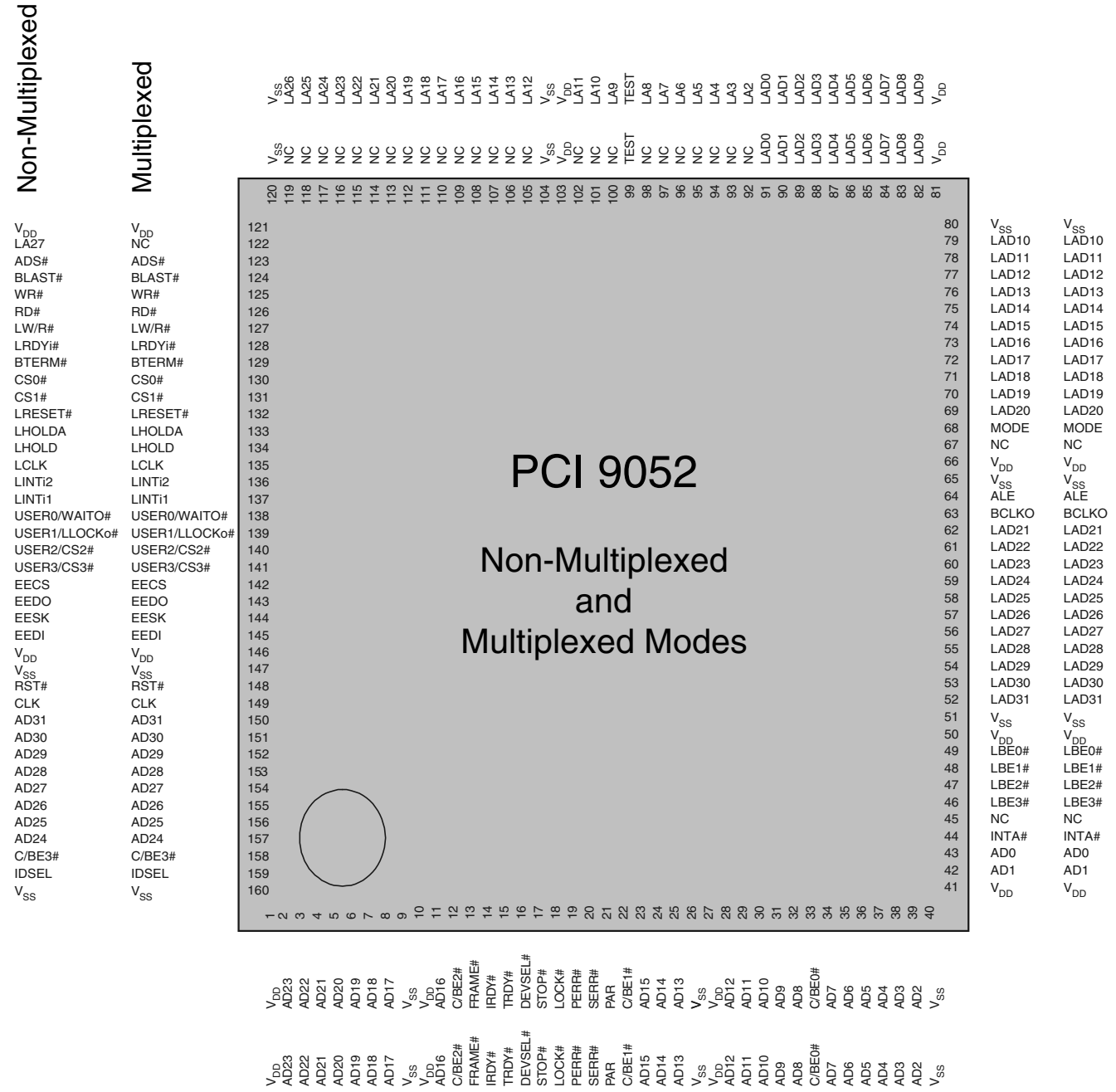


Figure 11-3. Pin Assignments, Non-Multiplexed and Multiplexed Modes

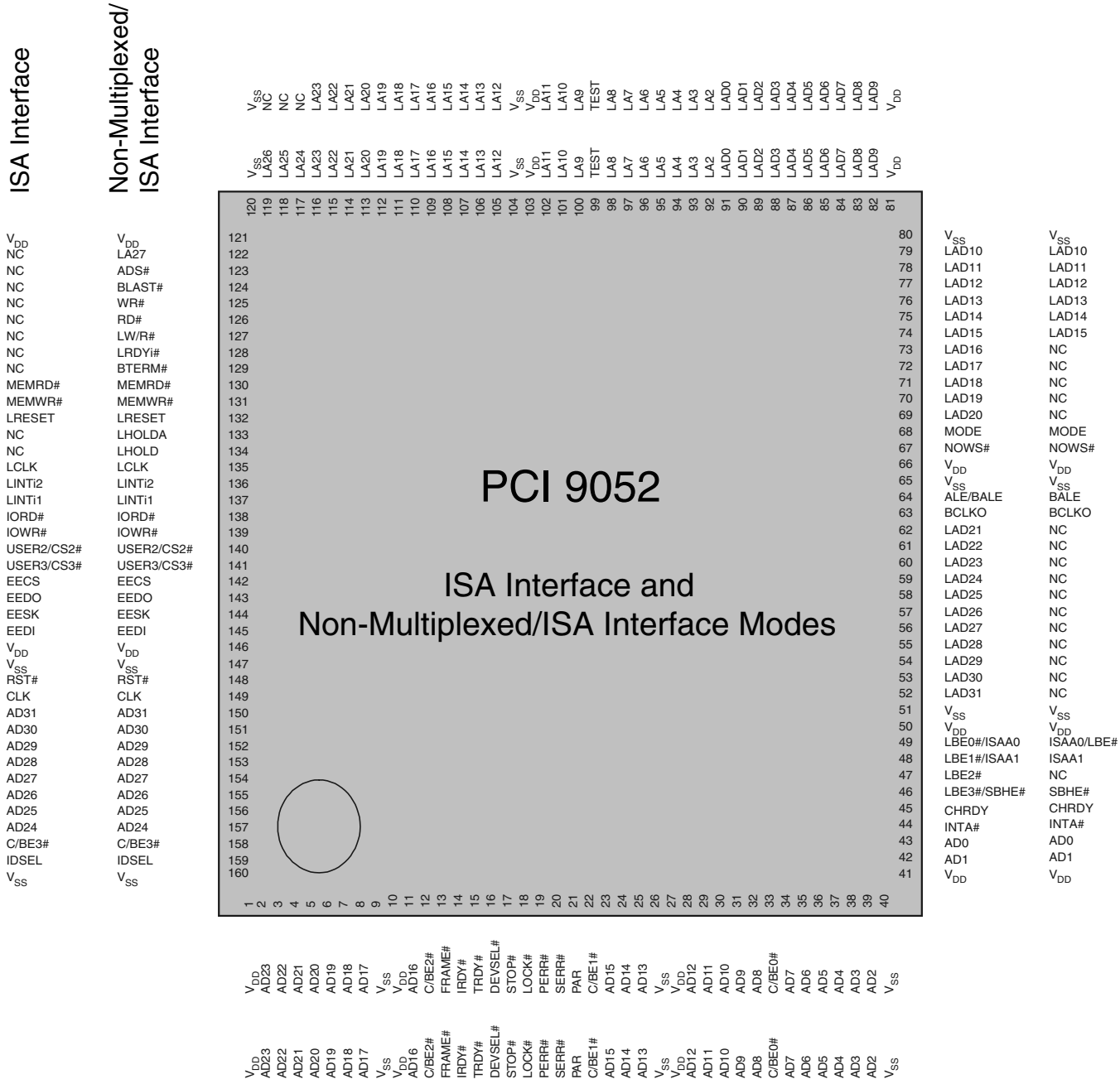


Figure 11-4. Pin Assignments, ISA and Non-Multiplexed/ISA Interface Modes

Notes: *Non-Multiplexed/ISA Interface mode refers to signals for Local Address Spaces 2 and 3 and Expansion ROM with the PCI 9052 in ISA Interface mode (INTCSR[12]=1).*

LRESET is inverted when ISA Interface mode is enabled.

A GENERAL INFORMATION

The PLX PCI 9052 family provides low-cost connectivity for PCI slave designs. It is specifically targeted at easing the transition of existing ISA designs to the more feature-rich and performance-oriented PCI Bus. The PCI 9052 provides Direct Slave PCI functions by interfacing the adapter's I/O circuitry (control, address, and data lines) to a host computer's microprocessor/memory architecture by way of the 32-bit PCI Bus, which typically runs at 33 MHz.

A.1 ORDERING INSTRUCTIONS

Continuing its drive to provide single-chip PCI interfaces for every market, PLX offers to designers its PCI 9052 PCI Bus Target Chip with Glueless ISA Interface Logic for Low-Cost Adapters.

Package	Ordering Part Number
160-pin PQFP	PCI 9052

A.2 UNITED STATES AND INTERNATIONAL REPRESENTATIVES, AND DISTRIBUTORS

A list of PLX Technology, Inc., representatives and distributors can be found at http://www.plxtech.com.

A.3 TECHNICAL SUPPORT

PLX Technology, Inc., technical support information is listed at http://www.plxtech.com; or call 408 774-9060 or 800 759-3735.

Index

A

Abort, Target 2-1, 8-4
AC electrical characteristics 10-3
accelerator, I/O 1-1
accesses
address decode enable 8-9
burst 2-3, 2-10, 4-1, 4-3
byte 2-1, 8-3
decode 4-4, 8-11
Direct Slave 2-1, 2-2, 4-1, 4-4, 4-5, 4-6, 8-15, 8-16
I/O 2-1, 4-1, 4-3, 8-3, 8-6
Local Bus 2-7, 2-10, 4-3
locked atomic operations 4-1
Lword 2-1, 8-3
Max_Lat 8-10
memory 2-8, 3-4, 3-5
memory base address 8-6–8-8
partial Lword 2-9
PCI 4-1, 8-11, 8-26
PCI base address registers 8-6–8-8
read 2-10, 4-3
word 2-1, 8-3
write 2-10
AD[31:0] 2-1, 9-5, 11-4, 11-5
adapter block diagram 11-2
address
base registers 4-1
bits for decoding 4-4
boundary 2-9
burst start 2-9
chip select registers 8-2, 8-22
cycle 2-8, 2-9, 4-3
decode 4-4, 6-1, 8-9, 8-14, 8-15, 8-16
detected 7-2
Direct Slave 4-4, 4-6
EROMBA 8-2, 8-16
invariance 2-1, 2-10
local bits 2-2
Local Bus
data transfer pins 9-9–9-12
initialization 4-4
local chip selects 6-1–6-2
local space registers 5-1, 5-2, 5-4, 5-5, 8-2, 8-11–8-20
local spaces 1-7, 2-10
mapping 4-4
PCI base address registers 8-6–8-8
PCI system bus interface pins 9-5
Read Ahead mode, Direct Slave 4-2
register 1-7
register mapping 8-1–8-2
serial EEPROM register load sequence 3-2–3-4
spaces 1-1, 1-2, 2-2, 2-4, 4-4
strobe 9-9
translation 4-1
Address/Data 2-3
ADS# 2-3, 2-4, 2-8, 4-2, 9-9, 10-3, 11-4, 11-5
ALE 2-3, 2-4, 4-2, 5-1, 5-2, 9-2, 9-9, 10-4, 11-4, 11-5
arbitration, Local Bus 2-3, 2-5, 2-12, 4-8
atomic operations
LLOCKo# 2-4, 9-8
LOCK# 4-1, 9-5, 11-4

B

back-to-back, fast 8-3, 8-4
BALE 5-1, 5-2, 5-6, 5-7, 9-2, 9-12, 10-4, 11-5
BCLKO 1-2, 1-3, 1-5, 9-2, 9-6, 10-3, 11-4, 11-5
Big/Little Endian
See Endian, Big/Little
BIOS 2-1, 3-4, 3-5, 5-1, 5-2, 5-5, 7-1, 7-2, 8-14
BIST 8-1, 8-5
BLAST# 2-3, 2-8, 4-7, 9-9, 10-3, 11-4, 11-5
block diagrams 1-3
adapter 11-2
Local Bus 2-2
BTERM# 2-3, 2-7, 2-8, 4-22, 4-28, 4-29, 4-30, 5-5, 8-17, 8-18, 8-19, 8-20, 8-21, 9-10, 11-4, 11-5
built-in self test (BIST) 8-1, 8-5
burst
access 4-1, 4-3
last 9-9
Min_Gnt 8-10
mode and continuous burst mode (Bterm) 2-8–2-10
PCI read 4-1
read or write 9-5
terminate 9-10
Bus operation 2-1–2-12
bus region descriptors 4-4, 4-5
registers 2-4, 8-2, 8-7, 8-8, 8-17–8-21, 9-9
bus states 2-3
byte enables
C/BE[3:0]# 2-1, 8-17, 8-18, 8-19, 8-20, 8-21, 9-5, 11-4, 11-5
Direct Slave 4-6, 4-6–4-7
LBE[3:0]# 1-2, 1-3, 2-3, 2-4, 9-11

byte merging
2-1–2-2
byte swapping 8-19
See Endian, Big/Little, byte ordering and lane mode

C

C/BE[3:0]# 2-1, 4-2, 8-17, 8-18, 8-19, 8-20, 8-21, 9-5, 11-4, 11-5
cache line size, PCI 1-2, 3-4, 8-1, 8-5
capacitance 10-1
chip select
base address registers 6-1–6-3
IDSEL 9-5, 11-4
initialization device 9-5, 11-4
local 1-1, 1-2, 6-1–6-3
Local Bus support pins 9-6–9-8
procedure to use base address registers 6-2–6-3
registers 5-3, 5-4, 8-2, 8-22, 8-23
serial EEPROM 3-3, 8-26, 9-4
timing diagram 4-16, 6-3
CHRDY 1-3, 1-5, 5-1, 5-2, 5-6, 5-6–5-7, 9-1, 9-4, 9-12, 11-5
CIS 8-1, 8-9
CLK 9-1, 9-5, 11-4, 11-5
clocks
16- and 8-clock rules 4-2, 8-25
32000 PCI timeout 4-2
BCLKO 1-2, 1-3, 1-5, 9-2
buffered PCI 1-7
Bus access 9-9
CLK (PCI) 9-5
delay 8-26
Direct Slave Retry delay 4-3, 4-7, 8-26
EESK 3-1, 9-4
frequencies 10-2
LCLK 1-2, 1-3, 1-5, 2-3, 9-2, 9-6
local 2-3, 4-2, 7-2, 9-6, 10-2, 10-3, 10-4
PCI 1-2, 1-3, 1-5, 1-7, 3-1, 3-6, 4-2, 4-9, 7-2, 8-25, 8-26, 9-2, 9-6, 10-2
PCIMGR 8-10
serial data 9-4
serial EEPROM 3-1, 3-2, 5-2, 8-26, 9-4
TTL 1-2, 1-3, 1-5, 9-2
CMOS, low-power 1-2
CNTRL 1-7, 5-2, 5-4, 5-5, 7-2, 8-2, 8-25–8-26
command codes, Direct Slave 2-1
CompactPCI, Hot Swap capable 1-7
configuration
BTERM# 9-10
bus width 1-2, 1-3, 1-5, 9-2, 9-11
command type 2-1
Endian, Big/Little 4-3
ID 8-3
IDSEL 9-5, 11-4
initialization from serial EEPROM timing diagram 3-6
read and write 9-5, 11-4
registers 4-1, 9-10
timing diagrams, initialization 4-9–4-16
wait state counter 2-7
Continuous Burst mode 2-8–2-9
Control/Status 2-4
conversion, Big/Little Endian 1-7, 4-3
counter
prefetch 1-7, 4-1
wait state 2-7
CPU, Host 2-5
CS[1:0]# 1-3, 1-5, 5-1, 5-2, 5-4, 9-2, 9-6, 11-4
CS[3:0]# 5-6, 10-3
CS0BASE 5-3, 5-4, 8-2, 8-22
CS1BASE 5-4, 8-2, 8-22
CS2# 1-3, 1-6, 5-2, 7-2, 8-25, 9-2, 9-8, 11-4, 11-5
CS2BASE 5-4, 8-2, 8-23
CS3# 5-2, 7-2, 8-25, 9-8, 11-4, 11-5
CS3BASE 5-4, 8-2, 8-23

D

Data Transfer mode 1-1, 4-1–4-6
decode
accesses 4-4
address 4-4, 8-15, 8-16
address enable 8-9
memory 8-12, 8-13
Delayed Read mode, Direct Slave 1-2, 1-7, 2-10, 4-2, 8-25
descriptors, bus region 2-4, 4-4, 8-2, 8-7, 8-8, 8-17–8-21, 9-9
Design Notes, PCI 9052 1-4, 3-1, 9-2, 9-6, 9-8
device
add-in board 8-9
bridge 8-4
chip select control provided 6-1
configuration header 3-4
ID 3-1, 3-3, 3-4, 8-1, 8-3
initialization select 9-5
Local Bus 2-2, 9-7
Master 2-4
non-PCI 2-2
other bridge 8-4
PCI 9-5
ROM 4-1
Slave 2-4
SRAM 6-2

DEVSEL#
8-4, 9-5, 11-4, 11-5
Direct Master, not supported 2-5
Direct Slave
accesses, 8- or 16-bit Local Bus 2-2
BTERM# input 2-8
byte enables 4-6–4-7
CNTRL register 8-2, 8-25–8-26
command codes 2-1
Delayed Read mode 1-7, 4-2, 8-25
Direct Data Transfer mode 4-1–4-4
Endian, Big/Little 2-10
FIFO 4-7, 8-25
Lword accesses 2-9
operation 4-1–4-42
PCI-to-Local address 4-4
Read Ahead mode 1-2, 2-10, 3-1, 4-1, 4-1–4-3, 4-34, 5-1, 5-4, 8-26
single read, timing diagrams 4-18, 4-19, 4-38
single write, timing diagrams 4-17, 4-37
space enable in local address space registers 8-15, 8-16
wait states 2-7
disconnect
Direct Slave I/O accesses, after transfer 4-1
PCI Bus 3-5, 4-3
TRDY# 4-7
drivers
bus 1-2
SERR# 8-3

E

EECS 1-3, 1-5, 3-2, 9-2, 9-4, 11-4, 11-5
EEDI 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
EEDO 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
EESK 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
electrical specifications 10-1–10-4
Endian, Big
byte ordering and lane mode 8-19
Endian, Big, timing diagrams 4-37–4-42
Endian, Big/Little 2-10–2-11
byte ordering and lane mode 8-17–8-21
byte swapping 1-2
conversion 1-7, 4-3
ISA requirements 5-5
Endian, Little (as a PCI Bus) 2-1
EROMBA 8-2, 8-16
EROMBRD 8-2, 8-21
EROMRR 8-2, 8-14
Errata, PCI 9052 1-4, 3-4, 8-9
Expansion ROM 8-2, 8-14, 8-16, 8-21
PCI-to-Local 3-3
spaces 2-2, 2-10, 3-3, 3-5, 4-1, 4-3, 4-4, 4-6, 8-1, 8-9, 8-16

F

fast back-to-back 8-3, 8-4
FIFOs
bi-directional 1-1
Continuous Burst mode 2-9
Direct Slave 4-1, 4-2, 4-3, 8-25
Read Ahead mode 3-1, 8-26
number of 1-7
response to 4-7
FM93C46L 3-2
FM93CS56 3-2
FRAME# 9-5, 11-4, 11-5
frequencies 10-2
functional description 3-1–4-42

G

generator
internal wait states 2-3
interrupts 1-2
programmable wait state 4-1, 9-10

H

header
format 8-14
PCI Expansion ROM format 8-14
PCI type 3-4, 8-5
High-Polarity mode 8-24
hold and setup waveform, local input 10-2
Host CPU 2-5
Hot Swap capable, CompactPCI 1-7

I

I/O 2-1
access 4-1, 4-3, 8-6
base address 8-6
devices 5-6
ISA space 5-2, 5-4, 5-5
mapped configuration registers 8-1
pin type 9-5
space access 8-3, 8-6, 8-7, 8-8, 8-11, 8-13, 8-15, 8-16
user 7-1
i960J function, not supported 2-9
ID
device and vendor 1-2, 1-7, 3-2, 3-3, 3-4, 8-1, 8-3
revision 3-4, 8-1, 8-4
subsystem 3-3, 8-1, 8-9

IDSEL
9-5, 11-4, 11-5
initialization
configuration timing diagrams 4-9–4-16
control register 8-2, 8-25–8-26
Direct Slave example 4-6
Direct Slave initialization 4-4
functional description 3-1
IDSEL 9-5, 11-4
Local Bus Direct Slave 4-4
PCI 4-6
reset 4-4
serial EEPROM timing diagram, from 3-6, 4-9
INTA# 4-12, 7-1, 7-2, 7-3, 8-10, 9-5, 11-4, 11-5
INTCSR 5-1, 5-2, 5-4, 7-2, 8-24, 9-13
internal wait states 2-3, 2-4, 2-7, 2-8, 2-10, 4-19–4-24, 4-27–4-33, 4-38–4-42, 5-5, 8-17–8-21, 9-9
Interrupt Request
See IRQ
interrupts 7-1–7-6
control/status 3-4
generator 1-2
INTA# 9-5
ISA requirements 5-5
local 4-13, 7-4, 9-7
pin 3-3
registers 3-5, 8-1, 8-2, 8-10, 8-24
request 4-12, 7-3, 8-10, 9-5, 11-4
timing diagrams 7-3–7-6
IORD# 5-2, 5-4, 5-6, 5-6–5-7, 9-12, 11-5
IOWR# 5-2, 5-4, 5-6, 5-6–5-7, 9-12, 11-5
IRDY# 2-1, 9-5, 11-4, 11-5
IRQ 7-1, 7-2
ISA Interface mode 1-2, 1-3, 1-5, 1-7, 4-6, 5-1–5-14, 9-2, 9-11
designs A-1
INTA# trigger 7-1, 7-2
Local Bus data transfer pins 9-12
logic configuration 6-1
LRESET inverted 9-7
pin assignments 9-6, 11-5
timing diagrams 5-8–5-14
ISA memory cards, 8-bit 5-2
ISAA[1:0] 5-1, 9-12, 11-5

L

LA[23:2] 9-12, 11-5
LA[27:2] 1-2, 1-3, 2-2, 2-3, 5-1, 9-10, 10-3, 11-4, 11-5
LAD[15:0] 9-12, 11-5
LAD[31:0] 1-2, 1-3, 2-3, 2-10, 4-6, 5-1, 9-10, 10-3, 11-4, 11-5
LAD[7:0] 9-12, 11-5
LAS0BA 5-1, 5-4, 8-2, 8-15
LAS0BRD 5-3, 5-4, 5-5, 5-7, 8-2, 8-17
LAS0RR 5-3, 5-4, 8-2, 8-11
LAS1BA 5-1, 5-4, 8-2, 8-15
LAS1BRD 5-3, 5-4, 5-5, 5-7, 8-2, 8-18
LAS1RR 5-3, 5-4, 8-2, 8-12
LAS2BA 8-2, 8-16
LAS2BRD 5-7, 8-2, 8-19
LAS2RR 8-2, 8-13
LAS3BA 8-2, 8-16
LAS3BRD 8-2, 8-20
LAS3RR 8-2, 8-14
latency timer, PCI not supported 8-1, 8-5
LBE[3:0]# 1-2, 1-3, 1-5, 2-4, 4-2, 4-6, 9-2, 9-11, 10-3, 11-4, 11-5
LCLK 1-2, 1-3, 1-5, 2-3, 9-2, 9-6, 10-2, 11-4, 11-5
Level-Sensitive mode 7-1, 7-2, 9-7
LHOLD 1-5, 2-5, 9-1, 9-6, 11-4, 11-5
LHOLDA 1-5, 2-5, 9-1, 9-6, 10-3, 11-4, 11-5
LINTi1 1-5, 4-12, 7-2, 7-3, 9-1, 9-7, 11-4, 11-5
LINTi2 1-5, 4-12, 7-2, 7-3, 9-1, 9-7, 11-4, 11-5
LLOCKo# 1-3, 1-6, 1-7, 2-4, 5-1, 5-2, 7-2, 8-25, 9-2, 9-8, 10-3, 11-4
local
clocks 7-2, 9-6, 10-2, 10-3
input setup figure 10-2
interrupts 7-1
signal output delay 10-3
Local Address
bits LA[1:0] 2-2, 2-9, 4-6, 9-11
Direct Slave example 4-6
EROMBA 8-2, 8-16
mapping 4-4
PCI base address registers 8-7–8-8
space registers 5-1, 5-2, 5-3, 5-4, 5-5, 5-7, 8-2, 8-11–8-20
spaces 1-7, 4-1, 8-1
Local Bus
1-1, 1-2, 1-3, 1-5, 1-7, 2-1–2-12, 9-1
arbitration 4-8
characteristics 4-4
control 4-3
data transfer pins 9-9–9-14
Delayed Read mode, Direct Slave 4-2
Direct Slave
access 4-5
operation 4-1
memory map example 6-2
prefetch counter 4-1
Read Ahead mode, Direct Slave 3-1, 4-2, 8-26

region
descriptors 4-4, 8-2, 8-17–8-21, 9-9
registers 8-2, 8-17–8-21
response to FIFO 4-7
support pins 9-6–9-8
timing diagrams, Multiplexed mode 4-37–4-42
timing diagrams, Non-Multiplexed mode 4-17–4-36
width 4-6
local chip selects
See chip select
Local configuration registers 8-11–8-21
address mapping 8-2
lock
cycles 1-7
Direct Slave (atomic operations) 4-1
Direct Slave enable 8-26
LOCK# 4-1, 9-5, 11-4
mechanism and sequences 1-2
LOCK# 4-1, 9-5, 11-4, 11-5
LRDYi# 1-2, 1-3, 1-5, 2-3, 2-4, 2-7, 2-8, 2-10, 4-1, 9-1, 9-9, 11-4, 11-5
LRESET (ISA) 5-1, 5-2, 9-13, 11-5
LRESET# 1-3, 1-6, 3-1, 3-6, 4-9, 5-1, 5-2, 9-2, 9-7, 10-3, 11-4
LW/R# 2-4, 9-9, 11-4, 11-5

M

map
memory 6-2
read accesses 4-3
remap 4-4, 4-6
serial EEPROM memory 3-2
mapping
local registers 4-1
memory, PCI prefetchable 2-1–2-2, 8-7, 8-8
register address 8-1–8-2
registers 8-2, 8-15–8-16
mask revision 8-26
maximum rating 10-1
mechanical layout 11-1
memory
accesses 2-8, 3-4, 3-5, 8-6–8-8
address spaces 8-7–8-13
base address 8-6–8-8
BTERM# 2-8
commands aliased to basic 2-1
decode 8-11, 8-12, 8-13
devices 2-2, 5-6
Direct Slave transfer 4-3
local controller 2-7
map example 6-2
mapped configuration registers 8-1
mapping 8-11, 8-12, 8-13, 8-15, 8-16
mapping, prefetchable 2-1–2-2, 8-7, 8-8
PCI base address registers 8-6–8-8
prefetchable 8-7, 8-8
read 2-1, 4-3
register location 8-6–8-8
remap 8-15, 8-16
serial EEPROM map 3-2
space indicator 8-6–8-14
spaces 8-12–8-16
timing diagrams 4-11
write 2-1, 8-5
MEMRD# 1-3, 1-5, 5-1, 5-2, 5-4, 5-6, 5-6–5-7, 9-2, 9-6, 9-13, 11-5
MEMWR# 1-3, 1-5, 5-1, 5-2, 5-4, 5-6, 5-6–5-7, 9-2, 9-6, 9-13, 11-5
MODE 1-3, 1-6, 2-5, 9-2, 9-7, 11-4, 11-5
Multiplexed mode
Endian, Big/Little 2-10
input pins 9-1–9-2
LAD[31:0] bus 2-3
Local Bus 2-2–2-11
interface and Bus cycles 2-5
programming to 1-1, 1-2
support pins 9-7, 9-10
timing diagrams 4-37–4-42
types 2-5
output pins 9-2
pin assignments 11-4
recovery states 2-3, 2-9
multiplexed pins
I/O 7-2, 9-3, 9-6–9-8
PCI System Bus interface 9-5, 9-6–9-8

N

NANDTREE 9-4
NC (unused pins) 1-3, 1-5, 5-1, 5-2, 9-1, 9-3, 9-4, 11-4, 11-5
networking 1-1
Non-Multiplexed mode
Endian, Big/Little 2-10
ISA requirements 5-1, 5-6
LAD[31:0] bus 2-3
Local Bus 2-2–2-11
ISA Interface mode data transfer pins 9-12–9-14
programming to 1-1, 1-2
support pins 9-7
timing diagrams 4-17–4-36
pin assignments 11-4

NOWS#
1-3, 1-5, 5-3, 5-6–5-7, 9-1, 9-4, 9-14, 11-5
NRAD, NRDD, NWAD, NWDD, and NXDA 2-8, 5-5, 8-17–8-21
See Also internal wait states

O

on-the-fly conversion, Big/Little Endian 4-3
operating ranges 10-1
ordering instructions A-1

P

package mechanical dimensions 11-1
package specs 11-1–11-5
PAR 9-5, 11-4, 11-5
PCI
burst read 4-1, 4-36
cache line size 1-2, 3-4
clock 1-2, 1-3, 1-5, 1-7, 3-1, 3-6, 4-2, 4-9, 7-2, 9-2, 9-6, 10-2
configuration registers 8-3–8-10
address mapping 8-1
Expansion ROM 3-5
header 3-4
industrial implementations 1-1
initialization 4-4
interrupts 3-5, 7-1
Master accesses 4-1
software 4-4
specs *See Preface*
PCI 9030 1-7
PCI 9050 1-4–1-7, 8-4, 10-4
PCI 9052
compatibility with PCI 9050 1-4
Design Notes 1-4, 3-1, 9-2, 9-6, 9-8
product ordering and technical support A-1
PCI 9052RDK 3-3
PCI Bus 2-1–2-2
Direct Slave operation 4-1, 4-3
disconnect 4-3
Latency Timer, not supported 8-1, 8-5
local address spaces 4-4, 4-6
region 4-4, 4-5, 8-7, 8-8
response to FIFO 4-7
system bus interface pins 9-5–9-6
transactions 4-3
V_{CC} 1-7
PCI Initiator, not supported 2-5
PCI Local Bus Specification, Revision 2.1
See PCI r2.1
PCI Local Bus Specification, Revision 2.2
See PCI r2.2
PCI r2.1 **1-1**, **1-2**, **4-36**, **8-25**, **9-5**
PCI r2.2 **1-7**, **2-1**, **3-4**, **4-2**, **8-11**, **8-12**, **8-13**, **8-14**
PCI Target
See Direct Slave
PCIBAR0 8-6
PCIBAR1 8-6
PCIBAR2 5-1, 5-5, 8-7
PCIBAR3 5-1, 5-5, 8-7
PCIBAR4 8-8
PCIBAR5 8-8
PCIBISTR 8-1, 8-5
PCICCR 8-1, 8-4
PCICIS 8-1, 8-9
PCICLSR 3-4, 8-1, 8-5
PCICR 8-1, 8-3
PCIERBAR 3-5, 8-1, 8-9
PCIHTR 3-4, 8-1, 8-5
PCIIDR 8-3
PCIILR 8-1, 8-10
PCIIPR 8-1, 8-10
PCILTR 8-1, 8-5
PCIMGR 8-1, 8-10
PCIMLR 8-1, 8-10
PCIREV 8-4
PCISID 8-9
PCISR 8-1, 8-3, 8-4
PCISVID 8-9
PERR# 9-5, 11-4, 11-5
physical specs 11-1–11-5
pin descriptions 9-1–9-14
pinout 9-4–9-14, 11-4–11-5
pins, ISA Local Bus Data Transfer
BALE 5-1, 5-2, 5-6, 5-7, 9-2, 9-12, 10-4, 11-5
CHRDY 1-3, 1-5, 5-1, 5-2, 5-6, 5-6–5-7, 9-1, 9-4, 9-12, 11-5
IORD# 5-2, 5-4, 5-6, 5-6–5-7, 9-12, 11-5
IOWR# 5-2, 5-4, 5-6, 5-6–5-7, 9-12, 11-5
ISAA[1:0] 5-1, 9-12, 11-5
LA[23:2] 9-12, 11-5
LAD[15:0] 9-12, 11-5
LAD[7:0] 9-12, 11-5
LRESET 5-1, 5-2, 9-13, 11-5
MEMRD# 1-3, 1-5, 5-1, 5-2, 5-4, 5-6, 5-6–5-7, 9-2, 9-6, 9-13, 11-5
MEMWR# 1-3, 1-5, 5-1, 5-2, 5-4, 5-6, 5-6–5-7, 9-2, 9-6, 9-13, 11-5
NOWS# 1-3, 1-5, 5-3, 5-6–5-7, 9-1, 9-4, 9-14, 11-5
SBHE# 5-1, 9-14, 11-5

pins, Local Bus data transfer
ADS# 2-3, 2-4, 2-8, 4-2, 9-9, 10-3, 11-4, 11-5
ALE 2-3, 2-4, 4-2, 5-1, 5-2, 9-2, 9-9, 10-4, 11-4, 11-5
BLAST# 2-3, 2-8, 4-7, 9-9, 10-3, 11-4, 11-5
BTERM# 2-3, 2-7, 2-8, 4-22, 4-28, 4-29, 4-30, 5-5, 8-17, 8-18, 8-19, 8-20, 8-21, 9-10, 11-4, 11-5
LA[27:2] 1-2, 1-3, 2-2, 2-3, 5-1, 9-10, 10-3, 11-4, 11-5
LAD[31:0] 1-2, 1-3, 2-3, 2-10, 4-6, 5-1, 9-10, 10-3, 11-4, 11-5
LBE[3:0]# 1-2, 1-3, 1-5, 2-4, 4-2, 4-6, 9-2, 9-11, 10-3, 11-4, 11-5
LRDYi# 1-2, 1-3, 1-5, 2-3, 2-4, 2-7, 2-8, 2-10, 4-1, 9-1, 9-9, 11-4, 11-5
LW/R# 2-4, 9-9, 11-4, 11-5
RD# 1-2, 1-3, 1-5, 2-4, 5-5, 8-17–8-21, 9-2, 9-4, 9-9, 10-3, 11-4, 11-5
WR# 1-2, 1-3, 1-5, 2-5, 5-5, 8-17–8-21, 9-2, 9-9, 10-3, 11-4, 11-5
pins, Local Bus support
BCLKO 1-2, 1-3, 1-5, 9-2, 9-6, 10-3, 11-4, 11-5
CS[1:0]# 1-3, 1-5, 5-1, 5-2, 5-4, 9-2, 9-6, 11-4
CS[3:0]# 5-6, 10-3
CS2# 1-3, 1-6, 5-2, 7-2, 8-25, 9-2, 9-8, 11-4, 11-5
CS3# 5-2, 7-2, 8-25, 9-8, 11-4, 11-5
LCLK 1-2, 1-3, 1-5, 2-3, 9-2, 9-6, 10-2, 11-4, 11-5
LHOLD 1-5, 2-5, 9-1, 9-6, 11-4, 11-5
LHOLDA 1-5, 2-5, 9-1, 9-6, 10-3, 11-4, 11-5
LINTi1 1-5, 4-12, 7-2, 7-3, 9-1, 9-7, 11-4, 11-5
LINTi2 1-5, 4-12, 7-2, 7-3, 9-1, 9-7, 11-4, 11-5
LLOCKo# 1-3, 1-6, 2-4, 5-1, 5-2, 7-2, 8-25, 9-2, 9-8, 10-3, 11-4
LRESET# 1-3, 1-6, 3-1, 3-6, 4-9, 5-1, 5-2, 9-2, 9-7, 10-3, 11-4
MODE 1-3, 1-6, 2-5, 9-2, 9-7, 11-4, 11-5
USER[3:0] 10-3
USER0 1-3, 1-6, 4-14, 4-15, 5-1, 5-2, 5-4, 5-6, 7-2, 7-5, 7-6, 8-25, 9-2, 9-7, 11-4
USER1 1-3, 1-6, 5-1, 5-2, 5-4, 5-6, 7-2, 8-25, 9-2, 9-8, 11-4
USER2 1-3, 1-6, 7-2, 8-25, 9-2, 9-8, 11-4, 11-5
USER3 7-2, 8-25, 9-8, 11-4, 11-5
WAITO# 1-3, 1-6, 2-4, 5-1, 5-2, 7-2, 8-25, 9-2, 9-7, 10-3, 11-4
pins, PCI System Bus Interface
AD[31:0] 2-1, 9-5, 11-4, 11-5
C/BE[3:0]# 2-1, 4-2, 8-17, 8-18, 8-19, 8-20, 8-21, 9-5, 11-4, 11-5
CLK 9-1, 9-5, 11-4, 11-5
DEVSEL# 8-4, 9-5, 11-4, 11-5
FRAME# 9-5, 11-4, 11-5
IDSEL 9-5, 11-4, 11-5
INTA# 4-12, 7-1, 7-2, 7-3, 8-10, 9-5, 11-4, 11-5
IRDY# 2-1, 9-5, 11-4, 11-5
LOCK# 4-1, 9-5, 11-4, 11-5
PAR 9-5, 11-4, 11-5
PERR# 9-5, 11-4, 11-5
RST# 3-1, 3-6, 4-9, 9-6, 11-4, 11-5
SERR# 7-2, 8-3, 8-4, 9-6, 11-4, 11-5
STOP# 9-6, 11-4, 11-5
TRDY# 2-1, 4-3, 4-7, 8-25, 9-5, 9-6, 11-4, 11-5
pins, Power and Ground
TEST 1-3, 1-5, 9-1, 9-4, 11-4, 11-5
V_{DD} 9-4, 11-4, 11-5
V_{SS} 9-4, 11-4, 11-5
pins, pull-up/pull-down resistor requirements 9-1–9-3
pins, Serial EEPROM Interface
EECS 1-3, 1-5, 3-2, 9-2, 9-4, 11-4, 11-5
EEDI 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
EEDO 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
EESK 1-3, 1-5, 9-2, 9-4, 11-4, 11-5
pins, unused (NC) 9-3, 9-4, 11-4, 11-5
PLX Technology, Inc.
company background 1-1
product ordering and technical support A-1
PLXMon 3-2, 7-2
pointer, CIS 8-1, 8-9
power management, not supported in PCI 9052 1-7
preempt condition 2-5
prefetch
counter 1-2, 1-7, 4-1
Direct Slave 4-1, 4-2
PCI memory mapping 2-1–2-2
reads 8-6, 8-7, 8-8, 8-11, 8-13
timing diagrams 4-24, 4-25, 4-31–4-33
programmable
chip select 6-1
configurations 1-2, 1-3
prefetch counter 1-2, 4-1
registers 4-1, 4-3
wait state generator 9-9
pull-up/pull-down resistor requirements 9-1–9-3

R

ranges, operating 10-1, 10-2
RD# 1-2, 1-3, 1-5, 2-4, 5-5, 8-17–8-21, 9-2, 9-4, 9-9, 10-3, 11-4, 11-5
RDK, PCI 9052 3-3
read
1-7, 2-1, 2-9, 4-1, 4-2, 4-3, 4-4
configuration timing diagram 4-10
Direct Slave 4-7
Read Ahead mode 3-1, 8-26
timing diagrams 4-42

PCI Configuration timing diagram 4-10
PCI Memory timing diagrams 4-11
registers 8-3–8-26
serial EEPROM 3-2
Read Ahead mode, Direct Slave
1-2, 2-10, 3-1, 4-1–4-3, 4-34, 5-1, 5-4, 8-26
read strobe delay 1-2, 2-4, 5-5, 8-17–8-21, 9-9
recovery states 2-3, 2-9
registers
addresses 1-7, 8-1–8-2
chip select 8-2, 8-22
CNTRL 1-7, 5-2, 5-4, 5-5, 7-2, 8-2, 8-25–8-26
CS0BASE 5-3, 5-4, 8-2, 8-22
CS1BASE 5-4, 8-2, 8-22
CS2BASE 5-4, 8-2, 8-23
CS3BASE 5-4, 8-2, 8-23
EROMBA 8-2, 8-16
EROMBRD 8-2, 8-21
EROMRR 8-2, 8-14
INTCSR 5-1, 5-2, 5-4, 7-2, 8-24, 9-13
LAS0BA 5-1, 5-4, 8-2, 8-15
LAS0BRD 5-3, 5-4, 5-5, 5-7, 8-2, 8-17
LAS0RR 5-3, 5-4, 8-2, 8-11
LAS1BA 5-1, 5-4, 8-2, 8-15
LAS1BRD 5-3, 5-4, 5-5, 5-7, 8-2, 8-18
LAS1RR 5-3, 5-4, 8-2, 8-12
LAS2BA 8-2, 8-16
LAS2BRD 5-7, 8-2, 8-19
LAS2RR 8-2, 8-13
LAS3BA 8-2, 8-16
LAS3BRD 8-2, 8-20
LAS3RR 8-2, 8-14
PCIBAR0 8-6
PCIBAR1 8-6
PCIBAR2 5-1, 5-5, 8-7
PCIBAR3 5-1, 5-5, 8-7
PCIBAR4 8-8
PCIBAR5 8-8
PCIBISTR 8-1, 8-5
PCICCR 8-1, 8-4
PCICIS 8-1, 8-9
PCICLSR 3-4, 8-1, 8-5
PCICR 8-1, 8-3
PCIERBAR 3-5, 8-1, 8-9
PCIHTR 3-4, 8-1, 8-5
PCIIDR 8-3
PCIILR 8-1, 8-10
PCIIPR 8-1, 8-10
PCILTR 8-1, 8-5
PCIMGR 8-1, 8-10
PCIMLR 8-1, 8-10
PCIREV 8-4
PCISID 8-9
PCISR 8-1, 8-3, 8-4
PCISVID 8-9
remap
local base address 4-6
PCI-to-Local addresses 4-4
reset
initialization 4-4
software 3-1, 5-2, 8-26, 9-13
timing diagrams 3-6
resistor requirements, pull-up/pull-down 9-1–9-3
Retry delay timer 1-2, 4-3, 8-1
revision
class code 3-3
ID 3-4, 8-1
mask 8-26
PCI ID 8-4
RST# 3-1, 3-6, 4-9, 9-6, 11-4, 11-5

S

SBHE# 5-1, 9-14, 11-5
serial EEPROM 1-2, 1-7
address decode enable 8-14
base class code 8-4
chip select 8-26, 9-4
clocks 5-2, 8-26, 9-4
CNTRL register 8-2, 8-25–8-26
device ID 8-3
functional description 3-1–3-4
interface 9-1, 9-4
internal registers access 2-5
interrupt pin register 8-10
ISA requirements 5-1–5-4
register level programming interface 8-4
subclass code 8-4
subsystem 8-9
timing diagrams 3-6, 4-9–4-16
vendor ID 8-3
write bit to 8-26
SERR# 7-2, 8-3, 8-4, 9-6, 11-4, 11-5
setup and hold waveform, local input 10-2
signal specs 11-1–11-5
signaling, Local and PCI buses 1-7
Single Cycle mode
2-8

single cycle read and write
2-6
SMEMRD# and SMEMWR#, ISA memory card signals 5-2
software
compatibility 8-1, 8-2
development 1-1
PCI 4-4, 4-6
PLXMon 3-2, 7-2
reset 3-1, 5-2, 8-26, 9-13
specifications
See electrical specifications, physical specs or signal specs
start bit 3-1, 3-2
states, basic bus 2-3
STOP# 9-6, 11-4, 11-5
strobe 1-2, 1-3, 1-5, 2-4, 2-5, 5-5, 8-17–8-21, 9-2, 9-9
subsystem
ID 8-1, 8-9
vendor ID 3-3, 8-1, 8-9
supplemental documentation
See Preface

T

Target Abort 2-1, 8-4
TEST 1-3, 1-5, 9-1, 9-4, 11-4, 11-5
thermal resistance 10-1
32000 PCI Clock timeout 4-2
timer, Retry delay 1-2, 4-3, 8-1
timing diagrams 4-8–4-42
chip selects 6-3
interrupts 7-3–7-6
ISA Interface mode 5-8–5-14
Multiplexed mode Local Bus and Big Endian 4-37–4-42
Non-Multiplexed mode Local Bus 4-17–4-36
reset 3-6
serial EEPROM 3-6, 4-9–4-16
TRDY# 2-1, 4-3, 4-7, 8-25, 9-5, 9-6, 11-4, 11-5
TTL 1-2, 1-3, 1-5, 9-2

U

User I/O 4-14, 4-15, 7-1, 7-2, 7-5, 7-6
CNTRL register 8-2, 8-25–8-26
USER[3:0] 10-3
USER0 1-3, 1-6, 4-14, 4-15, 5-1, 5-2, 5-4, 5-6, 7-2, 7-5, 7-6, 8-25, 9-2, 9-7, 11-4
USER1 1-3, 1-6, 5-1, 5-2, 5-4, 5-6, 7-2, 8-25, 9-2, 9-8, 11-4
USER2 1-3, 1-6, 7-2, 8-25, 9-2, 9-8, 11-4, 11-5
USER3 7-2, 8-25, 9-8, 11-4, 11-5

V

V_{CC} 1-7, **9-1**
V_{DD} 9-4, **11-4**, **11-5**
vendor
add-in board ID 8-9
ID 1-2, 3-3, 3-4, 8-1, 8-3
subsystem ID 3-3, 8-1
Vital Product Data (VPD) not supported in PCI 9052 1-7
V_{SS} 9-4, **11-4**, **11-5**

W

wait states 2-5–2-7
generation 1-7, 2-10, 4-1, 4-3, 9-10
generator 2-3, 9-7, 9-9
internal 2-4, 4-19–4-24, 4-27–4-33, 4-38–4-42, 5-5, 8-17–8-21, 9-9
Local Bus 1-2, 1-3, 1-5, 9-1
PCI Bus 2-1
zero 4-19–4-24, 4-27–4-33, 4-38–4-42, 5-6, 5-7
WAITO# 1-3, 1-6, 2-4, 5-1, 5-2, 7-2, 8-25, 9-2, 9-7, 10-3, 11-4
WR# 1-2, 1-3, 1-5, 2-5, 5-5, 8-17–8-21, 9-2, 9-9, 10-3, 11-4, 11-5
write 1-7, 2-1, 2-9, 4-1
Direct Slave 4-3, 4-7
flush pending Delayed Read 4-2
PCI Configuration timing diagrams 4-10
PCI memory timing diagrams 4-11
registers 8-3–8-26
serial EEPROM sequential reads and writes 3-2
write cycle hold 1-2, 1-3, 1-5, 5-5, 8-17–8-21, 9-2
write strobe delay 1-2, 2-5, 5-5, 8-17–8-21, 9-9

Z

zero wait states
4-19–4-24, 4-27–4-33, 4-38–4-42, 5-6, 5-7