PCI 9052

Design Notes Rev. 1.1
May 2000

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9052	PCI 9052	Released Silicon	September 1997	October 1997

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.01	PCI 9052 Data sheet	December 1999

1. CS[3:0]# Signals (Chip Select)

Design Issue: The PCI 9052 drives CS[3:0]# all time. This results in a bus contention when the CS[3:0]# are shared by multiple masters.

Recommendation;

1. Tri-state CS[3:0]# from the PCI 9052 through an external 74LS125 (LHOLDA is used as a gate signal).
2. Add an external multiplexer to CS[3:0]# signals and use LHOLDA as the select signal.

2. External Pull-up and Pull-down Requirement

Design Issue: All local bus input signals are internally pulled to an inactive state through a 80K ohm pull-up resistor or 50K ohm pull-down resistor except for the MODE, LHOLD, EEDO, and LINTi[2:1] pins. Therefore, external pull-up or pull-down to some of these pins is required for proper functionality.

Recommendations:

MODE (pin #68): To select multiplexed bus mode, add a 2K ohm pull-up resistor to MODE pin. Add a 4.7K ohm pull-down resistor to select non-multiplexed bus mode.

LHOLD (pin #134): The local bus master request for the usage of the local bus uses LHOLD. It must be pull low through a 4.7K ohm resistor.

EEDO (pin #143): If a blank EEPROM is used, the PCI 9052 might load all zeros instead of the PCI 9050's default value. To prevent this from happening, add an external pull-up resistor on the EEDO signal.

LINTi[2:1]: Don't care

3. Floating Pin

Design Issue: Pin #45 is a multiplexed pin. In C-mode and J-mode, it is a N/C signal. It becomes HRDY signal in ISA-mode. This signal is not pulled-up internally.

Recommendation:

Therefore, external pull-up is recommended.

4. Delayed Read Retry/Disconnect

Design Issue: During Delayed Direct Slave Reads, if the delayed read mode bit, CNTRL[14] is set, the PCI 9052 will treat all PCI Delayed Read as Retries, which may allow for a second chance for the initial Master to complete the requested Read cycle. Any subsequent Direct Slave cycles to a different address other then from the address when the disconnect occurred will be retried until PCI address matches or a 32K clock timeout occurs.

Recommendations:

1. Software should recover from disconnect by retrying the initially requested Read cycle.
2. Software Software should wait for 32K clock timeout to occur before posting any other Reads to the PCI 9052.

5. PCI 9052 Initialization procedures

Design Issue: According to the PCI 9052 data book, during initialization when a serial EEPROM is installed, the first 16 bits are checked and if not FFFF, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise default values are used.

In actuality the PCI 9052 uses the first 48 bits, not 16 bits, to determine if the serial EEPROM is blank or not. If FFFFFFFFFFFF is not read, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise default values are used.

Recommendation:

No design changes are required.

6. Microsoft Win2000 Hardware compatibility test failure

Design Issue: The PCI 9052 fails the Win2000 hardware compatibility test due to the error message “ERROR: Extended Capabilities not supported on this device”.

Recommendation:

This result is expected, as the PCI 9052 does not support the Extended Capabilities feature. The PCI 9052 is compliant to PCI Specification v2.1. Extended Capabilities is part of the PCI Specification v2.2.

If a PCI Target device supporting PCI Specification v2.2 and Extended Capabilities is required, the PCI 9030 device is recommended.

7. Series Resistor for BCLKo signal

Design Issue: When the BCLKo signal is used to create a buffered version of the PCI clock for use by the local bus, a ringing effect can occur.

Recommendation:

If using the BCLKo signal, insert a 50-ohm resistor in series on the BCLKo signal and the ringing effect will be eliminated.