PCI 9052

Errata Rev. 1.0
January 1999

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9052	PCI 9052	Released Silicon	September 1997	October 1997

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.0	PCI 9052 Data Sheet	August 1997

The scope of this document encompasses the PCI 9052 PCI Bus Target Interface Device.

1. Delayed read during 32K PCI clocks timeout

Problem: As per PCI spec, when a master performs a delayed read, it must complete that delayed read. When a delayed read is not completed within 32K PCI clocks, the target with the pending delayed read should discard it. (protect against violations or PCI 2.0 devices). There is a one-clock window (last clock of 32K timeout) in which the PCI 9052 is discarding the delayed read. During this 1clock window, new PCI cycles are not monitored. If a new PCI cycle is begun during that 1 clock window, the PCI 9052 ignores the PCI cycle. Therefore, a master abort will occur on the PCI bus.

Solution/Workaround:

This is an extremely rare occurrence. If you encounter it, software should recover both the timeout and master abort with a retry.

2. LOCK# de-assertion during an idle phase

Problem: If a locked operation is done to the PCI 9052 and the LOCK# signal is de-asserted during an idle phase, the PCI 9052 has a one clock window in which it is loading LOCK# de-assertion condition into its FIFO. If a new PCI access (FRAME_ asserted) to the PCI 9052 occurs 1 clock after the LOCK# signal is de-asserted, the PCI 9052 will ignore it (master abort). This will occur because the PCI 9052 has not acknowledged the LOCK# de-assertion condition.

Solution/Workaround:

This is an extremely rare occurrence. If you encounter it, software should recover the master abort with a retry.

3. Window98 Operating System

Problem Description: To verify the Subsystem ID and Subsystem Vendor ID register (offset 2Ch), which is a "read only" register, Win98 performs a "configuration write" of value 0x0 to offset 2Ch during the OS loading. Since offset 2Ch is a "read only" register, its content remains the same. However, the "configuration write" to offset 2Ch also writes to offset 3Ch. This has the affect of zeroing out the Interrupt Line that was assigned by the host BIOS to the PCI9052 and therefore disable the PCI interrupt capability.

Solution/Workaround:

1. Under \HKEY_LOCAL_MACHINE \System \CurrentControlSet \Services \VxD \PCI, a flag value can be added for a specific PCI device that influences how PCI.VXD behaves with that device. Each binary flag value under this registry section is named using a numeric string based on the vendor and device ID of the corresponding PCI card. Bit 14 is the flag that controls whether or not PCI looks at the subsystem vendor ID of a PCI device. If this flag is set, PCI.VXD will not try to write to the subsystem vendor ID of that card. In addition, one needs to force a reboot from their INF after completing the installation of their device.
2. Use PCI 9050 if applicable