Design Notes Documentation

A. Affected Silicon Revision

This document details Design Notes in the following silicon:

Product	Part Number	Description	Status
PCI 9052	PCI9052	160-pin PQFP Package	Production Released Silicon

B. Documentation Revision

Document	Revision	Description	Publication Date
PCI 9052 Data Book	2.0	Data Book	September 2001
PCI 9052 Errata Documentation	See www.plxtech.com for latest revision	Errata Documentation	

C. Design Notes Summary

#	Description
1	CS[3:0]# Signals (Chip Selects) always driven
2	External Pull-up and Pull-down Requirements
3	Floating Pin
4	Delayed Read Retry/Disconnect
5	Detection of blank EEPROM during initialization
6	Microsoft Win2000 Hardware compatibility test failure
7	Series Resistor for BCLKo signal
8	Local bus Data signals driven randomly during reset

D. Design Notes Details

1. CS[3:0]# Chip Selects and/or ISA MEMRD# and MEMWR# signals always driven

Design Issue: The PCI 9052 always drives CS[3:0]# and/or MEMRD# and MEMWR# (in ISA mode CS[1:0]# pin functionality is MEMRD# and MEMWR#). Bus contention could occur if multiple local masters drive these signals.

Recommendation:
These signals can be isolated with three-state buffers, or a bus switch (such as a Pericom PI5C3125 (5V 4-bit bus switch)), or multiplexer (such as a Fairchild NC7SZ157). Device propagation delay of less than 3 ns is recommended.

A flip-flop can be used to enable signal output only when the PCI 9052 owns the Local bus. The active-low Output Enable input (or multiplexer Select input) of the isolation device can be driven by the output of a positive edge-triggered D-type flip-flop, as shown in Figure 1 below. Fast devices are recommended, such as the Fairchild NC7SZ175 Flip-Flop (propagation delay 2.6 ns typical), and NC7SZ32 OR gate (t_{pd} 2.4 ns typ).

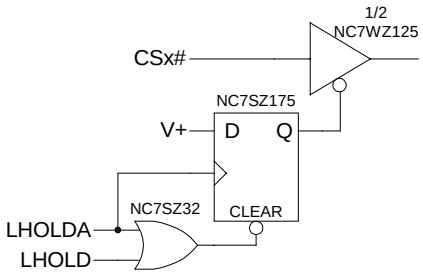

Figure 1. Disabling CSx# output when PCI9052 does not own the Local Bus

Once LHOLDA output has been asserted to give Local Bus ownership to another master in response to LHOLD assertion, the PCI 9052 will not assert LHOLDA again until LHOLD has been negated and subsequently re-asserted.

An alternative circuit shown in Figure 2 can be used to additionally guarantee that the CS[3:0]# and/or MEMRD# and MEMWR# signals are also isolated during reset.

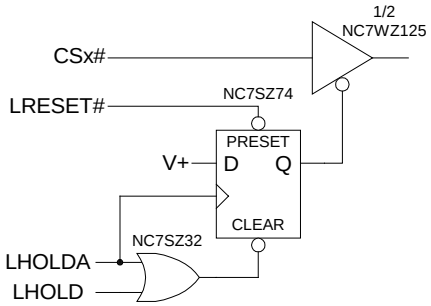

Figure 2. Disabling CSx# output during reset and when PCI 9052 does not own the local bus

2. External Pull-up and Pull-down Requirements

Refer to PCI 9052 Data Book revision 2.0, Section 9.2 for pull-up/pull-down recommendations.

3. Floating Pin #45

Refer to PCI 9052 Data Book revision 2.0, Section 9.2.1 for NC/CHRDY pin recommendations.

4. Delayed Read Retry/Disconnect

Design Issue: During Direct Slave Delayed Reads, if the Delayed Read Mode bit (CNTRL[14]) is set, the PCI 9052 will treat all PCI Delayed Reads as Retries, which may allow the initial Master a second chance to complete the requested read cycle. Any subsequent Direct Slave cycles to an address other than the address for which the disconnect occurred will be retried until the PCI address matches, or a 32K clock timeout occurs.

Recommendations:

1. Software should recover from a disconnect by retrying the initially requested read cycle.
2. Software should wait for a 32K clock timeout to occur before posting any other reads to the PCI 9052.

5. Detection of blank EEPROM during initialization

Design Issue: According to PCI 9052 Data Book revisions prior to revision 2.0, during initialization with a serial EEPROM installed, the first 16 bits are checked and if the value is not FFFF, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise default values are used.

In actuality the PCI 9052 checks the first 48 bits, not 16 bits, to determine whether the serial EEPROM is blank. If FFFF_FFFF_FFFF is not read, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise default values are used.

Recommendation: No design changes are required. Refer to PCI 9052 Data Book revision 2.0, Section 3.1 for further details of operation.

6. Microsoft Win2000 Hardware compatibility test failure

Design Issue: The PCI 9052 fails the Win2000 hardware compatibility test due to the error message “ERROR: Extended Capabilities not supported on this device”.

Recommendation: This result is expected, as the PCI 9052 does not support the Extended Capabilities feature. The PCI 9052 is compliant with PCI Specification r2.1, while Extended Capabilities is part of PCI Specification r2.2. If a PCI Target device supporting PCI Specification v2.2 and Extended Capabilities is required, the PCI 9030 is recommended. However, the PCI 9052 will work under Win2000 even though Extended Capabilities is not supported.

7. Series Resistor for BCLKo signal

Design Issue: When the BCLKo signal is used to provide a buffered version of the PCI clock for use as the local clock input (LCLK), a ringing effect can occur.

Recommendation: If using the BCLKo signal, insert a 50-ohm resistor in series on the BCLKo signal, and the ringing effect will be eliminated.

8. Local bus Data signals driven randomly during reset

Design Issue: During local bus reset (LRESET# active), the PCI 9052 drives the local data bus signals (LAD bus in multiplexed mode, or LD bus in non-multiplexed mode) to random high or low power-up states.

Recommendation: External logic is required to guarantee the logic state of the local data bus signals during reset. One solution is to use a bus switch to float

the data lines during reset. The Pericom P15C34X245, for example, a 32-bit, 5V device, provides a single chip solution for 32-bit bus isolation.

1. For non-ISA mode (INTCSR[12] = 0):
   Typically bus switch Enable inputs are active-low. Therefore, LRESET# can normally be connected through an inverter to the bus switch active-low Enable input.

2. For ISA mode (MODE = 0, INTCSR[12] = 1):
   In ISA mode, LRESET# polarity is switched from active-low to active-high to redefine the signal as LRESET. At boot time, this output is low during PCI reset, then high when RST# de-asserts, and then switches low approximately 750 µs later when the INTCSR register is loaded during EEPROM initialization. Therefore using LRESET# output to gate the bus switch is not a valid solution for ISA mode (as it is in non-ISA mode), and another solution should be considered if the data bus must be isolated during reset.