PCI 9050-1 Data Book

Version 1.02

December 1999

Website: http://www.plxtech.com
Email: apps@plxtech.com
Phone: 408-774-9060
800-759-3735
Fax: 408-774-2169

Order Number: 9050-SIL-DB-P1-1.02

Printed in the USA, December 1999

CONTENTS

Contents

FIGURES

This page intentionally left blank.

TABLES

Tables

TIMING DIAGRAMS

This page intentionally left blank.

REVISION HISTORY

Date	Revision	Comment
1996	1.0	Initial release
April 1996	1.01	Information not available.
December 1999	1.02	Applied minor format changes and corrected minor typographical errors. Changed title from “Data Sheet” to “Data Book”. Added 800 phone number. Changed copyright date to 1999. Added primary title page, disclaimer and trademarks, part number, and list of Figures, Tables, and Timing Diagrams. Changed “negate” to “de-assert.” Changed “field” to “bit” in register-related tables. Reorganized timing diagrams (Section 8) by type. Correct Figure 3-1 to state Spaces 0-3 for Local Base Address (Remap) for PCI to Local Address Space. Table 4-15, PCIBAR3[3], corrected reference to LAS1BRD. Section 7, requenced content and added section headings.

This page intentionally left blank.

1. GENERAL DESCRIPTION

The PCI 9050-1 provides a compact high performance PCI bus target (slave) interface for adapter boards. The PCI 9050-1 is designed to connect a wide variety of local bus designs to the PCI bus and allow relatively slow local bus designs to achieve 132 MB/sec burst transfers on the PCI bus.

The PCI 9050-1 can be programmed to connect directly to the multiplexed or nonmultiplexed 8, 16, or 32-bit local bus. The 8- and 16-bit modes enable easy conversion of ISA designs to PCI. (Refer to Figure 1-1.)

The PCI 9050-1 contains a bidirectional FIFO to speed match the 32-bit wide, 33 MHz PCI bus to a local bus, which may be narrower or slower. Up to five local address spaces and up to four chip selects are supported.

1.1 Major Features

PCI Specification v2.1 compliant. The PCI 9050-1 is compliant with PCI Specification v2.1, supporting low cost slave adapters. The chip allows simple conversion of ISA adapters to PCI.

Direct slave (Target) data transfer mode. The PCI 9050-1 supports memory mapped and I/O mapped burst accesses from the PCI bus to the local bus. Bidirectional FIFOs enable high-performance bursting on the local and PCI buses. The PCI bus is always bursting; however, the local bus can be set to bursting or continuous single cycle.

Interrupt generator. The PCI 9050-1 can generate a PCI interrupt from two local bus interrupt inputs.

Clock. The PCI 9050-1 local bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock, allowing the local bus to run at an independent rate from the PCI clock. The buffered PCI bus clock (BCLKo) may be connected to the local bus clock (LCLK).

Programmable local bus configurations. The PCI 9050-1 supports 8-, 16-, or 32-bit local buses, which may be multiplexed or nonmultiplexed. The PCI 9050-1 has four byte enables (LBE[3:0]#), 26 address lines (LA[27:2]), and 32-, 16-, or 8-bit data lines (LAD[31:0]).

Bus drivers. All control, address, and data signals generated by the PCI 9050-1 directly drive the PCI and local bus, without external drivers.

Serial EEPROM interface. The PCI 9050-1 contains an optional serial EEPROM interface, which can be used to load configuration information. This is useful for loading information unique to a particular adapter (such as Network ID, Vendor ID, and chip selects).

Four local chip selects. The PCI 9050-1 provides up to four local chip selects. The base address and range of each chip select are independently programmable from the EEPROM or host.

Five local address spaces. The base address and range of each local address space are independently programmable from the EEPROM or host.

Big/Little Endian byte swapping. The PCI 9050-1 supports Big and Little Endian byte ordering. The PCI 9050-1 also supports Big Endian byte lane mode to redirect the current word/byte lane during 16 or 8-bit local bus operation.

Read/write strobe delay and write cycle hold. The Read and Write (RD# and WR#) signals can be delayed from the beginning of the cycle for legacy interfaces (such as ISA bus).

Local bus wait states. In addition to the LRDYi# (local ready input) handshake signal for variable wait state generations, the PCI 9050-1 has an internal wait state(s) generator (R/W address to data, R/W data-to-data, and R/W data-to-address).

Programmable prefetch counter. The local bus prefetch counter can be programmed for 0 (no prefetch), 4, 8, 16, or continuous (prefetch counter turned off) Prefetch mode. The prefetched data can be used as cached data if a consecutive address is used (must be longword (Lword) aligned).

Delayed Read mode. The PCI 9050-1 supports PCI Specification 2.1 Delayed Read with

- PCI Read with Write Flush Mode
- PCI Read No Flush Mode
- PCI Read No Write Mode
- PCI Write Mode

PCI Read/Write request time out timer. The PCI 9050-1 has a programmable PCI Target Retry Delay timer, which, when expired, generates a RETRY to the PCI bus.

PCI LOCK mechanism. The PCI 9050-1 supports PCI target LOCK sequences. A PCI master can obtain exclusive access to the PCI 9050-1 device by locking to the PCI 9050-1.

PCI bus transfers up to 132 MB/sec.

Low power CMOS in 160-pin plastic QFP package (PQFP).

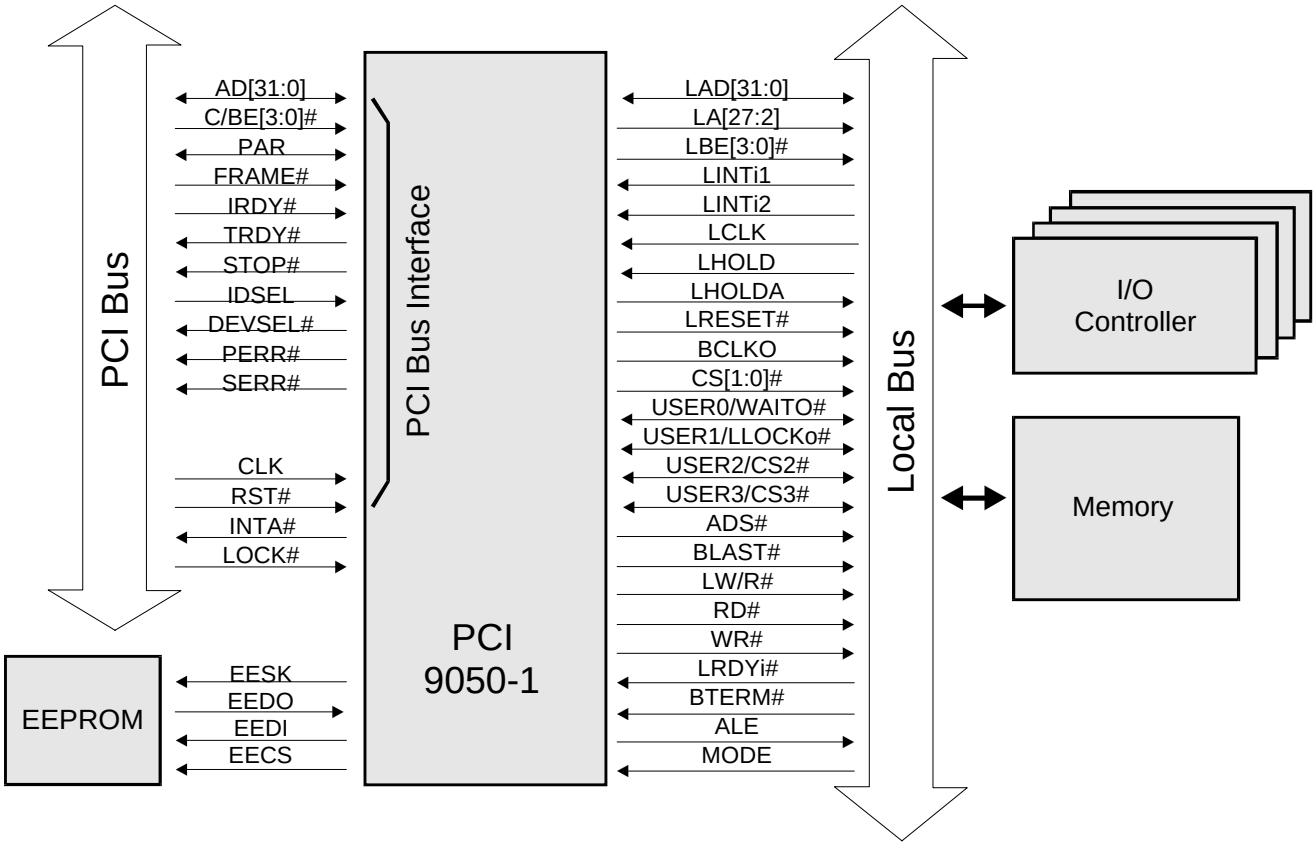


Figure 1-1. PCI 9050-1 Block Diagram

2. BUS OPERATION

2.1 PCI Bus Cycles

The PCI 9050-1 is PCI Specification 2.1 compliant.

2.1.1 PCI Target Command Codes

As a target, the PCI 9050-1 allows access to the PCI 9050-1 internal registers and the local bus, using the commands listed in Table 2-1.

Table 2-1. Target Command Codes

Command Type	Code(C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All read or write accesses to the PCI 9050-1 can be byte, word, or Lword accesses. All memory commands are aliased to the basic memory commands. All I/O accesses to the PCI 9050-1 are decoded to an Lword boundary. The byte enables are used to determine which bytes are read from or written to. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.2 Local Bus Cycles

2.2.1 Local Bus Slave

Not supported. No Direct Master capability. The internal registers are not readable/writable from the local side. The internal registers are accessible from the Host CPU on the PCI bus or from the serial EEPROM.

2.2.2 Local Bus Master

The PCI 9050-1 is the master of the local bus.

2.2.2.1 Ready/Wait-State Control

If the READY input is disabled, the external READY input has no effect on wait states for a local access. The wait-state counter internally generates wait states between address-to-data, data-to-data, and data-to-address cycles. The wait-state counter is initialized with its configuration register value at the start of each data access.

With the READY input enabled, the READY input has no effect until the wait-state counter is 0. The READY input then controls the number of additional wait states.

The BTERM input is not sampled until the wait-state counter is 0.

2.2.2.2 Burst Mode and Continuous Burst Mode (BTERM "Burst Terminate" Mode)

Burst Mode. If bursting is enabled and the BTERM input is not enabled, the PCI 9050-1 bursts as follows: Starts on any boundary and continues up to an address boundary, as described in Table 2-2. After transferring the data at the boundary, the PCI 9050-1 generates a new address cycle (ADS#).

Table 2-2. Burst Mode Boundaries

Bit Bus	Boundary
32	4 Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
16	4 words or up to a quad word boundary (LA2, LA1 = 11)
8	4 bytes or up to a quad byte boundary (LA1, LA0 = 11)

Continuous Burst Mode (BTERM "Burst Terminate" Mode). BTERM mode enables the PCI 9050-1 to

perform long bursts to devices that can accept longer than 4 Lword bursts. The PCI 9050-1 generates one address cycle, then continues to burst data. If a device requires a new address cycle after a certain address boundary, it can assert the BTERM# input to cause the PCI 9050-1 to generate a new address cycle. The BTERM# input is a ready input that acknowledges the current data transfer and requests that a new address cycle be generated (ADS#), which is the address for the next data transfer. Enable BTERM mode and the PCI 9050-1 asserts BLAST# only if the FIFOs become FULL or EMPTY, or a transfer is complete.

Partial Lword Accesses. Lword accesses (in which not all byte enables are asserted) break into single address and data cycles.

Table 2-3. Partial Lword Accesses

Bus Region Descriptor Register Bits		Result (Number of Transfers)
Burst Enable	**Bterm Enable**	
0	0	Single Cycle (Default)
0	1	Single Cycle
1	0	Burst Mode—4 Lwords at a time
1	1	Continuous Burst Mode—Burst until BTERM# input is asserted (See above descriptions)

2.2.2.3 Recovery States

In Nonmultiplexed mode, the PCI 9050-1 uses the NXDA (data-to-address wait states) value in the bus region descriptor register to determine how many recovery states to insert between the last data transfer and the next address cycle. This value can be programmed between 0 and 3 clock cycles.

In Multiplexed mode, the PCI 9050-1 inserts a minimum of one recovery state between the last data transfer and the next address cycle. Add recovery states by programming values greater than one into the NXDA bits of the bus region descriptor register.

2.2.2.4 Direct Slave Write Access to 8- and 16-Bit Bus

For direct slave writes/reads, only the bytes specified by a PCI bus master are written/read. Access to an 8- or 16-bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded to provide local address bits LA[1:0].

Do not use direct PCI access to an 8-bit bus with nonadjacent byte enables in a PCI Lword. Nonadjacent byte enables cause an incorrect LA[1:0] address sequence when bursting to memory. Therefore, for each Lword written to an 8-bit bus, the PCI 9050-1 does not write data after the first gap. Direct PCI accesses to an 8-bit bus with nonadjacent byte enables are not terminated with a Target Abort.

Therefore, for nonadjacent bytes (illegal byte enables), the PCI master must perform single cycles.

2.2.2.5 Local Bus Little/Big Endian

The PCI bus is a Little Endian bus, where data is Lword aligned to the lowermost byte lane. Byte 0 (address 0) appears in AD[7:0], Byte 1 appears in AD[15:8], Byte 2 appears in AD[23:16], and Byte 3 appears in AD[31:24].

The PCI 9050-1 local bus can be programmed to operate in Big or Little Endian mode. In Big Endian mode, the PCI 9050-1 transposes the data byte lanes. Transfer data as follows.

32-Bit Local Bus. Data is Lword aligned to the upper most byte lane. Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16], Byte 2 appears on Local Data [15:8], and Byte 3 appears on Local Data [7:0].

16-Bit Local Bus. For a 16-bit local bus, the PCI 9050-1 can be programmed to use the upper or lower word lane. Byte lanes and burst order appear in Table 2-4 and Table 2-5.

Table 2-4. Upper Word Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16]
Second transfer	Byte 2 appears on Local Data [31:24], Byte 3 appears on Local Data [23:16]

Table 2-5. Lower Word Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [15:8], Byte 1 appears on Local Data [7:0]
Second transfer	Byte 2 appears on Local Data [15:8], Byte 3 appears on Local Data [7:0]

8-Bit Local Bus. For an 8-bit local bus, the PCI 9050-1 can be programmed to use the upper or lower byte lane. Byte lanes and burst order appear in Table 2-6 and Table 2-7.

Table 2-6. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-7. Lower Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [7:0]
Second transfer	Byte 1 appears on Local Data [7:0]
Third transfer	Byte 2 appears on Local Data [7:0]
Fourth transfer	Byte 3 appears on Local Data [7:0]

For each of the following transfer types, the PCI 9050-1 local bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Direct Slave PCI access to Local Address Space 0
- Direct Slave PCI access to Local Address Space 1
- Direct Slave PCI access to Local Address Space 2
- Direct Slave PCI access to Local Address Space 3
- Direct Slave PCI access to Expansion ROM Space

2.2.2.6 Local Chip Selects

The PCI 9050-1 has four programmable chip selects. A chip select is asserted when the following are true:

- The value of the local address bus falls within the programmed range of the chip select
- The chip select is enabled (bit 0 of the Chip Select Base Address Register = 1)
- The local bus is in the address or data phase (chip select is asserted with ADS# and de-asserted at the end of the data phase)

Each chip select has an associated register, which determines the range of the chip select and the local base address. Starting from bit 1 of the register and scanning toward bit 27, the first “1” found defines the size. The most significant bits, excluding the first “1” found, define the base address.

Examples:

To program a chip select with a base of 04567000 and a range of 256 bytes, program 04567081 into the chip select register, determined as follows:

- Bit 0 ≤ 1 enables the chip select.
- Bits [7:1] ≤ 1000000 define a range of 256 bytes. Bit 7 is the first “1” found while scanning from bit 1 to bit 27, thus removing bits [7:1] from the decoding process.
- Bits [27:8] ≤ 0x045670 define the upper 20 bits of the base address

To program a chip select with a base of 00000000 and a range of 256 MB (entire local address space), program 8000001 into the chip select register, determined as follows:

- Bit 0 ≤ 1 enables the chip select.
- Bits [27:1] ≤ 8000000 define a range of 256 MB. Bit 27 is the first "1" found while scanning from bit 1 to bit 27, thus removing bits [27:1] from the decoding process.
- Since there are no more significant bits above bit 27, and the chip select spans the entire local address space, the base address defaults to 0.

Chip selects CS2# and CS3# are multiplexed with user bits USER2 and USER3. Program bits 6 and 9 in the Miscellaneous Control Register (CNTRL; 50H) to select the function of these pins.

3. FUNCTIONAL DESCRIPTION

3.1 PCI 9050-1 Initialization

During power up, the PCI RST# signal resets the default values of the PCI 9050-1 internal registers. In return, the PCI 9050-1 outputs the local reset signal (LRESET#) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI 9050-1 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9050-1 configuration registers can be written only by the optional serial EEPROM or the PCI host processor. During the serial EEPROM initialization, the PCI 9050-1 response to PCI target accesses is RETRYs.

3.2 Reset

3.2.1 PCI Bus Input RST#

The PCI bus RST# input causes all PCI bus outputs to float, resets the entire PCI 9050-1, and asserts the local reset output LRESET#.

3.2.2 Software Reset

A host on the PCI bus can set the software reset bit in the Miscellaneous Control Register (CNTRL; 50h) to reset the PCI 9050-1 and assert LRESET# output. The contents of the PCI and local configuration registers are not reset. When the software reset bit is set, the PCI 9050-1 responds only to configuration registers accesses, and not to local bus accesses. The PCI 9050-1 remains in this reset condition until the PCI host clears the software reset bit.

3.2.3 Local Bus Output LRESET#

LRESET# is asserted when PCI bus RST# input is asserted (4 to 10 ns delay) or bit 30 (the software reset bit) in the Miscellaneous Control Register (CNTRL; 50h) is set to a value of 1.

3.3 EEPROM

After reset, the PCI 9050-1 attempts to read the EEPROM to determine its presence. An active low start bit indicates the EEPROM is present. (Refer to the manufacturer's data sheet for the particular EEPROM being used.) If the first word in the EEPROM is not FFFF, then the PCI 9050-1 assumes the device is not blank, and continues reading.

The EEPROM first stores the most significant bit of each 32-bit word. (The first bit in the EEPROM is bit 15 of the Device ID.) The 25 32-bit words are sequentially stored in the EEPROM. (Example: National NM93CS46 or compatible.)

***Note**: 2K-bit devices, such as 93CS56, are not compatible.*

A host on the PCI bus can read or program the EEPROM. Bits [29:24] of the Miscellaneous Control Register (CNTRL: 50h) control the PCI 9050-1 pins, enabling reading or writing of EEPROM bits. (Refer to the manufacturer's data sheet for the particular EEPROM being used.)

To reload the Serial EEPROM data into the PCI 9050-1 Internal registers, write "1" to bit 29 of register (CNTRL; 50h).

To read/write to the serial EEPROM:

1. Enable the EEPROM CS[3:0]# by writing "1" to bit 25 of the register (CNTRL; 50h).
2. Generate the Serial EEPROM clock by writing "0" and "1". The data is read or written during the zero-to-one transition (refer to bit 24).
3. Send the command code to the Serial EEPROM.
4. If the Serial EEPROM is present, a "0" value is returned as a start bit after the command code.
5. Read or write the data.
6. Write "0" to bit 25 to end the Serial EEPROM access (the serial EEPROM CS[3:0]# pin will go low).

The EEPROM load sequence, listed in Table 3-1, uses the following abbreviations:

MSW = Most Significant Word Bits [31:16]

LSW = Least Significant Word Bits [15:0]

3.3.1 EEPROM Load Sequence

Table 3-1. EEPROM Load Sequence

Note: *EEPROM value shown is the register value for the PCI 9050-1 Demo Board.*

EEPROM Offset	Register Offset	EEPROM Value	Register Description
0h	PCI 02h	9050-1	Device ID.
2h	PCI 00h	10B5	Vendor ID.
4h	PCI 0Ah	0680	Class Code.
6h	PCI 08h	000x	Class code (revision is not loadable).
8h	PCI 2Eh	9050-1	Subsystem ID.
Ah	PCI 2Ch	10B5	Subsystem Vendor ID.
Ch	PCI 3Eh	xxxx	(Maximum Latency and Minimum Grant are not loadable.)
Eh	PCI 3Ch	01xx	Interrupt Pin (Interrupt Line Routing is not loadable).
10h	LOCAL 02h	0FFE	MSW of Range for PCI to Local Address Space 0 (1 MB).
12h	LOCAL 00h	0000	LSW of Range for PCI to Local Address Space 0 (1 MB).
14h	LOCAL 06h	0FFE	MSW of Range for PCI to Local Address Space 1.
16h	LOCAL 04h	0000	LSW of Range for PCI to Local Address Space 1.
18h	LOCAL 0Ah	0FFF	MSW of Range for PCI to Local Address Space 2.
1Ah	LOCAL 08h	0000	LSW of Range for PCI to Local Address Space 2.
1Ch	LOCAL 0Eh	0FFC	MSW of Range for PCI to Local Address Space 3.
1Eh	LOCAL 0Ch	0000	LSW of Range for PCI to Local Address Space 3.
20h	LOCAL 12h	0000	MSW of Range for PCI to Local Expansion ROM (64 KB).
22h	LOCAL 10h	0000	LSW of Range for PCI to Local Expansion ROM (64 KB).
24h	LOCAL 16h	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 0.
26h	LOCAL 14h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 0.
28h	LOCAL 1Ah	0002	MSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ah	LOCAL 18h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ch	LOCAL 1Eh	0004	MSW of Local Base Address (Remap) for PCI to Local Address Space 2.
2Eh	LOCAL 1Ch	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 2.
30h	LOCAL 22h	0008	MSW of Local Base Address (Remap) for PCI to Local Address Space 3.
32h	LOCAL 20h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 3.
34h	LOCAL 26h	0010	MSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
36h	LOCAL 24h	0000	LSW of Local Base Address (Remap) for PCI to Local Expansion ROM.

Table 3-1. EEPROM Load Sequence (continued)

EEPROM Offset	Register Offset	EEPROM Value	Register Description
38h	LOCAL 2Ah	0080	MSW of Bus Region Descriptors for Local Address Space 0.
3Ah	LOCAL 28h	0026	LSW of Bus Region Descriptors for Local Address Space 0.
3Ch	LOCAL 2Eh	0080	MSW of Bus Region Descriptors for Local Address Space 1.
3Eh	LOCAL 2Ch	003F	LSW of Bus Region Descriptors for Local Address Space 1.
40h	LOCAL 32h	0040	MSW of Bus Region Descriptors for Local Address Space 2.
42h	LOCAL 30h	0037	LSW of Bus Region Descriptors for Local Address Space 2.
44h	LOCAL 36h	5421	MSW of Bus Region Descriptors for Local Address Space 3.
46h	LOCAL 34h	38E9	LSW of Bus Region Descriptors for Local Address Space 3.
48h	LOCAL 3Ah	0000	MSW of Bus Region Descriptors for Expansion ROM Space.
4Ah	LOCAL 38h	0000	LSW of Bus Region Descriptors for Expansion ROM Space.
4Ch	LOCAL 3Eh	0004	MSW of Chip Select (CS) 0 Base and Range Register.
4Eh	LOCAL 3Ch	0001	LSW of Chip Select (CS) 0 Base and Range Register.
50h	LOCAL 42h	000A	MSW of Chip Select (CS) 1 Base and Range Register.
52h	LOCAL 40h	0001	LSW of Chip Select (CS) 1 Base and Range Register.
54h	LOCAL 46h	0000	MSW of Chip Select (CS) 2 Base and Range Register.
56h	LOCAL 44h	0000	LSW of Chip Select (CS) 2 Base and Range Register.
58h	LOCAL 4Ah	0004	MSW of Chip Select (CS) 3 Base and Range Register.
5Ah	LOCAL 48h	8001	LSW of Chip Select (CS) 3 Base and Range Register.
5Ch	LOCAL 4Eh	0000	MSW of Interrupt Control/Status Register.
5Eh	LOCAL 4Ch	0000	LSW of Interrupt Control/Status Register.
60h	LOCAL 52h	0005	MSW of EEPROM Control and Miscellaneous Control Register.
62h	LOCAL 50h	4291	LSW of EEPROM Control and Miscellaneous Control Register.

3.4 Internal Register Access

The PCI 9050-1 chip provides several internal registers, allowing maximum flexibility in bus interface design and performance. The register types are as follows:

- **PCI registers** (accessible from the PCI bus and EEPROM)
- **Local configuration registers** (accessible from the PCI bus and EEPROM)

***Note**: The Local Configuration Base Address Register access can be limited to memory mapped or I/O mapped. Access can also be disabled by way of bits [13:12] of the register at (CNTRL; 50h).*

3.4.1 Internal Registers

Device and Vendor IDs. There are two sets of device and vendor IDs. The Device and Vendor ID are located at offset 0 of the PCI Configuration Registers. The Subsystem Vendor ID and Subsystem Device ID are at offset 2Ch of the PCI configuration Registers. The Device ID and Vendor ID identify the particular device, and manufacturer of the device. The Subsystem Vendor ID and Subsystem ID provide a way to distinguish between vendors of the PCI interface chip and the manufacturer of the add-in board using the PCI chip.

Status Register. This register contains information of PCI bus-related events.

Command Register. This register controls the ability of a device to respond to PCI accesses. It controls whether the device responds to I/O space or memory space accesses.

Class Code Register. This register identifies the general function of the device. Refer to the PCI Specification for further details.

Revision ID Register. The value read from this register represents the current silicon revision of the PCI 9050-1.

Header Type. This register defines the format of the device's configuration header and whether the device is single-function or multifunction.

Cache Line Size. This register defines the system cache line size in units of 32-bit words.

PCI Base Address Register for Memory Accesses to Local Configuration Registers. The system BIOS uses this register to assign a segment of the PCI address space for memory accesses to the PCI 9050-1 Local Configuration Registers. The PCI address range occupied by these configuration registers fixes at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF70, determining the required memory space of 128 bytes. The host then writes the base address to bits [31:7].

PCI Base Address Register for I/O Accesses to Local Configuration Registers. The system BIOS uses this register to assign a segment of the PCI address space for I/O accesses to the PCI 9050-1 Local Configuration Registers. The PCI address range occupied by these configuration registers fixes at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF71, determining a required 128 bytes of I/O space. The host then writes the base address to bits [31:7].

PCI Base Address Register for Accesses to Local Address Space 0 (also true for Space 1, 2, and 3). The system BIOS uses this register to assign a segment of the PCI address space for accesses to Local Address Space 0. The PCI address range occupied by this space is determined by the Local Address Space 0 Range Register. During initialization, the host writes FFFFFFFF to this register, then reads back a value determined by the range. The host then writes the base address to the upper bits of this register.

PCI Expansion ROM Base Address Register. The system BIOS uses this register to assign a segment of the PCI address space for accesses to the Expansion ROM. The PCI address range occupied by this space is determined by the Expansion ROM Range Register. During initialization, the host writes FFFFFFFF to this register, then reads back a value determined by the range. The host then writes the base address to the upper bits of this register.

PCI Interrupt Line Register. This register identifies where the interrupt line of the device connects on the interrupt controller(s) of the system.

PCI Interrupt Pin Register. This register specifies the interrupt request pin (if any) to be used.

3.4.2 PCI Bus Access to Internal Registers

The PCI 9050-1 configuration registers are accessed from the PCI bus by way of a configuration type 0 cycle.

The PCI 9050-1 local configuration registers are accessed by one of the following:

- A memory cycle, with the PCI bus address matching the base address specified in the PCI Base Address Register for Memory Accesses to Local Configuration Registers (PCIBAR0; 10h)
- An I/O cycle, with the PCI bus address matching the base address specified in the PCI Base Address Register for I/O Accesses to Local Configuration Registers (PCIBAR1; 14h)

All PCI read or write accesses to the PCI 9050-1 registers can be byte, word, or Lword accesses. Memory accesses to the PCI 9050-1 registers can be burst or non-burst. The PCI 9050-1 responds with a PCI Disconnect for all I/O accesses to PCI 9050-1 registers.

3.5 Direct Data Transfer Modes

The PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI 9050-1 control decoding and remapping of these accesses to local address space. Bidirectional FIFOs enable high-performance bursting on the local and PCI buses.

3.5.1 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI 9050-1 supports memory mapped burst transfer accesses and I/O mapped single transfer accesses to the local bus from the PCI bus. PCI Base Address registers are provided to determine adapter location in PCI memory and I/O space. In addition, local mapping registers are provided to allow address translation from the PCI address space to local address space.

The PCI 9050-1 disconnects after one transfer for all Direct Slave I/O accesses. For single cycle Direct Slave reads, the PCI 9050-1 reads a single local bus Lword. For Direct Slave memory accesses, burst read pre-fetching is enabled or disabled through the Local Address Space Bus Region Descriptor Registers. If read prefetching is disabled, the PCI 9050-1 disconnects after one read transfer. If prefetching is enabled, the read prefetch size can be programmed through Local Address Space Bus Region Descriptor Registers.

The PCI 9050-1 can be programmed though the Miscellaneous Control Register (CNTRL; 50h) to perform delayed reads, as specified in the PCI Specification 2.1.

3.5.1.1 PCI to Local Address Mapping

Five local address spaces (local spaces 0-3 and expansion ROM) are accessible from the PCI bus. A set of four registers defines each space, defining the local bus characteristics:

- PCI Base Address
- Local Range
- Local Base Address (Remap)
- Local Bus Region Descriptor

Byte Enables (LBE[3:0]#, pins 46-49) are encoded based upon configured bus width:

For a 32-bit bus, four byte enables indicate which of the four bytes are active during a data cycle:

- LBE3# Byte Enable 3 = LAD[31:24]
- LBE2# Byte Enable 2 = LAD[23:16]
- LBE1# Byte Enable 1 = LAD[15:8]
- LBE0# Byte Enable 0 = LAD[7:0]

For a 16-bit bus, LBE3#, LBE1#, and LBE0# are encoded to provide BHE#, LA1, and BLE#:

LBE3# Byte High Enable (BHE#) = LAD[15:8]

- LBE2# Unused
- LBE1# Address bit 1 = (LA1)
- LBE0# Byte Low Enable (BLE#) = LAD[7:0]

For an 8-bit bus, LBE1# and LBE0# are encoded to provide LA1 and LA0:

- LBE3# Unused
- LBE2# Unused
- LBE1# Address bit 1 = (LA1)
- LBE0# Address bit 0 = (LA0)

Each PCI to Local Address space is defined as part of the reset initialization:

Local bus initialization software. Range specifies which PCI address bits to use to decode a PCI access to local bus space. Each of the bits correspond to an address bit, with bit 31 corresponding to address bit 31. Write “1” to all bits to be included in the decoding. Write “0” to all bits to be ignored.

Remap PCI address into a local address. The bits in this register remap (replace) the PCI address bits used in decoding into the local address bits.

Local Bus Region Descriptor specifies the local bus characteristics, such as bus width, bursting, prefetching, and number of wait states.

PCI Initialization Software. PCI host bus-initialization software determines the required address space by writing a value of all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9050-1 returns zeros (0) in don't care address bits, specifying the required address space. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register.

Example: A 1-MB local address space 02300000h through 023FFFFFh is accessible from the PCI bus at PCI addresses 78900000h through 789FFFFFh.

1. Local initialization software sets the Range and Local Base address registers as follows:
   - Range = FFF00000h (1 MB, decode the upper 12 PCI address bits)
   - Local Base Address (remap) = 023XXXXXh (Local Base Address for PCI to local accesses)
2. PCI Initialization software writes all ones (1) to the PCI Base Address, then reads back the value. The PCI 9050-1 returns a value FFF00000h. The PCI software then writes to the PCI Base Address register:
   - PCI Base Address = 789XXXXXh (PCI Base Address for access to Local Address space)

For PCI accesses to the local bus, the PCI 9050-1 has a 16-Lword (64-byte) write FIFO and an 8-Lword (32-byte) read FIFO. The FIFO enables the local bus to operate independently of the PCI bus. The PCI 9050-1 can be programmed to return a RETRY response or to throttle TRDY# for PCI bus transactions attempting to write to the PCI 9050-1 local bus when the write FIFO is full.

For PCI read transactions from the PCI 9050-1 local bus, the PCI 9050-1 holds off TRDY# while gathering the local bus Lword to be returned. For read accesses mapped to the PCI memory space, the PCI 9050-1 prefetches up to four Lwords from the local bus. Unused read data is flushed from the FIFO. For read accesses mapped to the PCI I/O space, the PCI 9050-1 does not prefetch read data. It breaks each read of the burst cycle into a single address/data cycle on the local bus.

The period of time that the PCI 9050-1 holds off TRDY# is programmed in the Miscellaneous Control Register (CNTRL: 50h). The PCI 9050-1 issues a RETRY to the PCI bus master when the programmed time period expires. This happens when the PCI 9050-1 cannot gain control of the local bus and return TRDY# within the programmed time period.

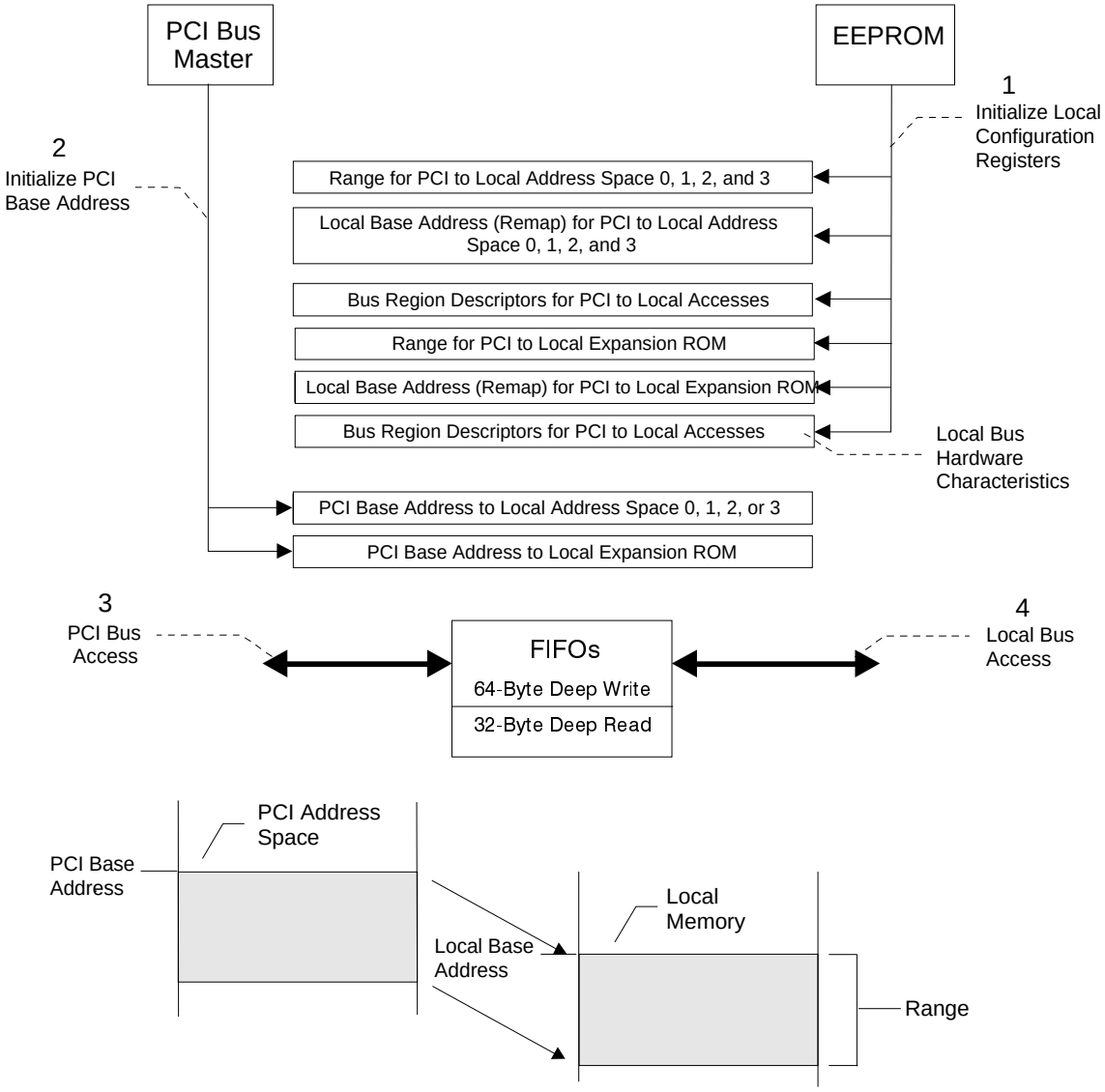


Figure 3-1. PCI Master Direct Access of Local Bus

3.5.1.2 Direct Slave Lock

The PCI 9050-1 supports direct PCI to local bus exclusive accesses (locked atomic operations). A PCI locked operation to local bus results in the entire address space 0-3 and expansion ROM space being locked until the PCI bus master releases the spaces. The PCI 9050-1 asserts LLOCKo# during the first clock of an atomic operation (address cycle) and de-asserts it a minimum of one clock following the last bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9050-1 detects PCI FRAME#, with PCI LOCK# de-asserted at the same time. (Refer to Section 8, "Timing Diagrams.") The Miscellaneous Control Register (CNTRL: 50h) enables locked operations.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. For example, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the local bus to other masters until the locked operation is complete.

3.5.1.3 Arbitration

When the PCI bus detects a new transfer request, the PCI 9050-1 takes control of the local bus. Another device can gain control of the local bus by asserting LHOLD. If the PCI 9050-1 has no cycles to run, it asserts LHOLDA, transferring control to the external master. If the PCI 9050-1 needs the local bus before the external master has finished, LHOLDA is de-asserted (preempt condition). The arbiter waits for LHOLD to be de-asserted before taking control of the bus.

3.6 PCI Interrupts (INTA#)

You can generate a PCI interrupt (INTA#) with local interrupt inputs LINTi1 and LINTi2, and the software interrupt (CNTRL register bit 30). Through the PCI 9050-1 Interrupt Control/Status Register, individual sources of an interrupt can be enabled or disabled. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI 9050-1 PCI bus interrupt is an asynchronous level output. Clear an interrupt by disabling an interrupt enable bit of a source or by clearing the cause of an interrupt.

3.7 PCI SERR# (PCI NMI)

The PCI 9050-1 generates a SERR# pulse if parity checking is enabled in the PCI Command Register and an address parity error is detected. Through the PCI Command Register, SERR# output is enabled.

4. REGISTERS

4.1 Register Address Mapping

Table 4-1. PCI Configuration Registers

PCI CFG Register Address	To ensure software compatibility with other versions of the PCI 9050 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 24 23 16 15 8 7 0				PCI Writable	EEPROM Writable
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	N
08h	Class Code			Revision ID	N	Y[31:8]
0Ch	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	N
10h	PCI Base Address 0 for Memory Mapped Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O Mapped Configuration Registers				Y	N
18h	PCI Base Address 2 for Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Local Address Space 1				Y	N
20h	PCI Base Address 4 for Local Address Space 2				Y	N
24h	PCI Base Address 5 for Local Address Space 3				Y	N
28h	Cardbus CIS Pointer (Not Supported)				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Base Address for Local Expansion ROM				Y	N
34h	***Reserved***				N	N
38h	***Reserved***				N	N
3Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	Y[15:8]

Table 4-2. Local Configuration Registers

PCI (Offset from Local Base Address)	To ensure software compatibility with other versions of the PCI 9050 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 0	PCI and EEPROM Writable
00h	Local Address Space 0 Range	Y
04h	Local Address Space 1Range	Y
08h	Local Address Space 2 Range	Y
0Ch	Local Address Space 3 Range	Y
10h	Local Expansion ROM Range	Y
14h	Local Address Space 0 Local Base Address (Remap)	Y
18h	Local Address Space 1 Local Base Address (Remap)	Y
1Ch	Local Address Space 2 Local Base Address (Remap)	Y
20h	Local Address Space 3 Local Base Address (Remap)	Y
24h	Expansion ROM Local Base Address (Remap)	Y
28h	Local Address Space 0 Bus Region Descriptors	Y
2Ch	Local Address Space 1 Bus Region Descriptors	Y
30h	Local Address Space 2 Bus Region Descriptors	Y
34h	Local Address Space 3 Bus Region Descriptors	Y
38h	Expansion ROM Bus Region Descriptors	Y
3Ch	Chip Select 0 Base Address	Y
40h	Chip Select 1 Base Address	Y
44h	Chip Select 2 Base Address	Y
48h	Chip Select 3 Base Address	Y
4Ch	Interrupt Control/Status	Y
50h	EEPROM Control, PCI Slave Response, User I/O Control, Init Control	Y

4.2 PCI Configuration Registers

All registers may be written to or read from byte, word, or Lword accesses.

Table 4-3. (PCIIDR; 00h) PCI Configuration ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX if no EEPROM is present.	Yes	EEPROM	10B5h
31:16	Device ID. Identifies the particular device. Defaults to the PLX part number for the PCI interface chip if no EEPROM is present.	Yes	EEPROM	9050-1

Table 4-4. (PCICR; 04h) PCI Command Register

Bit	Description	Read	Write	Value after Reset
0	I/O Space. A value of 1 allows the device to respond to I/O space accesses. A value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. A value of 1 allows the device to respond to memory space accesses. A value of 0 disables the device from responding to memory space accesses.	Yes	Yes	0
2	Master Enable. A value of 1 allows the device to function as a bus master. A value of 0 disables the device from generating bus master accesses.	Yes	No	0
3	Special Cycle. **Not Supported.**	Yes	No	0
4	Memory Write/Invalidate. **Not Supported.**	Yes	No	0
5	VGA Palette Snoop. **Not Supported.**	Yes	No	0
6	Parity Error Response. A value of 0 indicates a parity error is ignored and operation continues. A value of 1 indicates parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether the device does address/data stepping. A value of 0 indicates the device never does stepping. A value of 1 indicates the device always does stepping. ***Note:*** *Hardcoded to 0.*	Yes	No	0
8	SERR# Enable. A value of 1 enables the SERR# driver. A value of 0 disables the SERR# driver.	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. A value of 1 indicates fast back-to-back transfers can occur to any agent on the bus. A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15:10	***Reserved***.	Yes	No	0

Table 4-5. (PCISR; 06h) PCI Status Register

Bit	Description	Read	Write	Value after Reset
6:0	***Reserved***.	Yes	No	0
7	Fast Back-to-Back Capable. A value of 1 indicates the adapter can accept fast back-to-back transactions. A value of 0 indicates the adapter cannot accept fast back-to-back transactions.	Yes	No	1h
8	Master Data Parity Error Detected. **Not Supported.**	Yes	No	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. A value of 01 is medium.	Yes	No	01
11	Target Abort. A value of 1 indicates the PCI 9050-1 has signaled a target abort. Writing a value of 1 clears the bit (0).	Yes	Yes	0
12	Received Target Abort. A value of 1 indicates the PCI 9050-1 has received a target abort signal. **Not Supported.**	Yes	No	0
13	Received Master Abort. A value of 1 indicates the PCI 9050-1 has received a master abort signal. Not supported	Yes	No	0
14	Signaled System Error. A value of 1 indicates the PCI 9050-1 has reported a system error on the SERR# signal. Writing a value of 1 clears the error status bit (0).	Yes	Yes	0
15	Detected Parity Error. A value of 1 indicates the PCI 9050-1 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). To cause a bit to be set, one of these two conditions must exist: 1) the PCI 9050-1 detected a parity error during a PCI address phase; or, 2) the PCI 9050-1 detected a data parity error when it was the target of a write. Writing a value of 1 clears the bit (0).	Yes	Yes	0

Table 4-6. (PCIREV; 08h) PCI Revision ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. The silicon revision of the PCI 9050-1.	Yes	No	Current Revision

Table 4-7. (PCICCR; 09-0Bh) PCI Class Code Register

Bit	Description	Read	Write	Value after Reset
7:0	Specific Register Level Programming Interface (00h). No interface defined.	Yes	EEPROM	00
15:8	Subclass Encoding (80h). Other bridge device.	Yes	EEPROM	80h
23:16	Base Class Encoding. Other bridge device.	Yes	EEPROM	06h

Table 4-8. (PCICLSR; 0Ch) PCI Cache Line Size Register

Bit	Description	Read	Write	Value after Reset
7:0	System Cache Line Size (in units of 32-bit words). Can be written and read; however, the value has no effect on the operation of the chip.	Yes	Yes	0

Table 4-9. (PCILTR; 0Dh) PCI Latency Timer Register

Bit	Description	Read	Write	Value after Reset
7:0	PCI Latency Timer. **Not Supported.**	Yes	No	0

Table 4-10. (PCIHTR; 0Eh) PCI Header Type Register

Bit	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies the layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	No	0
7	Header Type. A value of 1 indicates multiple functions. A value of 0 indicates a single function.	Yes	No	0

Table 4-11. (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST) Register

Bit	Description	Read	Write	Value after Reset
7:0	Built-In Self Test. A value of 0 indicates the device has passed its test. **Not Supported.**	Yes	No	0

Table 4-12. (PCIBAR0; 10h) PCI Base Address Register for Memory Accesses to Local Configuration Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 0.*	Yes	No	0
2:1	Location of register: 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** ***Note:*** *Hardcoded to 0.*	Yes	No	0
3	Prefetchable. A value of 1 indicates no side effect on reads. ***Note:*** *Hardcoded to 0.*	Yes	No	0
6:4	Memory Base Address. Memory base address for access to local configuration registers (default 128 bytes). ***Note:*** *Hardcoded to 0.*	Yes	No	0
31:7	Memory Base Address. Memory base address for access to local configuration registers	Yes	Yes	0

Note: *PCIBAR0 can be enabled or disabled using bits [13:12] in the CNTRL register.*

Table 4-13. (PCIBAR1; 14h) PCI Base Address Register for I/O Accesses to Local Configuration Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 1.*	Yes	No	1h
1	***Reserved***.	Yes	No	0
6:2	I/O Base Address. Base address for I/O access to local configuration registers (default 128 bytes*).* ***Note:*** *Hardcoded to 0.*	Yes	No	0
31:7	I/O Base Address. Base address for I/O access to local configuration registers.	Yes	Yes	0

Note: *PCIBAR1 can be enabled or disabled using bits [13:12] in the CNTRL register.*

Table 4-14. (PCIBAR2; 18h) PCI Base Address Register for Memory Access to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS0RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS0RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). A value of 1 indicates no side effects on reads. This bit reflects the value of bit 3 in the LAS0RR register, only provides status to the system, and has no effect on the operation of the PCI 9050-1. The associated Bus Region Descriptor Register (LAS0BRD) controls prefetching features of this address space. (Specified in LAS0RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to the local address space.	Yes	Yes	0

Note: *PCIBAR2 can be enabled or disabled by setting or clearing bit 0 in the LAS0BA register.*

Table 4-15. (PCIBAR3; 1Ch) PCI Base Address Register for Memory Access to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS1RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS1RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). A value of 1 indicates no side effects on reads. This bit reflects the value of bit 3 in the LAS1RR register, only provides status to the system, and has no effect on the operation of the PCI 9050-1. The associated Bus Region Descriptor Register (LAS1BRD) controls prefetching features of this address space. (Specified in LAS1RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to the local address space.	Yes	Yes	0

Note: *PCIBAR3 can be enabled or disabled by setting or clearing bit 0 in the LAS1BA register.*

Table 4-16. (PCIBAR4; 20h) PCI Base Address Register for Memory Access to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS2RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS2RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS2RR register, only provides status to the system, and has no effect on the operation of the PCI 9050-1. The associated Bus Region Descriptor Register (LAS2BRD) controls prefetching features of this address space. (Specified in LAS2RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to the local address space.	Yes	Yes	0

Note: *PCIBAR4 can be enabled or disabled by setting or clearing bit 0 in the LAS2BA register.*

Table 4-17. (PCIBAR5; 24h) PCI Base Address Register for Memory Access to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS3RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS3RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS3RR register, only provides status to the system, and has no effect on the operation of the PCI 9050-1. The associated Bus Region Descriptor Register (LAS3RR) controls prefetching features of this address space. (Specified in LAS3RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to the local address space.	Yes	Yes	0

Note: *PCIBAR5 can be enabled or disabled by setting or clearing bit 0 in the LAS3BA register.*

Table 4-18. (PCICIS; 28h) PCI Cardbus CIS Pointer Register

Bit	Description	Read	Write	Value after Reset
31:0	Cardbus Information Structure Pointer for PCMCIA. **Not Supported.**	Yes	No	0

Table 4-19. (PCISVID; 2Ch) PCI Subsystem Vendor ID

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID. (Unique add-in board Vendor ID.)	Yes	EEPROM	0

Table 4-20. (PCISID; 2Eh) PCI Subsystem ID

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem ID. (Unique add-in board Device ID.)	Yes	EEPROM	0

Table 4-21. (PCIERBAR; 30h) PCI Expansion ROM Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. A value of 1 indicates the device accepts accesses to the expansion ROM address. A value of 0 indicates the device does not accept accesses to expansion ROM space.	Yes	Yes	0
10:1	***Reserved***.	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	0

Table 4-22. (PCIILR; 3Ch) PCI Interrupt Line Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Indicates to which system interrupt controller(s) input the interrupt line of the device is connected.	Yes	Yes	0

Table 4-23. (PCIIPR; 3Dh) PCI Interrupt Pin Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Pin Register. Indicates interrupt pin device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	EEPROM	1h

Table 4-24. (PCIMGR; 3Eh) PCI Min_Gnt Register

Bit	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Specifies needed length of Burst period for the device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

Table 4-25. (PCIMLR; 3Fh) PCI Max_Lat Register

Bit	Description	Read	Write	Value after Reset
7:0	Max_Lat. Specifies how often the device must gain access to the PCI bus. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

4.3 Local Configuration Registers

Table 4-26 (LAS0RR; 00h) Local Address Space 0 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates Local address space 0 maps into PCI memory space. A value of 1 indicates address space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, a value of 1 indicates that reads are prefetchable (Bit has no effect on the operation of the PCI 9050-1, but is for system status.) If mapped into I/O space, bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to local bus space 0. Each of the bits correspond to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration Register 18h). Default is 1 MB.	Yes	Yes	FF0000
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 4-27. (LAS1RR; 04h) Local Address Space 1 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates Local address space 1 maps into PCI memory space. A value of 1 indicates address space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, a value of 1 indicates that reads are prefetchable. If mapped into I/O space, bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to local bus space 1. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 1Ch).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 4-28. (LAS2RR; 08h) Local Address Space 2 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates Local address space 2 maps into PCI memory space. A value of 1 indicates address space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, a value of 1 indicates that reads are prefetchable. If mapped into I/O space, bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to local bus space 2. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with Configuration register 20h).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 4-29. (LAS3RR; 0Ch) Local Address Space 3 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. A value of 0 indicates local address space 3 maps into PCI memory space. A value of 1 indicates address space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, a value of 1 indicates that reads are prefetchable. If mapped into I/O space, bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to local bus space 3. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 24h).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 4-30. (EROMRR; 10h) Expansion ROM Range Register

Bit	Description	Read	Write	Value after Reset
10:0	Unused.	Yes	No	0
27:11	Specifies PCI address bits used to decode PCI to local bus expansion ROM. Each of the bits corresponds to an Address bit. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 30h). Default is 64 KB.	Yes	Yes	11111111111100000
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 4-31. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 0 Enable. A value of 1 enables Decode of PCI addresses for Direct Slave access to local space 0. A value of 0 disables Decode.	Yes	Yes	1
1	Unused.	Yes	Yes	0
3:2	If local space 0 is mapped into Memory space, bits are not used. If mapped into I/O space, bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 0 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in PCI 9050-1.)	Yes	No	0

Table 4-32. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 1 Enable. A value of 1 enables Decode of PCI addresses for Direct Slave access to local space 1. A value of 0 disables Decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If local space 1 is mapped into Memory space, bits are not used. If mapped into I/O space, bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 1 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in PCI 9050-1.)	Yes	No	0

Table 4-33. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 2 Enable. A value of 1 enables Decode of PCI addresses for Direct Slave access to local space 2. A value of 0 disables Decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If local space 2 is mapped into Memory space, bits are not used. If mapped into I/O space, bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 2 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in PCI 9050-1.)	Yes	No	0

Table 4-34. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 3 Enable. A value of 1 enables Decode of PCI addresses for Direct Slave access to local space 3. A value of 0 disables Decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If local space 3 is mapped into Memory space, bits are not used. If mapped into I/O space, bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 3 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in PCI 9050-1.)	Yes	No	0

Table 4-35. (EROMBA; 24h) Expansion ROM Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
10:0	Unused.	Yes	No	0
27:11	Remap of PCI Expansion ROM space into a Local Address Space. The bits in this register remap (replace) the PCI address bits used in decode as the local address bits. Default base is 1 MB (above default Local Address Space 0).	Yes	Yes	00000001000000000
31:28	Unused. (Local address bits [31:28] do not exist in PCI 9050-1.)	Yes	No	0

Table 4-36. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. A value of 1 indicates bursting is enabled. A value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. A value of 1 indicates READY input enabled. A value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. A value of 1 indicates BTERM Input is enabled. A value of 0 indicates BTERM Input is disabled. Burst length limited to 4 Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Used only if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. A value of 1 prefetches up to the number of Lwords specified in the prefetch count. A value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. A value of 1 indicates Big Endian. A value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. A value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. A value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until the end of the cycle (0-3).	Yes	Yes	0

Table 4-37. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. A value of 1 indicates bursting is enabled. A value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. A value of 1 indicates BTERM Input is enabled. A value of 0 indicates BTERM Input is disabled. Burst length limited to 4 Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Used only if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. A value of 1 prefetches up to the number of Lwords specified in the prefetch count. A value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. A value of 1 indicates Big Endian. A value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. A value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. A value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until the end of the cycle (0-3).	Yes	Yes	0

Table 4-38. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. A value of 1 indicates bursting is enabled. A value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. A value of 1 indicates BTERM Input is enabled. A value of 0 indicates BTERM Input is disabled. Burst length limited to 4 Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Used only if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. A value of 1 prefetches up to the number of Lwords specified in the prefetch count. A value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. A value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until the end of the cycle (0-3).	Yes	Yes	0

Table 4-39. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. A value of 1 indicates bursting is enabled. A value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. A value of 1 indicates BTERM Input is enabled. A value of 0 indicates BTERM Input is disabled. Burst length limited to 4 Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Used only if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. A value of 1 prefetches up to the number of Lwords specified in the prefetch count. A value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. A value of 1 indicates Big Endian. A value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. A value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. A value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe Is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until the end of the cycle (0-3).	Yes	Yes	0

Table 4-40. (EROMBRD; 38h) Expansion ROM Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. A value of 1 indicates bursting is enabled. A value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. A value of 1 indicates BTERM Input is enabled. A value of 0 indicates BTERM Input is disabled. Burst length limited to 4 Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Used only if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. A value of 1 prefetches up to the number of Lwords specified in the prefetch count. A value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	0
24	Byte Ordering. A value of 1 indicates Big Endian. A value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. A value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. A value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until the end of the cycle (0-3).	Yes	Yes	0

Table 4-41. (CS0BASE; 3Ch) Chip Select 0 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 0 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 0. Write zeroes in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first “1” found defines the size. The remaining most significant bits, excluding the first “1” found, define the base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 4-42. (CS1BASE; 40h) Chip Select 1 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 1 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 1. Write zeroes in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first “1” found defines the size. The remaining most significant bits, excluding the first “1” found, define the base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 4-43. (CS2BASE; 44h) Chip Select 2 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 2 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 2. Write zeroes in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first “1” found defines the size. The remaining most significant bits, excluding the first “1” found, define the base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 4-44. (CS3BASE; 48h) Chip Select 3 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 3 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 3. Write zeroes in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first “1” found defines the size. The remaining most significant bits, excluding the first “1” found, define the base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 4-45. (INTCSR; 4Ch) Interrupt Control/Status Register

Bit	Description	Read	Write	Value after Reset
0	Local Interrupt 1 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
1	Local Interrupt 1 Polarity. A value of 1 indicates Active high. A value of 0 indicates Active low.	Yes	Yes	0
2	Local Interrupt 1 Status. A value of 1 indicates Interrupt active. A value of 0 Interrupt not active.	Yes	No	0
3	Local Interrupt 2 Enable. A value of 1 indicates enabled. A value of 0 indicates disabled.	Yes	Yes	0
4	Local Interrupt 2 Polarity. A value of 1 indicates Active high. A value of 0 indicates Active low.	Yes	Yes	0
5	Local Interrupt 2 Status. A value of 1 indicates Interrupt active. A value of 0 Interrupt not active.	Yes	No	0
6	PCI Interrupt Enable. A value of 1 enables PCI interrupt.	Yes	Yes	0
7	Software Interrupt. A value of 1 generates interrupt.	Yes	Yes	0
31:8	Unused.	Yes	No	0

Table 4-46. (CNTRL; 50h) User I/O, PCI Target Response, EEPROM, Initialization Control Register

Bit	Description	Read	Write	Value after Reset
0	User I/O 0 or WAITO# Pin Select. This bit selects the function of the USER0/WAITO# pin. A value of 1 indicates pin is WAITO#. A value of 0 indicates pin is USER0.	Yes	Yes	0
1	User I/O 0 Direction. A value of 0 indicates Input. A value of 1 indicates Output. The pin is always an output if the WAITO# function is selected.	Yes	Yes	0
2	User I/O 0 Data. If programmed as an output, writing a value of 1 causes the corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
3	User I/O 1 or LLOCK Pin Select. This bit selects the function of the USER1/LLOCKo# pin. A value of 1 indicates pin is LLOCKo#. A value of 0 indicates pin is USER1.	Yes	Yes	0
4	User I/O 1 Direction. A value of 0 indicates Input. A value of 1 indicates Output. The pin is always an output if the LLOCK function is selected.	Yes	Yes	0
5	User I/O 1 Data. If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
6	User I/O 2 or CS2 Pin Select. This bit selects the function of the USER2/CS2# pin. A value of 1 indicates pin is CS2#. A value of 0 indicates pin is USER2.	Yes	Yes	0
7	User I/O 2 Direction. A value of 0 indicates Input. A value of 1 indicates Output. The pin is always an output if the CS2 function is selected.	Yes	Yes	0
8	User I/O 2 Data. If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
9	User I/O 3 or CS3 Pin Select. This bit selects the function of the USER3/CS3# pin. A value of 1 indicates pin is CS3#. A value of 0 indicates pin is USER3.	Yes	Yes	0
10	User I/O 3 Direction. A value of 0 indicates Input. A value of 1 indicates Output. The pin is always an output if the CS3 function is selected.	Yes	Yes	0
11	User I/O 3 Data. If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
13:12	PCI Configuration Base Address Register (PCIBAR) Enables. 00 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled. 01 = PCIBAR0 (Memory) only. 10 = PCIBAR1 (I/O) only. 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled.	Yes	Yes	00
14	PCI Read Mode. A value of 1 immediately disconnects for a read. Prefetch the data into the direct slave read FIFO. Returns data when PCI read cycle is reapplied (PCI 2.1 compatible). A value of 0 de-asserted TRDY# until read data is available.	Yes	Yes	0
15	PCI Read with Write Flush Mode. A value of 1 flushes a pending read cycle if a write cycle is detected. A value of 0 does not effect pending reads when a write cycle occurs (PCI 2.1 compatible).	Yes	Yes	0
16	PCI Read No Flush Mode. A value of 1 does not flush the read FIFO if the PCI read cycle completes (cached read mode). A value of 0 flushes the read FIFO if a PCI read cycle completes.	Yes	Yes	0
17	PCI Read No Write Mode. A value of 1 forces retry on writes if a read is pending. A value of 0 allows a write to occur while a read is pending.	Yes	Yes	0

Table 4-46. (CNTRL; 50h) User I/O, PCI Target Response, EEPROM, Initialization Control Register (continued)

Bit	Description	Read	Write	Value after Reset
18	PCI Write Mode. A value of 1 disconnects if the write FIFO becomes full. A value of 0 de-asserts TRDY# until space is available in the direct slave write FIFO.	Yes	Yes	0
22:19	PCI Target Retry Delay Clocks. The number of PCI clocks (multiplied by 8) after the beginning of a direct slave cycle until a retry is issued. Only valid for read cycles if bit 14 is low. Only valid for write cycles if bit 17 is low.	Yes	Yes	0
23	Direct Slave Lock Enable. A value of 1 enables PCI direct slave locked sequences. A value of 0 disables direct slave locked sequences.	Yes	Yes	0
24	EEPROM Clock for Local or PCI Bus Reads or Writes to EEPROM. Toggling this bit generates an EEPROM clock. (Refer to the manufacturer's data sheet for the particular EEPROM being used.)	Yes	Yes	0
25	EEPROM Chip Select. For local or PCI bus reads or writes to EEPROM, setting this bit to 1 provides the EEPROM chip select.	Yes	Yes	0
26	Write Bit to EEPROM. For writes, this output bit is the input to the EEPROM. Clocked into the EEPROM by the EEPROM clock.	Yes	Yes	0
27	Read EEPROM Data Bit. For reads, this input bit is the output of the EEPROM. Clocked out of the EEPROM by the EEPROM clock.	Yes	No	—
28	EEPROM Valid. A value of 1 indicates a valid EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When this bit is 0, writing a value of 1 causes the PCI 9050-1 to reload the local configuration registers from EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. A value of 1 resets the PCI 9050-1 and issues a reset to the local bus. The contents of the PCI and local configuration registers will not be reset.	Yes	Yes	0
31	Mask Revision.	Yes	No	0

5. PIN DESCRIPTION

5.1 Pin Summary

Table 5-2 through Table 5-5 describe the PCI 9050-1 pins:

- Power and ground
- EEPROM interface
- PCI system bus interface
- Local bus support

Table 5-6 through Table 5-8 describe the local bus data transfer pins:

- Mode independent
- Non-Multiplexed mode
- Multiplexed mode

Unspecified pins are no connects (NC).

For a visual view of the chip pin layout, refer to Figure 7-3, “PCI 9050-1 Pin Out,” in Section 7, “Package Specifications.”

Table 5-1 lists the abbreviations used in this section to represent the various pin types.

Table 5-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output pin
I	Input pin only
O	Output pin only
TS	Tri-state pin
OC	Open collector pin
TP	Totem pole pin
STS	Sustained tri-state pin, driven high for one CLK before float

All local bus inputs (pin type I) internally connect to Vcc through a 10k ohm, pull-up resistor.

Table 5-2. Power and Ground Pin Description (23 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	99	Test pin. Pull high for test. Pull low for normal operation. When TEST is pulled high, all outputs except RD# (pin 126) are placed in tri-state. RD# provides a NAND-TREE output when TEST is pulled high.
NC	Spare	2	N/A	45, 67	Unused.
VDD	Power	10	I	1, 10, 27, 41, 50, 66, 81, 103, 121, 146	Power supply pins (5 V). Liberal .01 µF to .1 µF decoupling capacitors should be placed near the PCI 9050-1.
VSS	Ground	10	I	9, 26, 40, 51, 65, 80, 104, 120, 147, 160	Ground pins.

Table 5-3. EEPROM Interface Pin Description (4 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	EEPROM Chip Select	1	O TP 6 mA	142	EEPROM Chip Select.
EEDO	EEPROM Data Out	1	I	143	EEPROM Read Data.
EEDI	EEPROM Data In	1	O TP 6 mA	145	EEPROM Write Data.
EESK	EEPROM Serial Data Clock	1	O TP 6 mA	144	EEPROM Clock.

Table 5-4. PCI System Bus Interface Pin Description (49 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS 6 mA	150-157, 2-8, 11, 23-25, 28-32, 34-39, 42-43	Multiplexed on the same PCI pins. A bus transaction consists of an address phase, followed by one or more data phases. The PCI 9050-1 supports both read and write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	158, 12, 22, 33	Multiplexed on the same PCI pins. During the address phase of a transaction, defines the bus command. During the data phase, used as Byte Enables. For additional information, refer to PCI Specification v2.1.
CLK	Clock	1	I	149	Provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	O STS 6 mA	16	When actively driven, indicates the driving device has decoded its address as the target of the current access.
FRAME#	Cycle Frame	1	I	13	Driven by the current master to indicate the beginning and duration of an access. Asserted to indicate a bus transaction is beginning. While asserted, data transfers continue. When de-asserted, the transaction is in the final data phase.
IDSEL	Initialization Device Select	1	I	159	Chip select used during configuration read and write transactions.
INTA#	Interrupt A	1	O OC 6 mA	44	Requests an interrupt.
IRDY#	Initiator Ready	1	I	14	Indicates the ability of the initiating agent (bus master) to complete the current data phase of the transaction.
LOCK#	Lock	1	I	18	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS 6 mA	21	Indicates even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.
PERR#	Parity Error	1	O STS 6 mA	19	Indicates only the reporting of data parity errors during all PCI transactions, except during a Special Cycle.
RST#	Reset	1	I	148	Brings PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	Systems Error	1	O OC 6 mA	20	For reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	O STS 6 mA	17	Indicates the current target is requesting the master to stop the current transaction.
TRDY#	Target Ready	1	O STS 6 mA	15	Indicates the ability of the target agent (selected device) to complete the current data phase of the transaction.

Table 5-5. Local Bus Support Pin Descriptions (14 Pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
MODE	Bus Mode	1	I	68	Selects the bus operation mode of the PCI 9050-1. 1 = Multiplexed Bus mode 0 = Non-Multiplexed mode
LINTi1	Local Interrupt 1 In	1	I	137	When asserted, causes a PCI interrupt. Polarity is determined by the INTCSR configuration register.
LINTi2	Local Interrupt 2 In	1	I	136	When asserted, causes a PCI interrupt. Polarity is determined by the INTCSR configuration register.
LCLK	Local Bus Clock	1	I	135	Local clock up to 33 MHz, and may be asynchronous to the PCI clock.
LHOLD	Hold Request	1	I	134	Asserted by a local bus master to request use of the local bus.
LHOLDA	Hold Acknowledge	1	O TP 6 mA	133	Asserted by the PCI 9050-1 to grant control of the local bus to a local bus master. When the PCI 9050-1 needs the local bus, it signals a preempt by de-asserting LHOLDA.
LRESET#	Local Reset Out	1	O TP 6 MA	132	Local bus reset output, asserted when the PCI 9050-1 is reset, and used to reset devices on the local bus.
BCLKO	BCLK Out	1	O TP 6 mA	63	Indicates a buffered version of the PCI clock for optional use by the local bus.
CS[1:0]#	Chip Selects	2	O TS 6 mA	131, 130	General purpose chip selects. The base and range of each may be programmed in the configuration registers.
USER0/WAITO#	User I/O 0 or WAIT Out	1	I/O TS 6 mA	138	Can be programmed to be a configurable User I/O pin, USER0, or the local bus WAIT out pin. WAITO# is asserted when wait states are caused by the internal wait-state generator. Serves as an output to provide ready-out status.
USER1/LLOCKo#	User I/O 1 or LLOCK Out	1	I/O TS 6 mA	139	Can be programmed to be a configurable User I/O pin, USER1, or the local bus LLOCK out pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the local bus to lock resources.
USER2/CS2#	User I/O 2 or CS2 Out	1	I/O TS 6 mA	140	Can be programmed to be a configurable User I/O pin, USER1, or as the Chip Select 2 output pin, CS2#.
USER3/CS3#	User I/O 3 or CS3 Out	1	I/O TS 6 mA	141	Can be programmed to be a configurable User I/O pin, USER3, or as the Chip Select 3 output pin, CS3#.

Table 5-6. Local Bus Data Transfer Pins Description (Mode Independent) (7 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	O TS 24 mA	123	Indicates valid address and the start of a new bus access. Asserted for the first clock of a bus access.
ALE	Address Latch Enable	1	O TS 6 mA	64	Asserted during the address phase and de-asserted before the data phase.
LW/R	Write/Read	1	O TS 6 mA	127	Asserted high for writes and low for reads.
BLAST#	Burst Last	1	O TS 6 mA	124	Signal driven by the current local bus master to indicate the last transfer in a bus access.
RD#	Read Strobe	1	O TS 24 mA	126	General purpose read strobe. The timing is controlled by the current Bus Region Descriptor Register.
WR#	Write Strobe	1	O TS 24 mA	125	General purpose write strobe. The timing is controlled by the current Bus Region Descriptor Register.
LRDYi#	Local Ready In	1	I	128	Local ready input indicates read data is on the local bus, or that write data is accepted. Used in conjunction with the programmable wait-state generator.

Table 5-7. Local Bus Data Transfer Pins Description (Non-Multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If disabled through the PCI 9050-1 configuration registers, the PCI 9050-1 bursts up to four transactions, Lword transfer depends upon the bus width and type. If enabled, the PCI 9050-1 continues to burst until BTERM# input is asserted. Ready input which breaks up a burst cycle and causes another address cycle to occur. Also used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. Increments during bursts to indicate successive data cycles.
LAD[31:0]	Data Bus	32	I/O TS 6 mA	52-62, 69-79, 82-91	Carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration. 8-bit = LAD[7:0] 16-bit = LAD[15:0] 32-bit = LAD[31:0]
LBE[3:0]#	Byte Enables	4	O TS 24 mA	46-49	Byte enables are encoded based on configured bus width: **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle. • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE3#, LBE1#, and LBE0# are encoded to provide BHE#, LA1, and BLE#. • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE1# and LBE0# are encoded to provide LA1 and LA0. • LBE3# Unused • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

Table 5-8. Local Bus Data Transfer Pins Description (Multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If disabled through the PCI 9050-1 configuration registers, the PCI 9050-1 bursts up to four transactions, Lword transfer depends upon the bus width and type. If enabled, the PCI 9050-1 continues to burst until BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. Also used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. During bursts LA[27:2] increments to indicate successive data cycles.
LAD[31:0]	Address/Data Bus	32	I/O TS 6 mA	52-62, 69-79, 82-91	During the address phase, the bus carries the upper 26 bits of the 28-bit physical address bus. During the data phase, the bus carries 32-, 16-, or - bit data quantities, depending on bus width configuration. 8-bit = LAD[7:0] 16-bit = LAD[15:0] 32-bit = LAD[31:0]
LBE[3:0]#	Byte Enables	4	O TS 24 mA	46-49	Byte enables are encoded based upon configured bus width: **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle. • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE3#, LBE1#, and LBE0# are encoded to provide BHE#, LA1, and BLE#. • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE1# and LBE0# are encoded to provide LA1and LA0. • LBE3# Unused • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

This page intentionally left blank.

6. ELECTRICAL AND TIMING SPECIFICATIONS

6.1 General Specifications

Table 6-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage temperature	-65 to +150 °C
Ambient temperature with power applied	-55 to +125 °C
Supply voltage to ground	-0.5 to +7.0 V
Input voltage (VIN)	VSS -0.5 V VDD +0.5 V
Output voltage (VOUT)	VSS -0.5 V VDD +0.5 V

Table 6-2. Operating Ranges

Ambient Temperature	Junction Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0 to +70 °C	115 °C Maximum	5 V ±5%	Min = VSS Max = VDD

Table 6-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0 V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0 V f = 1 MHz	Output	10	pF

Table 6-4. Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -4.0 mA	2.4	—	V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Tables	—	0.4	V
VIH	Input High Level	—	—	2.0	—	V
VIL	Input Low Level	—	—	—	0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
IOZ	Tri-State Output Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
ICC	Power Supply Current	VDD = 5.25 V, PCLK = LCLK = 33 MHz		—	130	mA

6.2 Local Inputs

Local Bus Input Setup and Hold Times:

- Hold time = 2 ns min
- Setup time = 8 ns max

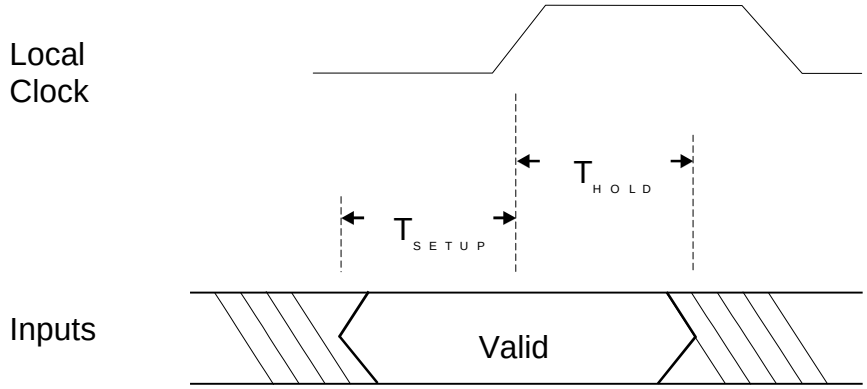


Figure 6-1. PCI 9050-1 Local Input Setup and Hold Waveform

Table 6-5. Clock Frequencies

Frequency	Min	Max
Local Clock Input	0	40 MHz
PCI Clock Input	0	33 MHz

6.3 Local Outputs

Table 6-6. AC Electrical Characteristics (Local Outputs) Measured over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, VCC = 5.0 ± 5%	$T_{VALID\ (MIN)\ NSEC}$ (HOLD)	$T_{VALID\ NSEC}$ Typical min/max	$T_{VALID\ (MAX)\ NSEC}$ (WORST CASE)
LHOLDA	3	—	9
ADS#	3	8	10
BLAST#	5	9	16
LBE[3:0]#	4	10	15
LW/R#	4	7	12
LAD[31:0]	5	11	16
LA[27:2]	5	10	14
LRESET#	5*	14	17*
RD#	7	16	27
ALE	4	8/23	12
WR#	4	8	13
BCLKO	2	7	8
USER0/WAITO#	4*	5 PCLK/8	12*
USER1/LLOCKo#	4*	5 PCLK/8	12*
USER2/CS2#	5*	5 PCLK/11	17*
USER3/CS3#	5*	5 PCLK/11	17*
CS[1:0]#	4	11	17

Note: *The values followed with an asterisk (*) are referenced from the PCI side.*

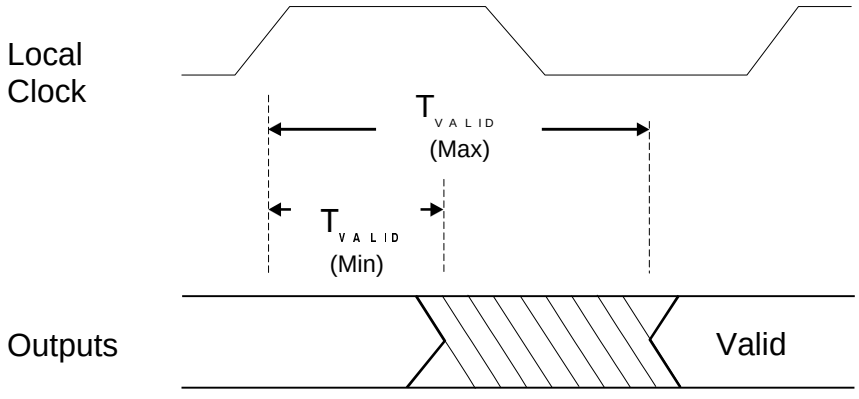


Figure 6-2. PCI 9050-1 Local Output Delay

This page intentionally left blank.

7. PACKAGE SPECIFICATIONS

7.1 Package Mechanical Dimensions

For 160-pin PQFP

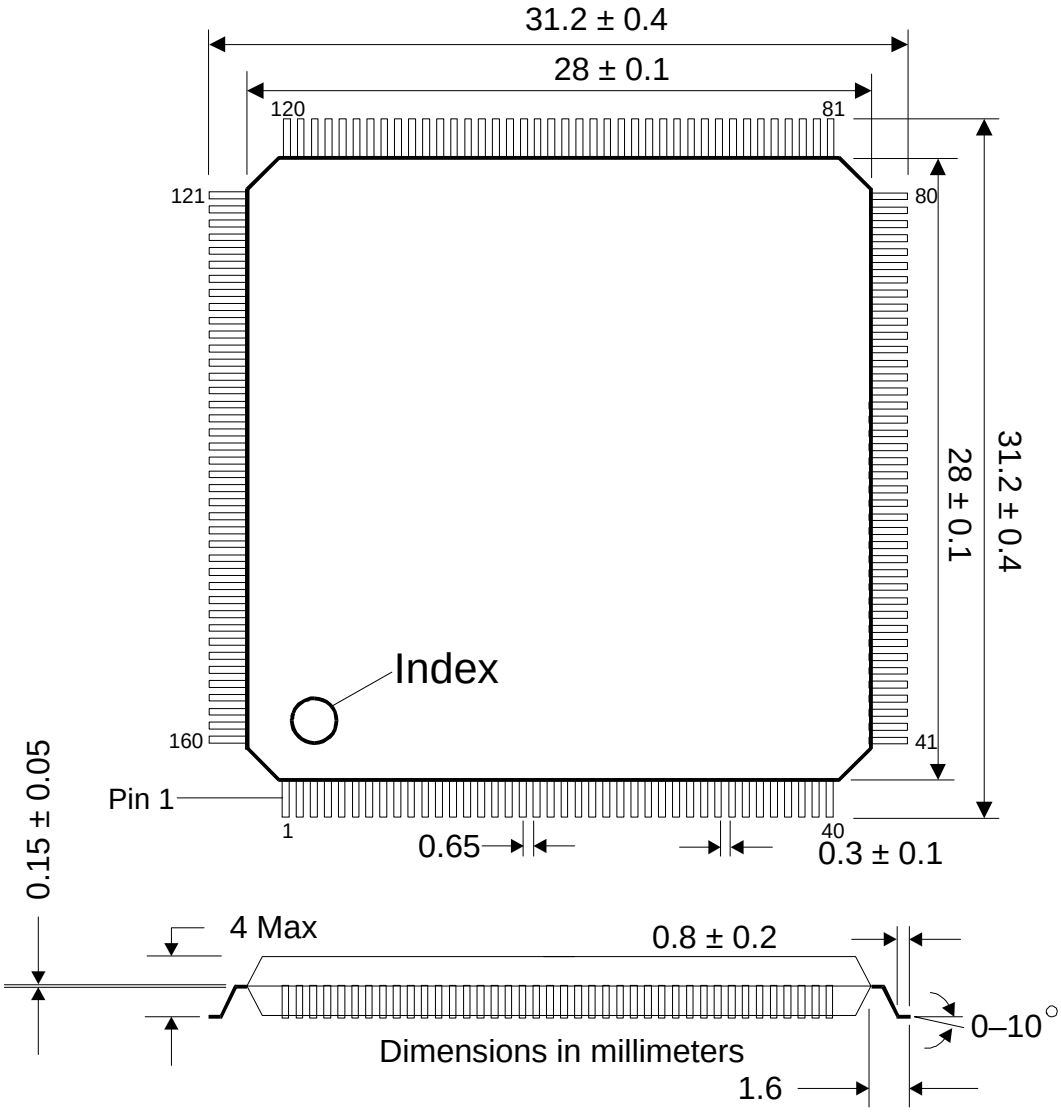


Figure 7-1. Package Mechanical Dimensions

7.2 Typical Adapter Block Diagram

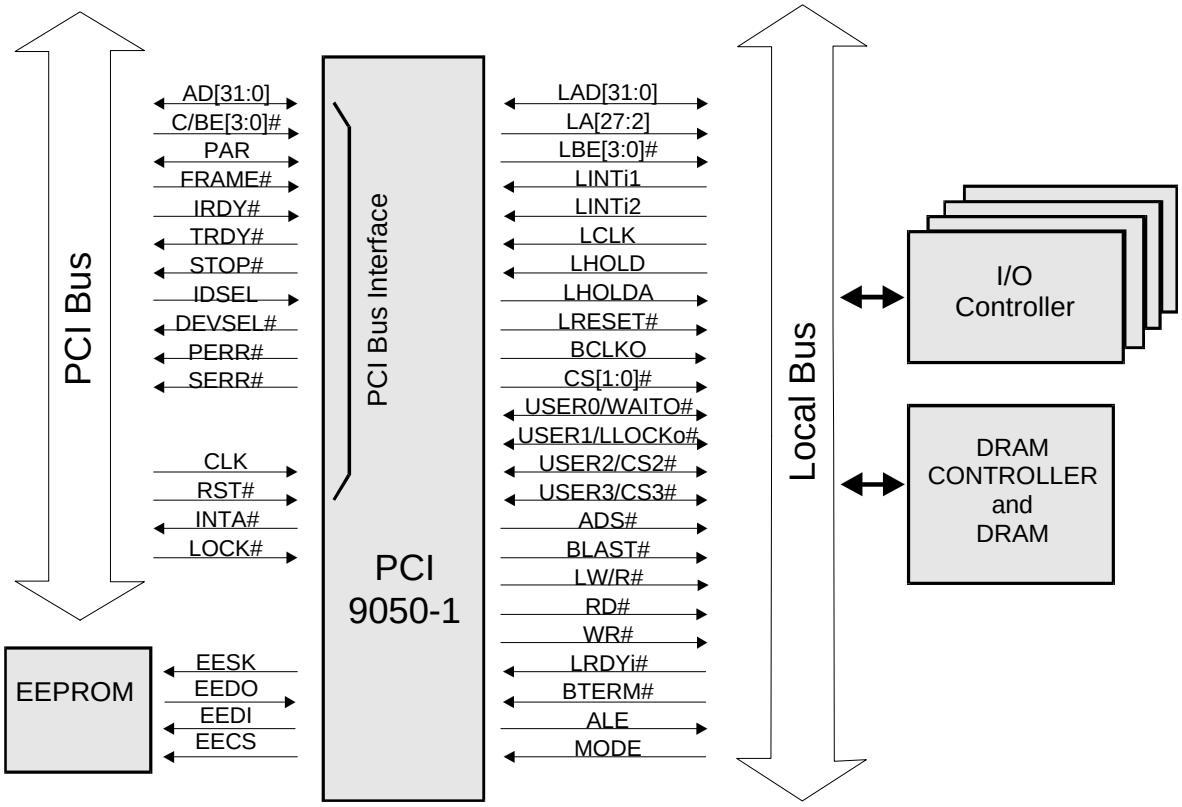


Figure 7-2. PCI 9050-1 Block Diagram

7.3 PCI 9050-1 Pin Out

Refer to Section 5, “Pin Description,” for a complete description of each pin.

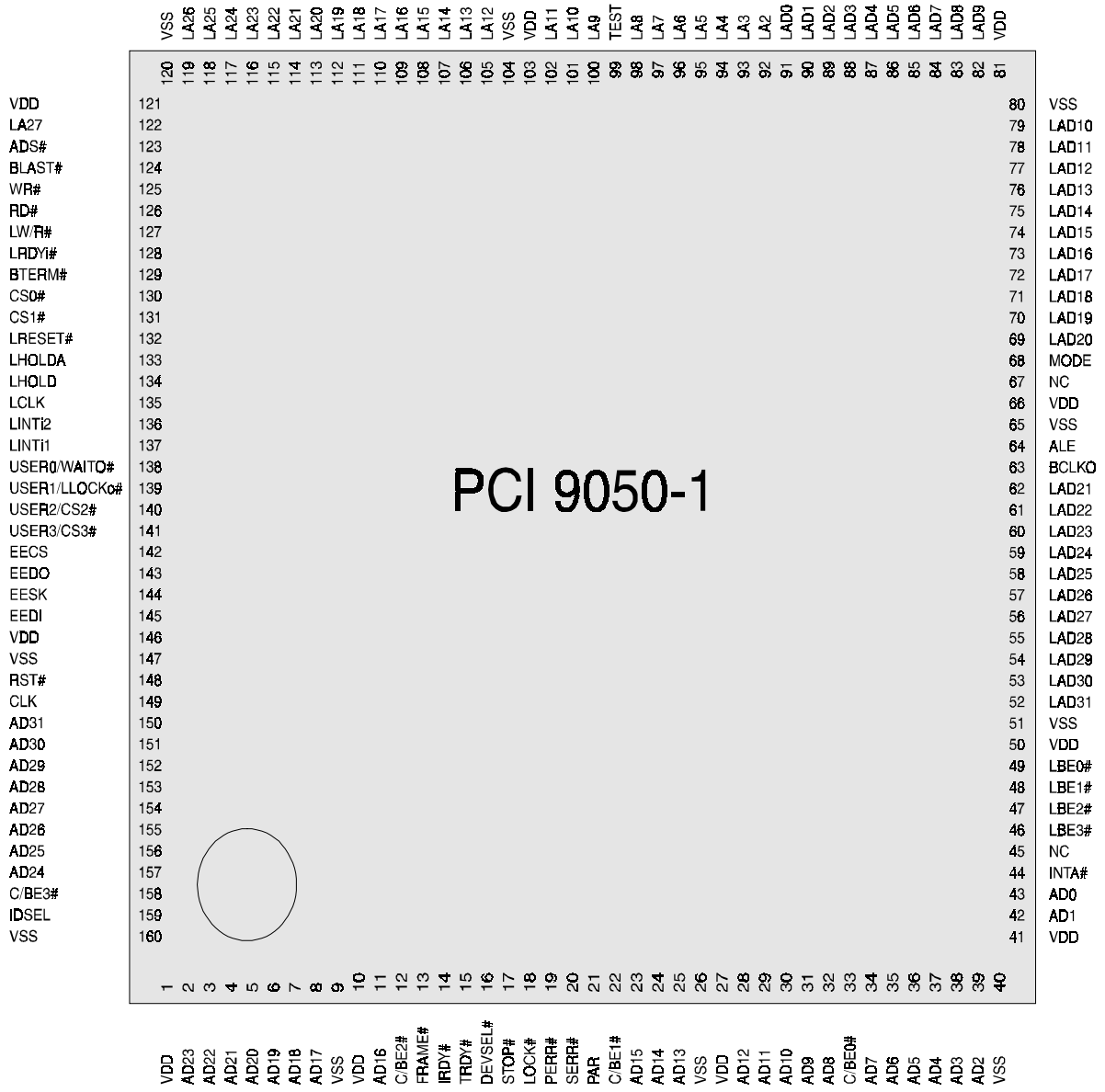
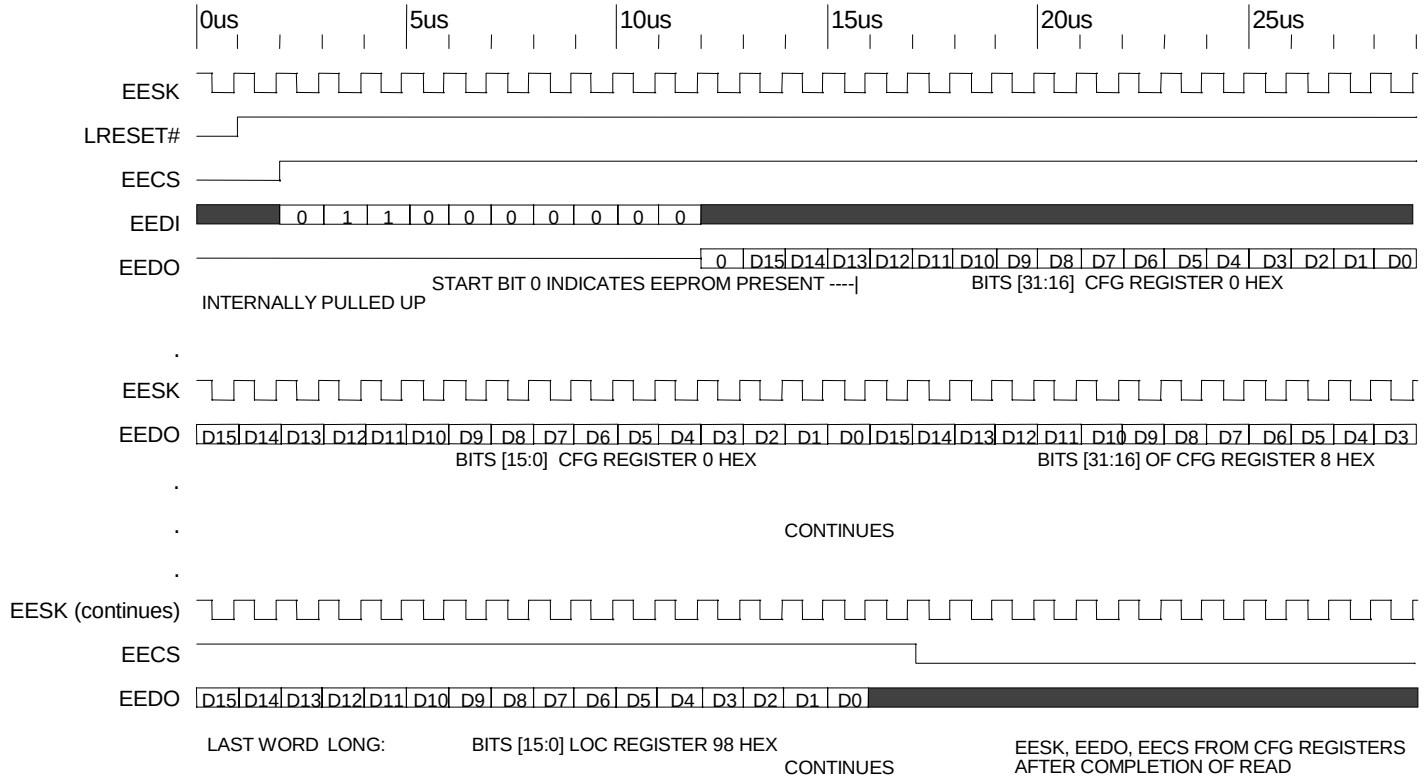


Figure 7-3. PCI 9050-1 Pin Out

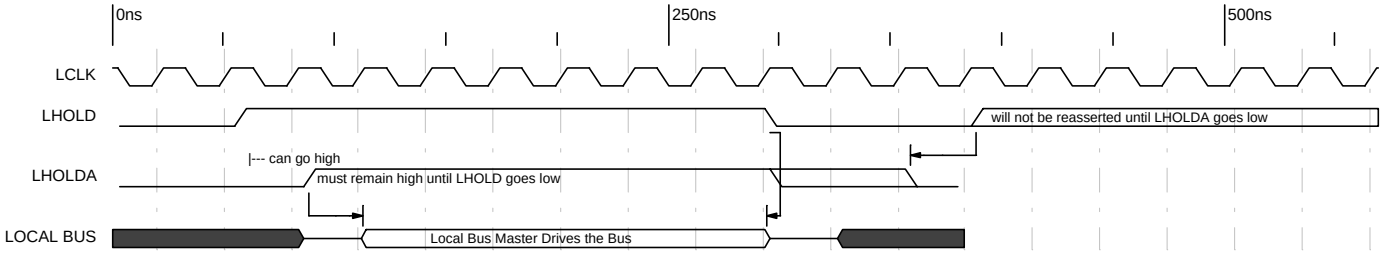
This page intentionally left blank.

8. TIMING DIAGRAMS

8.1 PCI 9050-1 Initialization

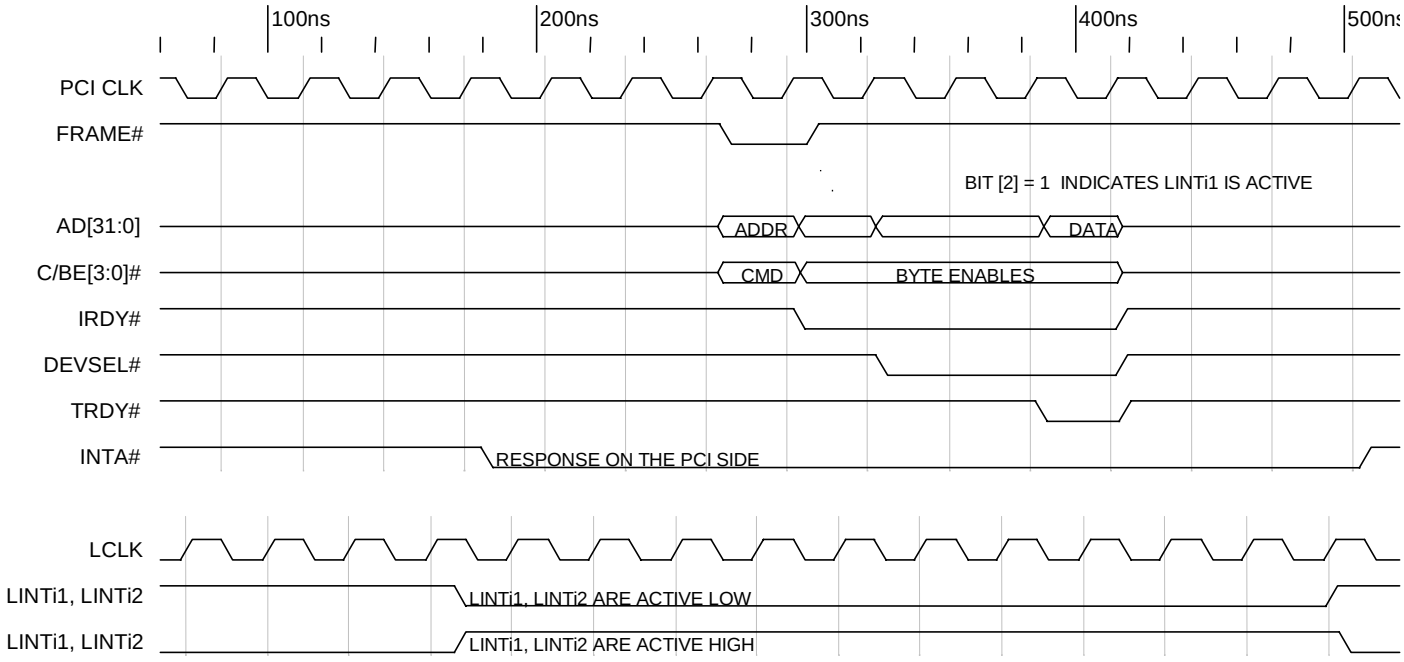


Timing Diagram 8-1. Initialization from Serial EEPROM

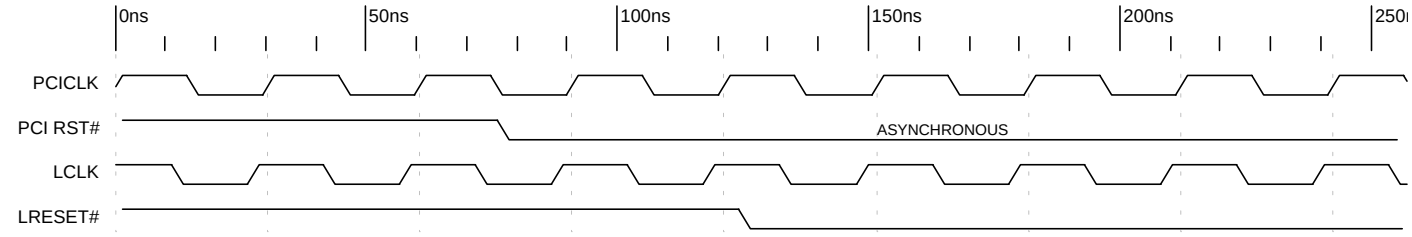


Note: *PCI 9050-1 always gives up bus between different Direct Slave accesses.*

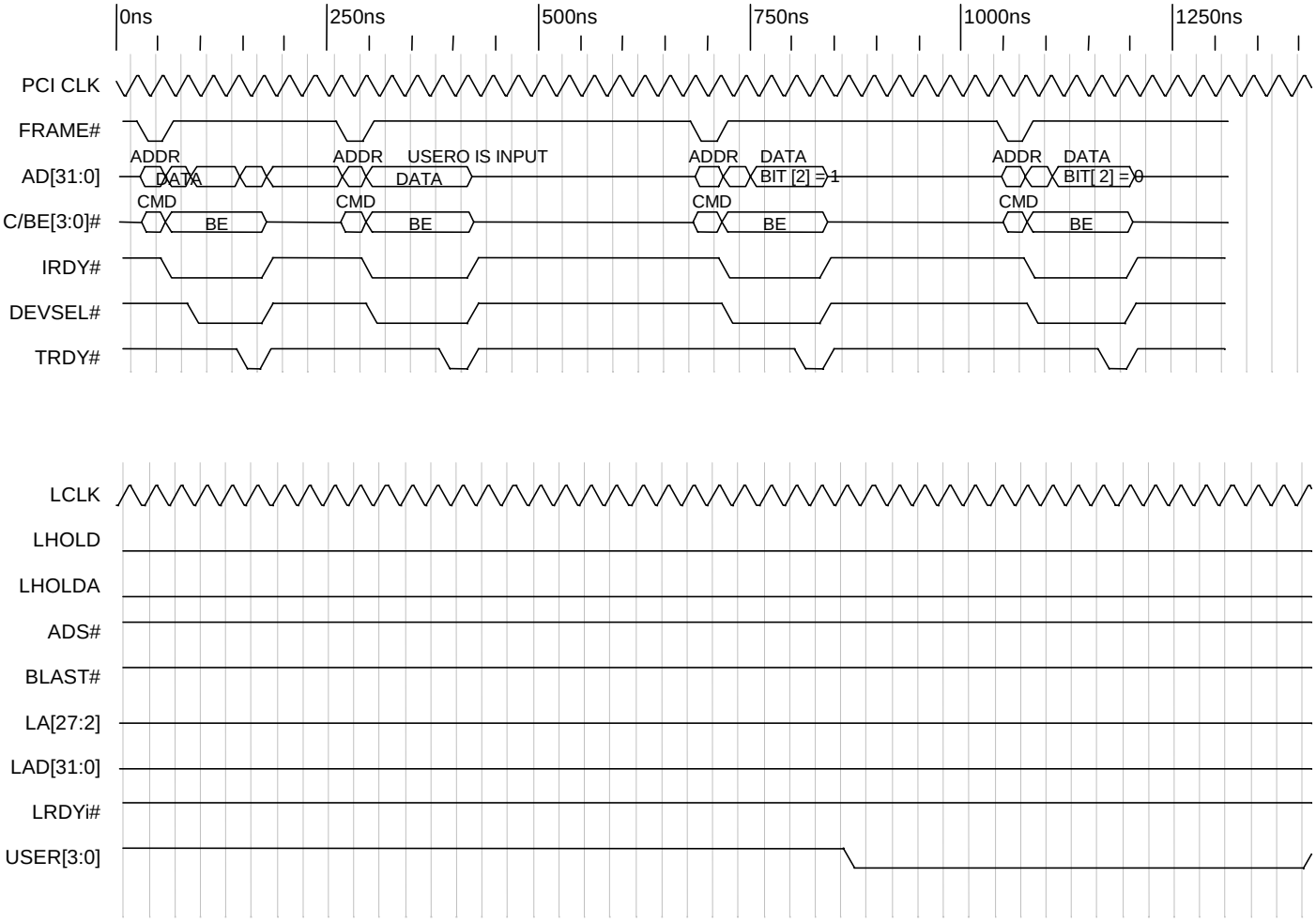
Timing Diagram 8-2. PCI 9050-1 Local Bus Arbitration



Timing Diagram 8-3. Local LINTi1# Input Asserting PCI Output INTA#

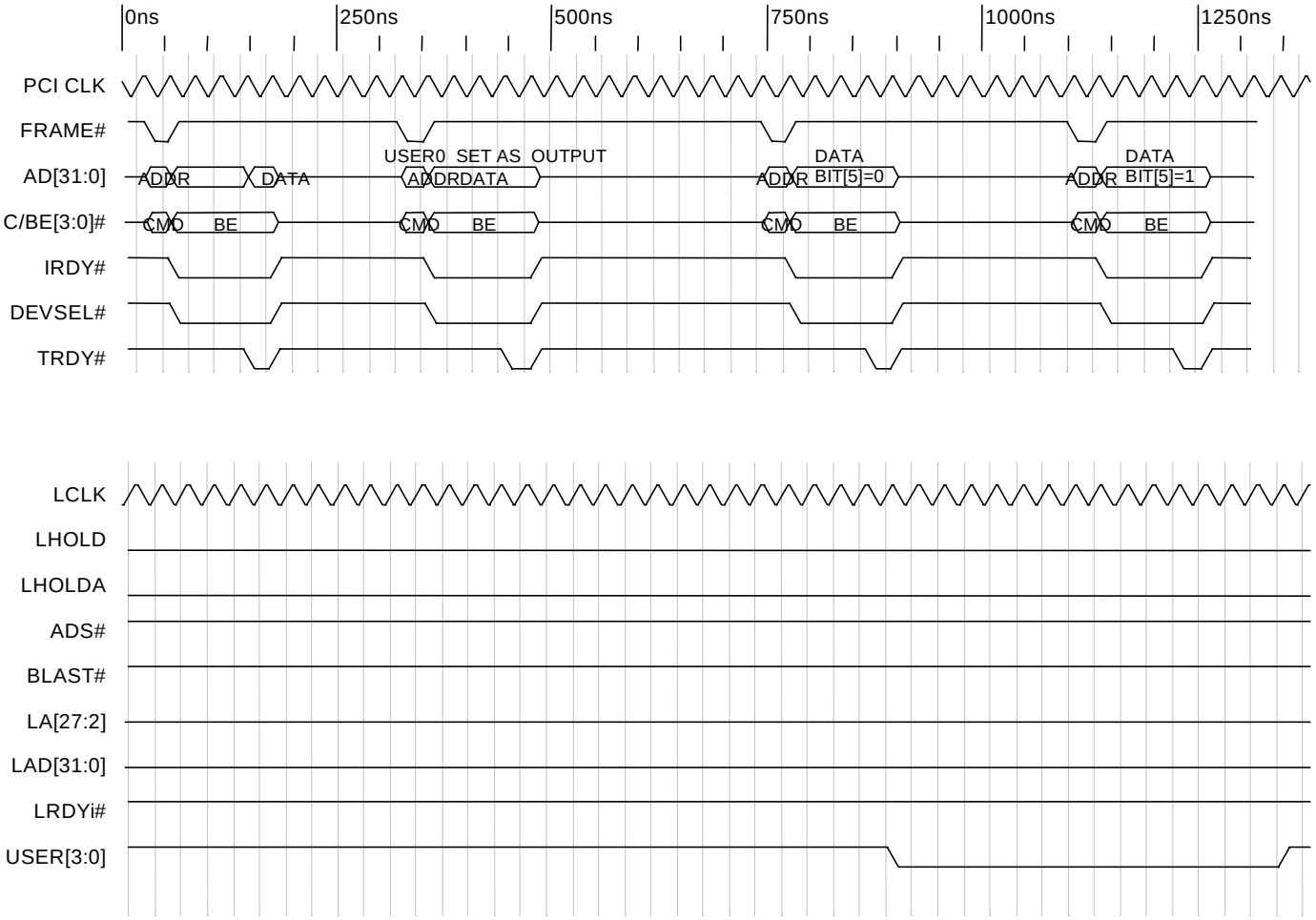


Timing Diagram 8-4. PCI RST# Asserting Local Output LRESET#



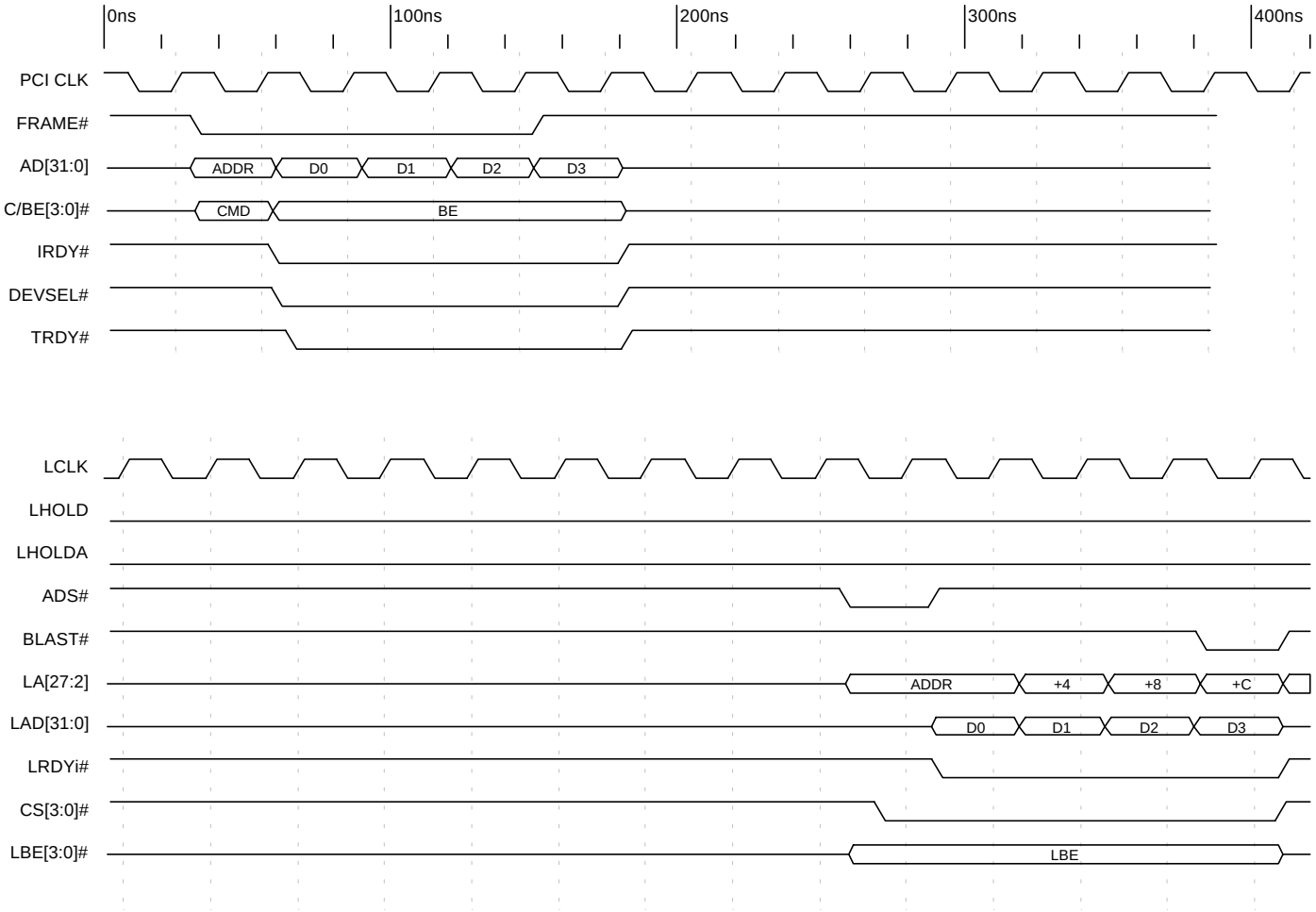
Note: *Same for USER1, USER2, and USER3*

Timing Diagram 8-5. USER I/O Pin 0 Is an Input



Note: *Same for USER0, USER2, and USER3*

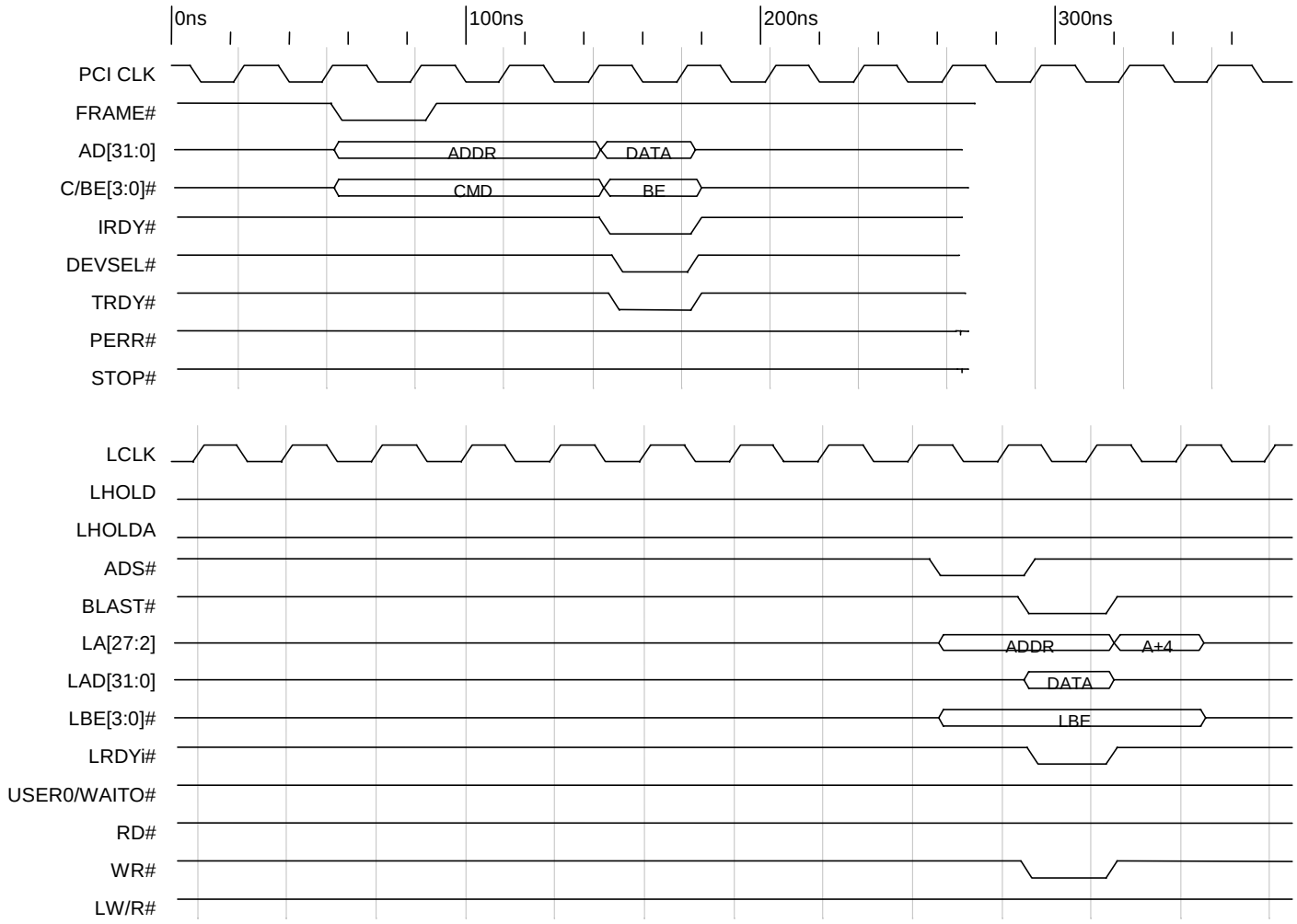
Timing Diagram 8-6. USER I/O Pin 1 is an Output



Note: *Same for CS1#, CS2#, and CS3#*

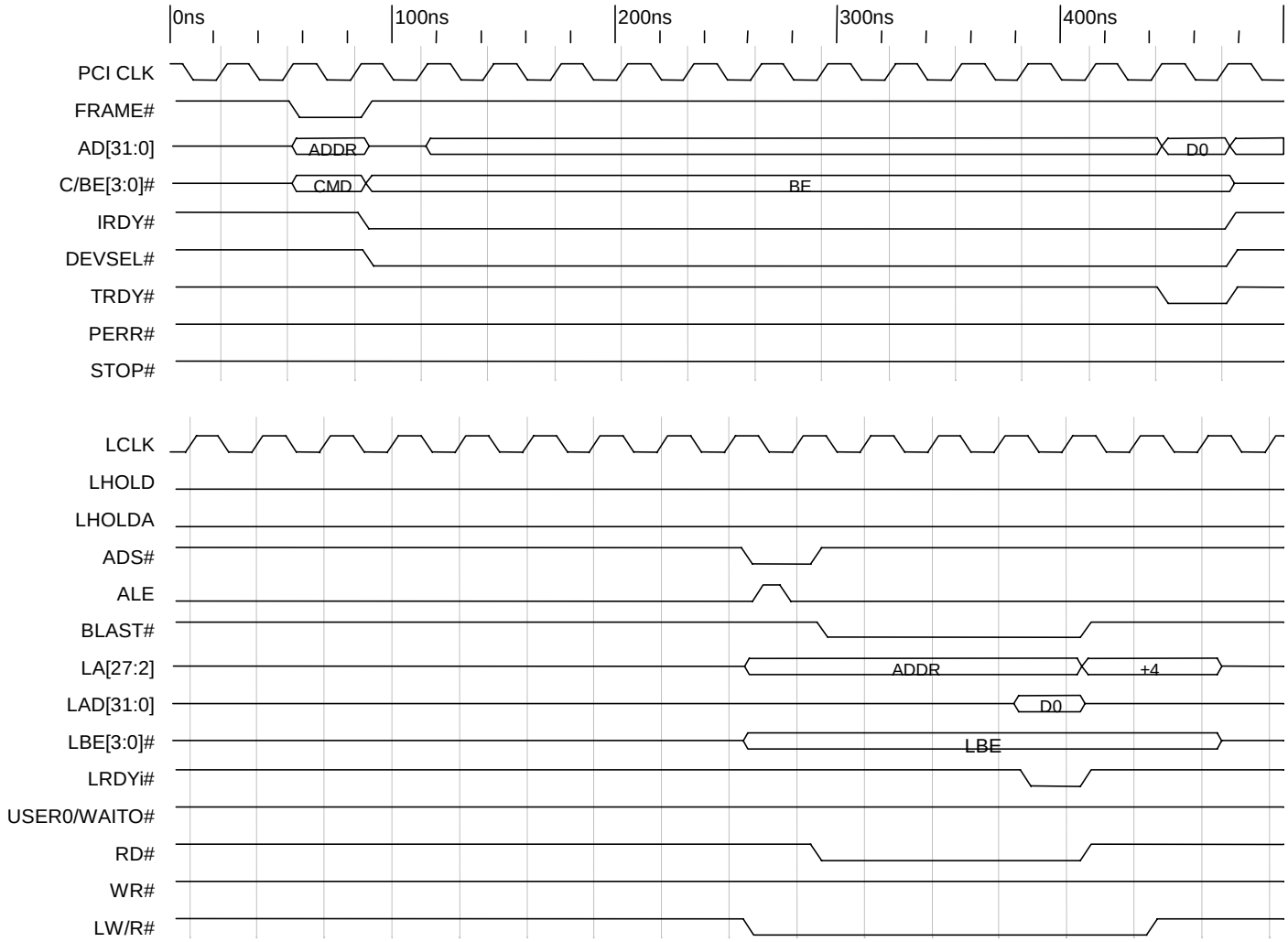
Timing Diagram 8-7. Chip Select 0 (CS0#)

8.2 Direct Slave Single

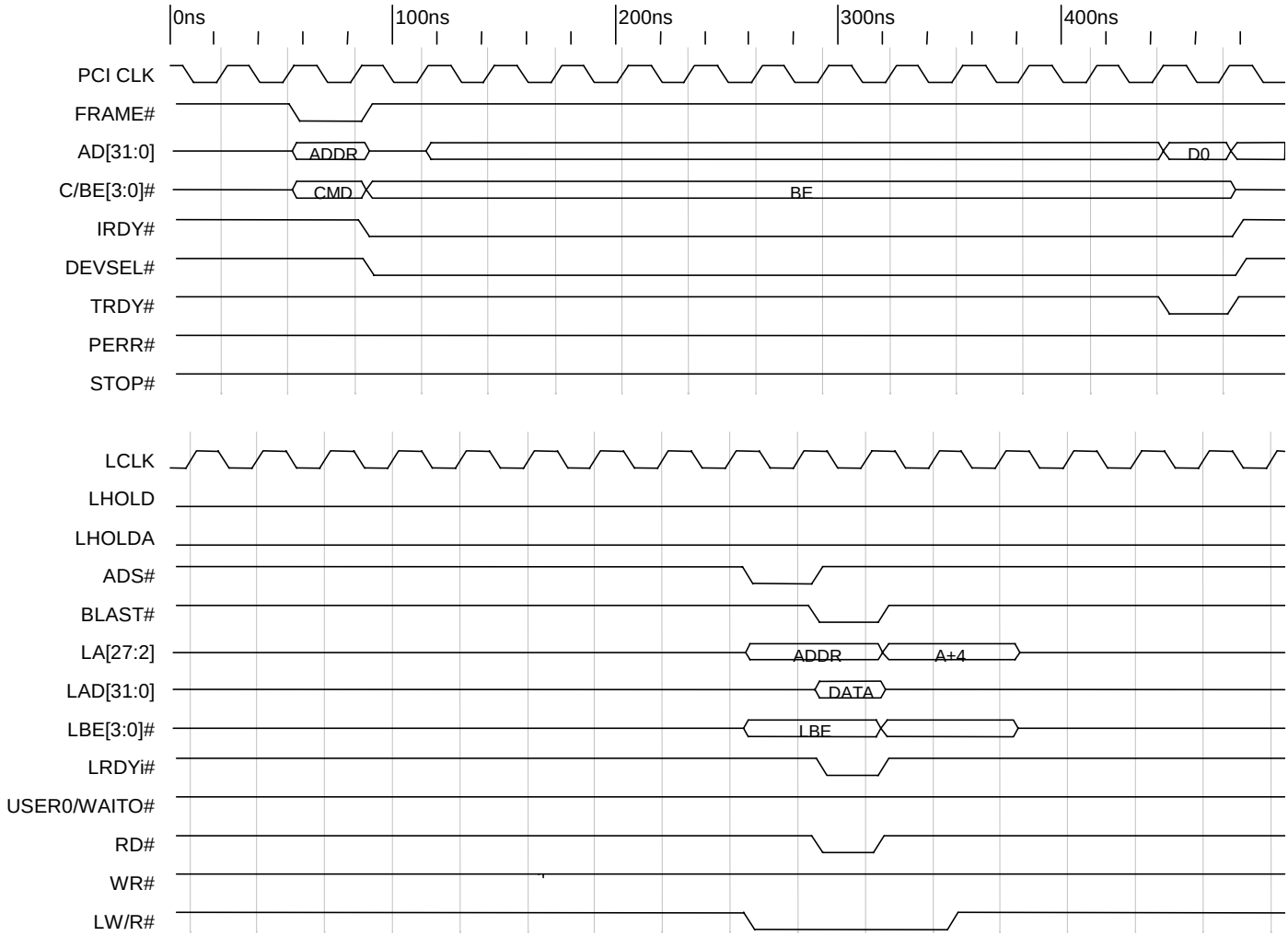


Note: *Without wait states.*

Timing Diagram 8-8. Direct Slave Single Write (32-Bit Local Bus)

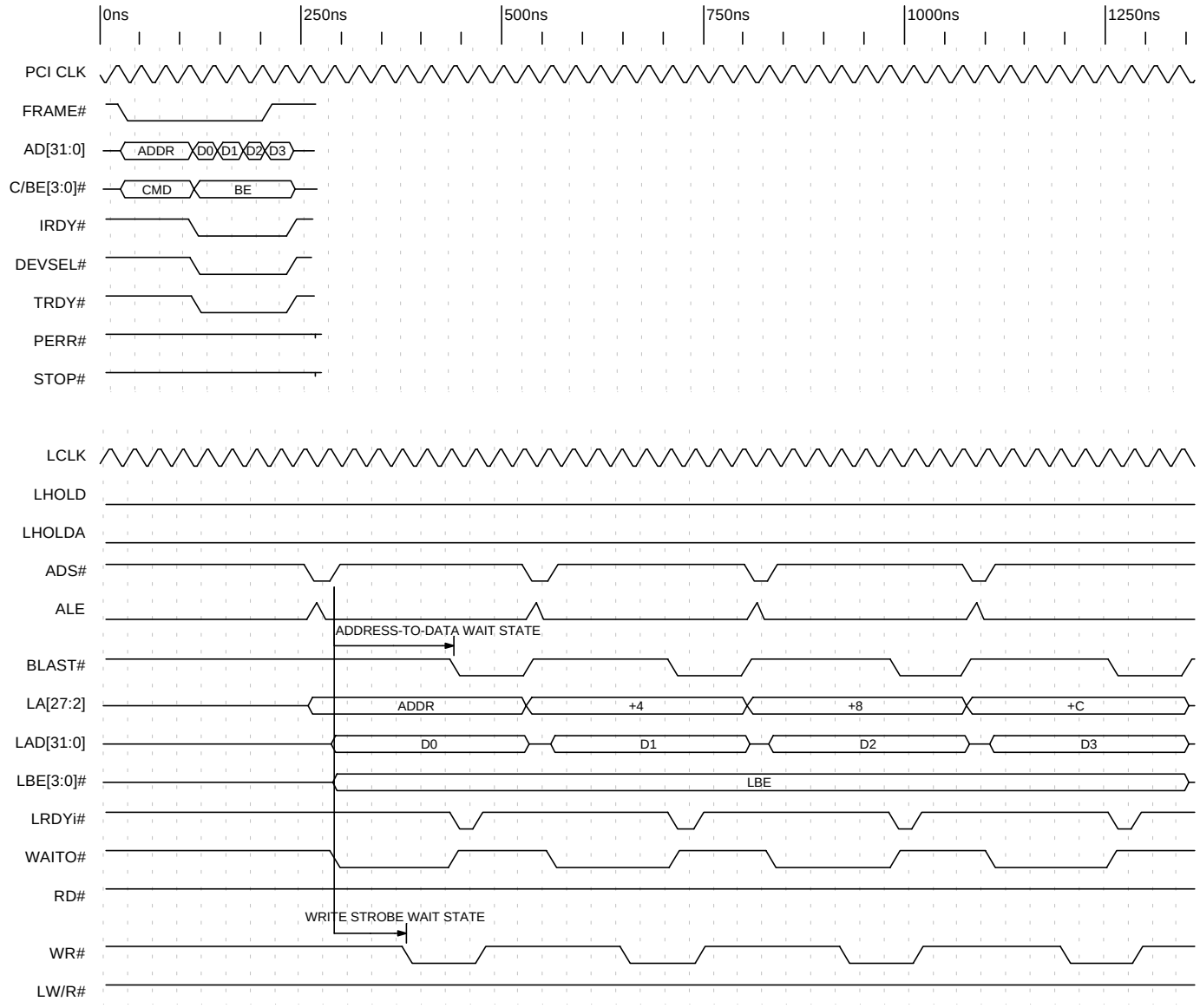


Timing Diagram 8-9. Direct Slave Single Read with Wait States (32-Bit Local Bus)



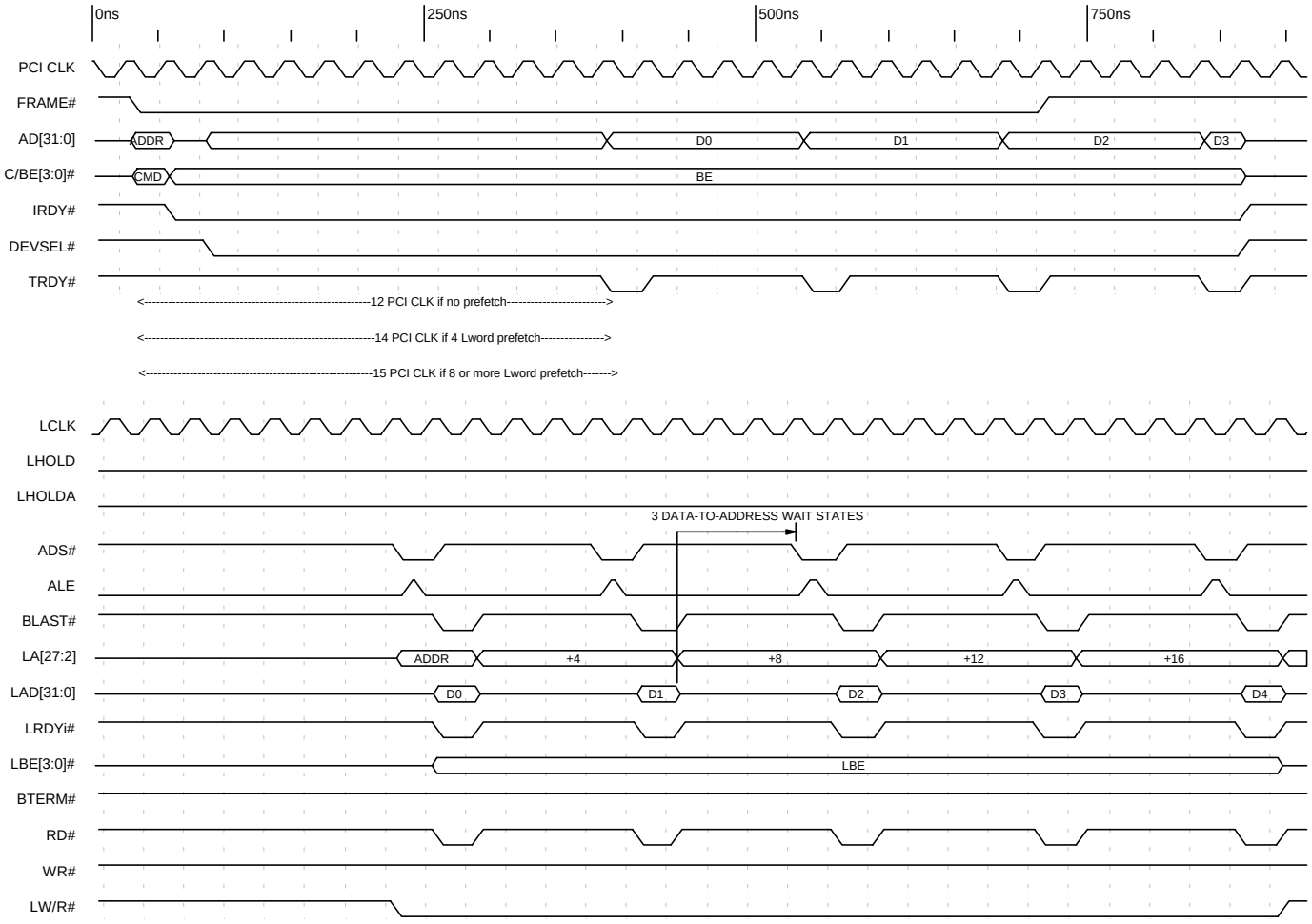
Timing Diagram 8-10. Direct Slave Single Read without Wait States (32-Bit Local Bus)

8.3 Direct Slave Non-Burst



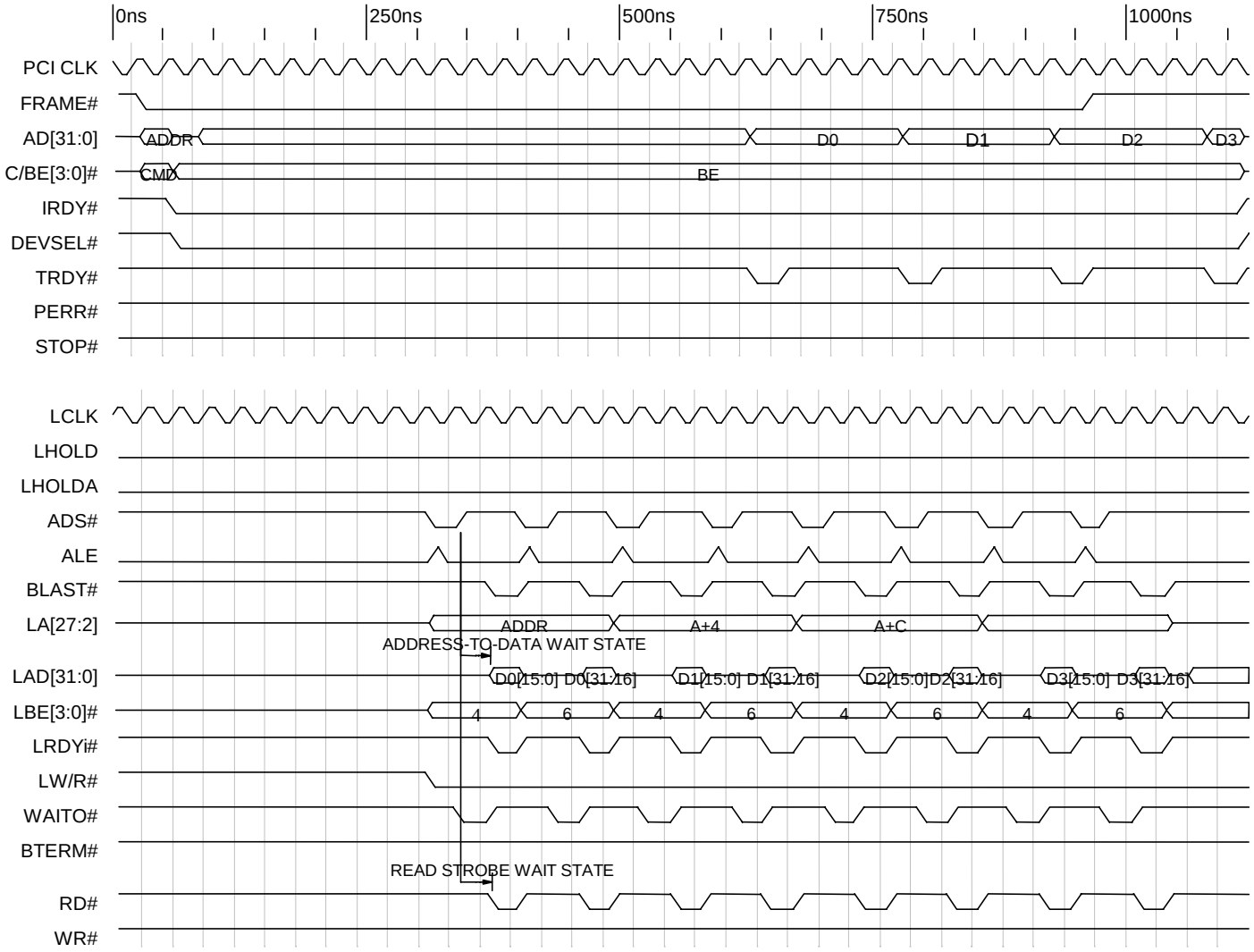
BTERM# is disabled, 32-bit local bus
ADDRESS-TO-DATA = 5 WAIT STATES
DATA-TO-DATA = 1 WAIT STATE
WRITE STROBE = 3 WAIT STATES
WRITE CYCLE HOLD = 2 WAIT STATES

Timing Diagram 8-11. Direct Slave Non-Burst Write with Wait States (32-Bit Local Bus)



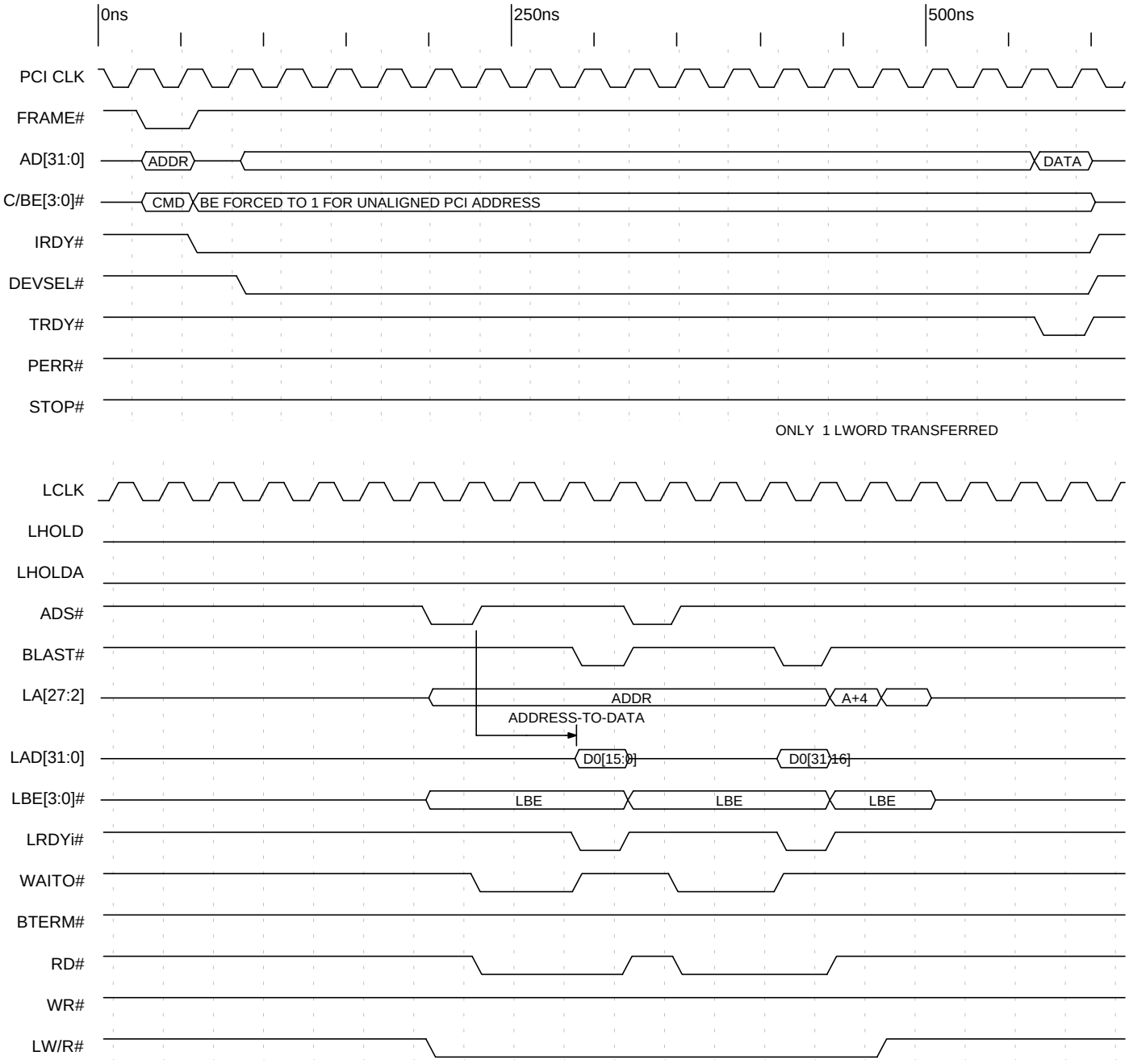
Burst Off, BTERM# is Enabled
DATA-TO-DATA = 3 WAIT STATES
WRITE STROBE = 0 WAIT STATES
WRITE CYCLE HOLD = 0 WAIT STATES

Timing Diagram 8-12. Direct Slave Non-Burst Read with BTERM# Enabled (32-Bit Local Bus)



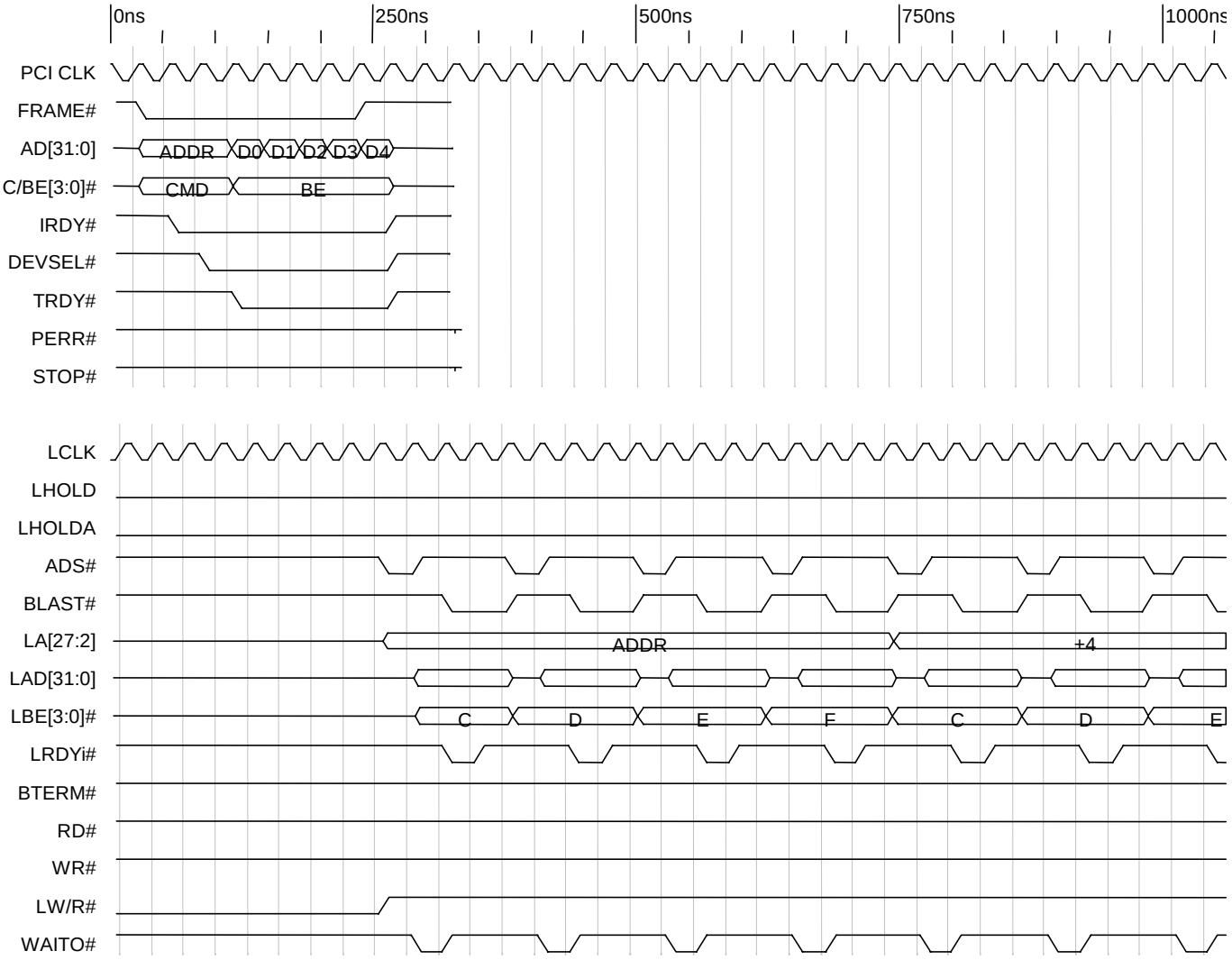
Non-Burst Read of 4 Lwords
ADDRESS-TO-DATA = 1 WAIT STATE
DATA-TO-DATA = 1 WAIT STATE
READ STROBE = 1 WAIT STATE

Timing Diagram 8-13. Direct Slave Non-Burst Read with Prefetch (16-Bit Local Bus)



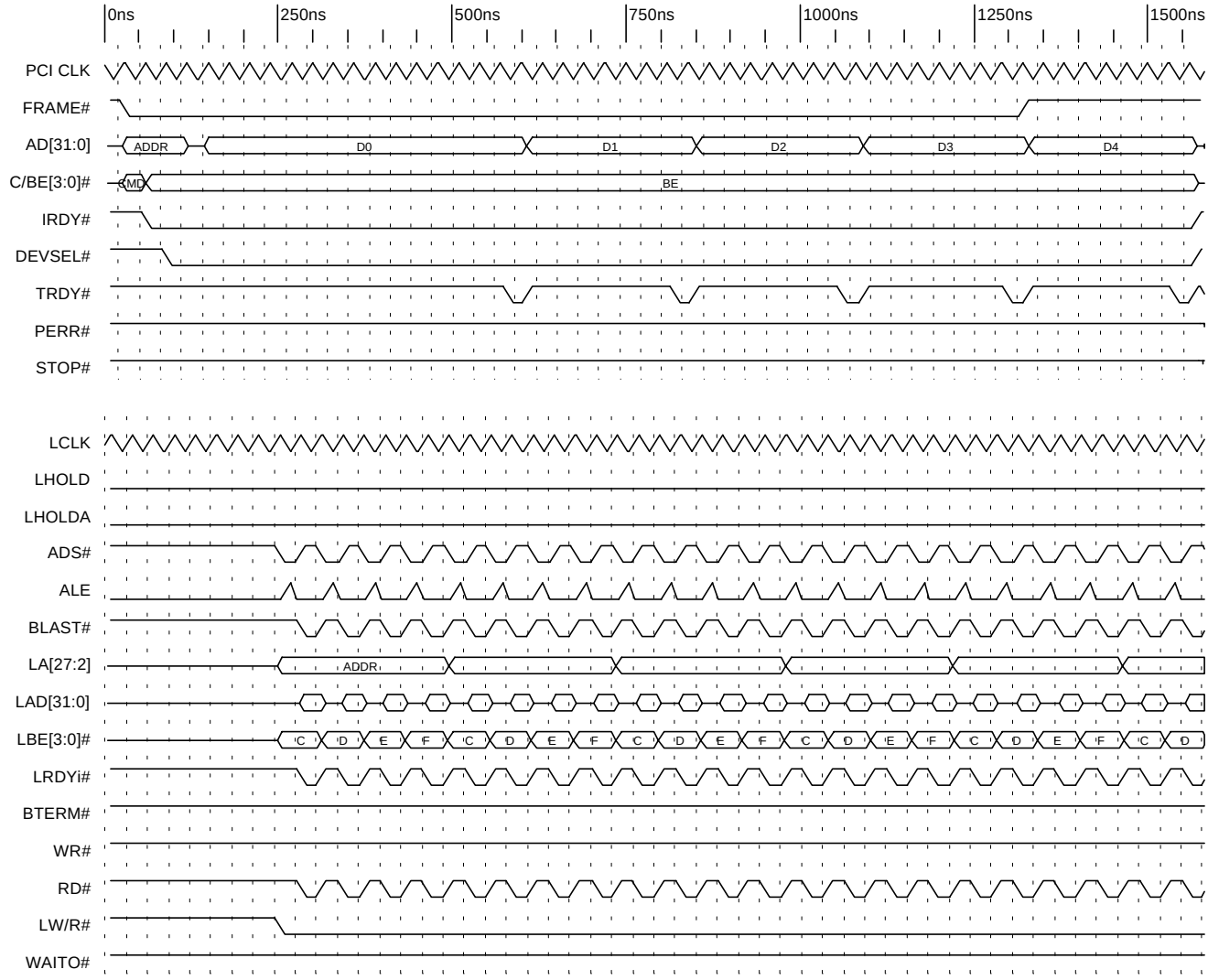
Non-Burst, Unaligned PCI Address
ADDRESS-TO-DATA = 2 WAIT STATES
DATA-TO-DATA = 0 WAIT STATES
READ STROBE = 0 WAIT STATES

Timing Diagram 8-14. Direct Slave Non-Burst Read with Unaligned PCI Address (16-Bit Local Bus)



Non-Burst Write of 5 Lwords
ADDRESS-TO-DATA = 1 WAIT STATE
DATA-TO-DATA = 0 WAIT STATES
WRITE STROBE = 2 WAIT STATES
WRITE HOLD CYCLE = 1 WAIT STATE

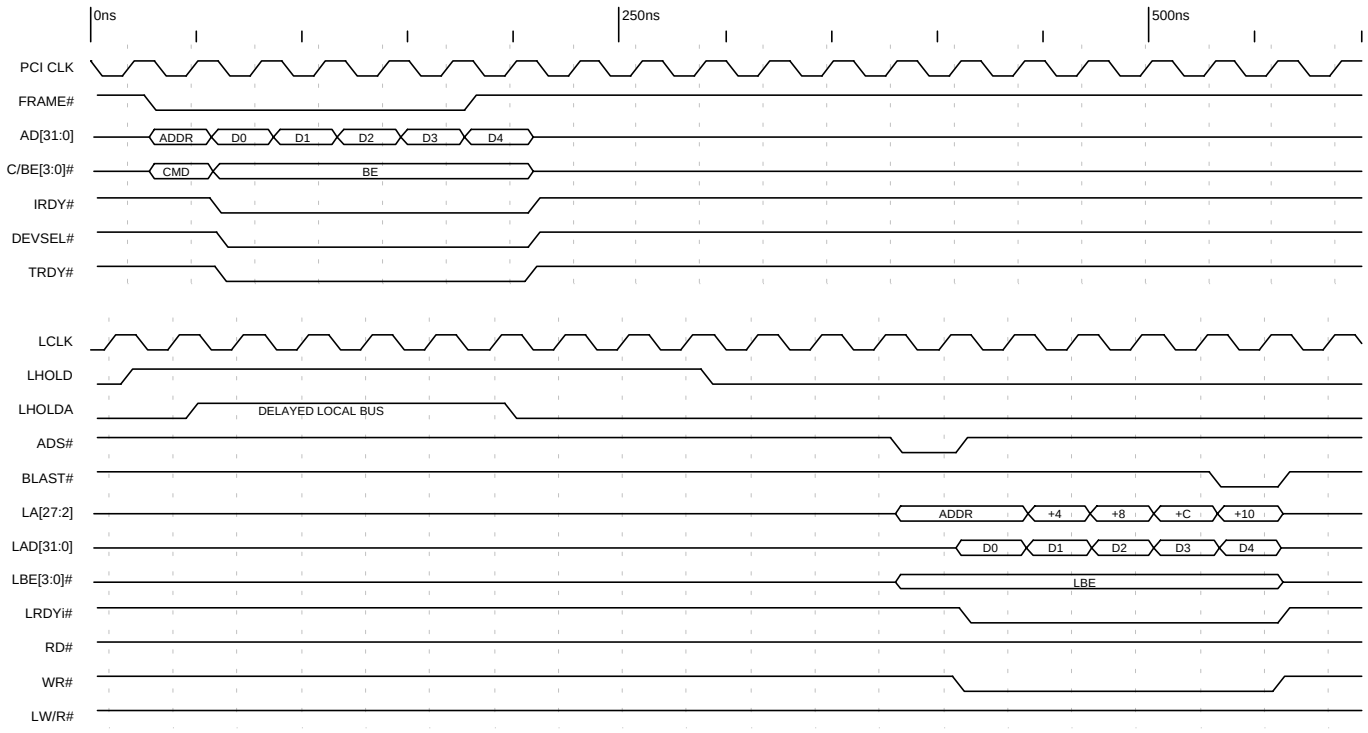
Timing Diagram 8-15. Direct Slave Non-Burst Write (8-Bit Local Bus)



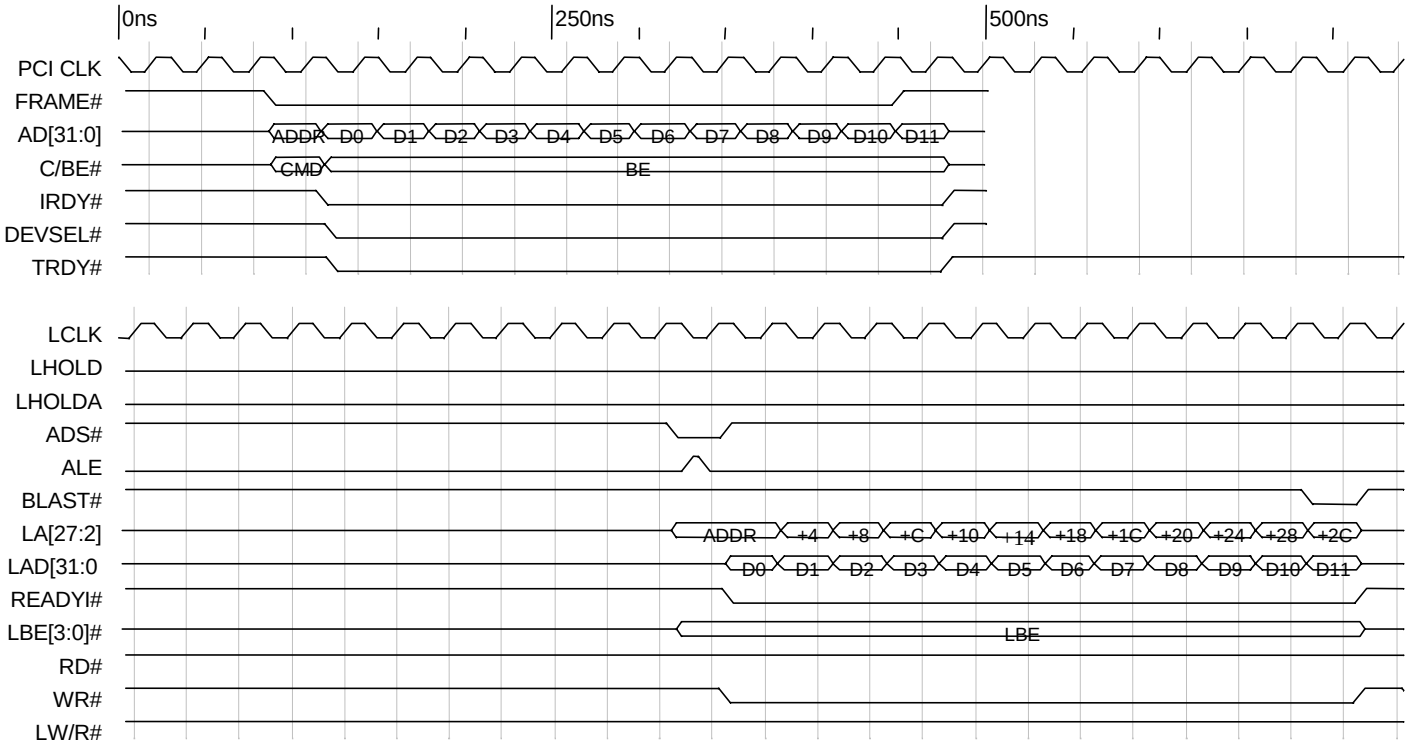
Non-Burst Read, Prefetch Enabled

Timing Diagram 8-16. Direct Slave Non-Burst Read with Prefetch (8-Bit Local Bus)

8.4 Direct Slave Burst

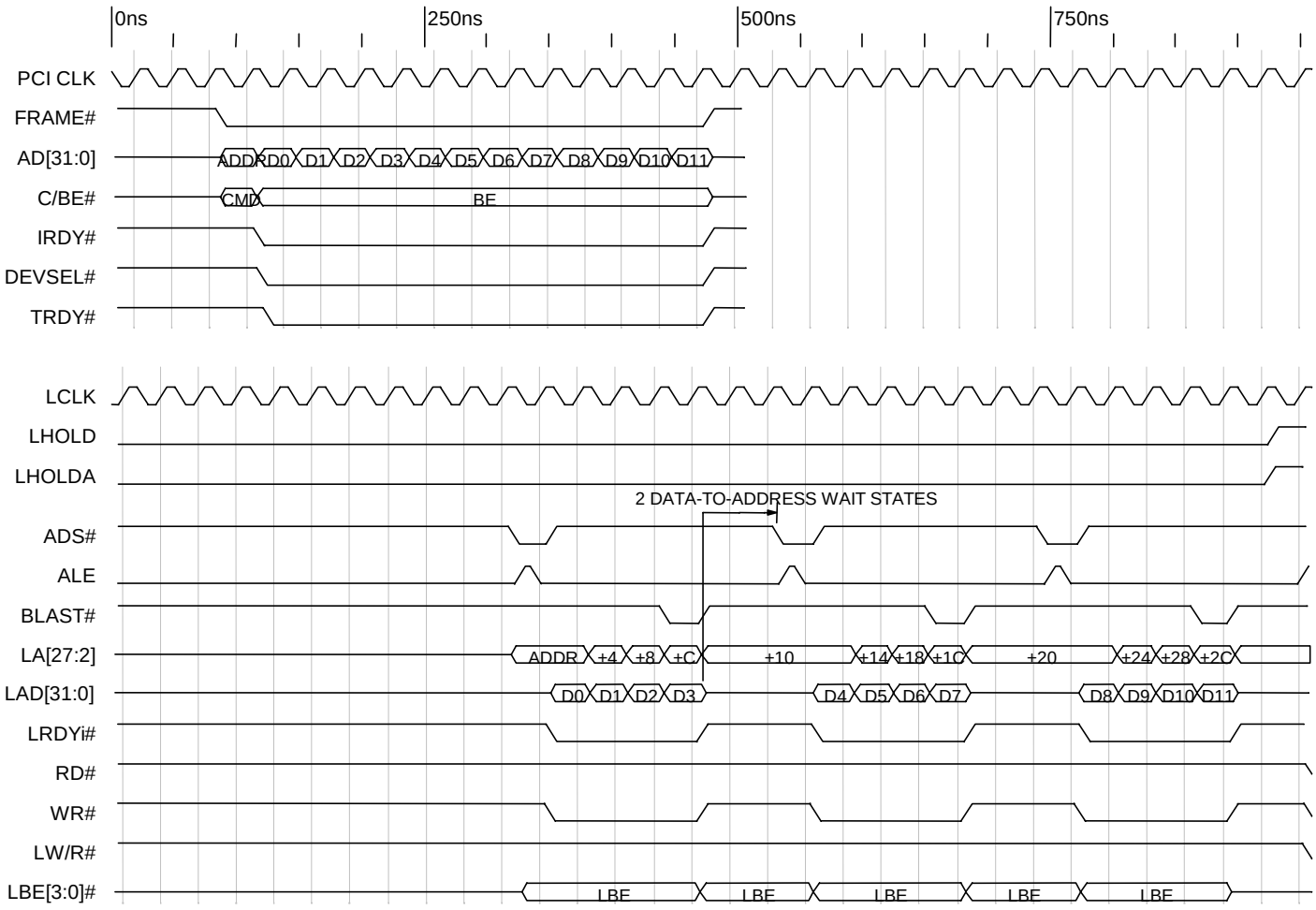


Timing Diagram 8-17. Direct Slave Burst Write with Delayed Local Bus (32-Bit Local Bus)



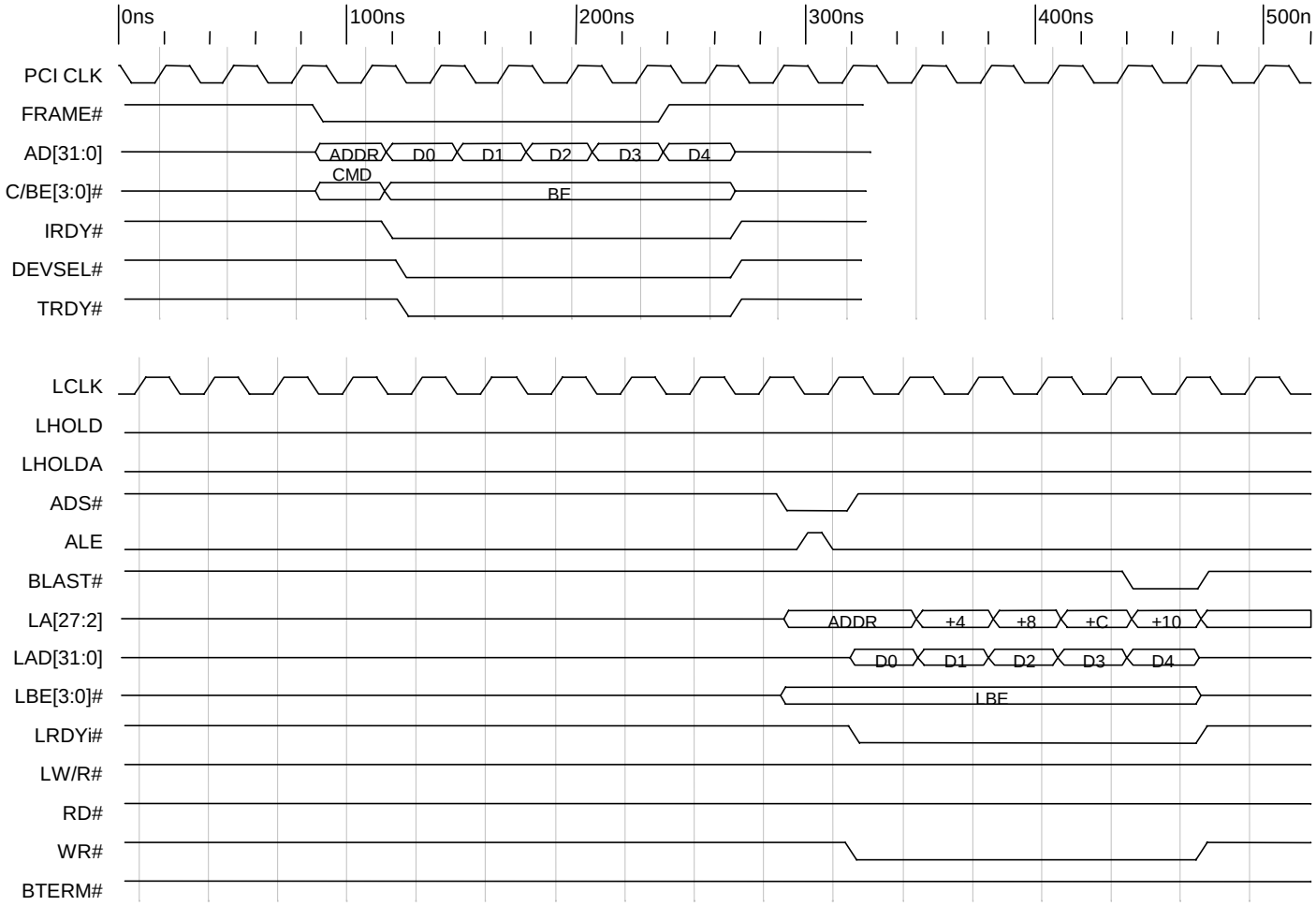
Burst is On, BTERM is On
This is for Space 2, but it is the same for Space 0, 1, 3, and Expansion ROM

Timing Diagram 8-18. Direct Slave Burst Write with BTERM on (32-Bit Local Bus)



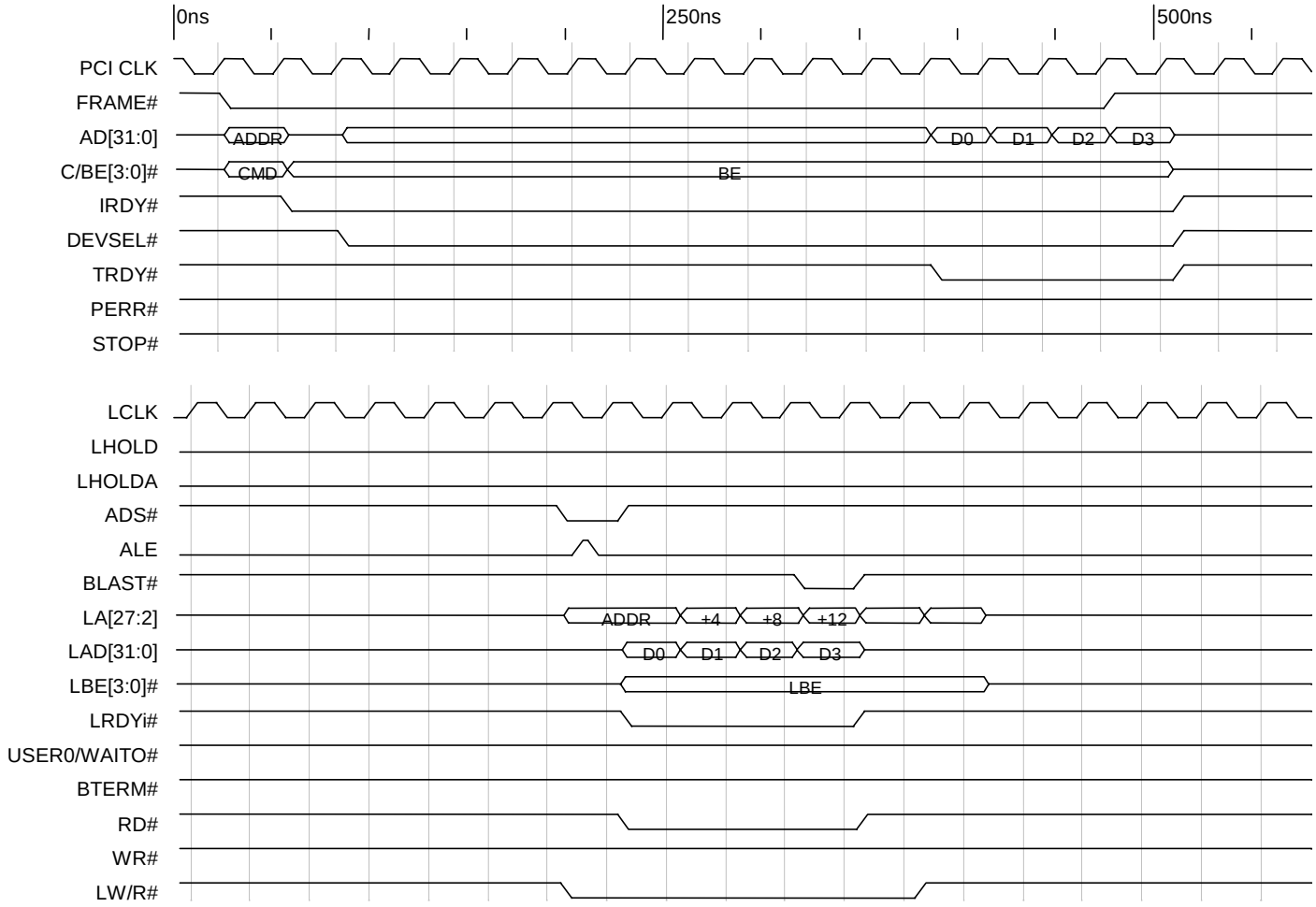
Direct Slave Write of 4 Lwords
32-Bit Local Bus, Burst is On, BTERM is Off
DATA-TO-ADDRESS = 2 WAIT STATES

Timing Diagram 8-19. Direct Slave Burst Write with BTERM off and with Wait States (32-Bit Local Bus)



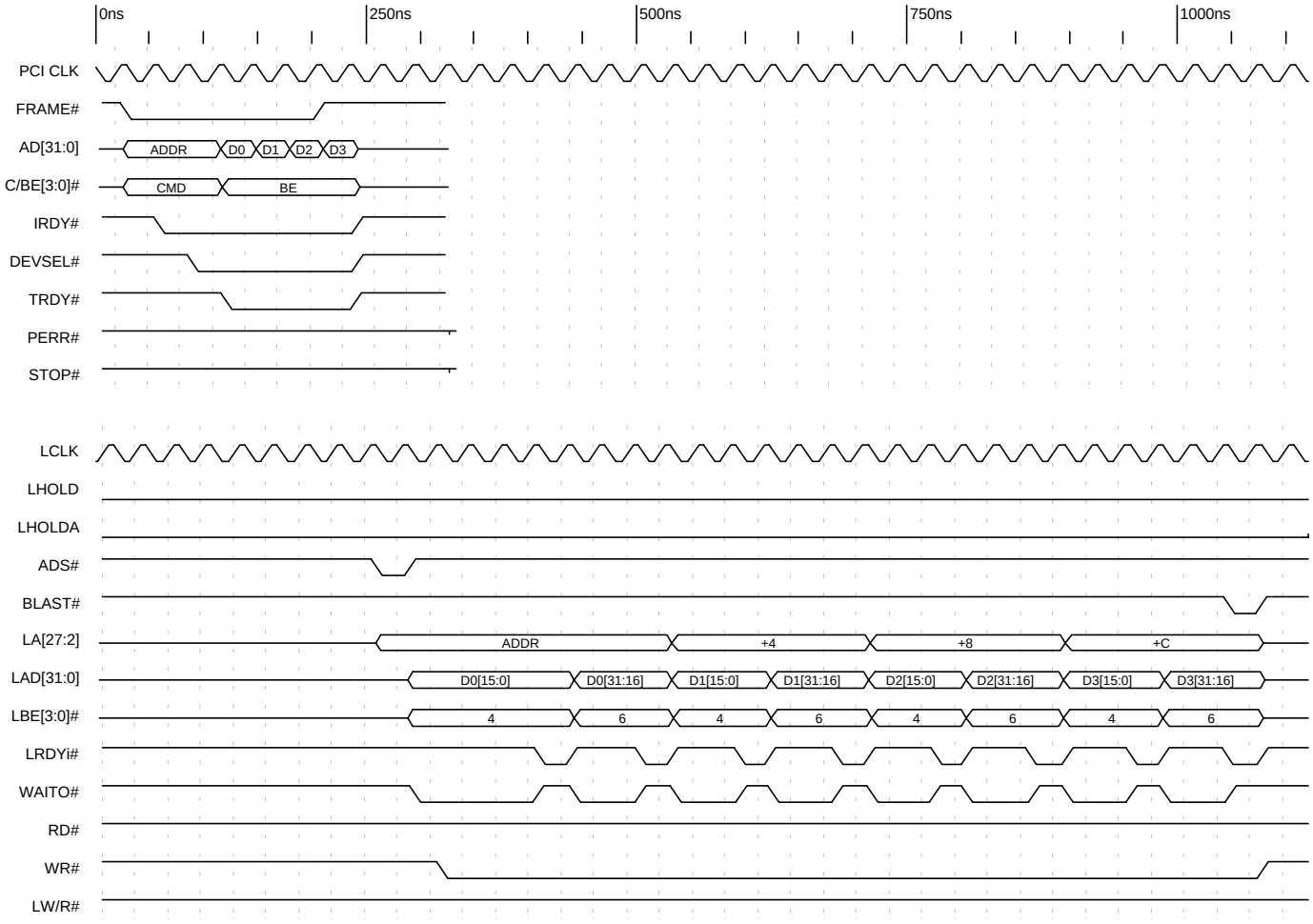
Burst Write of 5 Lwords
BTERM# is Enabled, 32-Bit Local Bus

Timing Diagram 8-20. Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus)



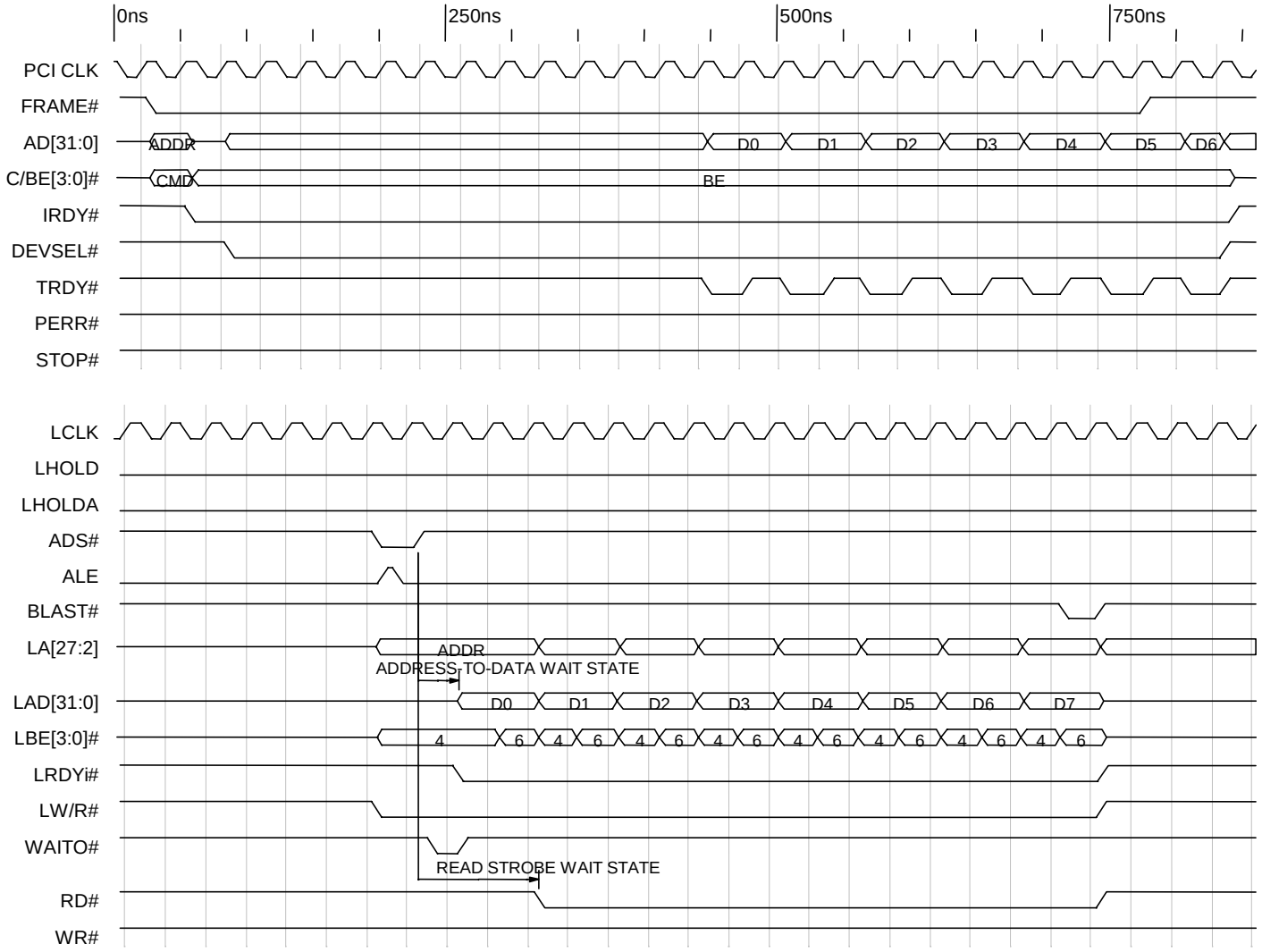
Burst is On, Prefetch 4 Lwords
ADDRESS-TO-DATA = 0 WAIT STATES
DATA-TO-DATA = 0 WAIT STATES
READ STROBE = 0 WAIT STATES

Timing Diagram 8-21. Direct Slave Burst Read with Prefetch of 4 Lwords (32-Bit Local Bus)



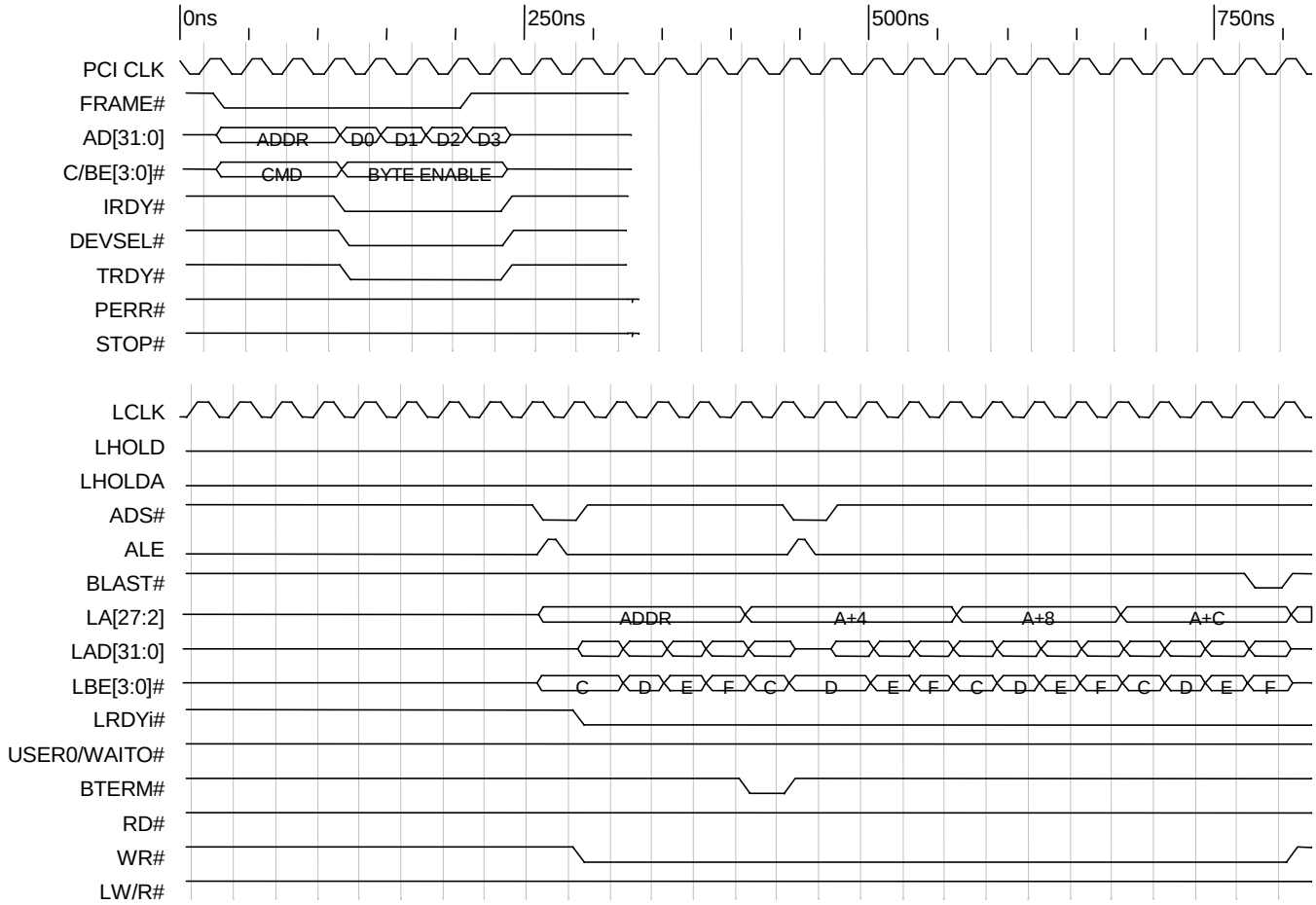
Burst is On
ADDRESS-TO-DATA = 4 WAIT STATES
DATA-TO-DATA = 2 WAIT STATES
WRITE STROBE = 1 WAIT STATE
WRITE CYCLE HOLD = 0 WAIT STATES

Timing Diagram 8-22. Direct Slave Burst Write (16-Bit Local Bus)



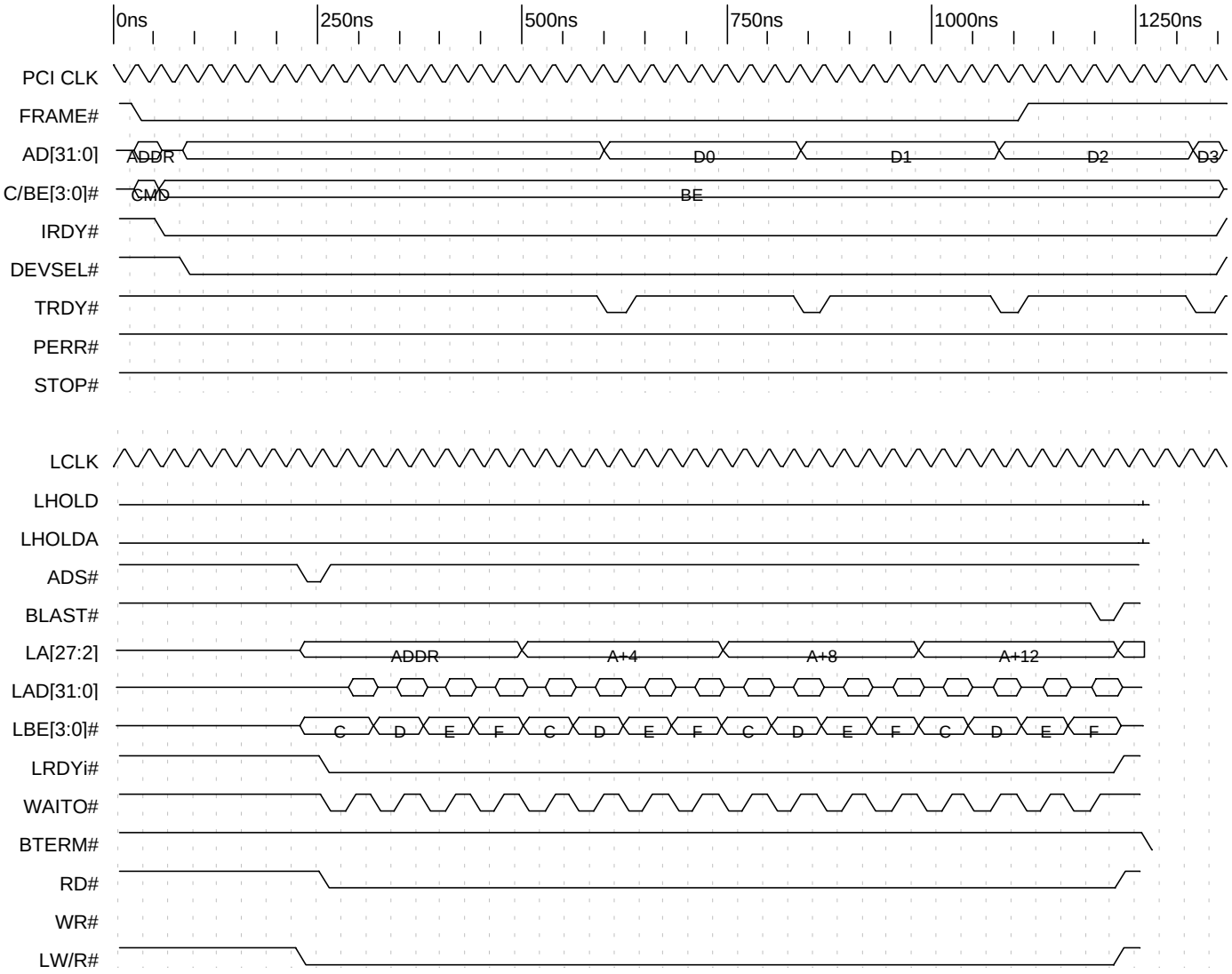
Burst Read of 7 Lwords, Prefetch 8 Lwords
ADDRESS-TO-DATA = 1 WAIT STATE
DATA-TO-DATA = 0 WAIT STATES
READ STROBE = 3 WAIT STATES

Timing Diagram 8-23. Direct Slave Burst Read with Prefetch (16-Bit Local Bus)



Burst Write of 4 Lwords, BTERM# Enabled

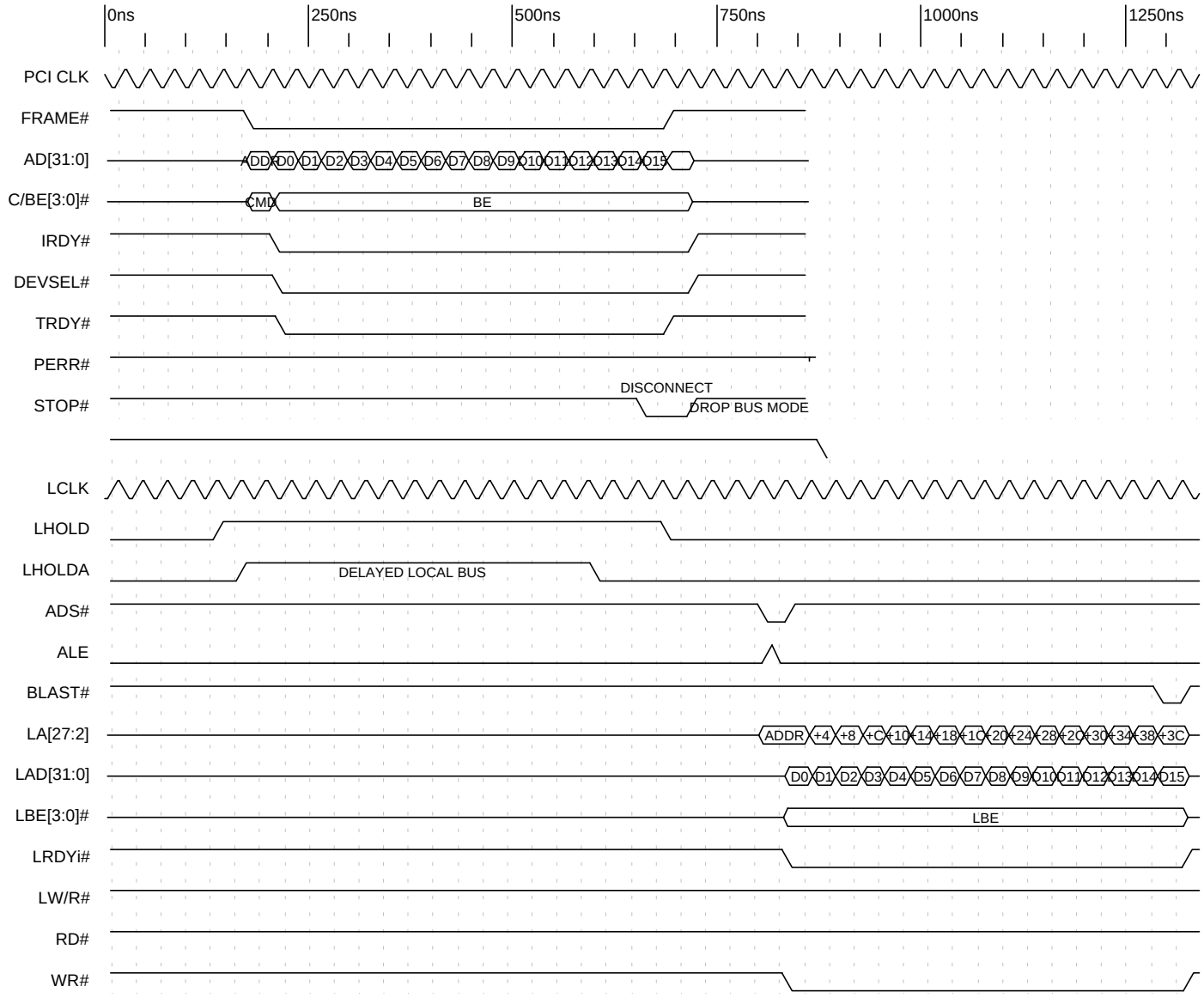
Timing Diagram 8-24. Direct Slave Burst Write with BTERM# Enabled (8-Bit Local Bus)



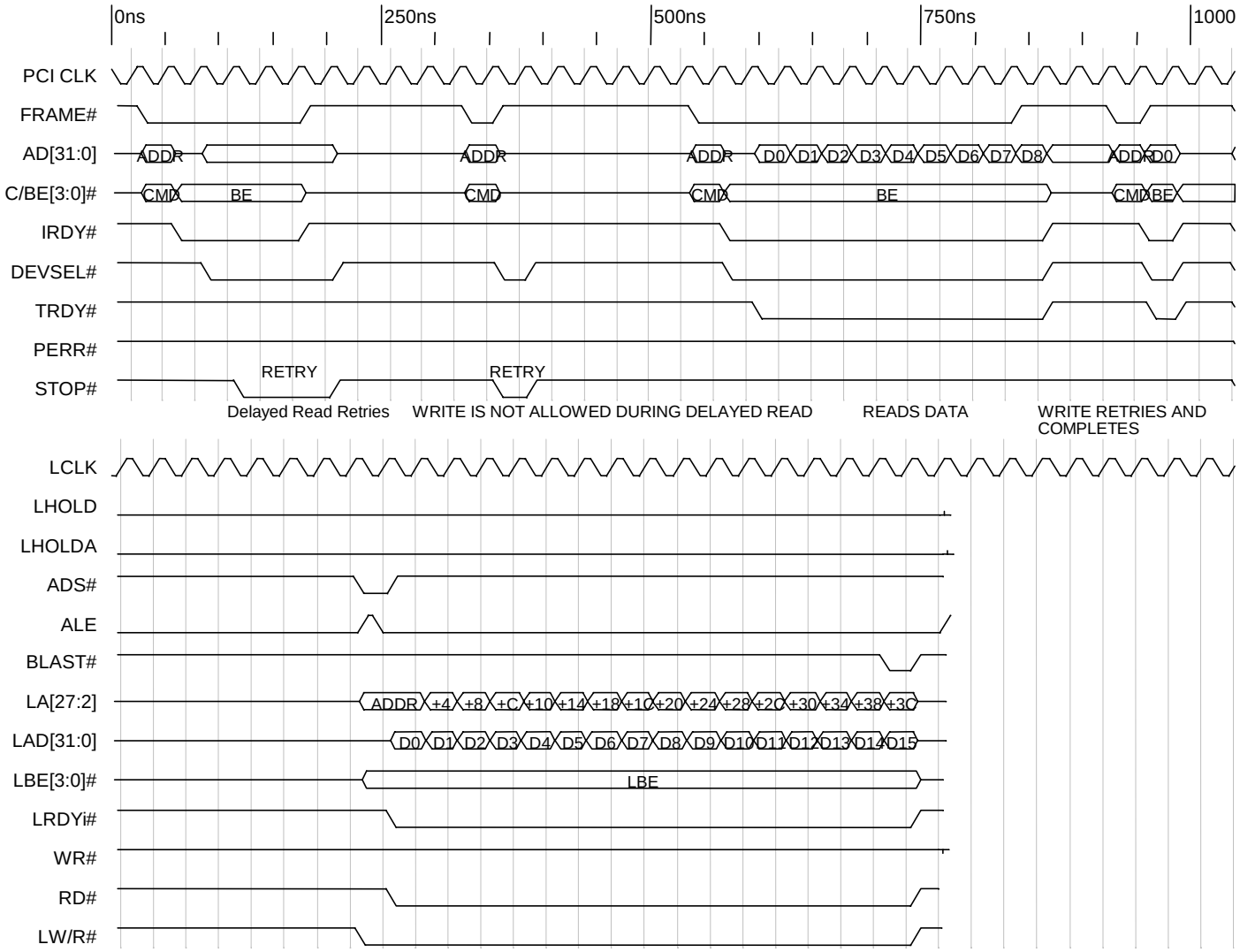
Burst Read of 4 Lwords, Prefetch of 4 Lwords
ADDRESS-TO-DATA = 1 WAIT STATE
DATA-TO-DATA = 1 WAIT STATE
READ STROBE = 0 WAIT STATES

Timing Diagram 8-25. Direct Slave Burst Read with Prefetch (8-Bit Local Bus)

8.5 Miscellaneous Functionality

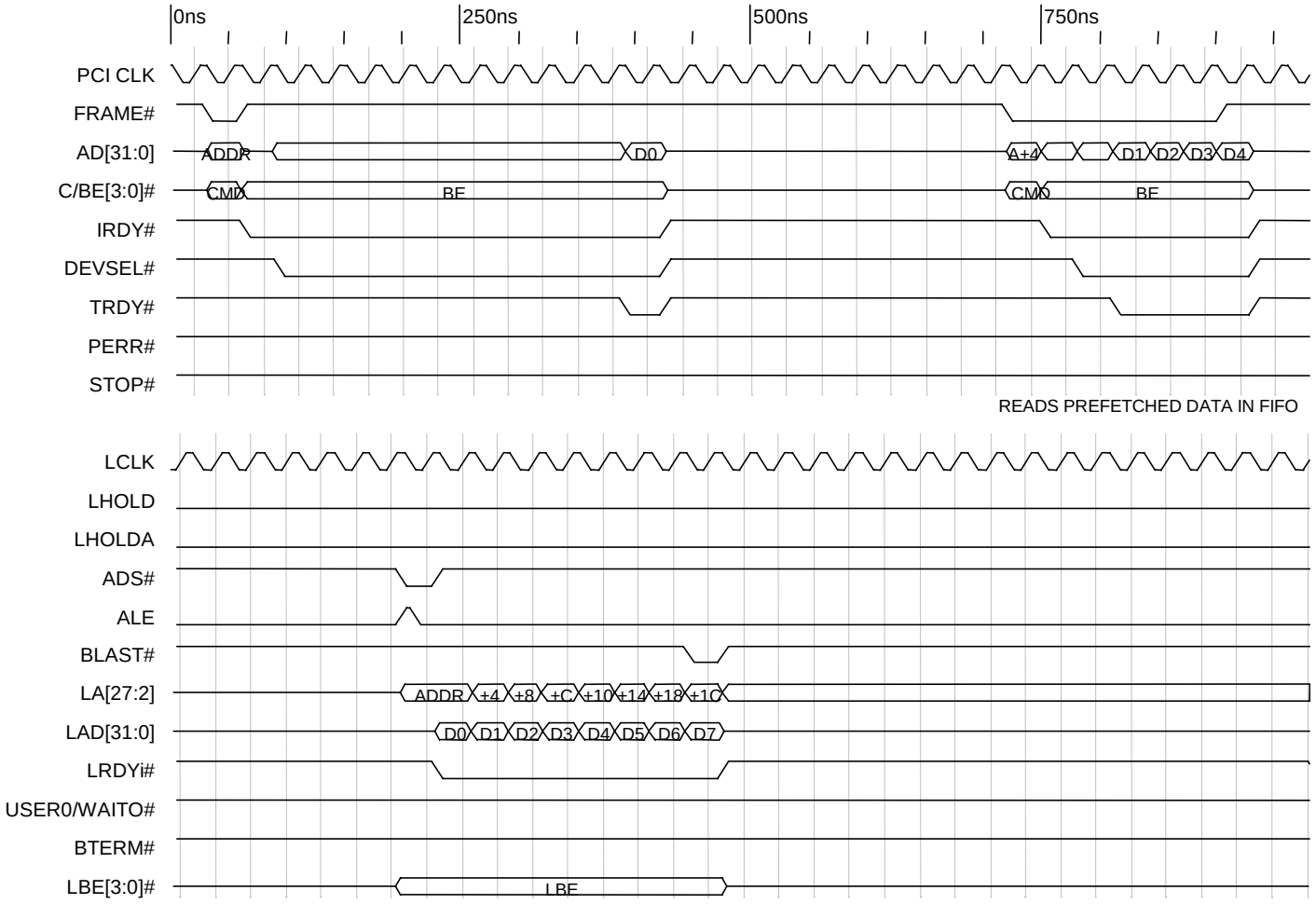


Timing Diagram 8-26. Direct Slave Write 2.1 Spec (32-Bit Local Bus)



Disconnects immediately for a Read
Don't Effect Pending Reads when a Write Cycle Occurs
Don't Flush the Read FIFO if the PCI Ready Cycle Completes
Force Retry on Write if Read is Pending

Timing Diagram 8-27. Direct Slave Read 2.1 Spec (32-Bit Local Bus)



Prefetch 8 Lwords, Cache Mode Enabled

Timing Diagram 8-28. Direct Slave Read with Cache Mode Enabled (32-Bit Local Bus)