PCI 9050

Technical Update
December 2, 1997

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9050	PCI 9050-1	First Silicon	August 1996	October 1996

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.0	Final data sheet	August 1996

The scope of this document encompasses the PCI 9050.

1. Reads from Local Configuration Registers

Problem:

If bit 7 of the base address for the I/O or Memory mapped Configuration Registers (PCI configuration register offset 14h or 10h) is set to 1, the local configuration registers can not be read. Under this condition, they will all return zeroes when the PCI master (typically the host) attempts to read them. They can be written to from both the PCI master and the EEPROM. In other words, the information is correctly written into the local configuration registers, but it can not be read the PCI Master. If bit 7 is set to 0, the local configuration registers can be read correctly. In a PCI system, the BIOS determines the base address (i.e. sets the value of bit 7) during the initial configuration cycle.

Solution/workaround:

During adapter hardware and driver development, it may be desirable to read the configuration registers to confirm that the local configuration registers were programmed properly. If the BIOS have bit 7 set to 0, a PCI master can read these registers. If the BIOS has set bit 7 to 1, change the base address of the memory or I/O mapped local configuration registers so that bit 7 is de-asserted. This value can be easily changed by writing to offsets 10h and 14h, which hold the base address. For example, say the host assign a value of 0000FC81h to I/O mapped local configuration register (PCR 14h). Use PLXMON (9050RDK) or your own driver to change this base address to 0000FC01h (type PCR 14 0000FC01 at the PLXMON command prompt).

Impact:

In the production phase, for some types of adapters it is never necessary to read the local configuration registers. In these cases, this erratum has no impact. However, in some situations, it is desirable to read the local configuration registers. Situations, which are impacted, are;

1. Interrupt Status. If there is only one local interrupt source, the errata has no impact. However, if there are two local interrupt sources, the PCI master can not read the local configuration registers to determine where the interrupt come from. In this case, the interrupt status should be stored in local memory or an on-board register. The PCI master should read the status from the local memory or register.

2. User Inputs (1,2,3, and 4), used for transferring bit or status data from the local side. If messages need to be passed to the host, a section of local memory can be defined and a direct slave read access could be made to retrieve the data.

3. Serial EEPRM read and valid bits, for host initiated read from an external serial EEPROM. This mode is generally used only in development.

2. Expansion ROM Space Enable

Problem:

If the PCI BIOS does not set the Expansion ROM Space enable bit in the PCI 9050 during initialization, the PCI 9050 will return all 0's for the range, indicating that there is no Expansion ROM. This problem applies only to boards that need to use Expansion ROM Space.

Solution/workaround:

Most standard PCI BIOS do not set the enable bit during initialization. Therefore, to use Expansion ROM, in most cases requires modification to the BIOS.

PCI 9050

Design-in Notes
December 2, 1997

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9050	PCI 9050-1	First Silicon	August 1996	October 1996

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.0	Final data sheet	August 1996

1. RD# Signal (Read Strobe), CS[3:0]# (Chip Select)

The PCI 9050 drives all local output signals when it owns the local bus. After it asserts LHOLDA to grant the local to another master, PCI 9050 floats all local output signals. However, PCI 9050 drives the RD# and CS[3:0]# signals at all time. This results in a bus contention when the RD# and CS[3:0]# signals are shared by multiple masters, to prevent this see work-around items 1 & 2.

1. Tri-state RD# and CS[3:0]# from the PCI 9050 through an external 74LS125 (LHOLDA is used as a gate signal).

2. Add an external multiplexer to RD# and CS[3:0]# signals and use LHOLDA as the select signal.

Note: Items 1 & 2 both require local output signals to be pulled up or pulled down to an inactive state.

2. Blank Serial EEPROM and Default Value for PCI Target Retry Delayed Clock

The PCI Target Retry Delayed Clock determines the number of PCI clocks (multiplied by 8) after the beginning of a direct slave cycle until a retry is issued. The default value for PCI Target Retry Delayed Clock is 0 and 64K of memory for the Expansion ROM Space. If a blank serial EEPROM is used, the PCI bus will get continuous retry when the PCI 9050 tries to look for the Expansion ROM on the local bus. To prevent this see work-around items 1 & 2.

1. The PCI 9050 application must be accompanied by a pre-programmed serial EEPROM and the PCI Target Retry Delayed Clock value equals or greater than 3 (multiplied by 8).

2. The PCI 9050 application must be accompanied by a pre-programmed serial EEPROM with the PCI Read mode (Delayed Read) bit set.

3. **Floating Local Signals**

PCI 9050 floats all local output and input/output signal when it does not drive the local bus.

To prevent this, keep these signals in an in-active mode, external pull-up on control signals such as, LA[27:0], LAD[31:0], ADS#, LW/R#, CS[3:0]#, RD#, and WR# and external pull-down on ALE are recommended.