IOP 480

I/O Processor

Highlights

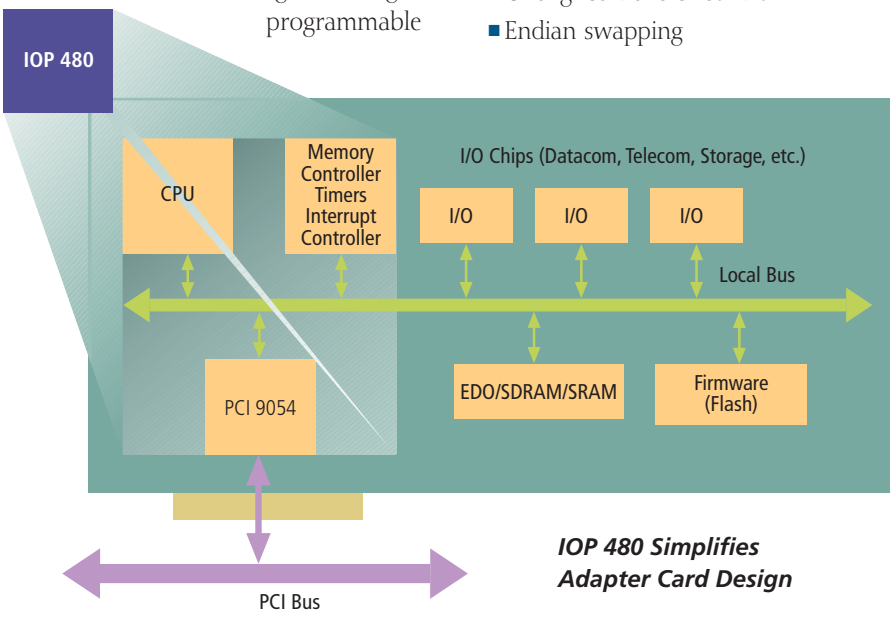
- PowerPC 32-Bit RISC CPU Core with MMU, 4KB I-Cache and 2KB D-Cache
- Performance up to 70 MIPS @ 66MHz
- PCI v2.2 Compliant 32-Bit 33MHz Controller with Two Block Mode or Scatter/Gather DMA Channels which allow unlimited bursts up to 132Mbytes/Second
- CompactPCI Hot Swap Friendly
- PCI Host, Target, and Initiator Capability
- PCI Bus Arbiter Supports Three External PCI Bus Masters
- I_2O Ready Messaging Unit with v2.0 Performance Extensions
- Flexible Memory Controller supports up to 256Mbytes of EDO/SDRAM/SRAM
- Programmable Interrupt Controller
- 32 Bit Multiplexed Local Bus up to 66MHz supports 8-, 16-, or 32-bit Peripheral and Memory Devices with unlimited bursting up to 264Mbytes/Second
- Local Bus Arbiter Supports Two External Local Bus Masters
- Fly-By Local to Local DMA Channel
- IEEE 1149.1 JTAG Port
- PCI Power Management Spec Compatible Low Power Modes: Operating, Standby, Sleep
- 600mW Typical Operating
- 3.3V, 5V tolerant signaling
- 3.3V CMOS in 208-pin PQFP or 225-ball PBGA packages

The rapid spread of PCI in embedded designs has led to the creation of a new class of products, the I/O Processor (IOP). Design requirements driving the development of the IOP include a distributed processing architecture, a high speed PCI system bus, a high performance, low cost processor, efficient memory management, flexible I/O device interface, high performance burst mode data transfers, intelligent message passing support, and efficient I/O transaction management. To meet these requirements, the new IOP 480 integrates a 50/66MHz, PowerPC® core and highly flexible memory controller with PLX's industry leading advanced Data Pipe Architecture™ PCI controller including dual DMA channels, programmable PCI Initiator and Target data transfer modes and PCI messaging functions. The IOP 480 is available in space saving PQFP or PBGA packages with power management and CompactPCI® Hot Swap support.

The IOP 480 provides a highly flexible local bus offering 8-, 16-, or 32-bit operation, at speeds up to 66MHz, and in 32-bit mode offers fly-by DMA with single cycle transfers between local memory and I/O devices. To maximize flexibility in design, the 3.3V IOP 480 offers 5V tolerant signaling on both the PCI and Local bus, complies with PCI v2.2, and supports the performance enhancements in I_2O v2.0. With support for both type 0 and 1 configuration cycles, and arbiters for both the PCI and Local bus, the IOP 480 is ideal for embedded host as well as adapter card designs. The IOP 480 I/O Processor is the next step in PLX's support of high performance embedded PCI design.

Advanced Data Pipe Architecture

IOP designs require highly efficient management of PCI bus bandwidth. The IOP 480 incorporates PLX's industry leading advanced Data Pipe Architecture™ including DMA engines, programmable PCI Initiator and Target data transfer modes and PCI messaging functions.



IOP 480 Simplifies Adapter Card Design

Dual Primary DMA Channels

- Dual independent channels with flexible prioritization scheme
- Direct H/W control of DMA
  - -Demand mode DMA operation
  - -Burst size control
  - -End of Transfer (EOT)
- Programmable burst length including unlimited burst
- Shuttle mode DMA channel support with automatic invalidation of used DMA descriptors
- Unaligned transfer support
- Supports PCI bus mastering from local slave-only devices
- Scatter/Gather list management
  - -Descriptors can be PCI or local bus
  - -Allows independent scatter/gather management

Local to Local DMA Channel

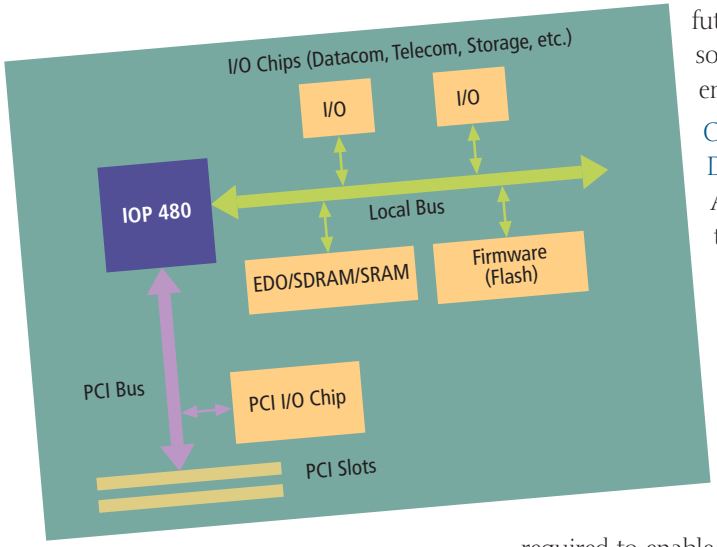
- Fly-By single cycle transfers between local memory and I/O or double cycle between local and host memory

PCI Initiator

- Type 0 and Type 1 configuration cycles
- All PCI cycle types supported
- Initiator READ prefetching
- Burst length control–programmable threshold pointer
- Unaligned transfer control
- Endian swapping

PCI Target

- Multiple independent address spaces
- Dynamic local bus width control
- Target READ prefetching
- Endian swapping
- Local bus priority control
- Latency timer



PCI Embedded Host System Design Simplified

PCI Messaging

- Complete messaging unit with mailbox registers, doorbell registers
- Queue management pointers which can be used for message passing under the I_2O protocol or a custom protocol.

IOP 480 Applications

PCI Adapter Cards

The IOP 480 provides an ideal solution for data intensive PCI adapter card applications including communications, network interface cards, RAID and disk control, multimedia and video adapters. Its combination of performance, small size and limited power requirements simplify the designers task, while enhancing product performance.

High Performance I_2O Design

As a member of the I_2O SIG, PLX helped define the I_2O specification, and was the first to offer a processor-independent I_2O implementation in the PCI 9080. The IOP 480 is the industry's first second-generation IOP, incorporating the latest I_2O and PCI performance enhancements.

I_2O also provides an efficient solution for embedded designs. I_2O takes advantage of PCI's performance features, while providing a level of abstraction from both the host operating system and I/O subsystem. Using I_2O simplifies the upgrade path of the designer's product to take advantage of future hardware and software performance enhancements.

CompactPCI Adapter Designs

Another key application for the IOP 480 is CompactPCI adapters for industrial and high availability applications, including networking and telecom.

The IOP 480 has the features required to enable live-insertion Hot Swap of CompactPCI adapters. The IOP 480 PICMG v2.1 compatible Hot Swap

Friendly PCI interface includes both Hot Swap Capable and Friendly functions:

Hot Swap Capable

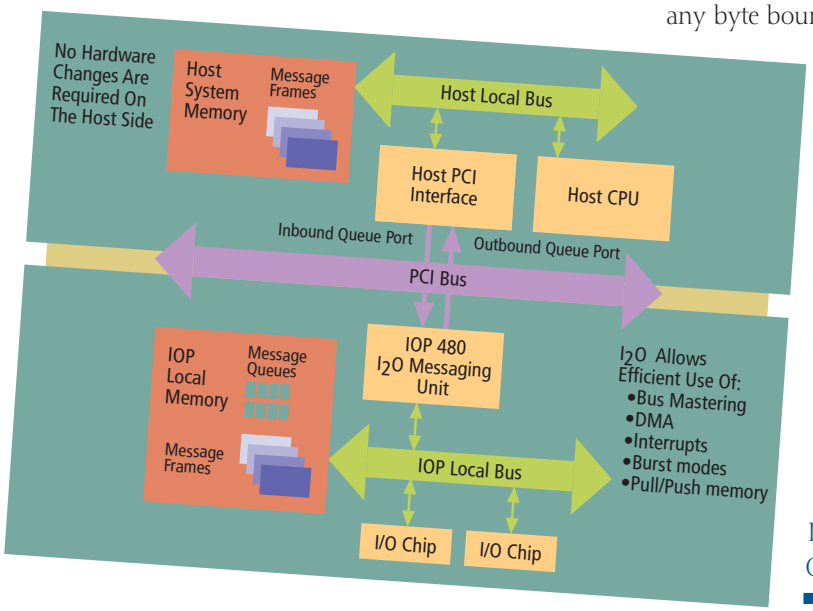
- PCI specification v2.1 or better
- Tolerant of V_{CC} from early power
- Tolerant of asynchronous reset
- Tolerant of precharge voltage
- Has limited I/O pin leakage at precharge voltage

Hot Swap Friendly

- Incorporates the Hot Swap Control/Status register (HS_CSR)
- Incorporates an Extended Capability Pointer (ECP) mechanism
- Incorporated added resources for software control of ENUM#, the ejector switch, and the status LED, which indicates to the user insertion/removal okay

PCI Embedded Host Designs

The IOP 480 provides a complete solution for PCI host embedded designs, such as network switches and routers, printer engines, set-top boxes, and industrial equipment. IOP 480 support for Type 0 and Type 1 PCI configuration cycles allows it to configure other PCI devices or cards on the PCI bus. The IOP 480 also provides a PCI Bus arbiter with support for up to three PCI Bus master devices or PCI slots.



Typical I_2O System Design

Additional Features

PowerPC RISC 32-Bit CPU

- 66MHz PowerPC RISC 32-bit core
- Thirty-two 32-bit general purpose registers
- Hardware multiply and divide
- MMU provides translation of logical address space into physical addresses
- Code Compatible with PowerPC User Instruction Set Architecture and Development Tools
- Separate 4KB-instruction cache and write-back/write-through 2KB data cache
- Four timer functions: time base, programmable interval timer (PIT), fixed interval timer (FIT), and a watchdog timer

PCI Bus Controller

- Compliant with all aspects of PCI specification v2.1 and v2.2, including PCI Power Management Features
- PCI Dual Address Cycle enables 64-bit adapter addressing in 64-bit PCI host systems
- Fully supports the Vital Product Data (VPD) PCI extension, which provides an alternate access method other than Expansion ROM for Vital Product Data
- Six FIFOs for concurrent zero wait-state burst in Initiator, Target, and DMA modes
- Interrupt Generator–The PCI controller can generate PCI and local interrupts to the internal interrupt controller from several sources, including PCI Interrupt, SERR, and PERR.
- Asynchronous Bus Clocks–The Local Bus interface runs from a local system clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock.
- The IOP 480 requires 3.3V V_{CC} and provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses. It can support universal PCI adapter designs.
- Serial EEPROM Interface–The IOP 480 provides an interface for an optional serial EEPROM, which can be used to load configuration information. This is useful for loading information that is unique to a particular adapter (such as Network ID or Vendor ID).
- Mailbox Registers–The PCI controller contains eight 32-bit mailbox registers that may be accessed from either the PCI Bus or the Local Bus.
- Doorbell Registers–The PCI controller includes two 32-bit doorbell registers. One generates interrupts from the PCI Bus, through the interrupt controller, to the Local Bus. The other generates interrupts from the Local Bus, through the interrupt controller, to the PCI Bus.
- Unaligned DMA Transfer Support–The PCI controller can transfer data on any byte boundary.
- Big/Little Endian Conversion–The PCI controller supports dynamic switching between Big Endian and Little Endian data for byte, word, or longword (Lword) transfers.

JTAG Interface

- IEEE 1149.1 JTAG Boundary Scan interface
- Used for Testing and PowerPC debug

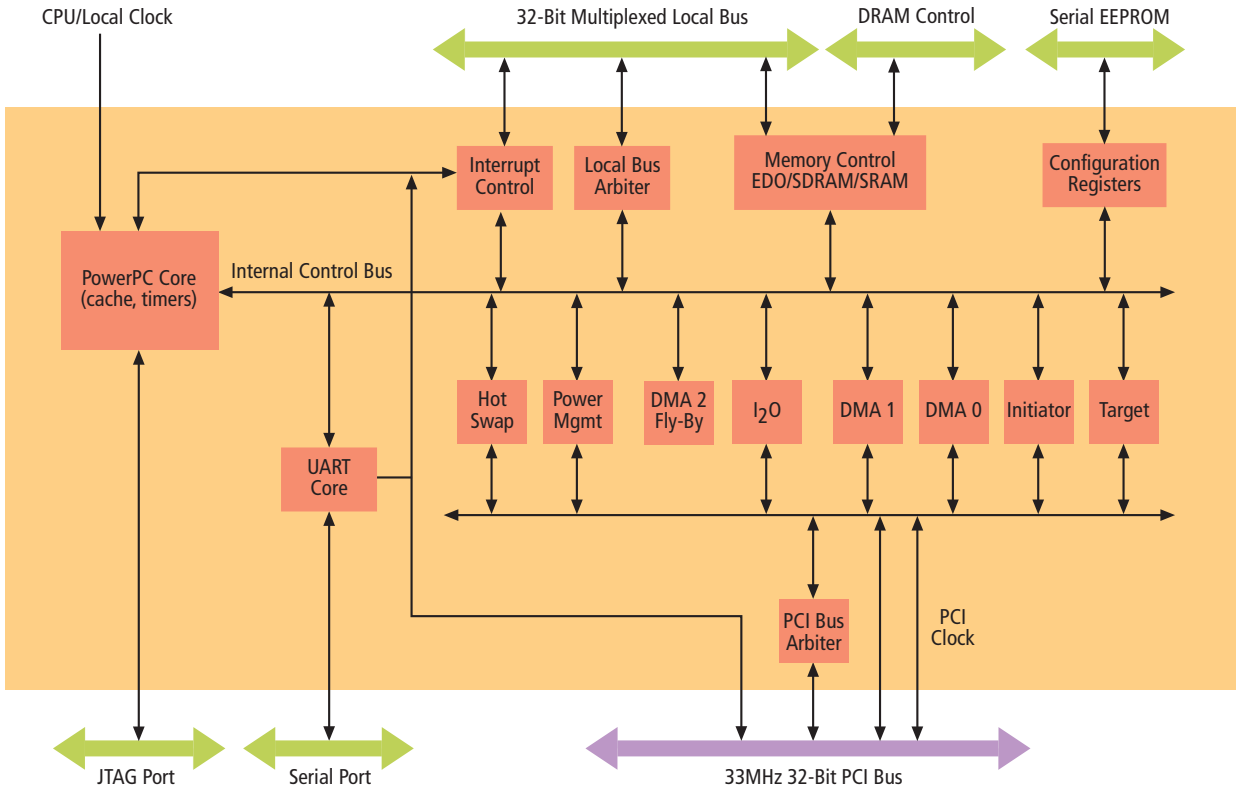
Programmable Interrupt Controller

- Critical Interrupt input (from external devices)
- External Interrupt input (from external devices)
- Timer and debug event interrupts
- Interrupts programmable as either active-high or active-low, and maskable

Memory Controller

- Supports up to 256MB in four banks of 32-bit SDRAM/EDO DRAM memory devices
- Supports up to four banks of 8-, 16-, 32-bit SRAM memory devices
- Separate memory control signals

PLX IOP 480 Block Diagram



Local Bus Interface

- Multiplexed 32-bit external bus
- J-type interface compatible with PLX PCI 9080 J Mode industry-standard signaling
- Supports 8-, 16-, or 32-bit peripherals
- Big-Endian or Little-Endian device attachment
- Programmable wait states
- Up to four external programmable peripherals/memory regions

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Local Bus Arbiter

- Supports two external Local Bus Master devices

Programmable Chip Selects

- Provides chip select pins for up to four external I/O or memory mapped devices (non-SDRAM) connected to the Local Bus
- Each chip select is programmable for bus width and wait states

Serial Port

- Debug Serial UART port for communication with serial devices
- TTL-level RX and TX signals

Development Tool Support

The IOP 480 is supported by a wide variety of development tools, including the IBM High C/C++ Compiler, IBM RISCWatch® and RISCTrace® emulator, third party compilers, debuggers, real time operating systems, and other tools available through the IBM PowerPC Embedded Tools Program.

The IOP 480 is fully compatible with PLX PCI SDK and I_2O SDK software development kits, which allow quick and easy development of high performance local and host PCI software through standard APIs, I_2O messaging protocols, PCI debug tools, and example device drivers.

IOP 480 design support is provided through Reference Design Kits (RDK) which provide a flexible IOP development board, complete with Orcad schematics, documentation, and software. IOP 480 simulation models will be supported by third party vendors.

Preliminary Information