IOP 480 SBC AN

July 5, 2000
Version 2.0

IOP 480 Single Board Computer Application Note

Features

The IOP 480 SBC is a PCI and local bus, single board computer with the following features:

- PLX IOP 480 I/O Processor with 32-bit, 66 MHz PowerPC RISC core
- SDRAM and Flash Memory Controller integrated within the IOP 480
- 8 Mbyte single chip SDRAM
- Socketed 512 Kbytes Flash memory
- Socketed 4 Kbit Serial EEPROM
- IBM RISCWatch® / JTAG connector
- IBM RISCTrace® connector
- DB-9 serial port connected to internal UART of the IOP 480
- 2x10 logic analyzer headers for IOP 480 local signals
- Two 400Mbit/s IEEE 1394 ports
- Single 100Mbit/s-ethernet port
- Super I/O chip containing keyboard and mouse controller, two UARTs, standard IBM parallel port, and GPIO pins
- 12 Mbit/s USB port
- Three PCI expansion sites: PCI rev 2.2, PC-MIP, PMC
- PLL clock driver on the Local bus providing divide-by-two clock for some peripheral devices

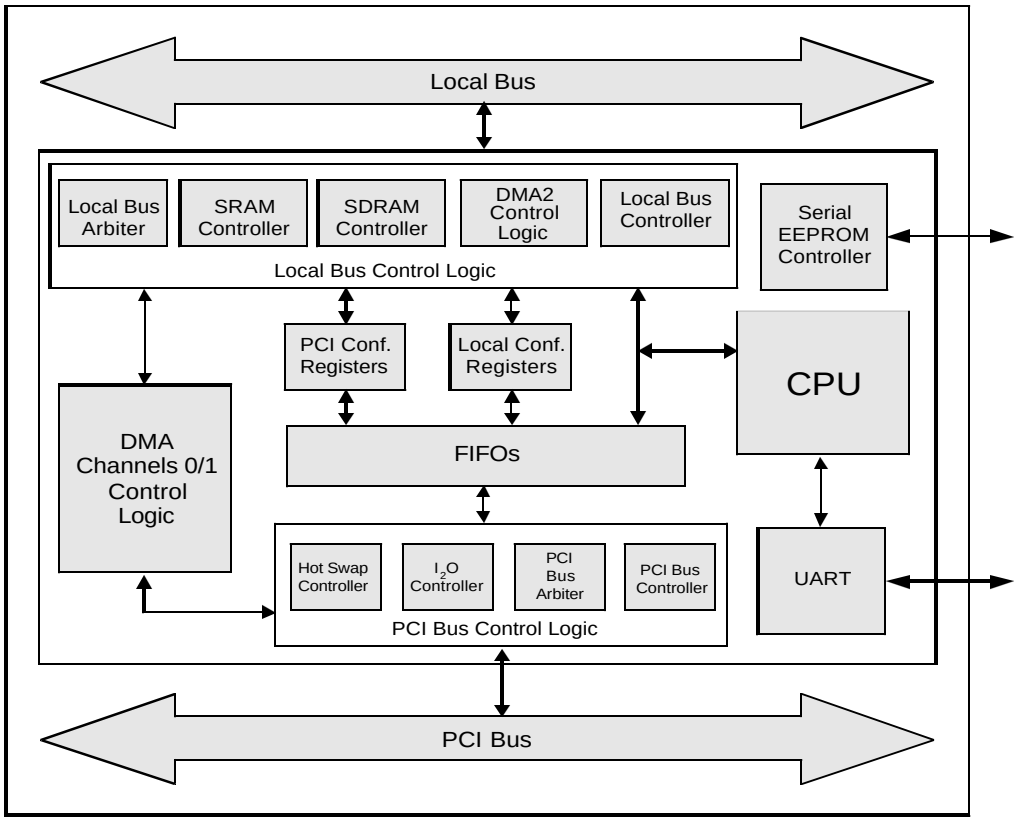

Figure 1. IOP 480 Block Diagram

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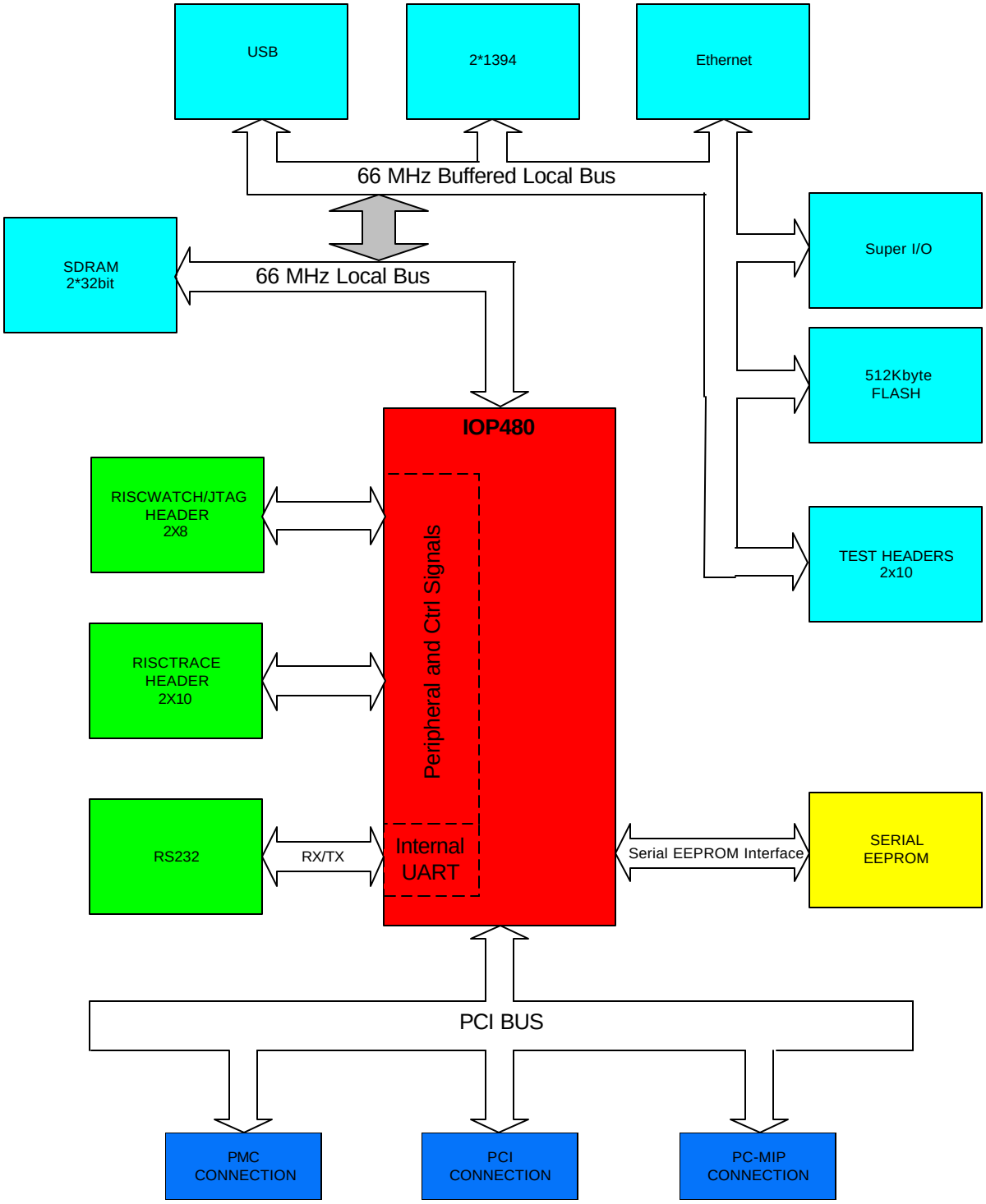

Figure 2. IOP 480 SBC Block Diagram

2. IOP 480 Architecture

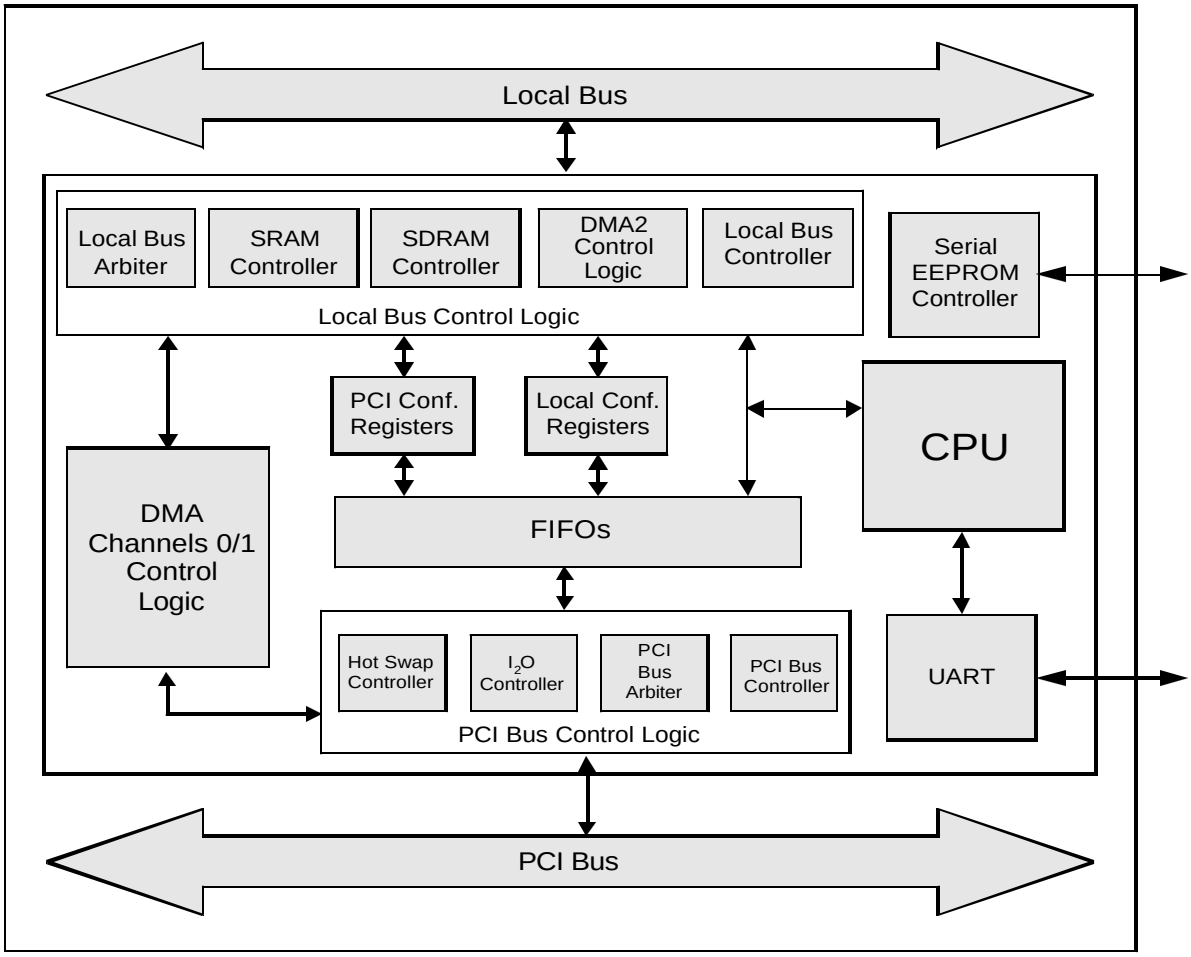

Figure 3. IOP 480 Block Diagram

The IOP 480 is an I/O Processor with a 32-bit, 66 MHz PowerPC RISC core, an integrated 32-bit PCI Bus interface, 3 DMA controllers, a powerful memory controller, PCI and Local Arbiters, and a UART. As shown in Figure 3, the IOP 480 RISC core, memory controller, and the Local bus run at 66 MHz, while the PCI interface runs at 33 MHz.

The integrated memory controller can support SDRAM, FLASH, SRAM, ROM, and other types of memory and peripherals.

When the IOP 480 is a Local bus master there are six memory regions:

- LCS0#
- LCS1#
- LCS2#
- LCS3#
- DRAM
- DEFAULT

The first four regions are the local chip select regions, used for SRAM or peripheral devices. The fifth space is the DRAM space. These five bus regions have registers describing, along with other items, the range of addresses each region decodes, the number of WAITSTATEs to insert during bus cycles, and burst qualities. The last region is the DEFAULT bus region. Any address that does not fall into the first five bus regions falls into the DEFAULT region. In this region all transactions are terminated with the assertion of the READY# signal.

3. IOP 480 SBC Hardware Architecture

This section provides a detailed description of the hardware of the IOP 480 SBC.

3.1 Hardware Memory Map

Table 1. IOP 480 SBC Memory Map shows the memory map of the IOP 480 SBC.

Address Range	Device	Bus Region	Comments
FFFF FFFF FFF8 0000	IOP 480 Boot Flash 512 Kbytes	LCS0#	8-bit wide accesses only
FFF7 FFFF F000 0000	Unused	–	–
EFFF FFFF E000 0000	Unused	–	–
DFFF FFFF D000 0000	Unused	–	–
CFFF FFFF C000 0000	Unused	–	–
BFFF FFFF B000 0000	Unused	–	–
AFFF FFFF A000 0000	Unused	–	–
8FFF FFFF 8010 0000	Unused	–	–
800F FFFF 8000 0000	LSI Ethernet Receive FIFO LSI Ethernet Transmit FIFO Lucent 1394 Link Controller	LCS3#	32-bit wide accesses, 33MHz clock synchronous with 66MHz bus clock
7FFF FFFF 6010 0000	Unused	–	–
600F FFFF 6000 0000	Lucent USS 820 USB Controller Winbond Super IO chip	LCS1#	8-bit wide accesses, asynchronous to local bus clock
5FFF FFFF 5000 0000	–	–	–
4FFF FFFF 4000 0000	Unused	–	–
3FFF FFFF 3000 0000	Unused	–	–
2FFF FFFF 2000 0000	LSI Ethernet Register Interface	LCS2#	16-bit wide accesses, asynchronous to local bus
1000 0024 1000 0000	IOP 480 Internal UART	–	IOP 480 CPU core accesses only
0FFF FFFF 0200 0000	Unused	–	–
01FF FFFF 0000 0000	SDRAM 32 Mbytes Decoded	DRAM (MCS0#)	32-bit wide access
FFFF FFFF FFF8 0000	IOP 480 Boot Flash 512 Kbytes	LCS0#	8-bit wide accesses only
FFF7 FFFF F000 0000	Unused	–	
BFFF FFFF B000 0000	Lucent 2 port 1394 Link Controller	DEFAULT*	32-bit wide accesses, 33MHz clock synchronous with 66MHz bus clock
AFFF FFFF A000 0000	Unused	–	

9FFF FFFF 9000 0000	LSI Ethernet Transmit FIFO	DEFAULT*	32-bit wide accesses, 33MHz clock synchronous with 66MHz bus clock
8FFF FFFF 8000 0000	LSI Ethernet Receive FIFO	DEFAULT*	32-bit wide accesses, 33MHz clock synchronous with 66MHz bus clock
7FFF FFFF 7000 0000	Winbond Super I/O	LCS1#	16-bit wide accesses, asynchronous to local bus clock
6FFF FFFF 6000 0000	Lucent USS 820 USB Controller	LCS2#	8-bit wide accesses, asynchronous to local bus clock
5FFF FFFF 5000 0000	Unused	–	
4FFF FFFF 4000 0000	Unused	–	
3FFF FFFF 3000 0000	Unused	–	
2FFF FFFF 2000 0000	LSI Ethernet Register Interface	LCS3#	16-bit wide accesses, asynchronous to local bus clock
1000 0024 1000 0000	IOP 480 Internal UART	–	IOP 480 CPU core accesses only
0FFF FFFF 0200 0000	Unused	–	
01FF FFFF 0000 0000	SDRAM 32 Mbytes Decoded	DRAM (MCS0#)	32-bit wide access

***Chip selects are decoded externally**

Table 1. IOP 480 SBC Memory Map

3.2 Chip Selects

The four local chip select signals are used to enable the FLASH device and local peripheral devices. LCS0# enables the FLASH device, and LCS2# enables the LSI Ethernet register interface. LCS1# and LCS3# are described in more detail.

3.2.1 LCS1#

LCS1#, along with external logic gates, is used to enable the Lucent USB device and the Winbond Super I/O chip. Both devices have 8-bit data access, are asynchronous to the local clock, and have very similar timing parameters requiring the same internal programmed WAITSTATES on the IOP 480. The LCS1# signal is first inverted and is then NANDed with MA15 to produce the Super I/O chip select signal. MA15 is actually local address bit 17, since for 8 bit accesses; MA0 is local address bit 2. This puts the Super I/O in the address range 6002 0000 to 6002 FFFF. Similarly, the Super I/O chip select signal is produced from MA16 (LA18) and LCS1#, putting it in the address ranges 6004 0000 to 6004 FFFF.

3.2.2 LCS3#

LCS3# is decoded with external logic to enable the ethernet transmit FIFO, ethernet receive FIFO, and 1394 link controller. All of the above devices have 32 bit data bus access, are clocked at 33MHz, which is synchronized the local clock, and terminate transactions by asserting the IOP 480's READY# signal. Using similar logic as LCS1#, the devices are located in the following addresses:

Ethernet receive FIFO: 8000 4000
Ethernet transmit FIFO: 8000 8000
1394 Link: 8001 0000 – 8001 FFFF

3.3 Interrupts

The IOP 480 I/O Processor has 5 PCI and 3 local interrupt pins. The PCI interrupts are PCI INTA#, PCI ENUM#, PCI PME, PCI SERR#, PCI PERR#. The PCI_ENUM# pin is not used on this SBC as the Hot Swap feature is not required for this type of application. The PCI_ENUM# pin would be applicable in CompactPCI systems. The behavior of the PCI INTA# pin is determined by the HMODE pin. The HMODE pin selects the mode for the IOP 480 as adapter or host. In the adapter mode, the PCI INTA# pin is an output only, while, in the host mode,

it is an input only. The SBC uses the IOP 480 in host mode, which makes the PCI INTA# pin an input. INTA# is common to all three PCI connectors.

All local interrupts are routed to the INTI pin. The IOP 480 can program this pin as active low or high. For the SBC this pin is set active low.

3.4 Microprocessor

The IOP 480 has a built-in PowerPC RISC core, compatible with the PowerPC Book D architecture from an instruction and register-level perspective. The maximum internal frequency and external local bus frequency of the IOP 480 Processor is 66 MHz. The local bus presented to the external world is the standard J-Mode multiplexed bus.

The processor has 4 Local bus Chip Select (LCS[3:0]#) pins used to select general memory and I/O devices, and 4 Memory Chip Select (MCS[3:0]#) pins dedicated to select EDO DRAM or SDRAM. The bus region descriptors for LCS[3:0]# and MCS[3:0]# can be programmed through their respective Bus Region Descriptor registers and Local Chip Select Control Timing registers to determine the bus width and timing for accesses to each region.

The IOP 480 can access 4 GB of address space, which is presented as a flat address space. The IOP 480 contains a Memory Management Unit (MMU) that provides address translation, protection functions, and storage attribute control for embedded applications. The MMU also supports demand-paged virtual memory and other management schemes that require precise control of logical-to-physical address mapping and flexible memory protection.

3.4.1 PCI Bus Interface

The IOP 480 has an integrated 32-bit PCI bus interface operating at 33 MHz. PCI bus operations can be initiated by a master on the Local bus, a master on the PCI Bus, or by the IOP 480's CPU. For the SBC, the IOP 480's CPU initiates PCI bus accesses. The IOP 480 has a 64-byte PCI Initiator Read FIFO and a 128-byte PCI Initiator Write FIFO.

Three PCI expansion sites are provided on the SBC:

- PCI rev 2.2
- PC-MIP
- PMC

Each PCI expansion site has its own REQUEST / GRANT pair, but all expansion sites share and use the same INTA# interrupt pin.

3.4.2 Local Bus Interface

The Local bus provides the address, data, and control path for non-PCI devices such as memory and peripherals. The Local bus is a 32-bit multiplexed bus, with bus memory regions that can be programmed for 8-, 16-, or 32-bit widths.

The IOP 480 can act as a master or slave on the Local bus. When the IOP 480 is acting as a Local bus slave, an external master on the Local bus can access all internal configuration registers, as well as perform PCI Initiator accesses to the PCI bus. When the IOP 480 is acting as a Local bus master, then the internal PCI Direct Slave controller, internal DMA controllers, or the internal IOP 480 CPU can perform transfers between the Local bus, internal registers, and FIFOs.

Transceivers are placed on the data and address buses to reduce excessive capacitive loading. Two 16 bit transceivers are placed on the LAD[0..31] bus signals between the IOP 480 and the FLASH, 1394, USB, ethernet, Super I/O devices and logic analyzer headers. Direction of data flow on the transceivers is controlled with the W/R_L signal. Series damping resistors are placed on both sides of the transceivers to minimize reflections.

Two uni-directional 16 bit buffers are placed on the MA[0…15] lines to buffer the address signals to the FLASH, 1394, USB, ethernet, Super I/O devices, and logic analyzer devices. Additional series damping resistors are not required on the buffer, as it has built in 25-Ohm series resistors on its outputs.

The SDRAM data and address signals connect directly (excluding damping resistors) to the IOP 480.

3.4.3 Memory Controller

The IOP 480's memory controller has enhanced bursting capabilities allowing much higher data transfer rates than have previously been available. Burst transactions initiated by a local external master, the on-chip DMA controllers, or the PCI bus, can be unlimited in length if the Local Bus Latency Timer is disabled, or up to 256 clocks in length if enabled. This is true regardless of the type of memory being accessed, including synchronous

DRAM (SDRAM). In this manner, startup overhead of memories such as SDRAMs becomes negligible, allowing higher performance when using the memory subsystem. Burst READ/ WRITE is not supported for the SBC peripheral devices.

The IOP 480's integrated memory controller supports up to four banks of SRAM or similar devices using the LCS[3:0]# chip select pins and up to four banks of either Extended Data Out (EDO) DRAM or Synchronous DRAM (SDRAM) using the MCS[3:0]# chip select pins. Because the LCS[3:0]# descriptors and timing are programmable, they can also be used to access ROMs, Flash memory, and I/O peripheral devices. The four different masters that can access these banks are the external PCI agent, internal DMA channels, internal IOP 480 CPU, and an external Local Bus Master.

3.4.4 Oscillator / Local Bus Clock

A 66 MHz oscillator provides the clock to a PLL clock driver whose outputs go to the IOP 480 Processor core and synchronous memory devices on the Local bus. Both the IOP 480 core and the Local bus interface operate at 66 MHz.

Several devices on the local bus cannot operate at speeds of 66MHz, so a 33MHz-clock signal is produced from the PLL clock driver. This clock is coherent with the 66MHz clock. Additional timing is controlled through WAITSTATEs.

3.4.5 IBM RISCWatch® / JTAG Connector

The IBM RISCWatch/JTAG Connector provides the capability for on-chip emulation, using IBM or compatible tools, and JTAG boundary scan, which is used for device testing during manufacturing. This connector is a 2x8-pin dual-in-line header.

The RISCWatch / JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the IEEE 1149.1 specification for specific extensions, are compatible with standard JTAG hardware for boundary-scan system testing.

For the IBM RISCWatch debug tool, edit the rwppc.env file as shown below. The rwppc.env file resides in the rwppc subdirectory belonging to the IBM RISCWatch software.

1. Change to PROC = 401D2
2. Add line IR_SEG0 = 100

The RISCWatch debugger type is specified in the rwppc.env file. For ethernet port RISCWatch debugger, the TARGET_TYPE = jtag_eth. For parallel port RISCWatch debugger TARGET_TYPE = jtag_par[n]. Refer to the IBM RISCWatch Debugger User's Guide for additional information. For the ethernet port RISCWatch debugger, use the RISCWatch software Version 4.3 or higher. For the parallel port RISCWatch debugger, use the RISCWatch software Version 4.4 or higher.

3.4.6 IBM RISCTrace® Connector

The IBM RISCTrace Connector provides real time trace and bus status information. There are six (6) Trace Status pins TS1 – TS6. TS0 on the RISCTrace Connector is tied to ground. This connector is a 2x10 pin dual-in-line header. Both the RISCWatch and RISCTrace debugger tools can use the data gathered from the RISCTrace connector to trace code running on the IOP 480 I/O Processor.

To enable the RISCTrace function in the IOP 480, RISCTrace Enable bit (bit4) and Serial EEPROM Data Output Enable bit (bit23) of the Device Initialization register (PCI Offset: 80h and Local Offset: 80h) must be set to 1. The user may use PLX's software tool PLXMon in PCI SDK 3.0 or higher to enable these bits through a simple graphical user interface.

Note: The accesses to the UART and to serial EEPROM will be disabled while the RISCTrace is running. This is due to the fact that these pins are multiplexed with the trace pins TS[1:6].

3.5 Serial EEPROM

The serial EEPROM is a MN93CS66LEN 4 Kbit serial EEPROM, which is used to initialize the IOP 480 after reset. After reset, while the IOP 480 attempts to read the serial EEPROM to determine its presence and during serial EEPROM load, the following occurs: 1) IOP 480 CPU is held in reset, 2) PCI accesses are retried, and 3) Local accesses are held off by not asserting READY.

3.6 Flash Memory

The Flash Memory is a 512K x 8 bit, 120 nanosecond, socketed device. This memory contains the code for the IOP 480 I/O Processor to execute after coming out of reset.

The Flash is both readable and writeable by any bus master device on the board. Note that the flash is an

8-bit only device, and therefore the bus width of LCS0# must be programmed to 8 bits. Both LBE0 and LBE1 are used to provide the lower 2 bits of address to the device.

Because the *Flash Memory* is relatively slow, flash code should be copied into SDRAM and executed from there.

3.6.1 Flash Control

The Flash memory controller is provided using the IOP 480 integrated memory controller. The memory controller uses the signal LCS0# to select the 512K x 8 bit Flash memory. This chip select can be programmed through the LCS0 Bus Region Descriptor, Write Timing, Read Timing, Base Address, and Range registers. It is possible to write-protect the Flash through software register programming.

3.7 SDRAM Memory

The IOP 480 has 64 Mbits of SDRAM. This is provided on a single chip from Samsung and is organized as 2M X 32 bits. For more information on connecting various SDRAM architectures to the IOP 480, see the IOP 480/SDRAM AN.

3.7.1 SDRAM Controller

The SDRAM controller is part of the integrated memory controller of the IOP 480 and is fully software-programmable. After the SDRAMs are powered up and have a stable clock, no commands are issued for at least 200 µsec to allow for pre-charging of the array. This time-out is based on 13,200 clock ticks at the local clock frequency of 66 MHz. The SDRAM's mode register is loaded during initialization by the IOP 480 memory controller and is used to set the operating parameters of the SDRAM.

3.8 Series Damping Resistors

Series damping resistors are used on many signals of the Local bus to minimize voltage overshoot and undershoot caused by reflections. For output pins such as MA, a single series resistor is placed close to the driver or the source of the signal (the IOP 480). For bi-directional pins such as LAD, two series resistors are used whereby each resistor is placed close to each end of the LAD signal trace.

3.9 Internal Serial Port

The IOP 480 SBC contains three UARTS: one internal UART on the IOP 480, and two UARTS on the Super I/O chip. The serial ports for the IOP 480 SBC are standard RS-232C DB-9 connectors. The DB-9 connector provides a serial connection to the UART of the IOP 480 through an external RS-232 voltage converter. This UART is built-in to the IOP 480 and is compatible with the industry-standard 16C450 design except for the hardware handshaking signals.

3.10 Power Supply

All devices on the IOP 480 SBC are either 3.3V or 5V devices. Power to the board is supplied through a standard 12-pin PC power connector. The pin connections are shown Figure 4.

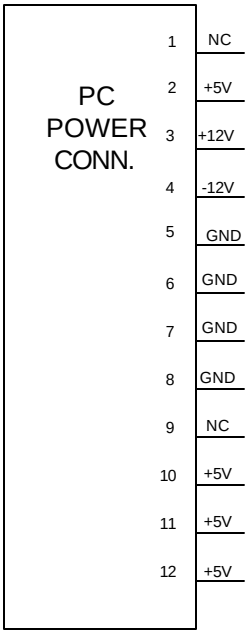

Figure 4. Power Conn pin diagram

3.11 Test Headers

Test headers are implemented with standard 0.1", 2x10 headers. All of the important signals are connected to test headers. The test headers allow for easy debugging as they can be readily hooked up to either the HP logic analyzer probe termination adapter 01650-63203 or DLI logic analyzer probe adapter.

Note: Pins 1 of JP5 and JP8 are at the bottom right corner, while pin 1 of JP 3, JP4, JP6, and JP7 are at the top left corner of the headers.

3.12 Reset Circuitry

3.12.1 IOP 480 Reset

The HMODE pin determines the IOP 480 reset behavior. When this pin is high, the IOP 480 is in host mode. When this pin is low, the IOP 480 is in adapter mode. In the adapter mode, the IOP 480 Local RESET# pin acts as an output only.

The HMODE pin is pulled up since the SBC is designed for PCI host mode. The PCI bus RST# will be driven when the local RESET# pin is asserted, the software bit is set, or the IOP 480 CPU initiates an external reset. The local RESET# pin is asserted by a pushbutton switch; this signal is also sent to the reset inputs of the local bus devices.

When the IOP 480 CPU executes a system-reset instruction or detects the reset input, it drives the Local RESET# pin for at least 62 clocks and fetches its first instruction from address 0xFFFF_FFFC.

3.12.2 Power-On-Reset

Power-on-reset is controlled by an external 3.3-Volt power supply supervisor. The valid power-on-reset period is 1ms, which is hardwired into the supply supervisor IC. This power-on-reset circuit is used to provide a reset to all Local bus devices.

3.13 1394 Ports

The SBC is provided with two 1394 ports to allow daisy-chaining of devices. The ports support data rates up to 400 Mbit/s. The 1394 is implemented using a Link and Phy pair. The Link chip is a Texas Instruments TSB12LV01, and the Phy chip is a Lucent FW802. Capacitive isolation is provided between the Link and Phy on all Link-Phy interface signals. A small signal return path is provided between the Phy and Link grounds to reduce noise in the Phy's analog circuitry.

The Link chip is located in the LCS3# bus region. The maximum bus clock frequency of the Link chip is 48 MHz. For this reason the Link is not clocked at 66MHz, but at 33MHz, which is obtained from the PLL clock driver. All transactions are then terminated by the CA# signal which is sent to the READY# signal on the IOP 480. Some logic is required to produce the single CS# pulse needed to start the read/write cycle.

3.14 Ethernet

A single 100Mbit/s-ethernet port is provided on the SBC. This is provided by a MAC / Phy pair of chips from LSI / SEEQ. The MAC has three chip selects. The first two are enables for the RX and TX FIFOS. The third is an enable for the register interface.

Data transfer on the TX and RX interfaces is synchronous to the local bus clock. The maximum clock frequency is specified as 33MHz. This frequency is obtained from the PLL clock driver. Although the 33MHz clock is in phase with the 66MHz clock, it is not known whether it is in a high or low state at the beginning of a read/write cycle. If the 33MHz clock is high at the beginning of the bus cycle, the bus signals will be latched half a 33MHz-clock period (one 66MHz-clock period) later than they would if the clock were low at the start of the cycle. For this reason, internal programmed WAITSTATEs in the IOP 480 cannot be used. As the MAC does not have a READY# signal of its own some glue logic is required to produce this signal. For a read cycle, a single 33MHz period active low read strobe is generated. This signal is then delayed by a 33MHz clock cycle and is sent to the IOP 480 READY# signal. The write cycle is very similar except that the write strobe is initially delayed by one 66MHz clock cycle to ensure valid data is on the bus; this signal is then delayed by an additional 66MHz clock cycle before it is sent to the IOP 480 READY# signal. The ethernet transmit and receive FIFOs reside in the LCS3# bus region along with the 1394 Link controller.

Before accessing the ethernet transmit and receive FIFOs, the RXRDY and TXRDY signals need to be queried. These signals indicate whether the FIFO threshold values have been reached. (i.e. If RXRDY is low, the RX FIFO is below the threshold number of double words available to be read. If TXRDY is low, the TX FIFO is below the threshold double word spaces available for writing.) The threshold values are configurable through the MAC register interface. Reading GP11 and GP12 respectively on the Super I/O chip accesses the RXRDY and TXRDY signals. The RXDY and TXRDY must first be enabled by setting the GP25 and GP13 signals low on the Super I/O chip.

The ethernet register interface is asynchronous to the Local bus clock and timing is therefore best controlled through internal programmed WAITSTATEs. The ethernet registers and located in the LCS2# region. The register access is 16 bit whereas the FIFOs accesses are 32 bit.

The MAC interfaces directly with the Phy with no required glue logic. The Phy is matched to a 100 Ohm unshielded twisted pair cable. Analog isolation is provided through a single transformer module chip from Pulse.

3.15 Super I/O

A Super I/O chip from Winbond is provided on the SBC to interface several serial/parallel devices to the IOP 480. The Super I/O chip provides an interface to many different devices. The following devices were chosen: 2 UARTS, keyboard and mouse controller, standard IBM parallel port, and several GPIO pins.

The Super I/O chip resides in bus region LCS1# and its timing is controlled by internally programmed WAITSTATEs on the IOP 480.

3.15.1 UARTs

As with the internal UART on the IOP 480, the UARTs are accessed externally through RS-232C DB-9 connectors. The UARTs are connected to the DB-9 connectors through a voltage converter. The UARTs can support data transmission rates of up to 12.5Mbit/s.

3.15.2 Keyboard / Mouse Controller

The Super I/O chip has a built in keyboard and mouse controller. The keyboard / mouse controller is a standard 8042. The keyboard/ mouse controller is accessed by an 8 bit input buffer and an 8 bit output buffer along with a set of control registers.

3.15.3 Parallel Port

The Super I/O chip allows several types of parallel ports to be connected. For simplicity, a standard IBM parallel port was chosen. This provides an 8-bit data bus along with the standard handshaking signals needed to connect devices such as a printer. The external connector is a DB-25 female connector.

3.15.4 GPIO

Several GPIO pins on the Super I/O chip are used to control the ethernet MAC operation.

3.16 USB

A single USB port is provided on the SBC. The USB controller is a Lucent USS-820C chip. The USS 820 local bus interface is asynchronous to the local clock. Its timing can be controlled by internally programmed WAITSTATEs in the IOP 480. The USB resides in the LCS2# bus region. Data transfer between the IOP 480 and USB is 8 bit. Since the SBC is self-powered it does not receive power from the USB bus neither does it provide power to the USB bus since it is not a USB host.

4. References

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5. Bill of Materials / Schematics

The following pages contain the bill of materials and the schematics for the IOP 480 SBC.

Table 2. Bill of Materials

Item	Qty.	Reference	DESCRIPTION	MANUFACTURER	PART NUMBER
SURFACE MOUNT COMPONENTS					
1	1	U1	IOP 480, PCI 32 bit I/O Processor	PLX	IOP480-AA66P1 IOP 480-AA66B1
2	1	U20	400Mb/s 1394 Link Controller	Texas Instruments	TSB12LV01
3	1	U25	2 port 400Mb/s 1394 Phy	Lucent	FW802
4	1	U33	LSI/SEEQ 100Mb/s ethernet MAC	LSI/SEEQ	80C300
5	1	U26	LSI/SEEQ Ethernet Phy	LSI/SEEQ	80221
6	1	U27	Ethernet transformer module	Pulse	H1038
7	1	U40	Winbond Super I/O chip	Winbond	W838777TF
8	1	U46	Lucent USB controller	Lucent	USS-820
9	1	U6	IC, 3.3V Regulator, 3A	Linear	LT1587CM-3.3
10	3	U10 U44 U45	RS232 Transceiver	Maxim	MAX3227CAE
11	1	U11	Reset Controller, 1ms reset	Maxim	MAX6306UK20D3-T
12	1	U12	Bus switch, 1 bit	Fairchild	NC7SZD384P5
13	4	U13 U17 U48 U64	UHS Single Inverter	Fairchild	NC7SZ04
14	2	U49 U51	16 Bit Transparent transceiver	Fairchild	74ABT16245
15	1	U15	UHS Single Buffer	Fairchild	NC7SZ125
16	1	U16	Dual quad input AND gate	Fairchild	DM74AS21
17	2	U52 U55	16 Bit address buffer	Fairchild	74ABT162244
18	2	U53 U54	Quad 2 input NAND gate	Fairchild	DM74AS00
19	1	U2	512KX8bit Flash	Atmel	At49LV04-12JC
20	8	U21 U57 U59 U61 U73 U74 U80 U81	UHS Single 2-input OR gate	Fairchild	NC7SZ32
21	24	U22 U23 U34 U58 U60 U65 U66 U67 U68 U69 U70 U71 U72 U75 U76 U78 U79 U82 U83 U85 U86 U87 U88 U89	UHS D-Flip Flop	Fairchild	NC7SZ175
22	3	U24 U77 U84	UHS Single 2-input AND gate	Fairchild	NC7SZ08
23	1	U32	Quad 2-input AND gate	Fairchild	DM74AS08
24	1	U39	32.768 Oscillator 5V, SMD	MTRON	M5M13TAN32.7680
25	1	U43	48 MHz Oscillator 5V,SMT	MTRON	M5M13TAN48.0000
26	1	U5	PLL clock driver with /2, *2 outputs	Quality Sem.	QS5LV919
27	1	U7	66.666MHz Oscillator, 3.3V, SMD	ECS	OECS-3953C-666-TR

28	1	U8	Zero delay clock buffer	Cypress	CY2305
29	1	U9	33MHz Oscillator, 3.3V, SMD	MTRON	M3M13TGN33.0000
30	1	Q1	2N7002, TMOS FET	Motorola	2N7002LT1
31	40	C7 C8 C9 C10 C11 C18 C20 C22 C29 C30 C35 C44 C46 C48 C50 C52 C75 C92 C93 C100 C101 C102 C103 C104 C105 C106 C108 C110 C112 C114 C116 C118 C120 C122 C124 C138 C144 C146 C148 C150 C151 C152 C153 C154 C156 C158 C160 C162 C164 C166 C168 C170	0.01uF SMT NP Cer. Cap. 50V 20% 0805	Kemet	C0805C103M5UAC
32	61	C2 C3 C4 C5 C6 C12 C14 C15 C16 C17 C19 C25 C26 C27 C28 C36 C38 C42 C43 C45 C47 C49 C51 C53 C73 C76 C78 C79 C80 C81 C82 C83 C84 C85 C86 C94 C95 C96 C97 C98 C99 C107 C109 C111 C113 C115 C117 C119 C121 C123 C125 C127 C132 C133 C134 C139 C142 C143 C145 C147 C149 C155 C157 C159 C161 C163 C167 C169	0.1uF SMT NP Cer. Cap. 50V 20% 0805	Kemet	C0805C104M5UAC
33	7	C1 C13 C21 C23 C24 C34 C77	10uF SMT P Tant. Cap. 20V 20% C CASE	Panasonic	ECS-T1DC106R
34	12	C37 C39 C40 C41 C126 C128 C129 C130 C131 C135 C136 C137	0.1uF SMT P TANT. Cap. 35V 20% A CASE	Kemet	T491A104K035AS
35	18	C55 C56 C57 C58 C59 C60 C62 C63 C64 C65 C66 C68 C74 C87 C88 C89 C90 C91	1000pF SMT NP Cer Cap. 50V 10% 0805	Kemet	C0805C102K5RAC
36	1	C70	0.033uF SMT NP Chip Cap. 50V 5% 1210	Panasonic	ECW-U1H333JB5
37	2	C69 C54	0.33uF SMT NP Chip Cap. 16V 5% 2416	Panasonic	ECW-U1C334JB9
38	2	C72 C61	220pF SMT NP Chip Cap. 50V 5% 0805	Panasonic	ECH-U1H221JB5
39	2	C71 C67	22pF SMT NP Chip Cap. 50V 5% 0805	Panasonic	ECU-V1H220JCN

40	2	C32 C33	22uF SMT P Electro. Cap. 50V E can	Panasonic	ECE-V1HA220P
41	1	C31	22uF SMT P Electro. Cap. 25V E can	Panasonic	ECE-V1A221P
42	2	C140 C141	15pF SMT NP Chip Cap. 50V 5% 0805	Panasonic	ECU-V1H220JCN
43	1	D1	LED, red, SMT	Hewlett Packard	HSMS-C650
44	1	D2	0.5A, 20V diode	Motorola	MBR0520L
45	1	JP1	Header, 20 pins, dual, 0.1", SMT	Samtec	TSM-110-01-L-DV-A
46	6	JP3 JP4 JP5 JP6 JP7 JP8	Header, 20 pins, dual, 0.1", SMT	Samtec	TSM-110-01-L-DV-A
47	1	JP2	Header, 16 pins, dual, SMT	Samtec	TSM-108-01-L-DV-A
48	1	J1	12 Pin connector, power_key	AMP	1-640383-2
49	1	J9	Thru hole, right angle PCB jack	Molex	43202
50	1	J10	Thru hole shielded kbd/mouse conn.	Molex	87220
51	1	J11	Thru hole shielded kbd/mouse conn.	Molex	87220
52	4	L1 L2 L3 L4	Ferrite, 500mA, 40Ohm, 0805	Steward	LIO805E400R
53	3	P1 P3 P4	Connector, DB9, plug SMT male	Kygon	K20HT-E9P-N
54	1	P2	Connector, 25 pin, SMT female	Molex	89221
55	1	SW1	Tact pushbutton switch	Omron	B3S-1002
56	1	Y1	24.576 MHz Crystal	MTRON	SX2090 24.5760
57	1	Y2	25 MHz Crystal	MTRON	SX2090 25.0000
58	1	Y3	12.000 MHz crystal	MTRON	SX2090 12.0000
59	1	J2	Universal 32 bit PCI edge connector	AMP	145098-1
60	4	J4 J3 J5 J6	64 position, SMT plug	AMP	120532-1
61	64	RN5 RN6 RN7 RN8 RN9 RN10 RN11 RN12 RN13 RN14 RN15 RN16 RN17 RN18 RN19 RN20 RN21 RN22 RN23 RN24 RN25 RN26 RN27 RN28 RN29 RN30 RN31 RN32 RN33 RN34 RN35 RN43 RN44 RN47 RN48 RN49 RN50 RN51 RN52 RN53 RN54 RN55 RN56 RN57 RN58 RN59 RN78 RN79 RN80 RN81 RN82 RN83 RN84 RN85 RN86 RN87 RN88 RN89 RN90 RN91 RN92 RN93 RN94 RN95	Resistor Network, 33 ohm, 5%	CTS	742-08-3-3303J-BK

62	23	R5 R6 R7 R8 R9 R10 R11 R12 R63 R64 R173 R174 R175 R176 R177 R178 R181 R182 R205 R206 R207 R208 R209	Resistor, Discrete, 33 Ohm, 5%	Philips	RC11J33R
63	9	RN36 RN37 RN38 RN39 RN40 RN41 RN42 RN45 RN46	Resistor Network, 10 Ohm, 5%	CTS	742-08-3-100-J-BK
64	13	RN60 RN61 RN62 RN63 RN69 RN70 RN71 RN72 RN73 RN74 RN75 RN76 RN77	Resistor Network, 10KOhm, 5%	CTS	742-08-3-103-J-BK
65	17	R1 R3 R13 R14 R70 R72 R73 R114 R184 R185 R186 R187 R210 R211 R212 R213 R214	Resistor Discrete, 10KOhm,5%	Philips	RC11J10K0
66	1	RN65	Resistor Network, 1KOhm, 5 %	CTS	742-08-3-102-J-BK
67	3	R2 R4 R16	Resistor Discrete, 1K, 5%	Philips	RC11J1K00
68	1	R15			
69	31	R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R32 R34 R36 R41 R42 R43 R44 R45 R46 R47 R49 R52 R54 R55 R56 R57 R58 R59 R60 R61 R62	Resistor Discrete, 8.2KOhm, 5%	Panasonic	ERJ-6GEYJ822V

70	101	R27 R28 R29 R30 R31 R33 R35 R37 R38 R39 R40 R48 R50 R51 R53 R75 R76 R77 R78 R79 R80 R81 R86 R94 R95 R96 R97 R100 R101 R102 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R128 R129 R131 R132 R133 R134 R137 R138 R139 R140 R141 R142 R143 R144 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R171 R201 R202 R203 R204 R218 R219 R220 R221 R224 R225 R226 R227 R228 R229 R230 R231 R232 R230 R231 R232 R233 R234 R235	Resistor Discrete, 5.1KOhm, 5%	Panasonic	ERJ-6GEYJ512V
71	8	R82 R83 R84 R85 R88 R89 R91 R92	Resistor Discrete, 56 Ohm, 5%	Panasonic	ERJ-6GEYJ560V
72	1	R87	Resistor Discrete, 2.49KOhm, 1%	Panasonic	ERJ-6ENF2491V
73	1	R90	Resistor Discrete, 100 Ohm, 5%	Panasonic	ERJ-6GEYJ101V
74	1	R93	Resistor Discrete, 390KOhm, 5%	Panasonic	ERJ-6GEYJ394V
75	1	R98	Resistor Discrete, 510KOhm, 5%	Panasonic	ERJ-6GEYJ514V
76	2	R99, R103	Resistor Discrete, 1.6KOhm, 5%	Panasonic	ERJ-6GEYJ162V
77	2	R194, R104	Resistor Discrete, 1.0Mohm, 5%	Panasonic	ERJ-6GEYJ105V
78	2	R105, R106	Resistor Discrete, 200Ohm, 5%	Panasonic	ERJ-6GEYJ201V
79	2	R107, R113	Resistor Discrete, 15 Ohm, 5%	Panasonic	ERJ-6GEYJ150V
80	2	R108, R109	Resistor Discrete, 36 Ohm, 5%	Panasonic	ERJ-6GEYJ360V
81	3	R110, R111, R112	Resistor Discrete, 75 Ohm, 5%	Panasonic	ERJ-6GEYJ750V
82	4	R145, R146, R147, R148	Resistor Discrete, 4.7KOhm, 5%	Panasonic	ERJ-6GEYJ472V
83	2	R188, R189	Resistor Discrete, 24 Ohm, 5%	Panasonic	ERJ-6GEYJ240V
84	2	R190, R191	Resistor Discrete, 1.5Mohm, 5%	Panasonic	ERJ-6GEYJ155V
85	1	R192	Resistor Discrete, 510KOhm, 5%	Panasonic	ERJ-6GEYJ514V
86	1	R193	Resistor Discrete, 1.5KOhm, 5%	Panasonic	ERJ-6GEYJ152V
87	1	R195	Resistor Discrete, 100KOhm, 5%	Panasonic	ERJ-6GEYJ104V

THRU HOLE COMPONENTS					
88	1	U47	USB type B receptacle, right angle, TH	Newnex	URB-1001
89	2	J7 J8	1394 Sock. TH, Right Angle, Shielded	Molex	53984-0611
90	1	J1	12 Pin connector, power_key	AMP	1-640383-2
91	1	J9	Thru hole, right angle PCB jack	Molex	43202
92	1	J10	Thru hole shielded kbd/mouse conn.	Molex	87220
93	1	J11	Thru hole shielded kbd/mouse conn.	Molex	87220
MANUALLY INSERTED COMPONENTS					
94	1	U4	Serial EEPROM, 4 Kbit	Fairchild	NM93CS66LEN
95	1	U3	8Megbyte SDRAM, 2MegX32bit	Samsung	KM432S2030C
PARTS THAT SHOULD NOT BE ASSEMBLED					
96	1	R200	Resistor Discrete, 10KOhm, 5%	Philips	RC11J10K0