IOP 480/SBSRAM AN

July 5, 2000
Version 2.0

IOP 480/SBSRAM
Application Note

Features

Two detailed implementations of IOP 480 I/O Processor to Synchronous Burst SRAM connection.

- Direct Connection
- High Performance Connection
- Synchronous Burst SRAM, 1 Mbit, 128K x 36, 32 data, 4 parity

General Description

This application note describes how to interface the PLX Technology IOP 480 to Synchronous Burst SRAM (SBSRAM). Two different implementations are shown. The first is a 'Direct' connection using no glue logic. The second is a High Performance (HP) connection using a CPLD.

The IOP 480 has PCI Initiator, DMA, and PCI Target data transfer capabilities. The PCI Initiator mode allows a device (IOP 480) on the Local bus to perform memory, I/O, and configuration cycles to the PCI bus. The PCI Target mode allows a master device on the PCI bus to access memory on the Local bus. The IOP 480 allows the Local bus to run asynchronously to the PCI bus through the use of bi-directional FIFOs. In this design example, the PCI bus runs at up to 33MHz while the IOP 480 Local bus is clocked at up to 66Mhz.

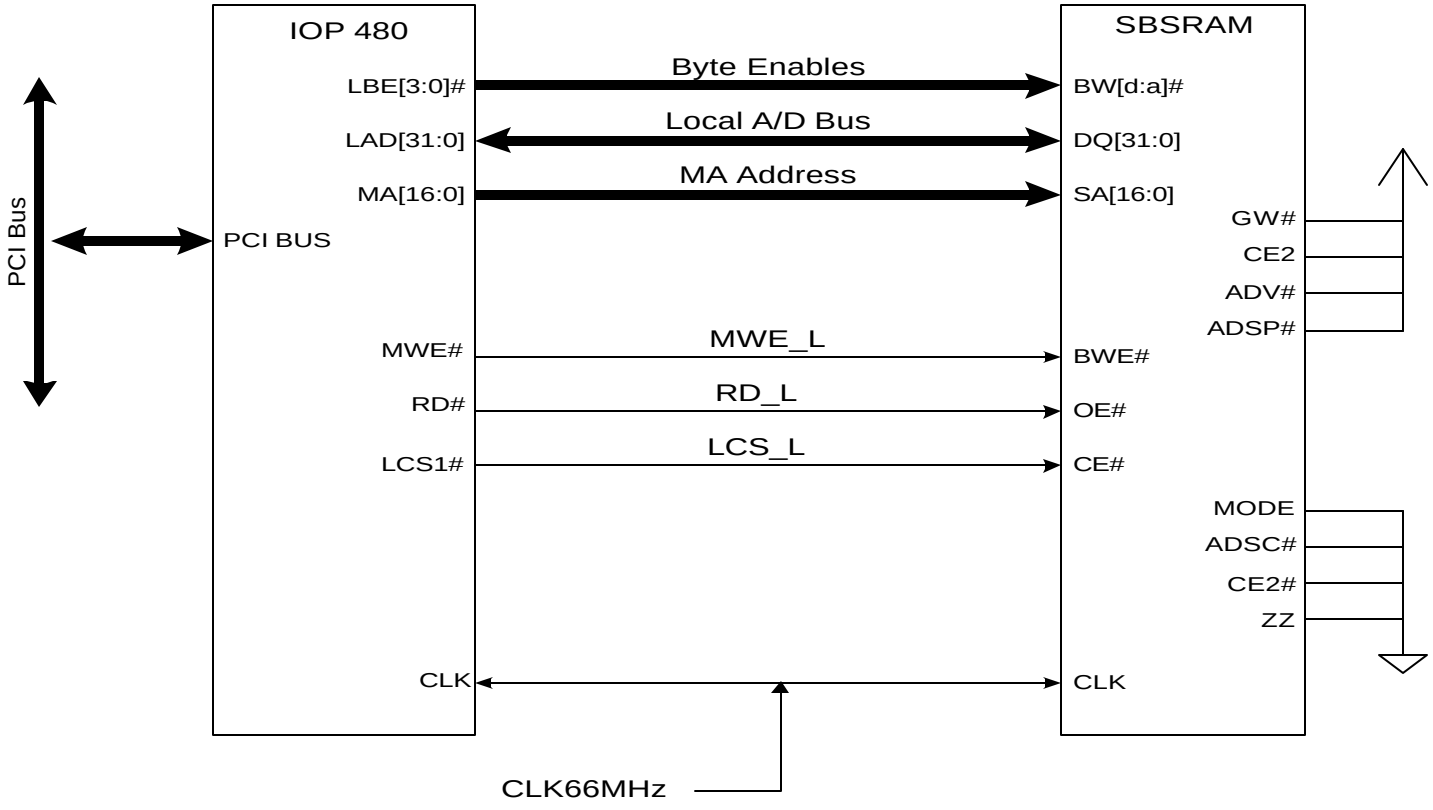


Figure 1-1 Direct Connection Block Diagram

PLX Technology, Inc., 390 Potrero Avenue, Sunnyvale, CA 94085, Phone 408-744-9060, Fax 408-774-2169

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Introduction

This application note describes two different methods for interfacing the PLX Technology IOP 480 to Synchronous Burst SRAM (SBSRAM). The first is a 'Direct' connection using no glue logic. The second is a High Performance (HP) connection using a CPLD. In both implementations the SBSRAM internal address counter is not used, because of the software restrictions it places on Direct Slave Burst accesses.

This note points out the design flexibility of the IOP 480 for both low cost and high performance designs. This information can be used to build either a PCI adapter or PCI host board.

The IOP 480's memory controller has enhanced bursting capabilities allowing much higher data transfer rates than have previously been available. Burst transactions initiated by a local external master, the on-chip DMA controllers, or the PCI bus, can be unlimited in length if the Local bus Latency Timer is disabled, or up to 256 clocks in length if enabled. This is true regardless of the type of memory being accessed, including SBSRAM and SDRAM. In this manner, startup overhead of memories becomes negligible, allowing higher performance characteristics of the memory subsystem.

The IOP 480 has an internal PowerPC RISC 32-bit CPU core running at up to 66MHz. The memory can be accessed even if the IOP 480 CPU is held in reset. The IOP 480 has three powerful DMA controllers. The DMA channels should be used for long and efficient burst transfers between a PCI host and an adapter's memory.

The PCI Initiator mode gives a master device such as the IOP 480 on the Local bus the ability to access the PCI devices on the PCI bus.

The PCI Target mode gives a master device on the PCI bus the ability to access the IOP 480 configuration registers or memory on the Local bus. This mode allows burst or single cycle PCI Target transfers.

This application note contains the following items:

- Direct Connection implementation
- High Performance implementation
- Schematics
- Waveforms
- CPLD Source Code

2. Direct Connect

The IOP 480 connects directly to SBSRAM. No glue logic is needed.

2.1 Features – Direct

The direct connection features are shown below:

- IOP 480 running the local bus at 66MHz.
- SBSRAM 1Mbit, 32Kx36, 32 data, 4 parity (not used).
- Burst and Single Cycle Accesses.
- Burst Forever with One Wait State.
- No Glue Logic.
- No Software Restrictions.

2.2 Architecture – Direct

A glueless connection requires that the IOP 480 MA bus drive the SBSRAM SA address pins. This is due to the address pipelining of the SBSRAM. A SBSRAM read requires that the address is valid one clock before the data is sampled. The IOP 480 provides for this by inserting one wait state between read data beats. The IOP 480 controls the SBSRAM byte enables directly. All components are clocked in phase at 66MHz.

Figure 1-1 is a block diagram of the direct connection. The components used in the direct connection are shown below:

1. I/O Processor, PLX Technology IOP 480, IOP 480-AA66PI (PQFP) or IOP 480-AA66BI (PBGA)
2. Synchronous Burst SRAM (SBSRAM), 128Kx36, Samsung, KM736V787-7 (7.5 ns access)

2.2.1 Software Restrictions - Direct

This connection imposes no software restrictions. A burst can cover the entire SBSRAM memory space. Critical word first caching is allowed.

2.2.2 Data Parity - Direct

Data parity is not supported since MA [16:13] is used to drive the address SBSRAM. The SBSRAM parity bits are not used. However, if a smaller SBSRAM is used, MA [16:13] can be used for data parity.

2.2.3 IOP 480 Register Settings - Direct

The table below shows the SRAM access programmable timing parameter settings to use for a direct connection.

Register Setting for Direct Connection				
RAD=1	RDD=0	RDLYA=1	RDLYD=0	RRCV=1
WAD=0	WDD=0	WHLD=1	WDLY=0	WRCV=0

Table 2-1 Register Settings - Direct

2.3 Performance - Direct

The table below shows the local bus performance for the direct connection. A burst can be as long as the SBSRAM memory (Burst Forever).

Bus Transaction	Data Beats: Clocks	Wait States
Single Write	1:3	2
Single Read	1:4	3
Burst-of-4 Write	4:9	2-1-1-1
Burst-of-4 Read	4:10	2-1-1-2
Burst Forever (Read or Write)	Approaches 2:1	Approaches 1

Table 2-2 Performance - Direct

The IOP 480 (version AA) requires that register bit WHDL is set to a value equal to or greater than one. When WHLD is set to one there is one data hold wait state for each SRAM write data beat.

One recovery clock is used on all reads to avoid contention on the LAD bus. This avoids contention as the SBSRAM tri-states while the IOP 480 comes on to the bus to drive the next address.

3. High Performance Connection

The High Performance (HP) connection provides higher performance by using a CPLD between the IOP 480 and the SBSRAM.

3.1 Features - HP

The features of the HP connection are shown below:

- IOP 480 running the local bus at 66MHz.
- SBSRAM 1Mbit, 32Kx36, 32 data, 4 parity.
- Burst and Single Cycle Access.
- Zero Wait States for forever read bursts
- Byte wise Parity.
- Nine spare CPLD I/O pins.

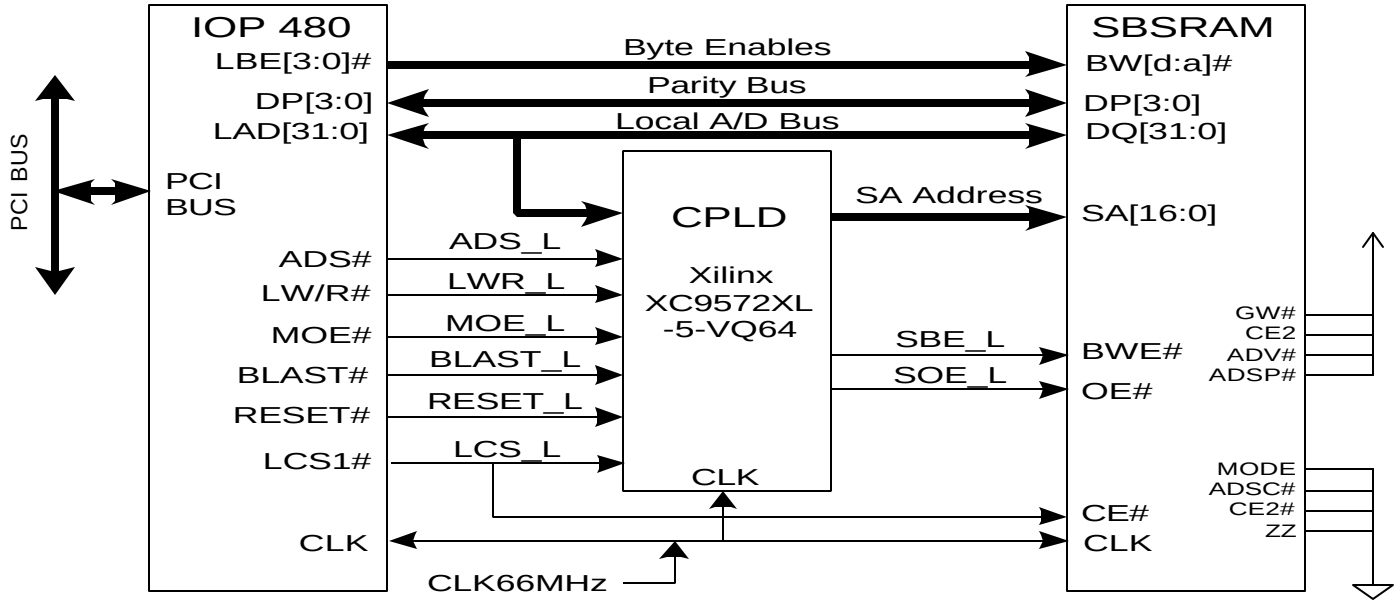


Figure 3-1 High Performance Connection Block Diagram

3.2 Architecture – HP

Figure 31 is a block diagram of the High Performance Connection. The components used are shown below:

1. I/O Processor, PLX Technology IOP 480, IOP 480-AA66PI (PQFP) or IOP 480-AA66BI (PBGA)
2. Synchronous Burst SRAM (SBSRAM), 128Kx36, Samsung, KM736V787-7 (7.5 ns access)
3. CPLD, Xilinx, XC9572XL-5-VQ64 (5 ns)

In the HP implementation a CPLD is used to provide the address to the SBSRAM one clock earlier for each data beat on reads. This way the one wait state per data beat of the Direct Connection is eliminated. The CPLD also drives the SBSRAM read and write enable pins. All components are clocked in phase at 66MHz.

3.2.1 CPLD

The CPLD is a 64 pin Xilinx XC9572XL-5-VQ64. The CPLD acts as an address latch/incrementor (17 bits) and generator of the SBSRAM read and write enables. There are nine spare I/O pins on the CPLD. The following subsections discuss the CPLD features.

3.2.1.1 Address Latch/Incrementor

The IOP 480 addresses (LAD[16:0]) on the multiplexed address/data bus are latched by the CPLD. The CPLD then drives this address to the SBSRAM and increments the address by one for each beat. The IOP 480 MA bus is not used for addressing the SBSRAM. If LAD bus loading is an issue, MA address lines could be latched instead. This requires minor CPLD code changes.

A different implementation could use less than 17 address bits and would result in a smaller CPLD. However, the roll over of this smaller counter would result in restricted maximum unbroken burst length and burst boundaries. A burst outside of the limits could be broken into smaller bursts by the CPLD asserting BTERM# and so forcing a new burst cycle.

3.2.1.2 SBSRAM Control Signals

The CPLD generates the SBSRAM read and write enable signals. The CPLD uses the IOP 480 CLK, ADS#, LW/R#, MOE#, BLAST#, and LCS1# to generate SBSRAM read and write enables.

3.2.2 Software Restriction - HP

All burst accesses must use increasing incremented addresses. This is because the CPLD automatically increments the SA address. One ramification of this is that critical word first caching cannot be used since the CPLD will not wrap the SA address.

3.2.3 Data Parity - HP

Since the MA bus is not used, the data parity bits of the SBSRAM can be connected to the IOP 480 data parity pins DP[3:0]. The IOP 480 can support both even and odd parity. The IOP 480 can be configured to interrupt upon a parity error.

3.2.4 IOP 480 Register Settings – HP

The table below shows the SRAM access programmable timing parameter settings for the high performance connection.

Register Settings for HP Connection				
RAD=0	RDD=0	RDLYA=0	RDLYD=0	RRCV=1
WAD=0	WDD=0	WHLD=1	WDLY=0	WRCV=0

Table 3-1 Register Settings - HP

3.3 Performance - HP

The table below shows the performance for the HP implementation. A burst can cover the entire SBSRAM memory (Burst Forever).

Bus Transaction	Data Beats: Clocks	Wait States
Single Write	1:3	2
Single Read	1:3	2
Burst-of-4 Write	4:9	2-1-1-1
Burst-of-4 Read	4:6	1-0-0-1
Burst Forever Write	Approaches 2:1	Approaches 1
Burst Forever Read	Approaches 1:1	Approaches 0

Table 3-2 Performance - HP

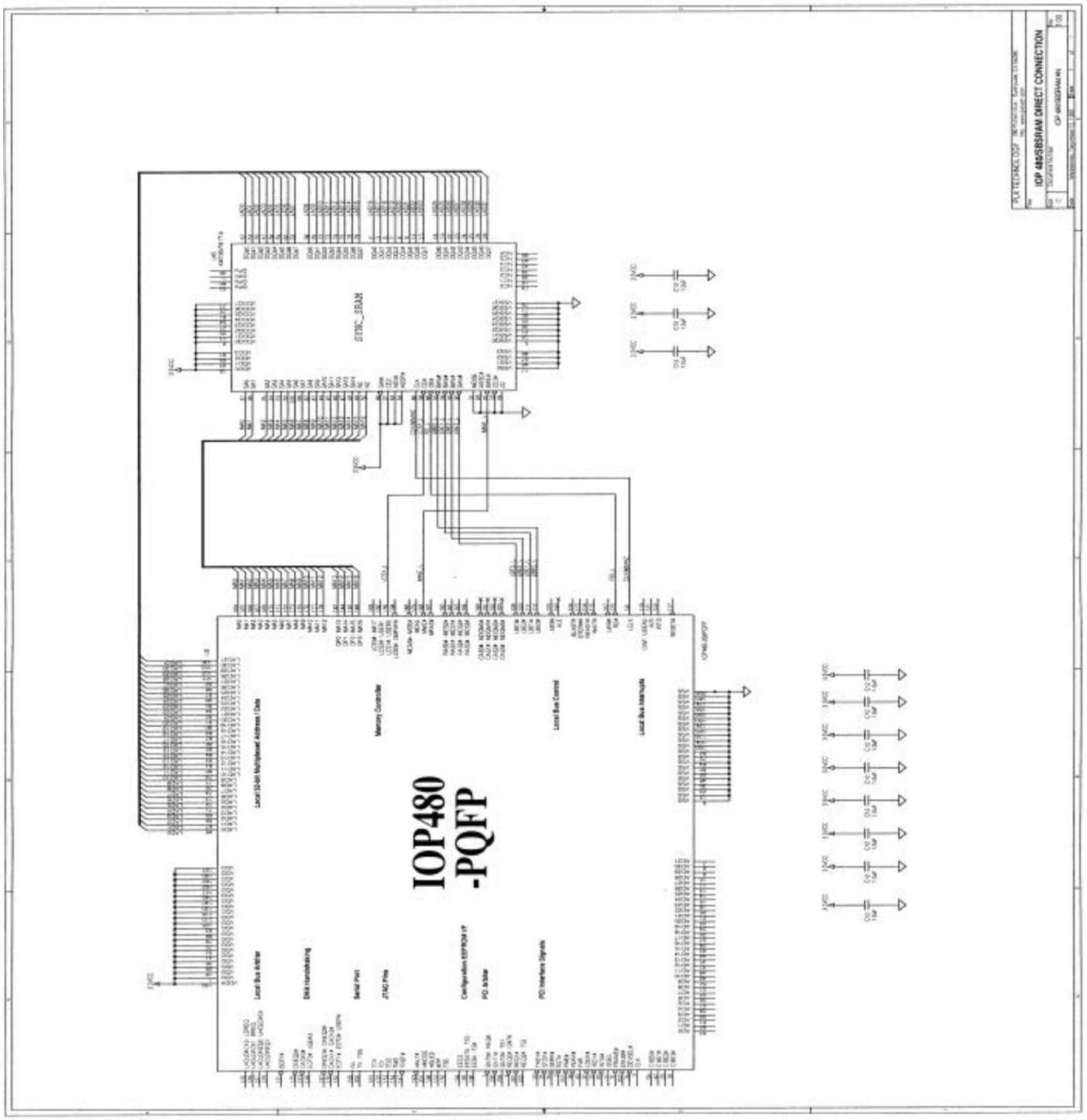
The IOP 480 (version AA) requires that register bit WHDL is set to a value equal to or greater than one. When WHLD is set to one there is one data hold wait state for each write data beat.

One recovery clock is used on all reads to avoid contention on the LAD bus. This avoids contention as the SBSRAM tri-states while the IOP 480 comes on to the bus to drive the next address.

4. Appendix

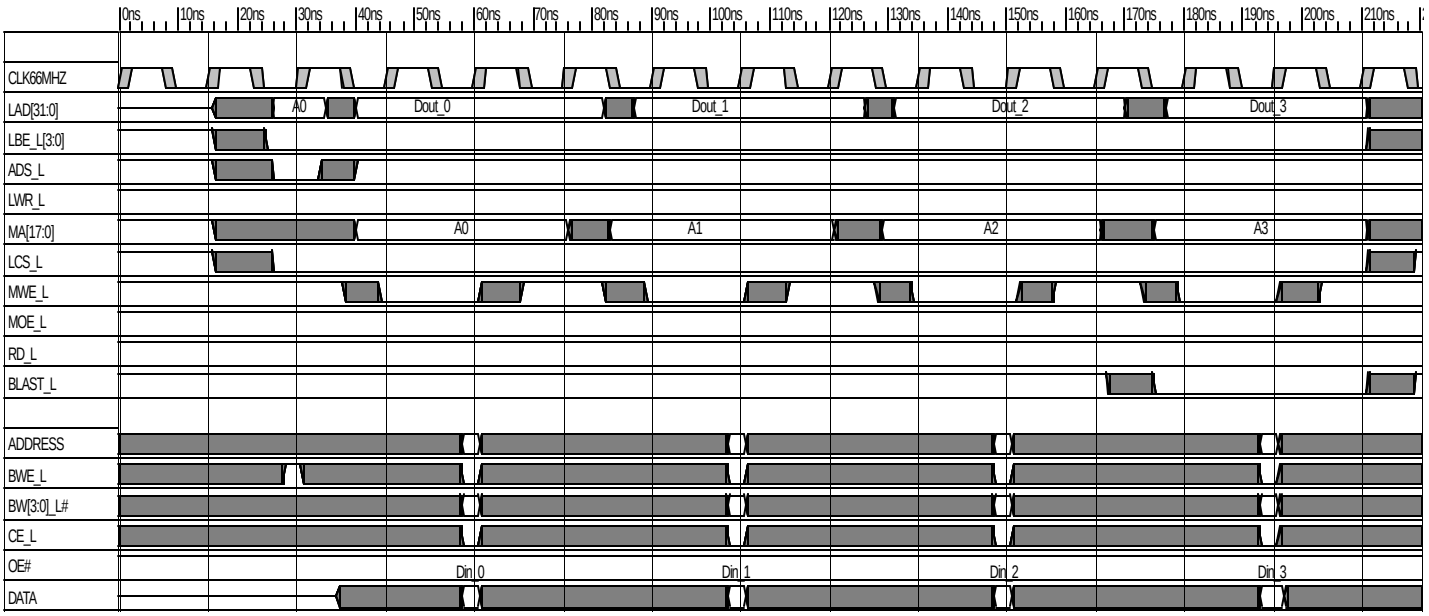
4.1 Direct Connection – Schematic

The Orcad source file is available from the PLX Technology Inc. website (http://www.plxtech.com/).

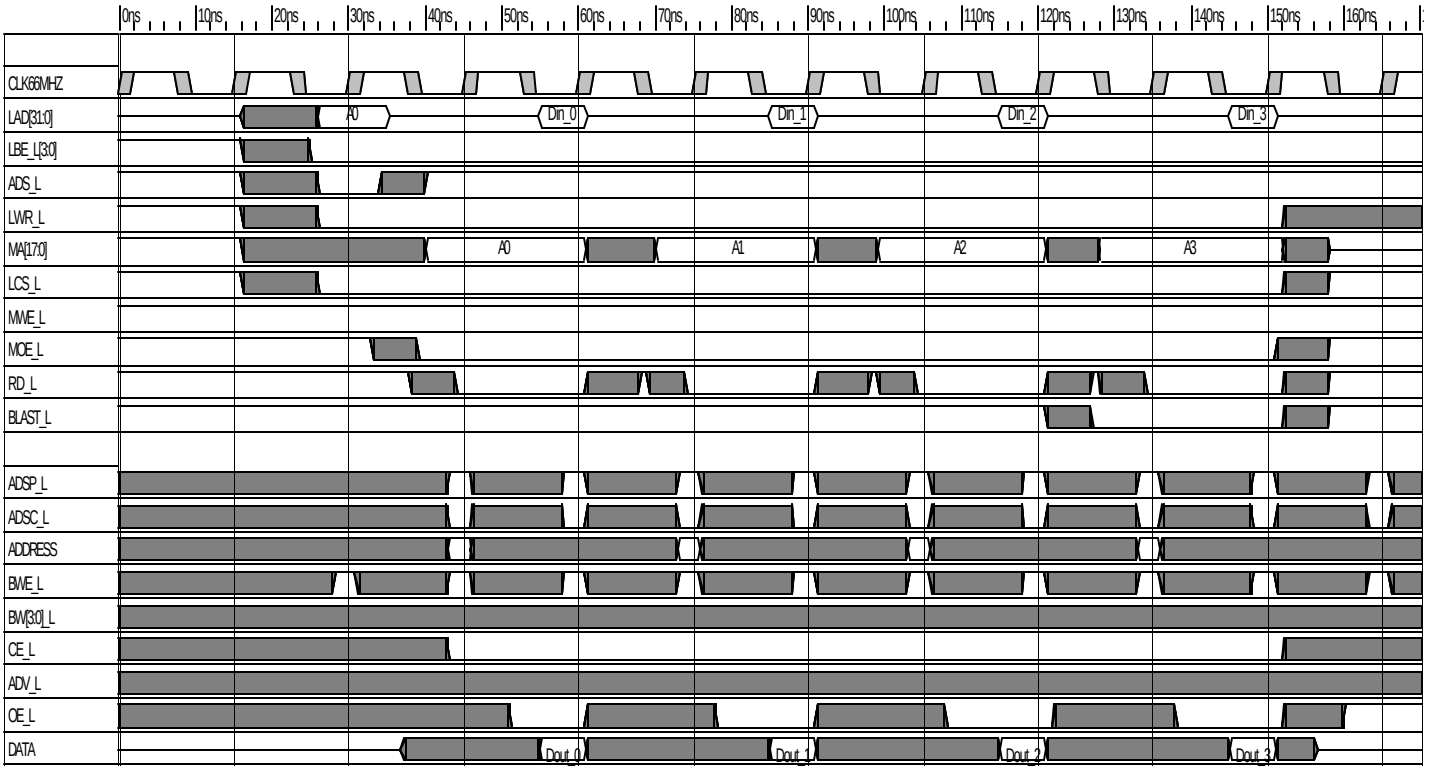


4.2 Direct Connection - Waveforms

Shown below are the waveforms for a Direct Connection Burst-of-four write. The upper group of waveforms is what the IOP 480 provides. The bottom group shows the requirements of the SBSRAM.

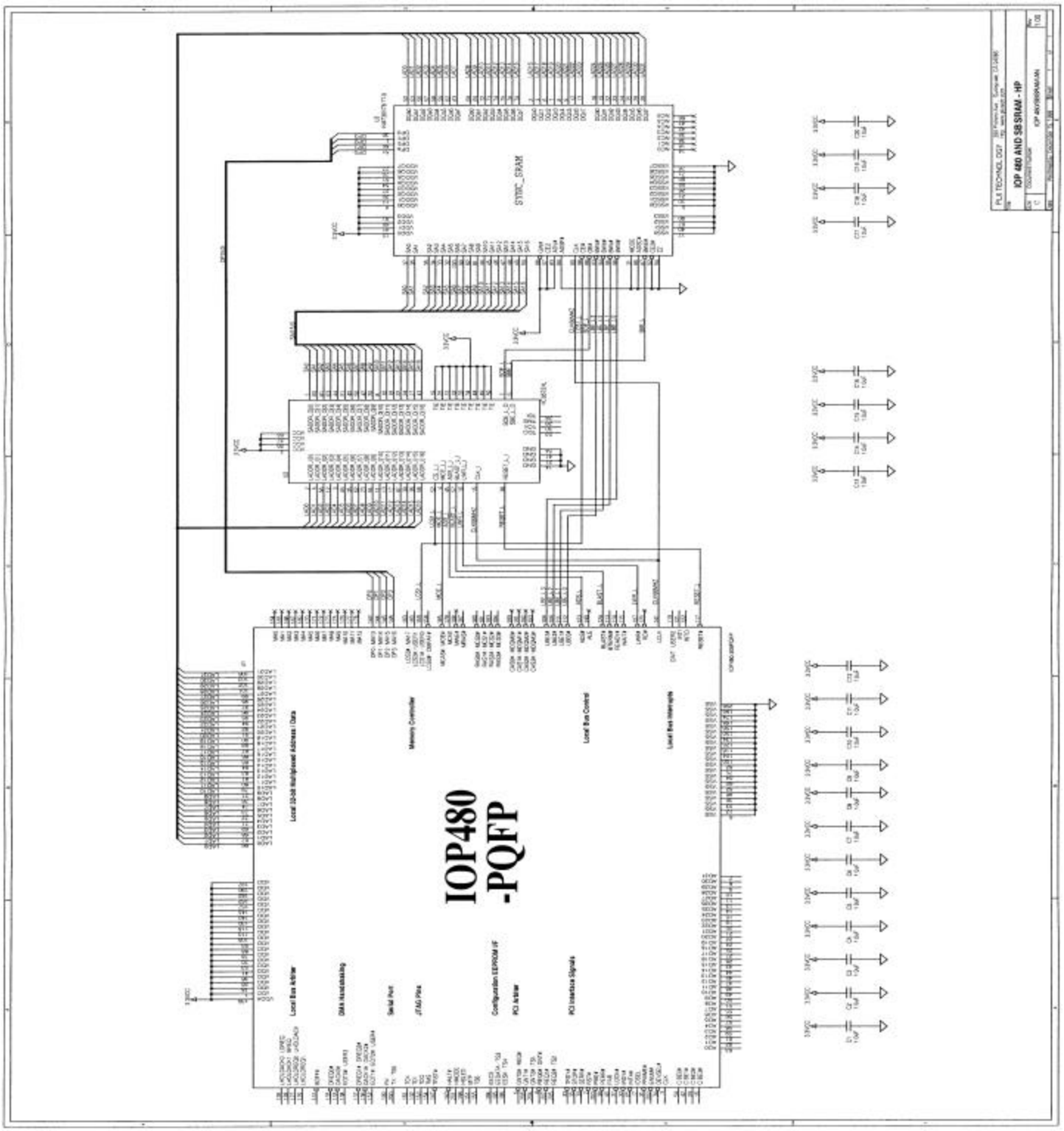


Shown below are the waveforms for a Direct Connection Burst-of-four read. The upper group of waveforms is what the IOP 480 provides. The bottom group shows the requirements of the SBSRAM.



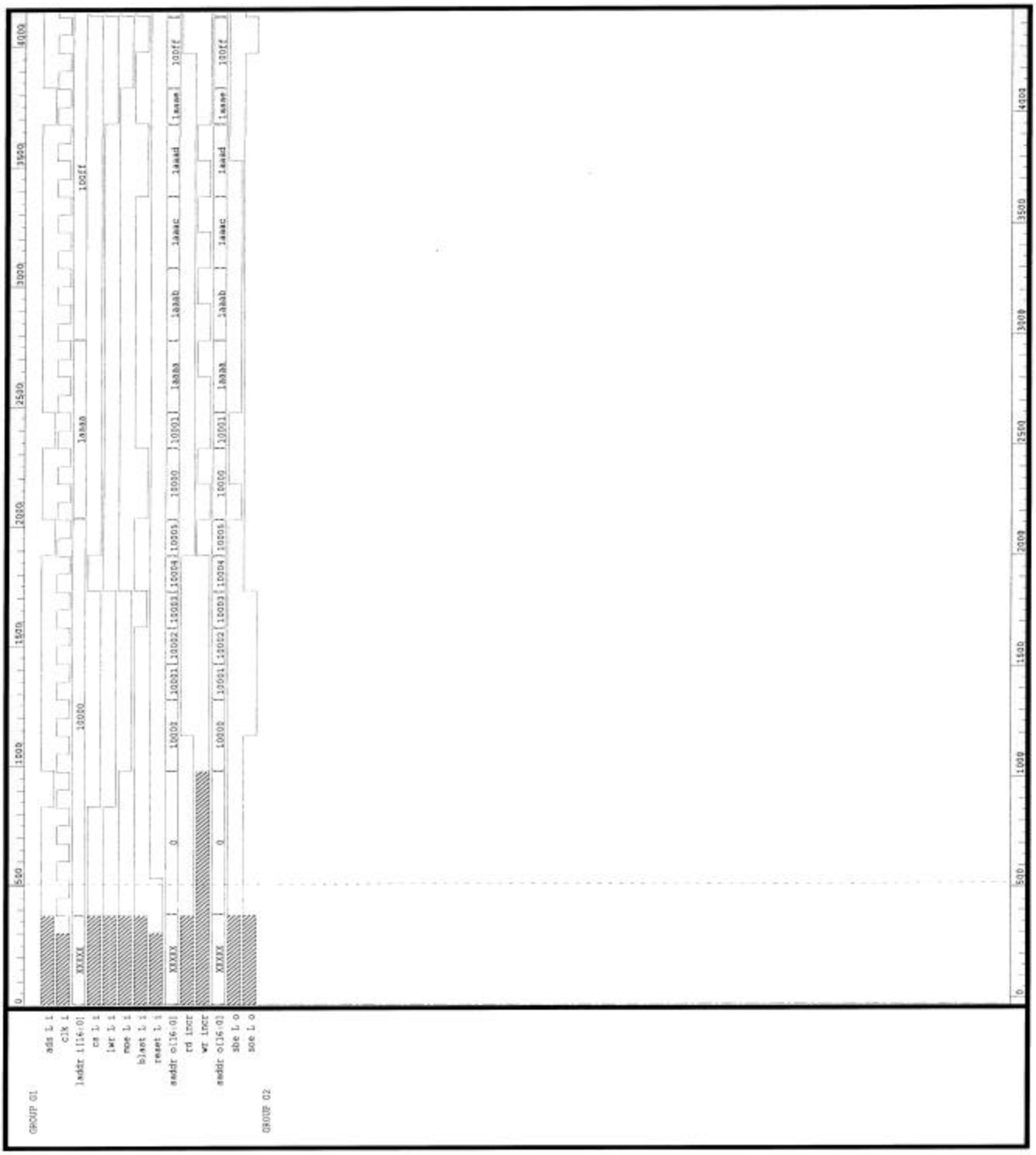
4.3 High Performance – Schematic

The Orcad source file is available from the PLX Technology Inc. website (http://www.plxtech.com/).



4.4 High Performance - Waveforms

The waveforms below show the bus cycles for the High Performance connection for Burst-of-four Read, Single Write, Burst of-four Write, and Single Read.



4.5 CPLD Source Code

```
/*****************************************************************************/
/* MODULE: IOP 480 High Performance Logic                                    */
/* AUTHOR: PLX Technology                                                    */
/* DATE:   Nov-22-1999                                                       */
/*                                                                           */
/* REVISION HISTORY:                                                         */
/* Rev A:  Initial Development                                               */
/*                                                                           */
/* DESCRIPTION:                                                              */
/*                                                                           */
/*  This is the logic for a high performance SBSRAM interface                */
/*  for the IOP 480. There is a loadable 17 bit address counter,             */
/*  control signals for SBSRAM OE and Write enable.                          */
/*                                                                           */
/*****************************************************************************/

`timescale 1ns/1ns

module      iop(
            clk_i,
            reset_L_i,
            ads_L_i,
            cs_L_i,
            moe_L_i,
            lwr_L_i,
            laddr_i,
            blast_L_i,

            saddr_o,
            soe_L_o,
            sbe_L_o
           );
//
// inputs and outputs
//
input clk_i;
input reset_L_i;
input ads_L_i;
input cs_L_i;
input moe_L_i;
input lwr_L_i;
input [16:0] laddr_i;
input blast_L_i;

output saddr_o;
output soe_L_o;
output sbe_L_o;

reg [16:0] saddr_o;
reg soe_L_o, sbe_L_o;

reg rd_incr;  // Detemines when to increment address on reads.
```

```
reg wr_incr;  // Detemines when to increment address on writes.

// Address latch and incrementer
// A read the address must be incremented one clock before strobing data.
// A write the address must be increment after strobing data.

always @ (posedge clk_i)
 begin
  rd_incr <= ( !lwr_L_i & ( ads_L_i ||  cs_L_i  ));
  wr_incr <= (  lwr_L_i & ( ads_L_i & !wr_incr ));
  soe_L_o <= !((!moe_L_i &!cs_L_i &!rd_incr)|(!soe_L_o &!cs_L_i & blast_L_i));
  sbe_L_o <= !((!cs_L_i & lwr_L_i &!ads_L_i)|(!sbe_L_o &!cs_L_i & blast_L_i));
 end

always @ (posedge clk_i)
  begin
    if (ads_L_i == 1'b0)
      begin
        #1 saddr_o = laddr_i;
      end
    else if ( wr_incr || rd_incr )
      begin
        saddr_o = saddr_o + 1;
      end
    if (reset_L_i == 1'b0)
      begin
        #5 saddr_o = 17'b0_0000_0000_0000_0000;
      end
  end

endmodule
```

5. ASSUMPTIONS

This application note is based on the following assumption:

- Some typically necessary design components (i.e. boot and code memory, EEPROM, and pull-up/down resistors) are not included in this application note.

The designer is expected to add such components as needed.

6. REFERENCES

- IOP 480 Data Book v1.0
  PLX Technology, Inc.
  390 Potrero Avenue
  Sunnyvale, CA 94085 USA
  Tel: 408 774-9060, 800 759-3735,
  Fax: 408 774-2169,
  http://www.plxtech.com/

- KM736V787 SBSRAM Data Book
  SAMSUNG SEMICONDUCTOR INC.
  3655 North First Street
  San Jose, CA 95134, U.S.A.
  Tel: +408-544-4000
  Fax: +408-544-4980,
  http://www.intl.samsungsemi.com/

- XC9572XL-5-VQ64 CPLD Data Book
  XILINX, Inc.
  2100 Logic Drive
  San Jose, CA 95124
  (408) 559-7778
  Tel: 510-600-8750
  Fax: 408-559-7114
  http://www.xilinx.com/