IOP 480/SDRAM AN

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Version 2.0

IOP 480 Interface to SDRAM Application Note

Features

- Detailed connection of IOP 480 I/O processor to 256 Mbit, 128 Mbit, and 64 Mbit (32-bit wide) SDRAM.
  - 256 Mbit : 16 Meg x 16 bit
    32 Meg x 8 bit
    64 Meg x 4 bit
  - 128 Mbit : 8 Meg x 16 bit
    16 Meg x 8 bit
    32 Meg x 4 bit
  - 64 Mbit : 2 Meg x 32 bit

General Description

This application note describes how to interface the PLX IOP 480 to higher density SDRAMs such as 256 Mbit and 128 Mbit sizes. In addition, the application note also describes how to interface to the 32-bit wide, 64 Mbit SDRAMs.

The IOP 480 has PCI Initiator, DMA, and PCI Target data transfer capabilities. The PCI Initiator mode allows a device (IOP 480) on the Local Bus to perform memory, I/O, and configuration cycles to the PCI Bus. The PCI Target mode allows a master device on the PCI bus to access memory on the Local Bus. The IOP 480 allows the Local Bus to run asynchronously to the PCI Bus through the use of bi-directional FIFOs. In this design example, the PCI Bus runs at up to 33 MHz while the IOP 480 Local Bus is clocked at up to 66 MHz.

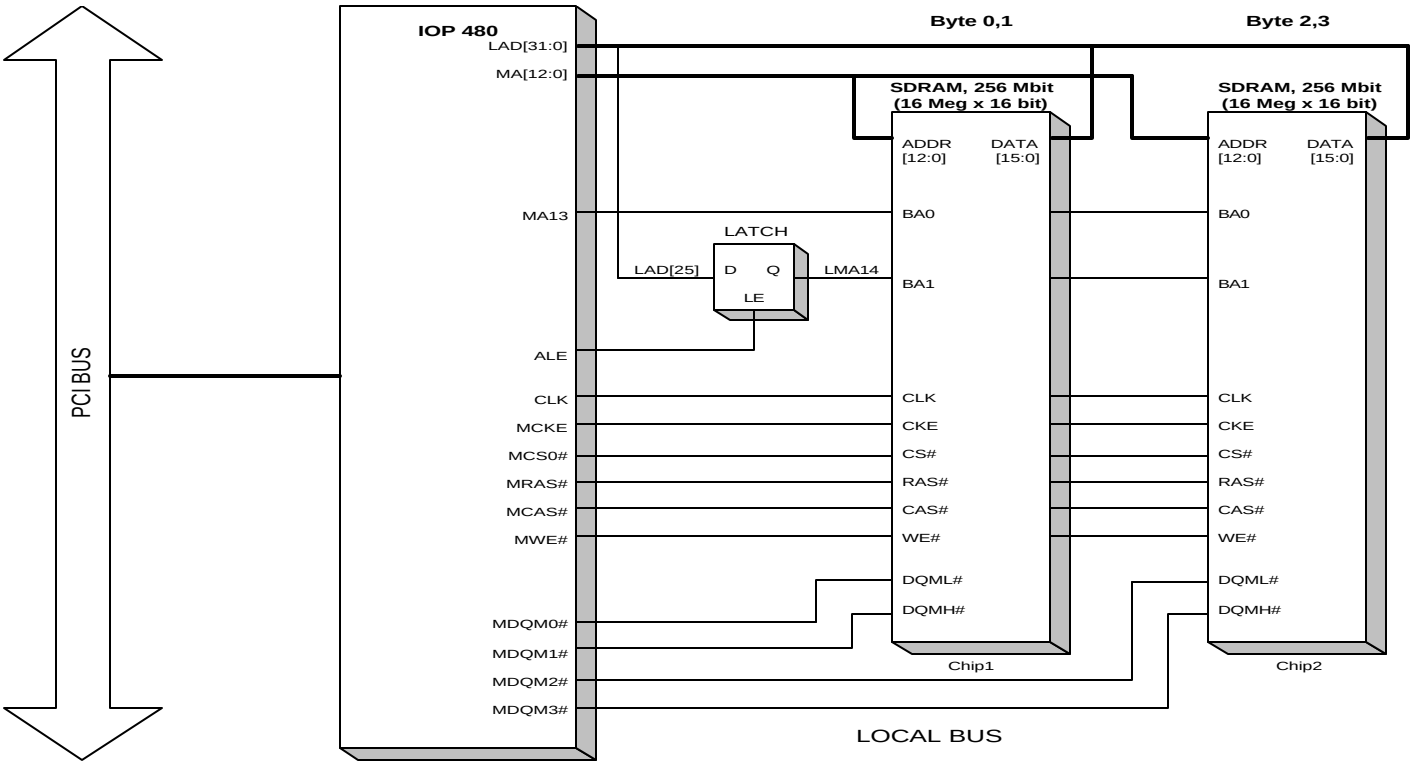

Figure 1-1. 256 Mbit (16 Meg x 16 bit) SDRAM Connection to IOP 480 I/O Processor
Total Memory Addressed = 64 Mbytes (Max = 256 Mbytes)

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1. INTRODUCTION

This application note describes how to interface 256 Mbit, 128 Mbit, and 64 Mbit (x 32 bit wide) memories to the IOP 480 I/O processor. The information can be used to build either a PCI adapter or PCI host board in an embedded system. The subsystem described in this note consists of an IOP 480 connected to SDRAM's of various densities and configurations. Figure 1 is a block diagram showing connections between the IOP 480 and two 16Mx16 SDRAMs. Other configurations and densities beyond the 256 Mbytes memory array are also possible.

The IOP 480's memory controller has enhanced bursting capabilities allowing much higher data transfer rates than have previously been available. Burst transactions initiated by a local external master, the on-chip DMA controllers, or the PCI bus, can be unlimited in length if the Local Bus Latency Timer is disabled, or up to 256 clocks in length if enabled. This is true regardless of the type of memory being accessed, including SDRAM. In this manner, startup overhead of memories such as SDRAMs becomes negligible, allowing higher performance characteristics of the memory subsystem.

The IOP 480 has an internal PowerPC RISC 32-bit CPU core running at up to 66 MHz. The SDRAM memory can be accessed even if the IOP 480 CPU is held in reset. The IOP 480 also has two powerful DMA controllers supervising the three DMA channels. The DMA channels should be used for long and efficient burst transfers between a PCI host and an adapter's memory.

The PCI Initiator mode gives a master device such as the IOP 480 on the Local Bus the ability to access the PCI devices on the PCI Bus.

The PCI Target mode gives a master device on the PCI Bus the ability to access the IOP 480 configuration registers or memory on the Local Bus. This mode allows burst or single cycle PCI Target transfers.

2. ARCHITECTURE

This section describes the implementation of the 256 Mbit, 128 Mbit, and 64 Mbit(x32 wide) memory densities with various internal configurations. Note that for 128 Mbit SDRAMs with the 8 Meg x 16 bit internal configuration, external logic along with additional SDRAM chips can be used to increase the total memory array to 256 Mbytes. Refer to section *2.2.3.1 256 Mbyte (8 Meg x 16 bit) Memory Array* for further details.

Figure 2-1. SDRAM Memory and Glue Logic Requirement

Memory Configuration	External Logic Required	Type of External Logic	Maximum Number Of Memory Chips	Maximum Memory Supported by IOP 480
256 Mbit				
16Mx16 bit	Yes	Latch	8	256 Mbyte
32Mx8 bit	Yes	Latch, AND Gate	8	256 Mbyte
64Mx4 bit	Yes	Latch, AND Gate, 2-to-1 Mux	8	256 Mbyte
128 Mbit				
8Mx16 bit	No	None	8	128 Mbyte, *Note 1
16Mx8 bit	No	None	16	256 Mbyte
32Mx4 bit	Yes	AND Gate 2-to-1 Mux	16	256 Mbyte
64 Mbit				
2Mx32 bit	No	None	4	32 Mbyte

Note: 1. Additional SDRAM chips and external logic can be used to increase to 256 Mbytes.

2.1 256 Mbit SDRAM

There are 3 common internal configurations for 256 Mbit SDRAM: 16 Meg x 16 bit, 32 Meg x 8 bit, and 64 Meg x 4 bit. Each 256 Mbit SDRAM is equivalent to 32 Mbytes. Table 2 on page 11 shows the connection of 256 Mbit SDRAMs to the IOP 480.

2.1.1 Address Latch

An external latch is used to extract an additional address signal from the multiplexed address and data LAD[31:0] bus. The output of the address latch provides the extra row address for the 256 Mbit SDRAM. Figure 1 shows the connection of two 256 Mbit SDRAMs using the 16 Meg x 16 bit configuration. The internal configuration of the 256 Mbit SDRAM will determine which LAD[n] signal to use as an input to the address latch. The LAD[25], LAD[26], and LAD[27] are used as inputs to the address latches for 16 Meg x 16 bit, 32 Meg x 8 bit , and 64M x 4 bit configurations respectively.

2.1.2 Memory Chip Selects

The memory chip selects for 256 Mbit SDRAM are defined in Table 2. Each MCSn# memory chip select pin can select up to 64 Mbytes of SDRAM.

2.1.3 16 Meg x 16 bit Connection

For the 16 Meg x16 bit configuration memories, as shown in Figures 1 and 2, two 256 Mbit SDRAM chips are used to create a 32-bit wide memory totaling 64 Mbytes. The MCS0# connects directly to the CS# pin of each SDRAM chip. In addition to MCS0#, the system designer may also connect MCS1#, MCS2#, and MCS3# to an additional six 256 Mbit SDRAM chips to increase the total memory array to 256 Mbytes, as shown in Table 2.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 9 columns respectively.

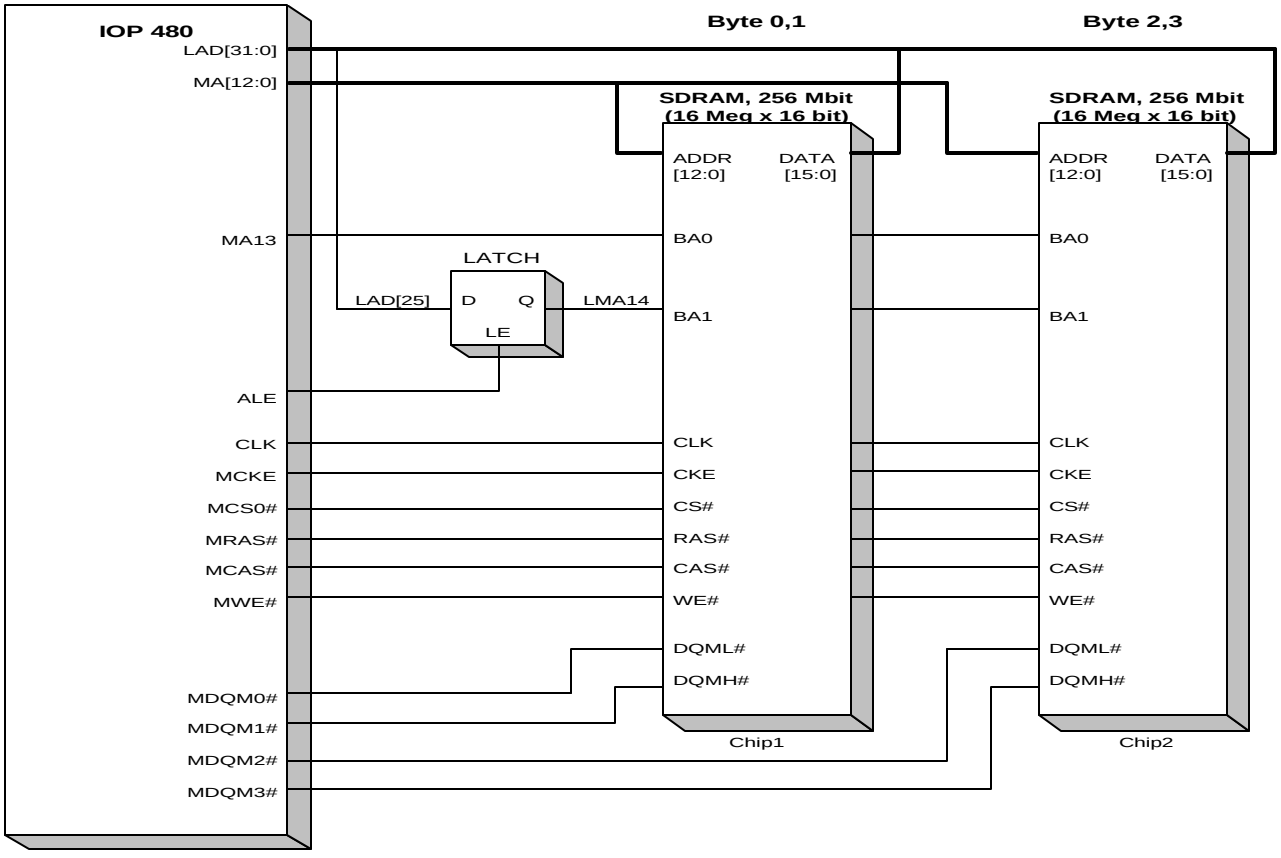

Figure 2-2. 256 Mbit (16 Meg x 16 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 64 Mbytes, (Max = 256 Mbytes)

2.1.4 32 Meg x 8 bit Connection

For 32 Meg x 8 bit configuration memories, as shown in Figure 3, four SDRAM chips are used to create a 32-bit wide memory totaling 128 Mbytes. Because each memory chip select pin of the IOP 480 addresses up to 64 Mbytes, two memory chip select pins, MCS0# and MCS1#, are required to access the 128 Mbyte of SDRAM. The chip select for the SDRAM, MCS_OUT0#, is created by logically ANDing the MCS0# and MCS1# signals of the IOP 480. The Boolean equation is MCS_OUT0# = (MCS0# *AND* MCS1#). In addition, the system designer may also use MCS2# and MCS3# to generate MCS_OUT1# and connect it to additional 256 Mbit SDRAM chips, as shown in Table 2. This would increase the total memory array to 256 Mbytes.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 10 columns respectively.

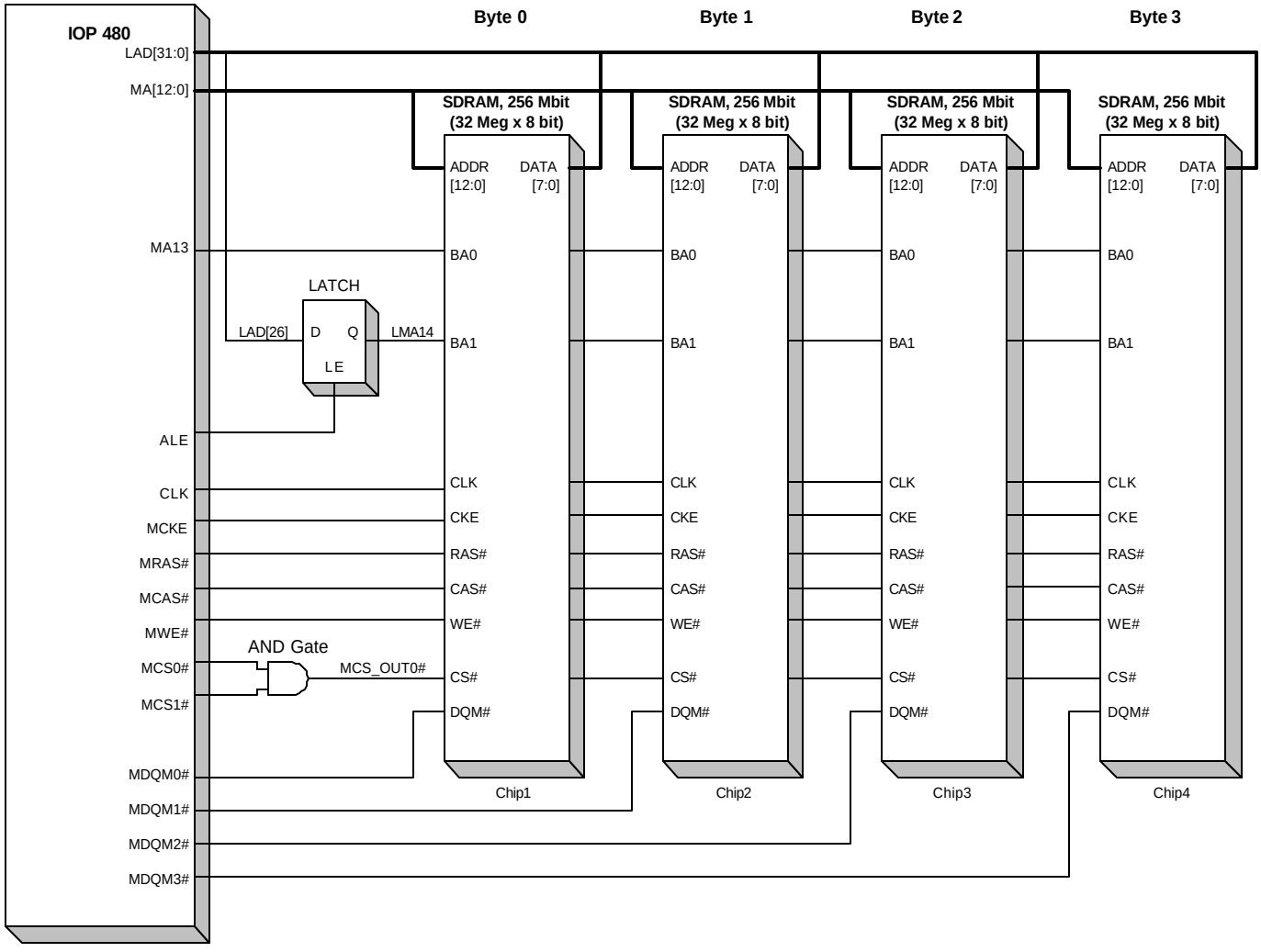

Figure 2-3. 256 Mbit (32 Meg x 8 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 128 Mbytes, (Max = 256 Mbytes)

2.1.5 64 Meg x 4 bit Connection

For 64 Meg x 4 bit configuration memories, as shown in Figure 4, eight SDRAM chips are used to create a 32-bit wide memory totaling 256 Mbytes. For this configuration, four memory chip select pins, MCS0#, MCS1#, MCS2#, and MCS3#, are used to access 256 Mbytes. The chip select for the SDRAM, MCS_OUT0#, is created by logically ANDing the MCS0#, MCS1#, MCS2#, and MCS3# signals of the IOP 480. The Boolean equation is MCS_OUT0# = (MCS0# *AND* MCS1# *AND* MCS2# *AND* MCS3#).

Note from the SDRAM datasheet that the column address of the 64 Meg x 4 bit SDRAM skips ADDR[10] pin and instead connects to ADDR[11] pin. Since the IOP 480 outputs the column address on the MA[10] and not MA[11], an external multiplexer controlled by MCAS# signal is used to select the row address, MA[11], and the column address, MA[10], for the ADDR[11] SDRAM pin.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 11 columns respectively.

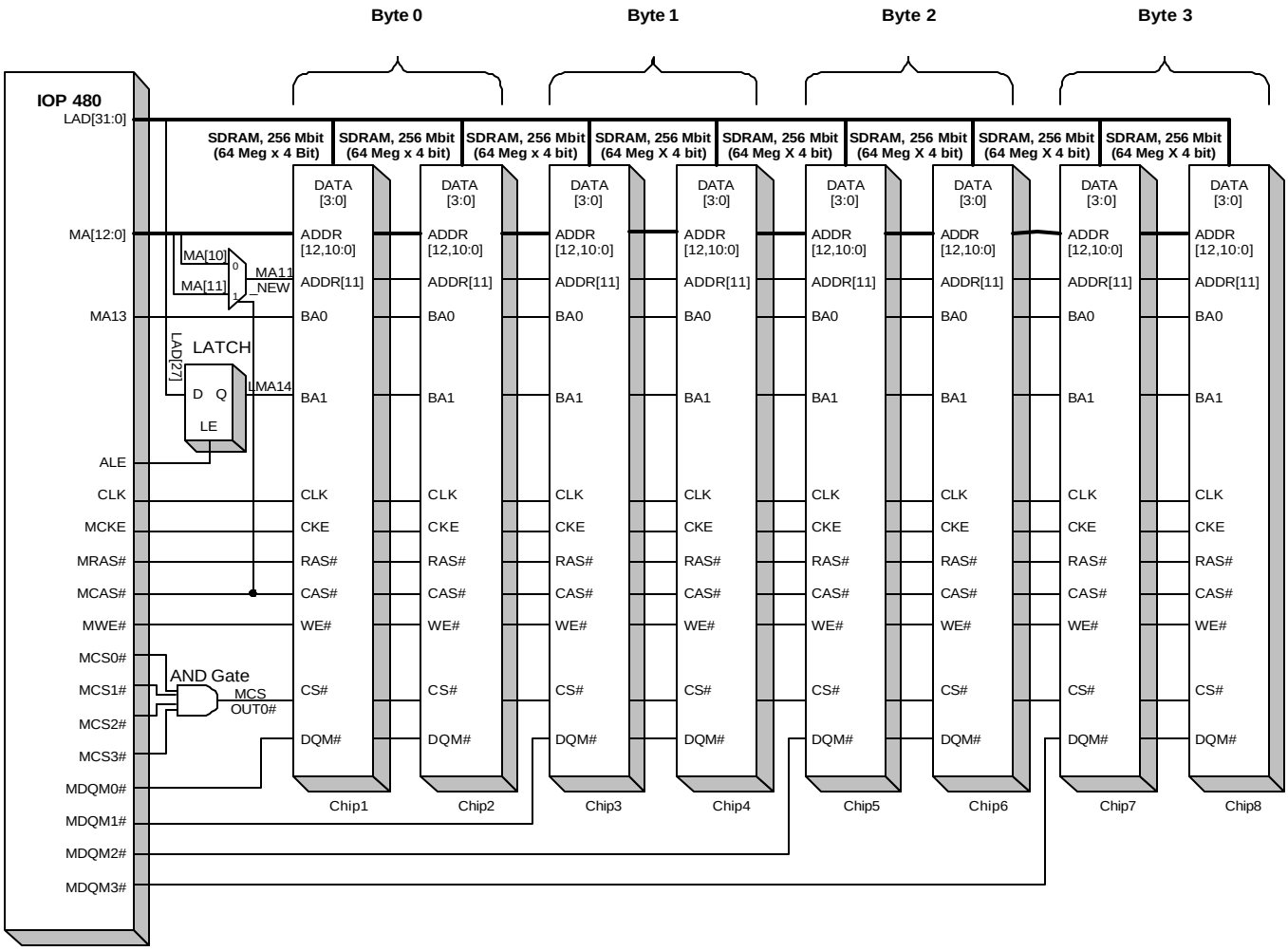

Figure 2-4. 256 Mbit (64 Meg x 4 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 256 Mbytes, (Max = 256 Mbytes)

2.2 128 Mbit SDRAM

There are 3 common internal configurations for 128 Mbit SDRAM: 8 Meg x 16 bit, 16 Meg x 8 bit, and 32 Meg x 4 bit. Each 128 Mbit SDRAM is equivalent to 16 Mbytes. Table 3 on page 12 shows the connection of 128 Mbit SDRAMs to the IOP 480.

2.2.1 Address Latch

No external latch is required for connecting 128 Mbit SDRAMs to the IOP 480. The IOP 480 generates the 12 row address bits required by the 128 Mbit SDRAMs.

2.2.2 Memory Chip Selects

The memory chip selects for 128 Mbit SDRAM are defined in Table 3. Each MCSn# memory chip select pin can select up to 64 Mbytes of SDRAM.

2.2.3 8 Meg x 16 bit Connection

For the 8 Meg x16 bit configuration memories, as shown in Figure 5, two SDRAM chips are used to create a 32-bit wide memory totaling 32 Mbytes. For this configuration, MCS0# directly connects to the CS# pin of each SDRAM chip. In addition to MCS0#, the system designer may also connect MCS1#, MCS2#, and MCS3# to additional 128 Mbit SDRAM chips to increase the total memory array to 128 Mbytes, as shown in Table 3.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 32 Mbytes and 9 columns respectively.

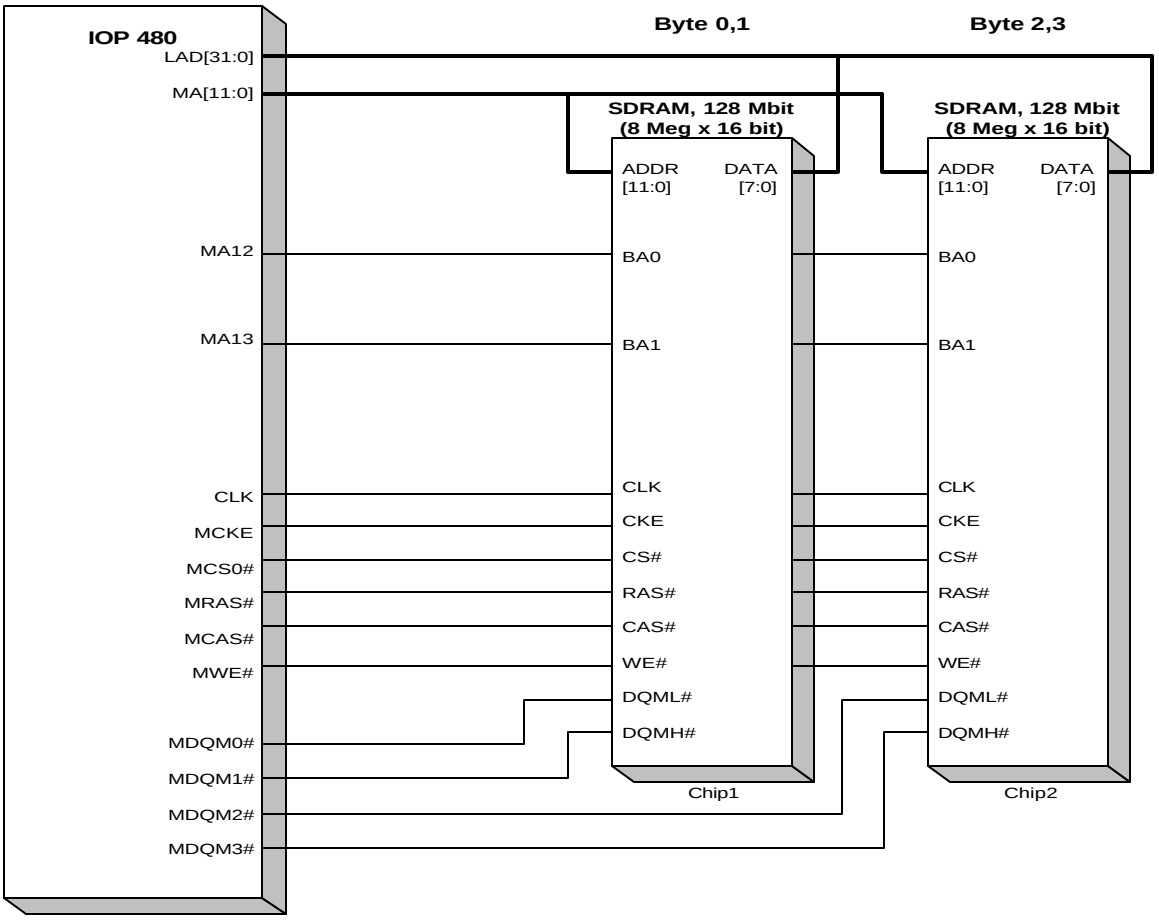

Figure 2-5. 128 Mbit (8 Meg x 16 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 32 Mbytes, (Max = 128 Mbytes)

2.2.3.1 256 Mbyte (8 Meg x 16 bit) Memory Array

Each pair of 8 Meg x 16 bit SDRAMs is equivalent to 32 Mbytes, which equates to 32 Mbytes per bank. From the perspective of the IOP 480, a bank is defined as the depth size of 32-bit wide memory array that each MCSn# signal can address and it is programmable up to 64 Mbytes per bank for the IOP 480. Although the IOP 480's memory controller is capable of addressing 64 Mbytes per bank, there are only 32 Mbytes per bank when using the 128 Mbit SDRAMs in 8 Meg x 16 bit internal configuration. This results in the limitation of the total addressable memory array to 128 Mbytes when using all four chip selects MCS[3:0]#.

With additional external logic, the total addressable memory can be increased to 256 Mbytes using sixteen 8 Meg x 16 bit memory chips. This is accomplished by programming the IOP 480's memory controller for 64 Mbytes/bank and using externally generated chip selects for the lower 32 Mbytes and upper 32 Mbytes physical memory array, as shown in Figure 6. Note that the output of the 4 input OR gate is used to indicate that the IOP 480 is running in a load mode, refresh, or precharge cycles. During load mode, refresh, and precharge cycles, the IOP 480 asserts the all four memory chip select MCS[3:0]# signals simultaneously.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 9 columns respectively.

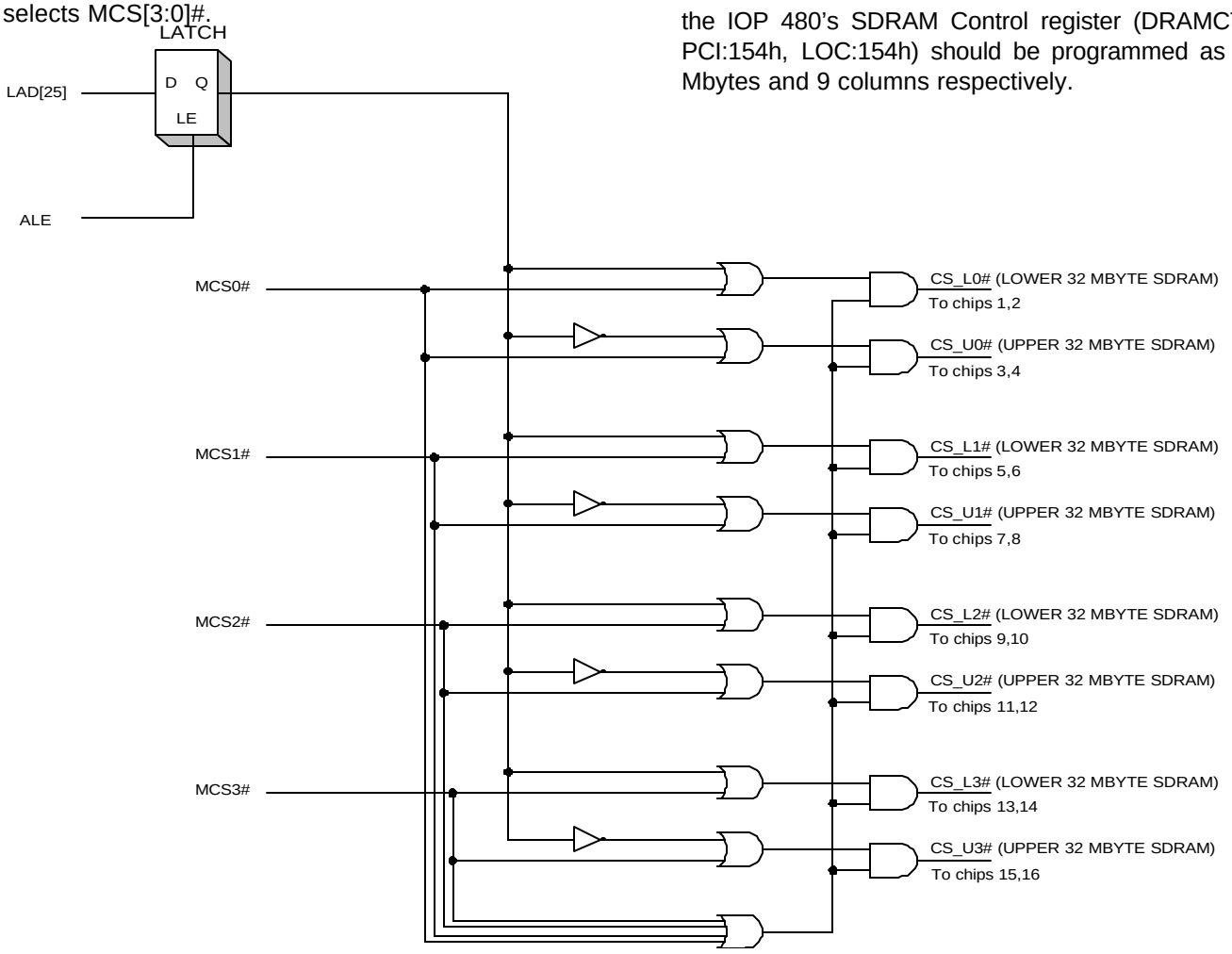

Figure 2-6. External Logic for 256 Mbyte Memory Array Using 128 Mbit (8 Meg x 16 bit) SDRAM

2.2.4 16 Meg x 8 bit Connection

For 16M x 8 configuration memories, as shown in Figure 7, four SDRAM chips are used to create a 32-bit wide memory totaling 64 Mbytes. For this configuration, MCS0# directly connects to the CS# pin of each SDRAM chip. In addition to MCS0#, the system designer may choose to connect MCS1#, MCS2#, and MCS3# to additional 128 Mbit SDRAM to increase the total memory array to 256 Mbytes, as shown in Table 3.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 10 columns respectively.

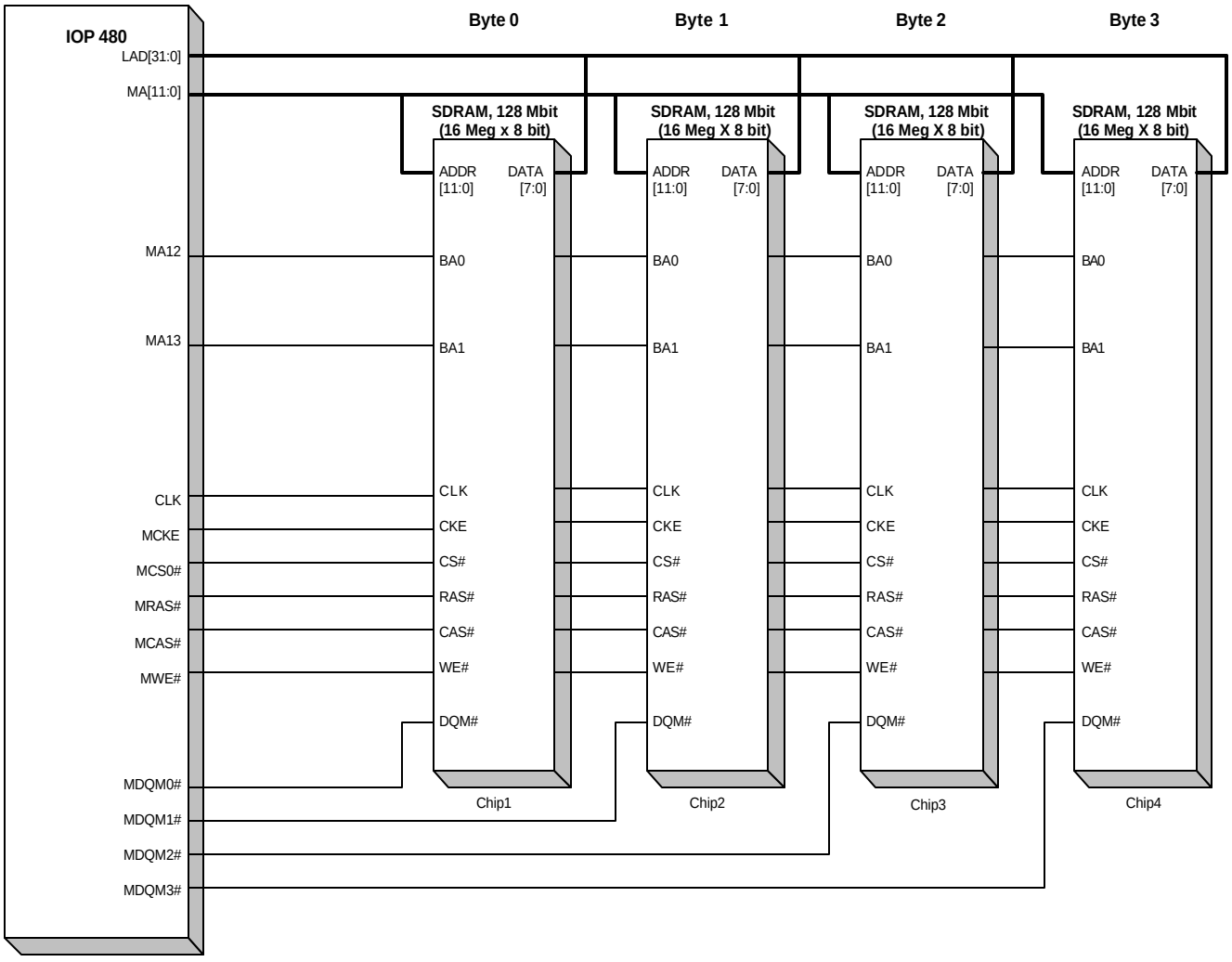

Figure 2-7. 128 Mbit (16 Meg x 8 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 64 Mbytes, (Max = 256 Mbytes)

2.2.5 32 Meg x 4 bit Connection

For 32 Meg x 4 bit configuration memories, as shown in Figure 8, eight SDRAM chips are used to create a 32-bit wide memory totaling 128 Mbytes. For this configuration, two memory chip select pins, MCS0# and MCS1#, are used to access 128 Mbytes. The chip select for the SDRAM, MCS_OUT0#, is created by logically ANDing the MCS0# and MCS1# of the IOP 480. The Boolean equation is MCS_OUT0# = (MCS0# *AND* MCS1#). In addition to MCS0# and MCS1#, the designer may also use MCS2# and MCS3# to generate MCS_OUT1# and connect it to additional 128 Mbit SDRAM chips, as shown in Table 3. This would increase total memory array to 256 Mbytes.

Note from the SDRAM datasheet that the column address of the 32 Meg x 4 bit SDRAM skips ADDR[10] pin and instead connects to ADDR[11] pin. Since the IOP 480 outputs the column address on the MA[10] and not MA[11], an external multiplexer controlled by MCAS# signal is used to select the row address, MA[11], and the column address, MA[10], for the ADDR[11] SDRAM pin.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 64 Mbytes and 11 columns respectively.

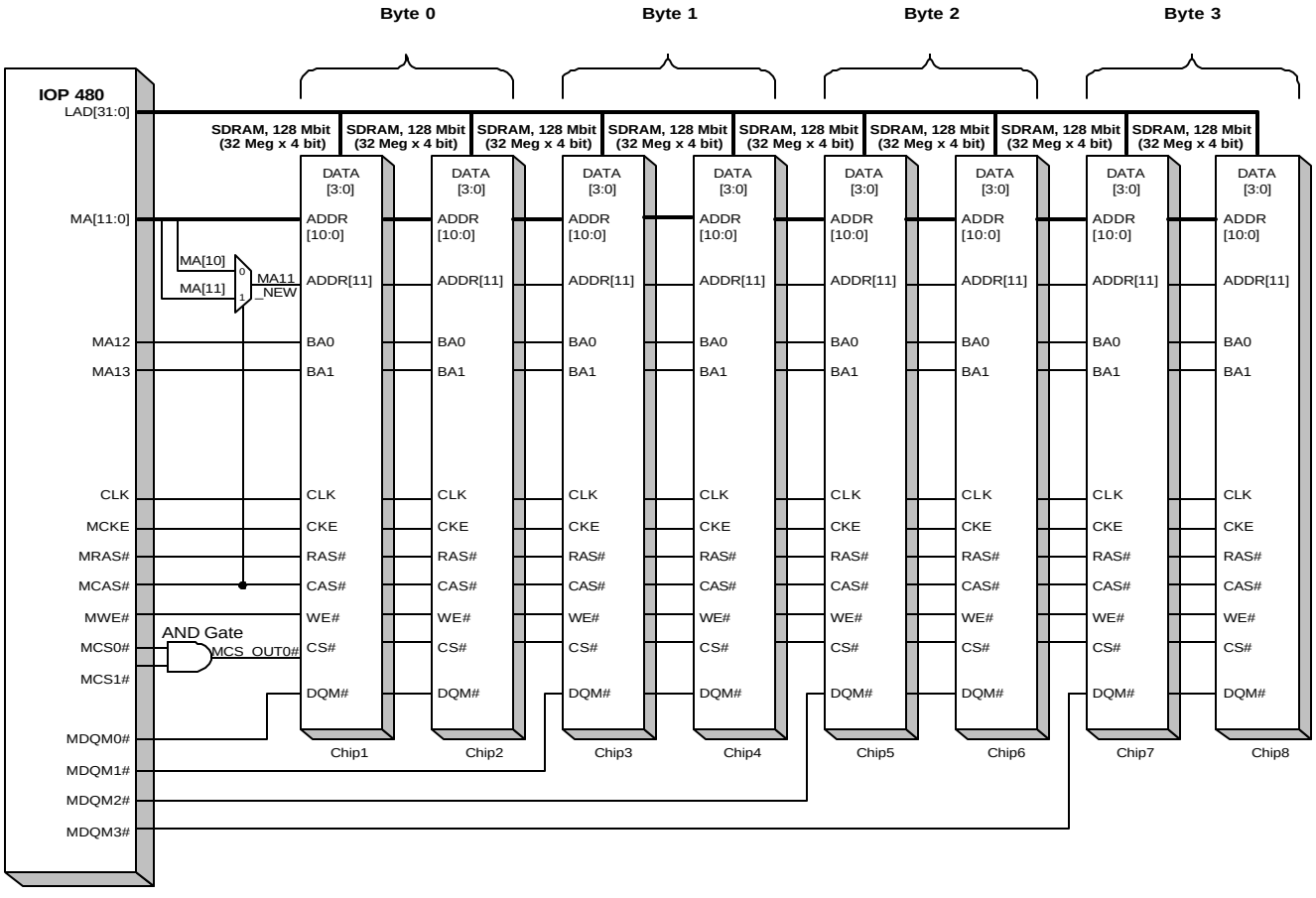

Figure 2-8. 128 Mbit (32 Meg x 4 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 128 Mbytes, (Max = 256 Mbytes)

2.3 64 Mbit, 2M x 32 bit SDRAM

There is a glueless connection between the 64 Mbit (2M x 32 bit) memory and the IOP 480, as shown in Figure 9. The 64 Mbit SDRAM is equivalent to 8 Mbytes. In addition to MCS0#, the designer may also connect MCS1#, MCS2# and MCS3# to additional 64 Mbit SDRAM chips to increase total memory array to 32 Mbytes, as shown in Table 4. If a 256 Mbyte memory array is desirable, then use 64 Mbit SDRAMs with 4 Meg x 16 bit, 8 Meg x 8 bit, or 16 Meg x 4 bit internal configuration since they make a glueless connection to the IOP 480.

The Bank Size and the Number of Columns fields in the IOP 480's SDRAM Control register (DRAMCTL; PCI:154h, LOC:154h) should be programmed as 8 Mbytes and 8 columns respectively.

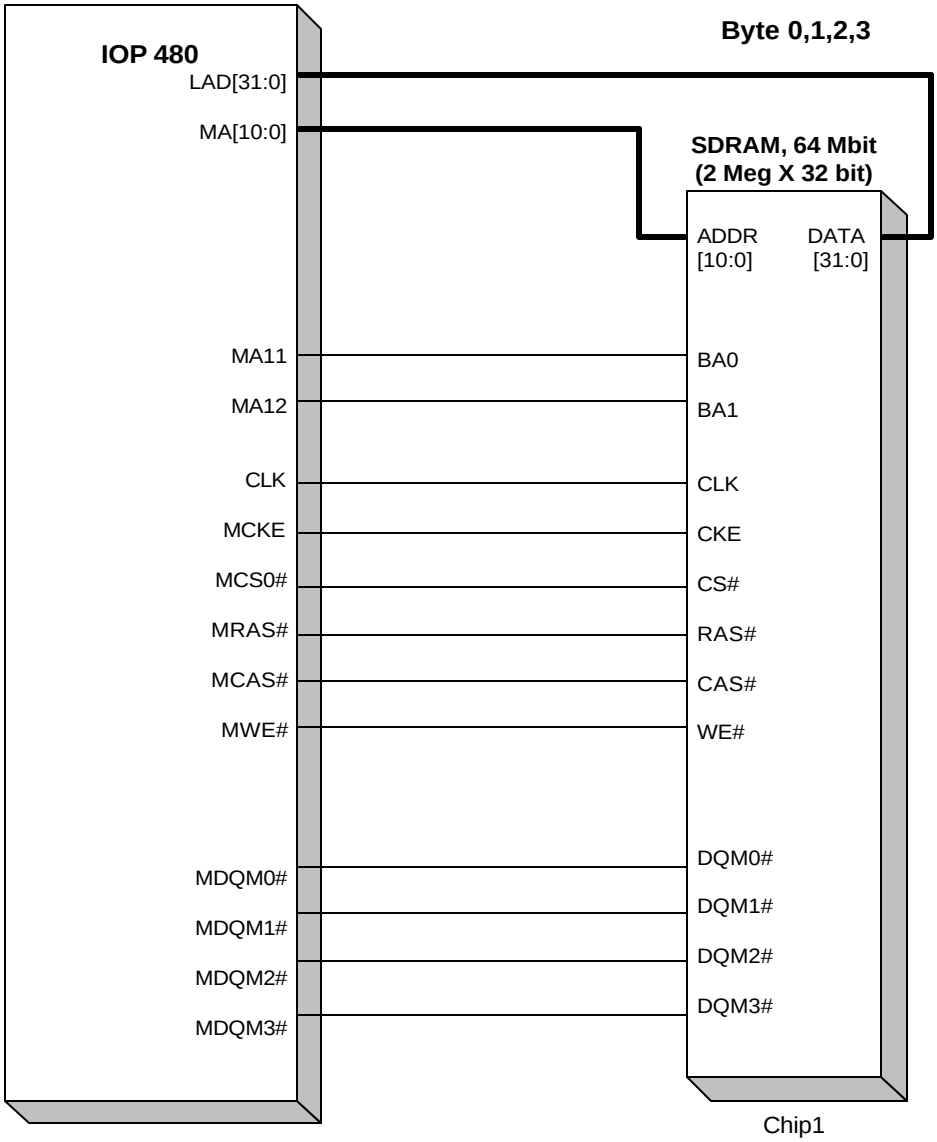

Figure 2-9. 64 Mbit (2 Meg x 32 bit) SDRAM Connection to IOP 480
Total Memory Addressed = 8 Mbytes, (max = 32 Mbytes)

3. Signal Buffering

Signal buffering needs to be taken into account for large memory arrays. The IOP 480 timings listed in the IOP 480 Data Book are specified at 25 pF for a 66 MHz clock on the Local Bus. When the SDRAM loading exceeds the specified 25 pF, external buffers may be required to drive the memory signals. The designer may also forgo the use of external buffers for higher bus loading, if the Local Bus clock can be lowered to less than 66 MHz.

Tables 1, 2, 3 and 4 do not show any buffering specification when connecting to SDRAMs. Buffering requirements depend on the SDRAM configuration, number of SDRAM chips, and Local Bus speed used in the design. It is up to the system designer to determine if external buffers are necessary in the application.

4. Propagation Delay

Very fast logic is required to reduce the propagation delay of the external logic circuits such as AND gate used for the MCS_OUTn# signal and the 2-to-1 multiplexer. The SDRAM memory controller has a programmable 0 or 1 trailing wait states for data during write cycles and a fixed 0 trailing wait state for data during read cycles. Registering of the outputs of the external combinatorial logic should not be used because the data will appear at least 1 clock too late during read cycles. Therefore, the outputs of the external logic must generate within the same clock period as the assertions of the inputs of the external logic and still meet the set up time of the SDRAMs. For large memory arrays, the system designer may need to slow down the Local Bus clock and use the fastest logic available.

5. Using Latch or D Flip-Flop with Clock Enable

A standard way of extracting the extra address signal for use in the 256 Mbit SDRAM is to use an external latch, as shown in Figure 10a. The latch uses the ALE signal to qualify the address from the multiplexed LAD[31:0] bus.

An alternative method of extracting the extra address signal for use in the 256 Mbit SDRAM is to use the ADS# signal and a D flip-flop with Clock Enable to qualify the address from the multiplexed LAD[31:0] bus, as shown in Figure 10b . This alternative method would be used in the case where an external processor doesn't put out an ALE signal but does generate the ADS# signal and it uses the IOP 480 memory controller on the Local Bus.

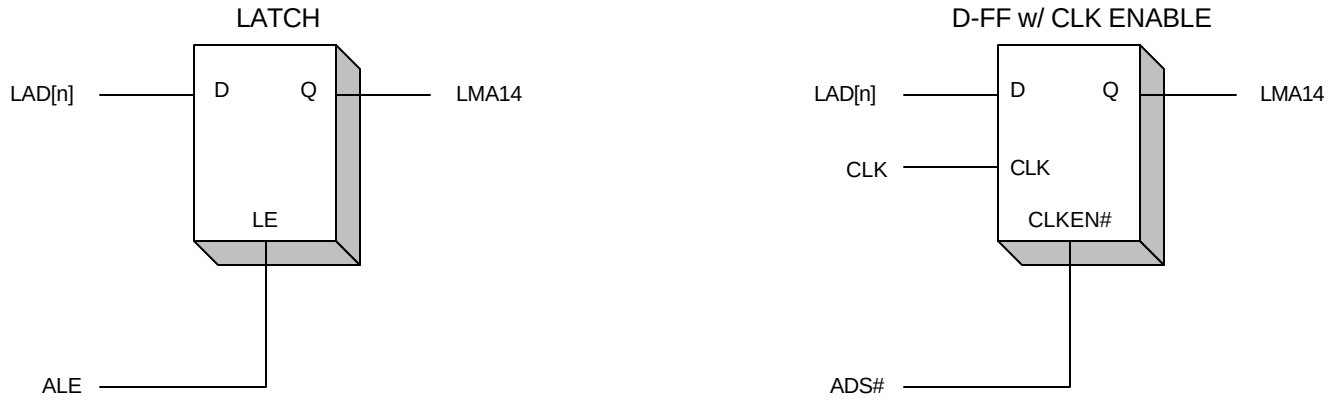

Figure 5-1. (a) Using Latch and (b) Using DFF with Clock Enable

6. SDRAM Connection Tables

Table 6-1. 256 Mbit SDRAM Connection to IOP 480

IOP 480 Signals	256 Mbit SDRAM		
	16M x16 Signals	32M x 8 Signals	64M x 4 Signals
MA0	A0	A0	A0
MA1	A1	A1	A1
MA2	A2	A2	A2
MA3	A3	A3	A3
MA4	A4	A4	A4
MA5	A5	A5	A5
MA6	A6	A6	A6
MA7	A7	A7	A7
MA8	A8	A8	A8
MA9	A9	A9	A9
MA10	A10	A10	A10
MA11	A11	A11	*NA*
MA11_NEW,*Note(2)	*NA*	*NA*	A11
MA12	A12	A12	A12
MA13	BA0	BA0	BA0
LMA14,*Note(3)	BA1	BA1	BA1
MCS0#	CS# (Chips 1,2)	*NA*	*NA*
MCS1#	CS# (Chips 3,4)	*NA*	*NA*
MCS2#	CS# (Chips 5,6)	*NA*	*NA*
MCS3#	CS# (Chips 7,8)	*NA*	*NA*
MCS_OUT0#, *Note(4)	*NA*	CS# (Chips 1-4)	CS# (Chips 1-8)
MCS_OUT1#, *Note(4)	*NA*	CS# (Chips 5-8)	*NA*
MDQM0#	DQML# (Chips 1,3,5,7)	DQM# (Chips 1,5)	DQM# (Chips 1,2)
MDQM1#	DQMH# (Chips 1,3,5,7)	DQM# (Chips 2,6)	DQM# (Chips 3,4)
MDQM2#	DQML# (Chips 2,4,6,8)	DQM# (Chips 3,7)	DQM# (Chips 5,6)
MDQM3#	DQMH# (Chips 2,4,6,8)	DQM# (Chips 4,8)	DQM# (Chips 7,8)
LCLK	CLK	CLK	CLK
MCKE	CKE	CKE	CKE
MRAS#	RAS#	RAS#	RAS#
MCAS#	CAS#	CAS#	CAS#
MWE#	WE#	WE#	WE#
LAD[7:0]	DQ[7:0] (Chips 1,3,5,7)	DQ[7:0] (Chips 1,5)	DQ[3:0] (Chips 1,2)
LAD[15:8]	DQ[15:8] (Chips 1,3,5,7)	DQ[7:0] (Chips 2,6)	DQ[3:0] (Chips 3,4)
LAD[23:16]	DQ[7:0] (Chips 2,4,6,8)	DQ[7:0] (Chips 3,7)	DQ[3:0] (Chips 5,6)
LAD[31:24]	DQ[15:8] (Chips 2,4,6,8)	DQ[7:0] (Chips 4,8)	DQ3:0] (Chips 7,8)

NOTE:

1. ***LMA11_NEW is the output signal of the 2-to-1multiplexer.***
2. ***x16 : Use external latch where LMA14 = Latched Address of IOP 480's LAD25.***
   x 8 : Use external latch where LMA14 = Latched Address of IOP 480's LAD26.
   x 4 : Use external latch where LMA14 = Latched Address of IOP 480's LAD27.
3. ***x16 : No glue logic required.***
   x 8 : External AND gate required : MCS_OUT0# = IOP 480's (MCS0# AND MCS1#), MCS_OUT1# = IOP 480's (MCS2# AND MCS3#).
   x 4 : External AND gate required : MCS_OUT0# = IOP 480's (MCS0# AND MCS1# AND MCS2# AND MCS3#).

Table 6-2. 128 Mbit SDRAM Connection to IOP 480

IOP 480 Signals	128 Mbit SDRAM		
	8M x16 Signals	16M x 8 Signals	32M x 4 Signals
MA0	A0	A0	A0
MA1	A1	A1	A1
MA2	A2	A2	A2
MA3	A3	A3	A3
MA4	A4	A4	A4
MA5	A5	A5	A5
MA6	A6	A6	A6
MA7	A7	A7	A7
MA8	A8	A8	A8
MA9	A9	A9	A9
MA10	A10	A10	A10
MA11	A11	A11	*NA*
MA11_NEW, *Note(2)	*NA*	*NA*	A11
MA12	BA0	BA0	BA0
MA13	BA1	BA1	BA1
MCS0#	CS# (Chips 1,2)	CS# (Chips 1-4)	*NA*
MCS1#	CS# (Chips 3,4)	CS# (Chips 5-8)	*NA*
MCS2#	CS# (Chips 5,6)	CS# (Chips 9-12)	*NA*
MCS3#	CS# (Chips 7,8)	CS# (Chips 13-16)	*NA*
MCS_OUT0#, *Note(5)	*NA*	*NA*	CS# (Chips 1-8)
MCS_OUT1#, *Note(5)	*NA*	*NA*	CS# (Chips 9-16)
MDQM0#	DQML# (Chips 1,3,5,7)	DQM# (Chips 1,5,9,13)	DQM# (Chips 1,2,9,10)
MDQM1#	DQMH# (Chips 1,3,5,7)	DQM# (Chips 2,6,10,14)	DQM# (Chips 3,4,11,12)
MDQM2#	DQML# (Chips 2,4,6,8)	DQM# (Chips 3,7,11,15)	DQM# (Chips 5,6,13,14)
MDQM3#	DQMH# (Chips 2,4,6,8)	DQM# (Chips 4,8,12,16)	DQM# (Chips 7,8,15,16)
LCLK	CLK	CLK	CLK
MCKE	CKE	CKE	CKE
MRAS#	RAS#	RAS#	RAS#
MCAS#	CAS#	CAS#	CAS#
MWE#	WE#	WE#	WE#
LAD[7:0]	DQ[7:0] (Chips 1,3,5,7)	DQ[7:0] (Chips 1,5,9,13)	DQ[3:0] (Chips 1,2,9,10)
LAD[15:8]	DQ[15:8] (Chips 1,3,5,7)	DQ[7:0] (Chips 2,6,10,14)	DQ[3:0] (Chips 3,4,11,12)
LAD[23:16]	DQ[7:0] (Chips 2,4,6,8)	DQ[7:0] (Chips 3,7,11,15)	DQ[3:0] (Chips 5,6,13,14)
LAD[31:24]	DQ[15:8] (Chips 2,4,6,8)	DQ[7:0] (Chips 4,8,12,16)	DQ3:0] (Chips 7,8,15,16)

NOTE:

1. x16 : No glue logic required.
x 8 : No glue logic required.
x 4 : External AND gate required : MCS_OUT0# = IOP 480's (MCS0# AND MCS1#),
MCS_OUT1# = IOP 480's (MCS2# AND MCS3#).

Table 6-3. 64 Mbit (2M x 32 Bit) SDRAM Connection to IOP 480

IOP 480 Signals	64 Mbit SDRAM 2M x 32 Signals
MA0	A0
MA1	A1
MA2	A2
MA3	A3
MA4	A4
MA5	A5
MA6	A6
MA7	A7
MA8	A8
MA9	A9
MA10	A10
MA11	BA0
MA12	BA1
MCS0#	CS# (Chip1)
MCS1#	CS# (Chip2)
MCS2#	CS# (Chip3)
MCS3#	CS# (Chip4)
MDQM0#	DQM0#
MDQM1#	DQM1#
MDQM2#	DQM2#
MDQM3#	DQM3#
LCLK	CLK
MCKE	CKE
MRAS#	RAS#
MCAS#	CAS#
MWE#	WE#
LAD[31:0]	DQ[31:0] (Chips 1,2,3,4)

7. REFERENCES

The following is a list of additional documentation to provide the reader with further information about the IOP 480 and SDRAM.

- PLX IOP 480 Data Book
  PLX Technology, Inc.
  390 Potrero Avenue
  Sunnyvale, CA 94085 USA
  Tel : 408-774-9060
  800-759-3735
  Fax : 408-774-2169
  http://www.plxtech.com

- Micron 256Mb : x4,x8,x16 SDRAM Datasheet
  SDRAM Part # : MT48LC64M4A2,
  MT48LC32M8A2,
  MT48LC16M16A2
  Micron 128Mb : x4,x8,x16 SDRAM Datasheet
  SDRAM Part # : MT48LC32M4A2,
  MT48LC16M8A2,
  MT48LC8M16A2
  Micron 64Mb : x32 SDRAM Datasheet
  SDRAM Part # : MT48LC2M32B2

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  P.O. Box 6
  Boise, ID 83707-0006
  Tel : 208-368-3900
  http://www.micron.com