Vortex86DX

Fact Sheet

32-BIT x86 SoC

V0.9A

Revision History

Rev.	Date	History
REV 0.9A	2008/ 06 / 12	Version 0.9A Released

CONTENTS

1. Overview

The **Vortex86DX** is a high performance and fully static 32-bit x86 compatible processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, direct map 256KB L2 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, DDR2, ROM controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE controller within a single 581-pin BGA package to form a system-on-a-chip. It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

- **X86 Compatible Processor Core**
  - 6 stage pipeline
- **Floating point unit support**
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 256KB L2 Cache
- **DDRII Control Interface**
  - 16 bits data bus
  - DDRII clock support up to 333MHz
  - DDRII size support up to 1Gbytes
- **IDE Controller**
  - Support 2 channels Ultra-DMA 100
  - Primary channel support two SD cards
- **LPC (Low Pin Count) Bus Interface**
  - Support 2 programable registers to decode LPC address
- **MAC Controller x 1**
- **PCI Control Interface**
  - Up to 3 sets PCI master device
  - 3.3V I / O
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
- **DMA Controller**
- **Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- **MTBF Counter**
- **Real Time Clock**
  - Less than 2uA (3.0V) power comsuption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 5 (5 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1/COM2
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port x 1**
  - Support SPP/EPP/ECP mode
- **General Chip Selector**
  - 2 sets extended Chip Selector
  - I / O-map or Memory-map could be configurable
  - I / O Addressing: From 2 byte to 64 K byte
  - Memory Address: From 512 byte to 4G Byte

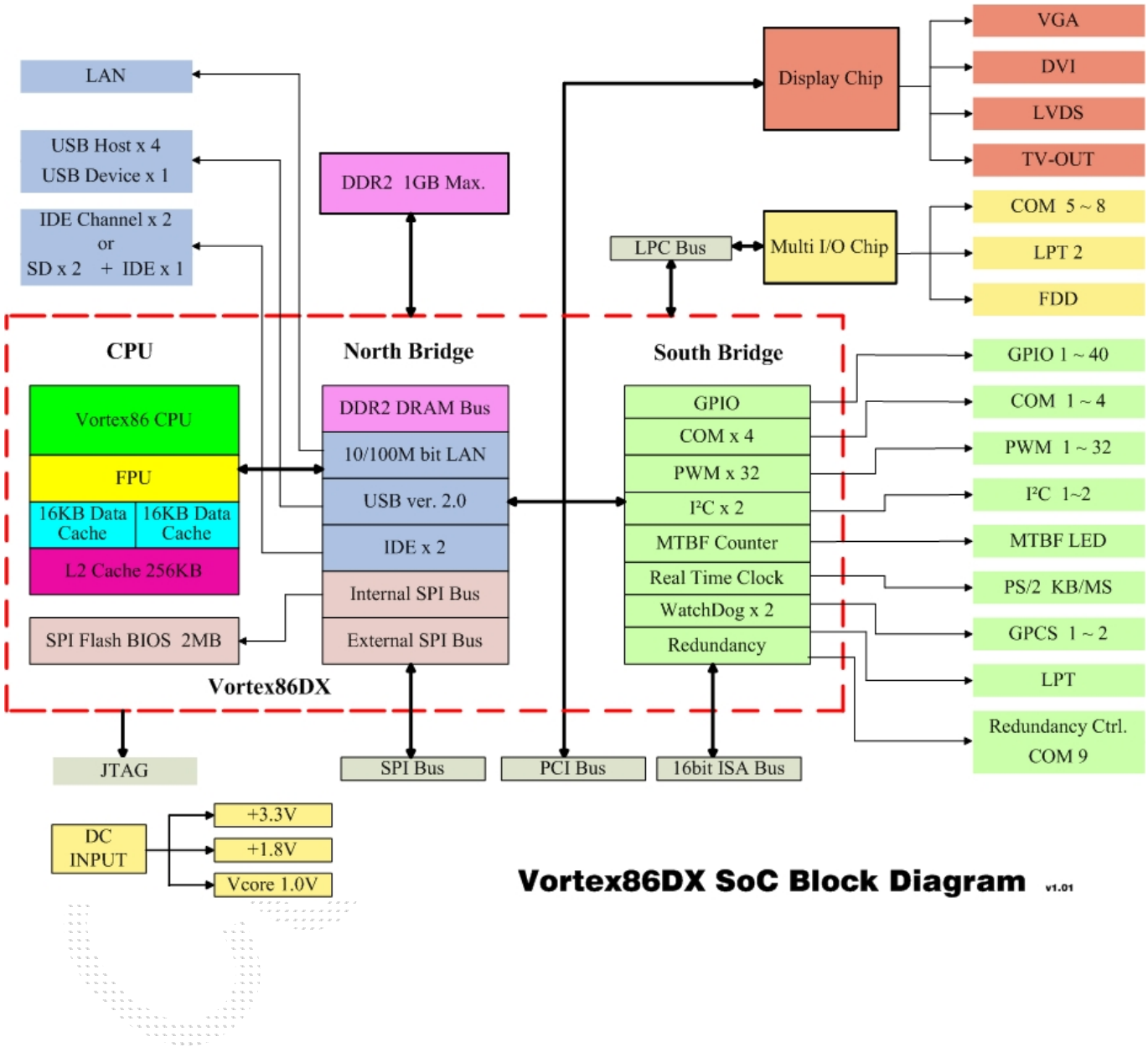
- **General Programmable I/O**
  - Supports 40 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P3 can be program by internal 8051
  - GPIO_P0 and GPIO_P1 with interrupt support (input/output)
- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 4 port
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **Redundant System Support**
- **Speaker out**
- **Embedded 2MB Flash**
  - For BIOS storage
  - The Flash could be disable & use external Flash ROM
- **I^2C bus x 2**
  - Compliant w/t V2.1 (Note 1)
- **Servo Control interface support**
- **General Shift interface support**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 14.318 MHz
  - 32.768 KHz
- **Output clock**
  - 24 MHz
  - 25 MHz
  - PCI clock
  - ISA clock
  - DDRII clock
- **Operating Voltage Range**
  - Core voltage: 0.9 V ~ 1.1V
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - -40℃ ~ 85℃ (Note 2)
- **Package Type**
  - 27x27, 581 Ball BGA

Note 1: The I^2C bus is without the support of some master code which are general call, START and CBUS.

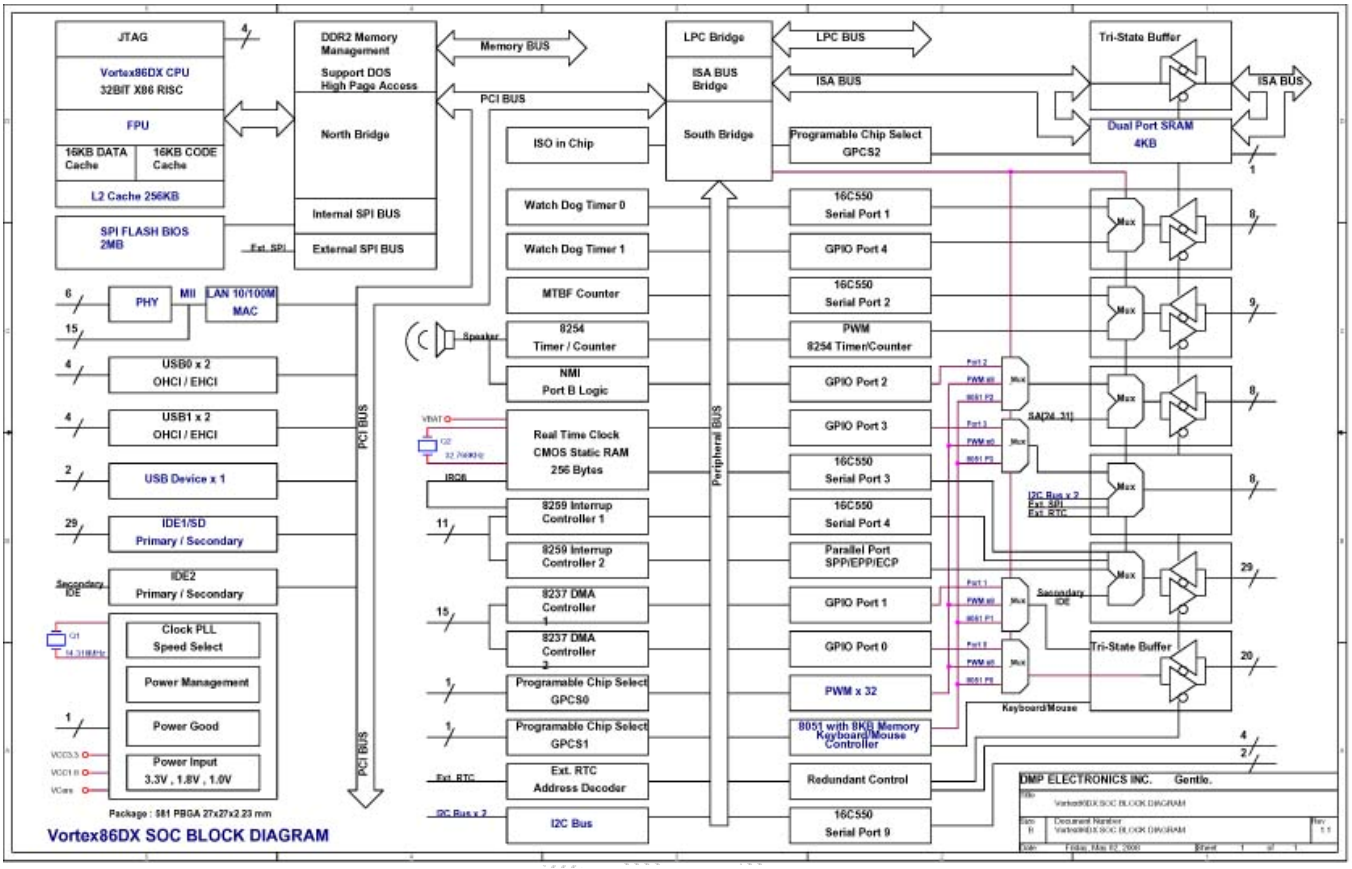
Note 2: The operating temperature of -40℃ ~ 85℃ is only for 600MHz, when CPU is running at higher frequency, the operating temperature range will decrease.

Block Diagram

2.1. System Block Diagram



2.2. Functions Block Diagram

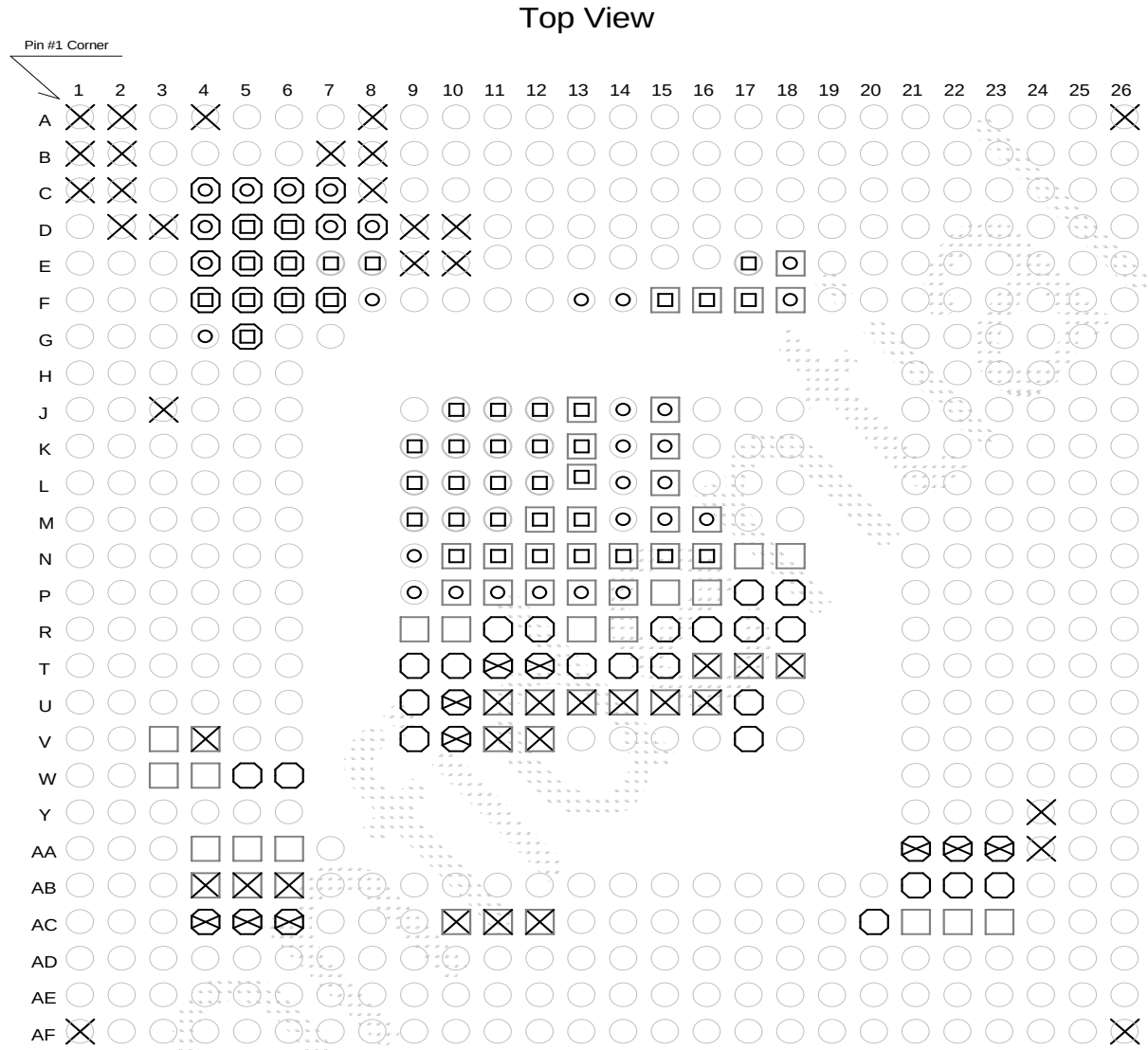


2.3. PCI Device List

ID SEL	AD 11	AD 12	AD 13	AD 14	AD 15	AD 16	AD 17	AD 18	AD 19	AD 20	AD 21	AD 22	AD 23	AD 24	AD 25	AD 26	
Device#	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	
Function0	NB0	PCI Device						SB	MAC		USB0 OHCI	USB1 OHCI	IDE	VGA	Audio (reserved)	USB Device	
Function1	NB1										USB0 OHCI	USB1 EHCI					

3. PIN Function List

3.1. BGA Ball Map



GND_R3 : F15,F16,F17,J13,K13,L13,M12,M13,N10,N11,N12,N13,N14,N15,N16

GNDK : E7,E8,E17,J10,J11,J12,K9,K10,K11,K12,L9,L10,L11,L12,M9,M10,M11

GNDO : D5,D6,E5,E6,F4,F5,F6,F7,G5

Vss_core :T16,T17,T18,U11,U12,U13,U14,U15,U16,V4,V11,V12,AB4,AB5,AB6,AC10,AC11,AC12

Vss_io : P17,P18,R11,R12,R15,R16,R17,R18,T9,T10,T13,T14,T15,U9,U17,V9,V17,W5,W6,AB21,AB22,AB23,AC20

VCC3V : E18,F18,J15,K15,L15,M15,M16,P10,P11,P12,P13,P14

VCCK : F8,F13,F14,G4,J14,K14,L14,M14,N9,P9

VCCO : C4,C5,C6,C7,D4,D7,D8,E4

Vdd_core : T11,T12,U10,V10,AA21,AA22,AA23,AC4,AC5,AC6

Vdd_io : N17,N18,P15,P16,R9,R10,R13,R14,V3,W3,W4,AA4,AA5,AA6,AC21,AC22,AC23

NC Pin : A1,A2,A4,A8,A26,B1,B2,B7,B8,C1,C2,C8,D2,D3,D9,D10,E9,E10,J3,Y24,AA24,AF1,AF26

Signal Pin :

3.2. PIN Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	NC	F17	VSS	P2	PA1	AA14	SD4
A2	NC	F18	VCC3V	P3	PIORDY	AA15	LA20
A3	ODT1	F19	INTB_	P4	PDD10	AA16	SD3
A4	NC	F20	INTC_	P5	PDD12	AA17	GPIO_06/ 8051_GPIO_06/ SERVO6
A5	NC	F21	ATSTN	P6	CTS4_/SIOW_	AA18	GPIO_07/ 8051_GPIO_07/ SERVO7
A6	NC	F22	ATSTP	P9	VCCK	AA19	GPIO_17/ 8051_GPIO_17/ SERVO15
A7	NC	F23	Vdd_io	P10	VCC3V	AA20	GPIO_27/ 8051_GPIO_27/ SERVO23/SA31
A8	NC	F24	CBE0	P11	VCC3V	AA21	Vdd_core
A9	SDRAMCLKN	F25	AD9	P12	VCC3V	AA22	Vdd_core
A10	MA0	F26	AD10	P13	VCC3V	AA23	Vdd_core
A11	MA1	G1	RI3_/SIORDY	P14	VCC3V	AA24	NC
A12	MA10	G2	SOUT3	P15	Vdd_io	AA25	MTBF
A13	MD6	G3	SIN3	P16	Vdd_io	AA26	PWRGOOD
A14	MD5	G4	VCCK	P17	VSS	AB1	RST_DRV
A15	MD2	G5	VSS	P18	VSS	AB2	SA14
A16	MD3	G6	TDO	P21	VBat	AB3	DACK1_
A17	MD4	G7	TCK	P22	RTC_RD_/GPIO_36/ 8051_GPIO_36/ I2C1_SCL	AB4	VSS
A18	PCICLK_1	G21	ROM_CS_	P23	AVSS0	AB5	VSS
A19	PCICLK_0	G22	CBE1	P24	AVDD33_0	AB6	VSS
A20	PCICLK_2	G23	AD11	P25	AVSSPLL0	AB7	SA10
A21	AD29	G24	PAR	P26	REXT0	AB8	AEN
A22	AD28	G25	AD7	R1	PDRQ	AB9	SA17
A23	AD27	G26	AD5	R2	PA0	AB10	DACK5_
A24	AD26	H1	DSR3_/SCBLID_	R3	PIOW_	AB11	SA4
A25	AD25	H2	CTS3_/SIOR_	R4	PDD5	AB12	DRQ0
A26	NC	H3	RTS3_/SRST_	R5	PDD2	AB13	SA2
B1	NC	H4	NC	R6	DCD4_/SA2	AB14	IRQ9
B2	NC	H5	GNDPLL0	R9	Vdd_io	AB15	LA18

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
B3	ODT0	H6	TDI	R10	Vdd_io	AB16	IOR_
B4	CS1_	H21	AD8	R11	VSS	AB17	GPIO_11/ 8051_GPIO_11/ SERVO9
B5	Vref1	H22	AD12	R12	VSS	AB18	GPIO_13/ 8051_GPIO_13/ SERVO11
B6	OCDBIAS	H23	INTA_	R13	Vdd_io	AB19	GPIO_20/ 8051_GPIO_20/ SERVO16/SA24
B7	NC	H24	AD0	R14	Vdd_io	AB20	GPIO_26/ 8051_GPIO_26/ SERVO22/SA30
B8	NC	H25	AD4	R15	VSS	AB21	VSS
B9	SDRAMCLKP	H26	AD3	R16	VSS	AB22	VSS
B10	MA3	J1	INIT_/SDD13	R17	VSS	AB23	VSS
B11	MA5	J2	DCD3_/SDRQ	R18	VSS	AB24	Vdd_pll
B12	MA6	J3	NC	R21	VbatGnd	AB25	24MOUT
B13	MA14	J4	NC	R22	RTC_IRQ8_/GPIO_34/ 8051_GPIO_34/ I2C0_SCL	AB26	25MOUT
B14	DQM0	J5	GNDPLL1	R23	AVDD3	AC1	IRQ6
B15	MD7	J6	SOUT9	R24	AVDD0	AC2	SA6
B16	MD1	J9	TMS	R25	USB3_DM	AC3	SA0
B17	MD0	J10	VSS	R26	USB3_DP	AC4	Vdd_core
B18	PREQ1_	J11	VSS	T1	PDACK_	AC5	Vdd_core
B19	PREQ2_	J12	VSS	T2	PCS0_	AC6	Vdd_core
B20	AD30	J13	VSS	T3	PDD0	AC7	SA8
B21	AD20	J14	VCCK	T4	PDD6	AC8	IRQ12
B22	AD18	J15	VCC3V	T5	PDD1	AC9	DRQ2
B23	AD16	J16	MDC	T6	DSR4_/SCS1_	AC10	VSS
B24	CBE2	J17	TXD02	T9	VSS	AC11	VSS
B25	CBE3	J18	TXD03	T10	VSS	AC12	VSS
B26	AD24	J21	TXC0	T11	Vdd_core	AC13	SBHE_
C1	NC	J22	AD6	T12	Vdd_core	AC14	SD2
C2	NC	J23	VCCAPLL	T13	VSS	AC15	LA23
C3	CKE	J24	ISET	T14	VSS	AC16	GPCS0_
C4	VCCO	J25	AD2	T15	VSS	AC17	GPIO_01/ 8051_GPIO_01/ SERVO1

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C5	VCCO	J26	AD1	T16	VSS	AC18	GPIO_12/ 8051_GPIO_12/ SERVO10
C6	VCCO	K1	PA2	T17	VSS	AC19	GPIO_16/ 8051_GPIO_16/ SERVO14
C7	VCCO	K2	PD0/SDD0	T18	VSS	AC20	VSS
C8	NC	K3	PD3/SDD3	T21	RTC_WR_/GPIO_35/ 8051_GPIO_35/ I2C0_SDA	AC21	Vdd_io
C9	MA2	K4	PD7/SDD7	T22	RTC_PS	AC22	Vdd_io
C10	MA4	K5	PD6/SDD6	T23	LAD0	AC23	Vdd_io
C11	MA7	K6	SIN9	T24	AVSS3	AC24	Vss_pll
C12	BA2	K9	VSS	T25	USB2_DM	AC25	DTR2_/PWM2OUT
C13	WE_	K10	VSS	T26	USB2_DP	AC26	DCD2_/PWM0CLK
C14	MD13	K11	VSS	U1	PCBLID_	AD1	IRQ4
C15	MD11	K12	VSS	U2	PDD4	AD2	SA13
C16	MD9	K13	VSS	U3	PDD8	AD3	SA11
C17	MD14	K14	VCCK	U4	PDD7	AD4	DRQ1
C18	PREQ0_	K15	VCC3V	U5	PDD11	AD5	SA18
C19	PGNT0_	K16	MDIO	U6	RTS4_/SINT	AD6	SA7
C20	AD31	K17	TXD01	U9	VSS	AD7	IRQ5
C21	AD21	K18	TXD00	U10	Vdd_core	AD8	0WS_
C22	AD19	K21	TXEN0	U11	VSS	AD9	DACK0_
C23	AD17	K22	DUPLEX	U12	VSS	AD10	SD13
C24	FRAME_	K23	VSSAPLL	U13	VSS	AD11	DACK6_
C25	IRDY_	K24	VCCA0	U14	VSS	AD12	SD8
C26	TRDY_	K25	TXN	U15	VSS	AD13	LA22
D1	UD_DP	K26	TXP	U16	VSS	AD14	SD6
D2	NC	L1	STB_/SCS0_	U17	VSS	AD15	LA19
D3	NC	L2	PD1/SDD1	U18	LFRAME_	AD16	GPCS1_
D4	VCCO	L3	AFD_/SDD15	U21	ExtSysFailIn_	AD17	GPIO_00/ 8051_GPIO_00/ SERVO0
D5	VSS	L4	ACK_/SDD11	U22	SYSFAILOut_	AD18	GPIO_23/ 8051_GPIO_23/ SERVO19/SA27
D6	VSS	L5	PD5/SDD5	U23	LAD1	AD19	GPIO_15/ 8051_GPIO_15/ SERVO13

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
D7	VCCO	L6	PE/SDD9	U24	AVDD33_1	AD20	GPIO_25/ 8051_GPIO_25/ SERVO21/SA29
D8	VCCO	L9	VSS	U25	AVSSPLL1	AD21	TXD_EN1
D9	NC	L10	VSS	U26	REXT1	AD22	RI1_/GPIO_43/ SERVO27
D10	NC	L11	VSS	V1	PIOR_	AD23	DTR1_/GPIO_45/ SERVO29
D11	MA9	L12	VSS	V2	PDD15	AD24	RI2_/PWM1CLK
D12	BA0	L13	VSS	V3	Vdd_io	AD25	RTS2_/PWM1OUT
D13	RAS_	L14	VCCK	V4	VSS	AD26	CTS2_/PWM1GATE
D14	DQS0	L15	VCC3V	V5	RI4_/SA1	AE1	MEMCS16_
D15	MD12	L16	COL0	V6	DTR4_/SA0	AE2	IRQ3
D16	MD15	L17	RXD01	V9	VSS	AE3	IOCS16_
D17	DQM1	L18	RXD00	V10	Vdd_core	AE4	BALE
D18	PGNT1_	L21	RXDV0	V11	VSS	AE5	SA9
D19	PGNT2_	L22	LINK/ACTIVE	V12	VSS	AE6	IRQ10
D20	AD23	L23	VSSA0	V13	KBCLK/KBRST	AE7	IRQ7
D21	VSS	L24	VCCA1	V14	MSCLK	AE8	IOCHRDY_
D22	TEST2	L25	RXN	V15	MSDATA	AE9	LA17
D23	TEST0	L26	RXP	V16	KBDATA/A20GATE_	AE10	SD9
D24	DEVSEL_	M1	PRST_	V17	VSS	AE11	SD10
D25	STOP_	M2	PD2/SDD2	V18	LDRQ_	AE12	MEMW_
D26	PCIRST_	M3	SLIN_/SDD12	V21	EXT_GPCS_	AE13	SA5
E1	UD_DM	M4	PD4/SDD4	V22	EXT_SWITCH_FAIL_	AE14	LA21
E2	TEST7	M5	BUSY/SDD10	V23	LAD2	AE15	DRQ7
E3	TEST5	M6	SOUT4	V24	AVDDPLL1	AE16	SD15
E4	VCCO	M9	VSS	V25	RTC_XOUT	AE17	GPIO_04/ 8051_GPIO_04/ SERVO4
E5	VSS	M10	VSS	V26	RTC_XIN	AE18	GPIO_05/ 8051_GPIO_05/ SERVO5
E6	VSS	M11	VSS	W1	PCS1_	AE19	GPIO_14/ 8051_GPIO_14/ SERVO12
E7	VSS	M12	VSS	W2	PDD14	AE20	GPIO_24/ 8051_GPIO_24/ SERVO20/SA28

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
E8	VSS	M13	VSS	W3	Vdd_io	AE21	SIN1/GPIO_44/ SERVO28
E9	NC	M14	VCCK	W4	Vdd_io	AE22	SOUT1/GPIO_41/ SERVO25
E10	NC	M15	VCC3V	W5	VSS	AE23	CTS1_/GPIO_47/ SERVO31
E11	MA11	M16	VCC3V	W6	VSS	AE24	SOUT2/PWM0OUT
E12	CAS_	M17	RXD02	W21	E_SPI_CS/GPIO_30/ 8051_GPIO_30/ GSF_CH0	AE25	TXD_EN2/PWM2GATE
E13	CS0_	M18	RXD03	W22	E_SPI_CLK/GPIO_31/ 8051_GPIO_31/ GSF_CH1	AE26	DSR2_/PWM0GATE
E14	MD10	M21	RXC0	W23	LAD3	AF1	NC
E15	MD8	M22	VSSABG	W24	SERIRQ	AF2	IRQ14
E16	DQS1	M23	VCCABG	W25	AVSS2	AF3	IRQ11
E17	VSS	M24	VSSA1	W26	AVDD2	AF4	IRQ15
E18	VCC3V	M25	USB1_DM	Y1	SD1	AF5	TC
E19	INTD_	M26	USB1_DP	Y2	IOW_	AF6	REFRESH_
E20	AD22	N1	PDD3	Y3	DACK3_	AF7	DACK7_
E21	TEST3	N2	PINT	Y4	SD5	AF8	OSC14M
E22	TEST1	N3	PDD9	Y5	DRQ3	AF9	MEMR_
E23	TEST4	N4	ERR_/SDD14	Y6	SD7	AF10	SYSCLK
E24	AD15	N5	SLCT/SDD8	Y21	E_SPI_DO/GPIO_32/ 8051_GPIO_32/ GSF_CH2	AF11	DRQ6
E25	AD14	N6	SIN4	Y22	E_SPI_DI/GPIO_33/ 8051_GPIO_33/ GSF_CLK	AF12	SA1
E26	AD13	N9	VCCK	Y23	SPEAKER	AF13	DACK2_
F1	DTR3_/SDACK_	N10	VSS	Y24	NC	AF14	SD11
F2	TEST8	N11	VSS	Y25	XIN_14.318	AF15	SD12
F3	TEST6	N12	VSS	Y26	XOUT_14.318	AF16	SD14
F4	VSS	N13	VSS	AA1	SA15	AF17	GPIO_02/ 8051_GPIO_02/ SERVO2
F5	VSS	N14	VSS	AA2	SA12	AF18	GPIO_03/ 8051_GPIO_03/ SERVO3

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
F6	VSS	N15	VSS	AA3	SA16	AF19	GPIO_10/ 8051_GPIO_10/ SERVO8
F7	VSS	N16	VSS	AA4	Vdd_io	AF20	GPIO_22/ 8051_GPIO_22/ SERVO18/SA26
F8	VCCK	N17	Vdd_io	AA5	Vdd_io	AF21	GPIO_21/ 8051_GPIO_21/ SERVO17/SA25
F9	MA8	N18	Vdd_io	AA6	Vdd_io	AF22	RTS1_/GPIO_42/ SERVO26
F10	MA12	N21	RTC_AS/GPIO_37/ 8051_GPIO_37/ I2C1_SDA	AA7	SD0	AF23	DSR1_/GPIO_46/ SERVO30
F11	MA13	N22	AVDD1	AA8	SMEMW_	AF24	DCD1_/GPIO_40/ SERVO24
F12	BA1	N23	AVDDPLL0	AA9	SA19	AF25	SIN2/PWM2CLK
F13	VCCK	N24	AVSS1	AA10	SMEMR_	AF26	NC
F14	VCCK	N25	USB0_DM	AA11	DRQ5		
F15	VSS	N26	USB0_DP	AA12	SA3		
F16	VSS	P1	PDD13	AA13	IOCHCK_		

3.3. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, 25MOUT, XOUT_14318, XIN_14318, MTBF, 24MOUT, SPEAKER	7 PINs
DDRII	SDRAMCLKP,SDRAMCLKN,RAS_ ,CAS_,WE_,CKE,CS_[1:0],DQM[1:0],DQS[1:0],ODT[1:0], OCDBIAS, Vref1, BA[2:0],MD[15:0], MA[14:0]	50 PINs
USB Interface	USB_DP[3:0],USB_DM[3:0],REXT[1:0]	10 PINs
PCI	PREQ_[2:0],PGNT_[2:0],PCIRST_,PCICLK_0, PCICLK_1,PCICLK_2,AD[31:0],CBE[3:0], FRAME_, IRDY_, TRDY_, DEVSEL_, STOP_,PAR, INTA_, INTB_, INTC_, INTD_	56 PINs
External SPI/ GPIO port 3[3:0]/ 8051 GPIO port 3[3:0]/ General Shift	E_SPI_CS/GPIO_30/8051_GPIO_30/GSF_CH0, E_SPI_CLK/GPIO_31/8051_GPIO_31/GSF_CH1, E_SPI_DO/GPIO_32/8051_GPIO_32/GSF_CH2, E_SPI_DI/GPIO_33/8051_GPIO_33/GSF_CLK	4 PINs
ISA BUS	IOCHCK_, SD[15:0], IOCHRDY_, AEN, SA[19:0], SBHE_, LA[23:17], MEMR_, MEMW_, RST_DRV, IRQ[15:14], IRQ[12:9], IRQ[7:3], DRQ[7:5], DRQ[3:0], 0WS_, SMEMR_, SMEMW_, IOW_, IOR_, DACK_[7:5], DACK_[3:0], REFRESH_, SYSCLK, TC, BALE, MEMCS16_,IOCS16_, OSC14M	87 PINs
Chip Selection	GPCS0_, GPCS1_ , ROM_CS_	3 PINs
Redundant	ExtSysFailIn_, SYSFAILOut_, Ext_Switch_fail_, EXT_GPCS_	4 PINs
KBD / MOUSE	KBCLK/KBRST_, KBDATA/A20GATE_, MSCLK, MSDATA	4 PINs
RTC/ GPIO PORT 3[7-4]/ 8051 GPIO PORT 3[7-4]/ I2C	RTC_AS/GPIO_37/8051_GPIO_37/I2C1_SDA, RTC_RD_/GPIO_36/8051_GPIO_36/I2C1_SCL, RTC_WR_/GPIO_35/8051_GPIO_35/I2C0_SDA, RTC_IRQ8_/GPIO_34/8051_GPIO_34/I2C0_SCL, RTC_PS, RTC_Xout, RTC_Xin	7 PINs
COM1/ GPIO PORT 4/ SERVO[31:24]	SIN1/GPIO_44/SERVO28, SOUT1/GPIO_41/SERVO25, RTS1_/GPIO_42/SERVO26, CTS1_/GPIO_47/SERVO31 , DSR1_/GPIO_46/SERVO30, DCD1_/GPIO_40/SERVO24 , RI1_/GPIO_43/SERVO27 , DTR1_/GPIO_45/SERVO29, TXD_EN1	9 PINs
COM2/ PWM	SIN2 / PWM2CLK, SOUT2 / PWM0OUT, RTS2_ / PWM1OUT, CTS2_ / PWM1GATE, DSR2_ / PWM0GATE, DCD2_ / PWM0CLK, RI2_ / PWM1CLK, DTR2_ / PWM2OUT, TXD_EN2 / PWM2GATE	9 PINs
COM 3,4,9	SIN3, SOUT3, SIN4, SOUT4, SIN9, SOUT9	6 PINs
Primary IDE/SD	PDD0/SD0_DATA2, PDD1/SD0_DATA3, PDD2/SD0_CMD, PDD3/SD0_CLK, PDD4/SD0_DATA0, PDD5/SD0_DATA1, PDD6/SD0_CD, PDD7/SD0_WP, PDD8/SD1_DATA2, PDD9/SD1_DATA3, PDD10/SD1_CMD, PDD11/SD1_CLK, PDD12/SD1_DATA0, PDD13/SD1_DATA1, PDD14/SD1_CD, PDD15/SD1_WP, PRST_, PDRQ, PIOW_, PIOR_, PIORDY, PDACK_, PINT, PA[2 :0], PCBLID_, PCS0_, PCS1_	29 PINs
Secondary IDE/COM3, COM4 and	PD/SDD[7 :0], SLCT/SDD8, PE/SDD9, BUSY/SDD10, ACK_/SDD11, SLIN_/SDD12, INIT_/SDD13, ERR_/SDD14, AFD_/SDD15, RTS3_/SRST_, DCD3_/SDRQ, CTS4_/SIOW_, CTS3_/SIOR_, RI3_/SIORDY,	29 PINs

Function	Symbol	PIN Sum
Parallel Port	DTR3_/SDACK_, RTS4_/SINT, RI4_/SA1, DSR3_/SCBLID_, DTR4_/SA0, DCD4_/SA2, STB_/SCS0_, DSR4_/SCS1_	
LPC	SERIRQ, LAD[3:0], LFRAME_, LDRQ_	7 PINs
GPIO PORT 0,1,2/ 8051 GPIO PORT 0, 1, 2/ SERVO[23:0]/ SA[31:24]	GPIO_0[7:0] /8051_GPIO_0[7:0]/SERVO[7:0],GPIO_1[7:0] /8051_GPIO_1[7:0]/SERVO[15:8], GPIO_20/8051_GPIO_20/SERVO16/SA24, GPIO_21/8051_GPIO_21/SERVO17/SA25, GPIO_22/8051_GPIO_22/SERVO18/SA26, GPIO_23/8051_GPIO_23/SERVO19/SA27, GPIO_24/8051_GPIO_24/SERVO20/SA28, GPIO_25/8051_GPIO_25/SERVO21/SA29, GPIO_26/8051_GPIO_26/SERVO22/SA30, GPIO_27/8051_GPIO_27/SERVO23/SA31	24 PINs
Ethernet	Link/Active, DUPLEX, ISET, ATSTP, ATSTN, TXN, TXP, RXN, RXP MDC,MDIO, COL0, RXC0, RXD00, RXD01, RXD02, RXD03, RXDV0, TXC0, TXD00, TXD01, TXD02, TXD03, TXEN0	24 PINs
USB Device	UD_DP, UD_DM	2 PINs
JTAG	TDO, TMS, TCK, TDI	4 PINs
TEST PIN	TEST[8:0]	9 PINs
1 V Power	VCCK : 10 PINS	10 PINs
1.8V Power	VCCO: 8 PINs, Vdd_core: 10 PINs, AVDD[3:0], AVSS[3:0], AVDDPLL[1:0],AVSSPLL[1:0], GNDPLL: 2 PINs,	32 PINs
Battery Power	Vbat, VbatGnd : 2 PINs	2 PINs
3.3V Power	Vdd_pll, Vss_pll, VCC3V : 12 PINs, Vdd_io : 18 PINs, VSSAPLL, VCCAPLL, VSSABG, VCCABG, VCCA0, VSSA0, VCCA1, VSSA1,AVDD33_[1:0]	42 PINs
Digital Ground	VSS : PINs	83 PINs

3.4. Signal Description

This chapter provides a detailed description of Vortex86DX signals. A signal with the symbol "_" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

OD Output pin with open-drain

I/O Bi-directional Input/Output pin

- **System (7 PINs)**

PIN No.	Symbol	Type	Description
AA26	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The Vortex86DX uses this signal to generate reset sequence for the system.
AB26	25MOUT	O	***25MHz Clock output.***
Y26	XOUT_14318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
Y25	XIN_14318	I	***Crystal-in.*** 14.318MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
AA25	MTBF	O	***MTBF Flag output.***
AB25	24MOUT	O	***24MHz Clock output***
Y23	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker
	Strap_EPS	I	***Ethernet PHY Select*** Pull it low to select internal PHY. Pull it high to select External PHY. Tri-state to select Internal PHY AFE-test Mode. Default internal tri-state.

- **DDRII Interface (50 PINs)**

PIN No.	Symbol	Type	Description
B9	SDRAMCLKP	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
A9	SDRAMCLKN	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
D13	RAS_	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DDRII clock. This signal also allows row access and pre-charge.
E12	CAS_	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DDRII clock. This signal also allows column access and pre-charge.
C13	WE_	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.

PIN No.	Symbol	Type	Description
C3	CKE	I	***Clock Enable.*** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.
B4, E13	CS_[1:0]	O	***Chip Select CS_[1:0].*** These two pins activate the DDRII devices. First Bank of DDRII accepts any command when the CS0_ pin is active low. Second Bank of DDRII accepts any command when the CS1_ pin is active low.
D17, B14	DQM[1:0]	O	***Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
E16, D14	DQS[1:0]	I/O	***Data Strobe DQS[1:0] for DDRII only.*** Output with write data, input with the read data for source synchronous operation.
B3, A3	ODT[1:0]	O	***On Die Termination Control for DDRII only.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.
B6	OCDBIAS	I	***OCD BIAS for DDRII only.*** The OCD bias circuit generates a bias level voltage that makes the reference resistance for driver impedance calibration an appropriate value
B5	Vref1	O	***Reference voltage for DDRII only.*** Reference voltage for inputs for SSTL interface.
F12, D12, C12	BA[2:0]	O	***Bank Address BA[2:0].*** These pins are connected to DDRII as bank address pins.
D16, C17, C14, D15, C15, E14, C16, E15, B15, A13, A14, A17, A16, A15, B16, B17	MD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the DDRII data bus.
A10	MA0	O	***Memory Address MA0.*** Normally, these pins are used as the row and column address for DDRII.
A11	MA1	O	***Memory Address MA1.*** Normally, these pins are used as the row and column address for DDRII.
	Strap1	I	***Strap1.*** Pull it high to enable GPIO2. Default pull high. Pull it low to enable Address[31:24].
C9	MA2	O	***Memory Address MA2.*** Normally, these pins are used as the row and column address for DDRII.
B10	MA3	O	***Memory Address MA3.*** Normally, these pins are used as the row and column address for DDRII.
	Strap3	I	***Strap3.*** PLL_TEST_OUT_EN_, Default pull low. Pull it high to enable PLL_TEST_OUT_EN_. Pull it low to disable PLL_TEST_OUT_EN_.
C10	MA4	O	***Memory Address MA4.*** Normally, these pins are used as the row and column address for DDRII.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td>Strap4</td><td>I</td><td>Strap4. DDRII clock select, Default tri-state.
<table>
<tr><td>STRAP[10,4]</td><td>Frequency(MHz)</td></tr>
<tr><td>2’b01</td><td>166 (VortexDX default)</td></tr>
<tr><td>2’b1z</td><td>200</td></tr>
<tr><td>2’b10</td><td>233</td></tr>
<tr><td>2’b00</td><td>266</td></tr>
<tr><td>2’b0z</td><td>300</td></tr>
<tr><td>2’bz1</td><td>333</td></tr>
<tr><td>2’bz0</td><td>366</td></tr>
<tr><td>2’bzz</td><td>400</td></tr>
</table></td></tr>
<tr><td>11,B12,B11</td><td>MA[7:5]</td><td>O</td><td>Memory Address MA[7:5]. Normally, these pins are used as the row and column address for DDRII.

Strap[7:5]. CPU Clock select, default tri-state.
<table>
<tr><td>STRAP[7,6,5]</td><td>CPU Clock (MHz)</td></tr>
<tr><td>3’b100</td><td>Bypass mode (default)</td></tr>
<tr><td>3’b101</td><td>SYN_DISABLE_
(CPU clock same to DDRII Clock)</td></tr>
<tr><td>3’b11z</td><td>500</td></tr>
<tr><td>3’b110</td><td>600</td></tr>
<tr><td>3’b111</td><td>700</td></tr>
<tr><td>3’bzzz</td><td>800</td></tr>
<tr><td>3’bzz0</td><td>900</td></tr>
<tr><td>3’bzz1</td><td>933</td></tr>
<tr><td>3’bz0z</td><td>966 (Not support PLL, not applicable)</td></tr>
<tr><td>3’bz00</td><td>1000</td></tr>
<tr><td>3’bz01</td><td>1033</td></tr>
<tr><td>3’bz1z</td><td>1066</td></tr>
<tr><td>3’bz10</td><td>1066</td></tr>
<tr><td>3’bz11</td><td>1066</td></tr>
<tr><td>3’b0zz</td><td>1100</td></tr>
<tr><td>3’b0z0</td><td>1133</td></tr>
<tr><td>3’b0z1</td><td>1166</td></tr>
<tr><td>3’b00z</td><td>1200</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="2">F9</td><td>MA8</td><td>O</td><td>Memory Address MA8. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap8</td><td>I</td><td>Strap8. Pull it high to enable Vortex86DX JTAG. Default internal pull-high.</td></tr>
<tr><td rowspan="2">D11</td><td>MA9</td><td>O</td><td>Memory Address MA9. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap9</td><td>I</td><td>Strap9. Pulled low: 33 PINS is for IDE2.
Pulled high: 33 PINS is for COM3/4 and Parallel Port. Default internal pull-high.</td></tr>
<tr><td rowspan="2">A12</td><td>MA10</td><td>O</td><td>Memory Address MA10. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap10</td><td>I</td><td>Strap10. DDRII clock select, Default tri-state.
<table>
<tr><td>STRAP[10,4]</td><td>Frequency(MHz)</td></tr>
<tr><td>2’b01</td><td>166 (VortexDX default)</td></tr>
<tr><td>2’b1z</td><td>200</td></tr>
<tr><td>2’b10</td><td>233</td></tr>
<tr><td>2’b00</td><td>266</td></tr>
<tr><td>2’b0z</td><td>300</td></tr>
<tr><td>2’bz1</td><td>333</td></tr>
<tr><td>2’bz0</td><td>366</td></tr>
<tr><td>2’bzz</td><td>400</td></tr>
</table></td></tr>
<tr><td rowspan="2">E11</td><td>MA11</td><td>O</td><td>Memory Address MA11. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap11</td><td>I</td><td>Strap11. Pulled low is Internal RTC. Default internal pull-low.
Pulled high is External RTC</td></tr>
<tr><td rowspan="2">F10</td><td>MA12</td><td>O</td><td>Memory Address MA12. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap12</td><td>I</td><td>Strap12. 0 : flash-8bits
1 : Internal SPI. Default internal pull-high.</td></tr>
<tr><td rowspan="2">F11</td><td>MA13</td><td>O</td><td>Memory Address MA13. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>Strap13</td><td>I</td><td>Strap13. 0 : High speed PCI clock
1 : Normal speed PCI clock. Default internal pull-high.</td></tr>
<tr><td>B13</td><td>MA14</td><td>O</td><td>Memory Address MA14. Normally, these pins are used as the row and column address for DDRII.</td></tr>
</table>

- **USB Interface (10 PINs)**

PIN No.	Symbol	Type	Description
N26 N25	USB0_DP USB0_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.

PIN No.	Symbol	Type	Description
M26 M25	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
T26 T25	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
R26 R25	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
U26	REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 470Ω ±1%
P26	REXT0	I	Universal Serial Bus Controller 0 External Reference Resistance 470Ω ±1%

- **PCI Bus Interface (56 PINs)**

PIN No.	Symbol	Type	Description
B19, B18, C18	PREQ_[2:0]	I	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.
D19, D18 ,C19	PGNT_[2:0]	O	***PCI Bus Grant.*** These signals are the PCI bus grant output signals generated by the internal PCI arbiter.
D26	PCIRST_	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
A19 A18 A20	PCICLK_0 PCICLK_1 PCICLK_2	O	***PCI Clock Output.*** This clock is used by all of the Vortex86DX logic that is in the PCI clock domain.
C20, B20, A21 A22, A23, A24, A25, B26, D20, E20, C21, B21, C22, B22, C23, B23, E24, E25, E26, H22, G23, F26, F25, H21, G25, J22, G26, H25, H26, J25, J26, H24	AD[31:0]	I/O	***PCI Address and Data.*** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.
B25, B24, G22, F24	CBE[3:0]	I/O	***Bus Command and Byte Enables.*** During the address phase, CBE[3:0] define the Bus Command. During the data phase, CBE[3:0] define the Byte Enables.
C24	FRAME_	I/O	***PCI Frame.*** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.

PIN No.	Symbol	Type	Description
C25	IRDY_	I/O	***PCI Initiator Ready.*** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_ and TRDY_ are asserted low during the rising edge of the PCI clock.
C26	TRDY_	I/O	***PCI Target Ready*****.** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_ and TRDY_ are asserted low during the rising edge of the PCI clock.
D24	DEVSEL_	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
D25	STOP_	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
G24	PAR	I/O	***PCI Parity*****.** This pin is driven to even parity by PCI master over the AD[31:0] and CBE[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
H23	INTA_	I	***PCI INTA_*****.** PCI interrupt input A. It connects to PCI INTA_ when normal modes of PCI Interrupts are supported.
F19	INTB_	I	***PCI INTB_*****.** PCI interrupt input B. It connects to PCI INTB_ when normal modes of PCI Interrupts are supported.
F20	INTC_	I	***PCI INTC_*****.** PCI interrupt input C. It connects to PCI INTC_ when normal modes of PCI Interrupts are supported.
E19	INTD_	I	***PCI INTD_*****.** PCI interrupt input D. It connects to PCI INTD_ when normal modes of PCI Interrupts are supported.

- **EXTERNAL SPI/GPIO PORT[3-0]/8051 GPIO PORT[3-0]/General Shifter Interface (4 PINs)**

PIN No.	Symbol	Type	Description
W21	E_SPI_CS_	O	***External SPI Chip Select***
	GPIO_30	I/O	***General-Purpose Input/Output Port 3 bit 0.***
	8051_GPIO_30	I/O	***8051 General-Purpose Input/Output Port 3 bit 0.***
	GSF_CH0	I/O	***General Shifter Channel 0***
W22	E_SPI_CLK	O	***External SPI Clock***
	GPIO_31	I/O	***General-Purpose Input/Output Port 3 bit 1***
	8051_GPIO_31	I/O	***8051 General-Purpose Input/Output Port 3 bit 1***
	GSF_CH1	I/O	***General Shifter Channel 1***
Y21	E_SPI_DO	O	***External SPI Data Ouput it connects to device SDI input.***
	GPIO_32	I/O	***General-Purpose Input/Output Port 3 bit 2***
	8051_GPIO_32	I/O	***8051 General-Purpose Input/Output Port 3 bit 2***
	GSF_CH2	I/O	***General Shifter Channel 2***
Y22	E_SPI_DI	I	***External SPI Data Input t it connects to device SDI output.***
	GPIO_33	I/O	***General-Purpose Input/Output Port 3 bit 3***
	8051_GPIO_33	I/O	***8051 General-Purpose Input/Output Port 3 bit 3***
	GSF_CLK	O	***General Shifter reference Clock***

- **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
AA13	IOCHCK_	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
AE16, AF16, AD10, AF15, AF14, AE11, AE10, AD12,Y6, AD14, Y4, AA14, AA16, AC14, Y1, AA7	SD[15:0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
AE8	IOCHRDY	I/O	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
AB8	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AA3, AA1, AB2, AD2,AA2, AD3, AB7, AE5, AC7, AD6, AC2, AE13, AB11, AA12, AB13 AF12, AC3	SA[16:0]	I/O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AA9, AD5, AB9	SA[19:17]	I/O	**ISA slot address bus.** ISA slot address bus for 62-pin slot.
AC13	SBHE_	I/O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
AC15, AD13, AE14, AA15, AD15, AB15, AE9	LA[23:17]	I/O	**ISA latched address bus**. These are input signal during ISA master cycle.
AF9	MEMR_	I/O	**ISA memory read**. This signal is an input during ISA master cycle.
AE12	MEMW_	I/O	**ISA memory write**. This signal is an input during ISA master cycle.
AB1	RST_DRV	O	**Driver Reset**. This output signal is driven active during system power up.
AF4, AF2, AC8, AF3, AE6, AB14, AE7, AC1, AD7, AD1, AE2	IRQ[15:14], IRQ[12:9], IRQ[7:3]	I	**Interrupt request signals**. These are interrupt request input signals.
AE15, AF11, AA11, Y5, AC9, AD4, AB12	DRQ[7:5], DRQ[3:0]	I	**DMA device request**. These are DMA request input signals.
AD8	0WS_	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
AA10	SMEMR_	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
AA8	SMEMW_	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.

PIN No.	Symbol	Type	Description
Y2	IOW_	O	**ISA I/O write**. This signal is an input during ISA master cycle.
AB16	IOR_	O	**ISA I/O read**. This signal is an input during ISA master cycle.
AF7, AD11, AB10, Y3, AF13, AB3, AD9	DACK_[7:5], DACK_[3:0]	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
AF6	REFRESH_	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AF10	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
AF5	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
AE4	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
AE1	MEMCS16_	I/O	ISA 16-bit memory device select indicator signal.
AE3	IOCS16_	I/O	ISA 16-bit I/O device select indicator signal.
AF8	OSC14M	O	14.318MHz clock out

- **Chip Selection Interface (3 PINs)**

PIN No.	Symbol	Type	Description
AC16	GPCS0_	O	**ISA Bus Chip Select 0**. This pin is the chip select for ISA bus.
AD16	GPCS1_	O	**ISA Bus Chip Select 1**. This pin is the chip select for ISA bus.
G21	ROM_CS_	O	***ROM Chip Select.*** This pin is used as a ROM chip select.
	SPICS_	O	***SPI Chip Select.*** This pin is used as SPI flash chip select.
	Strap_BMS	I	***Boot Mode Select*** Pull it high to select Normal boot(Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.

- **Redundant (4 PIN)**

PIN No.	Symbol	Type	Description
U21	EXTSYSFAILIN_	I	**External system fail input**. This pin is the system fail in for redundant.
U22	SYSFAILOUT_	O	**System fail output**. This pin is the system fail out for redundant.
V22	EXT_SWITCH_FAIL_	I	**External switch fail**. This pin is the switch input for redundant.
V21	EXT_GPCS_	I	**External GPCS input**. This pin is the GPCS in for redundant.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
V13	KBCLK	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042.
	KBRST	I	**Keyboard Reset**. This pin is Keyboard reset when used external 8042.
V16	KBDAT	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042.

	A20GATE	I	**Address Bit 20 Mask**. This pin is A20 mask when used external 8042.
V14	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
V15	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

- **RTC/GPIO PORT3[7-4]/8051 GPIO PORT3[7-4]/I2C Interface (7 PINs)**

PIN No.	Symbol	Type	Description
N21	RTC_AS	O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC.
	GPIO_37	I/O	***General-Purpose Input/Output Port 3 bit 7.***
	8051_GPIO_37	I/O	***8051 General-Purpose Input/Output Port 3 bit 7.***
	I2C1_SDA	I/O	***I2C1 Serial Data.***
P22	RTC_RD_	O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC.
	GPIO_36	I/O	***General-Purpose Input/Output Port 3 bit 6.***
	8051_GPIO_36	I/O	***8051 General-Purpose Input/Output Port 3 bit 6.***
	I2C1_SCL	I/O	***I2C1 Serial Clock.***
T21	RTC_WR_	O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC.
	GPIO_35	I/O	***General-Purpose Input/Output Port 3 bit 5.***
	8051_GPIO_35	I/O	***8051 General-Purpose Input/Output Port 3 bit 5.***
	I2C0_SDA	I/O	***I2C0 Serial Data.***
R22	RTC_IRQ8_	I	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input.
	GPIO_34	I/O	***General-Purpose Input/Output Port 3 bit 4.***
	8051_GPIO_34	I/O	***8051 General-Purpose Input/Output Port 3 bit 4.***
	I2C0_SCL	I/O	***I2C0 Serial Clock.***
T22	RTC_PS	I	***RTC Battery Power Sense.***
V25	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
V26	RTC_XIN	I	***Crystal-in.*** 32.768KHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).

- **COM1/PORT4 Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AE21	SIN1	I	***Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_44	I/O	***General-Purpose Input/Output Port 4 bit 4.***

PIN No.	Symbol	Type	Description
	SERVO28	O	***SERVO28.***
AE22	SOUT1	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_41	I/O	***General-Purpose Input/Output Port 4 bit 1.***
	SERVO25	O	***SERVO25.***
AF22	RTS1_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_42	I/O	***General-Purpose Input/Output Port 4 bit 2.***
	SERVO26	O	***SERVO26.***
AE23	CTS1_	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS1_ signal by reading bit 4 of Modem Status Register (MSR). A CTS1_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1_ changes the state. The CTS1_ signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS1_.*
	GPIO_47	I/O	***General-Purpose Input/Output Port 4 bit 7.***
	SERVO31	O	***SERVO31.***
AF23	DSR1_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR1_ signal by reading bit5 of the Modem Status Register (MSR). A DSR1_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1_ changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR1_.*
	GPIO_46	I/O	***General-Purpose Input/Output Port 4 bit 6.***
	SERVO30	O	***SERVO30.***
AF24	DCD1_	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD1_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD1_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD1_ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD1_.*
	GPIO_40	I/O	***General-Purpose Input/Output Port 4 bit 0.***

PIN No.	Symbol	Type	Description
	SERVO24	O	***SERVO24.***
AD22	RI1_	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI1_ signal by reading bit 6 of the Modem Status Register (MSR). An RI1_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI1_ changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI1_.*
	GPIO_43	I/O	***General-Purpose Input/Output Port 4 bit 3.***
	SERVO27	O	***SERVO27.***
AD23	DTR1_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1_ signal to be inactive during the loop-mode operation.
	GPIO_45	I/O	***General-Purpose Input/Output Port 4 bit 5.***
	SERVO29	O	***SERVO29.***
AD21	TXD_EN1	O	***COM1 TX Status.*** This pin will be high when COM1 is trnamitting.

- **COM2/PWM Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AF25	SIN2	I	***COM2 Receive Data.*** FIFO UART receiver serial data input signal.
	PWM2CLK	I	***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AE24	SOUT2	O	***COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	PWM0OUT	O	***PWM Timer0 Output.*** This pin is PWM timer0 output when SB register C0h bit2 is 1 (PINs for PWM).
AD25	RTS2_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	PWM1OUT	O	***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).

PIN No.	Symbol	Type	Description
AD26	CTS2_	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS2_ signal by reading bit 4 of Modem Status Register (MSR). A CTS2_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS2_ changes the state. The CTS2_ signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS2_.*
	PWM1GATE	I	***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AE26	DSR2_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR2_ signal by reading bit5 of the Modem Status Register (MSR). A DSR2_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR2_ changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR2_.*
	PWM0GATE	I	***PWM Timer0 Gate.*** This pin is PWM timer0 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AC26	DCD2_	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD2_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD2_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD2_ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD2_.*
	PWM0CLK	I	***PWM Timer0 Clock.*** This pin is PWM timer0 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AD24	RI2_	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_.*
	PWM1CLK	I	***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when SB register C0h bit2 is 1 (PINs for PWM).

PIN No.	Symbol	Type	Description
AC25	DTR2_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation.
	PWM2OUT	O	***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AE25	TXD_EN2	O	***COM2 TX Status.*** This pin will be high when COM2 is trnamitting.
	PWM2GATE	I	***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

- **COM3, 4, 9 (6 PIN)**

PIN No.	Symbol	Type	Description
G3	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
G2	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
N6	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
M6	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
K6	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
J6	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

- **Primary IDE/SD Interface (29 PINs)**

PIN No.	Symbol	Type	Description
M1	PRST_	O	***IDE Primary Channel Reset.***
T3	PDD0	I/O	***IDE Primary Channel Data Bus Data 0.***
	SD0_DATA2	I/O	***SD0 Data Bus Data 2.***
T5	PDD1	I/O	***IDE Primary Channel Data Bus Data 1.***
	SD0_DATA3	I/O	***SD0 Data Bus Data 3.***
R5	PDD2	I/O	***IDE Primary Channel Data Bus Data 2.***
	SD0_CMD	I/O	***SD0 Command/Response.***
N1	PDD3	I/O	***IDE Primary Channel Data Bus Data 3.***
	SD0_CLK	O	***SD0 Clock.***
U2	PDD4	I/O	***IDE Primary Channel Data Bus Data 4.***
	SD0_DATA0	I/O	***SD0 Data Bus Data 0.***
R4	PDD5	I/O	***IDE Primary Channel Data Bus Data 5.***
	SD0_DATA1	I/O	***SD0 Data Bus Data 1.***
T4	PDD6	I/O	***IDE Primary Channel Data Bus Data 6.***
	SD0_CD	I	***SD0 Card Detect.***

PIN No.	Symbol	Type	Description
U4	PDD7	I/O	***IDE Primary Channel Data Bus Data 7.***
	SD0_WP	I	***SD0 Write Protect.***
U3	PDD8	I/O	***IDE Primary Channel Data Bus Data 8.***
	SD1_DATA2	I/O	***SD1 Data Bus Data 2.***
N3	PDD9	I/O	***IDE Primary Channel Data Bus Data 9.***
	SD1_DATA3	I/O	***SD1 Data Bus Data 3.***
P4	PDD10	I/O	***IDE Primary Channel Data Bus Data 10.***
	SD1_CMD	I/O	***SD1 Command/Response.***
U5	PDD11	I/O	***IDE Primary Channel Data Bus Data 11.***
	SD1_CLK	O	***SD1 Clock.***
P5	PDD12	I/O	***IDE Primary Channel Data Bus Data 12.***
	SD1_DATA0	I/O	***SD1 Data Bus Data 0.***
P1	PDD13	I/O	***IDE Primary Channel Data Bus Data 13.***
	SD1_DATA1	I/O	***SD1 Data Bus Data 1.***
W2	PDD14	I/O	***IDE Primary Channel Data Bus Data 14.***
	SD1_CD	I	***SD1 Card Detect.***
V2	PDD15	I/O	***IDE Primary Channel Data Bus Data 15.***
	SD1_WP	I	***SD1 Write Protect.***
R1	PDRQ	I	***IDE Primary Channel DMA Request.***
R3	PIOW_	O	***IDE Primary Channel IO Write Strobe.***
V1	PIOR_	O	***IDE Primary Channel IO Read Strobe.***
P3	PIORDY	I	***IDE Primary Channel IO Channel Ready.***
T1	PDACK_	O	***IDE Primary Channel DMA Acknowledge.***
N2	PINT	I	***IDE Primary Channel Interrupt.***
K1, P2, R2	PA[2:0]	O	***IDE Primary Channel Device Address***
U1	PCBLID_	I	***IDE Primary Channel Cable Assembly Type Identifier.***
W1	PCS1_	O	***IDE Primary Channel Chip Select.***
T2	PCS0_	O	***IDE Primary Channel Chip Select.***

- **Secondary IDE /COM3,4,PRINT1 Interface (29 PINs)**

PIN No.	Symbol	Type	Description
K4, K5, L5, M4, K3, M2, L2, K2	PD[7:0]	I/O	***Parallel port data bus bit .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD[7:0]	I/O	***IDE Secondary Channel Data Bus.***
N5	SLCT	I	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	SDD8	I/O	***IDE Secondary Channel Data Bus.***

PIN No.	Symbol	Type	Description
L6	PE	I	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD9	I/O	***IDE Secondary Channel Data Bus.***
M5	BUSY	I	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	SDD10	I/O	***IDE Secondary Channel Data Bus.***
L4	ACK_	I	***ACK_.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD11	I/O	***IDE Secondary Channel Data Bus.***
M3	SLIN_	OD	***SLIN_.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD12	I/O	***IDE Secondary Channel Data Bus.***
J1	INIT_	OD	***INIT_.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD13	I/O	***IDE Secondary Channel Data Bus.***
N4	ERR_	I	***ERR_.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD14	I/O	***IDE Secondary Channel Data Bus.***
L3	AFD_	OD	***AFD_.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SDD15	I/O	***IDE Secondary Channel Data Bus.***
H3	RTS3_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	SRST_	O	***IDE Secondary Channel Reset.***

PIN No.	Symbol	Type	Description
J2	DCD3_	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD3_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD3_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD3_ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD3_.*
	SDRQ	I	***IDE Secondary Channel DMA Request.***
P6	CTS4_	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The CTS_ signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_.*
	SIOW_	O	***IDE Secondary Channel IO Write Strobe.***
H2	CTS3_	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The CTS_ signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS_.*
	SIOR_	O	***IDE Secondary Channel IO Read Strobe.***
G1	RI3_	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_.*
	SIORDY	I	***IDE Secondary Channel IO Channel Ready.***
F1	DTR3_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation.

PIN No.	Symbol	Type	Description
	SDACK_	O	***IDE Secondary Channel DMA Acknowledge.***
U6	RTS4_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	SINT	I	***IDE Secondary Channel Interrupt.***
V5	RI4_	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI_.*
	SA1	O	***IDE Secondary Channel Device Address.***
H1	DSR3_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_.*
	SCBLID_	I	***IDE Secondary Channel Cable Assembly Type Identifier.***
V6	DTR4_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation.
	SA0	O	***IDE Secondary Channel Device Address.***
R6	DCD4_	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD4_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD4_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD4_ changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD4_.*

PIN No.	Symbol	Type	Description
	SA2	O	***IDE Secondary Channel Device Address.***
L1	STB_	OD	***STB_.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SCS0_	O	***IDE Secondary Channel Chip Select.***
T6	DSR4_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR_.*
	SCS1_	O	***IDE Secondary Channel Chip Select.***

- **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
W24	SERIRQ	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture.
W23, V23, U23, T23	LAD[3:0]	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function.
U18	LFRAME_	O	***Low Pin Count FRAME_ Signal.*** This signal is used as a frame signal of low pin count protocol..
V18	LDRQ_	I	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol.

- **GPIO Interface (24 PINs)**

PIN No.	Symbol	Type	Description
AA18, AA17, AE18, AE17, AF18, AF17, AC17, AD17,	GPIO_0[7:0]	I/O	***General-Purpose Input/Output Port 0[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_0[7:0]	I/O	***8051 General-Purpose Input/Output Port 0[7:0].***
	SERVO[7:0]	O	***SERVO[7:0].***
AA19, AC19, AD19, AE19, AB18, AC18, AB17, AF19	GPIO_1[7:0]	I/O	***General-Purpose Input/Output Port 1[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_1[7:0]	I/O	***8051 General-Purpose Input/Output Port 1[7:0].***
	SERVO[15:8]	O	***SERVO[15:8].***
AA20, AB20, AD20, AE20, AD18, AF20,	GPIO_2[7:0]	I/O	***General-Purpose Input/Output Port 2[7:0] .*** Those pins can be programmed input or output individually.

AF21, AB19	8051_GPIO_2[7:0]	I/O	***8051 General-Purpose Input/Output Port 2[7:0].***
	SERVO[23:16]	O	***SERVO[23:16].***
	SA[31:24]	O	***ISA Address[31:24].***

- **Ethernet Interface (24 PINs)**

PIN No.	Symbol	Type	Description
L22	LINK/ACTIVE	O	***LINK/ACTIVE:*** Link/active status
K22	DUPLEX	O	***DUPLEX:*** Duplex status
J24	ISET	I	***ISET:*** External resistor connecting pin for BIAS
F22	ATSTP	I/O	***ATSTP:*** VGA and ADC testing pin for input and output (positive)
F21	ATSTN	I/O	***ATSTN:*** VGA and ADC testing pin for input and output (negative)
K25	TXN	O	***TXN:*** 10B-T/100BT transmitting output pin/ reveiving input pin (positive)
K26	TXP	O	***TXP:*** 10B-T/100BT transmitting output pin/ reveiving input pin (negative)
L25	RXN	I	***RXN:*** 10B-T/100BT reveiving input pin/ transmitting output pin (positive)
L26	RXP	I	***RXP:*** 10B-T/100BT reveiving input pin/ transmitting output pin (negative)
J16	MDC	O	***MDC:*** MII management data clock is sourced by the Vortex86DX to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
K16	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and the Vortex86DX.
L16	COL0	I	***COL0:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
M21	RXC0	I	***RXC0:*** Supports the receive clock supplied by the external PMD device. This clock should always be active.
M18, M17, L17, L18	RXD0[3:0]	I	***RXD0[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
L21	RXDV0	I	***RXDV0:*** Data valid is asserted by an external PHY when the received data is present on the RXD0[3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
J21	TXC0	I	***TXC0:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
J18, J17, K17, K18	TXD0[3:0]	O	***TXD0[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
K21	TXEN0	O	***TXEN0:*** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.

- **USB Device (2 PINs)**

PIN No.	Symbol	Type	Description
D1 E1	UD_DP UD_DM	I/O	***Universal Serial Bus Device Controller Port.*** These are the serial data pair for USB Device. Need add 1.5kΩ pull up resistors to UD_DP externally.

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
G6	TDO	O	***TDO:*** JTAG Test Data Output pin.
J9	TMS	I	***TMS:*** JTAG Test Mode Select pin.
G7	TCK	I	***TCK:*** JTAG Test Clock Input pin.
H6	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **TEST PIN (9 PIN)**

PIN No.	Symbol	Type	Description
E23, E21, D22, E22, D23, F2, F3, E2, E3	TEST[8:0]	I/O	For Testing used. Test 3 and Test 4 must pull high to 3.3V.

- **1V POWER (10 PINs)**

PIN No.	Symbol	Type	Description
F8,F13,F14,G4,J14, K14,L14,N9,M14,P9	VCCK (10 PINs)	I	Core power

- **1.8V POWER (32 PINs)**

PIN No.	Symbol	Type	Description
C4,C5,C6,C7, D4,D7,D8,E4	VCCO (8 PINs)	I	DDRII Power
AA21,AA22, AA23,AC4, AC5,AC6,T11, T12,U10,V10	Vdd_core (10 PINs)	I	SB Core power
R23, W26, N22, R24	AVDD [3:0]	I	Analog Power USB 1.8 V Power
T24, W25, N24, P23	AVSS [3:0]	I	Analog ground USB 1.8 V ground
U25, P25	AVSSPLL [1:0]	I	USB PLL Ground
V24,N23	AVDDPLL [1:0]	I	USB PLL Power
J5, H5	GNDPLL1, GNDPLL0	I	Analog ground CPU PLL Ground

- **Battery POWER (2 PIN)**

PIN No.	Symbol	Type	Description
P21	VBat	I	Battery power for RTC
R21	VBatGnd	I	Battery ground for RTC

- **3.3V Power (81 PINs)**

PIN No.	Symbol	Type	Description
AB24	Vdd_pll	I	Analog power SB PLL Power
AC24	Vss_pll	I	Analog ground SB PLL Ground
E18, F18, J15, K15, L15, M15, M16, P10, P11, P12, P13, P14	VCC3V (12 PINs)	I	Analog power CPU I / O PAD Power
AA4, AA5, AA6, AC21, AC22, AC23, N17, N18, P15, P16, R9, R10, R13, R14, V3, W3, W4, F23	Vdd_io (18 PINs)	I	I/O power SB I/O PAD Power
K23	VSSAPLL	I	Analog Ground, E-PHY PLL
J23	VCCAPLL	I	Analog power, E-PHY PLL
M22	VSSABG	I	Analog ground, E-PHY BandGap
M23	VCCABG	I	Analog power, E-PHY BandGap
K24	VCCA0	I	Analog power, E-PHY
L23	VSSA0	I	Analog ground, E-PHY
L24	VCCA1	I	Analog power, E-PHY
M24	VSSA1	I	Analog ground, E-PHY
U24	AVDD33_1	I	USB Analog power
P24	AVDD33_0	I	USB Analog power

- **Digital Ground (83 PIN)**

PIN No.	Symbol	Type	Description
D21, P17, P18, R11, R12, R15, R16, R17, R18, T9, T10, T13, T14, T15, U9, U17, V9, V17, W5, W6, AB21, AB22, AB23, AC20, F15, F16, F17, J13,	VSS	I	Digital Ground

K13, L13, M12, M13, N10, N11, N12, N13, N14, N15, N16, T16, T17, T18, U11, U12, U13, U14, U15, U16, V4, V11, V12, AB4, AB5, AB6, AC10, AC11, AC12, D5, D6, E5, E6, F4, F5, F6, F7, G5, E7, E8, E17, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11			

3.5. PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance				pF
C_{OUT}	3.3V Output Capacitance				pF
C_{BID}	3.3V Bi-directional Capacitance				pF

3.6. PIN Pull-up / Pull-down Description

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
DCD1_/GPIO_40	I/O	Note18	Note1	--	--	Y	S	
SOUT1/GPIO_41	I/O	Note18	Note1	--	--	Y	S	
RTS1_/GPIO_42	I/O	Note18	Note1	--	--	Y	S	
RI1_/GPIO_43	I/O	Note18	Note1	--	--	Y	S	
SIN1/GPIO_44	I/O	Note18	Note1	--	--	Y	S	
DTR1_GPIO_45	I/O	Note18	Note1	--	--	Y	S	
DSR1_/GPIO_46	I/O	Note18	Note1	--	--	Y	S	
CTS1_/GPIO_47	I/O	Note18	Note1	--	--	Y	S	
TXD_EN1	O	8mA	--	--	--	--	S	
DCD2_/CLK0	I	--	--	--	Note2	Y	--	
SOUT2/OUT0	O	8mA	--	--	--	--	S	
RTS2_/OUT1	O	8mA	--	--	--	--	S	
RI2_/CLK1	I	--	--	--	Note2	Y	--	
SIN2/CLK2	I	--	--	--	Note2	Y	--	
DTR2_/OUT2	O	8mA	--	--	--	--	S	
DSR2_/GATE0	I	--	--	--	--	Y	--	
CTS2_/GATE1	I	--	--	--	--	Y	--	
TXD_EN2/GATE2	I/O	8mA	--	--	--	Y	S	
DCD3_/SDRQ	I	--	Note24	Note24	--	Y	--	
SOUT3	O	8mA	--	--	--	--	S	
RTS3_/SRST_	O	Note3	--	--	--	--	Note8	
RI3_/SIORDY	I	--	Note25	Note25	--	Y	--	
SIN3	I	--	--	--	--	Y	--	
DTR3_/SDACK_	O	Note3	--	--	--	--	Note8	
DSR3_/SCBLID_	I	--	Note25	Note25	--	Y	--	
CTS3_/SIOR_	I/O	Note4	Y	--	--	Y	F	
DCD4_/SA2	I/O	Note4	--	--	--	Y	F	
SOUT4	O	8mA	--	--	--	--	S	
RTS4_/SINT	I/O	8mA	Note26	Note26	--	Y	S	
RI4_/SA1	I/O	Note4	--	--	--	Y	F	
SIN4	I	--	--	--	--	Y	--	
DTR4_/SA0	O	Note3	--	--	--	0	Note8	
DSR4_/SCS_1	I/O	Note4	--	--	--	Y	F	
CTS4_/SIOW_	I/O	Note4	Y	--	--	Y	F	
STB_/SCS_0	O Note7	Note5	--	--	--	--	Note8	
AFD_/SDD15	I/O	Note5	--	Note23	--	Y	Note8	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
	Note7							
ERR_/SDD14	I/O	Note4	Note24	Note24	Note6	Y	F	
INIT_/SDD13	I/O Note7	Note5	--	Note23	--	Y	Note8	
SLIN_/SDD12	I/O Note7	Note5	--	Note23	--	Y	Note8	
ACK_/SDD11	I/O	Note4	Note24	Note24	Note6	Y	F	
BUST/SDD10	I/O	Note4	Note24	Note24	Note6	Y	F	
PE/SDD9	I/O	Note4	Note24	Note24	Note6	Y	F	
SLCT/SDD8	I/O	Note4	Note24	Note24	Note6	Y	F	
PD[7:0]/SDD[7:0]	I/O	Note5	--	Note23	--	Y	Note8	
SOUT9	O	8mA	--	--	--	--	S	
SIN9	I	--	--	--	--	Y	--	
PRST	O	Note11	--	--	--	--	F	
PDD[15:0]	I/O	Note11	Note22	Note22	--	Y	F	
PDRQ	I	--	--	Y	--	Y	--	
PIORDY	I	--	Y	--	--	Y	--	
PDACK_	O	Note11	--	--	--	--	F	
PINT	I	--	--	Y	--	Y	--	
PA[2:0]	O	Note11	--	--	--	--	F	
PCBLID_	I	--	Y	--	--	Y	--	
PCS0	O	Note11	--	--	--	--	F	
PCS1	O	Note11	--	--	--	--	F	
PIOW_	O	Note11	--	--	--	--	F	
PIOR_	O	Note11	--	--	--	--	F	
GPIO_0[7:0]	I/O	Note18	Note1	--	--	Y	S	
GPIO_1[7:0]	I/O	Note18	Note1	--	--	Y	S	
GPIO_20 / SA24	I/O	Note18	Note1	--	--	Y	S	
GPIO_21 / SA25	I/O	Note18	Note1	--	--	Y	S	
GPIO_22 / SA26	I/O	Note18	Note1	--	--	Y	S	
GPIO_23 / SA27	I/O	Note18	Note1	--	--	Y	S	
GPIO_24 / SA28	I/O	Note18	Note1	--	--	Y	S	
GPIO_25 / SA29	I/O	Note18	Note1	--	--	Y	S	
GPIO_26 / SA30	I/O	Note18	Note1	--	--	Y	S	
GPIO_27 / SA31	I/O	Note18	Note1	--	--	Y	S	
GPIO_30/E_SPI_CS	I/O	Note18	Note1	--	--	Y	S	
GPIO_31/E_SPI_CLK	I/O	Note18	Note1	--	--	Y	S	
GPIO_32/E_SPI_DO	I/O	Note18	Note1	--	--	Y	S	
GPIO_33/E_SPI_DI	I/O	Note18	Note1	--	--	Y	S	
GPIO_34 / RTC_IRQ8_	I/O	Note18	Note9	--	--	Y	S	
GPIO_35 / RTC_WR_	I/O	Note18	Note9	--	--	Y	S	
GPIO_36 / RTC_RD_	I/O	Note18	Note9	--	--	Y	S	
GPIO_37 / RTC_AS	I/O	Note18	Note9	--	--	Y	S	
OSC14M	O	Note19	--	--	--	Y	Note19	
ATCLK	O	Note19	Y	--	Y	Y	Note19	
LA[23:17]	I/O	Note19	Y	--	Y	Y	S	
SA[19:0]	I/O	Note19	Y	--	Y	Y	S	
SBHE_	I/O	Note19	Y	--	Y	Y	S	
SD[15:0]	I/O	Note19	Y	--	Y	Y	S	
MEMR_	I/O	Note19	Y	--	Y	Y	S	
MEMW_	I/O	Note19	Y	--	Y	Y	S	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
SMEMR_	O	Note19	Y	--	--	Y	S	
SMEMW_	O	Note19	Y	--	--	Y	S	
IOR_	O	Note19	Y	--	--	Y	S	
IOW_	O	Note19	Y	--	--	Y	S	
TC	O	Note19	--	Y	--	Y	S	
DRQ0	I	--	--	Y	Y	Y	--	
DRQ1	I	--	--	Y	Y	Y	--	
DRQ2	I	--	--	Y	Y	Y	--	
DRQ3	I	--	--	Y	Y	Y	--	
DRQ5	I	--	--	Y	Y	Y	--	
DRQ6	I	--	--	Y	Y	Y	--	
DRQ7	I	--	--	Y	Y	Y	--	
IRQ3	I	--	Y	--	Y	Y	--	
IRQ4	I	--	Y	--	Y	Y	--	
IRQ5	I	--	Y	--	Y	Y	--	
IRQ6	I	--	Y	--	Y	Y	--	
IRQ7	I	--	Y	--	Y	Y	--	
IRQ9	I	--	Y	--	Y	Y	--	
IRQ10	I	--	Y	--	Y	Y	--	
IRQ11	I	--	Y	--	Y	Y	--	
IRQ12	I	--	Y	--	Y	Y	--	
IRQ14	I	--	Y	--	Y	Y	--	
IRQ15	I	--	Y	--	Y	Y	--	
IOCHRDY	I/O	Note19	Y	--	Y	Y	S	
DACK0_	O	Note19	Y	--	--	Y	S	
DACK1_	O	Note19	Y	--	--	Y	S	
DACK2_	O	Note19	Y	--	--	Y	S	
DACK3_	O	Note19	Y	--	--	Y	S	
DACK5_	O	Note19	Y	--	--	Y	S	
DACK6_	O	Note19	Y	--	--	Y	S	
DACK7_	O	Note19	Y	--	--	Y	S	
MEMCS16_	I/O	Note19	Y	--	Y	Y	S	
IOCS16_	I/O	Note19	Y	--	Y	Y	S	
OWS_	I	--	Y	--	Y	Y	--	
AEN	O	Note19	--	Y	--	Y	S	
BALE	O	Note19	--	Y	--	Y	S	
IOCHCK_	I	--	Y	--	Y	Y	--	
REFRESH_	I/O	Note19	Y	--	Y	Y	S	
RESET_DRV	O	Note19	--	Y	--	Y	F	
ExtSysFailIn_	I	--	--	Y	Y	Y	--	
Ext_Switch_fail_	I	--	Y	--	Y	Y	--	
EXT_GPCS_	I	--	Y	--	Y	Y	--	
SYSFAILOut_	O	12mA	--	--	--	--	S	
ROM_CS	O	8mA	--	--	--	--	S	
GPCS0_	O	Note19	Y	--	--	Y	F	
GPCS1_	O	Note19	Y	--	--	Y	F	
KBCLK/KBRST	I/O	16mA	Y	--	Y	Y	S	
KBDAT/A20GATE	I/O	16mA	Y	--	Y	Y	S	
MSCLK	I/O	16mA	Y	--	Y	Y	S	
MSDAT	I/O	16mA	Y	--	Y	Y	S	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
AD[31:0]	I/O	Note20	--	--	--	--	--	Note10
CBE[3:0]	I/O	Note20	Y	--	--	--	--	Note10
PAR	I/O	Note20	Y	--	--	--	--	Note10
STOP_	I/O	Note20	Y	--	--	--	--	Note10
DEVSEL_	I/O	Note20	Y	--	--	--	--	Note10
TRDY_	I/O	Note20	Y	--	--	--	--	Note10
IRDY_	I/O	Note20	Y	--	--	--	--	Note10
FRAME_	I/O	Note20	Y	--	--	--	--	Note10
PCIRST_	O	Note20	--	--	--	--	--	Note10
INTA_	I	--	Y	--	--	--	--	Note10
INTB_	I	--	Y	--	--	--	--	Note10
INTC_	I	--	Y	--	--	--	--	Note10
INTD_	I	--	Y	--	--	--	--	Note10
PCICLK_0	O	Note21	--	--	--	--	--	Note10
PCICLK_1	O	Note21	--	--	--	--	--	Note10
PCICLK_2	O	Note21	--	--	--	--	--	Note10
REQ[2:0]_	I	--	Y	--	--	N	--	Note10
GNT[2:0]_	O	--	--	--	--	--	--	Note10
LAD[3:0]	I/O	Note18	Note12	--	--	--	--	Note10
LFRAME_	O	Note18	Note12	--	--	--	--	Note10
LDRQ_	I	Note18	Note12	--	--	--	--	Note10
SERIRQ	I/O	Note18	Note12	--	--	--	--	Note10
PWRGOOD	I	--	--	--	Y	Y	--	
25MOut	O	Note19	--	--	--	--	Note19	
24MOUT	O	Note19	--	--	--	--	Note19	
XOUT_14318	O	--	--	--	--	--	--	
XIN_14318	I	--	--	--	--	--	--	
MTBF_	O	8mA	--	--	--	--	F	
SPEAKER	O	8mA	--	--	--	--	S	
RTC_Xout	O	--	--	--	--	--	--	
RTC_Xin	I	--	--	--	--	--	--	
RTC_PS	I	--	--	--	--	--	--	
USB0_DP	I/O	--	--	Note21	--	--	--	Note13
USB0_DM	I/O	--	--	Note21	--	--	--	Note13
USB1_DP	I/O	--	--	Note21	--	--	--	Note13
USB1_DM	I/O	--	--	Note21	--	--	--	Note13
USB2_DP	I/O	--	--	Note21	--	--	--	Note13
USB2_DM	I/O	--	--	Note21	--	--	--	Note13
USB3_DM	I/O	--	--	Note21	--	--	--	Note13
USB3_DP	I/O	--	--	Note21	--	--	--	Note13
pdp	I/O	Note17	--	--	Note17	Y	Note17	
pdm	I/O	Note17	--	--	Note17	Y	Note17	
REXT0	I/O	--	--	--	--	--	--	Note13
REXT1	I/O	--	--	--	--	--	--	Note13
Link/Active	O	8mA	--	--	--	--	S	
DUPLEX	O	8mA	--	--	--	--	S	
ISET	O	--	--	--	--	--	--	Note14
ATSTP	I/O	--	--	--	--	--	--	Note15
ATSTN	I/O	--	--	--	--	--	--	Note15

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
TXN	I/O	--	--	--	--	--	--	Note16
TXP	I/O	--	--	--	--	--	--	Note16
RXN	I/O	--	--	--	--	--	--	Note16
RXP	I/O	--	--	--	--	--	--	Note16
MDC	I	--	--	--	Y	Y	--	
MDIO	I/O	8mA	--	--	--	Y	S	
COL0	O	8mA	--	--	--	--	S	
RXC0	O	8mA	--	--	--	--	F	
RXDV0	O	8mA	--	--	--	--	S	
TXC0	O	8mA	--	--	--	--	F	
TXEN0	I	--	--	--	--	Y	--	
RXD0[3:0]	O	8mA	--	--	--	--	S	
TXD0[3:0]	I	--	--	--	--	Y	--	
SDRAMCLKP	O	--	--	--	--	--	--	
SDRAMCLKN	O	--	--	--	--	--	--	
CS_[1:0]	O	--	--	--	--	--	--	
RAS_	O	--	--	--	--	--	--	
CAS_	O	--	--	--	--	--	--	
WE_	O	--	--	--	--	--	--	
MA0	I/O	--	--	--	--	--	--	
MA1	I/O	--	--	--	--	--	--	
MA2	I/O	--	--	--	--	--	--	
MA3	I/O	--	--	--	--	--	--	
MA4	I/O	--	--	--	--	--	--	
MA5	I/O	--	--	--	--	--	--	
MA6	I/O	--	--	--	--	--	--	
MA7	I/O	--	--	--	--	--	--	
MA8	I/O	--	--	--	--	--	--	
MA9	I/O	--	--	--	--	--	--	
MA10	I/O	--	--	--	--	--	--	
MA11	I/O	--	--	--	--	--	--	
MA12	I/O	--	--	--	--	--	--	
MA13	I/O	--	--	--	--	--	--	
MA14	I/O	--	--	--	--	--	--	
BA0	I/O	--	--	--	--	--	--	
BA1	I/O	--	--	--	--	--	--	
BA2	I/O	--	--	--	--	--	--	
MD[7:0]	I/O	--	--	--	--	--	--	
MD[15:8]	I/O	--	--	--	--	--	--	
DQM0	O	--	--	--	--	--	--	
DQM1	O	--	--	--	--	--	--	
DQS[1:0]	I/O	--	--	--	--	--	--	
ODT[1:0]	I/O	--	--	--	--	--	--	
CKE	O	--	--	--	--	--	--	
TDO	O	6mA	--	--	Y	N	S	
TMS	I	6mA	Y	--	Y	N	S	
TCK	I	6mA	Y	--	Y	N	S	
TDI	I	6mA	Y	--	Y	N	S	

4. System Address Map

The Vortex86DX microprocessor supports 4 Gbytes of addressable memory space and 64 Kbytes of addressable I/O space. In order to be compatible with PC/AT system, the lower 1 Mbytes of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only.

4.1. Memory Address Ranges

Figure 4-1 represents Vortex86DX mircoprocessor memory address map. It shows the main memory regions defined and supported by the Vortex86DX. At the highest level, the address space is divided into two main conceptual regions. One is the 0–1-Mbyte DOS compatibility region and the other is 1-Mbyte to 4-Gbyte extended memory region. The Vortex86DX processor supports several main memory sizes from 2MB to 256MB. The main memroy type and size in the system will be auto-detected by the system BIOS.

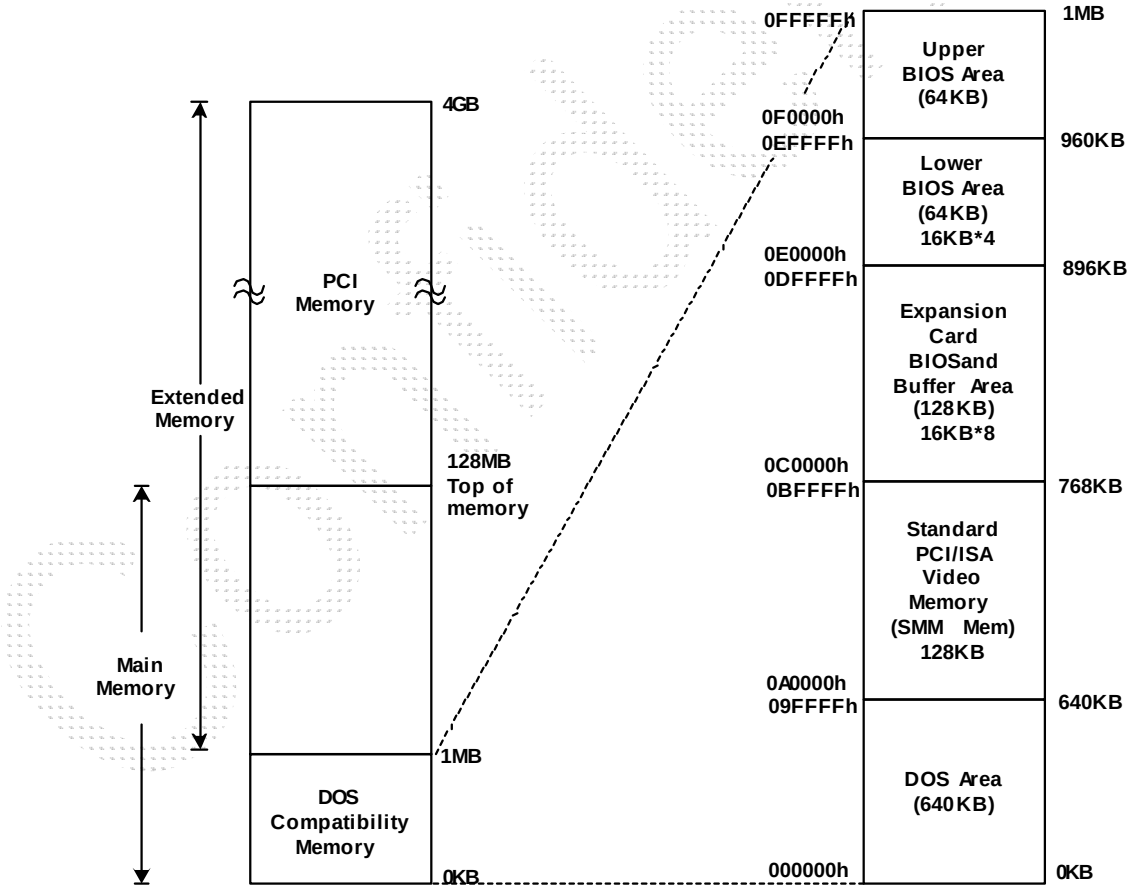


Figure 4-1. Memory Address Map

5. Functional Description

The core of the Vortex86DX 32-bit microprocessor is an x86-like, 6-stage pipeline CPU core. In addition, the Vortex86DX includes a DDRII controller, PCI bus controller, AT/PC compatible peripheral (DMA controller, Interrupt controller and Timer), LPC Controller, X-bus interface and UART. The Vortex86DX is a highly integrated SOC that is suitable for embedded system. With the inherent high performance of CPU core, the Vortex86DX enables the designers to take the advantage to implement a wide variety of performance intensive applications, such as IP sharing, access point, home gateway, and internet appliance, while still maintains the lowest overall system cost.

The following sections will discuss the sub-function of the Vortex86DX.

5.1. Vortex86DX Processor

The Vortex86DX integrates a high speed and high performance CPU core that is designed on advanced 32-bit, 6-stage pipeline architecture. The CPU core of Vortex86DX implements an MMU (Memory Management Unit) with 32 TLB buffers. With the MMU, the Vortex86DX is compatible with a wide variety of operating systems, including MS Windows, Linux and most popular modern RTOS.

This Vortex86DX processor core contains all the features of the 486SX microprocessor with enhancements to increase its performance. The instruction set includes the complete 486SX microprocessor instruction set along with extensions to serve new applications.

Bus Unit

The bus unit manages data transfers, instruction prefetches and control functions between the processor's internal units and the Vortex86DX NB. Internally, the bus unit communicates with the cache and the instruction prefetch units through the 32-bit bus. Externally, the bus unit provides the processor with bus functions, including external bus cycles, memory read/write, instruction fetch, cache line fill, etc.,

Prefetch Unit

When the BUS UNIT is not performing bus cycles to execute an instruction, the instruction prefetch unit uses the BUS UNIT to prefetch instructions. By reading instructions before they are needed, the processor rarely needs to wait for an instruction prefetch cycle on the processor bus.

Instruction prefetch cycles read 16-byte blocks of instructions, starting at addresses numerically greater than the last-fetched instruction. The prefetch unit, which has a direct connection to the paging unit, generates the starting address. The 16-byte prefetched blocks are read into both the prefetch and cache units simultaneously. The prefetch queue in the prefetch unit stores 32 bytes of instructions. As each instruction is fetched from the queue, the code part is sent to the instruction decode unit and (depending on the instruction) the displacement part is sent to the segmentation unit, where it is used for address calculation. If loops are encountered in the program being executed, the prefetch unit gets copies of previously executed instructions from the cache.

Decode Unit

The instruction decode unit receives instructions from the instruction prefetch unit and translates them in a two-stage process into low-level control signals and microcode entry points, as shown in Figure 10-.1. Most instructions can be decoded at a rate of one per clock.

The decode unit simultaneously processes instruction prefix bytes, opcodes, modR/M bytes, and displacements. The outputs include hardwired microinstructions to the segmentation, and integer units. The instruction decode unit is flushed whenever the instruction prefetch unit is flushed.

Memory Management Unit

The on-chip memory management unit (MMU) is completely compatible with the X86 microprocessor.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatability and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4 Kbytes segments. To implement a virtual memory system, full restartability for all page and segment faults is supported.

Memory is organized into one or more variable length segments, each up to four gigabytes (2^{32} bytes) in size. A segment can have attributes associated with it, which include its location, size, type (i.e., stack, code or data), and protection characteristics. Each task can have a maximum of 16,381 segments, each up to four gigabytes in size. Thus each task has a maximum of 64 terabytes (trillion bytes) of virtual memory.

5.2. L1 Cache

In order to maximize the performance, the Vortex86DX integrated a direct map, 16Kbyte code and 16Kbyte data cache in it. The level 1 cache supports write through policy. The on-chip L1 cache allows frequently used data and code to be stored on chip reducing accesses to the external bus. It significantly reduces the penalty of performance to access these codes and data from external slower memory devices.

5.3. L2 Cache

In order to maximize the performance, the Vortex86DX also integrated a direct map, 256Kbytes cache in it. The level 2 cache supports write through policy. The on-chip L2 cache allows frequently used data and code to be stored on chip reducing accesses to the memory. It significantly reduces the penalty of performance to access these codes and data from external slower memory devices.

5.4. DDR2 Controller

The Vortex86DX integrates a main memory DDR2 controller that supports a 16-bit DDR2 data bus width. The Vortex86DX DDR2 interface runs up to 667MHz. All of DDR2 SDRAM configurations provided by Vortex86DX are listed as below:

- **DDR2 16-bit data width:**

One Bank		
Memory Size	DDR2 SDRAM Type	
	x 8	x 16
32MB		16MB x 16 x 1
64MB	32MB x 8 x 2	32MB x 16 x 1
128MB	64MB x 8 x 2	64MB x 16 x 1
256MB	128MB x 8 x 2	128MB x 16 x 1
512MB	256MB x 8 x 2	

Two Banks		
Memory Size	DDR2 SDRAM Type	
	x 8	x 16
64MB		16MB x 16 x 2
128MB	32MB x 8 x 4	32MB x 16 x 2
256MB	64MB x 8 x 4	64MB x 16 x 2
512MB	128MB x 8 x 4	128MB x 16 x 2
1GB	256MB x 8 x 4	

5.5. PCI Bus Controller

In order to leverage the wide availability of low-cost peripherals, as well as to simplify the design off add-in functions, the Vortex86DX integrates a full 32-bit PCI bus interface. Key attributes of the PCI bus include:

- Supports PCI Rev 2.1 specification.
- 32-bit bus interface
- Supports PCI clock at 33 MHz.
- On-chip PCI arbiter
- Supports PCI master/slave

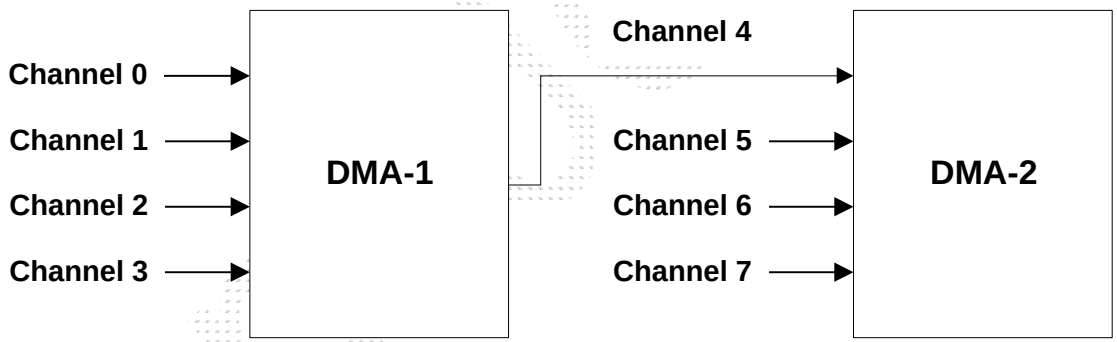
- Up to 133 Mbytes/sec maximum bandwidth
- Supports up to 3 external master devices on PCI
- Provides four PCI interrupt channels

PCI Bus Arbitration

The PCI Bus arbiter for the Vortex86DX allows concurrent host and PCI transactions to main memory. The arbiter supports three external PCI masters in addition to the Vortex86DX. REQ_[2:0]/GNT_[2:0] are used by PCI masters.

5.6. DMA Controller

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Figure 10-4). Master DMA Controller (DMA-1) corresponds to DMA Channels 0–3 and Slave DMA Controller (DMA-2) corresponds to Channels 5–7. DMA Channel 4 is used to cascade the two controllers and will default to cascade mode in the DMA Channel Mode (DCM) Register. This channel is not available for any other purpose. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that are initiated by software. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.



Internal DMA Controller

Each DMA channel is hardwired to the compatible settings for DMA device size: channel 3-0 are hardwired to 8-bit, count-by-bytes transfers, and channel 7-5 are hardwired to 16-bit, count-by-words (address shifted) transfers. The Vortex86DX SB provides the timing control and data size translation necessary for the DMA transfer between the memory (ISA or DRAM) and the ISA Bus IO.

The Vortex86DX SB provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-Compatible Current Register, which holds the 16 least-significant bits of the 24-bit address, an ISA-Compatible Page Register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and auto-initialization following a DMA termination.

The DMA controller is at any time either in master mode or slave mode. In master mode, the DMA controller is either servicing a DMA slave's request for DMA cycles, or allowing a 16-bit ISA master to use the bus via a cascaded DREQ signal. In slave mode, the Vortex86DX SB monitors both the ISA Bus and PCI, decoding and responding to I/O read and write commands that address its registers.

Note that a DMA device (I/O device) is always on the ISA Bus, but the memory referenced is located on either an ISA Bus device or on PCI. When the Vortex86DX SB is running a compatible DMA cycle, it drives the MEMR_ or MEMW_ strobes if the address is less than 16 Mbytes (000000h–FFFFFFh). These memory strobes are generated regardless of whether the cycle is decoded for PCI or ISA memory. The SMEMR_ and SMEMW_ are generated if the address is less than 1 Mbytes (0000000h–00FFFFFh). If the address is greater than 16 Mbytes (1000000h–7FFFFFFh), the MEMR_ or MEMW_ strobe is not generated to avoid aliasing issues.

5.7. Watchdog Timer

The watchdog timer uses 32.768kHz frequency source to count a 24-bit counter so the time range is from 30.5μ sec to 512 sec with resolution 30.5μ sec. When timer times out, a system reset, NMI or IRQ may happen to be decided by BIOS programming.

5.8. Real Time Clock

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the matchbetween the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 5-8 shows a typical PC board layout for isolation of the crystal and oscillator from noise.

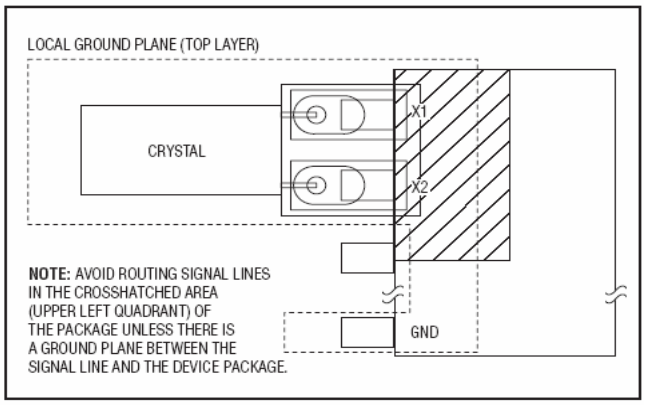


Figure 5-8 Layout Example

5.9. ProgrammableTimer

Vortex86DX SB contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one timer unit, referred to as Timer-1. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker. The 14.31818-MHz counters normally use OSC as a clock source.

5.10. Programmable Interrupt Controller

Vortex86DX SB provides an ISA-Compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers (Figure 5-10). The two controllers are cascaded, providing 13 external and three internal interrupts. The master interrupt controller provides IRQ[7:0] and the slave interrupt controller provides IRQ[15:8]. The three internal interrupts are used for internal functions only. IRQ0 is available to the user only when an external IO APIC is enabled. IRQ2 is used to cascade the two controllers and is not available to the user. IRQ0 is used as a system timer interrupt and is tied to Interval Timer 0, Counter 0. IRQ13 is reserved. The remaining 13 interrupt lines (IRQ[15:14,12:3,1]) are available for external system interrupts. IRQ[1] is fixed to edge trigger mode , IRQ[15:14, 12:3] edge or level sense selections are programmable on an individual channel-by-channel basis.

The Interrupt unit also supports interrupt steering. Vortex86DX SB can be programmed to allow the four PCI active low interrupts (PIRQ[A:D]_) to be internally routed to one of 11 interrupts (IRQ[15:14,12:9,7:3]).

The Interrupt Controller consists of two separate 82C59 cores. Interrupt Controller 1 (CNTRL-1) and Interrupt Controller 2 (CNTRL-2) are initialized separately and can be programmed to operate in different modes. The default settings are: 80x86 Mode, Edge Sensitive (IRQ[0:15]) Detection, Normal EOI, Non-Buffered Mode, Special Fully Nested Mode disabled, and Cascade Mode. CNTRL-1 is connected as the Master Interrupt Controller and CNTRL-2 is connected as the Slave Interrupt Controller.

Note that IRQ13 is generated internally (as part of the coprocessor error support) by Vortex86DX SB. IRQ12/M is generated internally (as part of the mouse support) when bit-4 in the XBCS is set to a 1. When set to a 0, the standard IRQ12 function is provided and IRQ12 appears externally.

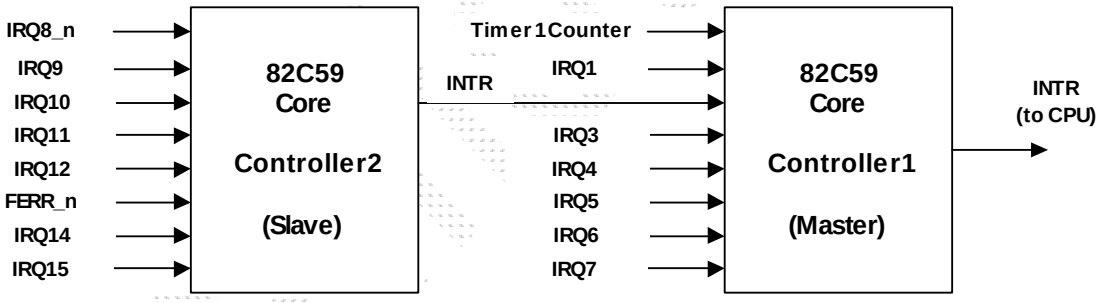


Figure 5-10. Interrupt Controller Block Diagram

5.11. KeyBoard Controller

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter power-down mode by executing two types of power- down instructions. The 8-bit microcontroller has 256 bytes of RAM for data memory and 2 Kbytes of ROM for the program storage.

The ROM codes may come from various vendors (or users), and are programmed during the manufacturing process. To assist in developing ROM codes, the keyboard controller has an external access mode. In the external access mode, the internal ROM is disabled and the instructions executed by the microcontroller come from an externally connected ROM.

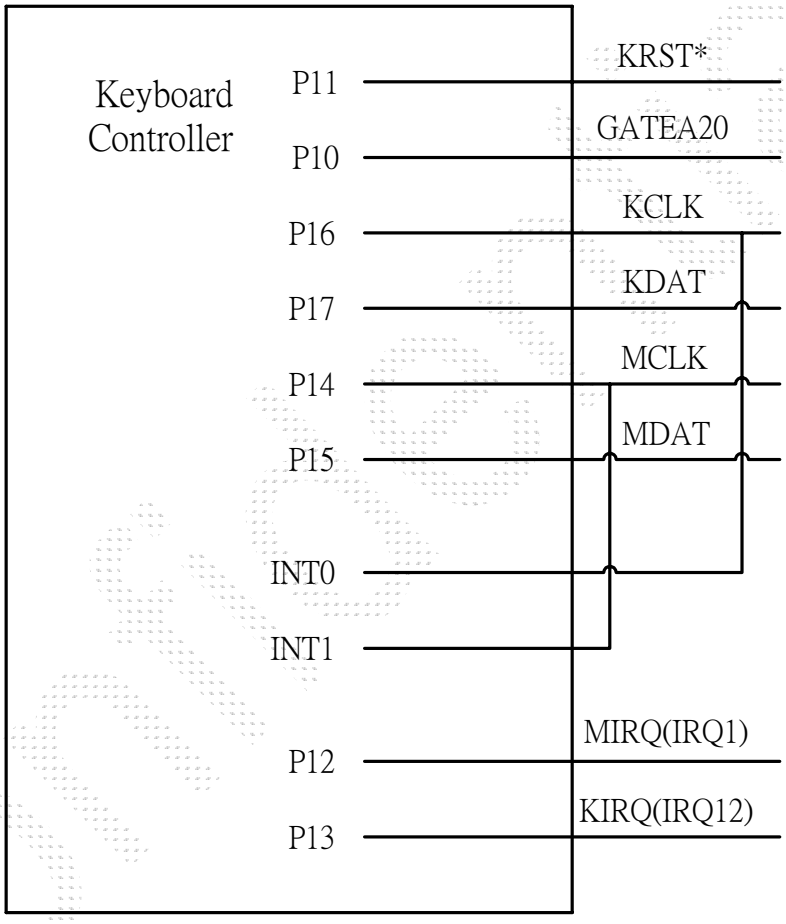


Figure Keyboard and Mouse Interface

5.12. PARALLEL PORT

The Vortex86DX incorporate one XT/AT compatible parallel port. The Vortex86DX support the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities parallel port (ECP) modes. Refer to the Vortex86DX Configuration Registers and Hardware Configuration description for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The address map of the Parallel Port and EPP registers are shown below:

DATA PORT	BASE ADDRESS + 00H	EPP DATA PORT 0	BASE ADDRESS + 04H
STATUS PORT	BASE ADDRESS + 01H	EPP DATA PORT 1	BASE ADDRESS + 05H
CONTROL PORT	BASE ADDRESS + 02H	EPP DATA PORT 2	BASE ADDRESS + 06H
EPP ADDR PORT	BASE ADDRESS + 03H	EPP DATA PORT 3	BASE ADDRESS + 07H

5.13. LPC Interface

The LPC (Low Pin Count) interface enables a system without an ISA bus. It reduces the cost of traditional ISA-bus devices while providing the extension of legacy PC IO peripherals (such as Super IO, keyboard, mouse and Flash ROM), increasing the memory space from 16MB to 4GB to allow the BIOS size to become much bigger than 1MB and the other memory devices to exceed the traditional 16MB capacity. Software is transparent. Do not require special drivers or configuration for this interface. The LPC features are listed as below:

- LPC revision 1.0 compliant
- Supports LPC/FWH (Firmware Hub) compliant interface
- Provides the interface to LPC/FWH Flash ROM or Super IO Chip
- Supports LPC DMA
- Supports Serial IRQ
- Supports bus master mode

5.14. FIFO UART

The Vortex86DX integrates an improved version of Universal Asynchronous Receiver/Transmitter (UART). The internal 16-byte FIFOs are activated and allowed to be stored in both receive and transmit modes. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operations. Reported status information includes the types and conditions of the transfer operations being performed by the FIFO UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

- Programmable word length, stop bit and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Two 16-byte FIFOs

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

5.15. ISA-Bus Interface

The Vortex86DX provides an ISA-bus interface to connect to system boot flash ROM or DOC (Disk On Chip).

- Supports 8-/16-bit data width
- Provides ROMCS_ for boot from ISA-bus Flash ROM
- Supports from 64 Kbytes to Max. 16 Mbytes ROM space addressing

5.16. GPIO Interface

40 GPIO pins are provided by the Vortex86DX for general usage in the system. All GPIO pins are independent and can be configured as inputs or outputs, with or without pull-up/pull-down resistors.

6. USB 2.0 Host Controller

6.1. Features

The USB2.0 Host Controller is a two-port host controller which contains one OHCI host controller compliant with OpenHCI standard and one EHCI host controller compliant with EHCI1.0 specification. Features of the USB2.0 host controller are described as below:

6.1.1. USB1.1 Host Controller

- Supports all full-speed (12MHz) and low-speed (1.5MHz) devices compliant with the "USB Specification" version1.1.
- Supports four transfers: control, bulk, interrupt and isochronous transfers.
- Supports up to 127 devices at the same time.
- Contains one 64-byte FIFO.

6.1.2. USB2.0 Host Controller

- Supports all high-speed (480MHz) devices compliant with the "USB Specification" version2.0.
- Supports four transfers: control, bulk, interrupt and isochronous transfers.
- Supports split transaction for USB2.0 Hub plugged with USB1.1 devices.
- Supports up to 127 devices at the same time.
- Contains one 1K-byte FIFO.

6.2. General Descriptions

The USB 2.0 Host Controller includes one high-speed mode host controller and one USB 1.1 host controller (OHCI). The high-speed host controller implements an EHCI interface. It is used for all high-speed communications to high-speed-mode devices connected to the root ports of the USB 2.0 host controller.The communications to full- and low-speed devices connected to the root ports of the USB 2.0 host controller are provided by the USB 1.1 host controller.

7. Fast Ethernet Control Unit

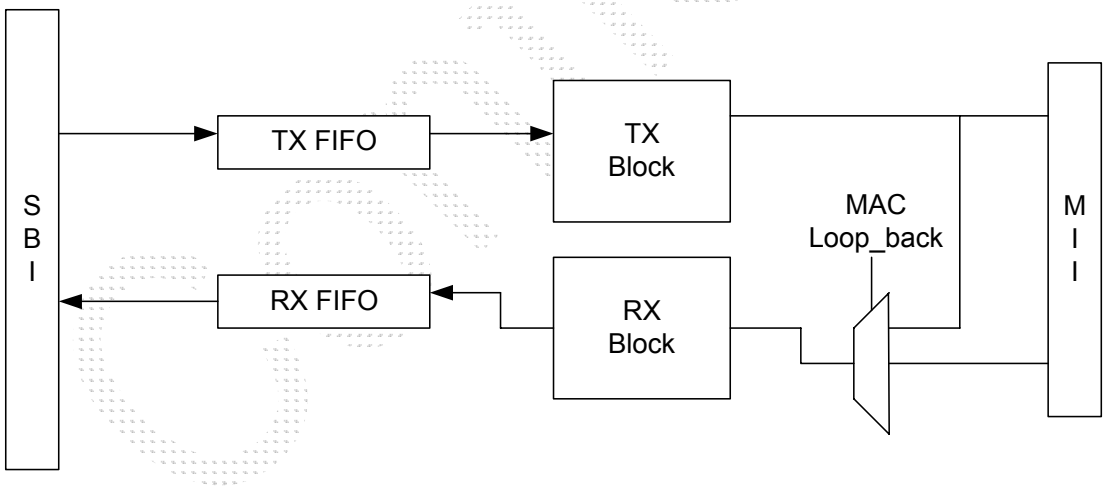
7.1. Overview

The Fast Ethernat Control unit provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Bast-T specifications and IEEE 802.3x Full Duplex Flow Control.

7.2. Features

- Integrated Fast Ethernet MAC and Physical chip
- 10Mbps and 100Mbps operation
- Supports 10Mbps and 100 Mbps N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
- Provides PCI bus master data transfers
- PCI memory space or I/O space mapped data transfer of operational registers
- Supports digital and analog loopback capability
- Half/Full duplex capability
- Support Full Duplex Flow Control which compliance with IEEE 802.3x
- 3.3V power supply

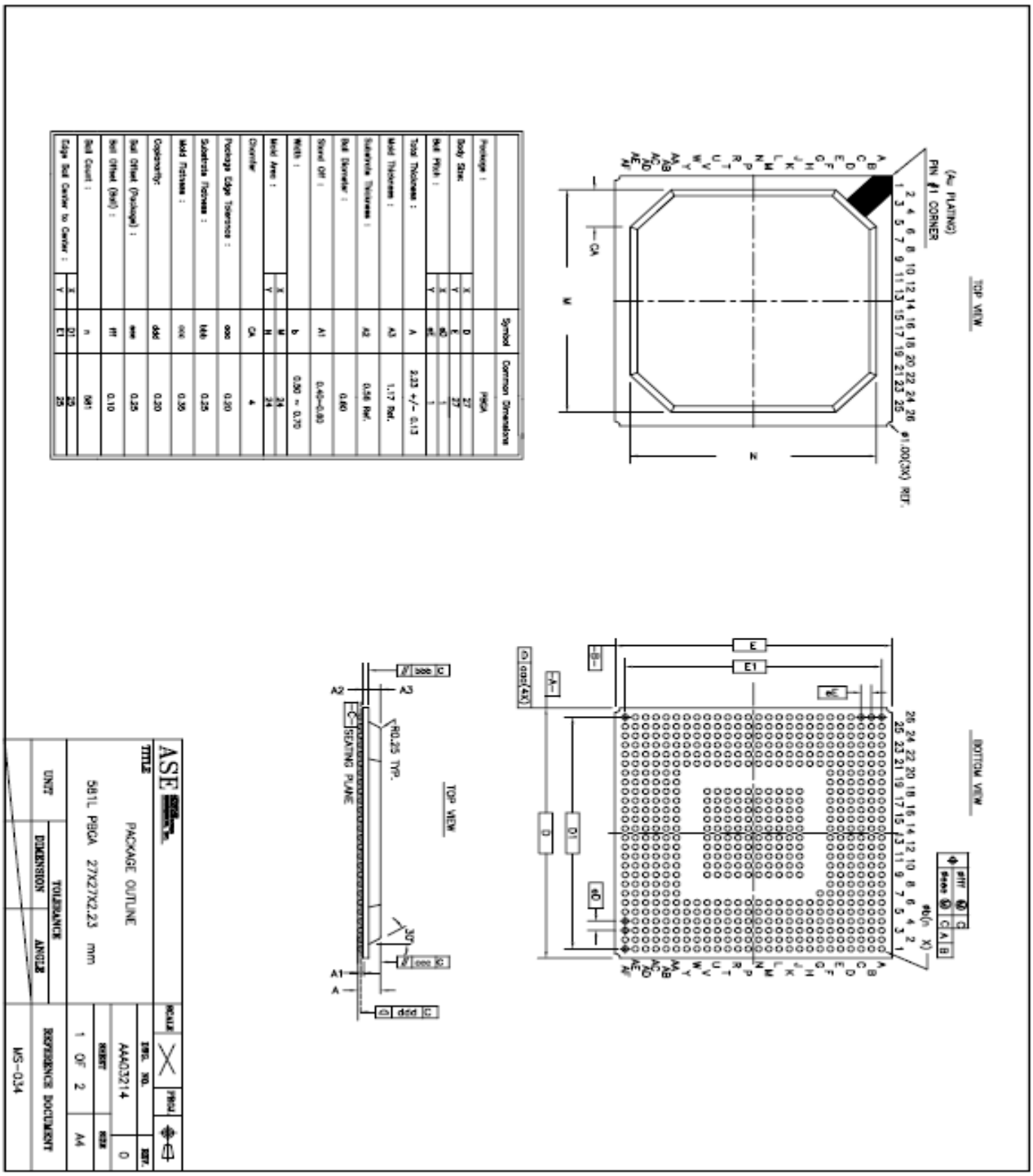
7.3. MAC Block Diagram



SBI : System Bus Interface

MAC Block Diagram

8. Package Information



		Symbol	Common Dimensions
Package :			PBGA
Body Size:	X	D	27
	Y	E	27
Ball Pitch :	X	eD	1
	Y	eE	1
Total Thickness :		A	2.23 +/- 0.13
Mold Thickness :		A3	1.17 Ref.
Substrate Thickness :		A2	0.56 Ref.
Ball Diameter :			0.60
Stand Off :		A1	0.40~0.60
Width :		b	0.50 ~ 0.70
Mold Area :	X	M	24
	Y	N	24
Chamfer		CA	4
Package Edge Tolerance :		aaa	0.20
Substrate Flatness :		bbb	0.25
Mold Flatness :		ccc	0.35
Coplanarity:		ddd	0.20
Ball Offset (Package) :		eee	0.25
Ball Offset (Ball) :		fff	0.10
Ball Count :		n	581
Edge Ball Center to Center :	X	D1	25
	Y	E1	25