Pixel
Semiconductor
A Cirrus Logic Company

CL-PX2070

Preliminary Data Book

APPLICATIONS

- **Presentation**
- **Video Editing**
- **Video Authoring**
- **Video Teleconferencing**
- **Interactive Education Systems**
- **Games**

FEATURES

- ❑ ***Extensive software support available — contact Cirrus Logic Sales office for complete details***
- **Supports up to three simultaneous video data streams**
- **Video scaling**
- **Supports both YCbCr and RGB formats**
- **Interfaces to CODECs, decoders, encoders**
- **Integrated ISA, MCA, and host bus interfaces**

(cont. next page)

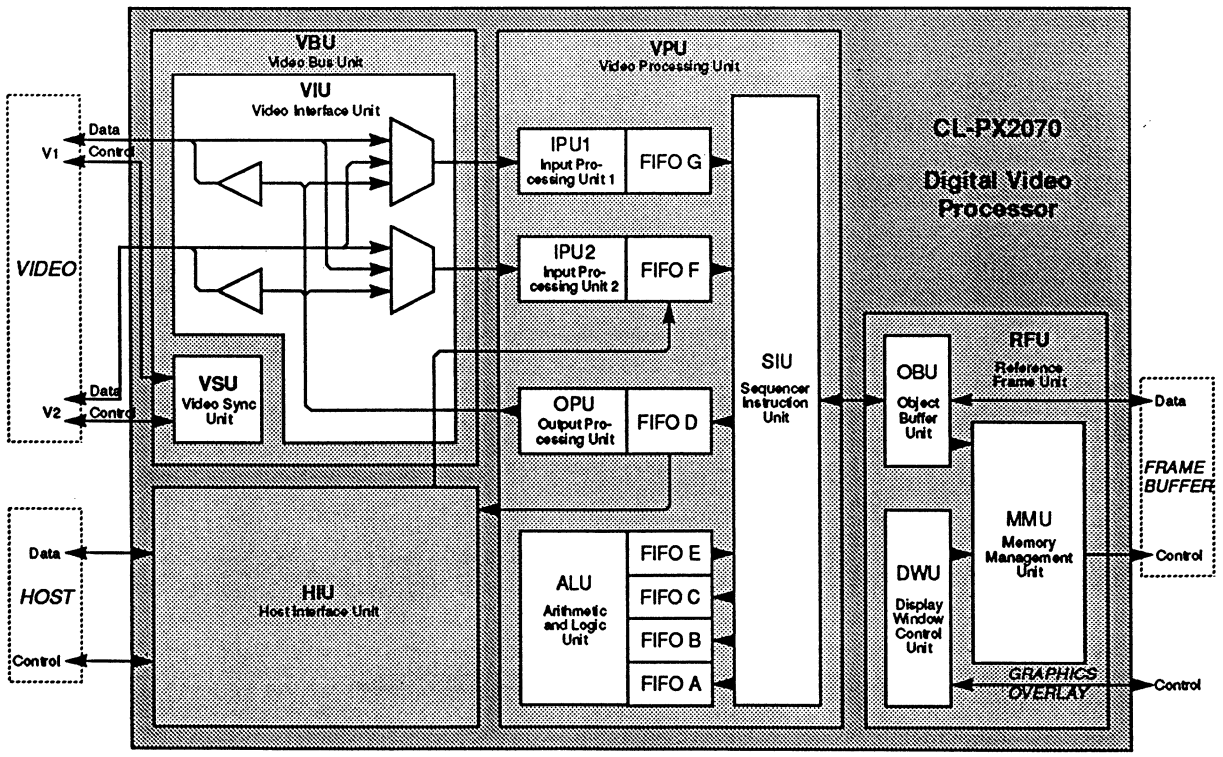
Digital Video Processor

OVERVIEW

The CL-PX2070 Digital Video Processor (DVP) provides a powerful, cost-effective desktop solution for computer graphics and imaging. The DVP can be used in presentations, video teleconferencing, animation, and video capture for scaling with video signal processors dedicated to compressing and decompressing video data streams.

(cont. next page)

Functional Block Diagram



FEATURES (cont.)

- **Complete frame buffer control**
- **1/2 - 8 Mbytes of frame buffer memory**
- **Video stream format conversion**
- **Color space conversion**
- **Supports up to eight simultaneous object buffers**
- **Programmable, triple-channel LUT RAM**
- **Prescaling, zoom, and windowing**
- **Graphic and bitmapped stream support**
- **Programmable sync slave or master**
- **When used with the CL-PX2080 MediaDAC™**
  - — Simultaneous video and graphics display
  - — Four simultaneous, overlapping (occluded) display windows
  - — Zooms from 1x to 256x
  - — 1024 x 768 display at 85 MHz

OVERVIEW (cont.)

The DVP combines the real-time video scaling features of the CL-PX0072 VWG with the frame buffer memory management, arithmetic and logical processing, a programmable host system bus interface, flexible mainstream video datapath, and windowing control for multiple, simultaneous video data streams.

The DVP has four major functional units:

- HIU: Host Interface Unit
- VBU: Video Bus Unit
- VPU: Video Processing Unit
- RFU: Reference Frame Unit

HIU: Host Interface Unit

The HIU interfaces the DVP to the host system. It transfers graphic or video data between the host system and the frame buffer through direct access to FIFOs in the VPU, and accesses the DVP control registers.

VBU: Video Bus Unit

The VBU manages the flow of video and graphic streams between the DVP and up to three independent devices (including the host system).

The VBU provides two independent, real-time video I/O ports (V1 and V2), and contains two subunits — the VIU and VSU.

V1 and V2 have the following characteristics:

- Each can be configured as input only, output only, or pixel- or field-duplexed I/O;
- Each provides programmable sync polarity;
- Either port can use the VSU sync generator;
- Each supports the following video formats:
  - — *Input:* YCbCr 16-bit 4:2:2, 12-bit 4:1:1; RGB 16-bit, 8-bit;
  - — *Output:* YCbCr 16-bit; RGB 16-bit, 8-bit;
- V2 controls the video stream data flow between the DVP and typical CODEC devices.

	ISA Bus	MCA Bus	Local Hardware
Interface	DVP interfaces with the host system interface bus.		DVP interfaces with the processor bus.
Multiplex Support	DVP signals support the required host system address/data impleading, and provide bidirectional buffering of the host system data bus.		N/A
Address Decode	DVP internally decodes the bus address during system I/O cycles.		The host system provides the decoded chip select signal for use with register select input signals.

The VIU (Video Interface Unit) controls the flow of internal video streams through the video ports to all external devices. It controls:

- the source and direction of video stream and sync control inputs;
- the field-toggling mode and field ID signals;
- the watchdog timer feature.

Two VIU master control registers provide matching fields that specify input and output sync modes.

The VSU (Video Sync Unit) implements identical, independent reference signals for each video port:

- Vertical sync signals specify the beginning of a field or frame.
- Horizontal sync signals specify the beginning of a line.
- Horizontal/composite blanking signals specify the horizontal/composite blanking interval.

VPU: Video Processing Unit

The VPU processes field-oriented video. It can simultaneously process two external, bidirectional real-time video streams and a single external, bidirectional host video or graphic data stream. It also provides a data path between the DVP and the host system for bidirectional graphic streams through the HIU. FIFO D can send to, and FIFO F can receive from the HIU directly.

The VPU has five subunits — the IPU1, IPU2, OPU, ALU, and SIU.

The IPU1 (Input Processor Unit 1) prepares an input video stream for ALU processing and/or storage in the frame buffer, then outputs the prepared stream to the frame buffer data bus. Its video processing features include:

- YCbCr and RGB input stream format conversion,
- color space conversion,
- programmable data tagging,
- three-channel lookup table operations,
- horizontal prescaling,
- window clipping,
- horizontal and vertical scaling, and
- output stream format conversion.

The IPU2 (Input Processor Unit 2) controls prescaling and windowing.

The OPU (Output Processing Unit) controls zoom, window clipping, and output format functions.

The ALU (Arithmetic Logic Unit) performs arithmetic, logical, and tagging operations for YCbCr streams, and logical and tagging operations only for RGB and 8-bit pseudocolor streams. It controls stream format, operand source selection, tagging operation selection, and arithmetic or logical operation for both field times, and can process up to three simultaneous video streams input through its FIFOs.

The SIU (Sequencer Instruction Unit) is a special-purpose microcontroller that coordinates the flow of multiple, simultaneous data streams between the IPU1, IPU2, OPU, ALU, and OBU.

The SIU is field-based when processing interlaced video data; that is, it distinguishes between the vertical sync pulses for each field and executes one of two different instruction sequences, causing multiple stream flows to appear concurrent.

RFU: Reference Frame Unit

The RFU provides simultaneous access to eight object buffers and four display windows. It has three subunits — the OBU, DWU, and MMU.

The OBU (Object Buffer Unit) specifies the size, location, operating mode, X and Y raster directions, FIFO association, chrominance and luminance channel masking, and output decimation for each object buffer. It allows each object buffer to be locked to either video source, or to be programmed to operate independently. Object buffers can also be placed anywhere within the linearly-addressable frame buffer.

The DWU (Display Window Unit) allows each display window to be any size or location. These display windows can overlap when the DVP is used with the CL-PX2080 MediaDAC™.

The MMU (Memory Management Unit) provides the frame buffer control interface for up to 8 megabytes of DRAM or VRAM.

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CONVENTIONS, ABBREVIATIONS, AND TRADEMARKS

CONVENTIONS

VIU_DPCf	Register names containing lower case variables represent groups of registers with similar functions. For example, VIU_DPCf represents *both* Datapath Control registers — VIU_DPC1 (Datapath Control, Field 1) and VIU_DPC2 (Datapath Control, Field 2). In this data book, the following register variables are used:		
	a (axis)	=	X, Y
	b (byte)	=	L (Low) or H (High)
	c (color space)	=	Y, U, V or R, G, B
	d (display window)	=	0:3
	f (field)	=	1:2
	n (number)	=	F (Fraction) or I (Integer)
	o (object buffer)	=	0:7
	p (port)	=	1:2
	s (SIM)	=	0:31
	x (channel)	=	Y, U, V

ABBREVIATIONS, ACRONYMS, and MNEMONICS

ALU	Arithmetic and Logic Unit
CODEC	COde/DEcode or Compress/decompress
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CTAG	Control TAG multiplexer signal
DRAM	Dynamic Random Access Memory
DWU	Display Window Unit
FBD	Frame Buffer Data
FIFO	First In, First Out
ISA	Industry Standard Architecture
I/O	Input/Output
LSA	Linear Start Address
JPEG	Joint Photographic Expert Group

LSB	Least Significant Byte
LSb	Least Significant bit
LUT	Look-Up Table
MCA	Micro Channel Architecture
MMU	Memory Management Unit
MSB	Most Significant Byte
MSb	Most Significant bit
OPU	Output Processor Unit
OTAG	Output TAG multiplexer signal
IPU1	Input Processor Unit 1
IPU2	Input Processor Unit 2
POS	Programmable Option Select
PQFP	Plastic Quad Flat Pack
PSE	PreScaler Enable
RGB	Red, Green, Blue
RAM	Random Access Memory
RFU	Reference Frame Unit
SIM	Sequencer Instruction Memory
SIU	Sequencer Instruction Unit
VPU	Video Processor Unit
VRAM	Video dynamic Random Access Memory
YCbCr	Components of the CCIR601 color representation standard. Y = luminance; CbCr = chrominance Y-blue, chrominance Y-red

TRADEMARKS

MediaDAC™ is a trademark of Pixel Semiconductor, Inc.

1. PIN INFORMATION

The CL-PX2070 DVP is available in a 160-lead Plastic Quad Flat Pack (PQFP) surface-mount package. It can be configured for ISA, MCA, and local hardware configurations, as shown in Figure 1-1.

NOTE: (*) denotes active-low signals.

1.1 Pin Diagram

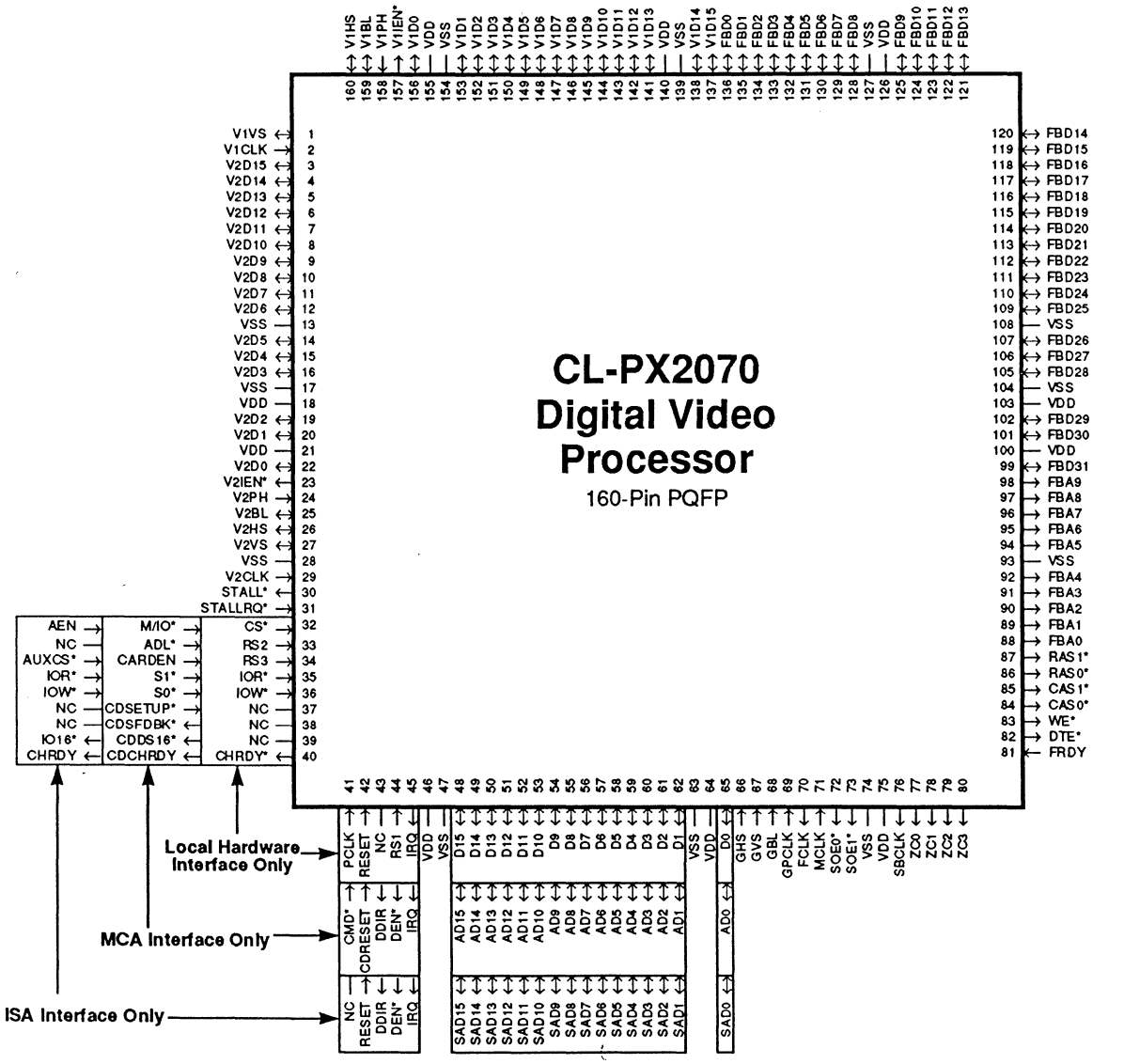
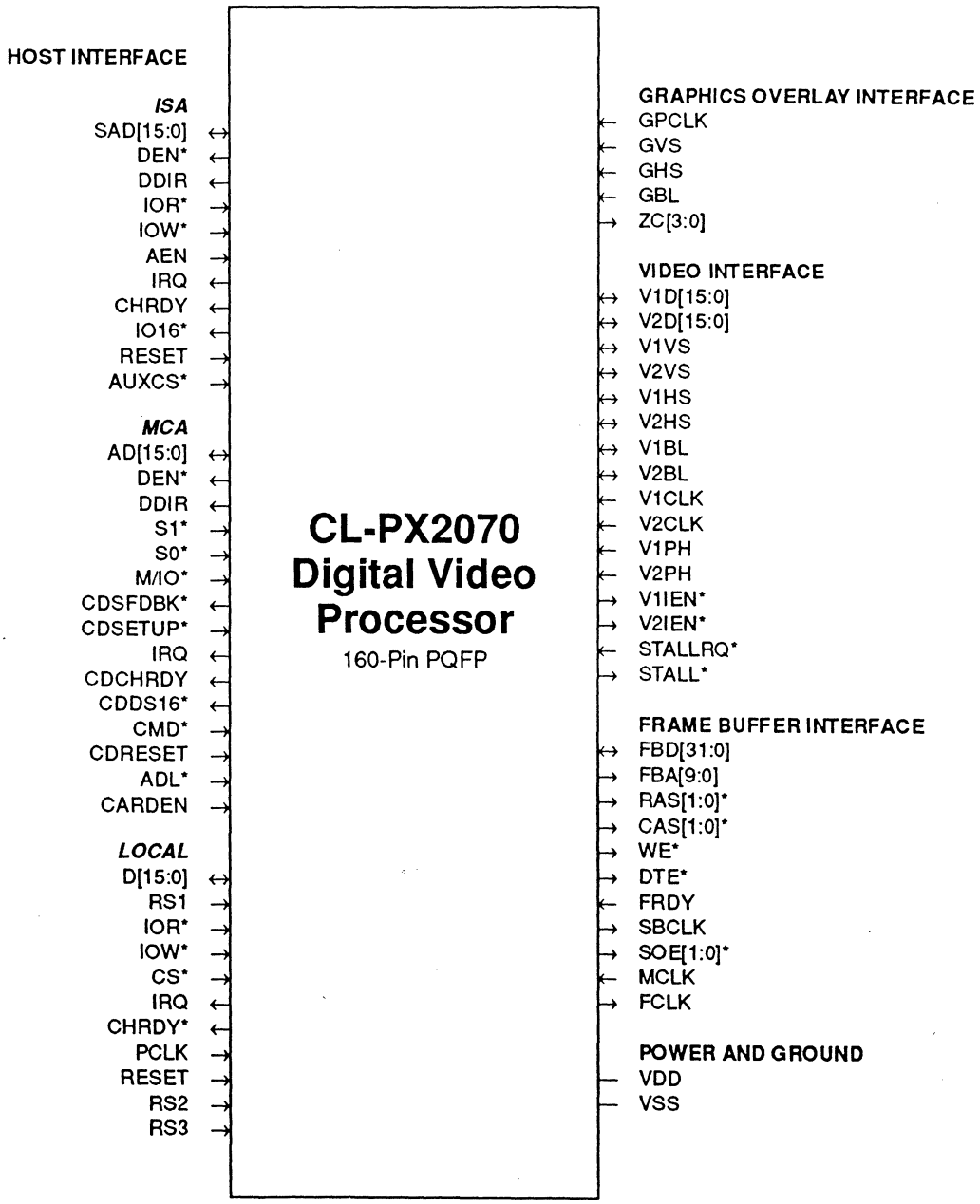


Figure 1-1. DVP Pin Diagram

1.2 DVP Functional Signal Groups



1.3 Pin Assignment Table

The following conventions are used in the pin assignment table:

(*) = active-low signal
I = input
O = output
PWR = power
TTL = the pad has standard TTL input threshold and output levels
OD = open drain, TTL inputs
4 = 4-mA sink and 2-mA source drive capability
24 = 24-mA sink and 8-mA source drive capability

NAME			PIN	TYPE	CELL	FUNCTION
HOST INTERFACE						
ISA	**MCA**	**LOCAL**				
Address/Data						
SAD[15:0]	AD[15:0]	—	48:62, 65	I/O	TTL, 4	Address/Data Bus
—	—	D[15:0]	48:62, 65	I/O	TTL, 4	Data Bus
Control						
DEN*	DEN*	—	44	OD	TTL, 8	Data Buffer Enable
—	—	RS1	44	I	TTL	Register Select
DDIR	DDIR	—	43	OD	TTL, 8	Data Buffer Direction
—	—	NC	43	N/A	N/A	No Connect (must be left floating)
IOR*	—	IOR*	35	I	TTL	I/O Read
—	S1*	—	35	I	TTL	Status 1
IOW*	—	IOW*	36	I	TTL	I/O Write
—	S0*	—	36	I	TTL	Status 0
AEN	—	—	32	I	TTL	Address Enable
—	M/IO*	—	32	I	TTL	Memory or I/O Cycle
—	—	CS*	32	I	TTL	Chip Select
NC	—	NC	38	N/A	N/A	No Connect (must be left floating)
—	CDSFDBK*	—	38	O	TTL, 4	Card Select Feedback
NC	—	NC	37	N/A	N/A	No Connect (must be left floating)
—	CDSETUP*	—	37	I	TTL	Card Setup
IRQ	IRQ	IRQ	45	O	TTL, 4	Interrupt Request
CHRDY	CDCHRDY	CHRDY*	40	OD	TTL, 24	Channel Ready
IO16*	—	—	39	OD	TTL, 24	16-bit I/O Cycle
—	CDDS16*	—	39	OD	TTL, 24	Card Data Size
—	—	NC	39	N/A	N/A	No Connect (must be left floating)
NC	—	—	41	N/A	N/A	No Connect (must be left floating)
—	CMD*	—	41	I	TTL	Command
—	—	PCLK	41	I	TTL	Processor Clock
RESET	CDRESET	RESET	42	I	TTL	Reset
NC	—	—	33	N/A	N/A	No Connect (must be left floating)
—	ADL*	—	33	I	TTL	Address Latch
—	—	RS2	33	I	TTL	Register Select
AUXCS*	—	—	34	I	TTL	Auxiliary Chip Select
—	CARDEN	—	34	I	TTL	Card Enable
—	—	RS3	34	I	TTL	Register Select

NAME	PIN	TYPE	CELL	FUNCTION
GRAPHICS OVERLAY INTERFACE				
GPCLK	69	I	TTL	Graphics Pixel Clock
GVS	67	I	TTL	Graphics Vertical Sync
GHS	66	I	TTL	Graphics Horizontal Sync
GBL	68	I	TTL	Graphics Blanking
ZC[3:0]	80:77	O	TTL, 4	Zoom Control Bus
VIDEO INTERFACE				
Data				
V1D[15:0]	137:138, 141:153, 156	I/O	TTL, 4	V1 (Video Port 1) Data Bus
V2D[15:0]	3:12, 14:16, 19:20, 22	I/O	TTL, 4	V2 (Video Port 2) Data Bus
Control				
V1VS	1	I/O	TTL, 4	V1 Vertical Sync
V2VS	27	I/O	TTL, 4	V2 Vertical Sync
V1HS	160	I/O	TTL, 4	V1 Horizontal Sync
V2HS	26	I/O	TTL, 4	V2 Horizontal Sync
V1BL	159	I/O	TTL, 4	V1 Horizontal/Composite Blanking
V2BL	25	I/O	TTL, 4	V2 Horizontal/Composite Blanking
V1CLK	2	I	TTL	V1 Data Clock
V2CLK	29	I	TTL	V2 Data Clock
V1PH	158	I	TTL	V1 Phase
V2PH	24	I	TTL	V2 Phase
V1IEN*	157	O	TTL, 4	V1 Input Enable
V2IEN*	23	O	TTL, 4	V2 Input Enable
STALLRQ*	31	I	TTL	Stall Request
STALL*	30	O	TTL, 4	Stall
FRAME BUFFER INTERFACE				
Address/Data				
FBD[31:0]	99, 101:102, 105:107, 109:125, 128:136	I/O	TTL, 4	Frame Buffer Data Bus
FBA[9:0]	98:94, 92:88	O	TTL, 8	Frame Buffer Address Bus
Control				
RAS[1:0]*	87:86	O	TTL, 8	Row Address Strobes
CAS[1:0]*	85:84	O	TTL, 8	Column Address Strobes
WE*	83	O	TTL, 12	Write Enable
DTE*	82	O	TTL, 12	Data Transfer Enable
FRDY	81	I	TTL	FIFO Ready
SBCLK	76	O	TTL, 8	Serial Bus Clock
SOE[1:0]*	73:72	O	TTL, 8	Serial Port Output Enable
MCLK	71	I	TTL	Memory Clock
FCLK	70	O	TTL, 8	FIFO Write Clock
POWER AND GROUND				
VDD	18, 21, 46, 64, 75, 100, 103, 126, 140, 155	PWR	N/A	+5 VDC for Digital Logic and Interface Buffers
VSS	13, 17, 28, 47, 63, 74, 93, 104, 108, 127, 139, 154	PWR	N/A	Ground for Digital Logic and Interface Buffers

2. DETAILED SIGNAL DESCRIPTIONS

2.1 Host Interface — ISA

Signal	Pin	Type	Cell	Function
SAD[15:0]	48:62, 65	I/O	TTL, 4	**Address/Data Bus.** Bidirectional, multiplexed address/data bus that transfers video data and operation status and commands between the host system and the DVP.
DEN*	44	OD	TTL, 8	**Data Buffer Enable.** 0 Enables the host data bus buffer.
DDIR	43	OD	TTL, 8	**Data Buffer Direction.** Specifies the direction of data flow on SAD[15:0]. 0 The host system is reading data from SAD[15:0]; 1 The host system is writing data to SAD[15:0].
IOR*	35	I	TTL	**I/O Read.** 0 Specifies an I/O read cycle.
IOW*	36	I	TTL	**I/O Write.** 0 Specifies an I/O write cycle.
AEN	32	I	TTL	**Address Enable.** 0 I/O cycle in progress. 1 DMA cycle in progress.
NC	38	N/A	N/A	**No Connect.** (must be left floating).
NC	37	N/A	N/A	**No Connect.** (must be left floating).
IRQ	45	O	TTL, 4	**Interrupt Request.** 1 The DVP is requesting service from the host system.
CHRDY	40	OD	TTL, 24	**Channel Ready.** 0 The DVP is not ready to complete the current host access cycle. 1 The current host access cycle is complete.
IO16*	39	OD	TTL, 24	**16-bit I/O Cycle.** 0 The DVP is able to respond as a 16-bit I/O data device for both read and write cycles.
NC	41	N/A	N/A	**No Connect.** (must be left floating).
RESET	42	I	TTL	**Reset.** 1 Stops all DVP activity and resets the hardware.
NC	33	N/A	N/A	**No Connect.** (must be left floating).
AUXCS*	34		TTL	**Auxiliary Chip Select.** When programmed for aux ISA mode, primary and secondary addresses are ignored; AUXCS* and SAD[3:1] select specific registers.

2.2 Host Interface — MCA

Signal	Pin	Type	Cell	Function
AD[15:0]	48:62, 65	I/O	TTL, 4	**Address/Data Bus.** Bidirectional, multiplexed address/data bus that transfers video data and operation status and commands between the host system and the DVP.
DEN*	44	OD	TTL, 8	**Data Buffer Enable.** 0 Enables the host data bus buffer.
DDIR	43	OD	TTL, 8	**Data Buffer Direction.** Specifies the direction of data flow on SAD[15:0]. 0 The host system is reading data from SAD[15:0]; 1 The host system is writing data to SAD[15:0].
S1*	35	I	TTL	**Status 1.** Specifies current bus cycle (used with M/IO* and S0*).
S0*	36	I	TTL	**Status 0.** Specifies current bus cycle (used with M/IO* and S1*).
M/IO*	32	I	TTL	**Memory or I/O Cycle.** Specifies current bus cycle current bus cycle (used with S0* and S1*): **M/IO* S0* S1*** 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
CDSFDBK*	38	O	TTL, 4	**Card Select Feedback.** 0 Specifies that the DVP has decoded the current address and status inputs. The DVP does not drive CDSFDBK* low during the configuration period (CDSETUP* = 0).
CDSETUP*	37	I	TTL	**Card Setup.** 0 Specifies that the host system is accessing the configuration registers of the MCA adapter. To obtain adapter ID and configuration data (containing POS [Programmable Option Select] 100, 101, and 102), perform an I/O read cycle to the DVP.
IRQ	45	O	TTL, 4	**Interrupt Request.** 0 The DVP is requesting service from the host system.
CDCHRDY	40	OD	TTL, 24	**Channel Ready.** 1 The DVP is ready to complete the current host access cycle.
CDDS16*	39	OD	TTL, 24	**Card Data Size.** 0 The DVP is able to respond as a 16-bit I/O data device for both read and write cycles.

2.2 Host Interface — MCA *(cont.)*

Signal	Pin	Type	Cell	Function
CMD*	41	I	TTL	**Command.** 0 Valid data is on AD[15:0] (write cycle); or DVP should place valid data on AD[15:0] (read cycle).
CDRESET	42	I	TTL	**Reset.** 1 Stops all DVP activity and resets the hardware.
ADL*	33	I	TTL	**Address Latch.** 0 Demultiplexes the address from bus AD[15:0], and status from signals M/IO*, S1*, and S0*. The address and status must be valid during the low-to-high transition.
CARDEN	34	I	TTL	**Card Enable.** 1 Specifies that the data on bus AD[15:8] is valid.

2.3 Host Interface — Local Hardware

Signal	Pin	Type	Cell	Function
D[15:0]	48:62, 65	I/O	TTL, 4	**Data Bus.** Bidirectional data bus that transfers video data between the host system and the DVP.
RS[3:1]	34:33, 44	I	TTL	**Register Select.** Specify the register address during a host access.
NC	43	N/A	N/A	**No Connect.** (must be left floating).
IOR*	35	I	TTL	**I/O Read.** 0 Specifies an I/O read cycle.
IOW*	36	I	TTL	**I/O Write.** 0 Specifies an I/O write cycle.
CS*	32	I	TTL	**Chip Select.** 0 The host system is accessing the DVP.
NC	38	N/A	N/A	**No Connect.** (must be left floating).
NC	37	N/A	N/A	**No Connect.** (must be left floating).
IRQ	45	O	TTL, 4	**Interrupt Request.** 0 The DVP is requesting service from the host system.
CHRDY*	40	OD	TTL, 24	**Channel Ready.** 0 The DVP is ready to complete the current host access cycle.
NC	39	N/A	N/A	**No Connect.** (must be left floating).

2.3 Host Interface — Local Hardware *(cont.)*

Signal	Pin	Type	Cell	Function
PCLK	41	I	TTL	**Processor Clock.** Input clock that synchronizes the flow of data on bus D[15:0] during DMA data transfers.
RESET	42	I	TTL	**Reset.** 1 Stops all DVP activity and resets the hardware.

2.4 Graphics Overlay Interface

Signal	Pin	Type	Cell	Function
GPCLK	69	I	TTL	**Graphics Pixel Clock.** Clocks display output pixel data from the graphics controller.
GVS	67	I	TTL	**Graphics Vertical Sync.** Identifies the start of the vertical sync interval. A vertical sync pulse is generated once every field time for interlaced data, and once every frame time for non-interlaced data. Register DWU_MCR, bit GVSP specifies GVS as active high or active low.
GHS	66	I	TTL	**Graphics Horizontal Sync.** Identifies the start of the horizontal sync interval. A horizontal sync pulse is generated once for each input line. Register DWU_MCR, bit GHSP specifies GHS as active high or active low.
GBL	68	I	TTL	**Graphics Blanking.** Identifies the blanking interval. Register DWU_MCR, bit GBP specifies GBL as active high or active low.
ZC[3:0]	80:77	O	TTL, 4	**Zoom Control Bus** (used only with CL-PX2080 MediaDAC™). Specifies to the MediaDAC™ the zoom factor to be used on the current data.

2.5 Video Interface

Signal	Pin	Type	Cell	Function	
V1D[15:0]	156, 153:141, 138:137	I/O	TTL, 4	**V1 (Video Port 1) Data Bus.**	*VnD[15:0].* Bidirectional data bus that transfers video data between the DVP and an external device through video port Vn.
V2D[15:0]	3:12, 14:16, 19:20, 22	I/O	TTL, 4	**V2 (Video Port 2) Data Bus.**	
V1VS	1	I/O	TTL, 4	**V1 Vertical Sync.**	*VnVS.* Identifies the start of the vertical sync interval. A vertical sync pulse is generated once every field time for interlaced data, and once every frame time for non-interlaced data. Register VIU_MCRp (bits OVSP/IVSP) specifies VnVS as active high or active low.
V2VS	27	I/O	TTL, 4	**V2 Vertical Sync.**	
V1HS	160	I/O	TTL, 4	**V1 Horizontal Sync.**	*VnHS.* Identifies the start of the horizontal sync interval; register VIU_MCRp (bits OHSP/IHSP) specifies VnHS as active high or active low.
V2HS	26	I/O	TTL, 4	**V2 Horizontal Sync.**	
V1BL	159	I/O	TTL, 4	**V1 Horizontal/Composite Blanking.**	*VnBL.* Identifies the blanking interval; register VIU_MCRp (bits OBP/IBP) specifies VnBL as active high or active low.
V2BL	25	I/O	TTL, 4	**V2 Horizontal/Composite Blanking.**	
V1CLK	2	I	TTL	**V1 Data Clock.**	*VnCLK.* Clocks bidirectional video data on bus VnD[15:0].
V2CLK	29	I	TTL	**V2 Data Clock.**	
V1PH	158	I	TTL, 4	**V1 Phase.**	*VnPH.* Controls data qualification and duplexing of video data on VnD[15:0].
V2PH	24	I	TTL	**V2 Phase.**	
V1IEN*	157	O	TTL, 4	**V1 Input Enable.**	*VnIEN*.* Specifies that the DVP is not driving bus VnD[15:0]. VnIEN* can be used as a tristate control by an external buffer connected to bus VnD[15:0].
V2IEN*	23	O	TTL, 4	**V2 Input Enable.**	
STALLRQ*	31	I	TTL	**Stall Request.** 0 Requests that the current transfer of video data on bus V2D[15:0] be suspended.	
STALL*	30	O	TTL, 4	**Stall.** 0 The DVP has suspended transferring data on V2D[15:0].	

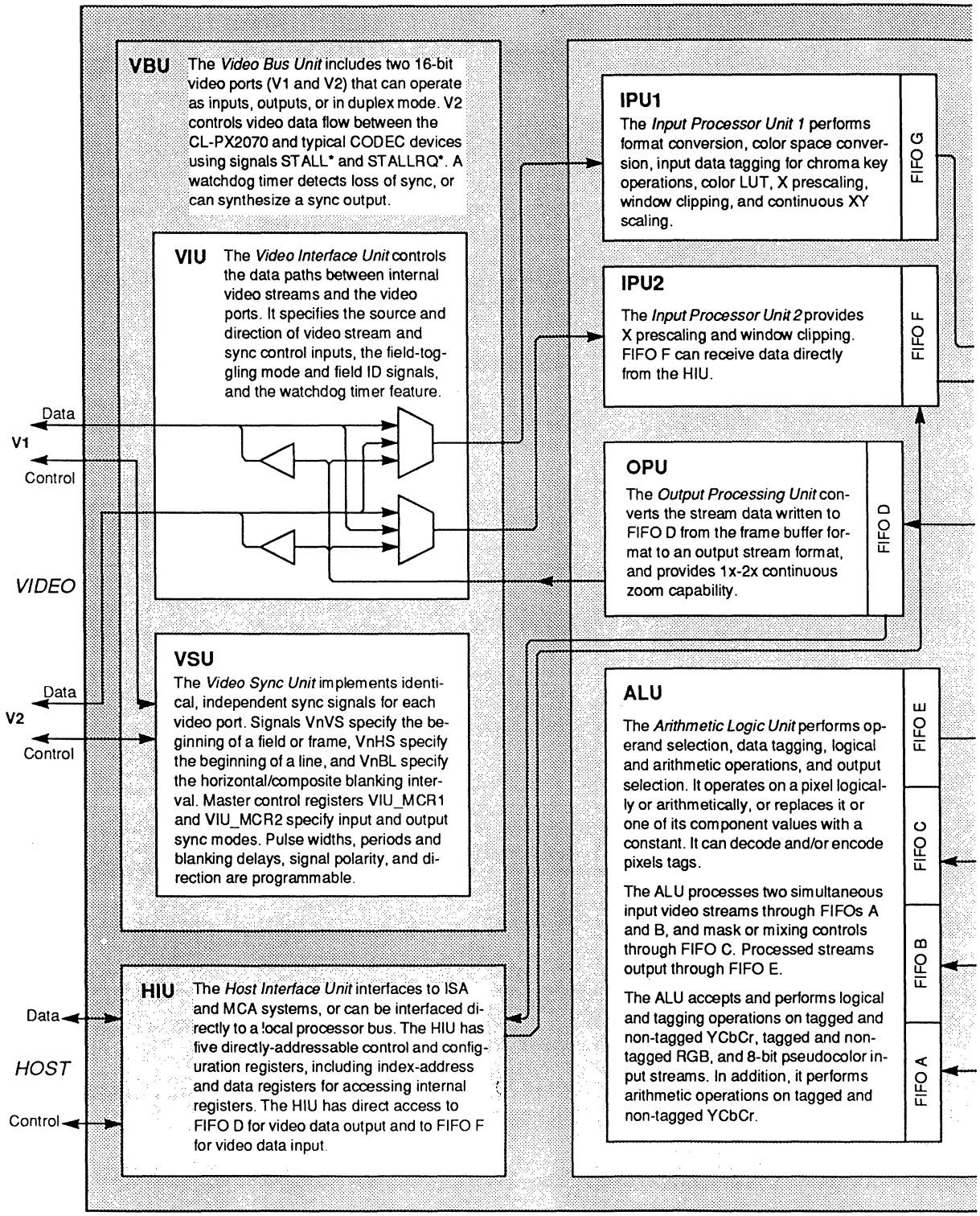
2.6 Frame Buffer Interface

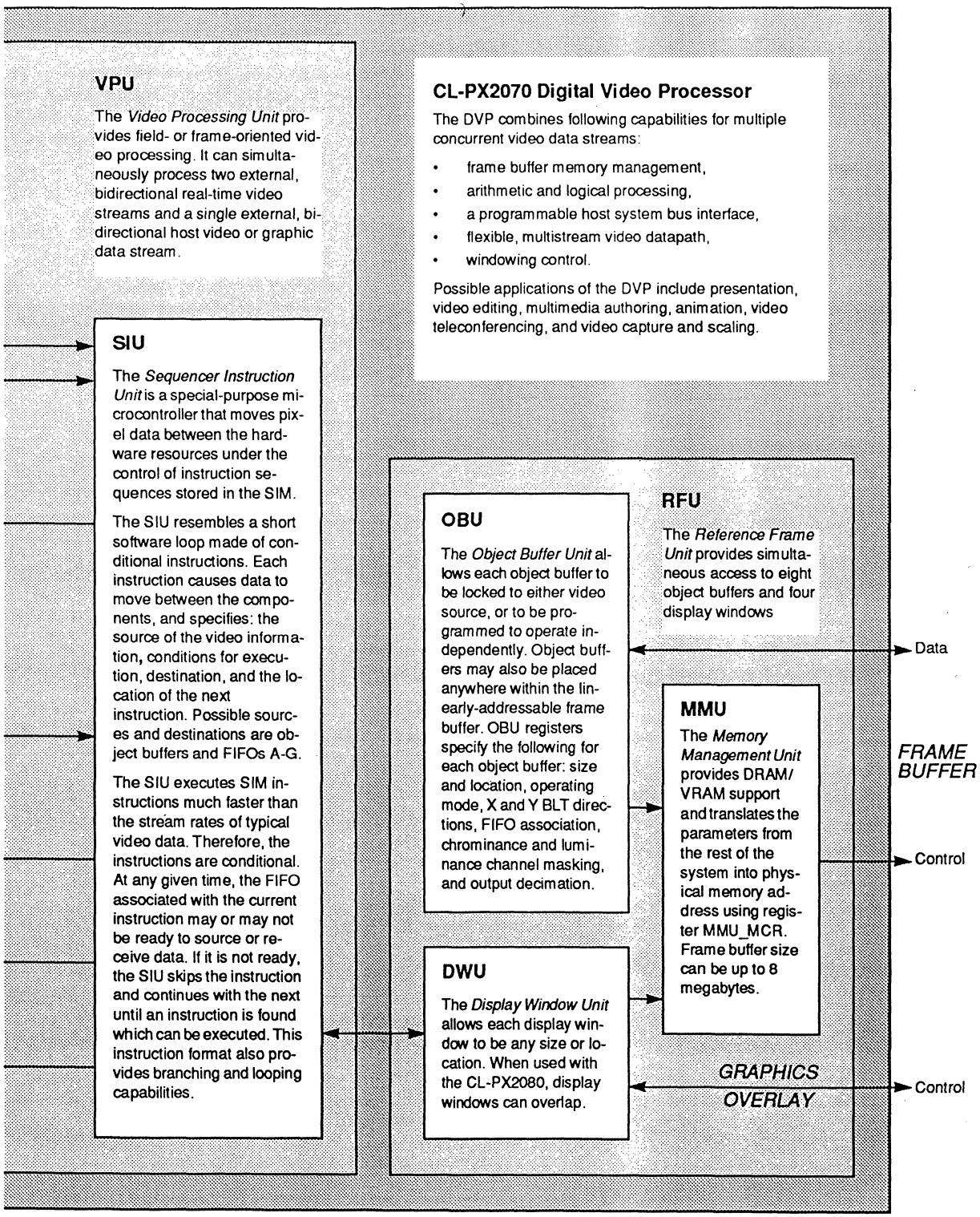
Signal	Pin	Type	Cell	Function
FBD[31:0]	136:128, 125:109, 107:105, 102:101, 99	I/O	TTL, 4	**Frame Buffer Data Bus.** Bidirectional data bus that transfers data between the DVP and the frame buffer.
FBA[9:0]	98:94, 92:88	O	TTL, 8	**Frame Buffer Address Bus.** Multiplexed output bus that specifies an address to the frame buffer. The row address is valid during the HIGH-to-LOW transition of signals RAS[1:0]*; the column address is valid during the high-to-low transition of CAS[1:0]*.
RAS[1:0]*	87:86	O	TTL, 8	**Row Address Strobes.** Instruct the frame buffer to latch the row address from bus FBA[9:0] during the HIGH-to-LOW transition.
CAS[1:0]*	85:84	O	TTL, 8	**Column Address Strobes.** Instruct the frame buffer to latch the column address from bus FBA[9:0] during the HIGH-to-LOW transition.
WE*	83	O	TTL, 12	**Write Enable.** Specifies a write cycle to the frame buffer.
DTE*	82	O	TTL, 12	**Data Transfer Enable.** Specifies a transfer cycle to the frame buffer (VRAMs only).
FRDY	81	I	TTL	**FIFO Ready.** (used only with CL-PX2080 MediaDAC™) Specifies that the input FIFO of the MediaDAC™ is ready to receive serial data from the frame buffer.
SBCLK	76	O	TTL, 8	**Serial Bus Clock.** Clocks serial data from the frame buffer (VRAMs only).
SOE[1:0]*	73:72	O	TTL, 8	**Serial Port Output Enable.** 0 Enable the frame-buffer serial data port output.
MCLK	71	I	TTL	**Memory Clock.** Synchronizes all frame buffer control signals.
FCLK	70	O	TTL, 8	**FIFO Write Clock.** (used only with CL-PX2080 MediaDAC™) Clocks serial data into the MediaDAC™.

2.7 Power and Ground

Signal	Pin	Type	Function
VDD	18, 21, 46, 64, 75, 100, 103, 126, 140, 155	PWR	**+5 VDC for Digital Logic and Interface Buffers.** Each VDD pin must be connected directly to the VDD plane.
VSS	13, 17, 28, 47, 63, 74, 93, 104, 108, 127, 139, 154	PWR	**Ground for Digital Logic and Interface Buffers.** Each VSS pin must be connected directly to the ground plane.

3. FUNCTIONAL DESCRIPTION




VPU
The Video Processing Unit provides field- or frame-oriented video processing. It can simultaneously process two external, bidirectional real-time video streams and a single external, bidirectional host video or graphic data stream.
CL-PX2070 Digital Video Processor
The DVP combines following capabilities for multiple concurrent video data streams:
• frame buffer memory management,
• arithmetic and logical processing,
• a programmable host system bus interface,
• flexible, multistream video datapath,
• windowing control.
Possible applications of the DVP include presentation, video editing, multimedia authoring, animation, video teleconferencing, and video capture and scaling.
SIU
The Sequencer Instruction Unit is a special-purpose microcontroller that moves pixel data between the hardware resources under the control of instruction sequences stored in the SIM.
The SIU resembles a short software loop made of conditional instructions. Each instruction causes data to move between the components, and specifies: the source of the video information, conditions for execution, destination, and the location of the next instruction. Possible sources and destinations are object buffers and FIFOs A-G.
The SIU executes SIM instructions much faster than the stream rates of typical video data. Therefore, the instructions are conditional. At any given time, the FIFO associated with the current instruction may or may not be ready to source or receive data. If it is not ready, the SIU skips the instruction and continues with the next until an instruction is found which can be executed. This instruction format also provides branching and looping capabilities.
OBU
The Object Buffer Unit allows each object buffer to be locked to either video source, or to be programmed to operate independently. Object buffers may also be placed anywhere within the linearly-addressable frame buffer. OBU registers specify the following for each object buffer: size and location, operating mode, X and Y BLT directions, FIFO association, chrominance and luminance channel masking, and output decimation.
RFU
The Reference Frame Unit provides simultaneous access to eight object buffers and four display windows
Data
MMU
The Memory Management Unit provides DRAM/VRAM support and translates the parameters from the rest of the system into physical memory address using register MMU_MCR. Frame buffer size can be up to 8 megabytes.
FRAME BUFFER
Control
DWU
The Display Window Unit allows each display window to be any size or location. When used with the CL-PX2080, display windows can overlap.
GRAPHICS OVERLAY
Control

4. DETAILED REGISTER DESCRIPTIONS

This section lists and defines the CL-PX2070 DVP registers.

NOTE: In order to maintain compatibility with future Pixel Semiconductor products, all reserved registers bits must be written as '0'. Data values in reserved register locations are not guaranteed on readback.

Register names containing lower-case variables represent groups of registers with similar functions. Refer to the *Conventions* table on page 8 for a list of DVP register variables.

4.1 HIU: Host Interface Unit

Table 4-1. HIU Register Address Map

Register	Pri. Map	Sec. Map	Definition	Used by Registers		Ref. Section
HIU_0	27C0	0290	Register I/O Address 0	HIU_CSU	Configuration Setup	4.1.1, p. 23
				HIU_DBG	Debug Control	4.1.2, p. 24
				HIU_DRD	Debug Read	4.1.3, p. 24
HIU_1	27C2	0292	Register I/O Address 1	HIU_OCS	Operation Control/Status	4.1.5, p. 26
				HIU_IRQ	Interrupt Request	4.1.4, p. 25
HIU_2	27C4	0294	Register I/O Address 2	HIU_RIN	Register Index	4.1.6, p. 27
HIU_3	27C6	0296	Register I/O Address 3	HIU_RDT	Register Data Port	4.1.7, p. 28
HIU_4	27C8	0298	Register I/O Address 4	HIU_MDT	Memory Data Port	4.1.8, p. 28

Table 4-2. HIU Registers Accessed by the Register Data Port

Register	Index	Definition	Ref. Section
HIU_ISU	0001	Interrupt Setup	4.1.9, p. 29

4.1.1 HIU_CSU: Configuration Setup

I/O Address 27C0 (Primary Map)
0290 (Secondary Map)

HIU_CSU is a read-only register that stores hardware configuration data for the DVP. An external configuration register must provide configuration data to bits 5:0 during the reset interval. HIU_CSU is shadowed by registers HIU_DBG and HIU_DRD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				VER				RSVD		HSB			RSVD	FBT	PAS

Bit #	Access	Reset	Description	
15:12	R	0000	RSVD	Reserved (read as '0').
11:8	R	0000	VER	DVP Device Version 0000 CL-PX2070 revision AB 0001 CL-PX2070, revision AC
7:6	R	00	RSVD	Reserved (read as '00')
5:3	R	111	HSB	Host System Bus. Specifies the type of host system connected to the DVP. 000 ISA bus 001 MCA bus 010 Reserved 011 Local hardware interface 100 Aux ISA 101 Aux MCA 111 Local hardware interface XXX All other configurations reserved
2	R	1	RSVD	Reserved (read as 1)
1	R	1	FBT	Frame Buffer Jumper State. (Used only for software configuration. Does not affect internal DVP operation.) 0 DRAM 1 VRAM
0	R	0	PAS	Port Address Select. Specifies the I/O address map that the host system should use when accessing the DVP. 0 Primary port map 1 Secondary port map

4.1.2 HIU_DBG: Debug Control

I/O Address 27C0 (Primary Map) 0290 (Secondary Map)

HIU_DBG is a write-only register that controls the diagnostic mode of the DVP. Register HIU_OCS, field MDE enables access to this register when set to '1.' HIU_DBG is shadowed by register HIU_DRD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						DRE	RSVD								

Bit #	Access	Reset	Description	
15:10	W	0h	RSVD	Reserved (read as '0').
9	W	0	DRE	Debug Read Enable. Enables access to shadow register HIU_DRD. 0 Disable debug read 1 Enable debug read
8:0	W	00h	RSVD	Reserved (read as '0').

4.1.3 HIU_DRD: Debug Read

I/O Address 27C0 (Primary Map) 0290 (Secondary Map)

See also: HIU_DBG: Debug Control, p. 24
HIU_OCS: Operation Control/Status, p. 26
SIU_MCR: SIU Master Control, p. 58
SIUs_SIM: Sequencer Instruction Memory, p. 61

HIU_DRD is a read-only register that provides diagnostic information, including the global Error Detection Trap, the current object buffer counters, and the SIU current index. HIU_DRD is a shadow register to HIU_CSU. Read access to this register is enabled when HIU_OCS, field MDE and HIU_DBG, field DRE are set to '1.'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EDT	XC					YC					SIMIN				

Bit #	Access	Reset	Description	
15	R	0	EDT	Error Detection Trap. This field is the logical OR of all FIFO overflow and underflow flags, and the watchdog timeout. 0 No error 1 Error detected
14:10	R	0h	XC	X Counter. Upper 5 bits of X Counter (Single-Step Mode). (0-1Fh)
9:5	R	0h	YC	Y Counter. Upper 5 bits of Y Counter (Single-Step Mode). (0-1Fh)
4:0	R	0h	SIMIN	Sequence Instruction Memory Current Index (0-1Fh)

4.1.4 HIU_IRQ: Interrupt Request

I/O Address 27C2 (Primary Map)
0292 (Secondary Map)

See also: HIU_OCS: Operation Control/Status, p. 26
HIU_ISU: Interrupt Setup, p. 29

HIU_IRQ is a read-only register that accesses all interrupt requests generated by the IPU1, IPU2, OBU, the watchdog timer, and the FIFO overflow and underflow flags. An interrupt service routine typically uses HIU_IRQ to determine the interrupt request source(s). HIU_IRQ shadows register HIU_OCS. HIU_OCS, field SRC must be set to '1' to enable this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										OBT	IP2C	IP1C	FUN	FOV	WDT

Bit #	Access	Reset	Description	
15:6	R	0h	RSVD	Reserved (read as '0').
5	R	0	OBT	Object Buffer Termination (auto reset on read). 0 No interrupt request 1 Specifies that an object buffer termination condition occurred in the OBU.
4	R	0	IP2C	IPU2 Counter (auto reset on read). 0 No interrupt request 1 Specifies that a line, field, or vertical sync pulse interrupt request occurred in the IPU2.
3	R	0	IP1C	IPU1 Counter (auto reset on read). 0 No interrupt request 1 Specifies that a line, field, or vertical sync pulse interrupt request occurred in the IPU1.
2	R	0	FUN	FIFO Underflow (auto reset on read). 0 No interrupt request 1 Specifies that an underflow condition occurred in a FIFO. (See SIU_FOU: FIFO Overflow/Underflow, p. 60.)
1	R	0	FOV	FIFO Overflow (auto reset on read). 0 No interrupt request 1 Specifies that an overflow condition occurred in a FIFO. (See SIU_FOU: FIFO Overflow/Underflow, p. 60.)
0	R	0	WDT	Watchdog Timer to generate signal IRQ (auto reset on read). 0 No interrupt request 1 Specifies that a timeout condition occurred in VIU_WDT.

4.1.5 HIU_OCS: Operation Control/Status

I/O Address 27C2h (Primary Map)
0292 (Secondary Map)

Register HIU_OCS controls the operating mode of the DVP and provides status indicators. HIU_OCS is shadowed during read cycles by register HIU_IRQ.

NOTE: Modifications to registers designated as posted do not affect the operation of the DVP until a post command is issued either manually using bit PMC, or automatically by the SIU. Automatic posting typically occurs between field or frame times.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	FDNE	FFNF	RSVD	SRC	MDE	DPC	MPC	PMC	RSVD		SR	IEM			

Bit #	Access	Reset	Description	
15	R	0	RSVD	Reserved (read as '0').
14	R	0	FDNE	FIFO D Nearly Empty. 1 FIFO D is within 16 pixels of being empty
13	R	0	FFNF	FIFO F Nearly Full. 1 FIFO F is within 16 pixels of being full
12	R	0	RSVD	Reserved (read as '0').
11	R/W	0	SRC	Status Read Select. Specifies register to access during a read cycle. 0 Read status from register HIU_OCS 1 Read status from shadow register HIU_IRQ
10	R/W	0	MDE	Master Debug Enable. 0 Disable debug support registers HIU_DBG and HIU_DRD 1 Enable access to registers HIU_DBG and HIU_DRD
9	R/W	0	DPC	Display Window Posting Operation Control (auto reset). Enables the register posting mode of the DWU. 0 Disable posting 1 Enable posting (auto reset on post)
8	R/W	0	MPC	Master Posting Control (auto reset). Enables all DVP register posting logic. 0 Disable posting 1 Enable posting (auto reset on post)
7	R/W	0	PMC	Posting Mode Control. 0 Specifies normal register posting operation (waits for vertical sync) 1 Forces immediate post all registers (DPC, MPC must = '1')
6:5	R/W	0	RSVD	Reserved (read as '0').

Bit #	Access	Reset	Description	
4	R/W	0	SR	Soft Reset. Causes a soft reset to be performed on all internal units. All registers are reset to 0, all FIFOs are cleared, and all counters are set to 0. Output signals are not placed in three-state. 0 No reset performed 1 Perform soft reset
3:0	R/W	0000	IEM	Interrupt Enable Mask. Enables interrupt requests. When more than one interrupt source is enabled, the requests are ORed — any source can assert signal IRQ. See Section 4.1.9 on page 29 for additional information on the interrupt system. 0001 Enable counter to generate signal IRQ 0010 Enable watchdog to generate signal IRQ 0100 Enable object buffer termination to generate signal IRQ 1000 Enable FIFO overflow/underflow to generate signal IRQ

4.1.6 HIU_RIN: Register Index

I/O Address 27C4 (Primary Map)
0294 (Secondary Map)

Register HIU_RIN specifies the index value of the next register to be accessed. An optional control (bit AIC) automatically increments the index address on consecutive read or write cycles.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIC	RIN														

Bit #	Access	Reset	Description	
15	R/W	0h	AIC	Automatic Increment Control (index address). 0 Disable 1 Enable
14:0	R/W	0h	RIN	Register Index. (0-7FFFh)

4.1.7 HIU_RDT: Register Data Port

I/O Address 27C6 (Primary Map)
0296 (Secondary Map)

HIU_RDT is the register data port. Registers are index-mapped to HIU_RDT by HIU_RIN.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIO															

Bit #	Access	Reset	Description	
15:0	R/W	0h	DIO	Register Data I/O

4.1.8 HIU_MDT: Memory Data Port

I/O Address 27C8 (Primary Map)
0298 (Secondary Map)

I/O port HIU_MDT accesses the frame buffer. To maintain data integrity when reading or writing to this port, first check the status of the appropriate FIFO.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIO															

Bit #	Access	Reset	Description	
15:0	R/W	0h	MIO	Memory Data I/O

4.1.9 HIU_ISU: Interrupt Setup

I/O Address HIU_RDT
Index 0001

Register HIU_ISU specifies the interrupt modes for the IPU1, IPU2, and the OBU. Any interrupt requests generated in the IPU1, IPU2, and OBU must also be enabled through register HIU_OCS, field IEM.

IPU interrupts are combined with an AND function. If more than one interrupt source is enabled within an IPnS field, all sources must be active before an interrupt request is posted.

The interrupt sources in the OBIS field use an OR function. If more than one interrupt source is selected, any one active source can trigger an interrupt.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		IP2S			IP1S			OBIS							

Bit #	Access	Reset	Description	
15:14	R/W	00	RSVD	Reserved (read as '0').
13:11	R/W	000	IP2S	IPU2 Interrupt Select. Specifies the IPU2 line count, field count, and input vertical sync pulse combination required to generate an interrupt request. 001 Interrupt on line count 010 Interrupt on field count 100 Interrupt on vertical sync
10:8	R/W	000	IP1S	IPU1 Interrupt Select. Specifies the IPU1 line count, field count, and input vertical sync pulse combination required to generate an interrupt request. 001 Interrupt on line count 010 Interrupt on field count 100 Interrupt on vertical sync
7:0	R/W	0h	OBIS	Object Buffer Termination Interrupt Request. Specifies the OBU object buffer termination conditions combination required to generate interrupt request signal IRQ. 01h Object buffer 0 termination 02h Object buffer 1 termination 04h Object buffer 2 termination 08h Object buffer 3 termination 10h Object buffer 4 termination 20h Object buffer 5 termination 40h Object buffer 6 termination 80h Object buffer 7 termination

4.2 VBU: Video Bus Unit

Register	Index	Definition	Posted?	Ref. Section
VIU: Video Interface Unit				4.2.1, p. 30
VIU_MCR1	1000	VIU Master Control V1	—	4.2.1.1, p. 30
VIU_MCR2	1001	VIU Master Control V2	—	4.2.1.1, p. 30
VIU_DPC1	1002	Datapath Control, Field 1	POSTED	4.2.1.2, p. 32
VIU_DPC2	1003	Datapath Control, Field 2	POSTED	4.2.1.2, p. 32
VIU_WDT	1004	Watchdog Timer	POSTED	4.2.1.3, p. 33
VIU_TEST	1006	Test Register	—	4.2.1.4, p. 34
VSU: Video Sync Unit				4.2.2, p. 35
VSU_HSW	1100	Horizontal Sync Width	POSTED	4.2.2.1, p. 35
VSU_HAD	1101	Horizontal Active Delay	POSTED	4.2.2.2, p. 36
VSU_HAP	1102	Horizontal Active Pixels	POSTED	4.2.2.3, p. 36
VSU_HP	1103	Horizontal Period	POSTED	4.2.2.4, p. 36
VSU_VSW	1104	Vertical Sync Width	POSTED	4.2.2.5, p. 37
VSU_VAD	1105	Vertical Active Delay	POSTED	4.2.2.6, p. 37
VSU_VAP	1106	Vertical Active Pixels	POSTED	4.2.2.7, p. 38
VSU_VP	1107	Vertical Period	POSTED	4.2.2.8, p. 38

4.2.1 VIU: Video Interface Unit

4.2.1.1 VIU_MCRp: VIU Master Control

I/O Address HIU_RDT
Index 1000 (VIU_MCR1: VIU Master Control V1) 1001 (VIU_MCR2: VIU Master Control V2)

Registers VIU_MCR1 and VIU_MCR2 specify the functional and I/O characteristics of Video Port Interfaces 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STM	OFP	OSS		OVSP	OHSP	OBP	OBT	IFP	ISS	IVSP	IHSP	IBP	IBT	IOM	

Bit #	Access	Res	Description	
15	R/W	0	STM	Stall Mode (VIU_MCR2 only). 0 Disabled 1 Enabled
14	R/W	0	OFP	Output Video Field Polarity. 0 Normal polarity 1 Inverted polarity
13:12	R/W	00	OSS	Output Video Sync Source. 00 VnVS, VnHS, and VnBL input to DVP 01 VnVS, VnHS input to DVP; VnBL output from OPU 10 VnVS, VnHS, and VnBL output from VSU 11 VnVS, VnHS output from VSU, VnBL output from OPU
11	R/W	0	OVSP	Output Video Vertical Sync Polarity. Specifies VnVS polarity when output. 0 Active low 1 Active high
10	R/W	0	OHSP	Output Video Horizontal Sync Polarity. Specifies VnHS polarity when output. 0 Active low 1 Active high
9	R/W	0	OBP	Output Video Blank Polarity. Specifies VnBL polarity when output. 0 Active low 1 Active high
8	R/W	0	OBT	Output Video Blank Type. Specifies VnBL type when output. 0 Horizontal blank 1 Composite blank
7	R/W	0	IFP	Input Video Field Polarity. 0 Active low 1 Active high
6	R/W	0	ISS	Input Video Sync Source. 0 VnVS, VnHS, and VnBL input to DVP 1 VnVS, VnHS, and VnBL output from DVP
5	R/W	0	IVSP	Input Video Vertical Sync Polarity. Specifies VnVS polarity when input. 0 Active low 1 Active high
4	R/W	0	IHSP	Input Video Horizontal Sync Polarity. Specifies VnHS polarity when input. 0 Active low 1 Active high
3	R/W	0	IBP	Input Video Blank Polarity. Specifies VnBL polarity when input. 0 Active low 1 Active high
2	R/W	0	IBT	Input Video Blank Type. Specifies VnBL type when input. 0 Horizontal blank 1 Composite blank
1:0	R/W	00	IOM	V1/V2 Input/Output Mode. 00 Input only 01 Output only 10 Duplex, output on VnPH high 11 Duplex, output on VnPH low

4.2.1.2 VIU_DPCf: Datapath Control

POSTED
I/O Address HIU_RDT
Index 1002 (VIU_DPC1: Datapath Control, Field 1)
1003 (VIU_DPC2: Datapath Control, Field 2)

Registers VIU_DPC1 and VIU_DPC2 specify the flow of stream data and the source of control sync references for the IPU1, the IPU2, and the OPU for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				VSUDC			IPU1DC			IPU2DC			ODC		

Bit #	Access	Reset	Description	
15:12	R/W	0000	RSVD	Reserved (read as '0').
11:9	R/W	000	VSUDC	VSU Datapath Control 000 V1 sources clock 001 V1 sources clock, V1PH qualified 010 V2 sources clock 011 V2 sources clock, V2PH qualified 100 MCLK÷3 (sequencer clock) timebase 101 MCLK÷6 timebase XXX All other configurations reserved
8:6	R/W	000	IPU1DC	IPU1 Datapath Control. Specifies the source of control sync references and input stream data for the IPU1. 000 V1 sources sync and data 001 V1 sources sync and data, V1PH qualified 010 V2 sources sync and data 011 V2 sources sync and data, V2PH qualified 100 OPU sources data, MCLK÷3 HS timebase, VSU sources sync 101 OPU sources data, MCLK÷6 HS timebase, VSU sources sync XXX All other configurations reserved
5:3	R/W	000	IPU2DC	IPU2 Datapath Control. Specifies the source of control sync references and input stream data for the IPU2. 000 V1 sources sync and data 001 V1 sources sync and data, V1PH qualified 010 V2 sources sync and data 011 V2 sources sync and data, V2PH qualified 100 OPU sources data, MCLK÷3 HS timebase, VSU sources sync 101 OPU sources data, MCLK÷6 HS timebase, VSU sources sync 110 HIU sources data directly to FIFO F, no sync controls 111 Reserved

Bit #	Access	Reset	Description	
2:0	R/W	000	ODC	OPU Datapath Control. Specifies the source of control sync references and the destination of output stream data from the OPU. 000 V1 sources sync 001 V1 sources sync, V1PH qualified 010 V2 sources sync 011 V2 sources sync, V2PH qualified 100 VSU sources sync, MCLK+3 timebase 101 VSU sources sync, MCLK+6 timebase 110 HIU receives data directly from FIFO D, no sync controls 111 Reserved

4.2.1.3 VIU_WDT: Watchdog Timer

POSTED
I/O Address HIU_RDT
Index 1004

Register VIU_WDT controls watchdog timer operation, and specifies the field toggle mode of the SIU.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	MMS	MFTS			WTE	TMOUT									

Bit #	Access	Reset	Description	
15	R/W	0	RSVD	Reserved (read as '0').
14	R/W	0	MMS	Manual Mode Start. Writing 0, then 1 while MFTS is programmed to 6h initiates a field toggle in manual mode.
13:11	R/W	000	MFTS	Master Field Toggle Select. Specifies the field toggle mode for the SIU. The field toggles on the leading edge of vertical sync. 000 Field timing from V1VS input 001 Field timing from V1VS output 010 Field timing from V2VS input 011 Field timing from V2VS output 100 Field timing from watchdog timer 101 Field timing from VSU vertical sync 110 Field timing from manual mode start 111 Reserved
10	R/W	0	WTE	Watchdog Timer Enable. 0 Disable watchdog timer 1 Enable watchdog timer
9:0	R/W	0h	TMOUT	Timeout. Specifies the watchdog timer interval. The timebase interval is MCLK prescaled by a factor of 49,152 (3 * 214). (0-3FFh)

4.2.1.4 VIU_TEST: Test Register

I/O Address HIU_RDT
Index 1006

VIU_TEST is a read-only test register for diagnostic use and software debugging. It allows user to monitor conditions between IPU1, IPU2, OPU, and VIU.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MF	MFID	RSVD			OBIN	OVS	OHS	OBL	OFID	I2VS	I2BL	I2FID	I1VS	I1BL	I1FID

Bit #	Access	Reset	Description	
15	R	0	MF	Master Field. Specifies which SIU loop is being executed. 0 SIU_MCR, field SI1 1 SIU_MCR, field SI2
14	R	0	MFID	Master Field ID. Monitors the state of the VIU_WDT Master Field Toggle Select condition. Inverted from selected source field ID. For example, if V1 and IPU1 are selected, this bit is inverted from I1FID. See Section 4.2.1.3 on page 33.
13:11	R	000	RSVD	Reserved.
10	R	0	OBIN	Blank in from OPU based on the clipping values programmed into registers OPU_XBI1, OPU_XEI1, OPU_YBI1, and OPU_YEI1.
9	R	0	OVS	OPU Vertical Sync.
8	R	0	OHS	OPU Horizontal Sync.
7	R	0	OBL	OPU Blank.
6	R	0	OFID	OPU Field ID. Value depends on OPU field polarity (specified by OPU_MCRf, bit FPS).
5	R	0	I2VS	IPU2 Vertical Sync.
4	R	0	I2BL	IPU2 Blank.
3	R	0	I2FID	IPU2 Field ID. Value depends on IPU2 field polarity (specified by IPU2_MCRf, bit FPS).
2	R	0	I1VS	IPU1 Vertical Sync.
1	R	0	I1BL	IPU1 Blank.
0	R	0	I1FID	IPU1 Field ID. Value depends on IPU1 field polarity (specified by IPU1_MCRf, bit FPS).

4.2.2 VSU: Video Sync Unit

The following sections describe the VSU registers, shown in Figure 4-1 and Figure 4-2.

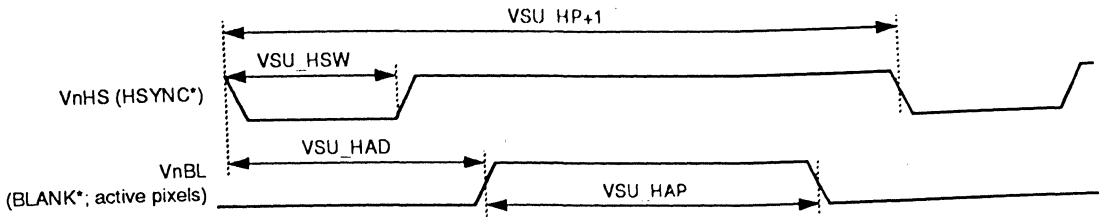


Figure 4-1. VSU Horizontal Sync Timing

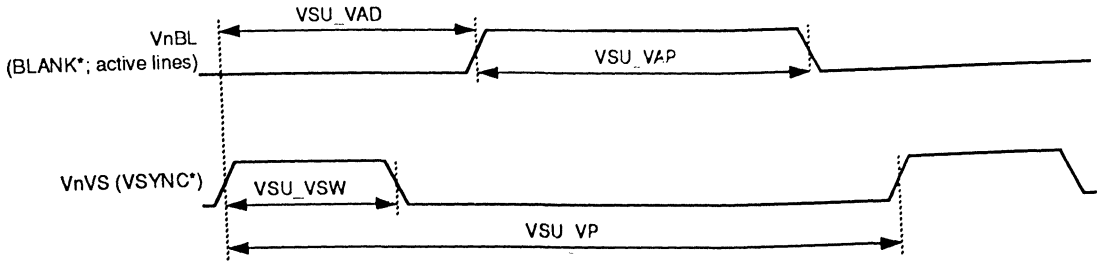


Figure 4-2. VSU Vertical Sync Timing

4.2.2.1 VSU_HSW: Horizontal Sync Width

POSTED
I/O Address HIU_RDT
Index 1100

Register VSU_HSW specifies the width of the horizontal sync pulse generated by the internal sync generator. The timebase is specified by registers VIU_DPCf, bits IPU1DC and IPU2DC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									HSW						

Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as '0').
6:0	R/W	0h	HSW	Horizontal Sync Width. (0-7Fh) (20h - 7Fh in loopback mode)

4.2.2.2 VSU_HAD: Horizontal Active Delay

POSTED
I/O Address HIU_RDT
Index 1101

Register VSU_HAD specifies the delay from the start of the horizontal sync pulse generated by the internal sync generator to the beginning of the horizontal active interval. The timebase is specified by VIU_DPCf, bits IPU1DC and IPU2DC. VSU_HAD must equal VSU_HSW+3 when OPU_MCRf, bit LSM = 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						HAD									

Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as '0').
9:0	R/W	0h	HAD	Horizontal Active Delay. (0-3FFh)

4.2.2.3 VSU_HAP: Horizontal Active Pixels

POSTED
I/O Address HIU_RDT
Index 1102

Register VSU_HAP specifies the width of the horizontal active interval generated by the internal sync generator. The timebase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified by VIU_DPCf, bits IPU1DC and IPU2DC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					HAP										

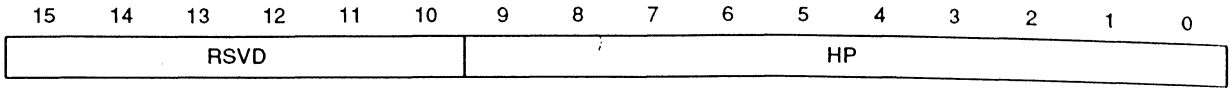
Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	HAP	Horizontal Active Pixels (0-3FFh)

4.2.2.4 VSU_HP: Horizontal Period

POSTED
I/O Address HIU_RDT
Index 1103

Register VSU_HP specifies the width of the horizontal sync period generated by the internal sync generator. The timebase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified by VIU_DPCf, bits IPU1DC and IPU2DC.

NOTE: The number entered in HP must be one less than the desired interval.

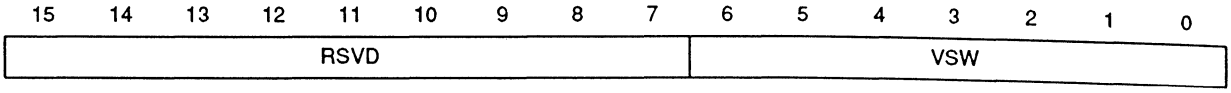


Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as '0').
9:0	R/W	0h	HP	Desired Horizontal Period = (0-3FFh) - 1

4.2.2.5 VSU_VSW: Vertical Sync Width

POSTED
I/O Address HIU_RDT
Index 1104

Register VSU_VSW specifies the width of the vertical sync pulse generated by the internal sync generator. The time-base is the horizontal sync interval specified by register VSU_HP.

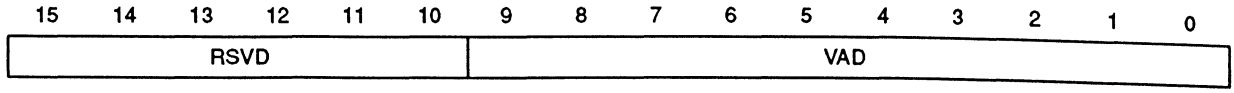


Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as '0').
6:0	R/W	0h	VSW	Vertical Sync Width (0-7Fh)

4.2.2.6 VSU_VAD: Vertical Active Delay

POSTED
I/O Address HIU_RDT
Index 1105

Register VSU_VAD specifies the delay from the start of the vertical sync pulse generated by the internal sync generator to the beginning of the vertical active interval. The timebase is the horizontal sync interval specified by register VSU_HP.



Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as '0').
9:0	R/W	0h	VAD	Vertical Active Delay. (0-3FFh)

4.2.2.7 VSU_VAP: Vertical Active Pixels

POSTED
I/O Address HIU_RDT
Index 1106

Register VSU_VAP specifies the width of the vertical active interval generated by the internal sync generator. The timebase is the horizontal sync interval specified by register VSU_HP.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					VAP										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	VAP	Vertical Active Pixels. (0-7FFh)

4.2.2.8 VSU_VP: Vertical Period

POSTED
I/O Address HIU_RDT
Index 1107

Register VSU_VP specifies the width of the vertical sync period generated by the internal sync generator. The timebase is the horizontal sync interval specified by register VSU_HP. This register also provides the enable and single sweep controls for the internal sync generator.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SGE	SSE	VFL	RSVD		VP										

Bit #	Access	Reset	Description	
15	R/W	0	SGE	Sync Generator Enable. (Enabled when SSE = 1.) 1 Another single sweep occurs (SGE resets to '0' at the end of the sweep)
14	R/W	0	SSE	Single Sweep Enable. Enables single sweep mode. 0 SGE ignored 1 SGE enabled
13	R/W	0	VFL	Video Field Lock. 0 No field lock 1 Field-locks (synchronizes) VSU to the incoming field of the video source selected as the master in register VIU_WDT, bit MFTS; allows an internal process that may run much faster to remain in sync with an incoming stream.
12	R/W	0000	RSVD	Reserved (read as '0').
9:0	R/W	0h	VP	Vertical Active Count. (0-7FFh)

4.3 VPU: Video Processor Unit

Name	Index	Definition	Posted?	Ref. Section
VPU Global Control				4.3.1, p. 44
VPU_MCR	2000	VPU Master Control	POSTED	4.3.1.1, p. 44
IPU1: Input Processor Unit 1				4.3.2, p. 45
IPU1_PIX	2100	Pixel Count	—	4.3.2.1, p. 45
IPU1_LIC	2101	Line Count	—	4.3.2.2, p. 45
IPU1_FLC	2102	Field Count	—	4.3.2.3, p. 46
IPU1_LIR	2103	Line Count Interrupt Request	—	4.3.2.4, p. 46
IPU1_FIR	2104	Field Count Interrupt Request	—	4.3.2.5, p. 46
IPU1_LRB	2200	LUT RAM Base Address	—	4.3.2.6, p. 47
IPU1_LRD	2201	LUT RAM Data	—	4.3.2.7, p. 47
IPU1_MCR1	3000	IPU1 Master Control, Field 1	POSTED	4.3.2.8, p. 48
IPU1_XBF1	3001	X Begin Fraction, Field 1	POSTED	4.3.2.9, p. 49
IPU1_XBI1	3002	X Begin Integer, Field 1	POSTED	4.3.2.9, p. 49
IPU1_XEI1	3003	X End Integer, Field 1	POSTED	4.3.2.10, p. 50
IPU1_XSF1	3004	X Shrink Fraction, Field 1	POSTED	4.3.2.11, p. 50
IPU1_XSI1	3005	X Shrink Integer, Field 1	POSTED	4.3.2.11, p. 50
IPU1_YBF1	3006	Y Begin Fraction, Field 1	POSTED	4.3.2.12, p. 51
IPU1_YBI1	3007	Y Begin Integer, Field 1	POSTED	4.3.2.12, p. 51
IPU1_YEI1	3008	Y End Integer, Field 1	POSTED	4.3.2.13, p. 51
IPU1_YSF1	3009	Y Shrink Fraction, Field 1	POSTED	4.3.2.14, p. 52
IPU1_YSI1	300a	Y Shrink Integer, Field 1	POSTED	4.3.2.14, p. 52
IPU1_KFC1	300b	Key Function Code, Field 1	POSTED	4.3.2.15, p. 52
IPU1_MMY1	300c	Chroma Key Y/R Max/Min, Field 1	POSTED	4.3.2.16, p. 53
IPU1_MMU1	300d	Chroma Key U/G Max/Min, Field 1	POSTED	4.3.2.16, p. 53
IPU1_MMV1	300e	Chroma Key V/B Max/Min, Field 1	POSTED	4.3.2.16, p. 53
IPU1_MCR2	3100	IPU1 Master Control, Field 2	POSTED	4.3.2.8, p. 48
IPU1_XBF2	3101	X Begin Fraction, Field 2	POSTED	4.3.2.9, p. 49
IPU1_XBI2	3102	X Begin Integer, Field 2	POSTED	4.3.2.9, p. 49

4.3 VPU: Video Processor Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
IPU1_XEI2	3103	X End Integer, Field 2	POSTED	4.3.2.10, p. 50
IPU1_XSF2	3104	X Shrink Fraction, Field 2	POSTED	4.3.2.11, p. 50
IPU1_XSI2	3105	X Shrink Integer, Field 2	POSTED	4.3.2.11, p. 50
IPU1_YBF2	3106	Y Begin Fraction, Field 2	POSTED	4.3.2.12, p. 51
IPU1_YBI2	3107	Y Begin Integer, Field 2	POSTED	4.3.2.12, p. 51
IPU1_YEI2	3108	Y End Integer, Field 2	POSTED	4.3.2.13, p. 51
IPU1_YSF2	3109	Y Shrink Fraction, Field 2	POSTED	4.3.2.14, p. 52
IPU1_YSI2	310a	Y Shrink Integer, Field 2	POSTED	4.3.2.14, p. 52
IPU1_KFC2	310b	Key Function Code, Field 2	POSTED	4.3.2.15, p. 52
IPU1_MMY2	310c	Chroma Key Y/R Max/Min, Field 2	POSTED	4.3.2.16, p. 53
IPU1_MMU2	310d	Chroma Key U/G Max/Min, Field 2	POSTED	4.3.2.16, p. 53
IPU1_MMV2	310e	Chroma Key V/B Max/Min, Field 2	POSTED	4.3.2.16, p. 53
IPU2: Input Processor Unit 2				4.3.3, p. 54
IPU2_PIX	2300	Pixel Count	—	4.3.3.1, p. 54
IPU2_LIC	2301	Line Count	—	4.3.3.2, p. 54
IPU2_FLC	2302	Field Count	—	4.3.3.3, p. 54
IPU2_LIR	2303	Line Count Interrupt Request	—	4.3.3.4, p. 55
IPU2_FIR	2304	Field Count Interrupt Request	—	4.3.3.5, p. 55
IPU2_MCR1	3200	IPU2 Master Control, Field 1	POSTED	4.3.3.6, p. 56
IPU2_XBI1	3202	X Begin Integer, Field 1	POSTED	4.3.3.7, p. 56
IPU2_XEI1	3203	X End Integer, Field 1	POSTED	4.3.3.8, p. 57
IPU2_YBI1	3207	Y Begin Integer, Field 1	POSTED	4.3.3.9, p. 57
IPU2_YEI1	3208	Y End Integer, Field 1	POSTED	4.3.3.10, p. 58
IPU2_MCR2	3300	IPU2 Master Control, Field 2	POSTED	4.3.3.6, p. 56
IPU2_XBI2	3302	X Begin Integer, Field 2	POSTED	4.3.3.7, p. 56
IPU2_XEI2	3303	X End Integer, Field 2	POSTED	4.3.3.8, p. 57
IPU2_YBI2	3307	Y Begin Integer, Field 2	POSTED	4.3.3.9, p. 57
IPU2_YEI2	3308	Y End Integer, Field 2	POSTED	4.3.3.10, p. 58

4.3 VPU: Video Processor Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
SIU: Sequencer Instruction Unit			—	4.3.4, p. 58
SIU_MCR	2800	SIU Master Control	—	4.3.4.1, p. 58
SIU_FCS	2801	FIFO Control/Status	—	4.3.4.2, p. 59
SIU_FOU	2802	FIFO Overflow/Underflow	—	4.3.4.3, p. 60
SIU_FAR	4001	FIFO Auto Reset	—	4.3.4.5, p. 62
SIU0_SIM	2e00	Sequencer Instruction Memory 0	—	4.3.4.4, p. 61
SIU1_SIM	2e01	Sequencer Instruction Memory 1	—	4.3.4.4, p. 61
SIU2_SIM	2e02	Sequencer Instruction Memory 2	—	4.3.4.4, p. 61
SIU3_SIM	2e03	Sequencer Instruction Memory 3	—	4.3.4.4, p. 61
SIU4_SIM	2e04	Sequencer Instruction Memory 4	—	4.3.4.4, p. 61
SIU5_SIM	2e05	Sequencer Instruction Memory 5	—	4.3.4.4, p. 61
SIU6_SIM	2e06	Sequencer Instruction Memory 6	—	4.3.4.4, p. 61
SIU7_SIM	2e07	Sequencer Instruction Memory 7	—	4.3.4.4, p. 61
SIU8_SIM	2e08	Sequencer Instruction Memory 8	—	4.3.4.4, p. 61
SIU9_SIM	2e09	Sequencer Instruction Memory 9	—	4.3.4.4, p. 61
SIU10_SIM	2e0a	Sequencer Instruction Memory 10	—	4.3.4.4, p. 61
SIU11_SIM	2e0b	Sequencer Instruction Memory 11	—	4.3.4.4, p. 61
SIU12_SIM	2e0c	Sequencer Instruction Memory 12	—	4.3.4.4, p. 61
SIU13_SIM	2e0d	Sequencer Instruction Memory 13	—	4.3.4.4, p. 61
SIU14_SIM	2e0e	Sequencer Instruction Memory 14	—	4.3.4.4, p. 61
SIU15_SIM	2e0f	Sequencer Instruction Memory 15	—	4.3.4.4, p. 61
SIU16_SIM	2e10	Sequencer Instruction Memory 16	—	4.3.4.4, p. 61
SIU17_SIM	2e11	Sequencer Instruction Memory 17	—	4.3.4.4, p. 61
SIU18_SIM	2e12	Sequencer Instruction Memory 18	—	4.3.4.4, p. 61
SIU19_SIM	2e13	Sequencer Instruction Memory 19	—	4.3.4.4, p. 61
SIU20_SIM	2e14	Sequencer Instruction Memory 20	—	4.3.4.4, p. 61
SIU21_SIM	2e15	Sequencer Instruction Memory 21	—	4.3.4.4, p. 61
SIU22_SIM	2e16	Sequencer Instruction Memory 22	—	4.3.4.4, p. 61
SIU23_SIM	2e17	Sequencer Instruction Memory 23	—	4.3.4.4, p. 61

4.3 VPU: Video Processor Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
SIU24_SIM	2e18	Sequencer Instruction Memory 24	—	4.3.4.4, p. 61
SIU25_SIM	2e19	Sequencer Instruction Memory 25	—	4.3.4.4, p. 61
SIU26_SIM	2e1a	Sequencer Instruction Memory 26	—	4.3.4.4, p. 61
SIU27_SIM	2e1b	Sequencer Instruction Memory 27	—	4.3.4.4, p. 61
SIU28_SIM	2e1c	Sequencer Instruction Memory 28	—	4.3.4.4, p. 61
SIU29_SIM	2e1d	Sequencer Instruction Memory 29	—	4.3.4.4, p. 61
SIU30_SIM	2e1e	Sequencer Instruction Memory 30	—	4.3.4.4, p. 61
SIU31_SIM	2e1f	Sequencer Instruction Memory 31	—	4.3.4.4, p. 61
ALU: Arithmetic and Logic Unit				4.3.4.5, p. 62
ALU_MCR1	2900	ALU Master Control, Field 1	POSTED	4.3.5.1, p. 62
ALU_MCR2	2901	ALU Master Control, Field 2	POSTED	4.3.5.1, p. 62
ALU_TOP	2902	Tag Operation	POSTED	4.3.5.2, p. 64
ALU_AV	2903	Alpha Value	POSTED	4.3.5.3, p. 64
ALU_LOPY	2904	Logic Operation Channel Y	POSTED	4.3.5.4, p. 65
ALU_LOPU	2905	Logic Operation Channel U	POSTED	4.3.5.4, p. 65
ALU_LOPV	2906	Logic Operation Channel V	POSTED	4.3.5.4, p. 65
ALU_CAY	2907	Constant A, Channel Y	POSTED	4.3.5.5, p. 65
ALU_CAU	2908	Constant A, Channel U	POSTED	4.3.5.5, p. 65
ALU_CAV	2909	Constant A, Channel V	POSTED	4.3.5.5, p. 65
ALU_CBY	290a	Constant B, Channel Y	POSTED	4.3.5.6, p. 66
ALU_CBU	290b	Constant B, Channel U	POSTED	4.3.5.6, p. 66
ALU_CBV	290c	Constant B, Channel V	POSTED	4.3.5.6, p. 66
ALU_CCY	290d	Constant C, Channel Y	POSTED	4.3.5.7, p. 66
ALU_CCU	290e	Constant C, Channel U	POSTED	4.3.5.7, p. 66
ALU_CCV	290f	Constant C, Channel V	POSTED	4.3.5.7, p. 66

4.3 VPU: Video Processor Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
OPU: Output Processing Unit				4.3.6, p. 67
OPU_MCR1	2a00	OPU Master Control, Field 1	POSTED	4.3.6.1, p. 67
OPU_XBI1	2a02	X Begin Integer, Field 1	POSTED	4.3.6.2, p. 68
OPU_XEI1	2a03	X End Integer, Field 1	POSTED	4.3.6.3, p. 68
OPU_YBI1	2a07	Y Begin Integer, Field 1	POSTED	4.3.6.4, p. 69
OPU_YEI1	2a08	Y End Integer, Field 1	POSTED	4.3.6.5, p. 69
OPU_MCR2	2b00	OPU Master Control, Field 2	POSTED	4.3.6.1, p. 67
OPU_XBI2	2b02	X Begin Integer, Field 2	POSTED	4.3.6.2, p. 68
OPU_XEI2	2b03	X End Integer, Field 2	POSTED	4.3.6.3, p. 68
OPU_YBI2	2b07	Y Begin Integer, Field 2	POSTED	4.3.6.4, p. 69
OPU_YEI2	2b08	Y End Integer, Field 2	POSTED	4.3.6.5, p. 69

4.3.1 VPU Global Control

4.3.1.1 VPU_MCR: VPU Master Control

POSTED
I/O Address HIU_RDT
Index 2000

Register VPU_MCR controls the operation of the IPU1, the IPU2, and the OPU for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			ALUE	OPFSS				IP2FSS				IP1FSS			

Bit #	Access	Reset	Description	
15:13	R/W	0h	RSVD	Reserved (read as '0').
12	R/W	0	ALUE	ALU Enable. 0 Disable ALU operation 1 Enable ALU operation
11:8	R/W	0000	OPFSS	OPU Field Sync Select. Enables OPU operation, specifies field synchronization and processing. 0000 Disable OPU operation 0001 Start OPU on next field, both fields processed 0010 Start OPU on field 1, single field processed 0011 Start OPU on field 1, both fields processed 0100 Start OPU on field 2, single field processed 0101 Start OPU on field 2, both fields processed
7:4	R/W	0000	IP2FSS	IPU2 Field Sync Select. Enables IPU2 operation, specifies field synchronization and processing. 0000 Disable IPU2 operation 0001 Start IPU2 on next field, both fields processed 0010 Start IPU2 on field 1, single field processed 0011 Start IPU2 on field 1, both fields processed 0100 Start IPU2 on field 2, single field processed 0101 Start IPU2 on field 2, both fields processed
3:0	R/W	0000	IP1FSS	IPU1 Field Sync Select. Enables IPU1 operation, specifies field synchronization and processing. 0000 Disable IPU1 operation 0001 Start IPU1 on next field, both fields processed 0010 Start IPU1 on field 1, single field processed 0011 Start IPU1 on field 1, both fields processed 0100 Start IPU1 on field 2, single field processed 0101 Start IPU1 on field 2, both fields processed

4.3.2 IPU1: Input Processor Unit 1

4.3.2.1 IPU1_PIX: Pixel Count

I/O Address HIU_RDT
Index 2100

Register IPU1_PIX is a read-only register that reads back the value of the current 11-bit pixel counter.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					PC										

Bit #	Access	Reset	Description	
15:11	R	0h	RSVD	Reserved (read as '0').
10:0	R	0h	PC	Pixel Count current line. Automatically resets to '0' at the beginning of each line. (0-7FFh)

4.3.2.2 IPU1_LIC: Line Count

I/O Address HIU_RDT
Index 2101

Register IPU1_LIC is a read-only register of the current 11-bit line count.

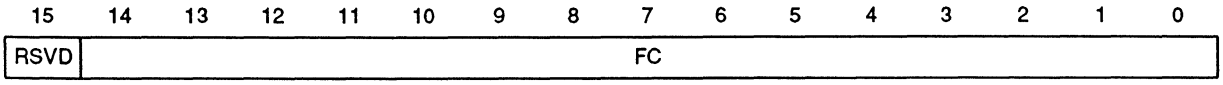
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					LC										

Bit #	Access	Reset	Description	
15:11	R	0h	RSVD	Reserved (read as '0').
10:0	R	0h	LC	Line Count current field. Automatically resets to '0' at the beginning of each field. (0-7FFh)

4.3.2.3 IPU1_FLC: Field Count

I/O Address HIU_RDT
Index 2102

Register IPU1_FLC returns the current 15-bit field count on read.

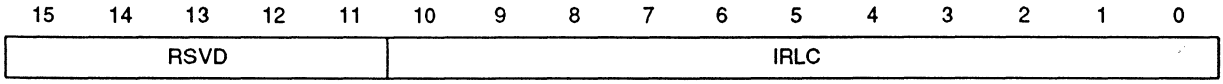


Bit #	Access	Reset	Description	
15	R	0h	RSVD	Reserved (read as '0').
14:0	R	0h	FC	Field Count. Resets to '0' when IPU1_FIR, bit FCE = '0.'

4.3.2.4 IPU1_LIR: Line Count Interrupt Request

I/O Address HIU_RDT
Index 2103

Register IPU1_LIR generates an interrupt request when the 11-bit value in field IRLC is equal to the value in IPU1_LIC, bit LC.

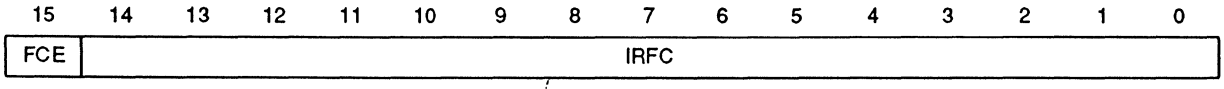


Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	IRLC	Interrupt Request Line Count (0-7FFh)

4.3.2.5 IPU1_FIR: Field Count Interrupt Request

I/O Address HIU_RDT
Index 2104

Register IPU1_FIR generates an interrupt request when the 15-bit value in field IRFC is equal to the value in IPU1_FLC, field FC.

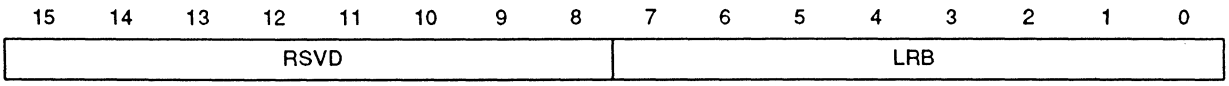


Bit #	Access	Reset	Description	
15	R/W	0h	FCE	Field Count Enable. 0 Disable field count 1 Enable field count
14:0	R/W	0h	IRFC	Interrupt Request Field Count.

4.3.2.6 IPU1_LRB: LUT RAM Base Address

I/O Address HIU_RDT
Index 2200

Register IPU1_LRB preloads the 8-bit LUT RAM address counter and initializes the channel pointer to the YR channel. The channel pointer automatically advances to the next channel after each LUT RAM access, and address counter automatically increments after accessing the CrB channel. LUT RAM elements are accessed in the following order: YR[LRB+0], CbG[LRB+0], CrB[LRB+0], YR[LRB+1], CbG[LRB+1], CrB[LRB+1], etc.

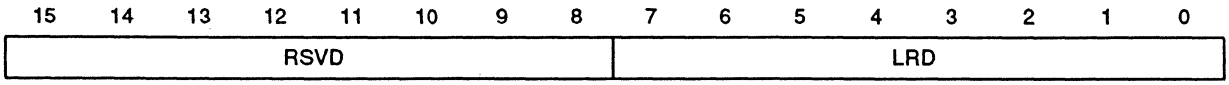


Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as '0').
7:0	R/W	0h	LRB	LUT RAM Base Address. Specifies the 8-bit address generator preload value. (0-FFh)

4.3.2.7 IPU1_LRD: LUT RAM Data

I/O Address HIU_RDT
Index 2201

Register IPU1_LRD is the bidirectional data port to the storage elements of the three-channel LUT RAM.



Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as '0').
7:0	R/W	0h	LRD	LUT RAM Data. Data written to this field transfers to the current LUT RAM element (R, G, B); data to be read from the current LUT RAM element appears in this field. (0-FFh)

4.3.2.8 IPU1_MCRf: IPU1 Master Control

POSTED
I/O Address Index HIU_RDT
3000 (IPU1_MCR1: IPU1 Master Control, Field 1)
3100 (IPU1_MCR2: IPU1 Master Control, Field 2)

Registers IPU1_MCR1 and IPU1_MCR2 control the operation of the IPU1 for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FPS	IM	PSE	CSCE	LE	YSP	ODT		OF				IF			

Bit #	Access	Reset	Description	
15	R/W	0	FPS	Field Polarity Select. Controls the polarity of the field ID signal supplied to the Window Clipping and XY Scaler. 0 Normal polarity 1 Invert polarity
14	R/W	0	IM	Interlace Mode. Specifies the input stream as interlaced or progressive-scan (non-interlaced) data. 0 Progressive-scan input 1 Interlaced input
13	R/W	0	PSE	X Prescaler Enable. 0 Bypass prescaler 1 Enable 0.5x prescaler
12	R/W	0	CSCE	Color Space Converter Enable. 0 Bypass Color Space Converter 1 Enable Color Space Converter
11	R/W	0	LE	LUT Enable. 0 Bypass LUT RAM 1 Enable LUT RAM
10	R/W	0	YSP	Y Scaling Path. Enables or disables the special Y Scaling Path Mode. 0 Enable IPU1 Y scaling 1 Disable IPU1 Y scaling (ALU performs Y scaling)
9:8	R/W	00	ODT	Output Data Tag. Controls input selection of Input Tag Unit tag mux. 00 Pass tag unchanged 01 Set tag to field ID 10 Set tag to inverse chroma key tag 11 Set tag to chroma key tag
7:4	R/W	0000	OF	Output Data Stream Format. 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 1:5:5:5 tagged data 1010 RGB 8:8:8 non-tagged data 1011 RGB 1:8:8:8 tagged data 1110 RGB 3:3:2 non-tagged data XXXX All other configurations reserved

Bit #	Access	Reset	Description	
3:0	R/W	0000	IF	Input Data Stream Format. 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 0010 YCbCr 4:1:1 non-tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 1:5:5:5 tagged data 1110 Pseudo color (indirect color mapping via IPU1 LUT) XXXX All other configurations reserved

4.3.2.9 IPU1_XBnf: X Begin

POSTED
I/O Address HIU_RDT
Index 3001 (IPU1_XBF1: X Begin Fraction, Field 1) 3101 (IPU1_XBF2: X Begin Fraction, Field 2)
3002 (IPU1_XBI1: X Begin Integer, Field 1) 3102 (IPU1_XBI2: X End Integer, Field 2)

Registers IPU1_XBnf specify the 11.3 format X begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BF			RSVD												
RSVD											BI				

Bit #	Access	Reset	Description	
IPU1_XBFf: X Begin Fraction Index				
15:13	R/W	0h	BF	Begin X Column Fractional Index. Specifies the 3-bit fractional portion of the 11.3 format X begin value. Allows the virtual left boundary of the post-scaled window to be aligned between pixels of the pre-scaled window for fields 1 and 2. (0-7h)
12:0	R/W	0h	RSVD	Reserved (read as '0').
IPU1_XEIf: X Begin Integer Index				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin X Column Integer Index. Specifies the 11-bit integer portion of the 11.3 format X begin value. Defines the left boundary of the pre-scaling window for fields 1 and 2. All video to the left of this boundary is clipped and is not used to generate the scaled window. (0-7FFh)

4.3.2.10 IPU1_XEIf: X End

POSTED
I/O Address HIU_RDT
Index 3003 (IPU1_XEI1: X End Integer, Field 1)
3103 (IPU1_XEI2: X End Integer, Field 2)

Registers IPU1_XEI1 and IPU1_XEI2 specify the 11-bit X end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	X End Column Integer Index. Specifies the 11-bit X end value. (0-7FFh)

4.3.2.11 IPU1_XSnf: X Shrink

POSTED
I/O Address HIU_RDT
Index 3004 (IPU1_XSF1: X Shrink Fraction, Field 1)
3005 (IPU1_XSI1: X Shrink Integer, Field 1)
3104 (IPU1_XSF2: X Shrink Fraction, Field 2)
3105 (IPU1_XSI2: X Shrink Integer, Field 2)

Registers IPU1_XSnf specify the 6.10 format X shrink value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF										RSVD					
RSVD										SI					

Bit #	Access	Reset	Description	
IPU1_XSFf: X Shrink Fraction				
15:5	R/W	0h	SF	X Shrink Fraction. Specifies the 10-bit fractional portion of the 6.10 format X shrink value. (0-3FFh)
4:0	R/W	0h	RSVD	Reserved (read as '0').
IPU1_XSIf: X Shrink Integer				
15:6	R/W	0h	RSVD	Reserved (read as '0').
5:0	R/W	0h	SI	X Shrink Integer. Specifies the 4-bit integer portion of the 4.10 format X shrink value. (0-Fh)

4.3.2.12 IPU1_YBnf: Y Begin

POSTED
I/O Address HIU_RDT
Index 3006 (IPU1_YBF1: Y Begin Fraction, Field 1) 3106 (IPU1_YBF2: Y Begin Fraction, Field 2)
3007 (IPU1_YBI1: Y Begin Integer, Field 1) 3107 (IPU1_YBI2: Y Begin Integer, Field 2)

Registers IPU1_YBnf specify the 11.3 format Y begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BF			RSVD												
RSVD					BI										

Bit #	Access	Reset	Description	
IPU1_YBFf: Y Begin Fraction Index				
15:13	R/W	0h	BF	Begin Y Row Fractional Index. Specifies the 3-bit fractional portion of the 11.3 format Y begin value. Allows the virtual top row of the post-scaled window to be aligned between rows of the pre-scaled window for fields 1 and 2. (0-7h)
12:0	R/W	0h	RSVD	Reserved (read as '0').
IPU1_YBIf: Y Begin Integer Index				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin Y Row Integer Index. Specifies the 11-bit integer portion of the 11.3 format Y begin value. Defines the top edge of the pre-scaling window for fields 1 and 2. All video above this boundary is clipped and does not become part of the scaled window. (0-7FFh)

4.3.2.13 IPU1_YEIf: Y End

POSTED
I/O Address HIU_RDT
Index 3008 (IPU1_YEI1: Y End Integer, Field 1) 3108 (IPU1_YEI2: Y End Integer, Field 2)

Registers IPU1_YEI1 and IPU1_YEI2 specify the 11-bit Y end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	End Y Row Integer Index. Specifies the 11-bit Y end value. (0-7FFh)

4.3.2.14 IPU1_YSnf: Y Shrink

POSTED
I/O Address HIU_RDT
Index 3009 (IPU1_YSF1: Y Shrink Fraction, Field 1) 3109 (IPU1_YSF2: Y Shrink Fraction, Field 2)
300a (IPU1_YSI1: Y Shrink Integer, Field 1) 310a (IPU1_YSI2: Y Shrink Integer, Field 2)

Registers IPU1_YSnf specify the 4.10 format Y shrink value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF										RSVD					
RSVD										SI					

Bit #	Access	Reset	Description	
IPU1_YSFf: Y Shrink Fraction				
15:6	R/W	0h	SF	Y Shrink Fraction. Specifies the 10-bit fractional portion of the 4.10 format Y shrink value. (0-3FFh)
5:0	R/W	0h	RSVD	Reserved (read as '0').
IPU1_YSIf: Y Shrink Integer				
15:6	R/W	0h	RSVD	Reserved (read as '0').
5:0	R/W	0h	SI	Y Shrink Integer. Specifies the 4-bit integer portion of the 4.10 format Y shrink value. (0-Fh)

4.3.2.15 IPU1_KFCf: Key Function Code

POSTED
I/O Address HIU_RDT
Index 300b (IPU1_KFC1: Key Function Code, Field 1) 310b (IPU1_KFC2: Key Function Code, Field 2)

Registers IPU1_KFC1 and IPU1_KFC2 specify the tag values used by the key function code multiplexers for fields 1 and 2 in the tag unit, allowing a match on any combination of YUV to trigger a tag.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								KEYFC							

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as '0').
7:0	R/W	0h	KEYFC	Key Function Code. Specifies eight 1-bit input tag values used by the key function code multiplexers. (1 = match, or within range.) (0-FFh) *YUV* *YUV* *YUV* *YUV* 000 = KEYFC0 010 = KEYFC2 100 = KEYFC4 110 = KEYFC6 001 = KEYFC1 011 = KEYFC3 101 = KEYFC5 111 = KEYFC7

4.3.2.16 IPU1_MMxf: Chroma Key Max/Min

POSTED
I/O Address HIU_RDT
Index 300c (IPU1_MMY1: Chroma Key Y/R Max/Min, Field 1)
300d (IPU1_MMU1: Chroma Key U/G Max/Min, Field 1)
300e (IPU1_MMV1: Chroma Key V/B Max/Min, Field 1)
310c (IPU1_MMY2: Chroma Key Y/R Max/Min, Field 2)
310d (IPU1_MMU2: Chroma Key U/G Max/Min, Field 2)
310e (IPU1_MMV2: Chroma Key V/B Max/Min, Field 2)

Registers IPU1_MMxf specify the maximum and minimum 8-bit chroma key comparator values used by the Input Tag Unit for fields 1 and 2. These values are used for each of three 8-bit input channels for both fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YRMAX								YRMIN							
UGMAX								UGMIN							
VBMAX								VBMIN							

Bit #	Access	Reset		Description
IPU1_MMYf: Key Y/R Maximum/Minimum				
15:8	R/W	0h	YRMAX	Key Y/R Maximum. Specifies the upper threshold for the 8-bit Y/R channel comparator. (0-FFh)
7:0	R/W	0h	YRMIN	Key Y/R Minimum. Specifies the lower threshold for the 8-bit Y/R channel channel comparator. (0-FFh)
IPU1_MMUf: Key U/G Maximum/Minimum				
15:8	R/W	0h	UGMAX	Key U/G Maximum. Specifies the upper threshold for the 8-bit Cb/G channel comparator. (0-FFh)
7:0	R/W	0h	UGMIN	Key U/G Minimum. Specifies the lower threshold for the 8-bit Cb/G channel comparator. (0-FFh)
IPU1_MMVf: Key V/B Maximum/Minimum				
15:8	R/W	0h	VBMAX	Key V/B Maximum. Specifies the upper threshold for the 8-bit Cr/B channel comparator. (0-FFh)
7:0	R/W	0h	VBMIN	Key V/B Minimum. Specifies the lower threshold for the 8-bit Cr/B channel comparator. (0-FFh)

4.3.3 IPU2: Input Processing Unit 2

4.3.3.1 IPU2_PIX: Pixel Count

I/O Address HIU_RDT
Index 2300

Register IPU2_PIX is a read-only register that specifies the current 11-bit pixel count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					PC										

Bit #	Access	Reset	Description	
15:11	R	0h	RSVD	Reserved (read as '0').
10:0	R	0h	PC	Pixel Count current line. Automatically resets to '0' at the beginning of each line. (0-7FFh)

4.3.3.2 IPU2_LIC: Line Count

I/O Address HIU_RDT
Index 2301

Register IPU2_LIC is a read-only register that specifies the current 11-bit line count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					LC										

Bit #	Access	Reset	Description	
14:11	R	0h	RSVD	Reserved (read as '0').
10:0	R	0h	LC	Line Count current field. Automatically resets to '0' at the beginning of each field. (0-7FFh)

4.3.3.3 IPU2_FLC: Field Count

I/O Address HIU_RDT
Index 2302

Read-only register IPU2_FLC returns the current 15-bit field count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	FC														

Bit #	Access	Reset	Description	
15	R	0h	RSVD	Reserved (read as '0').
14:0	R	0h	FC	Field count.

4.3.3.4 IPU2_LIR: Line Count Interrupt Request

I/O Address HIU_RDT
Index 2303

Register IPU2_LIR specifies an 11-bit line count value that generates an interrupt request when equal to the realtime line count value in register IPU2_LIC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					IRLC										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	IRLC	Interrupt Request Line Count. (0-7FFh)

4.3.3.5 IPU2_FIR: Field Count Interrupt Request

I/O Address HIU_RDT
Index 2304

Register IPU2_FIR specifies a 16-bit field count value that generates an interrupt request when equal to the realtime field count value in register IPU2_FLC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FCE	IRFC														

Bit #	Access	Reset	Description	
15	R/W	0	FCE	Field Count Enable. 1 Enable field count 0 Disable field count
14:0	R/W	0h	IRFC	Interrupt Request Field Count.

4.3.3.6 IPU2_MCRf: IPU2 Master Control

POSTED
I/O Address HIU_RDT
Index 3200 (IPU2_MCR1: IPU2 Master Control, Field 1)
3300 (IPU2_MCR2: IPU2 Master Control, Field 2)

Registers IPU2_MCR1 and IPU2_MCR2 control the operation of the IPU2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FPS	IM	PSE	RSVD												

Bit #	Access	Reset	Description	
15	R/W	0h	FPS	Field Polarity Select. Controls the polarity of the field ID signal supplied to the XY Window Clipping subunit. 0 Normal polarity 1 Invert polarity
14	R/W	0h	IM	Interlace Mode. Specifies the input stream as interlaced or non-interlaced (progressive-scan) data. 0 Progressive-scan input 1 Interlaced input
13	R/W	0h	PSE	Prescaler Enable. Enables or disables the operation of the Prescaler. 0 Bypass Prescaler 1 Enable 0.5x Prescaler
12:0	R/W	0h	RSVD	Reserved (read as '0').

4.3.3.7 IPU2_XBIf: X Begin

POSTED
I/O Address HIU_RDT
Index 3202 (IPU2_XBI1: X Begin Integer, Field 1)
3302 (IPU2_XBI2: X Begin Integer, Field 2)

Registers IPU2_XBI1 and IPU2_XBI2 specify the 11-bit X begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					BI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin X Column Integer Index. Specifies the 11-bit integer portion of the 11.0 format X begin value. (0-7FFh)

4.3.3.8 IPU2_XEI1: X End

POSTED
I/O Address HIU_RDT
Index 3203 (IPU2_XEI1: X End Integer, Field 1)
3303 (IPU2_XEI2: X End Integer, Field 2)

Registers IPU2_XEI1 and IPU2_XEI2 specify the 11-bit X end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	End X Column Integer Index. Specifies the 11-bit X end value. (0-7FFh)

4.3.3.9 IPU2_YBIf: Y Begin

POSTED
I/O Address HIU_RDT
Index 3207 (IPU2_YBI1: Y Begin Integer, Field 1)
3307 (IPU2_YBI2: Y Begin Integer, Field 2)

Registers IPU2_YBI1 and IPU2_YBI2 specify the 11-bit Y begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					BI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin Y Row Integer Index. Specifies the 11-bit integer portion of the 11-bit Y begin value. (0-7FFh)

4.3.3.10 IPU2_YEIf: Y End

POSTED
I/O Address HIU_RDT
Index 3208 (IPU2_YEI1: Y End Integer, Field 1)
3308 (IPU2_YEI2: Y End Integer, Field 2)

Registers IPU2_YEI1 and IPU2_YEI2 specify the 11-bit Y end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	End Y Row Integer Index. Specifies the 11-bit Y end value. (0-7FFh)

4.3.4 SIU: Sequencer Instruction Unit

4.3.4.1 SIU_MCR: SIU Master Control

I/O Address HIU_RDT
Index 2800

Register SIU_MCR controls the operation of the SIU for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		SE		FT		SI2					SI1				

Bit #	Access	Reset	Description	
15:14	R/W	0h	RSVD	Reserved (read as '0').
13:12	R/W	00	SE	Sequencer Enable. Enables the operation of the SIU. 00 SIU disabled 10 SIU enabled, start on SI1 11 SIU enabled, start on SI2
11:10	R/W	00	FT	Field Toggle. Specifies the field toggle mode and the association of the start index values to a field. 00 No field toggle 01 SI1 and SI2 toggle on vertical sync; no field association 10 Field 1 associated to SI1, fields 1 and 2 toggle on vertical sync 11 Field 1 associated to SI2, fields 1 and 2 toggle on vertical sync
9:5	R/W	0h	SI2	Start Index 2. Specifies the 5-bit sequencer instruction Start Index 2. (0-1Fh)
4:0	R/W	0h	SI1	Start Index 1. Specifies the 5-bit sequencer instruction Start Index 1. (0-1Fh)

4.3.4.2 SIU_FCS: FIFO Control/Status

I/O Address HIU_RDT
Index 2801

Register SIU_FCS is a special read/write register that provides realtime access to the full and empty flags from FIFOs A-G. All flags are active high.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		FGF	FGE	FFF	FFE	FEF	FEE	FDF	FDE	FCF	FCE	FBF	FBE	FAF	FAE

Bit #	Access	Reset	Description	
15:14	R/W	0h	RSVD	Reserved (read as '0').
13	R	0h	FGF	FIFO G Full Flag
12	R/W	0h	FGE	FIFO G Empty Flag
11	R	0h	FFF	FIFO F Full Flag
10	R/W	0h	FFE	FIFO F Empty Flag
9	R	0h	FEF	FIFO E Full Flag
8	R/W	0h	FEE	FIFO E Empty Flag
7	R	0h	FDF	FIFO D Full Flag
6	R/W	0h	FDE	FIFO D Empty Flag
5	R	0h	FCF	FIFO C Full Flag
4	R/W	0h	FCE	FIFO C Empty Flag
3	R	0h	FBF	FIFO B Full Flag
2	R/W	0h	FBE	FIFO B Empty Flag
1	R	0h	FAF	FIFO A Full Flag
0	R/W	0h	FAE	FIFO A Empty Flag

For all FIFO Full flags (odd bits 13:1):
0 Enables FIFO
1 Resets FIFO

For all FIFO Empty flags (even bits 12:0):
1 FIFO is empty

4.3.4.3 SIU_FOU: FIFO Overflow/Underflow

I/O Address HIU_RDT
Index 2802

Register SIU_FOU is a read-only register that provides realtime access to the overflow and underflow flags from FIFOs A-G.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		FGO	FGU	FFO	FFU	FEO	FEU	FDO	FDU	FCO	FCU	FBO	FBU	FAO	FAU

Bit #	Access	Reset	Description	
15:14	R	0h	RSVD	Reserved (read as '0').
13	R	0h	FGO	FIFO G Overflow Flag
12	R	0h	FGU	FIFO G Underflow Flag
11	R	0h	FFO	FIFO F Overflow Flag
10	R	0h	FFU	FIFO F Underflow Flag
9	R	0h	FEO	FIFO E Overflow Flag
8	R	0h	FEU	FIFO E Underflow Flag
7	R	0h	FDO	FIFO D Overflow Flag
6	R	0h	FDU	FIFO D Underflow Flag
5	R	0h	FCO	FIFO C Overflow Flag
4	R	0h	FCU	FIFO C Underflow Flag
3	R	0h	FBO	FIFO B Overflow Flag
2	R	0h	FBU	FIFO B Underflow Flag
1	R	0h	FAO	FIFO A Overflow Flag
0	R	0h	FAU	FIFO A Underflow Flag

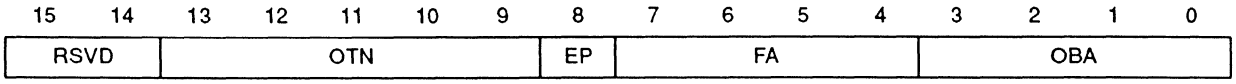
For all FIFO Overflow flags (odd bits 13:1):
0 Resets FIFO
1 FIFO overflow

For all FIFO Underflow flags (even bits 12:0):
0 Resets FIFO
1 FIFO underflow

4.3.4.4 SIUs_SIM: Sequencer Instruction Memory

I/O Address	HIU_RDT			
Index	2e00 (SIU0_SIM)	2e08 (SIU8_SIM)	2e10 (SIU16_SIM)	2e18 (SIU24_SIM)
	2e01 (SIU1_SIM)	2e09 (SIU9_SIM)	2e11 (SIU17_SIM)	2e19 (SIU25_SIM)
	2e02 (SIU2_SIM)	2e0a (SIU10_SIM)	2e12 (SIU18_SIM)	2e1a (SIU26_SIM)
	2e03 (SIU3_SIM)	2e0b (SIU11_SIM)	2e13 (SIU19_SIM)	2e1b (SIU27_SIM)
	2e04 (SIU4_SIM)	2e0c (SIU12_SIM)	2e14 (SIU20_SIM)	2e1c (SIU28_SIM)
	2e05 (SIU5_SIM)	2e0d (SIU13_SIM)	2e15 (SIU21_SIM)	2e1d (SIU29_SIM)
	2e06 (SIU6_SIM)	2e0e (SIU14_SIM)	2e16 (SIU22_SIM)	2e1e (SIU30_SIM)
	2e07 (SIU7_SIM)	2e0f (SIU15_SIM)	2e17 (SIU23_SIM)	2e1f (SIU31_SIM)

The 32 identical registers SIUs_SIM store the instruction sequence for fields 1 and 2.



Bit #	Access	Reset	Description	
15:14	R/W	0h	RSVD	Reserved (read as '0').
13:9	R/W	0h	OTN	Offset to Next Instruction. Specifies the signed, 5-bit displacement to the next instruction to execute. (0-1Fh)
8	R/W	0	EP	Exit Point. Identifies the current instruction as the exit point when the field toggle condition is detected. 0 Normal fall-through instruction 1 Exit point instruction
7:4	R/W	0000	FA	FIFO Association. Associates a FIFO with the current instruction. 0000 FIFO G 0001 FIFO F 0010 FIFO E 0011 FIFO A 0100 FIFO B 0101 FIFO C 0110 FIFO D XXXX All other configurations reserved
3:0	R/W	0000	OBA	Object Buffer Association. Associates an object buffer with the current instruction (see field FA). 0000 Object buffer 0 0001 Object buffer 1 0010 Object buffer 2 0011 Object buffer 3 0100 Object buffer 4 0101 Object buffer 5 0110 Object buffer 6 0111 Object buffer 7

4.3.4.5 SIU_FAR: FIFO Auto Reset

I/O Address HIU_RDT
Index 4001

Register SIU_FAR controls whether SIU FIFOs F and G are automatically reset (cleared) on the vertical sync from the video source designated as master in register VIU_WDT, bit MFTS.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									FGR	FFR	RSVD				

Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as '0').
6	R/W	0	FGR	FIFO G Reset. Reset FIFO G on the vertical sync master in register VIU_WDT, bit MFTS. 0 no auto reset 1 clear FIFO G on vertical sync.
5	R/W	0	FFR	FIFO F Reset. Reset FIFO F on the vertical sync master in register VIU_WDT, bit MFTS. 0 no auto reset 1 clear FIFO F on vertical sync.
4:0	R/W	0h	RSVD	Reserved (read as '0').

4.3.5 ALU: Arithmetic and Logic Unit

4.3.5.1 ALU_MCRf: ALU Master Control

I/O Address HIU_RDT
Index 2900 (ALU_MCR1: ALU Master Control, Field 1)
2901 (ALU_MCR2: ALU Master Control, Field 2)

Registers ALU_MCR1 and ALU_MCR2 specify the ALU operating mode for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GBM	TF		AOP				YOUT		UOUT		VOUT		OPCS	OPBS	OPAS

Bit #	Access	Reset	Description	
15	R/W	00	GBM	Three-operand Bit Mask selecting tag source. 0 Bit per bit mask — bit n in FIFO C will mask bit n of the pixel currently operated on (from FIFO A or B) by the ALU 1 Bit per pixel mask — bit n in FIFO C will mask pixel n from FIFO A or B

Bit #	Access	Reset	Description	
14:13	R/W	0000	TF	Tag Format. Specifies both the input and output stream tag formats. 00 No tag 01 Tagged 4:2:2 YCbCr data 10 Tagged 5:5:5 RGB data 11 Tagged 8:8:8 RGB data
12:9	R/W	00	AOP	Arithmetic Operation Select. 0000 Alpha mix using alpha register (dA + (1-d)B) 0001 Alpha mix using operand C (cA + (1-c)B) 0010 Operand A + Operand B 0011 Operand A - Operand B 0100 (Operand A - Operand B) / 2 0101 Reconstruct field from operands A and B 0110 Four frame interpolate from operands A and B XXXX All other configurations are reserved; results are unpredictable
8:7	R/W	00	YOUT	Y Output Source Select. 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
6:5	R/W	00	UOUT	U Output Source Select. 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
4:3	R/W	0	VOUT	V output Source Select. 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
2	R/W	0	OPCS	Operand C Source Select. 0 Operand sourced from constant register 1 Operand sourced from FIFO
1	R/W	0	OPBS	Operand B Source Select. 0 Operand sourced from constant register 1 Operand sourced from FIFO
0	R/W	0	OPAS	Operand A Source Select. 0 Operand sourced from constant register 1 Operand sourced from FIFO

4.3.5.2 ALU_TOP: Tag Operation

I/O Address HIU_RDT
Index 2902

Register ALU_TOP specifies the control and output tag multiplexer operation codes.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTC								OTC							

Bit #	Access	Reset	Description	
15:8	R/W	0h	CTC	Control Tag Code. (0-FFh)
7:0	R/W	0h	OTC	Output Tag Code. (0-FFh)

4.3.5.3 ALU_AV: Alpha Value

I/O Address HIU_RDT
Index 2903

Register ALU_AV specifies the alpha mix constant.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								AV							

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as '0').
7:0	R/W	0h	AV	Alpha Value. (0-FFh)

4.3.5.4 ALU_LOPx: Logic Operation

I/O Address HIU_RDT
Index 2904 (ALU_LOPY: Logic Operation Channel Y)
2905 (ALU_LOPU: Logic Operation Channel U)
2906 (ALU_LOPV: Logic Operation Channel V)

Registers ALU_LOPY, ALU_LOPU, and ALU_LOPV specify the constant values for logical multiplexers A, B, and C, respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MLOP															

Bit #	Access	Reset	Description	
15:0	R/W	0h	MLOP	Multiplexor Logical Operation.

4.3.5.5 ALU_CAx: Constant A

I/O Address HIU_RDT
Index 2907 (ALU_CAY: Constant A, Channel Y)
2908 (ALU_CAU: Constant A, Channel U)
2909 (ALU_CAV: Constant A, Channel V)

See also: ALU_MCRf: ALU Master Control, p. 62

Registers ALU_CAY, ALU_CAU, and ALU_CAV specify the constant values for Operand A, based on the value of register ALU_MCRf, field OPAS.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								CON							
RSVD							TAG	CON							

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as '0').
8	R/W	0h	TAG	Tag. (ALU_CAU and ALU_CAV only) Specifies the constant tag bit to insert in the input stream. (0-1h)
7:0	R/W	0h	CON	Constant. Specifies the constant 8-bit value to use in place of the real-time input stream channel for operand A. (0-FFh)

4.3.5.6 ALU_CBx: Constant B

I/O Address Index: HIU_RDT
290a (ALU_CBY: Constant B, Channel Y)
290b (ALU_CBU: Constant B, Channel U)
290c (ALU_CBV: Constant B, Channel V)

See also: ALU_MCRf: ALU Master Control, p. 62

Registers ALU_CBY, ALU_CBU, and ALU_CBV specify the constant values for Operand B, based on the value of register ALU_MCRf, field OPBS.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								CON							
RSVD							TAG	CON							

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as '0').
8	R/W	0h	TAG	Tag. (ALU_CBU and ALU_CBV only) Specifies the constant tag bit to insert in the input stream. (0-1h)
7:0	R/W	0h	CON	Constant. Specifies the constant 8-bit value to use in place of the real-time input stream channel for operand B. (0-FFh)

4.3.5.7 ALU_CCx: Constant C

I/O Address Index: HIU_RDT
290d (ALU_CCY: Constant C, Channel Y)
290e (ALU_CCU: Constant C, Channel U)
290f (ALU_CCV: Constant C, Channel V)

See also: ALU_MCRf: ALU Master Control, p. 62

Registers ALU_CCY, ALU_CCU, and ALU_CCV specify the constant values for Operand C, based on the value of register ALU_MCRf, field OPCS.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								CON							
RSVD							TAG	CON							

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as '0').
8	R/W	0h	TAG	Tag. (ALU_CCU and ALU_CCV only) Specifies the constant tag bit to insert in the input stream. (0-1h)

Bit #	Access	Reset	Description	
7:0	R/W	0h	CON	Constant. Specifies the constant 8-bit value to use in place of the real-time input stream channel for operand C. (0-FFh)

4.3.6 OPU: Output Processing Unit

4.3.6.1 OPU_MCRf: OPU Master Control

POSTED
I/O Address HIU_RDT
Index 2a00 (OPU_MCR1: OPU Master Control, Field 1) 2b00 (OPU_MCR2: OPU Master Control, Field 2)

Registers OPU_MCR1 and OPU_MCR2 control the operation of the OPU for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FPS	IM	ZE	RSVD		LSM	RSVD						IF			

Bit #	Access	Reset	Description	
15	R/W	0	FPS	Field Polarity Select. Controls the polarity of the field ID signal supplied to the OPU Window Clipping Unit. 0 Normal polarity 1 Invert polarity
14	R/W	0	IM	Interlace Mode. Specifies the input stream as interlaced or non-interlaced data. 0 Progressive scan input 1 Interlaced input
13	R/W	0	ZE	Zoom Enable. Enables or disables the operation of the 2:1 X zoom subunit. Only affects source object size. 0 Disable zoom 1 Enable 2X zoom
12:11	R/W	0h	RSVD	Reserved (read as '0').
10	R/W	0	LSM	Line Start Mode. 0 Active line starts on horizontal blank inactive 1 Active line starts on horizontal sync inactive (VSU_HAD must = VSU_HSW+3 in loopback mode.)
9:4	R/W	0h	RSVD	Reserved (read as '0').
3:0	R/W	0000	IF	Input Data Format. Specifies the format of the input data stream. 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 5:5:5 tagged data 1110 RGB 3:3:2 non-tagged data (non-zoom mode only)

4.3.6.2 OPU_XBI1: X Begin

POSTED
I/O Address HIU_RDT
Index 2a02 (OPU_XBI1: X Begin Integer, Field 1)
2b02 (OPU_XBI2: X Begin Integer, Field 2)

Registers OPU_XBI1 and OPU_XBI2 specify the 11-bit X begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					BI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin X Column Integer Index. Specifies the 11-bit integer portion of the 11-bit X begin value. (0-7FFh)

4.3.6.3 OPU_XEIf: X End

POSTED
I/O Address HIU_RDT
Index 2a03 (OPU_XEI1: X End Integer, Field 1)
2b03 (OPU_XEI2: X End Integer, Field 2)

Registers OPU_XEI1 and OPU_XEI2 specify the 11-bit X end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	End X Column Integer Index. Specifies the 11-bit X end value. (0-7FFh)

4.3.6.4 OPU_YBIf: Y Begin

POSTED
I/O Address HIU_RDT
Index 2a07 (OPU_YBI1: Y Begin Integer, Field 1)
2b07 (OPU_YBI2: Y Begin Integer, Field 2)

Registers OPU_YBI1 and OPU_YBI2 specify the 11-bit Y begin value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					BI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BI	Begin Y Row Integer Index. Specifies the 11-bit integer portion of the 11-bit Y begin value. (0-7FFh)

4.3.6.5 OPU_YEIf: Y End

POSTED
I/O Address HIU_RDT
Index 2a08 (OPU_YEI1: Y End Integer, Field 1)
2b08 (OPU_YEI2: Y End Integer, Field 2)

Registers OPU_YEI1 and OPU_YEI2 specify the 11-bit Y end value for fields 1 and 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					EI										

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	EI	End Y Row Integer Index. Specifies the 11-bit Y end value. (0-7FFh)

4.3.7 RFU: Reference Frame Unit

Name	Index	Definition	Posted?	Ref. Section
MMU: Memory Management Unit				
MMU_MCR	4000	MMU Master Control	POSTED	4.3.8.1, p. 73
OBU: Object Buffer Unit				4.3.9, p. 74
OBU0_MCR	4800	Object Buffer 0 Master Control	POSTED	4.3.9.1, p. 74
OBU0_RFX	4801	Object Buffer 0 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU0_LSL	4802	Object Buffer 0 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU0_LSH	4803	Object Buffer 0 Linear Start Address High	POSTED	4.3.10, p. 76
OBU0_BSX	4804	Object Buffer 0 X Size	POSTED	4.3.10.1, p. 77
OBU0_BSY	4805	Object Buffer 0 Y Size	POSTED	4.3.10.1, p. 77
OBU0_DEC	4806	Object Buffer 0 Decimate Control	POSTED	4.3.10.2, p. 78
OBU1_MCR	4810	Object Buffer 1 Master Control	POSTED	4.3.9.1, p. 74
OBU1_RFX	4811	Object Buffer 1 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU1_LSL	4812	Object Buffer 1 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU1_LSH	4813	Object Buffer 1 Linear Start Address High	POSTED	4.3.10, p. 76
OBU1_BSX	4814	Object Buffer 1 X Size	POSTED	4.3.10.1, p. 77
OBU1_BSY	4815	Object Buffer 1 Y Size	POSTED	4.3.10.1, p. 77
OBU1_DEC	4816	Object Buffer 1 Decimate Control	POSTED	4.3.10.2, p. 78
OBU2_MCR	4820	Object Buffer 2 Master Control	POSTED	4.3.9.1, p. 74
OBU2_RFX	4821	Object Buffer 2 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU2_LSL	4822	Object Buffer 2 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU2_LSH	4823	Object Buffer 2 Linear Start Address High	POSTED	4.3.10, p. 76
OBU2_BSX	4824	Object Buffer 2 X Size	POSTED	4.3.10.1, p. 77
OBU2_BSY	4825	Object Buffer 2 Y Size	POSTED	4.3.10.1, p. 77
OBU2_DEC	4826	Object Buffer 2 Decimate Control	POSTED	4.3.10.2, p. 78
OBU3_MCR	4830	Object Buffer 3 Master Control	POSTED	4.3.9.1, p. 74
OBU3_RFX	4831	Object Buffer 3 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU3_LSL	4832	Object Buffer 3 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU3_LSH	4833	Object Buffer 3 Linear Start Address High	POSTED	4.3.10, p. 76

4.3.7 RFU: Reference Frame Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
OBU3_BSX	4834	Object Buffer 3 X Size	POSTED	4.3.10.1, p. 77
OBU3_BSY	4835	Object Buffer 3 Y Size	POSTED	4.3.10.1, p. 77
OBU3_DEC	4836	Object Buffer 3 Decimate Control	POSTED	4.3.10.2, p. 78
OBU4_MCR	4840	Object Buffer 4 Master Control	POSTED	4.3.9.1, p. 74
OBU4_RFX	4841	Object Buffer 4 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU4_LSL	4842	Object Buffer 4 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU4_LSH	4843	Object Buffer 4 Linear Start Address High	POSTED	4.3.10, p. 76
OBU4_BSX	4844	Object Buffer 4 X Size	POSTED	4.3.10.1, p. 77
OBU4_BSY	4845	Object Buffer 4 Y Size	POSTED	4.3.10.1, p. 77
OBU4_DEC	4846	Object Buffer 4 Decimate Control	POSTED	4.3.10.2, p. 78
OBU5_MCR	4850	Object Buffer 5 Master Control	POSTED	4.3.9.1, p. 74
OBU5_RFX	4851	Object Buffer 5 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU5_LSL	4852	Object Buffer 5 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU5_LSH	4853	Object Buffer 5 Linear Start Address High	POSTED	4.3.10, p. 76
OBU5_BSX	4854	Object Buffer 5 X Size	POSTED	4.3.10.1, p. 77
OBU5_BSY	4855	Object Buffer 5 Y Size	POSTED	4.3.10.1, p. 77
OBU5_DEC	4856	Object Buffer 5 Decimate Control	POSTED	4.3.10.2, p. 78
OBU6_MCR	4860	Object Buffer 6 Master Control	POSTED	4.3.9.1, p. 74
OBU6_RFX	4861	Object Buffer 6 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU6_LSL	4862	Object Buffer 6 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU6_LSH	4863	Object Buffer 6 Linear Start Address High	POSTED	4.3.10, p. 76
OBU6_BSX	4864	Object Buffer 6 X Size	POSTED	4.3.10.1, p. 77
OBU6_BSY	4865	Object Buffer 6 Y Size	POSTED	4.3.10.1, p. 77
OBU6_DEC	4866	Object Buffer 6 Decimate Control	POSTED	4.3.10.2, p. 78
OBU7_MCR	4870	Object Buffer 7 Master Control	POSTED	4.3.9.1, p. 74
OBU7_RFX	4871	Object Buffer 7 Reference Frame X Size	POSTED	4.3.9.2, p. 75
OBU7_LSL	4872	Object Buffer 7 Linear Start Address Low	POSTED	4.3.10, p. 76
OBU7_LSH	4873	Object Buffer 7 Linear Start Address High	POSTED	4.3.10, p. 76
OBU7_BSX	4874	Object Buffer 7 X Size	POSTED	4.3.10.1, p. 77

4.3.7 RFU: Reference Frame Unit *(cont.)*

Name	Index	Definition	Posted?	Ref. Section
OBU7_BSY	4875	Object Buffer 7 Y Size	POSTED	4.3.10.1, p. 77
OBU7_DEC	4876	Object Buffer 7 Decimate Control	POSTED	4.3.10.2, p. 78
DWU: Display Window Unit			POSTED	4.3.11, p. 78
DWU_MCR	4100	Display Window Master Control	POSTED	4.3.11.1, p. 78
DWU_HCR	4101	Display Window Horizontal Control	POSTED	4.3.11.2, p. 80
DWU0_DZF	4400	Display Window 0 Zoom Factor	POSTED	4.3.11.3, p. 81
DWU0_RFX	4401	Display Window 0 Reference Frame X Size	POSTED	4.3.11.4, p. 81
DWU0_LSL	4402	Display Window 0 LSA Low	POSTED	4.3.11.5, p. 82
DWU0_LSH	4403	Display Window 0 LSA High	POSTED	4.3.11.5, p. 82
DWU0_WSX	4404	Display Window 0 X Size	POSTED	4.3.11.6, p. 82
DWU0_WSY	4405	Display Window 0 Y Size	POSTED	4.3.11.6, p. 82
DWU0_DSX	4406	Display Window 0 X Start	POSTED	4.3.11.7, p. 83
DWU0_DSY	4407	Display Window 0 Y Start	POSTED	4.3.11.7, p. 83
DWU1_DZF	4410	Display Window 1 Zoom Factor	POSTED	4.3.11.3, p. 81
DWU1_RFX	4411	Display Window 1 Reference Frame X Size	POSTED	4.3.11.4, p. 81
DWU1_LSL	4412	Display Window 1 LSA Low	POSTED	4.3.11.5, p. 82
DWU1_LSH	4413	Display Window 1 LSA High	POSTED	4.3.11.5, p. 82
DWU1_WSX	4414	Display Window 1 X Size	POSTED	4.3.11.6, p. 82
DWU1_WSY	4415	Display Window 1 Y Size	POSTED	4.3.11.6, p. 82
DWU1_DSX	4416	Display Window 1 X Start	POSTED	4.3.11.7, p. 83
DWU1_DSY	4417	Display Window 1 Y Start	POSTED	4.3.11.7, p. 83
DWU2_DZF	4420	Display Window 2 Zoom Factor	POSTED	4.3.11.3, p. 81
DWU2_RFX	4421	Display Window 2 Reference Frame X Size	POSTED	4.3.11.4, p. 81
DWU2_LSL	4422	Display Window 2 LSA Low	POSTED	4.3.11.5, p. 82
DWU2_LSH	4423	Display Window 2 LSA High	POSTED	4.3.11.5, p. 82
DWU2_WSX	4424	Display Window 2 X Size	POSTED	4.3.11.6, p. 82
DWU2_WSY	4425	Display Window 2 Y Size	POSTED	4.3.11.6, p. 82
DWU2_DSX	4426	Display Window 2 X Start	POSTED	4.3.11.7, p. 83

4.3.7 RFU: Reference Frame Unit *(cont.)*

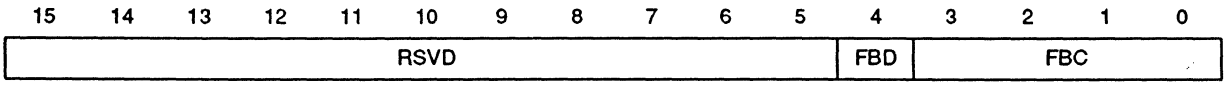
Name	Index	Definition	Posted?	Ref. Section
DWU2_DSY	4427	Display Window 2 Y Start	POSTED	4.3.11.7, p. 83
DWU3_DZF	4430	Display Window 3 Zoom Factor	POSTED	4.3.11.3, p. 81
DWU3_RFX	4431	Display Window 3 Reference Frame X Size	POSTED	4.3.11.4, p. 81
DWU3_LSL	4432	Display Window 3 LSA Low	POSTED	4.3.11.5, p. 82
DWU3_LSH	4433	Display Window 3 LSA High	POSTED	4.3.11.5, p. 82
DWU3_WSX	4434	Display Window 3 X Size	POSTED	4.3.11.6, p. 82
DWU3_WSY	4435	Display Window 3 Y Size	POSTED	4.3.11.6, p. 82
DWU3_DSX	4436	Display Window 3 X Start	POSTED	4.3.11.7, p. 83
DWU3_DSY	4437	Display Window 3 Y Start	POSTED	4.3.11.7, p. 83

4.3.8 MMU: Memory Management Unit

4.3.8.1 MMU_MCR: MMU Master Control

I/O Address HIU_RDT
Index 4000

Register MMU_MCR specifies the characteristics of the frame buffer used by the DVP.



Bit #	Access	Reset	Description	
15:5	R/W	0h	RSVD	Reserved (read as '0').
4	R/W	0	FBD	Frame Buffer Data Bus Width. 0 16-bit 1 32-bit
3:0	R/W	0000	FBC	Frame Buffer Memory Device Address Configuration. 0000 64K 0001 128K 0010 256K 0011 1 M

4.3.9 OBU: Object Buffer Unit

4.3.9.1 OBUo_MCR: Object Buffer Master Control

POSTED
I/O Address HIU_RDT
Index 4800 (OBU0_MCR: Object Buffer 0 Master Control)
4810 (OBU1_MCR: Object Buffer 1 Master Control)
4820 (OBU2_MCR: Object Buffer 2 Master Control)
4830 (OBU3_MCR: Object Buffer 3 Master Control)
4840 (OBU4_MCR: Object Buffer 4 Master Control)
4850 (OBU5_MCR: Object Buffer 5 Master Control)
4860 (OBU6_MCR: Object Buffer 6 Master Control)
4870 (OBU7_MCR: Object Buffer 7 Master Control)

The eight identical registers OBUo_MCR control the operation of the eight object buffers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			LME	CME	FL	OPM				SSM	YBDC	XBDC	FA		

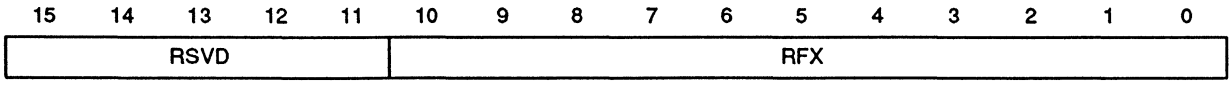
Bit #	Access	Reset	Description	
15:13	R/W	000	RSVD	Reserved (read as '0').
12	R/W	0	LME	Luminance Mask Enable. Specifies whether the MSB of a 16-bit input stream (typically the Y channel of YCbCr data) is written to the object buffer or masked. 0 Enable luminance data update (MSB written to object buffer) 1 Disable luminance data update (MSB masked)
11	R/W	0	CME	Chrominance Mask Enable. Specifies whether the LSB of a 16-bit input stream (typically the CbCr channel of YCbCr data) is written to the object buffer or masked. 0 Enable chrominance data update (LSB written to object buffer) 1 Disable chrominance data update (LSB masked)
10	R/W	0	FL	Field Lock. Field-locks the object to the video source selected as the master in register VIU_WDT, bit MFTS. 0 not field locked 1 field locked
9:6	R/W	0h	OPM	Operation Mode. Enables operation of the object buffer and specifies the synchronization and addressing modes. 0000 Disable OBU line 0001 Enable OBU; lock to IPU1, address generation locked to IPU1 (bit FL must = 1) 0100 Enable OBU; independent, interlaced addresses, start on line 1 0101 Enable OBU; independent, interlaced addresses, start on line 2 1100 Enable OBU; independent, normal addresses 1101 Enable OBU; independent, line replicate addresses (on read) 1110 Enable OBU; independent, block mode addresses (8 x 8 blocks, OBU0 only) 1111 Enable 16 x 8 blocks, OBU0 only XXXX All other configurations reserved.

Bit #	Access	Reset	Description	
5	R/W	0	SSM	Single Sweep Mode. 0 Disable single sweep mode 1 Enable single sweep mode (reset OPM to 00000 after one field)
4	R/W	0	YBDC	Y BLT Direction Control. Specifies whether the Y address counter is incremented or decremented after each line. 0 BLT to decreasing memory addresses 1 BLT to increasing memory addresses
3	R/W	0	XBDC	X BLT Direction Control. Specifies whether the X address counter is incremented or decremented after each line. 0 BLT to decreasing memory addresses 1 BLT to increasing memory addresses
2:0	R/W	000	FA	FIFO Association. Specifies whether the stream written into the object buffer is to be copied to one of the output FIFOs. 000 No FIFO copy 001 Copy object buffer to FIFO A during write 010 Copy object buffer to FIFO B during write 011 Copy object buffer to FIFO C during write 100 Copy object buffer to FIFO D during write XXX All other configurations reserved

4.3.9.2 OBUo_RFX: Object Buffer Reference Frame Size

POSTED
I/O Address Index — HIU_RDT
4801 (OBU0_RFX: Object Buffer 0 Reference Frame X Size)
4811 (OBU1_RFX: Object Buffer 1 Reference Frame X Size)
4821 (OBU2_RFX: Object Buffer 2 Reference Frame X Size)
4831 (OBU3_RFX: Object Buffer 3 Reference Frame X Size)
4841 (OBU4_RFX: Object Buffer 4 Reference Frame X Size)
4851 (OBU5_RFX: Object Buffer 5 Reference Frame X Size)
4861 (OBU6_RFX: Object Buffer 6 Reference Frame X Size)
4871 (OBU7_RFX: Object Buffer 7 Reference Frame X Size)

The eight identical registers OBUo_RFX specify, for each of the eight object buffers, the 11-bit width (in pixels) of the reference frame containing the object buffer.



Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	RFX	Reference Frame X size (0-7FFh)

4.3.10 OBUo_LSb: Object Buffer Linear Start Address

POSTED
I/O Address HIU_RDT
Index 4802 (OBU0_LSL: Object Buffer 0 Linear Start Address Low)
4812 (OBU1_LSL: Object Buffer 1 Linear Start Address Low)
4822 (OBU2_LSL: Object Buffer 2 Linear Start Address Low)
4832 (OBU3_LSL: Object Buffer 3 Linear Start Address Low)
4842 (OBU4_LSL: Object Buffer 4 Linear Start Address Low)
4852 (OBU5_LSL: Object Buffer 5 Linear Start Address Low)
4862 (OBU6_LSL: Object Buffer 6 Linear Start Address Low)
4872 (OBU7_LSL: Object Buffer 7 Linear Start Address Low)
4803 (OBU0_LSH: Object Buffer 0 Linear Start Address High)
4813 (OBU1_LSH: Object Buffer 1 Linear Start Address High)
4823 (OBU2_LSH: Object Buffer 2 Linear Start Address High)
4833 (OBU3_LSH: Object Buffer 3 Linear Start Address High)
4843 (OBU4_LSH: Object Buffer 4 Linear Start Address High)
4853 (OBU5_LSH: Object Buffer 5 Linear Start Address High)
4863 (OBU6_LSH: Object Buffer 6 Linear Start Address High)
4873 (OBU7_LSH: Object Buffer 7 Linear Start Address High)

Registers OBUo_LSL and OBUo_LSH specify the 23-bit linear starting address of the object buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSL															
RSVD										LSH					

Bit #	Access	Reset	Description	
Object Buffer Linear Start Address Low				
15:0	R/W	0h	LSL	Linear Start Address Low. Specifies the lower bits of the 22-bit linear starting address (LSb must = 0). (0-FFFEh)
Object Buffer Linear Start Address High				
15:6	R/W	0h	RSVD	Reserved (read as '0').
5:0	R/W	0h	LSH	Linear Start Address High. Specifies the upper 6 bits of the 22-bit linear starting address. (0-7Fh)

4.3.10.1 OBUo_BSa: Object Buffer Size

POSTED
I/O Address HIU_RDT
Index

4804 (OBU0_BSX: Object Buffer 0 X Size)	4805 (OBU0_BSY: Object Buffer 0 Y Size)
4814 (OBU1_BSX: Object Buffer 1 X Size)	4815 (OBU1_BSY: Object Buffer 1 Y Size)
4824 (OBU2_BSX: Object Buffer 2 X Size)	4825 (OBU2_BSY: Object Buffer 2 Y Size)
4834 (OBU3_BSX: Object Buffer 3 X Size)	4835 (OBU3_BSY: Object Buffer 3 Y Size)
4844 (OBU4_BSX: Object Buffer 4 X Size)	4845 (OBU4_BSY: Object Buffer 4 Y Size)
4854 (OBU5_BSX: Object Buffer 5 X Size)	4855 (OBU5_BSY: Object Buffer 5 Y Size)
4864 (OBU6_BSX: Object Buffer 6 X Size)	4865 (OBU6_BSY: Object Buffer 6 Y Size)
4874 (OBU7_BSX: Object Buffer 7 X Size)	4875 (OBU7_BSY: Object Buffer 7 Y Size)

Registers OBUo_BSX and OBUo_BSY specify the size of the object buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					BSX										
RSVD					BSY										

Bit #	Access	Reset	Description	
OBUo_BSX: Object Buffer X Size				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BSX	Buffer X Size. Specifies the object buffer's width in pixels. The hardware always forces the LSb to '0'. (0-7FFh)
OBUo_BSY: Object Buffer Y Size				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	BSY	Buffer Y Size. Specifies the object buffer's height in pixels. (0-7FFh)

4.3.10.2 OBUo_DEC: Object Buffer Decimate Control

POSTED
I/O Address HIU_RDT
Index 4806 (OBU0_DEC: Object Buffer 0 Decimate Control)
4816 (OBU1_DEC: Object Buffer 1 Decimate Control)
4826 (OBU2_DEC: Object Buffer 2 Decimate Control)
4836 (OBU3_DEC: Object Buffer 3 Decimate Control)
4846 (OBU4_DEC: Object Buffer 4 Decimate Control)
4856 (OBU5_DEC: Object Buffer 5 Decimate Control)
4866 (OBU6_DEC: Object Buffer 6 Decimate Control)
4876 (OBU7_DEC: Object Buffer 7 Decimate Control)

Register OBUo_DEC specifies the write decimation mask. DM7-DM0 are mapped to each successive group of eight pixels written into the object buffer. Do not drop the first line or pixel in a transfer to an object buffer (i.e., when BLT direction is up, DM0 must be '0'; when BLT direction is down, DM7 must be '0').

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as '0').
7	R/W	0h	DM7	Write Decimation Mask Bit 7.
6	R/W	0h	DM6	Write Decimation Mask Bit 6.
5	R/W	0h	DM5	Write Decimation Mask Bit 5.
4	R/W	0h	DM4	Write Decimation Mask Bit 4.
3	R/W	0h	DM3	Write Decimation Mask Bit 3.
2	R/W	0h	DM2	Write Decimation Mask Bit 2.
1	R/W	0h	DM1	Write Decimation Mask Bit 1.
0	R/W	0h	DM0	Write Decimation Mask Bit 0.

For all Write Decimation Bits 7:0:
0 Write pixel to frame buffer
1 Drop pixel

4.3.11 DWU: Display Window Unit

4.3.11.1 DWU_MCR: Display Window Master Control

POSTED
I/O Address HIU_RDT
Index 4100

Register DWU_MCR controls the operation of the display window and indicates to the RFU whether or not the CL-PX2080 is present.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GCS	GFP	GFM	GVSP	GHSP	GBP	OCC	IMS	RSVD				WC3	WC2	WC1	WC0

Bit #	Access	Reset	Description	
15	R/W	0	GCS	Graphics Clock Select 0 1/2x GPCLK 1 1x GPCLK
14	R/W	0	GFP	Graphics Field Polarity 0 normal polarity 1 inverted polarity
13	R/W	0	GFM	Graphics Field Mode 0 field polarity determined by value of GHSP on falling GVSP 1 GHSP input used as field select
12	R/W	0	GVSP	Graphics Vertical Sync Polarity. Specifies polarity of signal GVS. 0 active low 1 active high
11	R/W	0	GHSP	Graphics Horizontal Sync Polarity. Specifies polarity of signal GHS. 0 active low 1 active high
10	R/W	0	GBP	Graphics Blank Polarity. Specifies polarity of signal GBL. 0 active low 1 active high
9	R/W	0	OCC	Occluded Window Control. Specifies whether the present hardware configuration includes the CL-PX2080. 0 CL-PX2080 is present — system supports occluded windows 1 CL-PX2080 is not present — system does not support occluded windows
8	R/W	0	IMS	Interlace Mode Select. Specifies whether the stream stored in the object buffer for display by the current display window is interlaced or non-interlaced. 0 Progressive-scan video (non-interlaced) 1 Interlaced video
7:4	R/W	0000	RSVD	Reserved (read as '0').
3	R/W	0	WC3	Window 3 Control
2	R/W	0	WC2	Window 2 Control
1	R/W	0	WC1	Window 1 Control
0	R/W	0	WC0	Window 0 Control

For all Window Controls 3:0:
0 Disable window
1 Enable window

4.3.11.2 DWU_HCR: Display Window Horizontal Control

POSTED
I/O Address HIU_RDT
Index 4101

Register DWU_HCR shares two functions, depending on whether or not the DVP is operating with the CL-PX2080, as specified register DWU_MCR, bit OCC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					HAC										
RSVD								MWS							

Bit #	Access	Reset	Description	
Horizontal Active Count (DWU_MCR, bit OCC = 0)				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	HAC	Horizontal Active Count. Specifies the number of pixel periods in the horizontal line active interval for the output CRT display. (0-7FFh)
Minimum Window Separation (DWU_MCR, bit OCC = 1)				
15:8	R/W	0h	RSVD	Reserved (read as '0').
7:0	R/W	0h	MWS	Minimum Window Separation. Specifies the minimum number of pixel periods required to separate display windows. (0-ffh)

4.3.11.3 DWUd_DZF: Display Window Display Zoom Factor

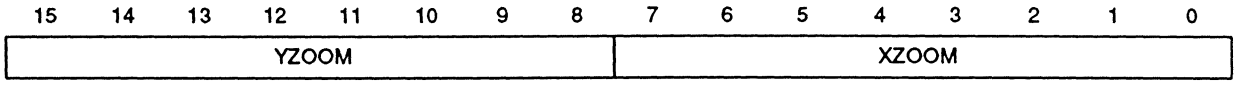
POSTED
I/O Address HIU_RDT
Index 4400 (DWU0_DZF: Display Window 0 Zoom Factor)
4410 (DWU1_DZF: Display Window 1 Zoom Factor)
4420 (DWU2_DZF: Display Window 2 Zoom Factor)
4430 (DWU3_DZF: Display Window 3 Zoom Factor)

Register DWUd_DZF specifies the X and Y zoom factors to be applied to the display window output (functional only when used with CL-PX2080). The image is scaled according to the following formula:

$$\text{Scaling} = \frac{256}{\text{ZOOM FACTOR}}$$

For example, a zoom factor of 128 yields a scaling factor of 2. A zoom factor of '0h' specifies a scaling factor of one (no change in image size).

NOTE: The contents of the object buffer are not affected by the zoom factors.

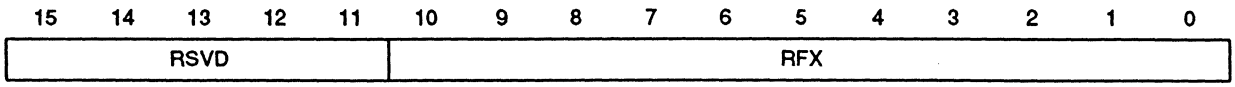


Bit #	Access	Reset	Description	
15:8	R/W	0h	YZOOM	Y Zoom Factor — line replication value. (0-FFh)
7:0	R/W	0h	XZOOM	X Zoom Factor — pixel replication value. (0-FFh)

4.3.11.4 DWUd_RFX: Display Window Reference Frame Size

POSTED
I/O Address HIU_RDT
Index 4401 (DWU0_RFX: Display Window 0 Reference Frame X Size)
4411 (DWU1_RFX: Display Window 1 Reference Frame X Size)
4421 (DWU2_RFX: Display Window 2 Reference Frame X Size)
4431 (DWU3_RFX: Display Window 3 Reference Frame X Size)

Register DWUd_RFX specifies the 11-bit pixel width of the reference frame containing the display window.



Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	RFX	Reference Frame X size. (0-7FFh)

4.3.11.5 DWUd_LSb: Display Window Linear Start Address

POSTED
I/O Address HIU_RDT
Index 4402 (DWU0_LSL: Display Window 0 LSA Low) 4403 (DWU0_LSH: Display Window 0 LSA High)
4412 (DWU1_LSL: Display Window 1 LSA Low) 4413 (DWU1_LSH: Display Window 1 LSA High)
4422 (DWU2_LSL: Display Window 2 LSA Low) 4423 (DWU2_LSH: Display Window 2 LSA High)
4432 (DWU3_LSL: Display Window 3 LSA Low) 4433 (DWU3_LSH: Display Window 3 LSA High)

Registers DWUd_LSL and DWUd_LSH specify the 23-bit linear starting address of the display window.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSL															
RSVD										LSH					

Bit #	Access	Reset	Description	
DWUd_LSL: Display Window Linear Start Address Low				
15:0	R/W	0h	LSL	Linear Start Address Low. Specifies the lower bits of the 22-bit linear starting address. (LSb must = 0). (0-7FFFh)
DWUd_LSH: Display Window Linear Start Address High				
15:7	R/W	0h	RSVD	Reserved (read as '0').
6:0	R/W	0h	LSH	Linear Start Address High. Specifies the upper 7 bits of the 22-bit linear starting address. (0-7Fh)

4.3.11.6 DWUd_WSa: Display Window Size

POSTED
I/O Address HIU_RDT
Index 4404 (DWU0_WSX: Display Window 0 X Size) 4405 (DWU0_WSY: Display Window 0 Y Size)
4414 (DWU1_WSX: Display Window 1 X Size) 4415 (DWU1_WSY: Display Window 1 Y Size)
4424 (DWU2_WSX: Display Window 2 X Size) 4426 (DWU2_WSY: Display Window 2 Y Size)
4434 (DWU3_WSX: Display Window 3 X Size) 4435 (DWU3_WSY: Display Window 3 Y Size)

Registers DWUd_WSX and DWUd_WSY specify the size of the display window.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					WSX										
RSVD					WSY										

Bit #	Access	Reset	Description	
DWUd_WSX: Display Window X Size				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	WSX	Window X Size. Specifies the X dimension of the display window in pixels. (LSb must = 0)
DWUd_WSY: Display Window Y Size				
15:11	R/W	0h	RSVD	Reserved (read as '0').
10:0	R/W	0h	WSY	Window Y Size. Specifies the Y dimension of the display window in pixels. (0-7FFh)

4.3.11.7 DWUd_DSa: Display Window Start

POSTED
I/O Address HIU_RDT
Index 4406 (DWU0_DSX: Display Window 0 X Start) 4407 (DWU0_DSY: Display Window 0 Y Start)
4416 (DWU1_DSX: Display Window 1 X Start) 4417 (DWU1_DSY: Display Window 1 Y Start)
4426 (DWU2_DSX: Display Window 2 X Start) 4427 (DWU2_DSY: Display Window 2 Y Start)
4436 (DWU3_DSX: Display Window 3 X Start) 4437 (DWU3_DSY: Display Window 3 Y Start)

Registers DWUd_DSX and DWUd_DSY specify the location of the top left corner of the display window relative to the top left corner of the output CRT display.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				DSX											
RSVD				DSY											

Bit #	Access	Reset	Description	
DWUd_DSX: Display Window X Start				
15:12	R/W	0h	RSVD	Reserved (read as '0').
11:0	R/W	0h	DSX	Display X Start. Specifies the pixel offset from the CRT column 0 to the left-most column of the display window. (0-7FFh)
DWUd_DSY: Display Window Y Start				
15:12	R/W	0h	RSVD	Reserved (read as '0').
11:0	R/W	0h	DSY	Display Y Start. Specifies the pixel offset from the CRT row 0 to the top-most row of the display window. (0-7FFh)

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the DVP. Stresses above those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Storage temperature ..... -65 to +150°C

Voltage on any pin with respect to ground ..... -0.5 Volts to V_{DD} +0.5V

Power Supply Voltage 7V

Lead Temperature (10 seconds) ..... 300°C

5.2 DVP Specifications (Digital)

Symbol	Parameter	MIN	MAX	Conditions
VDD	Power Supply Voltage	4.75 V	5.25 V	Normal Operation
V_{IL}	Input Low Voltage	0 V	0.8 V	
V_{IH}	Input High Voltage	2.0 V	V_{DD} + 0.8 V	
V_{OL}	Output Low Voltage		0.4 V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4 V	V	I_{OH} = 400 µA
I_{DD}	Digital Supply Current		N/A	VDD Nominal
I_L	Input Leakage	-10 µA	10 µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Input Capacitance		10 pF	
C_{OUT}	Output Capacitance		10 pF	

5.3 AC Characteristics/Timing Information

This section includes system timing requirements for the DVP. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0 to 70°C, and V_{CC} varying from 4.75 to 5.25V DC.

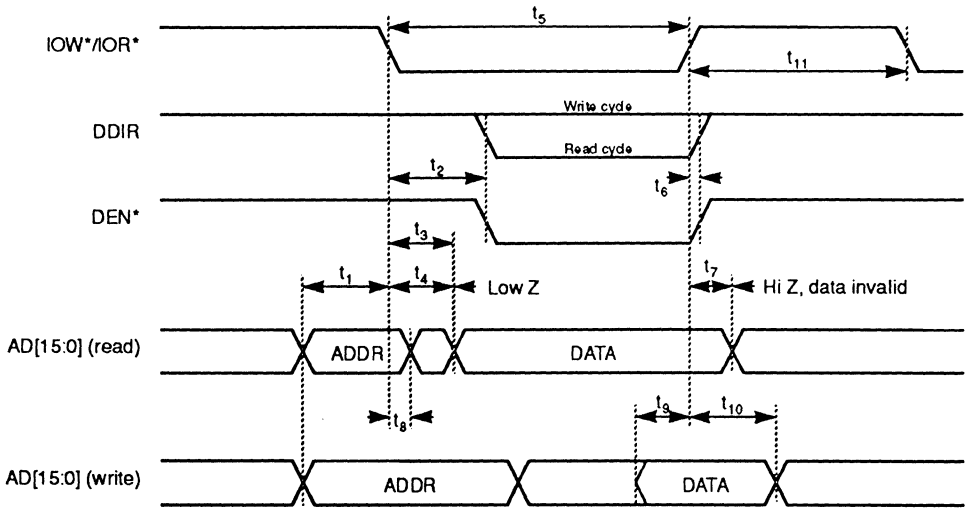
NOTE: 1. All timings assume a load of 50 pF.
2. TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

5.3.1 Index of Timing Information

5.3.2 ISA Bus Timing

Table 5-1. ISA Bus Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	AD[15:0] address valid before IOR*/IOW* active	30 ns	
t_2	Delay	IOR*/IOW* active to DEN* active, DDIR change	4 ns	20 ns
t_3	Delay	IOR* active to AD[15:0] read data out low Z	4 ns	75 ns
t_4	Delay	IOR* active to AD[15:0] read data out valid		75 ns
t_5	Pulse Width	IOR*/IOW*	100 ns	
t_6	Delay	IOR*/IOW* inactive to DEN* inactive, DDIR change	4 ns	20 ns
t_7	Delay	IOR* inactive to AD[15:0] read data invalid	4 ns	20 ns
t_8	Hold	AD[15:0] address valid after IOR*/IOW* active	4 ns	
t_9	Setup	AD[15:0] write data valid before IOW* inactive	50 ns	
t_{10}	Hold	AD[15:0] write data valid after IOW* inactive	4 ns	
t_{11}	Delay	IOW*/IOR* inactive to IOW*/IOR* active	80 ns	



NOTE: AEN must be low during cycle.

Figure 5-1. ISA Bus — I/O Timing

5.3.3 MCA Bus Timing

Table 5-2. MCA Bus Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	AD[15:0] address valid before ADL* active	40 ns	
t_2	Setup	S0*, S1* valid before ADL* active	7 ns	
t_3	Pulse Width	ADL*	35 ns	
t_4	Hold	S0*, S1* from ADL* inactive	20 ns	
t_5	Hold	AD[15:0] address from ADL* inactive	25 ns	
t_6	Hold	M/IO* from ADL* inactive		
t_7	Setup	AD[15:0] address valid before CMD* active	80 ns	
t_8	Setup	S0*, S1* valid before CMD* active	50 ns	
t_9	Setup	ADL* active before CMD* active	35 ns	
t_{10}	Hold	AD[15:0] address from CMD* active	25 ns	
t_{11}	Hold	S0*, S1* from CMD* active	25 ns	
t_{12}	Setup	AD[15:0] write data valid before CMD* active	15 ns	
t_{13}	Hold	AD[15:0] write data valid from CMD* inactive	0 ns	
t_{14}	Delay	CMD* active to AD[15:0] read data valid	45 ns	
t_{15}	Delay	CMD* inactive to AD[15:0] read data invalid	0 ns	
t_{16}	Delay	CMD* inactive to AD[15:0] read data high Z		30 ns
t_{17}	Delay	CMD* active to DEN* active/DDIR change		35 ns
t_{18}	Delay	CMD* inactive to DEN* inactive/DDIR change		20 ns
t_{19}	Delay	CMD* inactive to CMD* active		
t_{20}	Pulse Width	CMD*	90 ns	
t_{21}	Delay	AD[15:0] address, M/IO* valid to CDSFDBK* active		55 ns
t_{22}	Delay	AD[15:0] address, M/IO* invalid to CDSFDBK* inactive	0 ns	
t_{23}	Setup	CDSETUP* active before ADL* active	10 ns	
t_{24}	Hold	CDSETUP* active after CMD* active	25 ns	
t_{25}	Hold	CDSETUP* active after ADL* inactive	20 ns	

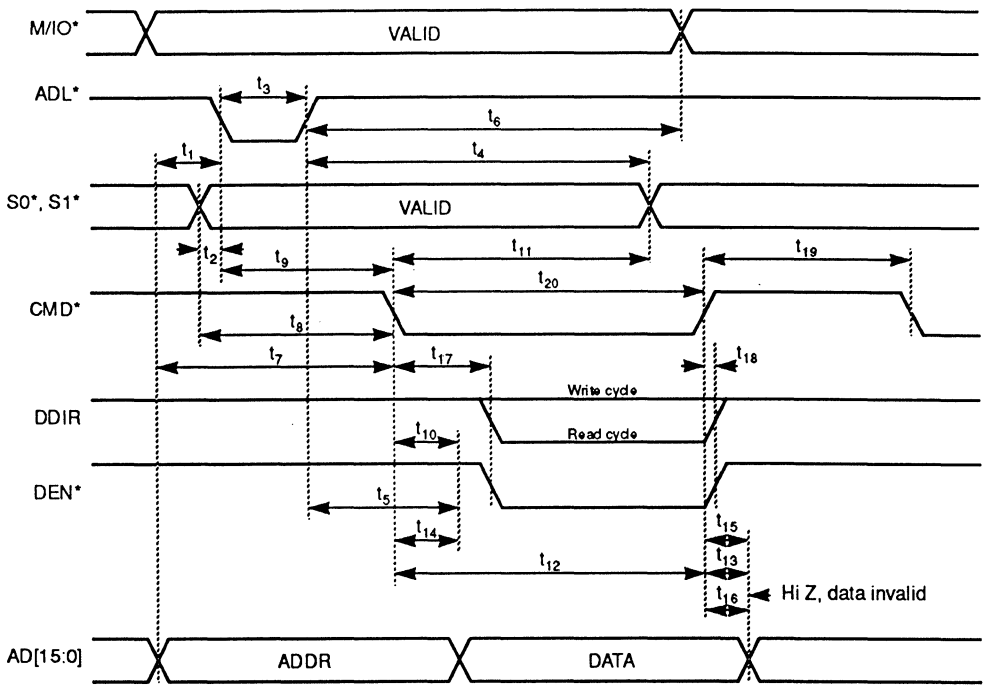
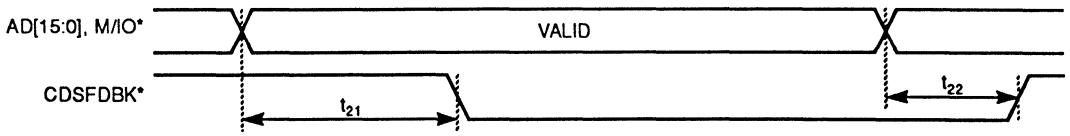


Figure 5-2. MCA Bus — I/O Timing



NOTE: Slaves do not drive CDSFDBK* when they are selected by the 'card setup' signal.

Figure 5-3. MCA Bus — CDSFDBK* Timing

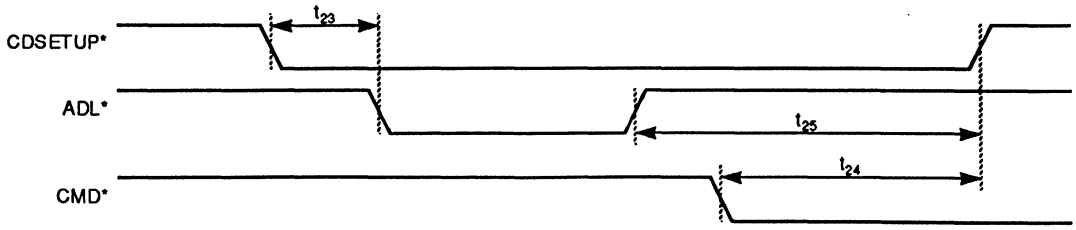
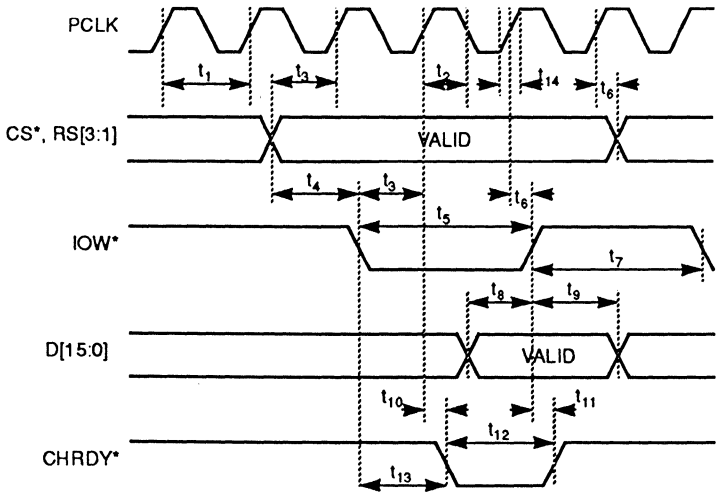


Figure 5-4. MCA Bus — CDSETUP* Timing

5.3.4 Local Hardware Interface Timing

Table 5-3. Local Hardware Interface — Write Timing

Ref.	Parameter		MIN	MAX
t_1	Period	PCLK	50 ns	
t_2	Pulse Width	PCLK	12 ns	
t_3	Setup	IOW*, CS* before PCLK rising edge	10 ns	
t_4	Setup	CS*, RS[3:1] before IOW* active	1 cycle	
t_5	Pulse Width	IOW*	2 cycles	
t_6	Hold	PCLK rising edge to IOW*, CS* transition	2 ns	
t_7	Delay	IOW* inactive to IOW* active	2 cycles	
t_8	Setup	D[15:0] valid before IOW* inactive	15 ns	
t_9	Hold	CS*, RS[3:1], D[15:0] valid to IOW* inactive	2 ns	
t_{10}	Delay	PCLK rising edge to CHRDY* active	4 ns	20 ns
t_{11}	Delay	IOW* inactive to CHRDY* inactive	4 ns	20 ns
t_{12}	Pulse Width	CHRDY*	1 cycle	2 cycles
t_{13}	Delay	IOW* active to CHRDY* active	1 cycle	1 cycle
t_{14}	Transition	PCLK		5 ns



NOTES: Timing is shown relative to clock. Internally, D[15:0], IOW*/IOR*, RS[3:1] must be stable for the entire cycle following CS* active. D[15:0] is sampled on the 2nd rising edge after CS* is asserted.

CS*, IOW*, RS[3:1] must be asserted.

If IOW* exceeds 2 cycles, CHRDY* is negated after 2 cycles. In this case, t_{11} is referenced to PCLK.

Figure 5-5. Local Hardware Interface — Write Timing

Table 5-4. Local Hardware Interface — Read Timing

Ref.	Parameter		MIN	MAX
t_1	Period	PCLK	50 ns	
t_2	Pulse Width	PCLK	12 ns	
t_3	Setup	IOR*, CS* active before PCLK rising edge	12 ns	
t_4	Setup	CS*, RS[3:1] valid before IOR* active	1 cycle	
t_5	Pulse Width	IOR*	3 cycles	
t_6	Hold	PCLK rising edge to IOR* inactive, CS* inactive	2 ns	
t_7	Delay	IOR* inactive to IOR*/IOW* active	2 cycles	
t_8	Delay	IOR* active to D[15:0] low impedance	4 ns	20 ns
t_9	Delay	IOR* active to D[15:0] valid	4 ns	40 ns
t_{10}	Hold	IOR* inactive to D[15:0], CS*, RS[3:1] invalid	2 ns	
t_{11}	Delay	PCLK rising edge to CHRDY* active	4 ns	20 ns
t_{12}	Delay	IOR* active to CHRDY* active	1 cycle	1 cycle
t_{13}	Pulse Width	CHRDY*	2 cycles	2 cycles
t_{14}	Delay	PCLK rising edge to CHRDY* inactive	4 ns	20 ns
t_{15}	Delay	IOR* inactive to D[15:0] high impedance	2 ns	20 ns
t_{16}	Transition	PCLK		5 ns

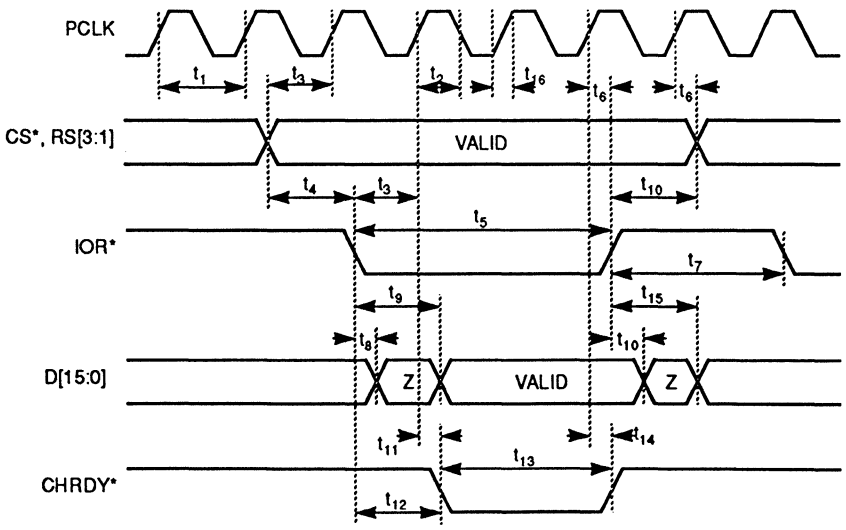


Figure 5-6. Local Hardware Interface — Read Timing

5.3.5 Video Port Timing

Table 5-5. Video Port Timing

Ref.	Parameter		MIN	MAX
t_1	Period	VnCLK	33 ns	
t_2	Pulse width	VnCLK high	12 ns	
t_3	Setup	VnPH before VnCLK rising edge	10 ns	
t_4	Hold	VnPH from VnCLK rising edge	2 ns	
t_5	Delay	VnD[15:0] output, VnVS/VnHS/VnBL valid after VnCLK rising edge	5 ns	15 ns
t_6	Delay	VnIEN* valid after VnCLK rising edge	5 ns	15 ns
t_7	Transition	GPCLK		5 ns
t_8	Transition	SBCLK		5 ns
t_9	Setup	VnD[15:0] input, VnVS/VnHS/VnBL before VnCLK rising edge	10 ns	
t_{10}	Hold	VnD[15:0] input, VnVS/VnHS/VnBL after VnCLK rising edge	2 ns	
t_{11}	Transition	VnCLK		5 ns
t_{12}	Setup	STALLRQ* active before V2CLK rising edge	10 ns	
t_{13}	Hold	STALLRQ* active after V2CLK rising edge	2 ns	
t_{14}	Hold	STALL* valid after V2CLK rising edge	7 ns	20 ns
t_{15}	Hold	STALL* invalid after V2CLK rising edge	7 ns	20 ns
t_{16}	Pulse Width	GPCLK high	4 ns	
t_{17}	Pulse Width	GPCLK low	4 ns	
t_{18}	Period	GPCLK	12.5 ns	12.5 ns
t_{19}	Setup	GHS, GVS, GBL before GPCLK rising edge	10 ns	
t_{20}	Hold	GHS, GVS, GBL after GPCLK rising edge	2 ns	
t_{21}	Delay	FCLK rising edge after GPCLK rising edge	5 ns	15 ns
t_{22}	Delay	SBCLK rising edge after GPCLK rising edge	5 ns	15 ns
t_{23}	Delay	SBCLK low from GPCLK rising edge	5 ns	15 ns
t_{24}	Delay	FCLK low from GPCLK rising edge	5 ns	15 ns
t_{25}	Delay	SBCLK rising edge from FCLK	0 ns	5 ns
t_{26}	Setup	FRDY valid before GPCLK rising edge	10 ns	
t_{27}	Hold	FRDY valid after GPCLK rising edge	2 ns	
t_{28}	Setup	ZC[3:0] valid before FCLK rising edge	10 ns	
t_{29}	Hold	ZC[3:0] valid after FCLK rising edge	2 ns	

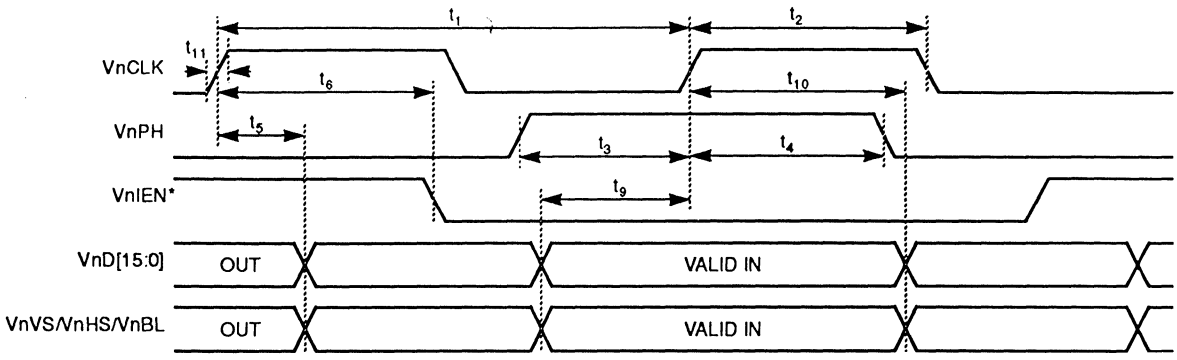


Figure 5-7. Video I/O Timing

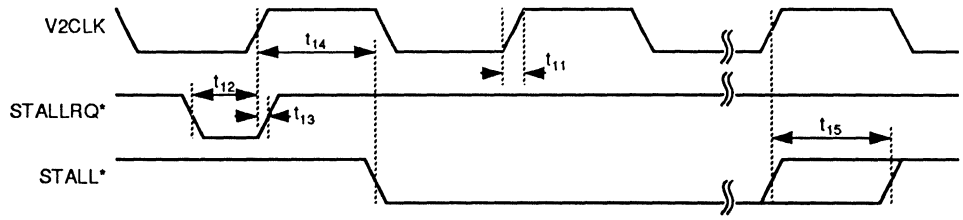


Figure 5-8. STALL* and STALLRQ* Timing

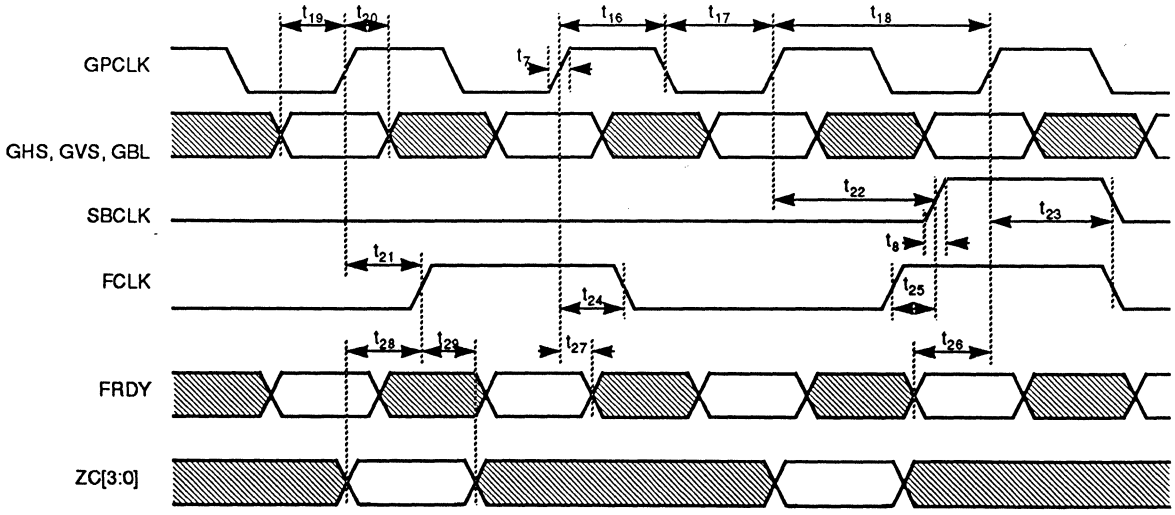


Figure 5-9. Video and Graphics Port Timing

5.3.6 Memory Timing

Table 5-6. Read Transfer Cycle Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	FBA[9:0] row address valid before RAS* active	160 ns	
t_2	Hold	FBA[9:0] row address valid after RAS* active	22 ns	
t_3	Setup	FBA[9:0] column address valid before CAS* active	6 ns	
t_4	Hold	FBA[9:0] column address valid after CAS* active	22 ns	
t_5	Setup	SBCLK falling edge (static interval) before RAS* active	86 ns	
t_6	Delay	RAS* active to CAS* active to SBCLK active	38 ns	
t_7	Delay	RAS* inactive to SBCLK active	86 ns	
t_8	Pulse Width	CAS*	22 ns	
t_9	Pulse Width	RAS[1:0]*	86 ns	
t_{10}	Period	MCLK	16 ns	
t_{11}	Transition	MCLK		5 ns
t_{12}	Setup	DTE* active to RAS[1:0]* active	10 ns	
t_{13}	Delay	RAS[1:0]* inactive to DTE* inactive		

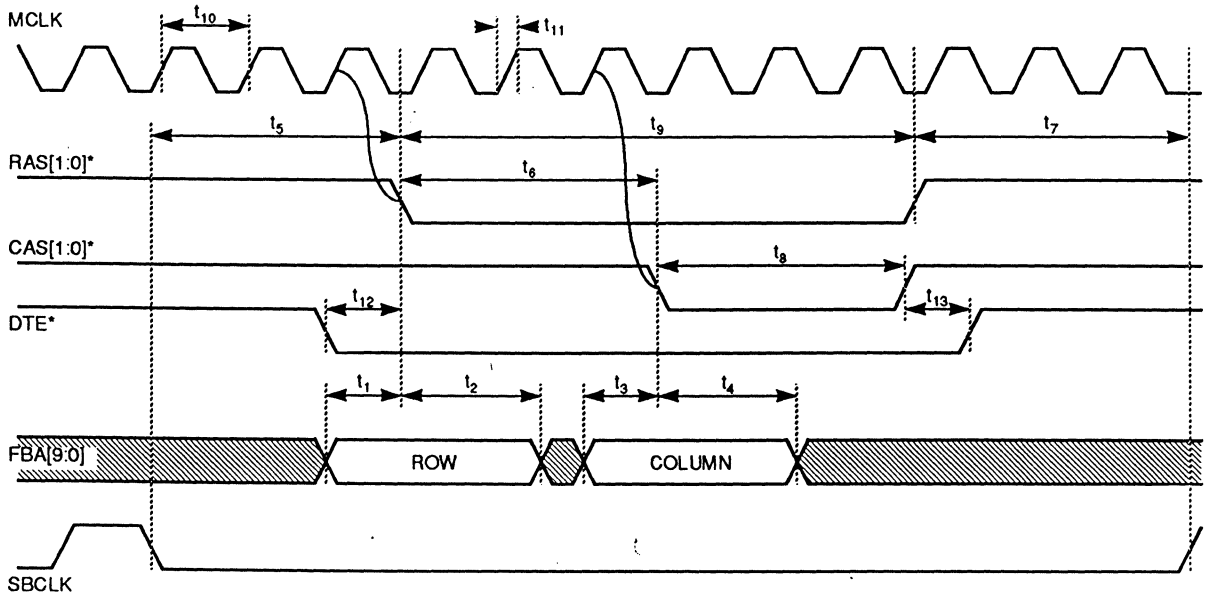


Figure 5-10. Read Transfer Cycle Timing

Table 5-7. CAS* Before RAS* Refresh Timing

Ref.	Parameter		MIN	MAX
t_1	Pulse Width	RAS1*	86 ns	
t_2	Pulse Width	RAS0*	86 ns	
t_3	Delay	CAS* active to RAS1* active	38 ns	
t_4	Delay	CAS* active to RAS0* active	38 ns	
t_5	Period	MCLK	16 ns	
t_6	Transition	MCLK		5 ns

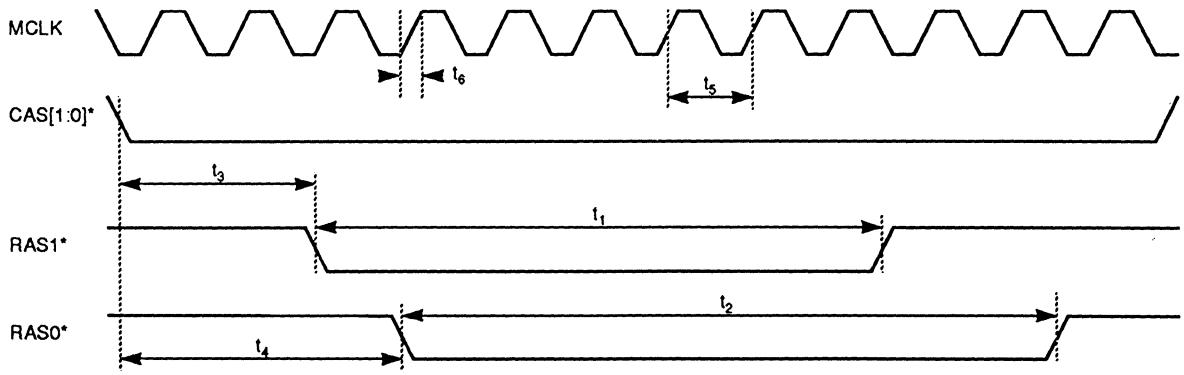


Figure 5-11. CAS* Before RAS* Refresh Timing

Table 5-8. Memory Read and Write Timing

Ref.	Parameter		MIN	MAX
t_1	Period	MCLK	16 ns	
t_2	Transition	MCLK		5 ns
t_3	Pulse Width	MCLK low	6 ns	
t_4	Setup	FBA[9:0] row address valid before RAS* active	6 ns	
t_5	Hold	FBA[9:0] row address valid after RAS* active	22 ns	
t_6	Setup	FBA[9:0] column address valid before CAS* active	6 ns	
t_7	Hold	FBA[9:0] column address valid after CAS* active	22 ns	
t_8	Delay	RAS* active to CAS* active	38 ns	
t_9	Delay	CAS* inactive to CAS* active (precharge)	11 ns	
t_{10}	Hold	RAS* active from CAS* active	38 ns	
t_{11}	Delay	RAS* inactive to RAS* active (precharge)	86 ns	
t_{12}	Pulse Width	CAS*	27 ns	
t_{13}	Setup	WE* inactive before RAS* active	38 ns	
t_{14}	Delay	FBD[31:0] valid after CAS* active (CAS* access time)	22 ns	
t_{15}	Hold	FBD[31:0] valid after CAS* inactive	0 ns	
t_{16}	Delay	FBD[31:0] valid after DTE* active	38 ns	
t_{17}	Setup	WE* active before CAS* active	6 ns	6 ns
t_{18}	Pulse Width	CAS*	27 ns	
t_{19}	Hold	WE* active from CAS* active	70 ns	
t_{20}	Setup	FBD[31:0] write valid before CAS* active	6 ns	
t_{21}	Hold	FBD[31:0] write valid after CAS* active	22 ns	

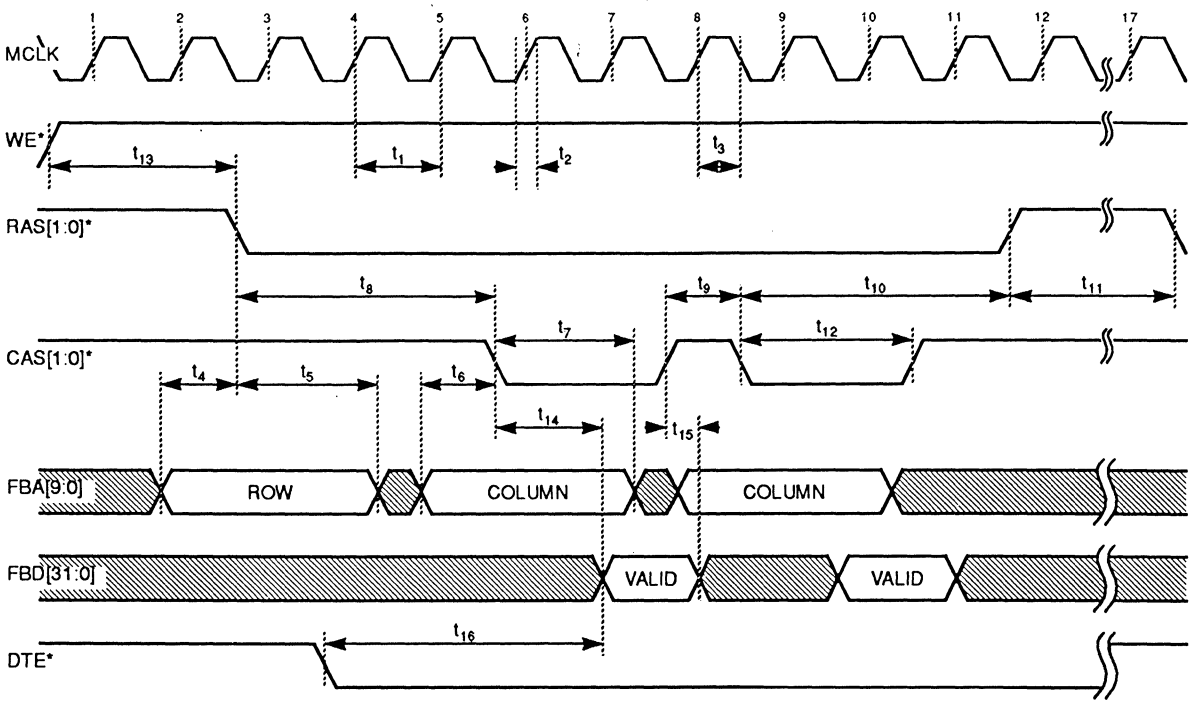


Figure 5-12. Memory Read Timing

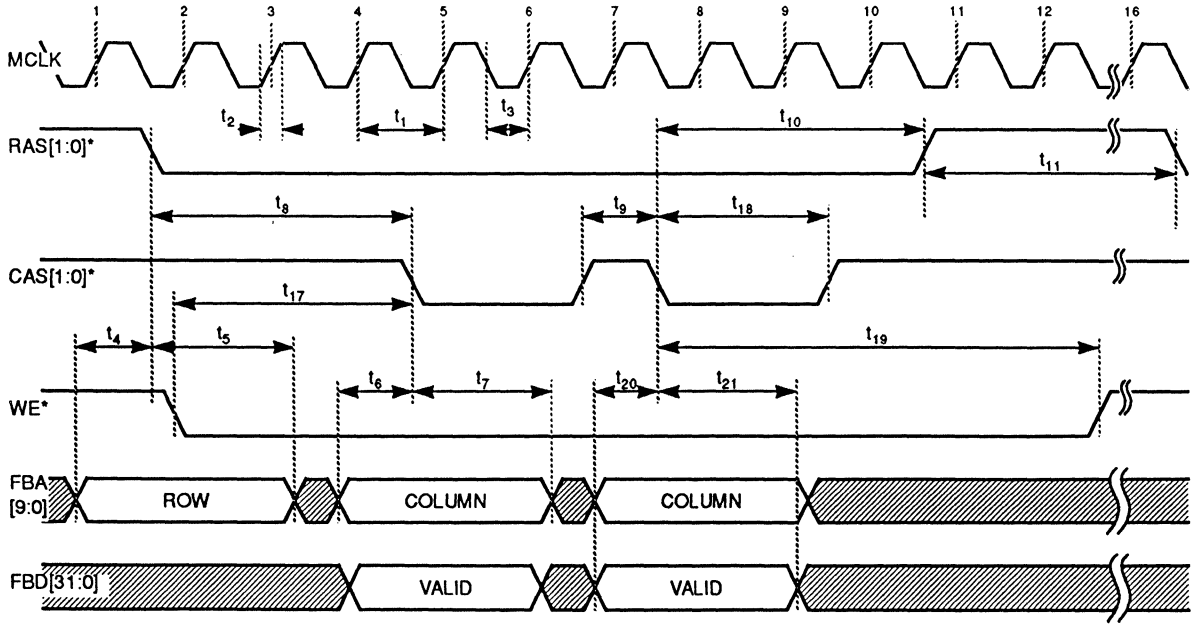


Figure 5-13. Memory Write Timing

6. PACKAGE DIMENSIONS — 160-Lead PQFP

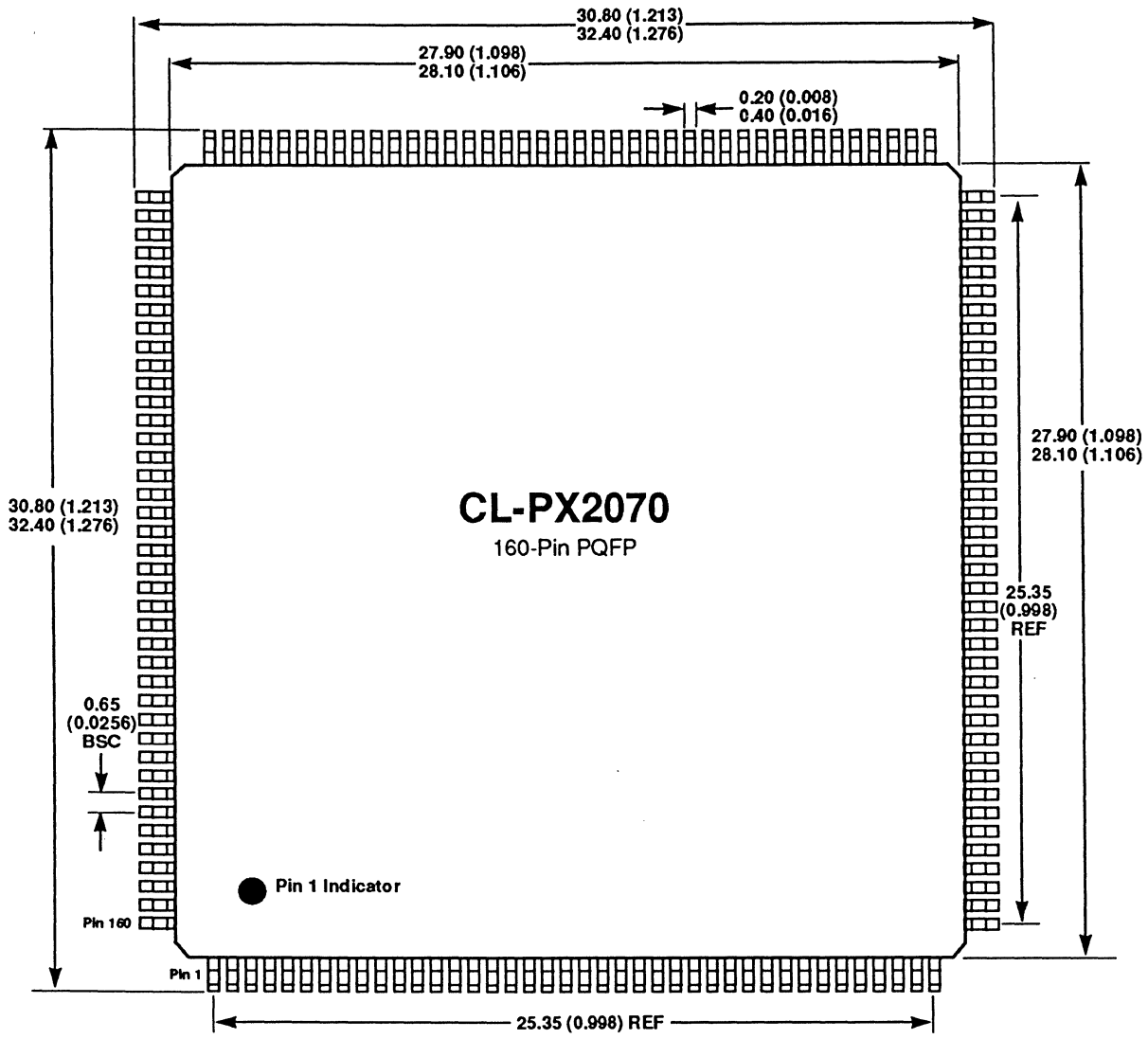


Figure 6-1. DVP Package Information

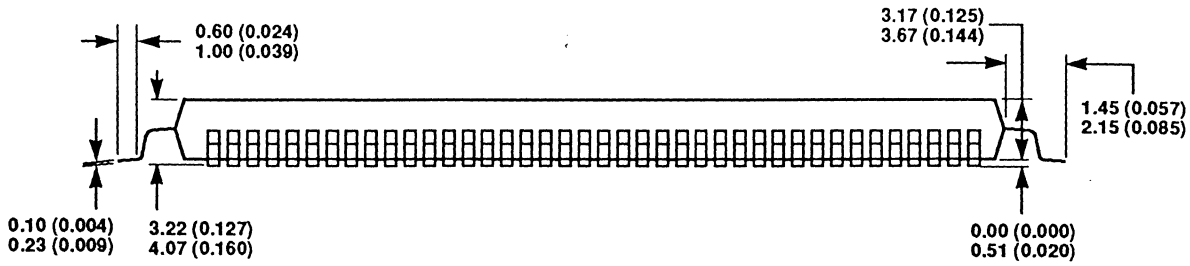
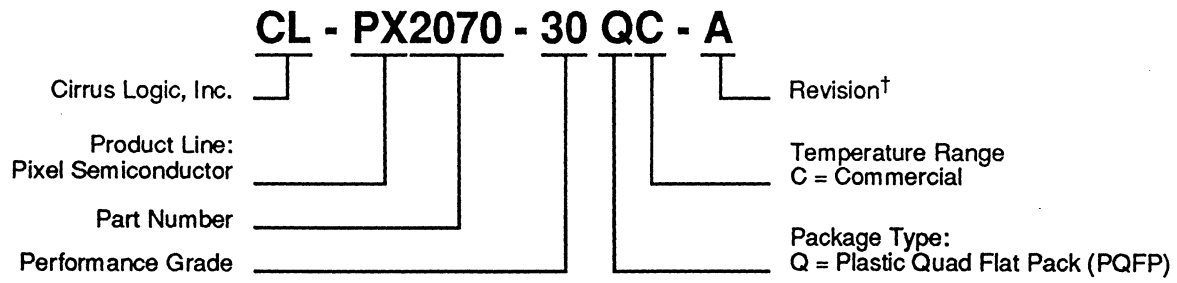


Figure 6-2. DVP Package Information (Expanded View)

7. ORDERING INFORMATION

When ordering the CL-PX2070 DVP, use the following format:



† Contact Cirrus Logic, Inc., for up-to-date information on revisions.

APPENDIX A. DVP REGISTERS — QUICK REFERENCE

HIU: Host Interface Unit

HIU_CSU	27C0	15:12	RSVD
	0290	11:8	VER
		7:6	RSVD
		5:3	HSB
		2	RSVD
		1	FBT
		0	PAS
HIU_DBG	27C0	15:10	RSVD
	0290	9	DRE
		8:0	RSVD
HIU_DRD	27C0	15	EDT
	0290	14:10	XC
		9:5	YC
		4:0	SIMIN
HIU_OCS	27C2	15	RSVD
	0292	14	FDNE
		13	FFNF
		12	RSVD
		11	SRC
		10	MDE
		9	DPC
		8	MPC
		7	PMC
		6:5	RSVD
		4	SR
		3:0	IEM
HIU_IRQ	27C2	15:6	RSVD
	0292	5	OBT
		4	IP2C
		3	IP1C
		2	FUN
		1	FOV
		0	WDT
HIU_RIN	27C4	15	AIC
	0294	14:0	RIN
HIU_RDT	27C6	15:0	DIO
	0296		
HIU_MDT	27C8	15:0	MIO
	0298		
HIU_ISU	0001	15:14	RSVD
		13:11	IP2S
		10:8	IP1S
		7:0	OBIS

VBU: Video Bus Unit

VIU_MCRp	1000	15	STM
	1001	14	OFP
		13:12	OSS
		11	OVSP
		10	OHSP
		9	OBP
		8	OBT
		7	IFP
		6	ISS
		5	IVSP
		4	IHSP
		3	IBP
		2	IBT
		1:0	IOM
VIU_DPCf	1002	P 15:12	RSVD
	1003	11:9	VSUDC
		8:6	IPU1DC
		5:3	IPU2DC
		2:0	ODC
VIU_WDT	1004	P 15	RSVD
		14	MMS
		13:11	MFTS
		10	WTE
		9:0	TMOUT
VIU_TEST	1006	15	MF
		14	MFID
		13:11	RSVD
		10	OBIN
		9	OVS
		8	OHS
		7	OBL
		6	OFID
		5	I2VS
		4	I2BL
		3	I2FID
		2	I1VS
		1	I1BL
		1	I2FID
VSU_HSW	1100	P 15:7	RSVD
		6:0	HSW
VSU_HAD	1101	P 15:10	RSVD
		9:0	HAD
VSU_HAP	1102	P 15:11	RSVD
		10:0	HAP
VSU_HP	1103	P 15:10	RSVD
		9:0	HP
VSU_VSW	1104	P 15:7	RSVD
		6:0	VSW
VSU_VAD	1105	P 15:10	RSVD
		9:0	VAD
VSU_VAP	1106	P 15:11	RSVD
		10:0	VAP
VSU_VP	1107	P 15	SGE
		14	SSE
		13	VFL
		12:10	RSVD
		9:0	VP

VPU: Video Processor Unit

VPU_MCR	2000	P 15:13	RSVD
		12	ALUE
		11:8	OPFSS
		7:4	IP2FSS
		3:0	IP1FSS
IPU1_PIX	2100	15:11	RSVD
		10:0	PC
IPU1_LIC	2101	15:11	RSVD
		10:0	LC
IPU1_FLC	2102	15	RSVD
		15:0	FC
IPU1_LIR	2103	15:11	RSVD
		10:0	IRLC
IPU1_FIR	2104	15	FCE
		14:0	IRFC
IPU1_LRB	2200	15:8	RSVD
		7:0	LRB
IPU1_LRD	2201	15:8	RSVD
		7:0	LRD
IPU1_MCRf	3000	P 15	FPS
	3100	14	IM
		13	PSE
		12	CSCE
		11	LE
		10	YSP
		9:8	ODT
		7:4	OF
		3:0	IF
IPU1_XBFf	3001	P 15:13	BF
	3101	12:0	RSVD
IPU1_XBIf	3002	P 15:11	RSVD
	3102	10:0	BI
IPU1_XEIf	3003	P 15:11	RSVD
	3103	10:0	EI
IPU1_XSFf	3004	P 15:5	SF
	3104	4:0	RSVD
IPU1_XSIf	3005	P 15:6	RSVD
	3105	5:0	SI
IPU1_YBFf	3006	P 15:13	BF
	3106	12:0	RSVD
IPU1_YBIf	3007	P 15:11	RSVD
	3107	10:0	BI
IPU1_YEIf	3008	P 15:11	RSVD
	3108	10:0	EI
IPU1_YSFf	3009	P 15:6	SF
	3109	5:0	RSVD
IPU1_YSIf	300a	P 15:6	RSVD
	310a	5:0	SI
IPU1_KFCf	300b	P 15:8	RSVD
	310b	7:0	KEYFC
IPU1_MMYf	300c	P 15:8	YRMAX
	310c	7:0	YRMIN
IPU1_MMUf	300d	P 15:8	UGMAX
	310d	7:0	UGMIN
IPU1_MMVf	300e	P 15:8	VBMAX
	310e	7:0	VBMIN

IPU2_PIX	2300		15:11	RSVD
			10:0	PC
IPU2_LIC	2301		14:11	RSVD
			10:0	LC
IPU2_FLC	2302		15	RSVD
			14:0	FC
IPU2_LIR	2303		15:11	RSVD
			10:0	IRLC
IPU2_FIR	2304		15	FCE
			14:0	IRFC
IPU2_MCRf	3200	P	15	FPS
	3300		14	IM
			13	PSE
			12:0	RSVD
IPU2_XBIf	3202	P	15:11	RSVD
	3302		10:0	BI
IPU2_XEIf	3203	P	15:11	RSVD
	3303		10:0	EI
IPU2_YBIf	3207	P	15:11	RSVD
	3307		10:0	BI
IPU2_YEIf	3208	P	15:11	RSVD
	3308		10:0	EI
SIU_MCR	2800		15:14	RSVD
			13:12	SE
			11:10	FT
			9:5	SI2
			4:0	SI1
SIU_FCS	2801		15:14	RSVD
			13	FGF
			12	FGE
			11	FFF
			10	FFE
			9	FEF
			8	FEE
			7	FDF
			6	FDE
			5	FCF
			4	FCE
			3	FBF
			2	FBE
			1	FAF
			0	FAE
SIU_FOU	2802		15:14	RSVD
			13	FGO
			12	FGU
			11	FFO
			10	FFU
			9	FEO
			8	FEU
			7	FDO
			6	FDU
			5	FCO
			4	FCU
			3	FBO
			2	FBU
			1	FAO
			0	FAU
SIU_FAR	4001		15:7	RSVD
			6	FGR
			5	FFR
			4:0	RSVD
SIUs_SIM	2e00...		15:14	RSVD
	2e1f		13:9	OTN
			8	EP
			7:4	FA
			3:0	OBA
ALU_MCRf	2900	P	15	GBM
	2901		14:13	TF
			12:9	AOP
			8:7	YOUT
			6:5	UOUT
			4:3	VOUT
			2	OPCS
			1	OPBS
			0	OPAS
ALU_TOP	2902	P	15:8	CTC
			7:0	OTC
ALU_AV	2903	P	15:8	RSVD
			7:0	AV
ALU_LOPx	2904...	P	15:0	MLOP
	2906			
ALU_CAx	2907	P	15:9	RSVD
	2908		8	TAG
	2909		7:0	CON
ALU_CBx	290a	P	15:9	RSVD
	290b		8	TAG
	290c		7:0	CON
ALU_CCx	290d	P	15:9	RSVD
	290e		8	TAG
	290f		7:0	CON
OPU_MCRf	2a00	P	15	FPS
	2b00		14	IM
			13	ZE
			12:11	RSVD
			10	LSM
			9:4	RSVD
			3:0	IF
OPU_XBIf	2a02	P	15:11	RSVD
	2b02		10:0	BI
OPU_XEIf	2a03	P	15:11	RSVD
	2b03		10:0	EI
OPU_YBIf	2a07	P	15:11	RSVD
	2b07		10:0	BI
OPU_YEIf	2a08	P	15:11	RSVD
	2b08		10:0	EI

RFU: Reference Frame Unit

MMU_MCR	4000		15:5	RSVD
			4	FBD
			3:0	FBC
OBUo_MCR	4800...	P	15:13	RSVD
	4870		12	LME
			11	CME
			10:6	OPM
			5	SSM
			4	YBDC
			3	XBDC
			2:0	FA
OBUo_RFX	4801...	P	15:11	RSVD
	4871		10:0	RFX
OBUo_LSL	4802...	P	15:0	LSL
	4872			
OBUo_LSH	4803...	P	15:7	RSVD
	4873		6:0	LSH
OBUo_BSX	4804...	P	15:11	RSVD
	4874		10:0	BSX
OBUo_BSY	4805...	P	15:11	RSVD
	4875		10:0	BSY
OBUo_DEC	4806...	P	15:8	RSVD
	4876		7	DM7
			6	DM6
			5	DM5
			4	DM4
			3	DM3
			2	DM2
			1	DM1
			0	DM0
DWU_MCR	4100	P	15	GCS
			14	OCC
			13	GFM
			12	GBP
			11	GBP
			10	GBP
			9	OCC
			8	IMS
			7:4	RSVD
			3	WC3
			2	WC2
			1	WC1
			0	WC0
DWU_HCR	4101	P	15:11	RSVD
			10:0	HAC
			15:8	RSVD
			7:0	MWS
DWUd_DZF	4400...	P	15:8	YZOOM
	4430		7:0	XZOOM
DWUd_RFX	4401...	P	15:11	RSVD
	4431		10:0	RFX
DWUd_LSL	4402...	P	15:0	LSL
	4432			
DWUd_LSH	4403...	P	15:7	RSVD
	4433		6:0	LSH
DWUd_WSX	4404...	P	15:11	RSVD
	4434		10:0	WSX
DWUd_WSY	4405...	P	15:11	RSVD
	4435		10:0	WSY
DWUd_DSX	4406...	P	15:12	RSVD
	4436		11:0	DSX
DWUd_DSY	4407...	P	15:12	RSVD
	4437		11:0	DSY

INDEX

Symbols

Numerics

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NOTES

NOTES

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

Pixel Semiconductor, Inc., a subsidiary of Cirrus Logic, Inc., is a developer of integrated circuits for advanced display systems. These circuits enable the integration of real-time video with traditional computer graphics.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

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