A Popular Embedded Control Processor Presents New Opportunities For Personal Computer Compatibility.

Bring PC Compatibility To The Intel 80C186

Many equipment manufacturers are considering moving the PC architecture from desktop to traditional embedded processor applications. There's a wide range of potential uses: consumer electronic devices, point-of-sale terminals, vending machines, industrial controllers. The architecture can also be used in such diverse areas as medical instrumentation, telecommunication systems, and electronic testing and measuring *(see "PC architecture for embedded systems").*

However, the 80186 (or 80C186), the most popular embedded 16-bit processor, isn't fully PC compatible. Until now, designers were forced to use either the less powerful 8080/8086 processor or the more complex, costly 80286 (or even the 80386). With the new VG-501/502 chip set, the popular embedded-system processor can now take full advantage of the PC's architecture with true PC compatibility. Simultaneously, the chip set supplies a substantially reduced component count and lower power consumption than the 80286/386 microprocessors, and also better performance than the 8088/8086 microprocessors.

The 80186 includes many peripheral components found in the PC, such as a direct-memory-access (DMA) controller, programmable-interrupt controller, programmable timers, clock generator, bus controller, and wait-state generator. Nevertheless, although the CPU is fully PC compatible, the architecture of the peripherals on the 80186 chip is different *(Table 1).*

PC architecture requires four DMA channels as supplied by the 8237 DMA controller. The 80186 only offers two, and they aren't 8237 compatible. The 8237 also uses a 16-bit address register and a 16-bit counter register for each channel. The 80186 has the same 16-bit counter register but uses 20-bit source and destination registers for

TABLE 1. 80186 vs. PC ARCHITECTURE

Feature	80186	PC
DMA	Two channels proprietary	Four channels (8237)
Timers	Two proprietary timers	Three timers (8253)
Interrupts	Single-level internal vector	Eight-level (8259A) external vector
Bus Cntrl	None	8288
Refresh	Internal (C186 only)	DMA channel 0

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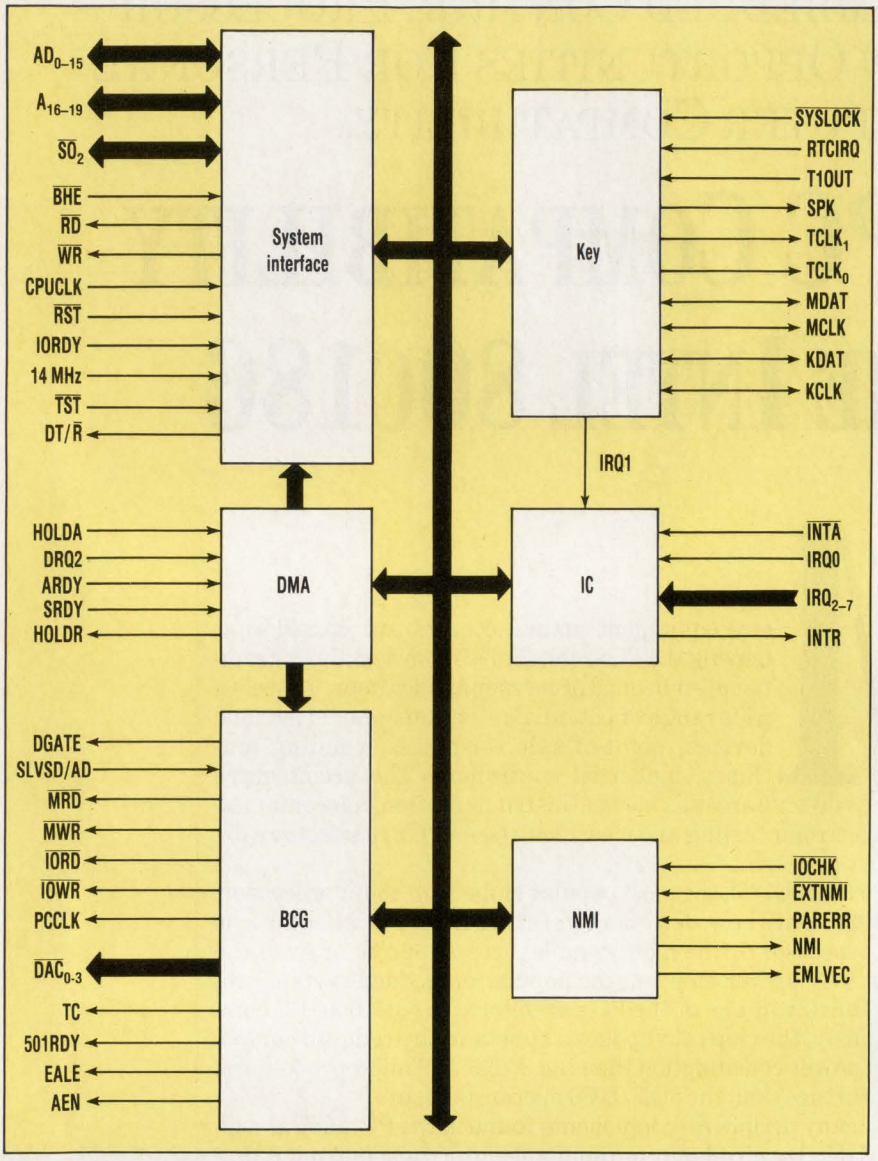
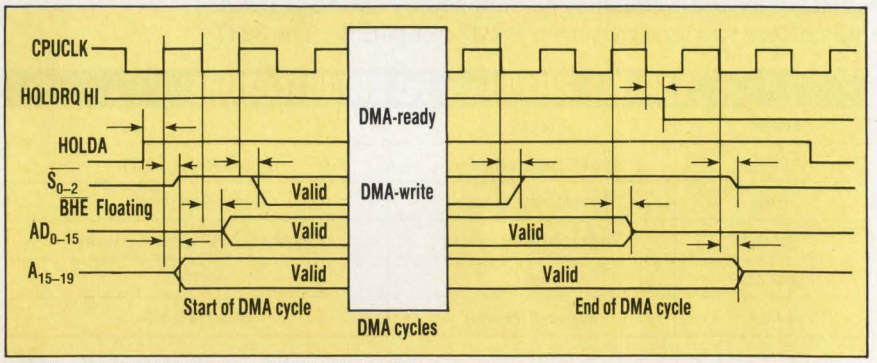


1. THE NEW VG-501/502 chip set lets the popular 80C186 take full advantage of the PC's architecture with true PC compatibility. The VG-501 chip acts as an external eight channel interrupt controller that is functionally compatible with the Intel 8259A.



2. WHEN THE CONTROLLER in the VG-501 is ready to do a DMA transfer, it issues a Hold-Request signal. Once the 80186 releases the bus and returns a Hold-Acknowledge signal, the VG-501 becomes a bus master and can perform the DMA activity.

DMA. In addition, the 8237 generates TC and DACK signals when DMA is complete; the 80186 doesn't.

Also, where the PC uses the eight-level 8259 priority-interrupt-controller chip, the interrupt controller integrated in the 80186 offers little more than one 8086 type of interrupt facility in the mode of operation closest to the PC. Consequently, for the 80186, the full capability of the 8259 must be externally duplicated. Furthermore, the two timers on the 80186 set up in different ways than the three timers on the 8253 timer chip used for the PC. A third timer must be added externally.

A COMPATIBLE 80186

Two critical elements bring PC compatibility to the 80186. The first element is extra hardware that supplements the on-board 80186 peripherals to match the configuration of the PC. Secondly, there's intercepting (trapping) and converting (if necessary) the way PC application software and hardware access peripheral components. If the PC application software is well behaved and performs all peripheral accesses through the BIOS, a special PC-compatible BIOS for the 80186 is all that is required to access the hardware with appropriate commands. But problems arise when ill behaved programs bypass the BIOS and go directly to the hardware to access the peripherals.

The PC software makers are notorious for supplying programs that wring every possible bit of performance from PCs by directly interfacing the hardware. Nevertheless, some early PC suppliers tried to supplement the 80186 hardware and use a special PC BIOS to hide the hardware differences. The few PC products released to the market that used this approach with the 80186 failed.

Fortunately, the PC architecture makes it possible to define a precise list of all possible incompatible peripheral accesses. Because the PC accesses peripherals with I/O addresses, hardware can be used to intercept the critical I/O addresses for correction *(Table 2)*. Accordingly, a hardware-based trapping mecha-

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nism in the VG-501/502 chip set saves the state of the machine in a FIFO register. It also delivers a nonmaskable interrupt (NMI) signal to the 80186 processor. Upon receiving this signal, the processor executes a short interrupt-service routine, which interrogates the FIFO register to determine the type of CPU cycle that was in progress.

Upon identifying the cycle type, the NMI-interrupt routine passes control to specific customized routines in the 80186's special BIOS. The special BIOS procedures extracts the parameters of the operation in progress. The BIOS then executes a functionally equivalent operation for the trapped command in a manner acceptable to the 80186/501/502 configuration. Afterwards, control returns to the application program. Using the NMI to trap doesn't affect the normal PC use of NMI for parity-error reporting.

Though this sequence may seem complex and slow, few instructions are needed to trap and execute an equivalent operation. Moreover, the chip-set hardware reduces the required software. Less than 1% of the overhead is used when the code is executed to correct peripheral setup. A typical operation takes less than 40 μs. Furthermore, because most PC applications employ relatively few peripheral accesses, overall performance degradation is barely noticeable.

Given the ability to detect and correct all accesses to the peripherals either through the BIOS or directly to the hardware, the next step is adding the necessary supplemental hardware to configure 80186 systems as a PC. This hardware is divided into three areas: interrupt control, DMA control, and timers.

TABLE 2. CRITICAL I/O ADDRESS FOR PERIPHERAL ACCESSES

Peripheral	I/O Address
Interrupt	20
Interrupt	21
DMA	00-0F
DMA Page	80-83
Timer	40-43
Model 30 RTC	B0-BF, E0-EF

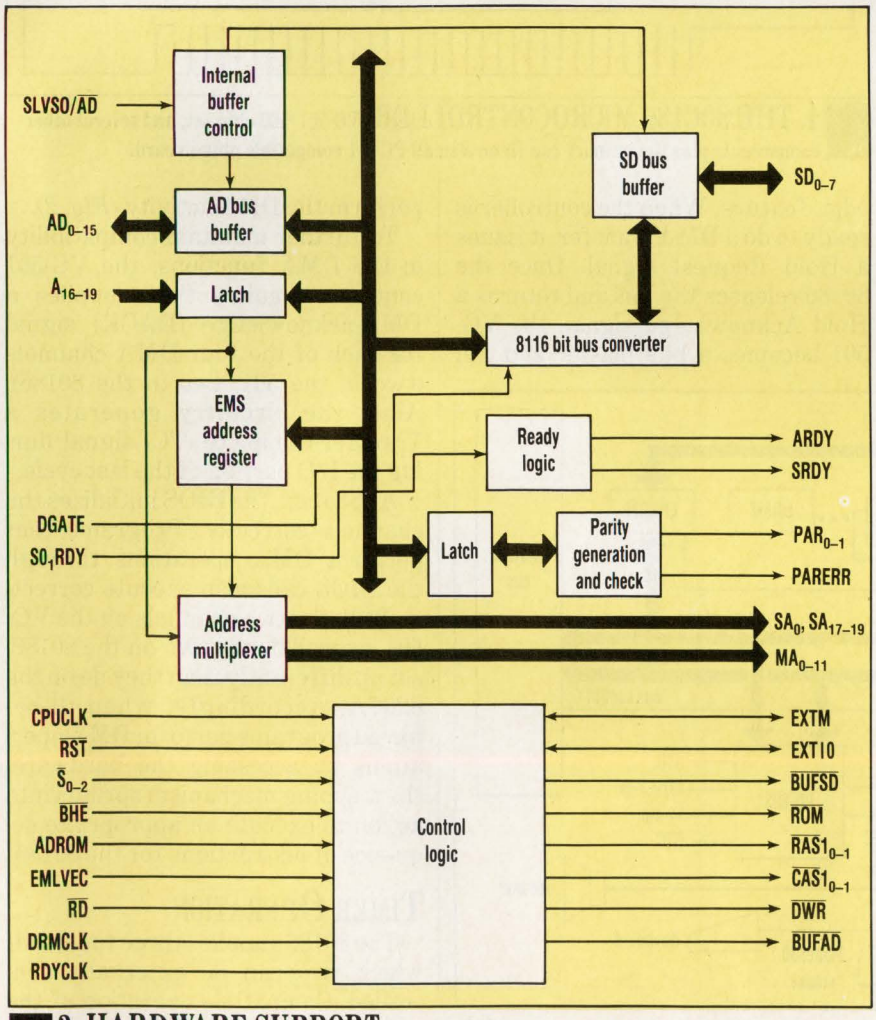
INTERRUPT CONTROLLER

The 80186 internal interrupt controller operates in several modes. All but one force the use of fixed, internal interrupt vectors. The VG-501 chip acts as an external eight-channel interrupt controller, which is functionally compatible with the Intel 8259A *(Fig. 1)*. The 80186 then operates in a mode functionally equivalent to the 8088/8086 interrupt system. Accordingly, the VG-501 typically receives interrupts intended for the 8259A in a PC-compatible system.

The VG-501 passes those interrupts on to the 80186, which is in a cascade mode. The 80186 doesn't generate internal interrupt vectors in the cascade mode, but it uses external vectors generated by the 8259A-like circuit contained in the VG-501. Of course, the 80186 requires proper initialization to enter this mode.

Seven of the VG-501 interrupt-controller channels (numbers 0 and 2 through 7) are externally accessible, and the remaining channel (number 1) connects to the VG-501's internal keyboard-mouse controller. The interrupt controller's output connects to the 80186's INT0 pin.

When the 80186 receives the interrupt, it carries out an Interrupt-Acknowledge (INTACK) cycle absorbed by the VG-501, which responds externally the same way as the 8259A. Consequently, PC-type software interrupt routines execute



3. HARDWARE SUPPORT for extended memory is built into the VG-502 chip, making it possible for transparent access to a memory space of 32 Mbytes.

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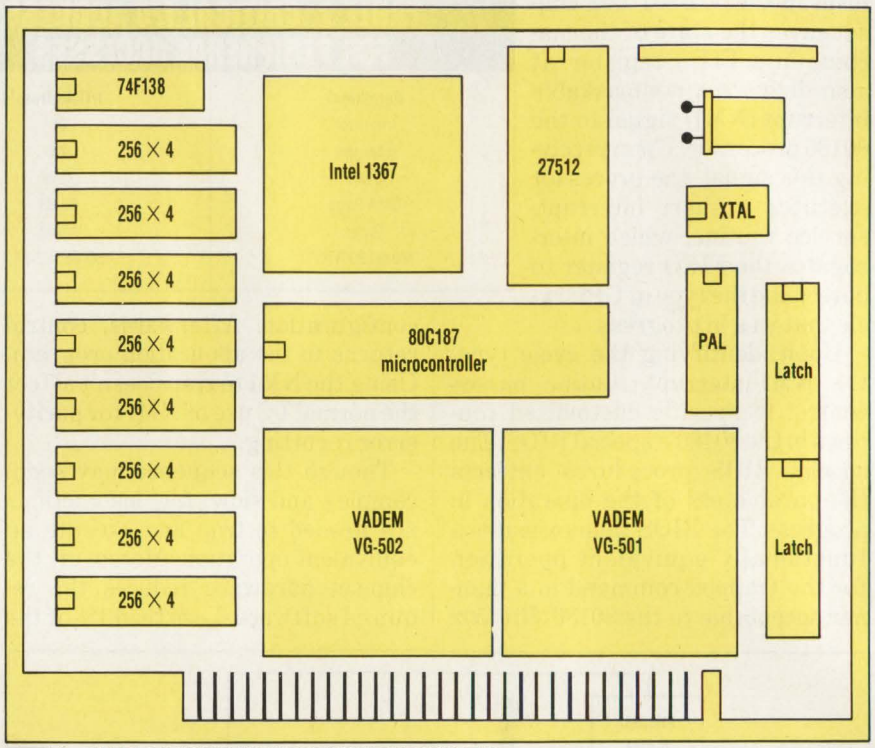
without change.

Although the interrupt controller in the VG-501/80186 functions identically with the 8259A in the PC, the VG501 interrupt controller is initialized differently. Ill-behaved programs, which attempt to access the interrupt controller directly through I/O address 20 and 21, are trapped in the hardware and corrected through the NMI structure. The BIOS handles the initialization at boot up in a normal fashion. Also, the application program, which interrogates or alters the interrupt controller operation by calls to the BIOS, operates in a normal fashion.



4. THE 80C186 MICROCONTROLLER, VG-501/502 chip set, and several other components plus the memory can fit on a small PC/XT compatible plug-in card.

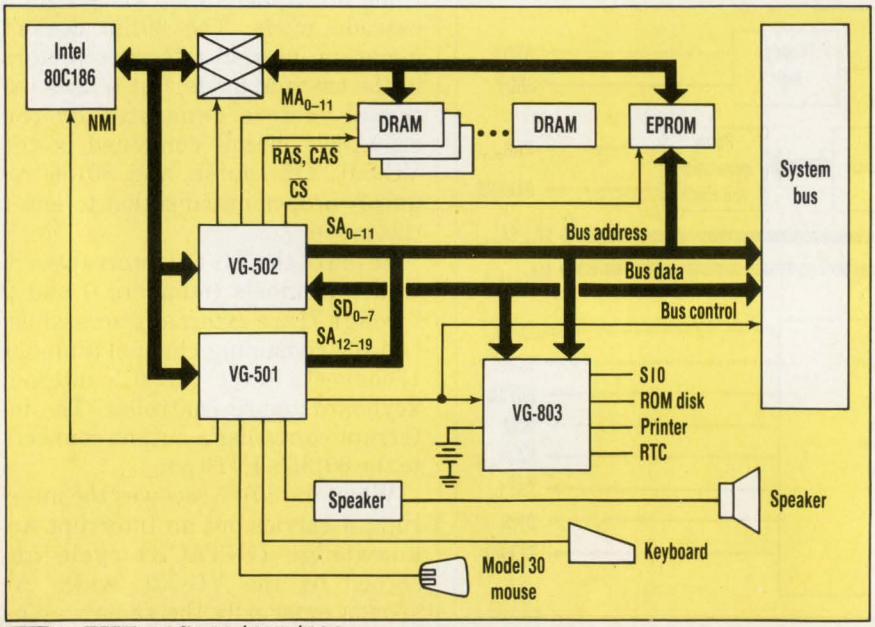
DMA Controller

The 80186 supplies two independent DMA channels, yet the PC architecture calls for four. Therefore, to make the 80186 PC compatible, the VG-501 chip includes the two additional channels. One channel transfers floppy-disk data, and is programmable in a single transfer mode compatible with the 8237A. The second channel serves refresh cycles. Though nonprogrammable, it's functionally compatible with channel 0 of the 8237A in the single transfer mode.

The VG-501's DMA controller uses the 80186 Hold Request/Acknowledge feature. When the controller is ready to do a DMA transfer, it issues a Hold Request signal. Once the 80186 releases the bus and returns a Hold Acknowledge signal, the VG-501 becomes a bus master and can perform the DMA activity *(Fig. 2)*.

To further maintain compatibility in the DMA functions, the VG-501 contains circuitry that supplies a DMA-acknowledge (DACK) signal for each of the four DMA channels (two in the 501, two in the 80186). Also, the circuitry generates a Transfer-Complete (TC) signal during the I/O portion of the last cycle.

At boot up, the BIOS initializes the channels correctly. Programs that perform DMA operations through the BIOS calls also execute correctly. Still, the two channels on the VG-501, as well as the two on the 80186, set up differently than they do on the 8237A. Accordingly, when ill-behaved programs perform DMA operations by accessing the hardware, the trapping mechanism springs into action to execute an appropriate sequence of instructions for the 80186.



5. THE 80C186/501/502 chip combination can also serve in a PS/2 Model 30 compatible system.

Timer Operation

The 80186 supplies three timers, of which two can be externally controlled. Compatible operation of the on-board 80186 timers was perhaps the most challenging problem. The

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code sequences that set up the 80186's timers differ from the 8253's timers used in the PC. As with the DMA, the BIOS handles initialization of the 80186 timers at boot up. Consequently, well-behaved programs that access the timers through BIOS calls operate correctly. Again, the NMI-trapping logic corrects the access to the timer hardware from ill-behaved PC applications that access the timer hardware directly. This underscores the importance of trapping-logic performance for the timers.

The 80186 timer channel 0 handles the system clock—the equivalent of the PC timer channel 0, and the 80186 timer channel 1 handles the speaker clock—the equivalent of the PC timer channel 2. The VG-501 supplies the inputs for these 80186 timer channels 0 and 1 by dividing the system's 14-MHz clock by 12. PC timer channel 1 normally serves as the refresh timer, a function handled completely within the VG-501.

Full control over the PC BIOS is a key element for successfully implementing an 80186-based PC. A standard off-the-shelf PC BIOS won't give the appropriate

PC ARCHITECTURE FOR EMBEDDED SYSTEMS

PC architecture isn't an obvious choice for embedded systems. PCs are generally associated with the MSDOS operating system and floppy or hard-disk drive usage. Embedded systems, however, are usually ROM based and diskless. Also, PCs don't require fast interrupt response times for handling external events. Furthermore, PC applications are single-threaded and generally deal with only one task at a time. PCs contain few elements to increase the reliability or maintainability of the system.

Nevertheless, the PC architecture isn't as bad a choice for embedded systems as it might appear. ROMable code can be written for PCs. New chip sets, BIOS developments enable existing PC applications to be based in ROM (or EPROM), whether or not the application was originally written for ROM. This capability even extends to DOS. The PC's interrupt architecture and response times are adequate for all but the most performance-intensive data gathering and control applications, and the higher speed processors now available for the PC architecture supply coverage of several of these applications.

Furthermore, a host of software companies now offer real-time multitasking operating systems for the PC architecture. They're either DOS compatible, run together with DOS, or take over the system completely. The fundamental underlying standard is the well-known PC architecture.

Because it's known that PC architecture deficiencies can be addressed for embedded applications, what are the advantages of the PC architecture? The most overwhelming gain may be the great wealth of off-the-shelf PC software and

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hardware.

Many portions of an embedded system can be purchased directly, as opposed to developed from scratch. This reduces time to market, which usually translates to higher prices, better margins, and a greater market share for the resulting product. Other factors that affect time to market include the availability of PC-compatible solutions at the box, board, and chip level. Board-level PC-compatible solutions are available for various popular bus architectures, such as the Multibus, VME, S-100, STD, and Eurocard, as well as the PC Bus. Such vendors as Ampro make a small form-factor busless single-board PC.

Even at the chip level, designs are simpler than ever due to the highly integrated chip sets available from various vendors. Embedded software can be prototyped on the ubiquitous desktop PCs before committing to EPROM for the embedded system prototyping.

Other factors favoring the PC architecture are the pricing for PC-compatible boards and chip sets that are driven by the high volume of PC sales themselves. These 10-million plus units per year bring down the manufacturing cost for PC-compatible components. Finally, the increasing attention on portable and laptop PCs is driving higher levels of integration for PC components, shrinking the size of PC implementations, and reducing power consumption to new low levels.

peripheral initialization for the 80186 and the necessary trapping code. Therefore, a special BIOS for the 80186 is needed. Without extensive PC-BIOS experience, the system designer would do best to steer clear of this task. The 80186 PC BIOS from Vadem designed to work with the VG-501/502 chip set offers full IBM PC/XT and PS/2 Model-30 compatibility.

Once the architectural approach to supplying PC compatibility with the 80186 is clear, the most difficult task is to supply adequate system performance. At initialization during boot up, and for well-behaved programs, the VG-501/502 chips' performance doesn't differ from the standard PC architecture. Ironically, those programs that access hardware directly to increase performance are the ones that impact the overhead of the trapping logic. With the timers integrated on the 80186, this is most difficult area of trapping logic.

Moreover, timer performance is most critical at slow processor-clock speeds, because the time to execute trapping code is most significant at this point. The timer adjustment for the trapping code must include the time consumed by the trapping logic, the decode logic, and the setup code. But the timers may not supply the accurate fine resolution needed at slow processor clock speeds with this VG-501/502 and 80186 approach. This problem has most impact on some game program sound effects.

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Nevertheless, it hasn't affected the correct operation of any of the hundreds of PC application programs tested to date.

In addition to the timer problem, the memory controller offered several special challenges. First, the 80C186 can operate at speeds up to 16 MHz. No other PC/XT or PS/2 Model-30 compatible processor performs at that level. While higher performance systems built around the 80286 and 80386 require 80 ns or faster dynamic RAMs, use of such expensive DRAMs with a lower cost microcontroller, such as the 80186, would defeat one purpose in selecting the 80186. Consequently, the VG-501/502 chip set highly optimizes the memory controller to work at 16 MHz, with zero wait states and DRAMs operating at 100 ns. Furthermore, the memory controller can support either 256-kbits, 1-Mbit, or 4-Mbits DRAMs in either the by-1 or by-4 configurations.

Finally, the original PC architecture systems are based on an addressable memory space of 1 Mbyte. In the DOS-compatible environment, only 640-kbytes of this space was available to application programs. Many current embedded systems seek to go beyond this 640-kbyte limitation and find the traditional DOS environment constraining. The PC system designers have evolved several extended-memory alternatives to solve the problem. The most recent, and perhaps the most popular, is the LIM (Lotus, Intel, Microsoft) standard known as EMS 4.0. Hardware support for this extended memory standard is built into the VG-502 chip, making it possible for transparent access to an extended-memory space of 32 Mbytes *(Fig. 3)*.

Accordingly, the task of supplying a full solution for 80186 usage in embedded PC-compatible systems is only slightly more difficult than supplying it for the 8086. The 80186, VG-501/502 chip set, and a few other components plus the memory can fit on a small PC/XT compatible plug-in card *(Fig.4)*. Similarly, this chip combination can serve in a PS/2 Model 30 compatible system *(Fig. 5)*. The remaining tasks are for design engineers working on embedded systems to evaluate the opportunities presented by PC compatibility for the processor, which has proven to be the most popular for embedded control applications.□

Paul Rosenfeld, Vadem's chief operating officer, has an extensive background in systems and component marketing, including seven years at Intel Corp. He holds a BA in Math from the University of California, Berkeley.

Ralph Woodard, a design engineer at Vadem, has experience both as an electronic technician and engineer. He is currently designing ASICs for PC compatible systems.

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549