```vhdl
-------------------------------------------------------------------------------
--
--  Purpose:
--
--      testbench of adder
--
--  Discussion:
--
--
--  Licensing:
--
--      This code is distributed under the GNU LGPL license.
--
--  Modified:
--
--      2012.09.14
--
--  Author:
--
--      Young W. Lim
--
--  Parameters:
--
--      Input:
--
--
--      Output:
-------------------------------------------------------------------------------

library STD;
use STD.textio.all;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

use WORK.cordic_pkg.all;
use WORK.all;


entity bshift_tb is
end bshift_tb;




architecture beh of adder_tb is

  component adder
    generic (
        WD      : in natural := 32;
        BD      : in natural := 4 );

    port (
        an      : in   std_logic_vector (WD-1 downto 0) := (others=>'0');
        bn      : in   std_logic_vector (WD-1 downto 0) := (others=>'0');
        ci      : in   std_logic := '0';
        cn      : out  std_logic_vector (WD-1 downto 0) := (others=>'0');
        co      : out  std_logic := '0');
  end component;



  begin

    add_0 : adder generic map (WD=>32, BD=>4)
      port map (an => , bn => , ci => , cn => , co => );


    clk <= not clk after half_period;
```

```vhdl
    rst <= '0', '1' after 2* half_period;


    process
    begin

    end process;


    process
    begin
      wait for 100* clk_period;
      assert false report "end of simulation" severity failure;
    end process;

--    XXXXXXX XXXXXX XXXXXX XXXXXX XXXXXXX XXXXXX XXXXX

end beh;
```