SystemC - Ports (04A)

SystemC

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Based on the following original work

- [1] Aleksandar Milenkovic, 2002 CPE 626 The SystemC Language – VHDL, Verilog Designer's Guide http://www.ece.uah.edu/~milenka/ce626-02S/lectures/cpe626-SystemC-L2.ppt
- [2] Alexander de Graaf, EEMCS/ME/CAS, 2010 SystemC: an overview ET 4351 ens.ewi.tudelft.nl/Education/courses/et4351/SystemC-2010v1.pdf
- [3] Joachim Gerlach, 2001 System-on-Chip Design with Systent of Computer Engineering http://www2.cs.uni-paderborn.de/cs/ag-hardt/Forschung/Data/SystemC-Tutorial.pdf
- [4] Martino Ruggiero, 2008 SystemC polimage.polito.it/~lavagno/codes/SystemC_Lezione.pdf
- [5] Deepak Kumar Tal, 1998-2012 SystemC Tutorial http://www.asic-world.com/systemc/index.html

Ports

- External interface of a module
- Passing data from and to processes / sub-modules
- Triggering of actions within the module
- A ports has a mode (direction) and a type

mode: in, out, inout

type: C++ type, SystemC type, user-defined type

- •Vector port / port array:
- •sc_out< int > result [32];

Mode and Type

```
// input port declaration
sc_in< type > in_port_name;

// output port declaration
sc_out< type > out_port_name;

// bidirectional port declaration
sc_inout< type > inout_port_name;
```

Port Base Class

- A port is an object through which a module, and hence its processes, can access a channel's interface
- A port type assumes a certain interface.
- A channel cannot be connected to a port if it doesn't implement the port's interface

sc_port<interface<type>, N > p;
N = number of channels that can be connected to the port

- The port base class is called sc_port
- Specialized ports can be created by refining the port base class sc port or one of the predefined port types

Predefined Port Types

- Derived from SystemC class sc_port<class IF,intN=1>
 (type of interface, number of connected interfaces)
- On the outside, ports connect to channels by means of interfaces
- Typical channel (in RTL models): sc_signal
 In this case, shortcuts exist:
 sc_in<class T>, sc_out<class T>, sc_inout<class T>
 (ports connected to N=1 interfaces of type sc_signal_in_if<class T>)
- Methods made available by the underlying interface:
 my_port.read(), my_port.write(), ...

TMP

References

- [1] Aleksandar Milenkovic, 2002 CPE 626 The SystemC Language – VHDL, Verilog Designer's Guide http://www.ece.uah.edu/~milenka/ce626-02S/lectures/cpe626-SystemC-L2.ppt
- [2] Alexander de Graaf, EEMCS/ME/CAS, 2010 SystemC: an overview ET 4351 ens.ewi.tudelft.nl/Education/courses/et4351/SystemC-2010v1.pdf
- [3] Joachim Gerlach, 2001 System-on-Chip Design with Systent of Computer Engineering http://www2.cs.uni-paderborn.de/cs/ag-hardt/Forschung/Data/SystemC-Tutorial.pdf
- [4] Martino Ruggiero, 2008 SystemC polimage.polito.it/~lavagno/codes/SystemC Lezione.pdf
- [5] Deepak Kumar Tal, 1998-2012 SystemC Tutorial http://www.asic-world.com/systemc/index.html