# Idea (2A)

- Latency Minimizing Architecture
- Multi-Phase Clock
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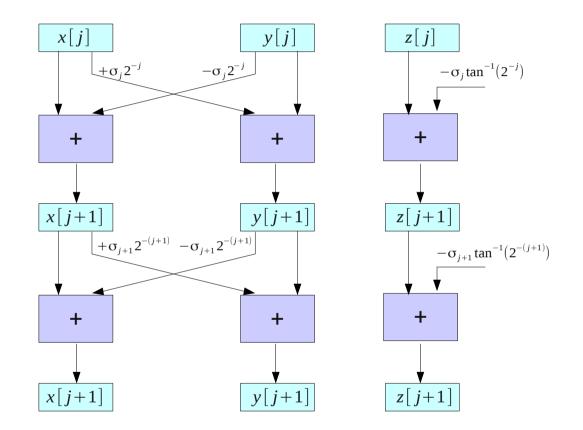
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Young Won Lim 12/12/2011

## The CORDIC Equations

$$\begin{pmatrix} x[j+1] \\ y[j+1] \end{pmatrix} = \begin{pmatrix} 1 & -\sigma_j 2^{-j} \\ +\sigma_j 2^{-j} & 1 \end{pmatrix} \begin{pmatrix} x[j] \\ y[j] \end{pmatrix}$$
$$\begin{pmatrix} x[j+2] \\ y[j+2] \end{pmatrix} = \begin{pmatrix} 1 & -\sigma_{j+1} 2^{-j-1} \\ +\sigma_{j+1} 2^{-j-1} & 1 \end{pmatrix} \begin{pmatrix} x[j+1] \\ y[j+1] \end{pmatrix}$$



### 2A Idea

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#### References

- [1] http://en.wikipedia.org/
- Branching CORDICAR (Angle Recording) CORDICAdaptive CORDIC

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