Structure (2A)

- Configuration

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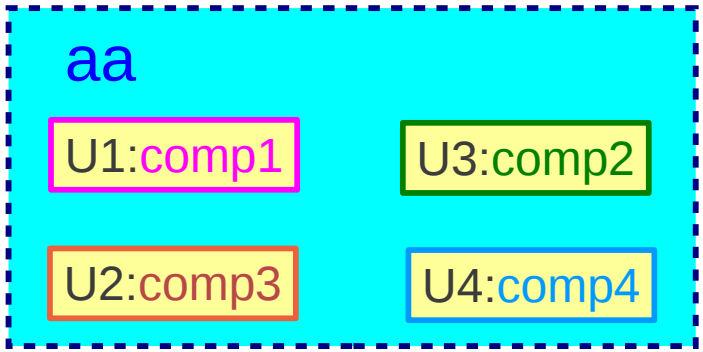
Sequential Assignment (2)



Component Declaration

```
component comp1 is
        port (        );
end comp1;

component comp2 is
        port (        );
end comp2;

component comp3 is
        port (        );
end comp3;

component comp4 is
        port (        );
end comp4;
```

```
architecture aa of ee is

begin

        Component Instantiation

        U1: comp1 port map (      );
        U2: comp2 port map (      );
        U3: comp3 port map (      );
        U4: comp4 port map (      );


end aa;
```

Default Binding

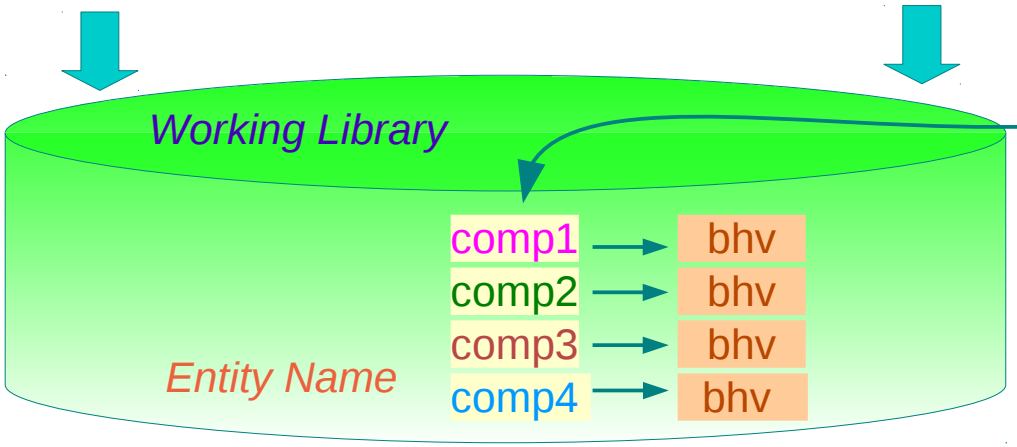
```
entity comp1 is
        port (        );
end comp1;

entity comp2 is
        port (        );
end comp2;

entity comp3 is
        port (        );
end comp3;

entity comp4 is
        port (        );
end comp4;
```

```
architecture bhv of  comp1 is
        . . .
end comp1;

architecture bhv of comp2 is
        . . .
end comp2;

architecture bhv of comp3 is
        . . .
end comp3;

architecture bhv of comp4 is
        . . .
end comp4;
```

```
architecture aa of ee is

begin

U1: comp1 port map (      );
U2: comp2 port map (      );
U3: comp3 port map (      );
U4: comp4 port map (      );

end aa;
```

Component Name

Component Name
= Entity Name

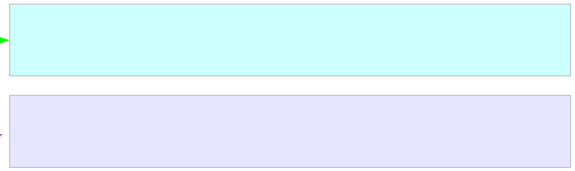


Last compiled Architecture

Configuration Specification

Component Declaration

```
component comp1 is
        port (          );
end comp1;

component comp2 is
        port (          );
end comp2;

component comp3 is
        port (          );
end comp3;

component comp4 is
        port (          );
end comp4;
```



```
architecture aa of ee is

begin

        Component Instantiation
    U1: comp1 port map (        );
    U2: comp2 port map (        );
    U3: comp3 port map (        );
    U4: comp4 port map (        );

end aa;
```

```
for   U1: comp1 use entity work.comp1(bhv);
for   U2: comp2 use entity work.comp2(bhv);
for   U3: comp3 use entity work.comp3(bhv);
for   U4: comp4 use entity work.comp4(bhv);
```

Configuration Declaration

Component Declaration

```
component comp1 is
        port (          );
end comp1;

component comp2 is
        port (          );
end comp2;

component comp3 is
        port (          );
end comp3;

component comp4 is
        port (          );
end comp4;
```

```
architecture aa of ee is

begin

        Component Instantiation

        U1: comp1 port map (      );
        U2: comp2 port map (      );
        U3: comp3 port map (      );
        U4: comp4 port map (      );


end aa;
```

```
configuration conf1 of ee is
  for aa
      for   U1: comp1 use entity work.comp1(bhv);          end for;
      for   U2: comp2 use entity work.comp2(bhv);          end for;
      for   U3: comp3 use entity work.comp3(bhv);          end for;
      for   U4: comp4 use entity work.comp4(bhv);          end for;
  end for;
end conf1;
```

Sequential Assignment (1)

Sequential Assignment (1)

Default Binding

Sequential Assignment (1)

Sequential Assignment (2)

Sequential Assignment (2)

References

[1] http://en.wikipedia.org/
[2] J. V. Spiegel, VHDL Tutorial,
http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
[3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
[4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
[5] D. Smith, HDL Chip Design
[6] http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html
[7] VHDL Tutorial - VHDL onlinewww.vhdl-online.de/tutorial/