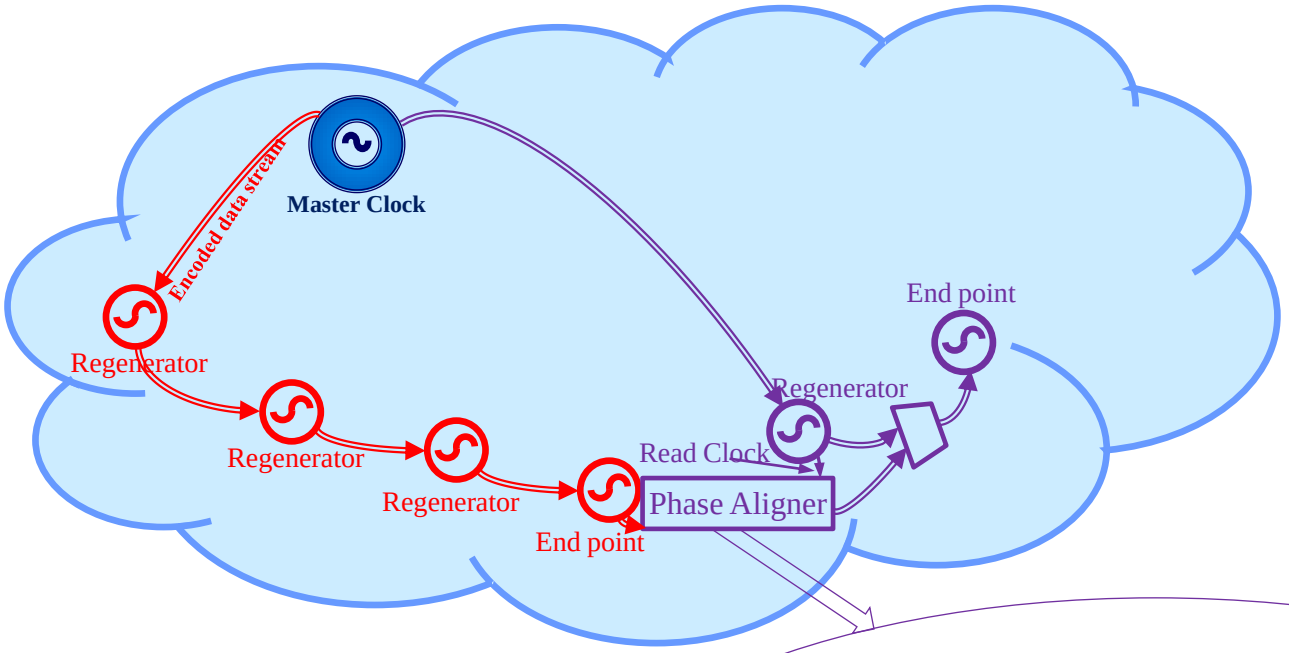
Definition of Phase Aligner

(the phase aligner normal operation involves just one clock domain)



The Phase Aligner is essentially composed of :

- **an elastic buffer and of**
- **a PLL that controls the delay (= phase) added to the incoming data stream.**

(Stricter sense of the definition of Phase Aligner)

In the actual implementation the slave CDR may be included, and possibly merged together with the other blocks of the Phase Aligner.

(Wider sense of the definition of Phase Aligner)