ELECTRONIC TRACK ALIGNMENT OF DIGITAL SIGNALS RECORDED AT HIGH DENSITY ON A MULTITRACK RECORDER

Erhard K. Kietz January 1971

Introduction

The methods used for data acquisition have shifted to a considerable extent from analog to digital for a wide variety of applications. This required the technology for temporary or permanent data storage to follow the same trend. Multichannel instrumentation tape recorders, originally designed for the storage of analog signals, can be used with minor modifications for the recording of digital signals at very high data rates and data packing densities on the tape (up to one million bits per square inch), if the data recorded on each separate track are independent of the data on the other tracks, or if data processing uses the reproduced data from a single track at a time. However, many applications, especially those using computer processing of the recorded data, require the simultaneous (parallel-track) recording and reproduction of the bits of a digital word. This technique has been used for a long time at densities of 800, 1600, and sometimes 3000 bits per inch of track length. But the requirements for higher information rates and, consequently, higher digital data rates, demand densities of 20 000, 40 000, and more bits per inch of track in order to record the information at reasonable tape speeds.

At 40 000 bits per inch, one bit is 25 microinches long on the tape. This is far less than the static and dynamic skew (interchannel time displacement) error between the tracks of a recorder. The simultaneously recorded bits of a digital word can therefore not be reproduced within a fraction of a bit period as it is the case with standard computer transports. The bits of a particular word will be displaced by many bit periods. A word alignment, or track alignment,

must therefore be applied before the data can be read correctly.

A description is given in the following two methods of electronic track alignment.

1.0 System Description

The upper part of Figure 1 shows a block diagram of a digital recording system in which a multitrack recorder is used in conjunction with electronic track alignment. This arrangement makes possible the recording and precise reproduction of a high-rate serial bit stream. Such a data input, assumed to be in NRZ-L form, is first broken down in a number of parallel streams which operate at a rate the recorder can reliably handle. Each of these n parallel streams is recorded on a separate track of the recorder, after conversion to Miller Code.* To this set of n tracks, one more track is added which carries a succession of sync words.

The timing diagram in the lower part of the figure shows on line 1 a serial bit stream with the bits sequentially numbered to be able to keep track of them through the system. Line 2 shows n = 3 parallel bit streams at 1/3 the input rate and a fourth track with the sync words. By means of proper gating in the Sync Distributor the four tracks are made to carry equal amounts of data and the sync words are distributed as shown in line 3 of the timing diagram. This method of adding one track to the n data tracks and distributing sync words and data sequentially over the (n+1) tracks obviates the large storage capacity and change of clock rates which would be necessary by the more customary method of multiplexing data and sync words in each track.

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*Also called delay modulation. The definition of the Miller Code is as follows: A binary "one" has a transition in the middle of the bit period; a binary "zero" has no transition unless it is followed by another "zero," in which case a transition occurs at the end of the bit period.

Line 4 of the timing diagram shows the recorder/ reproducer output, after reconversion of the reproduced signals from the Miller Code to NRZ. Here, the four tracks have various amounts of relative time displacements, due to the various sources of "Skew" errors in the recorder, e.g., gap scatter and azimuth differences between the recording and reproducing heads (static skew), and tape guiding imperfections (dynamic skew). It is the purpose of the Track Alignment Logic to eliminate these displacements. Two methods of achieving this will be discussed in the following paragraphs.

At point 5 of the block diagram the relative signal timing in the four tracks is exactly that which it was at point 3 during the recording process, and at point 6 the signals appear arranged as they were in point 2, except for the absence of the sync track. At point 7, the serial bit stream is restored as it was at the input of the system.

2.0 Electronic Track Alignment Using Elastic Store Memories

In the method of electronic track alignment described here, a register file memory with simultaneous write/ read capability is used in each of the tracks. A block diagram is shown in Figure 2. This block diagram refers to the particular example used in the timing diagram of Figure 1, namely, a four-track recorder with four-bit sync words.

Any one of the tracks may be chosen as reference track with respect to which the other tracks will be aligned. In the example used here, track 1 is designated as the reference track.

2.1 The Write Process

As can be seen by comparison of lines 3 and 4 of the timing diagram in Figure 1, track 2 is reproduced 2 bit periods of the input bit rate (line 1) too early, track 3 is another 2 bit periods, or a total of 4 bit periods earlier than track 1. Track 4 is one bit period late with respect to track 3, or 3 bit periods earlier than the reference track. The overall relative time displacement is therefore: -4,+0 bit periods in this example. Assume the maximum possible displacement between any two tracks, calculated from worst-case conditions of all factors contributing to the time displacements, is $\pm$12 bit periods of the input rate, or $\pm$ 4 bits of the track rate. To correct these timing errors, a 16-bit memory (also called elastic store), such as Texas Instruments 4-by-4 Register File SN 74170, is chosen. This figure of 16 bits refers to the track rate. The reason for this choice is discussed below.

Every time, a sync word in track one is received and verified by the Sync Word Recognizer (Figure 2), the Write Address Counter is reset to 0000, and the first bit after the sync word goes to that location in the memory associated with track 1. This is bit #25 (see upper track of line 4 in the timing diagram in Figure 1) The Write Address Counter is triggered by the input clock of that channel, so that the bit following next to #25, namely #28, goes to location 0001 of the memory, until the memory is loaded as follows:

Memory Location	Bit No.
0000	25
0001	28

Memory Location (cont'd)	Bit No.
0010	31
0011	34
0100	37
0101	40
0110	43
0111	46
1000	49
1001	52
1010	55
1011	58
1100	S1
1101	S2
1110	S3
1111	S4

As can be seen from the second track in line 4 of the timing diagram, the first bit after sync in this track is bit #38. It is the purpose of the memories in all the tracks to place bits which have been recorded simultaneously, according to line 3 in the timing diagram, in the same location (address). Therefore, since the sync word in track 2 is 4 bits later than the sync word in the reference track, track one, bit #38 must be addressed with 0100 in the memory for track 2. To this address, the Write Address Counter must be reset after each recognition of a sync word in track 2. Of course, after lock-up of the system has occurred, the previous bits (sync bits) are stored in the locations 00XX, so that the memory for track 2 is loaded as follows:

Memory Location	Bit No.
0000	S1
0001	S2
0010	S3
0011	S4
0100	38
0101	41
0110	44
0111	47
1000	50
1001	53
1010	56
1011	59
1100	61
1101	64
1110	67
1111	70

In track 3, the reset address must be 8 bits later than that of track one, i.e., it is 1000. In this location of the memory for track 3 will bit #51, the first bit after sync, be held, and the contents of this memory will be:

Memory Location	Bit No.
0000	26
0001	29
0010	32
0011	35
0100	S1
0101	S2
0110	S3
0111	S4

Memory Location (cont'd)	Bit No.
1000	51
1001	54
1010	57
1011	60
1100	62
1101	65
1110	68
1111	71

Similarly, the memory for track 4 contains:

Memory Location	Bit No.
0000	27
0001	30
0010	33
0011	36
0100	39
0101	42
0110	45
0111	48
1000	S1
1001	S2
1010	S3
1011	S4
1100	63
1101	66
1110	68
1111	72

2.2 The Read Process

The memories must never be fully occupied, because the write-in process is continuous and immediately after

location 1111 is filled, the next bit reproduced from the recorder in that track must go to location 0000.

2.2 The Read Process

At the instant when the memory of the reference track is filled exactly 50%, i.e., when write-in occurs at 1000, read-out of the first location, 0000, should take place. This read-out process is controlled by the clock of the reference track simultaneously for all memories. The same pulse which resets the Write Address Counter to 0000 after each sync recognition, resets the Read Address Counter to 1000 to obtain the 50% offset (See Figure 2). Therefore, the memory of the reference track is occupied exactly 50% at all times, while in the other memories the write-in process, and the amount of occupancy, vary according to the time base differences between a particular track and the reference track. If a track is reproduced from the recorder nearly maximally late, only a few addresses may be occupied in the memory associated with that track, but if the track is maximally early, nearly the entire memory may be filled up, depending on the total amount of storage provided. Since the time base differences are not constant, the occupancy of the memories varies, except that of the reference track. This is why they are called elastic stores. Each memory must therefore have a storage capacity at least equal to the peak-to-peak relative time base errors, expressed in numbers of bit periods. But, since the maximum timing differences cannot be predicted precisely, it is necessary to provide a generous margin of storage. These storage devices are usually produced with a binary number of bits. In the example treated here, an estimated relative time base error of ± 4 bit periods maximum was assumed. If this estimate was realistic, 16-bit storage elements are adequate.

3.0 Electronic Track Alignment Using Shift Registers

Another method of track alignment is characterized by the use of shift registers. Since shift registers can be assembled to form almost arbitrary amounts of delay, this approach is particularly well suited in situations where large intertrack time displacements occur, e.g., when tracks from different head stacks are be be aligned.

The principle of this method is to load a number of separate shift registers sequentially with the data reproduced from a recorder track, and to clock the data out, after an appropriate delay, with a common clock, i.e., the clock of the reference track. Figure 3 shows a block diagram which is based on the system parameters used in Section 2, i.e.,

four channels, carrying the equivalent of three data channels and one sync channel;

four-bit words;

every fourth word is a sync word;

the frame length (distance between identical bits of successive sync words) is 16 bits;

maximum intertrack time displacement: ±4 bits;

track #1 is the reference track.

As shown in the block diagram Figure 3, four shift registers, such as type 9391/7491, each having eight bits, are used per track. Considerations for the selection of the registers are given below. The sequence of events in the registers is quite similar to those described in the previous section for the elastic store memory.

Whenever a sync word is identified in track #1, a 32-step (5-bit) binary counter is reset to 00000. This counter

begins, through a set of clock gates, to clock the first eight data bits immediately following the sync word into register 1A. These first eight bits are, according to Figure 1, line 4, upper track: 25, 28, 31, 34, 37, 40, 43, and 46. Then the counter automatically switches to register 1B for the next eight bits, then to 1C, 1D, and back to 1A, where it waits for the next sync word to be reset. The fact that the last four bits in register 1B are sync bits, due to the particular choice of a short frame length in this example, makes it necessary to block every other sync word from resetting the counter.

When a sync word is identified in track #2, the counter in this track is reset to 00100. The instant of this event with respect to the events in track #1 depends on the time displacement error between these two tracks. Only if there is no mutual time displacement, bit #38, the first bit after sync, would be clocked into register 2A at the same instant bit #37 enters register 1A, since the sync in track #2 was recorded four bits later than the sync in track #1. Only data bits 38, 41, 44 and 47 enter register 2A before the counter switches to register 2B. Of course, after initial lockup, the four sync bits will be found in register 2A, ahead of bit #38. It does not appear necessary to describe the events in tracks #3 and #4.

At the moment register 1C begins to receive bits in track #1 (reference track), registers 1A, 2A, 3A, and 4A receive clock pulses from track #1, and the data gates at the output of the registers are opened to pass the bits coming from all "A" registers to the outputs. Here again, data input to the registers of track #1 and the output from the registers in track #1 are separated by exactly one-half of the total amount of storage, while the data in the other tracks may

be clocked in earlier or later with respect to the data received by the registers of track #1.

Figure 4a shows an overall timing diagram for one track of the track alignment system described here. The data clock-in process is shown in solid lines for the reference track, while the clock-out process is in dashed lines. Clocking-out occurs always at a fixed time in all tracks; the clock-in time of tracks other than the reference track can vary within the cross-hatched areas on both sides of the solid-line area. The blank area between the extreme variations of the data input and the beginning or end of the data output timing is a safety zone.

Figure 4a shows how to calculate the total amount of storage and the number of registers needed. Due to the existence of the shaded areas (time base variations) and the necessity of a safety zone, three is the minimum number of registers per track. If a safety zone of one-half of the maximum timing variation is considered adequate, the total storage needed is:

one register of x bits for writing, plus
one register of x bits for reading, plus
2 · 4 bits for time base variations, plus
2 · 2 bits for safety zones.

The storage capacity needed is therefore: $C = 2(x+6)$ bits. Since shift registers are frequently made in binary numbers per chip, x should be a binary number. Furthermore, the total storage capacity to be provided, C^1, should be an integer number of frames, so that the loading process always starts with a sync word. Another restriction, not necessary but very desirable, is that C^1 be a binary number. This simplifies the counting process in the clock counter (see Figure 3). If the

frame contains 16 bits, as in the example used here, the following table can be written:

No. of bits per register x bits	Storage capacity needed C bits	No. of frames to be stored	No. of Registers needed (per track)	Storage capacity to be provided C^1 bits
4	20	2	8	32
8	28	2	4	32
16	44	4	4	64

This makes the optimum choice in the example presented to be four eight-bit shift registers. The difference between the needed 28 and the available 32 bits makes the safety zones four bits long instead of the required two.

It should be mentioned that it is possible to design a system with three (instead of four) 16-bit shift registers as shown in the timing diagram of Figure 4b. In this case, the total capacity is 48 bits, the safety zones are four bits long. However, since 48 is not a binary number, the counters shown in the block diagram of Figure 3 are more complicated. Furthermore, because the interval between write-in and read-out (even for the reference track) does not cover an entire register of 16 bits, the gating arrangement is quite complicated. This consideration may show the importance of proper data formatting at the input of the recorder.

4.0 Bit Alignment with Respect to an External Timing Source

The two methods of electronic bit alignment described above accomplish a precise timing of all reproduced bits with respect to the clock of one of the recorded tracks which has been selected as a reference track. As a consequence, the reproduced data and their clock still contain the capstan servo error and other timing disturbances which are common to all tracks, e.g., effects of changes of tape dimensions due to variations of humidity and temperature between recording and reproduction. Since these time base errors are very slow with regard to the data rate, they are usually acceptable for computer evaluation of the data. Other applications, like visual presentation of the data from several sources (recorders) may require the alignment of the bits with respect to a stable timing signal exterior to the recorder.

To satisfy this requirement, the following steps must be taken:

a fixed relationship must be established in the recording operation between the data rate (clock frequency) of the data to be recorded and the tape speed;

the average rate of data reproduction from the tape, i.e., the average tape speed in the reproduce mode, must be controlled by the external timing source;

the electronic track alignment must eliminate not only the intertrack timing errors but, in addition, the errors of all tracks with respect to the external timing source, i.e., all variations of the data rate about the reproduced average rate mentioned above.

Modern multichannel instrumentation recorders have built-in provisions for controlling the average tape speed from external timing sources by recording the timing source on a control track and comparing the reproduced control track signal with the timing source used in the reproduce mode. These timing signals are standardized in IRIG Document 106-69, Paragraph 5.6.2.2.6. For instance, at a tape speed of 120 in/s, the control track frequency must be 200 kHz; for 60 in/s it is 100 kHz, etc.

For digital applications, the clock frequency associated with the input data must be converted in a suitable divider circuit to generate a control track frequency which is synchronous with the data and which results in the desired tape speed when fed to the EXTERNAL REFERENCE INPUT of the recorder. The tape speed to be selected is determined by the linear packing density of the data on the tape whose upper limit depends on the recorder design and the performance requirements for bit error rates.

There is no need to record a separate control track signal. The clock extracted from the reproduced signal and transformed to the required control track frequency can be used for comparison with the external timing source. The error signal derived from this comparison is used to control the tape speed.

The block diagram of Figure 5 shows these features added to the basic block diagram of Figure 1. In the record mode, the suitably divided clock frequency is connected to the EXTERNAL REFERENCE INPUT of the recorder. In the reproduce mode, the external timing source is converted into the desired output clock frequency which, through a divider, connects to the EXTERNAL REFERENCE INPUT of the recorder. In each reproduced, Ampex-coded data track the clock is extracted and used for decoding and for electronic track alignment. The clock from any one of these tracks is also used, through a divider and connection

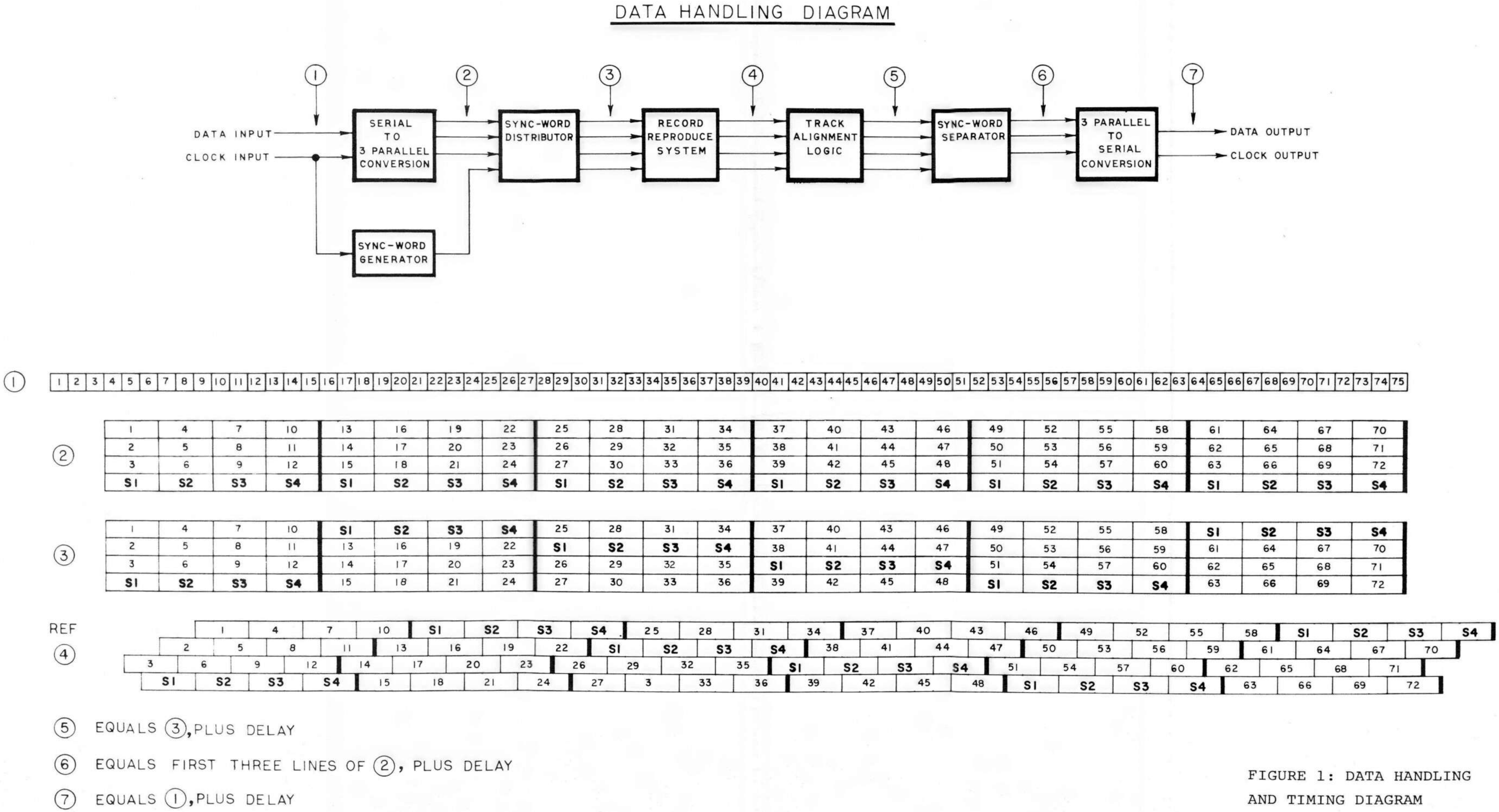


FIGURE 1: DATA HANDLING AND TIMING DIAGRAM

to the CONTROL TRACK INPUT terminal of the recorder, for time base error feedback to the capstan servo electronics. It is important that the clock extractor circuits have a sufficient time constant to override any dropout which may occur in the signal reproduced from tape. Otherwise, a dropout could result in a permanent change of the phase of the divided signal which feeds to the capstan servo, thereby introducing a permanent time shift in the reproduced data, or even cause the capstan servo to fall out of step. Clock-extracting circuits are usually fitted with a flywheel circuit to obtain a sufficiently noise-free clock signal. The above requirement constitutes therefore no additional complexity.

The amount of storage provided in the electronic track alignment circuits must be increased for this application because all data tracks carry, in addition to the mutual timing errors, a common displacement with respect to the external timing source. This common displacement consists mainly of the residual capstan servo error because the average tape speed, and slow variations of it, are regulated by the capstan servo. The extra amount of data storage needed in the alignment circuits is not significant because the residual capstan servo error is usually small compared to the sum of all intertrack errors.

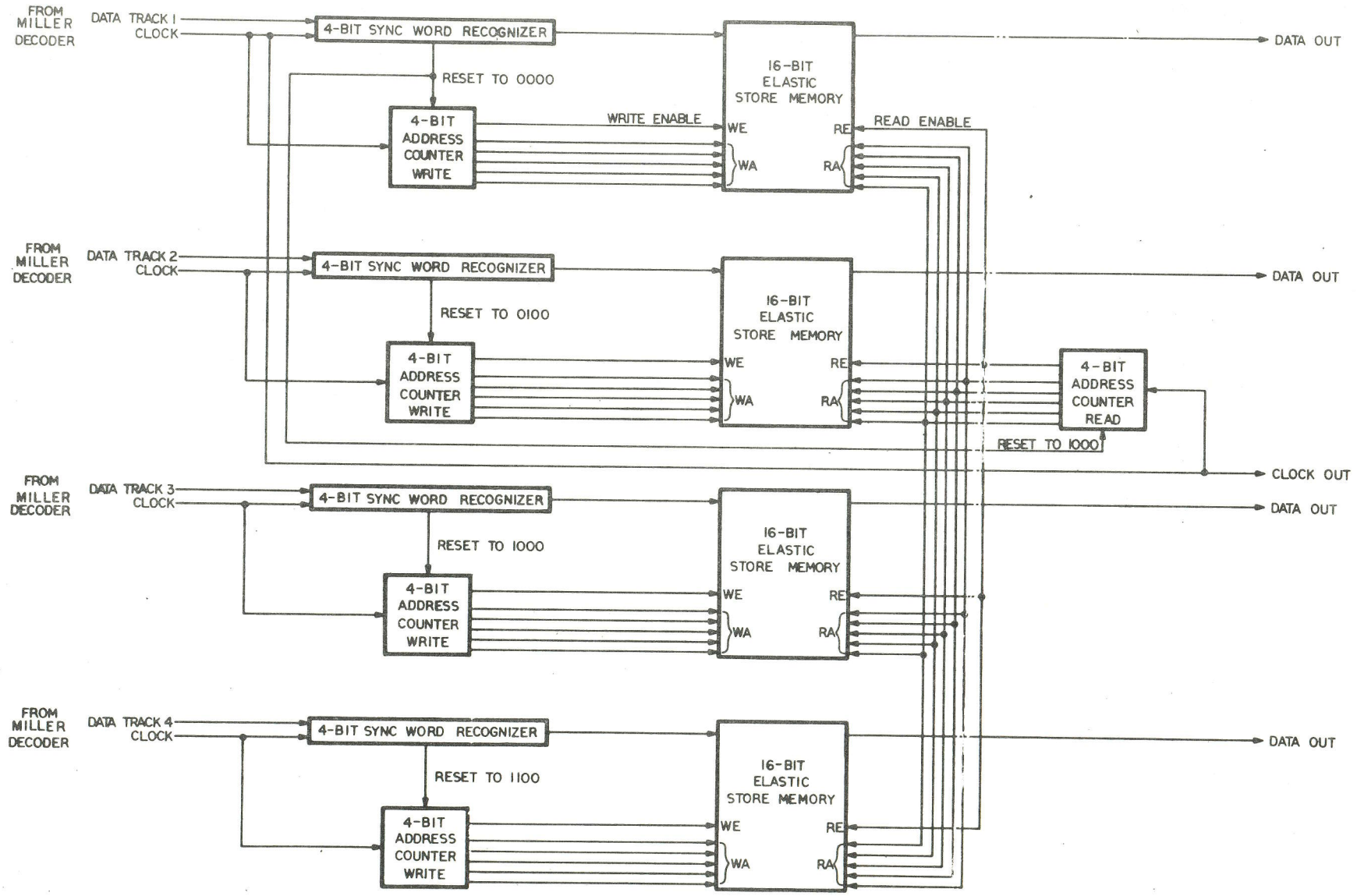


FIGURE 2: BLOCK DIAGRAM - ELECTRONIC TRACK ALIGNMENT USING ELASTIC STORE MEMORIES

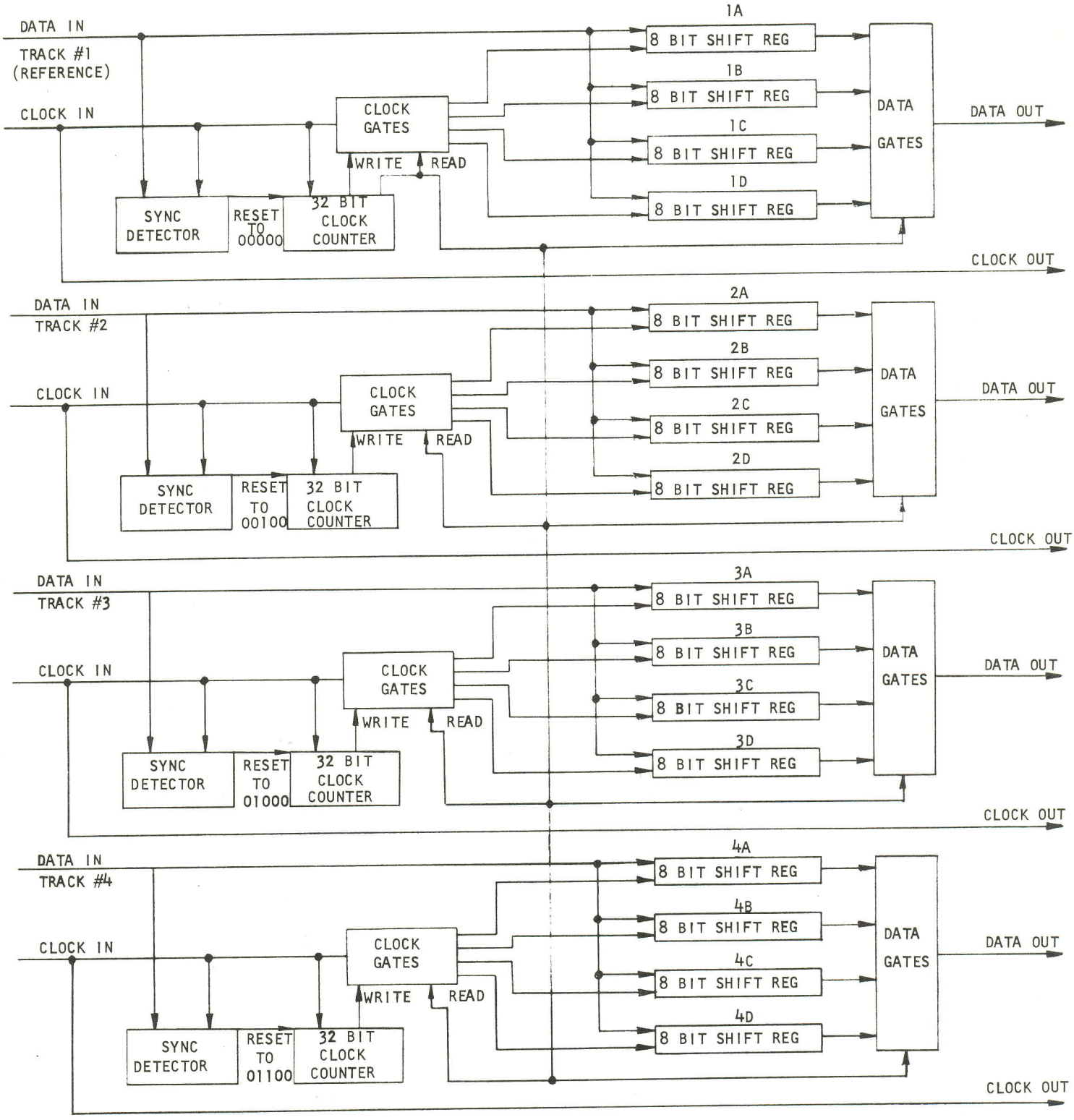
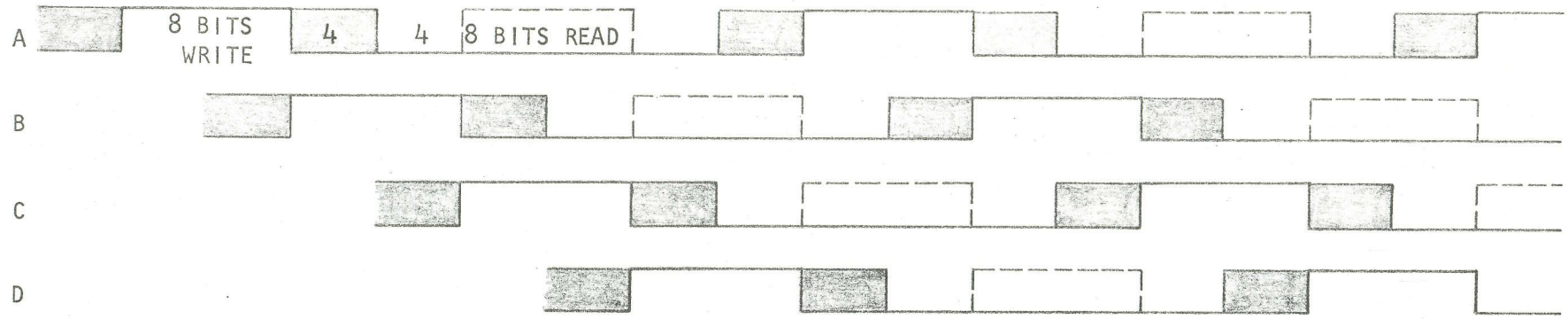
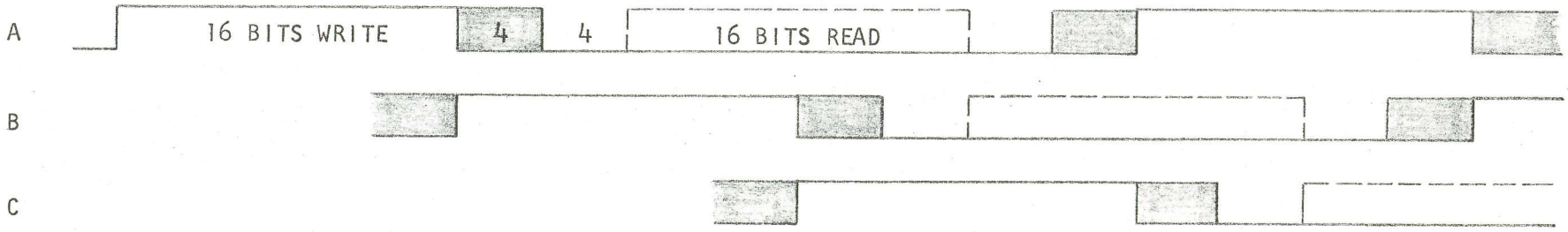


FIGURE 3: ELECTRONIC TRACK ALIGNMENT USING SHIFT REGISTERS



A. FOUR EIGHT-BIT SHIFT REGISTERS



B. THREE SIXTEEN-BIT SHIFT REGISTERS

FIGURE 4: TIMING DIAGRAMS FOR TWO TRACK ALIGNMENT SYSTEMS USING SHIFT REGISTERS

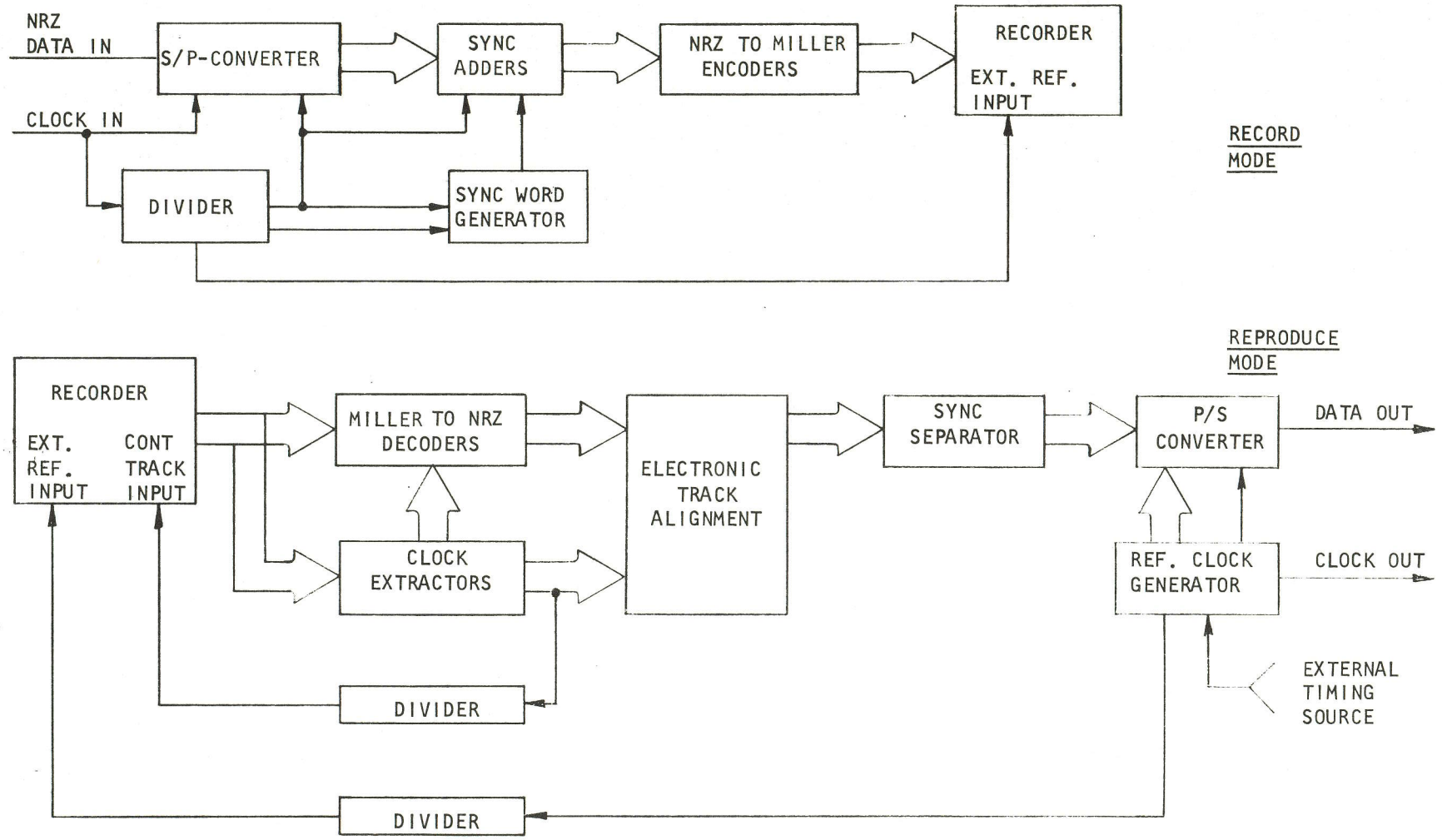


FIGURE 5: BLOCK DIAGRAM - ELECTRONIC TRACK ALIGNMENT
WITH RESPECT TO EXTERNAL TIMING SOURCE