User's Guide

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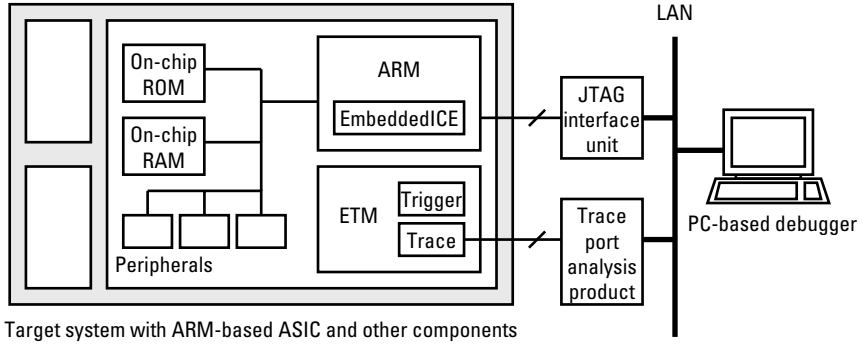
For Safety information, Warranties, and Regulatory information, see the pages behind the index.

Trace Port Analysis for ARM ETM

The ARM7 and ARM9 families of microprocessors can include an Embedded Trace Macrocell (ETM) that outputs information about processor execution to a *trace port*.

Software debuggers provide the user interface to the ARM ETM; they configure the trace port via a JTAG interface, and they display the data collected from the trace port.

(The JTAG interface is also used for downloading code, starting/stopping processor execution, single-stepping through a program, setting breakpoints, and displaying/modifying registers and memory.)



Agilent Technologies has two products for trace port analysis:

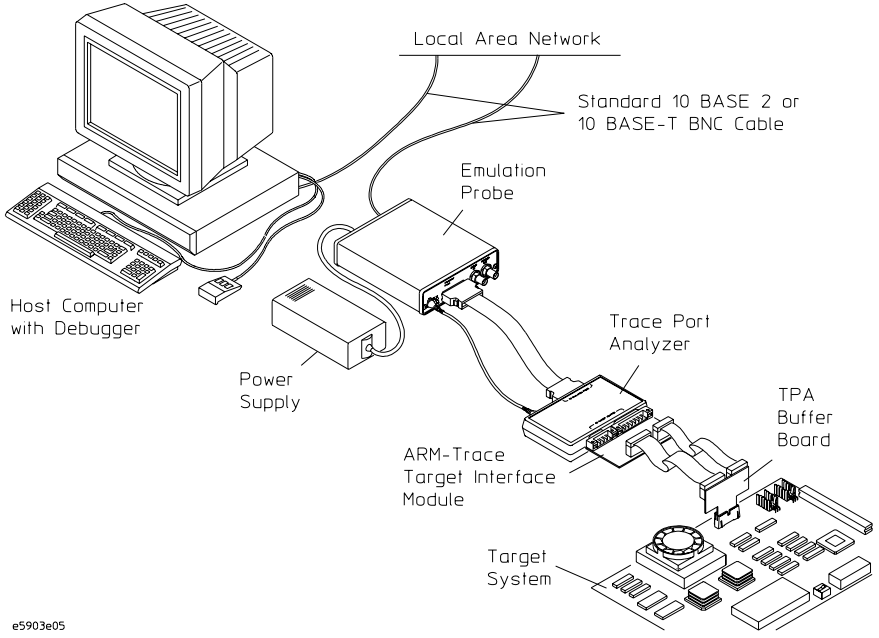
- Agilent Technologies E5903A Option 300/301 trace port analyzer for ARM ETM.
- Agilent Technologies E9595A Option 002 analysis probe for ARM ETM.

NOTE: A JTAG interface unit is required to set up trace/trigger specifications on the ARM ETM. This controller can be an Agilent Technologies emulation module, an Agilent Technologies emulation probe, or a JTAG interface unit from a third party.

Trace Port Analyzer for ARM ETM

The Agilent Technologies E5903A Option 300 trace port analyzer for ARM ETM is a low cost analyzer programmed specifically for collecting data from an ARM ETM.

The E5903A Option 301 trace port analyzer for ARM ETM includes an emulation probe, which is Agilent Technologies' JTAG interface unit.



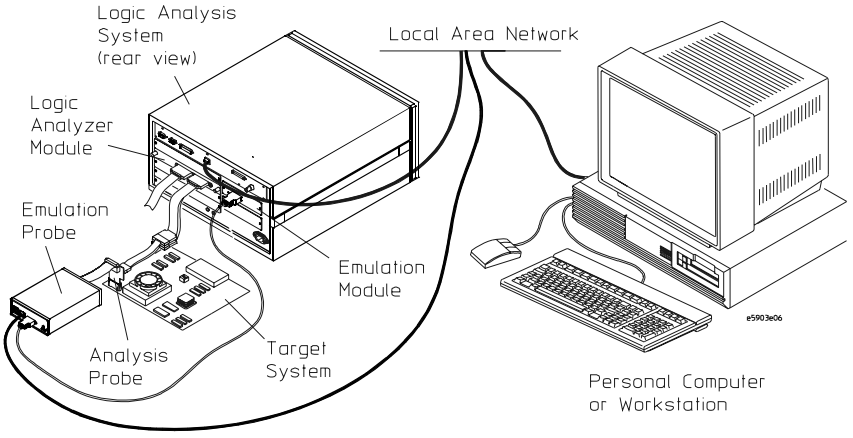
With the trace port analyzer, you can...

- Capture ARM ETM trace data at a relatively low cost. The trace port analyzer and an emulation probe are less expensive than an analysis probe and logic analysis system solution.
- Capture data on 8- or 4-bit wide trace packet buses.
- Store 512K trace states.

Analysis Probe for ARM ETM

The Agilent Technologies E9595A Option 002 analysis probe for ARM ETM, along with the Agilent Technologies 16700A/16600A-series logic analysis system and a logic analyzer module, function as a trace port analyzer.

The 16700A/16600A-series logic analysis system can also contain an emulation module, which is Agilent Technologies' JTAG interface unit.



With the analysis probe, you can...

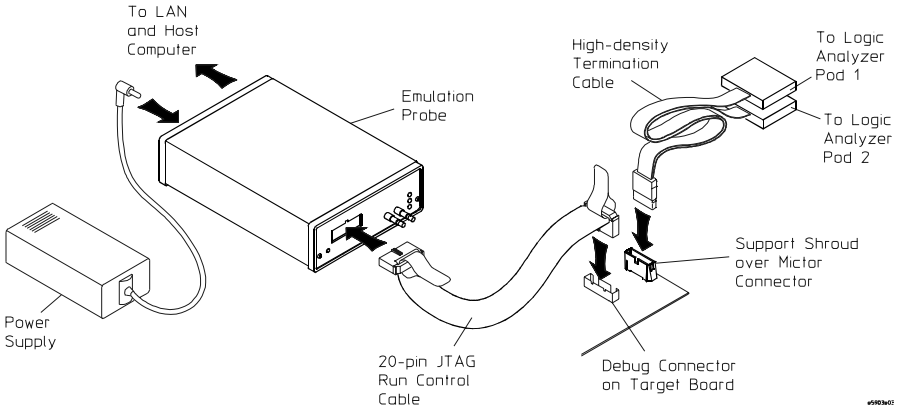
- Capture data on 4-, 8-, or 16-bit wide trace packet buses. The trace port analyzer supports 8- and 4-bit wide trace packet buses.
- Capture data on ARM ETM ports that have lower voltages and/or higher speeds than are allowed with the trace port analyzer.
- Capture more ARM ETM states. (Some logic analyzers have deeper memory than the trace port analyzer.)
- Use an existing JTAG interface unit. The trace port analyzer requires an Agilent Technologies emulation probe (although you can still use an existing JTAG interface unit).
- Capture time tag information. The trace port analyzer doesn't support time tags. (However, software debuggers may ignore time tags anyway.)
- Capture ARM ETM data at a lower additional cost if you already own an

Agilent Technologies 16700A/16600A-series logic analysis system with a logic analyzer module.

- You can correlate ARM ETM trace data with other target system activity.

Direct Logic Analyzer Connection

You can also capture ARM ETM information directly using a logic analyzer (without an analysis probe).



This configuration has the same advantages as when using the analysis probe except that the target system needs a JTAG interface connector in addition to the ARM ETM port connector.

In This Book

This book describes Agilent Technologies' trace port analysis products for ARM7/9 processors:

- Agilent Technologies E5903A Option 300/301 trace port analyzer for ARM ETM.
- Agilent Technologies E9595A Option 002 analysis probe for ARM ETM.

This manual describes:

- Target system design considerations and other requirements of Agilent Technologies' trace port analysis products.
- How to set up Agilent Technologies' trace port analyzer.
- How to set up Agilent Technologies' analysis probe.
- How to use third party debuggers with Agilent Technologies' trace port analysis products.
- How to coordinate measurements between the Agilent Technologies' trace port analysis products and the logic analysis of other parts of your target system.
- Specifications and characteristics of Agilent Technologies' trace port analysis products.

See Also

Agilent Technologies emulation probe/module documentation: *Emulation for the ARM7/ARM9 User's Guide*.

Agilent Technologies analysis and emulation documentation: *Solutions for the ARM7/ARM9 User's Guide*.

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Target Requirements

In order to use Agilent Technologies' trace port analysis products, the ARM7/9 microprocessor must have the Embedded Trace Macrocell (ETM), and its trace port signals must be routed to a header connector in the target system. This chapter describes the header connector and signals that should be provided by an ARM7/ARM9 target system.

The header connector and signals specified in this chapter apply to both the Agilent Technologies E5903A Option 300/301 trace port analyzer for ARM ETM and the Agilent Technologies E9595A Option 002 analysis probe for ARM ETM.

Trace Port Signals

The trace port signals consist of all of the signals provided by the ARM ETM and also the JTAG run control signals. These two groups of signals are combined onto a single connector to save space on the target system.

The trace port signals are described below.

ARM ETM Signals

TRACECLK. The trace clock signal provides the clock for the trace port. PIPESTAT[2:0], TRACESYNC, and TRACEPKT[n-1:0] signals are referenced to the rising edge of the trace clock.

PIPESTAT[2:0]. The pipeline status signals provide a cycle-by-cycle indication of what is happening in the execution stage of the processor pipeline.

TRACESYNC. The trace sync signal is used to indicate the first packet of a group of trace packets and is asserted HIGH only for the first packet of any branch address.

TRACEPKT[n-1:0]. The trace packet signals are used to output packaged address and data information related to the pipeline status. All packets are eight bits in length, irrespective of the number of trace packet signals implemented. There are three cases to consider for how trace packets are output on the trace packet signals:

- 4-Bit TRACEPKT Bus (TRACEPKT[3:0] signals). A packet is output over two cycles. In the first cycle, Packet[3:0] is output and in the second cycle, Packet[7:4] is output.

  In this case, Agilent Technologies' trace port analyzer or Agilent Technologies' analysis probe can be used to capture the trace data. TRACEPKT[15:4] signals are unused and should be connected to ground.

- 8-Bit TRACEPKT Bus (TRACEPKT[7:0] signals). A packet is output in a single cycle.

  In this case, Agilent Technologies' trace port analyzer or Agilent

Technologies' analysis probe can be used to capture the trace data. TRACEPKT[15:8] signals are unused and should be connected to ground.

- 16-Bit TRACEPKT Bus (TRACEPKT[15:0] signals). Up to two packets can be output per cycle. If there is only one valid packet, it is output on TRACEPKT[7:0] and TRACEPKT[15:8] is unpredictable. If there are two packets to output, the first is output on TRACEPKT[7:0] and the second on TRACEPKT[15:8].

  In this case, only Agilent Technologies' analysis probe can be used to capture the trace data.

EXTTRIG. EXTTRIG is an optional signal. It is intended to be an input to one of the external inputs on the ETM.

Depending on the design, ETM external triggers may not be available on the ASIC's external pins. In this case, the EXTTRIG has no function, and it is recommended that this pin is pulled to a defined state.

NOTE: This signal is important for making coordinated measurements.

ARM ETM and JTAG Signals

VTRef. The VTRef signal is intended to supply a logic-level reference voltage to allow debug equipment to adapt to the signaling levels of the target board.

NOTE: VTRef does NOT supply operating current to the debug equipment.

Target boards should supply a voltage that is nominally between 1V and 5V. With +/- 10% tolerance, this is minimum 0.9V, maximum 5.5V. The target board should provide a sufficiently low DC output impedance that the output voltage not change by more than 1% when supplying a nominal signal current (+/-0.4mA).

Debug equipment that connects to this signal should interpret it as a signal rather than a power supply pin and not load it more heavily than a signal pin. The recommended maximum source or sink current is +/- 0.4mA.

JTAG Signals

VSupply. The VSupply signal is intended to supply operating current to debug equipment so that an additional power supply is not required. This is not used by all debug equipment.

The Agilent Technologies trace port analysis products don't use the VSupply signal.

nTRST. The nTRST signal is an open collector output from the JTAG interface unit to the Reset signal on the target JTAG port. This pin should be pulled high on the target to avoid unintentional resets when there is no connection. Target board logic must ensure that there is a low pulse on the target ASIC's nTRST pin at power up.

TDI. TDI is the Test Data In signal from the JTAG interface unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TMS. TMS is the Test Mode signal from the JTAG interface unit to the target JTAG port. This pin should be pulled up on the target so that the effect of any spurious TCKs when there is no connection is benign.

TCK. TCK is the Test Clock signal from the JTAG interface unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

RTCK. RTCK is the Return Test Clock signal from the target JTAG port to the JTAG interface unit. Some targets need to synchronize the JTAG port to internal clocks. To assist in meeting this requirement, RTCK, which is a returned (and re-timed) TCK, can be used to dynamically control the TCK rate. Targets that don't require RTCK should tie it to a fixed signal level.

TDO. TDO is the Test Data Out from the target JTAG port to the JTAG interface unit.

nSRST. This is an open collector output from the JTAG interface unit to the target system reset. This is also an input to the JTAG interface unit so that a reset initiated on the target may be reported to the debugger.

This pin should be pulled up on the target to avoid unintentional resets when there is no connection.

DBGRQ. The DBGRQ signal is used by the JTAG interface unit as a debug request signal to the target processor. It is recommended that this pin is pulled to a defined state.

This signal is rarely implemented as a pin on the ASIC. This pin should be pulled down on the target to avoid unintentional debug requests when there is no JTAG interface unit connected.

If it is implemented, the DBGRQ signal can be used to enter debug mode after receiving a “BREAK-IN” signal from the logic analyzer through run control. This allows the logic analyzer triggering capability to be used for complex breakpoints.

DBGACK. The DBGACK signal is used by some emulation probes/ modules to detect entry or exit from the debug state. This signal is rarely implemented as a pin on the target ASIC.

If DBGACK is available, the “TRIGGER OUT” signal from run control can be used to start or stop the logic analyzer.

Target Header

The target header is an AMP MICTOR Connector (0.64mm [0.025in]) pitch. The header has 38 pins and is organized such that it can handle up to 16 trace data pins, 3 pipeline status pins, 1 trace sync pin, 1 trace clock pin, 1 external trigger pin, 1 voltage reference pin, 2 VDD pins, and 9 JTAG run control pins.

There are two choices for the target header: a vertical connector, and a right angle straddle mount connector.

NOTE: The vertical connector is recommended because it can accommodate an optional support shroud that provides additional strain relief and thus greater reliability. The notch on the support shroud should be placed on the same side as the odd numbered pins on the MICTOR connector. The support shroud is highly recommended.

The straddle mount connector should be used when board real-estate is a premium and there is no room for the vertical connector. A support shroud is not available for use with the straddle mount connector.

The AMP part numbers for the MICTOR target headers are given below. These connectors may be purchased directly from AMP. Support shrouds may be purchased from Agilent Technologies (part number E5346-44701). A set of five vertical MICTOR headers and support shrouds may be purchased from Agilent Technologies (part number E5346-68701).

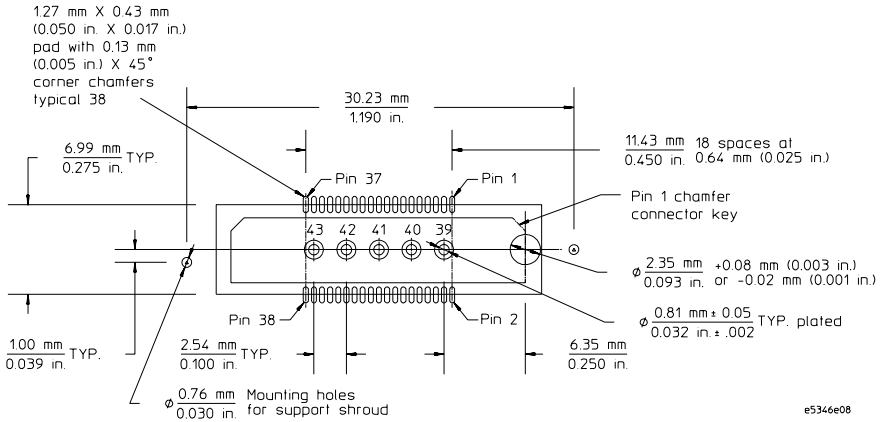
AMP MICTOR Header Part Numbers

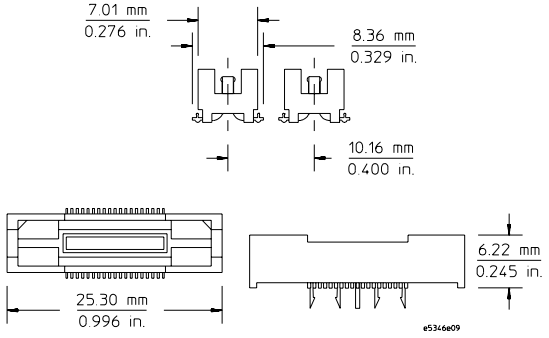
AMP Part Number	Description
2-767004-2	Vertical, Surface Mount, Board to Board/Cable connector (Ground lead length .055 mils)
767054-1	Vertical, Surface Mount, Board to Board/Cable connector (PCB Thickness of 0.062mils)
767061-1	Vertical, Surface Mount, Board to Board/Cable connector (PCB Thickness of 0.093mils)
767044-1	Right Angle, Straddle Mount, Board to Board/Cable connector (PCB Thickness of 0.062 mils)

For complete information on the AMP MICTOR connectors and the Agilent Technologies support shroud, refer to:

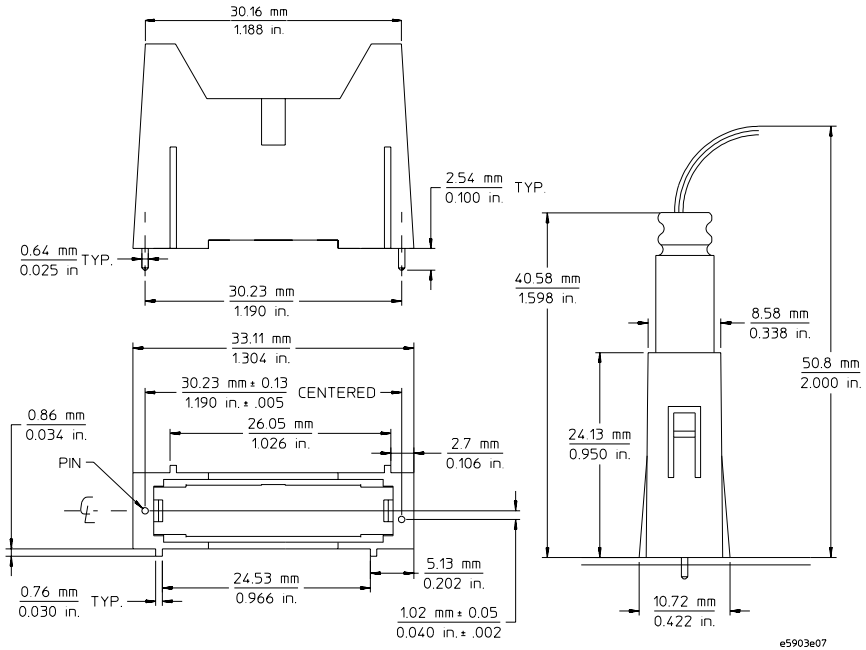
http://www.tm.agilent.com/tmo/datasheets/English/E5346A.html.

AMP MICTOR Connector Dimensions (AMP part # 2-767004-2)





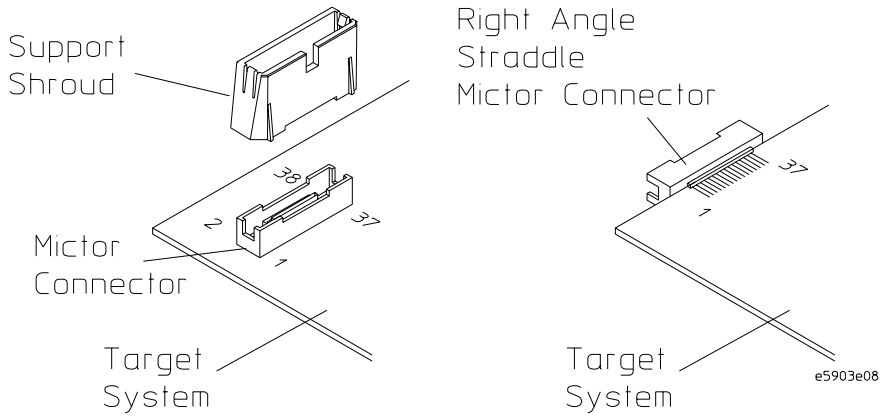
Support Shroud Dimensions



Connector Orientation

The recommended ARM Embedded Trace Macrocell trace port connector orientation is displayed in the following diagram.

Connector Orientation



Target Header Pin-Out

Newer specifications from ARM define the following target header pin-outs. If your device under test has these pin-outs, use either the E3459-66508 trace port analyzer buffer board or the E3459-66509 analysis probe board.

If your device under test uses the older specification, use either the E3459-66505 trace port analyzer buffer board or the E3459-66506 analysis probe board. For the pin-out of the older specification, see the "Old Target Header Pin-Out" appendix on page 85.

NOTE: The Agilent Technologies E5903A Option 300 trace port analyzer supports designs with 4 or 8 TRACEPKT signals. The Agilent Technologies E9595A Option 002 analysis probe for the ARM ETM trace port supports designs with 4, 8, or 16 TRACEPKT signals.

Target Header Pin-Out for the MICTOR Connector, Single Processor ETM

Pin	Signal Name	Pin	Signal Name
38	PIPESTAT0	37	TRACEPKT8
36	PIPESTAT1	35	TRACEPKT9
34	PIPESTAT2	33	TRACEPKT10
32	TRACESYNC	31	TRACEPKT11
30	TRACEPKT0	29	TRACEPKT12
28	TRACEPKT1	27	TRACEPKT13
26	TRACEPKT2	25	TRACEPKT14
24	TRACEPKT3	23	TRACEPKT15
22	TRACEPKT4	21	nTRST
20	TRACEPKT5	19	TDI
18	TRACEPKT6	17	TMS
16	TRACEPKT7	15	TCK
14	VSupply	13	RTCK
12	VTRef	11	TDO
10	EXTTRIG	9	nSRST
8	DBGACK	7	DBGRQ
6	TRACECLK	5	GND
4	No Connect	3	No Connect
2	No Connect	1	No Connect

NOTE: Pins 1, 2, 3, and 4 *must* be true no-connects. For designs with less than 16 trace data pins, pin 5 and any unused TRACEPKT pins *must* be connected to ground.

Target Header Pin-Out for the MICTOR Connector, Dual Processor ETM

Pin	Signal Name	Pin	Signal Name
38	PIPESTAT_A0	37	PIPESTAT_B0
36	PIPESTAT_A1	35	PIPESTAT_B1
34	PIPESTAT_A2	33	PIPESTAT_B2
32	TRACESYNC_A	31	TRACESYNC_B
30	TRACEPKT_A0	29	TRACEPKT_B0
28	TRACEPKT_A1	27	TRACEPKT_B1
26	TRACEPKT_A2	25	TRACEPKT_B2
24	TRACEPKT_A3	23	TRACEPKT_B3
22	TRACEPKT_A4	21	nTRST
20	TRACEPKT_A5	19	TDI
18	TRACEPKT_A6	17	TMS
16	TRACEPKT_A7	15	TCK
14	VSupply	13	RTCK
12	VTRef	11	TDO
10	EXTTRIG	9	nSRST
8	DBGACK	7	DBGRQ
6	TRACECLK_A	5	TRACECLK_B
4	No Connect	3	No Connect
2	No Connect	1	No Connect

NOTE: Pins 1, 2, 3, and 4 *must* be true no-connects. For designs with less than 16 trace data pins, unused TRACEPKT pins *must* be connected to ground.

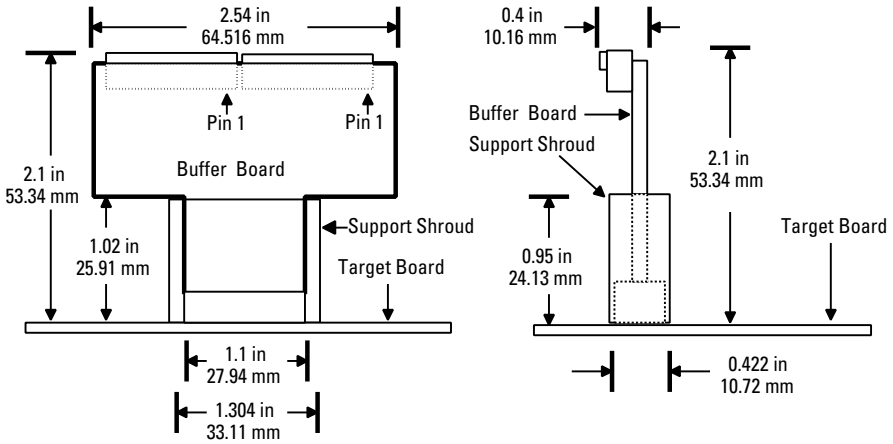
Target System Height Restrictions and Keep-Out

The Agilent Technologies trace port analysis products connect to the target MICTOR header with a small buffer board or analysis probe board. These boards connect either vertically or horizontally (right-angle), depending on which MICTOR header is on the target system.

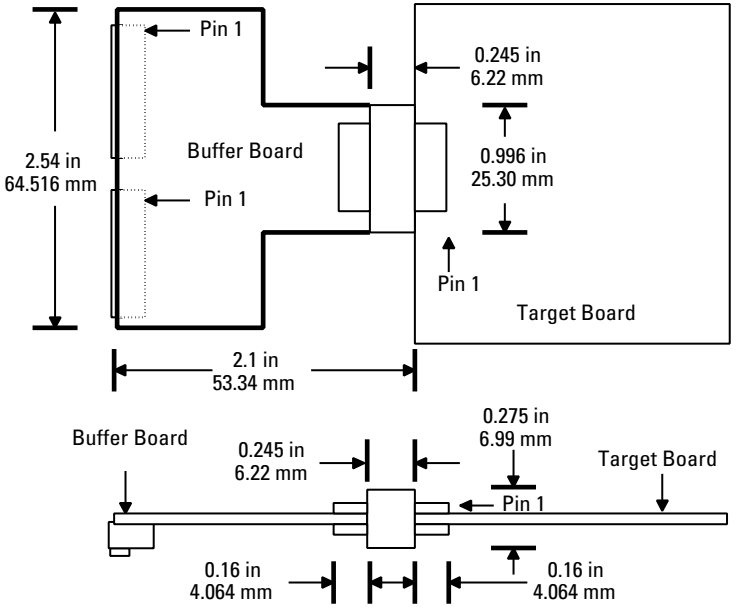
If the vertical header is used, make sure there is sufficient height clearance between the target system and the interface boards.

This section describes the height restrictions and keep-out for the buffer board and the analysis probe board.

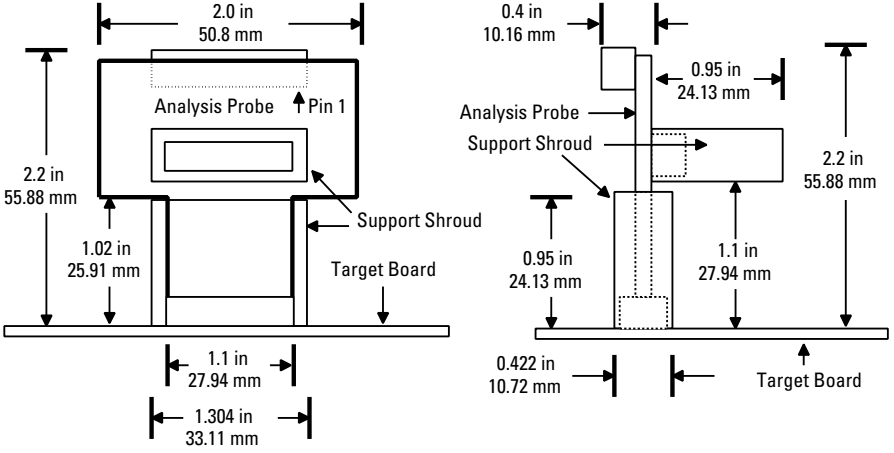
Height Restriction and Keep-Out when using the Buffer Board and the Vertical Header and Support Shroud



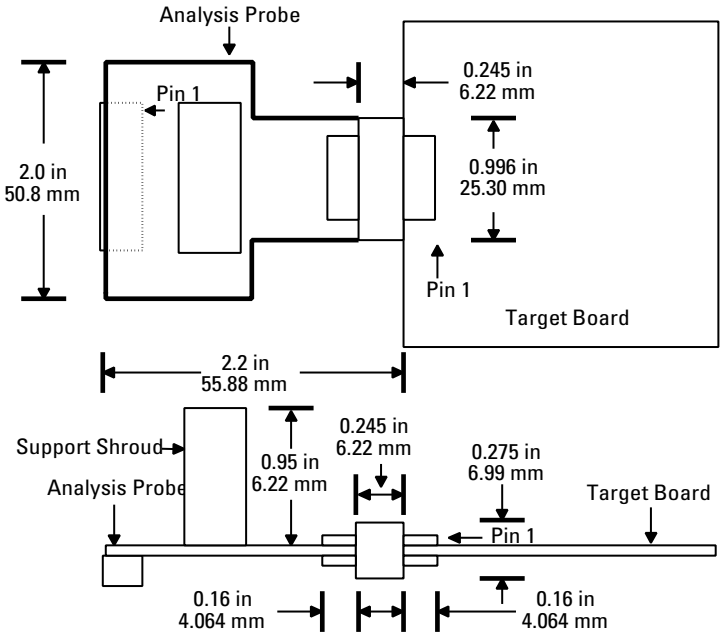
Keep-Out Area when using the Buffer Board and the Right Angle Connector



Height Restriction and Keep-Out when using the Analysis Probe and the Vertical Header and Support Shroud



Keep-Out Area when using the Analysis Probe and the Right Angle Connector



Target Board Source Terminations

Source termination of TRACECLK, PIPSTAT[2:0], TRACESYNC and TRACEPKT [15:0] is required. Failure to provide source termination will result in reflections and ringing on the trace signals that could make these signals unreadable at the ARM ETM trace port connector.

Source termination resistors must be chosen and placed such that:

- The output impedance of the trace signals on the ASIC, combined with the termination resistors, matches the target board trace impedance and pad characteristics.
- They are physically located as close to the ASIC as possible.

Depending on the rise time of the ARM ETM signals and the length of the trace between the ASIC and the connector, some target systems may work without source termination:

1. Calculate the electrical length of the trace to the trace connector.
2. For a printed-circuit board material with Er=4.9, use a propagation delay of 160 ps/inch.
3. Check that the propagation delay of the trace is less than 20% of the bus signal rise time (Tr); if it is, a source termination is not needed.

Example

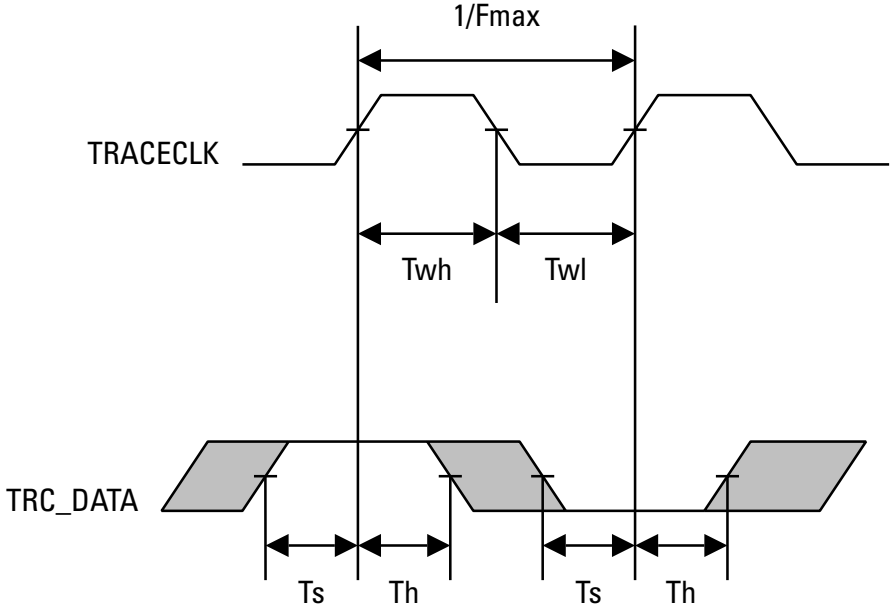
If the rise time of the bus signal is 1 ns, source termination resistors will be needed if the trace length is greater than 1.25 inches.

Timing and Voltage Specifications for Trace Port Signals

The signals from the target system must meet certain timing and voltage requirements in order for the trace port analysis tools to work correctly. The Agilent Technologies E5903A Option 300, 301 trace port analyzer for ARM ETM and the Agilent Technologies E9595A Option 002 analysis probe for ARM ETM have different voltage and timing requirements. Requirements for the two products are given in the following sections.

NOTE: Design your target system to meet the requirements of the trace port analysis product you plan to use. If you plan to use both trace port analysis products, design to the more stringent trace port analyzer requirements.

Trace Port Signal Requirements



When Using the Trace Port Analyzer

The following specifications and characteristics apply to the trace port analyzer along with its associated trace buffer board.

Signal Requirements for the Trace Port Analyzer

Trace Port Analyzer	Fmax	Setup/Hold Time (Ts/Th)	Clock Pulse Width (Twh)
E5903A Option 300, 301	100 MHz	2 ns/1 ns	2 ns

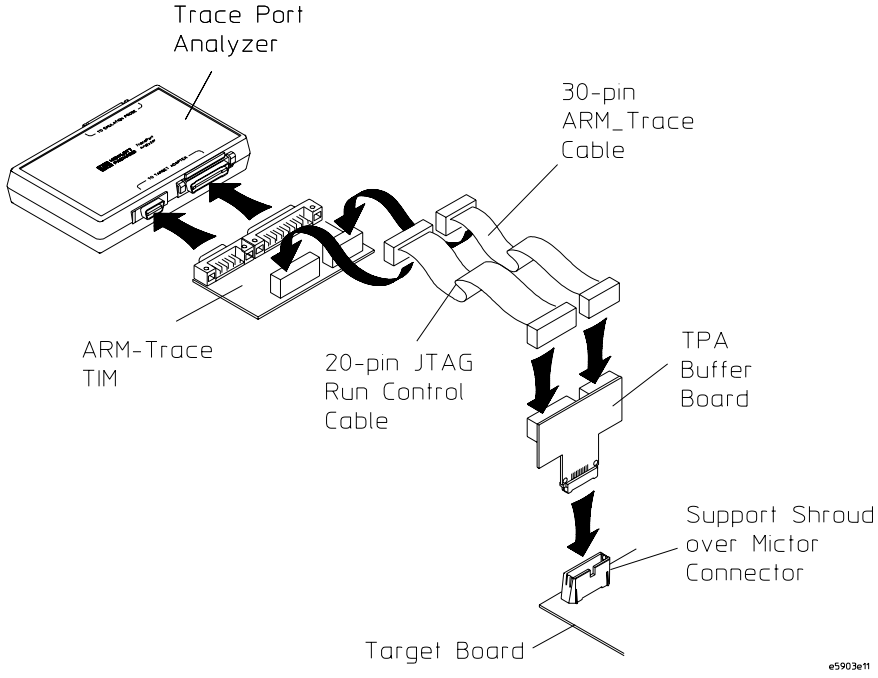
Required Voltage Levels for the Trace Port Analyzer

Parameter	Description	2.5 V Systems		3.3 V Systems	
		Min.	Max.	Min.	Max.
Vih	High-level input voltage	1.7 V		2.0 V	
Vil	Low-level input voltage		0.7 V		0.8 V

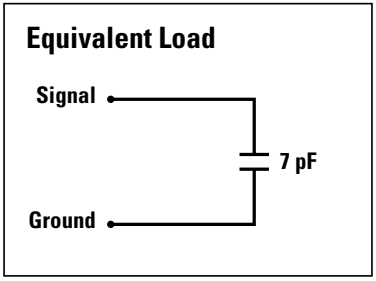
The required voltages are for the standard voltage buffer board which uses a BICMOS buffer/driver IC. This board has a high frequency capability of 100 MHz.

Loading Effects When Using the Trace Port Analyzer

Most target systems connect to the trace port analyzer via the trace port analyzer buffer as shown below:



The trace port analyzer buffer board presents the following equivalent load to each signal. Target systems must be capable of driving this load and meeting the signal requirements given above.



Modeling the Trace Port Analyzer Buffer Board. If it is necessary to model the trace port analyzer buffer board, it has the following characteristics:

- The Mictor connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 ohms and Tpd = 47 ps.
- The trace port analyzer buffer board has the following characteristics:
  - trace width = 0.005 inches
  - trace thickness = 0.0007 inches
  - distance from traces to ground plane = 0.007 inches
  - spacing between traces = 0.020 inches
  - ground plane thickness = 0.0014 inches
  - trace length = 0.6 inches
  - Er = 4.8
  - it is a microstrip
- Use the HSPICE model of a Philips 74ALVT16244 IC in a TSSOP package. This model can be found on the Philips Semiconductor web site.

When Using the Analysis Probe

The analysis probe for ARM ETM can handle TRACECLK frequencies up to 333 MHz and logic levels with Vih=0.5 to Vih=6.0. Frequency and set up and hold time requirements depend on the logic analyzer module. Key specifications and characteristics for several logic analyzer modules are given below. For complete information on these modules, see:

http://www.agilent.com/find/logicanalyzer

Signal Requirements for Logic Analyzer Modules

Logic Analyzer	Fmax	Setup/Hold Time (Ts/Th), Minimum*	Minimum Clock Pulse Width (Twh)
16557A/D	135 MHz	3.5/0 ns to 0/3.5 ns, adjustable in 0.5 ns steps	3.5 ns
16710/11/12A	100 MHz	3.5/0 ns to 0/3.5 ns, adjustable in 0.5 ns steps	3.5 ns
16715/16A	167 MHz	4.5/-2 ns to -2/4.5 ns, adjustable in 0.1 ns steps	1.2 ns
16717/18/19A	333 MHz	4.5/-2 ns to -2/4.5 ns, adjustable in 0.1 ns steps	1.2 ns

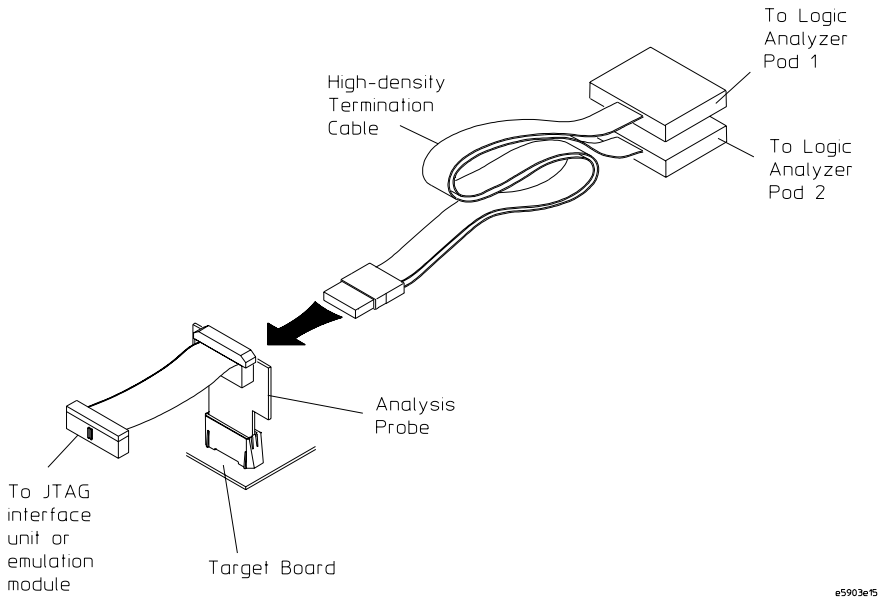
*Minimum setup/hold times are specified for single edge sampling clocks. For multiple edge sampling clocks, add 0.5 ns.

Required Voltage Levels for Logic Analyzer Modules

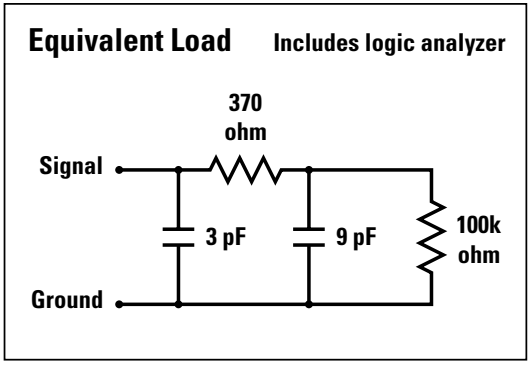
Parameter	Value
Minimum voltage swing	500 mV, peak-to-peak
Minimum input overdrive	250 mV
Threshold accuracy	±(100 mV + 3% of threshold setting)

Loading Effects When Using the Analysis Probe

Most target systems connect to the logic analyzer via an analysis probe board and an Agilent Technologies E5346A high-density adapter cable as shown below:



The logic analyzer, E5346A cable, and connectors present the following equivalent load to each signal. (This equivalent load includes the Mictor receptacle on the target system.) Target systems must be capable of driving this load and meeting the signal requirements given above.



For complete information on the Agilent Technologies E5346A high-density adapter cables with termination, see page 14 of the following PDF file:

http://literature.agilent.com:80/litwebbin/purl.cgi?pub_id=5968-4632E

Modeling the Analysis Probe. If it is necessary to model the analysis probe, it has the following characteristics:

- The Mictor connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 ohms and Tpd = 47 ps.
- The analysis probe has the following characteristics:
  - trace width = 0.005 inches
  - trace thickness = 0.0007 inches
  - distance from traces to ground plane = 0.007 inches
  - spacing between traces = 0.020 inches
  - ground plane thickness = 0.0014 inches
  - trace length = 1.12 inches
  - Er = 4.8
  - it is a microstrip
- The equivalent load represents the Mictor to logic analyzer connection.

Optional Run Control (JTAG) Header on the Target Board

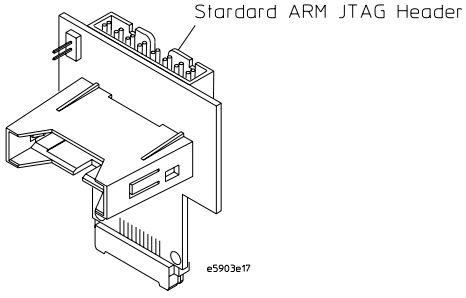
There are special situations where the target system designer may want to provide a separate run control (JTAG) header in addition to the MICTOR connector described in this document.

Situation 1

On a given design, some debug seats will use ARM ETM trace and JTAG run control. Other debug seats will use JTAG only.

Because the MICTOR connector is not compatible with most JTAG-only debug tools, the JTAG-only seats need some other way to connect to the target system.

One solution to this problem is to use an analysis probe to convert the JTAG signals that are on the Mictor header to a standard ARM JTAG header. Such an analysis probe is available from Agilent Technologies (part number E3459-66509 for the newer ARM specification or E3459-66506 for the older ARM specification).

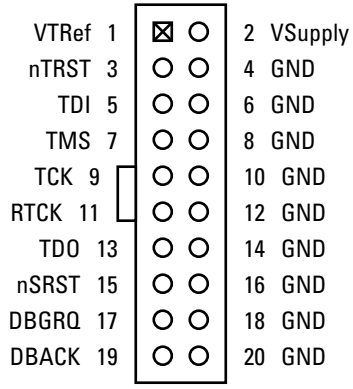


This board splits the signals from the MICTOR into two headers, one for ARM ETM trace signals and one for JTAG signals. The JTAG header on the analysis probe is specified below. It is compatible with JTAG debug tools from Agilent Technologies and other vendors.

An alternate solution is for the target board to provide a separate, run control-only (JTAG) header, in addition to the MICTOR connector

described in this document. This allows JTAG-only debug of the target board without requiring a analysis probe. The recommended header for the separate, JTAG-only connector is a medium-density 2 rows by 10 pins connector: 3M part number 2520-6002 or Agilent Technologies part number 1251-8106. JTAG signals may be routed to both the JTAG and MICTOR target headers; however, the two headers should be as close as possible to one another in order to avoid long signal paths and long stubs.

JTAG Run Control Connector Pin-Out



For complete information on the designing a JTAG run control connector into your target system, see:

http://www.tm.agilent.com/tmo/pia/LAuPDebug/PIAProd/support/English/arm_tr.html

Situation 2

The target system will be debugged using an Agilent Technologies logic analyzer to collect trace information and a non-Agilent tool for JTAG run control.

As described in situation 1, Agilent Technologies provides an analysis probe that splits the signals from the MICTOR into two headers, one for trace signals and one for JTAG signals. The JTAG header on the analysis probe is specified above.

If the JTAG tool requires a header other than the one described above, the target system should be designed with a header that meets the requirements of the JTAG tool.

Other Target Requirements

It is important to keep the trace length differences as small as possible to help minimize skew between trace pins.

Cross-talk on the trace port should be kept to a minimum; cross-talk can cause erroneous trace results.

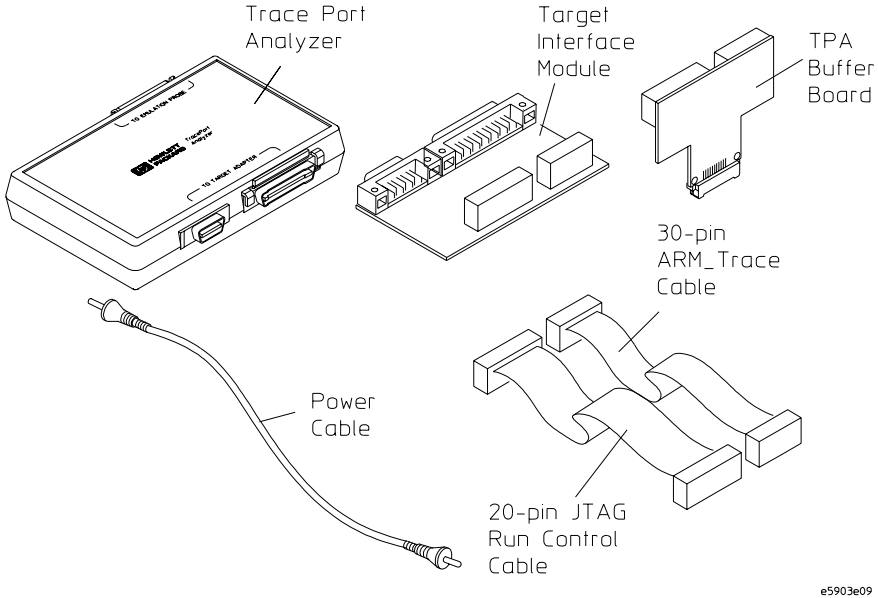
Stubs on these traces can cause unpredictable responses, especially at high frequencies, so it is recommended that no stubs exist on the trace lines. If stubs are necessary, they should be made as small as possible.

It is imperative that the clock signal be as free of noise as possible. Ground as many of the pins surrounding the clock pin as possible to prevent cross-talk from developing on the clock signal. Traces next to the clock traces should also be grounded or tied to VSupply. It is also recommended to use a higher power driver for the clock than are used for data signals.

2

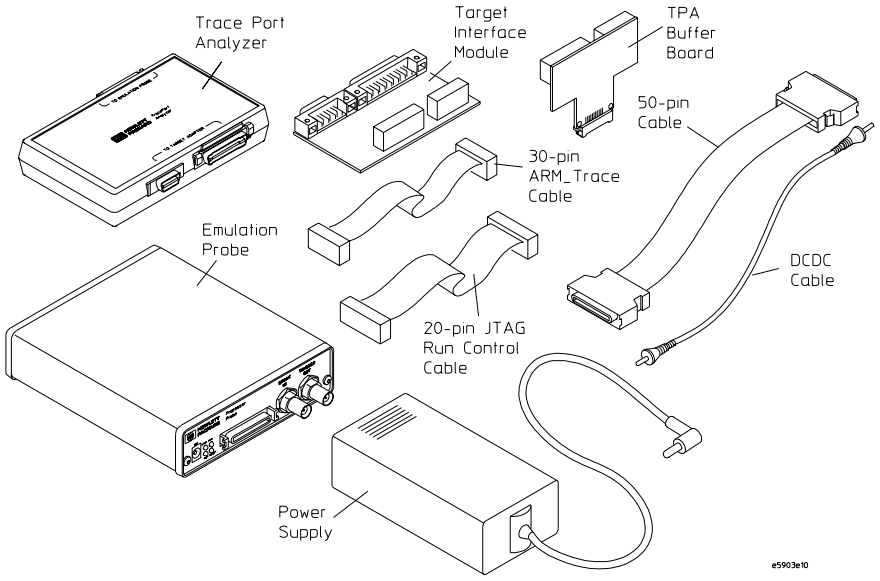
Setting Up the Trace Port Analyzer

The Agilent Technologies E5903A Option 300 trace port analyzer for ARM ETM consists of:



The trace port analyzer must be used with an emulation probe. This product is for customers who already own an emulation probe.

The Agilent Technologies E5903A Option 301 trace port analyzer for ARM ETM is the same as Option 300 except that it includes an emulation probe for ARM processors.

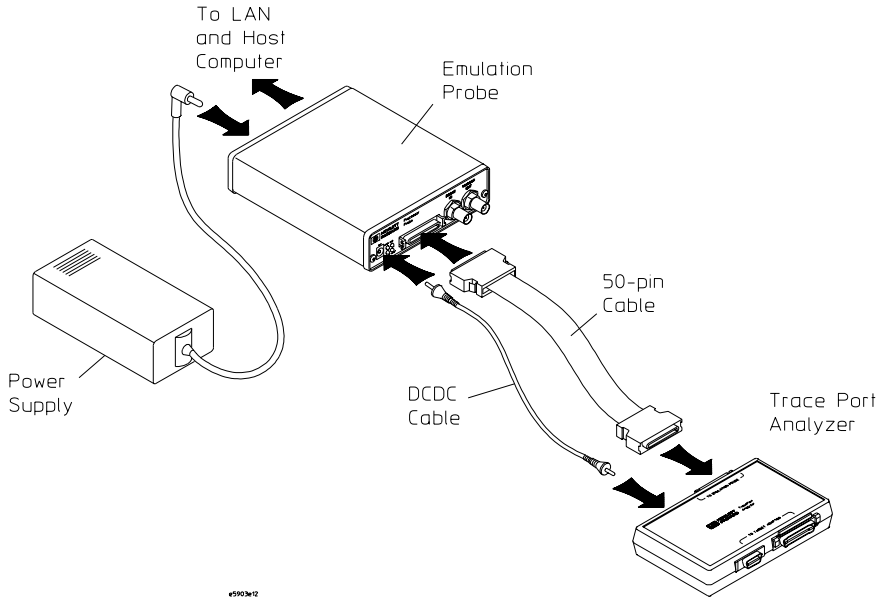


NOTE: The trace port analyzer firmware is programmed at the factory. If the need to update trace port analyzer firmware should arise, refer to the "Updating Trace Port Analyzer Firmware" chapter on page 79.

NOTE: Two trace port analyzer buffer boards are provided. If your device under test uses ARM's newer target header pin-out specification, use the E3459-66508 board. If your device under test uses ARM's older target header pin-out specification, use the E3459-66505 board.

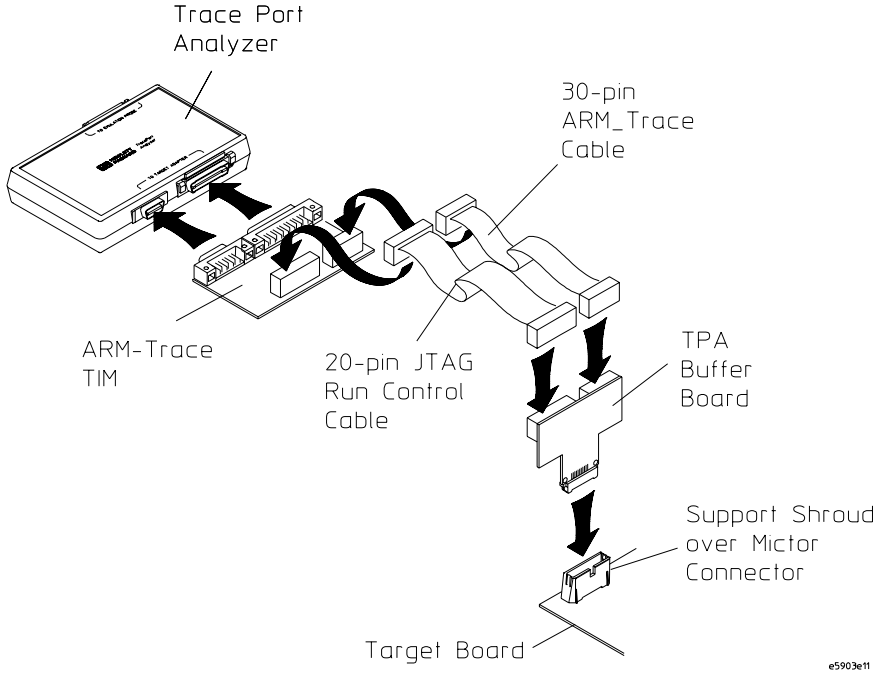
Connecting to the Emulation Probe

1. Plug one end of the 50-pin cable into the emulation probe.
2. Plug the other end of the 50-pin cable into the trace port analyzer.
3. Connect the DC to DC power cable from the emulation probe to the trace port analyzer.



Connecting to the Target System

1. Connect the ARM trace target interface module to the trace port analyzer.
2. Connect the 30-pin cable from the ARM trace target interface module to the buffer board.
3. Connect the 20-pin cable from the ARM trace target interface module to the buffer board.
4. Plug the buffer board into the target system Mictor header connector.



Connecting the Emulation Probe to the LAN

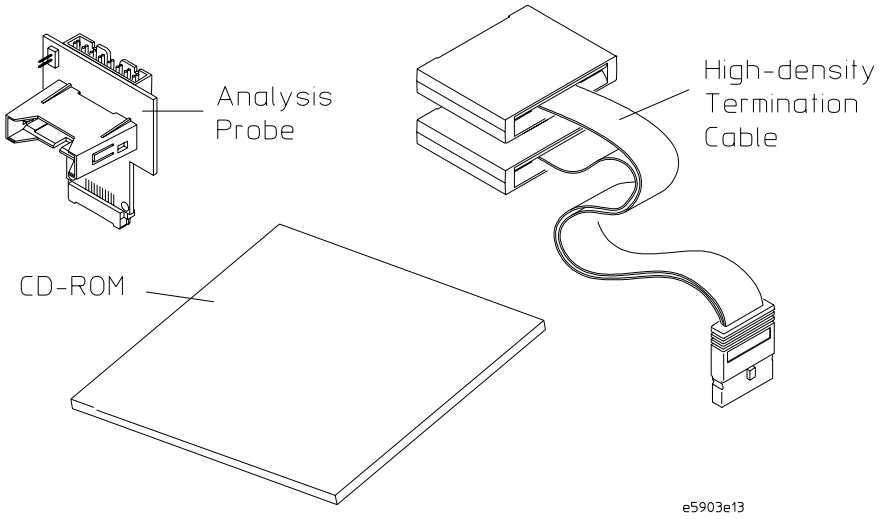
Once the emulation probe is connected to the LAN, the debugger will be able to communicate with it, configure the ARM ETM port, and get captured data from the trace port analyzer.

Refer to the *Emulation for the ARM7 User's Guide* for instructions on connecting the emulation probe to the LAN.

3

Setting Up the Analysis Probe

The Agilent Technologies E9595A Option 002 analysis probe for ARM ETM consists of:



NOTE: Two analysis probe boards are provided. If your device under test uses ARM's newer target header pin-out specification, use the E3459-66509 board. If your device under test uses ARM's older target header pin-out specification, use the E3459-66506 board.

With the analysis probe for the ARM ETM, the logic analyzer collects program execution data from the ETM's trace port.

In the simplest case, only the trace data from the ARM ETM is being traced. No other parts of the system are being traced by the logic analyzer. (See the "Making Coordinated Measurements" chapter on page 59 for coordinating ETM measurements with other logic analyzer measurements). In this model, useful trace information is displayed only in the software debugger's user interface. (Raw trace data is displayed on the logic analyzer, but it's of little practical value.) The data is unloaded from the logic analyzer by a third party debugger such as the ARM Debugger for Windows.

The debugger "decompresses" and displays the trace data.

An Agilent Technologies emulation probe/module (or a third party run

control tool) and a debugger are required to set up triggers.

Supported Logic Analyzers

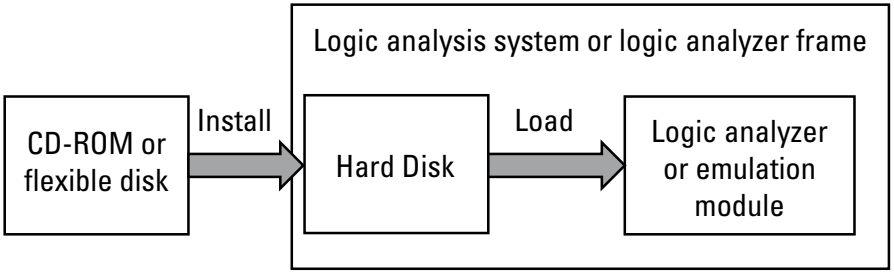
The Agilent Technologies E9595 Option 002 analysis probe for ARM ETM is compatible with Agilent Technologies 16700A/16600A-series logic analysis systems only. It does not work with the Agilent Technologies 16500 logic analysis system, the Agilent Technologies 1650 logic analyzer, the Agilent Technologies 16505A Prototype Analyzer, etc.

Installing Software

This section explains how to install the software you will need to use the analysis probe for ARM ETM.

Installing and loading

Installing the software will copy the files to the hard disk of your logic analysis system. Later, you will need to load some of the files into the appropriate measurement module.



What needs to be installed

If you ordered the analysis probe for ARM ETM with your logic analysis system, the software was installed at the factory. Otherwise, you need to install the ARM processor support package.

The following files are installed when you install a processor support package from the CD-ROM:

- Logic analysis system configuration files.
- Personality files for the Setup Assistant.
- Emulation module firmware (for emulation solutions).
- Emulation Control Interface (for emulation solutions).

To install software from CD-ROM

Installing a processor support package from a CD-ROM will take just a few minutes. If the processor support package requires an update to the Agilent Technologies 16600A/16700A-series logic analysis system's operating system, installation may take approximately 15 minutes.

1. Turn on the CD-ROM first; then, turn on the logic analysis system.
2. Insert the CD-ROM in the drive.
3. Click the System Admin icon.
4. Click Install... .

   Change the media type to "CD-ROM" if necessary.
5. Click Apply.
6. From the list of types of packages, select "PROC-SUPPORT."

   A list of the processor support packages on the CD-ROM is displayed.
7. Click on the "ARM" package.

   If you are unsure if this is the correct package, click Details for information on what the package contains.
8. Click Install....

   The dialog box will display "Progress: completed successfully" when the installation is complete.
9. Click Close.

   The configuration files are stored in /hplogic/configs/hp/arm/etm.

See Also

The instructions printed on the CD-ROM package for a summary of the installation instructions.

The on-line help for more information on installing, licensing, and removing software.

Using the Setup Assistant

The Setup Assistant is an on-line tool for connecting and configuring the Agilent Technologies 16600A/16700A-series logic analysis system for microprocessor, bus, and trace port analysis.

The Setup Assistant is a menu-driven tool that will guide you through the procedures for connecting the target system to a logic analyzer, emulation module, or other supported equipment.

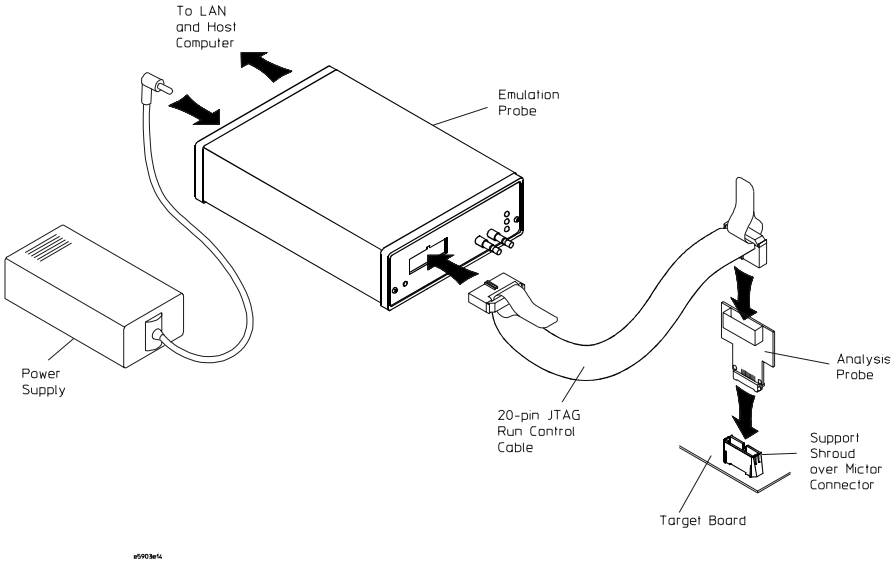
You can use the Setup Assistant in place of the connection and configuration procedures provided in this chapter.

Start the Setup Assistant by clicking its icon in the system window.

Connecting to the Target System

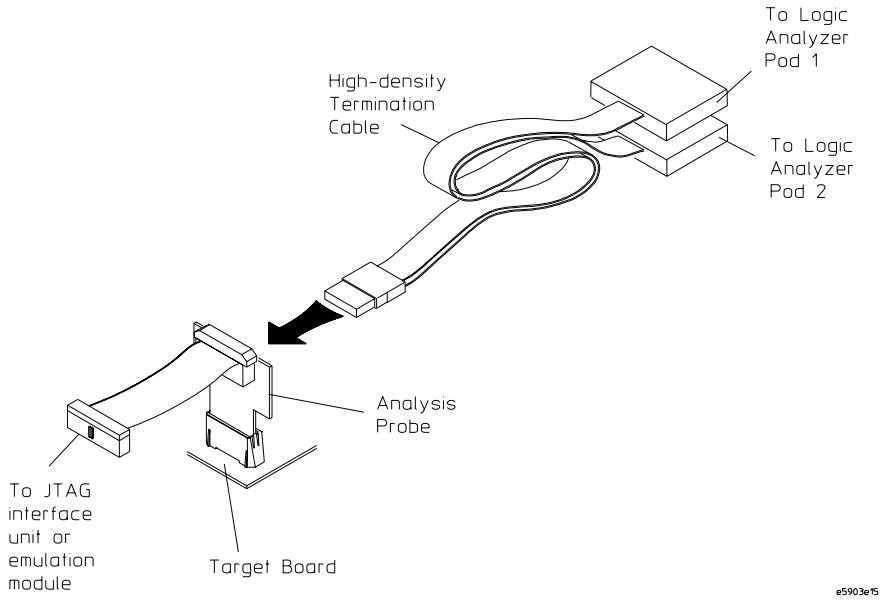
(The Setup Assistant also shows you how to connect to the target system. See "Using the Setup Assistant" on page 50.)

1 Connect the emulation module/probe (or other third party JTAG interface unit) to the analysis probe's JTAG connector.



2 Plug the analysis probe into the target system's Mictor header connector.

3 Connect the logic analyzer to the analysis probe.



Configuring the Logic Analyzer

Before starting the third party debugger, you must configure the logic analyzer and emulation module/probe. The debugger requires, but cannot perform, the proper configuration.

You can configure the logic analyzer in one of two ways:

- By using the Setup Assistant and answering a few questions about your target system (see "Using the Setup Assistant" on page 50).
- By loading one of the 18 supplied configuration files:

Agilent Technologies Logic Analyzer?	Trace Packet Width?	Include Time Tags?	ARM Target Header Pin-Out Specification	Use Configuration File
16550A	4- or 8-bit	yes	older	CARMETM_1
			newer	CARMETM_1
		no	older	CARMETM_2
			newer	CARMETM_2
	16-bit	yes	older	CARMETM_3
			newer	CARMETM_13
		no	older	CARMETM_4
			newer	CARMETM_14
16554/55/56/57 16600/1/2/3A 16710/11/12A	4- or 8-bit	yes	older	CARMETM_5
			newer	CARMETM_5
		no	older	CARMETM_6
			newer	CARMETM_6
	16-bit	yes	older	CARMETM_7
			newer	CARMETM_15
		no	older	CARMETM_8
			newer	CARMETM_16

Agilent Technologies Logic Analyzer?	Trace Packet Width?	Include Time Tags?	ARM Target Header Pin-Out Specification	Use Configuration File
16715/6/7/8/9A	4- or 8-bit	yes	older	CARMETM_9
			newer	CARMETM_9
		no	older	CARMETM_10
			newer	CARMETM_10
	16-bit	yes	older	CARMETM_11
			newer	CARMETM_17
		no	older	CARMETM_12
			newer	CARMETM_18

To load configuration files

1 Using File Manager, select the configuration file from the /logic/configs/hp/arm/etm/ directory; then, click Load.

If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

If the above directory does not exist, you need to install the ARM Processor Support Package. Close File Manager; then, use the procedure on the CD-ROM jacket to install the ARM Processor Support Package before you continue.

2 Close File Manager.

NOTE: The configuration files specify a TTL threshold voltage of 1.5 volts. This can be used for 5.0, 3.3, and 2.5 volt logic levels.

If your ARM ETM port uses 2.2, 1.8, or 1.2 volt logic levels, you must specify a different threshold voltage level in the Format tab of the logic analyzer's setup window.

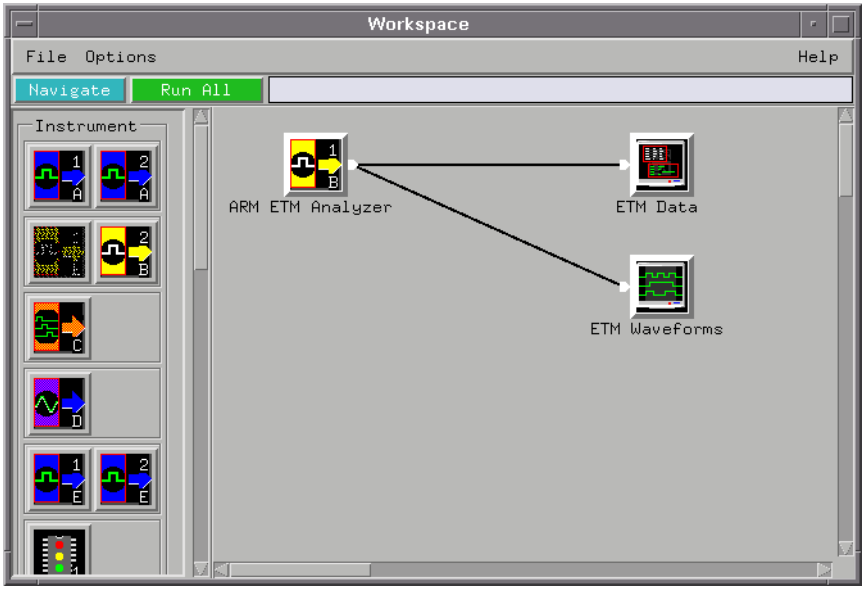
For 2.2 volt logic levels, use a threshold voltage setting of 1.2 volts.

For 1.8 volt logic levels, use a threshold voltage setting of 0.9 volts.

For 1.2 volt logic levels, use a threshold voltage setting of 0.6 volts.

NOTE: The ARM Debugger for Windows relies on certain values set up by the loaded configuration file. Changing the logic analyzer name from "ARM ETM Analyzer", the Lister display window name from "ETM Data", or the trigger specification from "trigger on 6 and store only (not 7 or not TRCPKT[0])" will result in incorrect debugger measurements. Don't change these values.

The configuration files set up a workspace that looks like:



Connecting the Logic Analysis System to the LAN

Once the logic analysis system is connected to the LAN, the debugger will be able to communicate with it, configure the ARM ETM port, and get captured data from the logic analyzer.

Refer to the *Agilent Technologies 16600A/16700A-Series Logic Analysis System Installation Guide* for instructions on connecting the logic analysis system to the LAN.

4

Using a Third Party Debugger

A third party debugger must be used with Agilent Technologies' trace port analysis products for ARM7/9 processors. Debuggers are available from ARM and other third party companies.

Debuggers are capable of working with both the Agilent trace port analyzer and the Agilent analysis probe (along with a general-purpose logic analyzer). In both cases, the debugger will:

- Set triggers, sequences, etc., in the Embedded Trace Macrocell using the Agilent Technologies emulation probe/module (or other JTAG interface unit).
- Collect trace information.
- Display execution flow and trace data.

5

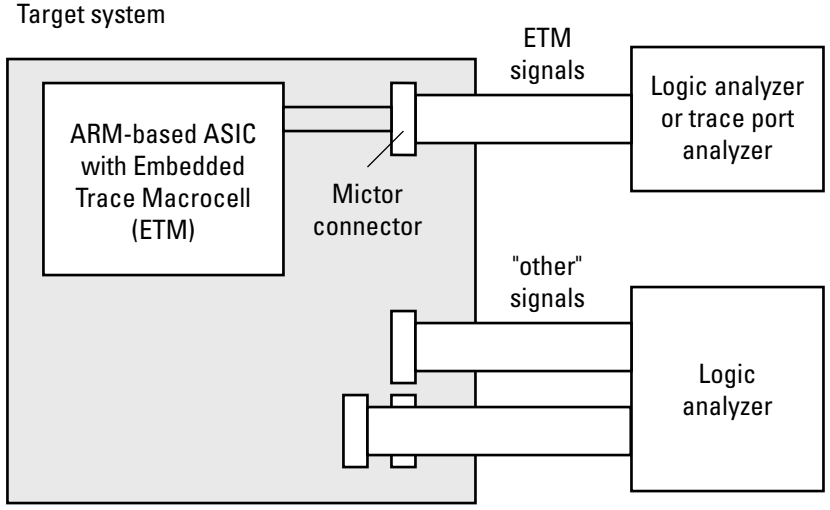
Making Coordinated Measurements

When you want to correlate real-time trace data from the Embedded Trace Macrocell with trace data from other parts of your target system, you can make coordinated measurements. Triggers can be set on either data set and cross triggered to the other.

When making coordinated measurements, the Embedded Trace Macrocell (ETM) data is displayed in the software debugger's user interface, and other logic analyzer signals are displayed in the logic analyzer's user interface. Both these user interfaces can be displayed on the same display monitor by exporting the logic analyzer user interface via an X Windows or internet connection.

This chapter assumes there are two streams of data from the target system:

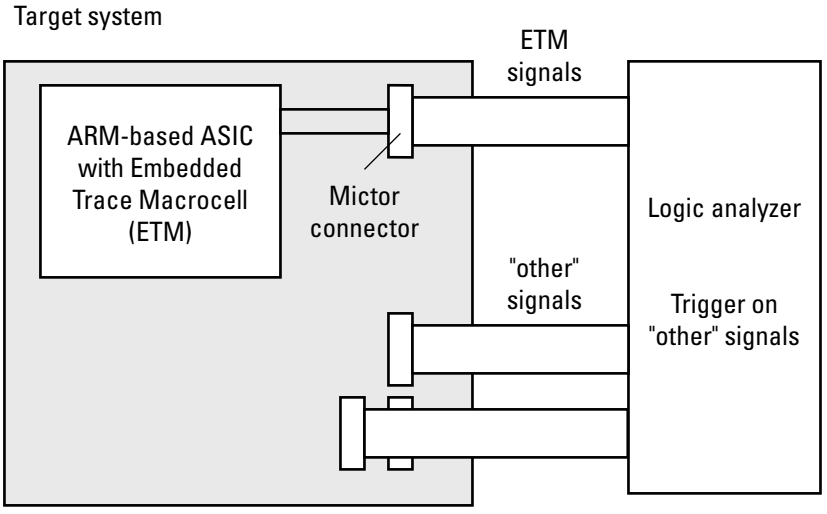
- General-purpose, non-ETM signals (for example, a PCI bus). This data stream is collected by a logic analyzer and is referred to the "other" stream.
- ARM ETM signals. This data stream is either collected by the same logic analyzer that collects the "other" signals, using the Agilent Technologies E9595A analysis probe for ARM ETM, or its collected by the Agilent Technologies E5903A Option 300 trace port analyzer.



Each analyzer can receive a trigger signal from, or can send a trigger signal to, the other analyzer.

Scenario 1: "Other" signals trigger single analyzer

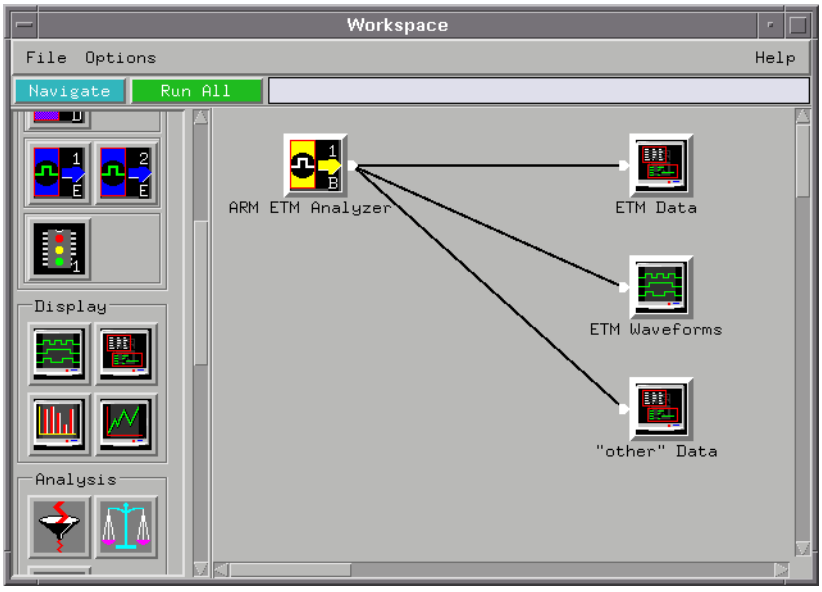
In this scenario, the logic analyzer module is set up as a single logic analyzer which captures the "other" signal data stream and the ARM ETM data stream using the same sampling clock. When you trigger on some event in the "other" data stream, the ARM ETM data stream is also captured.



1. Load the appropriate logic analyzer configuration file (see "Configuring the Logic Analyzer" on page 53).
2. Modify the logic analyzer configuration by assigning pods and formatting labels for the "other" data stream signals.

NOTE: The ARM Debugger for Windows recognizes data from the logic analyzer named "ARM ETM Analyzer" and the Lister display window named "ETM Data". The only label in the "ETM Data" Lister should be "TRCDATA". When you customize an Agilent supplied configuration, be sure not to change these names.

3 In the Workspace window, connect a second Lister display tool by dragging it onto the ARM ETM Analyzer instrument. Add the labels for the "other" data stream signals to second Lister display tool.



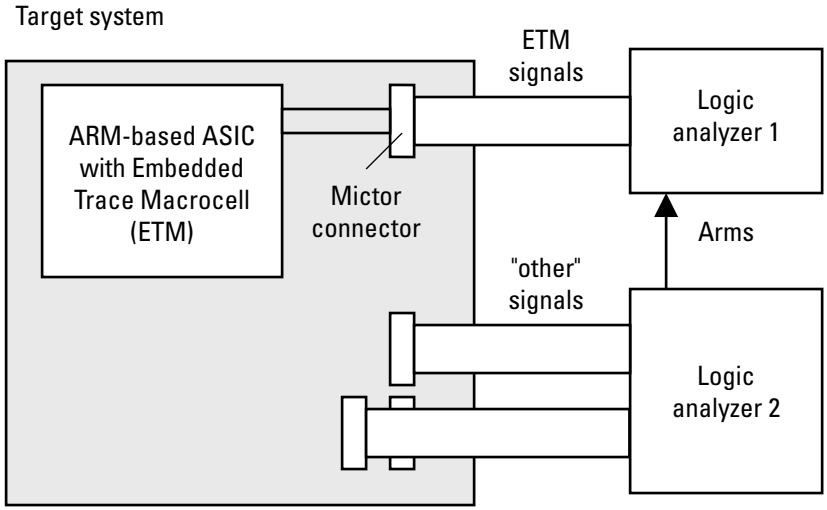
4 In the Setup window's Trigger tab, set up to trigger on an event in the "other" data stream.

5 Click Run All to start the logic analyzer measurement.

When the logic analyzer triggers, the contents of the original Lister window are read and decompressed by the ARM debugger and the "other" signals are displayed in the second Lister window.

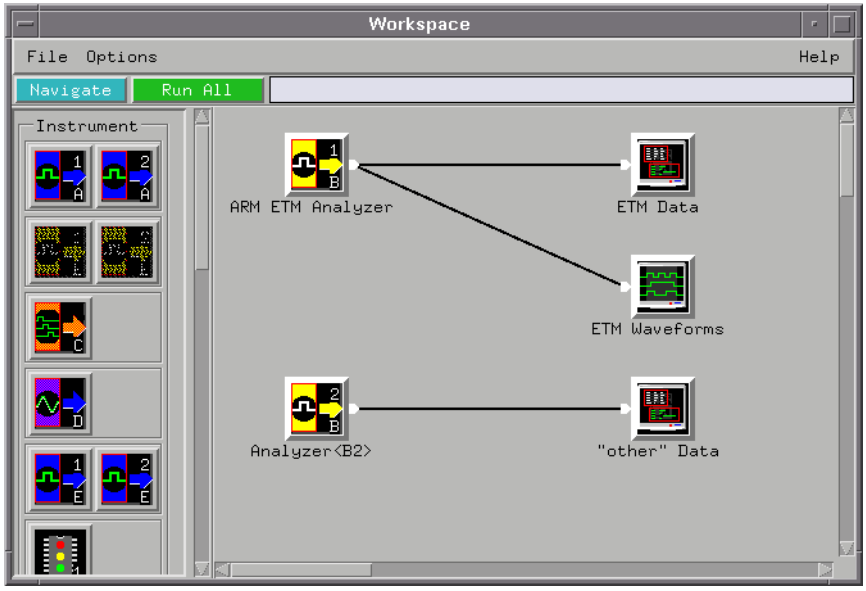
Scenario 2: "Other" analyzer triggers ARM ETM analyzer

In this scenario, the logic analyzer module is split into two analyzers, and the "other" analyzer triggers and sends its trigger signal to the ATM ETM analyzer.

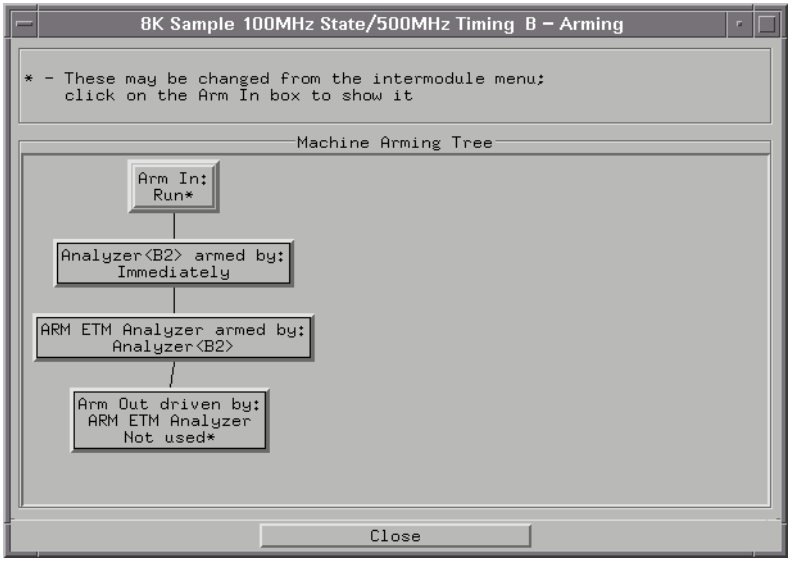


1. Load the appropriate logic analyzer configuration file into the ARM ETM analyzer (see "Configuring the Logic Analyzer" on page 53).
2. In the Workspace window, drag the second logic analyzer into the workspace and set it up to capture the "other" data stream:
   - **a** Configure the "other" analyzer as a state analyzer.
   - **b** Set up the state analyzer sampling clock.
   - **c** Assign pods to the "other" analyzer.
   - **d** Set up labels for the "other" data stream signals.
   - **e** In the Workspace window, connect any desired display tools to

the "other" analyzer.



3 In the Setup window's Trigger tab, and Settings sub tab, click Arming Control... and specify that the ARM ETM analyzer be armed by the "other" analyzer.



4 Set up the "other" analyzer to trigger on an event in the data stream.

5 Change the ARM ETM trigger so that it will trigger on any state. It will wait for the arm signal from the "other" analyzer and then trigger on any state.

NOTE: The ARM Debugger for Windows recognizes data from the logic analyzer named "ARM ETM Analyzer" and the Lister display window named "ETM Data". The only label in the "ETM Data" Lister should be "TRCDATA". When you customize an Agilent supplied configuration, be sure not to change these names.

6 In the ARM debugger, set up an ETM measurement. Use cycle accurate settings in the debugger.

7 Click Run All to start the "other" logic analyzer measurement.

When the "other" logic analyzer triggers, it arms the ARM ETM analyzer which triggers on any state.

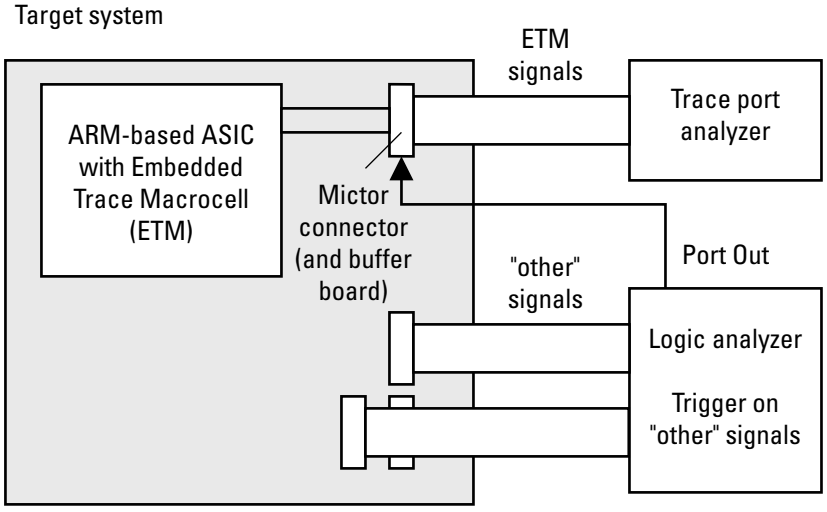
Scenario 3: "Other" analyzer triggers trace port analyzer

In this scenario, the "other" analyzer triggers and sends its trigger signal to the trace port analyzer for ARM ETM.

NOTE:

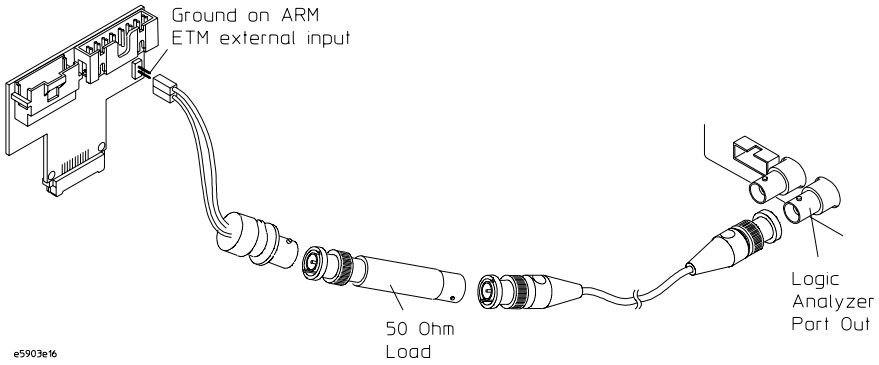
In order for this scenario to work, pin 25 of the target Mictor connector, EXTTRIG, must be connected to one of the external trigger inputs on the ETM.

If the ARM ASIC doesn't make any external triggers available on the ASIC's external pins, it was recommended that the EXTTRIG trace port signal be pulled to a defined state. In this case, the trace port analyzer cannot be triggered by another analyzer.



1 Connect a cable from the logic analysis system's Port Out connector to the ARM ETM external input connector on the trace port analyzer buffer board.

CAUTION: The cable from the logic analyzer's Port Out connector MUST be terminated by a 50 ohm load to prevent damage to the ASIC. With a 50 ohm load connected, the ASIC must be able to handle 3.3 volt logic levels.



2 Configure the logic analyzer appropriately for capturing the "other" data stream signals.

3 To enable the logic analysis system's Port Out signal:

   a Open the InterModule window.

   b Click the Port Out icon and select port out to be armed by the logic analyzer that is capturing the "other" data stream signals.

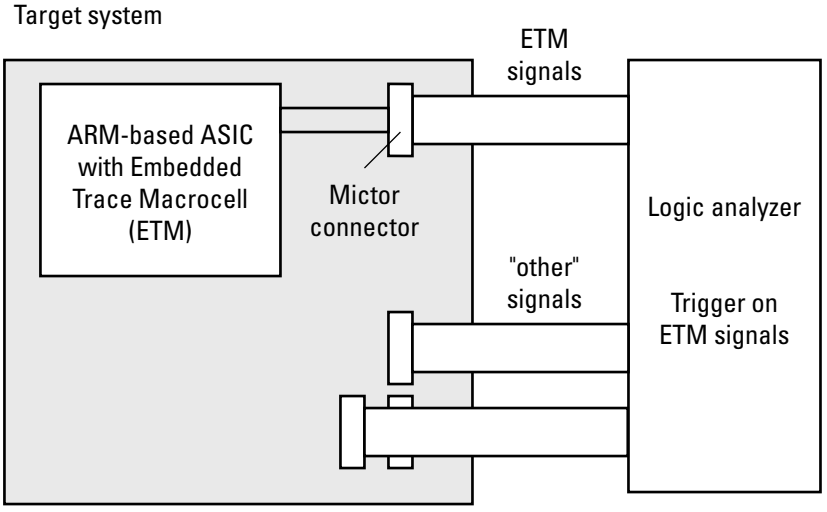
4 Set up the ARM debugger to trigger from the external input connected to the ARM ETM buffer board.

5 Click Group Run to start the logic analyzer measurement.

   When the logic analyzer triggers, the Port Out signal will go from low to high and stay high until the measurement is complete.

Scenario 4: ARM ETM signals trigger single analyzer

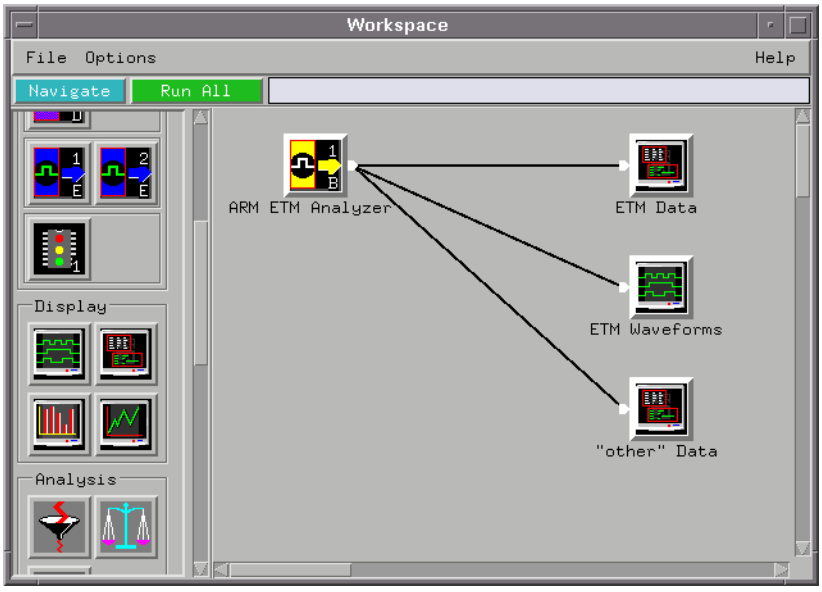
In this scenario, the logic analyzer module is set up as a single logic analyzer which captures the ARM ETM data stream and the "other" signal data stream using the same sampling clock. When you trigger on some event in the ARM ETM data stream, the "other" data stream is also captured.



1. Load the appropriate logic analyzer configuration file (see "Configuring the Logic Analyzer" on page 53).
2. Modify the logic analyzer configuration by assigning pods and formatting labels for the "other" data stream signals.

NOTE: The ARM Debugger for Windows recognizes data from the logic analyzer named "ARM ETM Analyzer" and the Lister display window named "ETM Data". The only label in the "ETM Data" Lister should be "TRCDATA". When you customize an Agilent supplied configuration, be sure not to change these names.

3 In the Workspace window, connect a second Lister display tool by dragging it onto the ARM ETM Analyzer instrument. Add the labels for the “other” data stream signals to second Lister display tool.



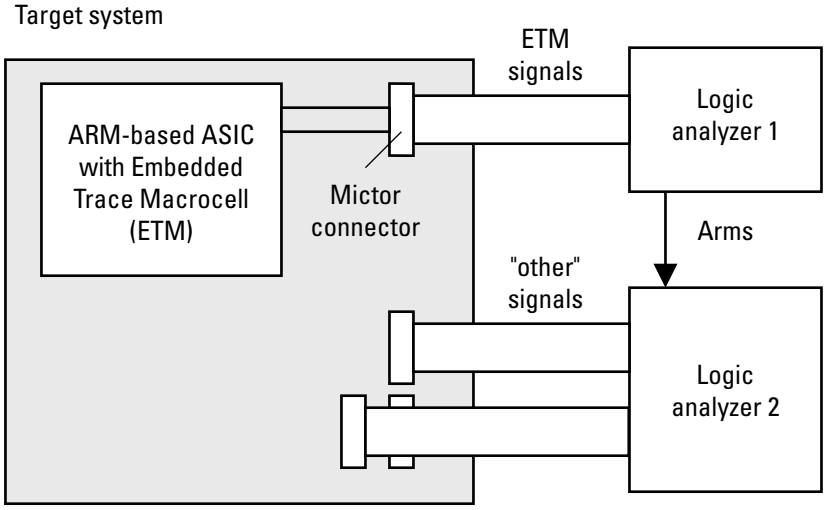
4 In the ARM debugger, set up an ETM measurement. Use cycle accurate settings in the debugger.

5 Click Run All to start the logic analyzer measurement.

When the logic analyzer triggers, the contents of the original Lister window is read and decompressed by the ARM debugger and the “other” signals are displayed in the second Lister window.

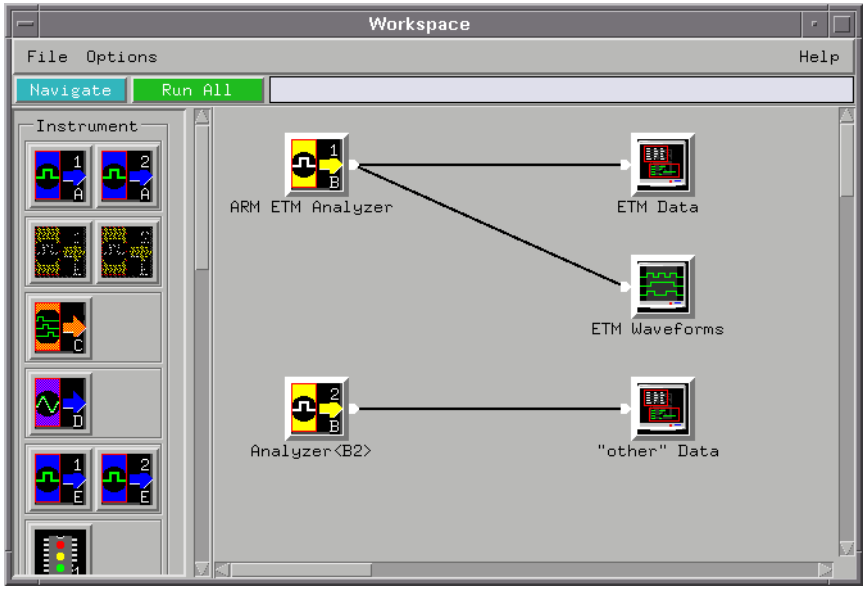
Scenario 5: ARM ETM analyzer triggers "other" analyzer

In this scenario, the logic analyzer module is split into two analyzers, and the ATM ETM analyzer triggers and sends its trigger signal to the "other" analyzer.

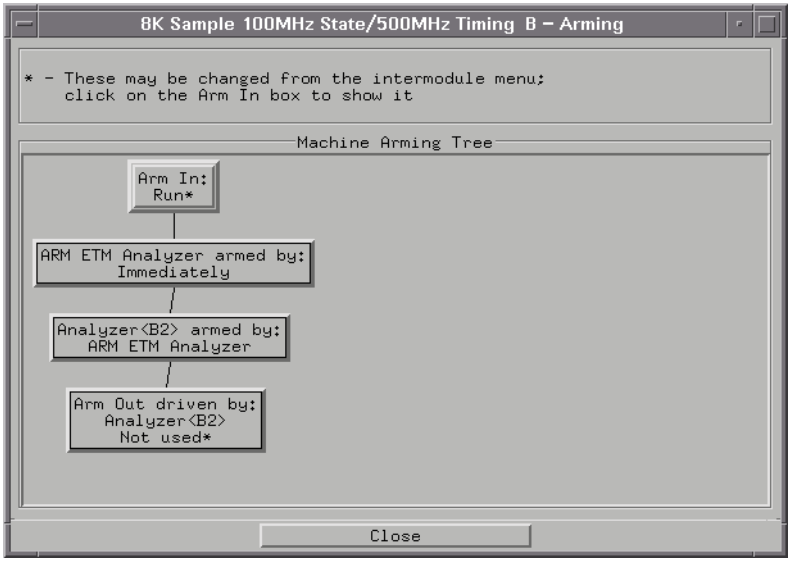


1. Load the appropriate logic analyzer configuration file into the ARM ETM analyzer (see "Configuring the Logic Analyzer" on page 53).
2. In the Workspace window, drag the second logic analyzer into the workspace and set it up to capture the "other" data stream:
   - **a** Configure the "other" analyzer as a state analyzer.
   - **b** Set up the state analyzer sampling clock.
   - **c** Assign pods to the "other" analyzer.
   - **d** Set up labels for the "other" data stream signals.
   - **e** In the Workspace window, connect any desired display tools to

the "other" analyzer.



3 In the Setup window's Trigger tab, and Settings sub tab, click Arming Control... and specify that the "other" analyzer be armed by the ARM ETM analyzer.



4 Set up the "other" analyzer to trigger on any state. It will wait for the arm signal from the ARM ETM machine and then trigger on any state.

5 In the ARM debugger, set up an ETM measurement. Use cycle accurate settings in the debugger.

6 Click Run All to start the ARM ETM logic analyzer measurement.

When the ARM ETM logic analyzer triggers, it arms the second analyzer which triggers on any state.

Scenario 6: Trace port analyzer triggers "other" analyzer

In this scenario, the trace port analyzer for ARM ETM triggers and sends its trigger signal to the "other" analyzer.

This scenario is not currently possible because the trace port analyzer cannot send its trigger signal to a logic analyzer.

6

Specifications and Characteristics

Trace Port Analyzer Characteristics

- 512K trace states- (independent of trace packet bus data width)
- 100 MHz @ 2.5V or 3.3V-5V (TTL)
- Each trace state is 4 or 8 bits of data plus 3 bits of pipe status and one bit of sync
- Trace upload speed : 150 K states/sec (3.3 seconds to upload the entire 512K buffer, independent of trace packet bus width)

Analysis Probe Characteristics

This specification applies to analyzers that are available today.

- Trace depth: up to 2 M trace states depending on the logic analyzer module (independent of trace packet bus width).
- Speed: up to 333 MHz depending on logic analyzer module.
- Voltage: 0.5 V to 6 V.
- Each trace state is 4, 8, or 16 bits of data plus 3 bits of pipe status and one bit of sync.
- Trace upload speed: 34.5 K states/sec (independent of trace packet bus width).

7

Updating Trace Port Analyzer Firmware

In the event of a product upgrade, you can reprogram the CPLDs in the Agilent Technologies E5903A Option 300/301 trace port analyzer for ARM ETM. The Agilent Technologies emulation probe must be used to perform this update. Special trace port analyzer programming firmware is first flashed into the emulation probe. The emulation probe then programs the CPLDs on the trace port analyzer. The emulation probe must then be restored to its normal operational state. There are two ways you can perform the upgrade:

- Using the Agilent Technologies 16600A/16700A-series logic analysis system.
- If you don't have a logic analysis system.

No matter which method you choose, the basic steps for updating the trace port analyzer firmare are the same:

1. Get the proper files for changing the emulation probe to "programming" mode.
2. Flash the programming firmware into the emulation probe.
3. Program the CPLDs in the trace port analyzer.
4. Restore the emulation probe to its normal operational state.

The rest of this chapter describes these steps in detail.

Using the Logic Analysis System

This section describes the steps for updating the trace port analyzer firmware using the Agilent Technologies 16600A/16700A-series logic analysis system.

Step 1: Get the proper files for emulation probe "programming" mode

The files for updating the trace port analyzer are present on the Agilent Technologies 16600A/16700A-series logic analysis system software CD-ROM, version A.01.41.00 or later.

Step 2: Flash the programming firmware into the emulation probe

1. End any run control sessions which may be running.
2. In the Workspace window, remove any Emulator icons from the workspace.
3. Install the processor support package from the CD-ROM, if necessary.
4. In the Workspace window, drag an emulation probe icon onto the workspace, right-click the icon, and select Update Firmware.
5. In the Update Firmware window, enter the emulation probe's LAN name and select the E3459Q ARM7/9 Trace Port Analyzer firmware to load into the emulation probe.
6. Click Update Firmware.

   In about 20 seconds, the firmware will be installed and the screen will update to show the current firmware version.

See Also

"To install software from CD-ROM" on page 49 for instructions on how to install the processor support package from the CD-ROM.

Step 3: Program the CPLDs in the trace port analyzer

After the programming firmware is flashed into the emulation probe, the probe will automatically program the CPLDs in the trace port analyzer as long as it determines that the CPLDs are being programmed to a newer version. This operation will take up to 10 minutes.

To manually force a programming cycle:

1. Telnet to the emulation probe.
2. Run the `pldpgm -f` command to program the trace port analyzer connected to the emulation probe.

Step 4: Restore the emulation probe to its normal operational state

1. Back in the logic analysis system's Workspace window, right-click the emulation probe icon, and select Update Firmware.
2. In the Update Firmware window, enter the emulation probe's LAN name and select the E3459B ARM7/9 JTAG Emulator firmware to load into the emulation probe.
3. Click Update Firmware.

   In about 20 seconds, the firmware will be installed and the screen will update to show the current firmware version.

If You Don't Have a Logic Analysis System

This section describes the steps for updating the trace port analyzer firmware when you don't have an Agilent Technologies 16600A/16700A-series logic analysis system.

Step 1: Get the proper files for emulation probe "programming" mode

You can get the proper files for updating the trace port analyzer firmware from:

- The world-wide web at:

  http://www.agilent.com/find/sw-updates

- The FTP server at:

  ftp://col.hp.com/dist/probe/

- The Agilent Technologies Call Center at:

  1-800-452-4844

Step 2: Flash the programming firmware into the emulation probe

To set up the emulation probe for trace port analyzer programming, you must have a PC or a workstation connected to your emulation probe.

The README file included with the firmware files contains instructions for installing the firmware using a PC or workstation.

Step 3: Program the CPLDs in the trace port analyzer

After the programming firmware is flashed into the emulation probe, the probe will automatically program the CPLDs in the trace port analyzer as long as it determines that the CPLDs are being programmed to a newer version. This operation will take up to 10 minutes.

To manually force a programming cycle:

1. Telnet to the emulation probe.
2. Run the `pldpgm -f` command to program the trace port analyzer connected to the emulation probe.

Step 4: Restore the emulation probe to its normal operational state

To restore the emulation probe firmware, you must have a PC or a workstation connected to your emulation probe.

The README file included with the firmware files contains instructions for installing the firmware using a PC or workstation.

A

Old Target Header Pin-Out

An older specification from ARM defined the following target header pin-out (differrences from the new specification are shaded). If your device under test has this pin-out, use either the E3459-66505 trace port analyzer buffer board or the E3459-66506 analysis probe board.

NOTE: The Agilent Technologies E5903A Option 300 trace port analyzer supports designs with 4 or 8 TRACEPKT signals. The Agilent Technologies E9595A Option 002 analysis probe for the ARM ETM trace port supports designs with 4, 8, or 16 TRACEPKT signals.

Target Header Pin-Out for the MICTOR Connector

Pin	Signal Name	Pin	Signal Name
38	PIPESTAT0	37	TRACEPKT12
36	PIPESTAT1	35	TRACEPKT13
34	PIPESTAT2	33	TRACEPKT14
32	TRACESYNC	31	TRACEPKT15
30	TRACEPKT0	29	VSupply
28	TRACEPKT1	27	VSupply
26	TRACEPKT2	25	EXTTRIG
24	TRACEPKT3	23	VTRef
22	TRACEPKT4	21	nTRST
20	TRACEPKT5	19	TDI
18	TRACEPKT6	17	TMS
16	TRACEPKT7	15	TCK
14	TRACEPKT8	13	RTCK
12	TRACEPKT9	11	TDO
10	TRACEPKT10	9	nSRST
8	TRACEPKT11	7	DBGRQ
6	TRACECLK	5	DBGACK
4	No Connect	3	No Connect
2	No Connect	1	No Connect

NOTE: Pins 1, 2, 3, and 4 *must* be true no-connects. For designs with less than 16 trace data pins, any unused TRACEPKT pins *must* be connected to ground.

A

analysis probe A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Formerly called a "preprocessor."

D

debug port A hardware interface designed into a microprocessor that allows developers to control microprocessor execution, set breakpoints, and access microprocessor registers or target system memory using a tool like the emulation probe.

E

emulation module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See also *emulation probe*.

emulation probe An emulation probe is a stand-alone instrument connected via LAN to the mainframe of a logic analyzer or to a host computer. It provides run control within an emulation and analysis test setup. Formerly called a "processor probe" or "software probe." See also *emulation module*.

F

flexible adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

H

high-density adapter cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

high-density termination adapter cable Same as a *high-density adapter cable*, except it has a termination in the Mictor connector.

I

inverse assembler Software that decodes microprocessor bus states (captured by the login analyzer) into assembly language mnemonics.

Typically, inverse assemblers are included with analysis probes, but when the processor can be in any type of chip package, as is the case with microprocessor cores, the inverse assembler is a separate product and connections for the logic analyzer are designed into the target system.

J

JTAG port See *debug port*.

JTAG interface unit See *emulation probe* or *emulation module*.

jumper Moveable direct electrical connection between two points.

L

label A name that you assign to a number of logic analysis channels. Typically, these names map to signal and/or bus names in the target system.

M

mainframe logic analyzer A logic analyzer that resides on one or more board assemblies installed in an Agilent Technologies 16500, 1660-series, or 16600A/700A-series mainframe.

N

N-trace A method for embedded processor cores in ASICs to output information about program execution using relatively few pins on the ASIC.

P

preprocessor See *analysis probe*.

pod A collection of logic analyzer channels associated with a single cable and connector.

preprocessor interface See *analysis probe*.

processor probe See *emulation probe*.

R

run control probe See *emulation probe* and *emulation module*.

S

Setup Assistant A software program that guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor.

solution Agilent Technologies' term for a set of tools for debugging your target system. A solution includes probing, inverse assembly, the Agilent Technologies B4620B source correlation tool set, and an emulation module.

stand-alone logic analyzer A stand-alone logic analyzer has a pre-defined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

state analysis When the logic analyzer is configured to capture data synchronously with a clock signal in the target system.

T

target interface module (TIM) A small circuit board which connects the 50-pin cable from an emulation module or emulation probe to signals from the debug port on a target system.

threshold voltage The level at which voltages above are logic "highs" (1) and voltages below are logic "lows" (0).

TIM See *target interface module*.

timing analysis When the logic analyzer is configured to capture data at a rate determined by an internal sample rate clock, asynchronous to signals in the target system.

trace port analyzer A tool that collects an N-trace port's execution information and presents it to a software debugger.

trigger specification A set of conditions that must be true before the instrument triggers. See the printed or on-line documentation for your logic analyzer for details.

transition board A board assembly that obtains signals connected to one side and rearranges them in a different order for delivery at the other side of the board.

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DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	Agilent Technologies
Manufacturer's Address:	Digital Design Product Generation Unit 1900 Garden of the Gods Road Colorado Springs, CO 80907 USA

declares, that the product

Product Name:	Trace Port Analyzer
Model Number(s):	E5903A
Product Option(s):	All

conforms to the following Product Specifications:

Safety:	IEC 1010-1:1990+A1 / EN 61010-1:1993 UL3111 CSA-C22.2 No. 1010.1:1993	
EMC:	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 555-2:1982 + A1:1985 / EN 60555-2:1987	
	IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991	
	IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
	IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
	IEC 801-4:1998 / EN 50082-1:1992	0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE marking accordingly.

This product was tested in a typical configuration with Agilent Technologies test systems.

Colorado Springs, 8/10/98

Ken Wyatt, Product Regulations Manager

European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

Product Regulations

Safety

IEC 1010-1:1990+A1 / EN 61010-1:1993
CSA-C22.2 No. 1010.1:1993

EMC

CE
ISM 1-A

This Product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.

Emissions

EN55011/CISPR 11 (ISM, Group 1, Class A equipment)
EN60555-2 / IEC555-2
EN60555-3 / IEC555-3

Immunity

EN50082-1	Code[1]
IEC 801-2 (ESD) 8kV AD	1
IEC 801-3 (Rad.) 3 V/m	1
IEC 801-4 (EFT) 1kV	1
IEC 801-6 (CI) 3 V (rms)	1

[1]Performance Codes:
1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

Sound Pressure Level

NA

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Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.
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- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
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- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

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About this edition

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New editions are complete revisions of the manual. Many product updates do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.