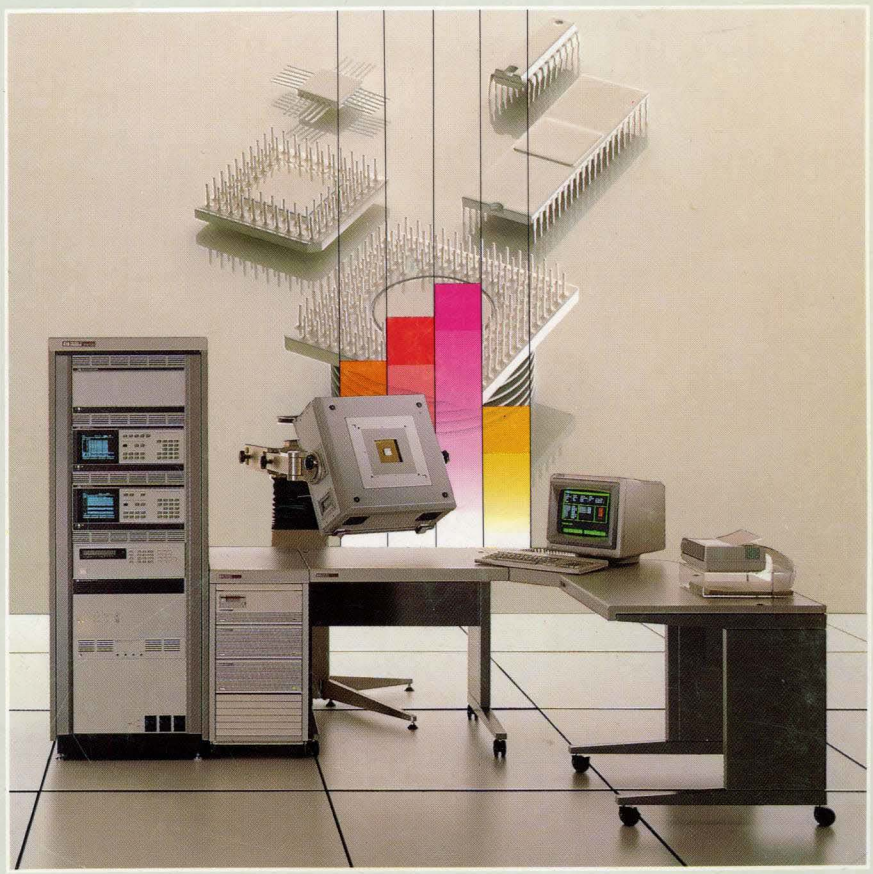
HEWLETT-PACKARD

HP 81810S IC Design Verification System

HP 8180 Data Generator
HP 8181 Data Generator Extender
HP 8182 Data Analyzer

Service Information



HP 81810S IC Design Verification System

HP 8180 Data Generator

HP 8181 Data Generator Extender

HP 8182 Data Analyzer

Service Information

Manual Part Number: 08180-90067

Printed in West Germany. December 1987

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of the other International Standard's Organization members.

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Warranty services of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, HP service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to buyer. Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted and error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer supplied software or interfacing, unauthorized modifications or misuse, operation outside of the environmental specifications for the products, or improper site preparation or maintenance.

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LIST OF EFFECTIVE PAGES

The list of effective pages gives the date of the current edition, and lists the dates of all pages of that edition and all updates. Within this manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. Changes are marked with a vertical bar in the margin. If an update is incorporated when an edition is reprinted, these bars and dates remain. No information is incorporated into a reprint unless it appears as a prior update.

Issue 1.0 December 1987

Effective Pages	Date
ALL	December 1987

PRINTING HISTORY

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PREFACE

PURPOSE OF THIS MANUAL

The purpose of this manual is to provide the necessary information to troubleshoot and repair faults on the HP 8180A/B Data Generator, HP 8181A/B Data Generator Extender and HP 8182A/B Data Analyzer, which are part of the HP 81810S IC Design Verification System.

AUDIENCE

This manual is aimed at Service Personnel involved in the repair of the above mentioned instruments.

HOW TO USE THIS MANUAL

This manual should be used as a guide when troubleshooting the individual instruments. Section 1 gives information on how to begin the fault-finding process.

RELATED PUBLICATIONS

This section contains a list of all publications related to installation, operation and maintenance of the HP 81810S IC Design Verification System. The publications can be ordered by quoting the relevant part number.

Title	Part Number
HP 8180 Data Generator HP 8181 Data Generator Extender HP 8182 Data Analyzer Operating and Programming Manual	08180-90066
HP 15466A 256 Pin Testhead Operating and Programming Manual	15466-90001
HP 81804A CAE Link Software Users Manual	81804-90001
HP 81810A System Software Users Manual	81810-90001
System Configuration Manual	81810-90010
System Service Information	81810-90012
HP 8180 Data Generator HP 8181 Data Generator Extender HP 8182 Data Analyzer Service Information (this manual)	08180-90067

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General Information

1-1 Introduction

This chapter contains information on safe working practices, recommended test equipment and using the test procedures described in the following chapters.

1-2 Safe Working Practices

The Models 8180A/B, 8181A/B and 8182A/B are Safety Class 1 instruments (instruments with an exposed metal chassis that is directly connected to earth via the power supply cable).

Before operation, the instruments and manual, including the red safety page, should be reviewed for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instruments in a safe condition.

CAUTION

The HP 8180A/B, HP 8181A/B and HP 8182A/B contain assemblies and components that are sensitive to electrostatic discharge. Ensure that your working area conforms to Corporate Standard 741.080.

Carefully observe precautions and recommended procedures outlined below to avoid compromising the instrument's reliability because of component damage from static electricity.

- Treat all assemblies, components and connections as static sensitive.
- When unpacking new boards, keep them in their conductive plastic bags until you are ready to install them.
- Before removing the top cover from the instrument, select a work area where potential static sources are minimized. If possible, use a controlled-static workstation (HP 9300-0933 or equivalent) that includes personnel grounding provisions.
- Avoid touching any metal parts on the boards. When you are ready to install an upgrade board, remove it from its protective bag and lay it on top of the bag while keeping your free hand in contact with the bag.

1-3 Recommended Equipment

Test Equipment

The test equipment required for the adjustment and performance verification procedures is listed below. Critical specifications of substituted test instrument must meet or exceed the standards given with the equipment list.

Instrument	Type	Critical Specification	
Oscilloscope	HP54100D	Resolution	100ps/DIV
		Time base acc.	<=100 ps
Probe	HP54001A	Bandwidth	>=700MHz
		Transition time	<450 ps
Probe	HP54002A	50 Ohm	
		Transition time	<=350 ps
Counter	HP5370B	Frequency range	>50 MHz
DVM	HP3456A	Range	10V
		Resolution	100 uV
Signature Analyzer	HP5005A	f max	>20 MHz
Pulse Generator:	A pulse generator capable of meeting all requirements is not available. The critical specifications are given in each test/adjustment procedure. You need to select a pulse generator from the HP range that fits the particular application.		
Power Supply:	HP6002A	Voltage range	>20V
		Resolution	1 mV
Data Generator:	HP8018A	Vector depth	1kBit
		Bit rate	>50 MHz

Accessories

Cables

Strobe/Clock	15422A
DATA Cable	15423A
Clock Probe	15406A
DATA Cable	15407A
Interface Cable	08181-61604
Interface Cable	08181-61603

Adapters

Grabbers	15408A
BNC Adaptor	15409A
Miniprobe Adaptor	15415A
Solder in receptacles	15426A

Connectors

50 OHM Feedthrough	10100C
BNC Attenuator 20dB/20W	Texscan HFP 50/20
BNC TEE Connector	1250-0781
BNC female/female	1250-0080
Scope Probe Adapter	1250-1454
BNC/Dual Banana	1251-2277

Delay Lines

90.5 ns (A-version)	08180-61636
90.5 ns (B-version)	08180-61696
34 ns	08182-61622
3 ns	08182-61621

Extender Boards

BD AY Extender	08180-66557
BD AY Extender	08180-66556
BD AY Extender	08180-66555
BD AY Extender	08180-66554
BD AY Extender	08180-66553
BD AY Extender	08180-66552
BD AY Extender	08180-66551
BD AY Extender	08180-66550

Adjustment Cover	08180-04103

1-4 Using the Test Procedures

General

1. Before adjusting an 8180A/B, 8181A/B or 8182A/B allow the instrument to warm up for 30 minutes.

2. Power supply adjustments must be done with all boards inserted.

3. The adjustment procedures can be used for the A- as well as the B-version. Any differences in the adjustment procedures for the two versions are notified in text.

4. Timing adjustments must be performed with the adjustment cover in place. For the A-version all adjustment holes in the adjustment cover must be blocked with adhesive tape. During adjustment, the tape should only be removed for a few seconds. Each adjustment hole should be closed immediately after the adjustment has been performed.

5. If a B instrument needs to be adjusted, the adjustment cover should be prepared as follows: block the circular hole with adhesive tape, block the two holes which are located above the A8 board with adhesive tape.

6. If only a sub procedure is to be performed, always carry out the whole adjustment procedure starting with step 1.

7. Trigger delay of the channel used as reference, as well as interchannel delay of the 54100D scope must be calibrated before timing measurements can be performed.

Chapter 2
Exploded Diagrams, Parts Lists

2-1 Introduction

This chapter gives the exploded diagrams and associated parts lists, and exchange boards lists for the HP 8180B generator, the HP 8181B extender and the HP 8182B analyzer. The A-versions are fully documented in the service part of the existing Operating and Service Manual.

2-2 Parts Lists for the HP 8180B

Module Parts List

Reference Designator	HP Part Number	Description
FRAME		
A61	08180-66561	BD AY U-PRCP
A62	08180-66562	BD AY INTERF
A63	08180-66563	BD AY ADDRESS
A64	08180-66564	BD AY SYNC
A65	08180-66565	BD AY TIMING
A66	08180-66566	BD AY MODULE
A68	08180-66568	BD AY ADDR. CTRL. II
A72	08180-66572	BD AY MOTHER
A76	08180-66576	BD AY TEMP CTRL
A661	08180-62661	MDL AY PWR SPLY
A672	08180-62672	MDL AY DISP
A663	08180-62663	PNL AY REAR
B1	3160-0510	DC MOTOR FAN
B2	3160-0510	DC MOTOR FAN
F1A	2110-0051	FUSE 10A 115V
F1E	2110-0010	FUSE 5A 250V
FL1	9135-0192	FILTER LINE
MP0	1250-0083	CONN BNC BLKHD
MP1	08180-00262	PANEL REAR
MP4	08180-01205	BRACKET FAN
MP5	08180-00204	PANEL REAR PS
MP6	08180-04111	COVER TOP PS
MP7	08180-04102	PANEL SIDE PS
MP8	08180-01202	BRACKET PERF.
MP9	01830-23201	COUPLER SW 10-24
MP10	0403-0374	BUMPER FOOT
MP11	5040-1148	SHAFT SHORT/GRAY

Reference Designator	HP Part Number	Description
MP12	5040-1149	SHAFT LONG/GRAY
MP13	08180-04101	PANEL SIDE PS
MP14	08180-01206	BRKT PS
MP15	08180-04110	COVER TOP CRT MOD
MP16	08180-64701	MODULE CRT
MP17	08180-01203	CLAMP CRT
MP18	5021-0508	PANEL FRONT
MP19	08180-00201	PANEL KEYBD
MP20	4040-2097	FACEPLATE SAFETY
MP21	1400-0678	CLAMP
MP22	08180-04115	PLATE SAFETY
MP23	08180-04155	COVER TOP
MP25	5041-6820	CAP, HANDLE REAR
MP26	5060-9804	STRAP HDL 18IN
MP28	5041-6819	CAP, HANDLE FRONT
MP30	5021-0519	FRM FRNT 7SPCL
MP31	1460-1345	TILT STAND
MP32	5040-7201	FOOT
MP33	5061-9447	COVER BOTTOM
MP34	08160-04101	COVER SIDE PERF.
MP134	5060-9884	COVER SIDE
MP35	5001-8233	SIDE GUSSET
MP36	08180-05001	CATCH
MP37	08180-02301	HOLDER DISTANCE
MP38	08180-00102	CAGE CARD
MP39	5021-5837	CORNER STRUT
MP40	5021-5806	FRAME REAR 7IN
MP41	5040-7221	FOOT REAR
MP42	5040-9319	SHAFT PWR SWITCH
MP43	5040-9320	STOP PWR SWITCH
MP44	08160-0438	RFI STRIP FINGER
MP45	0363-0125	CONTACT FINGER
MP47	5040-7202	TRIM STRIP TOP
MP48	5001-0440	TRIM STRIP SIDE
MP50	9140-0726	WIRE AY YOKE
MP52	08180-03101	GUIDE POWER SHAFT
MP53	2140-0352	LAMP INDC TI 18V
MP54	08180-47401	KEY CUP
MP135	1251-0218	POST CON
MP136	08180-01282	STRAP TOP
V1	2090-0706	CRT

Reference Designator	HP Part Number	Description
W7	08180-61681	CBL AY SHLD STROBE
W8/9	08180-61609	CBL AY PAIR
W10	08180-61670	CBL AY MASTER
W11	08180-61616	CBL AY REAR #2
W12	08180-61688	CBL AY SHLD SET
W16	08180-61661	CBL AY RBN TW 8P
W17	08180-61662	CBL AY RBN TW 7P
W18	5180-2418	CBL AY RBW 230 MM
W20	08180-61607	CBL AY VIDEO
W21	08180-61639	CBL AY CRT
W30	5180-2413	CBL RBN 230 MM

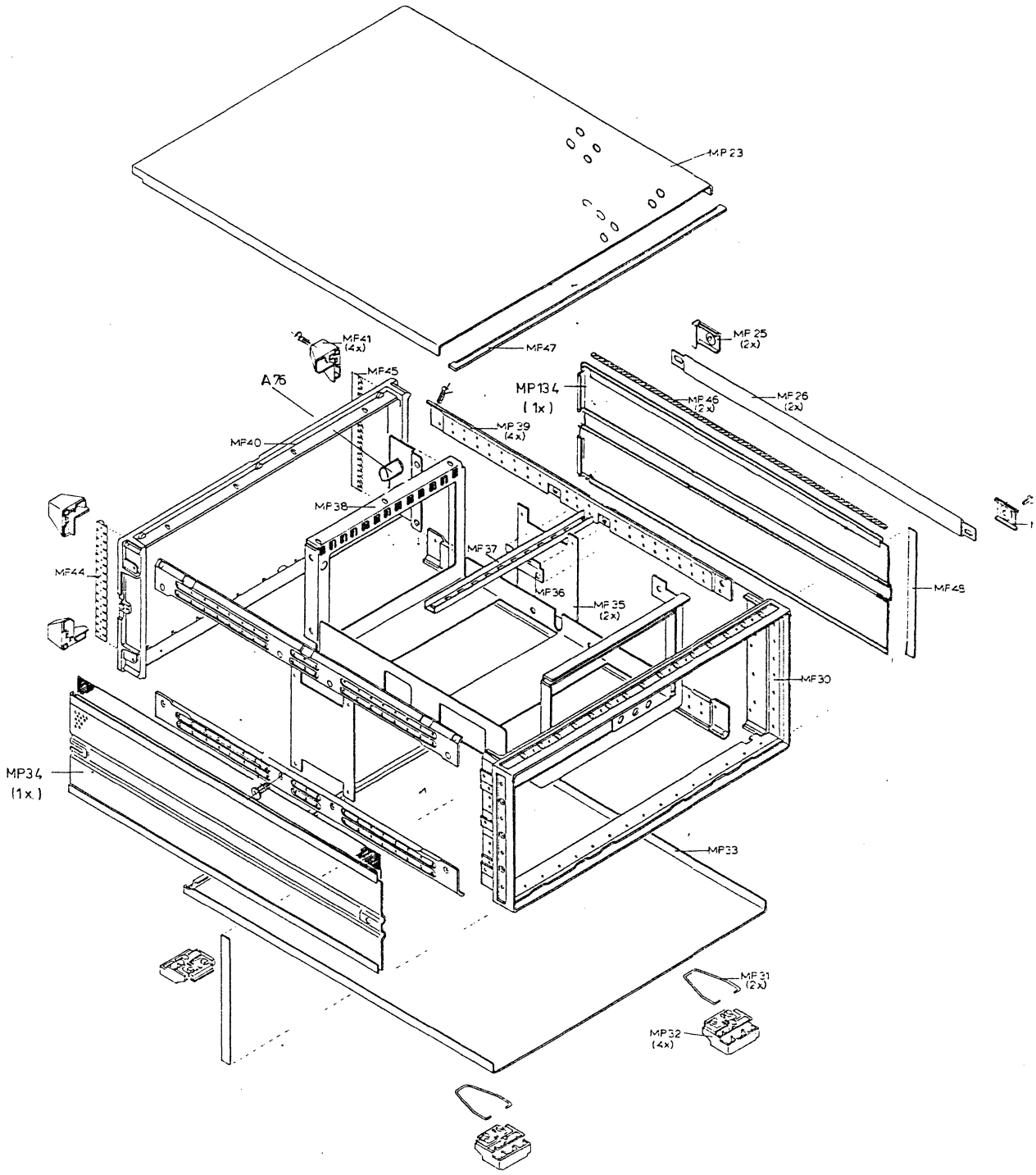


Figure 2-1. 8180B Chassis Parts

Power Supply Parts List 8180B

Reference Designator	HP Part Number	Description	BD NO.
A661	08180-62661	MDL PWR SUPPLY	
A24	08180-66524	BD AY FILTER	
A26	08180-66526	BD AY REG +15, -7V	
A28	08180-66528	BD AY CAPACITOR	
A81	08180-66581	BD AY MOTHER	
A82	08180-66582	BD AY RECTIFIER	
A83	08180-66583	BD AY SWITCHING	
A85	08180-66585	BD AY +5V -5V	
A87	08180-66587	BD AY +23V	
F101	2112-0002	FUSE 2A 250V NT	
J1	1251-0472	CONN PC	A81
J2	1251-2035	CONN PC	A81
J3	1251-2035	CONN PC	A81
J5	1251-2034	CONN PC	A81
J6	1251-2034	CONN PC	A81
J7	1251-2034	CONN PC	A81
J8	1251-2034	CONN PC	A81
S1	3101-2624	SWITCH PWR	A81
T1	08180-61105	XFMR AY	A81
F201	2110-0456	FUSE 10A 125V	A82
F202	2110-0456	FUSE 10A 125V	A82
F203	2110-0653	FUSE MINI 15A	A82
F204	2110-0653	FUSE MINI 15A	A82
F205	2110-0653	FUSE MINI 15A	A82
F206	2110-0653	FUSE MINI 15A	A82
F207	2110-0456	FUSE 10A	A82
F208	2110-0456	FUSE 10A	A82
F209	2110-0456	FUSE 10A	A82
F210	2110-0456	FUSE 10A	A82
F211	2110-0456	FUSE 10A	A82
F212	2110-0456	FUSE 10A	A82
F213	2110-0456	FUSE 10A	A82
F214	2110-0456	FUSE 10A	A82
F215	2110-0456	FUSE 10A	A82
MP1	4040-0750	BD EXTR RED	A82
MP2	4040-0748	BD EXTR POLY	A82
MP1	4040-0751	BD EXTR ORN	A83
MP1	4040-0753	BD EXTR GRN	A85
MP1	4040-0755	BD EXTR VIO	A87

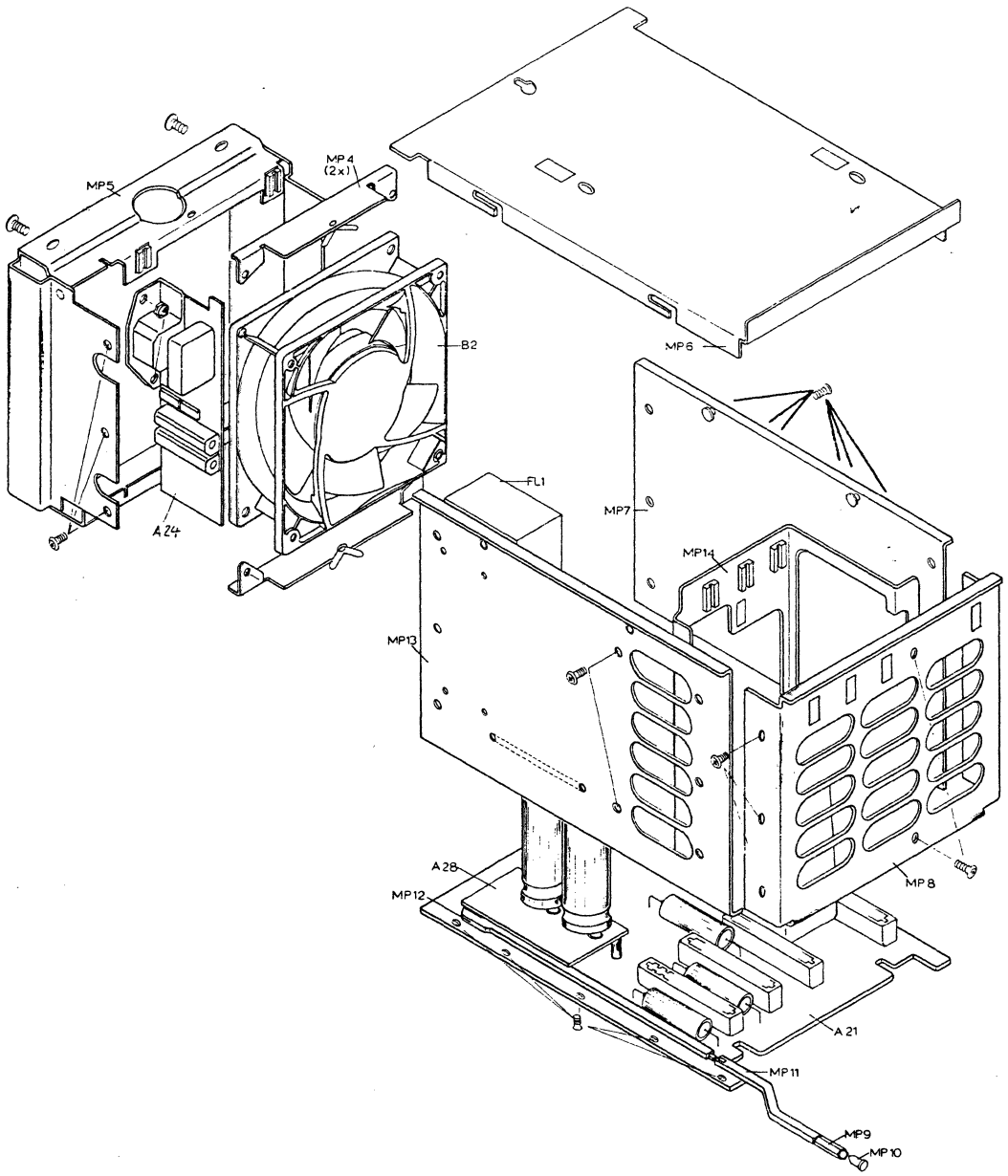


Figure 2-2. A661 Power Supply Module

Display Module Assembly Parts List 8180B

Reference Designator	HP Part Number	Description	BD NO.
A15	08180-66515	BD AY KEY	
A30	08180-66530	BD AY CNTL	
A32	08180-66532	BD AY DFL VRT	
AA34	08180-66534	BD AY DFL HORZ	
MP15	08180-04110	COVER TOP CRT	
MP16	08180-64701	MODULE CRT	
MP17	08180-01203	CLAMP CRT	
MP18	5021-0508	PANEL FRONT	
MP19	08180-00201	PANEL KEYBD	
MP20	4040-2097	FACEPLATE SAFET	
MP21	1400-0678	CLAMP	
MP30	5021-0519	FRM FRNT	
MP47	5040-7202	TRIM STRIP TOP	
MP48	5001-0440	TRIM STRIP SIDE	
MP50	9140-0726	DEFLECTION YOKE	
MP53	2140-0352	LAMP INCD TI18V	
V1	2090-0706	CRT	
W21	08180-61639	CBL AY CRT	

Keyboard Assembly Parts List

A15	08180-66515	BD AY KEY
MP70	5041-0846	KNOB NOM 0
MP71	5041-0847	KNOB NOM 1
MP72	5041-0848	KNOB NOM 2
MP73	5041-0849	KNOB NOM 3
MP74	5041-0850	KNOB NOM 4
MP75	5041-0851	KNOB NOM 5
MP76	5041-0852	KNOB NOM 6
MP77	5041-0853	KNOB NOM 7
MP78	5041-0854	KNOB NOM 8
MP79	5041-0855	KNOB NOM 9
MP80	5041-2756	KNOB A
MP81	5041-2757	KNOB B
MP82	5041-2758	KNOB C
MP83	5041-2759	KNOB D
MP84	5041-2760	KNOB E
MP85	5041-2761	KNOB F

MP86	5041-2763	KNOB +/-
MP87	5041-0841	KEY CUP
MP88	5041-0409	KNOB NOM BLK
MP89	5041-2765	KNOB RUN
MP90	5041-2755	KNOB STOP
MP91	5041-2766	KNOB BREAK
MP92	5041-2767	KNOB BACK
MP93	5041-2764	KNOB FWD
S1/34	5060-9436	SW P-BTN SINGLE
W21	5180-2421	CBL RBN

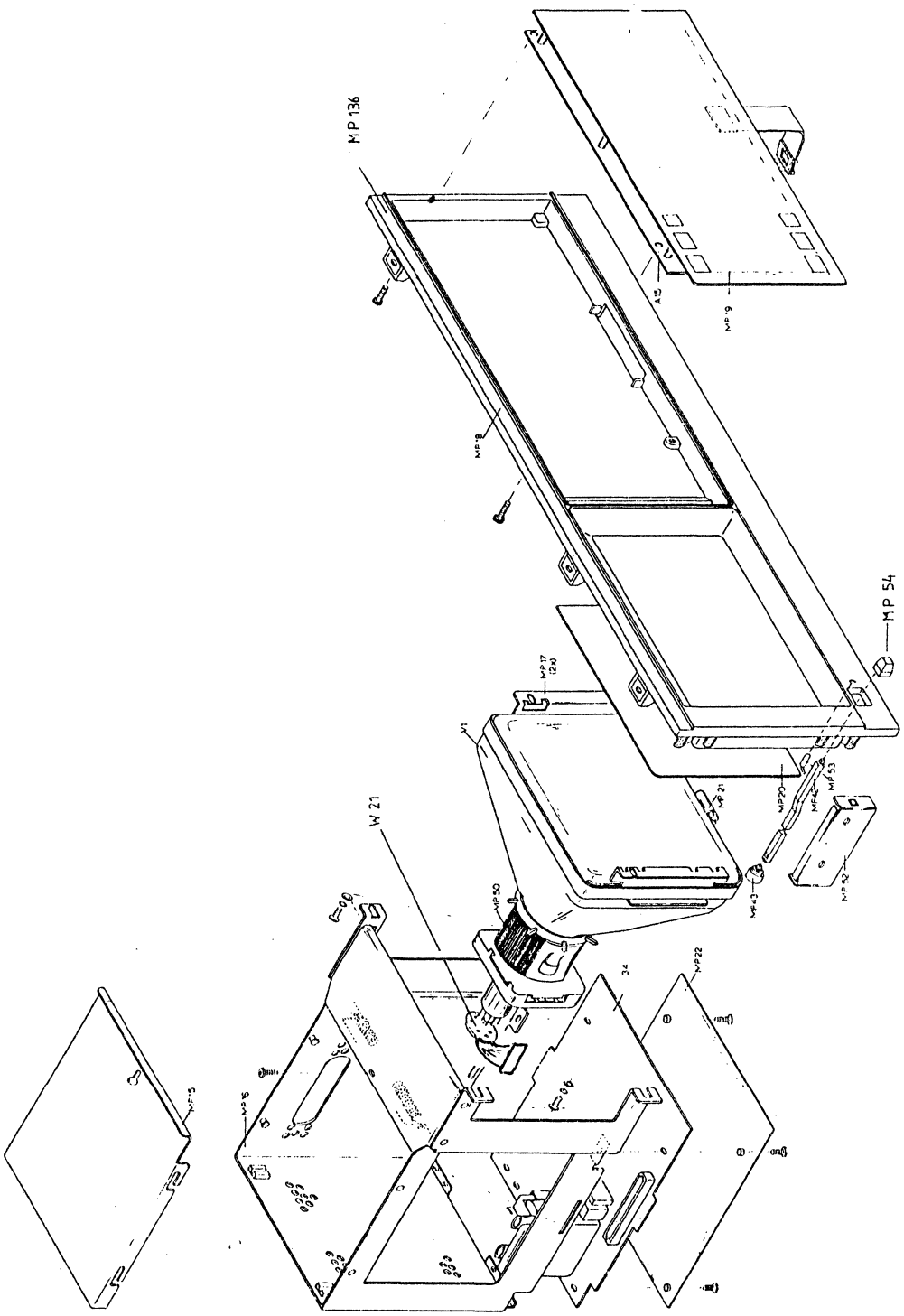


Figure 2-3. A672 Display Module

Rear Panel Assembly Parts List 8180B

Reference Designator	HP Part Number	Description	BD NO.
A663	08180-62663	PNL AY REAR	
A40	08180-66540	BD AY HP-IB	
B1	3160-0510	FAN - DC	
MP0	1250-0083	CONN BNC BLKHD	
MP1	08180-00262	PANEL REAR	
MP4	08180-01205	BRACKET FAN	
W11	08180-61616	CBL AY REAR #2	
W20	08180-61607	CBL AY VIDEO	
W8/9	08180-61609	CBL AY PAIR	

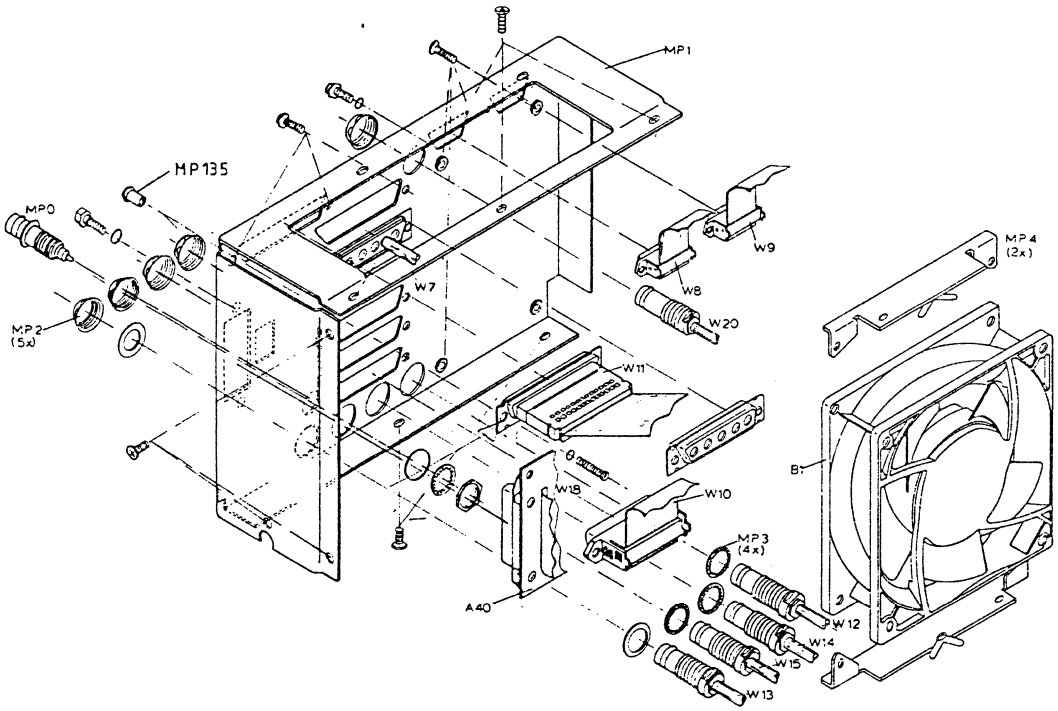


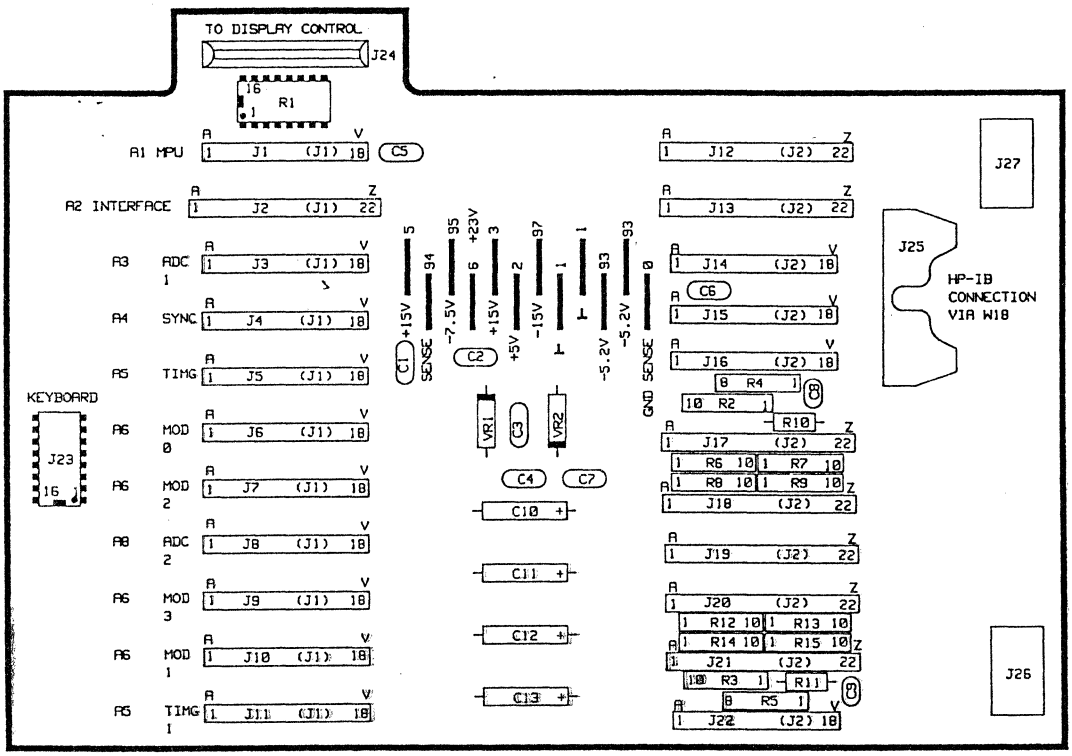
Figure 2-4. Rear Panel Assembly

This is a replaceable parts list on a sub-assembly level.

Reference Designator	HP Part Number	Description	BD NO.
A61	08182-66561	BD AY U PRCR	
BT100	1420-0251	BATTERY NICAD	A61
MP1	4040-0749	PC EXTR BD BRN	A61
MP2	4040-0748	PC EXTR BD POLY	A61
A62	08182-66562	BD AY INTERFC	
BT1	1420-0251	BATTERY NICAD	A62
J3	1251-4267	CONNECTOR POST	A62
J3A	1250-1737	CC AXIAL TEST P	A62
MP3	4040-0750	PC EXTR BD RED	A62
MP2	4040-0748	PC EXTR BD POLY	A62
A63	08182-66563	BD AY ADDRESS	
DL110	1810-0616	DEL LINE 14 P	A63
DL111	1810-0616	DEL LINE 14 P	A63
J3/4	1250-1737	CC AXIAL TEST P	A63
MP1	4040-0751	PC EXTR BD ORN	A63
MP2	4040-0748	PC EXTR BD POLY	A63
A64	08182-66564	BD AY CNTL	
DL101	1810-0616	DELAY LINE 14 P	A64
DL103	1810-0616	DELAY LINE 14 P	A64
DL104	1810-0616	DELAY LINE 14 P	A64
DL201	1810-0616	DELAY LINE 14 P	A64
J4/J8	1250-1737	CC AXIAL TEST P	A64
MP1	4040-0752	PC EXTR BD YEL	A64
MP2	4040-0748	PC EXTR BD POLY	A64
A65	08182-66565	BD AY DATA	
DL107	1810-0616	DELAY LINE 14 P	A65
DL207	1810-0616	DELAY LINE 14 P	A65
DL307	1810-0616	DELAY LINE 14 P	A65
DL407	1810-0616	DELAY LINE 14 P	A65
MP1	4040-0754	PC EXTR BD BL	A66
MP2	4040-0748	PC EXTR BD POLY	A66
W1	08180-61601	CBL AY MDL	A66

This is a replaceable parts list on a sub-assembly level.

Reference Designator	HP Part Number	Description	BD NO.
A68	08180-66568	BD AY ADR CTL 2	
DL1/DL7	1810-0616	DELAY LINE 14 P	A68
DL8	1810-0893	DELAY LINE 10 NS	A68
J3/J5	1250-1737	CC AXIAL TEST P	A68
J6	1200-0588	SOCKET IC 16 CON	A68
J8/J11	1200-0548	SOCKET IC 14 CON	A68
MP1	4040-0747	PC EXTR BD GRA	A68
MP2	4040-0748	PC EXTR BD POLY	A68
A72	08180-66572	BD AY MOTHER	
J1	1251-2026	CONN PC 36 CONT	A72
J2	1251-1365	CONN PC 44 CONT	A72
J3	1251-2026	CONN PC 36 CONT	A72
J4	1251-2026	CONN PC 36 CONT	A72
J5	1251-2026	CONN PC 36 CONT	A72
J6	1251-2026	CONN PC 36 CONT	A72
J7	1251-2026	CONN PC 36 CONT	A72
J8	1251-2026	CONN PC 36 CONT	A72
J9	1251-2026	CONN PC 36 CONT	A72
J10	1251-2026	CONN PC 36 CONT	A72
J11	1251-2026	CONN PC 36 CONT	A72
J12	1251-1365	CONN PC 44 CONT	A72
J13	1251-1365	CONN PC 44 CONT	A72
J14	1251-2026	CONN PC 36 CONT	A72
J15	1251-2026	CONN PC 36 CONT	A72
J16	1251-2026	CONN PC 36 CONT	A72
J17	1251-1365	CONN PC 44 CONT	A72
J18	1251-1365	CONN PC 44 CONT	A72
J19	1251-1365	CONN PC 44 CONT	A72
J20	1251-1365	CONN PC 44 CONT	A72
J21	1251-1365	CONN PC 44 CONT	A72
J22	1251-2026	CONN PC 36 CONT	A72
J23	1200-0607	SKT IC 16 CONT	A72
J24	1251-3004	CONN POST	A72
J25	1251-0541	CONN 34 PIN	A72



A12 MOTHERBOARD 08180-66572

Figure 2-5. A12 Motherboard

2-3 Parts Lists for the HP 8181B

Reference Designator	HP Part Number	Description	BD NO.
Frame			
A61	08181-66561	BD AY MULTIPLEX	
A62	08180-66562	BD AY GEN MDL	
A66	08180-66566	BD AY MODULE	
A68	08181-66568	BD AY ADR CNTL2	
A72	08181-66572	BD AY MOTHER	
A76	08180-66576	BD BD AY Fan Filter	
A661	08180-62661	MDL AY PWR SPLY	
A663	08181-62663	PNL AY REAR	
B1	3160-0510	DC MOTOR FAN	
B2	3160-0510	DC MOTOR FAN	
F1A	2110-0051	FUSE 10A 115V	
F1E	2110-0010	FUSE 5A 250V	
FL1	9135-0192	FILTER LINE	
MP1	08181-00264	PANEL REAR	
MP4	08180-01205	BRACKET FAN	
MP5	08180-00204	PANEL REAR PS	
MP6	08180-04111	COVER TOP PS	
MP7	08180-04102	PANEL SIDE PS	
MP8	08180-01202	BRACKET PERF.	
MP9	01830-23201	COUPLER SW 10-24	
MP10	0403-0374	BUMPER FOOT	
MP11	5040-1148	SHAFT SHORT/GRAY	
MP12	5040-1149	SHAFT LONG/GRAY	
MP13	08180-04101	PANEL SIDE PS	
MP14	08180-01206	BRKT PS	
MP18	08181-00262	PANEL FRONT	
MP23	08181-04155	COVER TOP	
MP25	5041-6820	CAP, HANDLE REAR	
MP26	5060-9804	STRAP HDL 18IN	
MP28	5041-6819	CAP, HANDLE FRONT	
MP30	5021-0519	FRM FRNT 7SPCL	
MP32	5040-7201	FOOT	
MP33	5061-9447	COVER BOTTOM	
MP34	08160-04101	COVER SIDE PERF.	
MP134	5060-9884	COVER SIDE	
MP35	5001-8233	SIDE GUSSET	

Reference Designator	HP Part Number	Description	BD NO.
MP36	08180-05001	CATCH	
MP37	08180-02301	HOLDER DISTANCE	
MP38	08181-00102	CAGE CARD	
MP39	5021-5837	CORNER STRUT	
MP40	5021-5806	FRAME REAR 7IN	
MP41	5040-7221	FOOT REAR	
MP42	5040-9319	SHAFT PWR SWITCH	
MP43	5040-9320	STOP PWR SWITCH	
MP44	08160-0438	RFI STRIP FINGER	
MP45	0363-0125	CONTACT FINGER	
MP46	8160-0428	RFI ROUND STRIP	
MP52	08180-03101	GUIDE POWER SHAFT	
MP53	2140-0352	LAMP INDC TI 18V	
MP54	08180-47401	KEY CUP	
MP135	1251-0218	POST CON	
MP136	08181-1282	STRAP TOP	
W7	08180-61609	CBL AY PAIR	
W8	08181-61601	CBL AY BUS	

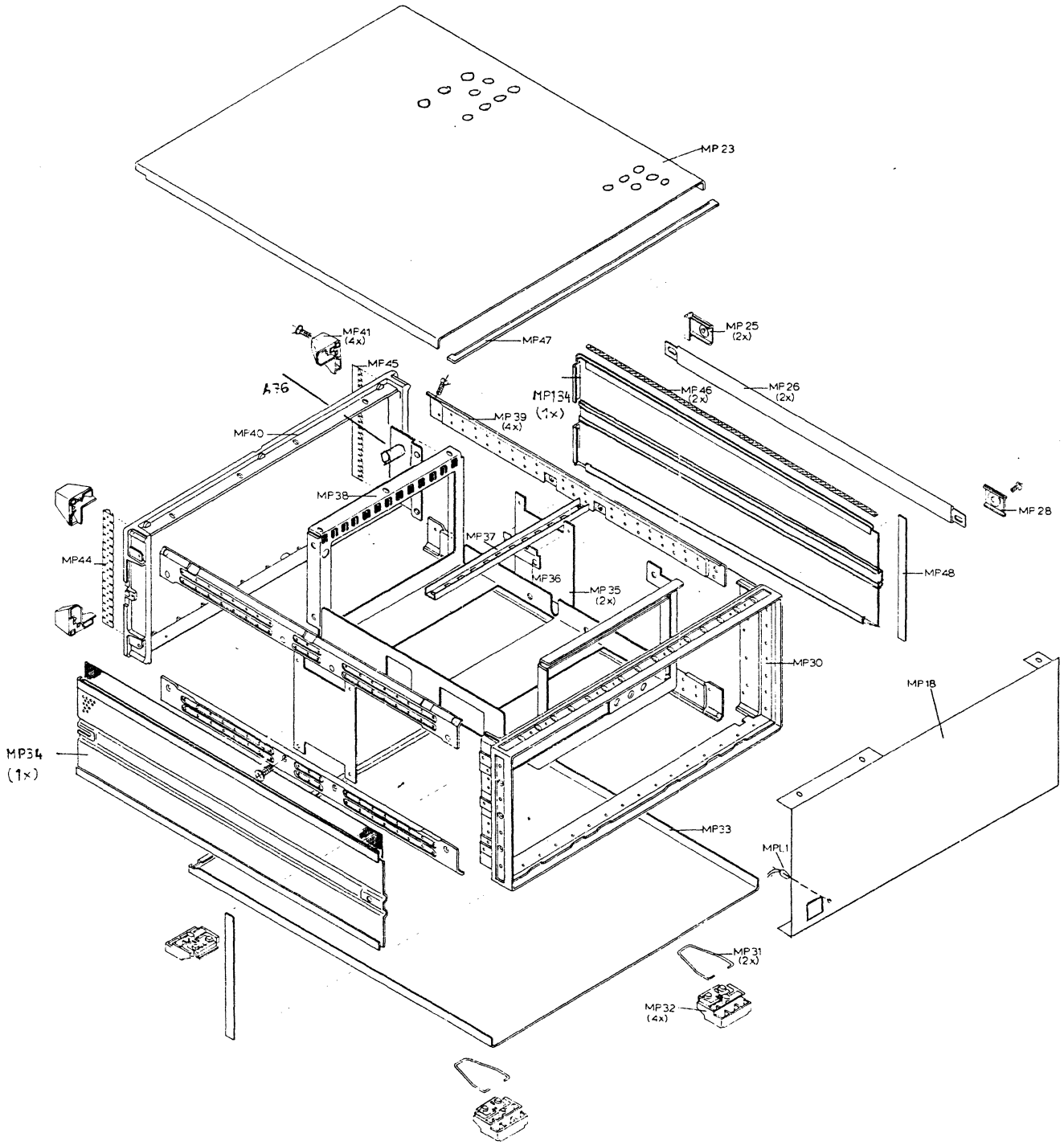


Figure 2-6. 8181B Chassis Parts

Power Supply Module Parts List 8181B

Reference Designator	HP Part Number	Description	BD NO.
A661	08180-62661	MDL PWR SUPPLY	
A24	08180-66524	BD AY FILTER	
A26	08180-66526	BD AY REG +15, -7V	
A28	08180-66528	BD AY CAPACITOR	
A81	08180-66581	BD AY MOTHER	
A82	08180-66582	BD AY RECTIFIER	
A83	08180-66583	BD AY SWITCHING	
A85	08180-66585	BD AY +5V -5V	
A87	08180-66587	BD AY +23V	
F101	2112-0002	FUSE 2A 250V NT	
J1	1251-0472	CONN PC	A81
J2	1251-2035	CONN PC	A81
J3	1251-2035	CONN PC	A81
J5	1251-2034	CONN PC	A81
J6	1251-2034	CONN PC	A81
J7	1251-2034	CONN PC	A81
J8	1251-2034	CONN PC	A81
S1	3101-2624	SWITCH PWR	A81
T1	08180-61105	XFMR AY	A81
F201	2110-0456	FUSE 10A 125V	A82
F202	2110-0456	FUSE 10A 125V	A82
F203	2110-0653	FUSE MINI 15A	A82
F204	2110-0653	FUSE MINI 15A	A82
F205	2110-0653	FUSE MINI 15A	A82
F206	2110-0653	FUSE MINI 15A	A82
F207	2110-0456	FUSE 10A	A82
F208	2110-0456	FUSE 10A	A82
F209	2110-0456	FUSE 10A	A82
F210	2110-0456	FUSE 10A	A82
F211	2110-0456	FUSE 10A	A82
F212	2110-0456	FUSE 10A	A82
F213	2110-0456	FUSE 10A	A82
F214	2110-0456	FUSE 10A	A82
F215	2110-0456	FUSE 10A	A82
MP1	4040-0750	BD EXTR RED	A82
MP2	4040-0748	BD EXTR POLY	A82
MP1	4040-0751	BD EXTR ORN	A83
MP1	4040-0753	BD EXTR GRN	A85
MP1	4040-0755	BD EXTR VIO	A87

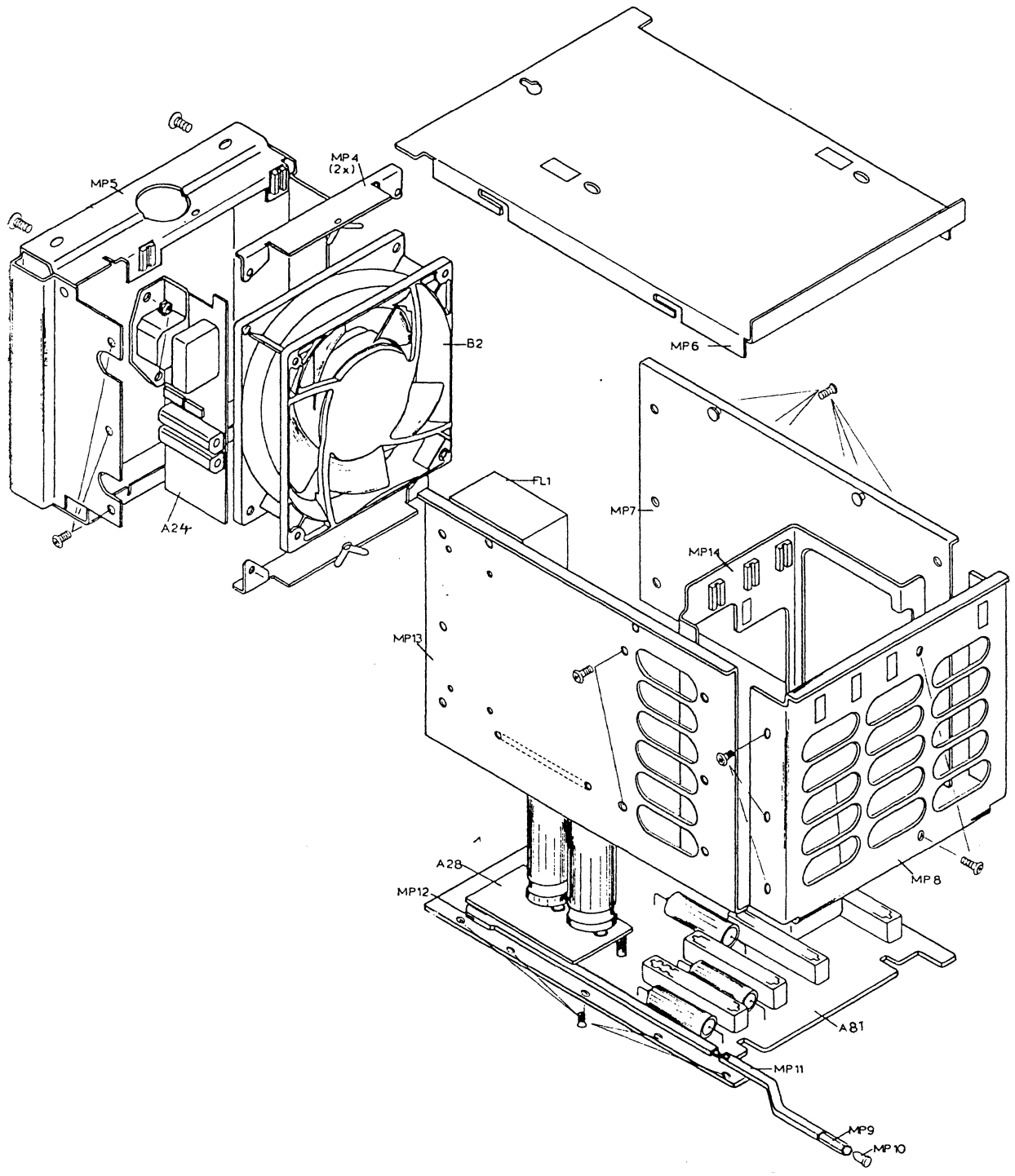


Figure 2-7. A661 Power Supply Module

Rear Panel Assembly Parts List for the 8181B

Reference Designator	HP Part Number	Description	BD NO.
A663	08181-62663	PNL AY REAR	
B1	3160-0510	FAN - DC	
MP1	08181-00264	PANEL REAR	
MP4	08180-01205	BRACKET FAN	
W7	08180-61609	CBL AY PAIR	
W8	08181-61601	CBL AY BUS	

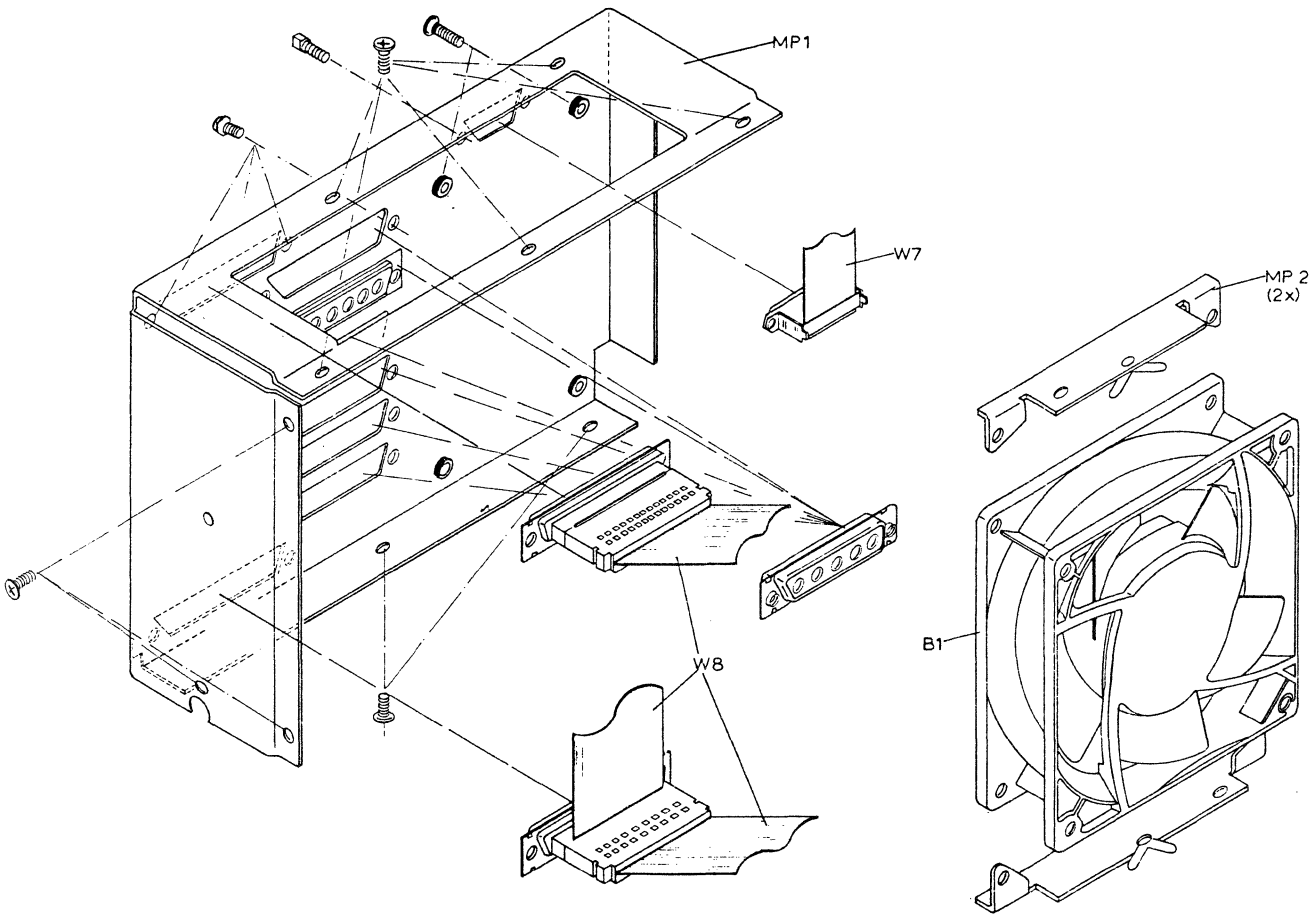
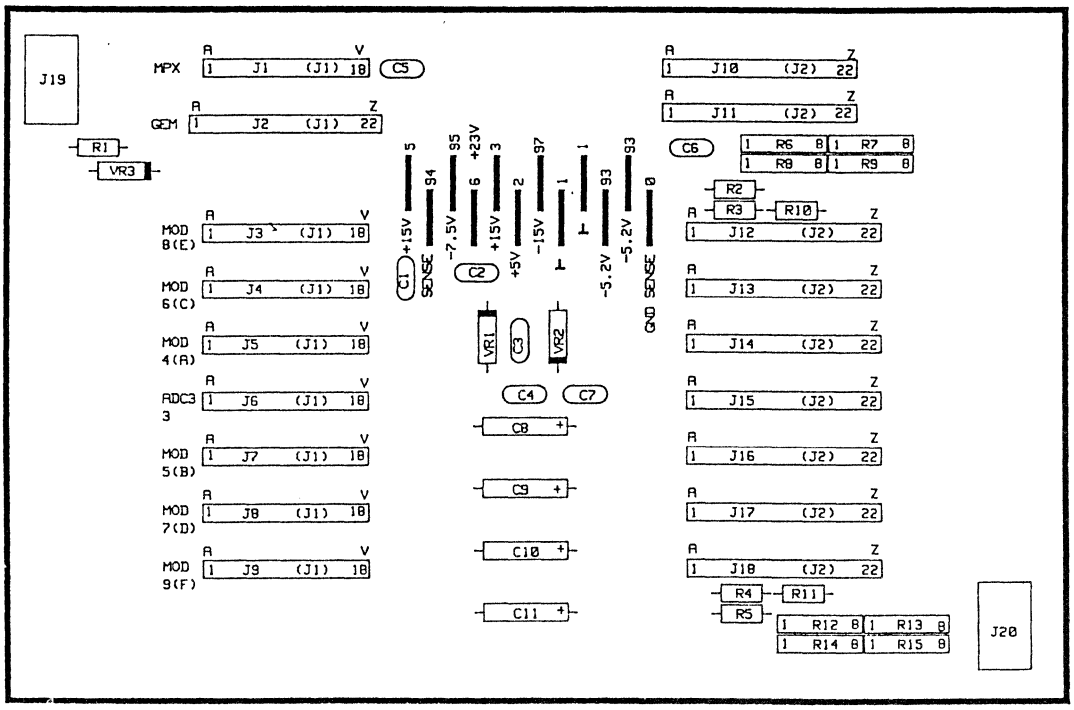


Figure 2-8. A663 Rear Panel Assembly

This is a replaceable parts list on a sub-assembly level

Reference Designator	HP Part Number	Description	BD NO.
A61	08181-66561	BD AY MULTIPLEXER	
J3	1251-3782	CONN	A61
MP1	4040-0749	PC EXTR BD BRN	A61
MP2	4040-0748	PC EXTR BD POLY	A61
A62	08180-66562	BD AY GEN MDL	
BT1	1420-0251	BATTERY NICAD	A62
MP1	4040-0750	PC EXTR BD RED	A62
MP2	4040-0748	PC EXTR BD POLY	A62
A66	08180-66566	BD AY MODULE	
MP1	4040-0754	PC EXTR BD BL	A66
MP2	4040-0748	PC EXTR BD POLY	A66
W1	08180-61601	CBL AY MDL	A66
A68	08181-66568	BD AY ADR CTL 3	
DL1	08181-61665	CBL AY DELAY LINE	A68
DL3	1810-0893	DELAY LINE 10 NS	A68
A72	08181-66572	BD AY MOTHER	
J1	1251-2026	CONN PC 36 CONT	A72
J2	1251-1365	CONN PC 44 CONT	A72
J3	1251-2026	CONN PC 36 CONT	A72
J4	1251-2026	CONN PC 36 CONT	A72
J5	1251-2026	CONN PC 36 CONT	A72
J6	1251-2026	CONN PC 36 CONT	A72
J7	1251-2026	CONN PC 36 CONT	A72
J8	1251-2026	CONN PC 36 CONT	A72
J9	1251-2026	CONN PC 36 CONT	A72
J10	1251-1365	CONN PC 44 CONT	A72
J11	1251-1365	CONN PC 44 CONT	A72
J12	1251-1365	CONN PC 44 CONT	A72
J13	1251-1365	CONN PC 44 CONT	A72
J14	1251-1365	CONN PC 44 CONT	A72
J15	1251-1365	CONN PC 44 CONT	A72
J16	1251-1365	CONN PC 44 CONT	A72
J17	1251-1365	CONN PC 44 CONT	A72
J18	1251-1365	CONN PC 44 CONT	A72
A76	08180-66576	BD AY TEMP CTRL	



A12 MOTHERBOARD 08181-66572

Figure 2-9. A12 Motherboard

2-4 Parts Lists for the HP 8182B

Module Parts List

Reference Designator	HP Part Number	Description	BD NO.
FRAME			
A61	08182-66561	BD AY U-PRCP	
A62	08182-66562	BD AY INTERF	
A63	08182-66563	BD AY ADDRESS	
A64	08182-66564	BD AY CNTL	
A65	08182-66565	BD AY DATA	
A6	08182-66506	BD AY CLOCK	
A8	08182-66508	BD AY HP-IB	
A67	08182-66567	BD AY MOTHER	
A661	08182-62661	MDL AY PWR SPLY	
A672	08182-62672	MDL AY DISP	
A663	08182-62663	PNL AY REAR	
B1	3160-0510	DC MOTOR FAN	
B2	3160-0510	DC MOTOR FAN	
F1A	2110-0249	FUSE 12A 115V	
F1E	2110-0056	FUSE 6A 250V	
FL1	9135-0192	FILTER LINE	
MP1	08182-00265	PANEL REAR	
MP4	08180-01205	BRACKET FAN	
MP5	08182-00204	PANEL REAR PS	
MP6	08180-04111	COVER TOP PS	
MP7	08180-04102	PANEL SIDE PS	
MP8	08180-01202	BRACKET PERF.	
MP9	01830-23201	COUPLER SW 10-24	
MP10	0403-0374	BUMPER FOOT	
MP11	5040-1148	SHAFT SHORT/GRAY	
MP12	5040-1149	SHAFT LONG/GRAY	
MP13	08180-04101	PANEL SIDE PS	
MP14	08182-01206	BRKT PS	
MP15	08180-04110	COVER TOP CRT MOD	
MP16	08180-64701	MODULE CRT	
MP17	08180-01203	CLAMP CRT	
MP18	5021-0508	PANEL FRONT	
MP19	08182-00201	PANEL KEYBD	
MP20	4040-2097	FACEPLATE SAFETY	
MP21	1400-0678	CLAMP	
MP22	08180-04115	PLATE SAFETY	

Reference Designator	HP Part Number	Description	BD NO.
MP23	08182-04155	COVER TOP	
MP25	5041-6820	CAP, HANDLE REAR	
MP26	5060-9804	STRAP HDL 18IN	
MP28	5041-6819	CAP, HANDLE FRONT	
MP30	5021-0519	FRM FRNT 7SPCL	
MP31	1460-1345	TILT STAND	
MP32	5040-7201	FOOT	
MP33	5061-9447	COVER BOTTOM	
MP34	08160-04101	COVER SIDE PERF.	
MP134	5060-9884	COVER SIDE	
MP35	5001-8233	SIDE GUSSET	
MP36	08180-05001	CATCH	
MP37	08182-02301	HOLDER DISTANCE	
MP38	08182-00101	CAGE CARD	
MP39	5021-5837	CORNER STRUT	
MP40	5021-5806	FRAME REAR 7IN	
MP41	5040-7221	FOOT REAR	
MP42	5040-9319	SHAFT PWR SWITCH	
MP43	5040-9320	STOP PWR SWITCH	
MP44	08160-0438	RFI STRIP FINGER	
MP45	0363-0125	CONTACT FINGER	
MP46	8160-0428	RFI ROUND STRIP	
MP47	5040-7202	TRIM STRIP TOP	
MP48	5001-0440	TRIM STRIP SIDE	
MP50	9140-0726	WIRE AY YOKE	
MP52	08180-03101	GUIDE POWER SHAFT	
MP53	2140-0352	LAMP INDC TI 18V	
MP54	08180-47401	KEY CUP	
MP136	08182-01282	STRAP TOP	
V1	2090-0706	CRT	
W1	08182-61610	CBL AY CLOCK QUAL	
W2	08182-61671	CBL AY TRG ARM	
W3	08182-61672	CBL AY TRG QUAL	
W4	08182-61673	CBL AY STOP	
W5	08182-61614	CBL AY CLOCK OUT	
W6	08182-61675	CBL AY ACTIVE OUT	
W7	08182-61676	CBL AY TRG OUT	
W8	08182-61677	CBL AY PULSED ERROR	
W9	08182-61678	CBL AY LATCHED ERROR	
W10	08182-61619	CBL AY SHLD VID	
W11	08182-61605	CBL AY CLOCK	
W12	08182-61601	CBL AY TWIN	
W14	08182-61606	CBL AY DATA	
W19	5180-2421	CBL AY HP-IB	
W21	08180-61639	CBL AY CRT	

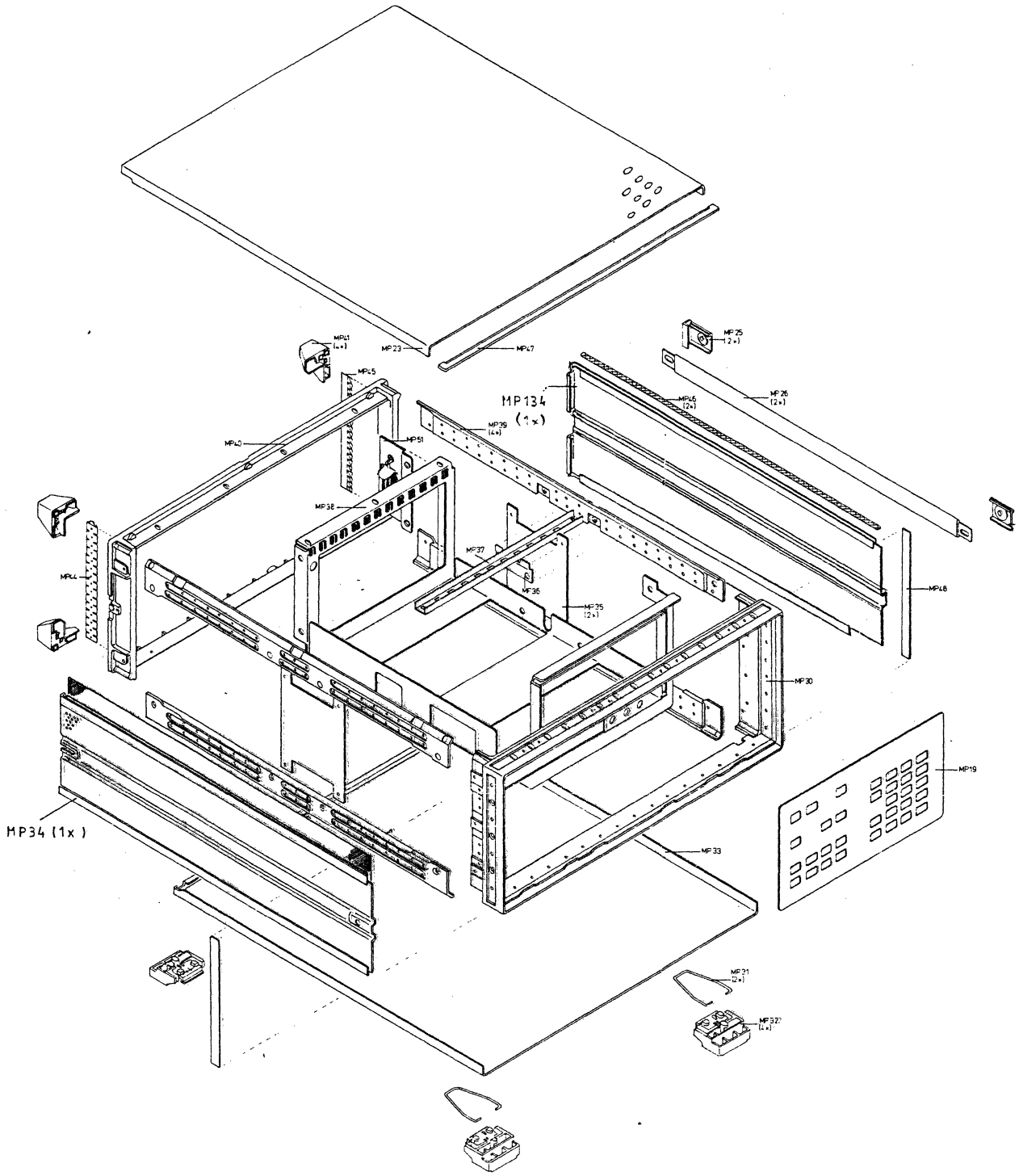


Figure 2-10 8182 Chassis Parts

Power Supply Module Parts List of the 8182B

Reference Designator	HP Part Number	Description	BD NO.
A661	08182-62661	MDL PWR SUPPLY	
A24	08182-66524	BD AY POST REG	
A25	08182-66526	BD AY INDUCTOR	
A26	08182-66526	BD AY REG +15, -10V	
A28	08180-66528	BD AY CAPACITOR	
A81	08182-66581	BD AY MOTHER	
A82	08182-66582	BD AY RECTIFIER	
A83	08182-66583	BD AY SWITCHING	
F101	2112-0002	FUSE 2A 250V NT	
J1	1251-0472	CONN PC	A81
J2	1251-5160	CONN PC	A81
J6	1251-2034	CONN PC	A81
J7	1251-2034	CONN PC	A81
S1	3101-2624	SWITCH PWR	A81
T1	08182-61105	XFMR AY	A81
F201	2110-0446	FUSE 10A 125V	A82
F202	2110-0446	FUSE 10A 125V	A82
F203	2110-0446	FUSE 10A 125V	A82
F204	2110-0446	FUSE 10A 125V	A82
F205	2110-0446	FUSE 10A 125V	A82
F206	2110-0446	FUSE 10A 125V	A82
F207	2110-0653	FUSE MINI 15A	A82
F208	2110-0653	FUSE MINI 15A	A82
F209	2110-0653	FUSE MINI 15A	A82
F210	2110-0653	FUSE MINI 15A	A82
F211	2110-0653	FUSE MINI 15A	A82
F212	2110-0653	FUSE MINI 15A	A82
F213	2110-0446	FUSE 10A 125V	A82
F214	2110-0446	FUSE 10A 125V	A82
MP1	4040-0750	BD EXTR RED	A82
MP2	4040-0748	BD EXTR POLY	A82
MP1	4040-0751	BD EXTR ORN	A83

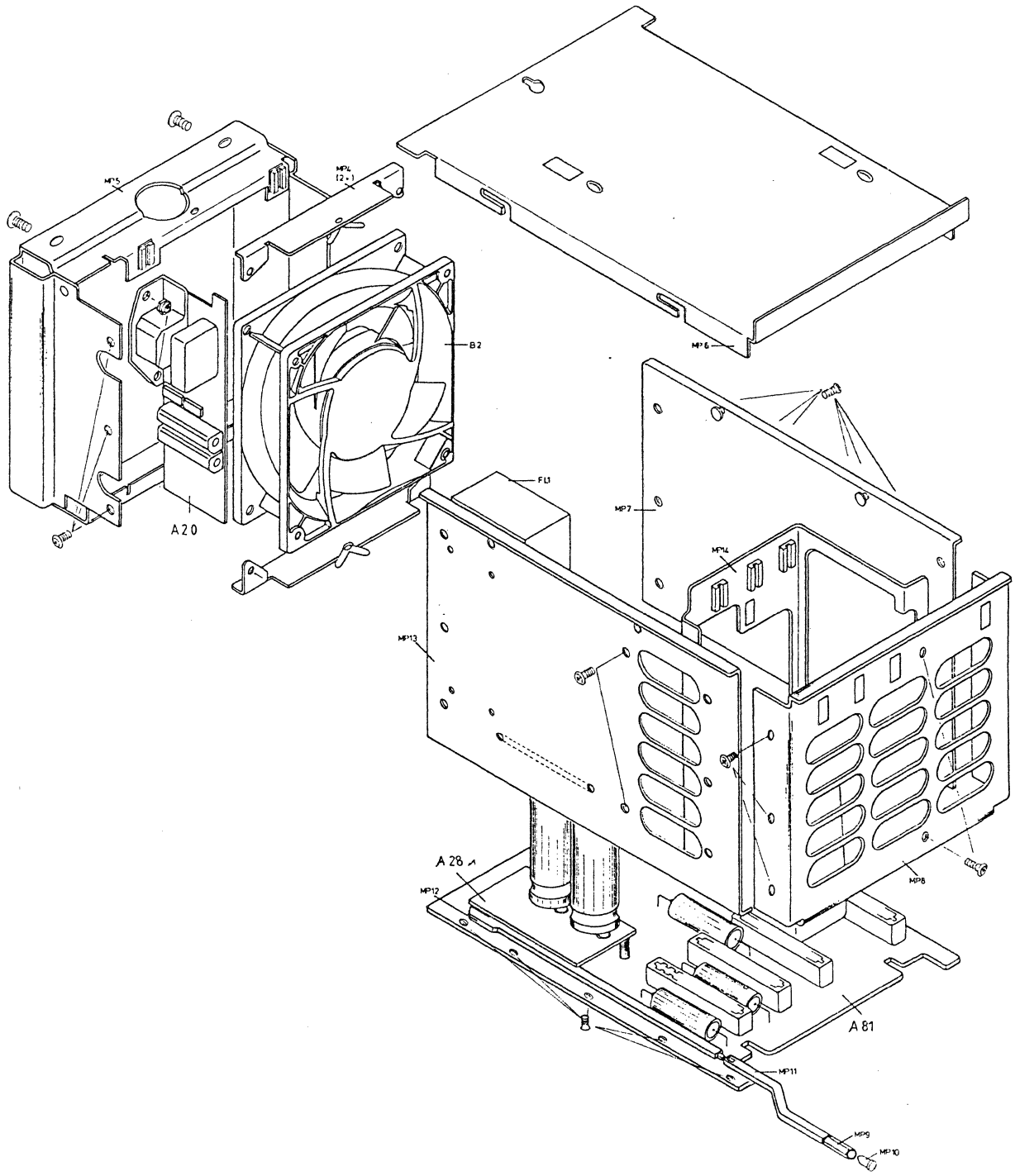


Figure 2-11. A661 Power Supply

Display Module Assembly Parts List of the HP8182B

Reference Designator	HP Part Number	Description	BD NO.
A672	08182-62672	MDL AY DISPLY	
A17	08180-66517	BD AY KEY	
A30	08180-66530	BD AY CNTL	
A32	08180-66532	BD AY DFL VRT	
A34	08180-66534	BD AY DFL HORZ	
MP15	08180-04110	COVER TOP CRT	
MP16	08180-64701	MODULE CRT	
MP17	08180-01203	CLAMP CRT	
MP18	5021-0508	PANEL FRONT	
MP19	08182-00201	PANEL KEYBD	
MP20	4040-2097	FACEPLATE SAFET	
MP21	1400-0678	CLAMP	
MP30	5021-0519	FRM FRNT	
MP47	5040-7202	TRIM STRIP TOP	
MP48	5001-0440	TRIM STRIP SIDE	
MP50	9140-0726	DEFLECTION YOKE	
MP53	2140-0352	LAMP INCD TI18V	
MP54	08180-47401	KEY CUP	
V1	2090-0706	CRT	
W21	08180-61639	CBL AY CRT	
W30	5180-2413	CBL RBN 230 MM	

Keyboard Assembly Parts List of the HP8182B

Reference Designator	HP Part Number	Description	BD NO.
A17	08180-66517	BD AY KEY	
MP70	5041-0846	KNOB NOM 0	
MP71	5041-0847	KNOB NOM 1	
MP72	5041-0848	KNOB NOM 2	
MP73	5041-0849	KNOB NOM 3	
MP74	5041-0850	KNOB NOM 4	
MP75	5041-0851	KNOB NOM 5	
MP76	5041-0852	KNOB NOM 6	
MP77	5041-0853	KNOB NOM 7	
MP78	5041-0854	KNOB NOM 8	
MP79	5041-0855	KNOB NOM 9	
MP80	5041-2756	KNOB A	
MP81	5041-2757	KNOB B	
MP82	5041-2758	KNOB C	
MP83	5041-2759	KNOB D	
MP84	5041-2760	KNOB E	
MP85	5041-2761	KNOB F	
MP86	5041-2763	KNOB +/-	
MP87	5041-0841	KEY CUP	
MP88	5041-0409	KNOB NOM BLK	
MP89	5041-2765	KNOB RUN	
MP90	5041-2755	KNOB STOP	
MP91	5041-2762	KNOB X	
MP92	5041-2768	KNOB SAMPLE	
S1/33	5060-9436	SW P-BTN SINGLE	

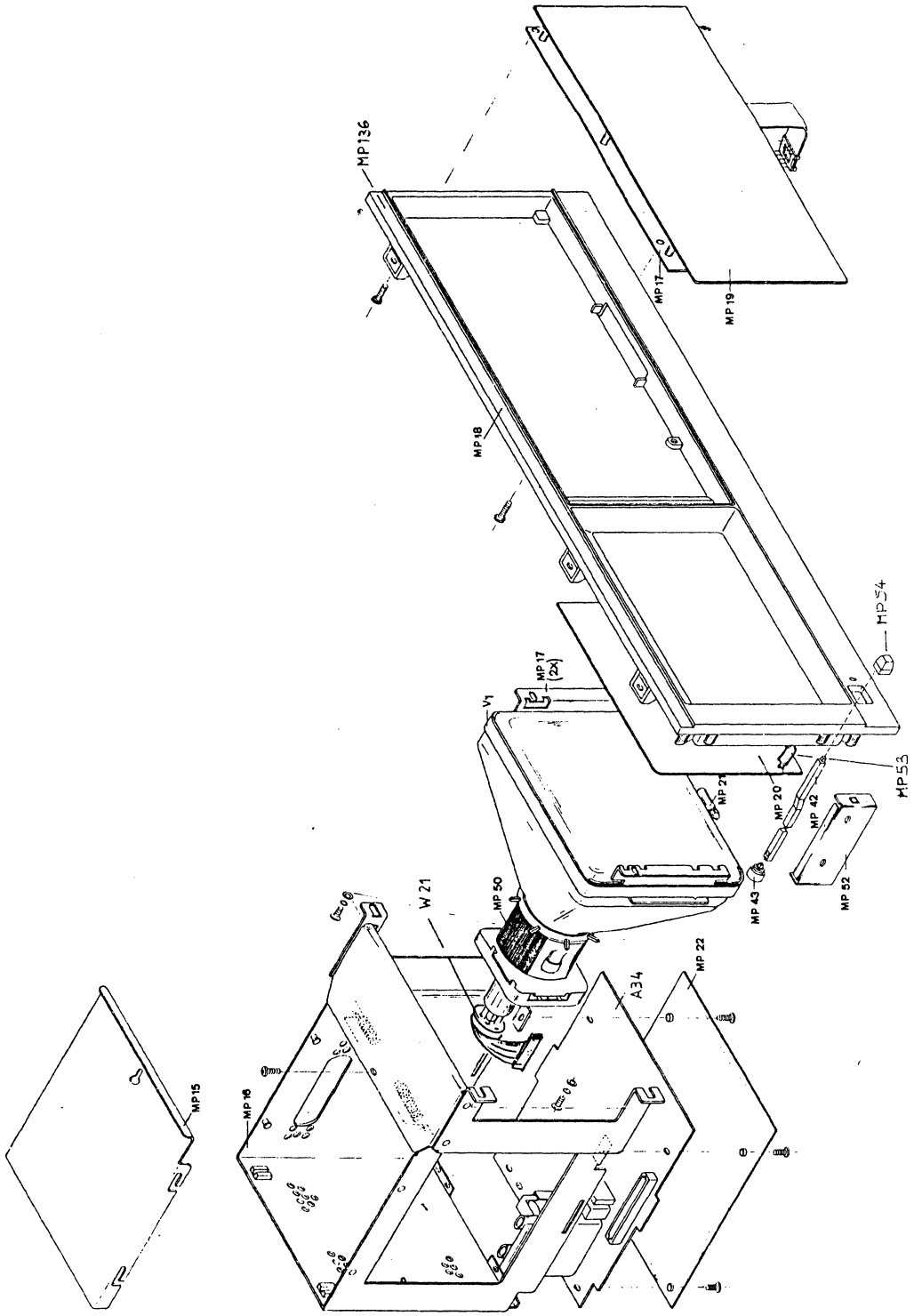


Figure 2-12. A672 Display Module

Rear Panel Assembly Parts List of the HP8182B

Reference Designator	HP Part Number	Description	BD NO.
A663	08182-62663	PNL AY REAR	
A8	08182-66508	BD AY HP-IB	
B1	3160-0510	FAN - DC	
MP1	08182-00265	PANEL REAR	
MP4	08180-01205	BRACKET FAN	
MP135	1251-0218	CONN DS POST	
W10	08182-61619	CBL AY SHLD VID	
W11	08182-61605	CBL AY CLOCK	
W12	08182-61601	CBL AY TWIN	
W14	08182-61606	CBL AY DATA	

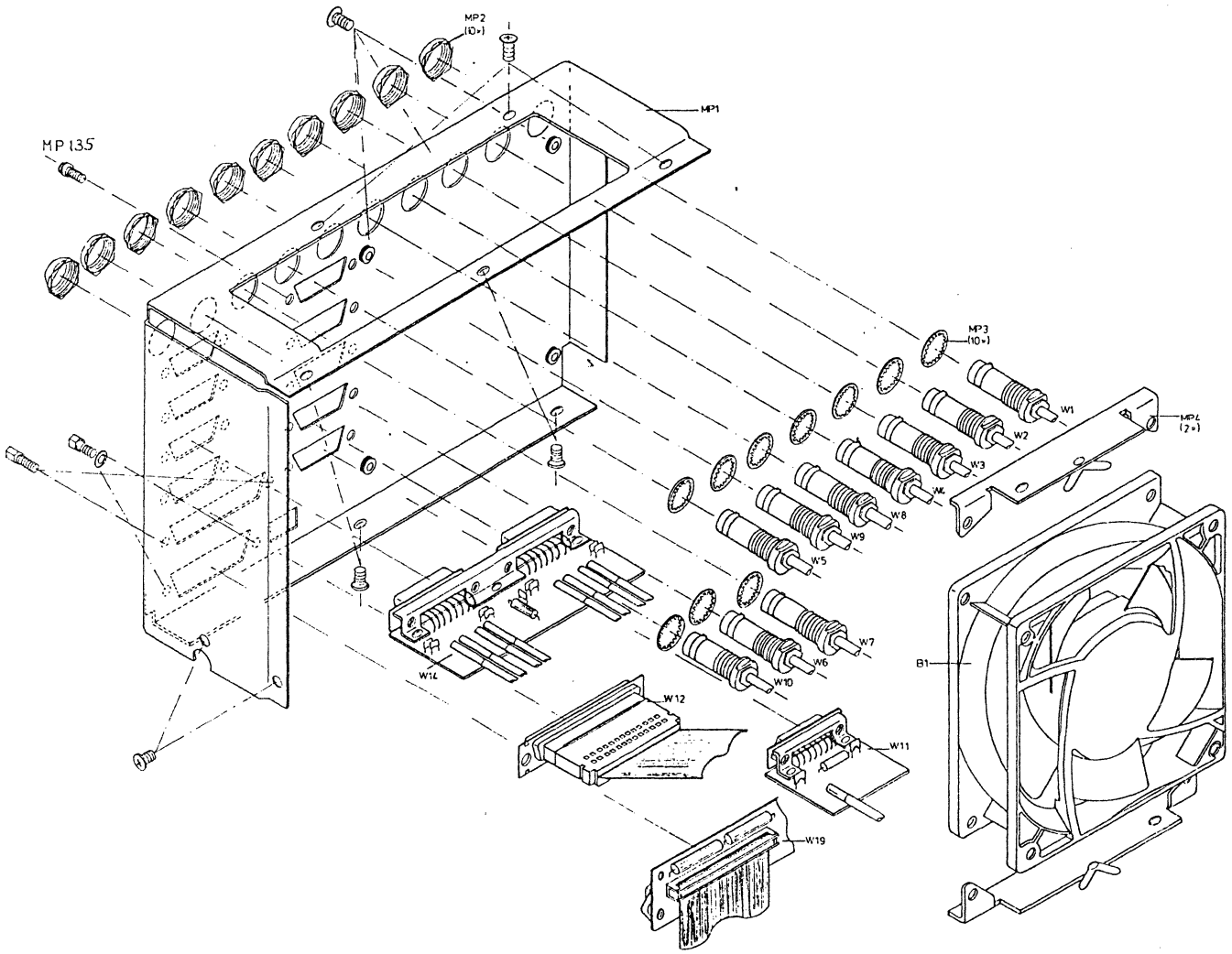


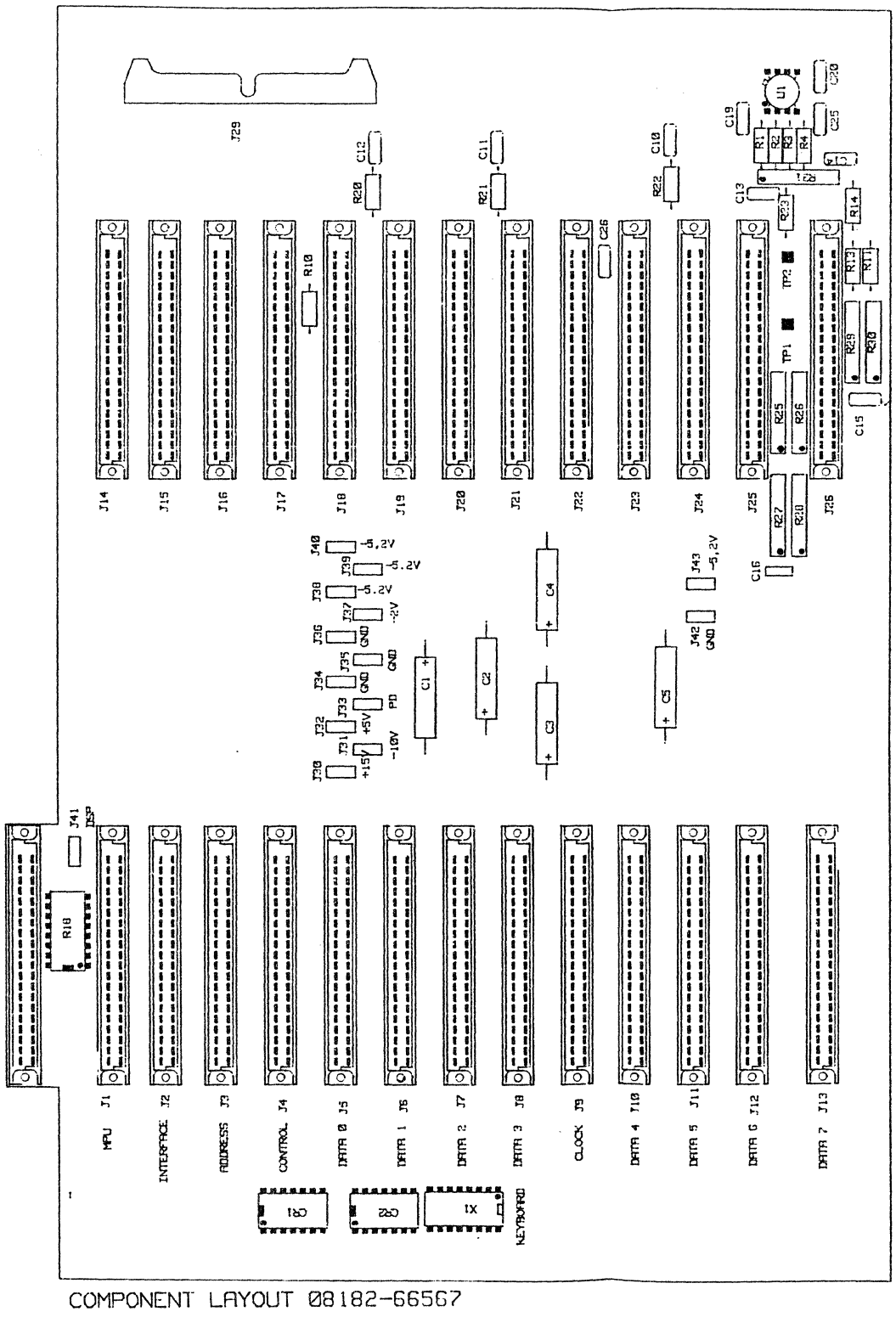
Figure 2-13. Rear Panel Assy

This is a replaceable parts list on a sub-assembly level

Reference Designator	HP Part Number	Description	BD NO.
A61	08182-66561	BD AY U PRCR	
BT100	1420-0251	BATTERY NICAD	A61
MP1	4040-0749	PC EXTR BD BRN	A61
MP2	4040-0748	PC EXTR BD POLY	A61
A62	08182-66562	BD AY INTFC	
J3	1251-4267	CONNECTOR POST	A62
J3A	1250-1737	CC AXIAL TEST P	A62
MP3	4040-0750	PC EXTR BD RED	A62
MP2	4040-0748	PC EXTR BD POLY	A62
A63	08182-66563	BD AY ADDRESS	
DL110	1810-0616	DEL LINE 14 PI	A63
DL111	1810-0616	DEL LINE 14 PI	A63
J3/4	1250-1737	CC AXIAL TEST P	A63
MP1	4040-0751	PC EXTR BD ORN	A63
MP2	4040-0748	PC EXTR BD POLY	A63
A64	08182-66564	BD AY CNTL	
DL101	1810-0616	DELAY LINE 14 PI	A64
DL103	1810-0616	DELAY LINE 14 PI	A64
DL104	1810-0616	DELAY LINE 14 PI	A64
DL201	1810-0616	DELAY LINE 14 PI	A64
J3/J8	1250-1737	CC AXIAL TEST P	A64
MP1	4040-0752	PC EXTR BD YEL	A64
MP2	4040-0748	PC EXTR BD POLY	A64
A65	08182-66565	BD AY DATA	
DL107	1810-0616	DELAY LINE 14 PI	A65
DL207	1810-0616	DELAY LINE 14 PI	A65
DL307	1810-0616	DELAY LINE 14 PI	A65
DL407	1810-0616	DELAY LINE 14 PI	A65

This is a replaceable parts list on a sub-assembly level

Reference Designator	HP Part Number	Description	BD NO.
MP1	4040-0753	PC EXTR BD GRN	A65
MP2	4040-0748	PC EXTR BD POLY	A65
A6	08182-66506	BD AY CLOCK	
J301	1251-4267	CONNECTOR POST	A6
J601	1251-4267	CONNECTOR POST	A6
MP1	4040-0754	PC EXTR BD BLA	A6
MP2	4040-0748	PC EXTR BD POLY	A6
A67	08182-66567	BD AY MOTHER	
J1/J26	1251-1365	CONN PC 44 CONT	A67
J27	1251-8828	CONN POST 40CON	A67
J29	1251-8980	CONN POST TP HD	A67
J30/J43	1251-7871	CONN ICONT R AN	A67



COMPONENT LAYOUT 08182-66567

Figure 2-14. A67 Motherboard

2-5 Exchange Boards Parts Lists

Exchange Boards for the HP 8180B

EXCHANGE PART NO.	PARENT PART NO.	DESCRIPTION	CAN ALSO BE USED IN THE 8180A
08180-69561	08180-66561	BD AY U PROC	NO
08180-69562	08180-66562	BD AY GEN MDL	NO
08180-69563	08180-66563	BD AY ADDRESS	NO
08180-69564	08180-66564	BD AY SYNC	YES
08180-69565	08180-66565	BD AY TIMING	YES
08180-69566	08180-66566	BD AY MODULE	NO
08180-69568	08180-66568	BD AY ADR CTL II	NO
	08180-66515	BD AY KEY	YES
	08180-66524	BD AY FILTER	YES
	08180-66526	BD AY REG	YES
	08180-66528	BD AY CAPACITOR	YES
	08180-66530	BD AY CNTL	YES
	08180-66532	BD AY DEFL VERT	YES
	08180-66534	BD AY DEFL HORZ	YES
	08180-66540	BD AY HP-IB	YES
	08180-66572	BD AY MOTHER	NO
	08180-66576	BD AY TEMP CTRL	YES
	08180-66581	BD AY MOTHER PS	YES
08180-69582	08180-66582	BD AY RECT	YES
08180-69583	08180-66583	BD AY SWITCH	YES
	08180-66585	BD AY REG	YES
	08180-66587	BD AY REG	YES

Exchange Boards for the HP 8181B

EXCHANGE PART NO.	PARENT PART NO.	DESCRIPTION	CAN ALSO BE USED IN THE 8181A
	08181-66561	BD AY MULTIPL.	NO
08180-69562	08180-66562	BD AY GEN MDL	NO
08180-69566	08180-66566	BD AY MODULE	NO
08181-69568	08181-66568	BD AY ADR CTL3	NO
	08180-66524	BD AY FILTER	YES
	08180-66526	BD AY REG	YES
	08180-66528	BD AY CAPACITOR	YES
	08181-66572	BD AY MOTHER	NO
	08180-66576	BD AY TEMP CTRL	YES
	08180-66581	BD AY MOTHER PS	YES
08180-69582	08180-66582	BD AY RECT	YES
08180-69583	08180-66583	BD AY SWITCH	YES
	08180-66585	BD AY REG	YES
	08180-66587	BD AY REG	YES

Exchange Boards for the HP 8182B

EXCHANGE PART NO.	PARENT PART NO.	DESCRIPTION	CAN ALSO BE USED IN THE 8182A
08182-69561	08182-66561	BD AY U PROC	NO
08182-69562	08182-66562	BD AY INTFC	NO
08182-69563	08182-66563	BD AY ADDRESS	NO
08182-69564	08182-66564	BD AY CNTL	NO
08182-69565	08182-66565	BD AY DATA	NO
08182-69506	08182-66506	BD AY CLOCK	YES
	08182-66508	BD AY HP-IB	YES
	08182-66517	BD AY KEY	YES
	08180-66524	BD AY FILTER	YES
	08182-66524	BD AY REG	YES
	08182-66525	BD AY INDUCT.	YES
	08182-66526	BD AY REG	YES
	08180-66528	BD AY CAPACITOR	YES
	08180-66530	BD AY CNTL	TES
	08180-66532	BD AY DEFL VERT	YES
	08180-66534	BD AY DEFL HORZ	YES
	08182-66567	BD AY MOTHER	NO
	08182-66581	BD AY MOTHER PS	YES
08182-69582	08182-66582	BD AY RECT	YES
08182-69583	08182-66583	BD AY SWITCH	YES

Chapter 3
8180A/B Adjustment Procedures

3-1 Introduction

This chapter covers the adjustments procedures necessary for the HP 8180A and 8180B generators.

When performing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

3-2 Power Supply Adjustment 8180B

Equipment:

Digital Voltmeter, testleads HP3456A

WARNING

High voltage is present when performing this adjustment.

NOTE

These adjustments must be done with all PC-Boards inserted. When retrofitting options, first install all new boards, adjust the power supply and then continue with the other adjustments.

1. Remove cover from power supply.
2. Allow instrument to warm up for 10 minutes.
3. Connect DVM to TP4 on the A85 board and adjust A83 R323 to -6.1V reading.

Output voltage adjustment of the -5.2V post regulator

NOTE

If two timing boards are installed, remove right hand cover, connect DVM to the upper lead of A65 C520.

5. Adjust A85 R520 to -5.2V reading.

CAUTION

Base current and storage time adjustment of switching transistor Q304 are optimized in the factory. Therefore, never try to adjust A83 R360 and A83 R32.

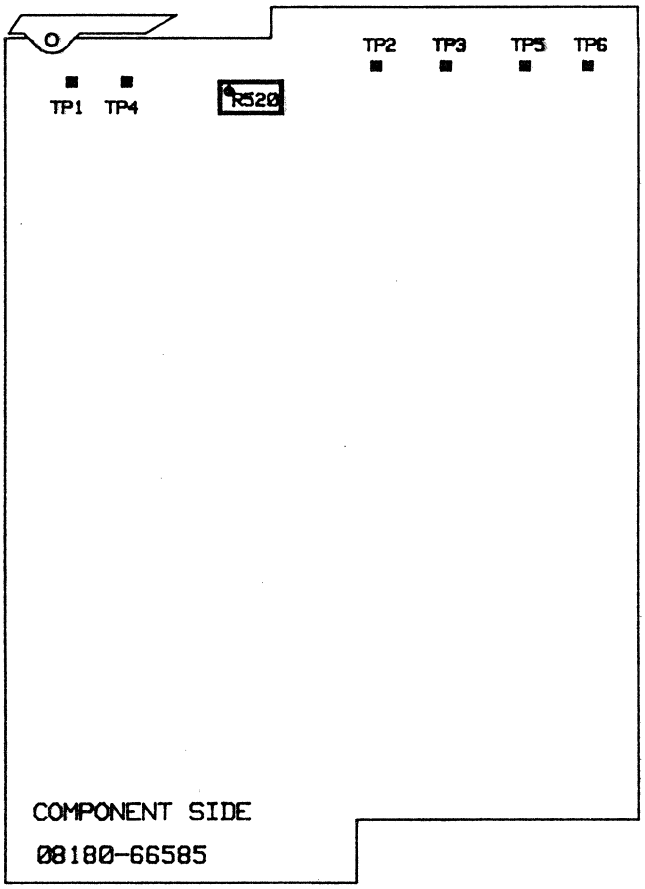


Figure 3-1. A85 Post Regulator Board

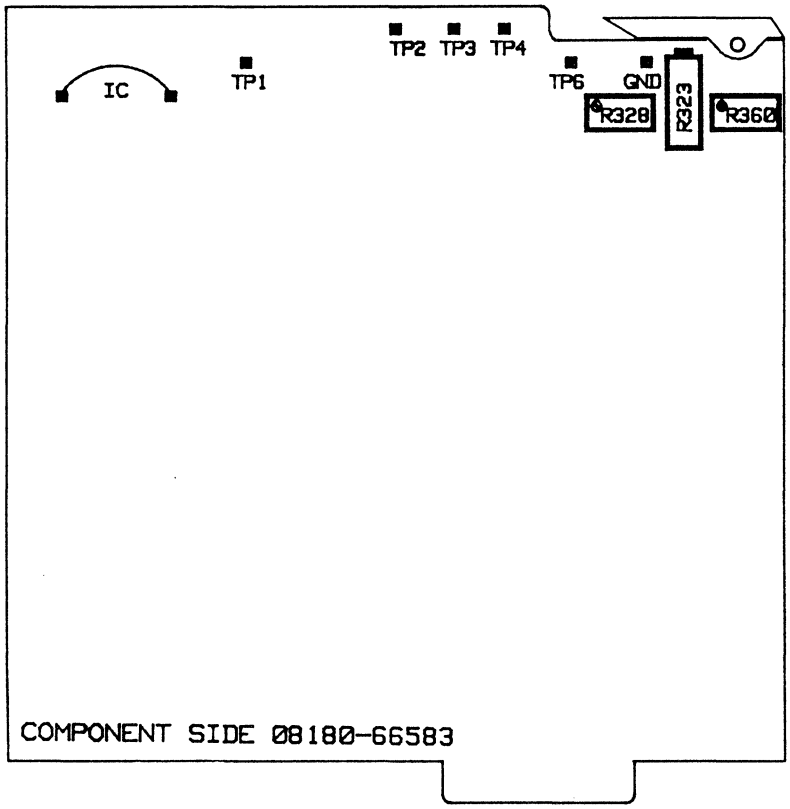


Figure 3-2 A83 Switching Board

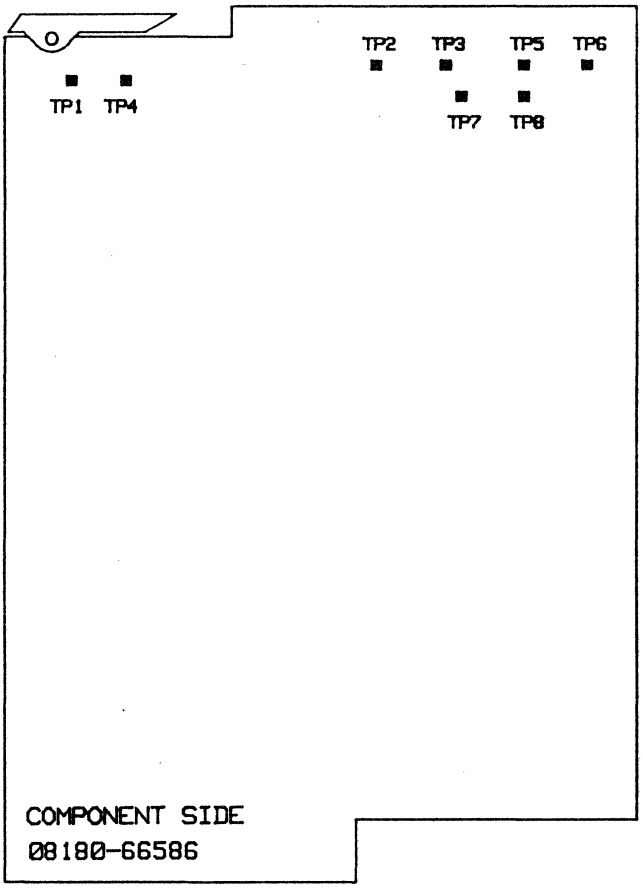


Figure 3-3. A86 Postregulator Board

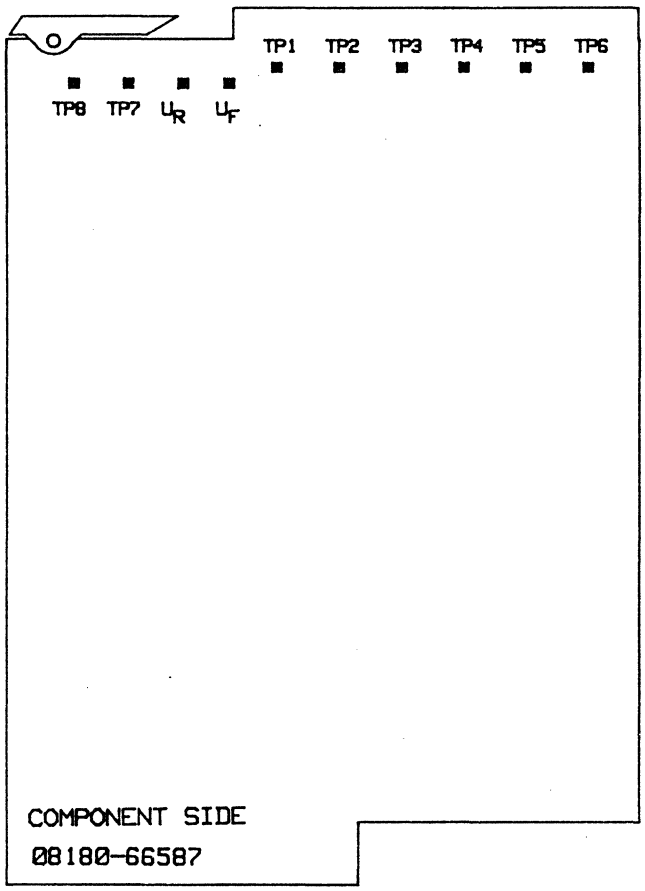


Figure 3-4. A87 Postregulator Board

3-3 Display Control Board 08180-66530

Display Adjustment

If the display has to be completely adjusted (after a CRT change), set A34R3 clockwise and all other potentiometers to mid range. Position the deflection yoke nearest to the screen and fasten it lightly.

1. Set A1S1 to the position as shown in the following figure.

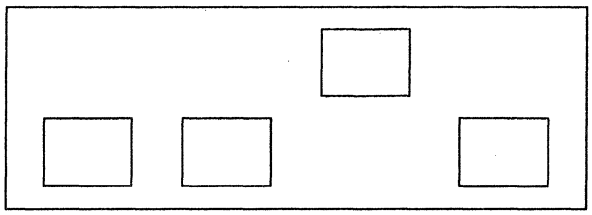


Figure 3-5. Switch 1 Microprocessor Board A1

2. Remove A32J4 (Vertical Deflection Board) and turn the instrument on.
3. If necessary slightly increase the intensity with A32R37.

NOTE

If a bright dot is not visible, set A1S1 to the position as shown in the following figure.

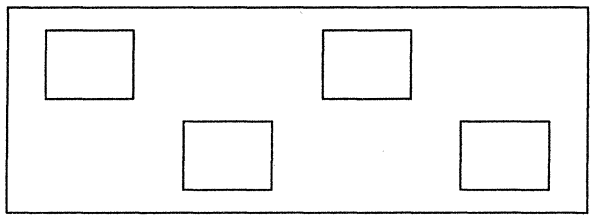


Figure 3-5 continued

4. Using the two ring magnets on the deflection yoke, position the dot approximately 3 mm (1/8 in) above the center of the screen.

NOTE

After ring magnet adjustment set A1S1 to the position as shown in the first figure on this page.

5. Turn the instrument off and reconnect A32J4, press A2S1 and select the test pattern by pressing the left upper softkey (Adjst Display).
6. Adjust A32R21 (Freq.) for a stable display.
7. Center the test pattern with A34R1 (Hor. Pos.) and adjust A34L2 (Hor. Lin.) for maximum horizontal deflection.

8. Adjust A34R3 (Hor. Sync) so that no intensified lines appear.
9. Adjust A34L4 (Hor. Amp.) for approx. 12.5 cm (4 1/2 in) horizontal deflection.
10. Re-adjust A34L2 for best horizontal linearity.
11. Re-centre the test pattern with A34R1 and repeat steps 8 to 10.
12. Adjust A32R27 (Vert. Amp.) for approx. 9 cm (3 1/2 in) vertical deflection.
13. Adjust A32R22 (Vert. Lin.) for best vertical linearity.
14. Re-adjust and fasten the deflection yoke, and repeat steps 2 to 13 if necessary.
15. Correct any 'pin cushion' distortion by adding small correction magnets to the deflection yoke.

Intensity and Focus Adjustment

16. Press A1S1 and select Brightness on the Miscellaneous page: (Pages > Miscellaneous > Brightness > Increase [until maximum brightness is obtained]).
17. Adjust A32R37 (Intens.) until the line flyback is no longer visible.
18. Adjust A32R36 for the best possible focusing.
19. Secure the ring magnets, deflection yoke and correction magnets using silicon compound.

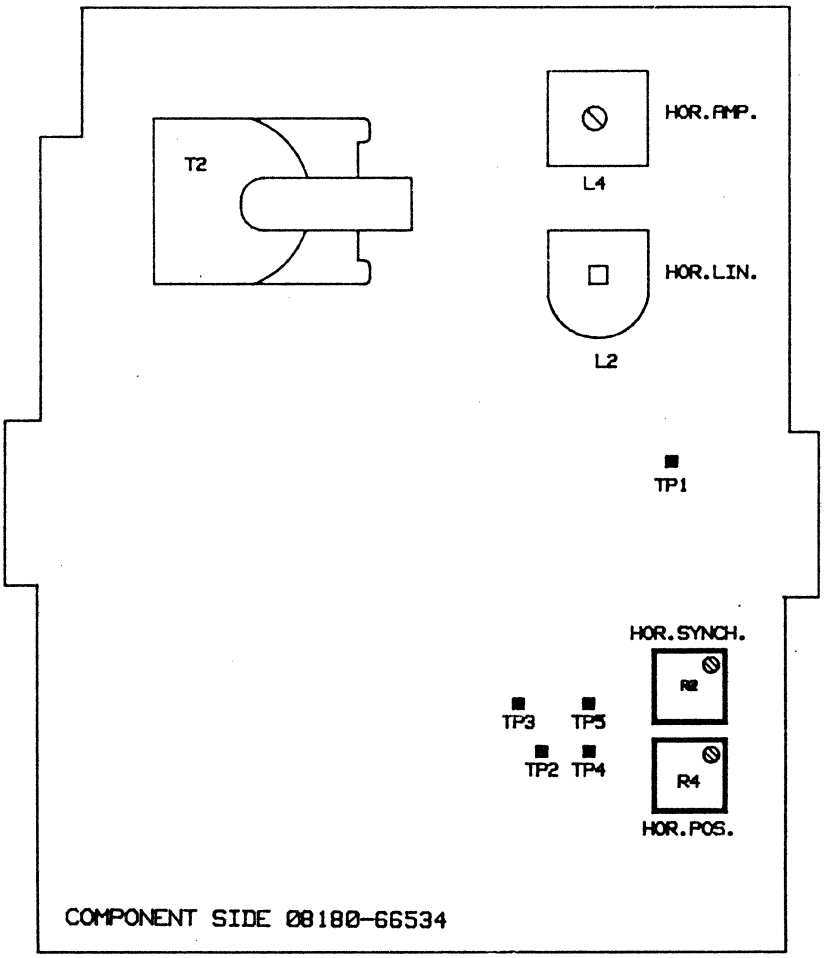


Figure 3-6. High Voltage Board

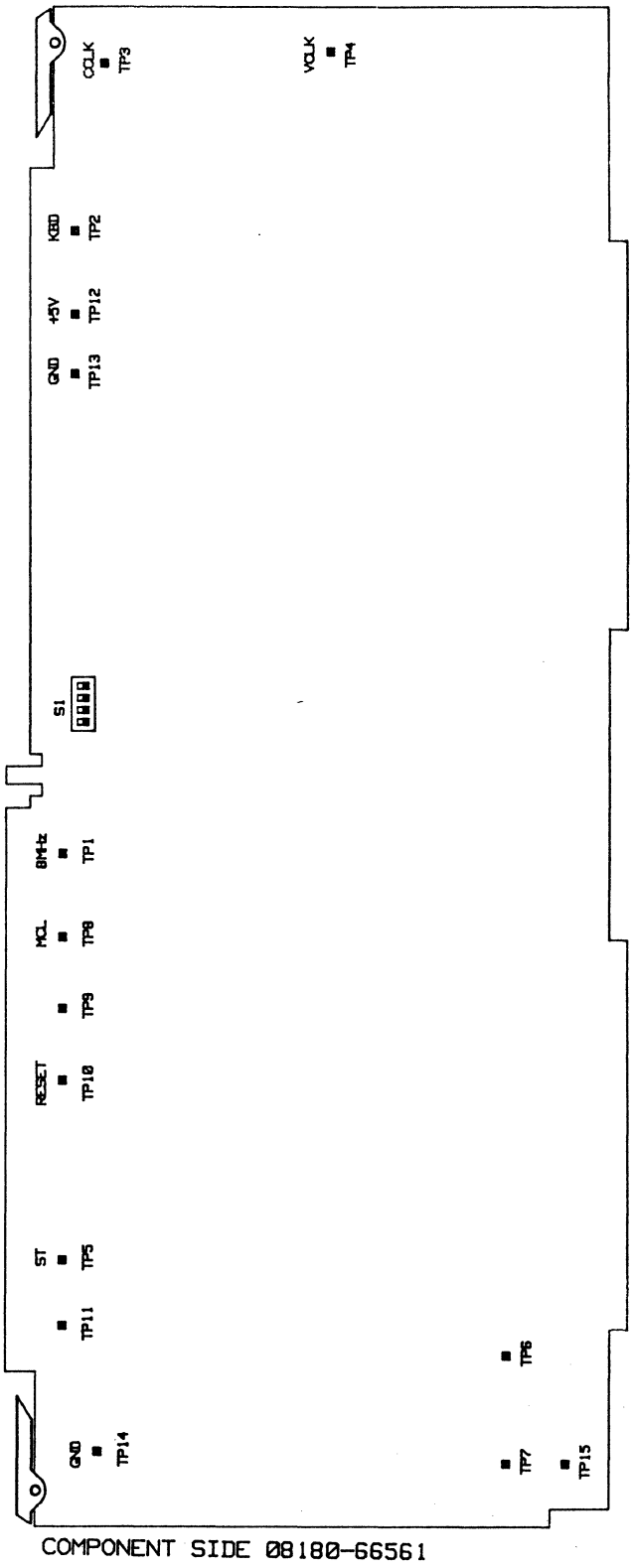


Figure 3-7. A61 Microprocessor Board

3-4 GEM Interface Board 08180-66502 (8180A); 08180-66562 (8180B)

Restart Circuit Adjustment 08180-66502

Equipment:

Oscilloscope with Probe	HP54100D
Digital Voltmeter, testleads	HP3456A
5V Power Supply	HP6624A

1. Remove the A2 Interface Board from the 8180A.
2. Set the power supply output voltage to +4.80V and connect the supply to the +5V and GND TP on the A2 board.
3. Connect the oscilloscope probe to the RES TP and GND TP and adjust A2 R4 so that the RES signal just switches from high to low.
4. Insert A2 and fit board distance holder.

D-A Converter Adjustment 08180-66502

Equipment:

Digital Voltmeter	HP3456A

1. Program 8180A : Standard Set.
   (Pages > Store/Recall > Rcl Std Set > Execute).
2. Label B; Low Level -2V; High Level -1.5V: (Pages > Output > Level > Next Label [B] > Low <-> High [Low] > -2 > Volt > Low <-> High [High] > -1.5 > Volt)
3. Connect DVM to A2 TP5 and the nearest GND TP and adjust A2 R129 for -0.75 Volt ±2mV reading.
4. Set Label B; High Level to +5.5V (5.5 > Volt) and adjust A2 R127 for +2.75 Volt +/- 1mV reading.
5. Set Label B; High Level to 0V (0 > Volt) and readjust A2 R129 to 0.000V +/- 0.5mV reading.
6. Repeat steps 2 to 5 if necessary.
7. Program Label B; High Level +1.00V; Low Level 0.00V: (1 > Volt > Low <-> High [Low] > 0 > Volt).
8. Connect DVM to A2 TP6 and adjust A2 R130 for 0.000V ±0.5mV reading.

DA-Converter Adjustment 08180-66562

Equipment:

Digital Voltmeter	HP3456A

1. Program 8180B : Standard Set.
   (Pages > Store/Recall > Rcl Std Set > Execute).
2. Label B; Low Level -2V; High Level -1.5V: (Pages > Output > Level > Next Label [B] > Low <-> High [Low] > -2 > Volt > Low <-> High [High] > -1.5 > Volt)

3. Connect DVM to A62 TP5 and the nearest GND TP and adjust A62 R129 for -0.75 Volt ±2mV reading.

4. Set Label B; High Level to +5.5V (5.5 > Volt) and adjust A62 R127 for +2.75 Volt +/- 1mV reading.

5. Set Label B; High Level to 0V (0 > Volt) and readjust A62 R129 to 0.000V +/- 0.5mV reading.

6. Repeat steps 2 to 5 if necessary.

7. Program Label B; High Level +1.00V; Low Level 0.00V: (1 > Volt > Low <-> High [Low] > 0 > Volt).

8. Connect DVM to A62 TP 6 and adjust A62 R130 for 0.000V ±0.5mV reading.

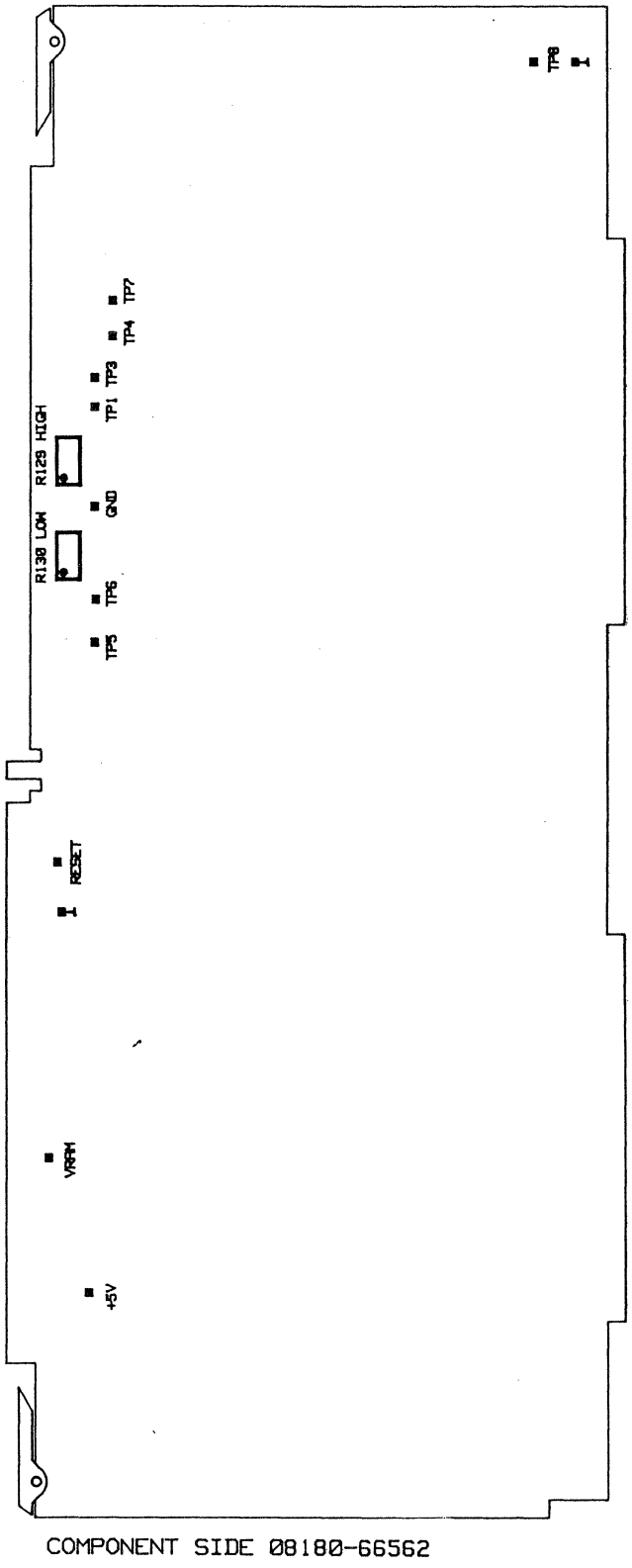


Figure 3-8. A62 Interface Board

3-5 Address Control 1 Board 08180-66503 (8180A); 08180-66563 (8180B)

Equipment:

Universal Counter	5370B
Adjustment Cover	08180-04103
Strobe/Clock Cable Set	15422A
BNC Adapter	15409A

NOTE

Final adjustment must be done with the adjustment cover in place. Close adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes. Refer to Section 1-4, paragraphs 4 and 5.

Measurement setup:

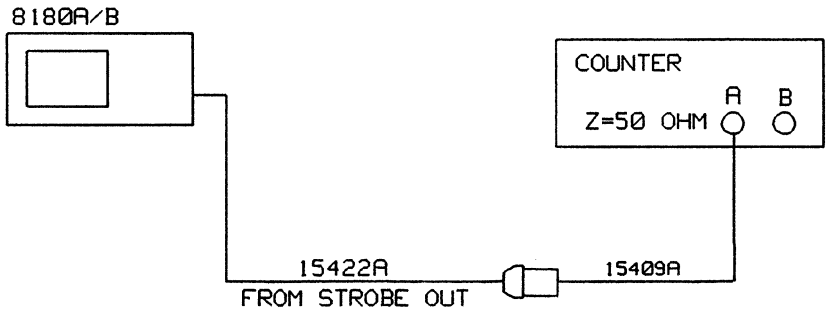


Figure 3-9. Clock Generator Adjustment

Internal Clock Generator Adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
3. Outputs On: (Pages > Output > Outp on/off > On)
4. Frequency 10 MHz: (Pages > Timing > Frequency > 10 > Megahertz)
5. Connect equipment as shown in measurement set up and press RUN.
6. Adjust A3 (A63)R67 for 9.90 MHz.
7. Set 8180A/B to 50 MHz: (50 > Megahertz), and adjust A3 (A63) R75 for 50.50 MHz.
8. Set 8180A/B to 1 MHz: (1 > Megahertz), and adjust A3 (A63) R66 for 0.990 MHz.
9. Set 8180A/B to 9.99 MHz: (9.99 > Megahertz), and adjust A3 (A63) R74 for 9.890 MHz.

Zero Delay of Clock 1 and Clock 2 Adjustment

Equipment:

Scope	54100D
Active Pods	54001A
Extender Board	08180-66551
Extender Board	08180-66557

NOTE

This adjustment is to be done only for the 8180B. Before installing the A3 (A63) and A8 (A68) boards on extenders fit distance holder.

Measurement setup:

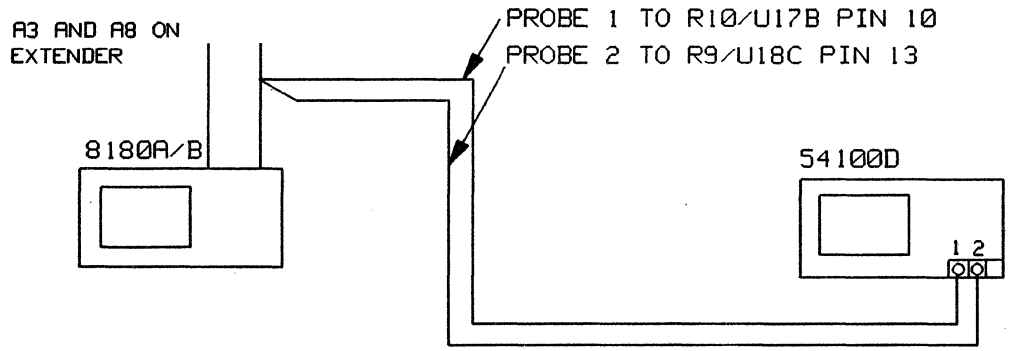


Figure 3-10. Zero Delay - Clk1/Clk2

1. Program 8180B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute).
2. Frequency 10 MHz: (Pages > Timing > Frequency > 10 > Megahertz).
3. Connect equipment as shown in measurement set up and press RUN.
4. Before performing the adjustment cancel out the channel to channel skew of the scope.
5. Set scope to: (Autoscale > Display > Split Screen to Off > Timebase > Sec/Div > 1ns >Trigger > Trigger Source to Chan 1 > Slope to POS).
6. Adjust A63DL3 for 0ns difference between the displayed transitions.

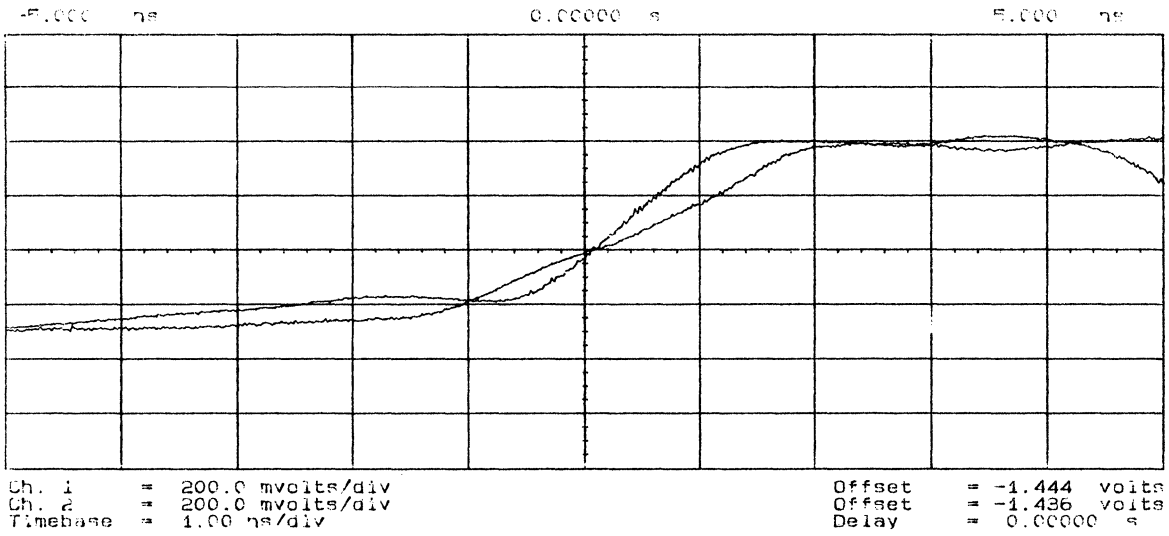


Figure 3-11. Zero Delay

External Inputs, D-A Converter Adjustment

Equipment:

Digital Voltmeter, testleads 3456A

1. Program 8180A/B Input Threshold -10V: (Pages > Control > Inputs > Threshold > -10 > Volt).
2. Connect the DVM to TP1 and GND TP on the A3 (A63) board.
3. Adjust A3 (A63) R51 for 3.33V DVM reading.
4. Set 8180A/B input threshold to +10V(10 > Volt) and adjust A3 (A63) R50 for -3.33V.
5. Set threshold to 0V and check for 0V +/- 3mV.
6. Repeat step 1 to 5 and readjust if necessary.

External Clock Amplifier Adjustment

Equipment:

Pulse Generator	
Digital Voltmeter, testleads	HP 3456A
Extender Board	08180-66551
Scope	HP 54100D
Active Pods	HP 54001A
BNC to BNC cable	

NOTE

Before putting the A3 (A63) board on an extender, fit a board distance holder.

Measurement setup:

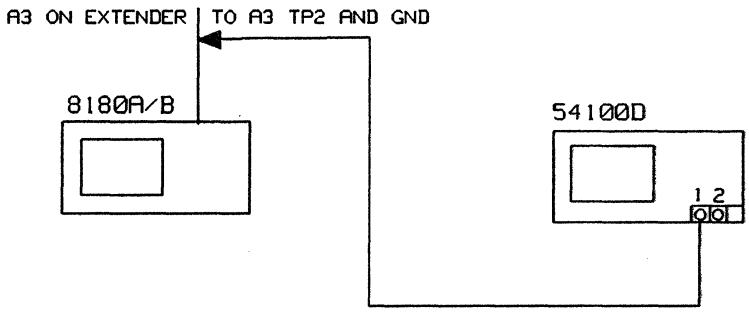


Figure 3-12. External Clock Amp Adjustment

1. Program 8180A/B Input Threshold 0V; Impedance 50 Ohm: External Clock positive transition (Pages > Control > Inputs > Threshold > 0 > Volt > Exit > Impedance > 50Ohm > Ex Clock Source > External[positive slope])
2. Connect DVM to A3 (A63) TP2 and GND TP and adjust A3 (A63) R18 for -15mv ±2mV.
3. Set pulse generator to 10 microsec squarewave and 2 Volt amplitude into 50 Ohm symmetrical about 0 Volt. Transition <5ns.
4. Connect pulse generator to the 8180A/B EXT.CLOCK INPUT
5. Connect scope probe to A3 (A63) TP2 and GND TP and adjust A3 (A63) C12 for best pulse response.

Frequency Error Adjustment

6. Set pulse generator to 51.0 MHz squarewave with 2V amplitude symmetrical about 0 Volt.
7. Adjust A3 (A63) R63 so that the word Clock is flashing in the upper left corner of the 8180A/B display.

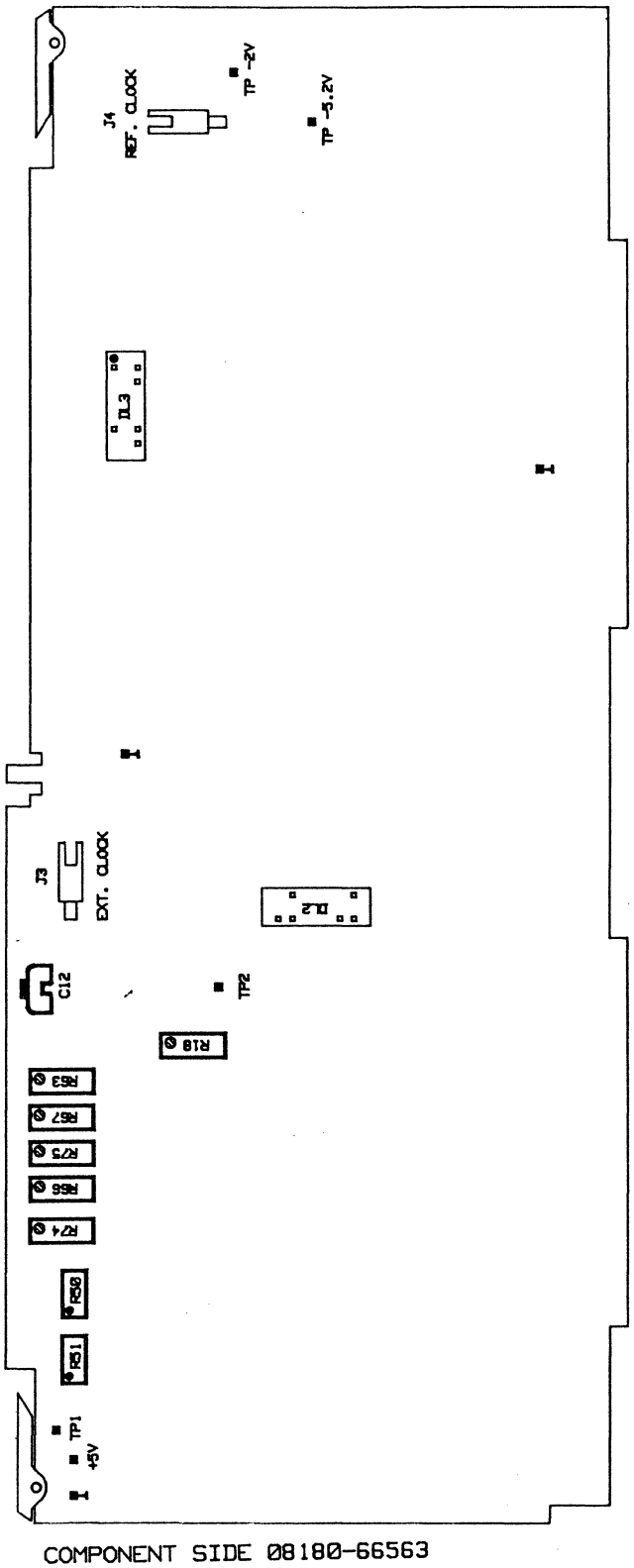


Figure 3-13. A63 ADC1 Board

3-6 Address Control 2 Board 08180-66508 (8180A); 08180-66568 (8180B)

External Break and Stop Amplifier Adjustment

Equipment:

Pulse Generator	
BNC to BNC Cable	
Oscilloscope	HP 54100D
Scope Probe	HP 54001A
Digital Voltmeter, Testleads	HP 3456

1. Program 8180A/B: Input Threshold 0V; Impedance 50 Ohm; Break Input ON (PAGES > Control > Inputs > Threshold > 0 > Volt > Exit > Impedance > 50 Ohm > Exit > Break Input > ON $\overline{b}$ > Exit > Stop Input > ON $\overline{b}$)

2. Set pulse generator to 10 µs (100 kHz) squarewave and 2 V amplitude (into 50 Ohm) symmetrical about 0 V. Transition time < 5 ns.

External Break Amplifier Adjustment

3. Connect DVM to A8 (A68) TP1 and GND TP and adjust A8 (A68) R131 for -15 mV ±2mV.

4. Connect pulse generator to the 8180A/B External Break Input.

5. Connect Oscilloscope probe to A8 (A68) TP1 and GND TP and adjust A8 (A68) C31 for best pulse response.

External Stop Amplifier Adjustment

6. Connect DVM to A8 (A68) TP2 and GND TP and adjust A8 (A68) R112 for -15 mV ±2 mV.

7. Connect pulse generator to the 8180A/B Stop Input.

8. Connect oscilloscope probe to A8 (A68) TP2 and GND TP and adjust A8 (A68) C23 for best pulse response.

Strobe Reference Delay Adjustment

Equipment:

Adjustment cover:	08180-04103 (8180A/B)
Reference delay line A	08180-61636
Reference delay line B	08180-61696
Cable set	15423A
BNC adapter	15409A
BNC adapter female/female	1250-0080
BNC male probe adapter	1250-1454
50 Ohm feedthrough	10100C
Scope	54100D
Active pods	54001A

Measurement setup:

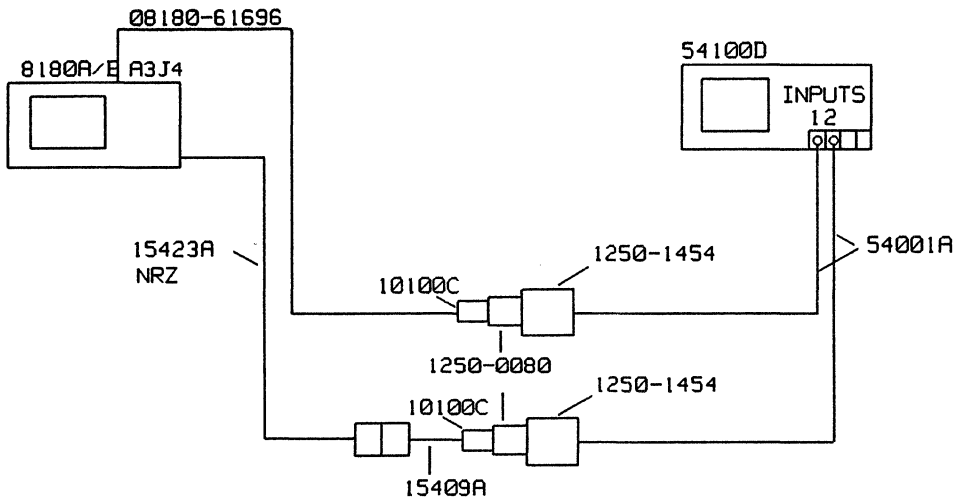


Figure 3-14. Equipment Setup - Strobe Ref Delay

1. Adjust interchannel skew of 54100D to zero.

   Connect scope inputs 1 and 2 to one signal source output via T-connector (20MHz square wave). Press scope front-panel keys in the following sequence:
   Autoscale > More > Cal+Test > Cal Menu > Trigger delay > Trigger delay > press Expand waveform until timebase = 500ps. Turn Knob until second transition crosses the horizontal graticule line at the same place where the first trace crosses the horizontal graticule line.

2. Connect the reference delay line through the hole in the adjustment cover of the 8180A/B to A3 (A63) J4 (Reference clock connector).

3. Adjustment must be done with the adjustment cover in place. Allow the generator to warm up for 30 minutes.

4. Program 8180A/B Standard set: (Pages > Store/Recall > Rcl Std Set > Execute)

5. Set Label A to TTL level, Strobe to TTL level: (Pages > Output > Level > Next Label(A) > TTL levels > Execute > Exit Strobe Level > TTL)

6. Set Strobe Output to Clock; set Last Address to 00001: (Pages > Control > Strobe Output > Clock > Exit > Last Address > 1 > Enter N)

7. Address 0 all bits high; Address 1 all bits low: (Pages > DATA > 1 . . 1 > Cursor(Address 1) > 0 . . 0)

8. Outputs on: (Pages > Output > Outp On/Off > On)

9. Connect equipment as shown in the measurement set up.

10. Press Run.

11. New Scope settings: (Autoscale > More > Trigger > Trigger Mode > Trigger Mode [to Mode "Time-Dly"])

12. Set Trigger conditions to:
After [Neg] Edge > On [Chan 2] > Del [40 ns] Then > Trig On [Pos] Edge > On [Chan 1]

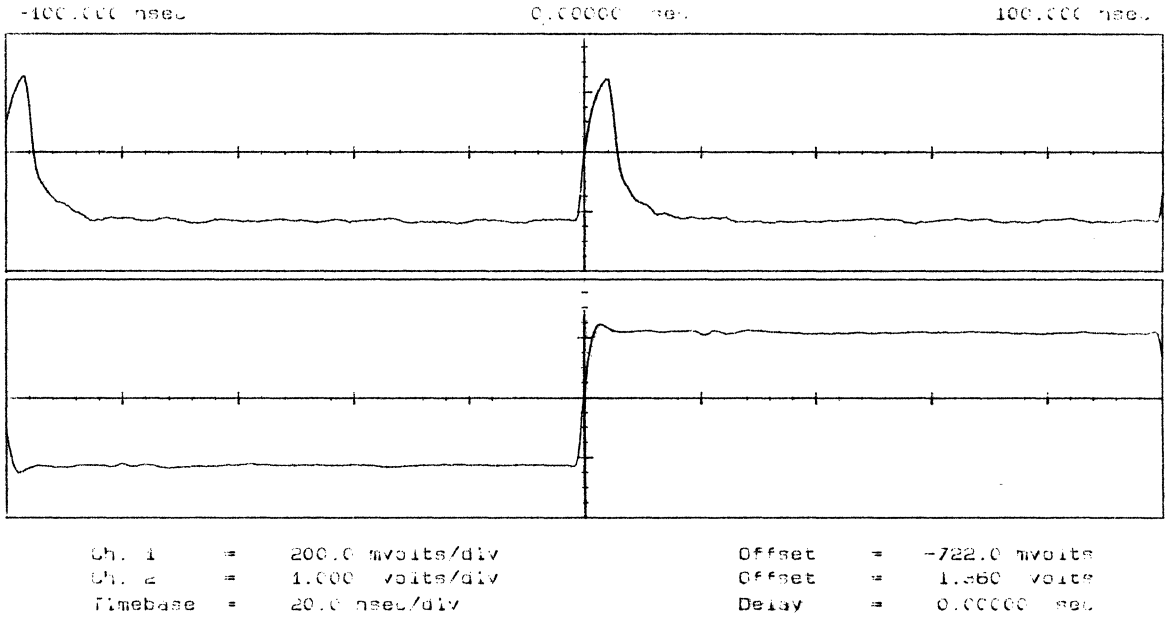


Figure 3-15. Strobe Ref Delay - 1

13. Center reference clock to vertical graticule line (Display > Split Screen > off > Graticule to (Grid) > Timebase to (500ps) > Channel 2 > Channel 2 Display to (Off) > Timebase > Delay) Adjust with Knob the 50% point of the reference clock transition to center graticule line.

14. Switch channel 1 display off, channel 2 display on
(Channel 1 > Channel 1 Display > off
Channel 2 > Channel 2 Display > on)

15. Set Timebase to 500ps (Timebase > Sec/Div > 500ps)

16. Store displayed transition to Memory 1 (More > Wfmsave > Clear Memory 1 > Memory 1 > on > Store to Memory 1.

17. Connect in turn all NRZ channels to Input 2 of 54100D. Store each displayed transition into Memory 1.

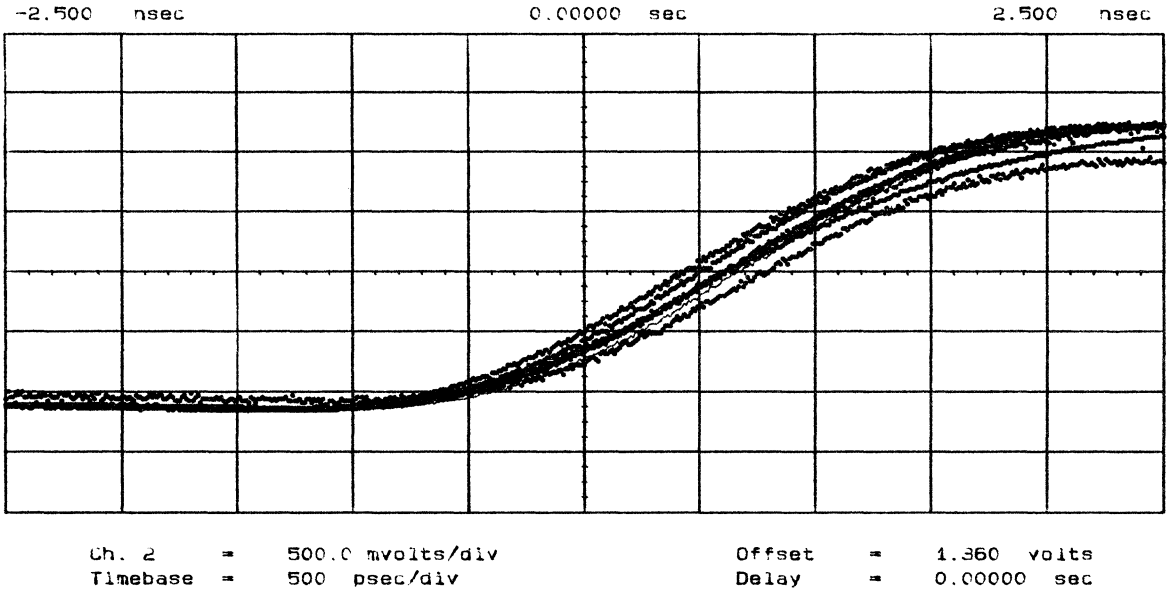


Figure 3-16. Strobe Ref Delay 2

Case 1: Data transitions appear after strobe reference clock.

18. Set Markers (More > Delta t > T Markers > on) Set with Knob the Start Marker to the first transition and the Stop Marker to the last transition of the displayed group.

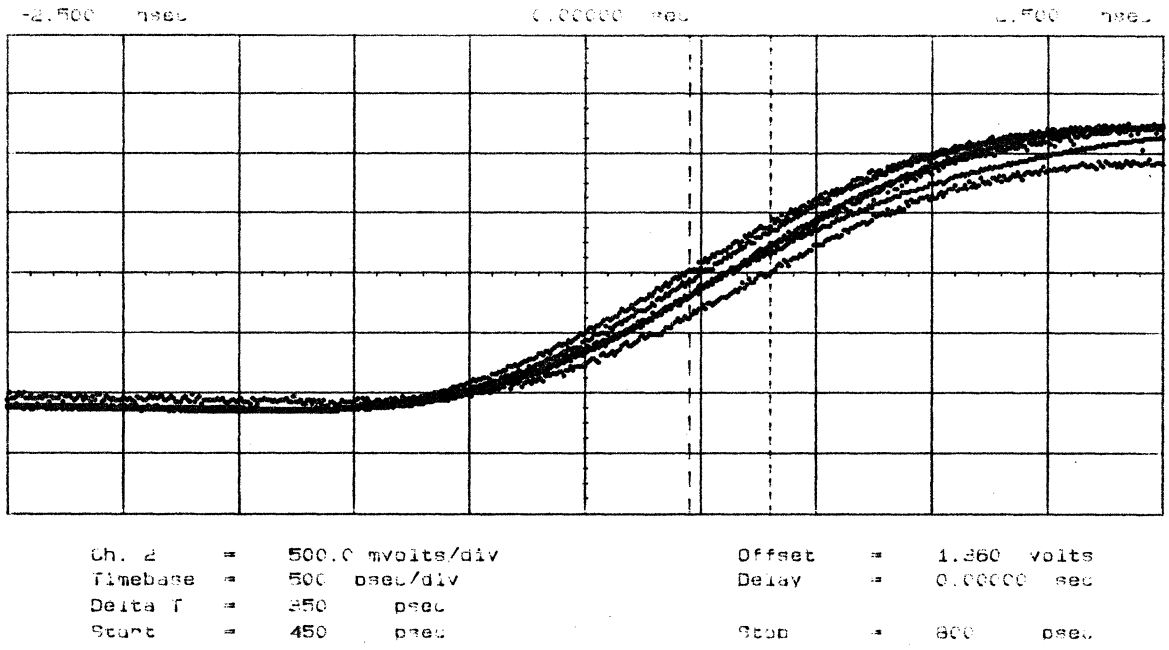


Figure 3-17. Strobe Ref Delay 3

19. Read Delta t.

20. Set Stop Marker to (Delta t)/2 exactly in the middle of the displayed group of transitions. Set Start Marker to center graticule line and read Delta t.

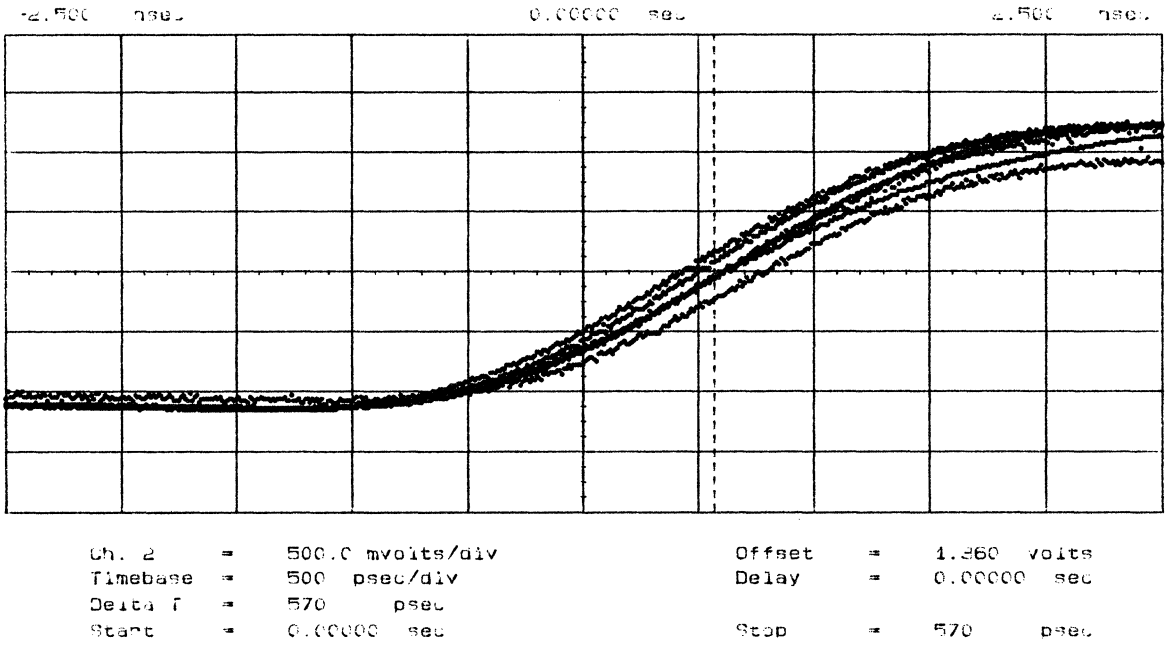


Figure 3-18 Strobe Ref Delay 4

21. Switch Memory 1 off: (More > Wfmsave > Memory 1 > Off)

22. Set Stop Marker to currently displayed transition; Set Start Marker to Delta t: (More > Delta t > Stop Marker > Knob > Start Marker > Knob until Delta t is displayed.)

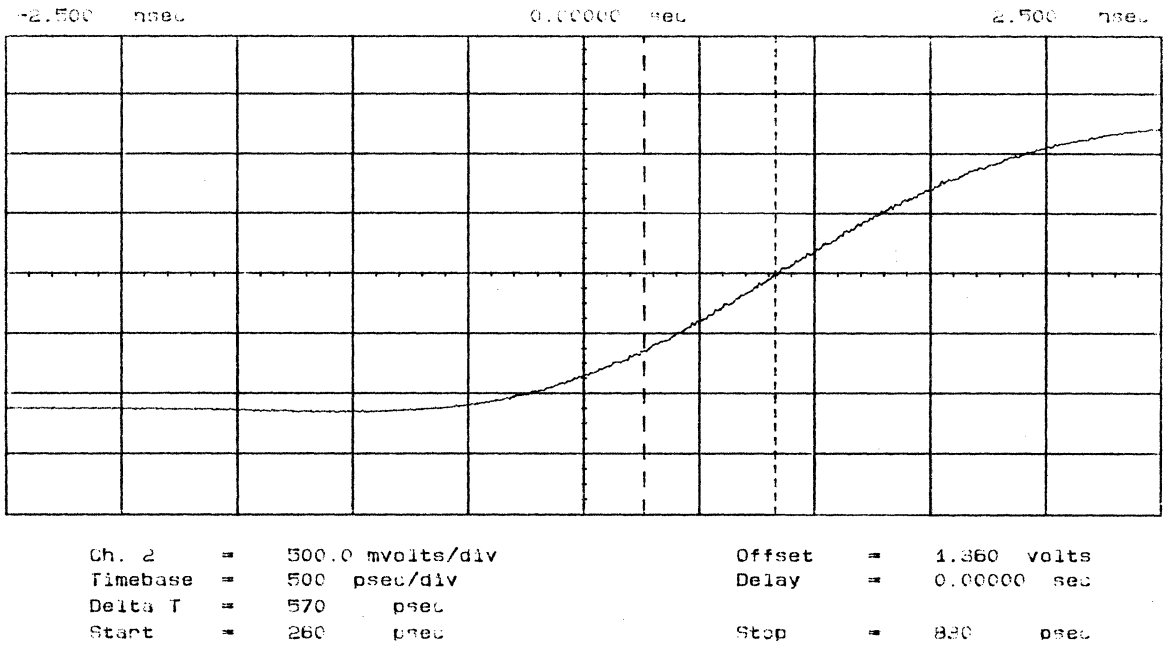


Figure 3-19. Strobe Ref Delay 5

23. Adjust A8 (A68) R64 so that the 50% point of the displayed DATA channel transition meets the Start Marker.

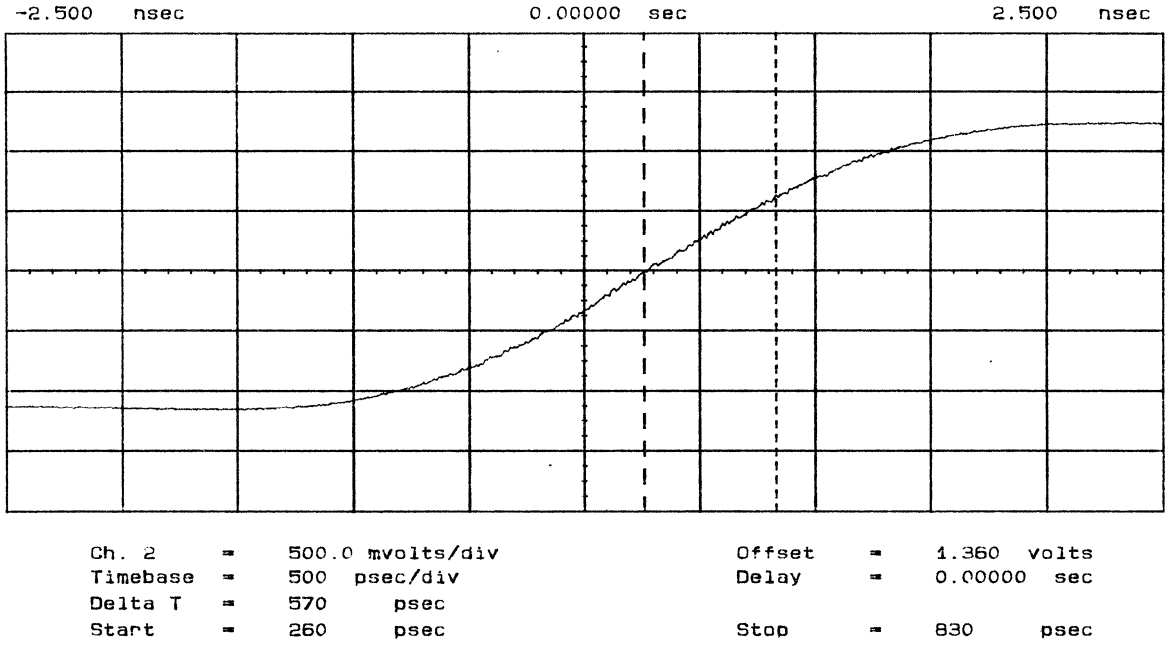


Figure 3-20. Strobe Ref Delay 6

Case 2: Data transitions appear before strobe reference clock.

24. Set Markers (More > Delta t > T Markers > on) Set with Knob the Start Marker to the first transition and the Stop Marker to the last transition of the displayed group.

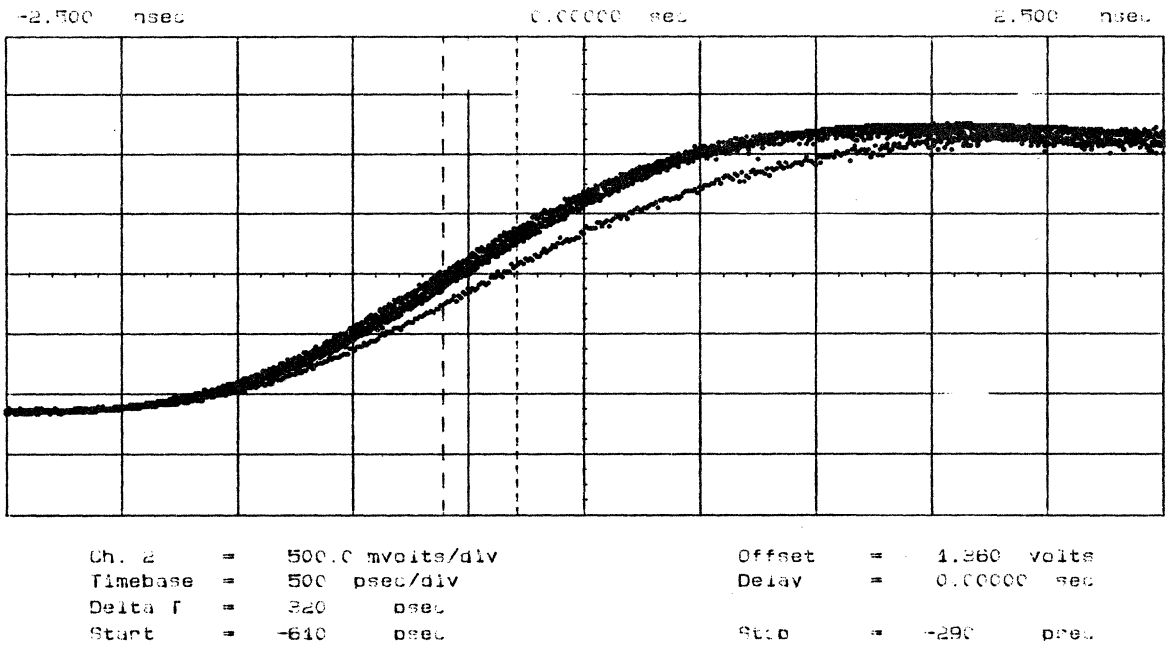


Figure 3-21. Strobe Ref Delay 7

25. Read Delta t.

26. Set Start Marker to (Delta T)/2 exactly in the middle of the displayed group of transitions. Set Stop Marker to center graticule line and read Delta t.

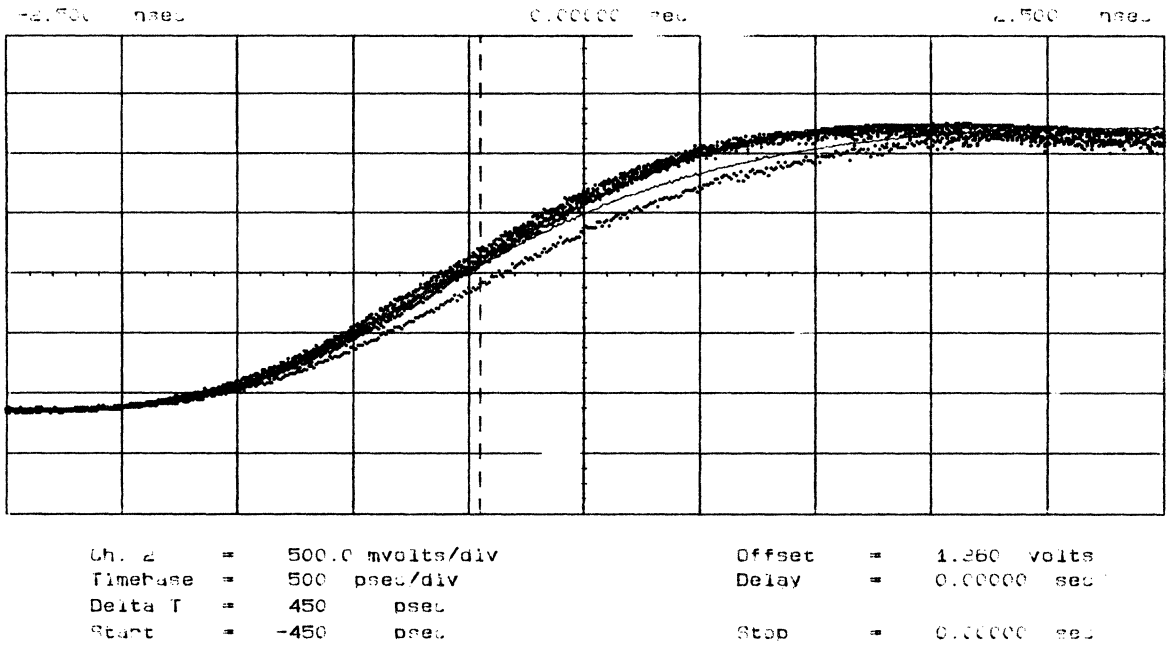


Figure 3-22. Strobe Ref Delay 8

27. Switch Memory 1 Off: (More > Wfmsave > Memory 1 > Off)

28. Set Start Marker to the 50% point of the currently displayed transition; Set Stop Marker to Delta t: (More > Delta t > Start Marker > Knob > Stop Marker > Knob)

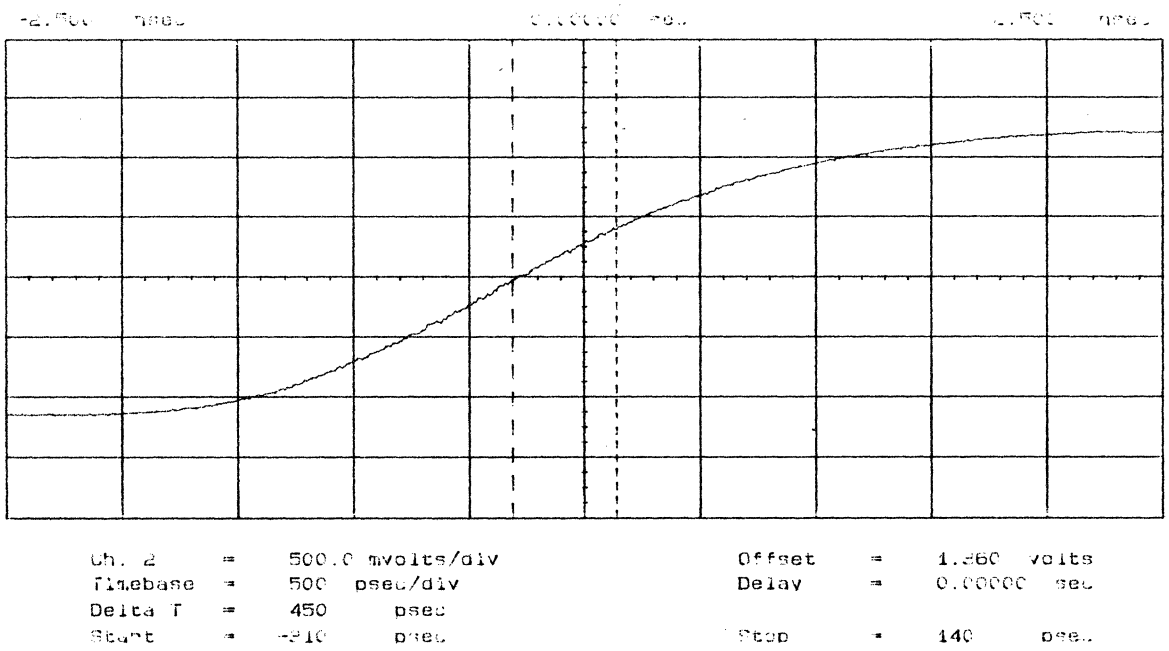


Figure 3-23. Strobe Ref Delay 9

29. Adjust A8 (A68) R64 so that the 50% point of the currently displayed DATA channel transition meets the Stop Marker.

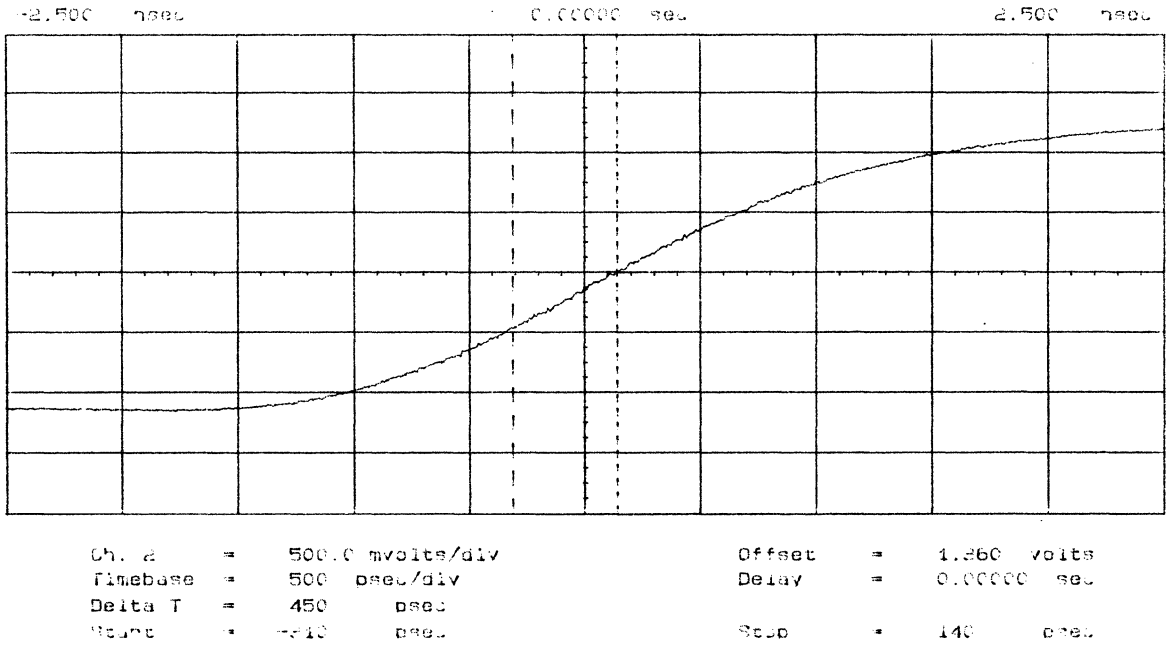


Figure 3-24. Strobe Ref Delay 10

30. Check all NRZ channels. The group of transitions should be symmetrical about the reference clock.

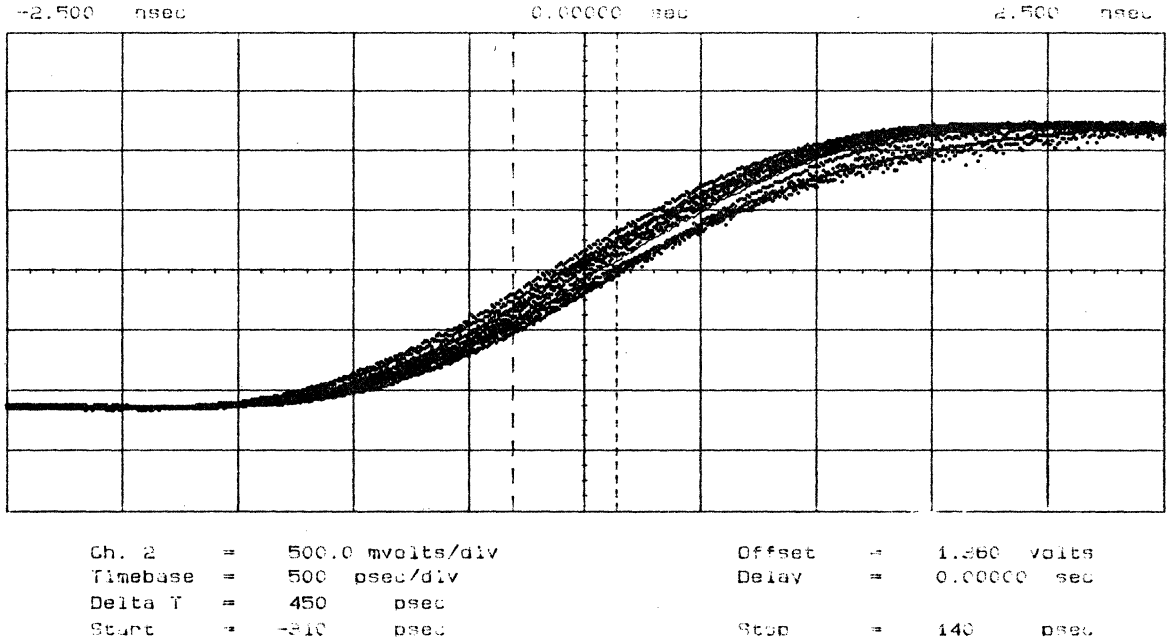


Figure 3-25. Strobe Ref Delay 11

31. Connect the Strobe output to scope channel 2 and adjust A8 (A68) R204 so that the 50% point of the positive going edge of the Strobe signal overlays with the 50% point of the strobe reference transition.

NOTE

The adjustment range of A8 (A68) R204 is approximately 1ns. If it is not possible to adjust for zero delay between Strobe and Strobe reference clock, set A8 (A68) R204 to the middle of the adjustment range and perform a pre-adjustment with A8 (A68) DL8. After the pre-adjustment, center the Strobe transition with A8 (A68) R204 .

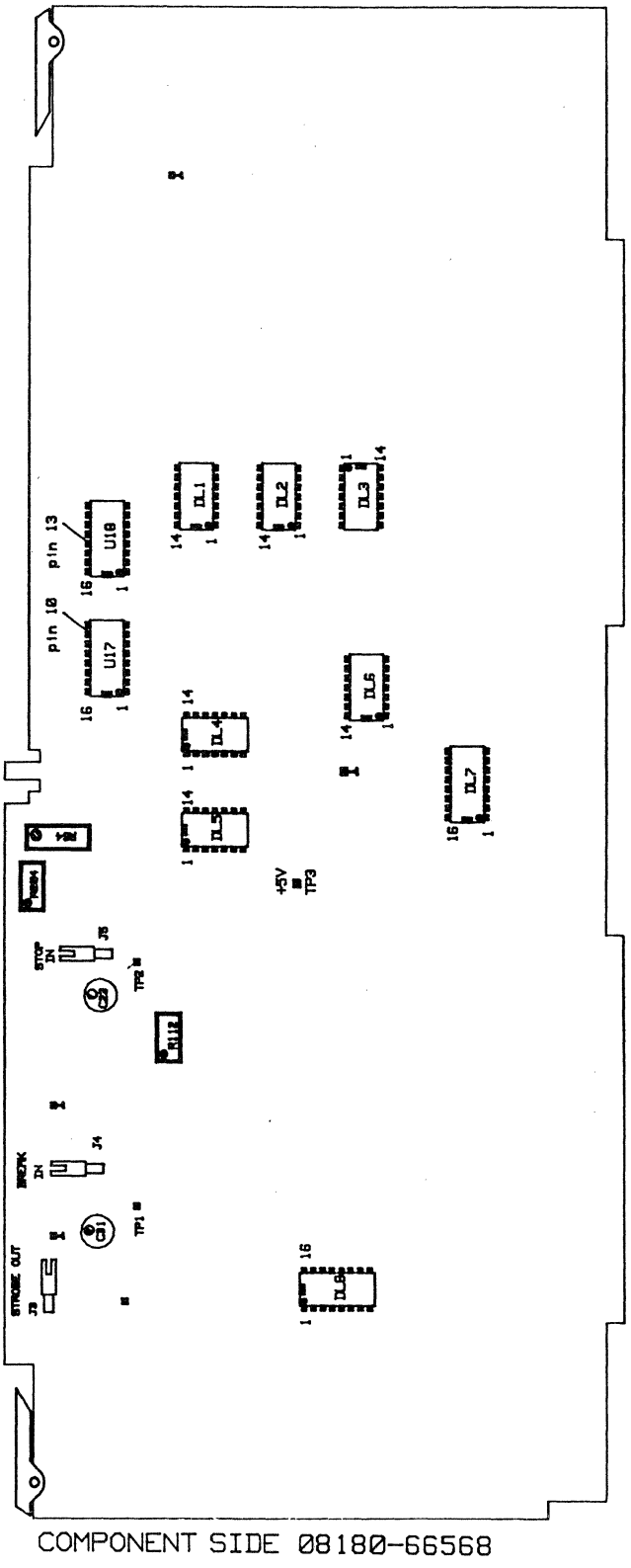


Figure 3-26. A68 Address Control 11

3-7 Module Board 08180-66506 (8180A); 08180-66566 (8180B)

Output Amplifier High/Low Level Adjustment

Equipment:

Digital Voltmeter	HP 3456A
BNC adapter	15409A
BNC (f) dual banana plug	1251-2277
DATA cable set	15423A

High Level Adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Memory Set: (Pages > Data > Edit > Clear & Set > Set Data > Execute)
3. Label A High Level 0V; Low Level -2V: (Pages > Output > Level > Next Label[to Label A] > Low<- > High[to High] > 0 > Volt > Low<- > High[to Low] > -2 > Volt)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. Connect Data channel to be adjusted to DVM. Press RUN. Adjust A6 (A66) A60 R2 for 0V +/-0.5mV DVM reading.

Low Level Adjustment

6. Memory Clear: (Pages > Data > Edit > Clear&Set > Clear Data > Execute)
7. Label A High Level +2V; Low Level 0V: (Pages > Output > Level > Low<- > High[to High] > 2 > Volt > Low<- > High[to L > 0 > Volt)
8. Press RUN and adjust A6 (A66) A60 R1 for 0v ±0.5mV reading.

Data Flatness and Overshoot Adjustment

Equipment:

Scope	54100D
Active pods	54001A
BNC scope probe adapter	1250-1454
BNC adapter female/female	1250-0080
BNC adapter	15409A
Data cable set	15423A
Strobe/Clock cable set	15422A
50 Ohm feedthrough	10100C

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Label A: High Level to +3V, Low Level to -2V: (Pages > Output > Level > Next Label[to Label A] > Low<- > High[to High] > 3 > Volt > Low<- > High[to Low] > -2 > Volt)
3. Frequency 250 Hertz: (Pages > Timing > Frequency > 250 > Hertz)
4. First Address 0; Last Address 1; Strobe Output Clock: (Pages > Control > Last Address > 1 > Enter Number > Exit > Strobe Output > Clock)

5. FAD Data High; LAD Data Low: (Pages > Data > 1 . . . . 1 [until FAD Data is high] 0 . . . . 0 [until LAD Data is Low])

6. Outputs On: (Pages > Output > Outp on/off > On)

7. Press RUN.

8. Connect DATA channel to be measured to scope channel no. 1

9. Set 54100D to Autoscale and Timebase to 1 ms: (Autoscale > Timebase > Sec/Div > 1 > millisec)

10. Adjust A6 (A66) A60 R4 and A6 (A66) A60 R6 for best flatness.

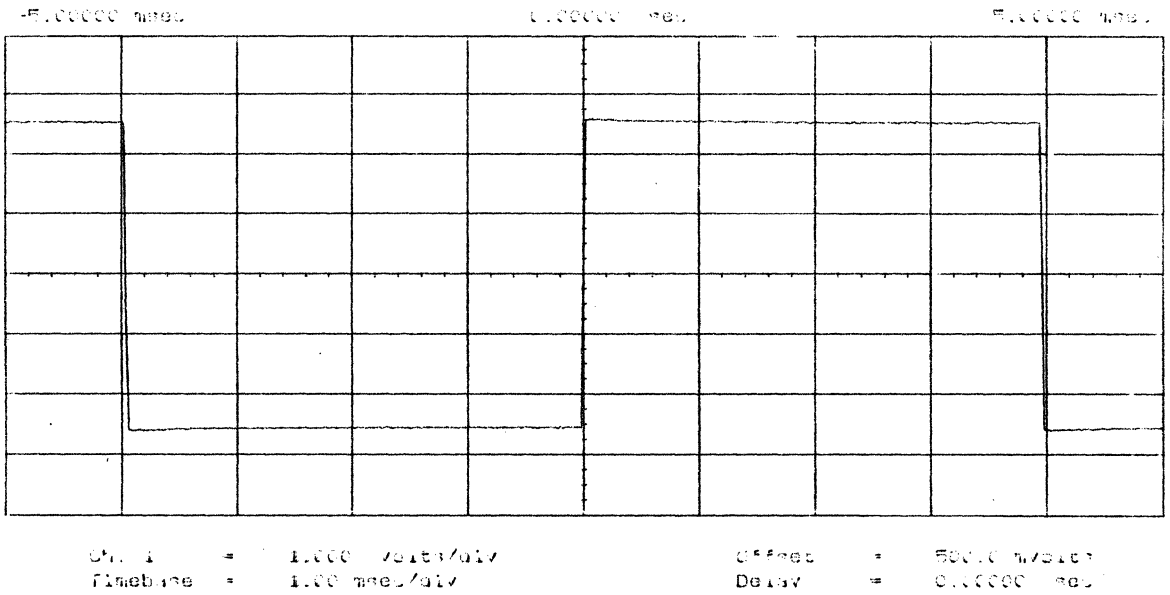


Figure 3-27. Data Flatness Adj

11. Connect 50 Ohm feedthrough to Data channel and adjust A6 (A66) A60 R5 for best flatness.

Overshoot Adjustment Module Board Output Amplifier 8180A

12. Set 8180A Frequency to 10MHz: (Pages > Timing > Frequency > 10 > Megahertz)

13. Label A ECL Levels: (Pages > Output > Level > ECL Levels > Execute)

14. Connect channel to be adjusted to scope input no. 1 and set scope to: (Autoscale > Delta V > Vmarkers- > on > Auto Top-Base > Timebase > 1 > nanosec)

15. Read Delta V and adjust A6 A60 R3 for < 9% of Delta V.

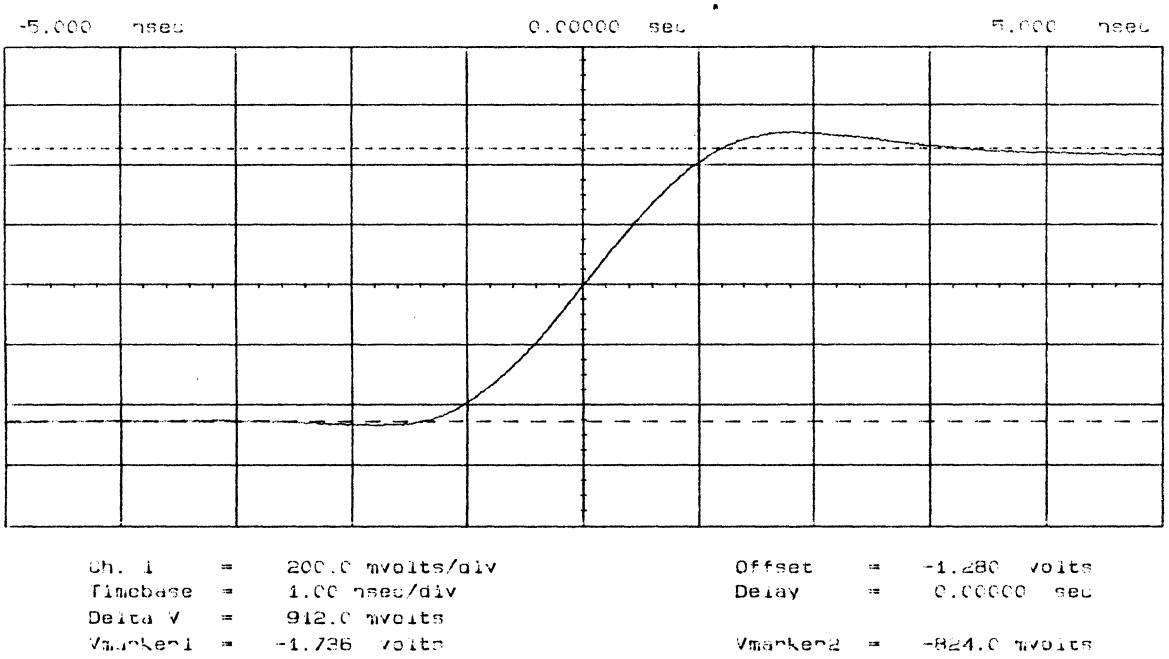


Figure 3-28. Overshoot Adj

16. Check rise and fall time for typ. 1.5ns measured from the 20% to 80% of amplitude.

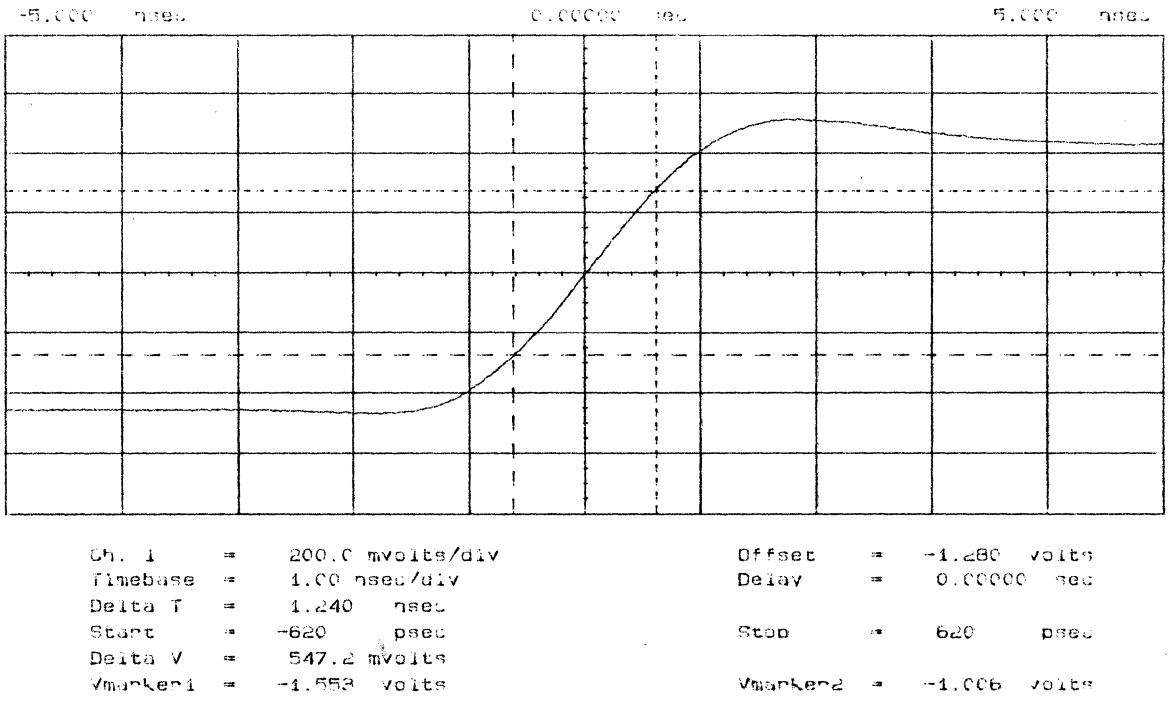


Figure 3-29. Rise Time

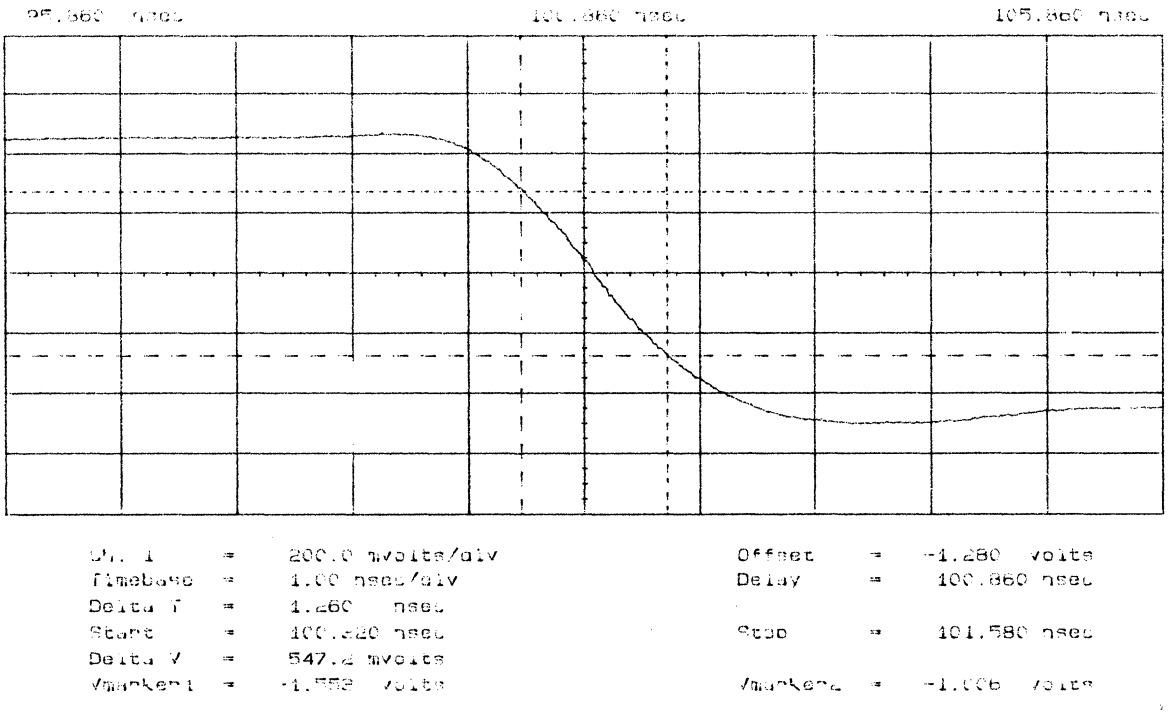


Figure 3-30 Fall Time

Overshoot Adjustment Module Board Output Amplifier 8180B

17. Set 8180B Frequency to 10MHz: (Pages > Timing > Frequency > 10 > Megahertz)

18. Label A ECL Levels: (Pages > Output > Level > ECL Level > Execute)

19. Connect 50 Ohm feedthrough to the data cable to be adjusted.

20. Connect data channel to scope input no. 1 and adjust A66 A60 R3 for <5% overshoot.

Transition Time Adjustment

21. Adjust rise and fall time for typ. 1.5ns with A66 A60 C27 (measured between the 20% and 80% point of transition).

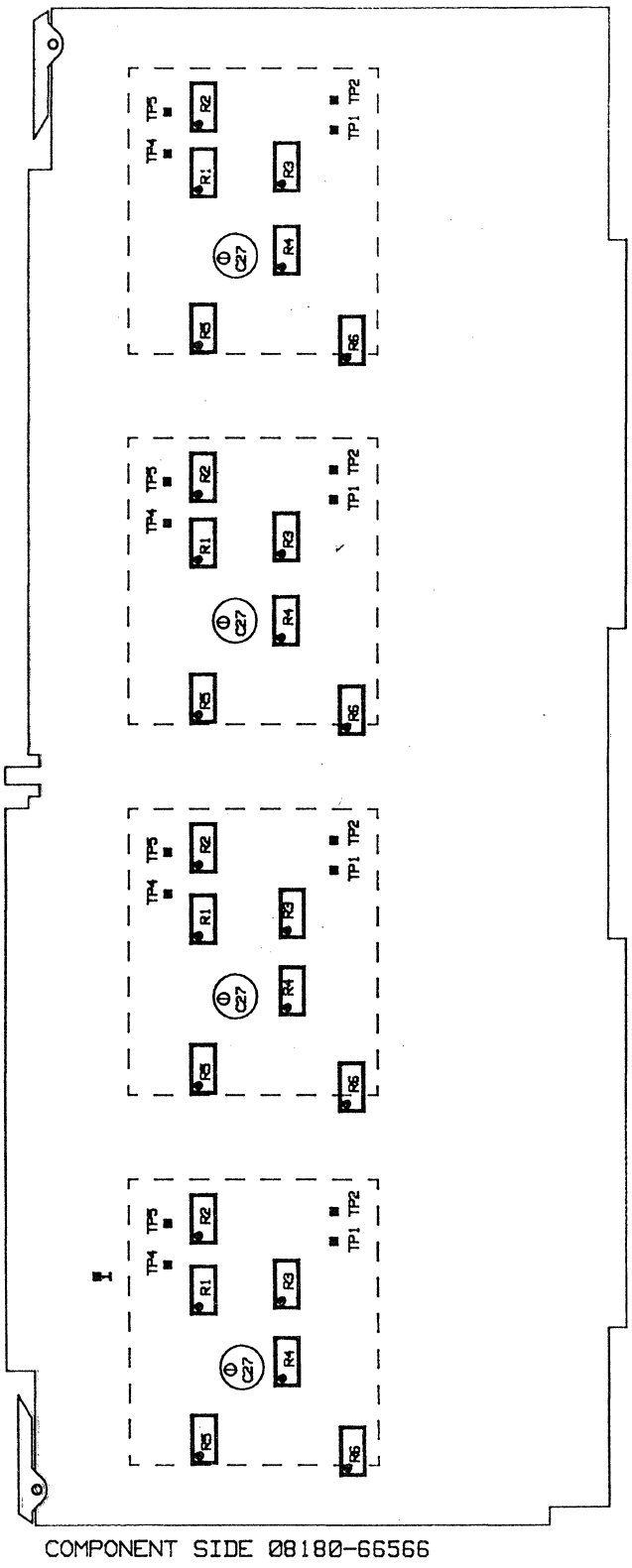


Figure 3-31 A66 Module Board

3-8 Timing Board 08180-66505 (8180A); 08180-66565 (8180B)

Timing Channels Pre-adjustment

Equipment:

Scope	54100D
Active pods	54001A
50 Ohm Feedthrough	10100C
BNC adapter female/female	1250-0080
BNC scope probe adapter	1250-1454
Adjustment cover	08180-04103
Data cable set	15423A
Strobe/Clock cable set	15422A

NOTE

Strobe Reference Delay must have already been adjusted in Section 3-7.

Measurement setup:

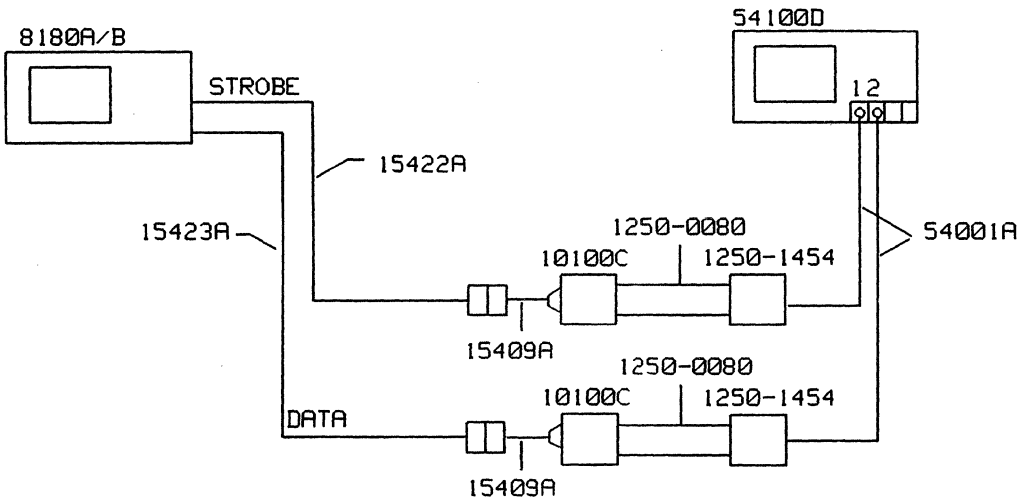


Figure 3-32 Equipment Setup - Timing Channel Pre-adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Frequency 600 KHz; All Channel Format RZ=50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Chnl Timing > All Ch Format > RZ=50%)
3. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label A] > TTL Levels > Execute)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. All Data set: (high) (Pages > Data > Edit > Clear&Set > Set Data > Execute)
6. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)

7. Connect equipment as shown in the measurement set up and press RUN.

8. Program All Channel Delay 990ns: (Pages > Timing > Chnl Timing > All Ch Delay > 990 > Nanosec)

9. Program scope to: (Autoscale > Chan 1 > Chan 1 Display to off > Display > Split Screen to off > Timebase > Sec/Div > 1ns > Delay > 990ns)

10. Connect in turn all Timing Channels to scope input no. 2 and adjust each positive going transition to 990ns with these pots:

    A5 (A65) R105 (Channel 0-0 or 1-0)
    A5 (A65) R305 (Channel 0-1 or 1-1)
    A5 (A65) R505 (Channel 0-2 or 1-2)
    A5 (A65) R705 (Channel 0-3 or 1-3)

11. Set 8180A/B All Channel Delay to 90ns: (90 > Nanosec)

12. Set scope Delay to 90ns: (Timebase > Delay > 90ns)

13. Connect in turn all Timing Channels to scope input no. 2 and store each positive going transition into Memory 1 of the scope: (More > Wfmsave > Memory 1 to on > Store to Memory 1)

14. Change the tap connection on the A8 (A68) DL6 Delay Line on the Address Control 2 Board A8 (A68), so that the deviation of most of the timing channels is closest to 90ns.

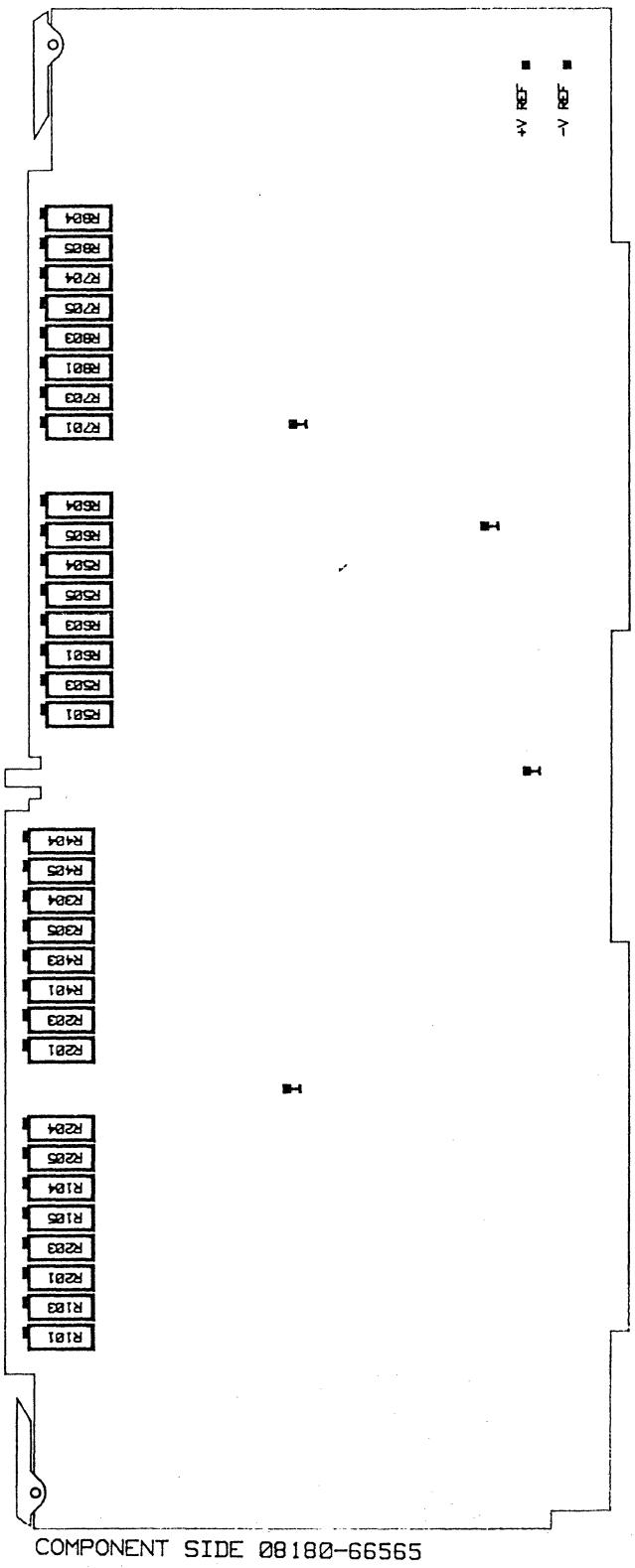


Figure 3-33. A65 Timing Board

Delay and Width Adjustment

Equipment:

Scope	HP 54100D
Active pods	HP 54001A
50 Ohm Feedthrough	HP 10100C
BNC adapter female/female	1250-0080
BNC scope probe adapter	1250-1454
Adjustment cover	08180-04103
Data cable set	HP 15423A
Strobe/Clock cable set	HP 15422A

NOTE

Final adjustment must be done with an adjustment cover in place. Close adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes. Refer to notes 4 and 5 in Chapter 1.

Measurement setup:

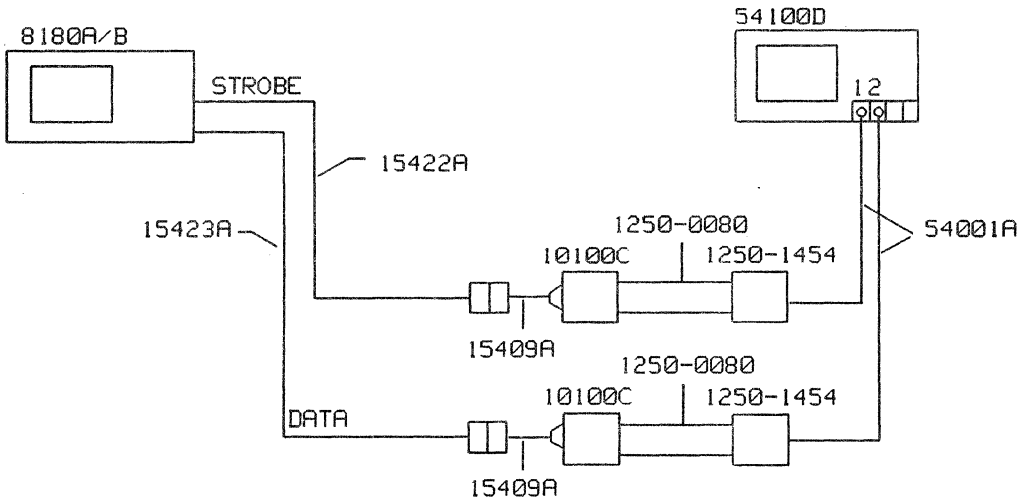


Figure 3-34. Timing Channel - Delay and Width Adj

Delay Adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Frequency 600 Kilohertz; All Channel Format RZ=50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Chnl Timing > All Ch Format > RZ=50%)
3. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label A] > TTL Levels > Execute)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. All Data Set (to high): (Pages > Data > Edit > Clear&Set > Set Data > Execute)
6. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)

7. All Channel Delay 0 ns: (Pages > Timing > Chnl Timing > All Ch Delay > 0 > Nanosec)

8. Connect equipment as shown in the measurement set up and press RUN.

9. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to off > Display > Split Screen to off > Timebase > Sec/Div > 500ps)

10. Connect in turn all Timing Channels to scope input no. 2 and adjust to 0 ns delay between Strobe and Data with the following pots:

    A5 (A65) R104 (Channel 0-0 or 1-0)
    A5 (A65) R304 (Channel 0-1 or 1-1)
    A5 (A65) R504 (Channel 0-2 or 1-2)
    A5 (A65) R704 (Channel 0-3 or 1-3)

11. Recheck zero delay adjustment for all channels and readjust if necessary.

12. Set scope Timebase Delay to 89.0ns: (Timebase > Delay > 89.0ns)

13. Set 8180A/B All Channel Delay to 89.9ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 89.0ns with the following pots:

    A5 (A65) R101 (Channel 0-0 or 1-0)
    A5 (A65) R301 (Channel 0-1 or 1-1)
    A5 (A65) R501 (Channel 0-2 or 1-2)
    A5 (A65) R701 (Channel 0-3 or 1-3)

14. Set 8180A/B All Channel Delay to 90.0ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 89.1ns with the following pots:

    A5 (A65) R105 (Channel 0-0 or 1-0)
    A5 (A65) R305 (Channel 0-1 or 1-1)
    A5 (A65) R505 (Channel 0-2 or 1-2)
    A5 (A65) R705 (Channel 0-3 or 1-3)

15. Set 8180A/B All Channel Delay to 989ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 979.1ns with the following pots:

    A5 (A65) R103 (Channel 0-0 or 1-0)
    A5 (A65) R303 (Channel 0-1 or 1-1)
    A5 (A65) R503 (Channel 0-2 or 1-2)
    A5 (A65) R703 (Channel 0-3 or 1-3).

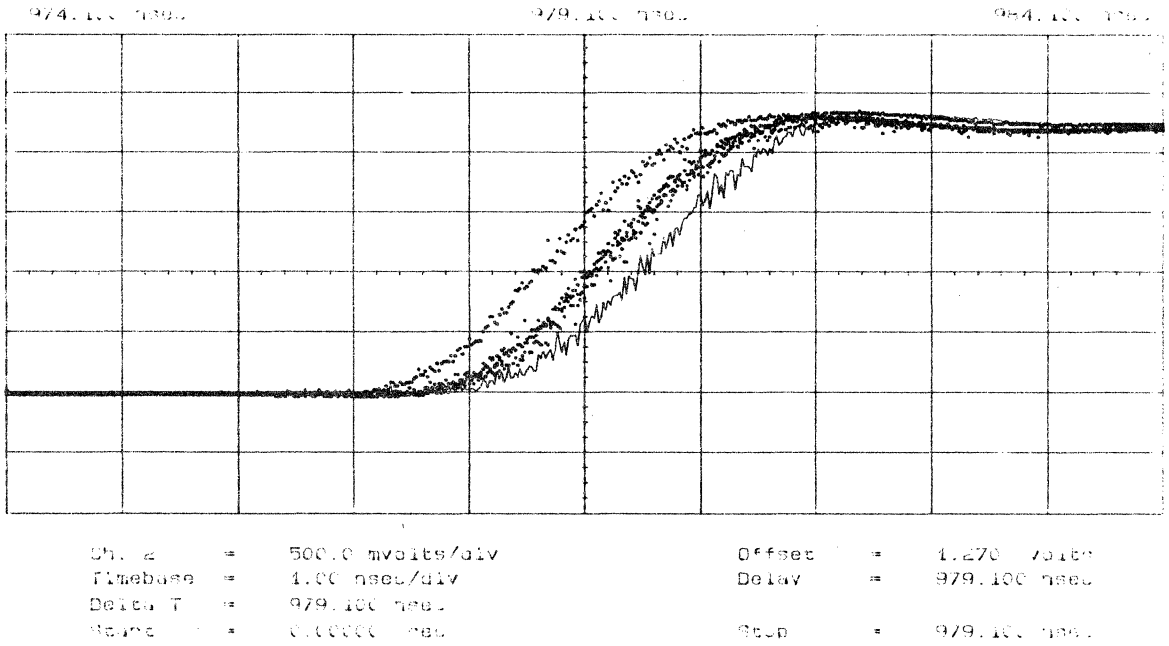


Figure 3-35. Delay Setting

Width Adjustment

16. Set 8180A/B to All Channel Format RZ, All Channel Delay O ns, All Channel Width 10ns: (Pages > Timing > Chnl Timing > All Ch Format > RZ > Exit > All Ch Delay > 0.0 > Nanosec > All Ch Width 10 > Nanosec)

17. Recheck zero delay between Strobe channel and Timing channel.

18. Set scope to: (Timebase > Sec/Div > 500ps > Delay > 0ns)

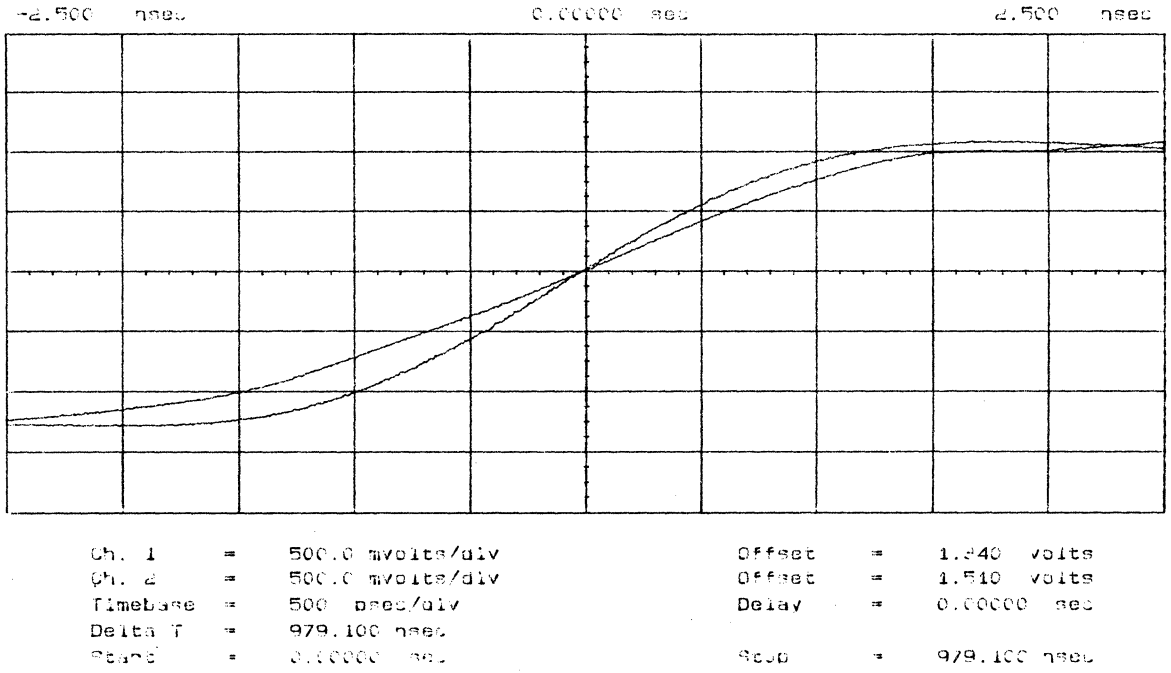


Figure 3-36 Zero Delay - Strobe/Timing Channel

19. Set scope Timebase Delay to 10ns (Timebase > Delay > 10ns)

20. Connect in turn all Timing Channels to scope input no. 2 and adjust the negative going transition (50% point) to 10.0ns with the following pots:

    A5 (A65) R204 (Channel 0-0 or 1-0)
    A5 (A65) R404 (Channel 0-1 or 1-1)
    A5 (A65) R604 (Channel 0-2 or 1-2)
    A5 (A65) R804 (Channel 0-3 or 1-3)

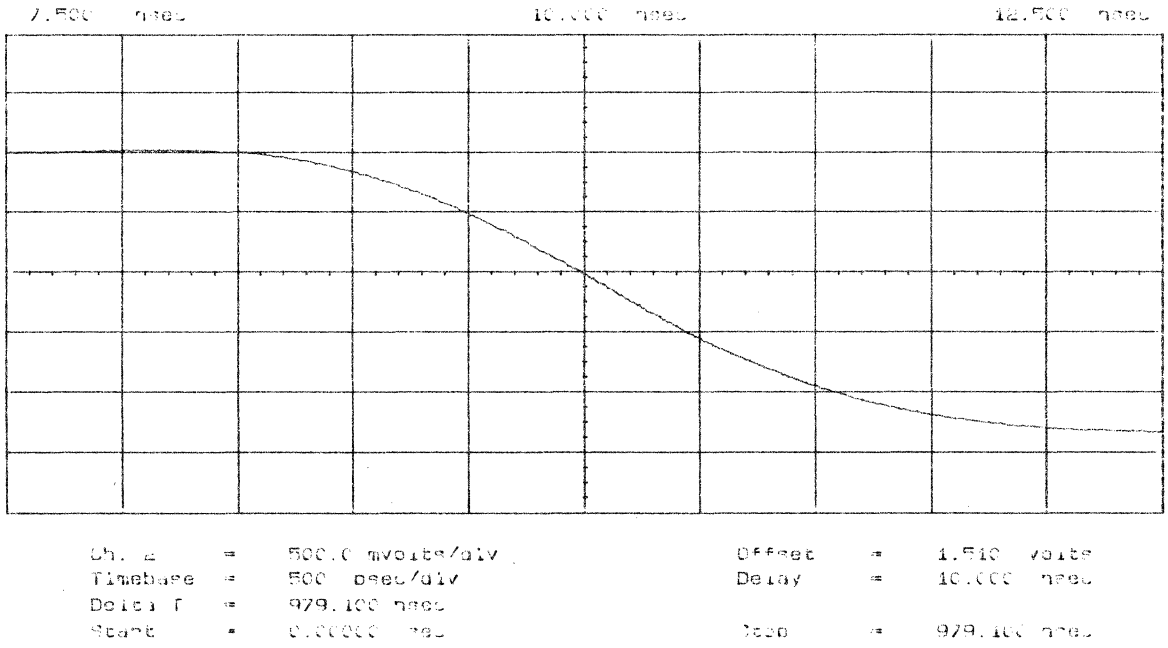


Figure 3-37. Width Adj 1

21. Set 8180A/B All Channel Width to 99.9ns: (99.9 > Nanosec)

22. Set scope Timebase Delay to 98.9ns: (Timebase > Delay > 98.9ns)

23. Connect in turn all Timing Channels to scope input no. 2 and adjust the negative going transition to 98.9ns with the following pots:

    A5 (A65) R201 (Channel 0-0 or 1-0)
    A5 (A65) R401 (Channel 0-1 or 1-1)
    A5 (A65) R601 (Channel 0-2 or 1-2)
    A5 (A65) R801 (Channel 0-3 or 1-3)

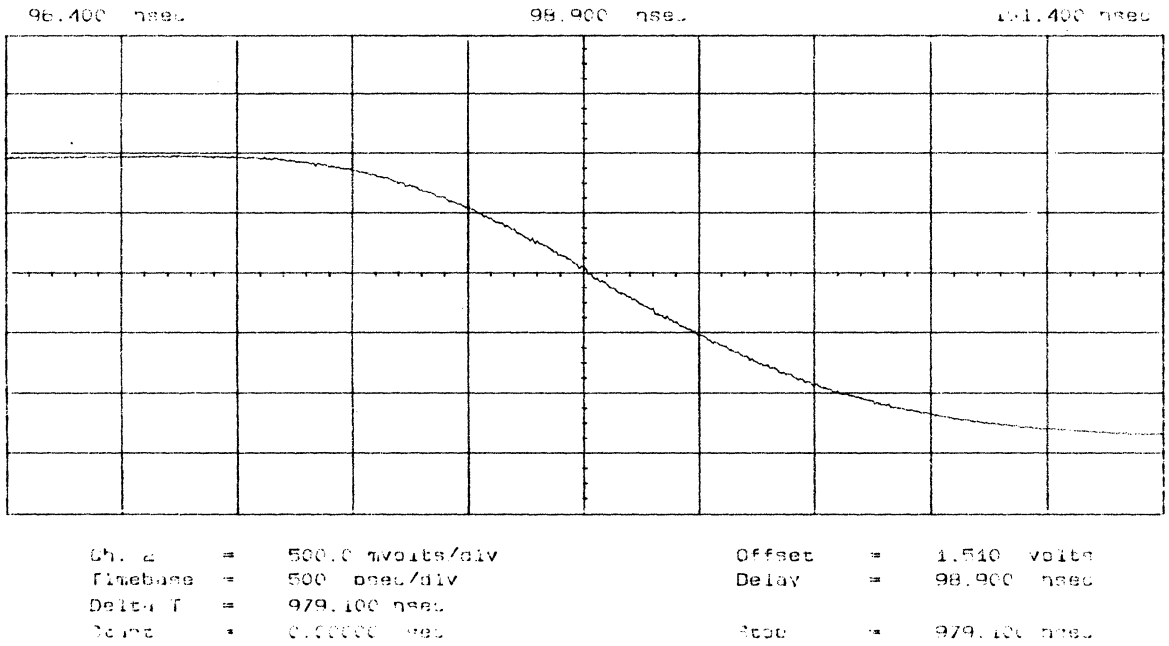


Figure 3-38 Width Adj 2

24. Set 8180A/B All Channel Width to 100ns and adjust the negative going transition to 99.0ns with the following pots:

    A5 (A65) R205 (Channel 0-0 or 1-0)
    A5 (A65) R405 (Channel 0-1 or 1-1)
    A5 (A65) R605 (Channel 0-2 or 1-2)
    A5 (A65) R805 (Channel 0-3 or 1-3)

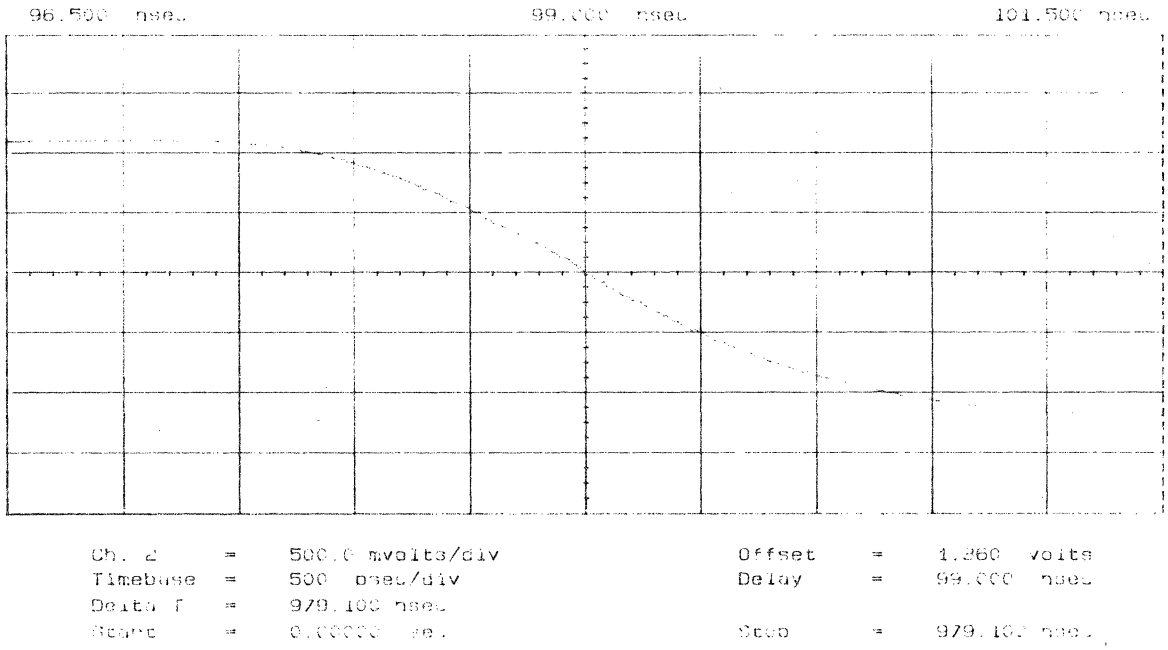


Figure 3-39. Width Adj 3

25. Set 8180A/B All Channel Width to 999ns.

26. Set scope Timebase Delay to 989ns: (Timebase > Delay > 989ns)

27. Adjust the negative going transition to 989 ns with the following pots:

    A5 (A65) R203 (Channel 0-0 or 1-0)
    A5 (A65) R403 (Channel 0-1 or 1-1)
    A5 (A65) R603 (Channel 0-2 or 1-2)
    A5 (A65) R803 (Channel 0-3 or 1-3)

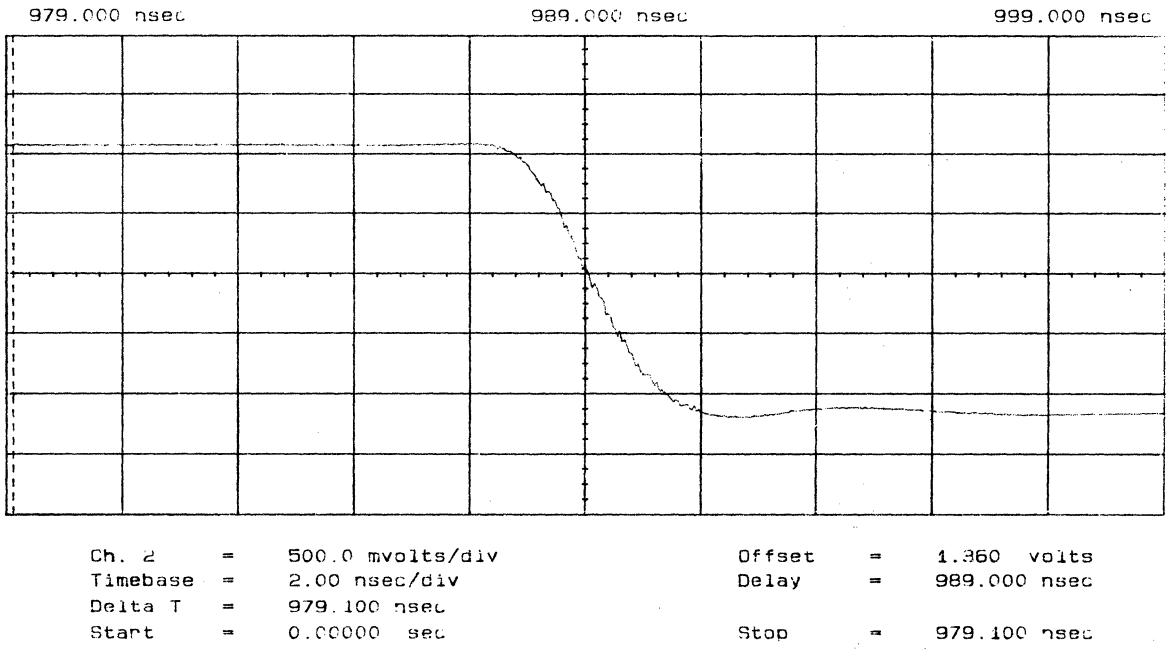


Figure 3-40 Width Adj 4

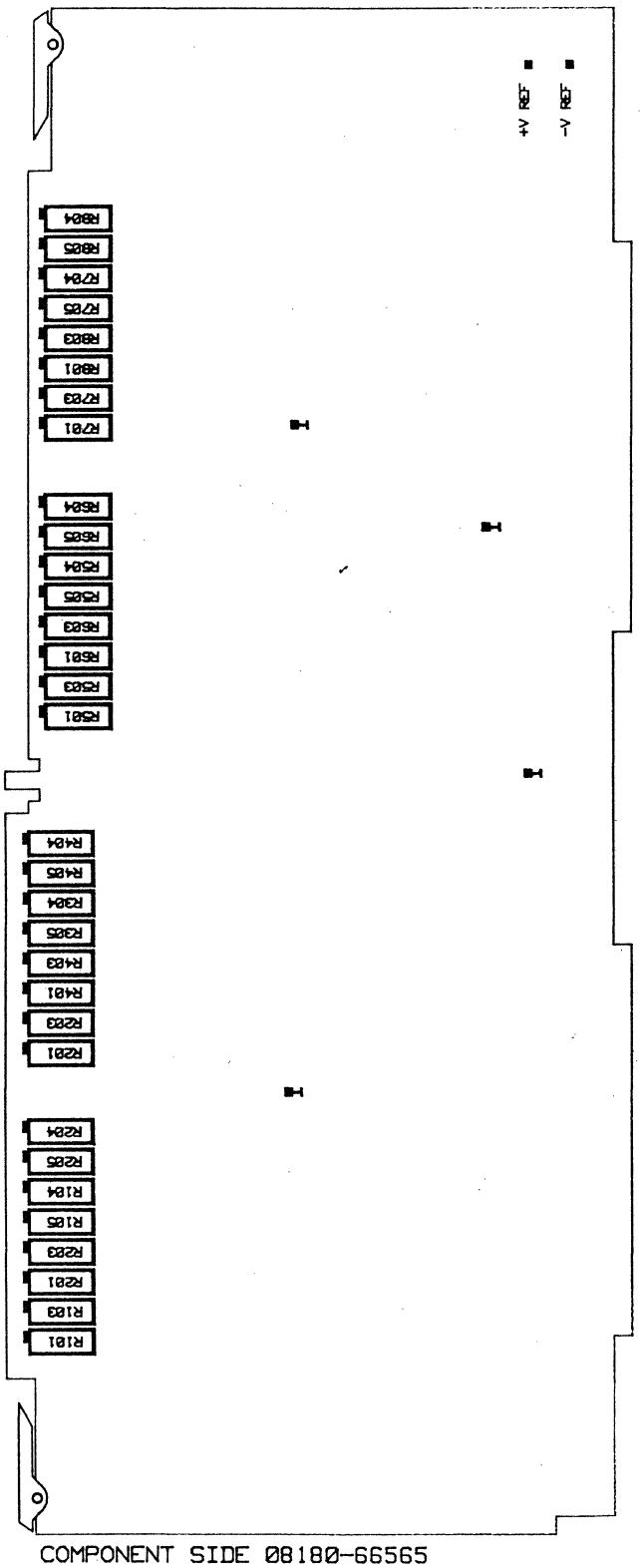


Figure 3-41. Timing Board

3-9 Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

External Run Amplifier Adjustment

Equipment:

Pulse Generator	
BNC to BNC cable	
Scope	54100D
Active Pods	54001A
DVM	3456A

1. Program 8180A/B Input Threshold 0V ; Impedance 50 Ohm RUN input On: (Pages > Control > Inputs > Threshold > 0.Volt > Exit > Impedance > 50 Ohm > Exit > Break Input > On[pos. slope] > Exit > RUN Input > On[pos slope]
2. Set pulse generator to 10 µs squarewave and 2 Volt amplitude into 50 Ohm symmetrical about 0 Volt. Transition Time < 5 ns
3. Connect DVM to A4 (A64) TP1 and GND TP and adjust A4 (A64) R15 for -15mV +/-2mV
4. Connect pulse generator to the 8180A/B EXTERNAL RUN, GATED INPUT.
5. Connect scope probe to A4 (A64) TP1 and GND TP and adjust A4 (A64) C3 for best pulse response.

Clock Output Amplifier High/Low Level Adjustment

Equipment:

Digital Voltmeter	HP 3456A
BNC adapter	15409A
BNC (f) dual banana plug	1251-2277
Clock/Strobe cable set	15422A

High Level Adjustment

1. Program 8180A Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Clock 1 Complement; Clock 2 Complement: (Pages > Output > Clock Output > Clock 1 Polar > Complement > Exit > Clock 2 Polar > Complement)
3. Label A High Level 0V; Low Level -2V: (Pages > Output > Level > Next Label [to Label A] > Low <- > High [to High Level] > 0 > Volt > Low <- > High [to Low Level] > -2 > Volt)
4. Outputs On (Status Stop): (Pages > Output > Output On/Off > On)
5. Connect clock channel to be adjusted Adjust A4 (A64) A60 R2 for 0V ±0.5mV DVM reading.

Low Level Adjustment

6. Clock 1 Normal; Clock 2 Normal: (Pages > Output > Clock Output > Clock 1 Polar > Normal > Exit > Clock 2 Polar > Normal)
7. Label A High Level +2V; Low Level 0V: (Pages > Output > Level > Low <-> High [to High] > 2 > V > Low <-> High [to Low] > 0 > Volt)

8. Adjust A4 (A64) A60 R1 for 0V +/-0.5mV DVM reading.

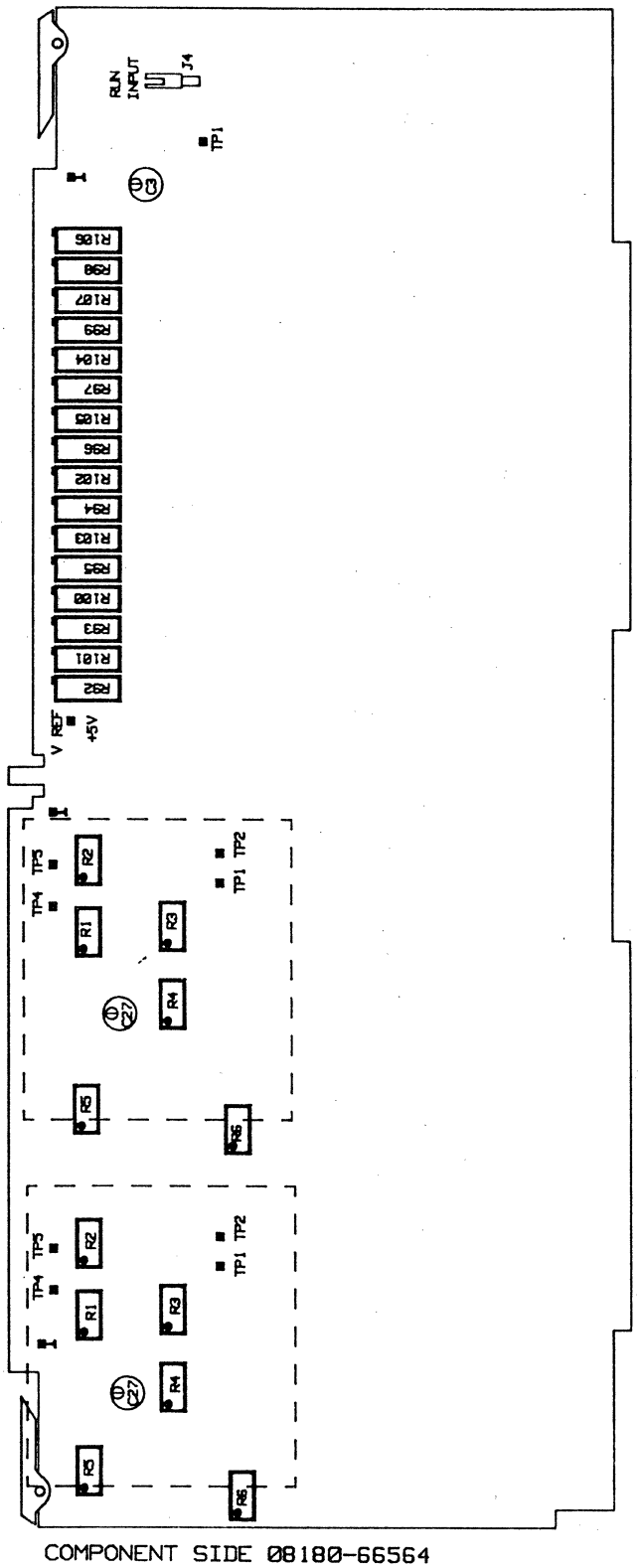


Figure 3-42. A64 Sync Board

Flatness and Overshoot Adjustment

Equipment:

Scope	HP 54100D
Active pods	HP 54001A
BNC adapter	HP 15409A
Strobe/Clock cable set	HP 15422A

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Label A TTL Levels; Strobe Level to TTL: (Pages > Output > Level > Next Label [to Label A] > TTL Levels > Execute > Exit > Strobe Level > TTL)
3. Frequency 250 Hertz: (Pages > Timing > Frequency > 250 > Hertz)
4. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
5. Clock 1 Format RZ=50%; Clock 2 Format RZ=50%: (Pages > Timing > Clock Timing > Clock 1 Format > RZ=50% > Exit > Clock 2 Format > RZ=50%)
6. Outputs On: (Pages > Output > Output on/off > on)
7. Connect Strobe Output to scope input no. 1 and clock channel to be measured to scope channel 2.
8. Set 54100D to Autoscale and Timebase to 500 µs: (Autoscale > Timebase > Sec/Div > 500 > microsec)
9. Adjust A4 (A64) A60 R4 and A4 (A64) A60 R6 for best flatness.

10. Connect 50 Ohm feedthrough to currently connected clock output and adjust A4 (A64) A60 R5 for best flatness.

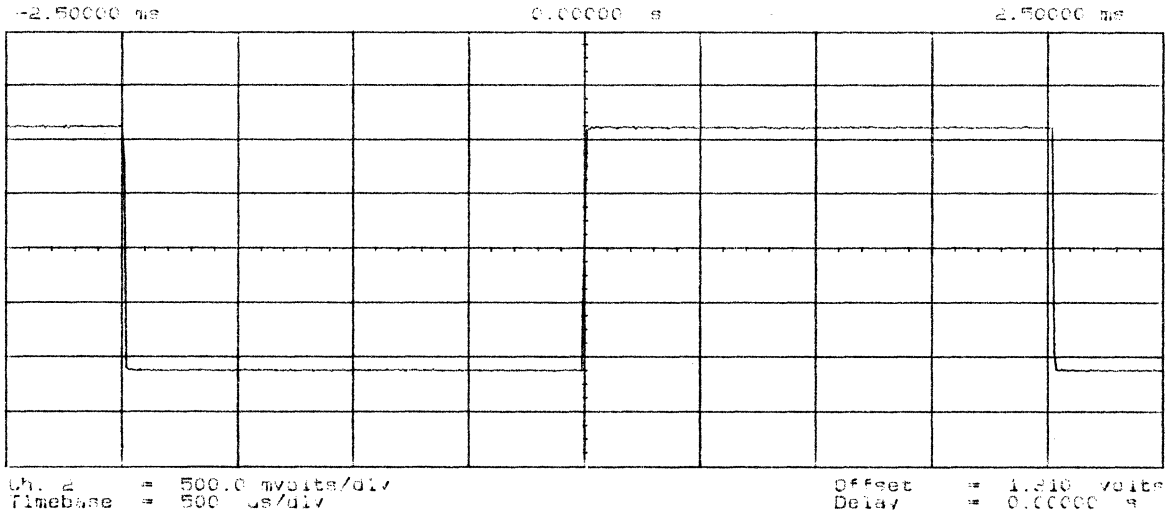


Figure 3-43. Sync Board O/p Amp Flatness Adj

Overshoot Adjustment Sync Board Output Amplifier 8180A

11. Set 8180A Frequency to 10MHz (Pages > Timing > Frequency > 10 > Megahertz)

12. Label A ECL Levels (Pages > Output > Level > ECL Level > Execute)

13. Connect clock channel to be adjusted to the scope input no. 2 (trigger to the 8180A strobe output-> scope channel no. 1) and adjust A4 A60 R3 for <9% overshoot.

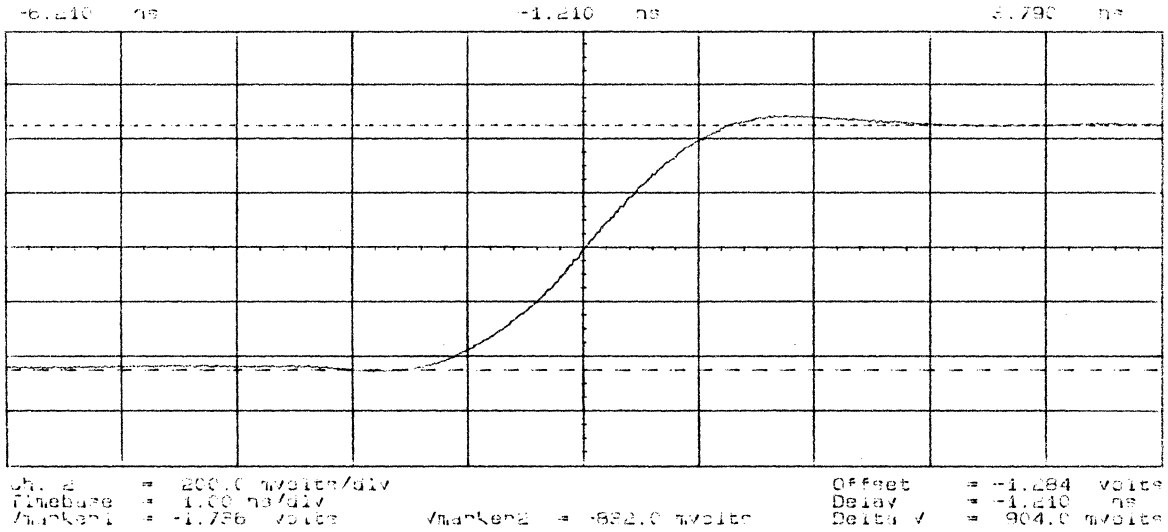


Figure 3-44 Sync Board O/P Amp Overshoot

14. Check rise and fall time for typical 1.5ns measured from the 20% to 80% of amplitude.

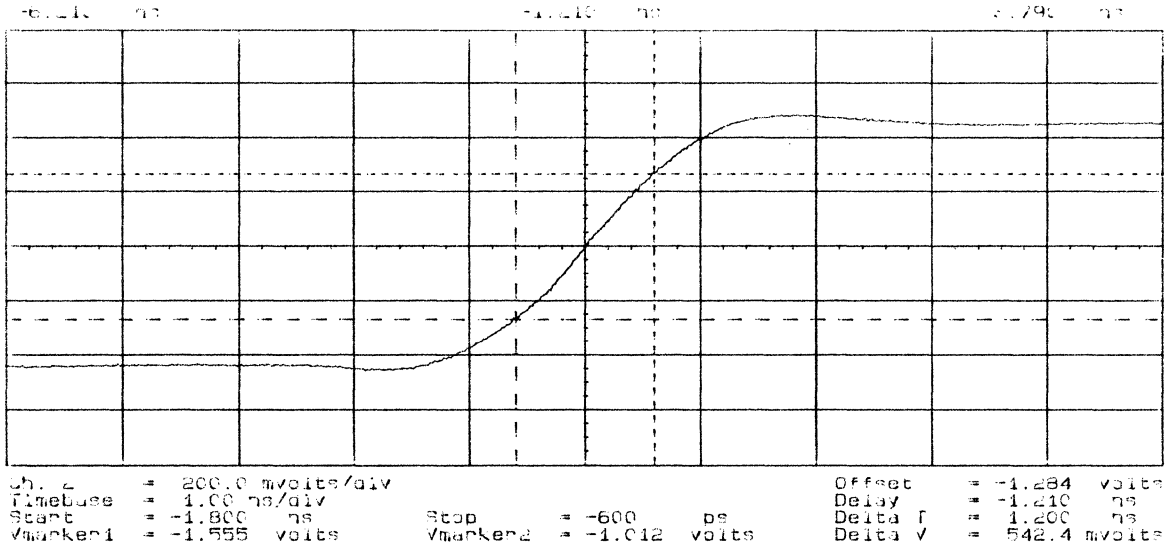


Figure 3-45 Sync Board O/P Amp Rise Time

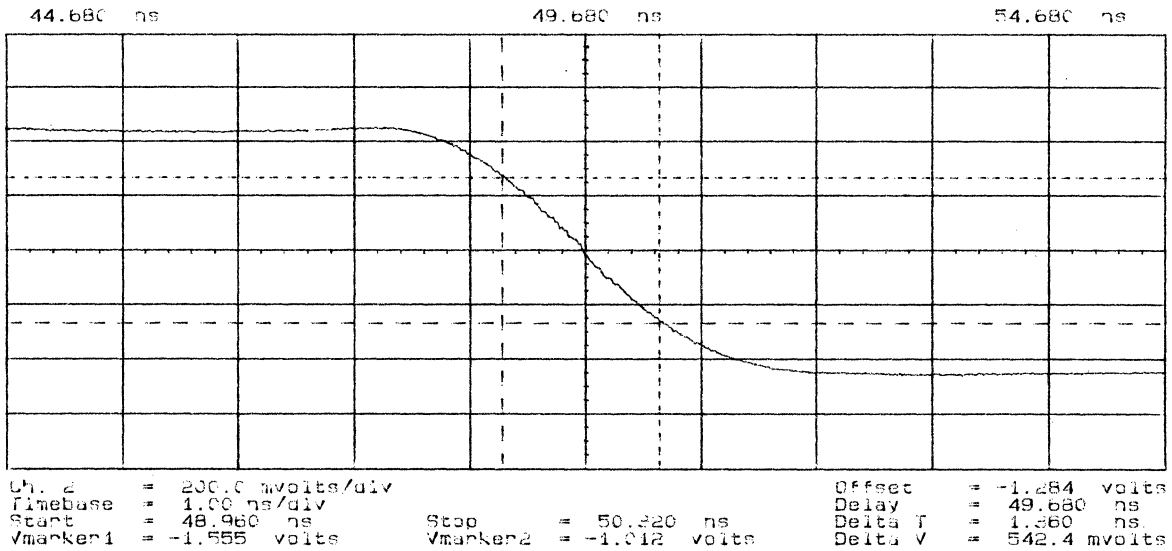


Figure 3-46 Sync Board O/P Amp Fall Time

Overshoot Adjustment Sync Board Output Amplifier 8180B

15. Set 8180B Frequency to 10MHz: (Pages > Timing > Frequency > 10 > Megahertz)

16. Label A ECL Levels: (Pages > Output > Level > ECL Level > Execute)

17. Connect a 50 Ohm feedthrough to the connected clock cable.

18. Connect the clock channel to be adjusted to the scope input no. 2 (Trigger to the 8180B strobe output- > scope input no. 1), and adjust A64 A60 R3 for <5% overshoot.

Transition Time Adjustment

19. Adjust rise time to 1.5ns with A64 A60 C27 (measured between the 20% and 80% point of transition).

3-10 Address Control 2 Board 08180-66508 (8180A); 08180-66568 (8180B)

Clock Channels Pre-adjustment

Equipment:

Scope	54100D
Active Pods	54001A
Adjustment Cover	08180-04103
Strobe/Clock cable set	15422A
BNC Adapter	15409A
50 Ohm Feedthrough	10100C
BNC Adapter female/female	1250-0781
BNC Scope probe Adapter	1250-1454

Measurement setup:

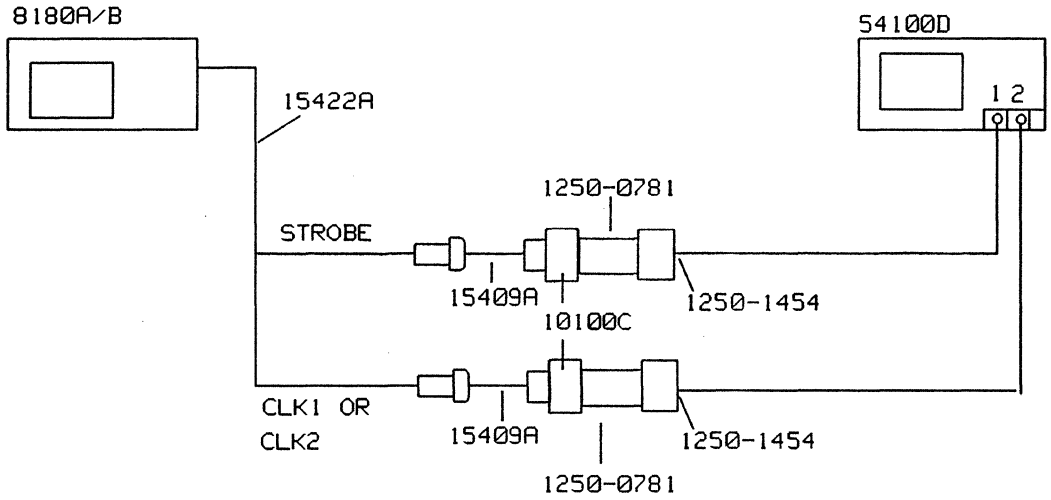


Fig 3-47. Clock Channels - Pre-adjustment

1. Cancel out the scope trigger delay of scope channel 1 and the interchannel delay between scope channel 1 and scope channel 2.
2. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
3. Frequency 600 kHz; Clock 1 Format RZ = 50%; Clock 2 Format RZ = 50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Clock Timing > Clock Format > RZ=50% > Exit > Clock 2 Format > RZ = 50%)
4. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label [to label > TTL Levels > Execute)
5. Outputs On: (Pages > Output > Output on/off > On)
6. Strobe Output to Clock and press RUN: (Pages > Control > Strobe Output > Clock > RUN)
7. Connect Strobe channel to scope input no. 1 and Clock 1 channel to scope input no. 2.
8. Program Clock 1 Delay and Clock 2 Delay to 990ns: (Pages > Timing > Clock Timing > Clock 1 Delay > 990 > Nanosec > Exit > Clock 2 Delay > 990 > Nanosec)

9. Set scope to: (Autoscale > Display > Split Screen to Off > Channel 1 > Channel 1 to Off > Delta t > T Markers to On > Start Marker to 0 ns > Stop Marker to 990ns > Timebase > Sec/Div > 5 n Delay > 990 ns)

10. Adjust A4 (A64) R101 so that the 50% point of the positive going transition of Clock 1 meets the center graticule line.

    Adjust A4 (A64) R105 so that the 50% point of the positive going transition of Clock 2 meets the center graticule line.

11. Set 8180A/B Clock 1 and Clock 2 Delay to 90 ns (Exit > Clock 1 Delay > 90 > Nanosec > Exit > Clock 2 Delay > 90 > Nanosec)

12. Set scope to (Timebase > Delay > 90ns > Delta t > Stop Marker > 90ns)

13. Measure and note the time deviation (+/-) of clock 1 to 90ns.

14. Adjustment for the 8180A: Change the tap of delay line A8 DL4 so that the deviation of the 50% point of the positive going transition is a minimum.

    Adjustment for the 8180B: Adjust A8 (A68) DL4 so that the 50% point of the positive going transition of clock 1 meets the center graticule line.

15. Measure and note the time deviation (+/-) of clock 2 to 90ns.

16. Adjustment for the 8180A: Change the tap of delay line A8 DL5 so that the deviation of the 50% point of the positive going transition is a minimum.

    Adjustment for the 8180B: Adjust A8 (A68) DL5 so that the 50% point of the positive going transition of clock 2 meets the center graticule line.

3-11 Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

Delay and Width Adjustment

Equipment:

Adjustment cover:	08180-04103 (8180A/B)
Strobe/Clock cable set	15422A
BNC adapter	15409A
50 Ohm feedthrough	10100C
BNC adapter female/female	1250-0080
BNC scope probe adapter	1250-1454

NOTE

On the 8180A, final adjustment must be done with the adjustment cover in place. Block adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes.

On the 8180B, final adjustment must be done with the adjustment cover in place. Block the circular hole during adjustment. Allow instrument to warm up for 30 minutes.

Before starting the measurements, cancel out the following delays:

- The trigger delay of scope channel 1:
  (More > Cal&Test > Cal Menu > Trigger Delay channel 1 > Knob)
- The interchannel delay between scope channel 1 and channel 2:
  (Trigger Delay Chan 1 > Chan to Chan Skew > Knob)

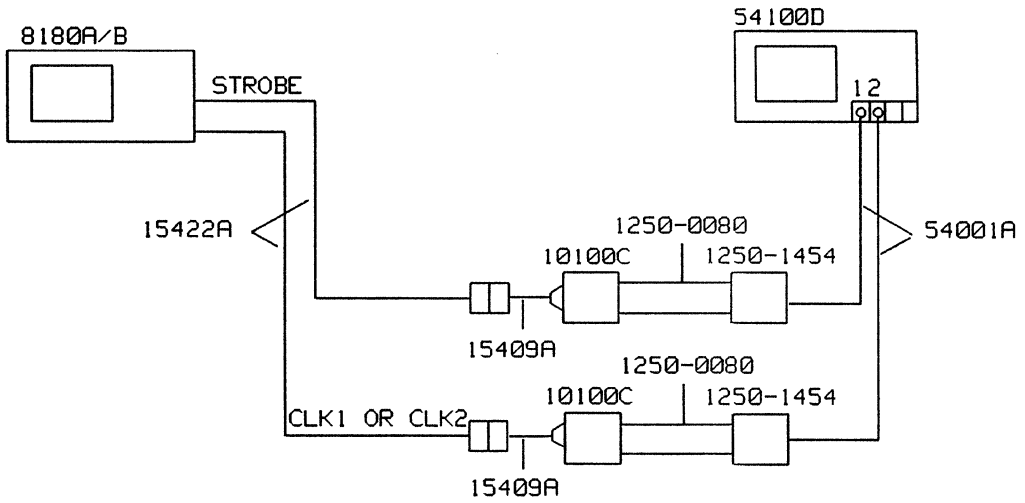


Figure 3-48. Measurement Setup - Clk Delay and Width

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)

2. Frequency 600kHz: (Pages > Timing > Frequency > 600 > Kilohertz)

3. Strobe Level TTL; Label A TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label > TTL Levels > Execute)

4. Outputs On: (Pages > Output > Output on/off > on)

5. Clock 1 Format RZ 50%; Clock 2 Format RZ 50%: (Pages > Timing > Clock Timing > Clock 1 Format > RZ=50% > Exit > Clock 2 Format > RZ=50%)

6. Strobe output Clock: (Pages > Control > Strobe output > Clock)

7. Clock 1 Delay 0ns; Clock 2 Delay 0ns: (Pages > Timing > Clock Timing > Clock 1 Delay > 0 > Nanosec. > Exit > Clock 2 Delay > 0 > Nanosec)

8. Connect equipment as shown in the measurement set up and press RUN.

9. Connect Strobe to scope input no.1 and Clock 1 to scope input No. 2.

10. Set the 54100D to: (Autoscale).

11. Switch Chan 2 off; Split Screen off; Timebase to 500ps; Trigger on positive slope: (Chan 2 > Chan 2 Display > off > Timebase > Sec/Div > 500 > psec > Trigger > Slope > positive)

12. Check if the 50% point of the displayed Strobe transition is centered on the center graticule line. Set Start marker to 50% point of transition: (Delta T > T markers > On > Start marker > Knob)

13. Switch Channel 1 Off and Channel 2 On: (Chan 1 > Chan 1 Display > Off > Chan 2 > Chan 2 Display > On)

Zero Delay Adjustment

14. Adjust A4 (A64) R100 (Clock 1) so that the 50% point of the displayed Clock 1 transition meets the center graticule line.

    Adjust A4 (A64) R104 (Clock 2) so that the 50% point of the displayed Clock 2 transition meets the center graticule line.

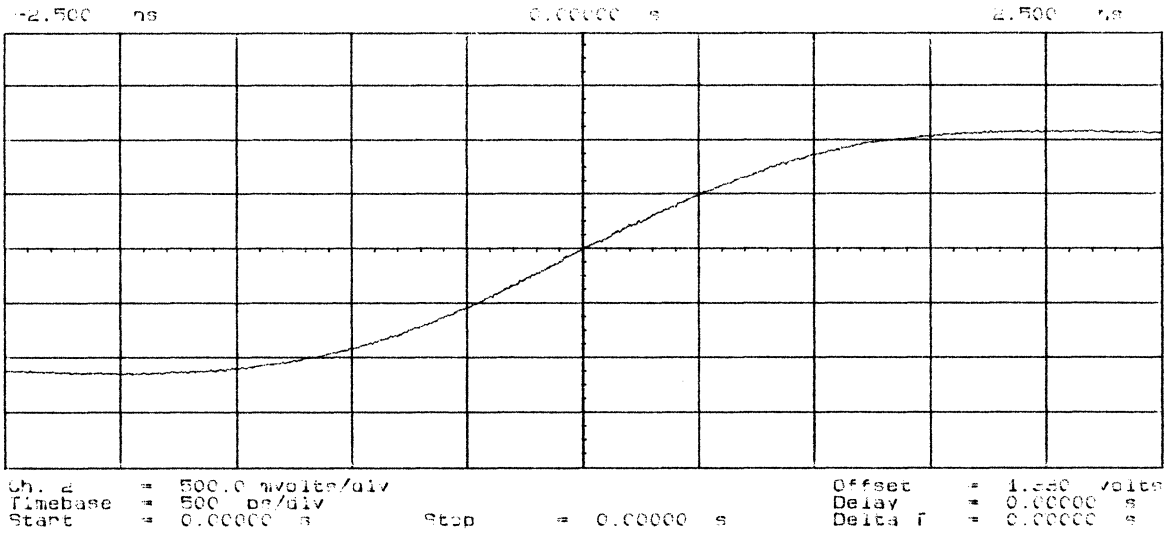


Figure 3-49. Zero Delay

15. Connect Clock 1 to scope.
16. Set scope Delay to 89ns: (Timebase > Delay > 89ns)
17. Set Clock 1 Delay to 89.9 nsec and adjust A4 (A64) R93 to 89.0 nsec.
18. Set Clock 1 Delay to 90.0 nsec and adjust A4 (A64) R101 to 89.1 nsec.
19. Set Clock 1 Delay to 989 nsec.
20. Set scope Timebase Delay to 979.1 nsec: (Timebase > Delay > 979.1nsec)
21. Adjust A4 (A64) R92 so that the 50% point of the displayed Clock 1 transition meets the center graticule line.

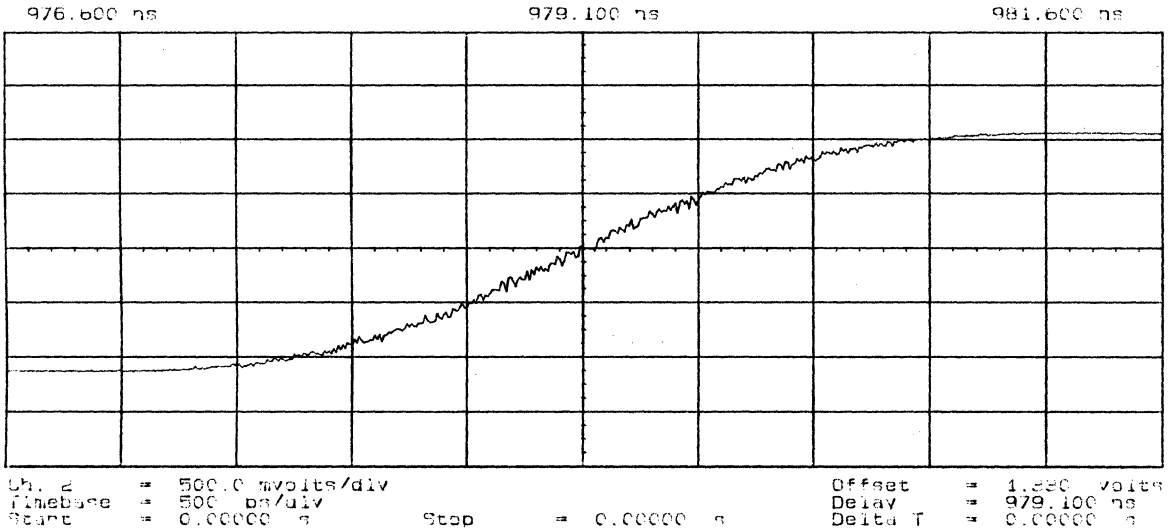


Figure 3-50 Clk Delay

22. Connect Clock 2 to scope channel 2 and program Clock 2 Delay: (Exit > Clock 2 Delay)

23. Set Clock 2 Delay to 89.9 nsec and adjust A4 (A64) R97 to 89 nsec. Set Clock 2 Delay to 90.0 nsec and adjust A4 (A64) R105 to 89.1 nsec. Set Clock 2 Delay to 989 nsec and adjust A4 (A64) R96 to 979.1 nsec.

Width Adjustment Clock 1

24. Connect Strobe to scope channel no.1 and connect Clock 1 to scope channel 2.

25. Set 8180A/B Clock 1 Format to RZ and Clock 2 Format to RZ: (Pages > Timing > Clock Timing > Clock 1 Format > RZ > Exit > Clock 2 Format > RZ)

26. Set Clock 1 Delay and Clock 2 Delay to 0.00 ns: (Clock 1 Delay > 0 > Nanosec > Exit > Clock 2 Delay > 0 > Nanosec)

27. Set Clock 1 Width and Clock 2 Width to 10ns: (Exit > Clock 1 Width > 10 > Nanosec > Exit > Clock 2 Width > 10 > Nanosec)

28. Set 54100D Timebase to 500ps/DIV and Timebase Delay to 10ns: (Timebase > SEC/DIV > 500ps > Delay > 10ns)

29. Adjust A4 (A64) R102 so that the 50% point of the negative going transition of Clock 1 meets the center graticule line.

30. Set Clock 1 Width to 99.9ns and set scope Timebase Delay to 98.9ns. Adjust A4 (A64) R94 so that the 50% point of the displayed transition meets the center graticule line.

31. Set Clock 1 Width to 100ns and set Stop marker to 99.0ns. Adjust A4 (A64) R103 so that the 50% point of the displayed transition meets the Stop marker.

32. Set Clock 1 Width to 999ns and set scope Timebase Delay to 989ns. Adjust A4 (A64) R95 so that the 50% point of the displayed transition meets the center graticule line.

Width Adjustment Clock 2

33. Connect Clock 2 to scope channel 2.

34. Set 54100D Timebase to 500ps/DIV and Timebase Delay to 10ns: (Timebase > SEC/DIV > 500ps > Delay > 10ns)

35. Adjust A4 (A64) R106 so that the 50% point of the negative going transition of Clock 2 meets the center graticule line.

36. Set Clock 2 Width to 99.9ns and set scope Timebase Delay to 98.9ns. Adjust A4 (A64) R98 so that the 50% point of the displayed transition meets the center graticule line.

37. Set Clock 2 Width to 100ns and set Stop marker to 99.0ns. Adjust A4 (A64) R107 so that the 50% point of the displayed transition meets the Stop marker.

38. Set Clock 2 Width to 999ns and set scope Timebase Delay to 989ns. Adjust A4 (A64) R99 so that the 50% point of the displayed transition meets the center graticule line.

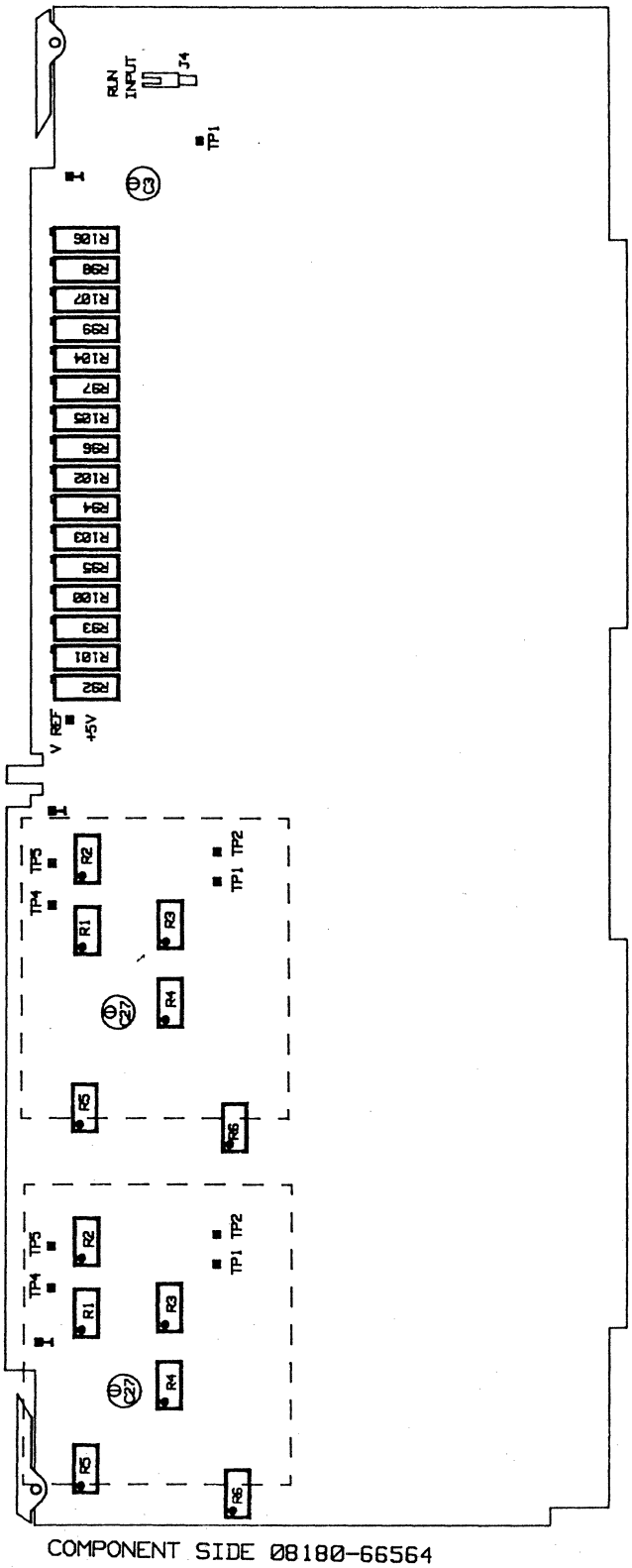


Figure 3-51. Sync Board

3-12 Adjustments to be made after Board Replacement

The following table gives the adjustments that need to be carried out whenever any of the 8180A/B boards listed are replaced.

Table 3-1. Board Replacement - Adjustments Required

Board (Version)	Exchange Part no.	Check and Adjustment	Adj. Cover required
A1 (A)	08180-69501	None	No
A61 (B)	08180-69561	None	No
A2 (A)	08180-69502	Restart Circuit function Output Amplifier High/Low Levels (A6) D-A Converter	No No No
A62 (B)	08180-69562	Output Amplifier High/Low Levels (A6) D-A Converter	No No
A3 (A)	08180-69503	Internal Clock Generator D-A Converter Ext. Clock Amp. Thres. & Pulse Resp. Frequency Error Notification Strobe Reference Delay	Yes No No Yes Yes
A63 (B)	08180-69563	Internal Clock Generator D-A Converter Ext. Clock Amp. Thres. & Pulse Resp. Frequency Error Notification Strobe Reference Delay Zero Delay Clock 1, Clock 2	Yes No No Yes Yes No
A4 (A)	08180-69504	Ext. RUN Amp. Thres. & Pulse Response Clock 1 & 2 Output Amplifier Clock 1 & 2 Delay and Width Clock Channels Pre-adjustment Overshoot Clock 1 & 2 Output	No No Yes No No
A64 (B)	08180-69564	Ext. RUN Amp. Thres. & Pulse Response Clock 1 & 2 Output Amplifier Clock 1 & 2 Delay and Width Clock Channels Pre-adjustment Overshoot Clock 1 & 2 Output Transition Time	No No Yes No No No
A5 (A)	08180-69505	Output Amplifier Timing Delay & Width Timing Channels Pre-adjustment	Yes No
A65 (B)	08180-69565	Output Amplifier Timing Delay & Width Timing Channels Pre-adjustment	Yes No
A6 (A)	08180-69506	Output Amplifier DC Levels Output Amplifier Overshoot	Yes No
A66 (B)	08180-69566	Output Amplifier DC Levels Output Amplifier Overshoot Output Amplifier Transition Time	Yes No No

3-13 Locating Components in the 8180A Data Generator

The following diagrams should be used when locating components/test-points in the HP 8180A Data Generator.

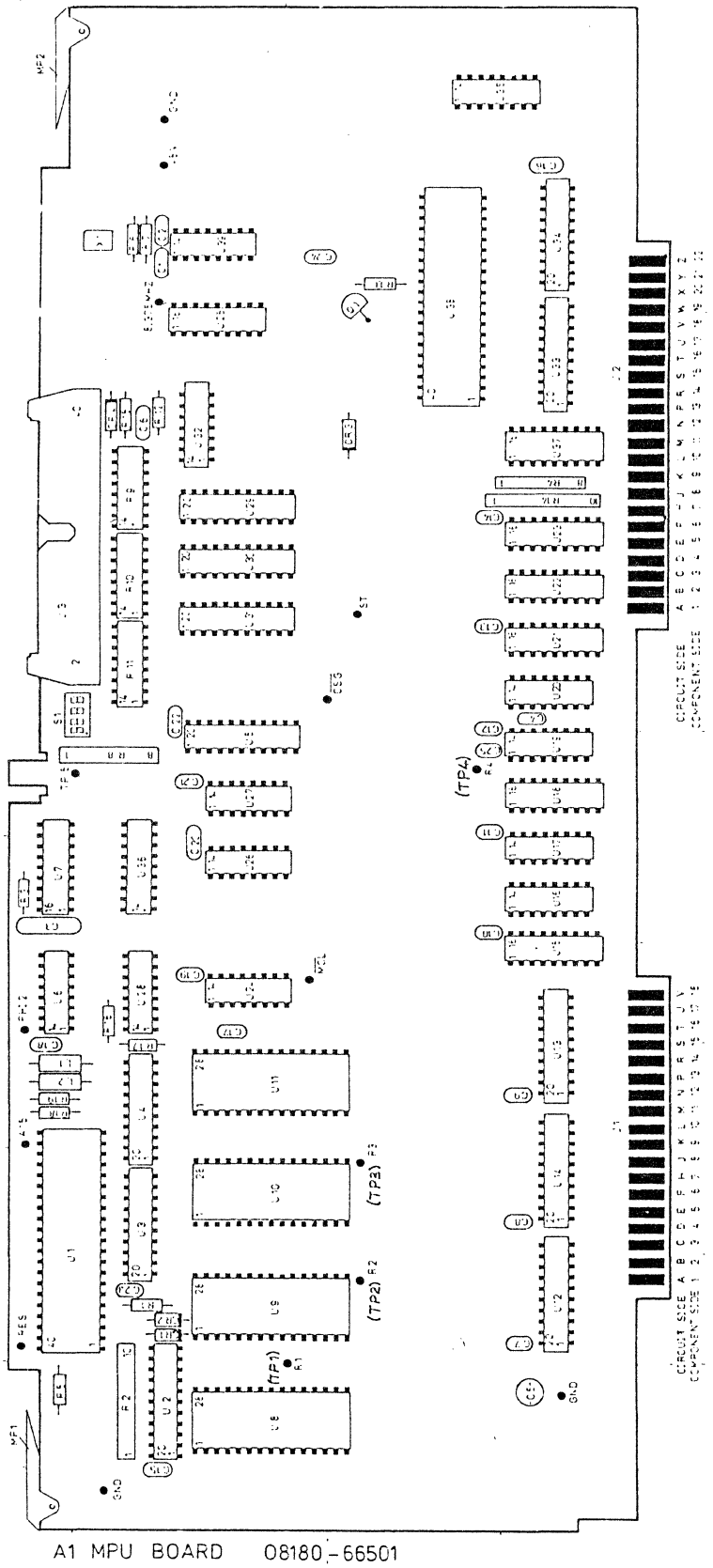


Figure 3-52. A1 Microprocessor Board

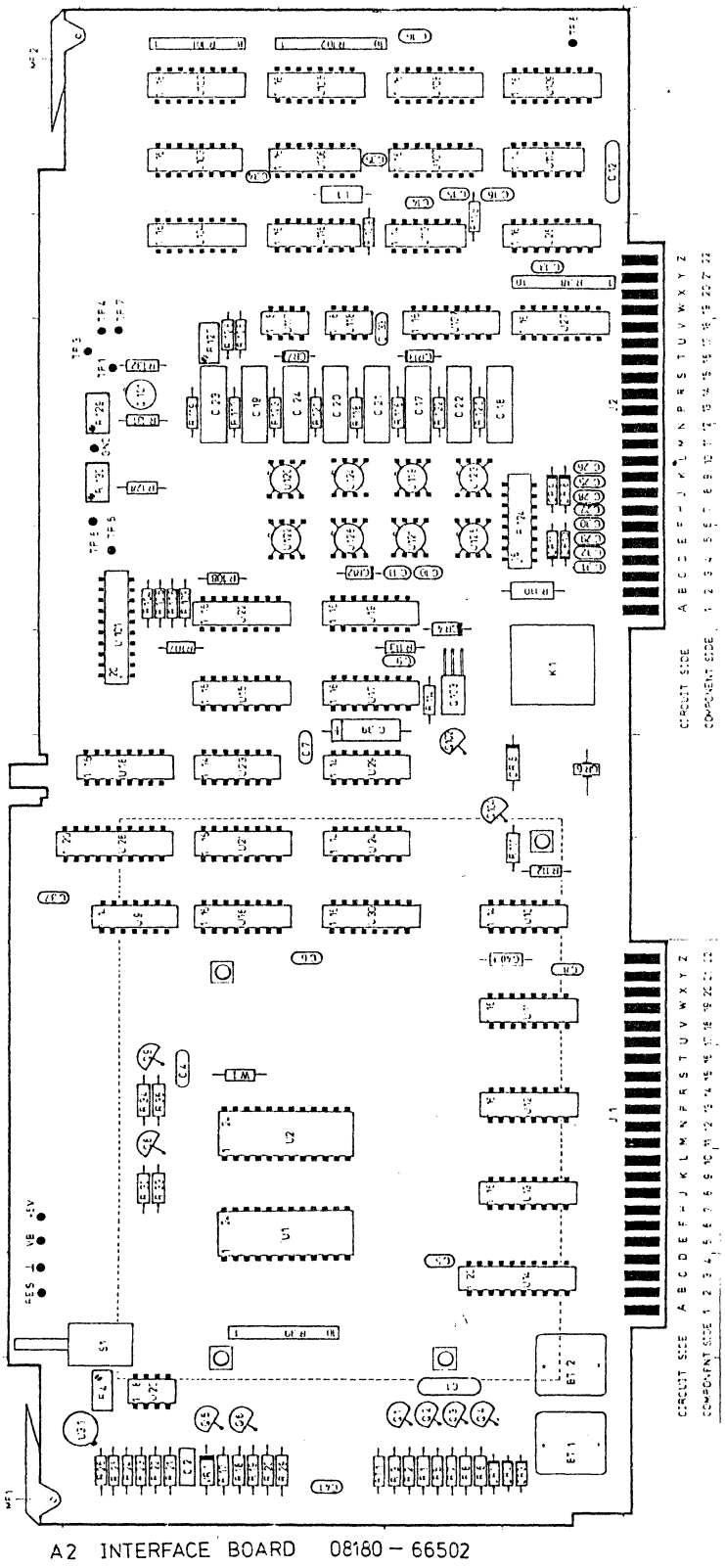


Figure 5-53. A2 Interface Board

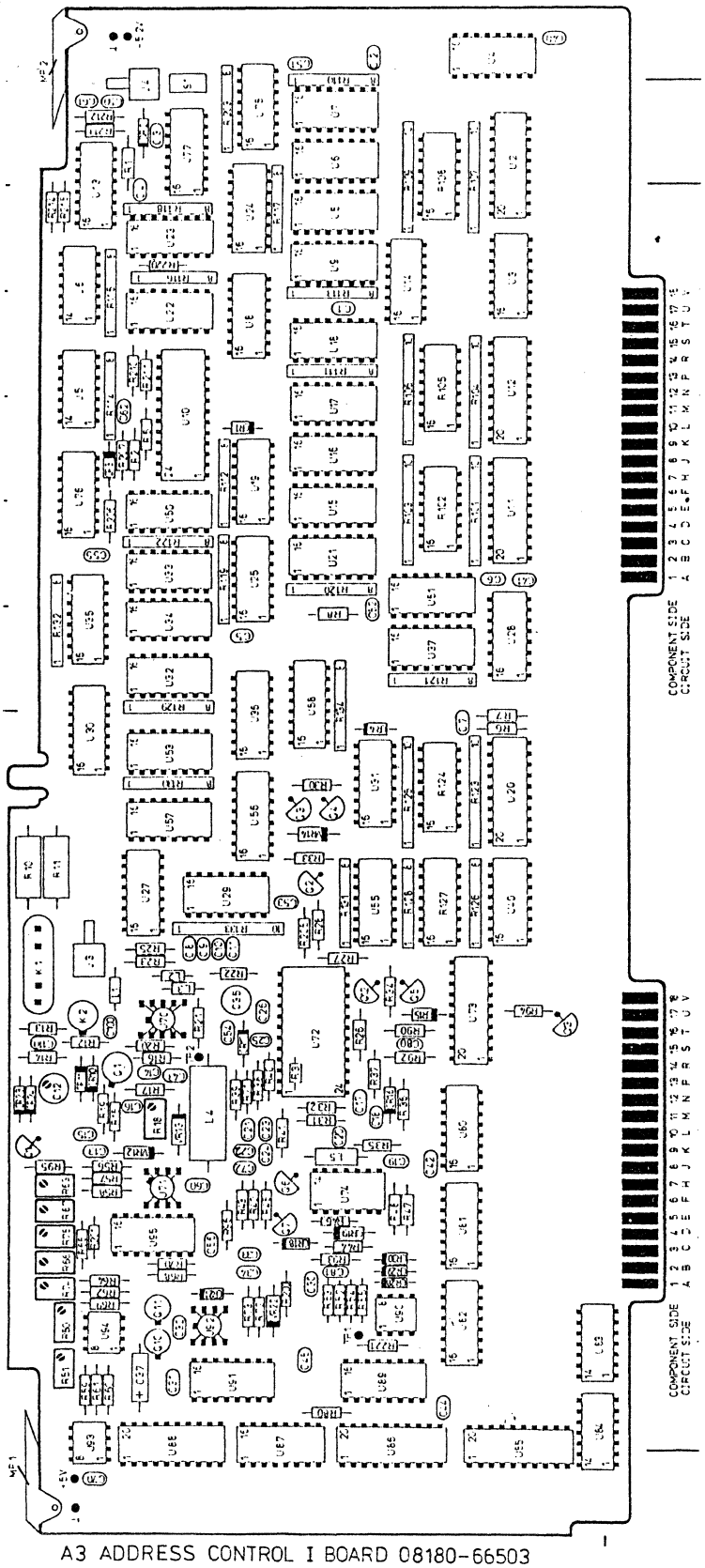


Figure 3-54. A3 Address Control I Board

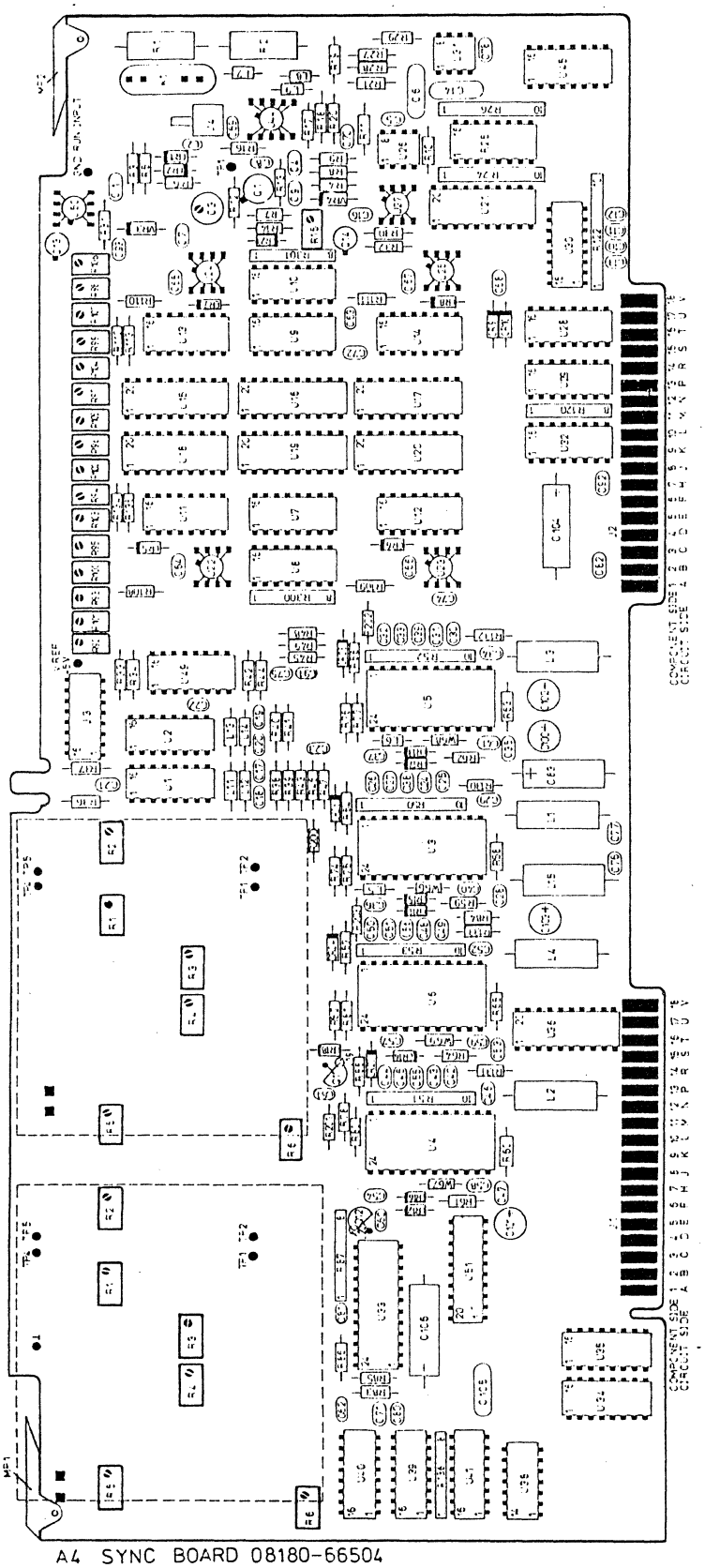


Figure 3-55. A4 Sync Board

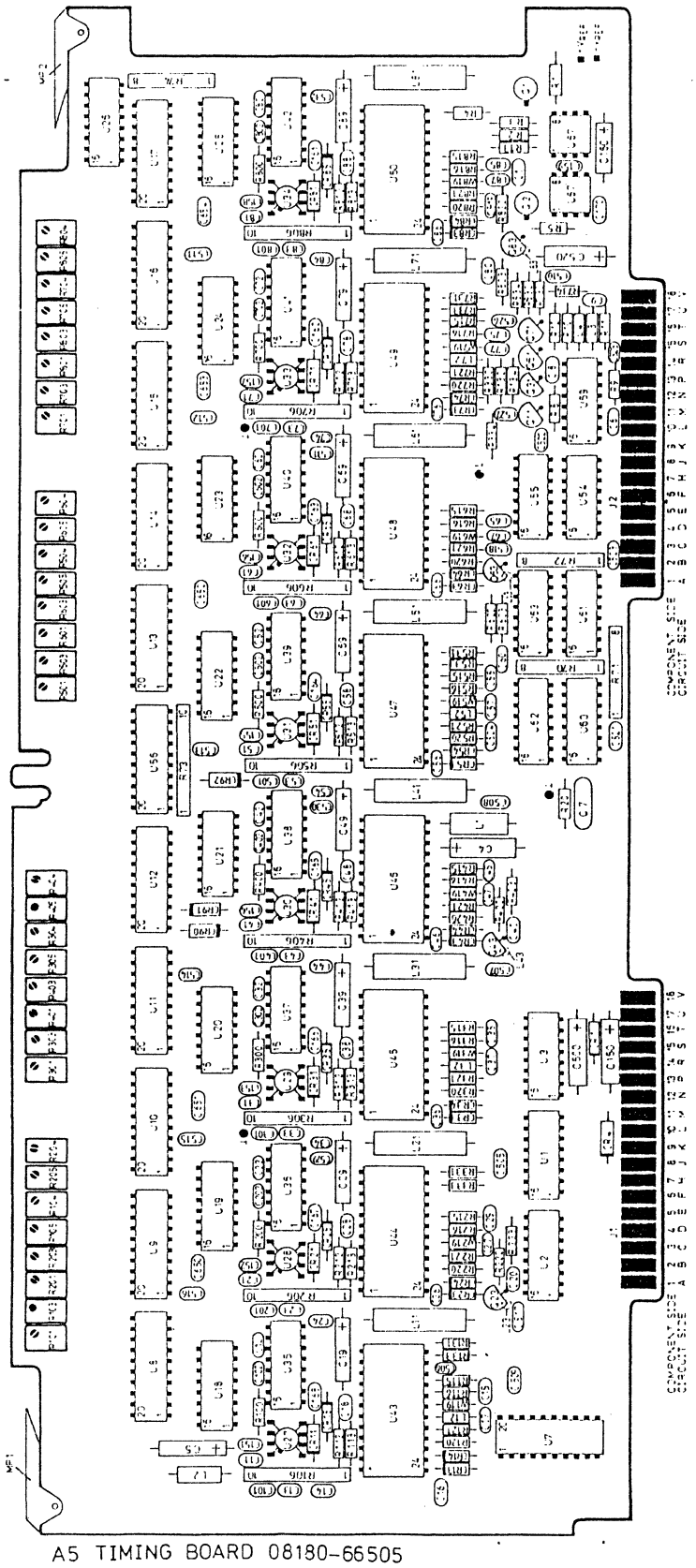


Figure 3-56. A5 Timing Board

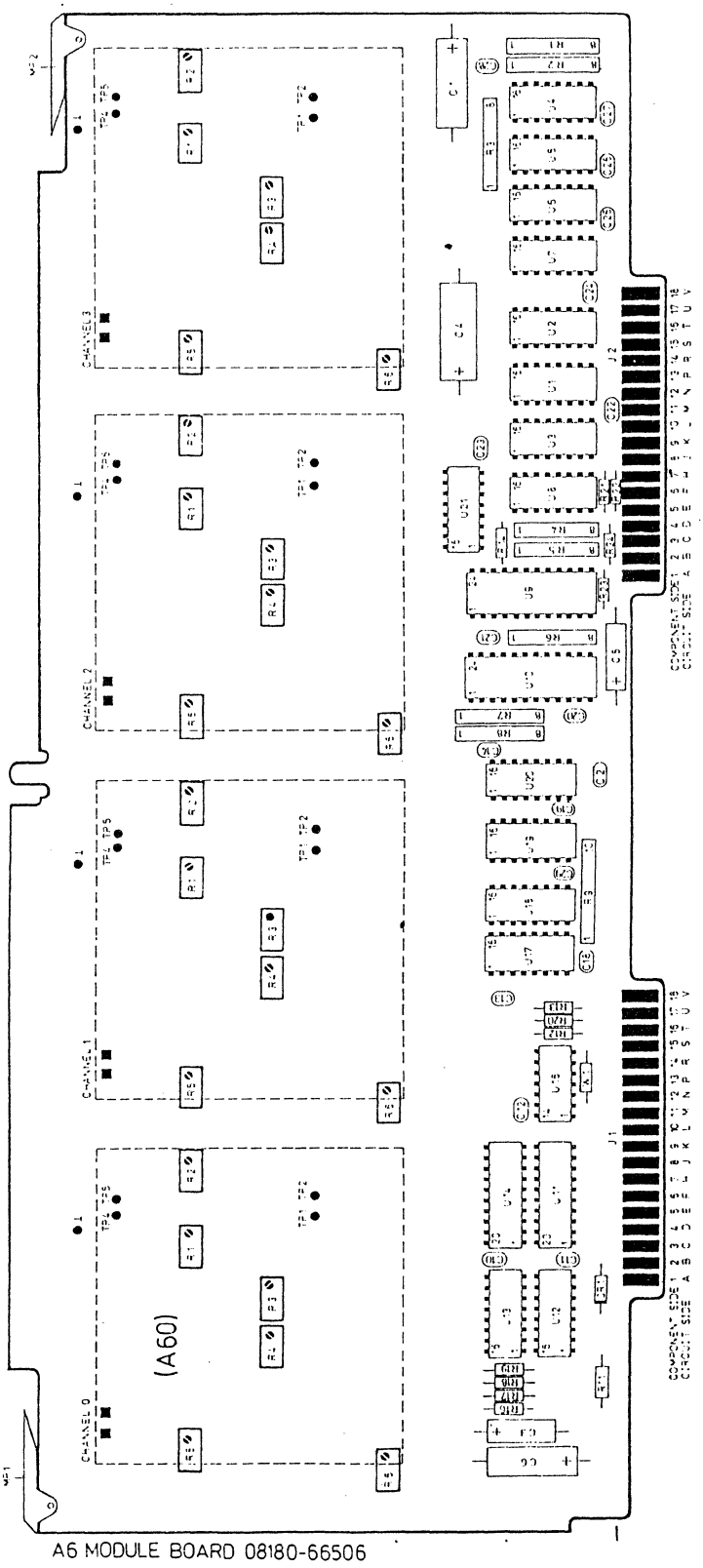


Figure 3-57. A6 Module Board

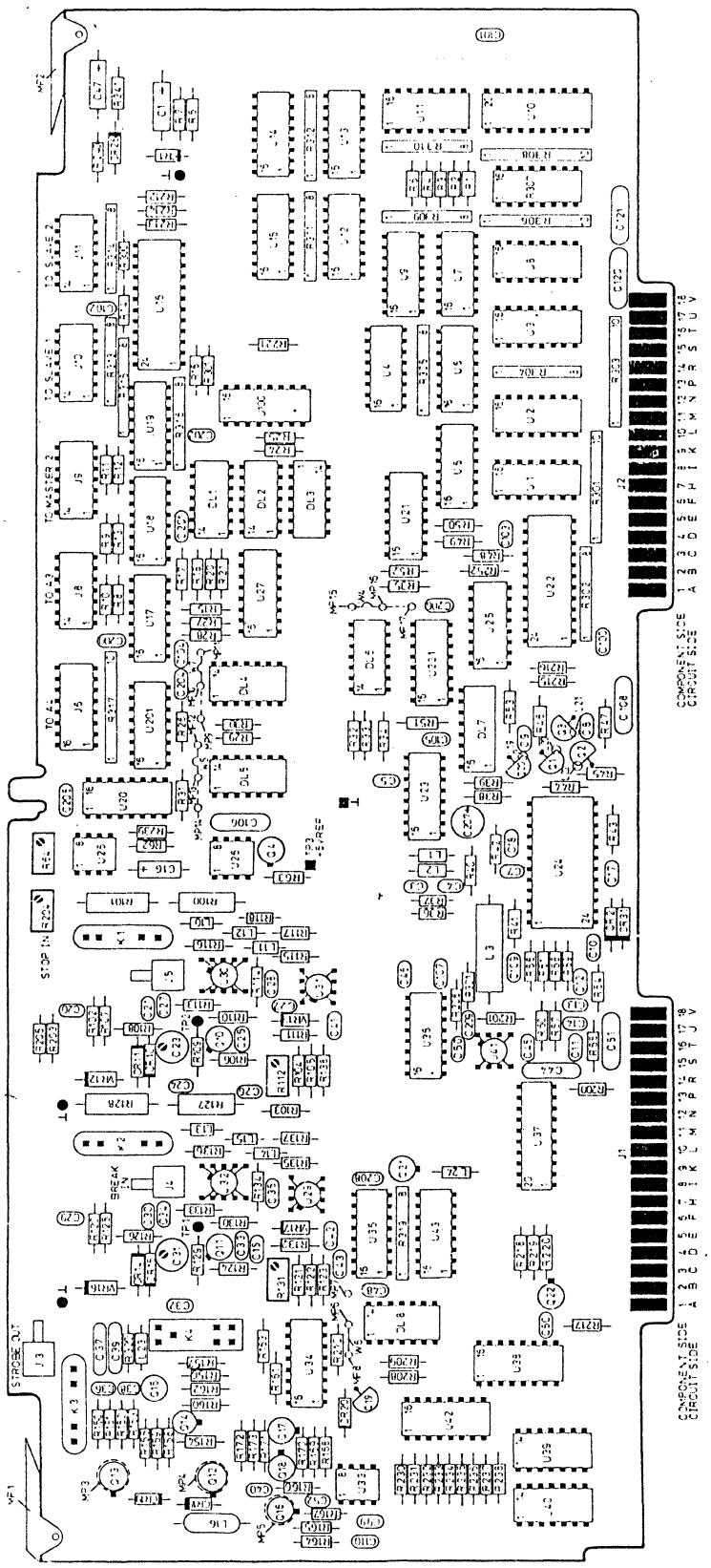


Figure 3-58. A8 Address Control II Board

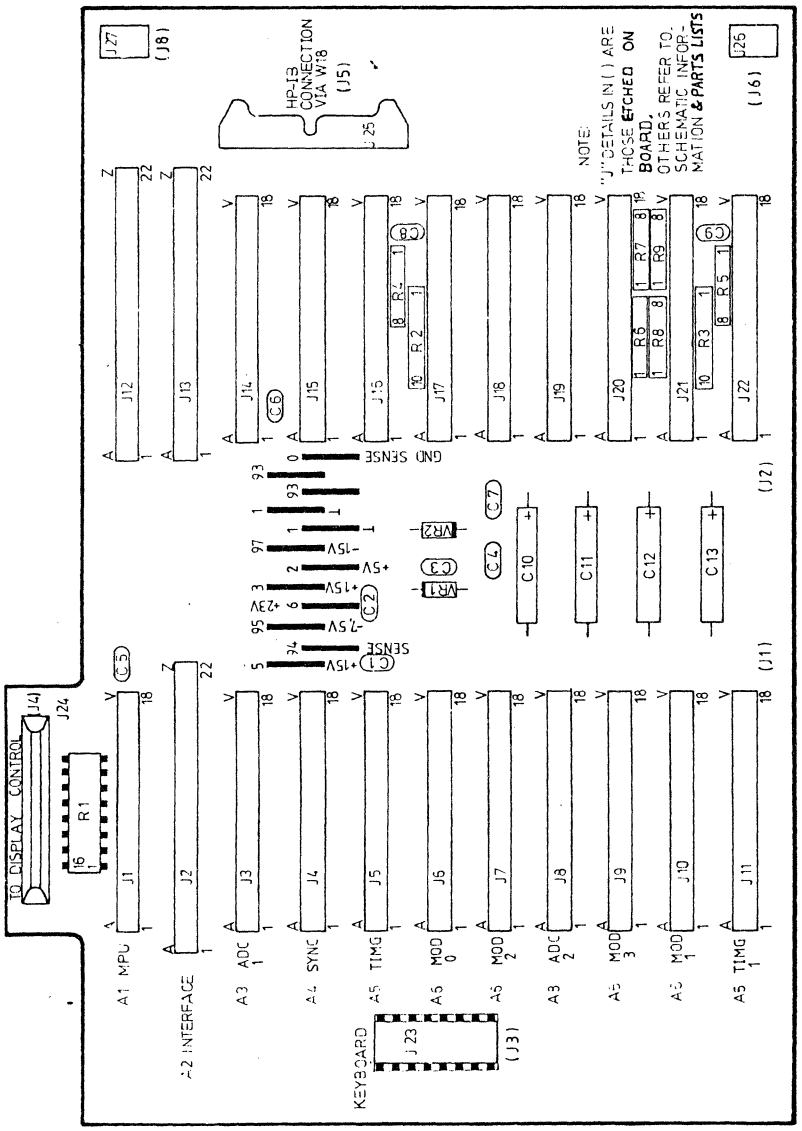
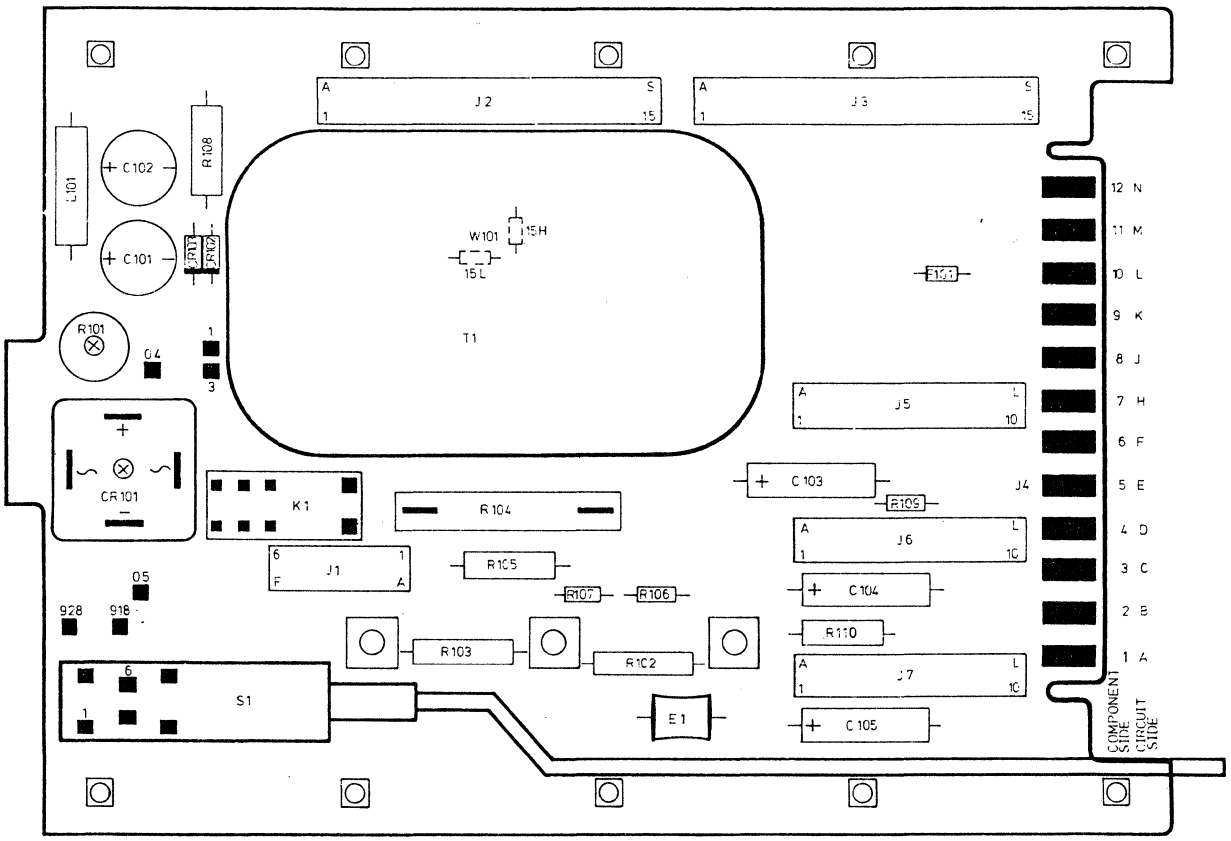
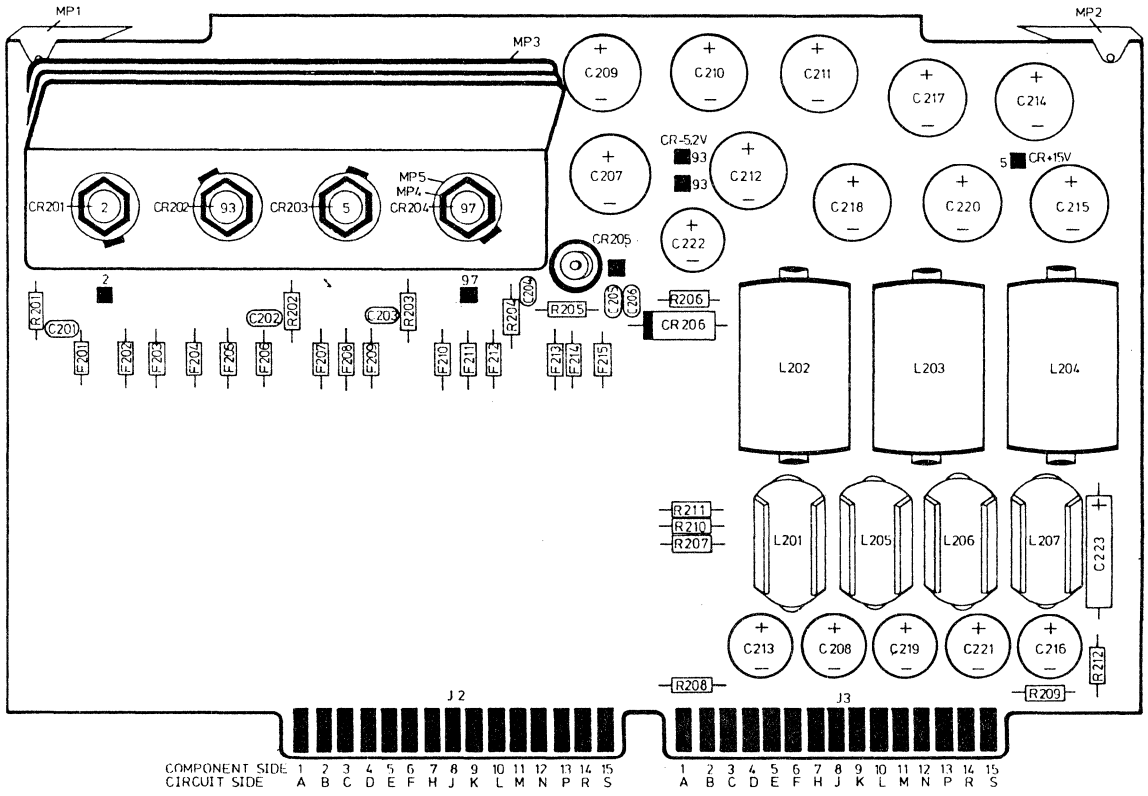


Figure 3-59. A12 Motherboard



A 21 MOTHERBOARD POWER SUPPLY 08180-66521

Figure 3-60. A21 Power Supply Module



A 22 RECTIFIER BOARD 08180-66522

Figure 3-61. A22 Rectifier Board

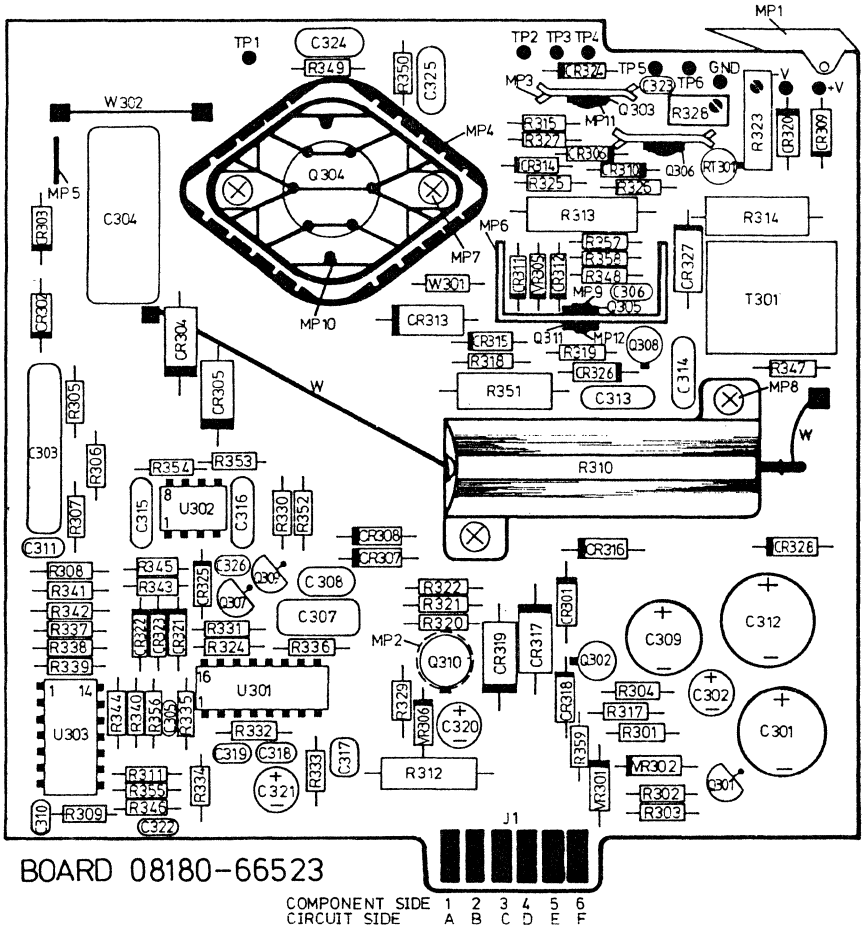


Figure 3-62. A23 Switching Board

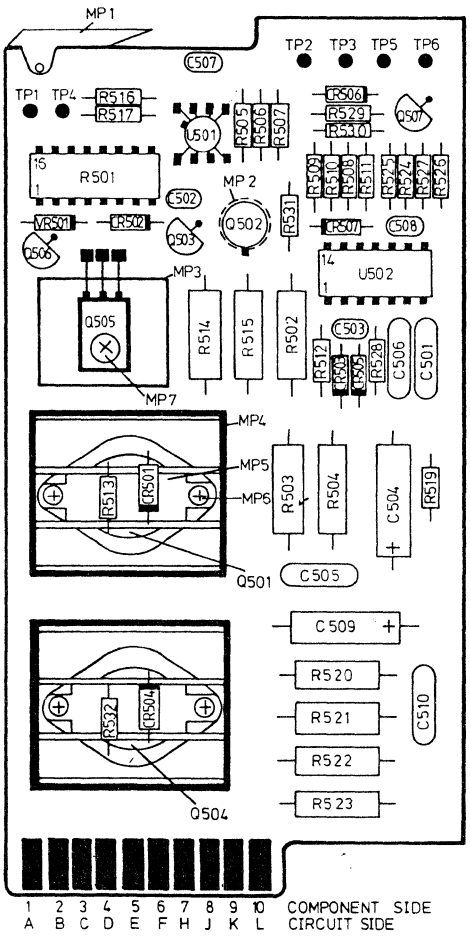


Figure 3-63. A25 Post Regulator Board

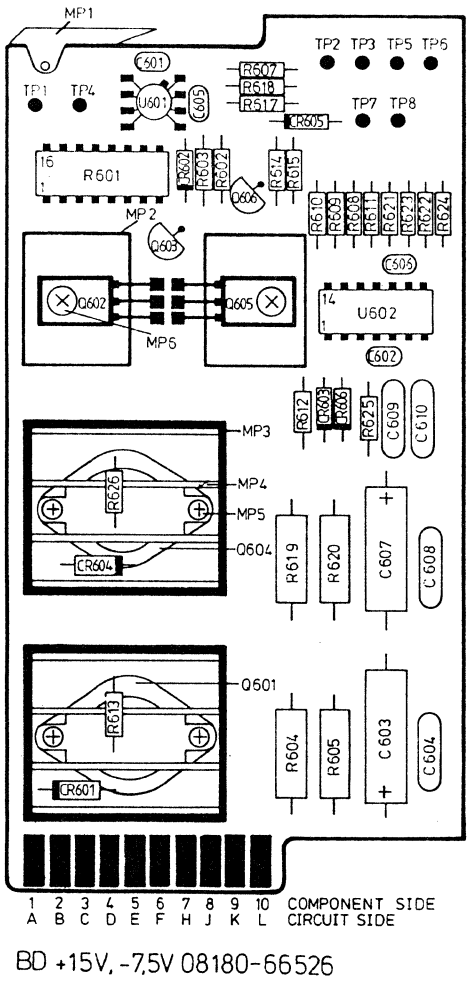
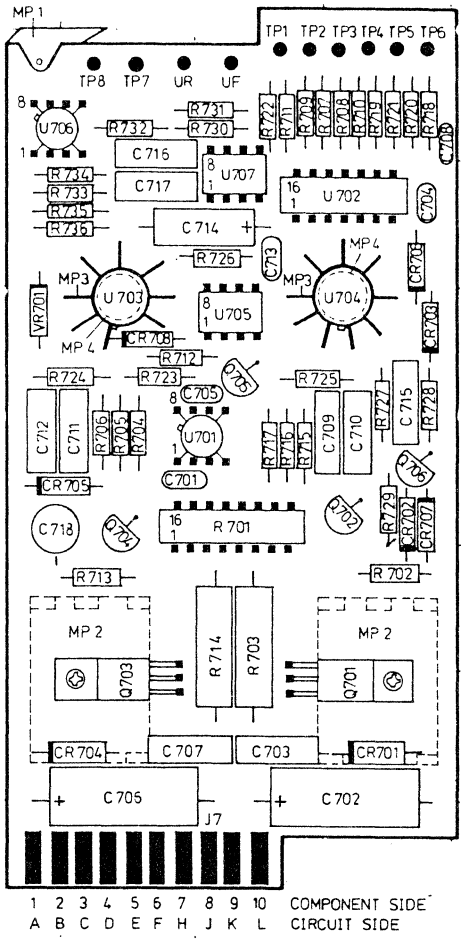


Figure 3-64. A26 Post Regulator Board



A27 +23V, -15V REGULATOR-BOARD 08180-66527

Figure 3-65. A27 Post Regulator Board

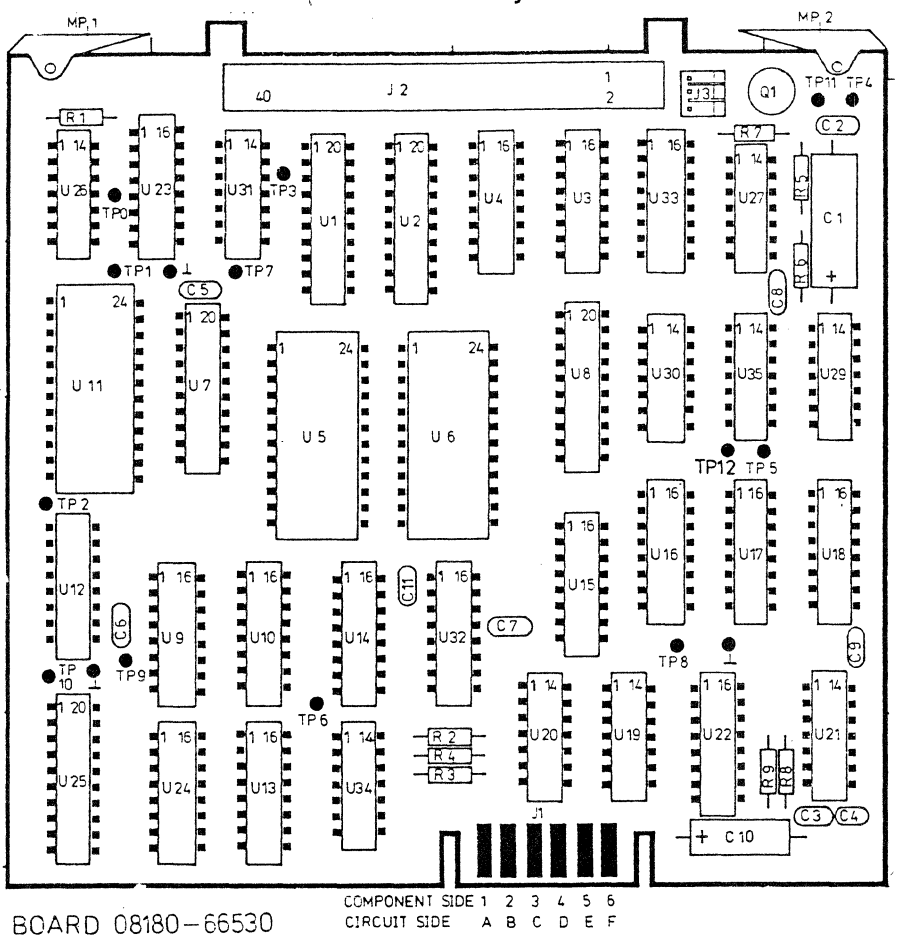


Figure 3-66. A30 Control - Board

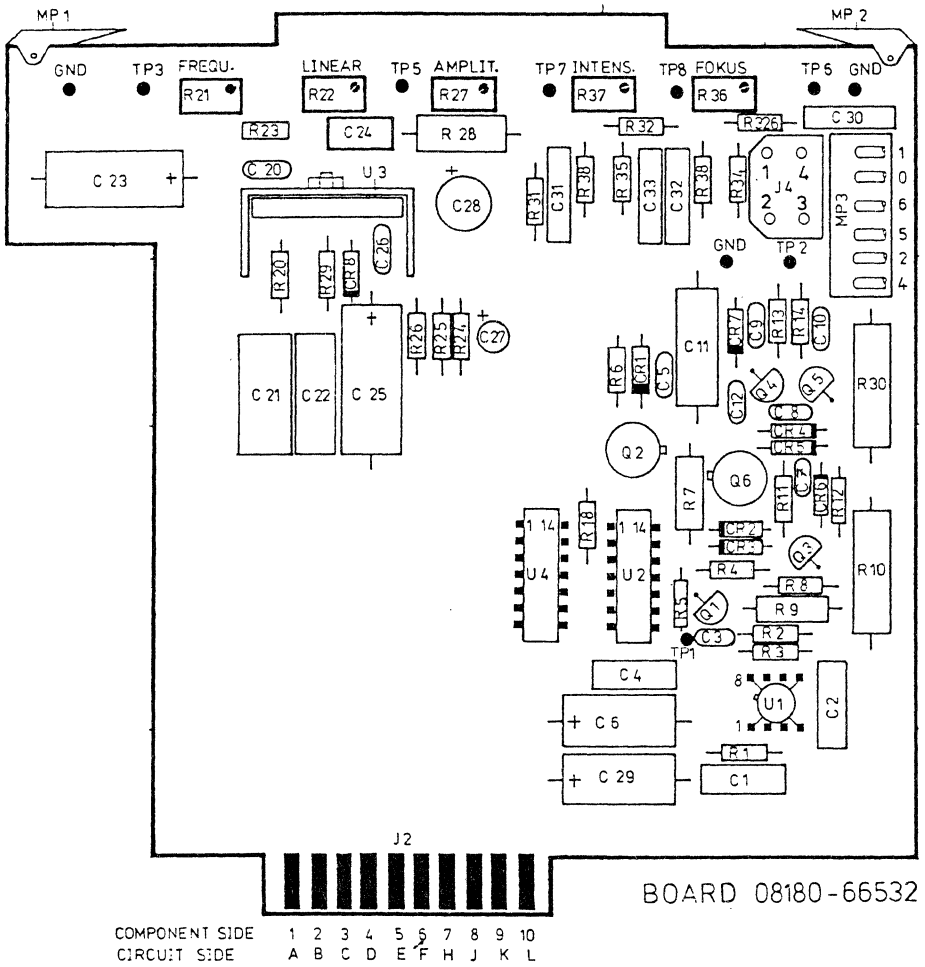
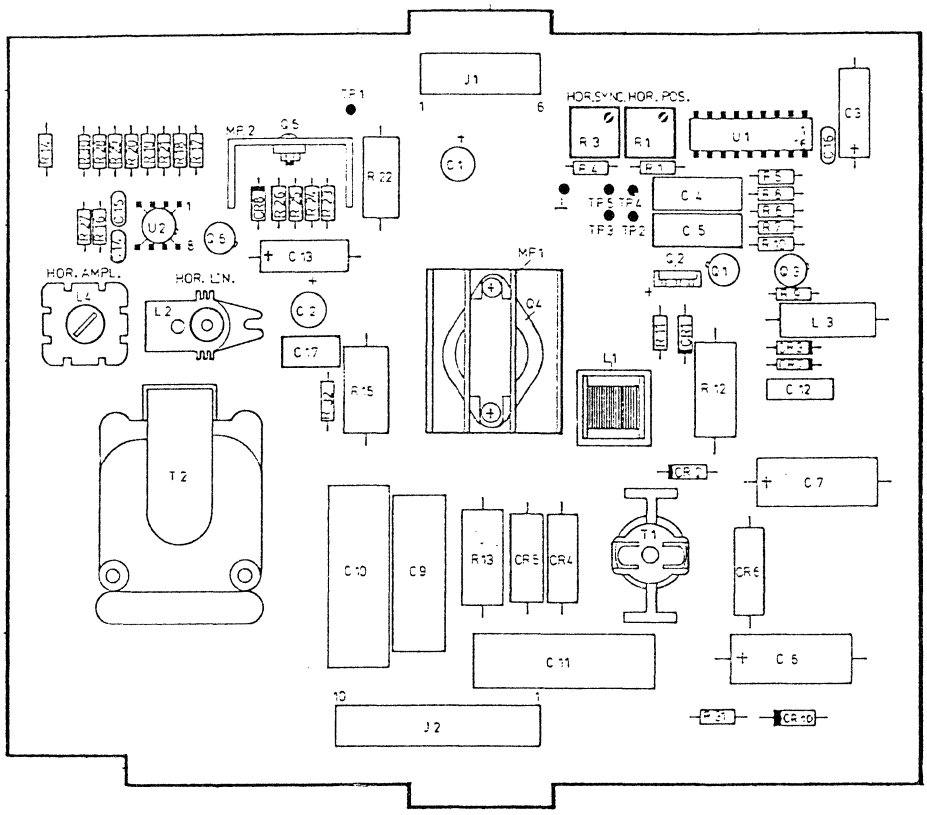


Figure 3-67. A32 Vertical Deflection Board



HIGH VOLTAGE-BOARD 08180-66534

Figure 3-68. A34 High Voltage Board

Chapter 4
8181A/B Adjustment Procedures

4-1 Introduction

This chapter deals with the adjustment procedures that need to be performed on the HP 8181A and HP 8181B generator extenders.

When doing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

NOTE

When performing power supply adjustment please refer to Chapter 3, section 3-2.
When performing Output Amplifier Adjustment please refer to Chapter 3, section 3-8.

NOTE

When adjusting the 8181A, section 4-3 PHI 2 Adjustment must be carried out before performing section 4-2 Extender Delay Adjustment.

4-2 Extender Delay Adjustment

Equipment:

Scope	
54100D Active pods	HP 54001A
Data Cable Set	HP 15423A
Strobe/Clock Cable Set	HP 15422A
BNC adapter	HP 15409A
BNC scope probe adapter	1250-1454
BNC adapter female/female	1250-0080
50 Ohm feedthrough	HP 10100C
Adjustment cover	08180-04103

NOTE

Before making any adjustments on the 8181A/B make sure that adjustments on the 8180A/B have completed. Allow instruments to warm up for 30 minutes.

Measurement setup:

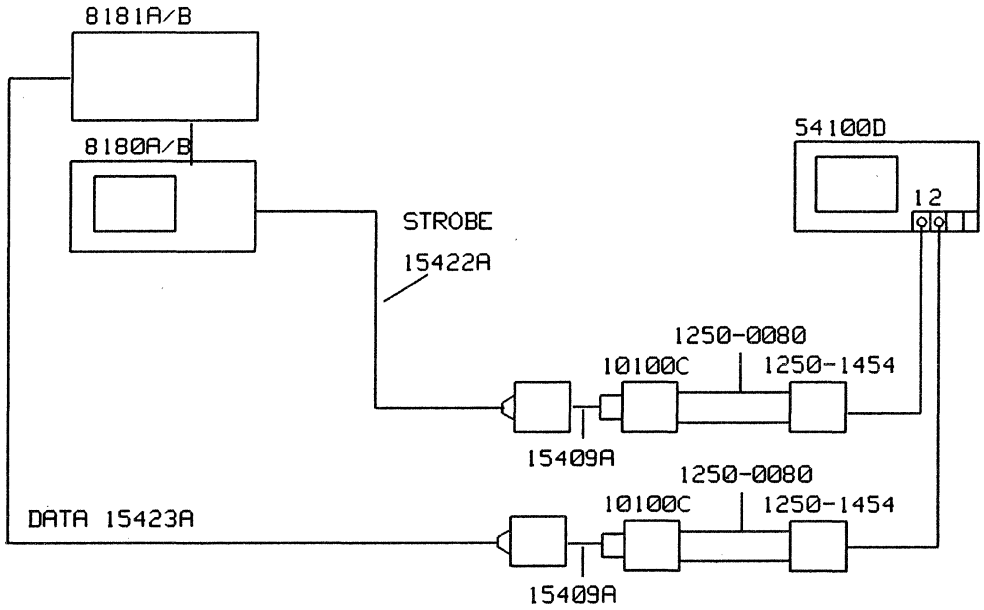


Figure 4-1. Equipment Setup - Delay Adjustment

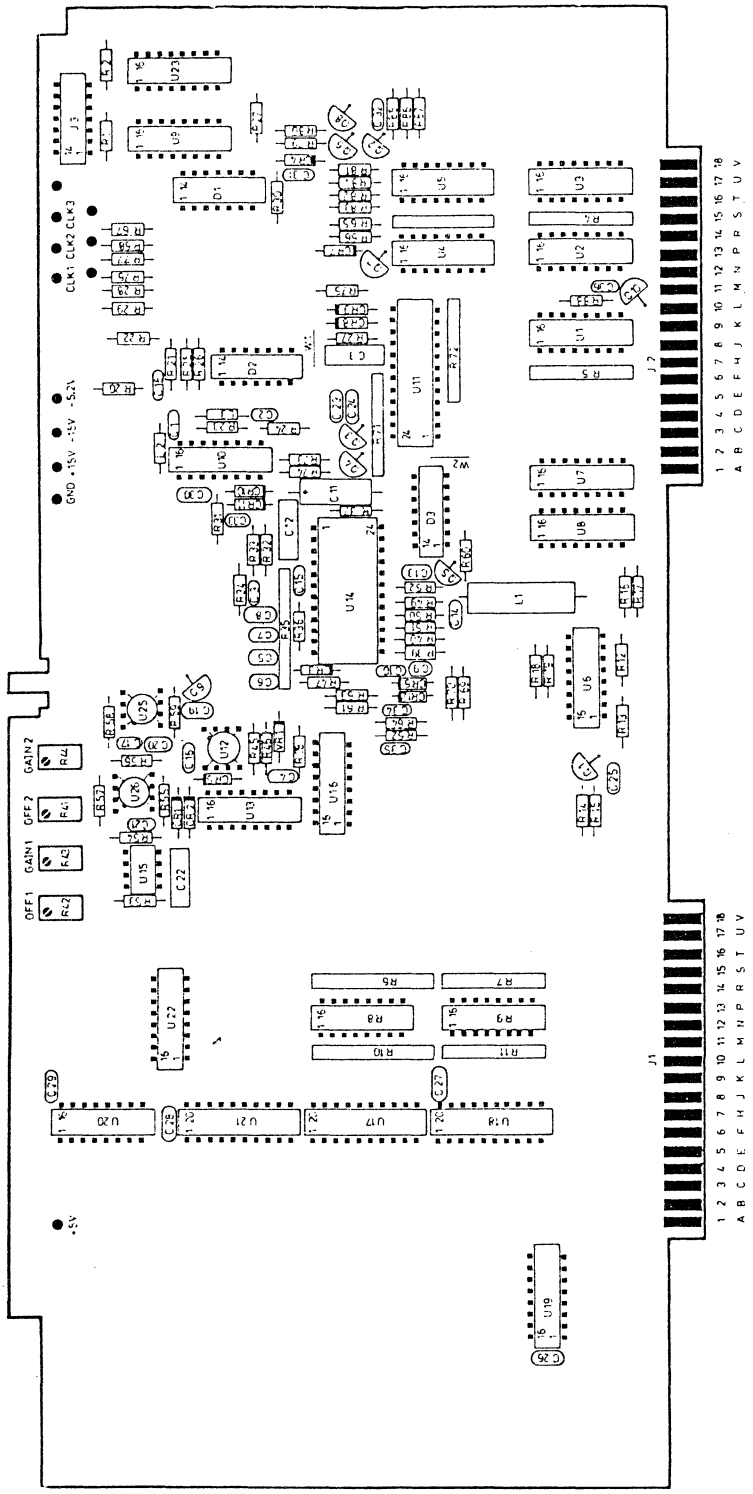


Figure 4-2. ADC3 Address Control Board

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Label A TTL Levels: (Pages > Output > Level > Next Label[to Label A] > TTL Level > Execute)
3. Strobe Level TTL: (Pages > Outout > Strobe Level > TTL)
4. Frequency 600 KHz: (Pages > Timing > Frequency > 600 > Kilohertz)
5. First Address 0; Last Address 1: (Pages > Control > Last Address > 1 > Enter Number)
6. Strobe Output to Data: (Pages > Control > Strobe Output > Data)
7. FAD Data and Strobe High; LAD Data and Strobe Low: (Pages > Data > 1 > F . . . [until all extender Data is set] > Cursor [to Strobe Addr. 1] > 0 . . . [for Strobe and Data channels])
8. Connect equipment as shown in the measurement set up and press RUN.

Preadjustment

9. Program extender delay to 990ns: (Pages > Timing > Extender 1[2] > 990 > Nanosec)
10. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split Screen to Off > Timebase > Sec/Div > 500ps > Delay > 990ns)
11. Adjust the positive going transition to 990ns with A8 R41.
12. Program extender delay to 90ns: (90 > Nanosec)
13. Set scope Timebase Delay to 90ns: (Timebase > Delay > 90ns)
14. Measure the time difference between the 50% point of the positive going transition and the center graticule line. Carry out the following steps:
    a) move tap on A8 DL3 (in 1 ns steps) so that the delay deviation is closest to 90ns (only for 8181A)
    b) adjust A8 DL3 to 90 ns (only for 8181B).

Final Adjustment

15.

Set Extender Delay to	Set scope Timebase Delay to	Adjust	Set positive transition to
0.0 ns	0 ns	A8 R42	0.0 ns
89.9 ns	89.0 ns	A8 R43	89.0 ns
90.0 ns	89.1 ns	A8 R41	89.1 ns
989 ns	980 ns	A8 R44	980 ns

Transition adjusted for 980 ns.

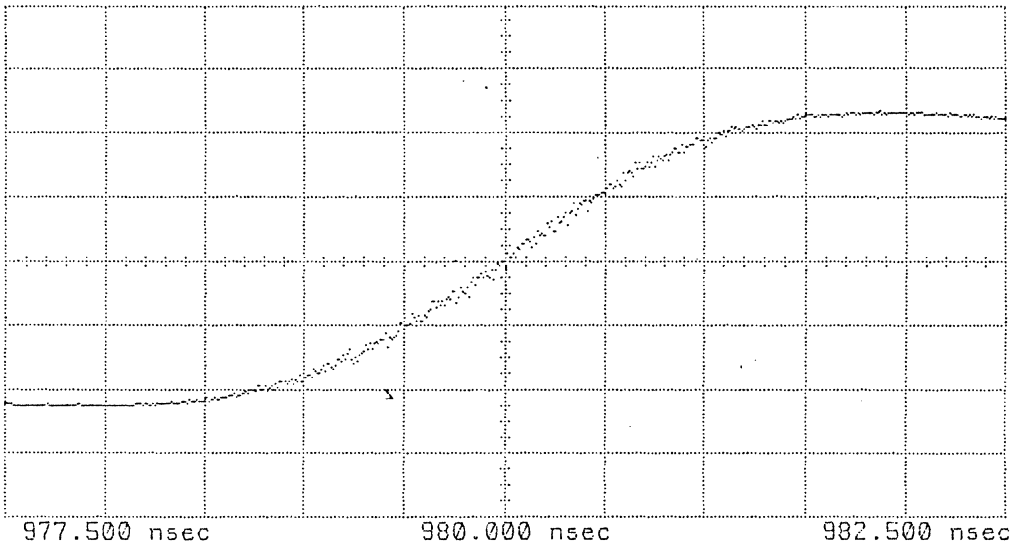


Figure 4-3. Extender Delay Adjustment

4-3 Multiplexer Board 08181-66501 (8181A)

PHI 2 Adjustment

Equipment:

Scope	54100D
Active pods	54001A

1. Connect channel A probe to A1 U4 pin 18 and channel B probe to testpoint PHI 2.
2. Set scope to: (Autoscale > Timebase > Sec/DIV > 50ns > Trigger > Trigger Mode to State Trigger On Negative Edge; On Chan 2; When Pattern H - X X)
3. Set Start Marker to 0ns; Stop Marker to 40ns: (Delta t > T Markers to On > Start Marker > 0ns > Stop Marker > 40ns >
4. Adjust with A1 R4 so that the trailing edge of the PHI 2 signal is 40ns ahead of the trailing edge of the tristate ramp as shown below.

NOTE

There is no PHI 2 adjustment on the 8181B Multiplexer Board.

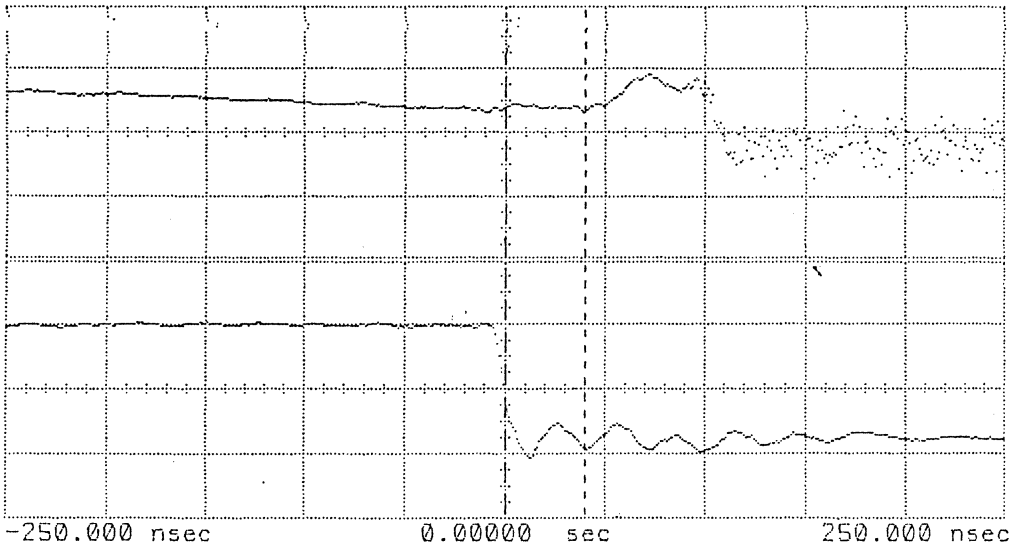


Figure 4-4. PHI 2 Adj

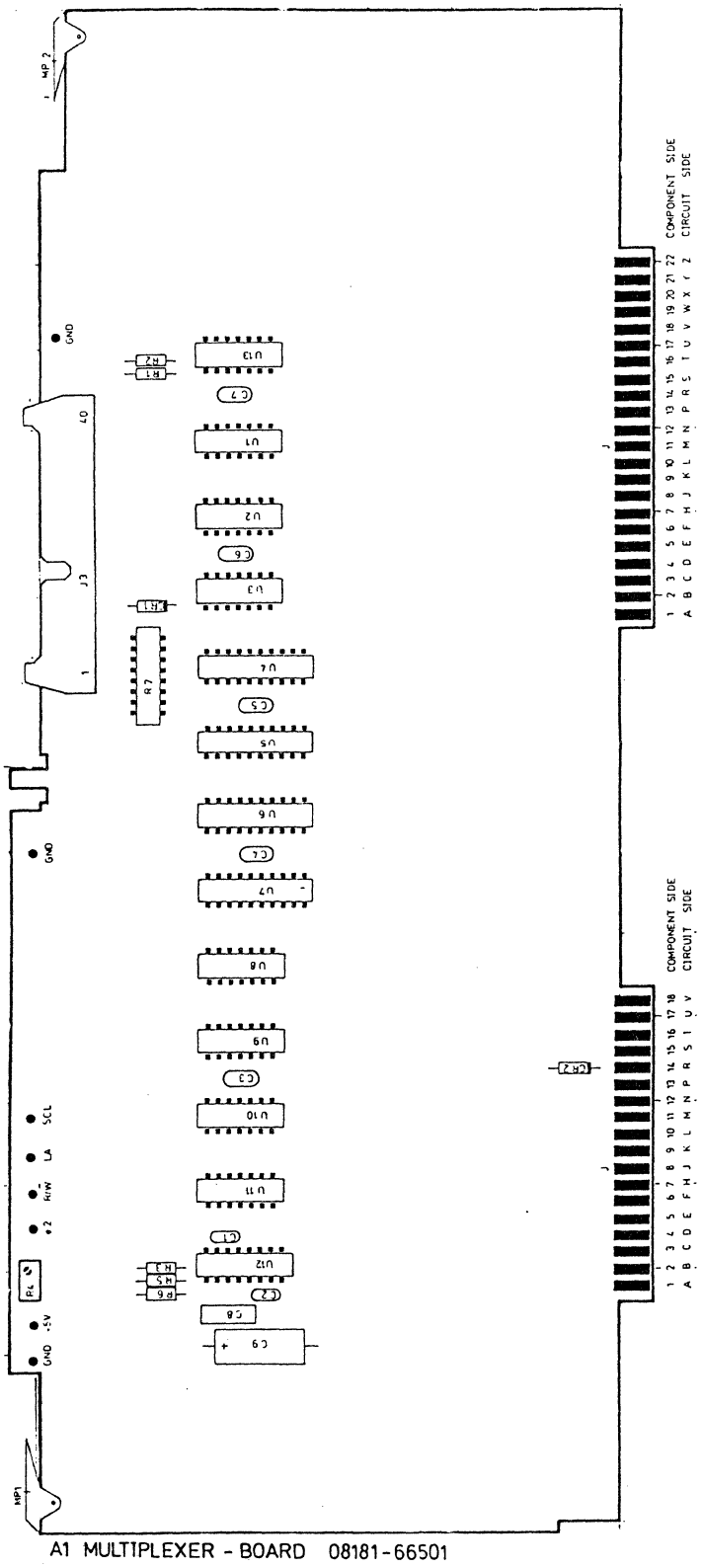


Figure 4-5. A1 Multiplexer Board

4-4 Locating Components in the 8181A Extender

The following diagrams are component/testpoint locators for the 8181A Data Extender.

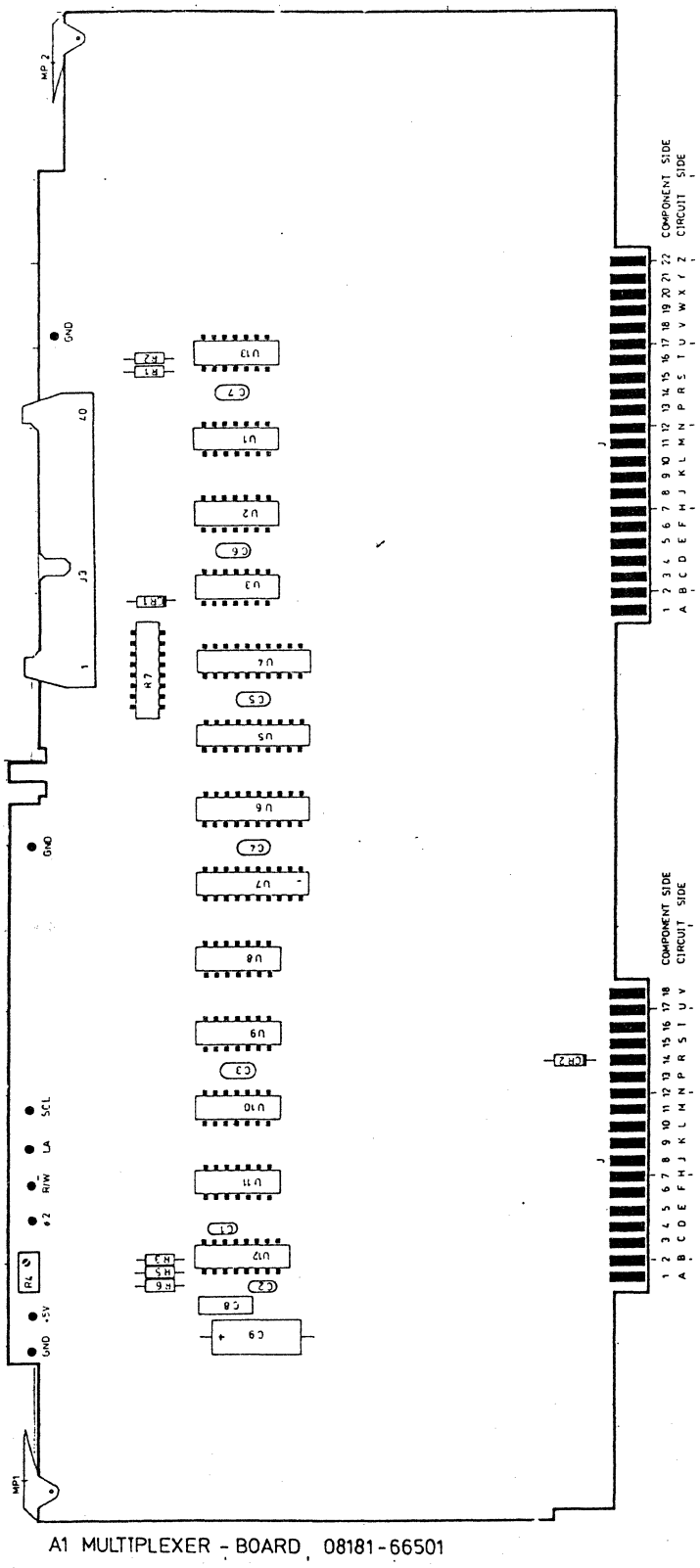


Figure 4-6. A1 Multiplexer Board

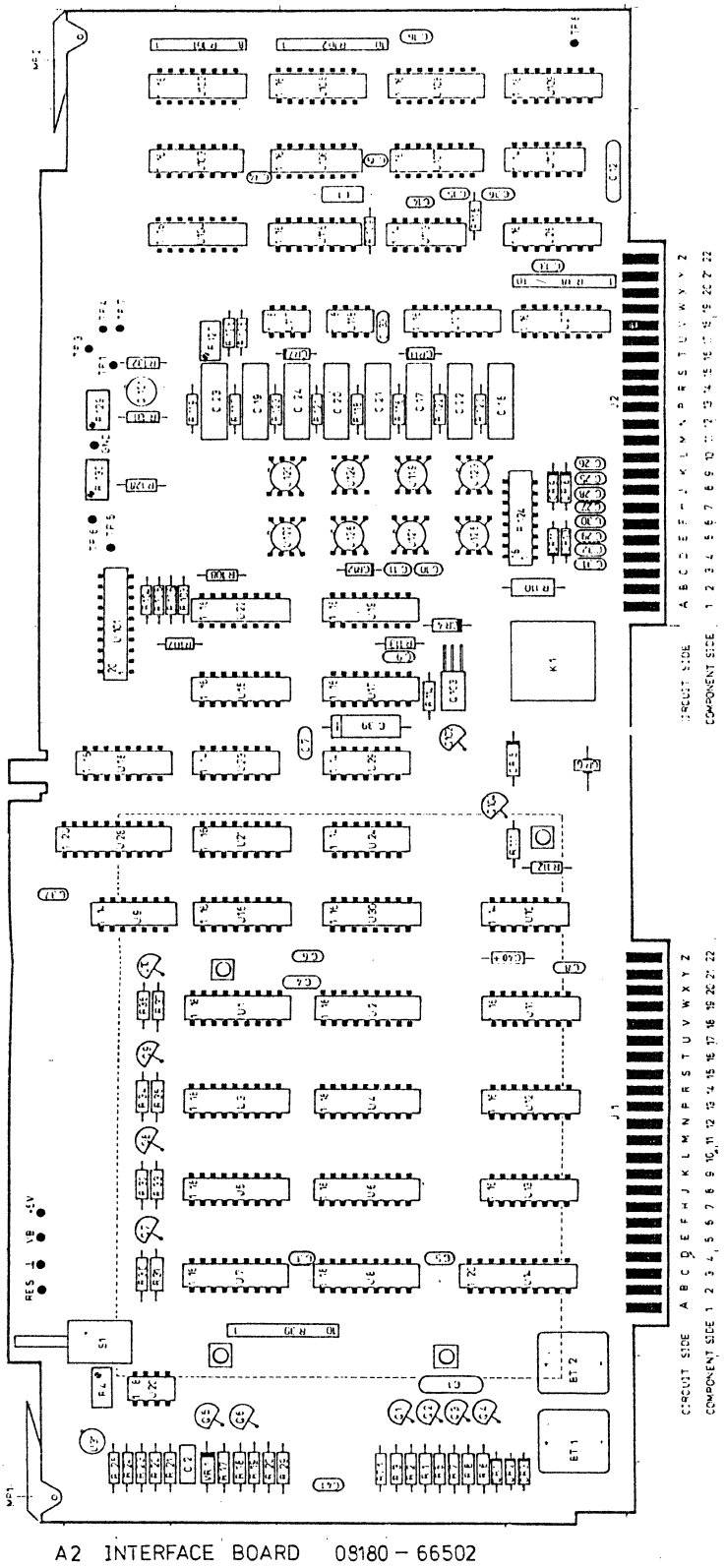


Figure 4-7. A2 Interface Board

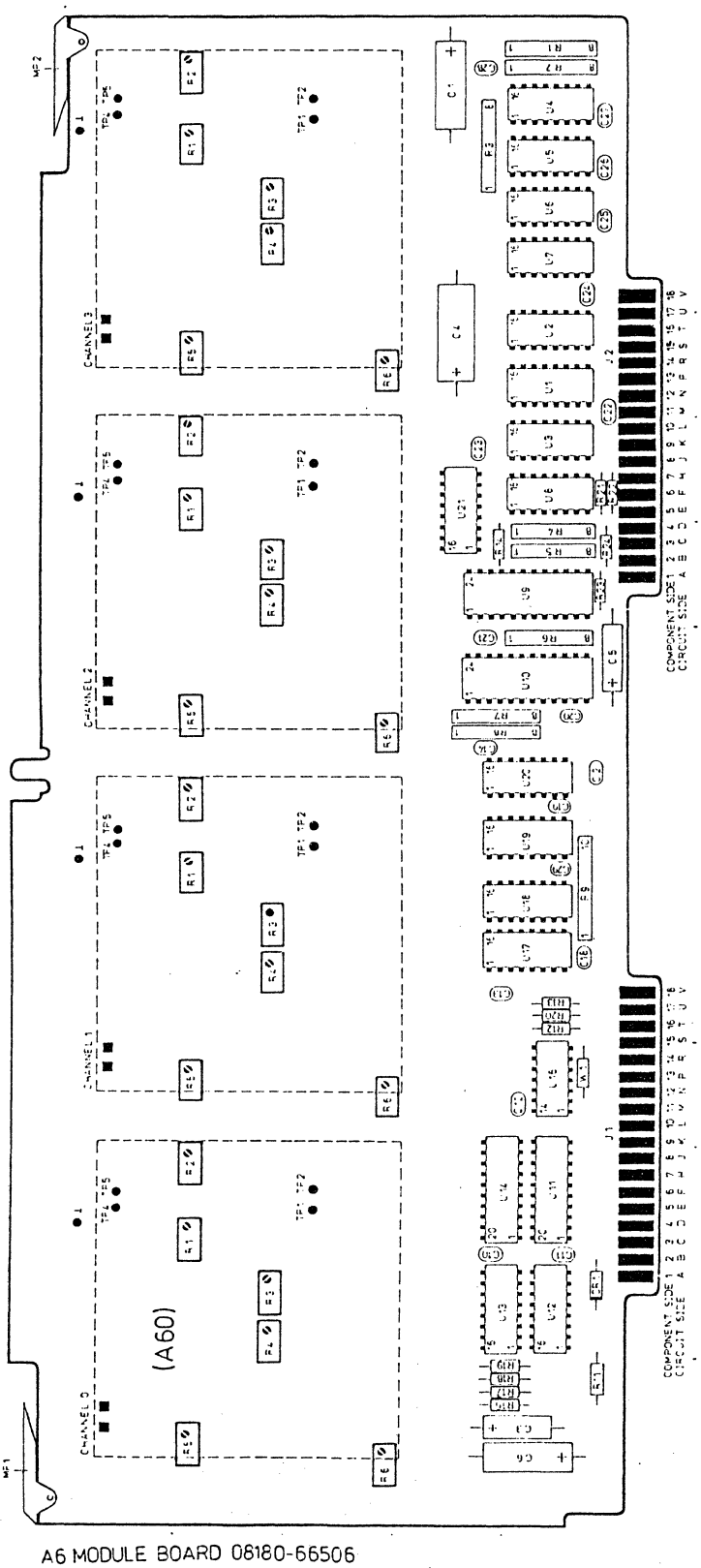


Figure 4-8. A6 Module Board

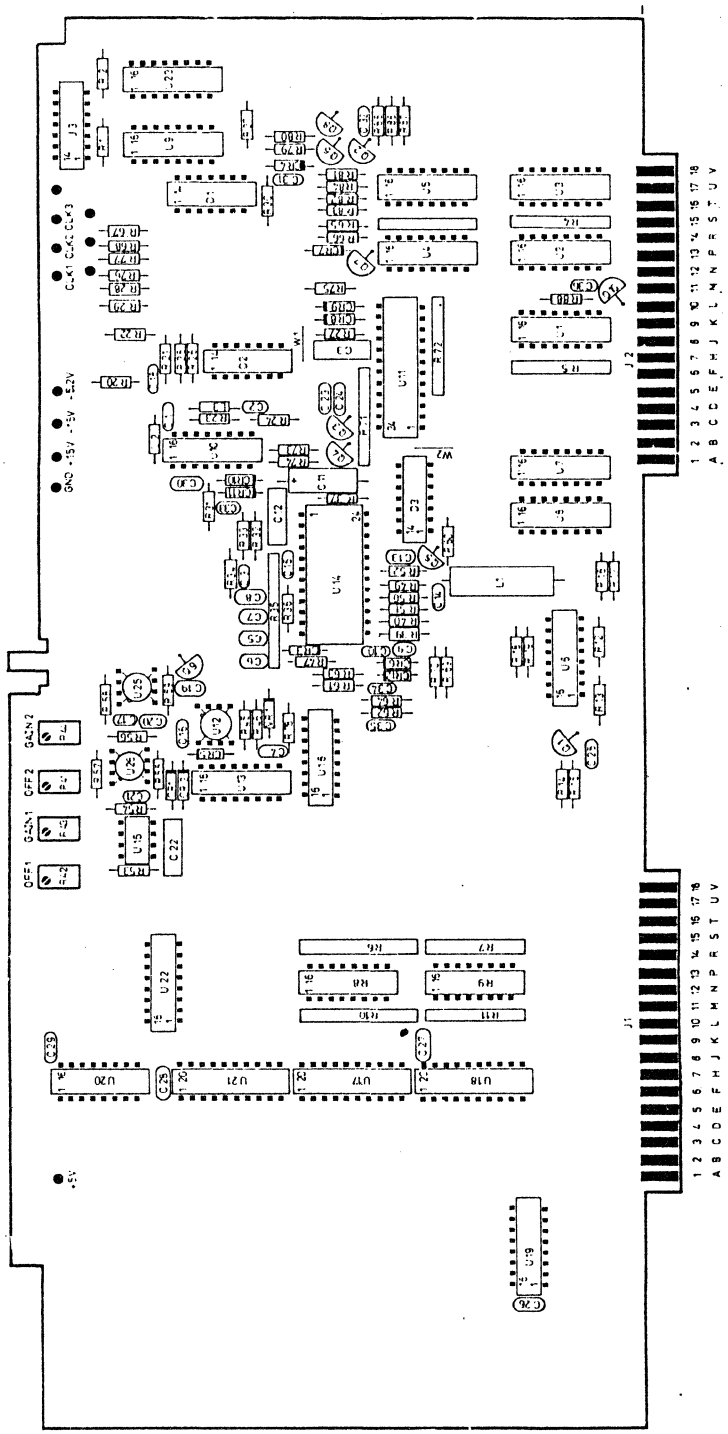
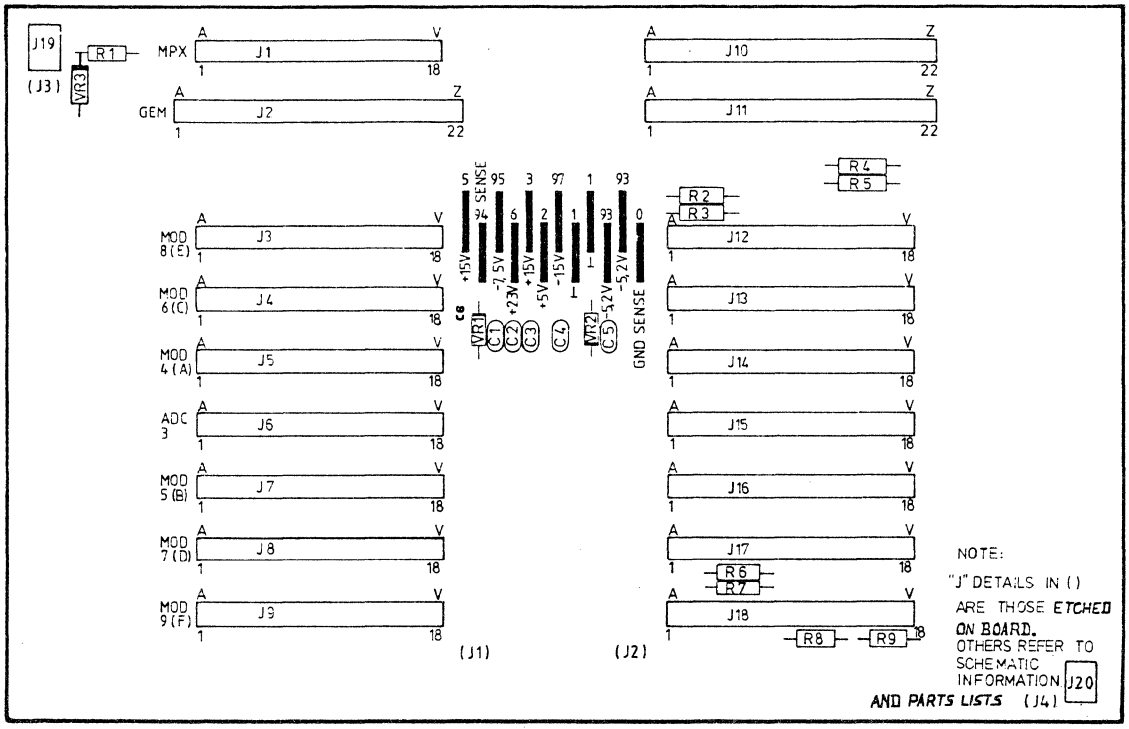
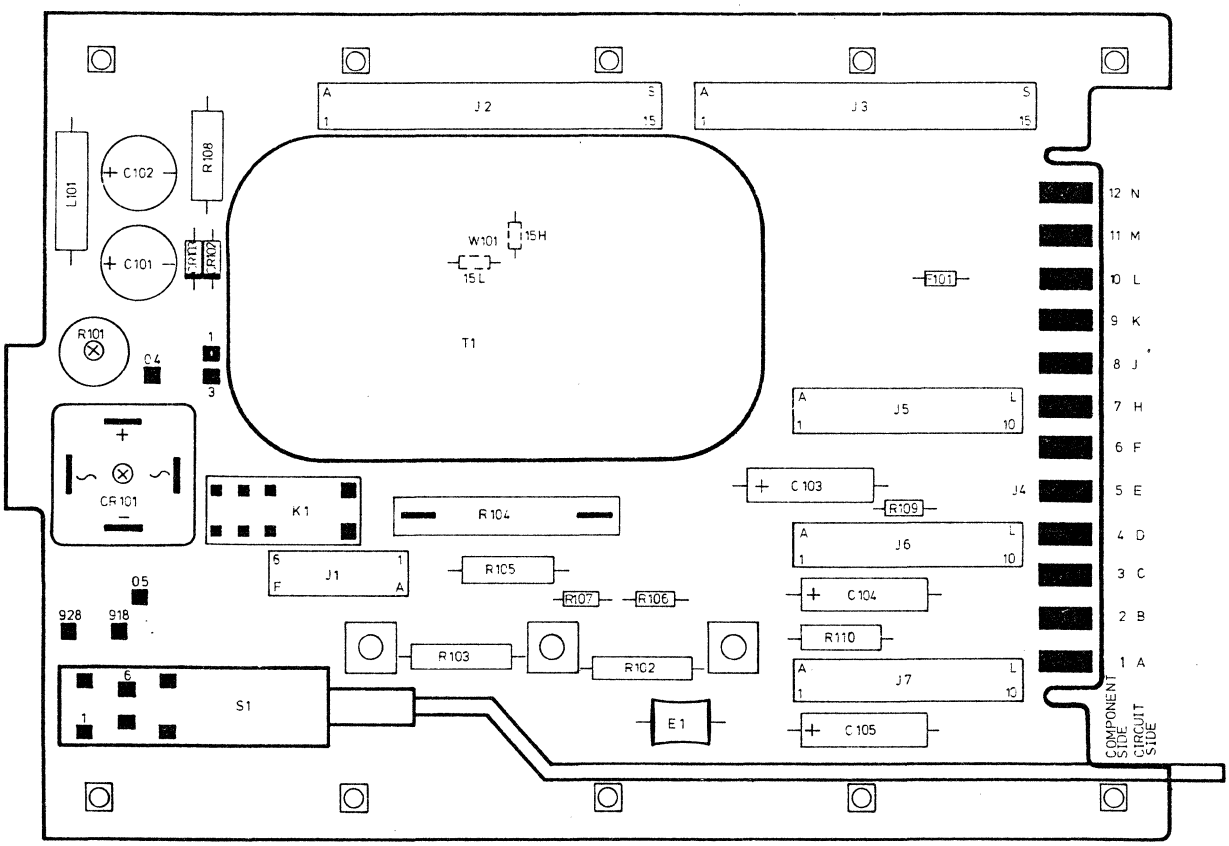


Figure 4-9. A8 Address Control III



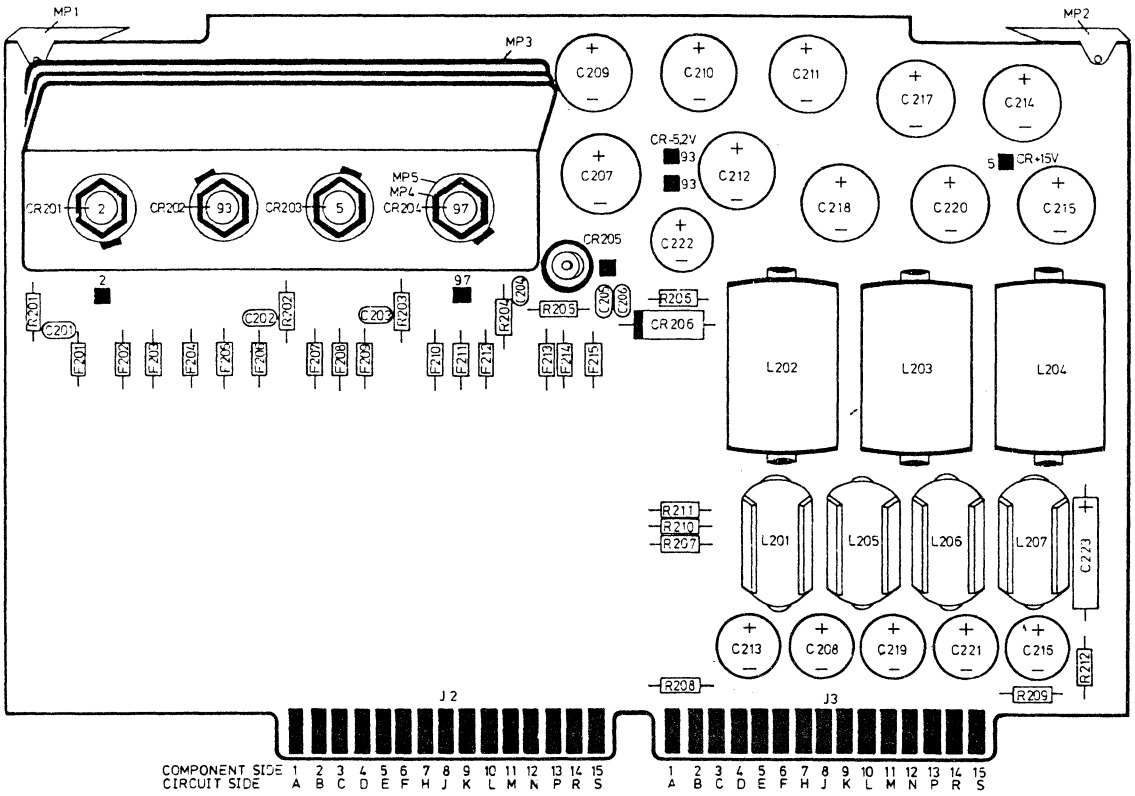
A12 MOTHERBOARD 08181-66512

Figure 4-10. A12 Mother Board



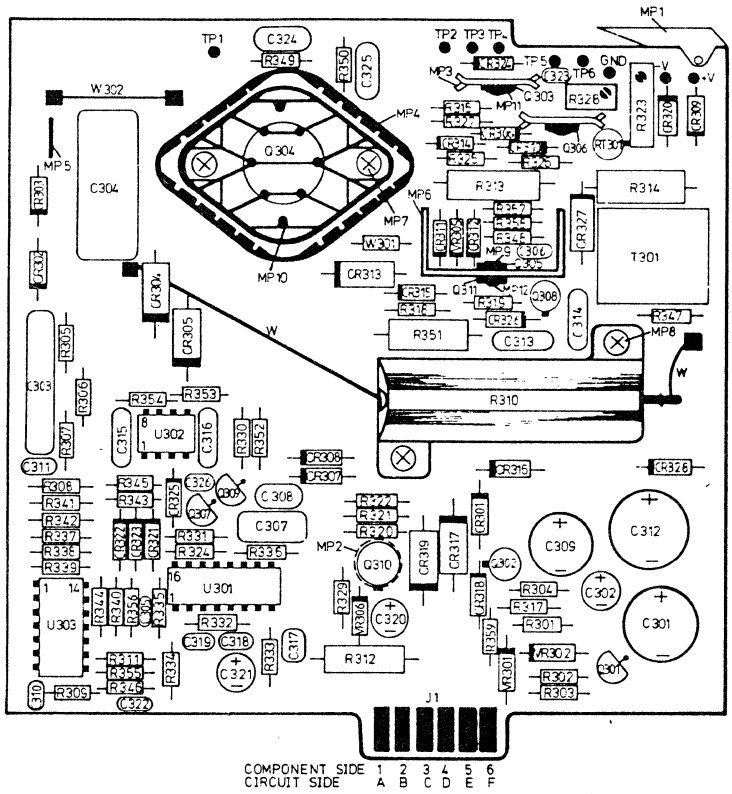
A 21 MOTHERBOARD POWER SUPPLY 08180-66521

Figure 4-11. A21 Power Supply Motherboard



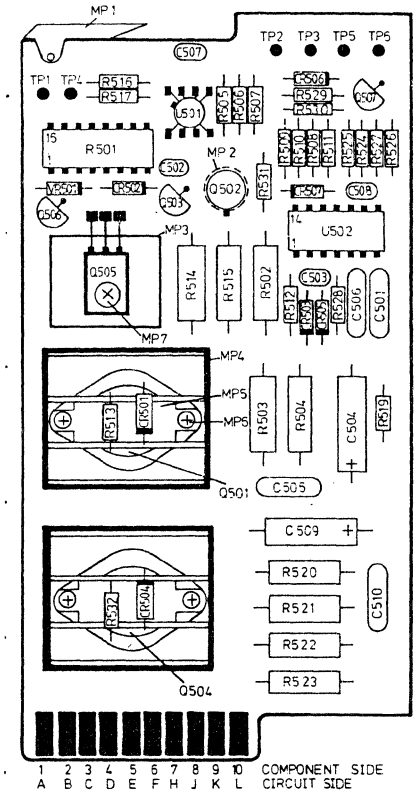
A 22 RECTIFIER BOARD 08180-66522

Figure 4-12. A22 Rectifier Board



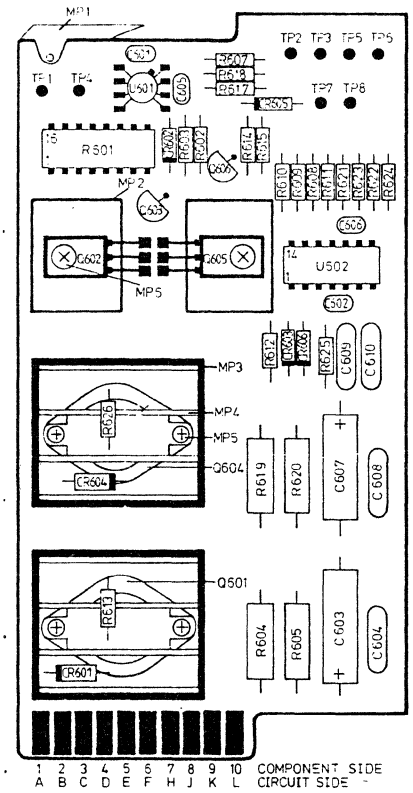
A 23 SWITCHING CONTROL BOARD 08180-66523

Figure 4-13. A23 Switching Board



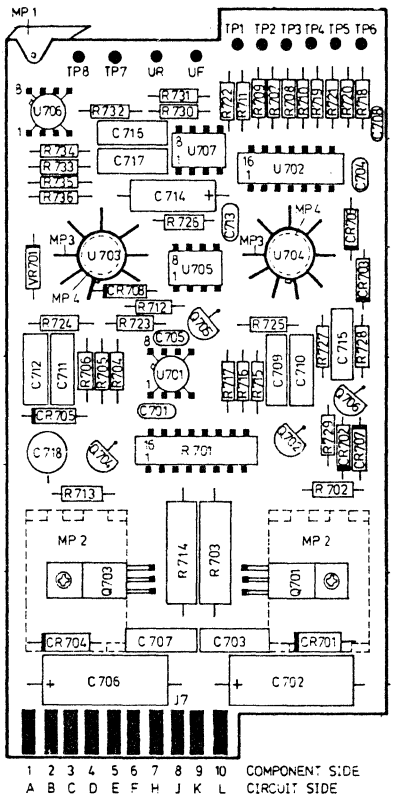
A 25 REGULATOR BD+5V,-5,2V 08180-66525

Figure 4-14. Post Regulator Board



A 26 REGULATOR BD +15V, -7,5V 08180-66526

Figure 4-15. A26 Post Regulator Board



A27 +23V, -15V REGULATOR-BOARD 08180-66527

Figure 4-16. A27 Post Regulator Board

Chapter 5
8182A/B Adjustment Procedures

5-1 Introduction

This chapter covers the adjustment procedures necessary for the HP 8182A and HP 8182B analyzers.

When performing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

5-2 Display Control Board 08182-66530 (8182A/B)

Display Adjustment

If the display has to be completely adjusted (after a CRT change), set A34R3 (on Motherboard) clockwise and all other potentiometers to mid range. Position the deflection yoke nearest to the screen and fasten it lightly.

1. Remove A32J4 (Vertical Deflection Board) and turn the instrument on.
2. If necessary, slightly increase intensity with A32R37.
3. Using the two ring magnets on the deflection yoke, position the dot approximately 3 mm (1/8 in) above the centre of the screen.
4. Turn the instrument off, reconnect A32 J4, turn it back on and press A1 (A61) S2.
5. Select the test pattern: (Pages > Miscellaneous > Right upper blank softkey > enter 8182 from the Data keys > Disp Adjust).
6. Adjust A32R21 (Freq.) for a stable display.
7. Center the test pattern with A34R1 (Hor. Pos.) and adjust A34L2 (Hor. Lin.) for maximum horizontal deflection.
8. Adjust A34R3 (Hor. Sync) so that no intensified lines appear.
9. Adjust A34L4 (Hor. Amp.) for approximately 12.5 cm (5 in) horizontal deflection.
10. Re-adjust A34L2 for best horizontal linearity.
11. Re-center the test pattern with A34R1 and repeat steps 8 to 10.
12. Adjust A32R27 (Vert. Amp.) for approximately 9 cm (3 1/2 in) vertical deflection.
13. Adjust A32R22 (Vert. Lin.) for best vertical linearity.
14. Re-adjust and fasten the deflection yoke and repeat steps 2 to 13, if necessary.
15. Correct any 'pin cushion' distortion by adding small correction magnets to the deflection yoke.

Intensity and Focus Adjustment

16. Press A1 (A61) S2 and select Brightness on the Miscellaneous Page: (Pages > Miscellaneous > Brightness > Increase [until maximum brightness is obtained]).

17. Adjust A32R37 (Intens.) until the line flyback is no longer visible.

18. Adjust A32R36 for the best possible focusing.

19. Secure the ring magnets, deflection yoke and correction magnets with silicon compound.

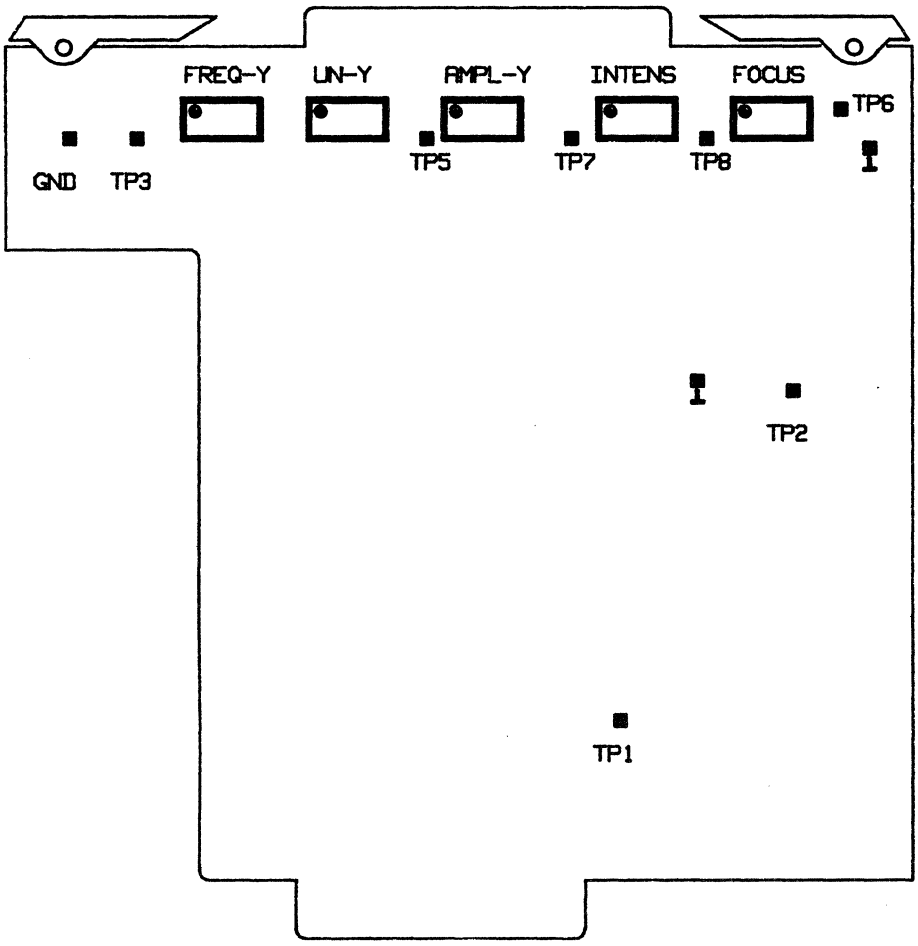


Figure 5-1. A32 Vertical Deflection Board

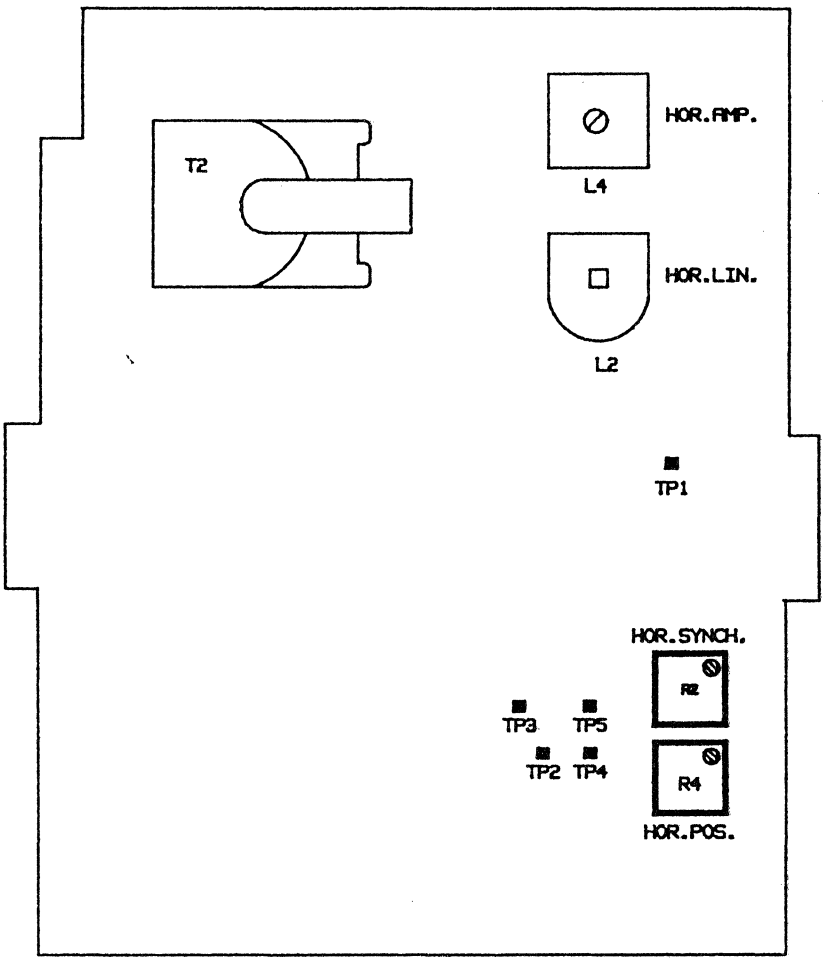


Figure 5-2 A34 High Voltage Board

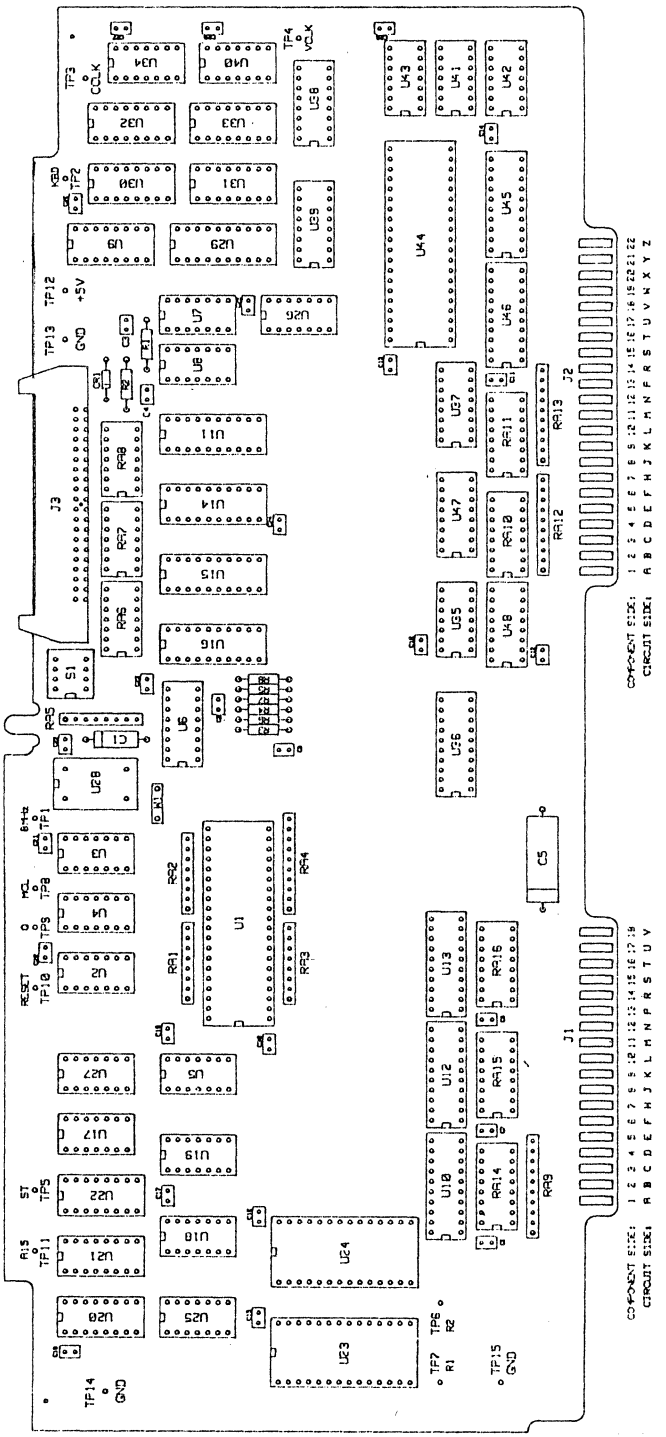


Figure 5-3. A61 Microprocessor Board

5-3 Microprocessor Board 08182-66501 (8182A)

Restart Circuit Adjustment

Equipment:

Oscilloscope with probes	HP 54100D
Digital Voltmeter, testleads	HP 3456A

1. Connect the DVM to VPower Down TP and GND TP.
2. Connect the oscilloscope probe to RES TP and GND TP.
3. Adjust A1 R133 for a 4.8V reading on the DVM. This simulates a decreasing supply voltage.
4. Adjust A1 R117 slowly until the RES signal toggles from high to low.
5. Recheck 4.8V and readjust A1 R133 and A1 R117 if necessary.
6. Turn A1 R133 fully clockwise and then slowly counter-clockwise until the RES signal toggles.
7. If the signal does not toggle at 4.8V ±0.002V repeat steps 3 to 6.
8. Turn A1 R133 back clockwise to get the normal supply voltage (< 5V) at the VPower Down TP.

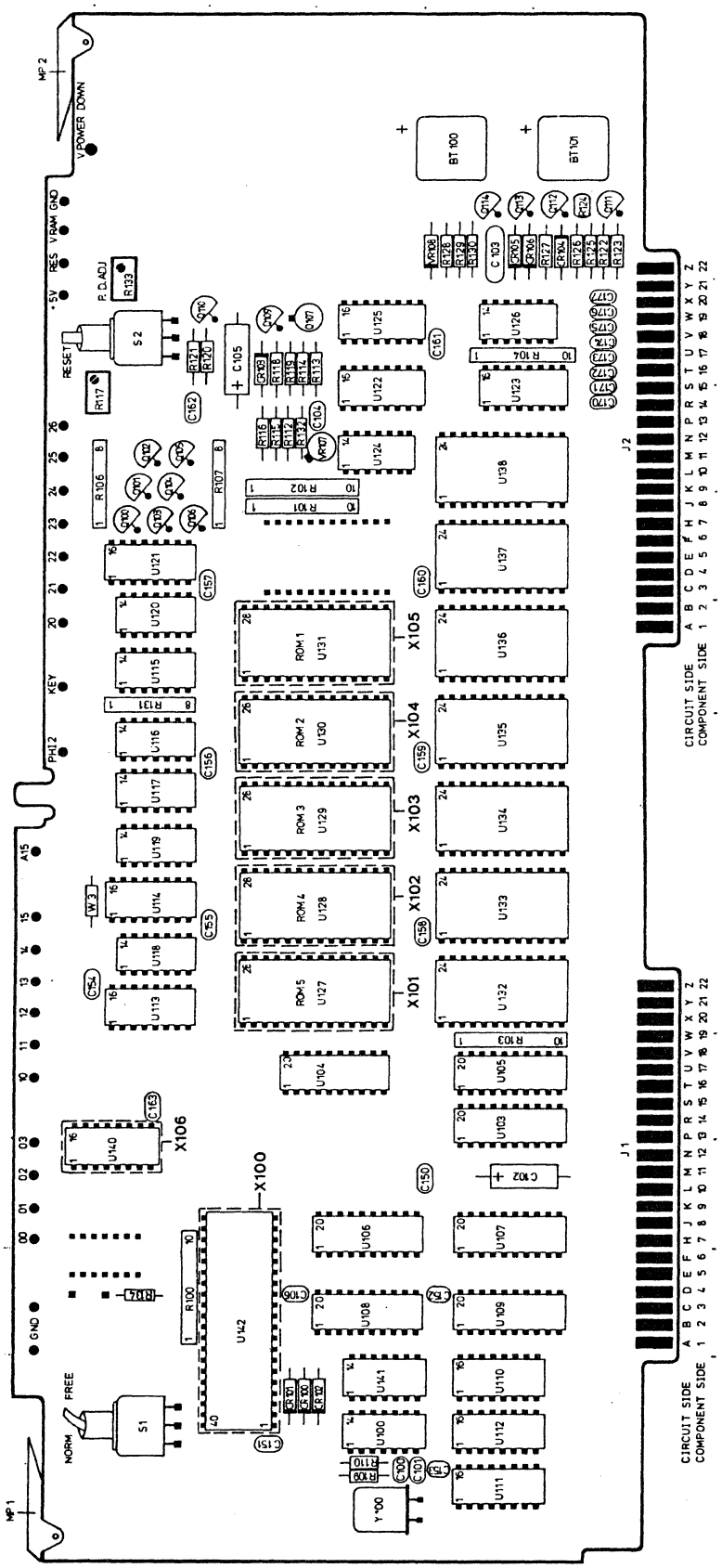


Figure 5-4. A1 Microprocessor Board

5-4 GEM Interface Board 08182-66502 (8182A) 08182-66562 (8182B)

Digital-Analog Converter Adjustment

Equipment:

Digital Voltmeter, testleads HP3456A

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Label A +10V: (Pages > Input > Threshold > 10 > Volt)
3. Connect DVM to A5 (A65) TP22 and the nearest GND TP on one of the A5 (A65) Data Boards.
4. Adjust A2 (A62) R115 for -5.000V.
5. Program Label A -10V: (-10 > Volt).
6. Adjust A2 (A62) R111 for +5.000V.
7. Recheck the voltage at A5 (A65) TP22 with threshold Label A programmed to +10V, 0V and -10V in turn. The voltages should be -5V ±3mV, 0V ±3mV, and +5V ±3mV respectively. Repeat steps 2 to 6 if necessary.

Internal Clock Generator Adjustment

Equipment:

Oscilloscope HP54100A

1. Program Clock Source Internal: (Pages > Control > Clock > Clock Source > Internal)
2. Connect the scope probe to A2 (A62) TP14 and GND TP and adjust A2 (A62) C124 for the cleanest waveform.

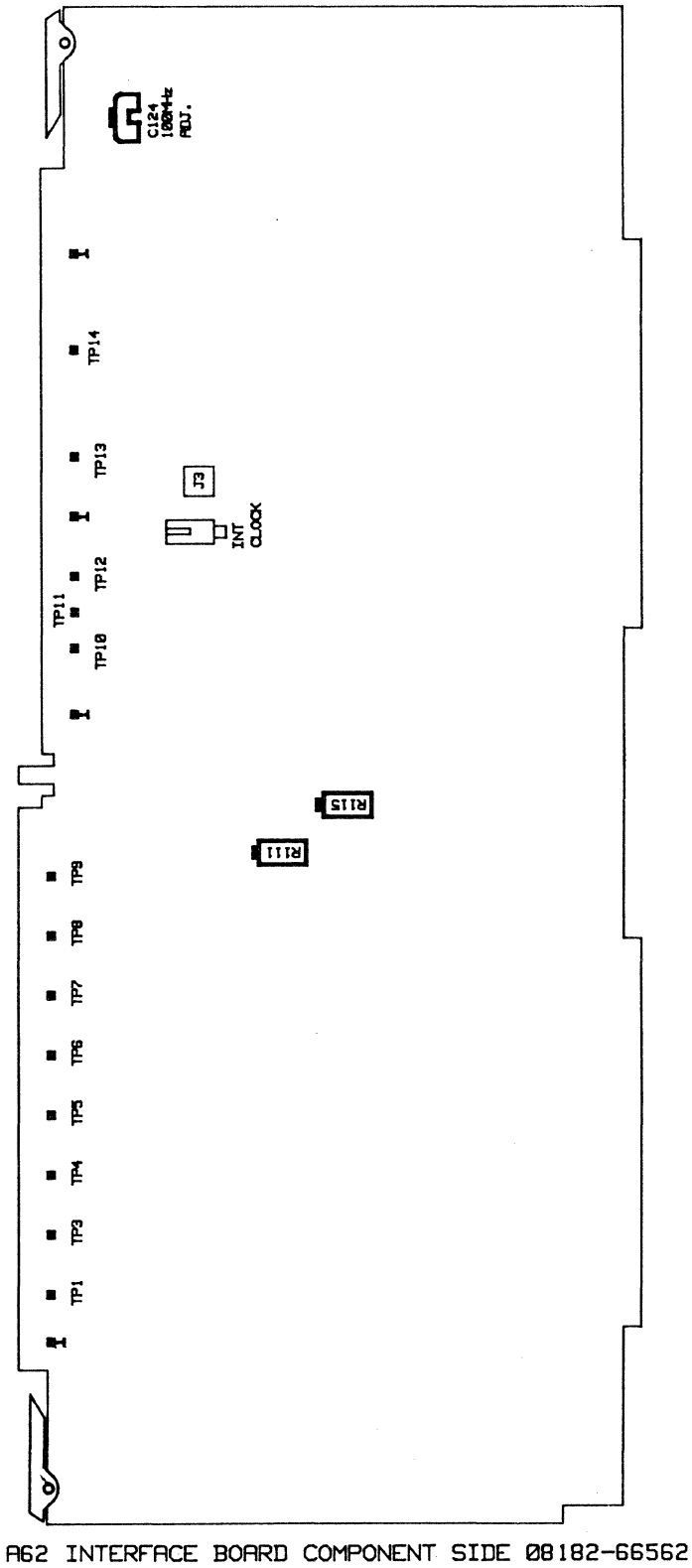


Figure 5-5. A62 Interface Board

5-5 Address Board 08182-66503 (8182A) 08182-66563 (8182B)

External Trigger Arm Amplifier Adjustment

Equipment:

Scope	54100D
Active Pods	54001A
Pulse Generator	(Risetime ≤2.5 ns)
50 Ohm Feedthrough	10100C
BNC Cable	
BNC Tee Connector	1250-0781
BNC scope probe Adapter	1250-1454
Extender Board	08180-66552

Measurement setup:

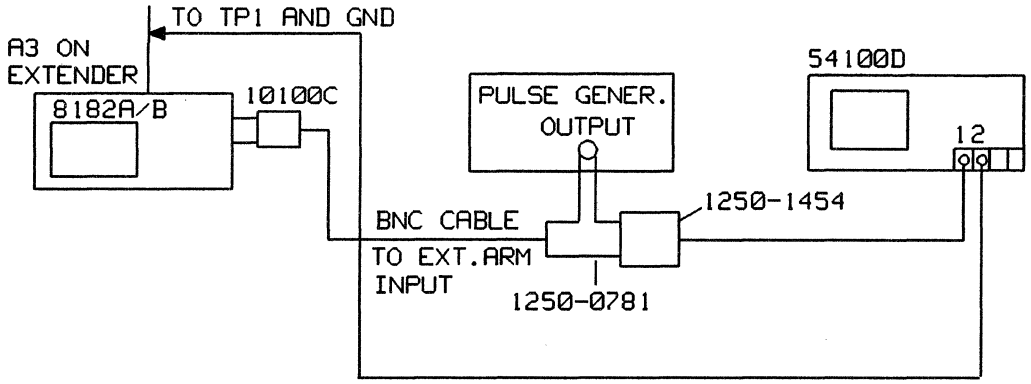


Figure 5- 6. External Trigger Arm Amp Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 KHz (20microsec) squarewave and 2.5V amplitude (2.5V into 50 Ohm, min rise and fall time, offset off).
3. Connect equipment as shown in measurement set up.
4. Connect scope to TP1 and ground TP without using a ground lead (remove insulating sleeve from the probe).
5. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen t Off > Chan 2 > Volt/DIV > 100 mV)
6. Adjust A3 (A63) C1 for best pulse response.

Trigger Arm Amplifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate Trigger Arm Input with 50 Ohm.
8. Program 8182A/B Trigger Arm Pos Slope; Threshold 0.0V: (Pages > Control > Trigger > Trg Arm > Slope > Pos Slope > Exit > Threshold > 0 > Volt)
9. Connect scope probe to TP3 and adjust A3 (A63) R1 until the signal toggles.

5-6 Address Board 08182-66503 (8182A) 08182-66563 (8182B)

External Stop Amplifier Adjustment

Equipment:

Scope	54100D
Active Pods	54001A
Pulse Generator	(Risetime ≤2.5 ns)
50 Ohm Feedthrough	10100C
BNC Cable	
BNC Tee Connector	1250-0781
BNC scope probe Adapter	1250-1454
Extender Board	08180-66552

Measurement setup:

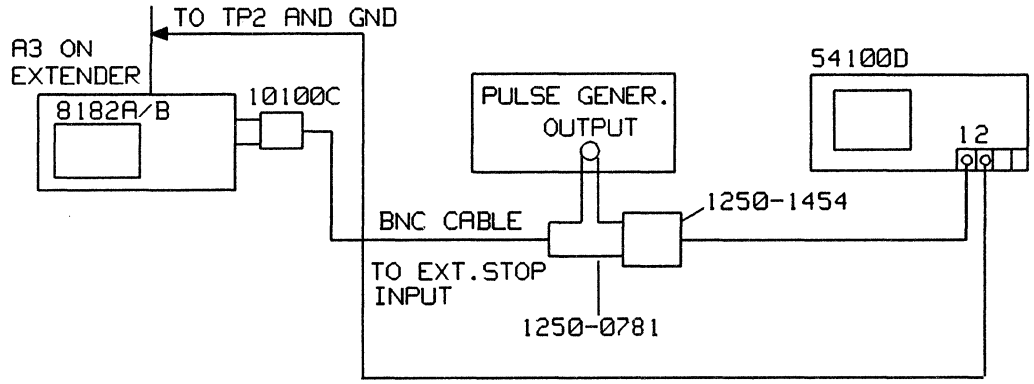


Figure 5-7. External Stop Amp Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 kHz (20 µs) squarewave and 2.5V amplitude (2.5 V into 50Ω, min. rise and fall time, offset to off).
3. Connect equipment as shown in the measurement setup.
4. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen to Off > Chan 2 > 2 Volt/DIV > 100 mV)
5. Adjust A3 (A63) C2 for best pulse response.

External Stop Amplifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate Stop Input with 50 Ω.
8. Program 8182A/B Stop Pos. Slope; Threshold 0.0V: (PAGES > Control > Stop > Stop Slope > Pos. Slope > Exit > Stop Thres. > 0 > Volt)
9. Connect scope probe to TP4 and adjust A3 (A63) R2 until the signal toggles.

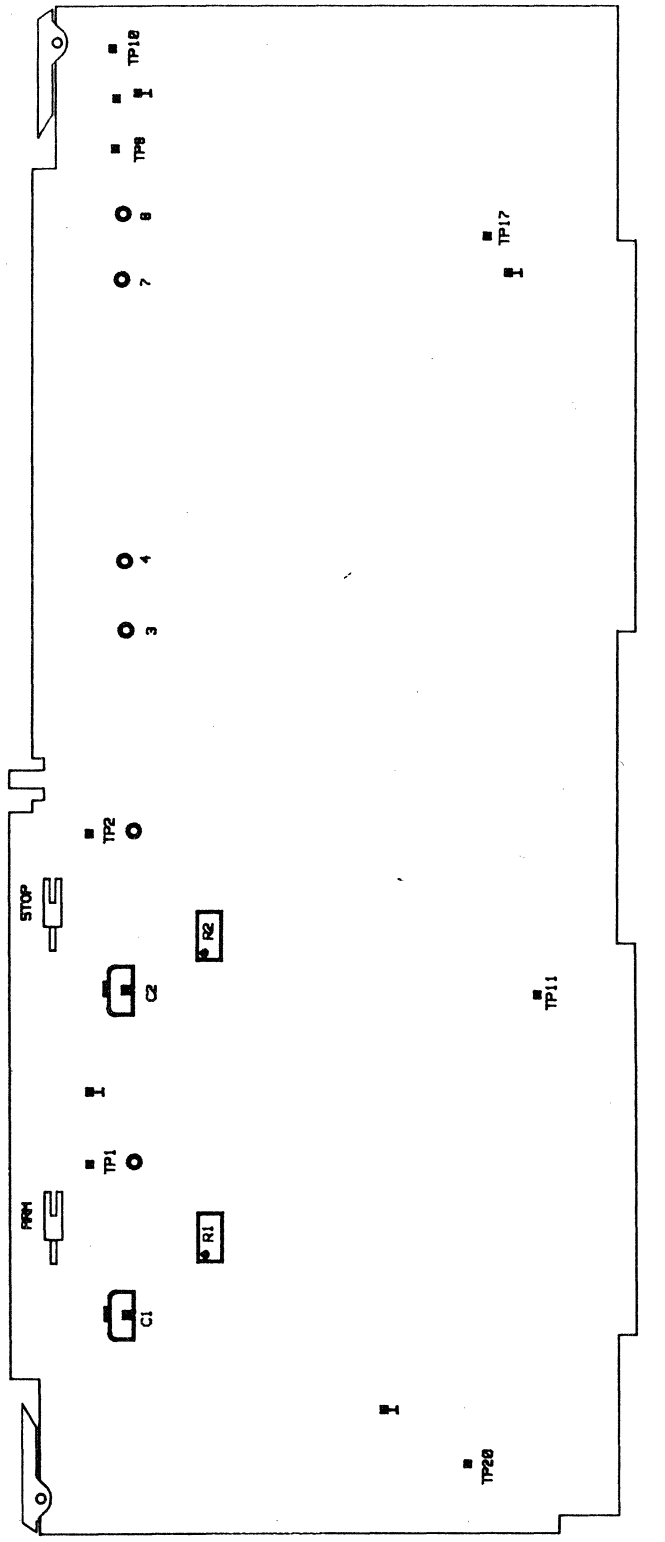


Figure 5-8. A63 Address Board

5-7 Control Board 08182-66504 (8182A) 08182-66564 (8182B)

Trigger Qualifier Adjustment

Equipment:

Scope	54100D
Active Pods	54001A
Pulse Generator	(Risetime ≤2.5 ns)
50 Ohm Feedthrough	10100C
BNC Cable	
BNC Tee Connector	1250-0781
BNC scope probe Adapter	1250-1454

Measurement setup:

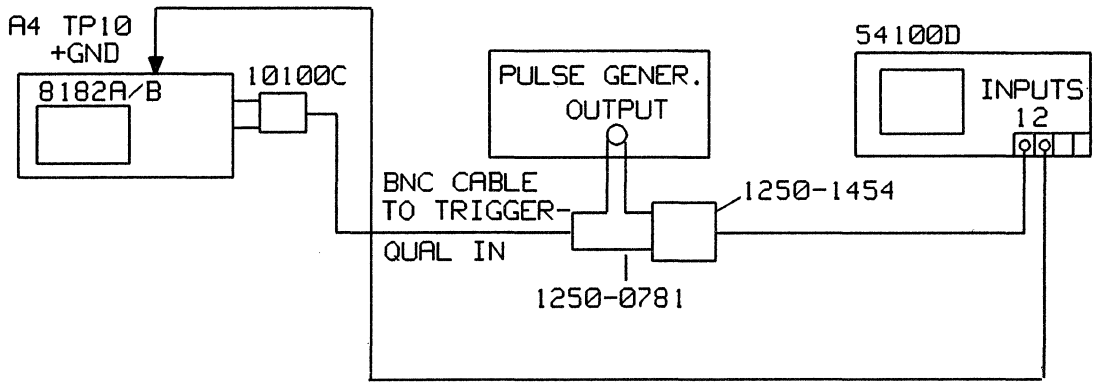


Figure 5-9. Trigger Qualifier Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 KHz (20microsec) squarewave and 2.5V amplitude (2.5V into 50 Ohm, min rise and falltime, offset off).
3. Connect equipment as shown in the measurement set up.
4. Connect scope to TP10 and ground TP without using a ground lead (remove insulating sleeve from the probe).
5. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen t Off > Chan 2 > Volt/DIV > 100 mV)
6. Adjust A4 (A64) C203 for best pulse response.

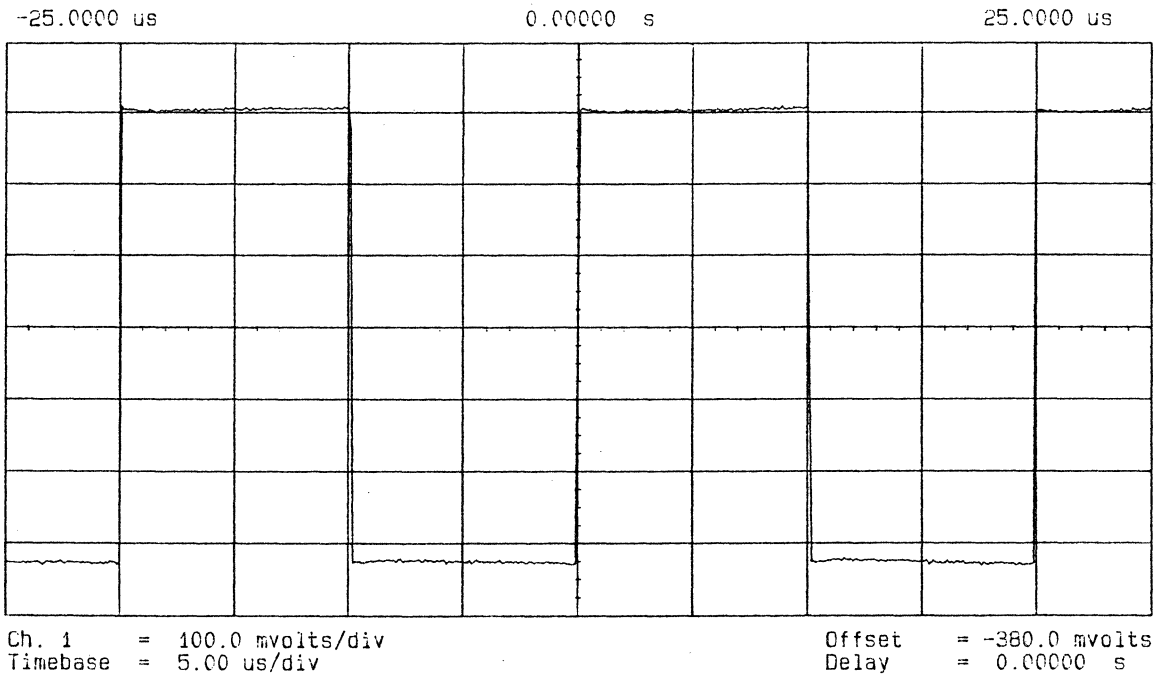


Figure 5-10. Trigger Qualifier - Scope Diplay

Trigger Qualifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate trigger qualifier input with 50 Ohm.
8. Program 8182A/B Trigger Qualifier High Level; Threshold 0.0V: (Pages > Control > Trigger > Trg Qualifier > Level > High Level > Exit > Threshold > 0 > Volt)
9. Connect scope probe to TP11 and adjust A4 (A64) R215 until the signal toggles.

Control Output Adjustment

Equipment:

Digital Voltmeter, testleads HP 3456A

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Connect DVM to A4 (A64) TP14 and next ground TP and adjust A4 (A64) R316 for 0V ±0.05V.

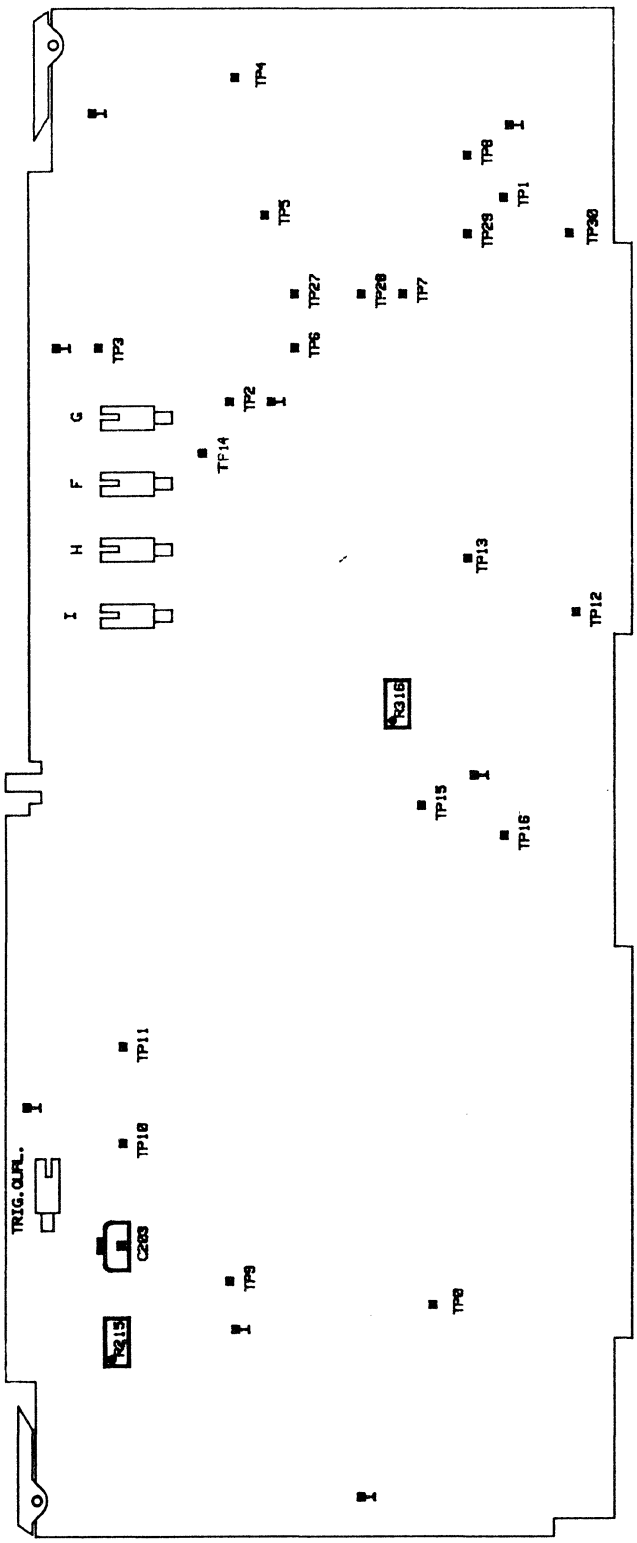


Figure 5-11 A64 Control Board

5-8 Clock Board 08182-66506 (8182A) 08182-66566 (8182B)

Clock Output Amplifier Offset Adjustment

Equipment:

Digital Voltmeter, testleads	HP3456A
BNC cable	
BNC(f) dual banana plug	1251-2277

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Connect DVM to the Clock Out connector (rear panel) and adjust A6 R616 for 0V ±0.05V. (Clock input remains open.)

Timing IC Supply Voltage Adjustment

Equipment:

Digital Voltmeter, testleads	HP3456A

1. Connect DVM to TP5 and TP6 (GND) and adjust A6 R474 to -5.2V ±0.05V.

Clock Amplifier Adjustment

Equipment:

Pulse Generator	(fmin=10Hz, fmax=10Mhz, tr<3ns)
Scope	HP 54100D
Active Pods	HP 54001
Extender Board (8182A)	08180-66552
Extender Board (8182B)	
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Clock Probe	HP 15406A

Measurement setup:

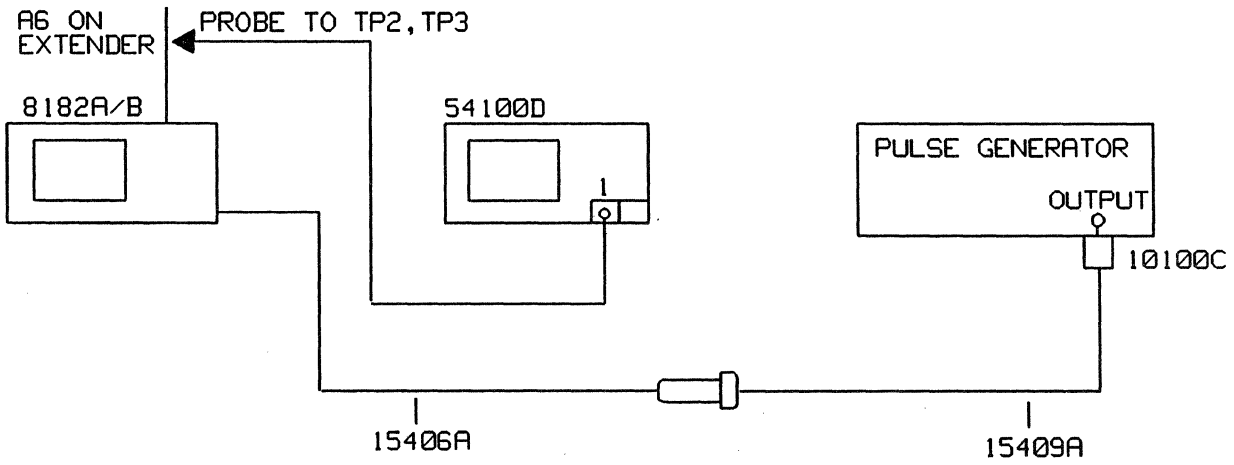


Figure 5-12. Clock Amplifier Adjustment

Low Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to: 10Hz, Squarewave, LOL=0V, HIL=2,5V, 2,5V into 50 Ohm.
3. Connect equipment as shown in the measurement set up.
4. Connect scope probe to TP2 and TP3 (GND). Do not use a ground lead. Remove insulating sleeve from probe.
5. Set scope to: (Autoscale).
6. Adjust A6 R341 for best pulse response (square).

High Frequency Response Adjustment

7. Set Pulse Generator to: 10MHz, Squarewave, LOL=0V, HIL=2,5V, 2,5V into 50 Ohm, transition <3ns.
8. Connect scope probe to TP2 and TP3 (GND). Do not use a ground lead. Remove insulating sleeve from the probe.
9. Set scope to: (Autoscale > Timebase > Sec Div > 2ns)
10. Adjust A6 C360 for best pulse response.

Clock Amplifier Offset Adjustment

Equipment:

Pulse Generator	
Scope	HP 54100D
Active Pods	HP 54001A
BNC Tee connector	1250-0781
BNC Adapter(female/female)	1250-0080
BNC scope probe Adapter	1250-1454
50 Ohm Feedthrough	HP 10100C
BNC Cable	
BNC Adapter	HP 15409A
Clock Cable	HP 15406A

Measurement setup:

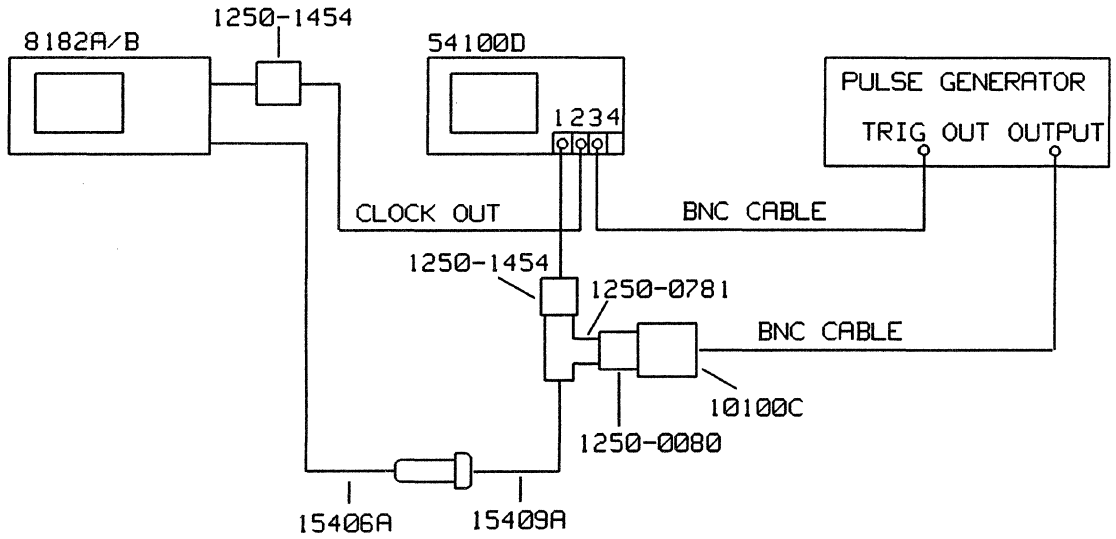


Figure 5-13. Clock Amplifier Offset Adjustment

1. Set Pulse Generator to:

Period	1ms
Pulse Width	0.5ms
Amplitude	200mV symmetrically to 0V
Transition Time	5µs to 250 µs

2. Adjust leading edge and trailing edge for a triangular waveform. Using the offset vernier, set the signal to be symmetrical about the center graticule line.

3. Program 8182A/B to Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute Pages > Control > Operatg Mode > Trg Start Comp > Execute)

4. Set Sampling Clock Slope to Both Slopes; Clock Threshold 0.00V: (Pages > Control > Clock > Clock Slope > Both Slps > Exit > Clock Thresh 0V > Exit > Clock Width > 50 Microsec)

5. Connect equipment as shown in measurement set up.

6. Set scope to: (Autoscale > Chan 2 > Chan 2 Display Off > Display > Split Screen Off > Trigger > Trigger Src > to Trig 3)

7. Check if generator signal is symmetrical about the center graticule line. Set the Start Marker to the crossover point / positive going transition and the Stop Marker to the crossover point / negative going transition and perform Delta t measurement: (Delta t > Tmarkers on > Start Marker > Knob > Stop Marker > Knob)

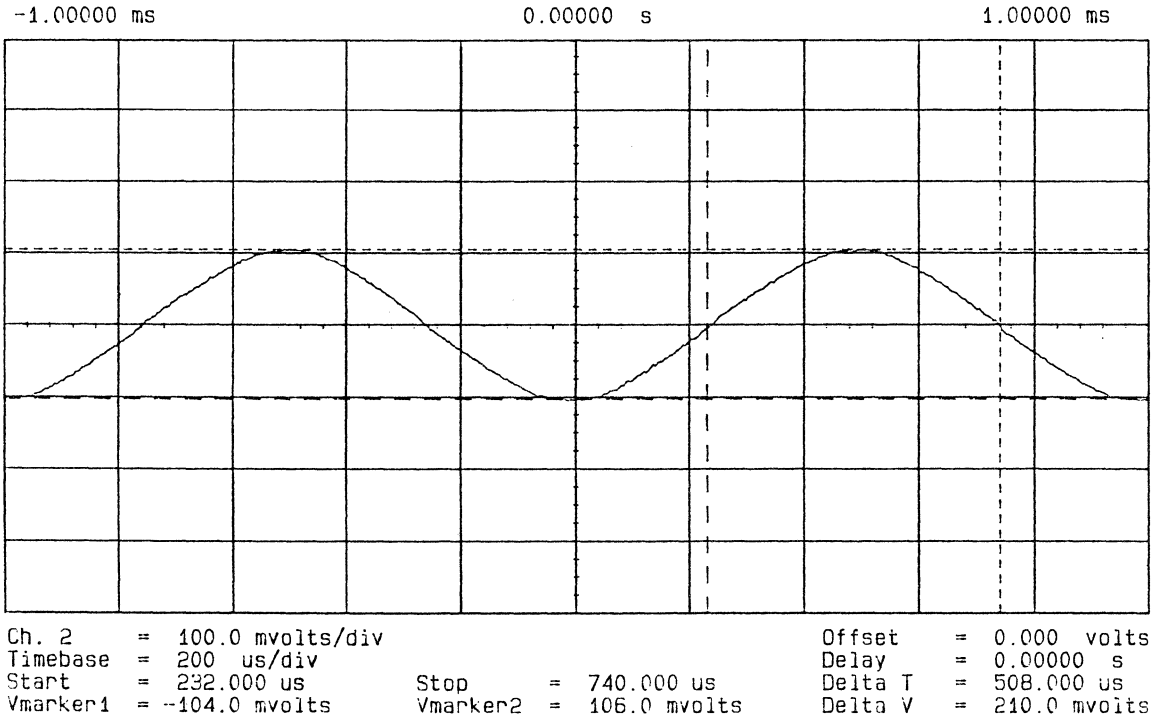


Figure 5-14. Clock Amp Offset Adjustment - Scope Display 1

8. Switch channel 1 off and channel 2 on: (Chan 1 > Chan 1 Display to off > Chan 2 > Chan 2 Display to on)

9. Adjust A6 R353 until measured time difference between the positive going edges of the displayed pulses shows the value measured in point 7.

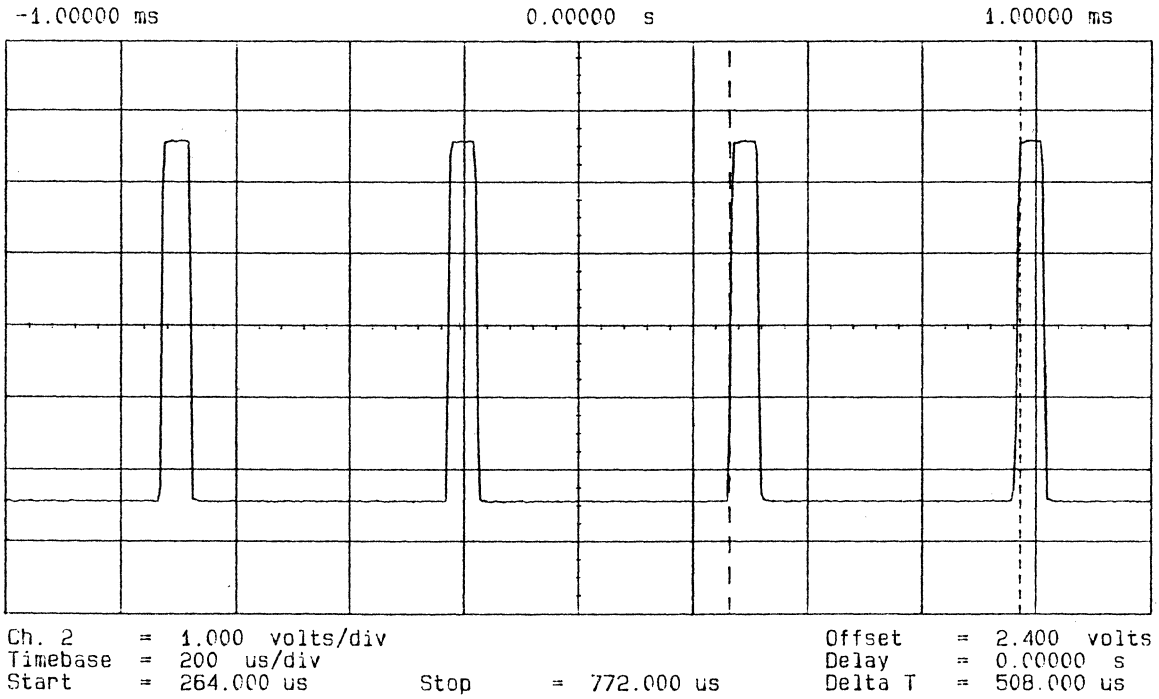


Figure 5-15. Clock Amp Offset Adjustment - Scope Display 2

Clock Qualifier Adjustment

Equipment:

Pulse Generator	(Risetime ⩽2.5 ns)
Scope	HP54100D
Active Pods	HP54001A
50 Ohm Feedthrough	HP10100C
BNC cable	

Measurement setup:

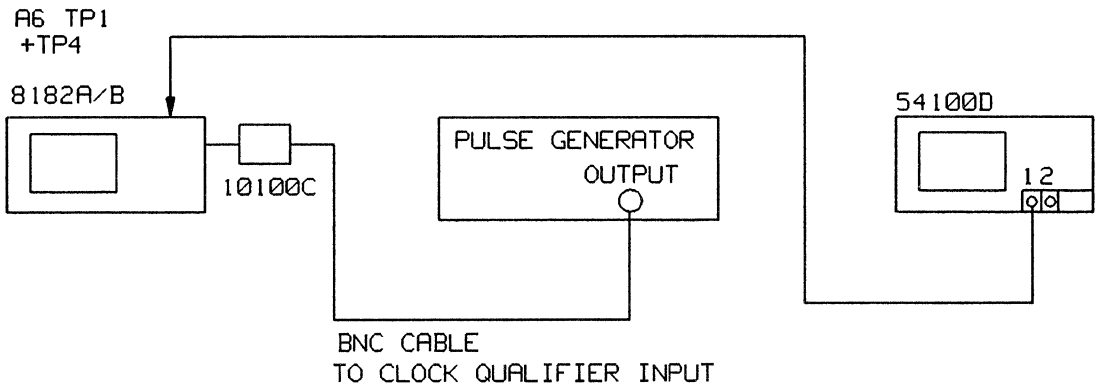


Figure 5-16. Clock Qualifier Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 kHz, (20 microsec.) squarewave and 2.5V amplitude. (2.5 V into 50 Ohm, min. rise and fall time, offset to Off)
3. Connect equipment as shown in the measurement set up.
4. Connect scope probe to TP1 and TP4 (GND). Do not use a ground lead. Remove insulating sleeve from probe.
5. Adjust A6 C304 for best pulse response (square wave).

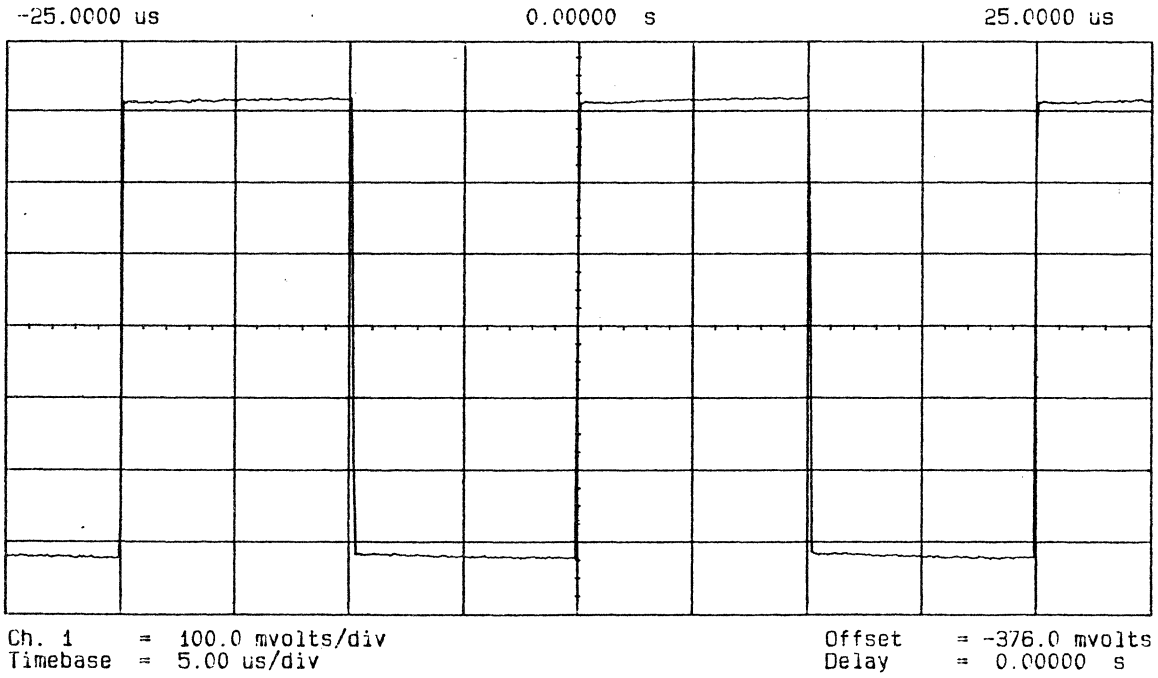


Figure 5-17. Frequency Response Adjustment - Scope Display

Clock Qualifier Offset Adjustment

Equipment:

Pulse Generator	
Scope	HP 54100D
Active Pods	HP 54001A
BNC Tee connector	1250-0781
BNC scope probe adapter	1250-1454
50 Ohm Feedthrough	HP 10100C
BNC cable	
Clock cable	HP 15406A
Grabber	HP 15408A

Measurement setup:

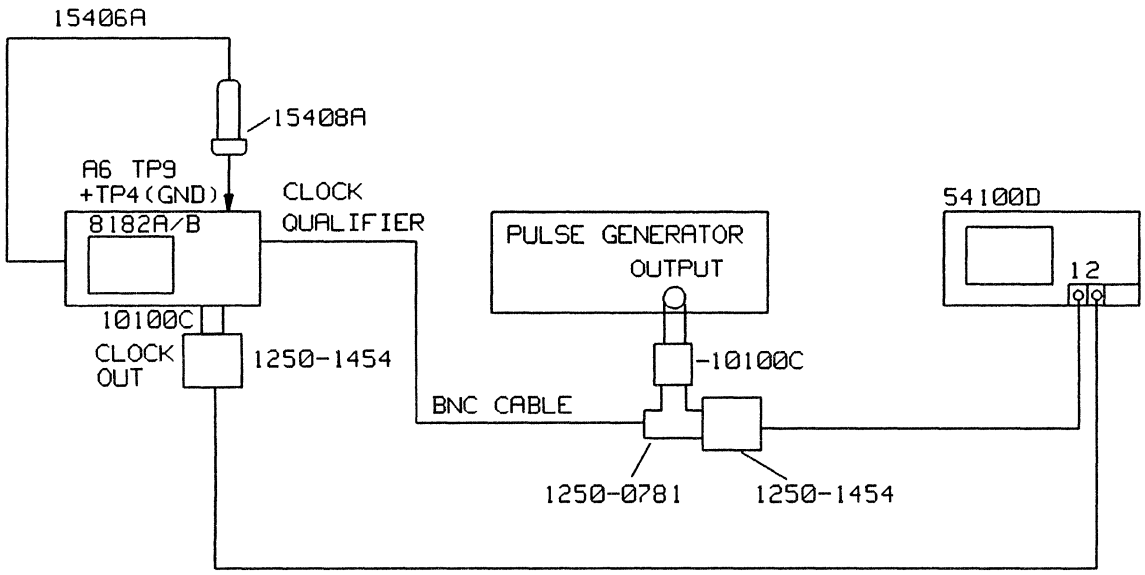


Figure 5-18. Clock Qualifier Offset Adjustment

1. Set Pulse Generator to:

Period	1ms
Pulse Width	0.5ms
Amplitude	200mV
Offset	On
Transition Time	5µs to 250µs

2. Adjust Leading Edge and Trailing Edge for a triangular waveform. Using the Offset Vernier set the triangular signal to be symmetrical about 0 Volts.

3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

4. Set the Operating Mode to Trigger Start Compare; Clock Source to External: Both Clock Slopes to Active; Clock Threshold to -1.2V: (Pages > Control > Operatg Mode > Trg Strt Comp > Execute > Exit > Clock > Clock Source External > Exit > Clock Slope > Both Slps > Exit > Clock Thres > -1.2V)

5. Set Clock Qualifier to Don't Care; Threshold 0V: (Clock Qual > Level > Don't Care > Exit > Threshold > 0.00V)

6. Set Clock Width to 100 microsec (Exit > Exit > Clock Width > 100 > Microsec)

7. Connect equipment as shown in measurement set up.

8. Set scope to: (Autoscale > Trigger > Trig Src to Chan 2 > Chan 2 > Chan 2 Disp to Off > Display > Split Screen to Off > Chan 1 > Offset > 0.00V)

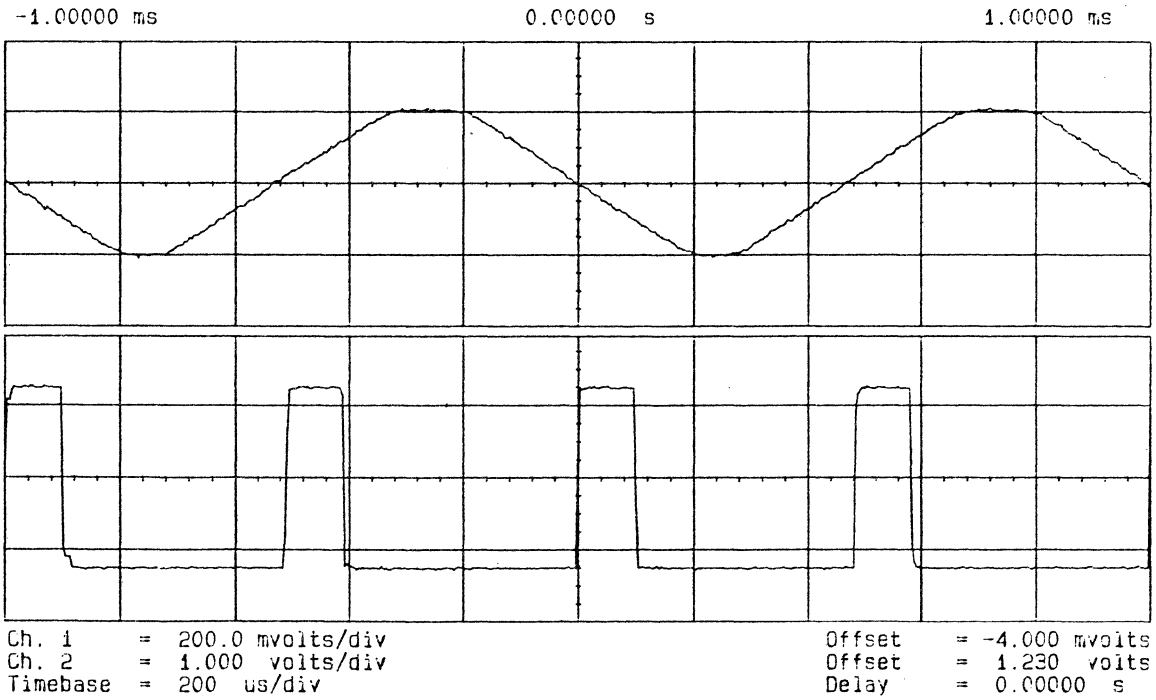


Figure 5-19. Clock Qualifier Offset Adjustment - Scope Display 1

9. Set Timebase to 100 ns and display mode to average: (Timebase > Sec/Div > 100 ns > Display Mode to Averaged > Number of Averages to 2 > Knob)

10. Set scope into magnify mode: (Chan 1 > Chan 1 Mode to Magnify > Magnify On > Volts/DIV to 20 mV using the Knob)

11. Adjust A6 R319 so that the dotted band on the screen is symmetrical about the center graticule line.

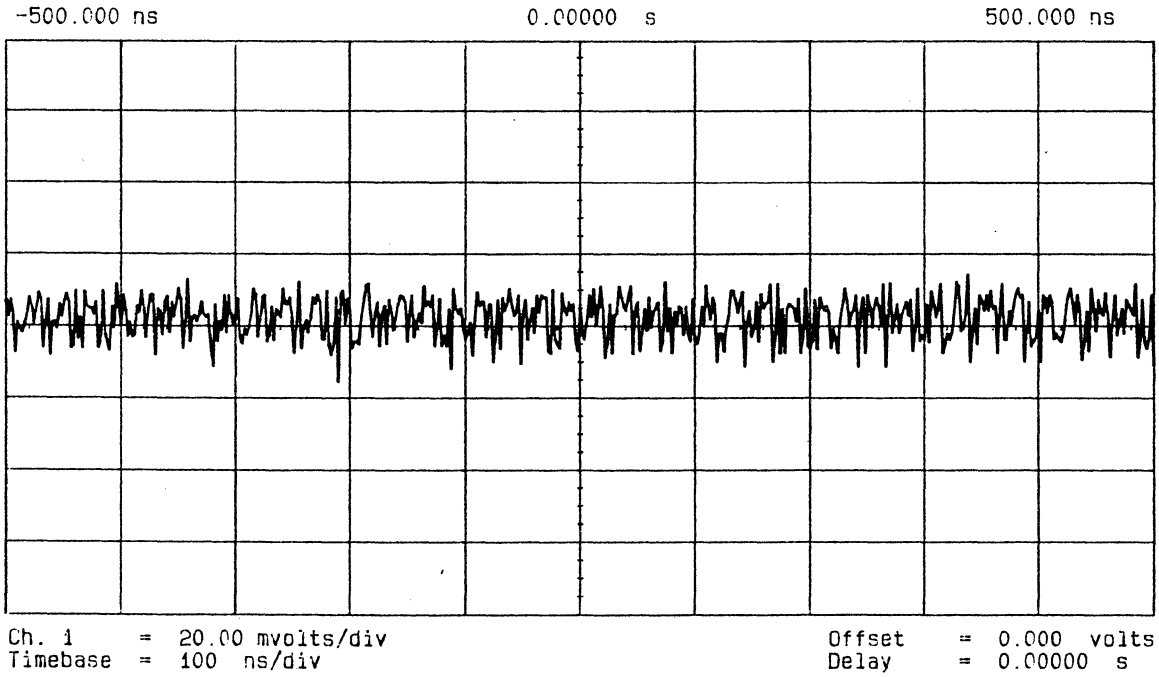


Figure 5-20. Clock Qualifier Adjustment - Scope Display 2

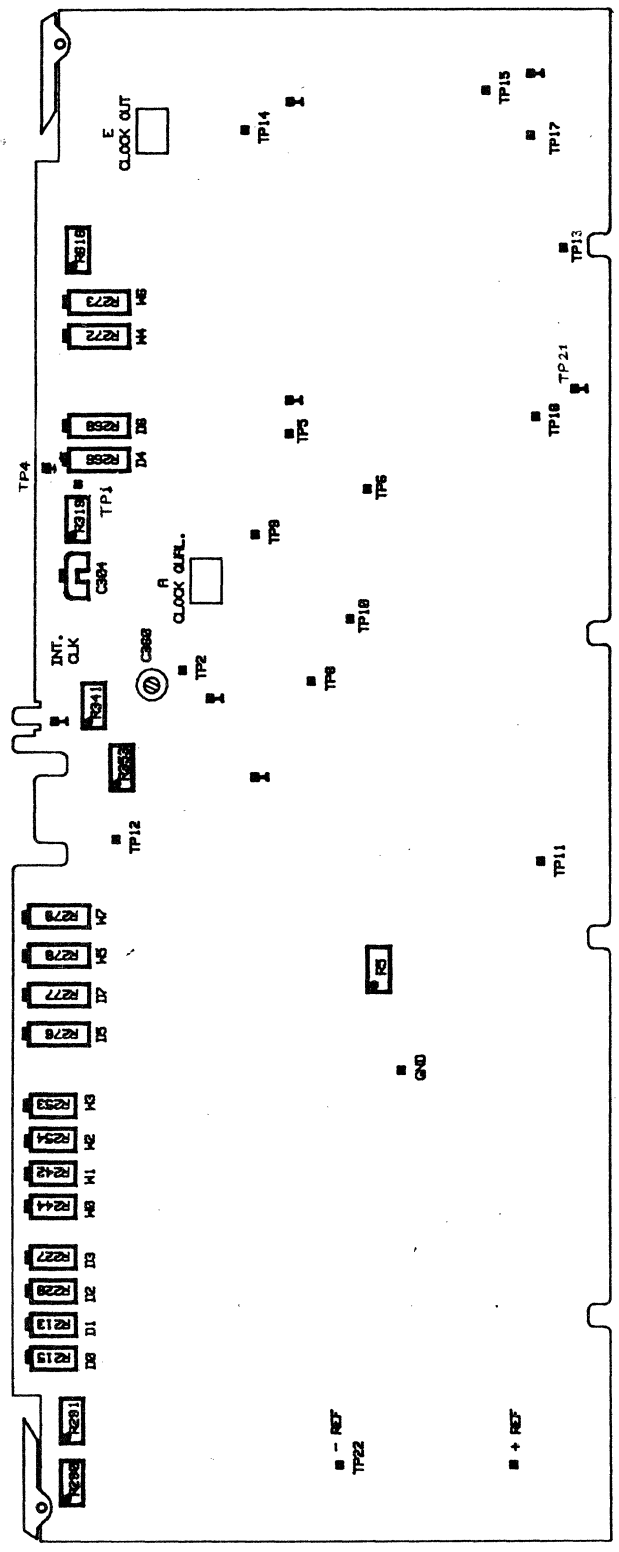


Figure 5-21. A66 Clock Board

Fixed Delay Adjustment

Equipment:

Scope	HP 54100D
Active Pods	HP 54001A
Pulse Generator	
Extender Board	08180-66552
BNC Tee connector	1250-0781
BNC Adapter	HP 15409A
BNC scope probe Adapter	1250-1454
Delay Line 34ns	08182-61622

Measurement setup:

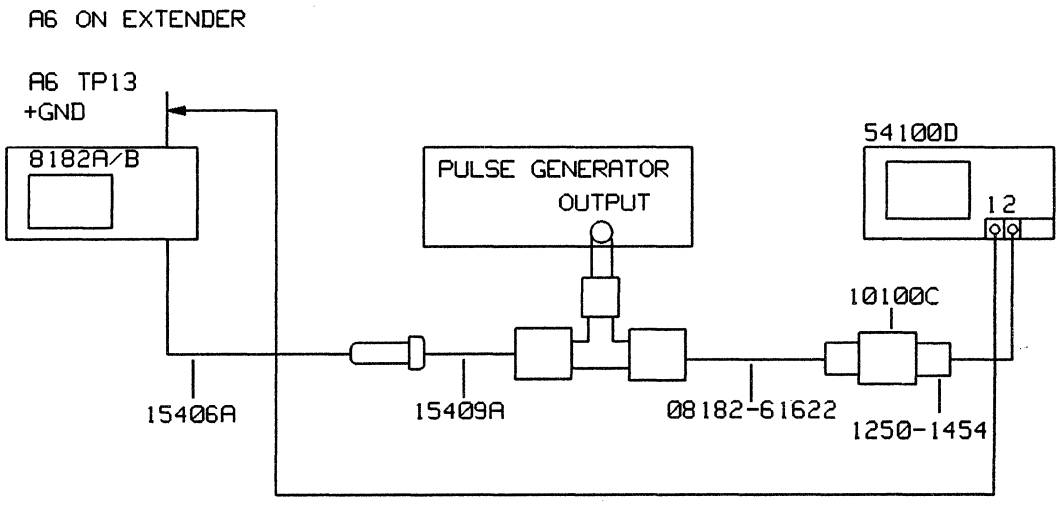


Figure 5-22. Fixed Delay Adjustment

1. Cancel out interchannel delay and trigger delay of scope.

2. Set Pulse Generator to:

Period	1 microsec
Pulse Width	0.5 microsec
Leading Edge	< 3ns
HIL	2.00 V
LOL	0.00 V into 50 Ohm

3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

4. Clock Threshold 1.00V: (Pages > Control > Clock > Clock Thres > 1 > Volt)

5. Connect equipment as shown in measurement set up.

6. Set scope to:

Channel 1	200mV/DIV
Channel 2	500mV/DIV ; Offset 1V
Trigger	on Channel 2; Trigger level 1V
Split Screen	Off

(Autoscale > Chan 1 > Volt/DIV > 200mV > Chan 2 > Volt/DIV > 500mV > Offset > 1V > Trigger > Trg Src to Chan 2 > Trigger Level > 1V > Display > Split Screen to Off)

7. Adjust Channel 1 Offset so that the base line of channel 1 meets the base line of channel 2: (Chan 1 > Offset > Knob)

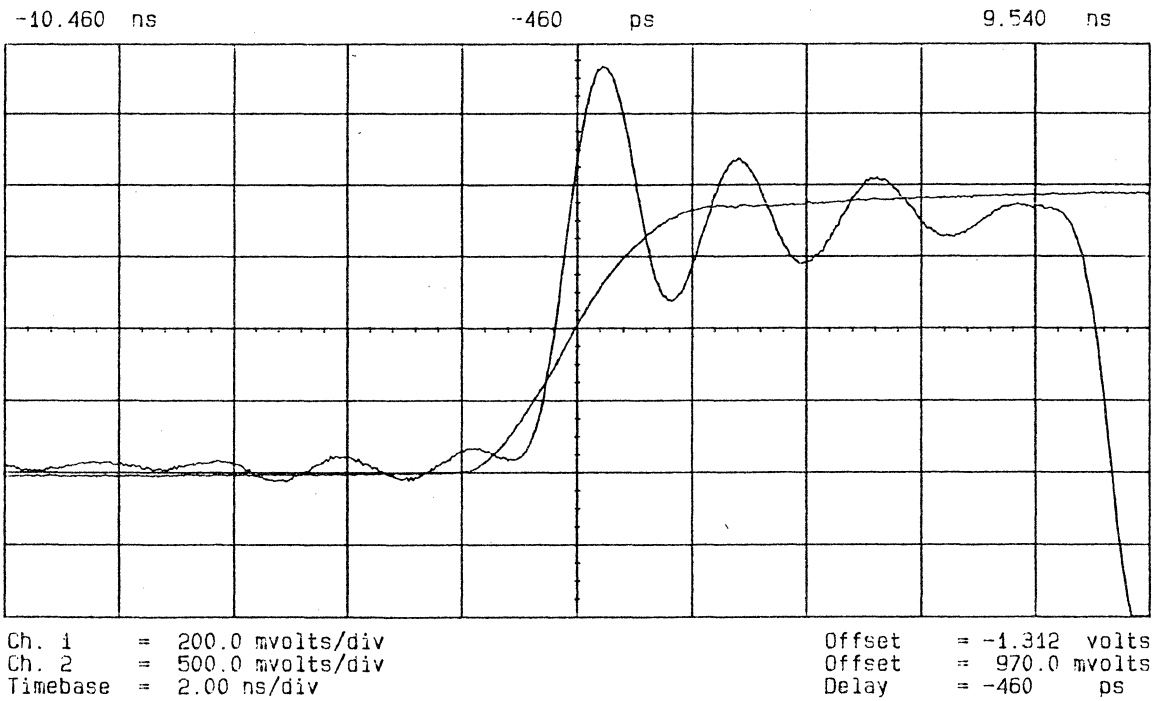


Figure 5-23. Fixed Delay Adjustment - Scope Display 1

8. Set Timebase to 500ps: (Timebase > 500ps)

9. Adjust A6 R215 for zero delay of both signals measured at the center graticule line.

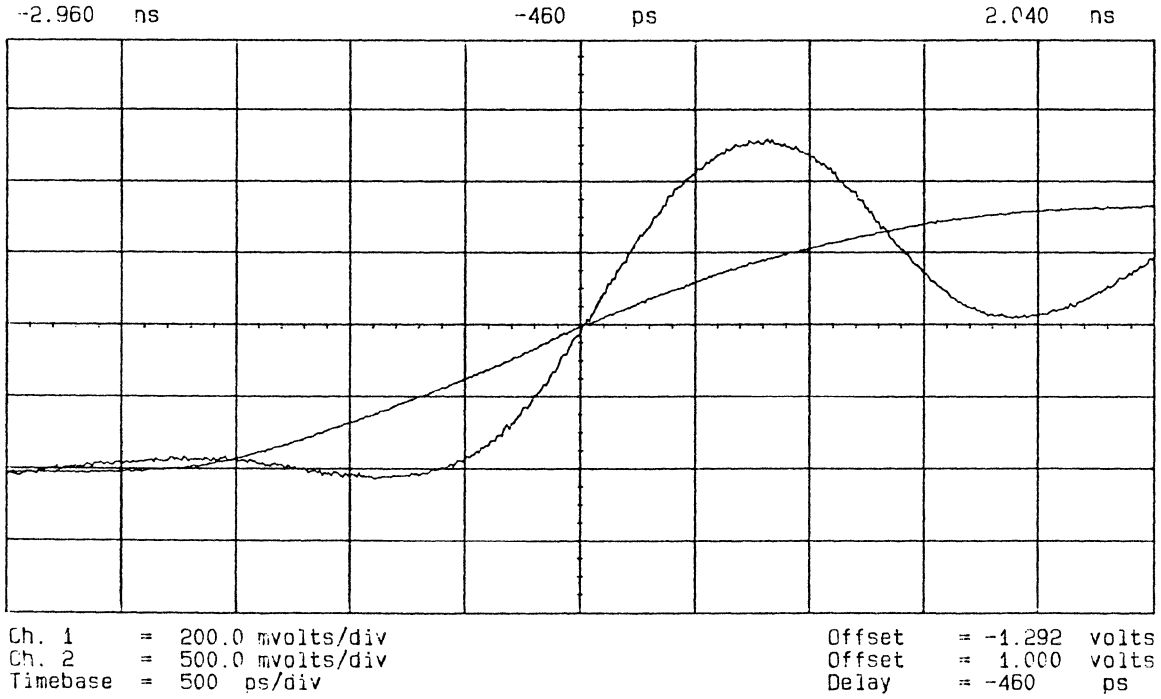


Figure 5-24. Fixed Delay Adjustment - Scope Display 2

Clock Delay Adjustment

Equipment:

Scope	HP 54100D
Active Pods	HP 54001A
Pulse Generator	
BNC Tee Adapter	1250-0781
50 Ohm Feedthrough	HP 10100C
BNC scope probe Adapter	1250-1454
BNC Adapter	HP 15409A
Clock Probe	HP 15406A

Measurement setup:

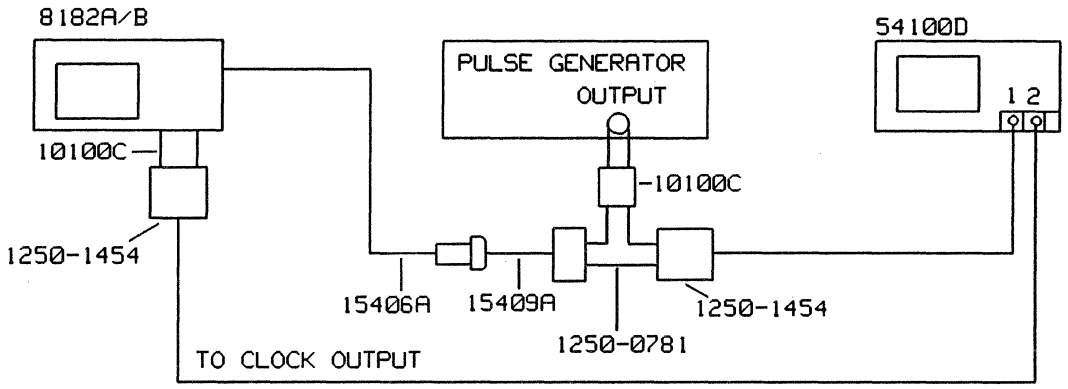


Figure 5-25. Clock Delay Adjustment

1. Set Pulse Generator to:

Period	100 microsec
Pulse Width	1.5 microsec
Transition Time	2 ns
HIL	2.5 V
LOL	0.00V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

3. Clock Threshold 1.2 V Clock Delay 0.00ns: (Pages > Control > Clock > Clock Thres > 1.2 > Volt > Exit > Clock Delay > 0 > Nanosec)

4. Connect equipment as shown in measurement set up.

5. Set scope to: (Autoscale > Trigger > Trg Src To Chan 1 > Chan 1 > Chan 1 Display to Off>Display> Split Screen to Off > Chan 2 > Volt/DIV > 500mV > Offset > 1.25V Timebase > Sec/DIV > 20 ns)

6. Set 50% point of positive going transition to center graticule line: (Delta V > V markers to Chan 2 > Auto Top Base > 50-50% > Chan 2 > Offset> Knob)

7. Move the pulse so that the 50% point of the positve going transition crosses the center horizontal and vertical graticules: (Timebase > Sec/DIV > 1ns > Delay > 38ns > Knob)

8. Set the Start Marker to 50% point of positive going transition: (Delta t > T Markers to On > Start Marker > Knob)

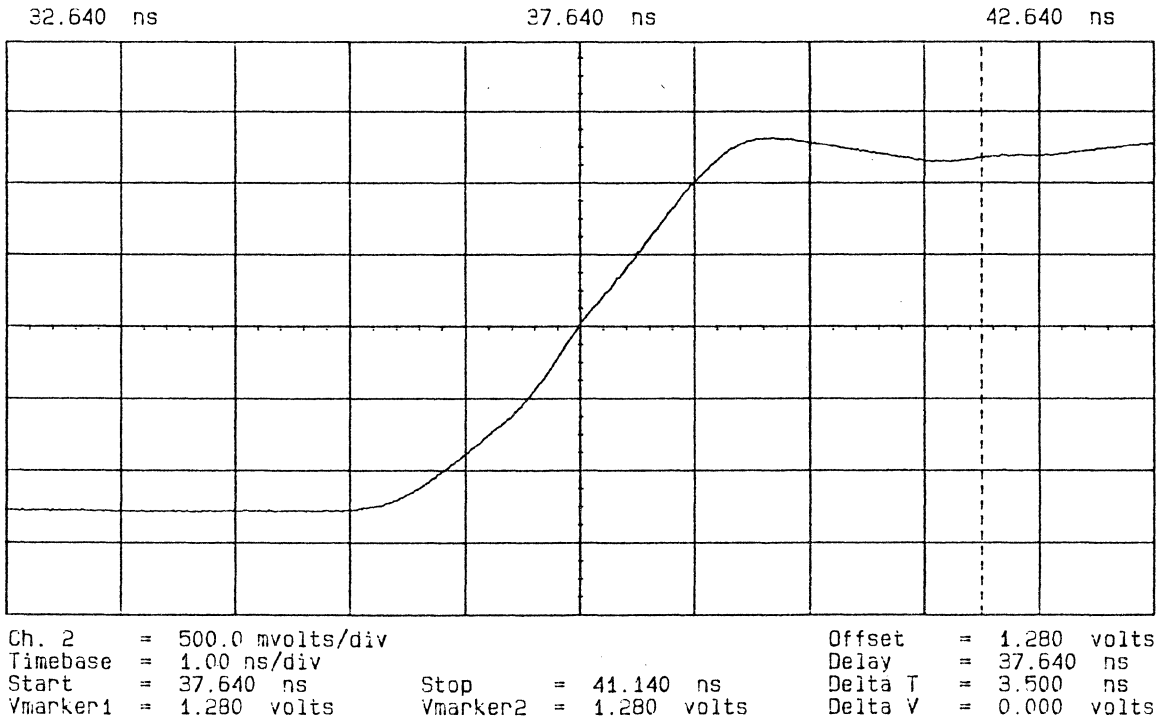


Figure 5-26. Clock Delay Adjustment - Scope Display 1

NOTE

The position of the start marker is used as the reference for the delay adjustment and should therefore not be moved during the following adjustments.

9. Program 8182A/B Clock Delay 5.9 ns: (Pages > Control > > Clock > Clock Delay > 5.9 > Nanosec)

10. Add to the programmed delay the zero delay (position of the Start marker) and program the Stop Marker to this value.
Example: Start marker position = 40ns, then Stop Marker = 45.9ns. Adjust Timebase Delay until the Stop Marker crosses the vertical center line.

11. Adjust A6 R213 (D1) so that the 50% point of the positive going transition crosses the center graticules (X & Y).

12. Repeat step 9 through to 11 with the following values:

Programmed Clock Delay	Adjust
6 ns	A6 R228 (D2)
21.9 ns	A6 R227 (D3)
22 ns	A6 R266 (D4)
117 ns	A6 R276 (D5)
10 µs	A6 R268 (D6)

Increase Pulse Generator Period to 150 µs.

99.9 µs	A6 R277 (D7)
118 ns	A6 R290 (D8)

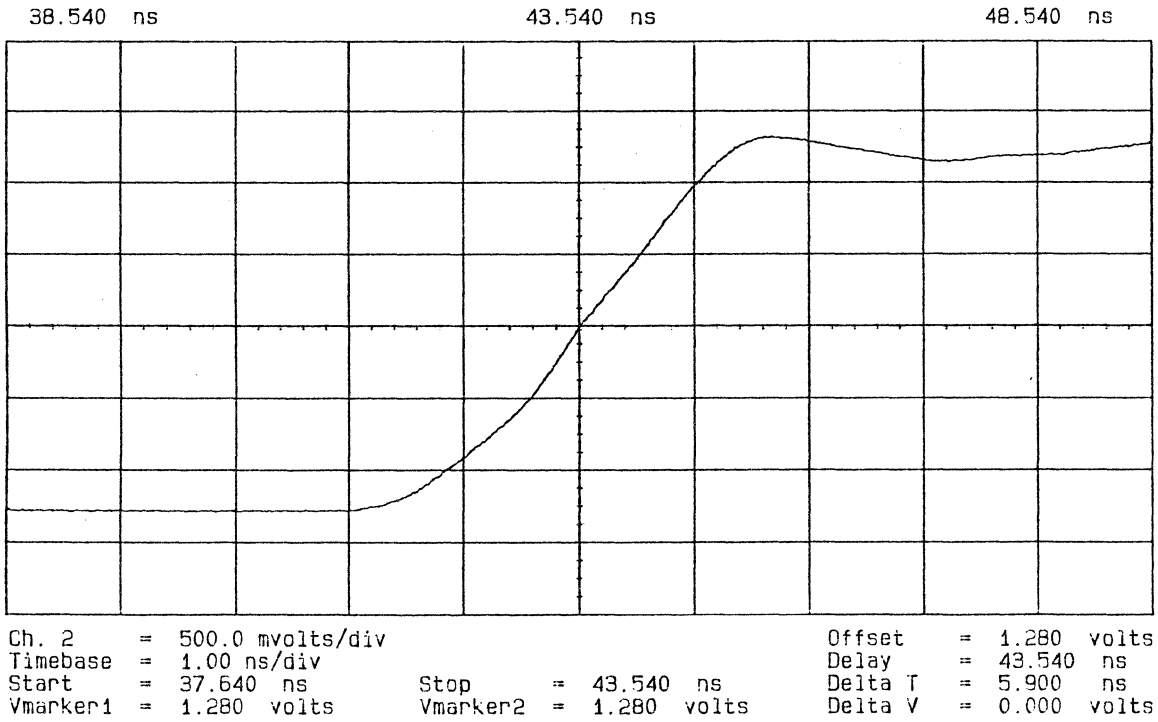


Figure 5-27. Clock Delay Adjustment - Scope Display 2

Clock Width Adjustment

Equipment:

Scope	HP 54100D
Active Pods	HP 54001A
Pulse Generator	
Clock Probe	HP 15406A

BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Scope probe Adapter	1250-1454

Measurement setup:

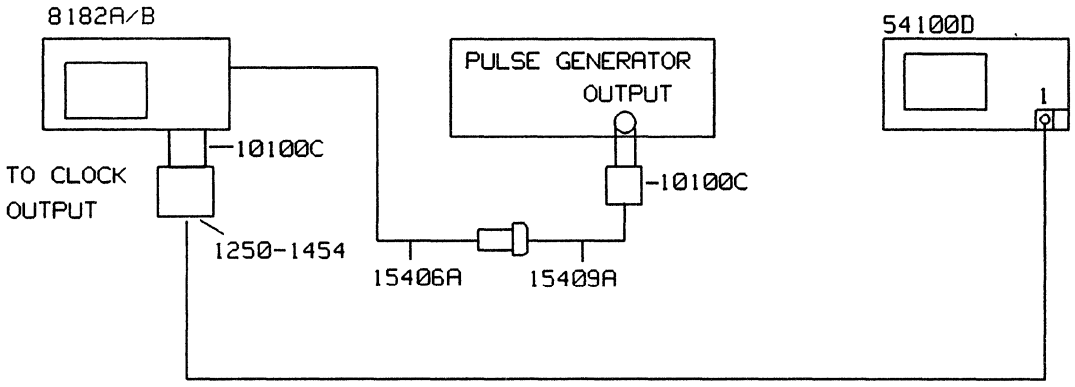


Figure 5-28. Clock Width Adjustment

1. Set Pulse Generator to:

Period	100 µs
Pulse Width	1.5 µs
Transition Time	2 ns
HIL	2.5 V
LOL	0.0 V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

3. Trigger Event Start Compare: (Pages > Control > Operating Mode > Trg Strt Comp > Execute)

4. Clock Width 10 ns: (Pages > Control > Clock > Clock Width > 10 > Nanosec)

5. Connect equipment as shown in measurement set up.

6. Cancel out trigger delay on scope channel 1.

7. Set scope to: (Autoscale > Delta V > V Markers to Chan 1 > Auto Top Base > 50-50%)
   Adjust displayed 50% level with Knob so that it crosses the center graticule: (Chan 1 > Offset > Knob)

8. Set Start Marker to 0.00 ns and check that 50% of the positive going transition crosses the center graticules (X & Y).
   If not, check trigger delay offset: (Timebase > Sec/DIV > 1 ns > Delata t > T markers to On > Start Marker > 0)

NOTE

The position of the start marker is used as reference for the width adjustment and should therefore not be moved during the following adjustment.

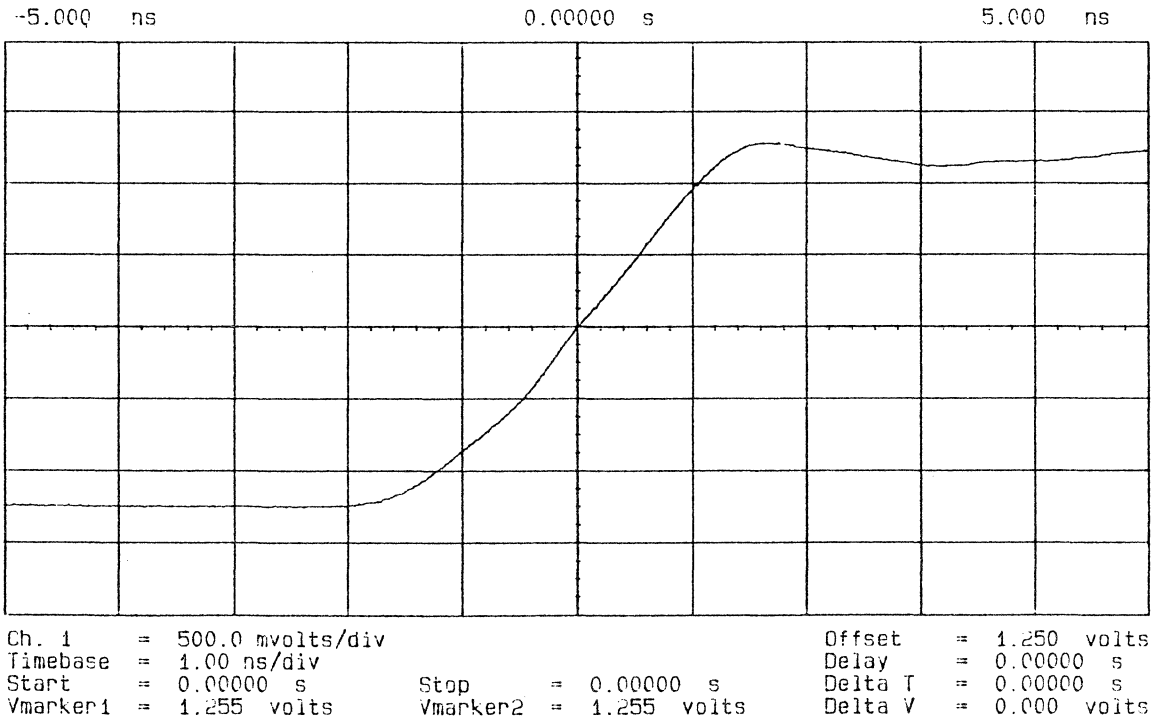


Figure 5-29. Clock Width Adjustment - Scope Display 1

9. Set Timebase Delay to 10 ns: (Timebase > Delay > 10ns)

10. Adjust A6 R244 so that the 50% point of the negative going transition crosses the center graticules.

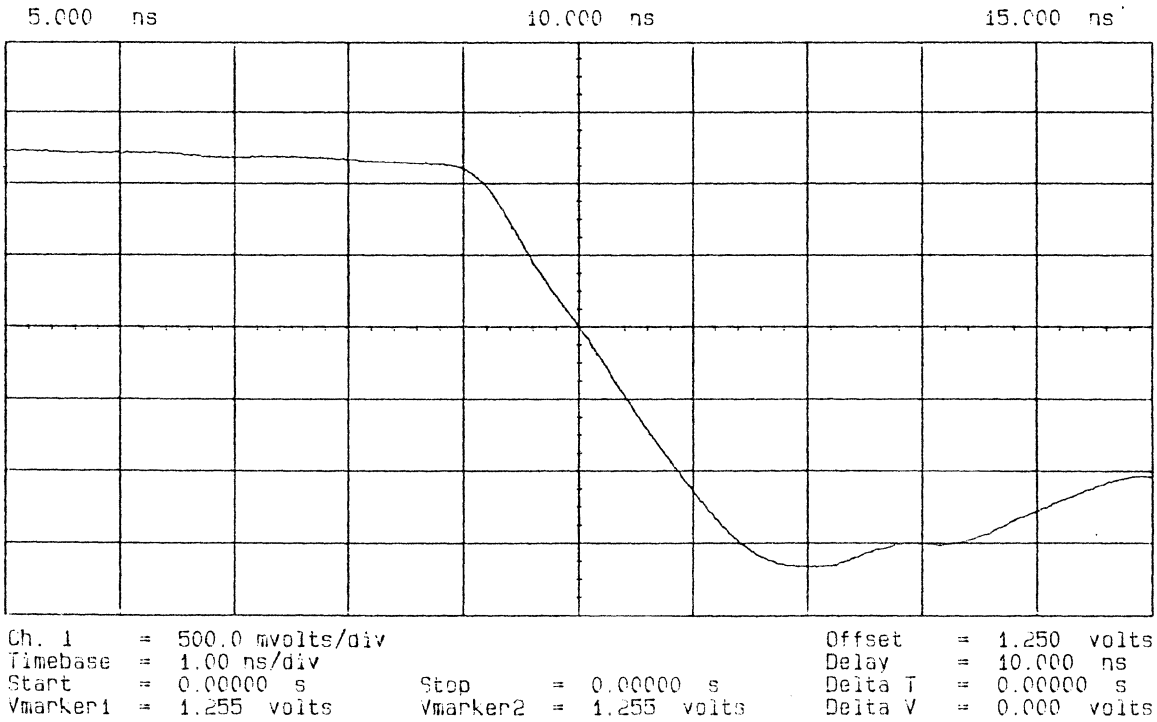


Figure 5-30. Clock Width Adjustment - Scope Display 2

11. Repeat step 9 and 10 for the listed Clock Width values and perform the corresponding adjustment.

8182A/B Clock Width	Adjust
16.9 ns	A6 R242 (W1)
17.0 ns	A6 R254 (W2)
31.9 ns	A6 R253 (W3)
32.0 ns	A6 R272 (W4)
127 ns	A6 R278 (W5)
10.0 µs	A6 R273 (W6)

Increase Pulse Generator Period to 150 microsec.

99.9 µs	A6 R279 (W7)
128 ns	A6 R291 (W8)

Table 5-1 summarizes the adjustments that are to be performed on the Clock Board.

Table 5-1. Clock Board Adjustments

Adjustment	Adjust	Adjust for:	Measured at:
Clock Out Offset	R616	0V +/-0.05V	Clock Out
Clock Amplifier LF	R341	best pulse response	TP2 TP3
Clock Amplifier HF	C360	best pulse response	TP2 TP3
Clock Amplifier Offset	R353	(A) both traces symm.to 0V	Clock Out
Clock Qual. Freq. Resp.	C304	best pulse response	TP1 TP4
Clock Qualifier Offset	R319	Less intens. pt. symm.to 0V	Clock Out
Fixed Clock Delay	R215	zero delay of both signals	TP13 GND
Timing IC Supply	R474	-5.2V +/-0.05V	TP5 TP6
Clock Delay	R213	5.90 ns	Clock Out
Clock Delay	R228	6.00 ns	Clock Out
Clock Delay	R227	21.9 ns	Clock Out
Clock Delay	R266	22.0 ns	Clock Out
Clock Delay	R276	117 ns	Clock Out
Clock Delay	R268	10.0 us	Clock Out
Clock Delay	R277	99.9 us	Clock Out
Clock Delay	R290	118 ns	Clock Out
Clock Width	R244	10.0 ns	Clock Out
Clock Width	R242	16.9 ns	Clock Out
Clock Width	R254	17.0 ns	Clock Out
Clock Width	R253	31.9 ns	Clock Out
Clock Width	R272	32.0 ns	Clock Out
Clock Width	R278	127 ns	Clock Out
Clock Width	R273	10.0 us	Clock Out
Clock Width	R279	99.9 us	Clock Out
Clock Width	R291	128 ns	Clock Out

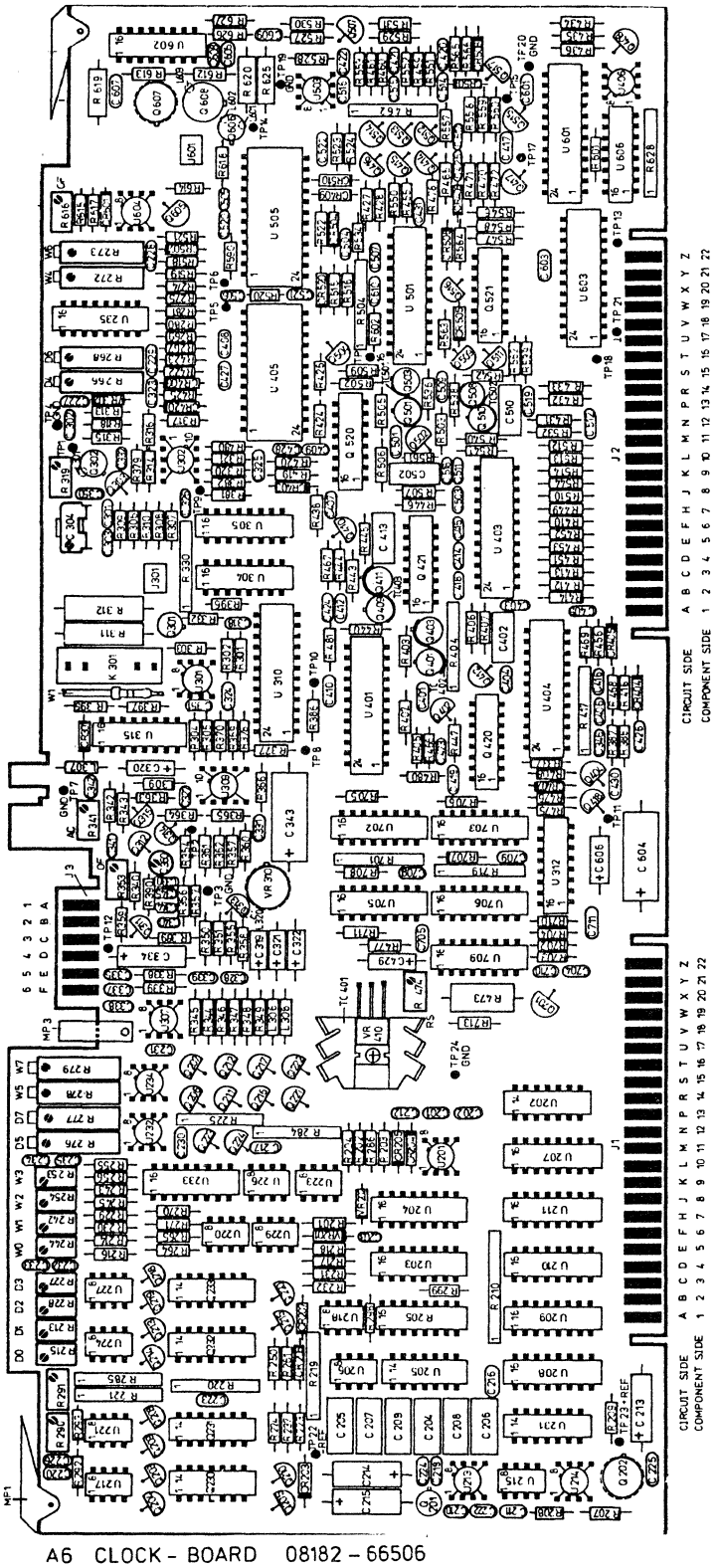


Figure 5-31. A6 Clock Board

5-9 Data Board 08182-66505 (8182A) 08182-66565 (8182B)

Input Amplifier Adjustment

Equipment:

Scope	HP 54100D
Active Probe	HP 54001A
Pulse Generator	(Fmin=10Hz; Fmax=10MHz; tr<3ns)
Extender Board	08180-66552
50 Ohm Feedthrough	HP 10100C
BNC Adapter	HP 15409A
DATA Probe	HP 15407A

NOTE

The following procedure describes the low and high frequency adjustment for Data Board 0 Channel 0. Adjustments for the other boards and channels are listed in the adjustment summary.

If you wish to do adjustments for one connector at a time use adjustment summary at the end of this section.

If you wish to do adjustments for one board at a time use adjustment summary at the end of this section.

Measurement setup:

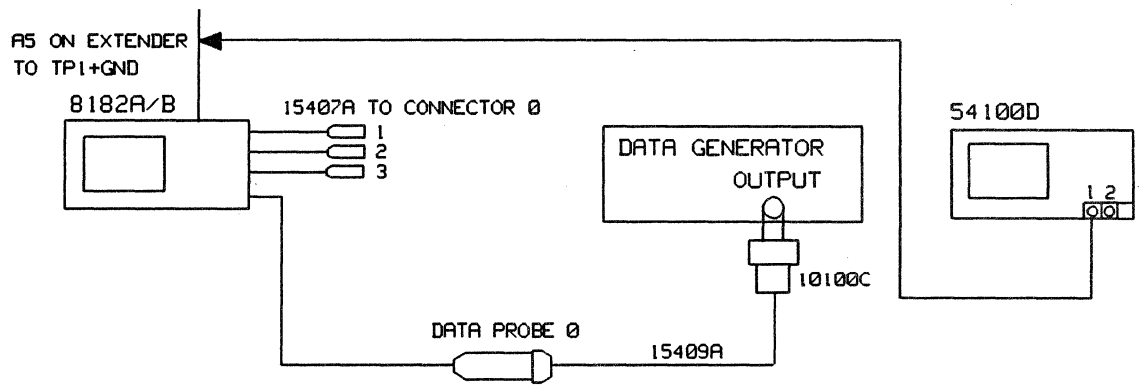


Figure 5-32. Input Amplifier Adjustment

Low Frequency Response Adjustment

1. Program 8182A/B Standard Set (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 10Hz squarewave and 2.5V amplitude into 50 Ohm
3. Connect equipment as shown in measurement set up.

4. Connect scope probe to TP1 and GND TP without using a ground lead. (Remove insulating sleeve from probe.)

5. Set scope to (Autoscale > Chan 1 > Volts/Div > 100mV)

6. Adjust A5 (A65) R2 for the best pulse response.

High Frequency Response Adjustment

7. Set Pulse Generator to 10MHz squarewave and 2.5V amplitude into 50 Ohm, risetime <3ns)

8. Connect equipment as shown in measurement set up.

9. Connect scope probe to TP1 and GND TP without using a ground lead.

10. Set scope to: (Autoscale > Chan 1 > Volts/Div > 100mV)

11. Adjust A5 (A65) C1 for the best pulse response.

Data Input Amplifier Offset Adjustment

Equipment:

Scope	HP 54100D
Active Pods	HP 54001A
Pulse Generator	
BNC Tee Connector	1250-0781
BNC scope probe adapter	1250-1454
50 Ohm Feedthrough	HP 10100C
Clock Probe	HP 15406A
DATA Probe	HP 15407A
Grabber	HP 5408A

Measurement setup:

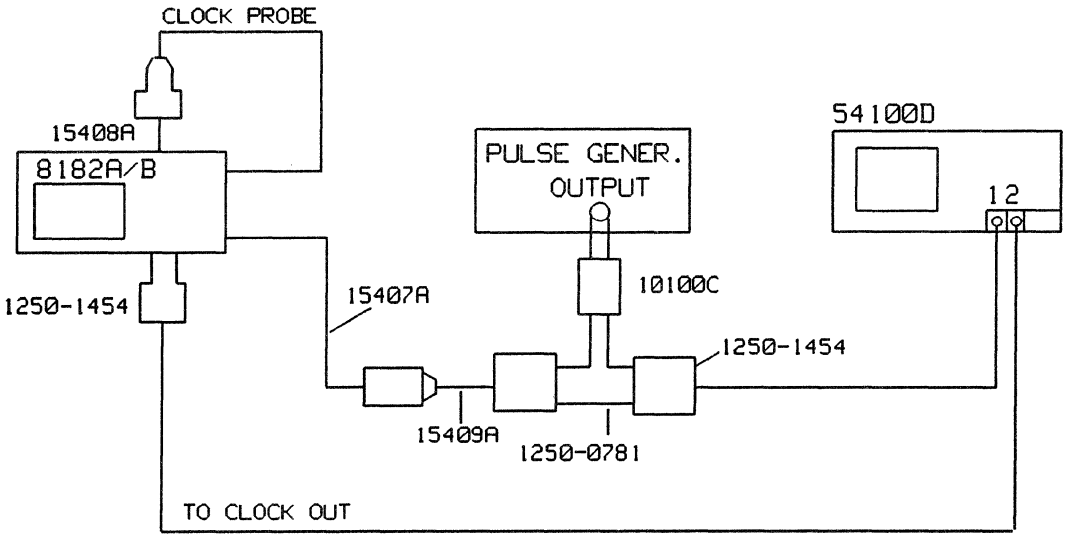


Figure 5-33. Data Input Amplifier Offset Adjustment

1. Set Pulse Generator to:

Period	1 ms
Pulse Width	0.5 ms

Amplitude	200 mV
Offset	On
Transition Time	5 - 250 µs

2. Adjust Leading Edge and Trailing Edge for a triangular waveform. Using the offset vernier, set the triangular signal to be symmetrical about the center graticule line.

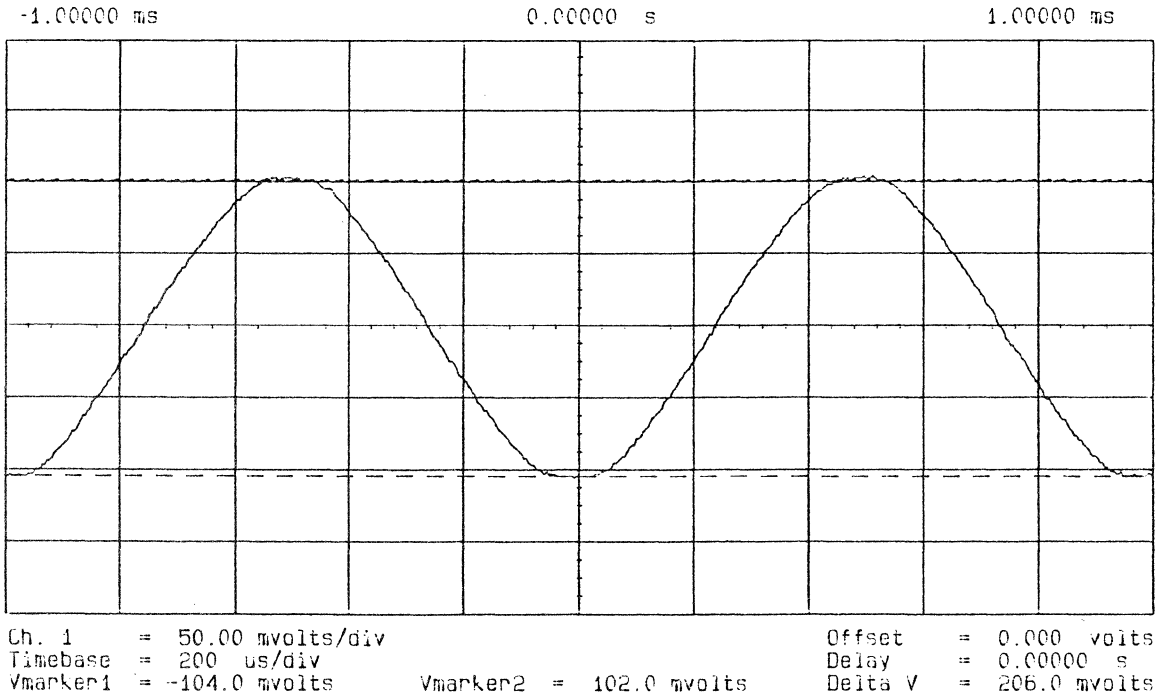


Figure 5-34. Data Input Amplifier Offset Adjustment - Scope Display 1

3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

4. Clock Slope Both; Clock Threshold -1.3 V: (Pages > Control > Clock > Clock Slope > Both Slps > Exit > Clock Thres > -1.3V)

5. Label A Single Threshold 0V: (Pages > Input > Threshold > 0 > Volt)

6. Connect equipment as shown in measurement set up.

7. Connect Clock Probe to A5 (A65) TP5.

8. Set scope to: (Autoscale > Trigger > Trigger source to Chan 2 > Chan 2 > Chan 2 Display to Off > Display > Split Screen to Off > Number of Averages to 2 > Timebase > 100ns > Chan 1 > Chan 1 Mode to Magnify > Magnify to On > Volts/Div > 10mV

10. Adjust A5 (A65) R1 until the displayed band of dots is symmetrical to the center graticule line.

Adjustments for all other data channels are listed in the Adjustment Summary.

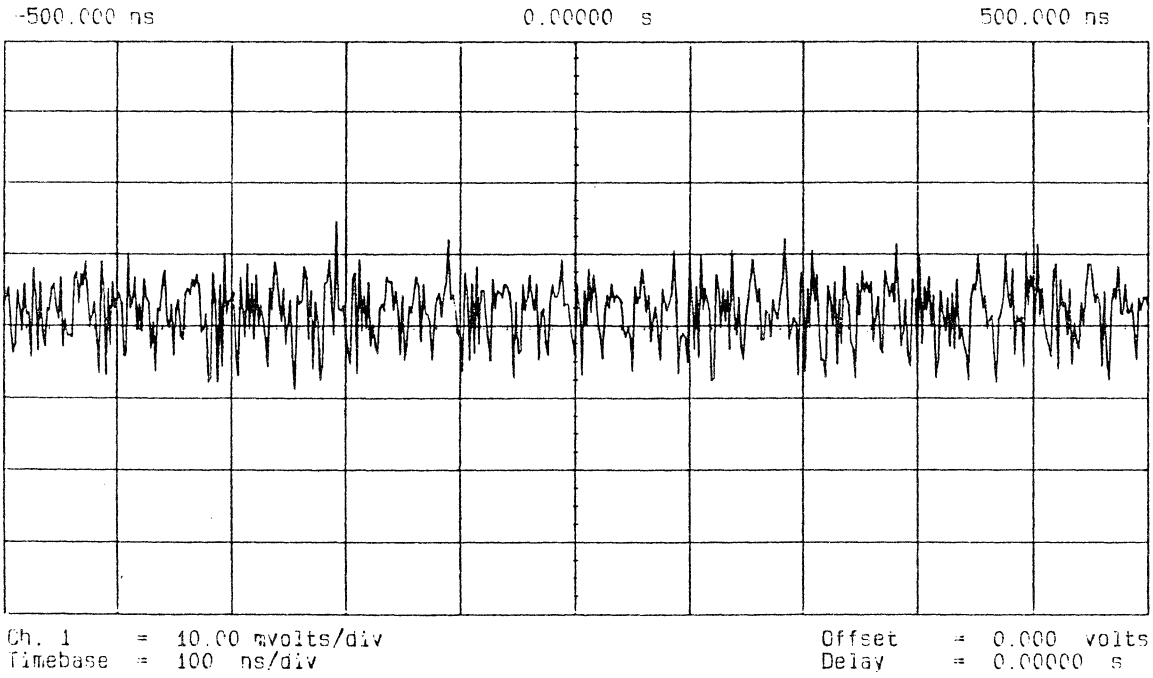


Figure 5-35 Data Input Amplifier Offset Adjustment - Scope Display 2

Dual Threshold Adjustment

Equipment:

BNC Adapter (15409A) with 50 Ohm Feedthrough (10100C)
Solder in receptacles wired to short probe inputs
15407 Data Probe Assembly

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

2. Clock Source Internal; Clock Period 1ms: (Pages > Control > Clock > Clock Source > Internal > Exit > Clock Period > Fast Increase [1ms])

3. Auto Arming Delay 0s: (Pages > Control > Autoarming > Delay 0s)

4. Stop Delay 40: (Pages > Control > Stop > Stop Delay > 40 > Enter Number)

5. Glitch Detect On: (Pages > Control > Glitch Detect > On)

6. Lower Level -0.10V; Upper Level 0.00V: (for Label A) (Pages > Input > Threshold > Sing/upp/low [to lower] > 0.1 > Volt > Sing/upp/low [to upper] > 0 > Volt)

7. Dual Threshold for all available connectors: (Pages > Input > Connector > 0 and 1 > Dual Thres > Execute > Exit > [2 and 3] > Dual Threshold > Execute > Exit)

8. Timing Diagram: (Pages > Timing Diagr)

9. Press RUN.

Adjustment Channels 0 to 3 Connector 0

10. Connect 15407A Data Probe Assembly to Connector 0.

11. Terminate probe of channel to be adjusted (0) with 50 Ohm or short all probe inputs by using wired 15426A solder in receptacles.

12. Adjust A5 (A65) R9 for channel 0 on Data Board 0 until the timing display for Connector 0 Channel 0 toggles and maximum glitches are displayed.

13. Adjust R10 for channel 1 connector 0 on Data Board 0.

14. Adjust R9 for channel 2 connector 0 on Data Board 1.

15. Adjust R10 for channel 3 connector 0 on Data Board 1.

Adjustments for all channels are listed in the Adjustment Summary at the end of this section.

NOTE

When adjusting data channels on connector 6, move the Timing Diagrams Page display upwards until the required channel is displayed. With Timing Diagram selected press: (Select Displ > Vert Window).

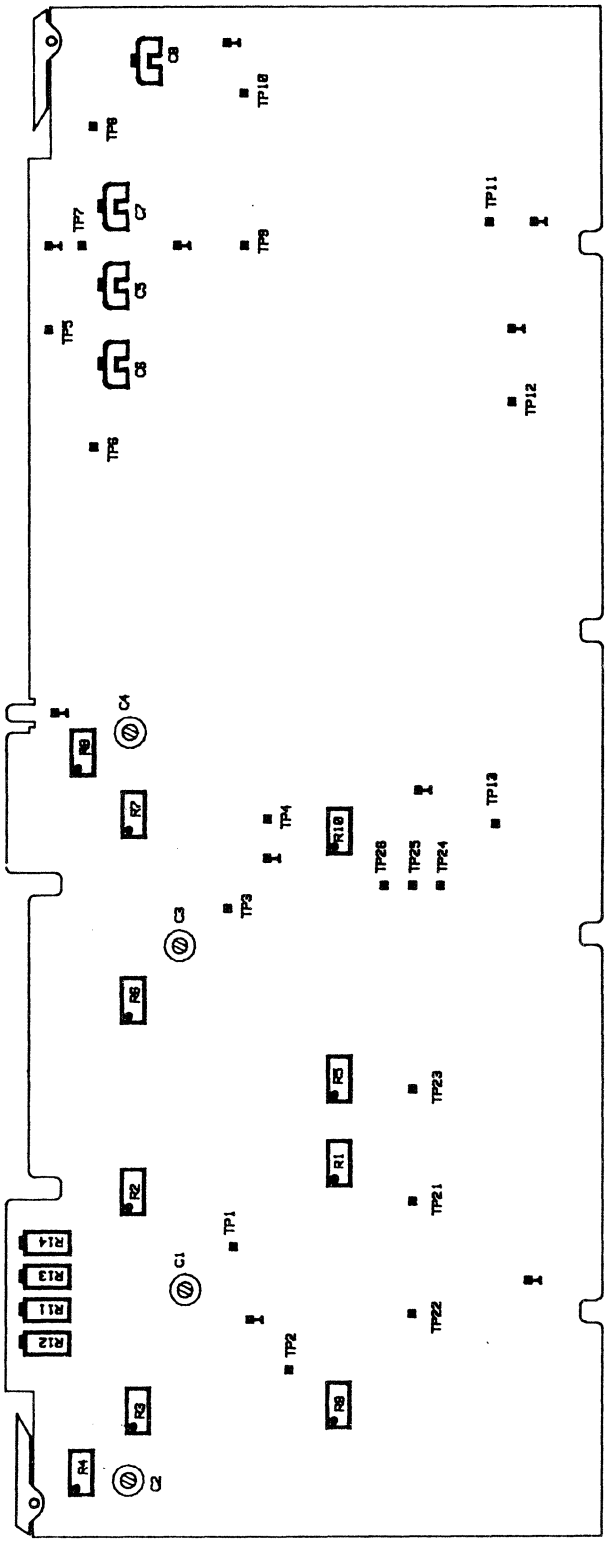


Figure 5-36. A65 Data Board

5-10 Sampling Point Adjustment

Equipment:

Pulse Generator	
Delay Line 3 ns	08182-61621
BNC Adapter	15409A
BNC Adapter (female/female)	1250-0080
BNC Tee Adapter	1250-0781
Clock Probe	15406A
Data Probe	15407A

NOTE

The offset adjustment for line drivers A65 U108, A65 U208, A65 U308 and A65 U408 on the Data Board 08182-66565 can only be performed at the factory. Therefore **never try to adjust A65 R11, A65 R12, A65 R13 and A65 R14.**

Measurement setup:

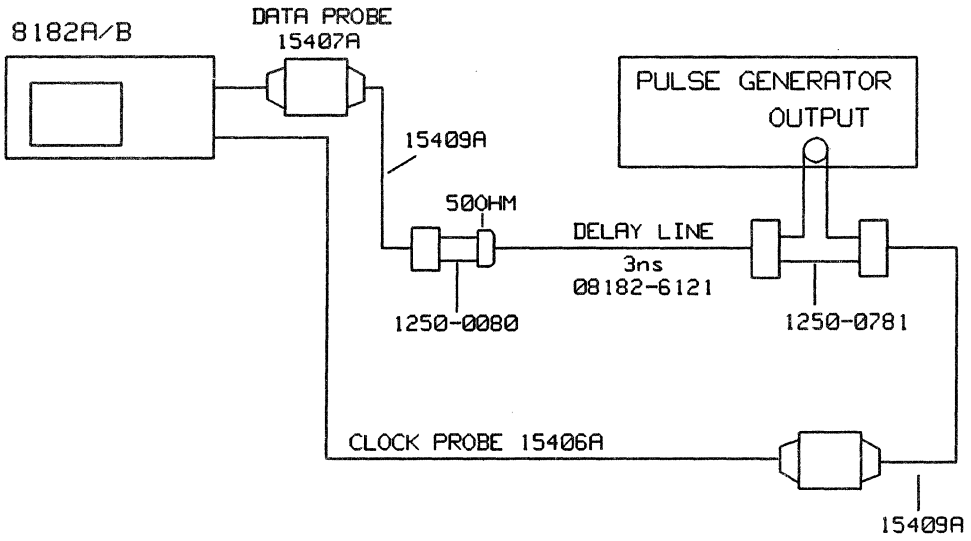


Figure 5-37. Sampling Point Adjustment

1. Set Pulse generator to:

Period	1 µs
Pulse Width	0.5 µs
Leading Edge	< 3 ns
Trailing Edge	< 3 ns
HIL	2 V
LOL	0 V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
3. Clock Threshold to +1 V: (Pages > Control > Clock > Clock Thres > 1 > Volt)
4. Label A Single Threshold to +1 V: ((Pages > Input > Threshold > Sing/Upp/Low[to Single Thres] > 1 > Volt)

5. Stop Delay to 40: (Pages > Control > Stop > Stop Delay > 40 > Enter Number)

6. Autoarming Delay 0s: (Pages > Control > Autoarming > Delay 0s)

7. Select Timing Diagrams: (Pages > Timing Diagram > Select Displ > Vert Window > <- or -> [until the required channel is displayed])

8. Using a mixed display, set Clock Delay to 3 ns: (Softkeys > Control > Clock > Clock Delay > 3 > Nanosec)

9. Connect equipment as shown in measurement set up and press RUN.

10. Using the Increment Softkey check first for a toggling action from low to high and note reading. If the signal does not toggle between 2 ns and 4 ns, perform Sampling Point Pre-adjustment.

11. Program Clock Slope Neg and select the Clock Delay softkey again: (Exit > Clock > Clock Slope > Neg Slope > Exit > Clock Delay)

12. Vary clock delay between 1 ns and 5 ns by pressing decrement and increment softkeys and note the delay when signal toggles from high to low.

13. Calculate delta between delay noted in step 10 (Clock Pos) and delay noted in step 12 (Clock Neg).

14. With negative Clock Slope selected set Clock Delay to 3 ns plus half of the delta delay calculated in step 13.

    Example:

    With Clock Slope Pos, signal switches from low to high at 1.8 ns. With Clock slope Neg, signal switches from high to low at 2.4 ns, Delta is 600 ps. Set Clock Delay to 3 ns plus 300ps = 3.3 ns.

15. Adjust A5 (A65) C5 until the signal toggles from high to low.

16. Reselect Clock Slope Pos: (Exit > Clock Slope > Pos Slope > Exit > Clock Delay)

17. Check that signal toggles between 2 ns and 4 ns. If signal does not toggle repeat the procedure from step 10.

NOTE

If the sampling point specifications cannot be reached by adjusting C5 it might be necessary to readjust the internal clock delay on the A6 clock board or to change the taps of delay line DL107 to DL407 on the Data Board.

Sampling Point Pre-adjustment (DL107, DL207, DL307 and DL407)

1. First check the sampling point of channels on the boards that have not been exchanged. If these channels are not in specifications refer to A6 Fixed Delay Adjustment.

2. If the other channels meet specifications, delayline DL107 [DL207, DL307, DL407] on the Data Board must be pre-adjusted.

3. Use the test set up and equipment settings as described under sampling point adjustment with the addition of a scope (54100D).

4. Trigger the scope with the pulse generator and connect the channel 1 probe to TP 5 on the DATA Board 0 (connector 0, channel 0)

5. Adjust A5 (A65) C5 for minimum delay as observed on scope.

6. Increment the clock delay from 0 ns onwards in 0.1 ns steps until the timing signal toggles, and note the delay difference to 3 ns.

7. The time difference between 3 ns and the noted delay setting is the required change in the setting of delayline DL107. Delay between two taps of the delay line is 1 ns; the delay range of A5 (A65) C5 is 0-1 ns.

Examples:

1. Minimum clock delay setting where the timing display can be forced to toggle is 1.3 ns. Time difference between 1.3 ns and 3 ns is 1.7 ns
   Required action: Add 1 ns delay (1 tap) at DL107 and adjust A5 (A65) C5 to 0.7 ns.

2. Minimum clock delay setting where the timing display can be forced to toggle is 5.3 ns. Time difference between 5.3 ns and 3 ns is 2.3 ns.
   A5 (A65).
   Required action: Advance data by 3 ns (- 3 taps) at DL107 and adjust C5 to +0.7 ns.

Table 5-2. 8182A/B Adjustments necessary after Board Change/Repair

BOARD	EXCH. P/N	ADJUSTMENT (CHECK)	PAGE
Display		Display Adjustment	5-1
A1 MPU Board *	08182-69501	Restart Circuit	5-6
A2 Interface Bd.	08182-69502	D-A Converter Internal Clock Generator	5-8
A3 Address Bd.	08182-69503	Trigger Arm Amplifier Freq. Response/Offset	5-10
		Stop Amplifier Freq. Response/Offset	5-11
A4 Control Board	08182-69504	Trigger Qualifier Amp. Freq. Response/Offset	5-13
		Control Outputs	5-13
A5 Data Board	08182-69506	Input Amplifier Adjustment LF Response/HF Response/Offset Dual Threshold	5-38 5-41
		Sampling Point	5-44
		Delay Line Preadjustment (Check Fixed Delay)	5-45
		Adjustments Summary	5-47
A6 Clock Board	08182-69506	Offset of Clock Output Circuit	5-16
		Timing IC Supply	5-16
		Clock Amplifier LF Response/HF Response	5-16
		Clock Amp. Offset Adjustment	5-18
		Clock Qual. Frequency Response	5-21
		Clock Qual. Offset Adjustment	5-23
		Fixed Delay	5-27
		Clock Delay	5-30
		Clock Width	5-32
		Adjustment Summary	5-36

(*) Version A only.

Table 5-3. 8182A/B Data Board Adjustments Summary

CONN-ECTOR	CHANNEL PROBE	DATA BOARD	LF(10Hz) TEST PT.	ADJ. LF	HF(10MHz) TEST PT.	ADJ. HF	OFFSET ADJUST	DUAL THR-ES. ADJUS	DELAY LINE	DELAY ADJ.
0	0	0	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
0	1	0	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
0	2	1	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
0	3	1	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
1	0	0	TP2	R4	TP2	C2	R3		DL207	TP6 C6
1	1	0	TP4	R8	TP4	C4	R7		DL407	TP8 C8
1	2	1	TP2	R4	TP2	C2	R3		DL207	TP6 C6
1	3	1	TP4	R8	TP4	C4	R7		DL407	TP8 C8
2	0	2	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
2	1	2	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
2	2	3	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
2	3	3	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
3	0	2	TP2	R4	TP2	C2	R3		DL207	TP6 C6
3	1	2	TP4	R8	TP4	C4	R7		DL407	TP8 C8
3	2	3	TP2	R4	TP2	C2	R3		DL207	TP6 C6
3	3	3	TP4	R8	TP4	C4	R7		DL407	TP8 C8
4	0	4	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
4	1	4	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
4	2	5	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
4	3	5	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
5	0	4	TP2	R4	TP2	C2	R3		DL207	TP6 C6
5	1	4	TP4	R8	TP4	C4	R7		DL407	TP8 C8
5	2	5	TP2	R4	TP2	C2	R3		DL207	TP6 C6
5	3	5	TP4	R8	TP4	C4	R7		DL407	TP8 C8
6	0	6	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
6	1	6	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
6	2	7	TP1	R2	TP1	C1	R1	R9 TP6	DL107	TP5 C5
6	3	7	TP3	R6	TP3	C3	R5	R10 TP8	DL307	TP7 C7
7	0	6	TP2	R4	TP2	C2	R3		DL207	TP6 C6
7	1	6	TP4	R8	TP4	C4	R7		DL407	TP8 C8
7	2	7	TP2	R4	TP2	C2	R3		DL207	TP6 C6
7	3	7	TP4	R8	TP4	C4	R7		DL407	TP8 C8

Note that the testpoints in column "DELAY ADJ." are also to be used for "OFFSET ADJUST".

Table 5-4. 8182A/B Data Connector Adjustments Summary

DATA BOARD	CONNEC-TOR	PROBE, CHANNEL	TEST POINT	LF ADJUST 10 Hz	HF ADJUST 10MHz	OFFSET ADJUST	DUAL THRES-HOLD ADJUST	DELAY ADJUST
0	0	0	TP1	R2	C1	R1	R9 TP6	TP5 C5
	0	1	TP3	R6	C3	R5	R10 TP8	TP7 C7
	1	0	TP2	R4	C2	R3		TP6 C7
	1	1	TP4	R8	C4	R7		TP8 C8
1	0	2	TP1	R2	C1	R1	R9 TP6	TP5 C5
	0	3	TP3	R6	C3	R5	R10 TP8	TP7 C7
	1	2	TP2	R4	C2	R3		TP6 C6
	1	3	TP4	R8	C4	R7		TP8 C8
2	2	0	TP1	R2	C1	R1	R9 TP6	TP5 C5
	2	1	TP3	R6	C3	R5	R10 TP8	TP7 C7
	3	0	TP2	R4	C2	R3		TP6 C6
	3	1	TP4	R8	C4	R7		TP8 C8
3	2	2	TP1	R2	C1	R1	R9 TP6	TP5 C5
	3	3	TP3	R6	C3	R5	R10 TP8	TP7 C7
	2	2	TP2	R4	C2	R3		TP6 C6
	3	3	TP4	R8	C4	R7		TP8 C8
4	4	0	TP1	R2	C1	R1	R9 TP6	TP5 C5
	5	1	TP3	R6	C3	R5	R10 TP8	TP7 C7
	4	0	TP2	R4	C2	R3		TP6 C6
	5	1	TP4	R8	C4	R7		TP8 C8
5	4	2	TP1	R2	C1	R1	R9 TP6	TP5 C5
	5	3	TP3	R6	C3	R5	R10 TP8	TP7 C7
	4	2	TP2	R4	C2	R3		TP6 C6
	5	3	TP4	R8	C4	R7		TP8 C8
6	6	0	TP1	R2	C1	R1	R9 TP6	TP5 C5
	7	1	TP3	R6	C3	R5	R10 TP8	TP7 C7
	6	0	TP2	R4	C2	R3		TP6 C6
	7	1	TP4	R8	C4	R7		TP8 C8
7	6	2	TP1	R2	C1	R1	R9 TP6	TP5 C5
	7	3	TP3	R6	C3	R5	R10 TP8	TP7 C7
	6	2	TP2	R4	C2	R3		TP6 C6
	7	3	TP4	R8	C4	R7		TP8 C8

Note that the testpoints in column "DELAY ADJ." are also to be used for "OFFSET ADJUST".

5-11 Locating components in the 8182A Data Analyzer

The following diagrams should be used when locating components/testpoints in the HP 8182A Data Generator.

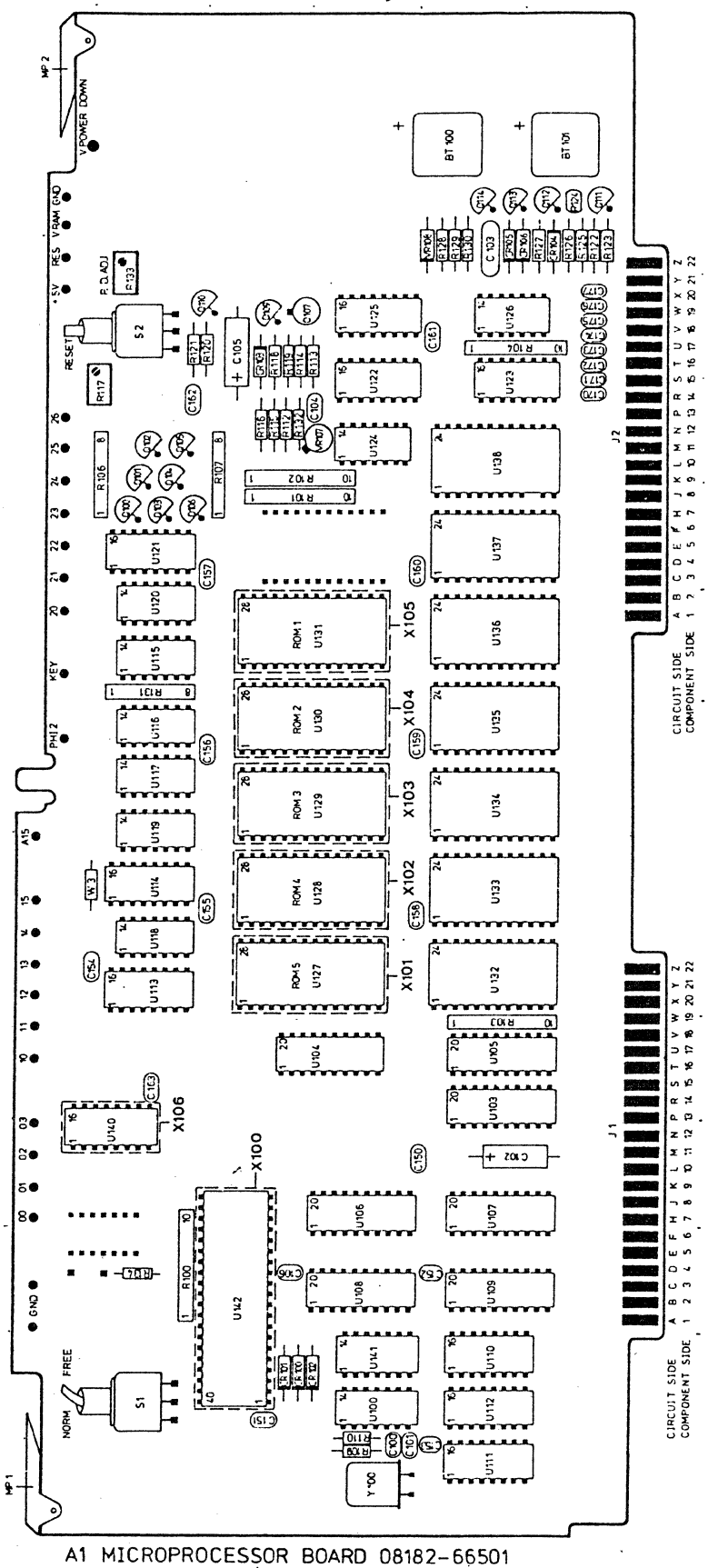


Figure 5-38. A1 Microprocessor Board

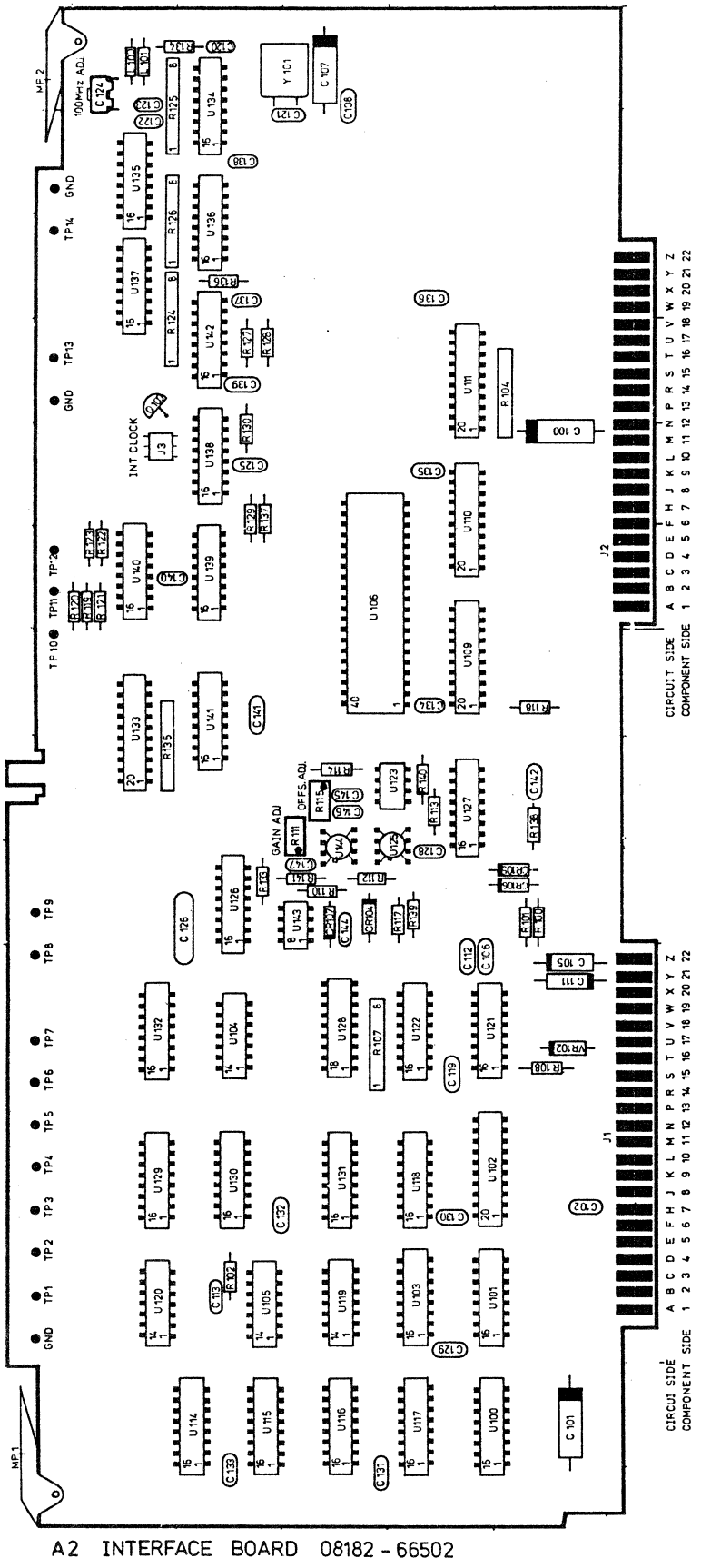


Figure 5-39. A2 Interface Board

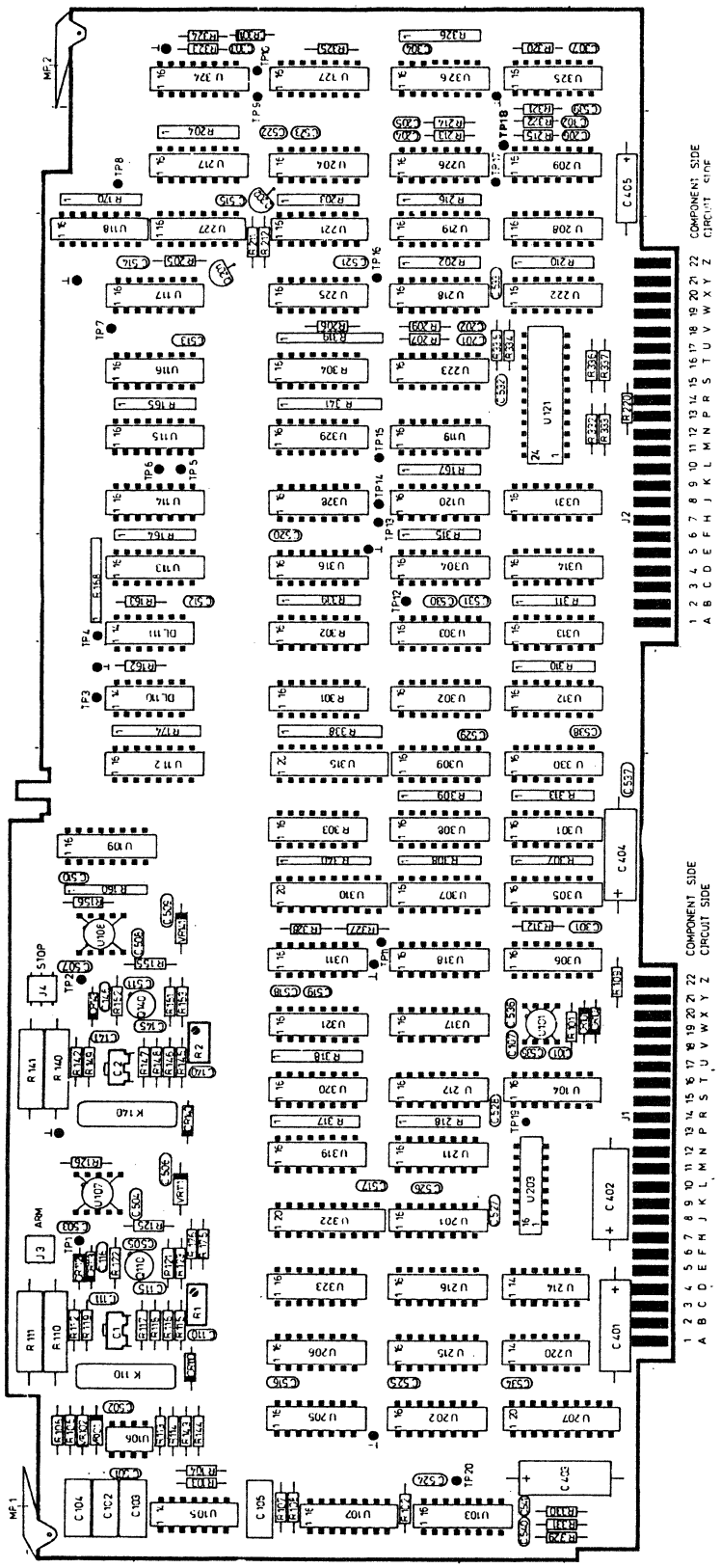


Figure 5-40. A3 Address Board

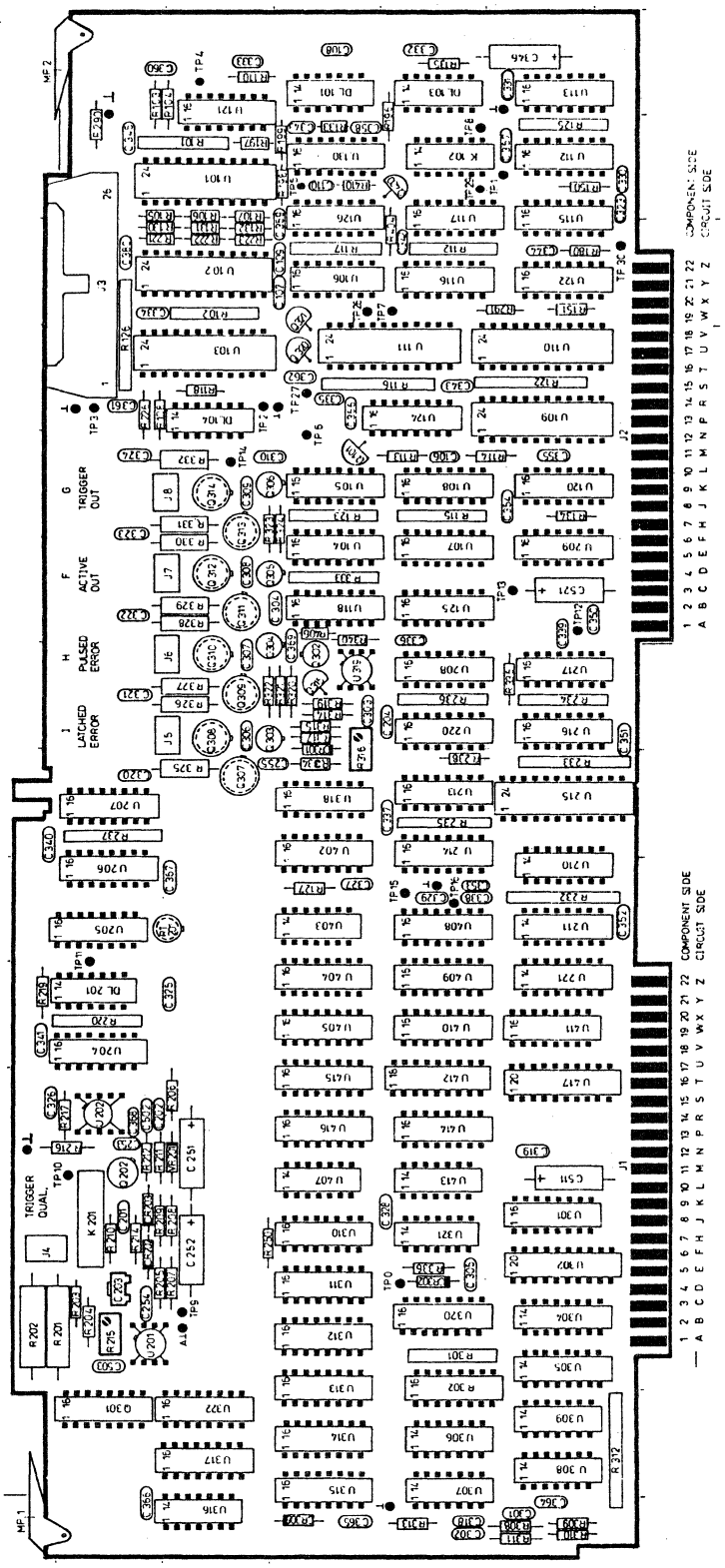


Figure 5-41. A4 Control Board

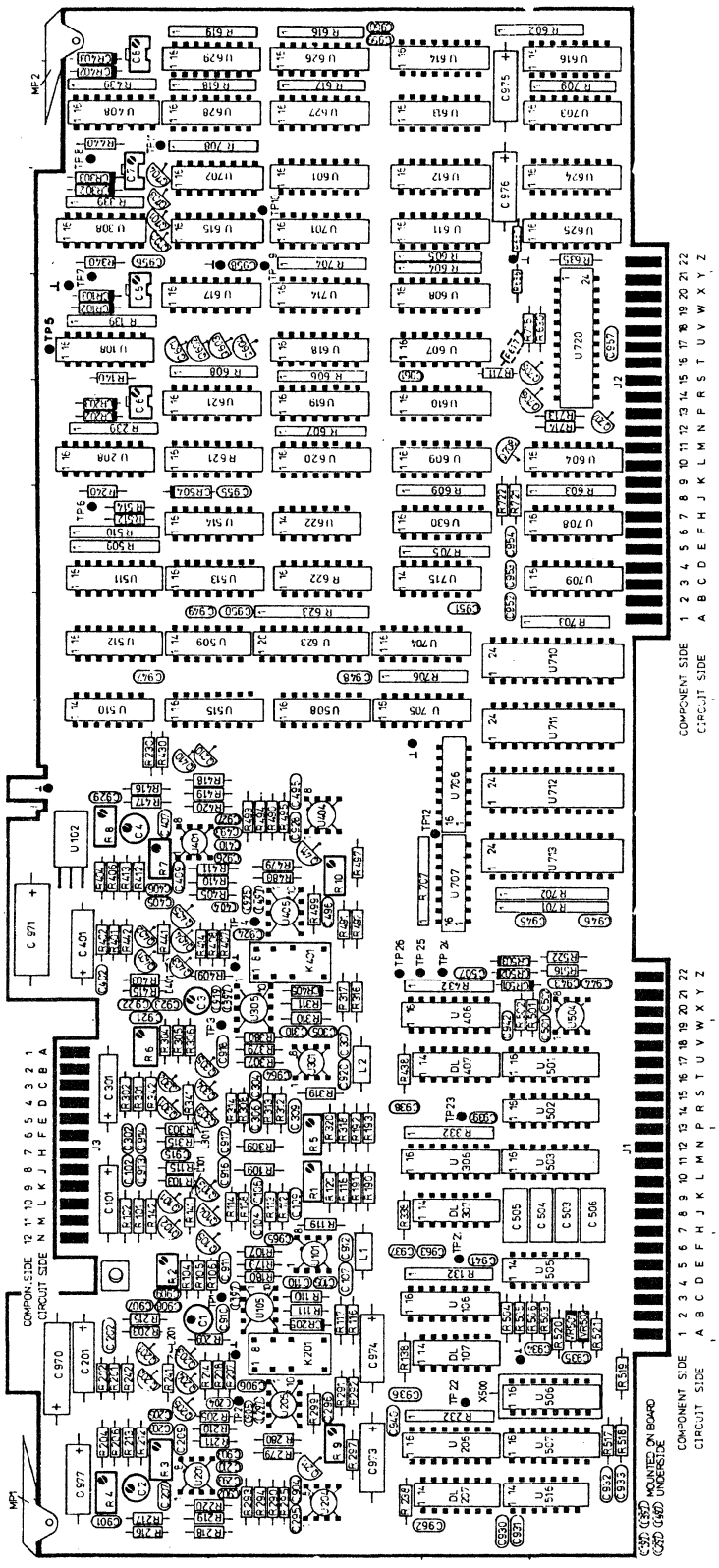
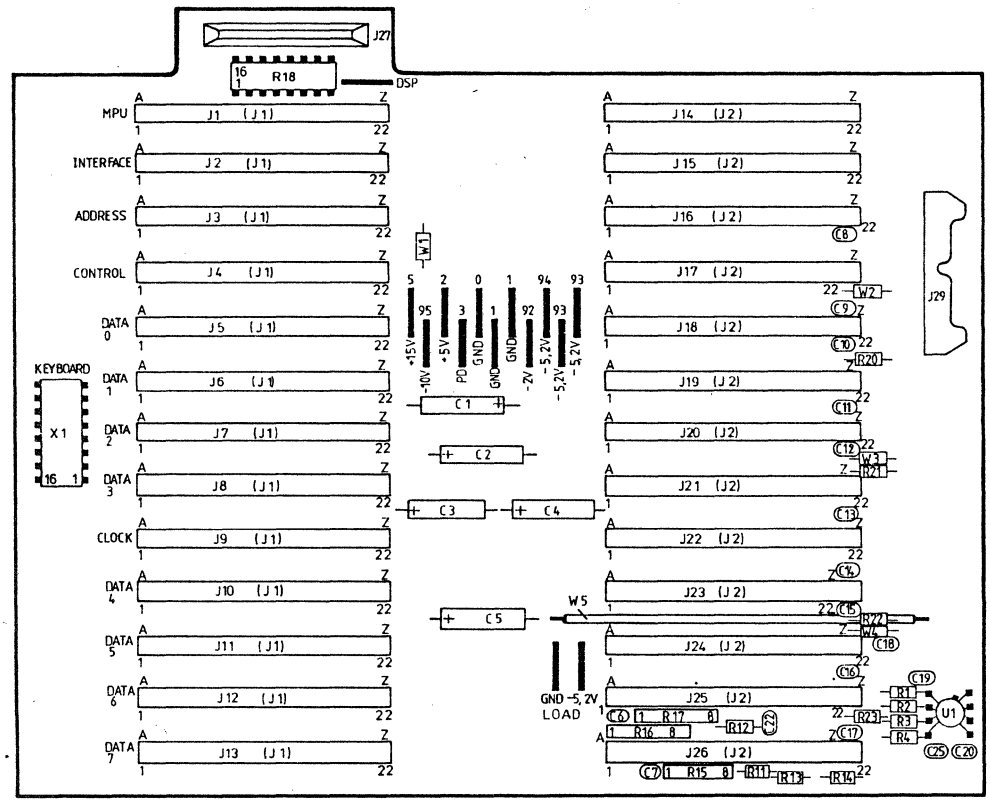


Figure 5-42. A5 Data Board



A7 MOTHERBOARD 08182-66507

Figure 5-43. A7 Mother Board

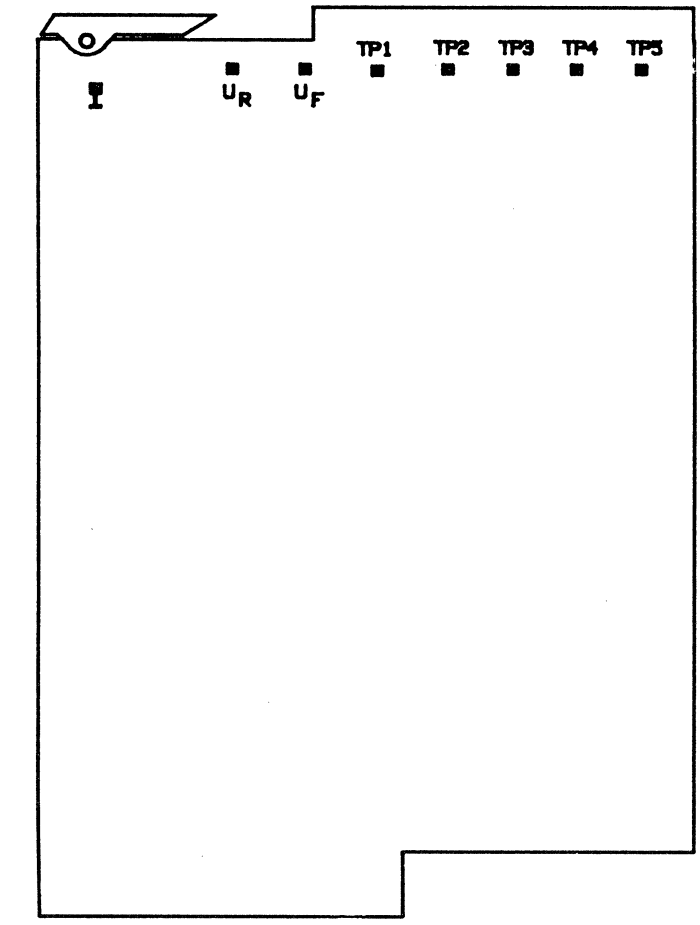


Figure 5-44. A24 Post Regulator Board

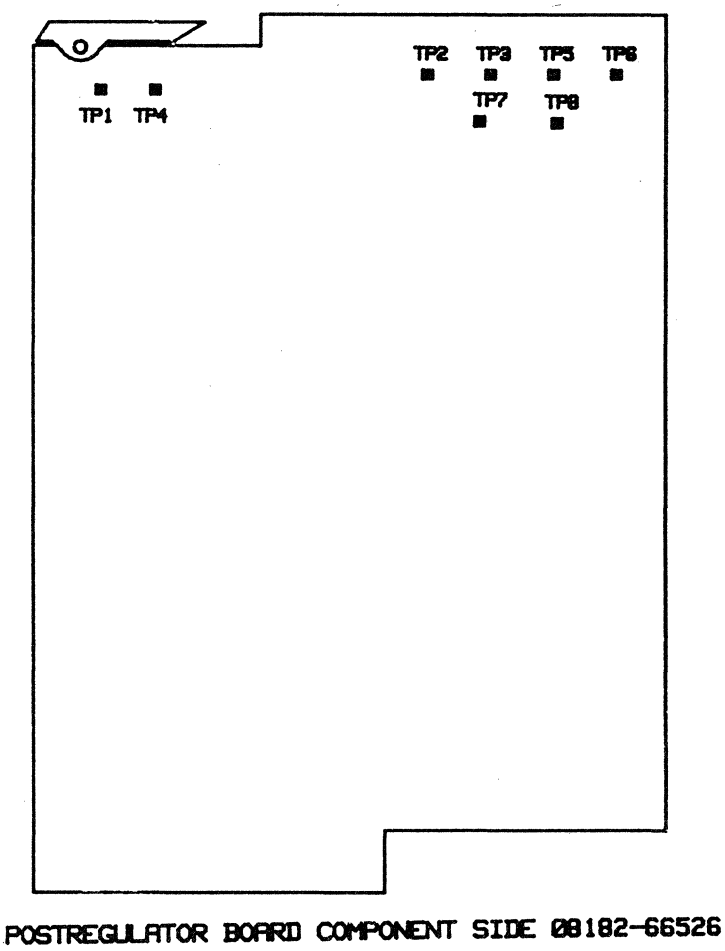
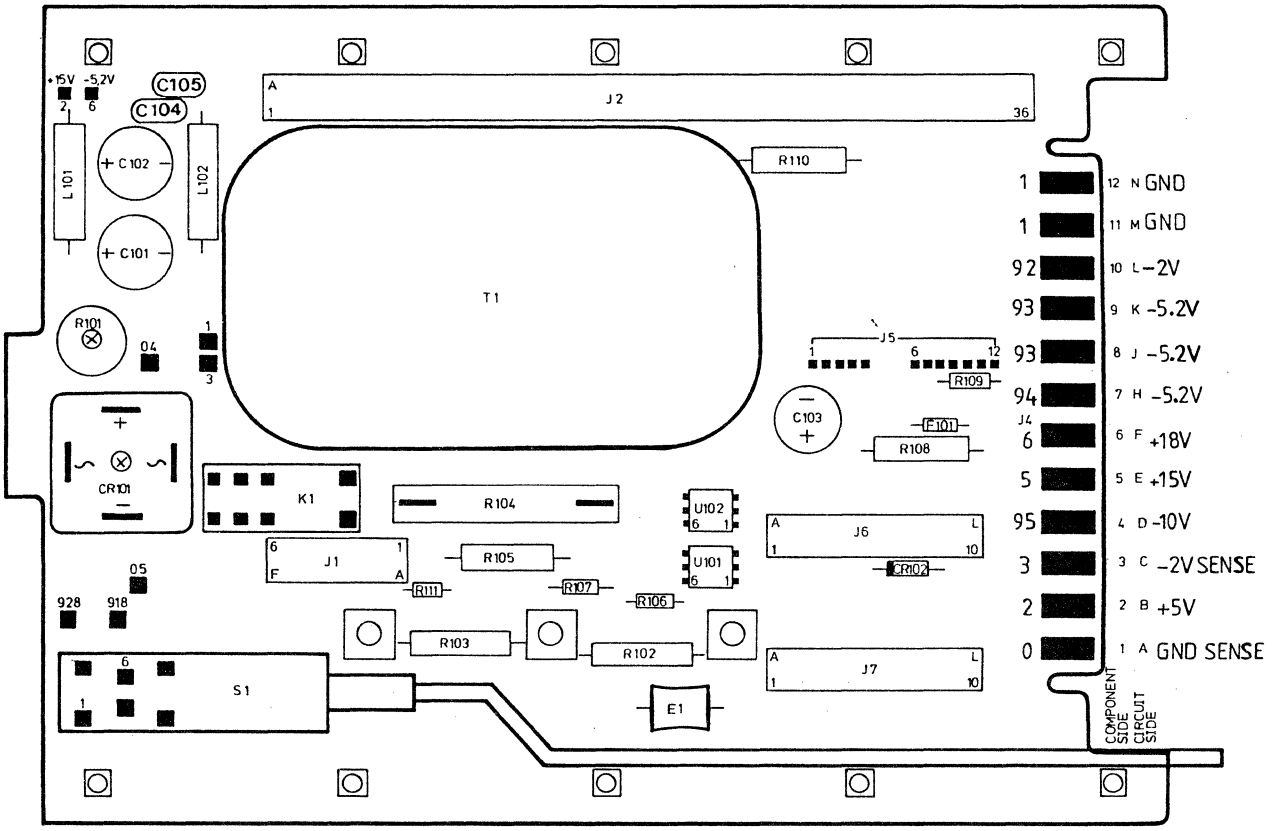
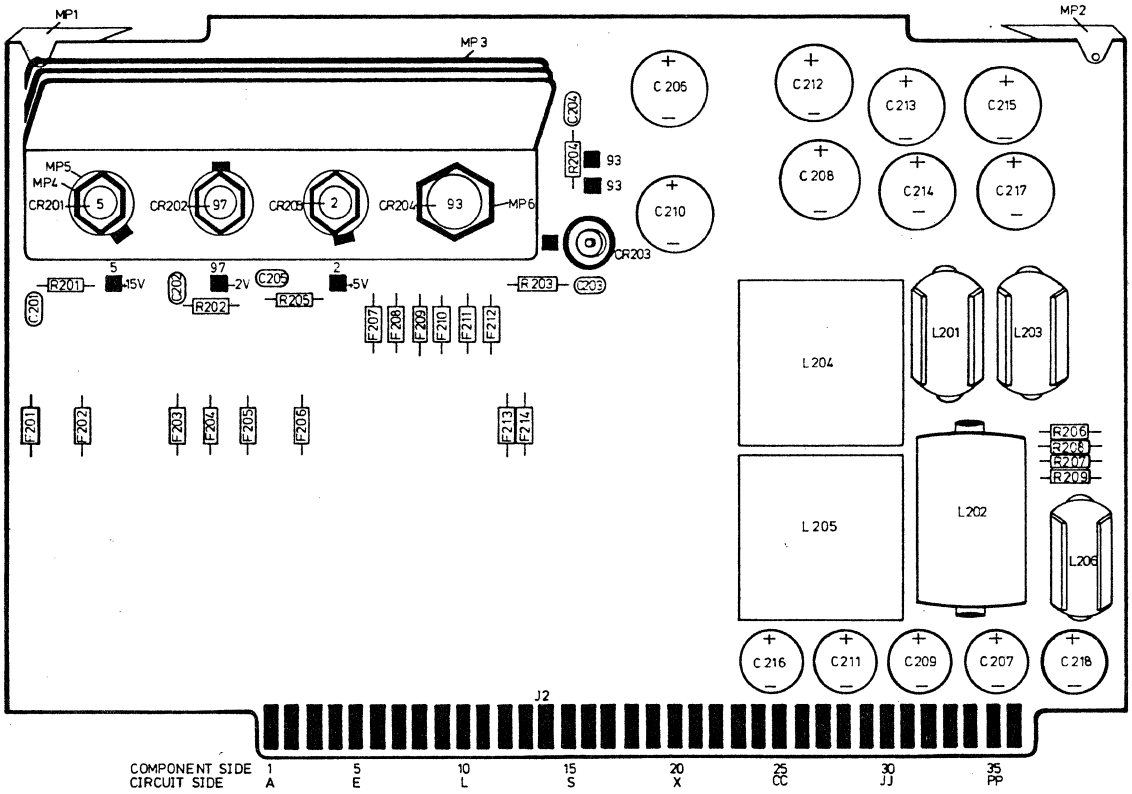


Figure 5-45. A26 Post Regulator Board



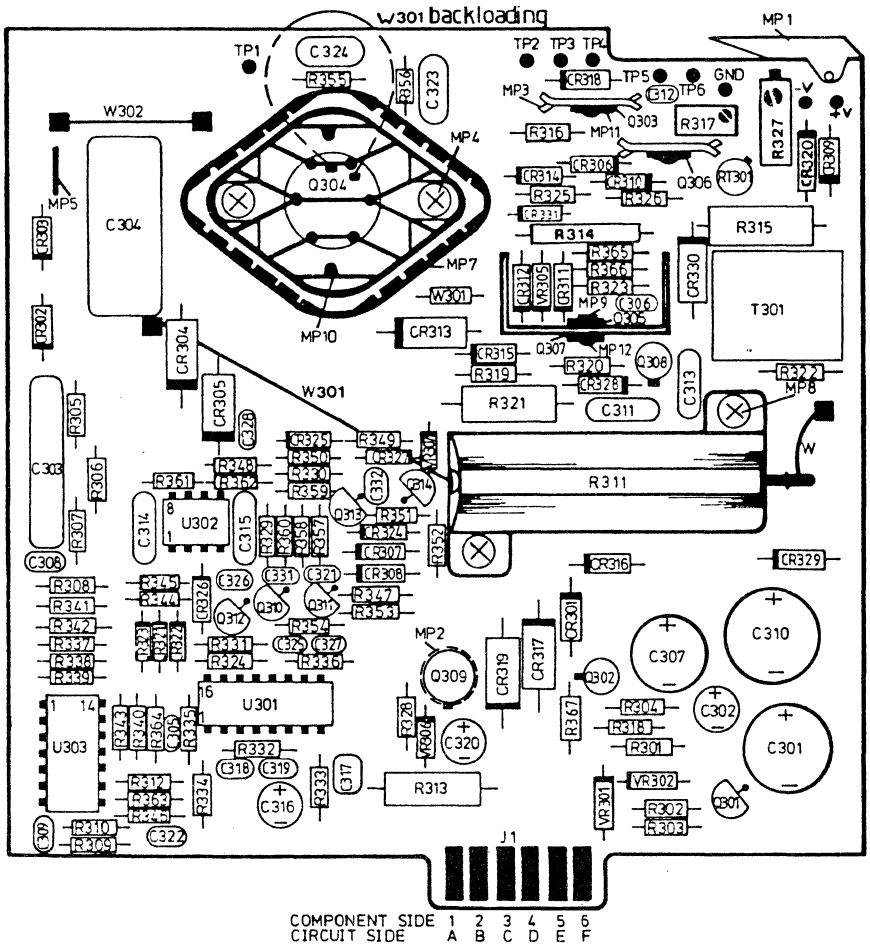
A 21 MOTHERBOARD POWER SUPPLY 08182-66521

Figure 5-46. A21 Power Supply Mother Board



A 22 RECTIFIER BOARD 08182-66522

Figure 5-47. A22 Rectifier Board



SWITCHING CONTROL BOARD 08182-66523

Figure 5-48 A23 Switching Board

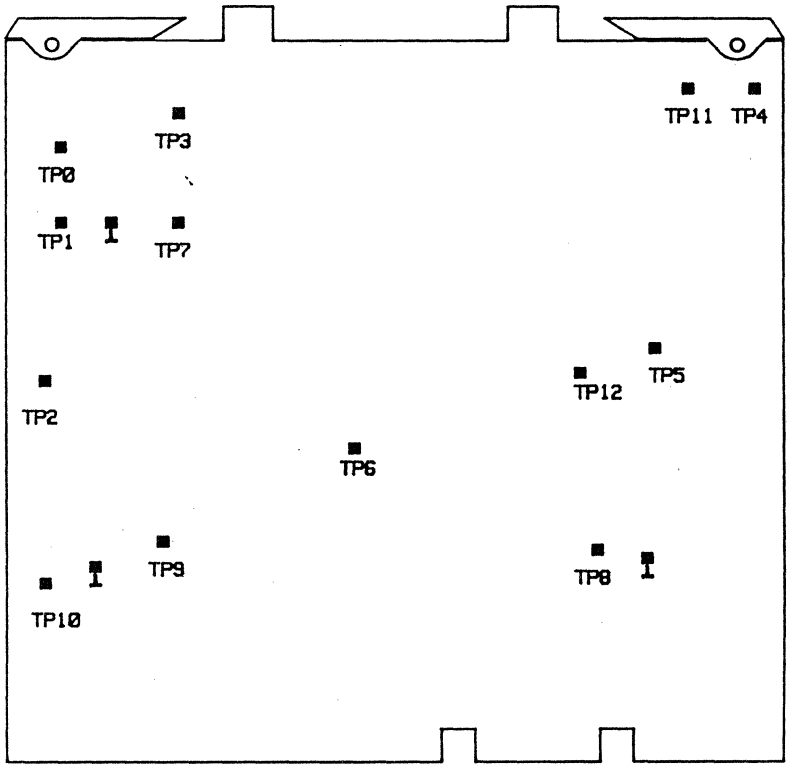


Figure 5-49. A30 Control Board

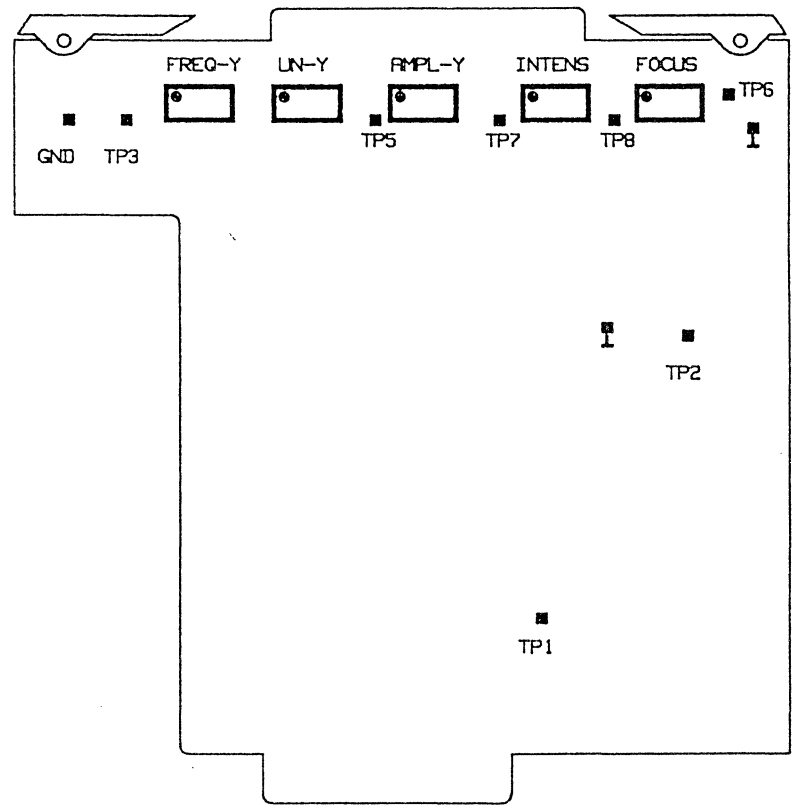


Figure 5-50. A32 Vertical Deflection Board

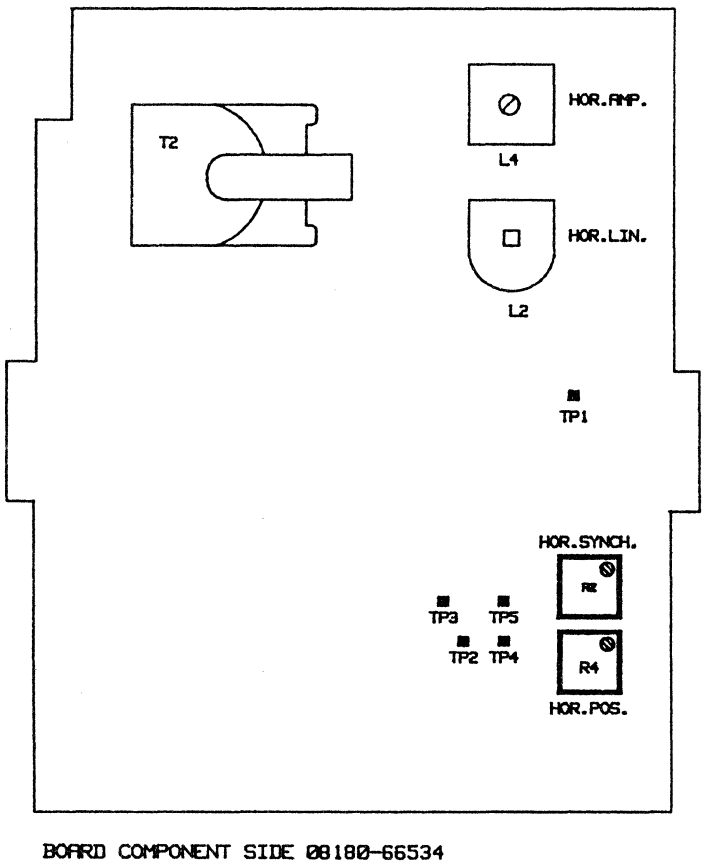


Figure 5-51. A34 Horizontal Deflection Board

Chapter 6
HP 8180A/B Performance Verification

6-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications for the HP 8180A/B Data Generator and the HP 8181A/B Data Generator Extender given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place. The tests must be performed in the order given.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

6-2 Cycle Modes / Run / Stop / Break / Forward / Back Tests

For testing the different cycle modes, a low frequency (10Hz) is used in order to be able to follow the address changes on the 8180A/B display. The external gate signal is simulated by changing the threshold level of the RUN/GATED input. First and last address detection at maximum speed is tested separately.

1. Program 8180A/B Standard Set.
   (PAGES, [illegible] , [illegible] , [illegible])

2. Clock Frequency 10 Hz.
   (PAGES, [illegible] , [illegible] , 10, [illegible])

3. Last Address 100.
   (PAGES, [illegible] , [illegible] , 100, [illegible])

Auto Cycle Test

4. Press RUN and check that the 8180A/B starts with address 00000 (upper right hand corner of the display), counts up to address 00100 and continues with address 00000.

Break; Forward; Back; Stop Test

5. Press **BREAK**. The 8180A/B should switch to BREAK.

6. Increment and decrement addresses by pressing **FWD** and **BACK**. Note that addresses can be decremented down to the First Address.

7. Press **RUN**. The 8180A/B should start one address after the Break Address.

8. Press **STOP** and **RUN**. The 8180A/B should start with the First Address.

Single Cycle Test

9. Program the 8180A/B to Single Cycle.
(PAGES, CONTROL , Cycle Mode , SINGLE)

10. Press **RUN** and check that the 8180A/B starts at address 00000 and stops at address 00100.

Gated Cycle Test

11. Program the following: Gated Cycle; Run (Gate) Input ON; Threshold +5V.
(PAGES, CONTROL , Cycle Mode , Gated , EXIT ↑ .
Inputs , Run Input , ON ↑ , EXIT ↑ .
Threshold , 5, VOLT)

12. Set threshold voltage to -5V (-, 5, VOLT). The 8180A/B should run between address 00000 and 00100 as in Auto Cycle.

13. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Gated Cycle Test

14. Program Init+Gated.
(PAGES, CONTROL , Cycle Mode , INIT+GATED)

15. First Address 30.
(PAGES, CONTROL , First Address , 30, ENTER NUMBER)

16. Input Threshold +5V.
(PAGES, CONTROL , Inputs , Threshold , 5, VOLT)

17. Program the threshold voltage to -5V (-, 5, VOLT) and check that the 8180A/B starts with address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.

18. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Auto Cycle Test

19. Program Init+Auto.
(PAGES , CONTROL , Cycle Mode , Init+Auto)

20. Run Input OFF.
(PAGES , CONTROL , Inputs , Run Input , OFF)

21. Press **RUN** and check that the 8180A/B starts at address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.

    To repeat the whole sequence press **STOP** and **RUN** again.

6-3 Last Address (Address Difference Counter) Test

This test ensures correct programmability of the address difference counters and proper operation up to 50 MHz.

1. Program 8180A/B Standard Set.
   (PAGES, Store/Recal , RCL Std Set , EXECUTE)

2. Clock 2 Delay to 0ns, Clock 1 Width to 10ns.
   (PAGES, TIMING , Clock Timing , Clock 2 Delay , 0, NANOSEC ,
   EXIT MT , Clock 1 Width , 10, NANOSEC)

3. Clock Frequency 50 MHz.
   (PAGES, TIMING , Frequency , 50, MEGAHERTZ)

4. Single Cycle.
   (PAGES , CONTROL , Cycle Mode , SINGLE)

5. Last Address 00001.
   (PAGES , CONTROL , Last Address , 1, ENTER NUMBER)

6. Press **RUN** and check that the 8180A/B stops at address 00001.

7. Change Last Address to 2 (2, ENTER NUMBER) press **RUN** and check cycle length.

8. Repeat Single Cycle test with the following Last Address settings:
   8; 16; 32; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.

6-4 Strobe Break (Strobe Difference Counter) Test

Correct programmability and proper strobe difference counter function at 50 MHz is verified with this test. After setting the Strobe Breaks, the instrument is stepped from Break to Break.

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALL , Rcl Std Set , EXECUTE)

2. Clock 2 Delay to 0ns, Clock 1 Width to 10ns.
   (PAGES, TIMING , Clock Timing , Clock 2 Delay , 0, NANOSEC ,
   EXIT ↑↑ , Clock 1 Width , 10, NANOSEC)

3. Clock Frequency 50 MHz.
   (PAGES , TIMING , Frequency , 50, MEGAHERTZ)

4. Clear Strobe.
   (PAGES , DATA , Edit , Clear & Set , Clear Strobe ,
   EXECUTE)

5. Strobe Breaks ON.
   (PAGES , CONTROL , Break Control , Strobe Breaks , ON)

6. Entry Mode Vertical.
   (PAGES , DATA , Edit , Entry Mode , VERTICAL ,
   EXIT ↑↑ , EXIT ↑)

7. Top Address 00000; Strobe Bit to 1.
   (Top Address , 0, ENTER NUMBER , EXIT ↑ , 1)

8. Using the Cursor softkey move cursor to address 00001 and set strobe bit high by pressing the 1 key on the data entry key pad.

9. Set strobe bits to high in following addresses as described in step 8:
   1; 2; 4; 8; 16; 32; 64; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.

10. Press **STOP** and **RUN**. The 8180A/B should be in BREAK at address 00000.

11. Press **RUN** again and the 8180A/B should break at address 00001.

12. Check that the 8180A/B breaks at addresses 2; 4; 8; 16; 32; 64; 128; 256, 512, 1024, 2048, 4096, 8192 and 0 each time after pressing **RUN** again. On the 8180A check up to 512.

6-5 Internal Clock Frequency Test

Specification

Accuracy: ±5% of programmed value.

Description

The Strobe output signal programmed as clock is used to measure the internal clock generator accuracy. Clock timing errors flagged up on the screen with Standard Set and 50 MHz programmed have no influence on the Strobe output.

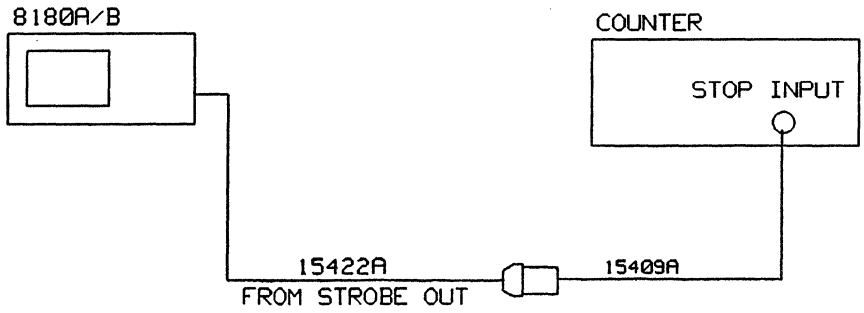


Figure 6-1. Test Setup for the Internal Clock Frequency Test

Equipment

Universal Counter	HP 5370B
Plug-on BNC Adapter	HP 15409A
Clock and Strobe Cable Set	HP 15422A

Procedure

1. Set counter as follows.
   Trig Level: +1.2V
   FUNCTION: FREQUENCY
   GATE: 0.01s
   STOP IMP: 50 Ohm
   START COM switch: SEParate

2. Program 8180A/B Standard Set
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

3. Strobe Level TTL
   (PAGES , OUTPUT , Strobe Level , TTL)

4. Strobe Output Clock; Outputs ON
   (PAGES, CONTROL , Strobe Output , CLOCK , EXIT , Output On/Off , ON)

5. Frequency 50 MHz
   (PAGES, TIMING , Frequency , 50, MEGAHERTZ)

6. Connect equipment as shown in Figure 6-1 and press **RUN**.

Internal Clock Frequency Test

7. Check 8180A/B internal clock generator at the set frequencies as detailed in Table 6-1.

Table 6-1. Internal Clock Frequency Test Values - Tested Frequencies

Set Frequency	Min. Frequency	Max. Frequency
50.00 MHz	47.50 MHz	52.50 MHz
25.00 MHz	23.75 MHz	26.25 MHz
10.00 MHz	9.50 MHz	10.50 MHz
9.99 MHz	9.49 MHz	10.49 MHz
3.00 MHz	2.85 MHz	3.15 MHz
1.00 MHz	0.95 MHz	1.05 MHz
1.05 Hz	1.00 Hz	1.10 Hz

6-6 Clock and Data Skew Test

Specification

Skew: ⩽ 1.6 ns for Clock and Data channels.

Description

A Square Wave pattern is used to test the Clock channels and all installed Data channels. The Strobe clock signal is used as a reference, the maximum deviation from positive going Strobe transition should be ⩽ ±0.8 ns. TTL levels are used for all outputs, the test is valid also for the 8181A/B NRZ Data channels.

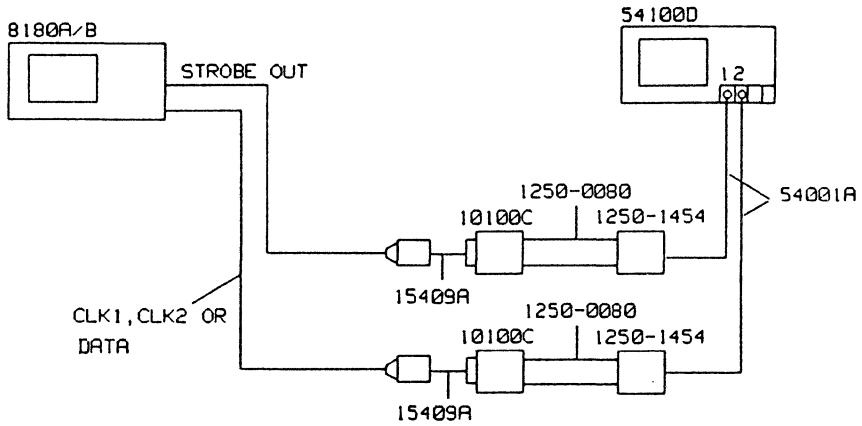


Figure 6-2. Test Setup for the Clock and Data Skew Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Scope Probe Adapter	1250-1454
BNC Adapter female/female	1250-0080
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Strobe/Clock Cable Assy	HP 15422A
Data Cable	HP 15423A

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , RCL STD SET , EXECUTE)

2. Label A TTL, Strobe TTL, Strobe to Clock.
   (PAGES , OUTPUT , Level , TTL Levels , EXECUTE ,
   EXIT 1
   Strobe Level , TTL
   PAGES , CONTROL , Strobe Output , CLOCK)

3. Clock 1 Format RZ=50%; Clock 2 Format RZ=50%; Clock 1 Delay 0 ns; Clock 2 Delay 0 ns.
   (PAGES , TIMING , Clock 1 Format , RZ=50 ,
   EXIT TIMING ,

Clock2 Format , RZ=50% , EXIT ↑↑ ,
Clock 1 Delay , 0, NANOSEC , EXIT ↑↑ ,
Clock 2 Delay , 0, NANOSEC)

4. First address 00000; Last Address 00001.
(PAGES , CONTROL , First Address , 0, ENTER NUMBER , EXIT ↑ ,
Last Address , 1, ENTER NUMBER)

5. Set Data.
(PAGES , Data [fill Data pattern at first address with 1's, and Data pattern at last address with 0's])

6. Connect the equipment as shown in Figure 6-2. Switch outputs ON and start the generator
(PAGES , OUTPUT , Outp on/off , ON)
Press **RUN**.

Cancel out interchannel delay between scope channel 1 and scope channel 2.

7. Set scope as follows:
(Autoscale > Display > Split Screen to OFF > [>Trigger >TRG Mode [to Time-Dly} > After [Neg Edge] > On [Chan 2] > Delay [40 ns] > Then > Trig On [Pos] Edge > On [Ch 1]] > Timebase > Sec/Div > 500ps > More > Wfmsave > Memory 1 to ON > Clear Memory 1 > Store to Memory 1).

8. Connect in turn all Clock and Data channels to scope input 2 and store each displayed transition to Memory 1.

9. Set Start Marker to the 50% point of the displayed strobe transition and measure with the Stop Marker the maximum ± deviation of the stored channel transitions (Delta t > T Markers to ON > Start Marker > Knob > Stop Marker > Knob)

10. The maximum deviation should be $\leqslant \pm 0.8$ ns. (B-version); $\leqslant \pm 1$ns (A-version).

6-7 Clock 1, Clock 2 Delay Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

The clock delays are referenced to the Strobe clock output signal. Delays longer than 300ns are measured with a time interval counter.

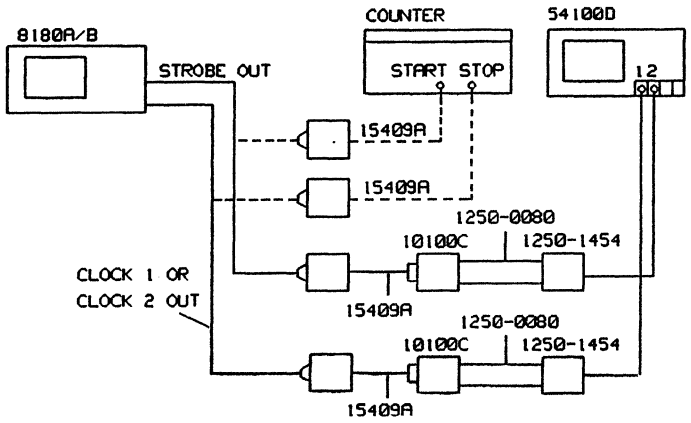


Figure 6-3. Test Setup for the Clock 1 and Clock 2 Delay Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Clock, Strobe Cable Assembly	HP 15422A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454
Counter	HP 5370B

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

2. Period 1 µs.
   (PAGES , TIMING , Period , 1, MICROSEC)

3. Label A TTL; Strobe TTL; Strobe output to Clock.
   (PAGES , OUTPUT , Level , TTL Levels , EXECUTE ,
   EXIT ,
   Strobe Level , TTL ,
   PAGES , CONTROL , Strobe Output , CLOCK)

4. Clock 1 and Clock 2 Format RZ = 50%; Clock 1 and Clock 2 Delay = 0.00 ns.
   (PAGES , TIMING , Clock 1 Timing , Clock 1 Format , RZ 50% ,
   EXIT ,
   Clock 2 Format , RZ 50% , EXIT ,
   Clock 1 Delay , 0, NANOSEC , EXIT ,
   Clock 2 Delay , 0, NANOSEC)

5. Outputs ON.
(PAGES , , ,)

6. Clock 1 (2) Delay in Softkey Area and start the generator.
(PAGES , , , y , ( ))
Connect the equipment as shown in Figure 6-3 and start the generator (press **RUN**).

   Cancel out scope trigger delay of channel 2 and interchannel delay between scope channel 1 and channel 2.

7. Connect equipment as shown in the measurement setup and set the scope as follows:
(Autoscale > Trigger > Trig Src to Chan2 > Slope to pos > Timebase > 1ns > Display > Split Screen to OFF > Delta > T Markers to ON > Start Marker to 0.00ns (50% point of the positive going transition of the Strobe clock signal))

   Note: The position of the start marker is used as reference for this test and should therefore not be moved during the measurement.

8. Set clock delay to 30 ns (30,).

9. Set the scope as follows:
(Timebase > Delay > 30ns > Delta t > Stop Marker > 30ns > Knob)

10. Position the Stop Marker at the 50% point of the displayed transition and read Delta t. Delta t must be in the following range:
    Delta t minimum = 27.5 ns
    Delta t maximum = 32.5 ns

11. Check also the clock delay for the settings detailed in Table 6-2.

Table 6-2. Clock 1, Clock 2 Delay Test Values - Clock Delay at 1 µs Period

Set Delay	Min. Delay	Max. Delay
89.9 ns	84.4 ns	95.4 ns
90.0 ns	84.5 ns	95.5 ns
300 ns	284 ns	316 ns

12. Disconnect the Strobe and Clock connections from the scope (between 15409A and 10100C) and connect Strobe cable to Start Input of the counter and the Clock 1 (2) cable to the Stop Input of the counter.

13. Set the counter as follows:

Function:	Time Interval
Sample Size:	1
Start/Stop input:	Both Channels to 1.2 V
Start/Stop slopes:	⨍
Start/Stop input impedance:	50 Ohm
AC/DC switches to:	AC
Start COM/SEP switch:	SEP

14. Change 8180A/B Clock Period to 200 ms and check delay at Clock 1 and 2 at settings given in Table 6-3:
(PAGES , TIMING , Period , 200, MILLISEC , EXIT ↑ ,
Clock Timing , Clock 1 Delay [Clock 2 Delay])

Table 6-3. Clock 1, Clock 2 Delay Test Values - Clock Delay at 200 ms Period

Set Delay	Min. Delay	Max. Delay
989 ns 100 ms	938.5 ns 95.0 ms	1039.5 ns 105.0 ms

6-8 Clock 1 , Clock 2 Width Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

The clock width is measured at 50% amplitude. Width ranges greater than 300 ns are measured with the counter.

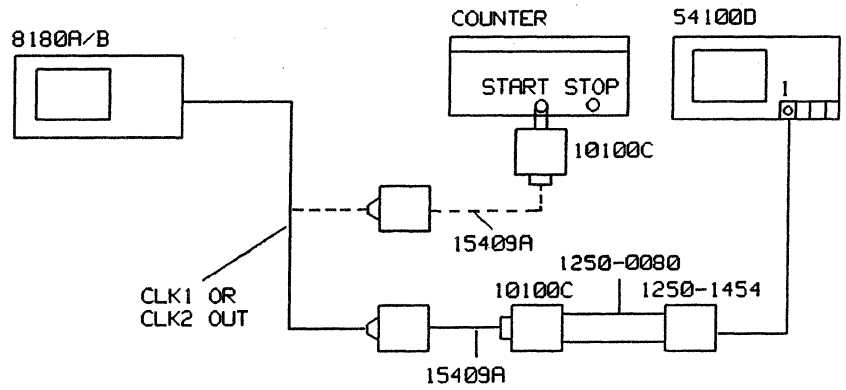


Figure 6-4. Test Setup for the Clock 1 and Clock 2 Width Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Clock, Strobe Cable Assembly	HP 15422A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Scope Probe Adapter	1250-1454
Counter	HP 5370B
BNC Adapter female/female	1250-0080

Procedure

1. Program 8180A/B Standard Set
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

2. Clock Period 1 µs
   (PAGES , TIMING , Period , 1, MICROSEC)

3. Label A TTL
   (PAGES , OUTPUT , Level , TTL Level , EXECUTE)

4. Outputs ON
   (PAGES , OUTPUT , Outp on/off , ON)

5. Connect the equipment as shown in Figure 6-4 and press **RUN**.

6. Set the scope as follows:
   (Autoscale > Timebase > Sec/DIV > 500 ps)

7. Set the Start Marker to the 50% point of the displayed positive going transition.
(Delta t > T Markers to ON > Start Marker > Knob)

8. Set Clock 1 Width to 10 ns.
(PAGES , TIMING , Clock Timing , Clock 1 Width , 10, NANOSEC EXIT TIMING)

9. Set the scope as follows:
(Timebase > Delay > 10 ns > Delta t > Stop Marker > Knob)

10. Adjust the Stop Marker to the 50% point of the negative going transition of the Clock 1 signal and read Delta t.

    Delta t minimum = 8.5 ns
    Delta t maximum = 11.5 ns

    Note: The position of the Start Marker is used as reference for the following measurements and should therefore not be moved.

11. Check step linearity when incrementing the width in 100 ps steps up to 20 ns.

12. Check clock width using the procedure described in steps 8 to 10 for the width settings given in Table 6-4.

Table 6-4. Clock 1, Clock 2 Width Test Values - Clock Width at 1 µs Period

Set Width	Min. Width	Max. Width
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns
300.0 ns	284.0 ns	316.0 ns

13. Disconnect the clock connection between the 10100C and 1250-0080 and connect the 10100C to the Start Input of the counter.

14. Set the counter as follows:

Function:	Time Interval
Sample Size:	1
Start/Stop Input Levels:	Preset
Start slope to:	ƒ
Stop slope to:	ι
Start & Stop Input Imp.:	1 MΩ
AC/DC switches to:	AC
START COM/SEP switch:	START COM
Divider:	divide by 10

15. Change 8180A/B Clock Period to 200 ms and check Clock 1 width at the settings given in Table 6-5.
(PAGES , TIMING , Period , 200, MILLISEC , EXIT TIMING , Clock Timing , Clock 1 Width)

Table 6-5. Clock 1, Clock 2 Width Test Values - Clock Width at 200 ms Period

Set Width	Min. Width	Max. Width
999 ns	948 ns	1050 ns
100 ms	95.0 ms	105 ms

16. Perform the above procedures for Clock 2.

6-9 Option 002 Timing Channel Delay Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

Data channel delays are referenced to the Strobe Clock output signal. Delays greater than 300 ns are measured with a time interval counter.

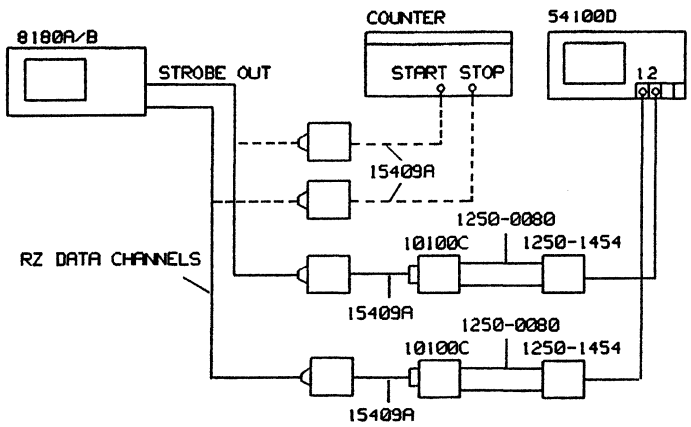


Figure 6-5. Test Setup for the Timing Channel Delay Test

Equipment

Scope	HP 54100D
Active Pads	HP 54001A
Counter	HP 5370B
Clock, Strobe Cable Assembly	HP 15422A
Data Cable set	HP 15423A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

2. Set Clock Period to 1 µs.
   (PAGES , TIMING , Period , 1, MICROSEC)

3. Label A TTL; Strobe TTL; Strobe Output to Clock.
   (PAGES , OUTPUT , Level , TTL Levels , EXECUTE ,
   EXIT ,
   Strobe Level , TTL
   PAGES , CONTROL , Strobe Output , Clock)

4. Outputs ON.
   (PAGES , OUTPUT , Outputs On/Off , ON)

5. Set Data.
(PAGES , Data , Edit , Clear & Set , Set DATA , EXECUTE)

6. Connect the equipment as shown in Figure 6-5 and press **RUN**.

NRZ Function Test

7. Check all installed RZ channels listed on the Timing Page for a static TTL high level (greater than +2V).

8. Set All Channel Format to RZ.
(PAGES , TIMING , Channel Timing , All Ch Format , RZ)

   Cancel out interchannel skew between scope channel 1 and channel 2 and the trigger delay of channel 2.

9. Set the scope as follows:
(Autoscale > Timebase > Sec/DIV > 500 ps > Trigger > Trg Src to Channel 2 > slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)

10. Position the Start Marker to the 50% point of the positive going Strobe transition (0.00 ns).

    Note: The position of the Start Marker is used as reference for this test and should therefore not be moved during the measurement.

Delay Test

11. Set All Channel Delay to 10 ns.
(PAGES , TIMING , Chnl Timing , All Ch Delay , 10, NANOSEC)

12. Set the scope as follows:
(Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Timebase > Delay > 10 ns > Delta t > Stop Marker > 10ns > Knob)

13. Place the Stop Marker at the 50% point of the displayed positive going transition and read Delta t.
Delta t minimum = 8.5 ns
Delta t maximum = 11.5 ns

14. Check in turn all RZ Data channels.

15. Repeat steps 11 to 14 for the settings given in Table 6-6.

Table 6-6. Timing Channel Delay Test Values - Clock Period at 1 µs

Set Delay	Min. Delay	Max. Delay
10.0 ns	8.5 ns	11.5 ns
30.0 ns	27.5 ns	32.5 ns
89.9 ns	84.4 ns	95.4 ns
90.0 ns	84.5 ns	95.5 ns
300 ns	284 ns	316 ns

16. Change the Clock Period to 200 ms.
(PAGES , TIMING , Period , 200, MILLISEC , EXIT , Chnl Timing , All Ch Delay)

17. Disconnect the Strobe and Data cable from the scope (between 15409A and 10100C) and connect the cables to the counter inputs as shown in the measurement setup.

18. Set the counter as follows:

Function:	Time Interval
Sample size:	1
Start/Stop levels:	Both Channels to 1.2 V
Start/Stop slope:	∫
Input impedances:	50 Ω
AC/DC switches:	AC
Start CAM/SEP switch:	SEP
Input Divider:	divide by 1

19. Check in turn all RZ Data channels for the delay settings given in Table 6-7.

Table 6-7. Timing Channel Delay Test Values - Clock Period at 200 ms

Set Delay	Min. Delay	Max. Delay
989.0 ns	938.5 ns	1039.5 ns
100.0 ms	95.0 ms	105.0 ms

6-10 Option 002 Timing Channel Width Test

Specification

Accuracy: ±5% of progammed value ±1 ns

Description

The Data channel width is measured at 50% of amplitude. Width ranges greater than 300 ns are checked with the counter.

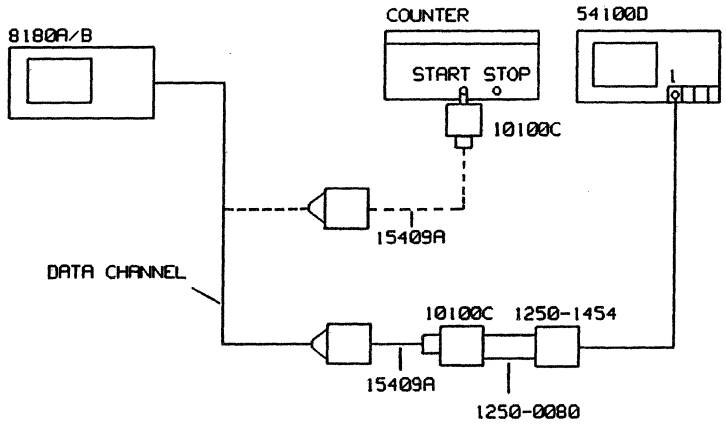


Figure 6-6. Test Setup for the Timing Channel Width Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Counter	HP 5370B
Data cable set	HP 15423A
BNC Adapter	HP 15409A
50 Ω Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , Store/Recall , Rcl Std Set , EXECUTE)

2. Period 1 µs (PAGES , Timing , Period , 1, MICROSEC)

3. Label A TTL; Outputs ON.
   (PAGES , Output , Level , TTL LEVELS , EXECUTE ,
   EXIT ↑ ,
   Outp on/off , ON)

4. Set Data.
   (PAGES , DATA ,
   Edit , Clear & Set , Set Data , EXECUTE)

5. All Channel Width 10 ns.
(PAGES , TIMING , Chnl Timing , All Ch Format , RZ , EXIT ↑ , All Ch Width , 10, NANOSEC)

6. Connect the equipment as shown in Figure 6-6 and press **RUN**.

   Cancel out the trigger delay of scope channel 1.

7. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 500 ps > Trigger > Trigger Src to Chan 1 > Slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)

8. Position the Start Marker at the 50% point of the positive going Data transition.

   Note: The position of the Start Marker is used as reference and should therefore not be moved during the measurements.

9. Set the scope as follows:
(Timebase > Delay >10 ns > Delta t > Stop Marker > 10 ns > Knob)

10. Position the Stop Maker at the 50% point of the negative going transition of the Data pulse and read Delta t.
    Delta t min. = 8.5 ns
    Delta t max. = 11.5 ns

11. Check in turn all RZ Data channels for the width settings given in Table 6-8.

Table 6-8. Timing Channel Width Test Values - Clock Period at 1 µs

Set Width	Min. Width	Max. Width
10.0 ns	8.5 ns	11.5 ns
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns
300.0 ns	284.0 ns	316.0 ns

12. Change 8180A/B clock period to 200 ms.
(PAGES , TIMING , Period , 200, MILLISEC , EXIT ↑ , Chnl Timing , All Ch Width)

13. Disconnect the Data probe from the scope (between 10100C and 1250-0080) and connect the open end of the 10100C to the counter Start input.

14. Set the counter as follows:

Function:	Time Interval
Sample size:	1
Start/Stop input levels:	Preset
Start slope:	∫
Stop slope:	⌊
Input impedances:	1 MΩ
AC/DC switches:	AC
Start COM/SEP switch:	Start COM
Input Divider:	divide by 10

15. Check in turn all RZ Data channels for the delay settings given in Table 6-9.

Table 6-9. Timing Channel Width Test Values - Clock Period at 200 ms

Set Width	Min. Width	Max. Width
999.0 ns	948.0 ns	1050.0 ns
100.0 ms	95.0 ms	105.0 ms

6-11 Data High / Low Level Accuracy Test

Specification

Level accuracy: ±0.5% of level ±60mV (add ±60mV for amplitudes smaller than 1.5V); only valid with standard cable length of 1.5m.

Description

High and low level accuracy is measured with a digital voltmeter. All data channels are set to the NRZ format. To measure the high level all data is set to high. Low level is measured with data cleared (low).

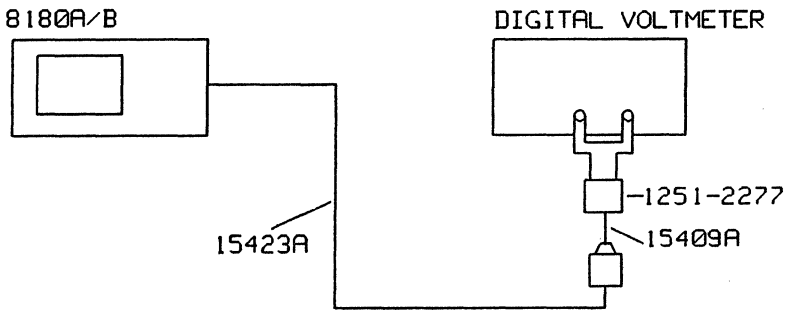


Figure 6-7. Test Setup for the Level Accuracy Test

Equipment

Digital Voltmeter	HP 3456A
BNC (f) to dual banana Plug	1251-2277
Plug-on BNC Adapter	HP 15409A
Data Cable Set	HP 15423A

High Level Accuracy Test

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALL , Rcl Std Set , EXECUTE)

2. Set Data.
   (PAGES , DATA , Edit , Clear & Set , Set Data , EXECUTE)

3. Load Impedance to Open.
   (PAGES , OUTPUT , Load Imp , Open)

4. Outputs ON.
   (PAGES , OUTPUT , Outputs on/off , ON)

5. Label A Low Level to -2V, High Level to -1V.
   (PAGES , OUTPUT , Levels , Low -> High [to low], -, 2, Volts , Low -> High [to high], -, 1, Volts)

6. Connect the equipment as shown in Figure 6-7 and press RUN.

7. Measure the output voltage at the high level settings given in Table 6-10.

Table 6-10. Data High Level Accuracy Test Values

Set Level	Min. Level	Max. Level
-1.00 V	-0.875 V	-1.125 V
0.00 V	-0.060 V	+0.060 V
+1.00 V	+0.935 V	+1.065 V
+5.00 V	+4.915 V	+5.085 V
+17.00 V	+16.860 V	+17.150 V

8. Repeat step 7 for all Data channels.

Low Level Accuracy Test

9. Clear Data.
(PAGES , DATA , Edit , Clear & Set , Clear Data , EXECUTE)

10. Set Label A High Level to +17V, Low Level to -2V.
(PAGES , OUTPUT , Level , Low <-> High [to high] , 17, Volt , Low <-> High [to low] , -, 2, Volt)

11. Measure the output voltage at the low level settings given in Table 6-11.

Table 6-11. Data Low Level Accuracy Test Values

Set Level	Min. Level	Max. Level
-2.00 V	-1.930 V	-2.070 V
-1.00 V	-0.935 V	+1.065 V
0.00 V	+0.060 V	+0.060 V
+1.00 V	+0.935 V	+1.065 V
+16.00 V	+15.800 V	+16.200 V

12. Repeat step 11 for all data channels.

6-12 20 MHz Memory Test

Description

The 8180A/B memory can be tested with a Signature Multimeter up to 20 MHz. Start/Stop conditions for the Signature Multimeter are established with a high bit in the strobe channel. A pseudo-random binary sequence which can be generated on all channels is used as the test pattern.

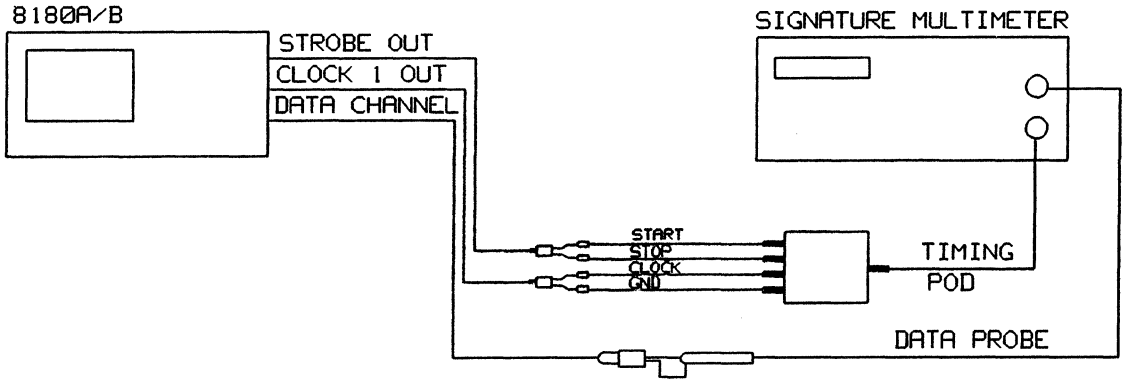


Figure 6-8. Test Setup for the 20 MHz Memory Test

Equipment

Signature Multimeter	HP 5005A
Data Cable Set	HP 15423A
Clock Strobe Cable Set	HP 15422A
Solder-in Receptacle	HP 15412A

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

2. Clock 1 Format to RZ 50%; Clock 1 Delay to 25 ns; Clock 2 Delay to 0 ns.
   (PAGES , TIMING , Clock Timing , Clock1 Format , RZ = 50 % ,
   EXIT ↑ ,
   Clock 1 Delay , 25, NANOSEC , EXIT ↑ ,
   Clock 2 Delay , 0, NANOSEC)

3. Clock Period to 50 ns.
   (PAGES , TIMING , Period , 50, NANOSEC)

4. Load Impedance Open; Label A TTL.
   (PAGES , OUTPUT , Load Imp , Open , EXIT ↑ ,
   Level , TTL Levels , EXECUTE)

5. Strobe Level TTL; Outputs ON.
   (PAGES , OUTPUT , Strobe Level , TTL , EXIT ↑ ,
   Outp on/off , ON)

6. Clear Strobe.
   (PAGES , DATA , Edit , Clear & Set , Clear Strobe ,
   EXECUTE)

7. PRBS on Channel 0-0.
   (PAGES , DATA , Edit , Channel Edit , Channel PRBS , —> ,
   [until PRBS channel 00 is displayed], EXECUTE , EXIT)

8. Copy Channel.
   Press Copy Channel and using the —> softkey in the right hand half of the display move the inverse video cursor until Copy Channel 0-0 to 0-0 is displayed.

9. Copy Channel 0-0 to all other channels.
   Press alternately (<— [on the right hand half of the display] and EXECUTE)
   until all Data channels contain the pattern in channel 0-0.

10. Set the Strobe Bit to High at address 00000.
    (PAGES , DATA , Top Address , 0, ENTER NUMBER , EXIT , 1)

11. Connect the equipment as shown in Figure 6-8 and press **RUN.**

12. Check all data channels for the following signature:
    On the 8180A - 46F9
    On the 8180B - H150

6-13 Ext. Clock; RUN; BREAK and STOP Hysteresis/Threshold Test

Specification

Threshold Accuracy: ±3% of programmed value ±50 mV

Description

A low frequency triangular wave signal is used to stimulate the 8180A/B external inputs. When the current threshold level of the 8180A/B inputs is reached, the 8180A/B starts or stops generating a signal at its Clock 1 output. Both signals, the triangular wave signal and the Clock 1 output signal are displayed on the scope. The level of the triangular wave signal where Clock 1 generation commences or stops is the actual input threshold.

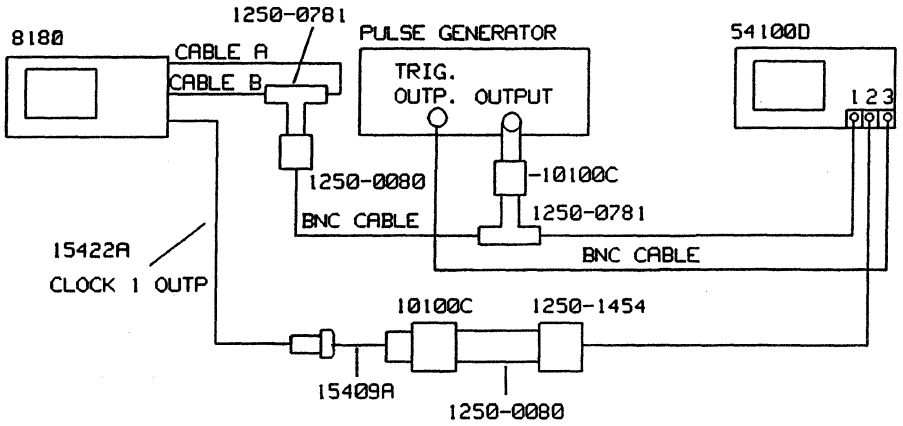


Figure 6-9. Test Setup for the External Input Test

Equipment

Pulse/Function Generator	HP 8007B/HP8116A
Scope	HP 54100D
Active Pods	HP 54001A
50 Ohm Pod	HP 54002A
50 Ohm Feedthrough	HP 10100C
BNC Tee Adapter	1250-0781
BNC female/female	1250-0080
Scope Probe Adapter	1250-1454
BNC Adapter	HP 15409A
Clock/Strobe cable set	HP 15422A
BNC Cable	

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , RCL Std Set , EXECUTE)

2. Clock 1 Width 20 ns; Clock 2 Delay 0 ns.
   (PAGES , CLOCK 1 , CLK 1 WIDTH , CLOCK 2 DELAY , 20, ns/s , EXIT , CLOCK 2 DELAY , 0, ns/s)

3. Label A TTL; Outputs ON.
(PAGES , OUTPUT , Levels , TTL Levels , EXECUTE ,
EXIT ↑↑ ,
Outp on/off , ON)

4. Input Impedance 100 KΩ
(PAGES , CONTROL , Inputs , Impedance , 100 kΩ)

5. Clock Source External Positive Edge
(PAGES , CONTROL , Clock Source , EXTERNAL ⌋)

6. Set the Pulse Generator as follows:

Period approx.	1 ms
Width	0.5 ms
Transition	5 µs to 250 µs
Amplitude	250 mVpp (into open)
Offset	ON

7. Adjust leading edge and trailing edge for a triangle waveform on the scope.

External Clock Test

8. Connect the equipment as shown in Figure 6-9 and press **RUN**. (BNC Cable A connected to External Clock Input.)

9. Adjust the triangular waveform such that it is symmetrical about 0V using the pulse generator's offset vernier.

10. Set the scope as follows:

(Autoscale > Chan 2 > Volts/Div > 1 Volt > Trigger > Trig Src to Chan 2 >Trigger Level > 1 Volt > Chan 1 > Chan 1 Mode to Magnify > Magnify to ON > Volts/Div > 20mV/Div > Offset > 0V > Timebase > Sec/Div > 50 µs)

11. The displayed transition should cross the vertical graticule line between ± 50 mV.

12. Change External Clock Slope (active edge) to negative. (EXTERNAL ⌊)

13. The displayed transition should cross the vertical graticule line between ± 50 mV.

External RUN and BREAK Test

14. Connect cable A to the Break Input (cable B to the Run Input).

15. Set the 8180A/B to Clock Source INTERNAL; RUN Input to ON, active edge positive; BREAK Input to ON, active edge negative.
(PAGES , CONTROL , Inputs , Clock Source , INTERNAL ,
EXIT ↑↑ ,
Run Input , ON ⌋ , EXIT ↑↑ ,
Break Input ON ⌊)

16. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 200 microsec/Div > Trigger > Trigger Source to Channel 3 > Trigger Level > 1 Volt > Delta t > T Markers to ON > Start Marker > Knob > Stop Marker > Knob)
Set the Start Marker to the positive going edge of displayed pulse on channel 2. Set the Stop Marker to the negative going edge of displayed pulse on channel 2.

17. Set the scope as follows:
(Timebase > Delay > Knob)
Adjust Start Marker to the vertical center graticule line.

18. Set the scope as follows:
Timebase to 50 µs; Chan 2 to OFF; Split Screen to OFF
(Sec/Div > 50 µs > Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Channel 1 > Channel 1 Mode to Magnify > Magnify ON > Volts/Div > 20 mV/Div.

19. The displayed transition should cross the vertical graticule line within the limits of ±50mV.

20. Repeat the measurement at the position where the Stop Marker is located. The displayed transition should cross the vertical graticule line within the limits of ±50mV.

21. Set the Run Input to ON, active edge negative; Break Input to ON, active edge positive.
(, , , ,
,)

22. Repeat step 15 through 20 with reversed slopes for Run and Break Inputs. Threshold Limit is ±50mV.

External STOP Test

23. Connect cable A to the Stop Input (cable B to the Run Input).

24. Check threshold levels of the Stop Input for both slopes as described above for the Break Input.

25. Check Clock, Run, Break and Stop inputs at +2 Volt and -2 Volt threshold settings.
(PAGES , , , , 2 [-2],).

    For this test set the pulse generator to triangular waveform with an amplitude of 8V pp symmetrical about 0V.

    Limits: Voltage Threshold minimum = 1.85 V
    Voltage Threshold maximum = 2.15 V

    Check inputs only at one slope setting.

6-14 Transition Time / Overshoot Test

Specification

Transition Time: less than 3.0 ns + |amplitude| x 0.2 ns.
Preshoot, Overshoot, Ringing: less than ± 10% of amplitude.
Specifications are valid for a cable length of 1.5 m.

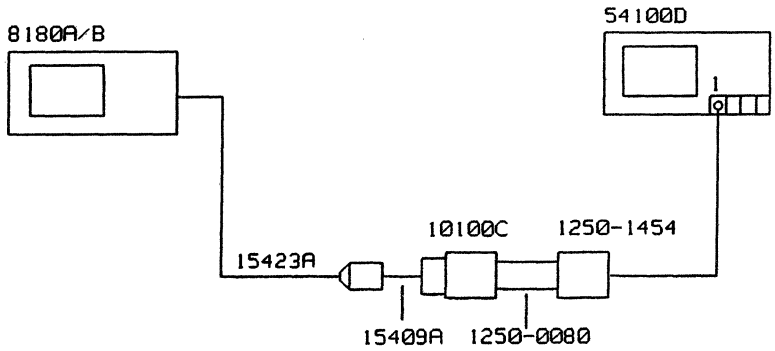


Figure 6-10. Test Setup for the Transition Time / Overshoot Test

Equipment

Scope	HP 54100D
Active Pod	HP 54001A
Data Cable	HP 15423A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC female/female	1250-0080
BNC scope probe adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , STORE/RECALL , Rcl Std Set , EXECUTE)

2. Set all bits at address 00000 High; Set all bits at address 00001 Low.
   (PAGES , DATA , Top Address , 0 , ENTER NUMBER , EXIT , 1)
   Press 1 until the strobe channel and all data channels at address 00000 are set to high.
   Press 0 until the strobe channel and all data channels at address 00001 are set to low.

3. Last Address 00001.
   (PAGES , CONTROL , Last Address , 1, ENTER NUMBER)

4. Outputs ON.
   (PAGES , OUTPUT , Outp on/off , ON)

5. Set Label A High Level to -1 V; Low Level -2 V.
   (PAGES , OUTPUT , Level , Low <-> High [to High], -1, Volt ,
   Low <-> High [to Low], -, 2, Volt)

6. Connect the equipment as shown in Figure 6-10 and press **RUN**.

7. Set the scope as follows:
   (Autoscale > Delta V > Vmarkers to ON > Marker 1 Position > Knob [set Marker 1 to 0% of pulse]

> Marker 2 Position > Knob [set Marker 2 to 100% of pulse] > 10-90% > Timebase > Sec/Div > 500 ps > Delta t > T Markers to ON > Start Marker > Knob [set the Start Marker to the crossing point at the 10% Level and displayed transition] > Stop Marker > Knob [Set the Stop Marker to the crossing point at the 90% Level and displayed transition]).

8. Measure the transition time (Delta t) from 10 % to 90 % of amplitude for all data channels.
   Specification: Transition Time = less than 3 ns.

9. Change Label A High Level to + 2 V; Low Level to 0 V.
   (PAGES , OUTPUT , Level , Low <-> High [to High], 2, VOLT , Low <-> High [to Low], 0, VOLT)

10. Measure preshoot, overshoot and ringing at all data channels.

    Specification: less than ±10% of amplitude.

Chapter 7
HP 8182A/B Performance Verification

7-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications of the HP 8182A/B Data Analyzer given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

7-2 Trigger Word and Operating Modes Tests

Description

The Data Generator HP-Model 8018A is used to generate the Trigger Word (bit) for two 8182A/B data channels. The error display indicates the Trigger Word position. Because of the cleared memory, the Trigger Word appears as an error. When selecting Trigger Event Start Compare Mode, the Trigger Delay is set to 00001. This causes the Trigger Word to be displayed in address 1023/16383.

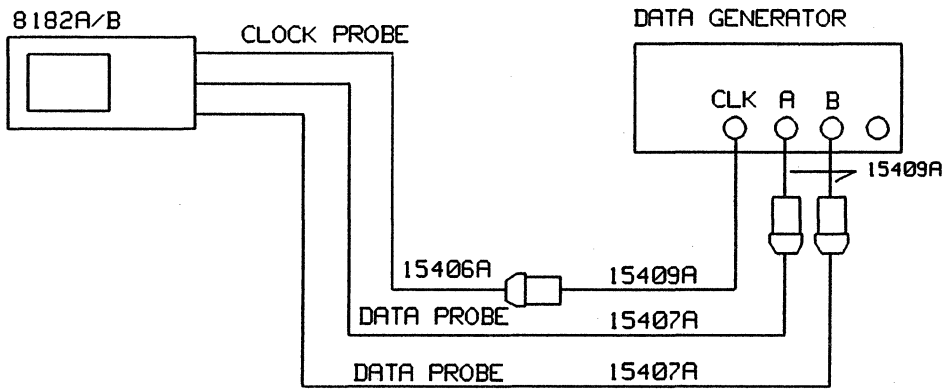


Figure 7-1. Test Setup for the Trigger Word and Operating Mode Test

Equipment Required

Data generator	HP 8018A
Plug-on BNC Adapter (3 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A

Procedure

Set the 8018A as follows:

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int.Clock	Amplitude	2.5V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm

1. Clear both 8018A Data Channels by selecting the channel and pressing the toggle switch to Channel Clear.

2. Select Word Address 01 and load bit 1 to high in channel A and channel B.

3. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Rcl Std Set , EXECUTE)

4. Clear Word Mask; Clear Data.
   (PAGES, EXPECTED DATA , Edit , Clear & Set , Clr Word Mask , EXECUTE , Clr Data , EXECUTE)

5. Clock Delay 5 ns.
   (PAGES, CONTROL , Clock , Clock Delay , 5, NANOSEC)

6. Autoarming Delay 1s.
   (PAGES, CONTROL , Autoarming , DELAY 1s)
   Set Stop Delay to 1023.
   (PAGES, CONTROL , Stop , Stop Delay , 1023, ENTER)

7. Error Map; Trigger Word in Softkey Area.
   (PAGES, Error Map , SOFTKEYS, CONTROL , Trigger , Trigger Word)

8. Connect the equipment as shown in Figure 7-1 and press **RUN**.

Trigger Start Analysis Test

With Trigger Word set to X (don't care) a single sporadic error should be displayed on the Error Map.

9. Set the Trigger Word for both connected data channels to 1.
   The Error Map should display only the Trigger Word in address 00000 as an error.

10. Set Trigger Word for one data channel to 0.
    The 8182A/B should switch to **ARMED** (no trigger recognition).

11. Set the Trigger Word back to 1 and the 8182A/B should trigger again.

12. Set the Trigger Word for the second channel to 0 and 1 and check Trigger Word recognition as described in steps 8 to 10.

Trigger Stop Analysis Test

13. Program 8182A/B to Trigger Stop Analysis.
(PAGES, CONTROL , Operatg Mode , Trg Stop Anal)

14. Error Map; Trigger Word in the Softkey Area.
(PAGES, Error Map , SOFTKEYS, CONTROL , Trigger , Trigger Word)

    With Trigger Word 1 for both connected data channels, the error display should stop always at address -00000 (the Trigger Word at address -00000 is indicated as error).

15. Set the Trigger Word for one connected channel to 0.
The 8182A/B should stay in ACTIVE (no trigger).

16. Set the Trigger Word back to 1.
The 8182A/B should trigger again.

17. Set the Trigger Word for the second connected data channel to 0 and 1 and check Trigger Word recognition as described in steps 14 to 16.

Trigger Event Start Compare Test

18. Program 8182A/B to Trigger Event Start Compare.
(PAGES, CONTROL , Operatg Mode , Trg Strt Comp , EXECUTE)

19. Select Error Map.
(PAGES, Error Map)

    The error display should show the Trigger Word indicated as error at address 1023 (caused by Trigger Delay 00001) and errors in the channel marking display for both connected data channels.

20. Program Trigger Start Analysis and Trigger Delay 0.
(PAGES, CONTROL , Operatg Mode , Trg Strt Anal , EXIT ↑ ,
Trigger , Trg Delay , 0, ENTER NUMBER)

21. Repeat the procedure starting with step 5 for the remaining data channel pairs.

7-3 Trigger Delay and Stop Delay Tests

Description

This test is to be performed with any one of the available channels to check the Trigger Delay and Stop Delay Functions. A data generator is used to generate the Trigger Word. The Trigger Word for unused data channels must be set to don't care (X).

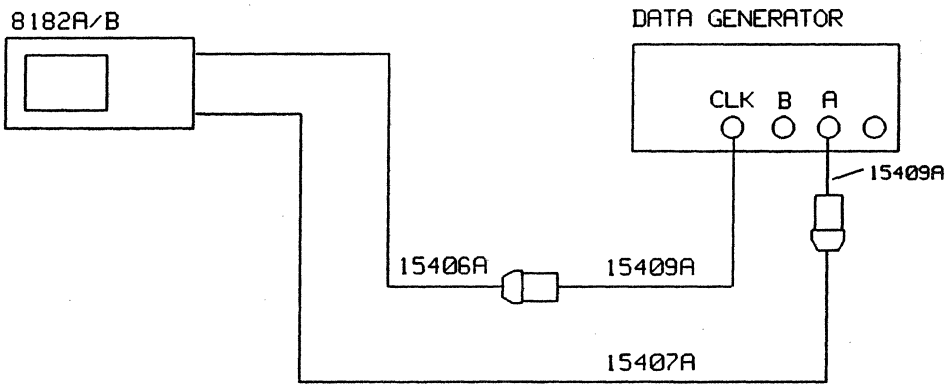


Figure 7-2. Test Setup for the Trigger Delay and Stop Delay Test

Equipment

Data Generator	HP 8018A
Plug-on BNC Adapter (2 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A

Procedure

Set the 8018A as follows:

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int. Clock	Amplitude (A)	2.5 V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm

1. Clear 8018A channel A data by selecting channel A and pressing the toggle switch to Channel Clear position.

2. Select Word Address 01 and load bit 1 to high.

3. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

4. Clear Word Mask; Clear Data.
   (PAGES, EXPECTED DATA , Edit , Clear & Set , Clr Word Mask , EXECUTE , Clr Data , EXECUTE)

5. Set Clock Delay to 5ns.
   (PAGES, CONTROL , Clock , Clock Delay , 5, NANOSEC)

6. Set Autoarming Delay to 1s; Set Stop Delay to 1023
   (PAGES, [CONTROL], [Autoarming], [Delay 1 s])
   (PAGES, [CONTROL], [Stop], [Stop Delay], 1023, [ENTER])

7. Connect the equipment as shown in Figure 7-2 and press **RUN**.

8. Set the Trigger Word to 1 for the connected data probe (all other channels to X, don't care)
   (PAGES, [CONTROL], [Trigger], [Trigger Word], 1)

9. Error Map; Trigger Delay in Softkey Area.
   (PAGES, [Error Map], SOFTKEYS, [CONTROL], [Trigger], [Trig Delay])

Trigger Delay Test

10. Increase Trigger Delay by pressing [INCREMENT], and check that the displayed error moves backwards from address 1023 (for Trg Delay 1) with increasing delay setting.

11. Set Trigger Delay back to 00000.

Stop Delay Test

12. Select Stop Delay in the Softkey Area and set Stop Delay to 1023/16383.
    (SOFTKEYS, [CONTROL], [Stop], [Stop Delay], 16383, [ENTER NUMBER])

13. Check that the Stored Words displayed in the upper right hand corner of the 8182A/B display indicates 1024/16384. Vary the Stop Delay and check that the Stop Delay setting + 1 is displayed as Stored Words in the upper right hand corner of the 8182A/B display.

7-4 Sampling Point Accuracy and Skew Tests

Specification

Sampling point accuracy: ± 5% of set Clock Delay ± 1 ns.
Channel skew: ⩽ 2 ns.

Description

The test setup uses a pulse generator as clock and data source for the 8182A/B Data Analyzer. The data is delayed by a fixed 3 ns delay line. Setting the 8182A/B Clock Delay to 3 ns then corresponds to zero delay between clock and data. The clock can now be advanced by 3 ns and delayed with respect to the data to check when the incoming data signal is recognized as a high or a low level.

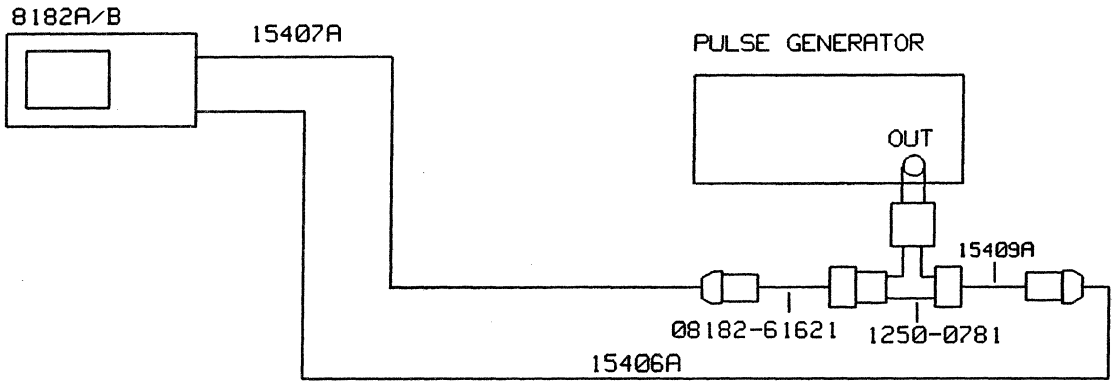


Figure 7-3. Test Setup for the Sampling Point Accuracy and Skew Test

Equipment

Pulse Generator	HP 8007B
BNC Tee	1250-0781
Plug-on BNC Adapter (2 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A
Delay Line (including 50 Ω) 3 ns	08182-61621

Procedure

1. Set Pulse Generator as follows:

Period:	1 µs
Pulse Width:	0.5 µs
Leading Edge:	< 3 ns
Trailing Edge:	< 3 ns
Amplitude High Level:	+2V into 50 Ω
Low Level:	0V

2. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS , Recall , Standard set , EXECUTE)

3. Set Clock Threshold to +1V.
(PAGES, CONTROL , Clock , Clock Thres , 1, VOLT)

4. Set Threshold Label A to +1 V.
(PAGES, Input , Threshold , 1, , VOLT)

5. Set Stop Delay to 40.
(PAGES, CONTROL , Stop , Stop Delay , 40, ENTER NUMBER)

6. Set Autoarming Delay to 0 s.
(PAGES, CONTROL , Autoarming , 0 s)

7. Select the Timing Diagrams Page.
(PAGES, TIMING DIAGR)

8. Press SOFTKEYS, CONTROL , Clock , Clock Delay , 3, NANOSEC)

9. Connect the equipment as shown in Figure 7-3 and press **RUN**. (Start with Connector 0 Channel 0.)

10. Using INCREMENT , check that the displayed timing signal switches from low to high within 2 to 4 ns of the Clock Delay setting.

11. Set the Clock Slope to Negative.
(PAGES, CONTROL , Clock , Clock Slope , NEG SLOPE ,
EXIT ↑↑ , Clock Delay)

12. Increment the Clock Delay starting from 2 ns and check that the timing signal switches from high to low within 2 to 4 ns of the Clock Delay setting.

13. Repeat the Skew Test for Positive Clock Slope and Negative Clock Slope for the remaining channels as described in steps 10 to 12.

    When checking skew from connector 3 channel 0 upwards, move the vertical display window.
    (PAGES, TIMING DIAGR , Select Displ , Vertical Window , ← [until the required channels are displayed])

7-5 Clock Delay Test

Specification

±5% of set Clock Delay ±1ns.

Description

The test setup uses a pulse generator as an external clock source. The Clock Delay is measured at the 8182A/B clock output referenced to 0.00ns programmed Clock Delay.

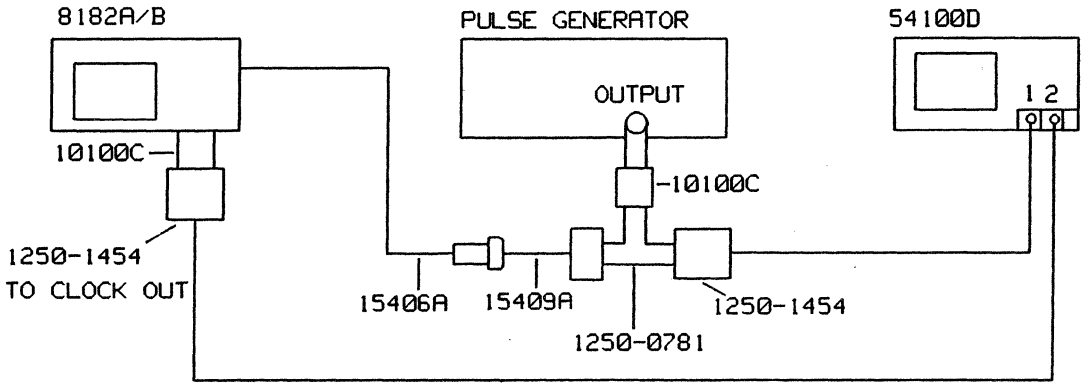


Figure 7-4. Test Setup for the Clock Delay Test

Equipment

Pulse Generator	HP 8007B
Scope	HP 54100D
Active scope Pods	HP 54001A
BNC Tee Adapter	1250-0781
50 Ohm Feedthrough	HP 10100C
BNC scope Probe Adapter	1250-1454
BNC Adapter	HP 15409A
Clock Probe	HP 15406A

Procedure

1. Cancel out channel to channel skew and the Trigger Delay of channel 2.
   Set the Pulse Generator as follows:

Period:	110 µs
Pulse Width:	1,5 µs
Transition Time:	2 ns
Amplitude LOL:	0 V
(into 50 Ohm) HIL:	2.5 V
Offset:	OFF

2. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

3. Set Clock Threshold to +1.2V; Set Clock Delay to 0.00ns.
   (PAGES, CONTROL , Clock , Clock Thres , 1.2, VOLT , EXIT , Clock Delay , 0, NANOSEC)

4. Connect the equipment as shown in Figure 7-4.

5. Set the scope as follows:
(Autoscale > Trigger > Trigger Src to Chan 1 > Chan 1 > Chan 1 Display to OFF > Display > Split Screen to OFF)

6. Center the 50% point of the positive going transition of the displayed clock pulse on the center graticule.
(Timebase > Sec/Div > 1ns > Delay > Knob)

7. Set the Start Marker to the 50% point of the displayed transition.
(Delta > Tmarkers to ON > Start Marker > Knob)

8. Using INCREMENT , step through the delay range of 0.00ns to 10.00 ns in 100 ps steps and check the accuracy.

   The position of the Start Marker is the reference for the following measurements and must therefore not be moved.

9. Program 8182A/B Clock Delay as listed in Table 7-1 and check that accuracy is in the range ±5% ±1 ns.

   Example: Zero delay between scope input Channel 1 and Channel 2 = 38 ns
   Programmed Clock Delay = 21.9 ns

   Set scope Timebase delay to 60 ns and position the Stop Marker to the 50% point of the displayed transition. Perform a delta t reading; the reading should be in the following range:
   Delta t min = 19.8 ns
   Delta t max = 24.0 ns

Table 7-1. Clock Delay Test Values

Set Delay	Delta t min.	Delta t max.
21.9 ns	19.8 ns	24.0 ns
22.0 ns	19.9 ns	24.1 ns
70.0 ns	65.5 ns	74.5 ns
117.0 ns	110.2 ns	123.9 ns
118.0 ns	111.1 ns	124.9 ns
500.0 ns	474.0 ns	526.0 ns
1.01 us	0.96 us	1.06 us
1.02 us	0.97 us	1.07 us
5.00 us	4.75 us	5.25 us
9.99 us	9.49 us	10.49 us
10.0 us	9.50 us	10.5 us
50.0 us	47.5 us	52.5 us
99.9 us	94.9 us	104.9 us

7-6 Compare Window Width Test

Specification

Compare window width accuracy ±5% of set value ±1ns.

Description

The test setup uses a pulse generator as an external clock source. Analyzer Clock Delay is measured at the 8182A/B Clock Output referenced to 0.00 ns programmed Clock Delay. Ranges up to 10 ns are measured with an oscilloscope. A time interval counter is used for higher ranges. A time offset is programmed on the counter in order to compensate for internal and cable delays, instead of adding these delays manually.

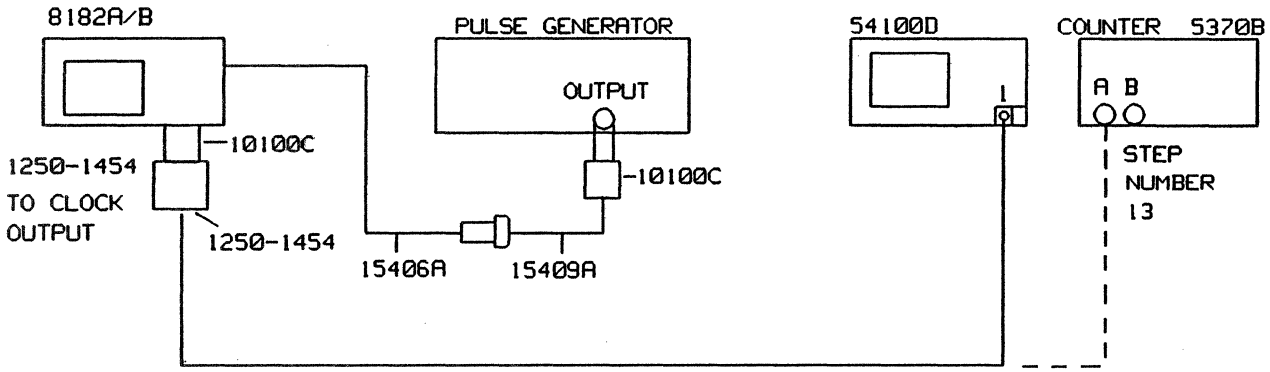


Figure 7-5. Test Setup for the Compare Window Width Test

Equipment

Scope	HP 54100D
Active scope Pods	HP 54001A
Pulse Generator	HP 8007B
Counter	HP 5370B
Clock Probe Assy	HP 15406A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Scope Probe Adapter	1250-1454

Procedure

Before performing this measurement cancel out the Trigger Delay of scope channel 1.

1. Set the Pulse Generator as follows:

Period:	1 µs
Pulse Width:	0.5 µs
Transition Time:	2 ns
HIL:	2.5 V
LOL:	0.0V

2. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

3. Select Trigger Event Start Compare.
(PAGES, CONTROL , Operatg Mode , Trg Strt Comp , EXECUTE)

4. Set the Clock Width to 10ns.
(PAGES, CONTROL , Clock , Clock Width , 10, NANOSEC)

5. Connect the equipment as shown in Figure 7-5.

6. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 500ps > Trigger > Trigger Src to Chan 1 > slope to pos)

7. Adjust the 50% point of the positive going transition to lie on the center horizontal graticule line.
(Chan 1 > Offset > Knob)

8. Move the Start Marker to the 50% point of the displayed transition.
(Delta t > Tmarkers to ON > Start Marker > Knob

   Note: The Start Marker is the reference for the following measurements and must therefore not be moved.

9. Set the scope timebase delay to 10ns.
(Timebase > Delay > 10ns)

10. Set the Stop Marker to the 50% point of the negative going transition and read delta t (Delta t > Stop Marker > Knob)

    Delta t must be in the following range:
    Delta t min: 8.5 ns
    Delta t max: 11.5 ns

11. Check linearity by incrementing the clock width in 100 ps steps up to 20 ns.

12. Check the Clock Width at the settings given in Table 7-2.

Table 7-2. Clock Width Test Values - Clock Period at 1 µs

Set Width	Min. Width	Max. Width
29.9 ns	27.4 ns	32.4 ns
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns

13. Connect 8182A/B Clock Output to counter channel A instead of scope.

    Counter settings:
    Function: Time Interval
    Sample Size: 1
    Start/Stop slopes: $\overline{b}/\overline{n}$
    Start/Stop inp. imp: 50Ω
    AC/DC switch to: AC
    Start COM/SEP switch: COM

    Change pulse generator period to 120 ms and repeat step 12 using the values in Table 7-3.

Table 7-3. Clock Width Test Values - Clock Period at 120 ms

Set Width	Min. Width	Max. Width
300.0 ns	284.0 ns	316.0 ns
999.0 ns	948.0 ns	1050.0 ns
100.0 ms	95.0 ms	105.0 ms

7-7 Clock Threshold and Hysteresis Tests

Specification

Threshold accuracy: ±2% of set value ±10mV.
Hysteresis: < ±50mV.

Description

The pulse generator is adjusted to generate a triangular waveform with a period of 1 ms. This signal is fed into the CLOCK input of the 8182A/B. When the 8182A/B clock threshold is reached the 8182A/B generates a clock pulse, which is available at its Clock Output. This clock pulse triggers a trace on the oscilloscope. The vertical offset from zero volts corresponds exactly to the level where the 8182A/B recognises a clock signal.

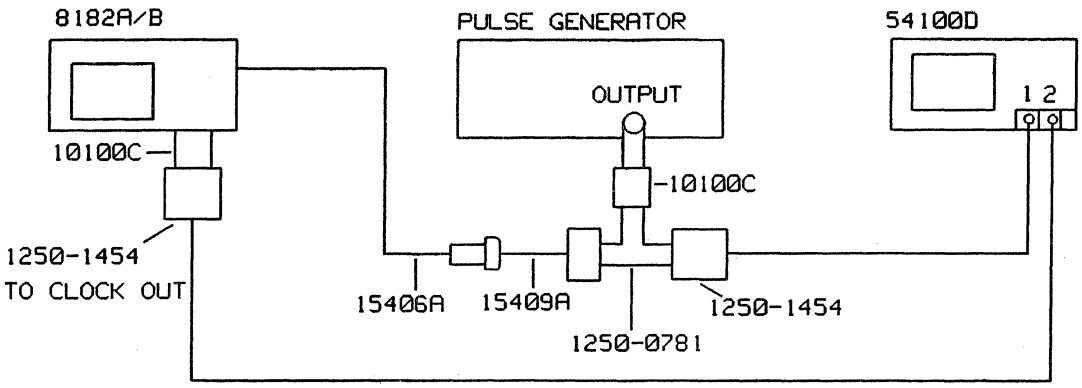


Figure 7-6. Test Setup for the Clock Threshold Hysteresis Test

Equipment

Scope	HP 54100D
Active scope Pods	HP 54001A
Pulse Generator	HP 8007B
BNC Tee Adapter	1250-0781
Scope Probe Adapter	1250-1454
50 Ohm Feedthrough	HP 10100C
Clock Probe	HP 15406A
BNC Adapter	HP 15409A

Procedure

1. Set the pulse generator as follows:

Period:	1 ms
Width:	0.5 ms
Transition Time:	5µs to 250 µs
Amplitude:	4V pp into 50Ω
Offset:	ON

2. Adjust the leading and trailing edges for a triangle waveform on the scope.

3. Using the pulse generator offset vernier, set the waveform symmetrical to 0V graticule line.

Hysteresis Test

4. Program 8182A/B to Standard Set.
(PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

5. Clock Slope Positive; Threshold 0.00V.
(PAGES, CONTROL , Clock , Clock Slope , POS SLOPE , EXIT ↑↑ , Clk Threshold , 0, VOLT)

6. Connect the equipment as shown in Figure 7-6.

7. Set the scope as follows:
(Autoscale > Trigger> Trig Src to Chan 2 > Display > Split Screen to OFF > Chan 2 > Chan 2 Display to OFF > Timebase > Sec/Div > 500ns > Chan 1 > Volts/DIV > 100mV > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV > Delta V > V Markers to ON > Marker 1 Position > Knob)

8. Position the Marker to the point where the transition crosses the vertical graticule line and read V(1).
V(1) ⩽ +50mV.

9. Change to negative Clock Slope.
(EXIT ↑↑ , Clock Slope , NEG SLOPE)
Move V Marker 1 to the crossing point and read V(1)
V(1) ⩽ -50mV

Threshold Test

10. Set the threshold to -1.4V.
(EXIT ↑↑ , Clock Thres , 1.4, VOLT)

11. Set the scope as follows.
(Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > -1.2 V > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV/DIV > Offset > -1.400V > Delta V > V markers to ON > Marker 1 Position > Knob)

12. Move Marker 1 to the crossing point where the displayed transition meets the vertical graticule line and read V(1)
V(1) min: -1.49 V
V(1) max: -1.31 V

13. Set Clock Slope to positive; Set Clock Threshold to +1.4V.
(EXIT ↑↑ , Clock Slope , POS SLOPE , EXIT ↑↑ , Clock Thres , 1.4, VOLT)

14. Set the scope as follows:
(Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > 1.200 V > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV > Offset > 1.400V)

15. Move V Marker 1 to the point where the transition crosses the vertical graticule line
(Delta V > Vmarker to ON > Marker 1 Position > Knob)

16. Read V(1). V(1) must be in the range of:
V(1) min: 1.31V
V(1) max: 1.49V

7-8 Data Threshold Level Accuracy and Linearity Tests

Specification

Single threshold accuracy:	±2% of set value ±10 mV.
Level detection accuracy 50 ms after input signal transition:	actual threshold = ±15 mV.

Description

This test is used to measure the high and low level detection voltage to determine the actual threshold voltage. The check-sequence is selected to ensure that all data lines used for level programming are working properly. To get a better resolution when adjusting the power supply, two 20 dB attenuators are used to reduce the output voltage. 20 W attenuators are recommended to avoid damage to the rest of the equipment. The capacitor across the DVM input suppresses spikes generated by the DVM.

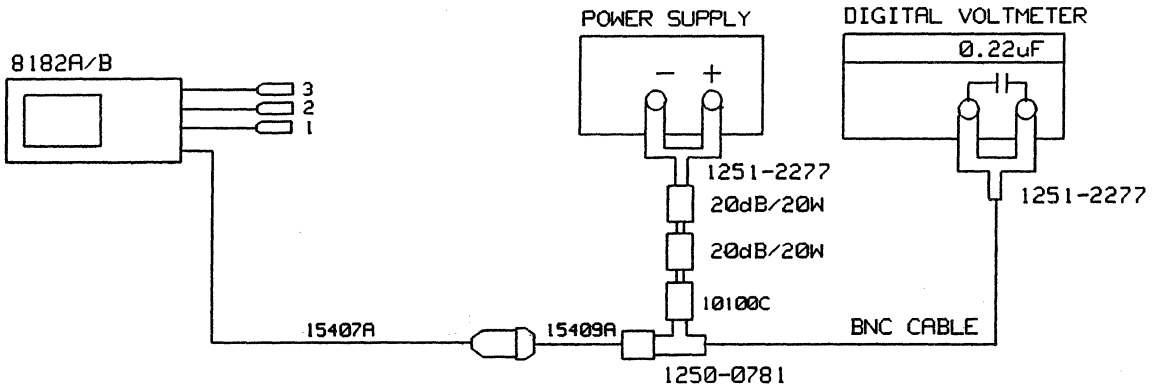


Figure 7-7. Test Setup for the Data Threshold Level Accuracy and Linearity Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
Plug-on BNC Adapter	HP 15409A
Data Probe Assy.	HP 15407A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
50 Ohm Feedthrough	HP 10100C
Capacitor	0.22 uF
2 x Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
Cable Assembly BNC to BNC	HP 11170C

Procedure

1. Program 8182A/B Standard Set.
   (PAGES, DISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Clock Source Internal.
   (PAGES, CONTROL , Clock , Clock Source , INTERNAL)

3. Select Autoarming Delay of 0s.
   (PAGES, CONTROL , AUTOARMING , DELAY 0s)

4. Set Stop Delay to 40.
(PAGES, CONTROL , Stop , Stop Delay , 40, ENTER NUMBER)

5. Set Channel Configuration to Connector 0 Channel 0.
(PAGES, Input , Chnl Config , DELETE CHNL [until only connector 0 channel 0 is displayed])

6. Select Timing Diagrams; Select Single Threshold Label A in the Softkey Area.
(PAGES, TIMING DIAGR , SOFTKEYS, Input , Threshold , [Next Label if necessary])

7. Set Single Threshold of Label A to +0.01 V.
(.01, VOLTS)

CAUTION

Set power supply voltage to minimum. Do not overload attenuators.

8. Connect the equipment as shown in Figure 7-7 and press **RUN**.

9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).

10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).
Level Detection Accuracy (Va - Vb) must be better than 30 mV.
Actual Threshold (Va + Vb)/2 must be within ±2% of the set value ±10 mV.

Example: Programmed Threshold = +0.01 V
High Level Voltage (measured in step 9) = +0.012 V
Low Level Voltage (measured in step 10) = +0.009 V
Level detection accuracy =(0.012 V - 0.009 V) = 0.003 V
Limit = <0.03 V
Single threshold accuracy = (0.012V + 0.009 V)/2 = 0.011 V
Limit = 0.00 V to 0.02 V

13. Program the thresholds given in Tables 7-5, 7-6 and 7-7, and check for specifications as described in step 10.

Table 7-5. Threshold Level Accuracy and Linearity Test - All Attenuators in Place

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy Min.	Actual	Max.
0.01 V	V	V	V	0.000V	.....	0.020V
0.02 V	V	V	V	0.010V	.....	0.030V
0.04 V	V	V	V	0.020V	.....	0.050V
0.08 V	V	V	V	0.068V	.....	0.092V
0.16 V	V	V	V	0.147V	.....	0.173V

Table 7-6. Threshold Level Accuracy and Linearity Test - One 20 dB Attenuator Removed

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy Min.	Actual	Max.
0.32 V	V	V	V	0.304V	.....	0.336V
0.64 V	V	V	V	0.617V	.....	0.663V
1.28 V	V	V	V	1.244V	.....	1.316V
2.56 V	V	V	V	2.499V	.....	2.621V

Table 7-7. Threshold Level Accuracy and Linearity Test - Both Attenuators and 50 Ω Feedthrough Removed

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy Min.	Actual	Max.
5.12 V	V	V	V	5.008V	.....	5.232V

7-9 Data Offset and Gain Tests

Specification

Single threshold accuracy:	±/2% of set value ±10 mV.
Level detection accuracy 50 ms after input signal transition:	actual threshold = ±15 mV.

Description

To determine the actual threshold and to check the threshold accuracy, the hysteresis between high and low level detection voltages must be measured first. The actual threshold is midway between high and low level detection voltages. This value must be within the specifications for single threshold.

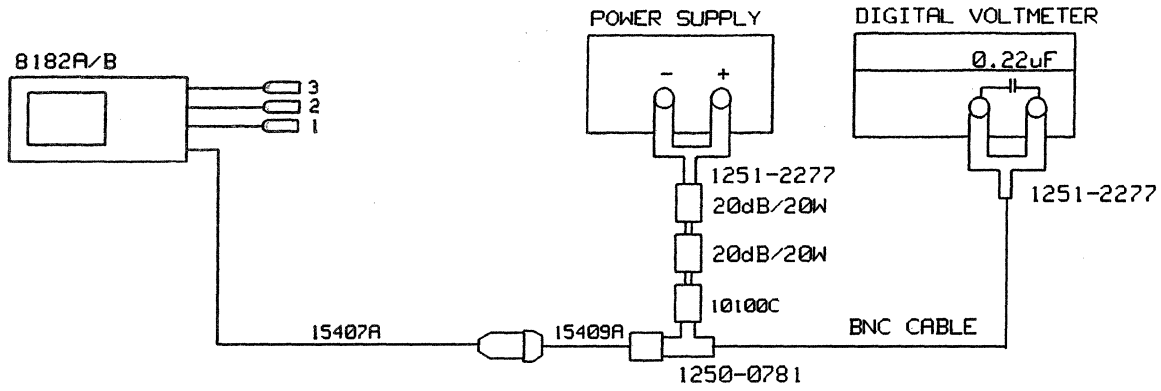


Figure 7-8. Test Setup for the Data Offset and Gain Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
Plug-on BNC Adapter	HP 15409A
Data Probe Assy.	HP 15407A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
50 Ohm Feedthrough	HP 10100C
Capacitor	0.22 uF
2 x Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
Cable Assembly BNC to BNC	HP 11170C

Positive Offset Test

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Set Clock Source to Internal.
   (PAGES, CONTROL , Clock , Clock Source , INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, CONTROL , Autoarming , DELAY 0s)

4. Set Stop Delay to 40.
   (PAGES, CONTROL , Stop , Stop Delay , 40, ENTER NUMBER)

5. Set Channel Configuration to Connector 0 Channel 0.
(PAGES, Input , Chnl Config , DELETE CHNL [until only connector 0 channel 0 is displayed])

CAUTION

Set power supply voltage to minimum. Do not overload attenuators.

6. Set Single Threshold Label A to +0.05 V.
(PAGES, Input , Threshold , Next Label [if necessary] .05, VOLT)

7. Select Timing Diagrams Report; Channel Configuration in Softkey Area.
(PAGES, TIMING DIAGR , SOFTKEYS, Input , Chnl Config)

8. Connect the equipment as shown in Figure 7-8 and press **RUN**.

9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).

10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).

Level Detection Accuracy (Va - Vb) must be less than 30 mV.
Actual Threshold (Va + Vb)/2 must be within ±2% of set value ±10mV.

Example: Programmed Threshold = 0.05 V
High Level Voltage (measured in step 9) = 0.056 V
Low Level Voltage (measured in step 10) = 0.043 V
Level detection accuracy = 0.056 V - 0.043 V = 0.013 V
Limit: < 0.03 V
Single thresh. accuracy = (0.056V + 0.043 V)/2 = 0.050 V
Limit: 0.039V to 0.061V

11. Select the connector and channel to be tested by pressing first the connector number and then the channel number on the data entry key pad. Connect in turn all data probes to the test setup and check for +50 mV ± 10 mV threshold accuracy.

Negative Offset Test

14. Change power supply polarity to negative and program the 8182A/B as follows:

15. Set Label A Single Threshold to -0.05 V.
(SOFTKEYS, Input , Threshold , -.05, VOLT)

16. Select Channel Configuration.
(SOFTKEYS, Input , Chnl Config)

17. Proceed as described for the Positive Offset Test and check all channels for -50 mV ±10 mV threshold accuracy.

Gain Test (Negative)

18. Remove both 40 dB attenuators and the 50 Ohm feedthrough from the test setup and set the power supply voltage to -9.00 V (reading on DVM).

19. Program Standard Channel Configuration.
(PAGES, Input , Config Control , Acq Control , EXECUTE)

20. Select Timing Diagrams; Select Single Threshold Label A in the Softkey Area.
(PAGES, TIMING DIAGR , SOFTKEYS, Input , Threshold , [Next Label if necessary])

21. Set the threshold to -8.81 V and check that the corresponding timing display is low. (-8.81, VOLT)

22. Set the threshold to -9.19 and on pressing VOLT , the timing display should jump to high.

23. Repeat step 21 and 22 for all data channels.

Gain Test (Positive)

24. Change power supply voltage to +9.00 V.

25. Set the threshold to +8.81 V and check that the corresponding timing display is high. (8.81, VOLT)

26. Set the threshold to +9.19 and on pressing VOLT , the timing display should jump to low.

27. Repeat step 25 and 26 for all data channels.

    Note: When testing channels at connectors 3 to 7, move the timing diagrams display up: (PAGES, TIMING DIAGR , Select Displ , Vert Window , ← or → [until required connectors are displayed], SOFTKEYS, Input , Threshold)

7-10 Qualifier Threshold and Impedance Tests

Specification

Threshold accuracy: ±3% of set value ±50mV.

Description

This test is used to measure the high and low level detection voltage (hysteresis) to determine the actual threshold voltage of the Qualifier Inputs (TTL setting). By measuring the voltage drop across the 20dB attenuator when switching the input to 50Ω, proper input impedance selection can be verified.

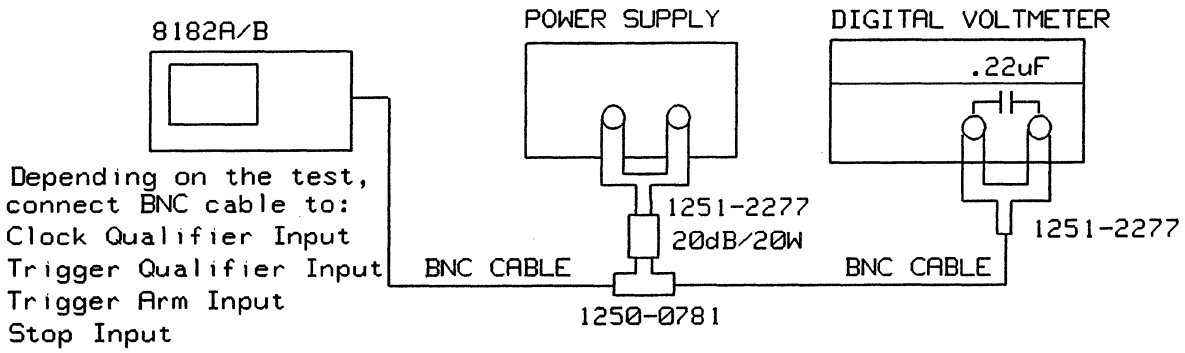


Figure 7-9. Test Setup for the Qualifier Threshold and Impedance Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
Capacitor	0.22 uF
Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
2x Cable Assembly BNC to BNC	HP 11170C

Clock Qualifier Threshold Accuracy Test

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Set Clock Source to Internal.
   (PAGES, CONTROL , Clock , Clock Source , INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, CONTROL , Autoarming , DELAY 0s)

4. Set Clock Qualifier to High Level; Set Threshold to +1.4V.
   (PAGES, CONTROL , Clock , Clock Qual , Level , HIGH LEVEL , EXIT , Threshold , 1.4, VOLT)

5. Connect the equipment as shown in Figure 7-9 and press **RUN**.

6. Increase power supply voltage slowly until a clock signal is just indicated in the upper left hand corner of the display and note the DVM reading.

7. Decrease the power supply voltage slowly until the clock indication just disappears and note the DVM reading.
   Result: The mean value should be between +1.31V and +1.49V.

8. Change power supply polarity and set 8182A/B threshold to -1.40V.

9. Increase power supply voltage slowly until the clock indication just disappears and note the DVM reading.

10. Decrease power supply voltage slowly until a clock signal is just indicated and note the DVM reading.
    Result: The mean value should be between -1.31V and -1.49V.

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.40V reading on the DVM.

12. Set the Clock Qualifier Input Impedance to 50Ω.
    (EXIT , Impedance , 50 Ω)

    The DVM should show approximately -0.7 V.

7-11 Trigger Qualifier Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Clock Source Internal.
   (PAGES, CONTROL , Clock , Clock Source , INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, CONTROL , Autoarming , DELAY 0s)

4. Trigger Qualifier High Level; Threshold +1.4V.
   (PAGES, CONTROL , Trigger , Trg Qualifier , Level , HIGH LEVEL , EXIT MM , Threshold)

5. Connect the equipment as shown in Figure 7-9 and press **RUN**.

6. Increase power supply voltage slowly until the status display in the upper right hand corner of the display jumps just from ARMED to IDLE (IDLE toggles) and note the DVM reading.

7. Decrease power supply voltage slowly until the display just jumps to ARMED and note the DVM reading.
   Result: The mean value should be between +1.31V and +1.49V

8. Change power supply polarity and set 8182A/B threshold to -1.40V.

9. Increase power supply voltage slowly until the display just jumps from IDLE to ARMED and note the DVM reading.

10. Decrease power supply voltage slowly until the display just jumps back to IDLE and note the DVM reading.
    Result: The mean value should be between -1.31V and -1.49V

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.4 V reading on the DVM.

12. Program Triger Qualifier Input Impedance to 50Ω.
    (EXIT MM , Impedance , 50 Ω)

    The DVM should show approximately - 0.7V.

7-12 Trigger Arm Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Set Clock Source to Internal; Set Clock Period to 1s.
(PAGES, CONTROL , Clock , Clock Source , INTERNAL , EXIT TM , Clock Period Increase [until 1 s is displayed])

3. Set Stop Delay (Internal) to 0.
(PAGES, CONTROL , Stop , Stop Delay , 0, ENTER NUMBER)

4. Set Autoarming Delay to 0s.
(PAGES, CONTROL , Autoarming , DELAY 0s)

5. Set Trigger Arm Slope to Positive (Threshold is +1.40).
(PAGES, CONTROL , Trigger , Trigger Arm , Slope , POS SLOPE)

6. Connect the equipment as shown in Figure 7-9 and press **RUN**.

7. Increase power supply voltage slowly until the 8182A/B switches from ARMED to ACTIVE (upper right hand corner of display).

NOTE

Continuous toggling may be caused by noise when the threshold level has just been reached.

The DVM reading should be between +1.31 V and +1.49 V.

8. Set Trigger Arm Slope to Negative; Set Threshold to -1.4 V.
(POS SLOPE , EXIT TM , Threshold , -1.4, VOLT)

9. Change power supply polarity, press **RUN** and increase power supply voltage slowly again until the 8182A/B switches from ARMED to ACTIVE. (See Note above.)

The DVM reading should be between -1.31 V and -1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40 V reading on the DVM.

11. Set Trigger Arm Input Impedance to 50Ω.
(EXIT TM , Impedance , 50 Ω)

The DVM should show approximately -0.7 V.

7-13 External Stop Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS , Recall , Standard Set , EXECUTE)

2. Set Clock Source to Internal; Set Clock Period to 100ms.
   (PAGES, CONTROL , Clock , Clock Source , INTERNAL ,
   EXIT TM , Clock Period Increase [until 100ms is displayed])

3. Set Stop Delay (Internal) to 0.
   (PAGES, CONTROL , Stop , Stop Delay , 0, ENTER NUMBER)

4. Set Autoarming Delay to 1s.
   (PAGES, CONTROL , Autoarming , DELAY 1s)

5. Set External Stop to Positive Slope (Threshold is +1.40).
   (PAGES, CONTROL , Stop , Stop Slope , POS SLOPE)

6. Connect the equipment as shown in Figure 7-9 and press **RUN**.

7. Increase power supply voltage slowly until the 8182A/B switches from ACTIVE to IDLE (upper right hand corner of display).

NOTE

Continuous toggling may be caused by noise when the threshold level has just been reached.

The DVM reading should be between +1.31V and 1.49V.

8. Program Negative Slope; Threshold -1.4 V.
   (NEG SLOPE , EXIT TM , Stop Thres , -1.4, VOLT)

9. Change power supply polarity, press **RUN** and increase power supply voltage again until the 8182A/B switches from ACTIVE to IDLE. (See the Note above.)

   The DVM reading should be between -1.31V and 1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40V reading on the DVM.

11. Set External Stop Input Impedance to 50Ω.
    (Stop Imp , 50 Ω)

    The DVM should show approximately -0.7V.

Chapter 8
Retrofit Procedures for HP Models 8180A/B, 8181A/B, 8182A/B

8-1 Introduction

This chapter describes the procedures when retrofitting (upgrading) the HP 8181A/B generator, the HP 8181A/B extender and the HP 8182A/B analyzer.

8-2 81801A/B Retrofit Procedure for 8180A/B (4 additional NRZ channels)

1. Remove top and bottom cover.

   When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rear frame as the holding screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector 3 if 0, 1 and 2 are already fitted).

3. Remove board spacer.

4. Ensure that the PC-edge connectors of the Module Board are clean.

5. Insert the Module Board A6 (A66) in the next available slot (e.g. Module 3 if Module 0, 1 and 2 are already installed).

6. Install data connector on the rear panel.

7. Install board spacer and readjust the Power Supply.

8. Perform Output Amplifier High/Low Level Adjustment for the retrofitted NRZ channels.

9. With top and bottom cover fitted, allow instrument to warm up for 30 minutes and check the skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version), referenced to the strobe clock signal (Performance test). If the skew of the NRZ channels is out of specification, readjust Strobe Reference Delay.

8-3 81801 A/B Retrofit Procedure for 8181 A/B (4 additional NRZ channels)

1. Remove top and bottom cover. When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rearframe as the holding screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector 7 if connectors 4, 5 and 6 are already occupied).

3. Remove board spacer.

4. Ensure that the PC-edge connectors of the Module Board are clean.

5. Insert the Module Board A6 (A66) in the next available slot (e.g. Module 7 if Module 4, 5 and 6 are already installed).

6. Install data connector on the rear panel.

7. Install board spacer and readjust the Power Supply.

8. Perform Output Amplifier High/Low Level Adjustment for the retrofitted NRZ channels.

9. With top and bottom cover fitted, allow instrument to warm up for 30 minutes and check skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version), referenced to the strobe clock signal (Performance test), of the 8180 A/B. If the skew of the NRZ channels is out of specification, readjust Extender 0 Delay slightly.

8-4 81802A/B Retrofit Procedure for 8180A/B (4 additional Timing channels)

1. Remove top and bottom cover. When removing the retaining screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rear frame as the retaining screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector3 if 0, 1 and 2 are already fitted).

3. Remove the board spacer.

4. Ensure that the PC-edge connectors of the Module Board and timing board are clean.

5. Insert the Module Board A6 (A66) in the next available location (e.g. Module 3 if Module 0, 1 and 2 are already installed).

6. Install data connector on the rear panel.

7. Insert the timing board A5 (A65) in location Timing 0 or Timing 1 if Timing 0 is already fitted.

8. Install board spacer.

9. Install bottom cover and continue with Power Supply Adjustment.

Module Board A6 (A66) Adjustment

10. Allow instrument to warm up and perform Output Amplifier High/Low Level Adjustment for retrofitted NRZ channels.

11. Check skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version) referred to the strobe clock signal.

NOTE

Readjust the Strobe Reference Delay only when the skew of the NRZ channels is out of specifications.

12. Check Date Flatness And Overshoot. Readjust only if necessary.

Timing Board A5 (A65) Adjustment

NOTE

Use Adjustment Cover and allow instrument to warm up for 30 minutes.

13. If this is the first time a timing board is being installed, then the Preadjustment For Timing Channels must be carried out.

14. Readjust Zero Delay for retrofitted Timing Channels and check Delay and Width ranges as described in Delay and Width Adjustment.

15. Check Zero Delay for both Clock Channels.

8-5 81821 A/B Retrofit Procedure for 8182 A/B (8 additional Data channels)

1. Remove top cover. When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the topcover, and gently levering the cover off the rear frame as the holding screw is removed.

2. Remover the cable cover from the rear frame.

3. Remove the blank cover from the next available connector (e.g. 4 and 5 if 0, 1, 2 and 3 are already fitted).

4. Remove the 4 screws from the connectors on the 08182-66530 board.

5. Install 08182-66530 board and fasten it with the additional 4 connector screws. (Discard the supplied washers.)

6. Ensure that the PC-edge connectors of the A5 (A65) Data boards are clean.

7. Insert the Data boards (08182-66505/66565) in the next two Data board locations (e.g. Data 4 and Data 5 if Data 0, 1, 2 and 3 are already installed).

NOTE

If more than 16 channels are installed, the -5.2V load must be removed. Disconnect the brown wire from the -5.2V connector and connect it to the GND connector (both located on the right hand side of the motherboard).

8. Connect the cables coming from the connector board 08182-66530 (installed in step 5 of this procedure) so that the connector marked with the blue dot is connected to the Data board with the even numbers (2, 4 or 6).

9. Fasten the connectors firmly to their corresponding Data boards using the supplied screws.

10. Perform adjustment as described for the A5 (A65) board in the adjustment procedure.

11. Ensure that all cables are correctly connected to their respective board.

12. Re-fit cable cover, board spacer and top cover.

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