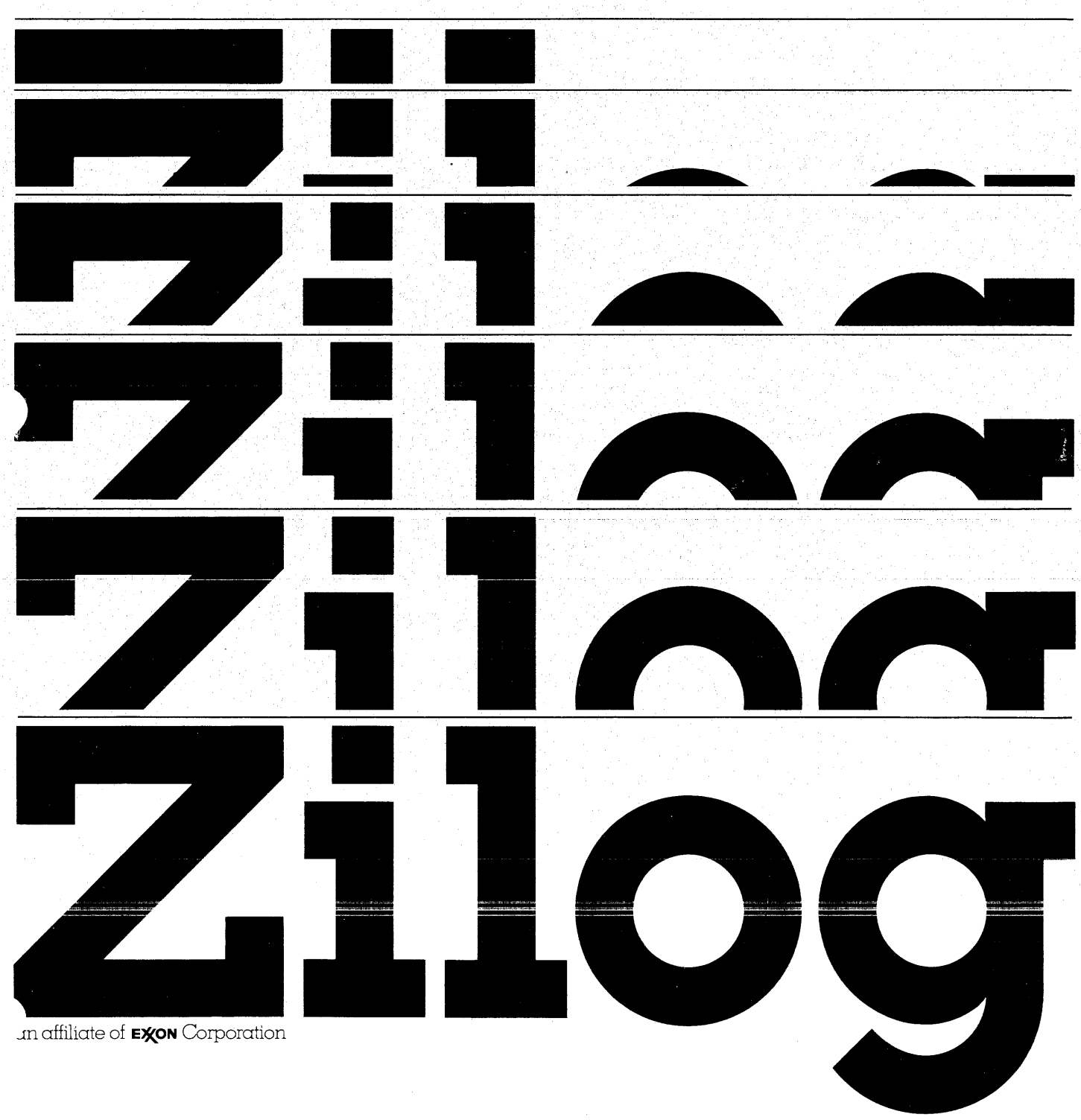
System 8000™ Central Processing Unit Hardware Reference Manual



an affiliate of EXXON Corporation

03-3200-01

September, 1982

PRELIMINARY MANUSCRIPT RELEASE

SYSTEM 8000 CENTRAL PROCESSING UNIT (CPU)

HARDWARE REFERENCE MANUAL

03-3200-01

PRELIMINARY VERSION

The information contained in this draft may undergo changes, both in content and organization, before arriving at its final form.

Preface

The System 8000 CPU Hardware Reference Manual describes the processor board capabilities and application within the System 8000. Logic Diagrams are provided within the Appendix and referenced to the circuit descriptions in Section 4. The board is factory prepared, installed and tested in the users system before shipment and should require no changes. Any field change should be by qualified field service personnel.

The following listed manuals provide more technical documentation for the System 8000:

Title	Zilog Number
System 8000 HRM	03-3237
Zeus System Administrator Manual	03-3246
Zeus Utilities Manual	03-3196
Zeus Reference Manual	03-3195

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SECTION 1
OVERVIEW

1.1. Description

The Zilog System 8000 Central Processor Unit (CPU) board (Figure 1-1) is the controlling processor board for the System 8000.

The System 8000 CPU is designed around the Zilog Z8001A 16-bit microprocessor which uses an advanced instruction set, 8 Mbyte segmented addressing space, and 16 bit registers. Memory management increases the addressing capability to 16 Mbyte by dynamic segment relocation and protection from three Z8010A Memory Management Units and special control logic. Software addressing is then independent of the physical memory address and eliminates the need to specify where information is actually located in memory.

The Zilog Z8001A segmented 6 MHz microprocessor runs the Zilog ZEUS operating system, a high performance implementation of UNIX. The operating system presently implements non-segmented operation while user programs can be either segmented or non-segmented.

The System 8000 CPU board initiates and controls transactions on both the system and input/output (I/O) bus. The Z8001A microprocessor acts as the host and controls the system bus Z-Bus Backplane Interconnect (ZBI) and all parallel and serial I/O to and from the system.

The CPU board (Figure 1-2), at P2/J21, connects directly to and controls the I/O bus and all I/O transactions pass through P2 to the parallel port or one of eight serial I/O ports. The eight serial channels support the RS-232C standard.

The System 8000 CPU board is one of several printed circuit boards in a system and is inserted into slot one of the card cage.

Plug P1/J11 connects to the ZBI bus and P2/J21 connects to the I/O bus. The connectors are three level 96 pin Euro standard. The Zilog ZBI is a 32-bit backplane bus which interconnects the boards of the system. Figure 1-1 identifies the components of the System 8000 CPU board.

1.2. Serial and Parallel I/O

Eight serial ports and one parallel printer port are implemented on the board using four Zilog Z80B Serial Input/Output(SIO) chips and a single Z80B Parallel Input/Output(PIO) chip. The eight asynchronous/full-duplex serial channels receive and transmit serial data. These channels support up to eight users, with channel 1 reserved for the console, and are RS232C compatible.

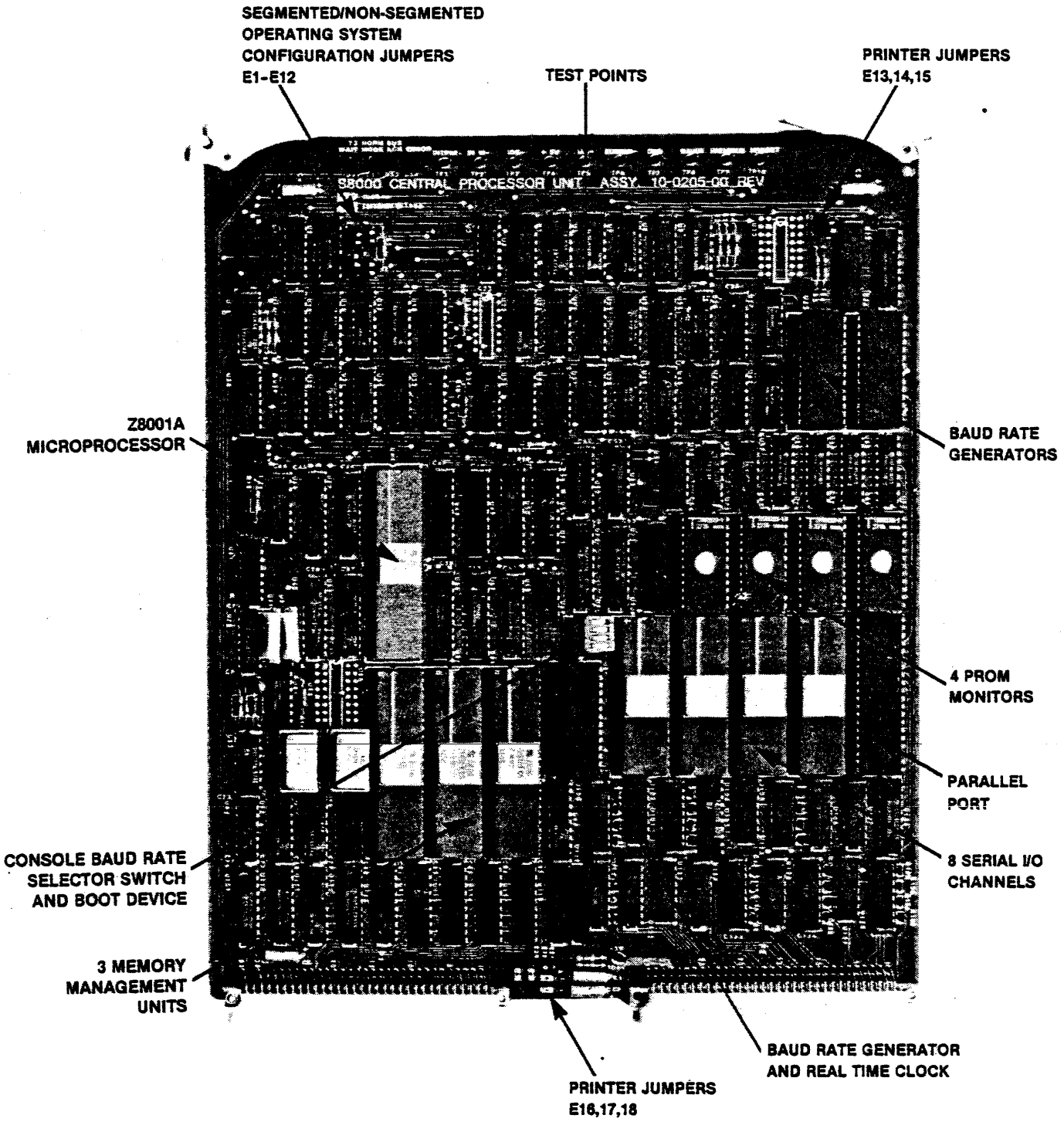


Figure 1-1 System 8000 CPU Board

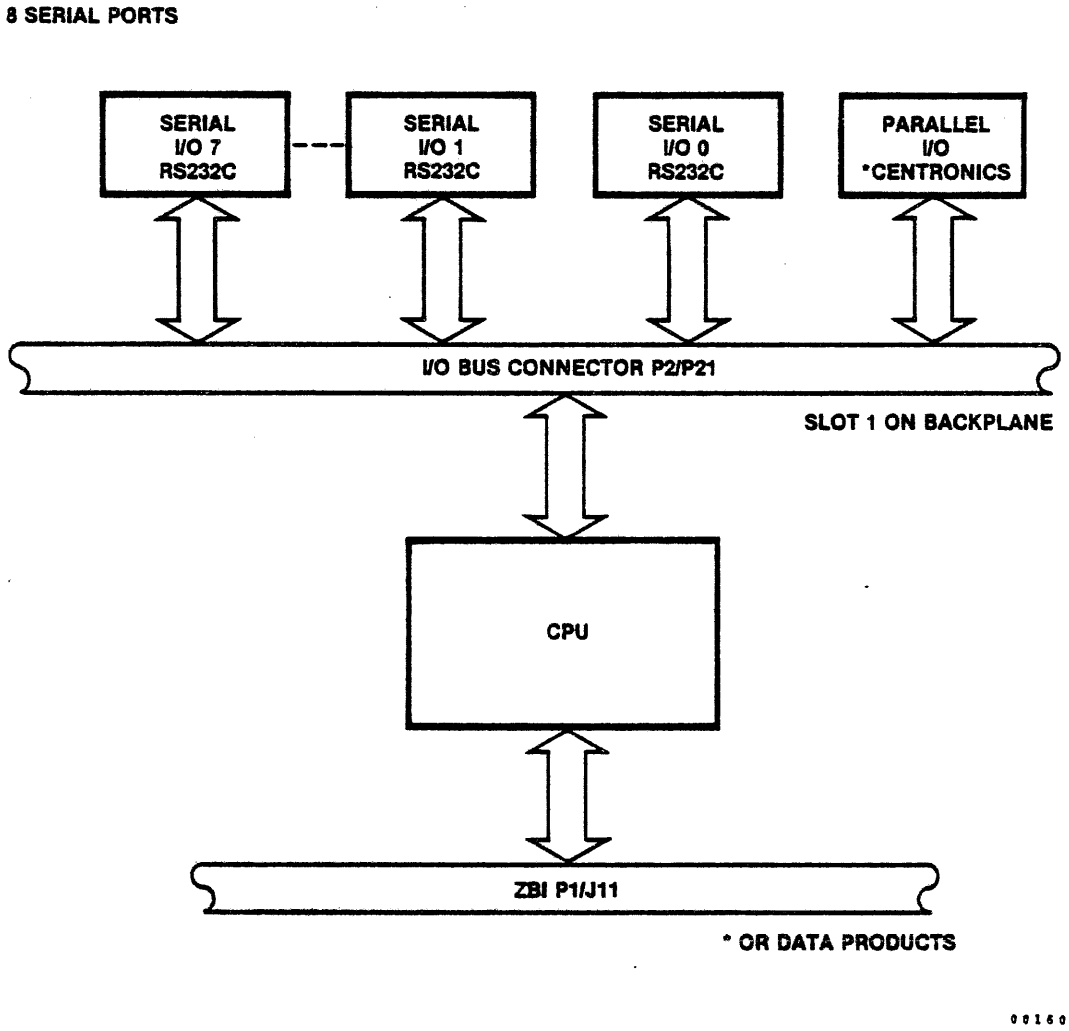


Figure 1-2 CPU Functional Diagram

Each channel has an independently programmed selectable baud rate from 300 Hz up to 19.2 KHz for individual terminals and supplied by three Z80B Counter Timer Circuits(CTCs). Each channel is limited to the same baud rate for receiving and transmitting. The CTCs are driven by a baud rate oscillator which is independent of the system clock frequency. A daisy-chain peripheral device priority scheme selects the highest priority onboard and offboard peripheral device.

Plug P2/J21 supplies the I/O connection to the offboard peripheral equipment. Either a Centronics or Data Products interface for a line printer is established by two jumper changes on the board.

1.3. Memory and Memory Management

The local onboard memory is used for bootstrapping the operating system and for hardware diagnostics. It consists of 8K bytes (4K words) of resident Erasable Programmable Read-Only Memory(EPROM) and 2K bytes (1K words) of Random Access Memory(RAM).

NOTE: The 8K EPROM has been increased to 16Kbytes as shown by the Logic Drawing (Appendix B) (DZ-0288).

Three Zilog Z8010A Memory Management Units (MMUs) facilitate an efficient and flexible usage of the System 8000 by dynamic relocation of tasks in main memory. Special control logic is implemented that supports all the major goals of memory management (Para.3.5). For the nonsegmented operating system, the three MMUS separate code(program),data, and stack areas, and the operating system uses segment 0 of each of the three MMUs for its code, data and stack space. The data and stack MMUs are selected by special hardware on the board that compares the logical address with the contents of a hardware system break register to determine the MMU selected. The MMU N/S- input selects the MMU.

The non-segmented user programs are run in any segment (2-63) while segmented user processes can use one or more logical segments (2-63) to (66-127). The SEG USER bit of the System Configuration Register must be set before running a segmented user process. The normal break register replaces the system break register and the NORMAL MMU input selects the MMU. This configuration reflects a non-segmented operating system for the segmented or non-segmented user.

SECTION 2
SPECIFICATIONS

2.1. Introduction

This section contains the electrical, physical, and environmental specifications. Information on ZBI and I/O bus signals, status signals and encoding, and jumpering is also included.

2.2. Electrical Specifications

Table 2-1 lists the CPU board power requirements for U.S. domestic systems.

Table 2-1. Electrical Requirements, Domestic

ITEM	REQUIREMENT
Voltage	+5Vdc, -5Vdc +-0.25Vdc
Current	3.5 Amps (Typical)

2.3. Physical Specifications

Table 2-2 lists the physical specifications for the board.

Table 2-2. Physical Specification

ITEM	REQUIREMENT
Height	27.9 cm (11 inches)
Width	22.9 cm (9 inches)

2.4. Environmental Specifications

The CPU board can be expected to perform reliably provided all environmental specifications are maintained.

Table 2-3. Environmental Specifications

Operating temperature:

10 degrees C (50 degrees F) minimum
40 degrees C (104 degrees F) maximum

Relative Humidity:

80% noncondensing

2.5. CPU I/O Connector

Figure 2-1 illustrates the 96 pin Euro standard connector with three rows (A,B,C,) of 32 pins each. This connector is used for both I/O (P2) and ZBI (P1) connection.

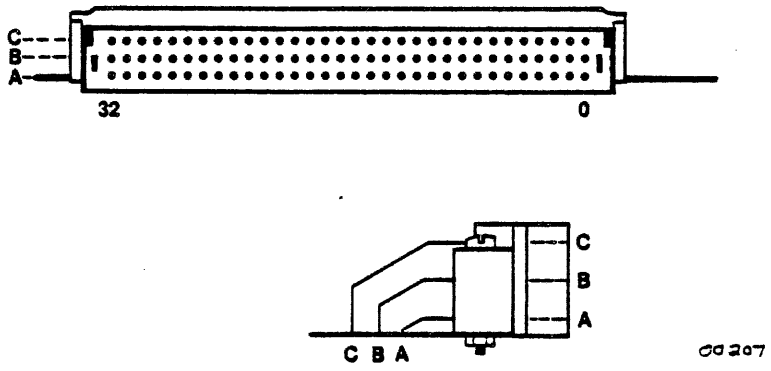


Figure 2-1 96 Pin Euro Standard Connector

Table 2-4 lists the I/O bus connections for plug P2 as well as listing the signal descriptions and pin assignments for each of the three rows of pins.

Table 2-4. CPU Pin Assignments (P2)

PIN	ROW A	ROW B	ROW C
1	TXRTN0	RXD0	DATA0
2	TXD0	CTS0	DATA1
3	RTS0	DTR0	DATA2
4	DSR0	RXD1	GND
5	TXD1	CTS1	DATA3
6	RTS1	DTR1	DATA4
7	DSR1	RXD2	GND
8	TXD2	CTS2	DATA5
9	RTS2	DTR2	DATA6
10	DSR2	RXD3	DATA7
11	TXD3	CTS3	GND
12	RTS3	DTR3	DATA STROBE/ DATA STROBE-
13	DSR3	RXD4	NOT USED
14	TXD4	CTS4	TXRTN1
15	RTS4	DTR4	GND
16	DSR4	RXD5	D.D./ ACKNOWLEDGE-
17	TXD5	CTS5	BUSY-
18	RTS5	DTR5	TXRTN2
19	DSR5	RXD6	GND
20	TXD6	CTS6	IF VALID/ FAULT-
21	RTS6	DTR6	ON-LINE/ SELECT
22	DSR6	RXD7	F.P. BUSACK INDICATOR
23	TXD7	CTS7	F.P. POWER-ON INDICATOR (GND)
24	RTS7	DTR7	F.P. NORMAL INDICATOR
25	DSR7	TXRTN5	NMI SWITCH (NORMALLY CLOSED)
26	TXRTN3	TXRTN6	NMI SWITCH (NORMALLY OPEN)
27	TXRTN4	TXRTN7	SWITCH RESET
28	+5Vdc	+5Vdc	F.P. INDICATOR V+ (+5Vdc)
29	-5Vdc	-5Vdc	-5Vdc
30	NOT USED	NOT USED	NOT USED
31	NOT USED	NOT USED	NOT USED
32	GND	GND	GND

NOTE: Pins 30 A,B,and C are connected to +12Vdc on the ZBI.

Table 2-5 lists the signal definitions for the CPU I/O bus.

Table 2-5. CPU I/O Bus, Signal Definitions

SIGNAL NAME	DEFINITION
TXD7 to TXD0	Transmit Data, 8-bits
RXD7 to RXD0	Receive Data, 8-bits
CTS7 to CTS0	Clear to Send
DTR7 to DTR0	Data Terminal Ready
RTS7 to RTS0	Request to Send
DSR7 to DSR0	Data Set Ready
TXRTN7 to TXRTN0	Transmit Return
DATA7 to DATA0	PIO Data
DATA STROBE	Data Products Data Strobe
DATA STROBE-	Centronics Data Strobe, Active Low
DATA DEMAND	Data Demand (Data Products) (Active High)
BUSY-	Printer busy
IFVALID	Interface valid (Data Products)
FAULT-	Paper Empty indication (Centronics)
ON-LINE	Online (Data Products)
F.P. BUSACK INDICATOR (Front Panel)	DMA in process. Disk or tape controller in control of bus
F.P.POWER-ON INDICATOR (GND) (Front Panel)	Ground for power-on indicator
F.P. POWER-ON INDICATOR V+ (Front Panel)	Indicates system is on
F.P. NORMAL INDICATOR (Front Panel)	CPU running user process

2.6. Bus Signals

Table 2-6 lists the pin assignments for the ZBI backplane 96 pin Euro connector (P1).

Table 2-6. ZBI Connector (P1) Pin Assignments

PIN	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	RESET-	WAIT-	CAVAIL
2	CAI-	CAO-	CPUREQ-
3	BAI-	BAO-	BUSREQ-
4	MMAI-	MMAO-	GND
5	IEI3	IEO3	MMREQ-
6	IEI2	IEO2	-
7	IEI1	IEO1	GND
8	INT1-	INT2-	INT3-
9	R/W-	B/W-	W/LW-
10	S2	S3	S4
11	S0	S1	GND
12	ME-	AS-	DS-
13	-	STOP-	N/S-
14	-	-	-
15	AD31	-	GND
16	AD28	AD29	AD30
17	AD25	AD26	AD27
18	AD22	AD23	AD24
19	AD20	AD21	GND
20	AD17	AD18	AD19
21	AD14	AD15	AD16
22	AD11	AD12	AD13
23	AD9	AD10	GND
24	AD6	AD7	AD8
25	AD3	AD4	AD5
26	AD0	AD1	AD2
27	PWRBAD-	MCLK	BCLK
28	+5V	+5V	+5V
29	-5V	-5V	-5V
30	+12V	+12V	+12V
31	-12V *	-12V *	-12V *
32	GND	GND	GND

* -12V is allocated space on the ZBI backplane, but is not used or generated by the System 8000. 12V is presently only used for Memory.

2.6.1. ZBI Signal Definitions: The ZBI signal definitions are listed in the System 8000 Hardware Reference Manual (03-3198-01)(Para.4.4)

2.6.2. ZBI Status Lines: The Z8001A CPU outputs the status (ST0-ST3) codes that when active high indicate the type of transaction currently on the ZBI bus. The S4 code is generated by board hardware. The encoding of these signals is shown in Table 2-7.

Table 2-7. Status Transaction Coding

S4	S3	S2	S1	S0	TRANSACTION
0	0	0	0	0	Internal Operation
0	0	0	0	1	Memory refresh
0	0	0	1	0	I/O reference
0	0	0	1	1	Special I/O reference
0	0	1	0	0	Segment trap acknowledge
0	0	1	0	1	INT 1 Interrupt Acknowledge
0	0	1	1	0	INT 3 Interrupt Acknowledge
0	0	1	1	1	INT 2 Interrupt Acknowledge
0	1	0	0	0	Data Memory Request
0	1	0	0	1	Stack memory request
0	1	0	1	0	Transfer between data memory and EPU
0	1	0	1	1	Transfer between stack memory and EPU
0	1	1	0	0	Program reference, nth cycle
0	1	1	0	1	Program reference, 1st cycle
0	1	1	1	0	Transfer between CPU and EPU
0	1	1	1	1	Reserved
1	x	x	x	x	Reserved

2.6.3. Data Width Codes: The Byte-Word Select (B/W-) and Word/Long-word Select (W/LW-) signals are encoded to define the data access width as shown in Table 2-8.

Table 2-8. Data Width: Byte, Word, Long Word

B/W-	W/LW-	DATA WIDTH
1	1	Sets data width to 8-bit byte on lines AD0-7.
0	1	Sets data width to 16-bit word on lines AD0-15
1	0	Sets data width to 32-bit double word size on AD0-32
0	0	Reserved

2.7. Jumper Selection

The CPU board is currently configured for a non-segmented operating system and shipped with jumper selection as listed under NON-SEGMENTED. The jumper selection is supported by software and can not be changed in the field. The segmented jumper selections are for reference only. Jumpers E1 through E12 determine the operating mode. The jumpers are configured as follows:

NON-SEGMENTED	SEGMENTED
E2 to E3	E1 to E2
E4 to E5	E5 to E6
E7 to E8	E8 to E9
E11 to E12	E10 to E12

CAUTION

These jumpers are properly set by the manufacturer and must not be changed by the user. Segmented jumper selections are for reference only.

2.8. Line Printer Jumper Selection

The line printer installation procedure is found in the System 8000 Hardware Reference Manual (03-3198-01). The ZEUS operating system can support a printer with either a Centronics/Printronix or Data Products interface. The CPU board is shipped with the jumpers E13 through E18 connected for a Centronics/Printronix printer interface. The printer interface may be selected as follows:

CENTRONICS/PRINTRONIX INTERFACE	DATA PRODUCTS INTERFACE
E13 to E14	E14 to E15
E17 to E18	E16 to E17

2.9. Baud Rate Selection

The console serial channel (channel 1) is identical to the other serial channels except that the monitor on the CPU board uses channel 1 to communicate with the system operator when the system is first turned on. The four-pole switch (U70) located toward the center of the CPU board uses switch positions one and four for baud rate selection. The switch positions two and three select the primary boot device listing for the SPUD diagnostics. The initial baud rate for channel 1 is factory set for 9600 baud. Table 2-9 lists the baud rate settings and selection of the primary boot devices. The baud rate settings allow a variety of terminals as the system console. The primary boot device as selected by the switch will always be listed and tested by the SPUD diagnostics as the first device on the list.

Table 2-9. Baud Rate Setting and Primary Boot Device (U70)

SWITCH 1, 4	BAUD RATE	SWITCH 2, 3	PRIMARY DEVICE
0 0	300	1 1	8 inch Disk
1 0	1200	0 1	5 1/4 inch Disk
0 1	9600	1 0	SMD Disk
1 1	19200	0 0	Reserved
		ON = 0	

SECTION 3
FUNCTIONAL DESCRIPTION

3.1. Description

The System 8000 CPU board combines the segmented addressing of the Z8001A CPU with the memory management capabilities of the Zilog Z8010 Memory Management Units (MMUs) for dynamic allocation of memory and segment relocation. This makes software addressing independent of the physical memory address when the MMUs are enabled by the programmable hardware System Configuration Register (SCR). This 8-bit hardware register controls and enables the onboard (local) and offboard (main) memory functions as well as selecting non-segmented or segmented user. The SCR is fully described in paragraph 3.2.2. Protection against segment violations is provided by attribute checking of the memory accesses. Main memory integrity is protected by the ECC Controller board which can detect and correct a single bit error and detect a double bit error.

The segmented memory address computed by the Z8001A microprocessor memory reference instruction is a 23-bit logical memory address. The memory address actually received by an offboard memory device is a 24-bit physical address when translated by the MMUs.

The onboard local memory is byte or word addressable on the CPU logical memory bus and is inaccessable to the system bus or the three MMUs. All instructions and word operands are word aligned and are addressed by even addresses. Local memory is entered for the power-up bootstrapping of the operating system and provides hardware diagnostics.

3.1.1. Z8001A CPU Memory Addressing: The Z8001A CPU computes 23-bit segmented logical memory addresses capable of addressing 128 relocatable segments of 64 Kbytes each for a total addressing range of 8 Mbytes. A 23-bit segmented address uses a 7-bit segmented address to point to the segment, and a 16-bit offset to address any byte relative to the beginning of the segment. The two parts of the segmented address can be manipulated separately. The segment number is an unsigned 7-bit integer ranging from zero to 127. The offset is an unsigned 16-bit integer ranging from zero to 65,535.

The Z8010A Memory Management Units transform the logical address output of the Z8001 CPU, comprised of concatenation of the segment and offset, into a 24-bit physical address.

The Z8001A CPU outputs status information from four status lines (ST0-ST3) and distinguishes between system mode and normal mode memory references by a status flag (N/S-). The status conditions are mutually exclusive and encoded to extend the addressing range or protect accesses to certain portions of memory. For each access to memory, the external circuit checks whether the CPU status is appropriate for the memory reference.

The Z8001A CPU can run in one of two modes: System or Normal. In the System mode, all of the instructions can be executed and all of the CPU registers can be accessed. This mode is is used for programs of the operating system. In normal mode, certain instructions including all I/O instructions are not executable. Also, the control registers of the CPU are inaccessible. User programs are run in normal mode.

The two running modes of the Z8001A CPU each have a copy of the stack pointer, one for system mode and the other for normal mode. Two sets of stack pointers facilitate task switching when interrupts or traps occur. The normal stack never contains system information.

The Memory Management Units (MMUs) use the NORMAL/SYSTEM(N/S-) input to select the appropriate MMU for memory management.

3.1.2. Z8010A Memory Management Units: The three MMUs support separate translation tables for each Z8001A CPU address space. Each of the Z8010A 64 variable sized segments (256 to 64 Kbytes) can be mapped into a total physical address space of 16 Mbytes. All 64 segments are randomly accessible.

Each MMU uses a translation table to transform the 23-bit logical memory address output from the Z8001A CPU into a 24-bit physical memory address which becomes the buffered output to the ZBI bus and memory controller. Three MMUs allow separation of code, data, and stack references. Each memory management unit can translate addresses for 64 segments. The memory management units are enabled by the D1 (MMU ONH) bit within the programmable hardware 8-bit I/O port System Configuration Register (SCR) described in paragraphs 3.2.2 and 3.2.3.

3.2. Memory Addressing

The address generated by the Z8001A CPU is always a byte address. However, the local memory addressing is organized in 16-bit words and the main (offboard) memory in 32-bit double words. All instructions and word operands are word aligned and addressed by even addresses. For all word transactions with memory, therefore, the least significant address bit is zero. For all memory byte transactions, the least significant address bit determines which byte of the memory word is needed. An even address specifies the most significant byte, and an odd address the least significant byte.

3.2.1. Local Memory: The local memory space is 8 Kbytes (4K words) of EPROM program memory and is organized as words at locations 0 through 1FFE hexidecimal. NOTE: Refer to Appendix A for substitute 16K EPROM. Also, 2 Kbytes of read/write memory are addressable from locations 2000 through 27FF hexidecimal. The RAM memory is both byte and word addressable. Onboard memory space facilitates the power-up bootstrapping of the operating system and provides the hardware diagnostics. It is entered on power-up or system reset on the logical memory bus of the Z8001A CPU and resides in segment zero.

3.2.2. SCR Memory Selection: The board hardware System Configuration Register (SCR) is a programmable 8-bit (D0-D7) input/output port with a 4-bit (D4-D7) upper read/only nibble configured by a four bit dip switch (U70) for console baud rate.

The lower four bits (D0-D3) provide the CPU with onboard memory, MMU, segmented user, and ECC Error NMI enabling functions. The D0-D3 bits are cleared (logic 0) on system RESET to initialize the system: Onboard memory is enabled, MMUS are disabled, nonsegmented user enabled, and ECC Error cleared.

As long as board memory enable bit D0 of the SCR is reset (logical 0),the total local memory space 0 through 27FF hex overlays the segment 0 main memory space 0 through 27FF. At power-up or system reset time, the SCR D0 bit is cleared to logic 0 and enables the local memory. Writing a logic 1 to bit D0 of the SCR disables onboard memory and maps all memory references to offboard main memory. The contents in local RAM are not lost.

The main memory address space begins at location 4000 hex, and when the local memory space is enabled, a dead space exists from locations 2800 through 3FFF hex. All references to local memory require one wait-state insertion. Main memory references require virtually no wait-states. However, main memory references that activate the error correction logic on the ECC controller do require one wait-state insertion.

3.2.3. Main Memory: The System 8000 CPU main memory address space is 16 Mbytes using the board memory management units (MMUs). The SCR D1 bit enables the MMUs.

At power-up or system reset, the SCR D1 bit (MMU ONH) is cleared (logic 0) and all memory references through the MMUs are inhibited. Main memory references are routed directly from the Z8001A CPU to the main memory over the ZBI bus. The logical addresses generated by the CPU are the physical addresses received by the main memory. Therefore, for addresses AD23 through AD0:

```
        AD23   =  0
AD22 - AD16    =  7-bit segment,by instruction or PC
AD15 - AD0     =  16-bit offset address,by instruction or PC
```

Memory Management references to main memory cannot be generated by the MMUs until the SCR D1 bit is set to logic 1. The status of this bit however, does not impair the programming of the three MMUs with special I/O instructions. Refer to the SCR and Memory Management sections for more detailed description.

3.2.4. Byte Transactions: When a byte transaction is being executed by the Z8001A CPU, the Byte-Word Select line (B/W-) is high for byte selection.

3.2.4.1 Byte Read: For a local memory read, the Read/Write (R/W-) output line is high and both banks of memory are read. The reading of the required byte is on either the upper or lower half of the Z8001A CPU address/data bus. Either the high or the low half of the address/data bus is selected by the CPU for the byte destination, depending on the least significant address bit A0 being even or odd respectively. When A0 is low, the upper (even) half of the address/data bus is read. If A0 is high, the lower (odd) half of the data bus is read. During a byte read transaction between the CPU and memory, the memory need only

respond with a 16-bit word containing the byte data. (See byte swap buffer Para.3.2.4.3)

3.2.4.2 Byte Write: For a local memory write, the Read/Write (R/W) line is low and either the odd or even bank of memory is enabled by the address bit A0. If A0 is high, the odd bank is enabled, if low the even bank is enabled. The Z8001A CPU duplicates the byte data on both halves of the CPU address bus when writing a byte of data to memory. Therefore, the memory can pick off the byte operand from either half of the bus by enabling the even or odd bank of memory contingent on the least significant address bit A0.

3.2.4.3 Byte Swap Buffer: Under ZBI specification, during byte transactions, only the low-order odd half of the system bus, AD0-AD7, can be used. The ZBI bus specification requires that all byte operands be read on the low-order odd half of the system bus regardless of their address. For byte reads with odd addresses or byte writes that duplicate the data on both halves of the bus, this is not a problem. However, byte reads with even addresses require that the byte operand be placed on the high-order even half of the CPU address/data bus.

A byte swap buffer is activated on byte reads with even addresses to duplicate the byte data on both halves of the CPU's internal address data bus. This ensures that the byte operand will appear on the high-order even half of the Z8001A CPU internal bus on an even address byte read memory transaction. The byte-swap buffer is totally transparent to the operating system and user.

3.3. I/O Addressing

The Z8001A CPU's input/output addresses are represented as 16-bit words that reference either byte or word operands. Two separate I/O address spaces, Standard I/O and Special I/O, are accessed through a separate set of I/O instructions which can be executed only when the Z8001A CPU is in the system mode. The standard I/O instructions transfer data between the CPU and onboard and offboard peripheral devices.

Special I/O instructions transfer data beween the Z8001A CPU and the three Z8010A MMUs for memory management.

3.3.1. Standard I/O: All of the System 8000 CPU onboard devices except the three Z8010 MMUs are byte addressable using standard I/O instructions which occupy the odd portion of the I/O address space from FF81 through FFFF hexidecimal.

The I/O addresses for the I/O devices and their channels are listed in Table 3-1. All onboard I/O devices except the MMUs have been placed on the odd address boundries and they receive and transmit byte data over AD0 through AD7 of the Z8001A CPU internal address/data bus.

Table 3-1. I/O Address,Device and Channel

I/O ADDRESS	I/O DEVICE AND CHANNEL
FF81	SIO 0, channel 0, data
FF83	SIO 0, channel 1, data
FF85	SIO 0, channel 0, control
FF87	SIO 0, channel 1, control
FF89	SIO 1, channel 2, data
FF8B	SIO 1, channel 3, data
FF8D	SIO 1, channel 2, control
FF8F	SIO 1, channel 3, control
FF91	SIO 2, channel 4, data
FF93	SIO 2, channel 5, data
FF95	SIO 2, channel 4, control
FF97	SIO 2, channel 5, control
FF99	SIO 3, channel 6, data
FF9B	SIO 3, channel 7, data
FF9D	SIO 3, channel 6, control
FF9F	SIO 3, channel 7, control
FFA1	CTC 0, channel 0, (baud 0 for SIO 0, channel 0)
FFA3	CTC 0, channel 1, (baud 1 for SIO 0, channel 1)
FFA5	CTC 0, channel 2, (baud 2 for SIO 1, channel 2)
FFA7	CTC 0, channel 3
FFA9	CTC 1, channel 0, (baud 3 for SIO 1, channel 3)
FFAB	CTC 1, channel 1, (baud 4 for SIO 2, channel 4)
FFAD	CTC 1, channel 2, (baud 5 for SIO 2, channel 5)
FFAF	CTC 1, channel 3
FFB1	CTC 2, channel 0, (baud 6 for SIO 3, channel 6)
FFB3	CTC 2, channel 1, (baud 7 for SIO 3, channel 7)
FFB5	CTC 2, channel 2
FFB7	CTC 2, channel 3
FFB9	PIO 0, channel A, data
FFBD	PIO 0, channel A, control
FFBB	PIO 0, channel B, data
FFBF	PIO 0, channel B, control
FFC1	SCR, read/write,System Config. Register
FFC9	SBR, read/write,System Break Register
FFD1	NBR, read/write,Normal Break Register
FFD9	SVR, read segment trap segment address
FFE9	Soft Reset
FFF1	Low-Byte Register,read segment trap low-byte address
FFF9	Low-Byte Register,read segment trap IF1 low-byte

3.3.2. Special I/O: The special I/O address space of the Z8001A CPU is used to communicate with one or more of the three Z8010A MMUs. Any special I/O reference detected in the CPU status disables both the onboard and offboard address buffers and enables the I/O registers internal to the MMUs.

The special I/O address determines at which port of the selected MMU the information is either read or written. Address bit AD0 must be low on all MMU references since the MMUs are addressed on even byte boundries. Address bits AD1, AD2,and AD3 can individually select the Code, Data, and Stack MMUs, respectively, when low (0). The same data can be written to the same input/output port of all three MMUs by a special I/O Write with all three address bits AD1 through AD3 low. The byte operands are transferred to the MMUs over AD8 through AD15 of the CPU's internal address/data bus. The address bits AD0 through AD7 are not recognized by any of the three MMUs. A summary of the special I/O addresses of the Code, Data, and Stack MMUs is given in Table 3-2.

Table 3-2. Special I/O MMU Address

CODE	DATA	STACK	DESCRIPTION
00FC	00FA	00F6	Read/write mode register
01FC	01FA	01F6	Read/write segment address register(SAR)
02FC	02FA	02F6	Read violation type register
03FC	03FA	03F6	Read violation segment number register
04FC	04FA	04F6	Read violation offset(high-byte) register
05FC	05FA	05F6	Read bus status register
06FC	06FA	06F6	Read instruction segment number register
07FC	07FA	07F6	Read instruction offset (high-byte) register
08FC	08FA	08F6	Read/write base field
09FC	09FA	09F6	Read/write limit field
0AFC	0AFA	0AF6	Read/write attribute field
0BFC	0BFA	0BF6	Read/write descriptor,all fields
0CFC	0CFA	0CF6	Read/write base field,increment SAR
0DFC	0DFA	0DF6	Read/write limit field, increment SAR
0EFC	0EFA	0EF6	Read/write attribute field,increment SAR
0FFC	0FFA	0FF6	Read/write descriptor,increment SAR
11FC	11FA	11F6	Reset violation type register
13FC	13FA	13F6	Reset SWW flag in VTR register
14FC	14FA	14F6	Reset Fatal flag in VTR register
15FC	15FA	15F6	Set all CPU inhibit attribute flags
16FC	16FA	16F6	Set all DMA inhibit attribute flags
20FC	20FA	20F6	Read/write descriptor selector counter

3.3.3. Offboard I/O: All I/O addresses from 0 to FF80 and even I/O addresses from FF80 through FFFF hexidecimal are mapped offboard and can be word addressable for all I/O addresses and byte addressable for even or odd I/O addresses for special and standard I/O. The offboard I/O devices with even addresses are subject to the byte swap buffer on I/O reads the same as the memory read byte transactions.

3.4. Reset, Interrupts and Traps

The Z8001A CPU supports three types of exceptions or conditions that can alter the normal flow of program execution. These are system reset, interrupts, and traps. Because the CPU responds to these exceptions and conditions in a similar manner, they are discussed together in the following paragraphs.

3.4.1. System Reset: The system reset is generated from the onboard power-up reset circuit or by the RESET button on the System 8000 front panel. It overrides all other operating conditions in the CPU, including interrupts, traps, bus requests, and stop requests. Upon system reset, the following occurs:

1. All bits in the SCR are cleared.

2. The local memory space is enabled, the CPU jumps to location 2 of segment 0 and reads the Flag and Control Word register(FCW). It then reads the 7-bit program counter (PC) segment number from location 4. Next it reads the 16-bit PC offset from location 6. The following CPU FETCH starts the program.

3. The MMU ONH bit (D1) is disabled and main memory references are direct and without MMU assistance. The mode register, violation type register, and descriptor selection counter are cleared on all MMUs. However, the Master Enable flag in the MMUs is not reset to zero.

4. The SEG USER bit (D2) is cleared to logic 0 and a non-segmented USER is supported.

5. Parity and ECC Error NMI (D3) is cleared.

6. All receivers and transmitters of the SIOs (channels) are disabled. All SIO control registers must be initialized. All SIO interrupts are disabled.

7. All CTC channels stop counting and all channel interrupt enable bits are cleared. All CTC control registers must be initialized.

8. All port mask registers in the Z80B PIO are cleared to inhibit all port data bits. All "ready" handshake signals are inactive. Mode 1 of the PIO is selected, port interrupt enable flip-flops are reset, port output registers are reset, and the vector address registers are not reset.

3.4.2. Non-maskable Interrupts: Non-maskable interrupts cannot be disabled (masked) by software and typically are reserved for external events that require immediate attention.

There are three sources of NMI in the System 8000:

1. A manual NMI can be generated in the System 8000 with the START pushbutton on the front panel. This can be disabled by turning the POWER/LOCK key switch on the front panel to the LOCK position. When the START pushbutton is pressed immediately after a RESET has occured (manual or power-up), the power-up diagnostics firmware is invoked. At the conclusion of this diagnostic, if no errors have been recorded, the words "POWER UP DIAGNOSTICS COMPLETE" appear on the console and the ZEUS operating system is automatically booted within the next 45 seconds.

2. A power-fail NMI is generated to the CPU if the System 8000 power supply detects an oncoming power failure. The CPU then provides an orderly shut-down of the system.

3. An NMI can be generated to the CPU if a double bit non-correctable ECC error has been flagged by the ECC Controller, and if the Clear ECC Error bit(D3) of the SCR has been set to enable an ECC NMI. This bit is initially cleared at the SCR on a system reset or power-up.

3.4.3. NMI Identification: If an interrupt or trap is detected by the Z8001A CPU, the subsequent initial instruction fetch is initiated, but aborted. The next CPU machine cycle is the interrupt acknowledge transaction. This transaction acknowledges an interrupt or trap and reads a 16-bit identifier word from the device that generated the interrupt (in this case an NMI source). The identifier word, along

with the program status information, is stored on the system stack and new information is loaded into the PC and FCW.

The CPU generates an NMI acknowledge status code "0101" (ST3-ST0) when the NMI source is one of those listed in Table 3-3. The external hardware on the System 8000 CPU enables a four bit error buffer to place on address/data lines AD0 through AD3 a 4-bit NMI identifier coded as in Table 3-3.

Table 3-3. NMI Identification

NMI SOURCE	AD3	AD2	AD1	AD0
MANUAL	0	0	0	1
POWER FAIL	0	0	1	0
ECC ERROR	0	1	0	0

Bits AD4 through AD15 are "don't care" bits in an NMI acknowledge identifier word if the NMI source is one of the above. If the NMI source is external to the processor and not listed above, the NMI error buffer remains off and a 16-bit identifier word is read from the system bus.

3.4.4. Vectored Interrupts: The 16-bit identifier word can be used to identify the source of an interrupt or trap. In a vectored interrupt(VI), the identifier is also used by the CPU as a pointer. The pointer selects a particular service routine associated with the source of the interrupt.

3.4.5. The VI Daisy Chain: The Z80B SIO, Z80B CTC and Z80B PIO are all Z-BUS peripherals designed to interface readily with the Zilog Z80 CPU. Special logic has been implemented on the System 8000 CPU board to mimic the Z80 CPU timing and the Z80 peripherals cannot discern that the Z8001A CPU is the host processor.

Because of the large number of Z80 peripherals on the System 8000 CPU, an interrupt daisy chain assigns priority to these devices to hasten the interrupt request time. Basically, each Z80 device on the processor contains two lines (IEI and IEO) which serve as links in the daisy chain. Figure 3-1 shows the interrupt daisy chain for the System 8000 CPU.

IEI : Interrupt Enable In (Input, active high)

The IEI signal is used with IEO to form a priority chain when there is more than one interrupt driven device. A logic 1 on this input indicates that no other device of higher priority is being serviced by the CPU.

IEO : Interrupt Enable Out (Output, active high)

The IEO output is high only if the input IEI is high and the CPU is not servicing an interrupt from this device. The IEO output is connected to the IEI input of the next lower priority device in the chain. Therefore, IEO blocks lower priority devices from interrupting the CPU while a higher priority device is being serviced. Table 3-4 lists the order of priority for the peripheral devices on the System 8000 CPU.

Table 3-4. Peripheral Device Priority

PRIORITY	PERIPHERAL DEVICE	FUNCTION
1	CTC-0	Single Step, also generates Baud 0, Baud 1,and Baud 2
2	CTC-1	Generates Baud 3,Baud 4,and Baud 5
3	CTC-2	Generates Baud 6,Baud 7 and the Real Time Clock
4	SIO-0	Serial Channels 0,1
5	SIO-1	Serial Channels 2,3
6	SIO-2	Serial Channels 4,5
7	SIO-3	Serial Channels 6,7
8	PIO-0	Line Printer Interface
9	(OFFBOARD I/O)	(Serial I/O Expansion,etc)

Vectored interrupts from any of the onboard peripherals automatically disables interrupts from lower priority peripheral devices in the chain. Offboard peripheral devices have the lowest priority.

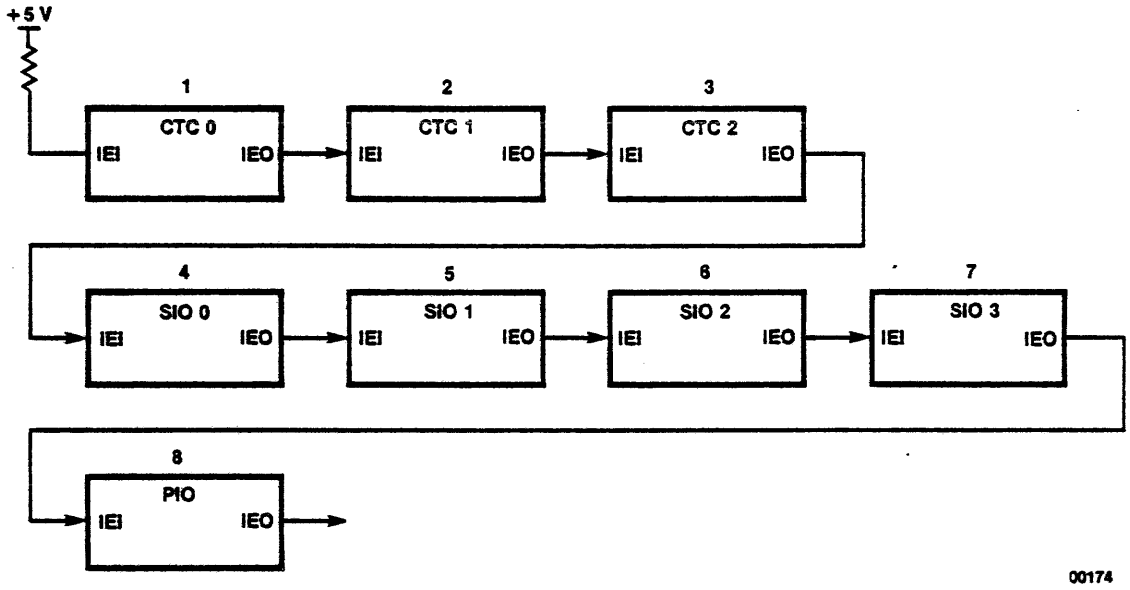


Figure 3-1 Peripheral Interrupt Priority

3.4.6. Non-vectored Interrupts: There are no non-vectored interrupt sources resident on the System 8000 CPU.

3.4.7. Traps: The Z8001A CPU supports three traps which can be generated internally, and one trap which may be generated externally by any of the three Z8010 MMUs.

3.4.7.1 Extended Instruction Trap: A trap occurs when the CPU encounters an extended instruction while the Extended Processor Architecture (EPA) bit in the Flag Control Word (FCW) is disabled (zero). This trap allows the program to simulate the operations of an Extended Processing Unit (EPU) when no such device exists in the system or to abort the program. There are no EPUs on the System 8000 CPU.

3.4.7.2 Priviledged Instruction Trap: A trap occurs when executing a priviledged instruction while the CPU is in Normal Mode. Priviledged instructions can only be executed in system mode.

3.4.7.3 System Call Trap: The System Call instruction always causes a trap. This instruction provides a controlled access from normal mode to system mode operation.

3.4.7.4 Segment Trap: This trap occurs when one of the three MMUs detects a memory access violation such as an offset greater than the assigned segment length. On a memory access violation, the MMU activates the Suppress line used to inhibit memory requests. Segment trap remains low until the CPU trap acknowledge signal is received. When an access violation occurs, Suppress is asserted for that cycle and all subsequent CPU memory references until the end of the instruction. The acknowledge cycle is always preceded by an instruction fetch cycle that is aborted.

Following the acknowledge cycle, the CPU automatically pushes the program status words and program counter onto the system stack, and loads a new program status word and program counter. The segment trap line is reset during the acknowledge cycle and no suppress is generated during the stack push.

The segment trap also occurs on a write warning of a write into the lowest 256 bytes of a stack. This sets the SWW flag but no segment trap request is generated. Separate hardware on the board detects and generates a segment trap and suppress if memory reference is made to a system segment while the CPU is in normal mode.

3.5. Memory Management

The major functions of the memory management Z8010 MMUs on the System 8000 CPU board are:

1. To provide flexible and efficient allocation of main memory resources during the execution of the operating system and user tasks.

2. To support multiple independent tasks that can share access to common resources.

3. To provide protection from unauthorized or unintentional access to data or other memory resources.

4. To detect obviously incorrect use of memory by an executing task.

5. To partition main memory resources and separate user from system functions.

The three Z8010 MMUs are connected to the Z8001A CPU with special logic that is used in one of the two following configurations:

Configuration 1 - Supports a non-segmented ZEUS operating system. In this mode, the operating system is expected to run in logical segments 0 and 1 while User processes can be either segmented or non-segmented. Non-segmented user processes can run in any logical segment from 2 through 63 while segmented User processes can run in one or more logical segments 2 through 63 or 66 through 127. The ZEUS operating system must configure the hardware correctly before it begins to run the corresponding type of User process. This is done by setting the SEG-USER bit of the SCR.

Configuration 2 - Supports a segmented operating system. In this mode, the operating system runs segmented and resides in all logical segments from 0 through 63. Non-segmented and segmented user processes have their own set of segments. Segmented User processes can reside in any of the segments from 0 through 127 while non-segmented User processes are still restricted to segments 2 through 63.

3.5.1. MMU Configuration and Control:

3.5.1.1 Non-segmented Operating System: The non-segmented operating system runs in segment 0 using Segment Descriptor Register (SDR) 0 of the MMUs M1,M2, and M3 for respective code, data, and stack areas. MMU M1 is used for translating program memory references while M2 and M3 are used for translating all other memory references.

The selection between M2 and M3 is based on a comparison between the logical address and the contents of the System Break Register (SBR), a program addressable hardware register. Logical addresses with values lower than the SBR are treated as data addresses and are directed to the Data MMU (M2). Logical addresses that are equal to or greater than the SBR are treated as stack addresses and are directed to the Stack MMU (M3).

3.5.1.2 Non-segmented User Program: A non-segmented User program runs in segment 63. However, the hardware permits any segment between 2 and 63 to be used. As in the case of the non-segmented operating system, the SDR in segment 63 in M1, M2, and M3 is used for separate code, data, and stack areas, respectively. However, the normal break register (NBR) is used instead of the SBR to distinguish between data, and stack references. The NBR is also a program addressable hardware register.

3.5.1.3 Segmented User Program: A segmented user program uses M2 and M3 for an address space consisting of 124 or 128 segments, again without separating code, data, and stack areas. For the non- segmented operating system, the segment numbers 0, 1, 64, and 65 are reserved since it requires the SDR 0 and 1 of M2 and M3. Refer to paragraph 3.5.2.

3.5.1.4 Jumper Configuration: The system segmented/ nonsegmented operation is by hardware jumpers on the board and by the operating system software. The hardware jumpers configure the MMU control logic for a non-segmented operating system when shipped. These jumpers are not to be changed in the field.

The hardware jumper connections are given in the Installation and Operation section.

3.5.1.5 Break Registers: For the nonsegmented operating system and User, two 8-bit hardware registers, the System Break Register (SBR) and the Normal Break Register (NBR), are accessable as input/output ports on the CPU board, and assist the Memory Management subsystem. During any memory reference, the 16-bit logical address offset generated by the CPU is compared to a break value given by the contents of either the SBR or the NBR. The SBR is referenced for the break value if the segment number is zero, one, 64, or 65; otherwise, the NBR is referenced.

3.5.1.6 System Segments and Protection: The processor logic partitions the segments into system segments, (logical segments 0, 1, 64, and 65) and user segments, (logical segments 2 through 63 and 66 through 127). A reference to a system segment always enables an SBR for comparison with the logical address offset. A reference to a user segment always enables the NBR. These comparisons are independent of whether the CPU is executing in system mode or normal mode.

The system segment detection logic prohibits normal mode programs from accessing system mode segments. Normal mode references to system segments are not allowed and result in no MMU being selected and a segment trap forced upon the CPU. This violation is maintained until cleared by the segment trap acknowledge status of the CPU.

The MMU also generates a segment trap when it detects an access violation or a write warning condition. In the case of an access violation, the MMU activates a Suppress used to inhibit memory access. Segment traps to the CPU are handled

similarly to other types of interrupts.

3.5.2. System Configuration: The system configuration for the System 8000 CPU is by choice of bit D2 (SEG USER) in the system configuration register for either a 0. (low) non-segmented user program or a 1 (high) for a segmented user program. The operating system is presently configured by jumpering of the board memory management control logic for a non-segmented operating system. The present configuration options are as follows:

Operating system SS = 0, SEG USER bit D2 SU = 0

Operating system SS = 0, SEG USER bit D2 SU = 1

3.5.2.1 SS=0,SU=0: This configuration is used for a non-segmented operating system running non-segmented user programs. The operating system runs in segment 0 while a user program runs in any segment 2 through 63 , with 63 the recommended segment. The MMU M1 is enabled for program references indicated by a CPU status code 11xx, an instruction space access.

For memory references other than program references, the address offset generated by the CPU is compared against the contents of the SBR if the segment number is zero or one, or with the NBR if the segment number is 2 to 63. If the result is less than zero, the select logic enables the data MMU (M2), otherwise the stack MMU M3 is enabled. Hardware on the board detects CPU Normal Mode reference to System Mode segment 0, generates a segment trap violation to the CPU and disables the MMUs.

3.5.2.2 SS=0, SU=1: When the SCR SEG USER bit D2 is a 1 (high), the configuration supports a non-segmented operating system running a segmented user process. When the CPU is in the system mode with the segment number zero or one, the operation is the same as above. The code, data and stack references are directed to M1,M2, and M3, respectively, and the contents of the SBR are used to select between data and stack references. In normal mode, MMU M2 is enabled for segment numbers 2 through 63, and MMU M3 is enabled for segment numbers 66 through 127.

If a memory reference is made to segment 0, 1, 64, or 65 while the CPU is in normal mode, a segment trap violation is generated and all three MMUs are disabled. A suppress

signal is also generated to protect the system data and system stack areas from being accessed by the user program.

In system mode, if the segment number of a user segment is generated (segments 2 through 63 or 66 through 127) the address translation is the same as in the normal mode. The separation of code, data, and stack spaces is deactivated, MMU M2 is enabled for segments 2 through 63, and MMU M3 is enabled for segments 66 through 127. This allows the operating system to access any user segment directly.

3.5.2.3 System Access to User Space: To access a user segment, the operating system can use a free segment slot and set up its SDR to point to the same memory area as the target user segments SDR. A non-segmented operating system running a non-segmented process can directly access the user data and stack areas by going to system mode and using the user segment number. To access the user code segment, one of the unused segment slots (e.g.62) is set up to point to the code segment. The SDRs for this slot in M2 and M3 are both set up to point to the code segment so that the contents of the NBR do not matter.

SECTION 4
CIRCUIT DESCRIPTION

The major elements of the System 8000 CPU board are described in this section and each element is explained in its relation to the system. The following text describes the major circuits and devices involved in the operation of the System 8000 CPU board. Reference is made to the logic drawings included in the Appendix for clarity and understanding.

4.1. Z8001A CPU

The 6MHz Z8001A CPU is the host microprocessor of the System 8000. It is a 48 pin segmented/nonsegmented CPU with 16-bit programmable accumulator and index registers for byte or word operation. The system and normal stack pointers separate system from normal program information.

Certain instructions, including all I/O instructions, can only be executed in system mode. Present configuration of the System 8000 CPU is as a nonsegmented operating system.

Program status from the status registers is provided to the program counter which consists of two 16-bit registers containing the program counter offset and 7-bit segment number. The flag and control word (FCW) consists of two 16-bit registers with flags for segmented/nonsegmented, system/normal, and vectored and nonvectored interrupt operation.

When an interrrupt or trap occurs, the current program status, consisting of the PC, FCW, and 16-bit identifier, is automatically pushed on the system stack.

The System 8000 CPU communicates with the System 8000 memory controller and peripherals through the Zilog ZBI bus backplane. However, I/O and terminal and printer communication is through the eight full duplex RS232C serial channels and one parallel printer I/O port supplied by the four SIO and single PIO onboard chips.

Handshaking logic generates M1-, RD-, and IORQ- signals that interface the Z80 peripherals and the Z8001A CPU and emulate the Z80 CPU.

The System 8000 uses the 16-bit word addressing of the Z8001A CPU for byte addressing of local memory and I/O addressing to the onboard I/O devices. The CPU board uses a 16-bit time shared data bus latched by the onboard memory address buffers (U62,U47 LS373 Octal Transparent Latches) and controlled by the Address Strobe (AS) signal. Onboard memory data buffers (U63,U46) are bidirectional bus transceivers, with data direction controlled by the W/R- signal from inverter (U68).

A BD DATA ENABLE- signal is generated to the onboard memory/I/O data buffers (U63,U46) from the onboard enable data logic which is gated by the IDS,IW/R- and the onboard memory selector NON BD signals. The CPU has 3-state buffered status and control signal outputs from U118 for off-board status and control. The BUS ACK- signal disables the CPU status and control bus buffers and notifies ZBI devices that the CPU has relinquished the bus. An indication of bus release is provided by an LED on the front edge of the board.

4.2. Clock Generation

The clocks on the CPU board for System 8000 and I/O timing originate from a 44.4 MHz oscillator (U85). The divide by 8 (U98) is used for the 5.5 MHz onboard square wave clocks A and B. After passing through a Z80 driver, Clock A is applied to the Z8001 CPU and the MMUs. Clock B is applied to the I/O peripheral devices (CTCs,SIOs, and PIO) also after passing through a Z80 driver.

The separate buffered output bus clock ,B CLK, synchronizes all elements of the system and ZBI bus transfers. A master clock (MCLK) output, four times the B clock frequency, is also derived from U98 and serves as the master clock for the System 8000. The clock generation circuit is shown in Figure 4-1.

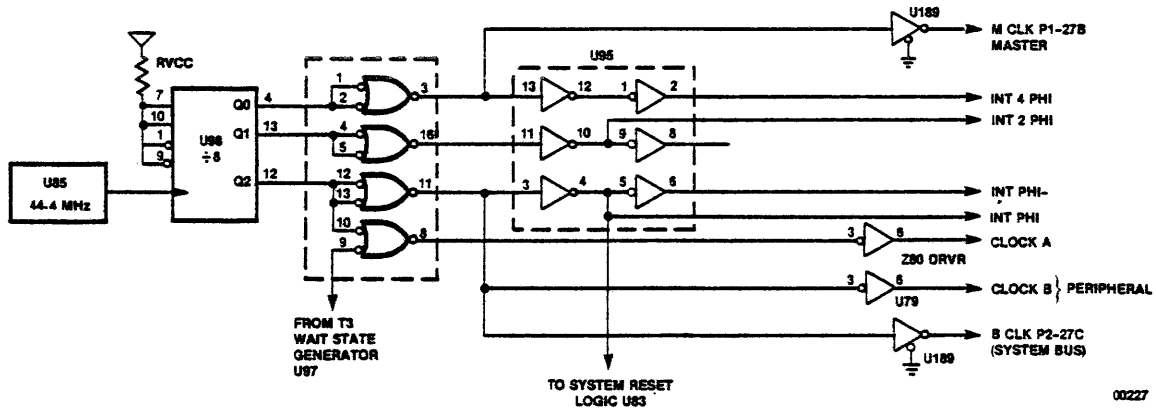


Figure 4-1 Clock Generation Circuit (Sheet 11)

4.2.1. Baud Clock: The 2.4576 MHz oscillator (U83) is divided by two by U83 and supplies baud rate clock to the counter-timer circuits (CTCs) for baud generation to the serial input/output (SIO) circuits. The baud rate clock is applied directly to the CTCs to produce a programmable baud rate independent of the system clock rate.

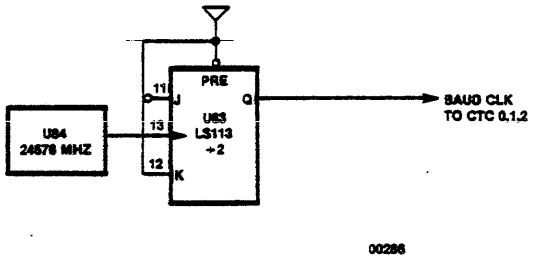


Figure 4-2 Baud Clock Generator (Sheet 11)

4.2.2. Real Time Clock: A real time clock is concatenated from two spare channels in CTC 2 (U89). These channels are driven by an independent baud rate oscillator so that CTC programming remains independent of the system clock frequency.

4.3. Parallel I/O Ports

The Z80B PIO (U94) uses ports A and B for interfacing the line printer (Centronics or Data Products) to the System 8000. At Port A, bidirectional buffer (U103) supplies the printer control output and printer status input lines. Port B is the printer data output port(B0-B7).

From Port B, the data bits (B0 through B7) are buffered (U108) and output as data bits (Data 0 through Data 7) through the P2/J21 I/O connector to the printer connector on the back panel. Figure 4-3 shows the parallel I/O circuit printer interface.

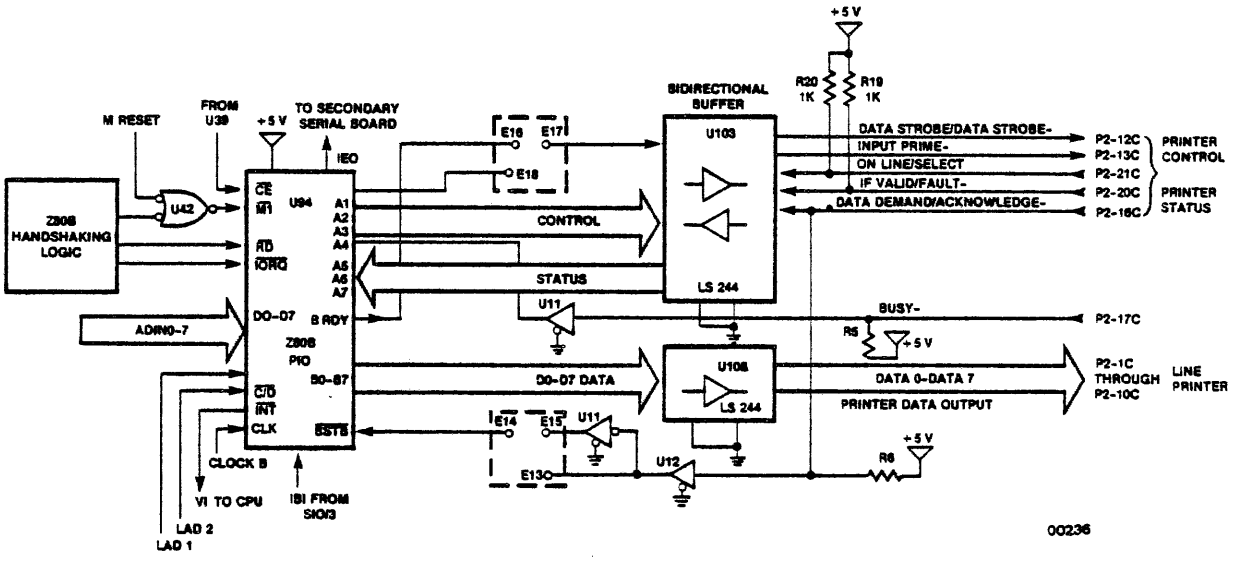


Figure 4-3 Parallel I/O (Sheet 7)

4.3.1. Printer Control Outputs: The parallel printer interface Data Strobe- or Data Strobe signal is configured by jumper from either the A port A0 output or the BRDY output of the PIO. The jumper configuration E17 - E18 is the Centronics/Printronix standard interface direct from the A0 output.

The E16 - E17 configuration supplies the Data Products positive Data Strobe signal from the BRDY PIO output. The remaining control bits A1,A2, and A3 are not used.

Table 4-1 lists the control signals for the two configurations.

Table 4-1. Printer Control Signals

Bit Number	Centronics	Data Products
0	Data Strobe-	Data Strobe
1	Not Used	Not Used
2	Not Used	Not Used
3	Not Used	Not Used

4.3.2. Printer Status Inputs: The printer status parallel inputs to the PIO are buffered by U103 and input at the A port bits A4 through A7. The jumper E13 to E14 puts an active low signal on the BSTB- strobe input to the PIO after the signal is passed through the buffer U12. At the same time, the signal is applied to the A7 bit input of Port A. This is the Centronics Acknowledge- signal that the printer is ready for data transmission.

The positive active signal Data Demand is the Data Products counterpart of this signal which is inverted by jumpering E14 to E15. A printer Busy status is received at A4 as an active positive signal, after being inverted by U11,and is the same for both printer interfaces. The A5 and A6 inputs remain high for both high and low input signals due to the +5V pull-up resistors R19 and R20. Table 4-2 shows the printer status signals for both the Centronics and Data Products printer interface.

Table 4-2. Printer Status Signals

Bit Number	Centronics	Data Products
4	Busy-	Busy-
5	Select	Online
6	Fault-	Interface Valid
7	Acknowledge-	Data Demand

4.4. Serial Input/ Output

The Z80B SIO/2 serial input/output supplies two fully independent full-duplex asynchronous serial data communications channels. Four SIO/2 devices on the System 8000 CPU board are the eight serial (SIO) input/output channels that support ,with additional hardware, the RS-232C standard for serial communications.

The SIO channels 0 through 7 are provided by the Z80B SIO/2 devices, SIO 0 through SIO 3 (U90 to U93). Each channel has separate programmable baud rate generation from one of three channels within the three Z80B Counter/Timers (CTCs), CTC 0 through CTC 2 (U43,U44 and U89).

Each SIO channel is supplied by a separate baud rate generator channel (ZC/TO0 - ZC/TO2) within the CTC. An independent 1.2288 MHz baud rate clock is supplied to the clock triggers of each CTC.

Figure 4-4 illustrates the SIO channels and the supporting baud generation from the CTCs. The SIO channels are intended for asynchronous communications only.

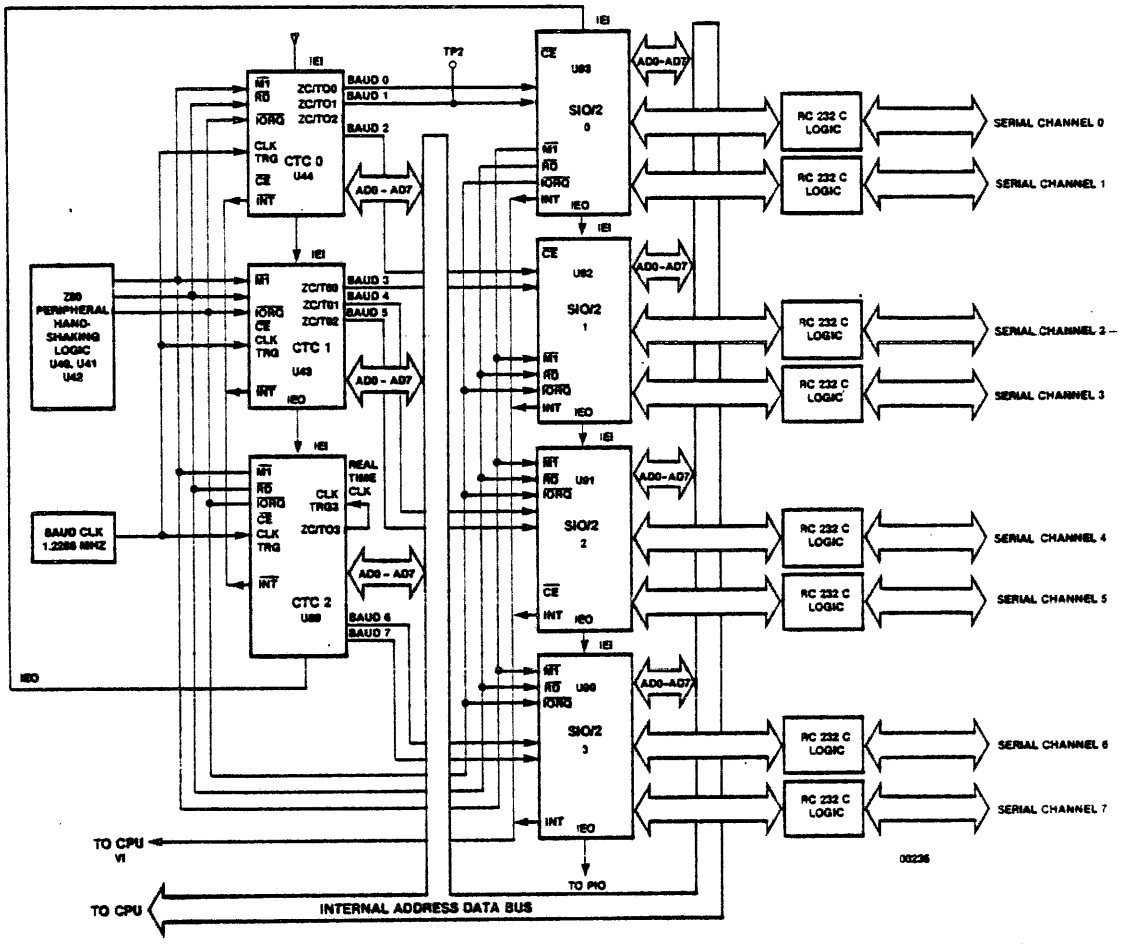


Figure 4-4 Serial I/O with CTC Channels
(Sheets 4, 5, 6, 7)

4.4.1. SIO/CPU Interface: The SIO devices communicate with the Z8001A CPU over the internal data bus using data bits D0 through D7. SIO options are controlled by software and set when control bytes are written from the CPU to the SIO registers. The options are established separately for each SIO channel of the four SIO devices. Once this initial step is complete, the remaining communication between the SIO and the CPU is by vectored interrupt. The SIO informs the CPU by the interrupt that a single character transfer is required. The CPU responds by branching to an interrupt service routine for the single character transfer. The memory address for beginning the service routine is derived from the interrupt vector supplied by the SIO. Each channel of each SIO is assigned a unique vector.

4.5. Interrupts

When an interrupt or trap is detected by the Z8001A CPU, the subsequent instruction fetch is initialized but aborted. The next CPU machine cycle is an interrupt acknowledge transaction. The transaction acknowledges an interrupt or trap and reads a 16-bit identifier word from the device that generated the interrupt. The identifier word is stored by the CPU in System stack along with program status information and either encoded for a vectored (VI) or non-maskable interrupt (NMI) and output on ZBI status lines S0 through S4 and also to the CPU Status Decode logic. A nonvectored interrupt is available on the ZBI, but it is unused on present board products.

4.5.1. Vectored Interrupt: For a vectored interrupt, transaction code 0111 is placed on the external hardware CPU Status Decode logic. Transaction code 0111 is presented at A,B,C, and G2A of the CPU Status Decode logic U25 and U26. A VI ACK signal is decoded and combined with the peripheral handshaking logic to produce the M1-, RD-, and IORQ- inputs on the Z80B device acknowledging the vectored interrupt. The device then places the 8-bit vector on the data bus to be read by the CPU. The CPU reads the 16-bit word (vector and 8-bit status byte) and it is stored on the system stack of the CPU. New status information is loaded into the program counter(PC) and the flag control word (FCW).

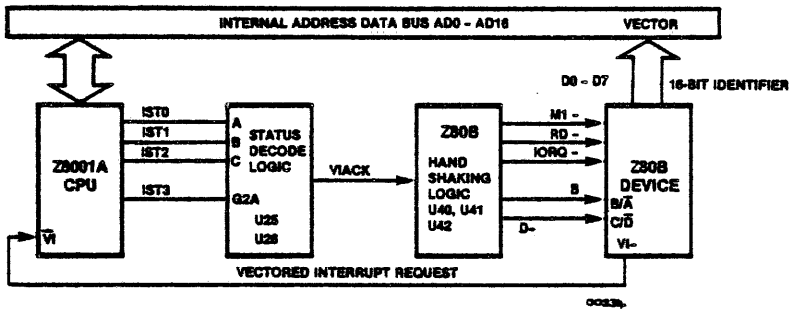


Figure 4-5 Vectored Interrupt

4.5.2. Vectored Interrupt Daisy Chain: The Z8001A CPU acknowledges the peripheral SIO,CTC, and PIO devices using a device priority "daisy chain" scheme. A vectored interrupt from a higher priority device in the chain automatically disables interrupts from those of lower priority. In Section 3, Table 3-4 lists the priority assigned to onboard and offboard peripherals.

The interrupt "daisy chain" has been implemented because of the large number of peripheral devices serviced both on and off the CPU board. Each Z80B peripheral device has a separate input and output line linked to the next device as shown in Figure 4-5. Both the Interrupt Enable In (IEI) and the Interrupt Enable Out (IEO) signals are active high.

A logic "1" on the IEI input to a device means that no other device of higher priority is being serviced by the CPU. The IEO output signal is high only when the IEI input signal is high and the CPU is not servicing an interrupt from this device. The IEO signal is connected to the IEI input of the next lower priority device, and blocks the lower priority devices from interrupting the CPU while a higher priority device is being serviced.

The order of priority is controlled by the IEO AND gating and by combining U37 and U38, the vectored interrupt accelerator, to produce the IEO signal block to the ZBI bus and the SIO 2,SIO 3, and PIO 0 IEI signals.

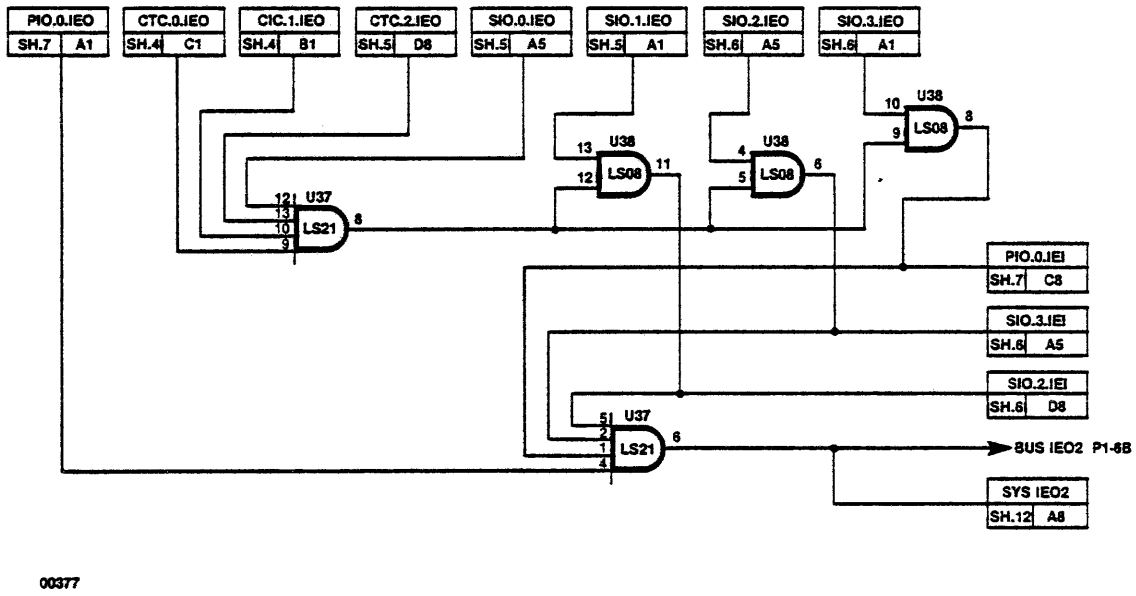


Figure 4-6 Interrupt Priority Connection (Sheet 14)

4.5.3. NMI Identification: On receiving an NMI, the CPU responds by generating an NMI Acknowledge transaction status code 0101 on the ZBI status lines (S3 -S0). The CPU status decoding logic (U25,U26) then produces an NMI logic enabling signal at the AND gate (U8). If the source of the NMI is from the CPU board, the NMI logic hardware on the board enables a four-bit error buffer, the NMI Identifier Register (U12).

The NMI identifier register encodes the first four data bits (AD0-AD3) of the AD0-AD15 internal address data bus as an NMI Identifier word. The CPU identifies the source of the NMI by reading the four data bits (AD0-AD3) of a 16-bit identifier word placed on the address/data bus.

This NMI identifier word is coded as a Manual, Power Fail, or ECC Error as shown in Table 3-3. If the NMI source is not one of the three listed and is external to the processor, the NMI identifier register is not enabled and the 16-bit identifier word is read from the system bus.

4.5.4. System Reset Logic (Sheet 11): The system reset logic is initiated by the front panel RESET pushbutton signal SW RESET- at P2-27. This signal is buffered and applied to the negative OR gate U78 (Figure 4-7).

Also applied to U78 is the onboard SOFT RESET- signal from the program shutdown in the event of power fail. The SOFT RESET- signal is generated by accessing I/O address FFE9. On being OR gated, either of these two signals enable the J-K flip-flop (U83) generating a reset.

When the system power supply detects a low voltage output, the POWER FAIL- signal at P1-27A comes from the system power supply to the K input of U83. The K input is normally high from pull-up resistor R18. Output Q- of U83 is clocked by an inverted Clock B signal to produce the system reset signal MRESET-.

The POWER FAIL signal is an inverted output to the NMI logic and produces the BUS NMI- to the CPU. The CPU then reads the NMI identifier from the address bus and issues a reset to the system by performing a soft reset.

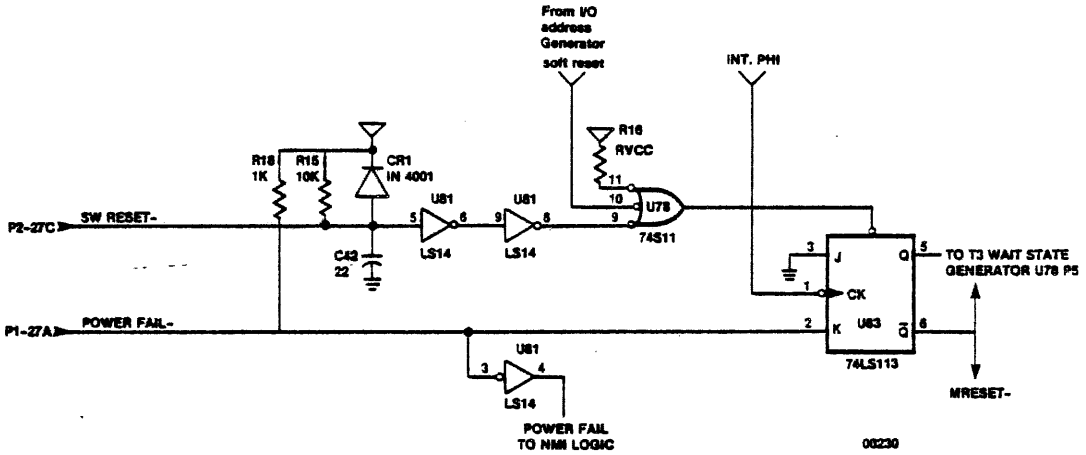


Figure 4-7 System Reset Logic (Sheet 11)

4.6. Memory Addressing

The address generated by the Z8001A CPU is either a byte or word address. However, the CPU board local memory is organized as 16-bit words. All the instructions and word operands are addressed by even addresses and for all word transactions the least significant address data bit (AD0) is zero.

For all byte transactions to local or main memory, the least significant address/data bit (AD0), determines that the most significant data byte is needed when AD0 is even (zero). The least significant byte is needed when address/data bit (AD0) is odd (one). For a data byte read from the ZBI bus of an even address to meet ZBI specification, the low order

data byte (AD0-AD7) is placed on the high order even half(IAD8-IAD15) of the CPU data bus.

4.6.1. Byte Transactions: For the least significant byte/read transaction to be executed by the CPU, the Byte/Word (B/W-) and Read/Write- (R/W-) output signals are both high and with buffers (U111 and U113) enabled, both halves of the address/data bus are then read by the CPU.

For an offboard byte read transaction between the CPU and memory, the address/data bit (AD0) when high enables the byte swap buffer (U112) and disables the buffers (U111 and U113) putting the low data byte on the upper even half of the board data bus. The CPU reads the appropriate byte from the data bus.

4.6.2. Read-Only Memory: The local read-only memory space consists of four (2k x 8) EPROMS (U74-U77) (8 Kbytes) addressed at locations 0 through 1FFE hexidecimal. (See Appendix for Model 10/11 and Models 21 and 31 applications.) Each pair of EPROMS store the low and high bytes of each word. Since the CPU always reads full words from local memory, the least significant address bit (AD0) is not used in address decoding. The EPROMS are addressed by latched addresses LAD1 through LAD11.

When the internal memory request(IMEM REQ-) and board memory on (BD MEM ON-) signals are received at the onboard memory address decoder (U55), logic addresses (LAD 12,13,14) and the ANDED LAD14 and LAD 15 are input and decoded to produce the signals for the onboard memory select logic (sheet 10) that separates the EPROM and RAM areas.

The one-of-eight memory address decoder selects between the EPROM high and low byte pairs by gating (U56) the decoder output signals (BDMEMA2K-,BDMEMB2K-) with IW/R-, all signals active low. The decoder output (BDMEMC2K-) enables the onboard RAM as part of the onboard memory select circuit (sheet 9).

4.6.3. Read/Write Memory: The local read/write 2Kbyte RAM memory consists of four 2114 RAMs (U57-U60).

The gating of the LAD 0, IR/W-, IW/B-, and BDMEMC2K- signals (logic diagram sheet 9) by the onboard memory select logic (U54 and U56) creates the MEMC2KLO- low byte chip select input at RAMS U57 and U58 and the MEMC2KHI- signal chip select high byte input to RAMS U59 and U60. When LAD 0 is

low the high byte is read or written, when high the low byte is read or written.

For word operations for both read and write, the B/W- CPU output is low and the select logic enables both banks of memory.

4.7. Byte Swap Buffer

The byte swap buffer (U112, sheet 13) is an LS244 octal three state buffer activated on an offboard byte read of an even address by a special byte swap control logic circuit. On an even address (AD0 low) the least significant data byte (AD0-AD7) on the ZBI bus is placed on the most significant half (IAD8- IAD15) of the CPU address/data bus when the byte swap buffer is enabled.

The signal ENA BYTE SWAP and the inverted ENA BYTE SWAP- are created by control logic (sheet 4) to enable the the byte swap buffer (U112) and disable the bidirectional buffers (U111,U113, sheet 13). The input signals IR/W-, IB/W-, and latched address bit LAD 0 are AND gated (U33), when high, to create the input buffer enable signal (ENA BYTE SWAP) and the inverted ENA BYTE SWAP- signal.

The ENA BYTE SWAP and NON BD signals are gated at U31 with the gated output of the IW/R- and IDS- signals from the bus address/data steering logic to enable the byte swap buffer. The inverted ENA BYTE SWAP- and NON BD signals are gated at the same time to disable the buffers U111 and U113.

The low byte (AD0-AD7) input of the ZBI bus, normally on the bidirectional buffer (U111), is placed by the byte swap buffer(U112) from the ZBI to the upper half of the CPU data bus (IAD8-IAD15).

4.8. Memory Management Control Logic

The three Zilog Z8010A memory management units (U86,U87,and U88) each having 64 separate segment descriptor registers that accept a 23-bit logical memory segment address to be translated into a 24-bit physical memory location.

Logic on the board partitions segments into system segments (0,1, 64, and 65) and user segments (logical segments 2-63, 66-127). A reference to a system segment always enables a system break register. A reference to user segment always enables the normal break register. Normal mode references to system segments are not allowed and result in a segment

violation to the CPU and no MMU selected.

4.8.1. Non-segmented Operating System: For a non-segmented operating system, the segment descriptor register (SDR) number 0 is used in each of the memory management units (MMUs). The MMUs M1,M2,and M3 are identified for code, data, and stack areas respectively. M1 translates program memory references while M2 and M3 translate all other memory references.

The selection of M2 or M3 is by a comparison of the upper byte of the 16-bit logical offset and the contents of the system break register(SBR) programmed at the FFC9 address of the I/O address generator (U24).

The SBR (U72,sheet 10) is a program addressable hardware register that inputs the programmable address byte to the comparator (U52, U53). When compared with the logical address upper byte (LAD 8 - LAD 15), logical values lower than what is contained in the register produce an active DATA REF output. The output is then gated and produces the MDATA- input to the Data MMU M2. If after comparison the logical values are greater than or equal to the SBR value, an inactive DATA REF is produced and activates the MSTACK- input of the stack MMU M3 (U86).

The memory management control logic produces the MCODE-, MDATA, and MSTACK- signals to the Normal/System- (N/S-) inputs of each of the three Code, Data, and Stack MMUs for MMU selection. When the N/S- line matches the Normal Mode Select (NMS) flag within the MMU, the MMU is enabled and address translation performed.

Logical addresses with values lower than the SBR are treated as data addresses and directed to the data MMU M2. Logical addresses equal to or greater than the SBR are treated as stack addresses and directed to the stack MMU M3.

4.8.2. Non-segmented User Program: A non-segmented user program runs in segment 63 using segment descriptor register 63 in M1,M2, and M3 to provide the separate code, data, and stack areas. The normal break register (NBR) (U71) replaces the SBR for the user program. The logical address comparison and MMU selection for user is the same however, the addressing of the NBR is FFD1.

4.8.3. Segmented User Program: A segmented user program uses M2 and M3 to provide an address space consisting of 124 segments without separating code, data, and stack areas. The high order segment line SN 6 on M2 and M3 is grounded (logic 0) and M2 and M3 only see segments 0 through 63.

When the segmented user control bit is set high (logic 1) in the SCR register, with the CPU in Normal mode, either M2 or M3 is enabled for address translation. This depends on whether the Z8001A CPU SN 6 line is logic 0 (OFF) or logic 1 (ON). If SN 6 is logic 0, MMU M2 is enabled. If SN 6 is logic 1, M3 is enabled. So even though MMU M3 is used for translating USER segments above 63, the Upper Range Select bit (URS) in the MMUs will always be zero.

Segment numbers 0,1,64 and 65 are reserved for the operating system since it requires SDR number 0 of M2 and M3. When a segmented user program is run under a non-segmented operating system, external hardware prohibits access to system segments in normal mode.

4.8.4. MMU Configuration: The MMU configuration on the System 8000 CPU board is organized in part by the board jumpers E1 through E11 in the memory management control logic, and in part by the operating system software. The hardware jumpers configure the MMU select logic for a non-segmented operating system.

The operating system configures the hardware System Configuration Register correctly for segmented or non-segmented user support before running the corresponding type of process.

NOTE

The E1 through E11 jumpers are factory installed and should not be changed in the field.

4.9. System Configuration Register

The CPU communicates with the system configuration register (SCR) as a programmable 8-bit I/O port (Figure 4-7). The lower nibble (D0-D3) can be written for different system functions, while the upper nibble (D4-D7) reads the switch selectable system console baud rate. The upper nibble bits D4 and D5 are used to choose one of four baud rates for the system console by setting the rocker DIP switches 1 and 4 of U70. The selectable baud rates are 300,1200,9600, and 19200 baud (Table 2-9). The board is shipped from the factory set for 9600 baud. It is important that terminal baud rates

agree with the system baud rate selection. Switches 2 and 3 of U70 are used to select the primary boot device listing for the SPUD Diagnostic.

When addressed by FFC1 from the address generator (U24,sheet 12) with write (IR/W-) and system configuration (SYS. CONFIG-) lines both low , the SCR register (U36,sheet 14) inputs the lower nibble data bits ADIN0 through ADIN3 and sets control bits D0 - D3. The D0 through D3 control bits BDMEMON-,MMUONH, SEG USER, and CLR PARITY- respectively, are part of the system configuration control of the separate board functions. When the CPU reads the system configuration from buffer (U51), the read (IW/R-) and SYS. CONFIG- inputs are both low gating U22 and enabling the buffer U51. The upper nibble (ADIN4-ADIN7) is preset and controled by the baud rate selector switch (U70).

The onboard diagnostic monitor requires that before power-up the system console serial channel be set to the appropriate baud rate (Figure 4-8).

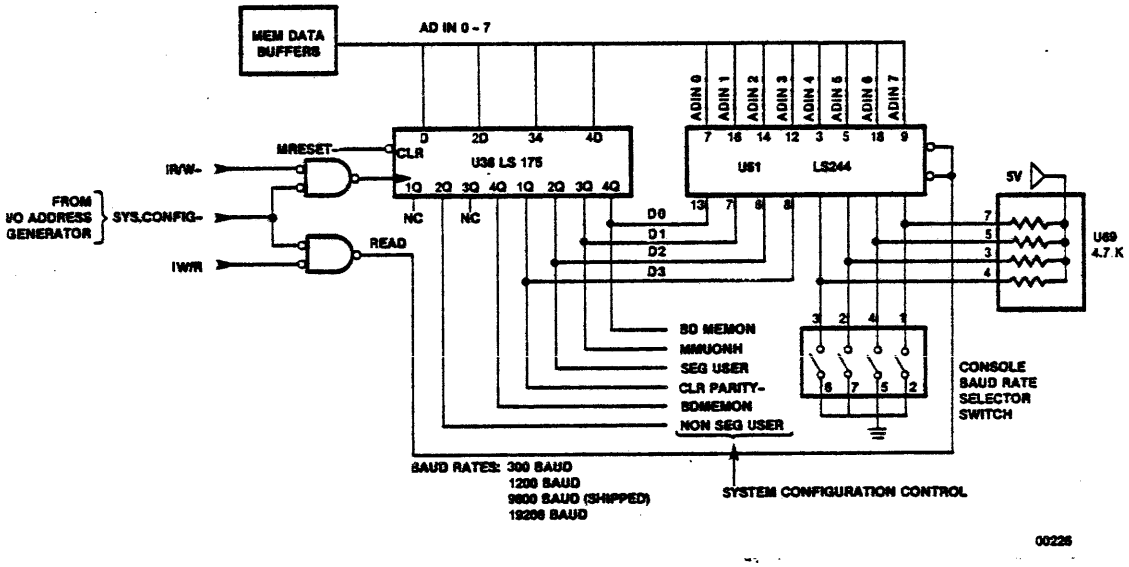


Figure 4-8 System Configuration Register (Sheet 14)

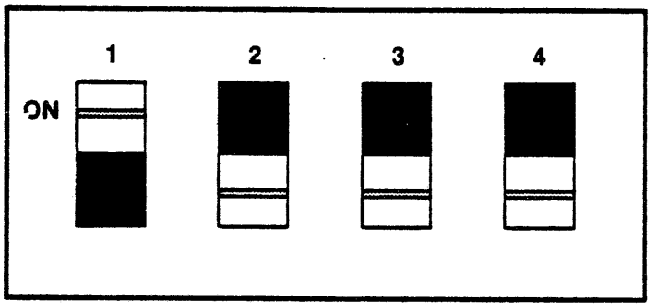


Figure 4-9 Setting Console Baud Rate (Table 2-9) (9600 Baud) for 8-inch Disk (Sheet 14)

4.9.1. SCR Configuration: The lower data bits D0 through D3 are read/write and enable the system configuration functions. All bits in the lower nibble are cleared on system reset to initialize the system. The D1 (MMU-ONH) and D2 (SEG USER) bits enable the MMUs and select segmented and non-segmented user respectively. The D0 (BDMEMON-) bit enables the onboard memory function at system reset (logic 0) and main memory on logic 1. On system reset, the D1 bit disables the three MMUs (logic 0) and all references to main memory are transmitted as logical addresses. Writing a logic 1 to the D1 bit enables all three MMUs for address translation and all main memory references are mapped through the MMUs. Bit D3 (CLR PARITY-) enables or disables the NMI derived from a parity error or a non-correctable double bit error from the ECC Controller.

4.9.2. Segmented/Non-segmented User: The operating system software configures the system configuration register(SCR) for segmented/non-segmented user. The SCR register (U36) outputs the configuration bit D2 (SEG USER) to enable the segmented user function. The D2 bit is cleared at RESET to a logic 0, for non-segmented user, and must be set to logic 1 (SEG USER) before the operating system can support a segmented user.

When the SCR D2 (SEG USER) bit is logic 0, the user process can occupy any one of the segments 2 through 63. The user code references are routed through the MMU M1. Data references are routed through the data MMU M2 if address offset is less than the normal break register and to the status MMU M3 if address offset is equal to or greater than the normal

break register.

4.9.3. Parity Error Checking: The SCR data bit (D3) CLR PARITY- enables or disables an NMI that results from a parity error or an noncorrectable double bit error from the ECC Controller. The D3 bit is reset to logic 0 on system RESET to disable an NMI that results from either of the above errors.

Once a parity or noncorrectable error is received by the board, it is latched by the parity error flip-flop (U14,sheet 4). When the flip-flop has been enabled at Pin 4 by the setting of D3 of the SCR to logic 1, on receiving a parity or ECC error, an onboard NMI is forced on the CPU through the NMI logic (U54,U8) and the board and panel error indicators are illuminated.

During an NMI acknowledge cycle generated by the CPU (status code 0101), the four-bit error buffer (U12,sheet 10) is enabled placing on the address/data lines (AD0-AD3) the the four-bit ECC ERROR NMI identifier (0010). The flip-flop (U14) is cleared by writing a logic 0 to the D3 bit of the SCR, followed by a logic 1 if future errors are to be allowed to cause an NMI.

4.10. Special Logic Circuits

4.10.1. External Violation Registers: The addressable registers U66 (sheet 2) and U48, U49, and U50 (sheet 3) record the low order 8 address bits of the current memory cycle, the low order 8 address bits of the preceeding IFETCH1 cycle instruction address, and the 7-bit segment number on a segment trap violation. Upon the MMU receiving a write violation, the port address FFD9 selects the segment violation register (U66). The port address FFF1 selects the low byte of the current memory cycle in register (U49). The port address FFF9 selects the low byte of previous instruction fetch in register (U50).

4.10.2. Address/Data Buffers and Steering Logic: When the CPU is the bus master, the addressing of memory or the I/O of data on the ZBI bus is controlled by the clock timing and the bus address/data steering logic (sheet 13) on the board. The steering logic internal address strobe (IAS-) and delayed clock (U13) combined with MMUONH enable the ZBI bus address buffers (U110,U114,U115, U116,U117).

For a translated physical address (TRAD 8-23) from the MMUs, the bus address buffers (U114,U117) are enabled and output AD8-AD23 to the ZBI. The low order byte (LAD 0-7) from address buffer(U110) is placed on the ZBI (AD0-AD7) .

For a nontranslated address of main memory, the logical address (LAD 8-15) and segment (ISNAD0-6) are directed to address buffers (U115,U116) and placed on the ZBI (AD8-23). The offset low order byte (LAD 0-7) is gated at the same time.

The address buffers are disabled and data buffers enabled during the offboard write or read data cycle. The bidirectional data buffers (U111,U113) (sheet 13) are controlled by the Write/Read and data strobe signals (IW/R-, IDS, and IDS-) and the bus acknowledge signal (Z BUS ACK-). For a write data cycle, IW/R- is high and IDS- is low at the gate U15 setting the write on the data buffers. The IDS high signal gates U21, U31,and enables a write to the ZBI.

For a data word read, IW/R- and IDS- are both low at U15 and the resulting high is inverted and sets the read input of both data buffers. The data strobe (IDS) strobes the 16-bit data word.

For a byte read of an even address, the byte swap buffer(U112) is enabled from the byte swap logic on the low byte by LAD0. The ENABLE BYTE SWAP signal generated is gated (U31) with the READ DATA STROBE from U15 to enable the byte swap buffer. The ENABLE BYTE SWAP- low signal disables U111 and U113 and the low byte from the ZBI becomes the high byte (IAD8-15) on the CPU data bus.

4.10.3. T2, T3 Wait State Generator Logic: On bootstrapping the system, references to local memory require an automatic one wait state insertion. This wait state is provided by U28 (sheet 14). The T2 WAIT- is activated for one CPU clock cycle during T2 clock period.

When necessary, the WAIT line is called upon to extend a transaction for I/O or memory if the device (or memory) is not ready or fast enough to keep up with the processor. If BUS WAIT is active in the middle of the T3 clock cycle, an additional wait state T3 is generated. This wait is supplied by the flip-flop (U97) (Figure 4-9) which inserts an additional clock period by holding the CPU clock at a high level for one clock cycle, (TW).

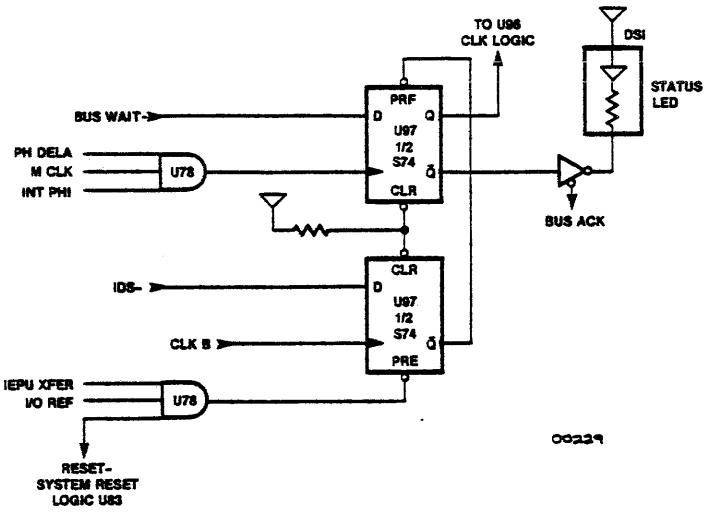


Figure 4-10 T3 Wait State Generator Logic (Sheet 11)

4.10.4. Peripheral Handshaking Logic: The Z80B Peripherals (PIO,SIOs,and CTCs) require the peripheral handshaking logic (Figure 4-10) for the Z8001A CPU to emulate the Z80B control signals IORQ-,M1-, and RD-. The two LS138 decoders (U24, U39,sheet12) are enabled by the decoded status signal I/O REF and decode the latched I/O address while generating chip enable (CE-) signals to the individual peripheral devices.

A write operation into the enabled peripheral is performed when IORQ- is low while RD- is high. A read operation is performed when both IORQ- and RD- are low. The peripheral interrupt of the CPU is by a vectored interrupt (VI) pulling the VI- input of the CPU low. The CPU samples this input at a specified time prior to the end of any instruction. The Z8001A CPU then acknowledges the interrupt with the specific status code (VIACK-) from the status logic (U25,sheet 3). The VIACK- signal is input at U41 and makes IORQ- active during an M1- (normally opcode fetch) cycle indicating a vectored interrupt acknowledge to the peripheral.

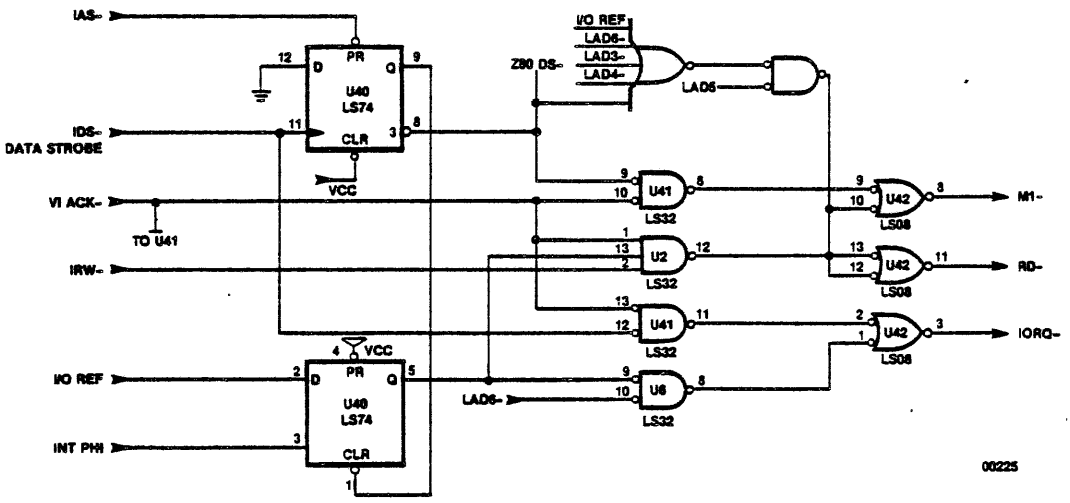


Figure 4-11 Peripheral Handshaking Logic (Sheet 12)

4.10.5. Segment Trap Logic and Suppress: During address translation , the MMU puts the translated physical memory location on its address lines and checks for two types of trap conditions, access violation and write warning. The two control signals that are used by the MMU to indicate access violation are the outputs SEGMENT TRAP (SEGT-) and SUPPRESS (SUP-). A SEGMENT TRAP request is generated upon the first detected occurrance of an access violation or write warning. The SEGT- output remains set (low) until a trap acknowledge signal is received from the CPU.

For an access violation, the MMU also activates SUP-. The SUP- output is used to inhibit memory writes and to request special data be returned on a read access. When the violation occurs, SUP- is asserted for that cycle and all subsequent CPU memory references until the end of the instruction. SUP- prevents data strobe (SYSDS) at U4 (sheet 14) thereby suppressing the data signal to memory.

The Z8001A CPU services a segment trap by entering a segment trap acknowledge cycle. The acknowledge cycle is preceded by a dummy instruction fetch cycle that the MMU ignores. During an acknowledge cycle, all enabled MMUs use the address data lines to indicate their status. An MMU that has generated a

segment trap request outputs a one on the Address/Data line associated with the number in its ID field. An MMU that has not generated a segment trap outputs a zero on its associated A/D line. Following the acknowledge cycle, the CPU automatically pushes the program status words and program counter onto the system stack, and loads a new program status word and program counter from the program status area. The SEGMENT TRAP (SEGT-) line is reset during the segment trap acknowledge cycle, and no SUP- signal is generated during the stack push.

The CPU board provides hardware which generates SEGMENT TRAP (SEGT-) and SUP- signals when an access is made to system segments (0, 1, 64, 65) in normal mode. The violation is detected by U3, U17 and U23 (sheet 10). Flip-flop U20 (sheet 8) generates SEGT- signal upon a violation. The SEGT- line is reset when segment trap is acknowledged (SEGTACK- goes high). Similarily, the other half of U20 generates the SUP- signal.

SECTION 5
MAINTENANCE

5.1. General

The board level preventive maintenance consists of board inspection and checking for correct jumpering, switch settings, voltage inputs, and front panel indicator readings. The onboard system power up diagnostics (SPUD) test the primary functions of the CPU and peripherals and test the system's ability to execute a limited number of instructions and communicate with the system peripherals. The selection of the primary boot device is by the four-pole switch U70 and is given in Table 2-9. The corrective maintenance for the CPU board is primarily by board replacement.

5.2. Preventive Maintenance

Preventive maintenance consists of routine inspection and cleaning procedures. These can be performed at the same interval as the processor and System 8000 inspections. Whenever it is necessary to remove the board from the card cage, inspect the board for signs of excess heat or dirty pin connectors.

5.3. Corrective Maintenance

The SPUD routine is automatically performed at system power-up in response to the RESET and START control functions. SPUD tests the primary functions of the CPU and exists in the onboard EPROM. The test functions are listed in Table 5-1. If a peripheral device is the primary boot device, as determined by switch U70, it will always be listed and tested and will be the first device on the list. Console operation from the serial channel 1 (SIO 0) I/O of the CPU board is necessary for the diagnostic routines to be used. If a problem exists in bootstrapping the system or console does not indicate "POWER-UP DIAGNOSTICS COMPLETE", check the console for recorded errors. "COMPLETE" indicates the completion of SPUD.

5.3.1. System Power-up Diagnostics:

1. System 8000 Instruction Test -- Specified System 8000 instructions are tested.

2. MMU -- All accessable internal registers and the segment trap functions are tested.

3. Memory Test -- All locations of memory are tested for read and write functions.

4. ECC Test -- The error detection capabilities of the system are tested.

5. Peripheral Equipment Test -- A cursory check of the System 8000 disk, tape, and storage module controller boards.

If the SPUD detects a problem, an error message is displayed on the console of the System Administrator (ZEUS superuser). The error messages and descriptions are listed in Table 5-1. If an error message is displayed, powerdown the system and verify that the cable connectors and PC boards are properly inserted. If the error message remains and more information is needed to isolate the problem, refer to the SADIE diagnostics in the System 8000 Hardware Reference Manual. When the problem is isolated to the CPU board, power down and replace the board. Return the defective board to the factory for repair.

NOTE

ZEUS is installed on disk at the factory. If SPUD runs correctly, pressing START also activates the automatic ZEUS boot-up procedures.

Table 5-1. SPUD Diagnostic Error List

ERROR #	P1	P2	P3	P4	CHRS * PRINTED	DESCRIPTION
0000	—	—	—	—	P	No External Memory**
0001	SEG #	ADDR	RD	—	O	Seg. Addr Fault **
0100	SEG #	ADDR	TD	RD	W	Mem. Addr Fault
0101	SEG #	ADDR	TD	RD		Data Line Fault
0102	SEG #	ADDR	TD	RD		'As' Data Fault
0103	SEG #	ADDR	TD	RD		'5s' Data Fault
0104	—	—	—	—		No Good Segments Above Zero**
0100	SEG #	ADDR	TD	RD	E	Segment Zero Memory Test
0101	SEG #	ADDR	TD	RD		(Descriptions As Above)
0102	SEG #	ADDR	TD	RD		
0103	SEG #	ADDR	TD	RD		
0200					R (sp)	ECC Single-bit Correction Failure
0201					U	ECC two-bit trap failure
0202					P (sp)	ECC two-bit error not reported
0203	SEG #	ADDR				ECC Check Byte RAM error
0300	MMU	SDR	TD	RD	D	MMU's Not Individually Addressable
	PORT #	FIELD #				
0301	MMU	SDR	TD	RD		SAR or DSCR Indexing Fault
	PORT #	FIELD #				
0302	MMU	SDR	TD	RD		SDR 'As' or '5s' Data Fault
	PORT #	FIELD #				
0303	MMU	TD	RD	—		MMU Control Register 'As' or '5s' Fault
	CMD #					
0304	REG #	TD	RD	—		System/Normal Break Register 'As' or '5s' Fault
0305	MMU ID #	SDR #	VDAT	—	I	Stack MMU Did Not Trap On Limit Test
0305					A	Unexpected Trap
0305					G	Unexpected Trap
0305					N	Data MMU Did Not Trap On Limit Test
0305					O	Stack MMU Did Not Trap On Read-Only Test
0305					S	Data MMU Did Not Trap On Read-Only Test
0306	MMU Port #	SDR #	TD	RD	T	Translation Fault On Data MMU
0307	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0308	MMU PORT #	SDR #	TD	RD	I	Translation Fault On Stack MMU
0309	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0310	MMU PORT #	SDR #	TD	RD	C	Translation Fault On Code MMU
0311	MMU PORT #	SDR #	VDAT	—		Unexpected Trap
0312	MMU PORT #	SDR #	—	—	S (sp)	No Trap On Code MMU Limit Test

Table 5-1. SPUD Diagnostic Error List (Continued)

ERROR #	P1	P2	P3	P4	CHRS * PRINTED	DESCRIPTION
1000	—	—	—	—		No WDC Board In System
1001	DS1	DS2	DS3	DS4		Self-Test Error
2000	—	—	—	—		No TCC Board In System
2001	—	—	—	—		Busy Bit Always Set***
2002	REG #	TD	RD	—		'5s' Data Fault
2003	REG #	TD	RD	—		'As' Data Fault
2004	IV REG	STATO REG	MIC REG	—		TCC Self-Test Error***
2005	IV REG	STATO REG	MIC REG	—		TCC Hardware Error***
3000						MDC Not Responding
3001	ADDR	—	—	—		RAM Error (P1 holds location)
3002						PROM Checksum Error
3003						Time Out Condition
3004						Read ABORT Error
3005						Wait ABORT Error
3006						Parity Error
3007						Not Used But Reserved
3008						Seek Not Complete Error
3009						Cylinder Not Found
3010						Drive Not Selected
3011						Head/Secter Not Found
3012						Invalid Command
3013						No Track 0 Found
3014						Drive Not Ready
3015						Bad Interrupt
3016						Bad MAP
3017						Illegal Cylinder Selected
3018						BEP Error
4000						SMC Not Responding
4001						SMC Initialization Error
4002						SMC RAM Error
4003	STATUS	—	—	—		SMC Self Test Timed Out Host Waiting (P1 holds SMC status register)
4004						Drive 0 Not Selected
4005						Drive 0 Not Ready
4006						Drive 0 Not On Cylinder
4007						Drive 0 Read Only
4008						Drive 0 Drive Fault
4009						Drive 0 Seek Error
4010						Drive 0 Not Formatted (Can't Size Disk)
COMPLETE						Last Characters of SPUD Message

Table 5-1. SPUD Diagnostic Error List (Continued)

* – Characters of SPUD message printed before entering test

** – Fatal error preventing further memory-related tests from being run

*** – The TCU test may take up to two minutes if the drive is busy or if the 'busy' status bit is stuck. The last two TCU error messages dump out the contents of the status registers for troubleshooting.

Pn – Test parameters of error printed (in hexadecimal):

SEG #	–	segment number
ADDR	–	address offset
TD	–	test data
RD	–	returned data
MMU PORT #	–	full work port number of MMU under test
MMU CMD #	–	MMU port number with command 'ored' in
SDR FIELD #	–	indicates a particular SDR in the range 0-255
MMU ID #	–	ID of MMU(s) returned from a segment trap
	–	1 = code MMU
	–	2 = data MMU
	–	4 = stack MMU
SDR #	–	logical segment number or set of SDR's (0-63)
VDAT	–	violation data from a single MMU trapping
(HB)	–	bus cycle status register data
(LB)	–	violation type register data
DS1	–	WDC detailed status - disk ready register
DS2	–	- disk status register
DS3	–	- operation error status
DS4	–	- self-test error status
REG #	–	register port number of unit under test
—	–	no parameter printed
STATUS	–	SMC status port contents

When the diagnostics are complete, the maximum available segment number will be displayed as follows (xx in hexadecimal):

```
POWER UP DIAGNOSTICS
ACTIVE PERIPHERALS:
    WDC
    TCC
    MDC
    SMC
COMPLETE
MAXSEG = <xx>
```

5.3.2. Inspection and Replacement: Inspection or replacement of the System 8000 CPU board is accomplished by the following procedure:

1. Remove the front panel by pulling toward the front of the unit.

2. Loosen knurled fasteners that secure top cover and slide it back from guideposts. For Model 10/11 six screws secure cover.

3. Inspect each board in card cage ensuring that it is properly seated in the appropriate backplane connector.

4. Locate test points 1 through 11 at the front edge of the CPU Board when viewed from the front of the card cage.

5. Test for required signal and voltages at each of these test points.

6. Locate power supply DC output test points on the right front corner of the backplane next to the card cage.

7. Check for the following DC voltages at their respective test points. Adjustment, if necessary, of the +5 Vdc can be made on the CPU module power supply and is labeled either V. ADJ or +5V ADJ. For the Model 10/11, refer to the voltage Adjustment procedure in the Model 10/11 Hardware Reference Manual.

   TEST EQUIPMENT REQUIRED: HP3466A Multimeter or equivalent

   a. +5 Vdc /(+- .05Vdc at TP2) (TP4 on Model 10/11)

   b. -5 Vdc /(+- .05Vdc at TP5) (TP2 on Model 10/11)

   c. +12 Vdc/(+- .05Vdc at TP3) (TP1 on Model 10/11)

8. If trouble is not found, replace the CPU board.

SECTION 6
TIMING

6.1. General

The System 8000 CPU, through the Z8001A microprocessor, executes instructions by stepping through sequences of basic machine cycles, memory read or write, I/O device read or write, interrupt and segment trap request acknowledge, and internal execution. Each of these basic cycles requires three to ten clock cycles to execute. Instructions that require more than ten clock cycles are divided into several machine cycles. No machine cycle is longer than ten clock cycles which provides a fast response to a Bus Request.

The following timing diagrams show the relative timing relationships of all the Z8001A CPU signals during each of the basic operations. When a machine cycle requires additional clock cycles for CPU internal operation, one to five clock cycles are added. Memory and I/O read and write, as well as the interrupt acknowledge cycles, are extended by activating the WAIT- input. For exact timing information, refer to the Memory Read and Write timing diagram.

The WAIT- input is asynchronous and the setup and hold times for WAIT- relative to the clock must be met. The asynchronous WAIT- signals generated, are synchronized with the CPU clock before transmission to the CPU.

6.2. Memory Read and Write

Memory read and instruction fetch cycles are identical, except for the status information on the ST0 - ST3 outputs. During a memory read cycle, the segment number is output one clock cycle earlier than the 16-bit address offset to compensate for a delay in the memory management circuitry. The MMUs on memory access violation provide SEGT- trap request input to the CPU that results in Segment Trap Acknowledge on the status outputs and the Segment Trap Acknowledge Cycle.

A valid address is indicated by the rising edge of the address strobe. Status and mode information become valid early in the memory access cycle and remain stable throughout.

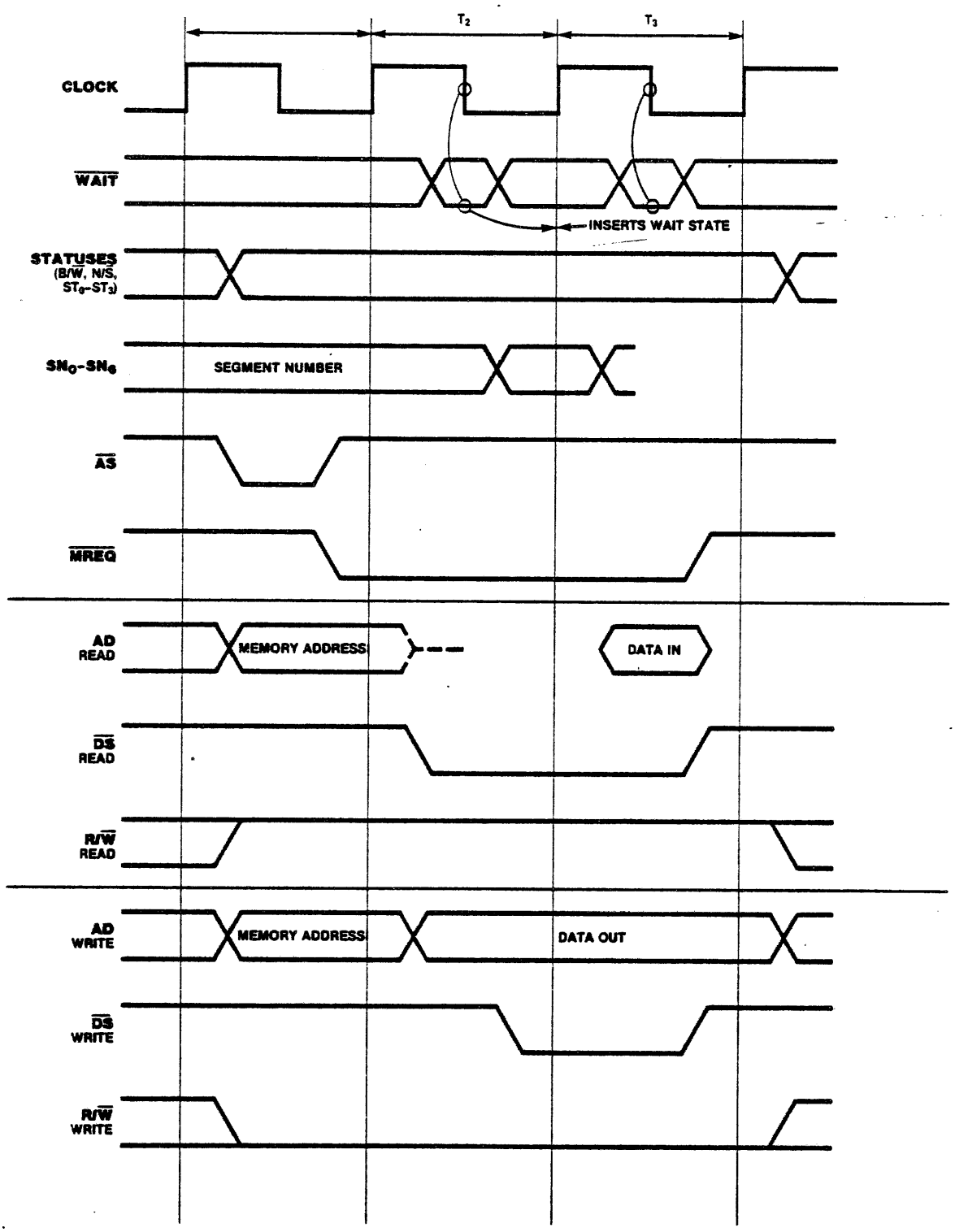


Figure 6-1 Memory Read and Write Timing

The state of the WAIT- input is sampled in the middle of the second clock cycle by the falling edge of the CLOCK. If WAIT- is low, an additional clock period is added between T2 and T3. WAIT- is sampled again in the middle of this wait cycle, and additional wait states can be inserted. In addition, the CPU board has hardware (T3 WAIT) that allows WAIT- to be sampled at the falling edge of the T3 clock cycle and extends the read/write cycle an extra clock period. Control outputs do not change during wait states.

Although main memory is double word organized, it is addressed as bytes. All instructions are word aligned, using even addresses. Within a 16-bit word, the most significant byte (D8-D15) is addressed by the low order address (A0 = Low), and the least significant byte (D0 - D7) is addressed by the high-order address (A0 = High).

6.3. Input/Output Timing

I/O timing is similar to the memory read/write timing, except that one wait state is automatically inserted between T2 and T3. A Z80 peripheral handshaking control translation circuit causes the Z8001A CPU to emulate the Z80B control signals IORQ-, M1-, RD-, and RETI.

Four different operations are performed between the CPU and its peripherals:

1. CPU writing into the peripheral device.

2. CPU reading from the peripheral device.

3. Peripheral interrupting the CPU, which responds with an Interrupt Acknowledge.

4. CPU simulating a Return from Interrupt (RETI) signal.

The first two operations - writing or reading from the peripheral - are fairly straight forward. Two three-to-eight LS138 decoders, enabled by the decoded status signal I/O REF-, decodes the latched I/O addresses and generates CE- signals to the CTC 0-2, SIO 0-3, and PIO individual peripheral devices. The Z8001A uses the full 16-bit address space for I/O. All ports require an odd address to interface with the data bus (lower byte).

Writing to the enabled peripheral is performed when IORQ- is low while RD- is high. A read operation is performed when IORQ- is low while RD- is low.

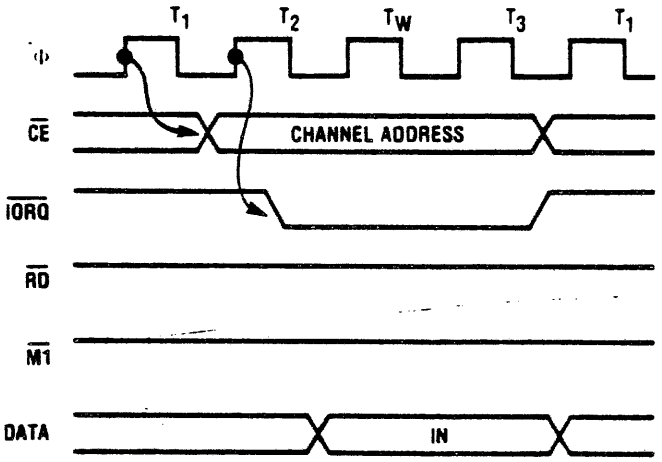


Figure 6-2 Write Cycle

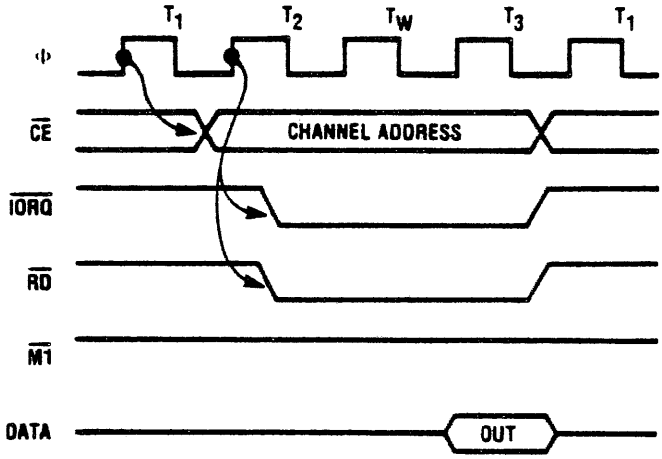


Figure 6-3 Read Cycle

6.4. Interrupt Operation

The Z8001 CPU recognizes the vectored, non-maskable, and segment trap interrupt inputs which are sampled at the beginning of T3 in the last machine cycle of any instruction. In response to the interrupt or trap, the subsequent status output instruction fetch cycle is exercised but aborted. The next machine cycle is the interrupt or segment trap acknowledge cycle. This cycle has five automatic wait states, with additional wait states possible. After the last wait state, The CPU reads the information on AD0 - AD15 which identifies the source of the interrupt or trap. After the acknowledge cycle, the N/S output indicates the automatic change to system mode.

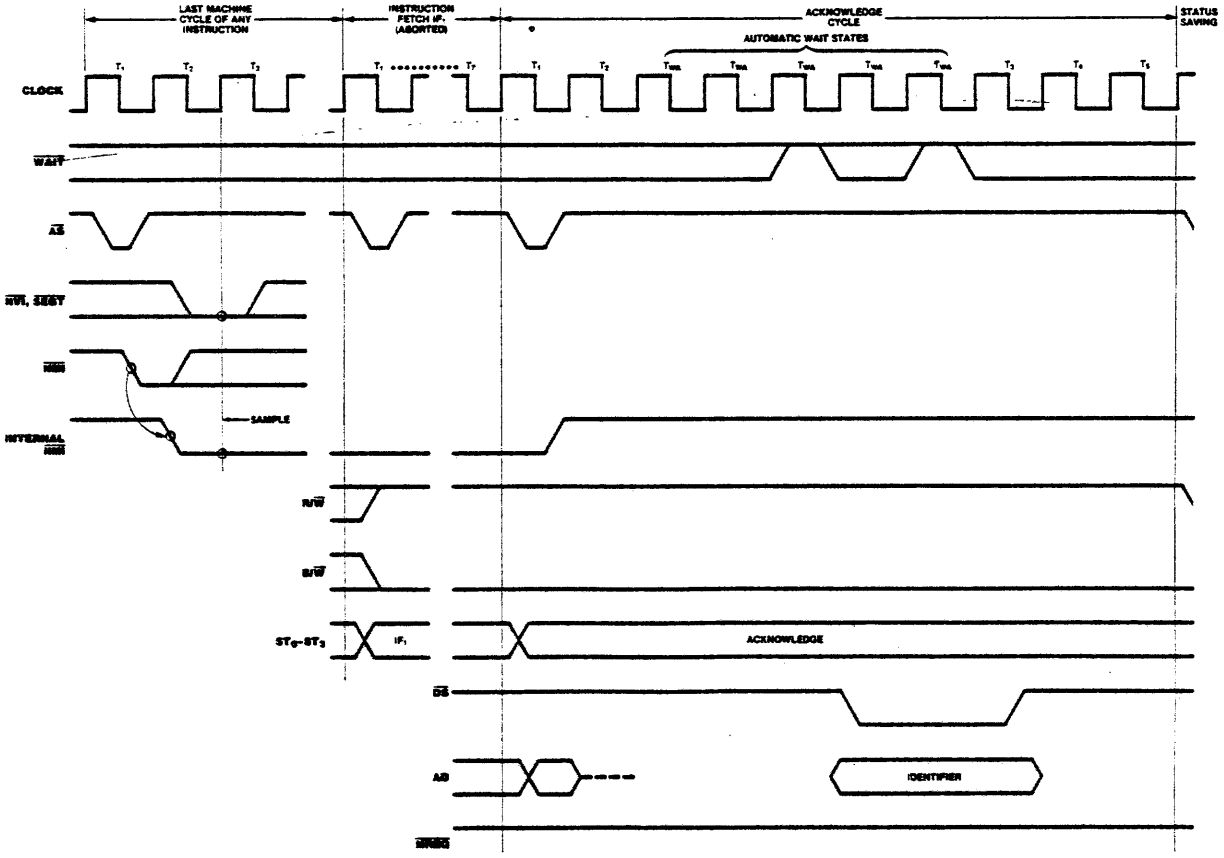


Figure 6-4 Segment Trap/Interrupt Acknowledge Cycle

6.4.1. Status Saving Sequence: The machine cycles following the interrupt acknowledge or segment trap acknowledge cycle push the old status information on the system stack in the following order: the 16 bit program counter, the 7-bit segment number, the flag and control word, and finally the interrupt/trap identifier. Subsequent machine cycles fetch the new program status from the program status area, and then branch to the interrupt trap service routine.

6.4.2. Bus Request Acknowledge Timing: A low on the BUSREQ- input indicates to the CPU that another device is requesting the Address/Data and Control buses. The asynchronous BUSREQ- input is synchronized at the beginning of any machine cycle. If BUSREQ- is low, an internal synchronous BUSREQ- signal is generated, which afer completion of the current machine cycle , causes the BUSACK- output to go low and all bus outputs to go into the high impedance state. The requesting device can then control the bus. When BUSREQ- is released, it is synchronized with the rising clock edge and the BUSACK- output goes high one clock period later, indicating the CPU will again take control of the bus.

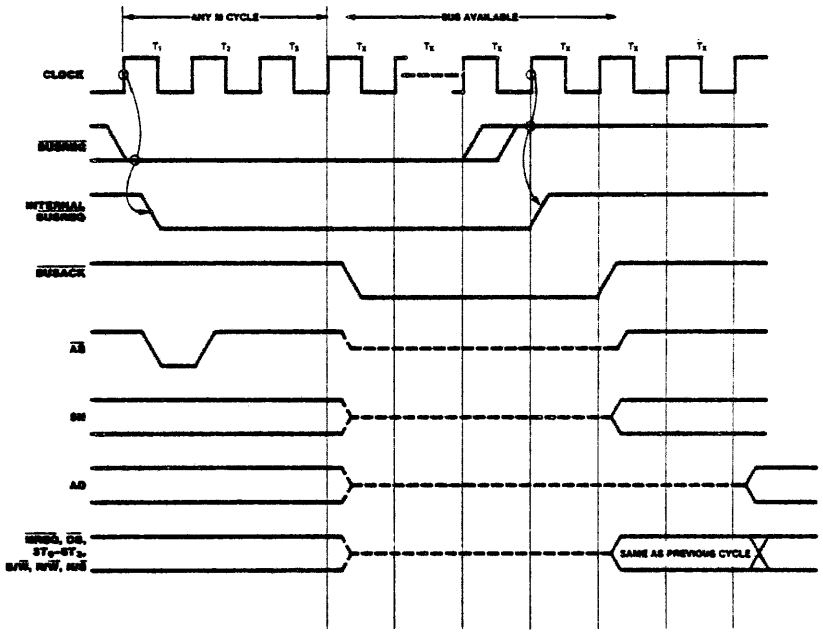


Figure 6-5 Bus Request Acknowledge Cycle

6.5. Peripheral Interrupt Timing

The peripheral interrupt requires handshaking logic and software to make the Z80B peripherals compatible with the Z8001A. The Z80B peripherals request a vectored interrupt by pulling the VI- input of the CPU low. The CPU samples this input at a specified time prior to the end of any instruction execution and acknowledges the interrupt with a specific status code VIACK-. The VIACK- input to the Z80 peripheral handshaking logic acknowledges interrupts by gating the combination of control signals IORQ- and M1- both active. Potential conflicts between overlapping interrupt requests are resolved with a daisy-chain arrangement between the IEO outputs and IEI inputs of the peripheral components.

The highest order peripheral has its IEI permanently tied high. For any peripheral that has no interrupt pending or under service, IEO = IEI. Any peripheral that has an interrupt pending or under service forces its IEO low.

To ensure stable conditions in the daisy-chain, all interrupt status signals are prevented from changing while M1- is low. When IORQ- is low, the highest priority interrupt requestor (IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

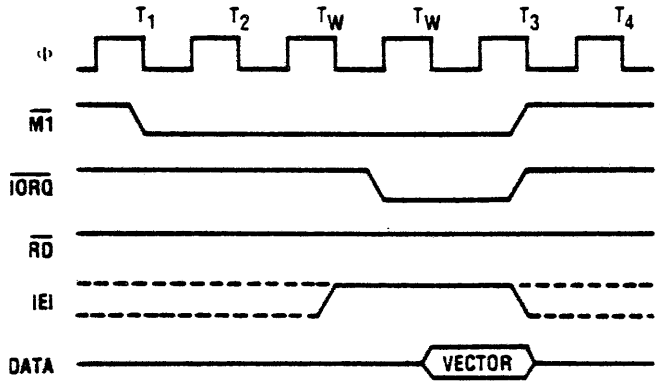


Figure 6-6 Interrupt Acknowledge Cycle

6.5.1. Return from Interrupt: At the end of an interrupt service routine, the interrupt- under- service latch in the peripheral must be reset. The normal daisy-chain operation can be used to detect an impending interrupt, however, it can not distinquish beween an interrupt under service and a pending unacknowledged interrupt of a higher priority. Whenever ED is decoded, the daisy-chain is modified by forcing high the IEO of any interrupt that has not yet been acknowledged. Thus, the daisy-chain identifies the device presently under service as the only one with an IEI high and a IEO low. If the next opcode byte is 4D, the interrupt-under-service latch is reset (Figure 6-7).

The Z8001A CPU emulates the instruction by a combination of hardware and software. A software sequence at the end of every interrupt service routine writes two consecutive bytes (ED and 4D), to a hardware FFE1 address which simulates the RETI.

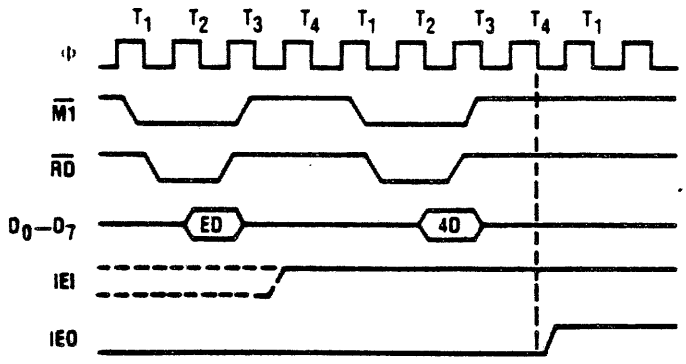


Figure 6-7 Return from Interrupt Cycle

APPENDIX A
16 KILOBYTE EPROM MEMORY

The CPU onboard memory (09-0288) has been increased in capacity by the substitute of four 2732 EPROMS for the previously used 2716 EPROMS. This change increases the EPROM capacity from 8 kilobytes to 16 kilobytes of resident EPROM for local read-only memory. The EPROM addressing is from 0 through 3FFF Hex. The 2 kilobytes of RAM read/write memory remains the same using four 2114 RAMS. However, the addressing of the RAM memory is from locations 4000 through 47FF Hex.

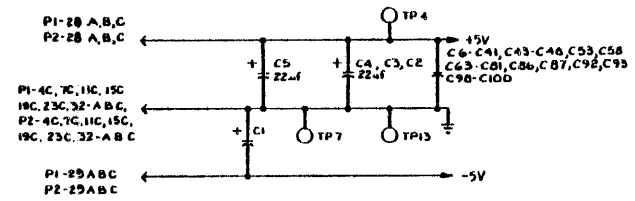
The main memory address begins at location 8000 Hex. When the local memory space is enabled, a dead space exists from locations 4800 through 7FFF Hex. As long as the board memory enable bit D0 of the SCR is reset (logic 1), the total local memory space 0 through 47FF Hex will overlay the segment 0 main memory space. On power-up or system reset, the SCR D0 bit is cleared to logic 0 and enables the local memory. Writing a logic 1 to bit D0 of the SCR disables onboard memory and maps all memory reference to offboard memory.

APPENDIX B
LOGIC DIAGRAMS

I.C. TYPE	+5V (PIN)	GND	-5V (PIN)	DESIGNATIONS	SPARE GATES
74S00	14	7		U6,9,17	U9-C,D; U6-B,D
74S02	14	7		U15	
74LS02	14	7		U18	U10-B
74S04	14	7		U1,29,95	U29-A
74LS04	14	7		U32,101,104,122, 127	U32-D
7407	14	7		U35	
74S08	14	7		U3,14	
74LS08	14	7		U38,42	
74S10	14	7		U2,23,30	U2-B
74S11	14	7		U78	
74LS11	14	7		U33	U33-C
74LS14	14	7		U81	
74S20	14	7		U7,31	U7-D
74LS21	14	7		U4,37	
74LS27	14	7		U54	
74S32	14	7		U21	
74LS32	14	7		U6,22,27,41	U8-C,D; U27-C,D
74S51	14	7		U16	
74S74	14	7		U5,13,97	
74LS74	14	7		U28,40	
74S85	16	8		U52,53	
74S113	14	7		U19,20,83	
74LS193	16	8		U45	
74LS138	16	8		U24,26,39,55	
74LS175	16	8		U36	

[3]

IC TYPE	+5V (PIN)	GND	-5V (PIN)	DESIGNATIONS	SPARE GATES
74S240	20	10		U11,60,109	
74S241	20	10		U91	
74LS244	20	10		U12,51,67,73,101, 108,110,112,114-116	
74LS245	20	10		U46,63,111,113	
74S260	14	7		U34	U34-A
74LS260	14	7		U61	U61-B
74S373	20	10		U47,62,71,72	
74LS374	20	10		U48,49,50,65,66	
26LS30	1	5	8	U100,102,105,124, 126,128	
26LS32	16	8		U104,107,120, 121,123,125	
93S16	16	8		U98	
2808-CTC	24	5		U43,44,89	
2114(p)-3	18	9		U51-60	
2900A CPU	11	36		U64	
2732	24	12		U76-77	
280 CLK DRV	1	5		U71,80	
2457.6 MHZ	14	7		U84	
4.4.444 MHZ	14	7		U85	
2400A PIO	11	35		U86,87,88	
2808-SIO/2	9	31		U90-93	
2808-PIO	26	11		U94	



REF DESIGNATION	
LAST USED	NOT USED
C100	—
CR1	—
DS4	—
R20	—
U128	—

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1KΩ, ¼ W, 5%
2. CAPACITOR VALUES ARE IN MICROFARADS.
[3] 3. ALPHANUMERIC DENOTES GATES.

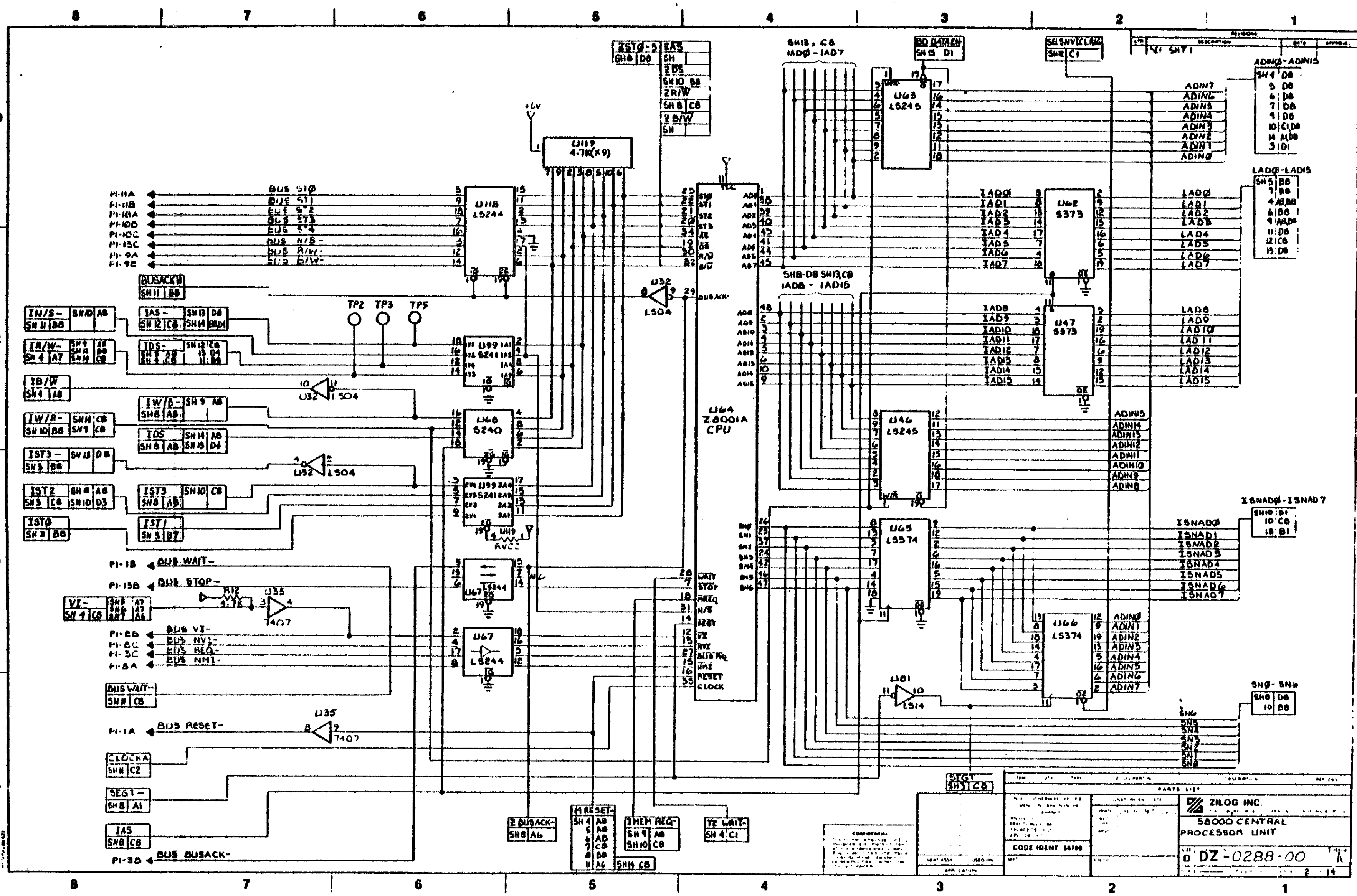
CONFIDENTIAL

ZILOG INC

SCHEMATIC S8000
CENTRAL PROCESSOR UNIT

CODE IDENT 56700

D DZ-C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Z8000 CENTRAL PROCESSOR UNIT
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Z8001A
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U62 S373
U47 S373
U46 LS245
U65 LS374
U66 LS374
U118 LS244
U68 S240
U67 LS244
ADINØ-ADIN15
LADØ-LAD15
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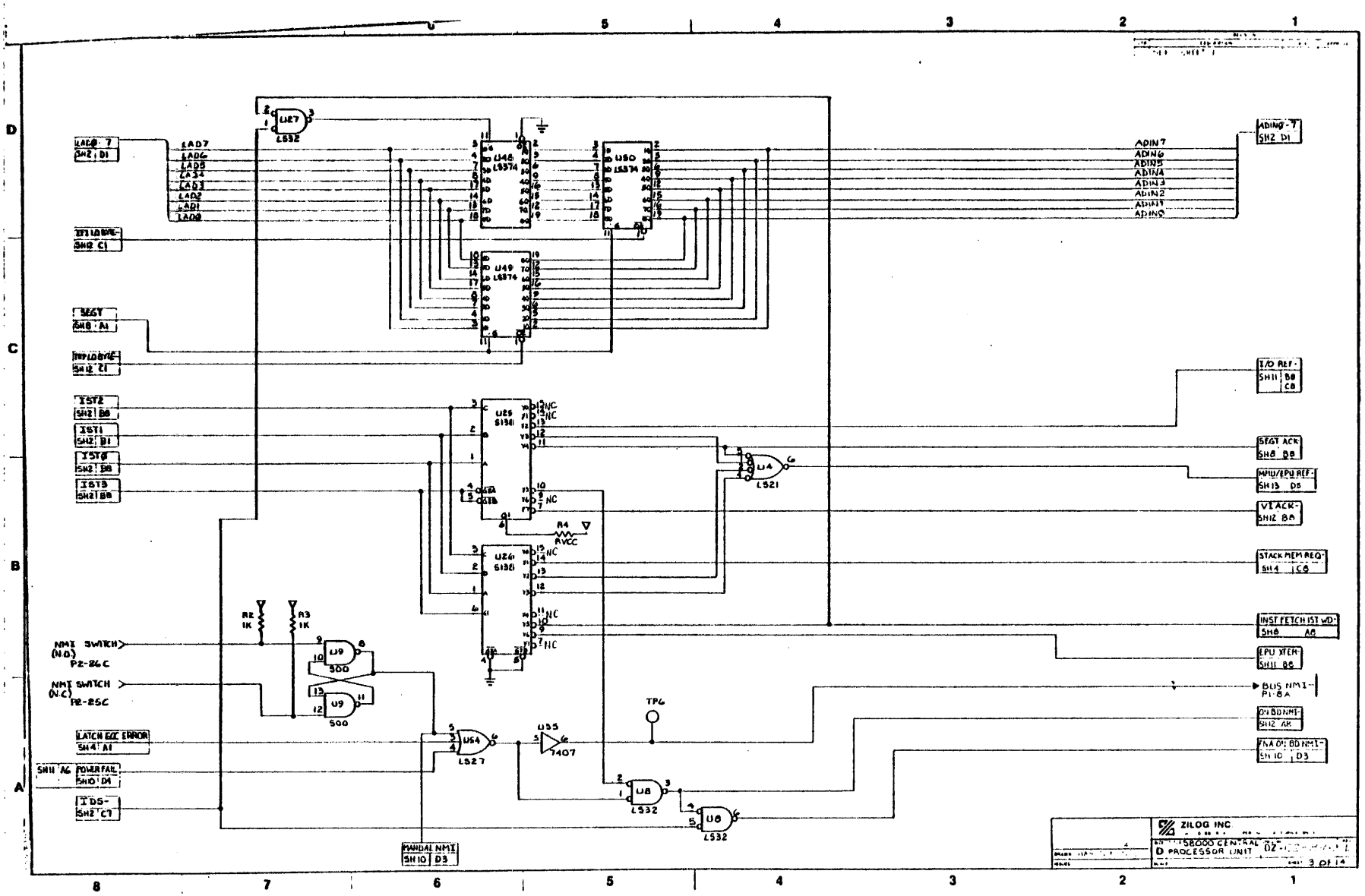
BUS STOP-
BUS RESET-
BUS BUSACK-
TP2
TP3
TP5


ZILOG INC
Z8000 CENTRAL
PROCESSOR UNIT
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LAD0-7
SH2 D1
LAD7
LAD6
LAD5
LAD4
LAD3
LAD2
LAD1
LAD0
ADIN7
ADIN6
ADIN5
ADIN4
ADIN3
ADIN2
ADIN1
ADIN0
ADIN0-7
SH2 D1
SEGT
SH8 A1
SH12 C1
ISTZ
SH2 B8
IST1
SH2 B1
IST0
SH2 B8
IST3
SH2 B8
U27
LS32
U46
LS374
U50
LS374
U49
LS374
U25
S138
U26
S138
U24
S138
U4
LS21
U9
S00
U9
S00
U54
LS27
U55
7407
U8
LS32
U8
LS32
R4
RVCC
R2
1K
R3
1K
TP6
NMI SWITCH (N.O) P2-26C
NMI SWITCH (N.C) P2-25C
LATCH ECC ERROR
SH4 A1
SH11 A6
POWERFAIL
SH10 D4
IDS-
SH2 C7
MANUAL NMI
SH10 D3
I/O REF-
SH11 B8 C8
SEGT ACK
SH8 B8
MMU/EPU REF-
SH13 D5
VI ACK-
SH12 B8
STACK MEM REQ-
SH4 C6
INST FETCH IST WD-
SH8 A6
EPU XFER
SH11 B5
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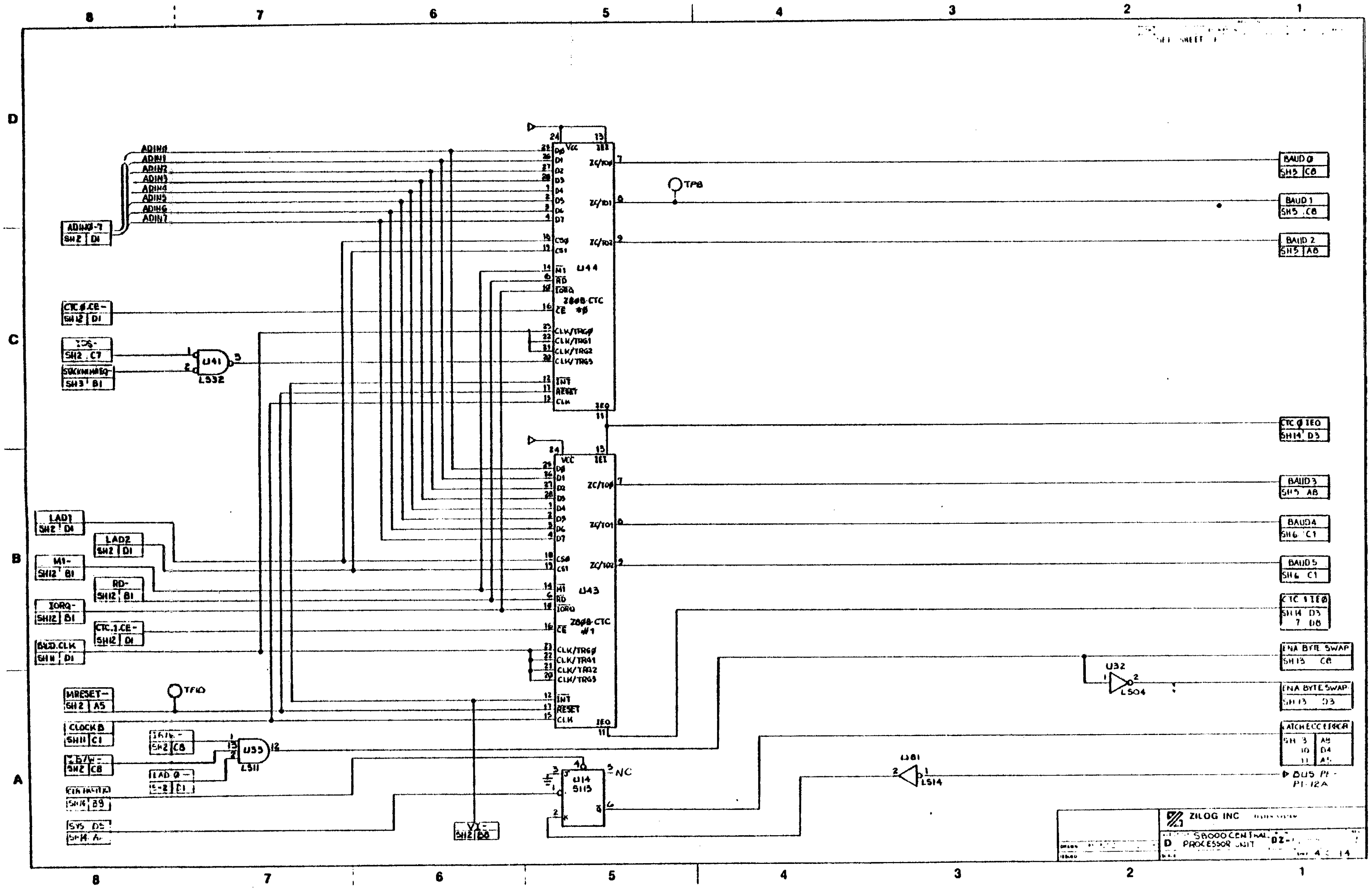
P1-8A
ON BD NMI-
SH2 A8
FNA ON BD NMI-
SH10 D3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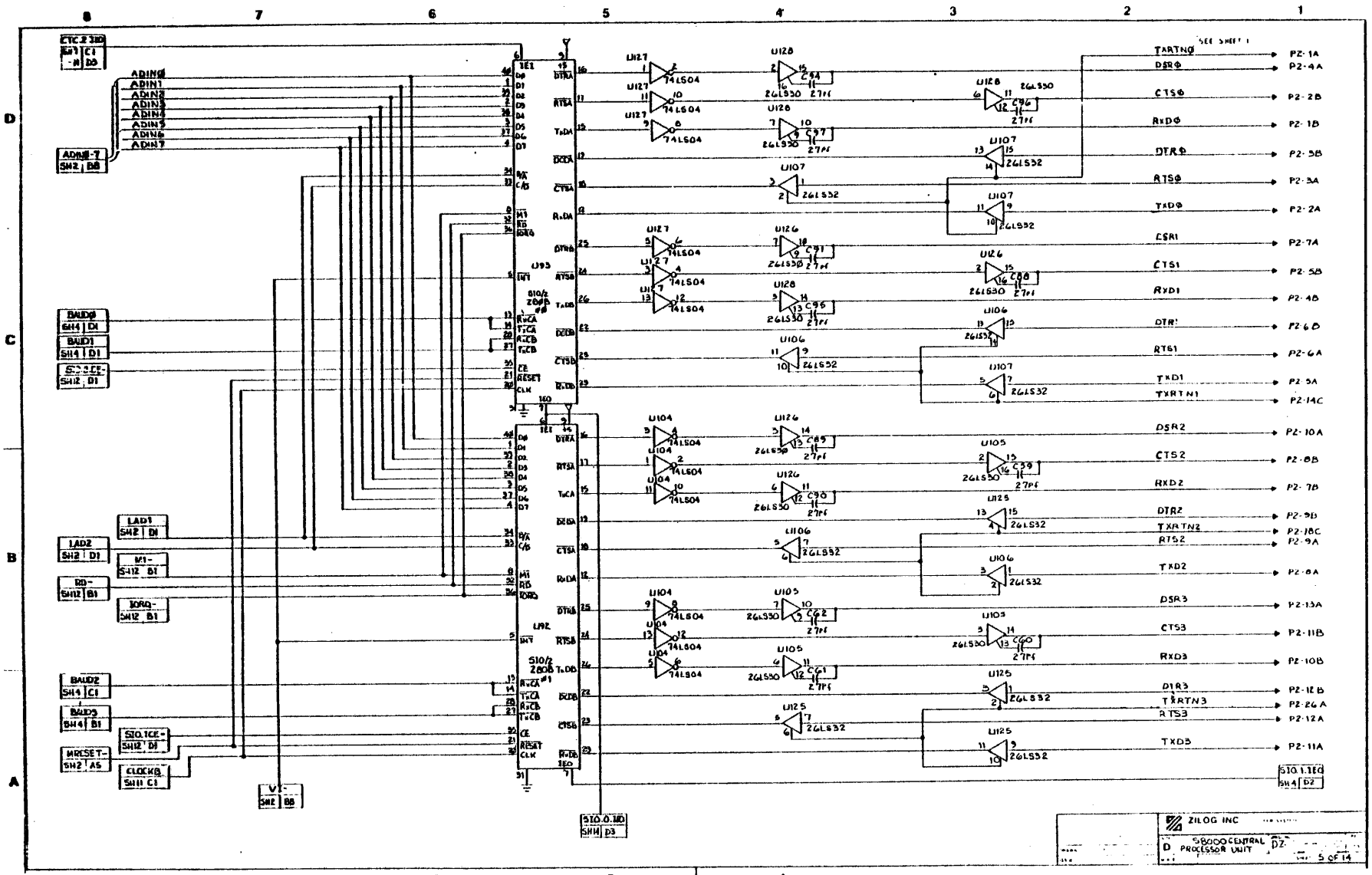
ADIN1
ADIN2
ADIN3
ADIN4
ADIN5
ADIN6
ADIN7
ADIN0-7 SH2 D1
CTC0.CE- SH12 D1
IOS- SH2 C7
U41
LS32
U44
Z80B-CTC #0
TP8
BAUD 0 SH5 C8
BAUD 1 SH5 C8
BAUD 2 SH5 A8
CTC 0 IEO SH14 D3
BAUD 3 SH5 A8
BAUD 4 SH6 C1
BAUD 5 SH6 C1
LAD1 SH2 D1
LAD2 SH2 D1
M1- SH12 B1
RD- SH12 B1
IORQ- SH12 B1
CTC.1.CE- SH12 D1
BAUD.CLK SH11 D1
U43
Z80B-CTC #1
ENA BYTE SWAP SH13 C8
U32
LS04
ENA BYTE SWAP SH13 D3
MRESET- SH2 A5
TP10
CLOCK B SH11 C1
U33
LS11
LAD 0 -
U14
S115
NC
U81
LS14
BUS PI-12A
LATCH ECC ERROR
SYS DS
ZILOG INC
S8000 CENTRAL PROCESSOR UNIT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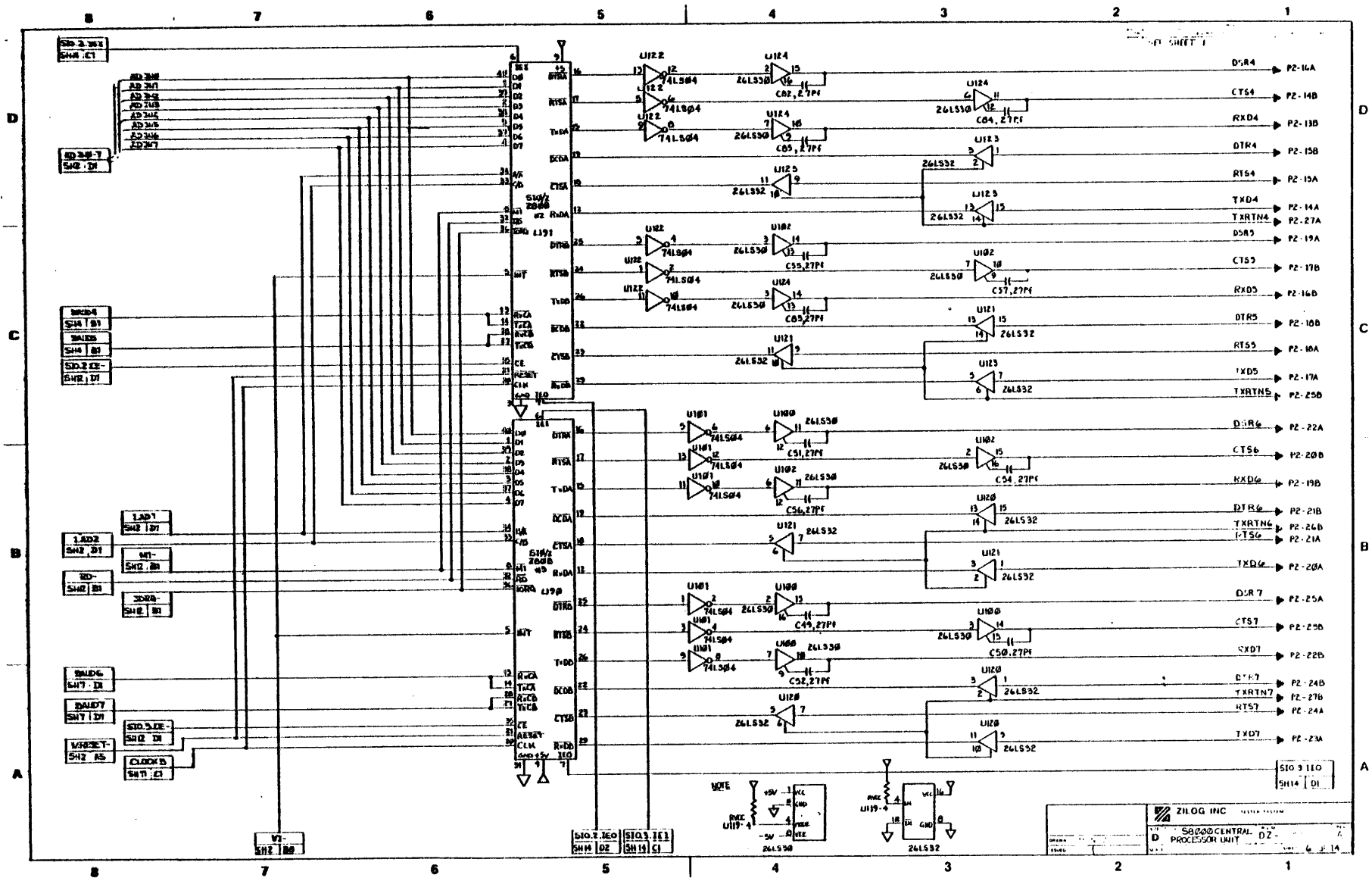
Z8000 CENTRAL PROCESSOR UNIT
D
DZ
5 OF 14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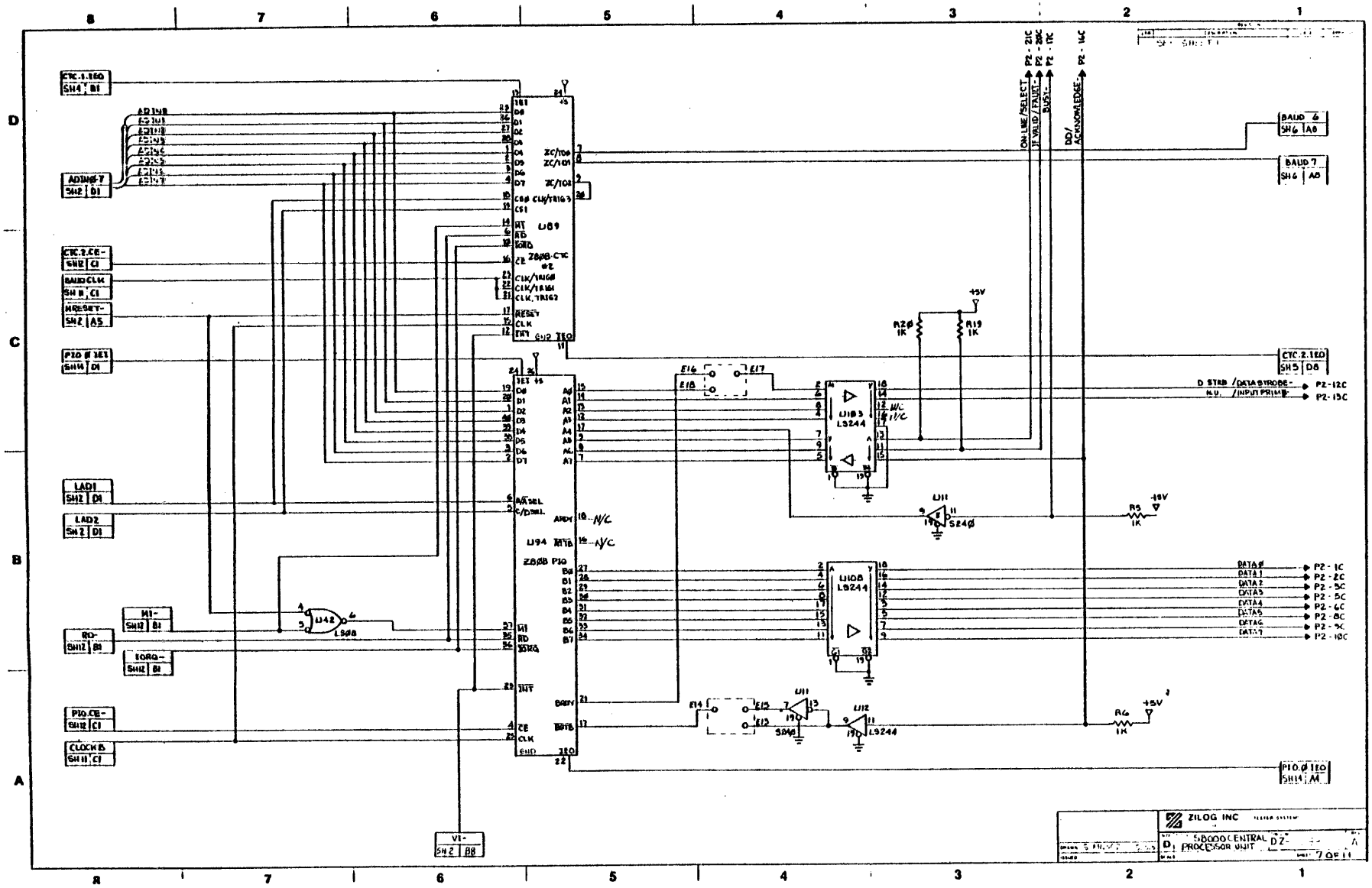
74LS04
26LS30
26LS32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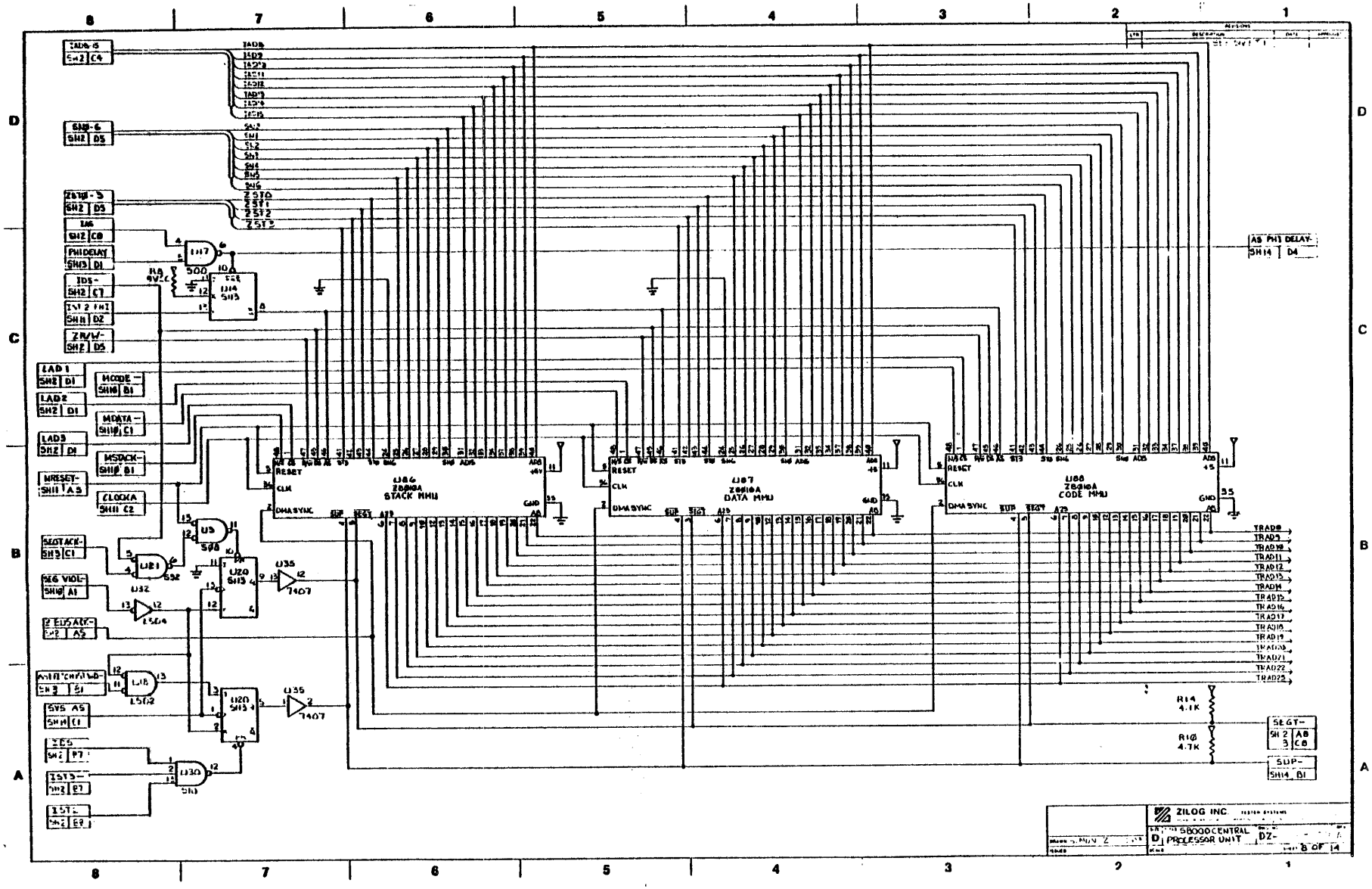
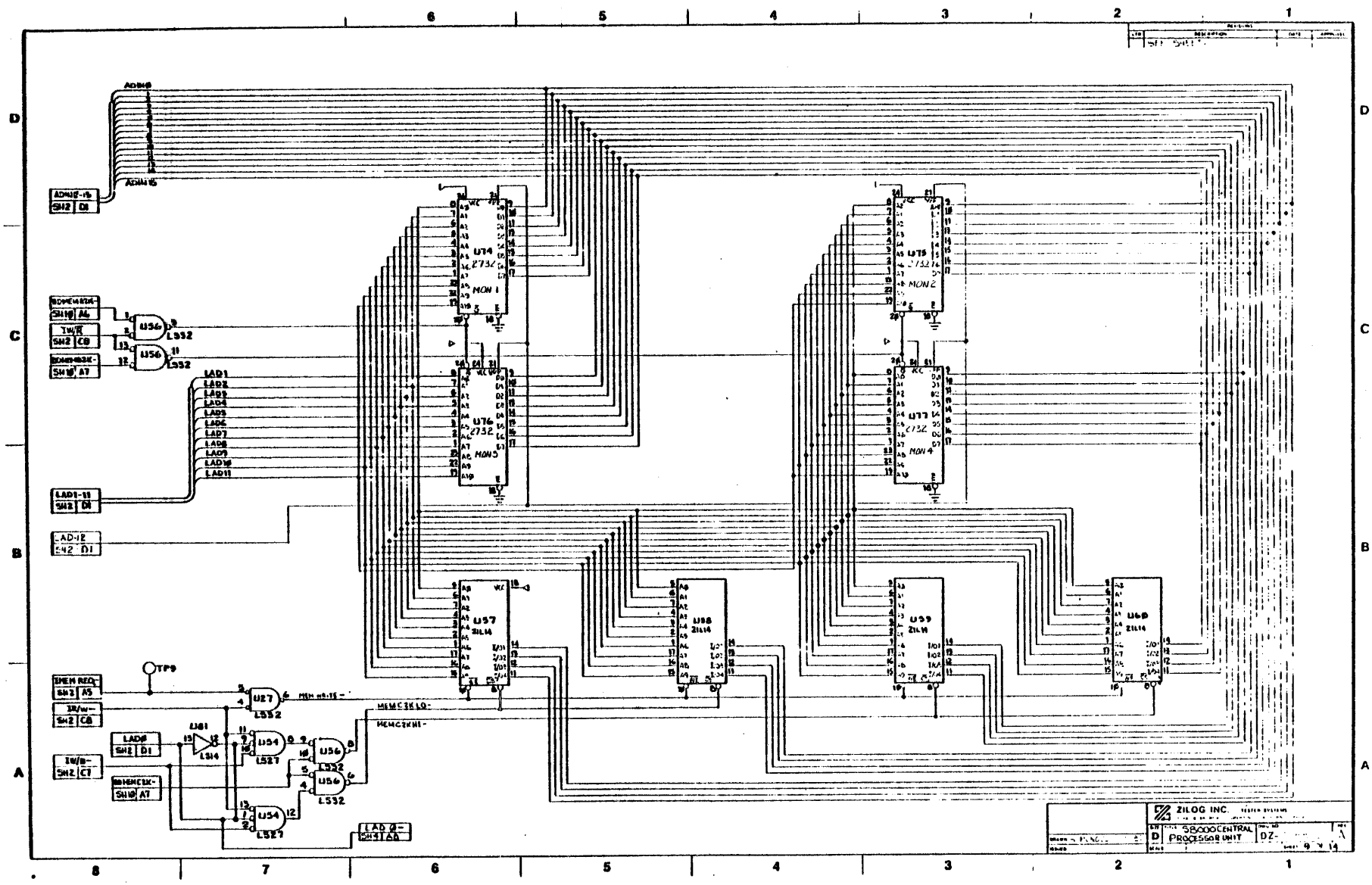
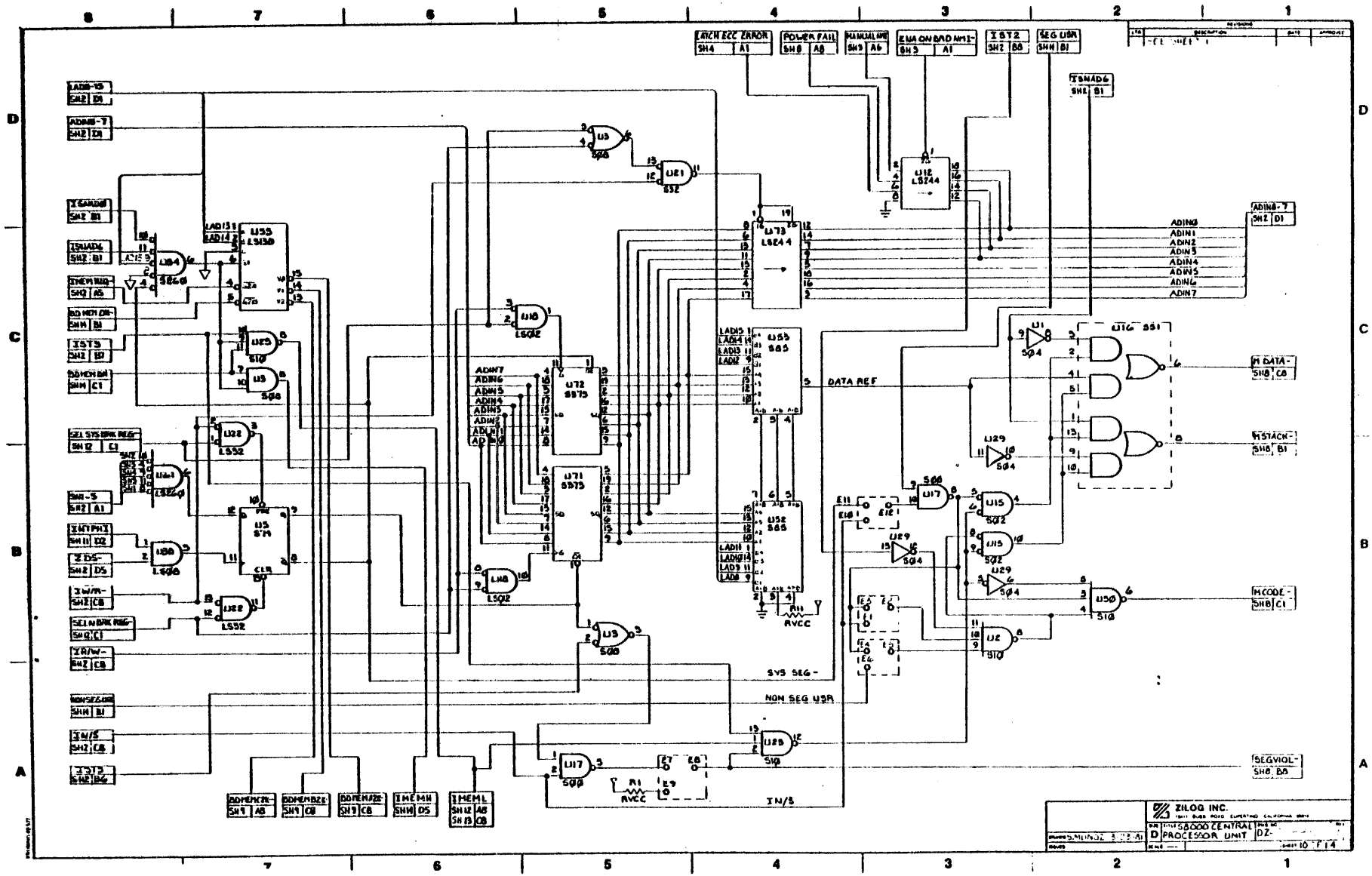
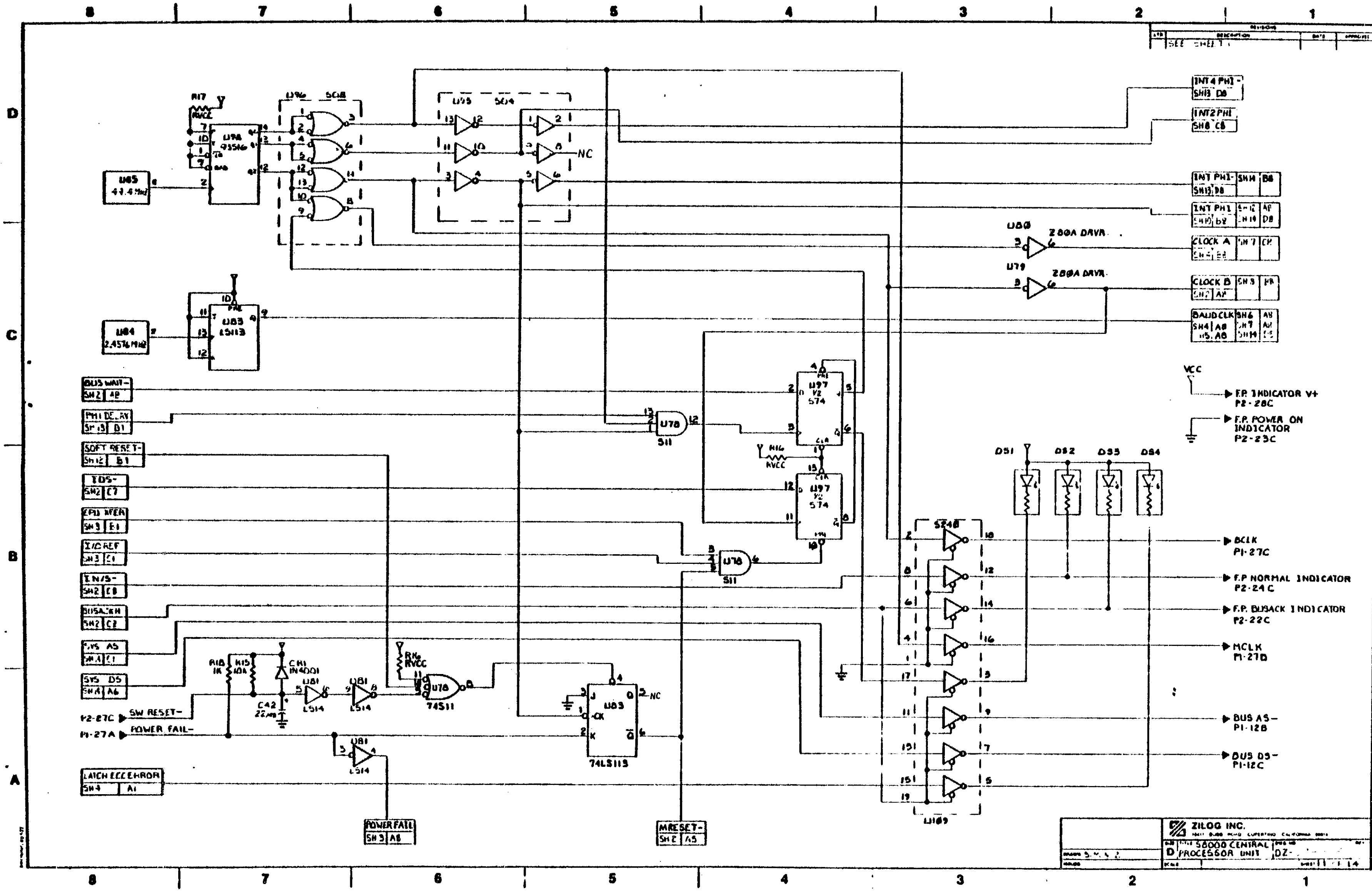
8000 CENTRAL PROCESSOR UNIT
DZ
7 OF 14

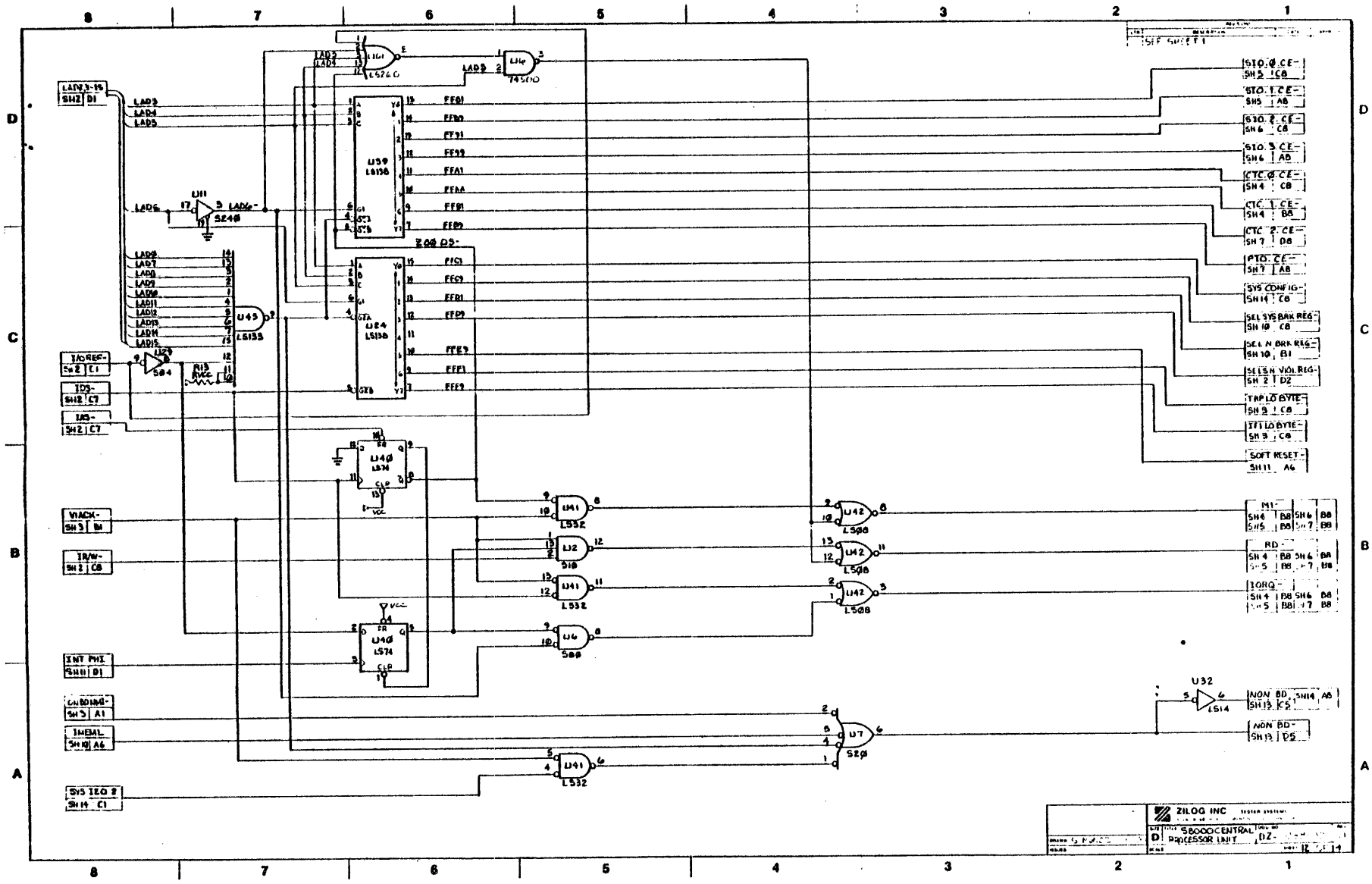

U86
Z8010A
STACK MMU
U87
Z8010A
DATA MMU
U88
Z8010A
CODE MMU
RESET
CLK
DMA SYNC
GND
U32
U35
7407
R14
4.1K
R10
4.7K
ZILOG INC.
8000 CENTRAL
PROCESSOR UNIT
8 OF 14

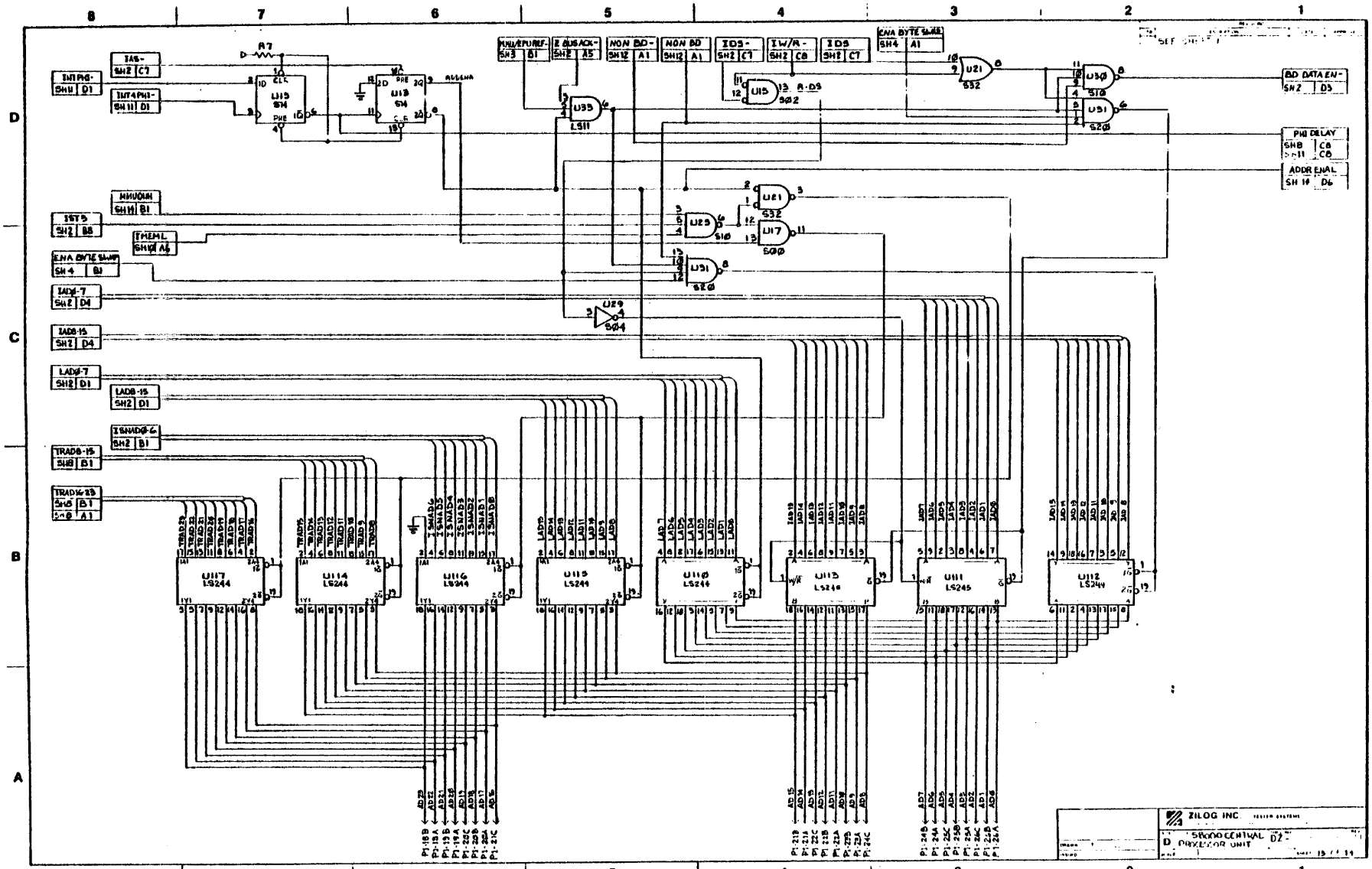

ZILOG INC.
Z8000 CENTRAL PROCESSOR UNIT
DZ-
U74 2732 MON1
U75 2732 MON2
U76 2732 MON3
U77 2732 MON4
U57 2114
U58 2114
U59 2114
U60 2114
U56 LS32
U56 LS32
U27 LS32
U54 LS27
U56 LS32
U56 LS32
U54 LS27
U61 LS14
TP9
MEMCSLO-
MEMCSHI-

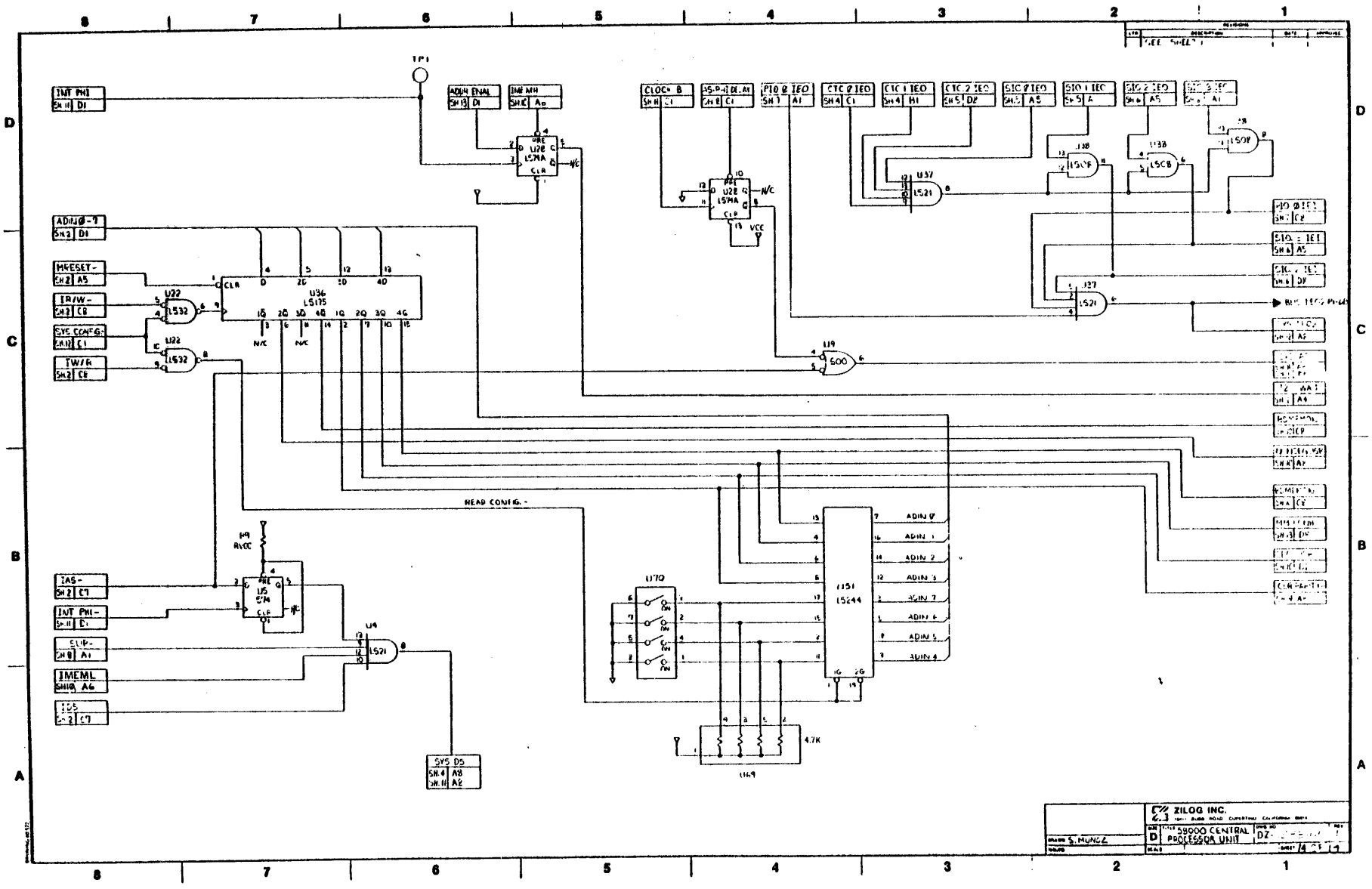

LATCH ECC ERROR
POWER FAIL
MANUAL INT
EMA ON BAD MAP
IST2
SEG USR
ISMAD6
ADIN0-7
ADIN0
ADIN1
ADIN2
ADIN3
ADIN4
ADIN5
ADIN6
ADIN7
DATA REF
M DATA-
MSTACK-
MCODE-
SEGVIOL-
SYS SEG-
NON SEG USR
IN/S
RVCC
ZILOG INC.
58000 CENTRAL
PROCESSOR UNIT



U85 44.4 MHz
U84 2.4576 MHz
BUS WAIT- SH2 A8
PHI DELAY SH13 B1
SOFT RESET- SH12 B1
EDS- SH2 C7
EPU WFER SH3 E1
I/O REF SH3 C1
EN/S- SH2 C8
BUSACKH SH2 C2
SYS AS SH4 C1
SYS DS SH4 A6
P2-27C SW RESET-
P1-27A POWER FAIL-
LATCH ECC ERROR SH4 A1
POWER FAIL SH3 A6
MRESET- SH2 A5
74LS113
74S11
INT4 PHI- SH13 D8
INT2 PHI SH8 C8
INT PHI- SH14 B8 SH15 D8
INT PHI SH16 D8
Z80A DRVR
CLOCK A
CLOCK B
BAUDCLK
VCC
F.P. INDICATOR V+ P2-28C
F.P. POWER ON INDICATOR P2-23C
DS1 DS2 DS3 DS4
BCLK P1-27C
F.P. NORMAL INDICATOR P2-24C
F.P. BUSACK INDICATOR P2-22C
MCLK P1-27B
BUS AS- P1-12B
BUS DS- P1-12C
ZILOG INC.
S8000 CENTRAL PROCESSOR UNIT


ZILOG INC
SBOOOCENTRAL
PROCESSOR UNIT
D
DZ-


ZILOG INC
5000 CENTRAL
D PROCESSOR UNIT


ZILOG INC.
Z-3
SIZE D
TITLE Z8000 CENTRAL PROCESSOR UNIT
DWG NO D2
DRAWN S. MUNOZ
SHEET 14 OF 14
INT PHI
ADIN ENAL
IME MH
CLOCK B
PIO Ø IEO
CTC Ø IEO
CTC 1 IEO
CTC 2 IEO
SIO Ø IEO
SIO 1 IEO
SIO 2 IEO
ADIN Ø-7
MRESET-
IR/W-
SYS CONFG-
TWFR
U36 LS175
U22 LS32
U23 LS32
U37 LS21
U38 LS08
U38 LS08
U38 LS08
U27 LS21
U19 S00
HEAD CONFIG.
R9 RVCC
U5 LS74
U4 LS21
IAS-
INT PHI-
SLIP-
IMEML
U170
U151 LS244
ADIN Ø
ADIN 1
ADIN 2
ADIN 3
ADIN 7
ADIN 6
ADIN 5
ADIN 4
4.7K
U169
SYS DS

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Printed in USA